

## PART A user guide

### 1. INTRODUCTION

#### 1.1 General

The Rodime RO 200 series of 5¼ inches (130mm) Winchester disk drives provides fast access data storage for use with small business computers, terminals and microprocessor based systems. There are four models in the series, RO 201 RO 202, RO 203 and RO 204 containing 1, 2, 3 and 4 magnetic disks respectively and ranging in total data storage from 6 to 27 Megabytes. The drive outline is shown in figure 1.

The drive is a microprocessor based device which receives and transmits MFM (modified frequency modulation) data, seeking the appropriate track in response to step commands across the disk control interface. The drive is soft sectored and is connected to the host system via a disk controller which is responsible for formatting, MFM encode and decode to NRZ, block address decode, CRC generation and verification and so on. Typical format schemes with 256 data bytes per sector and 32 sectors per track can realise an efficiency of about 80% giving formatted capacities up to about 20.97 MB.

Dimensions, mounting details and voltage requirements (DC voltage only) are the same as standard 5¼ inches floppy disk drives. The microprocessor is responsible for the control of the stepper motor used for head positioning. Fast seek times are achieved by means of programmed velocity profiles and microstepped damping routines. Automatic thermal compensation has been designed into the head positioning mechanism. A brake is provided as standard for the main DC disk motor and this permits shipment of the Rodime drive in a terminal or system provided it has been mounted in accordance with the correct procedure (see section 2). A further solenoid brake for the actuator can be supplied as an optional extra. The Microprocessor also monitors certain fault conditions in the drive and should one occur, flashes the

corresponding fault code on a red LED indicator on the front panel.

A significant feature of the RO 200 series is that boards are interchangeable without the use of oscilloscopes or other setting up equipment. This is made possible by the fact that there are no select-on-test components and no adjustments on the boards whatsoever. This, of course, in addition gives added reliability which is further emphasised by the fact that there are no mechanical adjustments.

Several engineering features are subject to patent application and these are listed in Appendix 1.

Full specifications of the RO 200 series disk drive are given in two documents:-

- PRO-0020 (Product specification)
- INT-0021 (Interface specification)

A summary of the important performance parameters is given below:-

#### Product Specifications

Models: RO 201, 202, 203, 204,

Disks : 1, 2, 3, 4

Heads : 2, 4, 6, 8

Unformatted capacity (M bytes) : 6.67, 13.33, 20.00, 26.67

#### Formatted capacity (typical)

Per drive (M bytes) : 5.24, 10.49, 15.73, 20.97

Per track (bytes) : 8192

Per sector (bytes) : 256

Sectors per track : 32

Cylinders : 320

Transfer rate (M bits/s) : 5

#### Seek times (ms) (including settling)

Track to track : 18

Average : 90

Maximum : 215

#### 1.2 Specifications

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Average latency (ms)	: 8.3
Flux reversals per inch (max)	: 8900
Tracks per inch	: 356
Rotational speed (r.p.m.)	: 3600
Power requirements (DC only)	: 5V (±5%) at 0.65A typical
(See para 2.5)	: 12V (±10%) at 2A typical (4A motor start)
Dimensions (inches)	: 8.00 x 5.75 x 3.25
Operating environment	: 10° C to 50° C 10%RH to 85%RH (non-condensing)
Vibration	
Operating	: .006 inch displ., 5-60 Hz 1g pk accln., 60-500 Hz
Non-operating	: .040 inch displ., 5-30 Hz 2g pk accln., 30-500 Hz
Shock	
Operating and non-operating (without transit lock)	: 3g pk, less than 10ms, max 2 per second.
Non-operating (with transit lock)	: 30g pk, less than 20 ms, max 1 per 10 second
Interface	: ST506 variant of SA1000 (see section 1.3 and 1.4)

**1.3 Connectors** The RO 200 drive interfaces to host systems via a variant of the SA 1000 interface which is becoming a de facto standard for 5¼ inch Winchester disk drives. There are separate connectors for data (in MFM code); for control lines and for DC power. The connector positions are shown in Figure 1 and the connectors themselves are defined in Figures 2, 3 and 4. The corresponding control, power and data interfaces are given in Figures 5 and 6. A chassis ground tab is also provided. The convention for control is that a TTL logical zero is true and a

TTL logical one is false. Up to four drives may be connected to a host system and each drive is provided with a four-pole switch for selection. The control lines may be daisy-chained but the data lines must be radially (individually) connected to the host (see section 2).

Control signals for the drive are provided via a 34 pin edge connector (P1/J1). The pins are numbered 1 through 34 with the even pins located on the solder side of the board. Pin 2 is located on the end of the board connector closest to the DC power connector and is labelled. A key slot is provided between pins 4 and 6. The recommended mating connector is AMP ribbon connector A/N 88373-3.

Radial connection of read/write data signals is provided via a 20 pin edge connector (P2/J2). The pins are numbered 1 through 20 with the even pins located on the solder side of the board. The recommended mating connector is AMP ribbon connector A/N 88373-6.

DC power is provided via a 4 pin AMP Mate-N-Lok connector (P3/J3) P/N 350211-1 mounted via the component side of the board. The recommended mating connector is AMP P/N 1-480424-0 utilising AMP pins P/N 350078-4.

A ground connection is provided via a "Faston" connector AMP P/N 61664-1 located on a metal stand-off on the chassis between the power and control signal connectors. However, the DC and chassis grounds are common on the drive and the use of the "Faston" connector is not essential. Wiring should be in accordance with Figure 5. The frame ground of the host system should be properly earthed.

This section is intended to give some guidance on the technical capabilities of the main 5¼ inch Winchester Disk Controllers on the market at present. It is not intended to be a complete list or a definitive specification. Further information is available from the Rodime Marketing Department or from the Controller Manufacturers themselves.

**1.4 Controllers**

1.4 CONTROLLERS  
 SET 4 OF

- 14) Integrated Solutions : 1350 Dell Avenue No 201, Campbell, California 95008, (408) 374 2441.
- 15) Cameo Electronics Inc. : 162 Clementine Street, Anaheim, California 92802, (714) 535 1682.
- 16) General Robotics Corporation : 57, North Main Street, Hartford, Wisconsin 53027, (414) 673 6800.

As a general rule all controllers which will operate with the RO 100 series will also operate with the RO 200 series. However not all controllers will be able to address the full 320 cylinders on the RO 200.

The drive may be operated in either a direct or buffered step mode. In the direct mode, the step rate should not exceed 3.1 ms per step. A slower rate up to 8ms per step can be accommodated by the cutting of link A on the master electronics board (see Figure 23). In the buffered mode the rate must lie in the range 10 us to 200 us. The access times quoted in paragraph 1.2 refer to the buffered mode. The drive will not operate with a variable step rate exceeding the above limits.

**1.5 Illegal Address Map** Each drive is accompanied by a map indicating addresses of sectors which should not be used. This map (label) is fixed to the base casting wall. These illegal sectors have been identified during unit test in the factory and contain a repeatable disk defect, greater than one bit in length. No such illegal address will exist in cylinders 0, 1 and 2,

An illegal address is specified by cylinder, head and sector. It should be noted that the format used for this purpose is 33 sectors of 256 bytes each. The maximum number of illegal addresses is:-

Model Number	201	202	203	204
Max number of illegal addresses	2	4	6	8

The stepper motor shipping lock is a label fixed to the top cover of the drive and covering a plastic pulley on the stepper motor shaft, thus preventing movement of the read/write heads across the disk surfaces.

**This label must be removed** prior to power-on.

**Warning:** Once the label is removed the stepper motor shaft should never be rotated by hand since this could lead to head/disk damage.

**Note:** This label is not present on units which are fitted with the automatic stepper motor lock. This lock also releases on application of 12V.

The drive can operate with step rates in the range 10 us to 8 ms. However, this range is broken into two bands and either band can be selected by the user by either leaving or removing Link A on the master electronics board. (A full discussion of the step rate is given in section 9.1).

2.2.1. Link A in : step rate 10 us to 3.1 ms

2.2.2. Link A out : step rate 3.1 ms to 8.0 ms.

All drives are supplied with Link A in. If Link A is removed the drive will still operate for step rates in the range of 2.2.1 but will not use the fast seek velocity ramp routine even when appropriate.

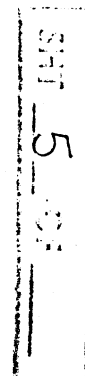
Side brackets with tapped holes are provided with each drive and permit base or side mounting, see Figure 7. These brackets are fixed to the drive chassis via shock-absorbing grommets. The drive may be oriented in any axis. When installing into an enclosure at least 0.1 inch clearance must be maintained around the entire drive to allow vibration isolation and to prevent obstruction of the breather filter and the creation of ground loops.

Up to four drives may be connected to one host in a "daisy-chain" fashion. A 4-pole drive select switch is fixed to each drive and is accessible via a port in the side bracket. To identify a drive as number 1, close the first pole of this switch

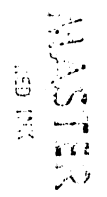
## 2. INSTALLATION

### 2.1 Shipping lock

### 2.2 Step rate select



### 2.3 Mounting



### 2.4 Multiple drive configuration

nearest the facia. Similarly for drives 2, 3 and 4. Only one pole should be in the closed position. All "daisy-chained" drives should have the line terminator pack removed except for the last drive in the chain. All drives are supplied for single usage, that is, pole 1 is closed and the terminator pack is present. (See figure 1).

Note that, in the multiple drive configuration all data interface lines are radially connected to the host. Figure 8 shows a four drive configuration.

## 2.5 Power requirements The drive requires DC voltages only.

VOLTAGE	CURRENT		
	Typ	Max	Peak During Power-up
+5V $\pm$ 5%	0.65A	0.75A	
+12V $\pm$ 10%	2.0A	2.4A	4A

No damage will result if power is applied or removed in any order. However, to avoid tripping the fault detection circuitry two conditions must be met:

- 2.5.1. 5V risetime must not exceed 1 second.
- 2.5.2. 12V must follow the 5V within 5 seconds if the 5V is applied first.
- 2.5.3. When checking the power supplies, the following loads should be used:

For the 12V supply, the power-up current may be measured using a standard load of 3 ohms in series with 1 mH and the operating current may be measured using 5 ohms in series

with 1 mH. With a 7 ohm resistive load on the 5V supply and the above loads on the 12V supply, noise and ripple should not exceed 100 mV peak to peak up to 500 Hz and 50 mV peak to peak from 500 Hz to 5 MHz.

In operation, the maximum rate of change of the 12V load due to the disk drive is 8A/ms.

Two red LED's fixed to the master electronics board are visible through the facia when they are illuminated.

## 2.6 Indicators

2.6.1. The "Power-On" LED is on when the drive is READY with no error condition present. It is also used to indicate fault conditions in the drive.

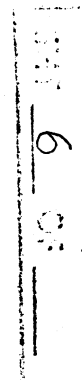
2.6.2. The "Select" LED is on when the drive is selected by the host provided the "Power-On" LED is on.

The "Power-On" LED is positioned closest to the centre of the facia. Note that this LED will not come on if the condition 2.5.1, 5V risetime, is not met since the microprocessor will not receive an initial reset.

The "Power-On" LED is used to flash error messages should certain fault conditions arise on the drive. A four bit binary code is used (long flash = logical 1, short flash = logical 0) with the most significant bit occurring first:

e.g. short, short, long, short = 2 (0010)

- Fault Code 1 (0001)** : No index track data burst.
- Fault Code 2 (0010)** : No Flag  $\emptyset\emptyset$
- Fault Code 3 (0011)** : Motor speed outside  $\pm$ 1% tolerance at end of power-up sequence.



## 3. FAULT FINDING

### 3.1 Front panel fault codes

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- Fault Code 4 (0100)** : Motor speed outside  $\pm 10\%$  tolerance in normal operation.
- Fault Code 5 (0101)** : Flag  $\emptyset\emptyset$  stays TRUE.
- Fault Code 6 (0110)** : STEP received while WRITE GATE is TRUE.
- Fault Code 7 (0111)** : WRITE FAULT.
- Fault Code 8 (1000)** : Not used.
- Fault Code 9 (1001)** : Microprocessor self-test fail.
- Fault Code 10 (1010)** : No index.
- Fault Code 11 (1011)** : Motor not up to speed.

Fault codes 1, 2, 3, 5, 9, 10 and 11 are monitored during the initial power-up sequence of the drive. The remaining codes, namely 4, 6 and 7 are constantly monitored during normal operation. All fault codes are latched by the processor and the drive must be restarted to clear. Codes 3, 4, 10 and 11 generate an interface WRITE FAULT as do those fault conditions leading to code 7.

### 3.2 Fault codes at power-up

From power-on to drive READY the microprocessor performs a number of checks and calibrations on the drive. Should any of these checks fail the drive will not come READY and the microprocessor will flash the appropriate fault code on the front panel. The power-up routine is shown in Figure 19.

**3.2.1. Codes 9, 10, 11.** The first check is a microprocessor self-test. A check sum is performed on all the code bytes and failure results in the display of fault code 9. Following the self-test, the microprocessor checks for an INDEX pulse (Hall sensor output) from the DC motor. If this does not occur during a period of 8 seconds, then fault code 10 is displayed. Since this condition is likely to be the result of the DC motor not starting, the microprocessor attempts to reduce head/disk static friction during the period of 8 seconds by moving the positioner

Note that a WRITE FAULT condition removes power from the DC motor by means of a relay thus preventing thermal damage.

The DC motor speed is then checked to within  $\pm 1\%$  of 3600 rpm. Each check takes one motor revolution and during this time the power-on LED is flashed at intervals of approximately 0.5 second. If the processor does not see 4 consecutive speed samples correct to  $\pm 1\%$  within 25 seconds it will display fault code 11.

**3.2.2. Codes 5, 2.** When the speed check is successfully completed, WRITE FAULT interrupts are enabled. The microprocessor then begins the recalibration of the actuator to track  $\emptyset\emptyset$ . The exact routine is shown in Figure 20. Two possible fault codes may occur. If flag  $\emptyset\emptyset$  does not go false within 25 steps towards the centre of the disk, fault code 5 will be displayed. After going false, if flag  $\emptyset\emptyset$  cannot then be set true within 512 steps in the out direction, fault code 2 is displayed.

**3.2.3. Codes 1, 3.** After calibrating the actuator to track  $\emptyset\emptyset$ , the processor initiates the routine for selecting the correct INDEX pulse (see section 6.6 for an explanation of INDEX). The actuator is moved to track -2 to find the index data burst on head  $\emptyset$  and so select the corresponding Hall sensor phase, thus establishing INDEX. Failure to complete this operation, which involves checking for the data burst on track -3 if it cannot be located in track -2, results in fault code 1 provided link B is present and is ignored if link B is cut. The actuator is then re-positioned on track  $\emptyset\emptyset$  and a final check made on the DC motor speed, again to  $\pm 1\%$ . Should this fail, fault code 3 is displayed.

At the successful completion of the power-up routine, READY and TRACK  $\emptyset\emptyset$  are both set true and the head selects are enabled.

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3.3 Fault codes during operation During normal operation of the drive, fault codes 4, 6 and 7 may be displayed.

3.3.1. Codes 4, 6. While the processor is waiting for a step pulse from the interface it continuously monitors the DC motor speed. Should the speed vary from nominal by more than +10% or -5%, fault code 4 will be displayed. The processor will not allow a step pulse to be received while WRITE GATE is true. This is considered to be a catastrophic controller fault. The drive returns WRITE FAULT status and displays fault code 6.

3.3.2. Code 7: WRITE FAULT. On receipt of a WRITE FAULT interrupt from the drive's hardware detection circuitry the processor latches this condition, delays for 2 seconds and samples the hardware input to check if the WRITE FAULT condition still exists. If it does, fault code 7 is displayed. If not, the processor enters the power-up routine thus setting the actuator to track 00. See Figure 21.

In the above sense, fault code 7 represents a static WRITE FAULT status. There are ten fault conditions which cause WRITE FAULT to be true. One is defined above in 3.3.1. Three are related to read/write heads, namely

- write current in a head when WRITE GATE is false
- no write current in any head when WRITE GATE and DRIVE SELECTED are both true
- more than one head selected

Two relate to the DC supply, namely

- 12V supply lower than about 10.3
- 5V supply lower than about 4.5

The remaining four are abnormal motor conditions as detailed by fault codes 3, 4, 10 and 11.

In practice, it is likely that the vast majority of WRITE FAULT conditions are caused by power supply transients. Thus, the 2 second delay and re-check allows a fast transient to be recognised but the condition is not latched if the re-check is successful. The controller will receive TRACK 00 and READY status and can repeat the command which had to be interrupted.

A table showing likely causes of the fault codes is given below. The simplest action to take is that of replacing either the master board or the motor speed board and verifying if the fault code persists. However, a set of diagnostic routines is presented which determine more accurately the cause of each fault code. A voltmeter or oscilloscope and the "TRACKER" exerciser (see section 3.5) are needed for this investigation. The causes of fault conditions other than those given by the fault codes may be more difficult to trace. In practice, the most likely sources of trouble are (a) power supplies not meeting specification and (b) step rates outside the drive constraints (section 9.1). This presumes that the host controller meets the requirements of the Rodime interface specification INT-0021.

In any event, it should be verified that the shipping label is removed, the connectors are clean and properly attached, the interface terminator is present or absent according to the configuration, link A is removed for pulse rates in range 3.1 to 8.0 ms, the drive chassis is clear of any system network, the DC power lines are short twisted pairs and data and control cables are preferably shielded and do not run close to high current switching circuits.

3.4.1. For each fault code a possible cause is indicated by a letter. This is used in the Diagnostics Table for identification.

### 3.4 Fault diagnosis

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Fault Table

Fault Code	Possible Causes	Action
1	<p>A: Faulty flag <math>\emptyset\emptyset</math> position</p> <p>B: Fault in data burst detection circuitry</p> <p>C: Fault in head <math>\emptyset</math> or pre-amp board</p> <p>D: Data burst erased</p>	<p>Contact service organisation</p> <p>Replace master board</p> <p>Contact service organisation or replace pre-amp board</p> <p>Rewrite with "TRACKER"</p>
2,5	<p>E: Transit lock label not removed/faulty stepper lock option (if fitted)</p> <p>F: Connector fault between motor speed board and stepper motor/flag <math>\emptyset\emptyset</math> assembly</p> <p>G: Short circuit between motor speed board and casting</p> <p>H: Faulty flag <math>\emptyset\emptyset</math> transducer</p> <p>J: Fault in stepper motor control circuitry</p> <p>K: Fault in stepper motor control circuitry</p> <p>L: Faulty stepper motor</p> <p>M: Defective positioner assembly</p>	<p>Remove label/check stepper lock solenoid</p> <p>Check connector and/or replace motor speed board</p> <p>Reassemble board</p> <p>Contact service organisation</p> <p>Replace master board</p> <p>Replace motor speed board</p> <p>Contact service organisation</p> <p>Contact service organisation</p>

Fault Code	Possible Causes	Action
3,4,10,11	<p>N: Brake failure</p> <p>P: No 12V supply</p> <p>Q: Faulty DC motor/Hall element</p> <p>R: Faulty motor speed board</p>	<p>Replace</p> <p>Check supply/connector</p> <p>Contact service organisation</p> <p>Replace</p>
6	<p>S: Controller/Interface fault</p> <p>T: Faulty master board</p>	<p>Check controller/connector</p> <p>Replace</p>
7	<p>U: Faulty master board</p> <p>V: Faulty pre-amp board</p> <p>W: 5V and/or 12V too low</p>	<p>Replace</p> <p>Replace</p> <p>Check supply</p>
9	<p>X: Faulty micro-processor</p>	<p>Replace master board</p>

3.4.2 A numbered set of checks is given for each fault code displayed on the front panel. The action after each test is indicated by a number or a letter. The number refers to another check, normally the next, shown for that fault code in this table. The letter refers to the determined cause as given in the previous table.

Fault Code	Procedure	Test is faulty?	
		Yes	No
1	1. Cut link B to let drive become ready.		2

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Fault Code	Procedure	Test is faulty?	
		Yes	No
	2. Use "TRACKER" to check on IC11/11 that flag $\emptyset$ switches between tracks 2 and 4.	A	3
	3. Use "TRACKER" to re-write data bursts, replace link and retest.	4	D
	4. Replace master board, re-write data bursts and retest.	C	B
2,5	1. Check if transit lock label is removed./Check stepper lock Solenoid (if fitted).	E	2
	2. Remove connector J8 from motor speed board and check for 18 ohm between J8/1 and J8/4, J8/1 and J8/6, J8/2 and J8/3, J8/2 and J8/7.	3	4
	3. Check J8 crimp joints.	F	
	4. Check for diode between J8/8 and J8/5.	5	6
	5. Check J8 crimp joints	F	H
	6. Check beneath motor speed board for shorts to casting.	G	7
	7. Replace master board and retest.	8	J
	8. Replace motor speed board and retest.	M	K
3,4 10,11	1. Check brake operation.	2	3
	2. Check 12V supply.	P	N
	3. Change link on motor speed board to use spare Hall element.	3	Q

Fault Code	Procedure	Test is faulty?	
		Yes	No
	4. Replace motor speed board and retest.	Q	R
6	1. Check interface cables/controller.	S	T
7	1. Test 12V to be in range 10.8V to 13.2V. Test 5V to be in range 4.75V to 5.25V.	W	2
	2. Replace master board and retest.	V	U

Rodime has developed a hand-held exerciser, the "TRACKER" which simulates a host controller and allows the user to exercise any 5¼ inch Winchester disk drive which operates via the SA 1000/ST 506 interface. It is a useful tool for checking a drive which is believed defective or which has been repaired. The "TRACKER" comes complete with interface connectors for data and control and with a 5V supply connector. It basically comprises a keypad for parameter and instruction input and six LED's for response.

It will perform the following commands:

- Recalibrate.
- Seek track  $\emptyset$  to 1023.
- Select head  $\emptyset$  to 7.
- Continuous seek between two tracks.
- Key selectable step rate (30 us to 25 ms in 100 us increments).
- Seek demonstration routine (random, planet satellite).
- Write pattern select (1F, 2F, DB Hex).
- Write/erase for one revolution.

### 3.5 'TRACKER' exercise

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- Write/erase for one surface (head).
- Continuous write.
- Check index tracks -2 and -3.

This device would typically be used with an oscilloscope and allows actuator and head/media verification, for example.

It may be purchased direct from Rodime, and customers wishing to do so should contact the plant in Glenrothes or the appropriate Sales Office.

#### 4. REPAIR AND MAINTENANCE

There is no preventative maintenance and there are no adjustments on the drive. Field repair is restricted to brake and board replacement and selection of the spare Hall sensor. Repair to the module can only be effected by use of Rodime special tooling and Class 100 clean room conditions. **USERS ARE REMINDED THAT REMOVAL OF THE MODULE COVERS WILL RENDER WARRANTY VOID.**

##### 4.1 Tools

The tools required for field repair consist of:

- Supadriv screwdriver, number 1.
- Pozidriv screwdriver, number 2.
- Box spanner, 1/4 inch AF.
- Hex driver (Allen) 5/64 inch.
- .015 inch feeler gauge.
- "TRACKER" exerciser (Optional).

##### 4.2 Procedure

Access to the brake, pre-amplifier board and motor speed board is achieved firstly by removing the facia, then the master board and finally the side brackets.

##### 4.2.1 Master board replacement (time 5 minutes).

Using number 1 Supadriv, remove 4 screws holding facia and remove from drive. Using 5/64 inch Allen key remove the five (5) screws securing the board to the drive, and carefully lift the board free of the drive.

Disconnect the flat cable connector from the motor speed board.

Reassemble the replacement board in the reverse order ensuring that the pre-amp connector mates correctly with the pre-amp board, and the flat cable connector is correctly polarised.

**4.2.2 Brake replacement (time 10 minutes).** Remove the master board as described in 4.2.1 but do not disconnect the flat cable from the motor speed board. Disconnect the brake connector from the motor speed board.

Remove the two screws securing the brake to the casting using the number Pozidriv screwdriver, and remove brake.

Position the replacement brake and refit the screws loosely.

Place the .015 inch feeler gauge between the motor rotor and the brake pad and push the brake body such that the plunger fully depresses against its spring. Ensure that the centre line of the brake lines up with the motor centre and lock the screws. Reconnect the brake connector.

Reconnect the power connector ensuring correct polarisation.

Power up the drive with the master board lying alongside and check that the brake does not contact the motor rotor.

Power off and check that the stopping time is in the range 5 to 8 seconds.

Refit the master board as described in 4.2.1.

##### 4.2.3 Motor speed board replacement (time 10 minutes).

Remove the master board as described in 4.2.1.



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Remove the three screws and stand-off securing the mounting brackets to the casting and carefully remove the side brackets.

Disconnect the brake, DC motor and stepper motor from the motor speed board.

Unscrew the rear stand-off and remove the motor speed board.

If the spare Hall element is to be connected this is achieved by removing the link on the motor speed board and reconnecting it as shown in Figure 9.

Reassemble the motor speed board in the reverse order ensuring correct polarisation of connectors, check that the ground contact is correctly positioned between the motor speed board and the casting.

**4.2.4 Pre-amplifier board replacement (time 30 minutes).**

Remove the master board and side brackets as described in 4.2.1. and 4.2.3.

Desolder the flexible cables from the pre-amp board using solder wick, a fine tipped soldering bolt (maximum temperature 300°C). Care must be taken to minimise the heating of the flexible cables.

Remove the two (2) screws securing the pre-amplifier board to the casting and remove the pre-amp board.

Ensure that the replacement board has adequate solder "blobs" on the pads for flexible cable connection, and fit it to the casting using three (3) nylon washers behind each screw position.

Place the flexible cables on the pre-amplifier board in

alignment with the pads and reflow the solder using the fine tipped bolt.

Complete the reassembly as described in 4.2.3.

**4.2.5 Verification.** The Rodime hand-held "TRACKER" exerciser is a useful tool for verification of a repaired drive prior to final systems use. This device is more fully described in Section 3.5.

It should be emphasised that the following figures are recommendations only and that it will be up to each individual customer to decide upon the appropriate spares holding.

**4.3 Spares holding.**

Description	Part No.	Drives on site		
		1-99	100-250	> 250
Master board assembly	ASY 5062	1	2	5
Speed board assembly	ASY 5024	1	1	2
Pre-amp board assembly	ASY 5025	1	1	1
Failsafe brake assembly	ASY 2072	1	1	2

Other spare parts such as bracket/facia assemblies, terminator packs, ground tabs and consumable items such as warning labels are also available.

Spare parts for use as a customer spares holding may be purchased directly from Rodime or from Rodime appointed distributors.

**4.4 Purchase of spares**

Spares may also be purchased on an exchange basis under which Rodime will supply a new or refurbished sub-assembly making a financial allowance on the returned unit.

Price lists may be obtained from Rodime, its sales offices or authorised distributors.

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**4.5 Repair services** Rodime operates a repair service under which drives will be repaired for a standard service charge.

Drives which are out of warranty when this service is required, should be packaged in the original shipping container and returned to Rodime or to the distributor from which the drive was purchased together with a full description of the fault condition.

If the original packaging has been mislaid, a suitable container may be purchased from Rodime or the distributor.

Rodime cannot assume any responsibility for damage incurred to the drive during the shipment and insurance is the responsibility of the customer.

Rodime will return the goods carriage collect and a charge will be made for any shipping container which Rodime may have to provide.

Further details of this service may be obtained from Rodime or its authorised distributors.

**4.6 Return of drives under warranty.** Rodime Terms and Conditions of Trade include a warranty for a period of 12 months from date of shipment. The procedure for return of drives under warranty is as follows:-

If the drive fails within the first five days of operation please immediately contact the Marketing Department at Rodime or the distributor from whom the drive was purchased.

In the event of other problems Rodime, or the appropriate distributor, should be informed in writing of the suspected defect. If the drive is required to be returned a Return Authorisation Number will be given

and the drive should be returned pre-paid. The same procedure as in 4.5 above applies.

If on examination the drive is proved defective under terms of the warranty, the drive will be repaired or replaced, at Rodime's sole discretion and returned to the customer at no charge. If the defect is found to be due to mis-handling or other causes, the drive will be treated as a standard repair and charged accordingly. If, on examination, no fault is found, the drive will be returned at the customer's expense. Rodime reserve the right to make a charge for testing and handling under these circumstances.

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## PART B product description

The important performance and reliability aspects of the RO 200 disk drive mechanical design may be summarised as follows:

- Up to four disks in "mini-floppy" size compatible unit.
- Designed for easy assembly of heads and disks.
- Minimum number of components to maximise reliability.
- Two chamber principle with heads/media in one and actuator mechanisms in the other.
- Low inertia positioner for reliability and fast access.
- Geometry designed to minimise head yaw.
- Drive components designed to compensate for thermal head/disk movement.
- DC brushless motor with ferrofluidic seal and integral ventilated hub.
- Breather filter positioned to equalise pressure across DC motor bearing.
- Air flow designed to locate drive components upstream from re-circulating filter and downstream from heads/media thereby creating an optimum purge cycle.

### 5. MECHANICAL DESIGN

#### 5.1 General

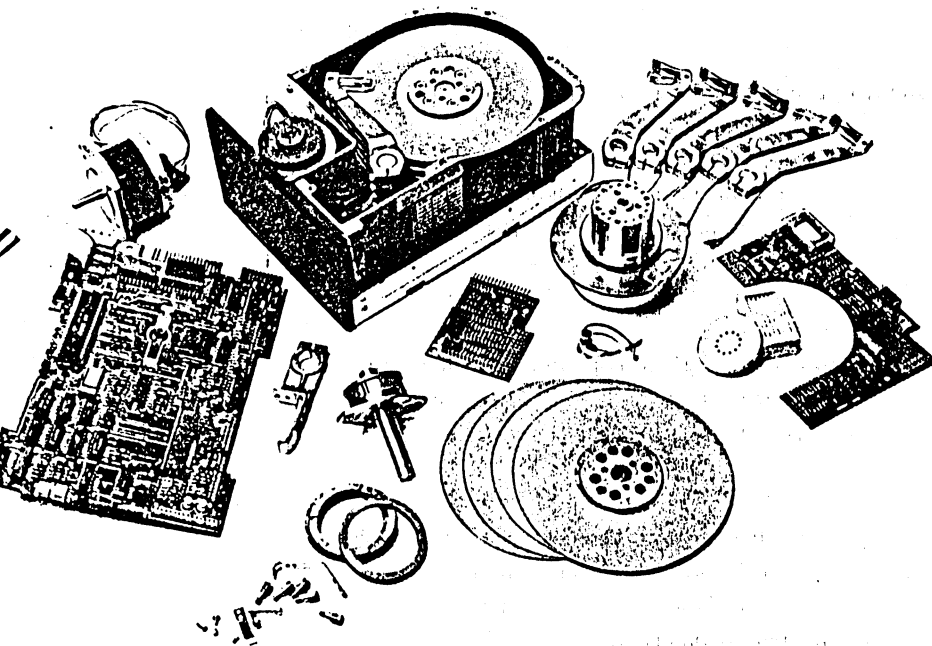
The positioning system consists of a stepper motor which drives a tensioned steel band via a pulley. The band in turn moves a drive arm which is attached to a shaft. The shaft rotates in a bearing system and moves the head arms across the disk. Simplicity of components ensures easy assembly and reduces failure risk.

The four phase stepper motor operates in the half-step mode under microprocessor control (0.9° per track).

5.2.1 Stepper Load. The positioner has low inertia to provide

#### 5.2 Rotary actuator

Component parts of RO200 series disk drive



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fast seek times (maximum velocity 1900 tracks per second) from the available stepper motor power.

**5.2.2 Yaw.** The geometry of the positioning system restricts head yaw to a range of only 8°. The distribution of this angle is chosen such that the ratio of yaw angle to linear disk speed is approximately the same at outermost and innermost tracks.

**5.2.3 Bearings.** The actuator system utilises two half-shielded deep groove ABEC 3 ball bearings arranged in a back-to-back configuration with a dimensional axial preload of 5 lbf for optimum stiffness.

**5.2.4 Band.** The drive band geometry is designed to give symmetry of movement and to minimise band radii and flexing angles. The band is etched from stainless steel with a typical tensile strength of 250K psi. There is a safety factor of approximately 40 between the breaking stress of the band and the dynamic peak tension.

End stops restrict over-travel should control be lost and will prevent read/write heads from either striking the disk hub or coming off the disk.

**5.2.5. Flag  $\emptyset\emptyset$ .** Track  $\emptyset\emptyset$  is defined from a combination of a particular stepper motor phase (one of eight) and a flag mounted on the drive arm. This flag is set up, using a special assembly fixture to switch on opto-interrupter (track  $\emptyset\emptyset$  transducer) mounted on the base casting. The flag is set to switch between tracks 3 and 4. Track  $\emptyset\emptyset$  requires the flag to be true (transducer interrupted) and the correct stepper phase to be selected. Note that the opto-interrupter and drive components are in the sealed lower chamber and hence protected from contamination and accidental handling damage.

## 5.3 Head/track positioning tolerances

The requirements of the positioning system are (a) that tracks do not touch and (b) that an acceptable signal to noise ratio is obtained when the same track is overwritten. Broadly speaking, the first condition determines the maximum track pitch error. In the case of the RO 200 drive it relates mainly to the static stepper motor accuracy. The second condition relates to the repeatability of the positioning system. Thus given a specification for the repeatability tolerance the required mean (static) step accuracy of the motor can be determined for a given track density.

With a minimum track pitch of 0.00275 inch and a read/write gap width of 0.0021 inch, a positioning accuracy of  $\pm 150$  micro inch would give a worse case 1F signal to 2F noise of better than 15:1.

The airflow generated by disk rotation causes air to flow from the disk chamber through an aperture into the drive chamber and to return via a recirculating filter. This flow system ensures equalisation of temperature during warm up by moving air over all components. By positioning the recirculating filter upstream from the heads and the drive components downstream from the heads optimum purge conditions can be achieved. The disk hub is designed to ventilate the inter disk spaces from both ends thus ensuring adequate air flow across the disks.

The breather filter situated on the top cover is positioned on the disk rotational axis. This compensates for atmospheric changes and maintains a pressure balance across the DC motor bearings reducing the risk of ingress of contaminants. The breather filter is 99.97% efficient to 0.5  $\mu$ m particles and the time taken to equalise pressure is less than one second.

The recirculating filter is positioned in the drive chamber

## 5.4 Airflow and filters

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upstream from the disk chamber. This ensures that any particles generated by moving parts are retained by the filter and prevented from contaminating the disk chamber. The recirculating filter is 99% efficient to 0.5  $\mu\text{m}$  particles giving a purge time of 12 seconds.

## 5.5 Thermal compensation

The positioning mechanism is designed to compensate automatically for head to track mispositioning caused by thermal effects. The thermal loop in the disk chamber (motor hub, disk, head flexure, head arm, shaft, bearings, bearing housing and base casting) causes the read/write head to move outwards from track centre as temperature rises. By careful design of geometry and materials, the thermal loop in the drive chamber (stepper motor, band, drive arm, shaft, bearings, bearing housing and base casting) causes a counter rotation of the actuator thereby maintaining the heads on track centre. See Figure 12.

The resulting misposition is about 1  $\mu\text{in}$  per  $1^\circ\text{C}$  temperature change. It is estimated that this would be about 8-10  $\mu\text{in}$  per  $^\circ\text{C}$  in the absence of this compensation mechanism.

## 5.6 D.C. motor and brake

The motor is a brushless 2-phase external rotor DC motor with integral hub and commutation effected by Hall sensor. A spare Hall sensor is provided in each motor. The motor uses preloaded ABEC 7 bearings and is balanced in two planes to better than 0.25 gm cm. A ferrofluidic seal is fitted above the top bearing. The disk hub is grounded to the master electronics board via the motor shaft and a button contact.

The brake is a plunger solenoid designed to stop the motor in 5 seconds and to provide a restraining torque during handling. The brake pulls in at 12V and holds off at 5V.

The master electronics board layout and schematics are given in Figures 23 and 26 (a) — (d). This board provides the following circuit functions:

- data read channel.
- data write channel.
- head selection.
- interface circuitry.
- fault detection.
- stepper motor control.

In addition the master board provides DC power distribution and control to the motor speed control board and the pre-amplifier board. The interconnections between the various boards are illustrated in Figure 13.

Read data from the pre-amplifier board is received differentially on the lines RD+ and RD-. The 592 video amplifier, IC1, amplifies the readback signal by a factor of 33. Components R7, R8, C6, C7, L1, L2, C53, L5, L6 form a fifth order low pass Butterworth filter with a characteristic frequency of 4.5 MHz. The second 592, IC2, is configured as a differentiator and transforms the peaks of the readback pulses to zero crossings which are detected by the zero-crossing detector, IC3.

The output signal on IC3 pin 1 is high when the input signal is positive and low when negative. IC3 pin 10 provides a negative pulse of duration 100 ns for every zero-crossing on the input signal. These two signals are used as the data and clock inputs to the D-type flip-flop, IC4. This connection provides a time domain filter which will reject zero-crossings occurring at less than 100 ns intervals.

The exclusive-or gate IC5 generates a pulse for every edge output from IC4 pin 5 using the delay generated by the series connection through the elements of IC6 and IC7.

## 6. MASTER ELECTRONICS BOARD

### 6.1 Data read channel

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The signals  $\pm$  MFM READ DATA are transmitted to the host for decode.

Figure 14 illustrates a typical readback signal at various stages in the read channel. Figure 15 shows read/write data timings.

## 6.2 Data write channel

Write data from the host is received on the lines  $\pm$  MFM WRITE DATA. This signal is divided by 2 using IC4, and used to drive the write current switching transistors Q1 and Q2, via the open collector outputs of IC8 pins 6 and 8.

Q3, D3 and R29 comprise a write current source which supplies current to a head through either Q1 or Q2. The signals WD+ and WD- carry the current to the head, through a diode matrix on the pre-amplifier board.

The signal WRITE GATE (WTG) from the host enables the current source and drive signals to Q1 and Q2. The signal REDUCED WRITE CURRENT (RWC) from the host enables the current sink formed by Q5, D2 and R31. When enabled, current is diverted from the head during a write and hence the effective write current is reduced. This signal should be set true when writing to cylinders 132 through 319. Pre-compensation (early and late) of write data is recommended and a preferred scheme is shown in Appendix 2. The compensation applies to the centre bit of each five bit pattern. The value of compensation should be 10 to 12 ns and it is recommended that it be applied to all cylinders.

## 6.3 Head selection

Up to eight read/write heads may be selected using the three bit code placed on the lines HEAD SELECT 0, HEAD SELECT 1 and HEAD SELECT 2. This 3 bit code is decoded using IC10 and a corresponding output line, HD0 to HD7, is held low. These signals are connected directly to the head centre taps through the pre-amplifier board. A diode matrix on the pre-amplifier board ensures that all other heads are

isolated from the select head. The 680 ohm pull-up resistors provide a reverse bias for the diodes on the unselected heads.

All input lines on the control interface are terminated by a 220 ohm resistor to +5V, and a 330 ohm resistor to logic ground. The input line receivers and output line drivers are 74LS244 buffers with tri-state outputs.

## 6.4 Interface circuitry

**6.4.1. Input lines.** WRITE GATE, REDUCED WRITE CURRENT and HEAD SELECT 0, 1, 2, have been already mentioned and are hard wired to their appropriate circuits on the master electronics boards. DIRECTION IN and STEP are connected to input pins on the 8048 microprocessor, since the control of the stepper motor is achieved totally through firmware.

**6.4.2. Output lines.** SEEK COMPLETE, TRACK 00 and READY are generated by the 8048 microprocessor. INDEX is derived by dividing the output from a Hall sensor on the drive motor by 2, since two pulses occur per revolution of the motor. The width of the output pulse is set to approximately 200 us before transmission. WRITE FAULT is set true if any of the drive fault conditions occur, as described in section 3.3. DRIVE SELECTED is set true if the DRIVE SELECT signal from the host corresponds with the drive select switch setting on P9, and if the drive is READY.

Two modes of fault detection are used in the drive. One is implemented in the microprocessor firmware and is described in section 3. The other, which is implemented in hardware, is described in this section. Four drive faults are detected using comparator based circuits.

**6.5.1. Multiple heads selected.** IC9 pin 4 has a reference voltage of 4.9V established on it by R40 and R41. IC9 Pin 5 is connected to the common rail of the pull-up resistors for

## 6.5 Fault detection

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the head centre tap lines. If one head is selected, pin 5 will be biased at 6.0V and the output, pin 2, will be high. If two or more heads are selected simultaneously, then pin 5 will be biased at 4.0V, or less, and the output will be low, signalling a WRITE FAULT condition.

**6.5.2. Low + 12V rail.** IC9 pin 6 has a reference voltage of 5.1V established on it by D9. IC9 pin 7 is 5.1V below the +12V rail by virtue of D8. Hence, if the +12V rail is higher than 10.2V, then IC9 pin 1 will be high. If the +12V rail falls below 10.2V, then IC9 pin 1 will be low, signalling a WRITE FAULT condition.

**6.5.3. Low + 5V rail.** IC18 detects that the +5V rail falls below +4.0V, and IC18 pin 1 prevents the write current source from being turned on. In addition, the microprocessor reset capacitor, C31, will be discharged by this condition. This circuit was primarily intended to protect data from spurious writes during power up/down sequences.

**6.5.4. WRITE GATE true, no write current or vice versa.** The presence of write current is detected by D5, D6, R37 and IC9 pins 10, 11 and 13. IC9 pin 11 is biased at 0.7V using D7. If write current is present, IC9 pin 10 will be at 1.4V, since two diode forward voltage drops will be established by the pre-amplifier diode matrix. The output IC9 pin 13 will then be low. If no write current is present, IC9 pin 10 will be at 0V, and IC9 pin 13 will be high.

By gating these conditions with WRITE GATE through an exclusive - or using IC5, WRITE FAULT will be signalled if WRITE GATE is true and there is no write current, or if WRITE GATE is false and there is write current.

**6.6 Stepper motor circuitry** Stepper motor control is achieved totally by firmware in the 8048 microprocessor. See section 9.2. Eight lines from the microprocessor control the stepper motor drive circuits on the

master electronics board. Figure 16 illustrates the connection between the microprocessor, the drive circuits and the stepper motor via the motor speed control board.

The stepper motor has four phases A, B, C and D. The signals PHA, PHB, PHC and PHD control the stepper motor drive circuits. Each signal can switch on a phase driver, current being limited by the resistors R14 and R15. A phase driver consists of 74LS14 gate switching two ULN2003 Darlington elements in parallel.

The signals SCA, SCB, SCC and SCD switch on transistor elements in IC13 and IC14 and these short out their corresponding windings.

The PH signals switch the motor phases on in the correct sequence to step the motor at a rate and direction determined by the microprocessor. The SC signals short out inactive windings during settling to improve the damping characteristics of the motor. The timing for step pulses is shown in Figure 17.

INDEX is an interface signal used to mark a fixed reference point relative to the disk. The Rodime drive does not have a separate INDEX transducer but instead uses the output of the Hall sensor inside the DC motor. This sensor output is a square wave which has a 50% duty cycle and makes 4 transitions in one disk revolution. This is then divided by two and used to trigger a monostable which gives a 200 us pulse once per disk revolution.

This hardware scheme results in a non-unique INDEX that is one of two each 180° apart. Normally this would not be significant since INDEX should only be used during a drive format. However, some controllers require a unique INDEX for reading.

6.7 Index

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The following procedure is used to ensure the INDEX is always unique. A special data pattern is written by head Ø on one half of tracks -2 and -3 during drive manufacture. At power-up a comparison is made between the Hall sensor output and the data burst and a unique index is selected. If the data burst is not found on track -2 an automatic search is made for the same pattern on track -3. If the pattern is not found on track -3 the drive will display fault code 1. Since the uniqueness of the INDEX signal is only relevant to certain controllers provision has been made to ignore this fault code. Cutting Link B will cause the drive to ignore the loss of the data pattern. Section 9.2 gives details of features designed to protect track -2 from accidental overwrite.

**6.8 Links** There are two user definable links on the master board close to the microprocessor.

Link A. This link should be cut if the STEP rate is between 3.1 ms and 8 ms. See Figure 23.

Link B. This link is cut to circumvent the fault caused by the loss of the INDEX calibration tracks. See section 6.7.

**7. PRE-AMPLIFIER BOARD** The pre-amplifier board layout and schematic are given in Figures 24 and 27. This board provides three functions:-

- a low noise, high common mode rejection ratio first stage of amplification for the read channel.
- a means of selecting and isolating up to eight read/write heads.
- a means of physical connection for up to eight read/write heads.

**7.1 First stage amplifier** The first stage amplifier is a discrete, differential amplifier with a constant current sink in the emitter circuit, to provide

a high C.M.R.R. It is realised using an LM3046 five transistor array denoted IC1 in the schematic. The reference current for the constant current sink is generated by the transistor Q1 and the Zener diode D21. When writing, the reference current is turned off to improve the write/read recovery time of the read channel. The overall differential gain of the amplifier is nominally 18.

The diodes D1 through D16 form a diode matrix which can select or isolate up to eight heads. Each head is isolated by two diodes, which are reverse biased when the head is de-selected, and forward biased when selected. To select a head, the head centre tap connection (HSØ through HS7) is held at logic '0'.

Diodes D19 and D20 isolate the read channel when writing. Similarly, diodes D17 and D18 isolate the write channel when reading. Resistor R3 provides a means of damping for the recording heads during a write.

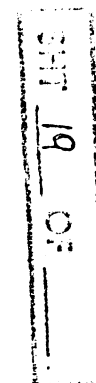
Signals designated P4 are those which are sent to, or received from the master electronics board. Signals designated P10 are the signals sent to and received from the recording heads via the flexible circuits.

The motor speed control board layout and schematic are given in Figures 25 and 28. This board provides the following circuit functions:-

- DC motor speed control.
- stepper motor R.F. suppression and current limiting.
- solenoid brake power supply.
- track zero transducer power supply and output termination.

Speed control of the drive motor is achieved using a phase-locked loop (P.L.L.) technique. The drive motor rotates at

**7.2 Head selection and isolation**



**7.3 External connections**

**8. MOTOR SPEED CONTROL BOARD**

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**8.1 Drive motor speed control**

3600 rev/min and generates two feedback pulses per revolution from an internal Hall effect IC. This results in a 120 Hz feedback signal which is phase-locked to a reference signal generated from the microprocessor crystal oscillator on the master electronics board. A speed variation of less than 0.1% is achieved.

The Address Latch Enable (A.L.E.) signal from the microprocessor is used as the reference. This signal (REF: CLK), frequency 400 KHz, is divided by 3336 using IC1 and IC2 to give a 120 Hz input to the phase/frequency detector IC3. The other input to IC3 is the feedback signal from the motor Hall sensor.

The output signal on IC3 pin 8 is a DC voltage proportional to the phase difference between the two input signals. R4, R18, C2 and IC4 form the electronic compensation network that ensures the stability of the control loop. The resultant signal on IC4 pin 7 drives the motor via the emitter followers Q1 and Q2, and the power amplifier Darlington transistors Q3 and Q4.

A two phase drive motor is used, and commutation between the two phases is accomplished using the Hall IC output. This signal, and its inverse, alternatively enables either Q3 or Q4, depending upon the phase of the commutation cycle.

The Hall sensor signal is also sent to the master electronics board, where it is divided by 2 and used as the drive INDEX signal. A spare Hall sensor output is provided, and in the event of output failure, the spare may be connected by wire link selection.

The capacitors C6, C7, C8 and C9 are connected between each of the stepper motor windings and 0V to provide suppression of any high frequency signals. The resistors

### 8.2 Stepper motor suppression and current limiting

R14 and R15 limit the current in any winding to 0.4A when active. A maximum of two windings can be active at any time.

Power is supplied to the solenoid brake initially from the +12V rail until it pulls in and the DC motor is up to speed. Thereafter, power is supplied from the +5V rail via diode D2 to reduce running power dissipation.

### 8.3 Brake

In addition to the above friction type of brake, a relay is used which provides dynamic braking by applying a short circuit across the motor windings when the drive is switched off.

The relay is de-energised by means of the FET Q7. This removes drive power from the motor preventing thermal damage under fault conditions.

The resistor R16 is a bias resistor for the LED in the opto-interrupter. A nominal forward current of 30 mA is supplied. The resistor R17 is a pull-up resistor for the photo-transistor which is connected in the open-collector output configuration.

### 8.4 Track $\emptyset\emptyset$ transducer

The microprocessor used on the drive is a member of the 8048 family of single-chip processors. Early production units use the 8748 EPROM version. The 8048 is used in the stand alone mode with no external memory and the 8048 in this mode has 1000 bytes of program memory, 64 bytes of RAM and 24 I/O lines. It is driven by a 6 MHz crystal which gives a 2.5  $\mu$ s instruction time.

## 9. MICROPROCESSOR

The microprocessor has three main functions:-

- stepper motor control.
- power-on auto-recalibration.
- status and fault monitor.

It also indirectly controls the DC drive motor since the 400 KHz output from the processor is used as a reference frequency for the P.L.L.

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The power-on sequence and fault monitor functions have been already described in section 3. The stepper motor control function is described below:

**9.1 Stepper motor control** Four interface signals are used to control the stepper motor.

**STEP.** This input signal is used in conjunction with DIRECTION IN to move the stepper motor. It is connected to the 8048 T1 pin. This is a special input to the microprocessor which is used to clock an internal 8 bit counter. This counter is reset prior to each seek. Once the first STEP pulse is received the processor issues stepper motor phase changes until the number of changes equals the value in the counter. At this point the seek is terminated and SEEK COMPLETE is set true after final step damping.

**DIRECTION IN.** This input is connected directly to an I/O pin of the processor. It defines the direction of motion of the stepper motor. Once the first STEP of any seek has been received the microprocessor samples this input and internally stores the result. The input is then ignored until the next seek.

**SEEK COMPLETE.** This status line is driven by a S-R flip-flop. STEP resets the flip-flop false. It is set true with an output from the microprocessor.

**TRACK 00** This status line is driven directly from the microprocessor. It will be set true when the read/write heads are positioned with correct stepper motor phase over track 00, false otherwise.

A four-phase stepper motor is used to control the read/write heads. The motor is half stepped in an eight step sequence. This step sequence and winding configuration are given in figure 18. Four outputs from the processor (PHA-PHD) are used to control switches for each winding. A further four outputs (SCA-SCD) are used to control a shorting

circuit which is connected across each winding. This is used to provide additional damping by shorting unused windings.

Further damping is obtained from a technique used during phase changes. Instead of instantaneously switching from one winding set to another the microprocessor digitally chops between phases with a variable mark to space ratio to effect a gradual change from one track to the next.

The microprocessor always buffers step pulses. Three factors govern the rate at which the stepper motor is pulsed. (1) The interface step rate, (2) a user definable link and (3) and length of seek. The following table gives the relationship between these variables:

Step Rate	Link A	Seek Length	Stepper rate
N (10us-8ms)	Not Present	1 to 319	Nms if N > 3ms 3ms if N < 3ms
N (700us-3.1ms)	Present	1 to 319	3ms
N (10us-200us)	Present	≤ 5	3ms
N (10us-200us)	Present	> 5	Ramped

All other combinations are undefined and may cause seek errors.

In the ramped mode of operation the microprocessor accelerates the stepper motor to a maximum step rate of 1900 steps/sec, then decelerates to the requested track. For all seeks the last phase change to the stepper motor is different to all others in order to achieve the correct settling characteristics. To do this, the microprocessor must be able to detect the last step of any desired seek. This imposes limitations on the maximum time between step pulses (3.1ms — link A present, 8 ms — link A not present).

The microprocessor eliminates stepper motor hysteresis automatically by always approaching tracks from the same

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direction. If a seek is in the OUT direction an overshoot is performed beyond the requested track so that it may be approached from the IN direction. This is achieved within the specified track-to-track access time.

The complete flow chart for the STEP operation is shown in Figure 22 (a)-(e).

## 9.2 Protection of index selection track

Protection of track -2 is considered to be of prime importance and a number of safeguards have been built into the firmware.

9.2.1. Interface controlled seeks to negative tracks have been inhibited in the following manner:-

(a) If the drive is operating in the 3ms mode, a check is made of the TRACK  $\emptyset\emptyset$  status after each step of the stepper motor. SEEK COMPLETE is forced at track  $\emptyset\emptyset$ .

(b) In the ramp mode, the flag  $\emptyset\emptyset$  signal is used to indicate a potential seek beyond track  $\emptyset\emptyset$ . Flag  $\emptyset\emptyset$  is used to switch from the ramp mode and revert to the 3ms step mode. Protection is then as case (a).

Protection in the ramp mode is not fail safe and should not be used by the controller to recalibrate the drive to track  $\emptyset\emptyset$ . That is, the recalibrate operation should be conducted in the 3ms mode.

9.2.2. At the end of each seek and before SEEK COMPLETE, a check is made. If the phase combinations for track -2 and flag  $\emptyset\emptyset$  are both true the microprocessor will perform an auto-recalibration to track  $\emptyset\emptyset$  and issue SEEK COMPLETE.

## APPENDIX 1

### Patents

UK Application Number	US Application Number	Title
8041323	332003	"Read-Write Head Thermal Compensation System."
8113614	373281	"Method and Apparatus for Controlling a Stepper Motor."
8120092	391010	"Generation of Unique Index Mark from the Commutation of DC Brushless Motor."
8120093	391150	"Damping of Stepper Motor using Non-Active Windings."
	388165	"Ventilation System for computer Disc Drive Hub Assembly."

## APPENDIX 2

### Write Data Pre-Compensation Scheme

Data sequence	Required write
leftmost bit written first	pre-compensation of centre bit

00	0	10	EARLY
00	0	11	EARLY
00	1	10	LATE
00	1	11	LATE
01	1	00	EARLY
01	1	01	EARLY
10	0	00	LATE
10	0	01	LATE
10	1	10	LATE
10	1	11	LATE
11	1	00	EARLY
11	1	01	EARLY

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## APPENDIX 3

### Format Recommendations

1.0 The following sections describe the general formatting recommendations for the RO 200 series disk drives.

2.0 **Encoding.** It is recommended that data be written on the disk using an MFM encode. The algorithm to convert from NRZ data to MFM data is as follows:-

For a "1" write a flux transition in the middle of the bit cell; for a "0" write a flux transition at the start of the bit cell except when a "0" follows a "1".

3.0 **General Requirements.** The format of the data recorded on the disk is totally a function of the host controller. The two most common formats allow 32 x 256 byte sectors or 16 x 512 byte sectors to be written on each track. A soft sectored format should be used. The start of each sector is identified by a unique byte which is written on the disk. This byte is normally an invalid MFM code (eg. Hex A1 with a missing clock bit). This unique byte is used to flag the start of the sector address field (containing the physical sector address) and also to flag the start of the sector data field.

4.0 **Sector Format Example.** An example of a recommended format for a 256 byte sector is given in Figure A. A full description of each item is given below:-

1. **Inter Sector Gap.** (15 bytes of Hex "4E"). Tolerance gap to allow for disk speed variations.
2. **Sync Field.** (13 bytes of "00"). Provides VFO lock-on prior to data retrieval. The minimum number of bytes is dependent on VFO lock up performance of host data separator.

3. **Address Mark.** (1 byte of Hex "A1" with missing clock). Identifies beginning of address field.

4. **Address Mark. I.D. Field Identifier** (1 byte Hex "FE") Identifies with previous address mark the beginning of the address field.

5. **Cylinder Address.** (1 byte, "0" to Hex "FF"). The most significant bit in the Head Address field (6) can be used to represent the most significant bit of the Cylinder Address.

6. **Head Address.** (1 byte, "0" to "7").

7. **Sector Address.** (1 byte, "0" to Hex "1F").

8. **Address ECC.** (3 bytes). Available for ECC check of the address field.

9. **Gap.** (2 bytes "00"). Allows write turn-on time when updating the sector data field.

10. **Sync Field.** (13 bytes of "00"). Provides VFO lock-on prior to data retrieval.

11. **Address Mark.** (1 byte of Hex "A1" with missing clock). Identifies beginning of data field.

12. **Address Mark Data Field Identifier** (1 byte Hex "F8"). Identifies with previous address mark the beginning of the data field.

13. **Data.** (256 bytes of data).

14. **Data ECC.** (3 bytes). Available for ECC check of the data field.

15. **Gap.** (2 bytes of "00"). Allows write turn-off time when updating the sector data field.

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- 5.0 **Index Gap.** The gap at the beginning of index allows for head switching recovery, so that sequential sectors may be read without losing a complete disk revolution. Minimum length is 12 bytes; Hex pattern "4E". Normal recommendation is 16 byte lengths.
- 6.0 **Speed Tolerance Gap.** This gap at the end of the last physical sector (before index) provides a spindle speed tolerance buffer for the whole track. A full track format routine begins and ends with detection of index. It is usually a Hex pattern "4E", and the actual number of bytes depends on media speed during the format operation.
- 7.0 **Sector Interleaving.** It is possible to interleave sectors to improve data throughput during typical read/write operations by allowing multiple sector transfer within a single revolution.

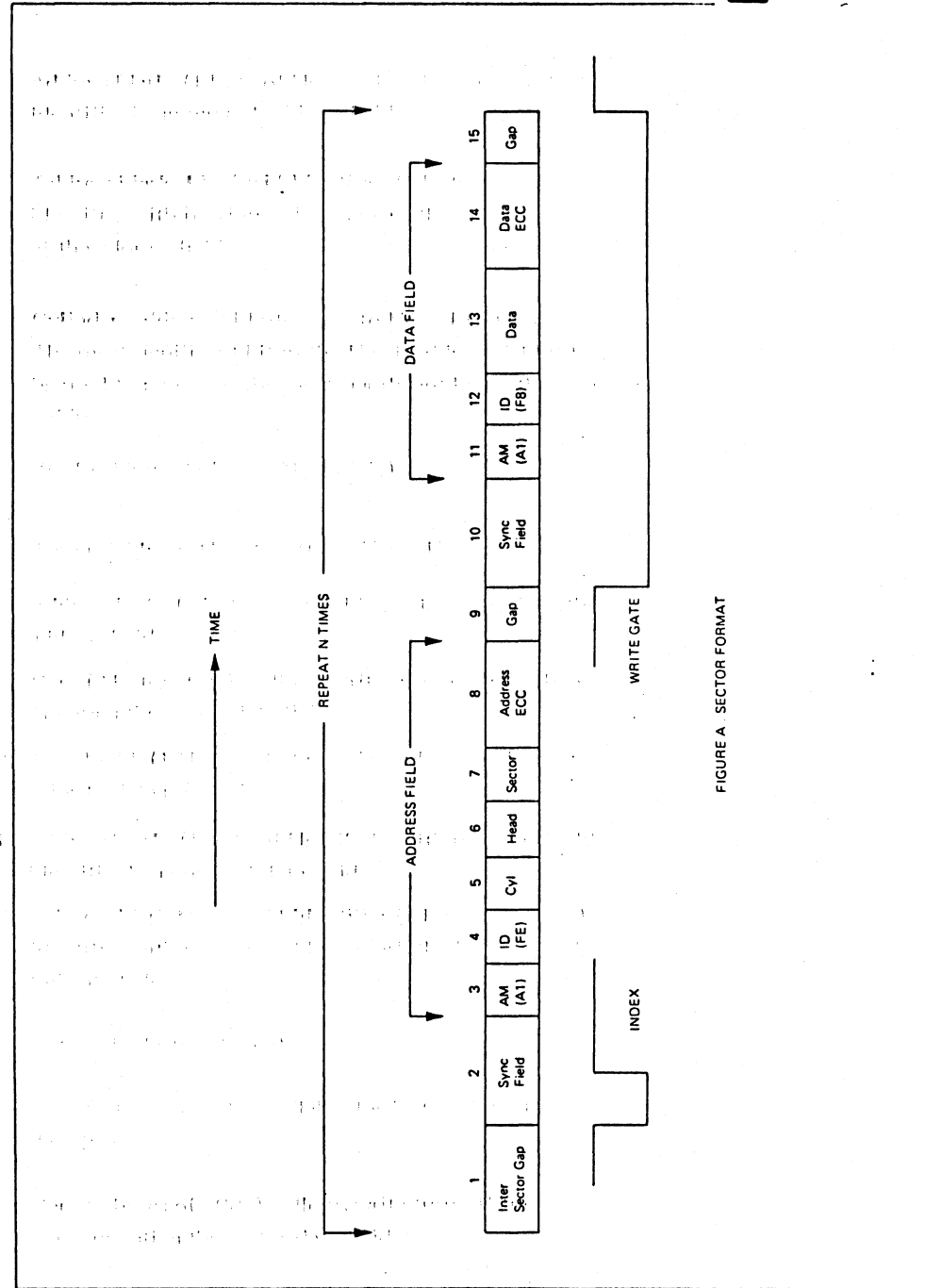
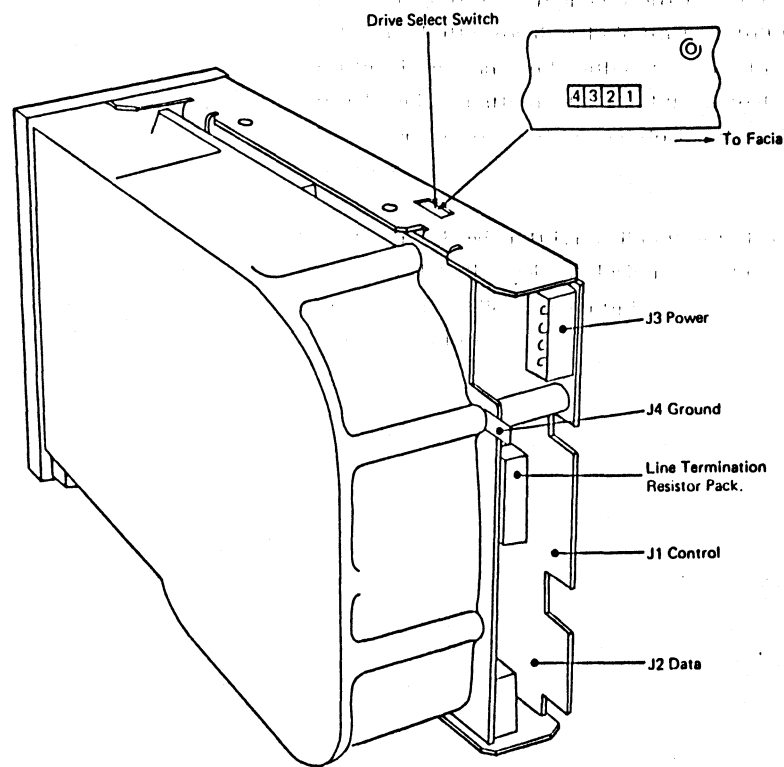
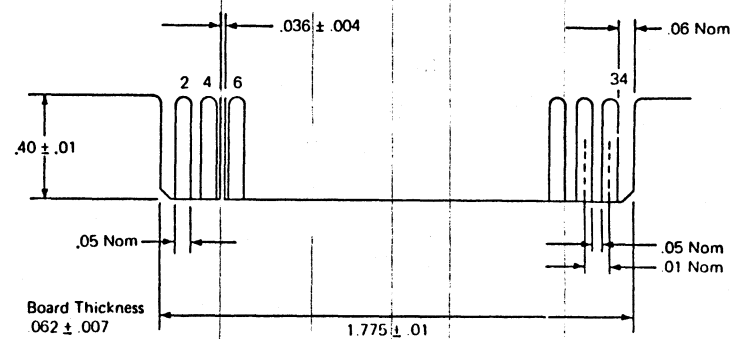


FIGURE A. SECTOR FORMAT

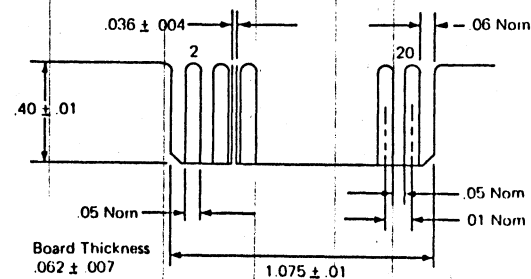
**FIGURE 1**  
Drive outline showing connector positions



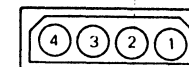
**FIGURE 2**  
J1 Connector – Control



**FIGURE 3**  
J2 Connector – Data



**FIGURE 4**  
J3 Connector – Power



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FIGURE 5  
Control and power bus

Flat Ribbon or Twisted  
Pair 20 Ft. Max.

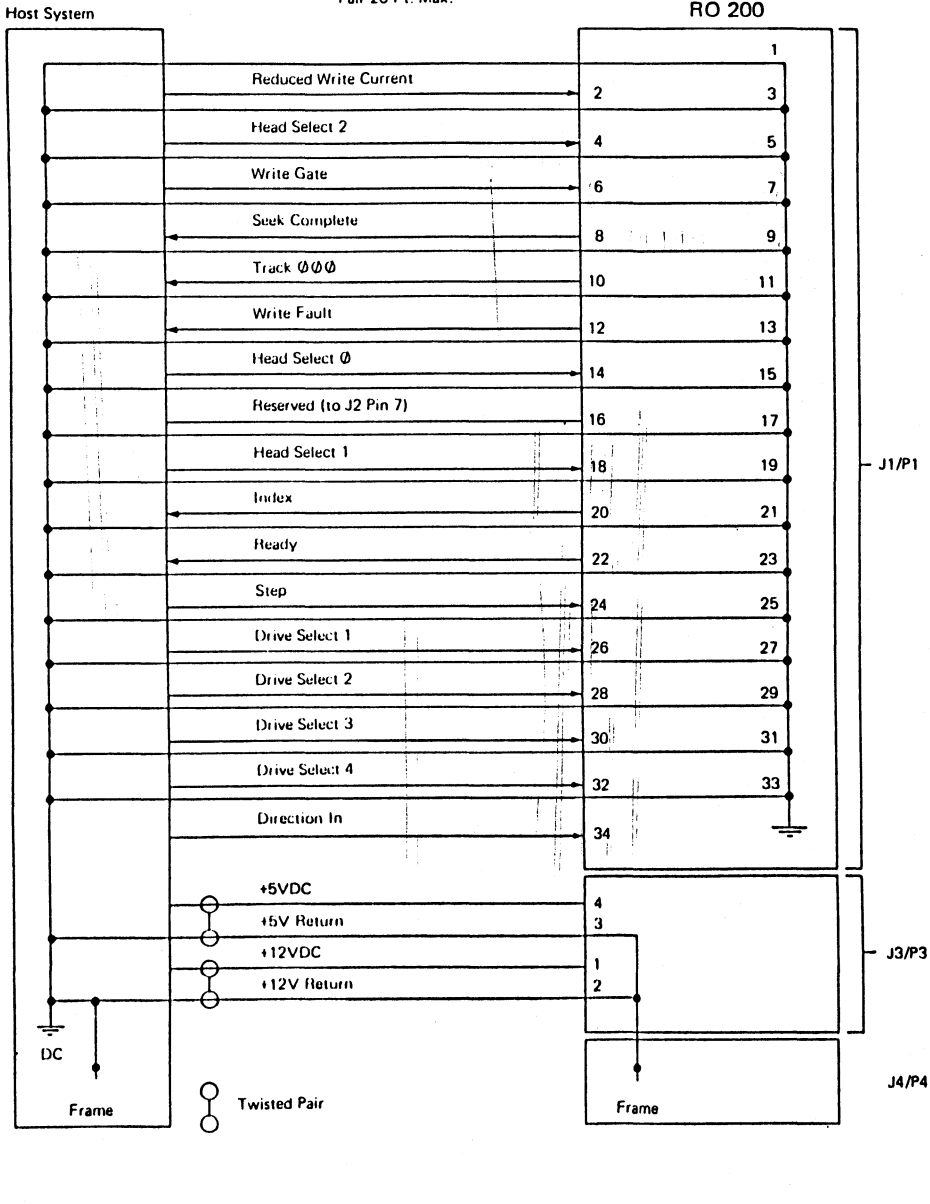
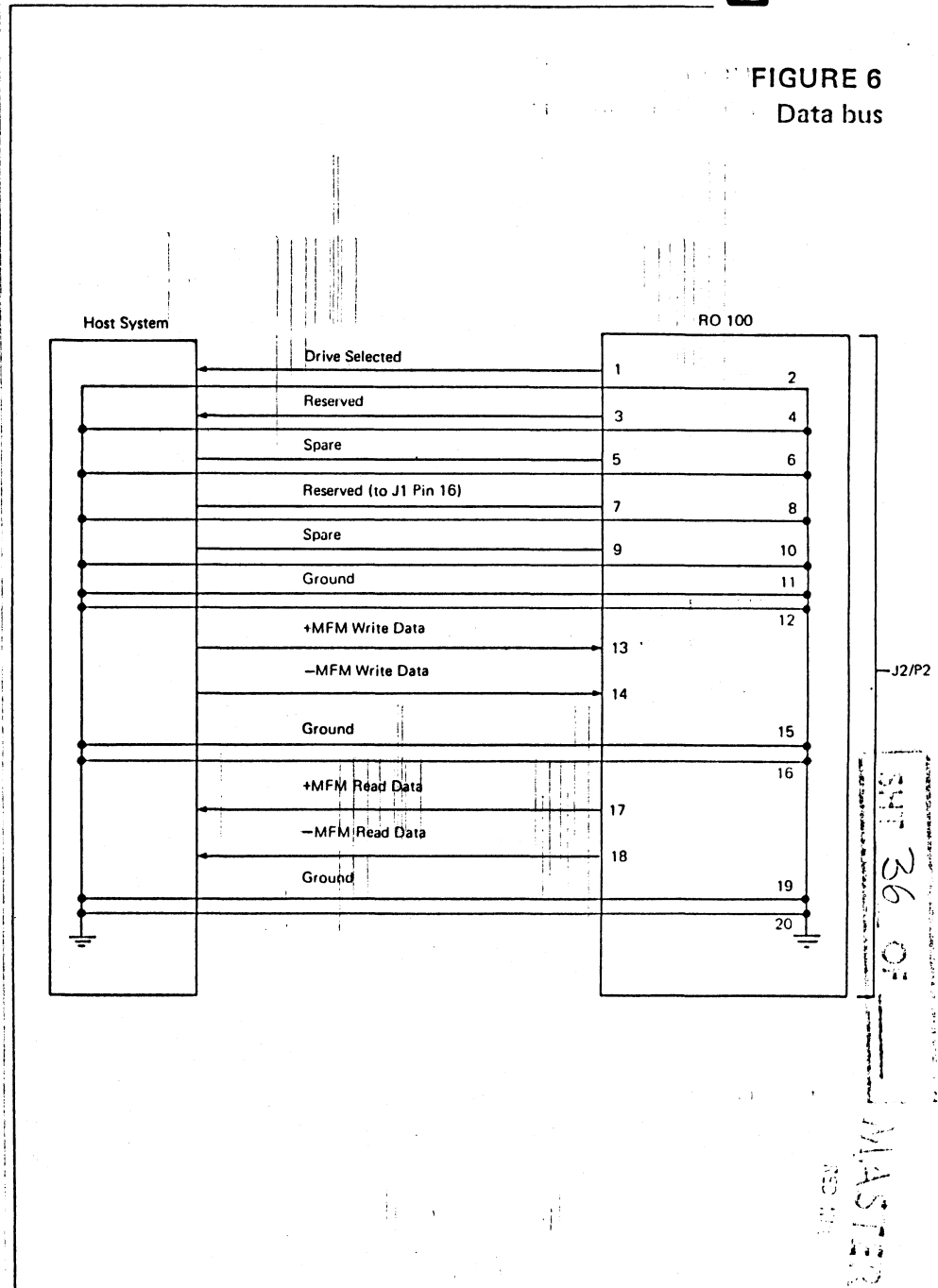
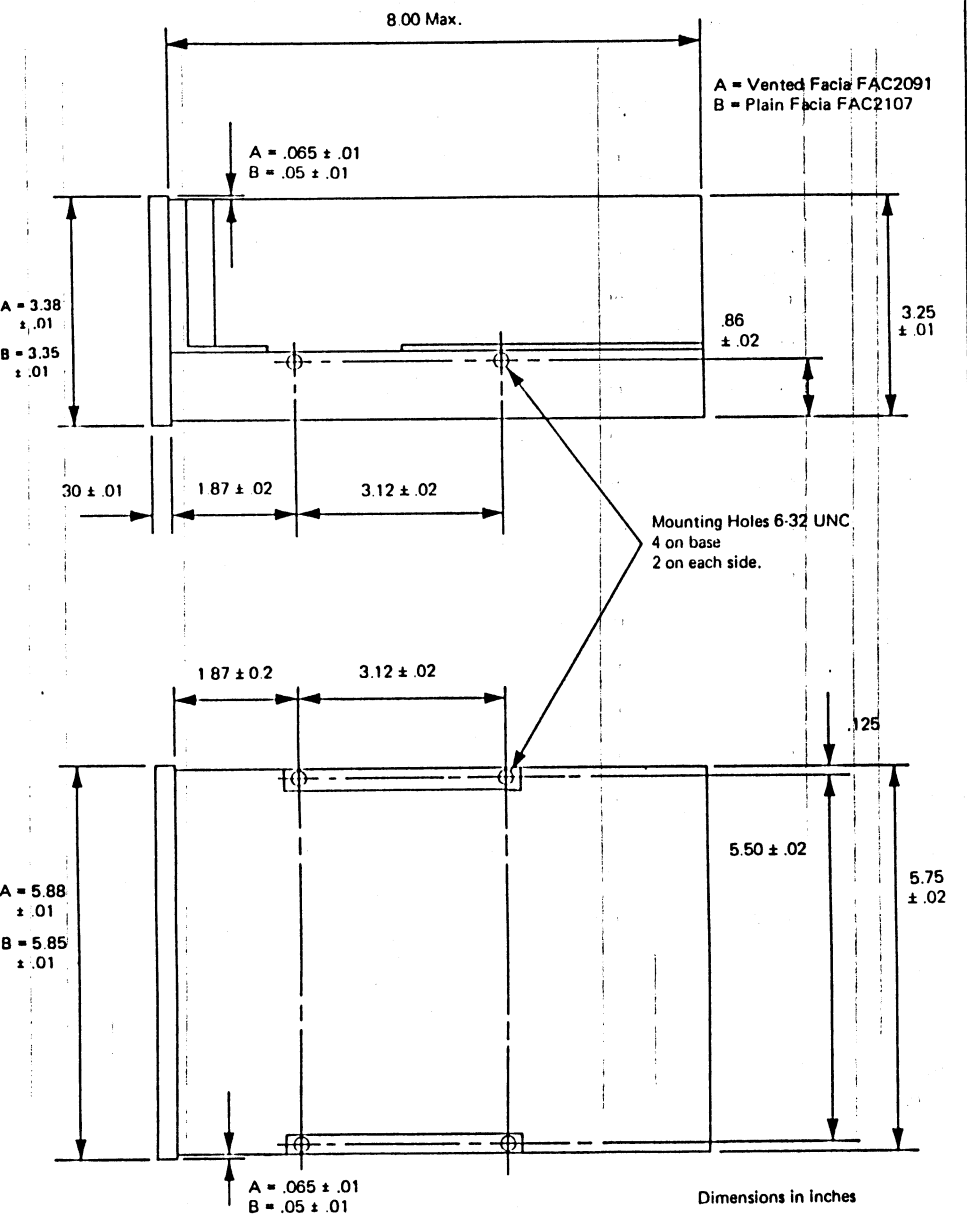


FIGURE 6  
Data bus

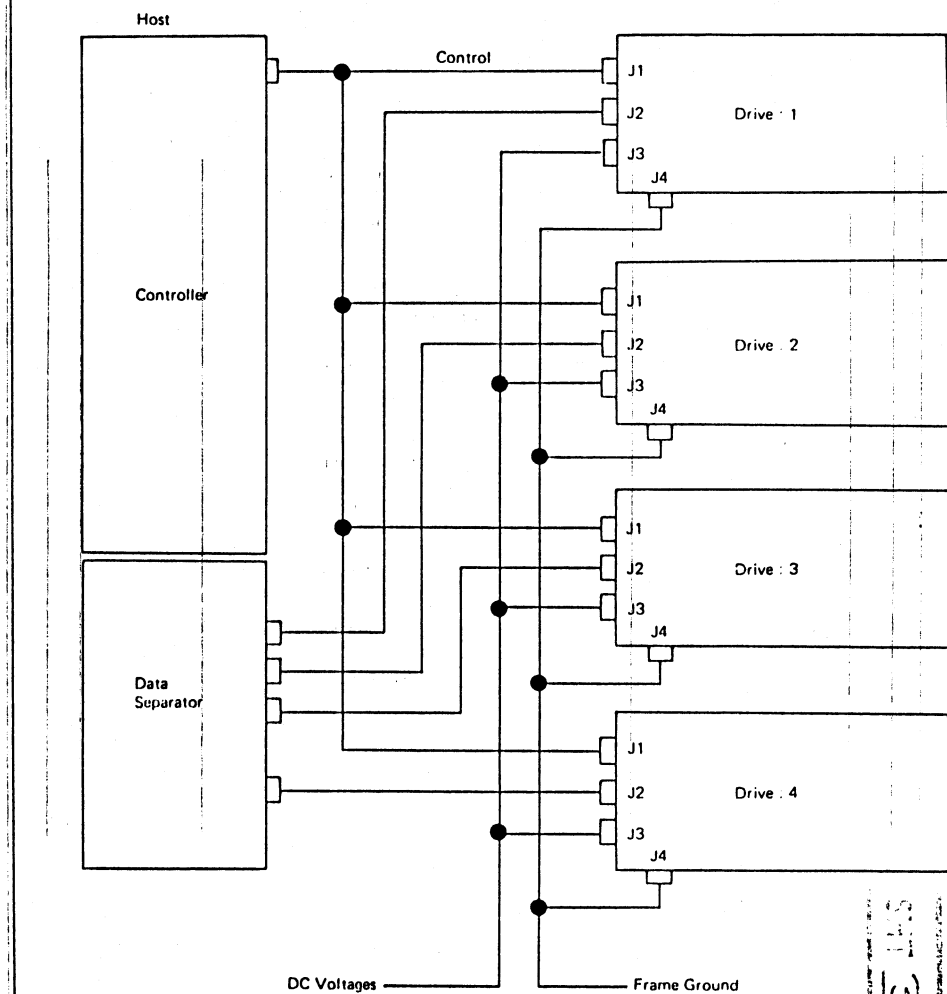




**FIGURE 7**  
Mounting details

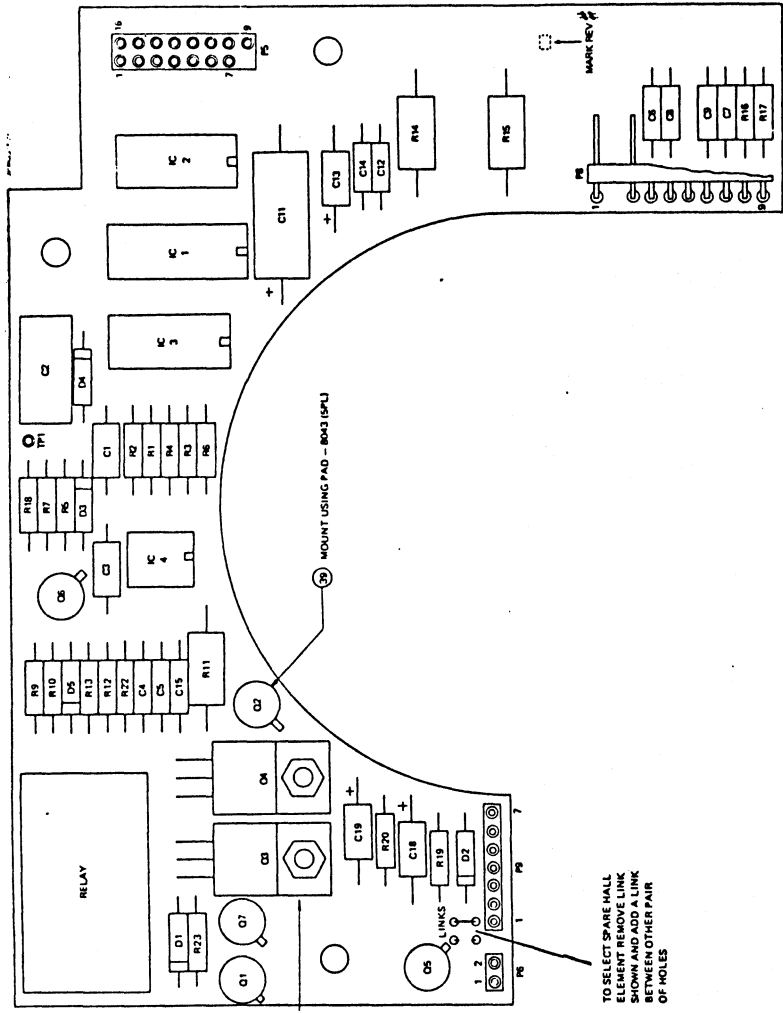


**FIGURE 8**  
System with 4 drives



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**FIGURE 9**  
Wiring of spare hall element

**FIGURE 10**  
Non-planar section of RO 204

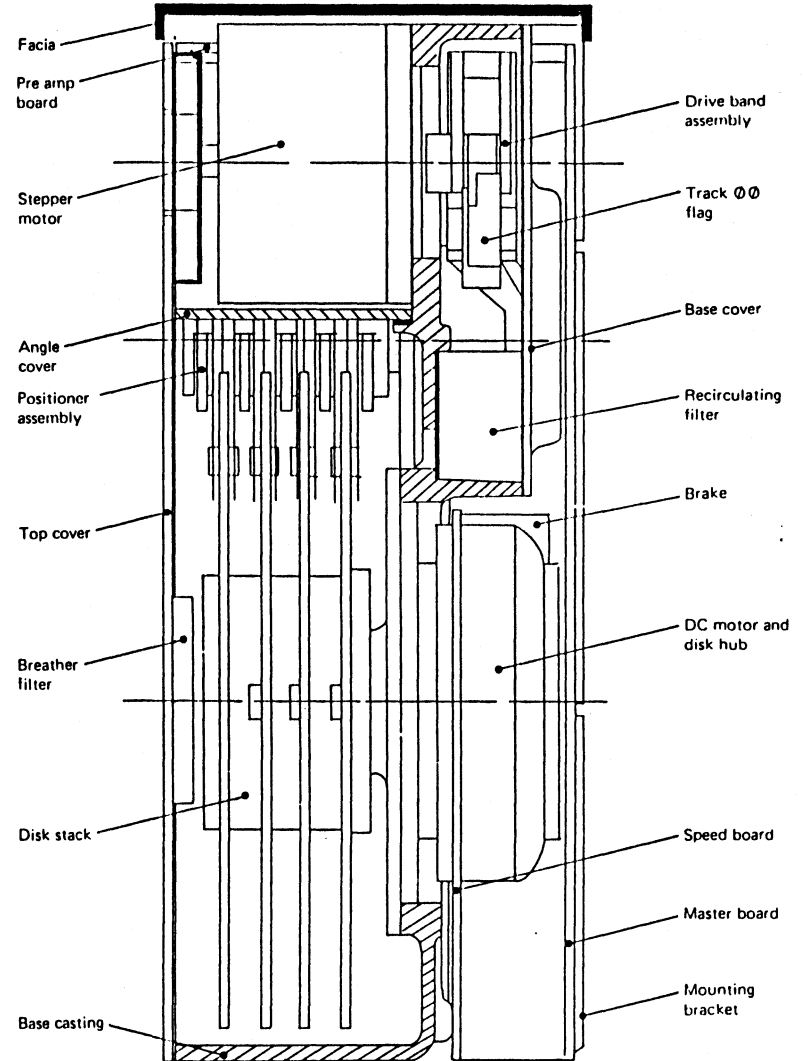


FIGURE 11  
Air flow and filter system

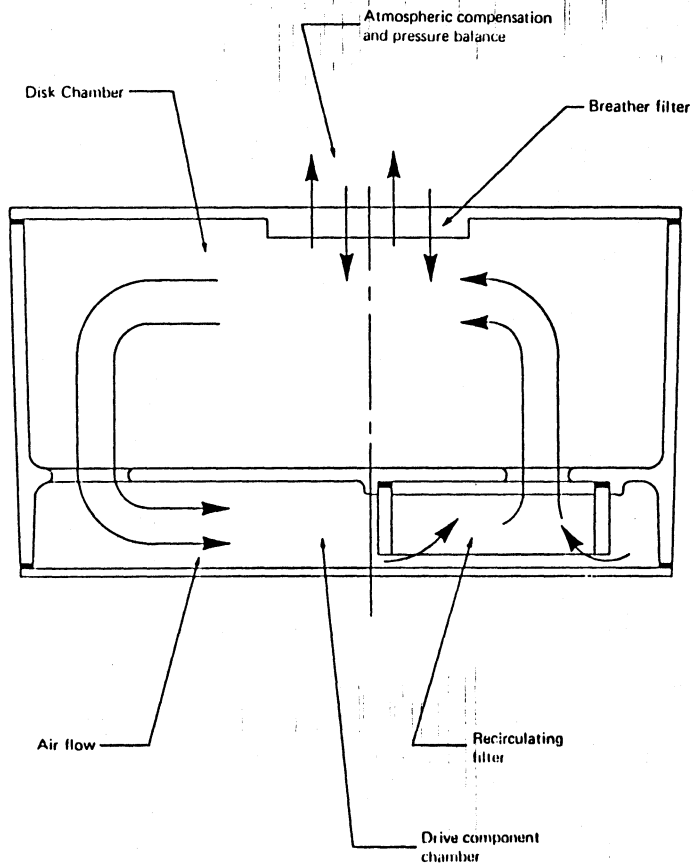
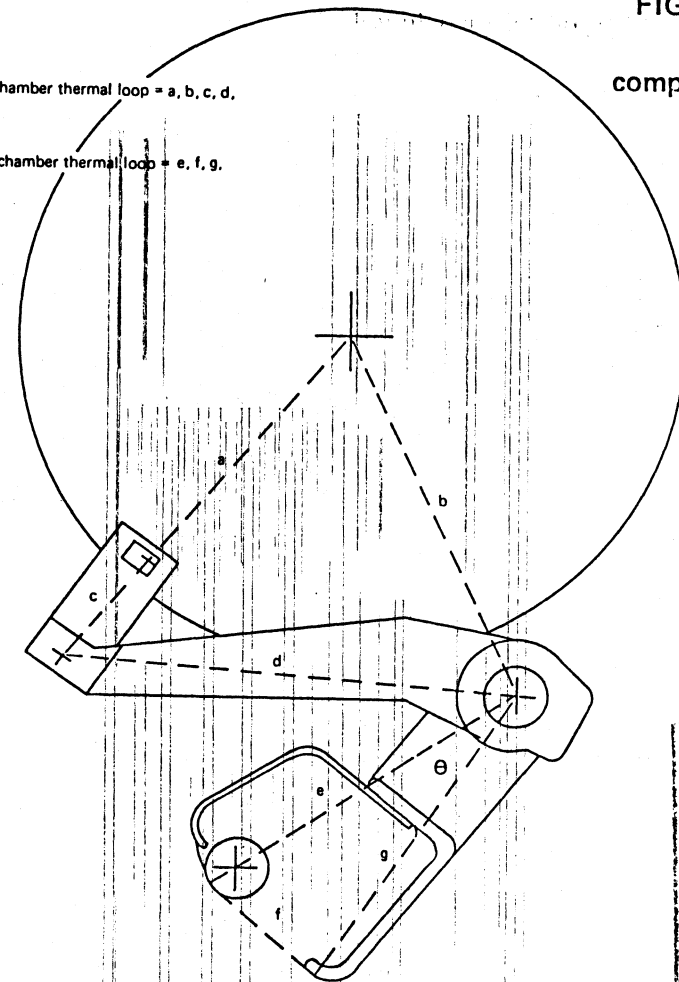


FIGURE 12  
Thermal compensation

Disk chamber thermal loop = a, b, c, d.

Drive chamber thermal loop = e, f, g.



for a given temperature rise

$$\Delta c < \Delta a, \Delta b \text{ and } \Delta d \text{ therefore } r/w \text{ gap tends}$$

to move outward from track centre

but  $\Delta e > \Delta f$  and  $\Delta g$  : therefore angle  $\theta$  tends  
to decrease causing a clockwise rotation of the  $r/w$  gap back towards centre

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FIGURE 13 Board interconnections

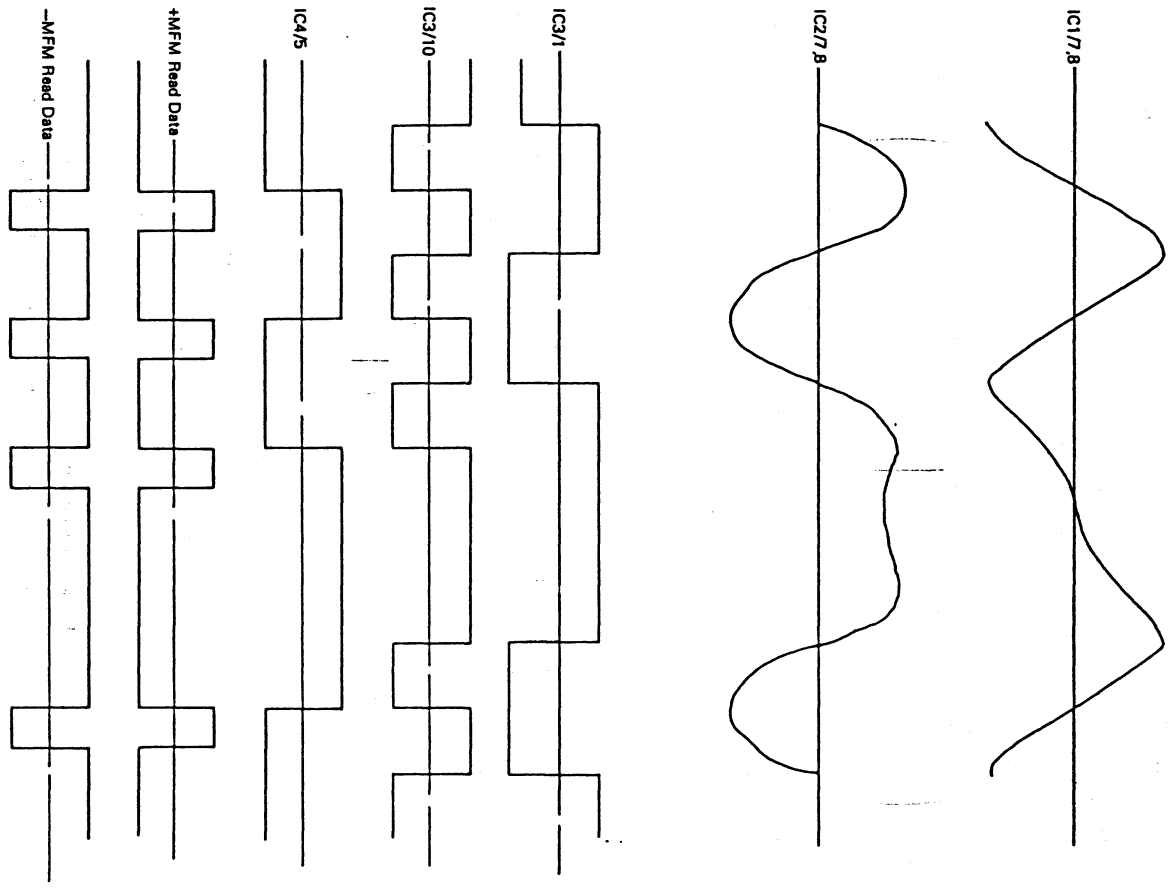
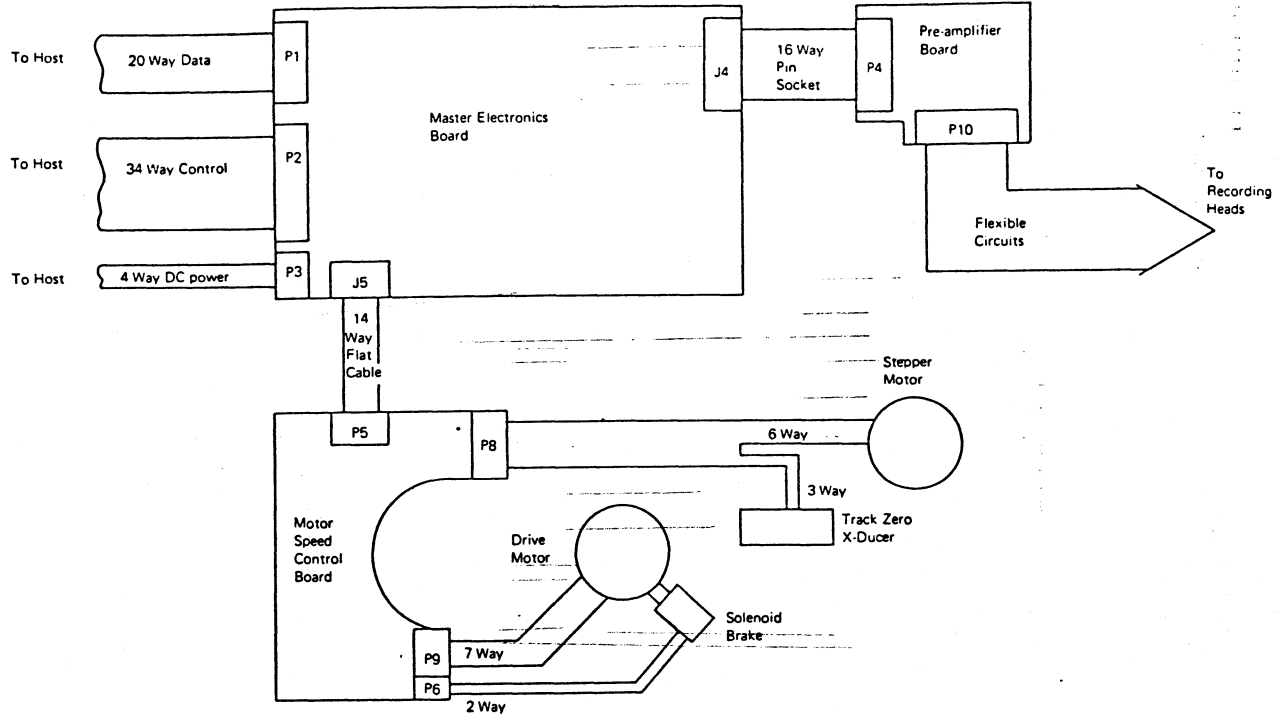
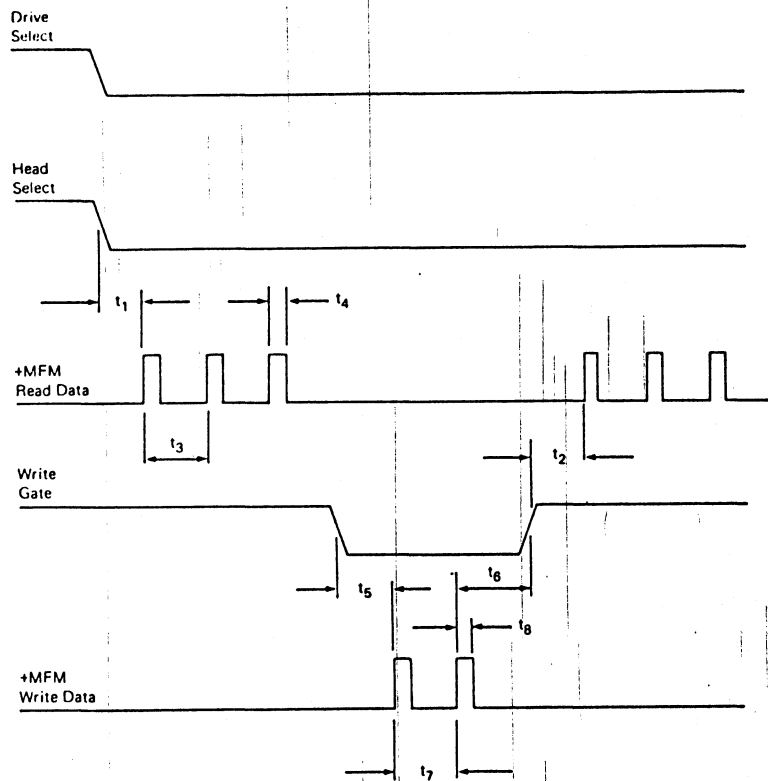


FIGURE 14 Read channel signals

**FIGURE 15**  
Read/Write data timing



Label	Description	Min	Typ	Max	Units
t <sub>1</sub>	Select to Read Data			5	us
t <sub>2</sub>	Write to Read Recovery			5	us
t <sub>3</sub>	Read bit cell		200		ns
t <sub>4</sub>	Read Data pulse width	25		200	ns
t <sub>5</sub>	Write Gate true to Write Data			400	ns
t <sub>6</sub>	Write Data to Write Gate False			400	ns
t <sub>7</sub>	Write bit cell		200		ns
t <sub>8</sub>	Write Data pulse width	25			ns

**FIGURE 16**  
Stepper motor drive configuration

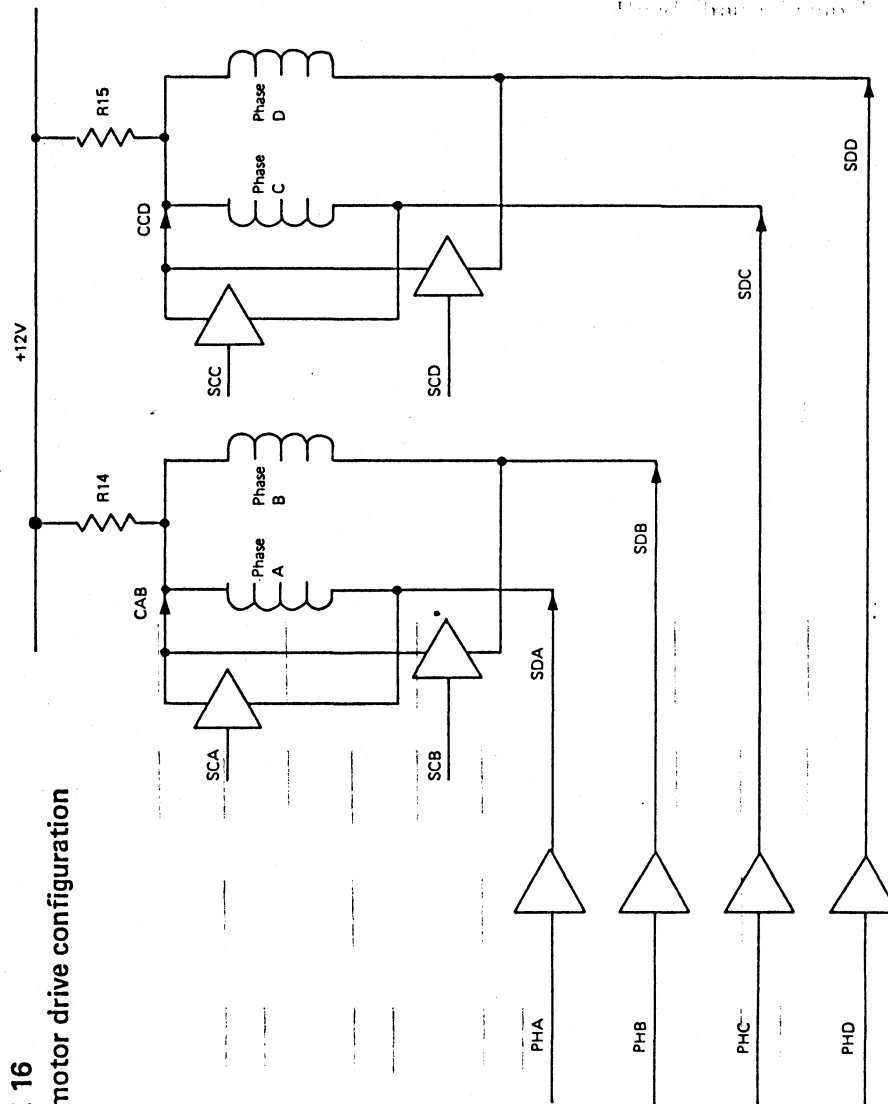
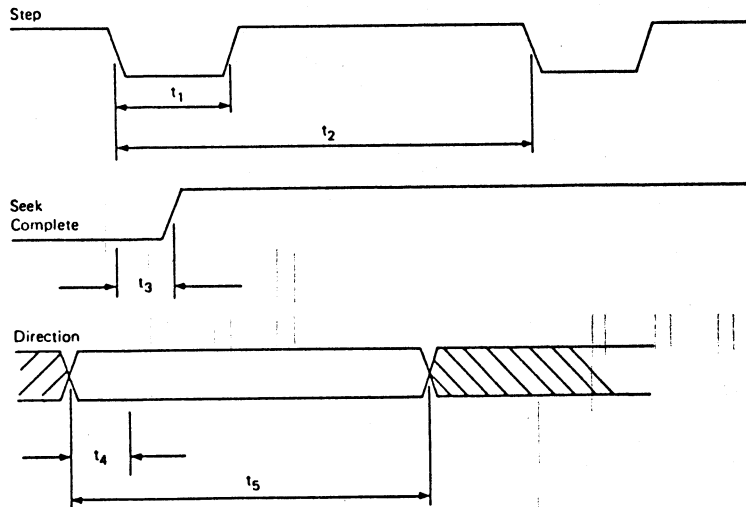


FIGURE 17  
Step pulse timing



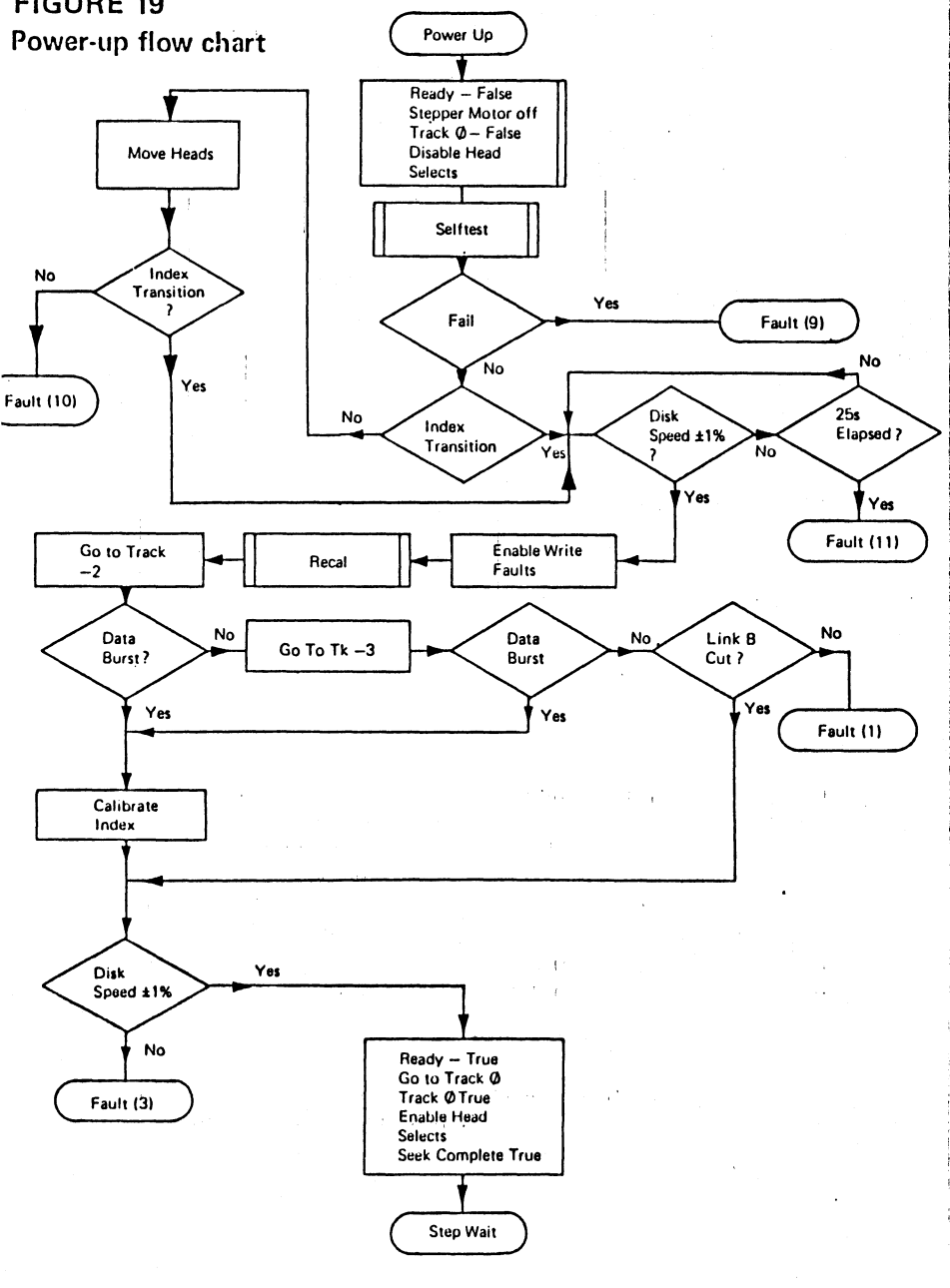
Label	Description	Min	Typ	Max	Units
t <sub>1</sub>	Width of Step pulse	0.5	5		us
t <sub>2</sub>	Time between Step pulses	10		3100	us*
t <sub>3</sub>	Time from first Step to Seek Complete False		40		ns
t <sub>4</sub>	Direction set to first Step	0			ns
t <sub>5</sub>	First Step to direction change (for overlap seek)	150			us

\*Maximum time between step pulses can be increased to 8000 us with a user selectable option.

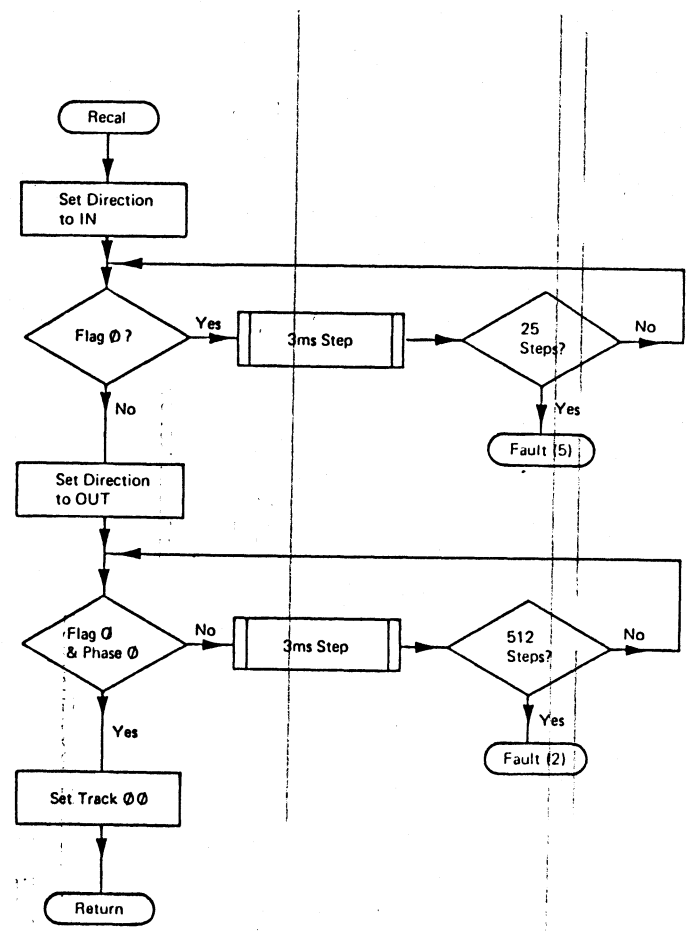
FIGURE 18  
Stepper winding configuration

Track	Winding configuration				Return
	A Yellow	B Blue	C Red	D Black	
0	1	0	0	1	Green
1	0	0	1	1	
2	0	1	0	1	White
3	0	1	0	0	
4	0	1	1	0	Green
5	0	0	1	0	
6	1	0	1	0	White
7	1	0	0	0	

**FIGURE 19**  
Power-up flow chart



**FIGURE 20**  
Recalibration flow chart



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FIGURE 21  
Write fault flow chart

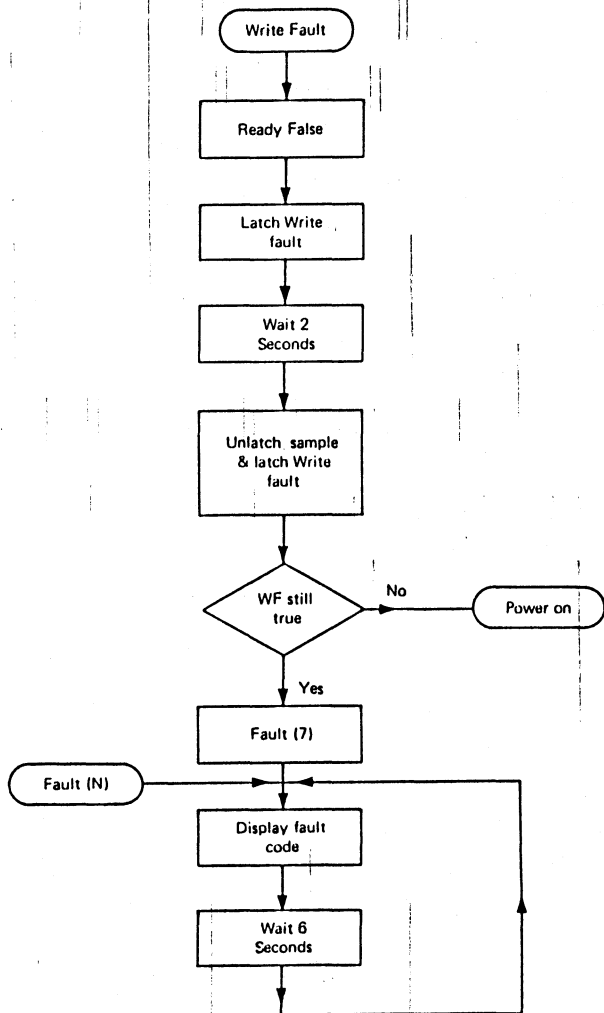
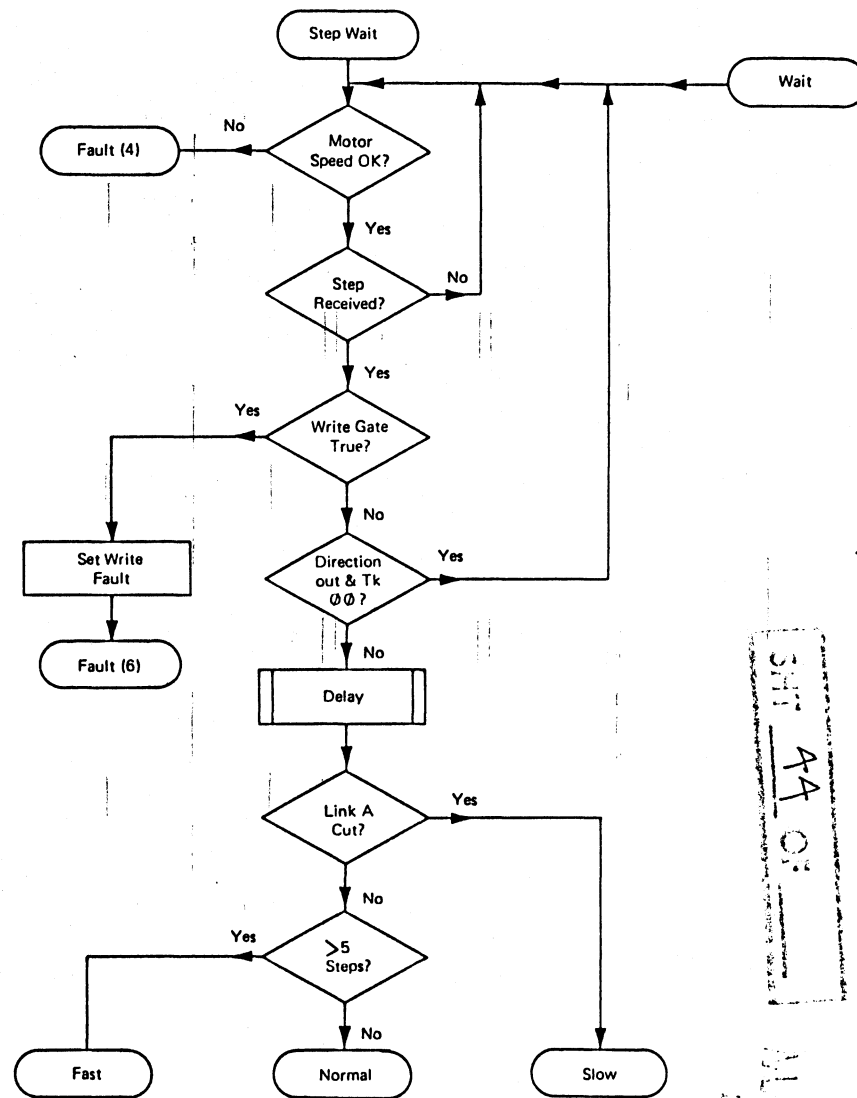


FIGURE 22(a)  
Step flow chart



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FIGURE 22(b)  
Step flow chart

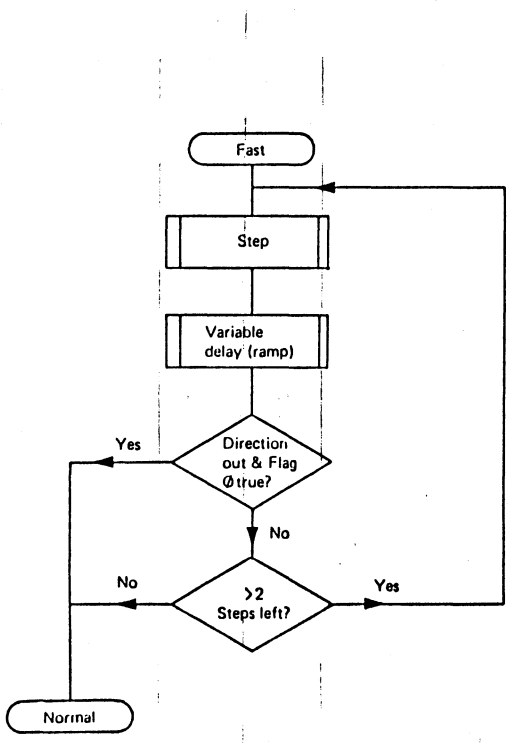
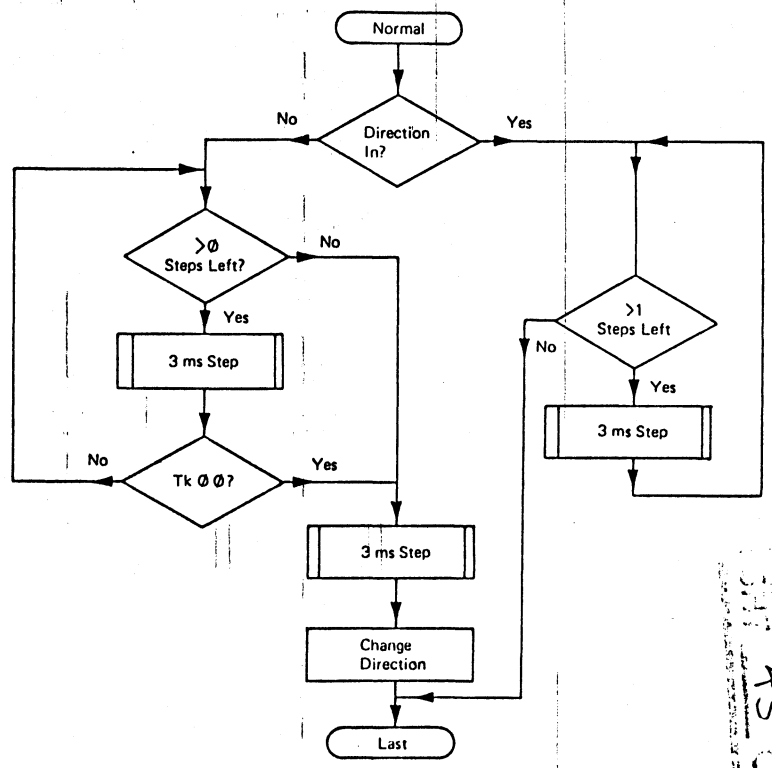


FIGURE 22(c)  
Step flow chart



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FIGURE 22(d)  
Step flow chart

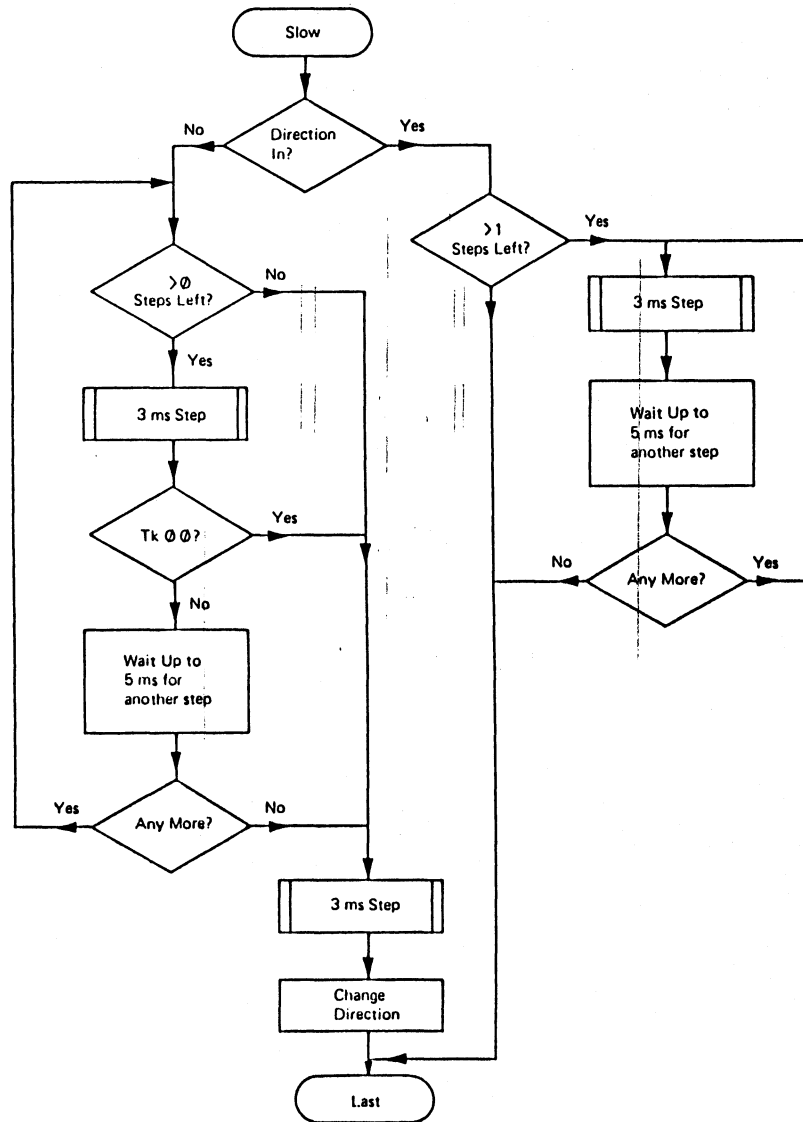
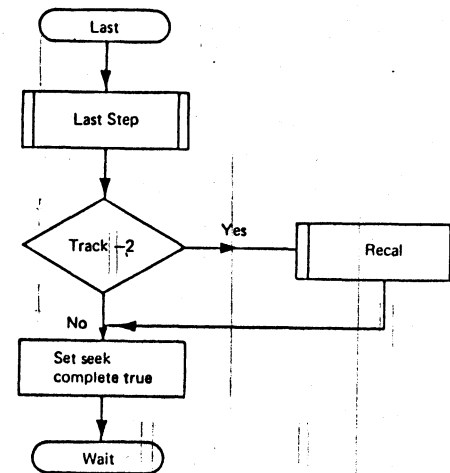


FIGURE 22(e)  
Step flow chart



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FIGURE 23  
Master PCB layout

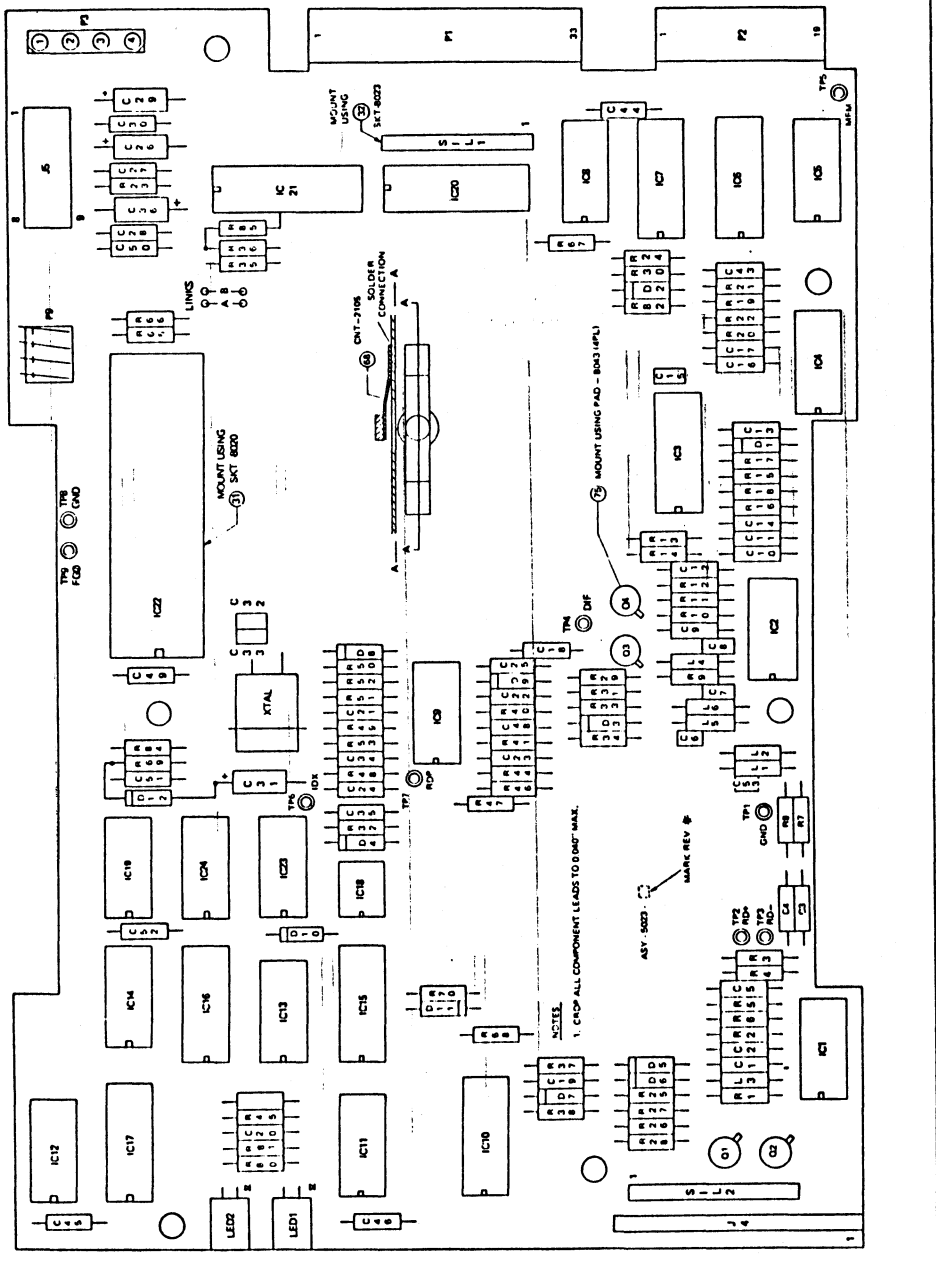
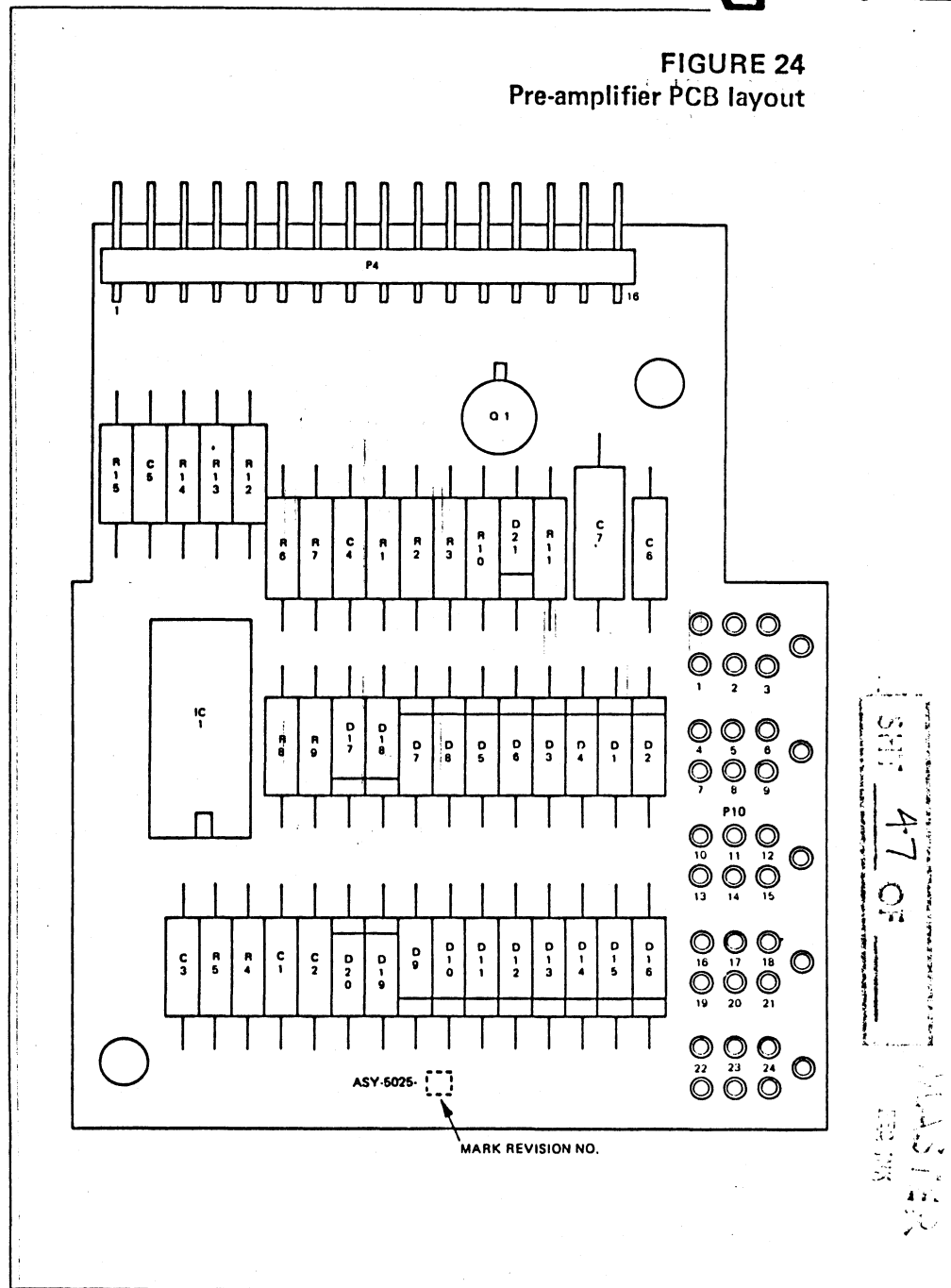


FIGURE 24  
Pre-amplifier PCB layout



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MASTER

FIGURE 25  
Motor speed control PCB layout

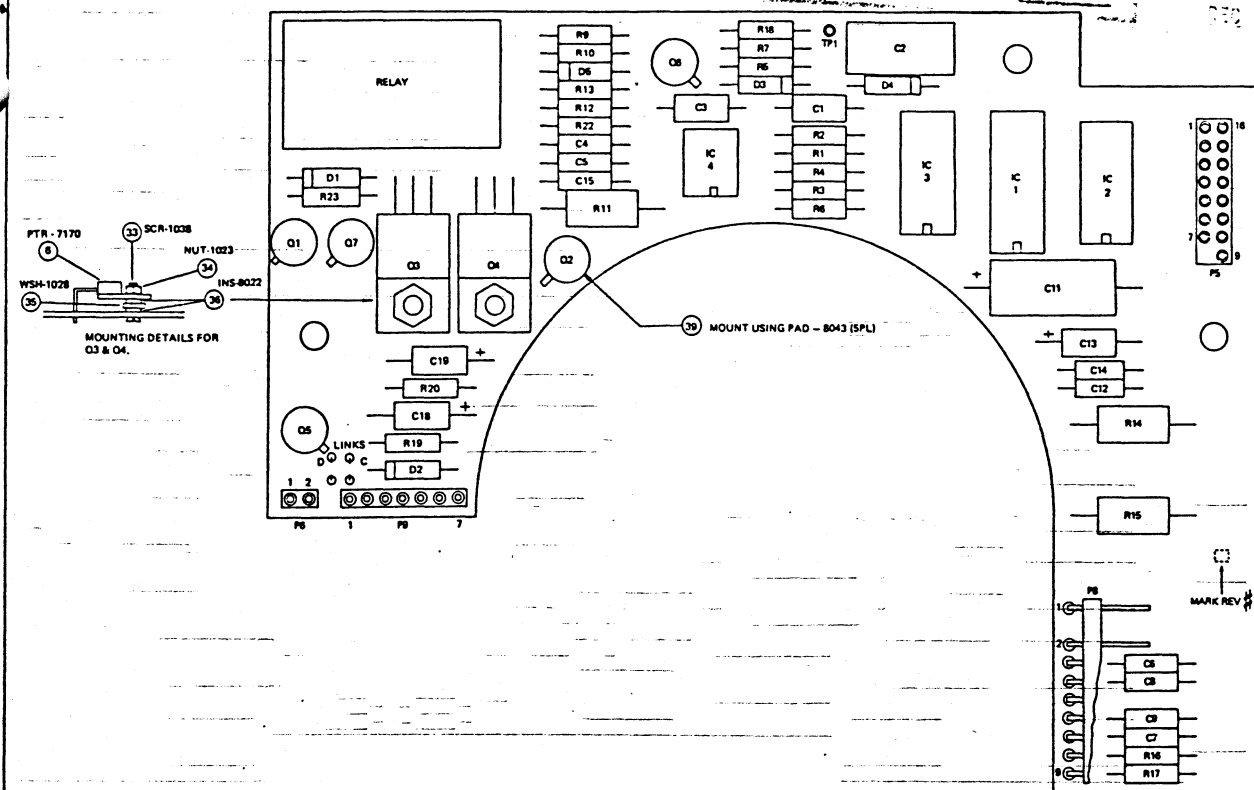


FIGURE 26(a)  
Master PCB schematic

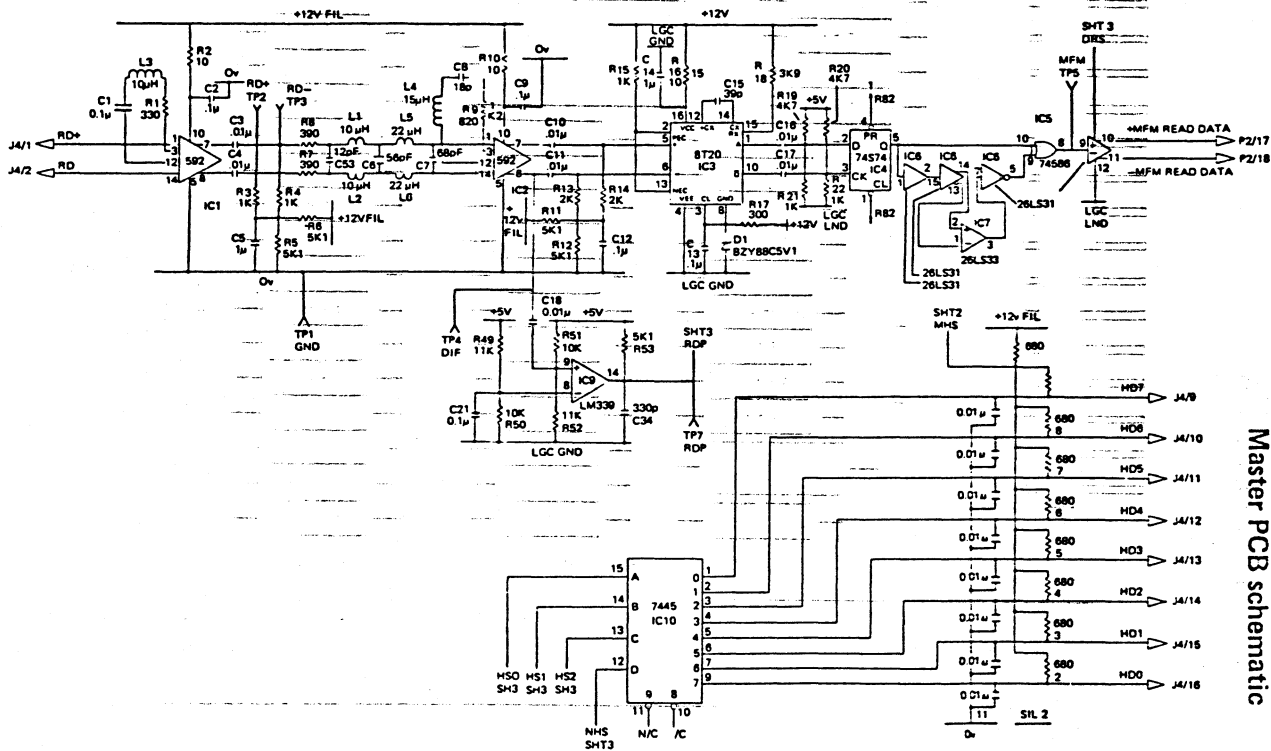


FIGURE 26(b)  
Master PCB schematic

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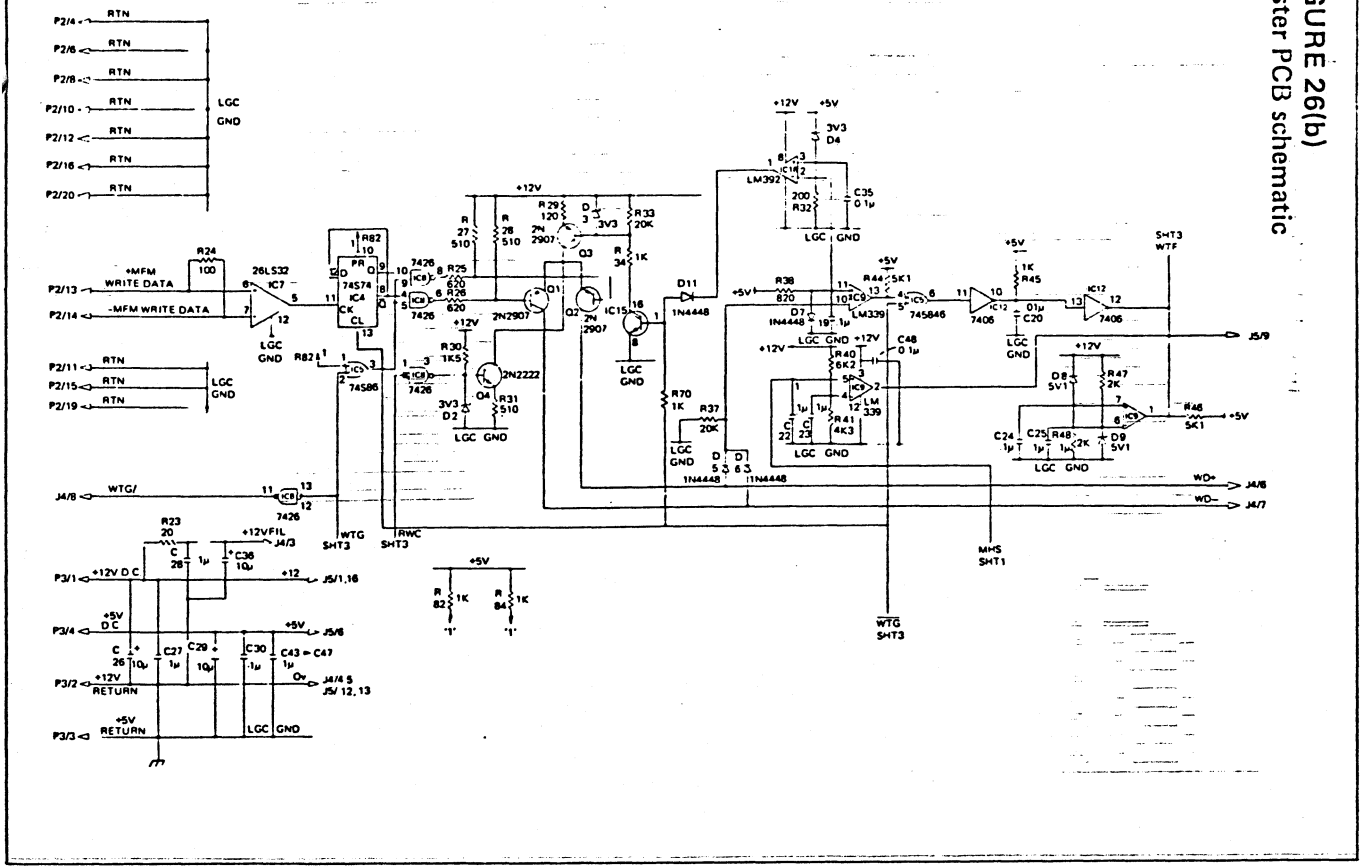
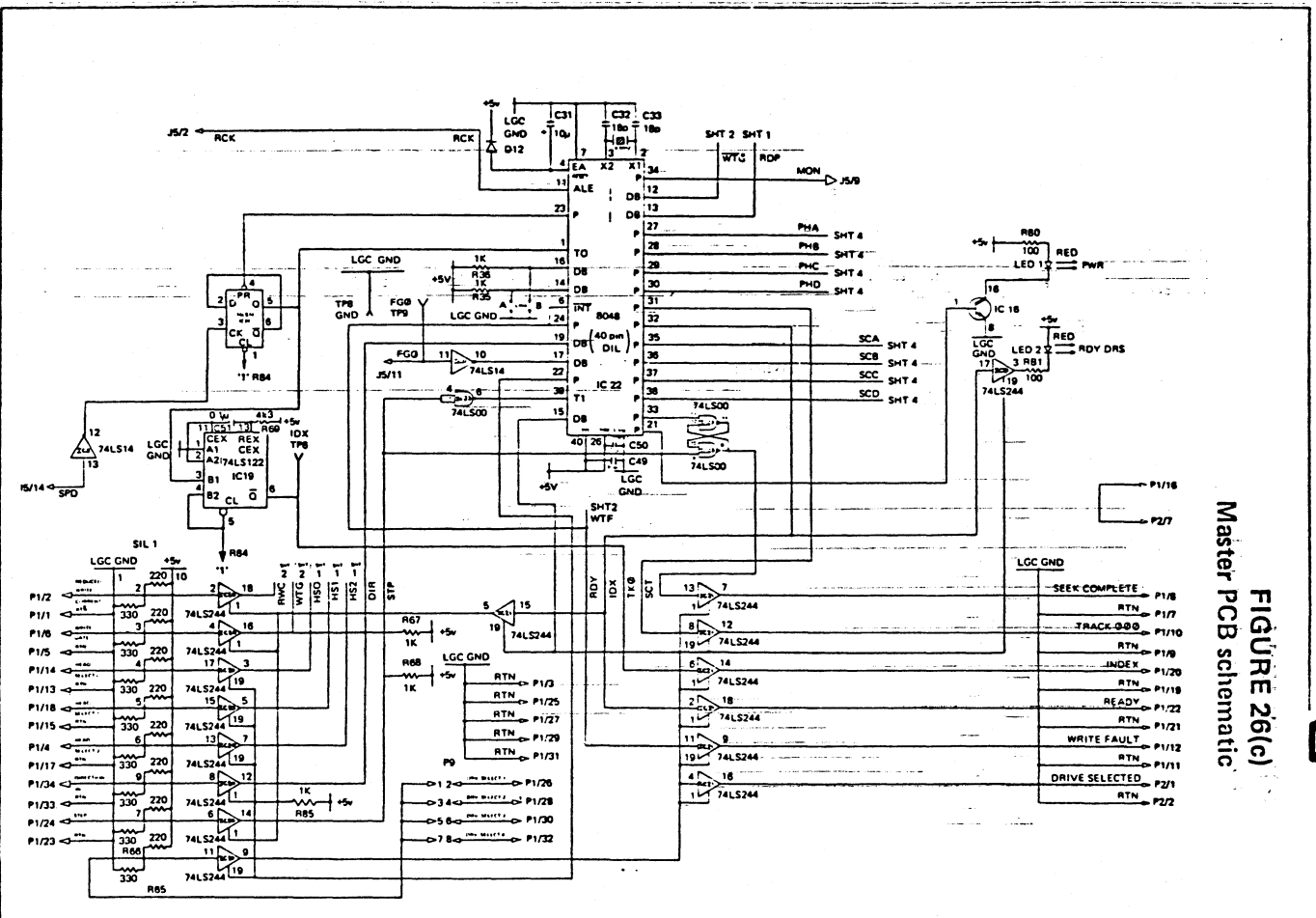


FIGURE 26(c)  
Master PCB schematic



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FIGURE 26(D)  
Master PCB schematic

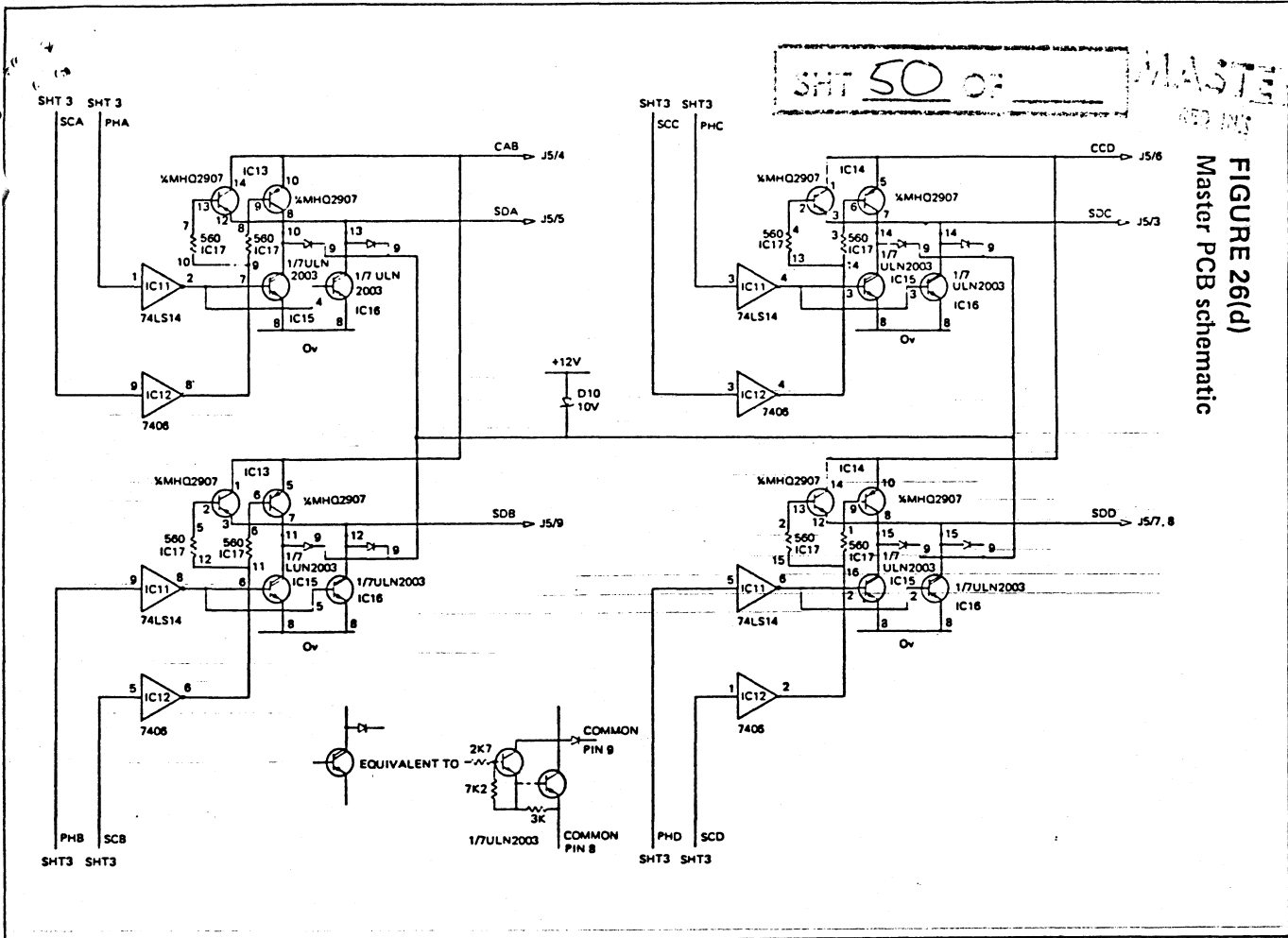
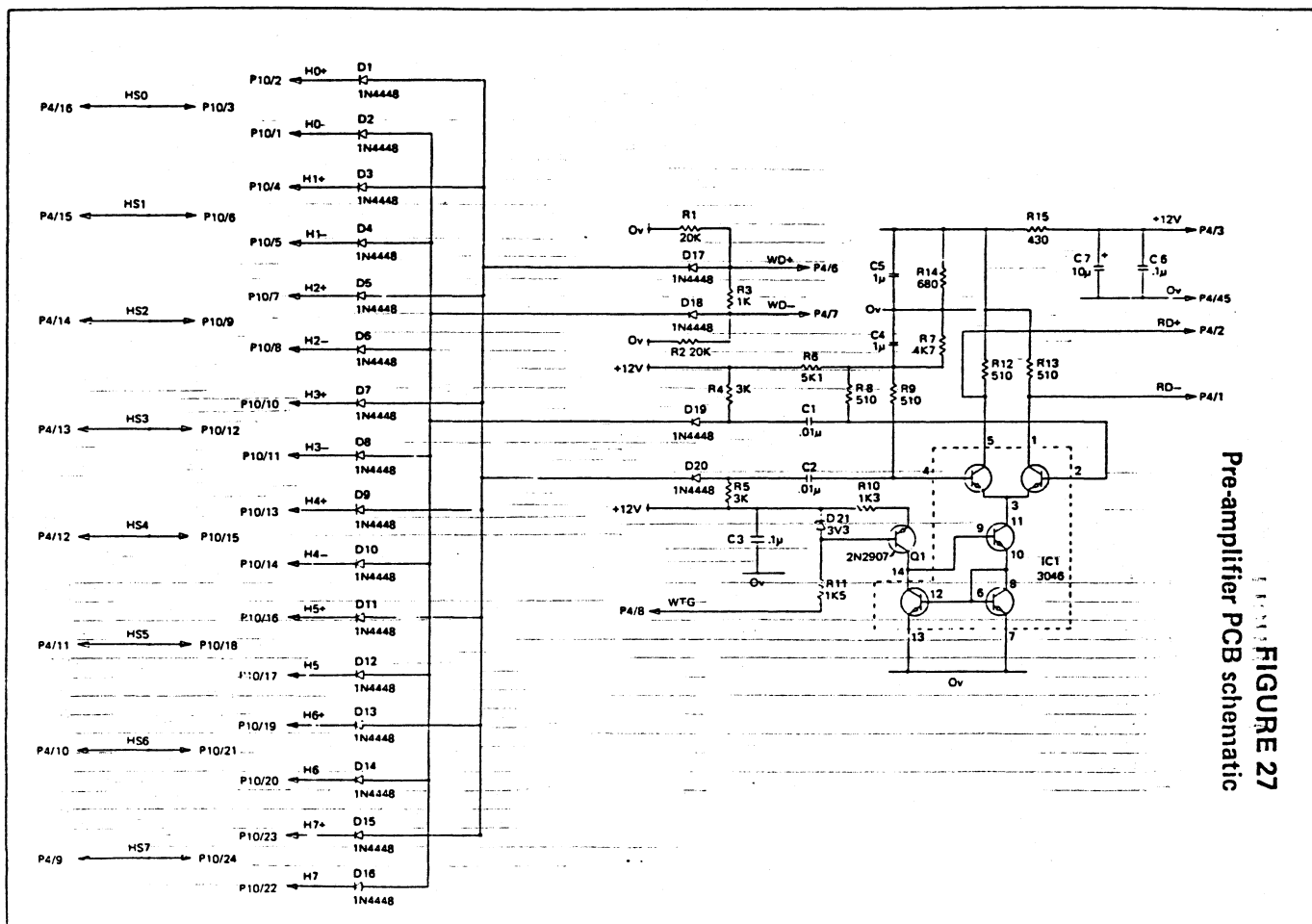


FIGURE 27  
Pre-amplifier PCB schematic



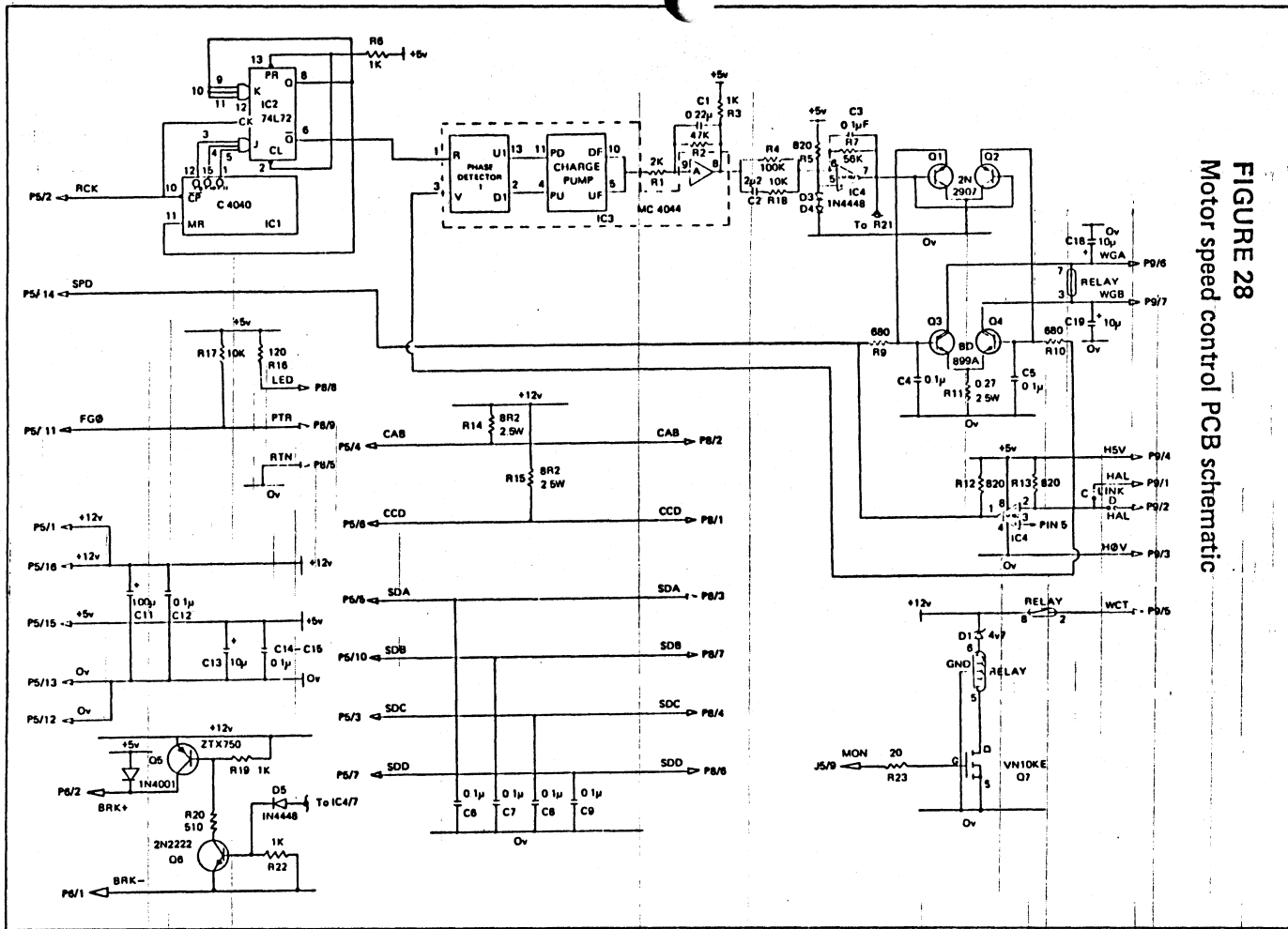


FIGURE 28  
Motor speed control PCB schematic

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