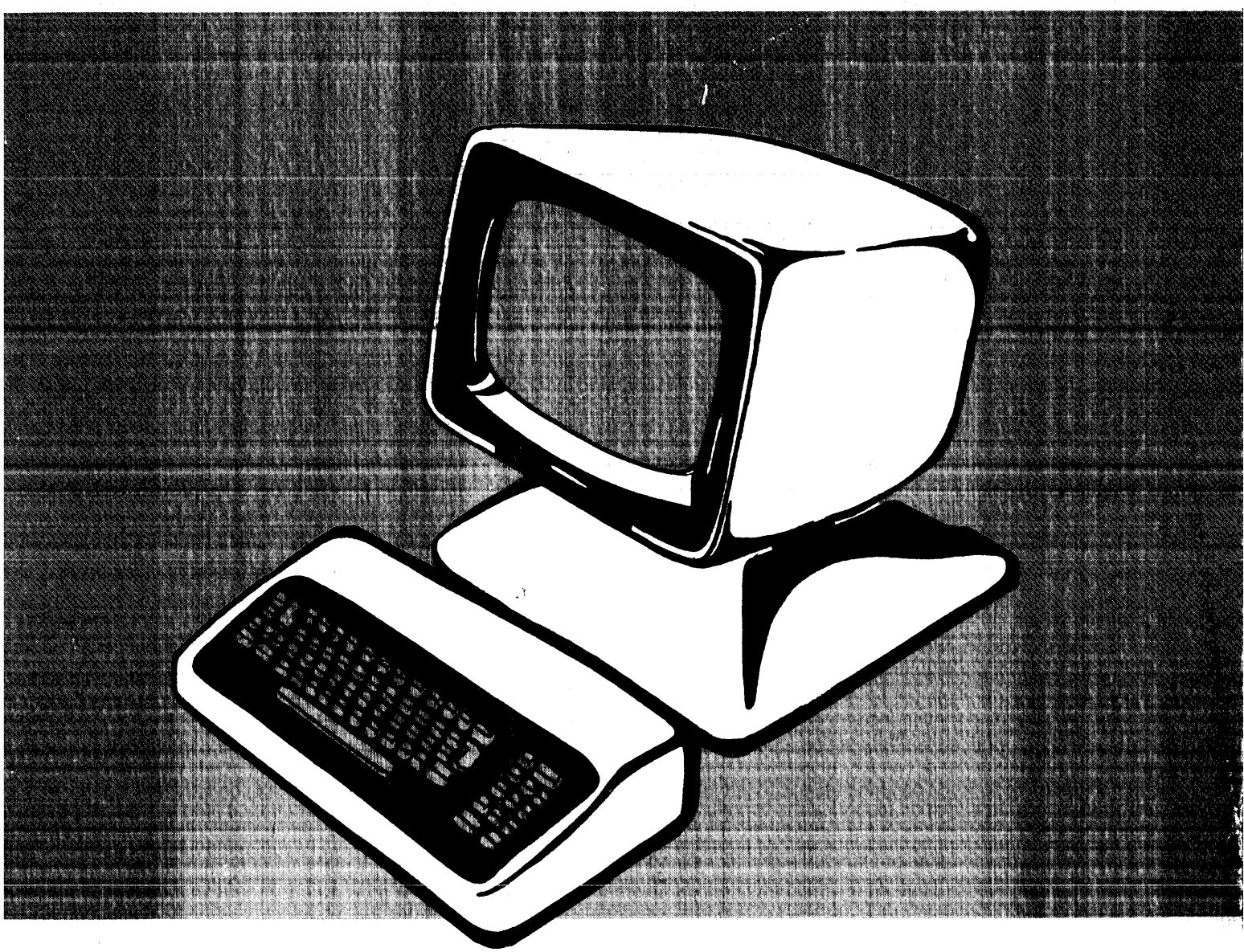
MOHAWK DATA SCIENCES

SERVICE DIVISION

VT3

Theory of Operation



TD-4102

Technical Manual

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VT3 Theory of Operation

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Hardware

PHYSICAL DESCRIPTION

The various components of the Qantel Video Terminal 3 reside within three separate enclosures: the display cabinet, the pedestal base, and the keyboard. Within the fully pivoting display cabinet are the Z-8Ø based control logic board and the CRT with its monitor board. The supporting pedestal base contains the PS-9, a standard linear power supply providing the DC voltages for VT3 operation. The keyboard, with interchangeable keytops to match different character sets, contains a single board featuring a small speaker (for the alarm). Three variations of character sets are available - domestic, Swedish, and Japanese. Other sets are planned for the future.

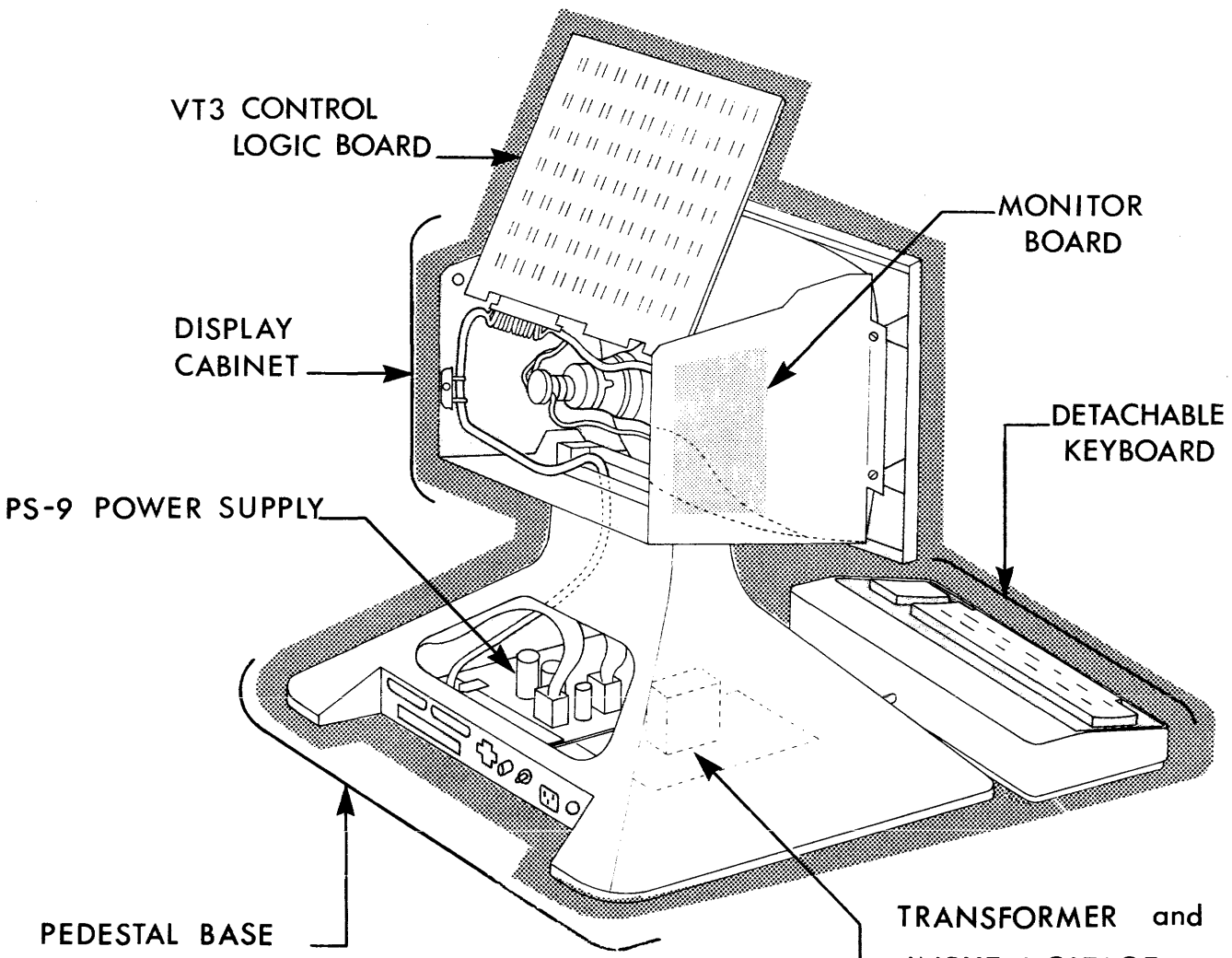


Fig. 1

Convection cooling is used in each of these enclosures to maintain normal operating temperatures.

External controls are minimal; the back of the pedestal features an on-off switch and brightness control. The J6 and J7 connectors, also on the back panel, permit system interfacing and daisy-chaining of additional VT3's. The AC power cable is detachable. The main power fuse, rated at 1 amp, 250 volts, is also located on this back panel.

Switch settings provided within the display cabinet condition the VT3 for variables in operation. The control logic board allows switch setting of asynchronous communication speeds ranging from 300 bps to 19,200 bps; 50 Hz or 60 Hz operation; individual VT3 address within the communication network; and initial display screen parameters (27 lines of 64 characters or 24 lines of 80 characters).

Input voltages can be matched to transformer capabilities by means of a ten-position terminal strip connecting with the primary windings of the transformer. Thus, operation is possible with input voltages of 100, 115, 215, 230, and 240 VAC.

A maximum of thirty-one VT3's may be configured off a single controller through direct connection, hub units, line drivers, and modems. The IOU-39Q performs the role of controller in conjunction with the VT3.

BLOCK DIAGRAM EXPLANATION

The block diagram illustrates the components of the control logic board in relation to the keyboard, the communications line, and the CRT. The basic operations, as dictated by the instructions in the Program ROM, are carried out by the Z-8Ø microprocessor. The Z-8Ø must continually update the Display RAM with character information derived from the keyboard and central processor. Each character space on the CRT display screen is represented by a memory location within the Display RAM. By actively monitoring the communications line through the UART (Universal Asynchronous Receiver-Transmitter), and the keyboard interface, and loading arriving characters into the RAM, the Z-8Ø is able to ensure the display screen presentation is current within the realm of system program activities.

The Z-8Ø microprocessor directs data on the 8-bit DB bus by selectively enabling the appropriate components upon the control logic board. The 16-bit AD (Address) bus carries this directional information to one of the following (depending on the address value):

- A decoder network which provides chip select signals to activate specific components.
- The address inputs of the Program ROM or Private Utility RAM.
- The Address circuitry for the Display RAM, tied into the CRT's video timing network through a Character Counter and Multiplexer.

The timing network is designed to allow the Z-8Ø access to the Display RAM during a brief period between individual character accessing by the scan circuitry. Access is available as well during the horizontal and vertical blanking periods.

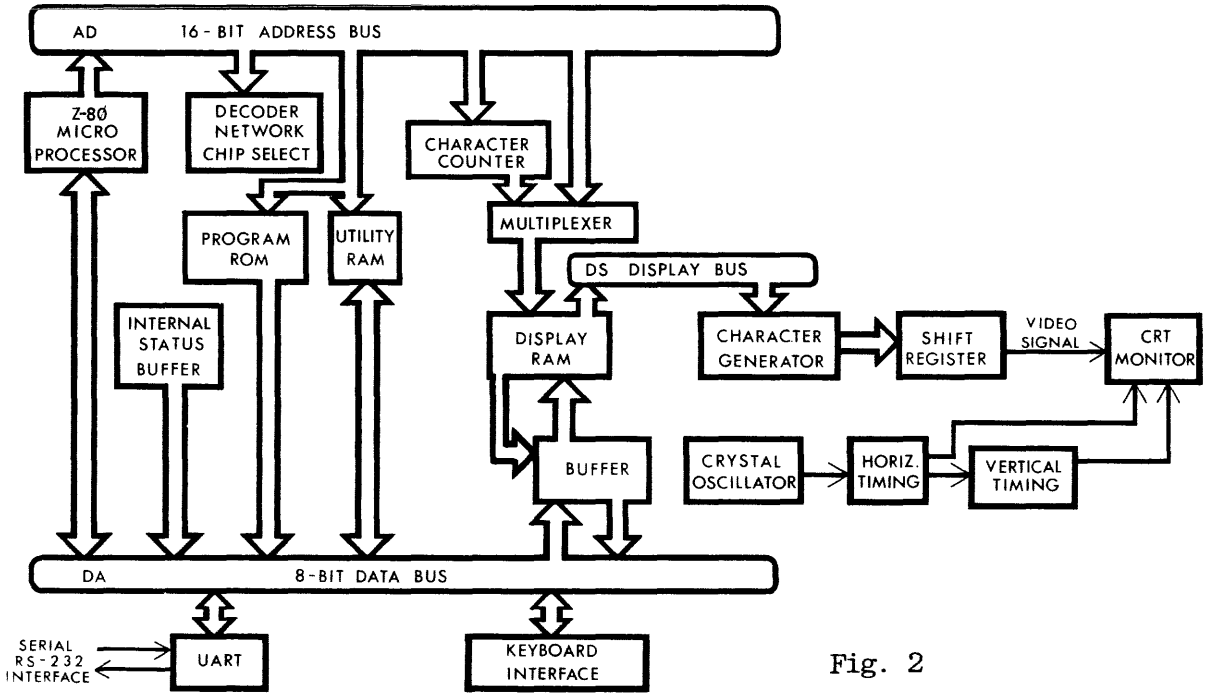


Fig. 2

Z-8Ø clock periods are regulated by a 4.0 Megahertz oscillator. This results in a 0.25 microsecond duration for each T-state.

The Decoder Network generates chip select signals based on information the Z-8Ø provides along the AD bus and certain control lines (MREQ, MONE, and IORQ). As illustrated on Sheet 7 of the logic drawings, two high-speed 1-of-8 Decoder chips handle selection of memory (CSAØ - CSA5) and selection of I/O ports (CSCØ - CSC7). The specific chip select information is presented in the Appendix of this manual.

The Program ROM contains 6K bytes of microcode used to structure the activities of the Z-8Ø in performing basic operations of the VT3. Three 2K by 8 bit memory chips are used, selected by chip selects CSAØ or CSA1 and address lines AD1Ø and AD11.

The Utility RAM acts as a storage area for the Z-8Ø for program variables and scratchpad space during various program sequences. It consists of four 1K by 4 bit memory chips accessed

in pairs for a total memory area of 2K by 8 bits.

The Internal Status Buffer is a tri-state buffer (7B seen on Sheet 1 of the logic drawings) which, when enabled, can supply the Z-8Ø with the following information: selected VT3 address as represented by jumpers J8 through J12; presence of the DRV+ signal and ODDCT+, both indicative of key aspects of video timing; and the 60HZ signal, showing the condition of jumper J14 - the 50 or 60 Hz switch.

The Character Counter supplies the address to the Display RAM for accessing a particular location, akin to a position on the CRT display screen. Consisting of three 4-bit presettable counters, the Character Counter is loaded by the Z-8Ø with the appropriate address to start each row. The counter is incremented throughout the horizontal scan automatically. The Z-8Ø may bypass addressing the Display RAM through the Character Counter, addressing instead directly through the Multiplexer. When a specific signal is present as a result of timing considerations (SMEN-), the Z-8Ø can use this mode of addressing.

The Multiplexer, three Quad 2-Input Data Selector/Multiplexer chips, feeds the inputs to the Display RAM chips with addresses from either the Character Counter or directly off the Z-8Ø's AD bus.

The Display RAM consists of four 1K x 4 bit memory chips accessed in pairs to create a 2K by 8 bit display memory. Characters encoded in ASCII values are stored in locations to represent a one-to-one relationship with the CRT display screen. A timing signal releases accessed characters to the

DS bus (Display Bus) where the ASCII value is applied to a Character ROM to produce the correct dot matrix pattern. A pair of octal latches, one for input and the other for output, act as a buffer between the Display RAM and the DA bus.

The Character Generator, 16K of ROM, receives the 8-bit ASCII value from the DS bus and produces a portion of the dot pattern, one slice of the matrix, based on the horizontal scan row information received from a line counter. The line counter consists of a Dual-D flip-flop and 4-Bit Synchronous Counter that maintains count of the slice of a particular character being produced, one row of a possible fifteen. During the course of each horizontal scan row, eight slices of a character are assembled (all even or all odd lines). The interlaced scan returns after finishing the rest of the frame and inserts the slices that were missed the first time.

The Shift Register (Parallel In - Serial Out/Serial In - Serial Out 8-Bit Shift Register) accepts a parallel byte from the Character Generator and shifts it out serially to form the video signal sent directly to the CRT. A LOAD+ signal generated as a part of the horizontal timing controls the rate of the video signal.

The Horizontal and Vertical Timing circuitry is based on the clock signal sent from an 11.25 MHz oscillator. The resulting signals are used to control access of the Display RAM, clock the shift register, produce specific interrupts to the Z-8Ø, create the horizontal and vertical inputs to the video monitor board, produce the blanking signals, and generate the odd-even interlace flag.

BLOCK DIAGRAM EXPLANATION CONTINUED

The Keyboard Interface allows the Z-8Ø through a tri-state buffer to receive incoming strobe signals from the keyboard, detect the New Key Pressed flag, and receive serial bits from the keyboard on the DKEY+ data line. Incoming data bits are clocked by the Z-8Ø sending out the signal CLOCK+ to the keyboard. The Z-8Ø may also sound the alarm, the keyboard audio signal, by setting the Alarm Latch.

The UART (Universal Asynchronous Receiver-Transmitter) provides the link to the RS-232 serial communication line, directly interfacing the UART of the managing IOU-39Q controller. The Z-8Ø monitors the state of the UART to detect the Data Ready condition (indicating incoming data) or Transmit Holding Register Empty (allowing the Z-8Ø to transmit data).

EXPLANATION OF THE LOGIC DRAWINGS - SHEET 1
MICROPROCESSOR AND INPUT PORTS

In the upper lefthand corner of Sheet 1, the IC chip 6C, a 4.00 MHz clock oscillator, provides the Z-8Ø with a square-wave clock input resulting in a basic T-state period of 0.25 microseconds. The diode-clamped driver network provides edge-shaping and voltage control for the clock signal to meet Z-8Ø requirements (necessary at higher frequency operation). The 4 MHz signal also is routed to a timing network to control the UART's baud rate.

The RC network located at A8 on the sheet remains low for 50 microseconds after power up to reset the Z-8Ø microprocessor and the UART.

The connector P2, shown at the far left and right of the sheet, allows access to the Z-8Ø control, data, and address lines through test panel interface.

The Z-8Ø, operating according to the microprogram stored in the 6K ROM, must coordinate tasks on two levels. Data and control characters must be received and properly channeled as they arrive from the UART and the keyboard. The functions required to accomplish this may be thought of as a foreground operation. Also, the display screen must be continually refreshed. The Z-8Ø performs this as a background level task by generating addresses and timing control signals at regular intervals.

MICROPROCESSOR AND INPUT PORTS CONTINUED

The Interrupt line (INT-) is used to notify the Z-8Ø of the conclusion of a horizontal scan, vertical scan, or act as a prompt for the Z-8Ø to check communications line activity through the UART. The method by which these interrupts are generated is discussed further on the sheets on which they originate (see Sheets 4 and 5).

The WAIT line when activated produces a condition within the Z-8Ø suspending all operations until the line goes inactive. WAIT in this case is used to prevent the Z-8Ø from accessing the Display RAM during certain periods of the memory access cycle.

The 8-bit Data Bus, DAØ through DA7, links the Z-8Ø to the significant components of the control logic board. Refer to the block diagram on page I-4 for an overview of which components are interfaced.

Tri-state buffer 7B is used by the Z-8Ø by activating Chip Select CSC5 to obtain the following information. DRV+ (the Vertical Drive signal) when absent indicates the presence of the vertical blanking period. ODDCT+, a product of the vertical timing network, differentiates between the odd and even scan as dictated by the interlace pattern. 60Hz- denotes the presence of jumper J14, necessary for operation with 60Hz power input. (Jumper J14 removed conditions the timing for 50Hz operation.)

Jumpers J8-J12 are used to select the address for the video terminal within a terminal network. The address $1F may not be used as it is reserved for broadcast messages (to all terminals simultaneously). The Z-8Ø thus derives the terminal identity by reading the state of these jumpers.

Tri-state buffer 7A allows the Z-8Ø upon sensing an Interrupt to determine the nature of the Interrupt (Scan Interrupt or Timer Interrupt). The Z-8Ø reacts to its INT line being pulled by issuing active IORQ and MI. These signals ANDed create INTAK (Interrupt Acknowledge) which clocks Buffer 7A, loading restart vector at its inputs. This restart vector will be an $FF if the signal INTS+ is present (a timing indication that a Scan Interrupt is occuring). The absence of INTS+ result in $CF, denoting a Timer Interrupt.

EXPLANATION OF THE LOGIC DRAWINGS - SHEET 2
PROGRAM ROM AND UTILITY RAM

Three 2716 programmable read only memory chips store the microprogram for the Z-8Ø, providing a maximum of 6K bytes (by 8-bit) storage area. Address lines ADØ through AD1Ø from the Z-8Ø interface the address inputs of the chips.

AD11 in combination with chip select signals CSAØ and CSA1 select the individual IC for the chosen portion of memory. CSAØ, when AD11 is low, selects IC 11A. IC 12A is accessed when AD11 is high at the same time as CSAØ. This covers memory addresses $ØØØØ through $ØFFF. CSA1 in combination with a low AD11 selects 1C 13A. This begins memory addressing at $1ØØØ. Although only 6K of ROM is currently used, space is allotted so that the addition of another memory IC would expand addressing through $1FFF. The decoding that produces CSAØ and CSA1 can be seen on Sheet 7 of the logic drawings.

Microinstructions are drawn from ROM (via the 8-bit DA bus) during an instruction fetch cycle preceding each Z-8Ø operation. The microprogram as executed by the Z-8Ø is examined in the Operational Description segment of this manual.

The four 2114 random access memory chips shown on the right half of the sheet represent the Utility RAM. Each memory IC has a capacity of 1Kx4 bits; they are accessed in pairs to produce a total RAM storage area of 2K by 8 bits. Pins 11, 12, 13, 14 offer bidirectional data inputs and outputs, interfacing with the DA bus.

The signal CSA4 selects RAM chips 11B and 12B. CSA5 selects 10B and 13B. Pin 10 acts as the Write Enable, activated by the Z-8Ø (by the signal WR) whenever data is to be loaded into the RAM. Each chip select signal provides 1K (1024 bytes) of

storage area; CSA4 from $4ØØØ to $43FF and CSA5 from $5ØØØ to $53FF.

The Utility RAM allows the Z-8Ø a "scratchpad" area to manipulate program variables, maintain flags, keep track of counts during transfer operations, and provide buffer space for transmit and receive handling. Qantel document #L30786, the microcode listing, describes labels associated with the various Utility RAM addresses.

EXPLANATION OF THE LOGIC DRAWINGS - SHEET 3
ADDRESS COUNTER, MUX, and DISPLAY RAM

The Display RAM stores characters in a one-to-one ratio corresponding with the characters to appear on the video screen. The scan logic circuitry accesses these characters in a manner synchronized to the horizontal and vertical timing signals; the Z-8Ø need only intervene to provide a starting address at the advent of each horizontal scan row. The character information in the Display RAM is updated by the Z-8Ø during "window periods", times when the scan logic is not actively accessing Display RAM or during free time at horizontal or vertical retrace intervals.

LOAD+, a signal originating in the horizontal timing network, acts as a clock for IC 1ØF, an Octal D flip-flop, storing the data outputs of the Display RAM in preparation for sending the character data out on the Display Bus to be converted to an appropriate dot pattern on the screen. LOAD+ will vary in frequency (see Sheet 4) depending on whether a 64 or 80 character line is being employed. This coordinates character generation with the fixed time of the electron beam scan across the screen to accomodate the number of characters per line.

The Address Counter consists of three 74LS193 chips, asynchronously parallel-loading 4-bit up-down counters. Timing hardware generates a maskable interrupt before each horizontal or vertical retrace. Within the microcode, the scan interrupt routine accesses a table to acquire an address which is parallel-loaded into the counters. CSA3-, a signal produced by decoding address lines AD12+, AD13+, AD14+, and AD15+, is generated whenever the Z-8Ø produces an address between $3ØØØ to $37FF or $38ØØ (to create a blank scan row) and triggers the parallel-loading. Note that outputting $38ØØ on the address lines results in $ØØØ being loaded into the counters. Actual Display

ADDRESS COUNTER, MUX and DISPLAY RAM CONTINUED

RAM addresses range between $2ØØØ and $27FF. Once the 4-bit counters are loaded, they increment automatically, clocked by the LOAD- signal, thus stepping through each address of the horizontal row a character at a time. BLANK+, present during blanking intervals, inhibits clocking at AND-gate 7D.

The signal SMEN-, Scan Memory Enable, controls the Select pin of multiplexers 13D, 12D and 11D. This determines whether addressing to the Display RAM will be gated through directly off the Address lines or through the 4-bit counters. When SMEN- is active (low), during execution of scan logic, the Address Counter outputs are gated through. SMEN- going true allows the Z-8Ø to directly address any location in the Display RAM.

The Z-8Ø directly addressing the Display RAM, using addresses $2ØØØ to $27FF, creates the decoded signal CSA2-. CSA2- sets a flip-flop (5D) in the horizontal timing network to activate the WAIT line to the Z-8Ø (synchronizing the slow RAM memory inputs to the faster Z-8Ø). WRE+ is then produced by horizontal timing. WRE+ and SMEN- dictate the period of the "window" during which the Z-8Ø can write to the RAM. At the same time CSA2- combined with WR- (from the Z-8Ø) are ANDed to latch data from the DA bus into Octal Latch 13F. The output is enabled through this latch to the Display RAM (by pin 1 - the output enable - pulled active by the WRE+ signal). A READ of the Display RAM can be accomplished in similar fashion by the Z-8Ø activating the RD- line rather than WR-, thus enabling Octal Latch 12F, gating Display RAM output lines to the DA bus for reading by the Z-8Ø.

EXPLANATION OF THE LOGIC DRAWINGS - SHEET 4
HORIZONTAL TIMING

All video operation depends on the synchronizing of a dot pattern, produced by the character generator network, with the movement of an electron beam across the face of the video monitor. Thus, the horizontal timing must not only send out a horizontal drive signal to the video monitor and a similarly derived vertical drive signal; but must tell the control logic hardware when characters are to be loaded, what the dot clock rate should be, when Scan and Timer Interrupts should occur, when the Z-8Ø is clear to load new data into the Display RAM without interfering with Scan Logic, and where blanking periods should take place.

The scanning rate of the video screen electron beam is constant for a given input voltage to the VT3. Obviously, if 80 characters are going to be compressed into a horizontal row rather than 64 characters, the dot clock must operate at a faster frequency and the LOAD+ signal, which draws characters out of Display RAM, must be faster. This is the purpose of flip-flop 3F - to select one of two crystal oscillators to regulate timing of these factors.

The Z-8Ø activates CSCØ by performing an I/O function to I/O Port $8Ø. Outputting DA4+ high, when CSCØ clocks sets flip-flop 3F. The Q output will thus be high allowing AND-gate 1F to channel the upper crystal oscillator output (1E) through to the horizontal timing network. The CLST (dot clock) will, therefore, become 11.25 MHz. The Q output also goes to 74LS161, a parallel-loading 4-bit counter, presetting it to $C. This adapts the rest of the timing chain to the requirements of a 64 character per line screen format.

HORIZONTAL TIMING CONTINUED

TINT- and SINT- are routed to the clock inputs of two flip-flops seen on Sheet 5, used to regulate the intervals that the Timer Interrupt and the Scan Interrrupt occur. TINT- is generated every 32 microseconds, but the actual Interrupt to the Z-8Ø occurs less frequently as controlled by the data input pin 2 of flip-flop 2C (see Sheet 5). SINT- invariably results in an Interrupt to the Z-8Ø each 64 microseconds (the data input at pin 12 of 2C is held low).

CTH+ (Count Horizontal) produces a positive-going pulse for each horizontal raster row (15.625 KHz) and provides the primary clock for the vertical timing chain.

The BLH- (Horizontal Blanking) and DRH+ (Horizontal Drive) signals are created by 4-bit counter 2F. As the pin 15 carry-out of counter 4F goes low, counter 2F is clocked. When counter 2E carry out is active, counter 2F is preset to $8, counts to $F causing the carry-out at pin 15 to load a preset value of $4. By a count of $5, CTH+ goes inactive and disables counter 2F. Horizontal Blanking (BLH-) occurs at pin 12, Horizontal Drive at pin 11. See the timing chart, figure , for details.

If an 80 character per line format is selected, by the Z-8Ø pulling DA4+ low with CSCØ, the bottom oscillator, 1D, is channeled through AND-gate 1F. The dot clock in this case becomes 14.0625 MHz. LOAD+ occurs at a faster rate and counter 4F is preset with a $B, thus changing the timing relationship of the rest of the chain to ensure that BLH-, DRH+, and CTH+ are the same as with 64 C.P.L. format.

HORIZONTAL TIMING CONTINUED

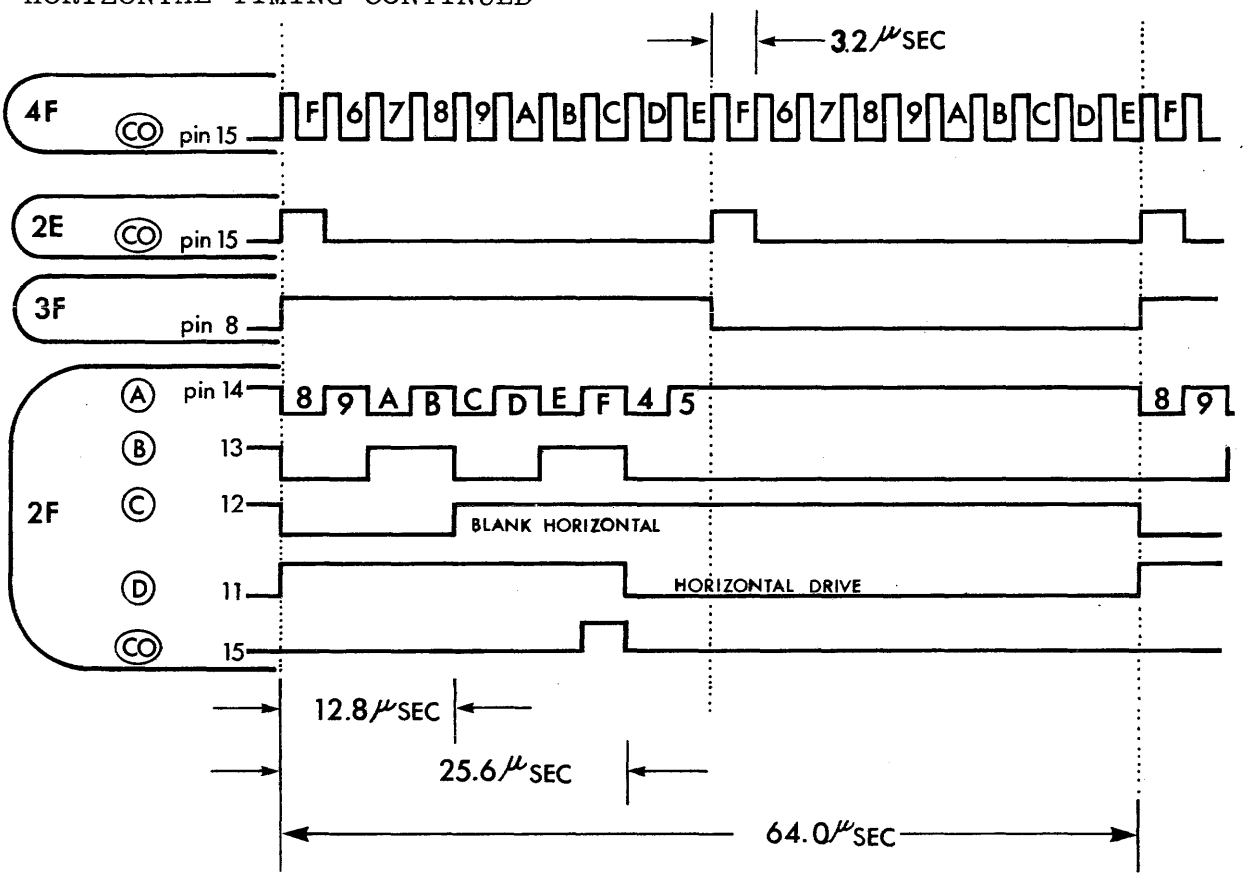
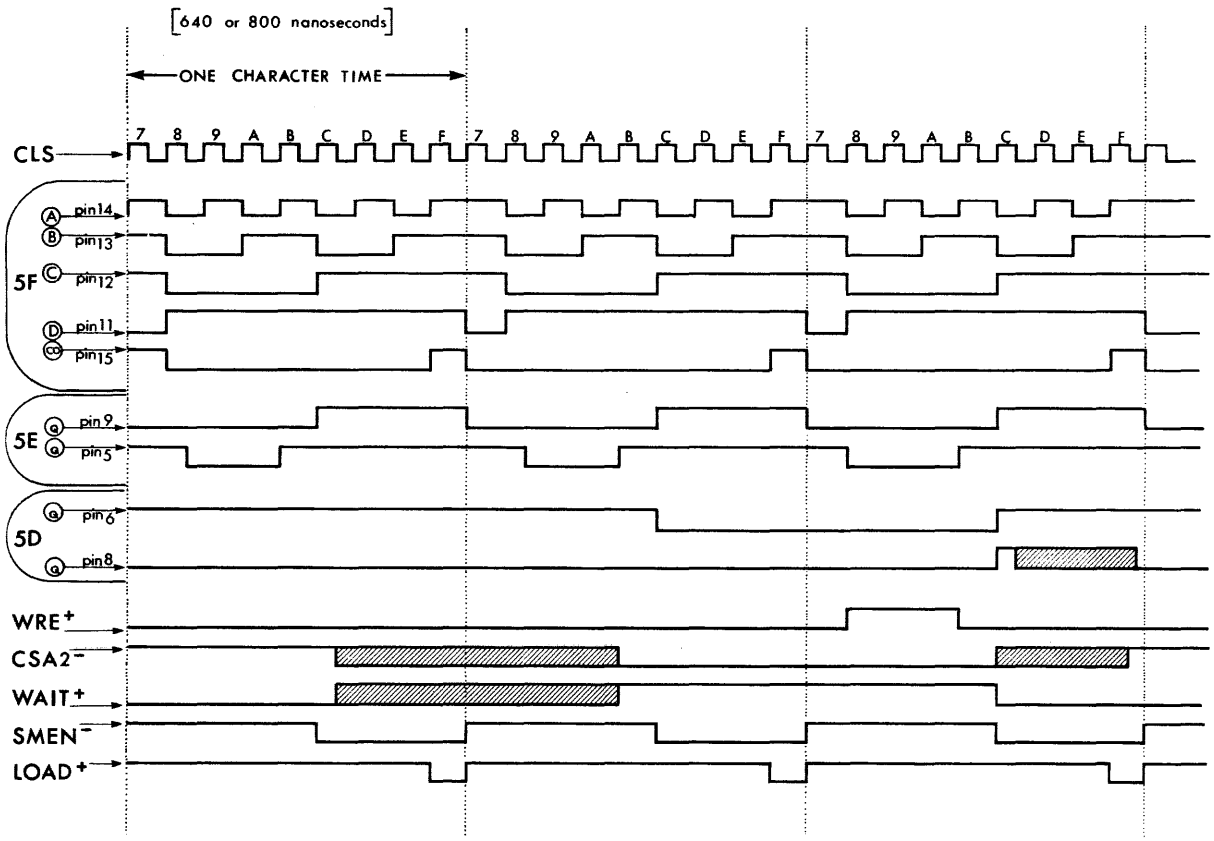


Fig. 3 **HORIZONTAL TIMING**

CSA2-, seen at the top of the sheet, is activated whenever the Z-8Ø tries to access address $2ØØØ through $27FF (the Display RAM). The factors allowing the Z-8Ø to access the Display RAM are as follows.

SMEN- must be inactive - the output of flip-flop 5E pin 8 high. WAIT+ is set in response to CSA2- and flip-flop 5D pin 8 going low as that flip-flop is set. WAIT+ being active removes the reset to Pin 1 of flip-flop 5D which then can set at a positive clock from 5E pin 9. The ANDing of 5D pin 6 and 5E pin 5 produces the WRE+ signal. WRE+ routes data into (or out of) the Display RAM through the appropriate Octal Latch to the address

multiplexed off the Address lines (as permitted by SMEN- high). Pin 6 of flip-flop 5D will go high as the timing chain continues, thus clocking 5D pin 8 to a reset condition. The resulting high from pin 8 removes the WAIT+ condition to the Z-8Ø. CSA2- will be dropped, once again setting flip-flop 5D pin 9.



HORIZONTAL TIMING

Fig. 4

EXPLANATION OF THE LOGIC DRAWINGS - SHEET 5
VERTICAL TIMING AND INTERRUPT CONTROL

The signal CTH+, derived from the horizontal timing chain and oscillating at 15,625 Hertz, is the basis for all vertical timing chain activity. CTH+ clocks the 4-bit counter 4E. The value preset into 4E is dependent on the state of jumper J14, the 50 or 60 Hz select, seen in the upper left of the sheet. The IL- (Initial Load) signal is also a component of the preset to 4E, occurring once for the first horizontal scan frame.

Notice that the signal 60Hz is accessible to the Z-8Ø (see Sheet 1) through Tri-State Buffer 7B.

Thus, the three primary elements of the vertical timing network, 4-bit counters 4D and 4E, and flip-flop 6F, tailor the vertical drive signal to the monitor, DRV+, by counting a specific number of horizontal scans to fit within the frame rate. With 60Hz selected (the timer counts 59.98 Hz at this rate), 260.5 horizontal scans appear per 1 frame. At 50Hz, 312.5 horizontal scans appear per frame. The vertical timing diagram, figure 5 , illustrates the relationship of these signals.

ODDCT- (Odd Count) is produced to mark the sequence of the interface pattern sent to the video screen. A complete frame requires two complete Vertical Drives, one to display the even horizontal scan rows; one to display the odd. ODDCT- is directed to the slice counter, 4-bit counter 9E on Sheet 6, and becomes a part of the address to the Character ROM to select an odd or an even slice. The reciprocal of this signal, ODDCT+, is sent to Tri-State Buffer 7B (seen on Sheet 1) to cue the Z-8Ø to whether an odd or an even scan is in progress.

VERTICAL TIMING AND INTERRUPT CONTROL CONTINUED

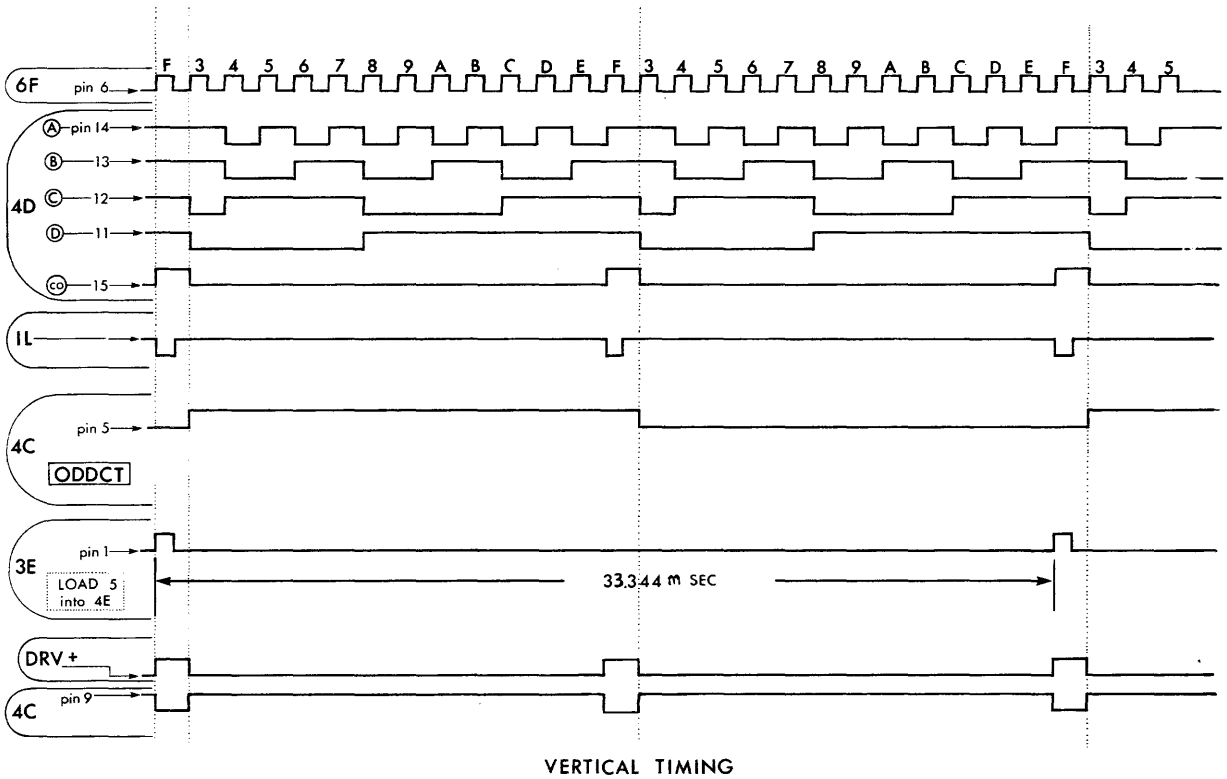
The signals BLANK+ and BLANK- are created to inhibit the video output to the monitor during horizontal retrace or vertical retrace periods. Notice that BLH- (Blanking Horizontal) and the complement to the Drive Vertical signal (4C pin 9) are ORed at 3C to ensure the video is inhibited in both instances. BLANK+ is routed to the Scan RAM Address Counter to prevent counting during blanking periods. BLANK- is sent to the Character Generator network (Sheet 6) as the actual video inhibit signal.

At periodic intervals in the timing cycle, two maskable interrupts to the Z-8Ø occur. Flip-flop 2C regulates the incidence and the nature (timer or scan interrupt) of these interrupts.

The Scan Interrupt has a higher priority - the Z-8Ø must be notified at the end of each horizontal scan to load an address for the next scan row. A Scan Interrupt occurs every 64 microseconds - before each horizontal and vertical retrace. SINT- (Scan Interrupt) from the horizontal timing network or the Vertical Drive Flip-flop (4C pin 9) clock 2C pin 9 low to generate the signal INTSD+ to the Z-8Ø, which simultaneously sets 2C pin 8 high identifying it as a Scan Interrupt.

A Timer Interrupt occurs less frequently, roughly every 256 microseconds, and is a cue for the Z-8Ø to check the UART for transmit or receive activity. Z-8Ø Interrupts are enabled as soon as a Timer Interrupt is recognized to allow the higher priority Scan Interrupt to take place if necessary. The clock for Timer Interrupt also comes from Horizontal Timing at the rate of once per 32 microseconds. However, notice the origin of the data input, 2C pin 2. The signal CTH- and the B output of counter 4E are ANDed at 3C. Since 4E counts

intervals which vary according to its preset value, the data input 2C pin 2 will be active at varying intervals ranging from 64 to 320 microseconds. Identity of a Timer Interrupt is based on the fact 2C pin 8 will be low. The Z-8Ø responds to its Interrupt line being pulled by checking Tri-State Buffer 7B. The INTS+ line will create a value of $FF for Scan Interrupt; $CF for a Timer Interrupt. The Z-8Ø issues INTAK to read the buffer; the inversion of this signal sets both sides of 2C, clearing INTSD+.



VERTICAL TIMING

Fig. 5

EXPLANATION OF THE LOGIC DRAWINGS - SHEET 6
CHARACTER GENERATOR AND CRT INTERFACE

The ASCII values from the Display RAM are converted to dot patterns synchronized with the horizontal and vertical timing signals. The Character ROM, 9F, receives the ASCII value on the Display Bus and raster row orientation from the Slice Counter 9E. The resulting 8-bit "slice" of visual character information is loaded into a shift register in parallel form, and shifted out serially at the Dot Clock rate. The ninth bit of the slice comes from the DS pin input (pin 1).

To maintain a valid raster row address, Slice Counter 9E receives the signals DRV+ (Vertical Drive), ODDCT- (Odd Count), and DRH+ (Horizontal Drive). The Slice Counter is preset to 1 initially, but the outputs are wired to the Character ROM address inputs in a manner to simulate counting by two's.

DRV+ clocks the value of ODDCT- into flip-flop 4E, thus resulting in an $8 being loaded into counter 9E for the first scan of every other frame. The Slice Counter appears to count by two's because of the configuration of its outputs with the Character ROM address inputs. 9E pin 11 (D output) connects with the low order ROM address input. Pins 14, 13, 12 (A, B, C) of 9E connect with the next significant address inputs. This causes the interlacing of the alternate line to occur. With a $1 preset into it, the Slice Counter will present a '2' to the address inputs. The next horizontal slice, triggered by DRH+, clocks the Slice Counter to '4'. Counting continues... 6, 8, A, C, E ... until the completion of one character row triggers the loading of a '2' to start a fresh character row. With flip-flop 8E changing with the next DRV+ clock, the Slice Counter receives an '8' preset value and proceeds to count the odd lines... 1, 3, 5, 7, 9, B, D, F of each character row.

Shift register 8F loads an 8-bit parallel "dot pattern" each time it receives a LOAD+ signal from the horizontal timing network. Additionally, the bit in the eighth position is serially loaded into pin 1, the DS input, where it becomes the first bit in the stream to be serially clocked out. Thus, dots in the first and ninth position of each character slice will be identically displayed.

Two signals ORed provide the data input to the Inverse Video Flip-Flop. DS7+, the uppermost bit of the character information word, is one of these signals. The other is derived from the A, B, and C outputs of the Slice Counter, ANDed at 2D so that a count of 14 or 15 produces the active low output. The inverse video function is a result of a high 'not Q' output from 8E applied to exclusive-OR gate 7F. This effectively inverts the video signal, turning highs to lows and lows to highs.

The CRT's video brightness is adjusted by R24, the potentiometer at the rear of the pedestal base.

Flip-flop 6F is set by the Z-8Ø accessing memory location $38XX (creating the decoded CSA3+ clock and making data input AD11+ high). This flip-flop controls blanking, a low from pin 8 inhibits all video signals to the monitor. The signal BLANK- from the Vertical Timing network also inhibits the video during horizontal and vertical retrace times.

Junction P1 illustrates the interface with the video monitor circuitry. The monitor converts the DRHC+ and DRVC- signals into sawtooth waves driving the yokes to regulate the motion of the CRT's electron beam. The video signal determines

which dot positions will be illuminated during scanning to produce the displayed characters and graphics.

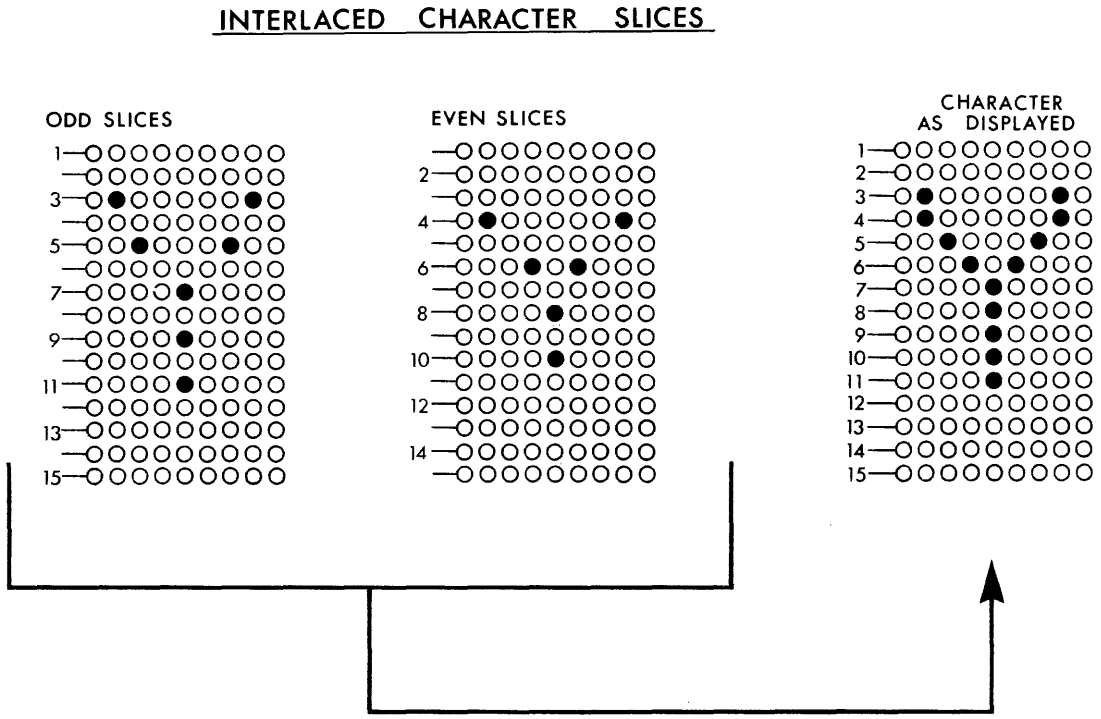


Fig. 6

EXPLANATION OF THE LOGIC DRAWINGS - SHEET 7
BAUD RATE GENERATOR AND UART

The UART (Universal Asynchronous Receiver-Transmitter) links the VT3 to the serial communications line, interfacing an IOU-39Q controller which contains an identical UART at its communication line junction. At turn on, the RESET+ pulse activates the UART's Master Reset. The microprogram then dictates the parameters of UART operation by sending out a control word selecting number of data bits and type of parity to be used.

It is through the UART that the Z-8Ø becomes aware of communication line activity. By issuing an IN9Ø Input/Output instruction, the Z-8Ø receives the contents of the UART's status register. Information conveyed includes presence of data in the Receive Register (Service Request), Transmit Holding Register cleared (Ready for Transmitting Data), Transmit Register empty (Data Transmitted), Clear to Send, and error notification. See the Appendix for the actual bit map of this status word. An IN9Ø also cues the Z-8Ø to the state of the 64 / 80 character per line jumper (J13) by enabling the buffer 5A on Sheet 8.

The baud rate is selectable through the group of jumpers J1 - J7 in the lower left portion of the sheet. The 4MHz clock signal channelled into 4-bit counter 6D's clock input produces a Pin 15 Carryout frequency of 307.7 KHz. Since the UART clock input responds with one receiver shift pulse for every 16 received cycles, this corresponds to a baud rate of 19.2K. For lower baud rates, the selection of J2 - J7 connects the outputs of 12-bit ripple counter 7C to the UART's clock input.

Within the B8 grid on the sheet, the interface with the

communication lines at connector P1 is shown. Incoming data at RS-232-C levels (+12, -12 volts) is translated to TTL levels (+5, 0 volts) by the circuit surrounding comparator 2B. The data is then serially shifted into the UART's Receive Register utilizing the predetermined format of stop bits, character length, parity, and baud rate. Data being transmitted out the UART's Transmit Register undergoes the reverse of this operation. TTL levels from Pin 25 of the UART are translated to RS-232-C levels by the comparator circuit and channelled to the communication line through Pin 9 of connector P1.

The Appendix contains a list of pin descriptions further detailing UART operation.

Two octal decoders, 9C and 10C, using 8 address lines and 4 Z-8Ø control lines, create the chip select signals to steer addresses and data to proper destinations on the control logic board. The following diagram details the nature of the chip selects. Note that Decoder 10C is used for memory decoding; Decoder 9C is used for input/output decoding.

EXPLANATION OF THE LOGIC DRAWINGS - SHEET 8
KEYBOARD INTERFACE AND DC VOLTAGE

The Tri-State Buffer 5A has two individual sections consisting of four input-outputs. By activating one of the two chip selects, the Z-8Ø accesses the desired lines obtaining information about keyboard activities (CSC6-) or status of the UART (CSC1-).

The top portion of the buffer, as illustrated, allows the Z-8Ø to read the New Key Pressed Latch (3A), the STROBE+ signal, and the DKEY+ line where character information bits are clocked in from the keyboard. STROBE+ becomes active whenever the operator depresses a key. This signal also clocks in the tied-low data line (Pin 2) of Flip-flop 3A, the New Key Pressed Latch. Pin 6 of this flip-flop is tied around to the input of buffer 5A for reading by the Z-8Ø.

Repeat keys are detected when STROBE+ and the New Key Pressed Latch remain active beyond a specified time. The Z-8Ø will, in such an instance, enter the keyboard repeat routine.

Character information bits are clocked in the DKEY+ line by the Z-8Ø toggling the Clock Latch 4A. Pin 11 is clocked by CSC7- while the Data input, Pin 12, is varied by the Z-8Ø manipulating DA7+ (seen at 1A on the sheet).

Flip-flop 4A also contains the elements of the ALARM latch. CSC7- provides the clock to pin 3 while DA5+ provides the Data input to Pin 2. With ALARM activated, a 3.5 KHz signal is generated on the keyboard circuit board to sound the audio speaker. The ALARM latch is reset by the Z-8Ø microprogram after approximately ¼ of a second, stopping the speaker tone.

The Z-8Ø notifies the controller of data ready to be transmitted over the communication line by setting Request to Send to the modem. Chip select CSC4- clocks pin 11 of Flip-flop 3A while DA1+ is high to accomplish this. A driver network converts the TTL output of 3A to RS-232-C levels.

The bottom third of the sheet illustrates the diode isolated +15 volt and -12 volt levels which connect with the external terminator shoe. The +5V and Ground connections between P1 and P2 are also illustrated.

EXPLANATION OF THE LOGIC DRAWINGS - Sheet 9
SIGNAL AND DC POWER DISTRIBUTION

The logic control board fingers at P1 plug into junction J1 illustrated at the left hand side of Sheet 9. The interconnections between elements of the VT-3 are shown on this page.

EXPLANATION OF THE LOGIC DRAWINGS - Sheet 10
TRANSFORMER AND WIRING DIAGRAMS

Sheet 10 illustrates the AC power input as fed to the transformer terminal strip. To accomodate the various possible input voltages (100, 115, 215, 230, 240), the jumper wires to the terminal strip must be placed according to the table on the sheet.

PS-9 POWER SUPPLY

The PS-9 functions as a normal, linear power supply within the VT3, providing three DC outputs: +5 volts (3.0 amps); +15 volts (1.5 amps); and -12 volts (.05 amps). Physically, it consists of a printed circuit board and a transformer, both residing within the pedestal base of the VT3.

Input voltages are variable and selected through connections made to the terminal strip of the transformer. Refer to Sheet 10 of the Logic Drawings for configuration of the winding points. Operation is regulated at the expressed voltages between 47 and 63 Hz.

Output voltages are variable by altering the value of the adjustment resistor corresponding to the specific DC output. Outputs when tested should comply to the following parameters.

	Minimum	Maximum	Adjusted by
+5V	4.75.....	5.25	R11
+15V	14.85.....	15.15	R6
-12V	-10.8	-13.2	Fixed

Specific procedures for selecting resistor values are detailed in Qantel Document #A30903.

Overvoltage protection is provided on the +5 VDC output, dropping the voltage output to Ø V if the value reaches 5.8 VDC. Each output line is equipped with current protection -- the +5V and +15V to 120% of full load; the -12V to 400% of full load.

Pin designations for J3 and J4 follow.

PS-9 POWER SUPPLY CONTINUED

Signal	Color	Pin
16V SEC	Yellow	4
16V SEC	Yellow	6
16V Center Tap	Yellow/ White	3
34V SEC	Gray	5
34V SEC	Gray	2
34V Center Tap	Gray/ White	1

Signal	Pin
+5VDC	1
+5VDC	2
+5VDC	3
GND	4
GND	5
GND	6
+15VDC	8
+15VDC	9
-12VDC	12

VT3 DOCUMENTS

A30694	IOU-39 Design Specification
A30730	IOU-39Q Design Specification
A30786	VT3 Functional Specification
A30809	PS-9 Design Specification
A30822	Qantel Standard Protocol
A30880	VT3/QSP Driver Specification
A30901	Character Set Dot Matrix: ASCII
A30902	Character Set Dot Matrix: Kana
A30903	PS-9 Test Procedures/Theory of Operation
A30917	Character Set Dot Matrix: Swedish
A30935	IOU-39Q Cabling
A31022	VT3 Test Procedures
A31023	VT3 Control Logic
D30785	VT3 Logic Drawings
D30807	PS-9 Logic Drawings
F30730	IOU-39Q Functional Specifications
F30786	VT3 Firmware
L30730	IOU-39Q Microcode Listing
L30786	VT3 Microcode Listing

IC LISTING FOR THE VT3

1863B.....Universal Asynchronous Receiver-Transmitter

2114-2.....1K X 4 bit RAM

2716-1.....16K Erasable Programmable Read-Only Memory

4040.....12-Bit Ripple Counter

74LSØØ.....2-Input NAND gate

74LSØ2.....2-Input NOR gate

7426.....2-Input NAND gate, open collector

74LS74.....Dual-D Flip-Flop

74LS138.....Octal Decoder

74LS158.....Quad 2-Input Data Selector/Multiplexer

74LS161.....4-Bit Synchronous Counter

74LS166.....PI-SO/ SI-SO, 8-Bit Shift Register

74LS193.....Presettable 4-Bit Binary Up/Down Counter

74LS244.....Octal Bus Buffer, Non-Inverting Tri-State

74LS273.....Octal D-Type Flip-Flop

74LS373.....Octal Latch with Tri-State Output

CM2000.....Crystal Oscillator

Z-8ØA.....Microprocessor

Operational Description

DISPLAY SCREEN

The character sets, English and KANA, illustrated in the Appendix demonstrate the range of VT3's display capabilities. Most of these characters are available to the keyboard operator; however, the graphic symbols (shown as $1Ø through 1F) may be entered only through a Write from the main CPU.

The actual display presented on the CRT is subject to a number of variables. Display format, field parameters, cursor position, transmit marks, data display, and other elements are structured in ways discussed in the following section.

The aspect ratio of the display screen, the number of lines by the number of characters per line, varies according to two considerations. A jumper switch, J13, sets screen format at turn-on or reset to 27 lines by 64 characters (1728 display characters) or 24 lines by 80 characters (1920 display characters). This switch-selected format may be changed by computer command at any time.

Characters stored in the Display RAM fit within set classifications. Foreground characters appear on the screen as positive, green on black, images. Background characters appear on the screen as negative, black on green, images. Suppressed background characters are represented by foreground spaces. Within the Display RAM, certain control information is stored in the locations seen as suppressed background characters.

Fields further define data display, offering boundaries within which characters may be entered. A normal field is distinguished by a lack of any special background character before it. It may encompass any area of the screen not limited by background or suppressed background characters.

A Right-justified field follows an $0B. Only numeric characters may be entered into it, including one decimal and one minus sign. To the operator at the keyboard, data being entered occurs at the far right portion of the screen, and shifts to the left as additional data is entered.

Kana fields are available with the Japanese VT3. A $0F preceding provides identification in the Display RAM.

The main CPU conditions the Display Screen as is appropriate to the User Program being utilized by writing background areas. The operator cannot enter data into these areas. They generally contain information structuring data entry into foreground fields.

The cursor is a blinking character notifying the operator of the location of the next position for data entry. The cursor skips over any background areas as it proceeds left to right a space at a time across the display screen. During right-justified entry, however, the cursor remains stationary, marking the righthand point at which new data will appear before being shifted right.

The cursor is not displayed during Blind Entry Mode, a method by which the operator may enter password information without displaying it on the screen. 32 characters may be entered in this mode. Read Request to the main CPU is set by TAB, RETURN, or TRANSMIT through the used of Transmit Stop characters at both ends of the blind buffer. Following password entry and main CPU recognition, the cursor is positioned in the first foreground field on the display screen.

The control line occupies the last line of the display screen; the 28th line of a 64 character per line screen or the 25th line of the 80 character per line screen (a line is skipped following the 24th line). The control line is used for system messages. Flag 2 and Flag 3 states are stored as the first 6 characters of the control line. Information used in test sequences is also stored within this line.

CONTROL CODES RECOGNIZED BY THE VT3

CODE	CHARACTER	DESCRIPTION
00	Null	Ignored, except causes write initialization.
01xxyy	Set Cursor	Causes the terminal to place the cursor at the Row xx, Column yy; xx between 1 and 27 (24), yy between 0 and 63 (79).
04	Escape	Escape - next character is a control character.
0401	Remember Cursor	Saves current value of cursor for Restore Cursor command(09).
0402	Select 64	Sets the display mode to 64 characters per line and 27 lines. The screen is cleared to blanks and the cursor is positioned to home (or the 27th line if typewriter mode).
0403	Select 80	Sets the display mode to 80 characters per line and 24 lines. The screen is cleared to blanks and the cursor is positioned to home (or the 24th line if typewriter mode).
0404	Select Default	Sets either the 64 or 80 character display mode depending on the hardware default switch. The screen is cleared to blanks and the cursor is positioned to home (or the last line if typewriter mode).
0405	Set Blind Entry	Clears the 32-byte blind buffer to blanks. At the completion of the write, the cursor is positioned to the beginning of the blind buffer.
0406	Blank Fill Line	Replaces all characters from cursor position to end of line with blanks (foreground, background, or suppressed-background). Positions cursor to beginning of next line (or home).
0407	Clear Field	Replaces all characters in field where cursor resides with foreground blanks. Positions cursor to first entry in field (right-most position if RJ field).
0408	Force Transmit	Causes the VT3 to set 'Read Request'. The VT3 acts as if the operator pressed TRANSMIT after the completion of the Write.
0409	Transmit Stop	Stored on the screen as a suppressed background character. When the operator presses TAB or RETURN and the cursor advances past a Transmit Stop, the VT3 posts Read Request. In addition SHIFT/TAB and SHIFT/RETURN will not back up over a Transmit Stop character.
040A	Rollup	Moves the screen portion below the cursor line up one line. The cursor line is lost; blank foreground is inserted at the bottom. The cursor is positioned to the beginning of the bottom line. The control line is not affected.
040B	Roll Down	Moves the screen portion below the cursor line down one line. The cursor line is lost. A blank foreground line is inserted at the cursor line. The cursor is positioned to the beginning of the current line. The control line is not affected.
040C	Set Suppressed-Background	Causes terminal to accept subsequent data characters as suppressed-background (displayed as spaces).
05	Clear Screen	Clears the screen to foreground blanks and positions the cursor to home. The control line is not affected.

CONTROL CODES CONTINUED

CODE	CHARACTER	DESCRIPTION
06	Clear Foreground	Clears all foreground positions on screen to blanks and positions cursor to first foreground position on screen. The control line is not affected.
07	Alarm	Causes audible alarm to sound.
08	Set Background	Causes terminal to accept subsequent characters as background (displayed as black on green).
09	Restore Cursor	Positions the cursor to the position it occupied at the start of the write or to the last 'remembered' cursor location.
0A	Set Foreground	Causes terminal to accept subsequent characters as foreground (displayed as green on black).
0B	Right-Justified	When placed as the character immediately preceding a foreground field, it designates the field to be right-justified. It is stored on the screen as suppressed-background.
0C	Transmit Mark	Stored on screen as suppressed-background. When the operator presses TAB or RETURN and the cursor advances past a Transmit Delimiter, the VT3 posts Read Request.
0D	Cursor Return	Causes terminal to position cursor to beginning of the next line on screen (or home).
0E	Escape	Next character is control character.
0E02	Reset F2	Resets Flag 2.
0E03	Reset F3	Resets Flag 3.
0E04	Reset F2 & F3	Resets Flag 2 and Flag 3.
0E05	Enter Typewriter	Sets typewriter mode for writing.
0E06	Enter Normal Mode	Sets normal mode. Clears typewriter mode.
0E07	Write Control Line	Clears the control line to blanks. Subsequent data is written to the control line.
0E0F	Execute Test Program	The remainder of the data is used as a Z80 program to execute. Use a RETURN to exit the program.
0F	Kana Field	On English systems it is ignored except as a screen place-holder. On Kana systems it causes the field to be declared a Kana field. Characters from the keyboard are interpreted as being in Kana mode until the 'ALPHA MODE' key is pressed or the cursor is moved to a new field.

VT3 KEYBOARD

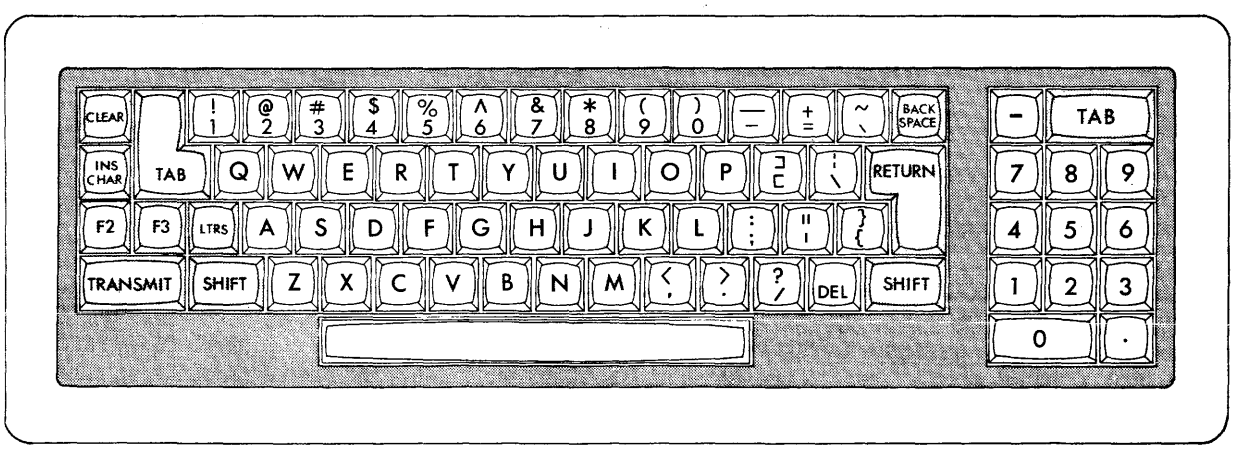


Fig. 7

KEYBOARD

73 momentary contact keys with N-key rollover are incorporated into the VT3 keyboard. Repeat capabilities are possible with some keys and any character key may be repeated if preceded by simultaneously depressing SHIFT and the decimal point key on the numeric cluster. Control keys provide a means for editing (BACKSPACE, CLEAR, and INS CHAR) and data capture when entry is complete (TRANSMIT, TAB, and RETURN). Two flag states, stored in flip-flops, are provided to allow the main CPU to initiate escape sequences: FLAG 2 (F2) and FLAG 3 (F3). Following turn-on or reset, all alphabetic characters will be uppercase; depressing LTRS allows control of upper and lowercase generation. The SHIFT key alters the control function of several keys as shown in the following description:

CONTROL KEY	NORMAL FUNCTION	WITH SHIFT
BACKSPACE	Moves cursor one position left. Stops at first foreground in field or at beginning of screen. In right-justified (RJ) fields it removes the last number entered and shifts the remaining characters one position right.	Moves cursor one position right. Stops at last foreground in screen. Illegal in RJ fields.
TAB	Moves cursor to beginning of next foreground field (may be several lines or less than one line). Sets "Read Request" at end of screen or transmission delimiter (Transmit Mark or Transmit Stop).	Moves cursor to beginning of present foreground field, or if already there (or RJ field), to beginning of previous foreground field. Will not pass beginning of screen or Transmit Stop character.
INS CHAR	Inserts blank character at cursor position and shifts all characters to the end of the field one position right. The last character is lost. Illegal in RJ fields.	Deletes character at cursor position and shifts all characters to the right of the cursor in the same field, one to the left. A blank is inserted at the end of the field. Illegal in RJ field.
CLEAR	Replaces all characters in field where cursor resides with blanks. Cursor is positioned to normal position of first entry in field (left if normal, right if RJ).	Clears foreground. Resets all foreground characters on the screen to blanks. Cursor is positioned to first foreground field on screen. In blind entry mode, it acts like CLEAR.
RETURN	Moves cursor to first foreground position after end of line. Sets "Read Request" at end of screen or if a transmission delimiter is encountered. If RJ field, same as TAB.	Moves cursor to first foreground position in line, or if already there, to first foreground position on last previous line containing foreground. Will not pass the beginning of the screen or a Transmit Stop. If RJ field, then same as SHIFT/TAB.
F2	Toggles "Flag 2", a switch tested by the software.	Performs a terminal reset.

KEYBOARD CONTINUED

CONTROL KEY	NORMAL FUNCTION	WITH SHIFT
NUMERIC .	Produces decimal point display.	Starts keyboard repeat mode. The following key is repeated at a rate of 15 cps as long as it is depressed by the operator. Note that this applies to the numeric cluster only.

ADDITIONAL CONTROL KEYS	FUNCTION
TRANSMIT	Sets "Read Request" in order to transmit data to the computer.
F3	Toggles "Flag 3". This is used by the operating system as an escape condition to abort the current program.
LTRS	Allows upper and lower case alphabetic characters to be entered. When pressed a second time, it restores 'upper case' mode.

MICROCODE SUMMARY

It is beyond the scope of this manual to provide a detailed description of the VT3's firmware. Further information, including flowcharts, may be found in Qantel document #F30786 and by studying the actual microcode listing, document # L30786.

This description will cover in a general way the basic processes carried out by the microcode.

The firmware can be examined most easily by reducing the routines to four, logically independent groups.

1 MAIN ROUTINES

Initialization prepares the logic elements (flags, RAM variables, operation modes) to proceed with the program sequence.
Main Control Loop monitors for incoming data and branches to routines to process it.
Keyboard Processing and Input handles keyboard data arriving as a result of operator input.
Write processes data sent from the main CPU.
Read turns display screen information into a QSP data stream for sending to the main CPU.

2 SCAN INTERRUPT HANDLER

Provides a new address for each line of the Display RAM to initiate the refresh process of the display screen.

3 TIMER INTERRUPT HANDLER

Provides periodic checking of the communication line, processes QSP data streams, and handles data transmission.

4 TEST PANEL INTERRUPT HANDLER

Handles the input from the Z-8Ø test panel interface at the P2 junction.

INITIALIZATION

Initialization occurs immediately following power on or whenever a reset action is performed. Essentially, initialization is designed to set up program variables (represented by internal Z-8Ø flags, RAM storage locations, and applicable flip-flops, and other variables) to allow execution of the program from the beginning stage.

The steps during Initialization include the following:

- Z-8Ø Stack Pointer set to top of stack.
- Maskable Interrupts are disabled.
- Keyboard speaker turned off.
- Request to Send flip-flop cleared.
- Index register IX is set to start of Private RAM ($4000).
- Private RAM cleared to zeroes.
- Keyboard line accessed for random characters.
- Screen format is set according to jumper J13.
- Display RAM cleared.
- Auxilliary Z-8Ø registers (which are used for Scan Interrupt information) are prepared for the first scan.
- Terminal Address is read (from control board Address Switches) and stored.
- UART received register cleared.

INITIALIZATION CONTINUED

- Receive routine prepared (through RAM variables) to expect EOT character from communications line.
- Z-8Ø Interrupt Mode 0 set.
- Maskable Interrupts enabled.
- Main Control Loop entered.

MAIN CONTROL LOOP

The Main Control Loop consists of a very basic sequence. The keyboard is checked to determine if a key has been pressed. If so, the incoming information is processed. If not, the Main Control Loop checks Private RAM to determine if a Write or a Read command has been received from the main CPU. The appropriate branch is carried out. When the necessary operations are completed, the program returns to the start of the Main Control Loop.

KEYBOARD ROUTINE

The Keyboard Routine is designed to respond to operator input from the keyboard: each key pressed initiates either a display or a control sequence. The Kinput Subroutine is contained within the Keyboard Routine and is used for recognizing and clocking in serial keyboard data; translating data to ASCII; handling certain control key functions (LTRS, F2, REPEAT); and turning off the audio alarm after a set time.

The essential processes in the Keyboard Routine are:

- Checks the READ PENDING flag in Private RAM.
  - If true, call KINPUT searching for the key pressed indication.
  - If a key is pressed, the audio alarm is sounded -- keys cannot be processed while the Read Pending is active.
  - If false, checks the FORCE TRANSMIT flag (equivalent to the operator pressing TRANSMIT).
- Blinks the cursor.
- Checks for key pressed.
- Responds to the type of key by initiating the correct sequence.
  - Character keys are processed by entering display sequence.
  - Control key functions are carried out.

The setting of the READ PENDING flag results in a READ REQUEST being delivered to the IOU-39Q during its scanning cycle, thus notifying the main CPU that data is available for reading. The operator can cause READ PENDING to be posted in three ways. The most straightforward way is by simply pressing the TRANSMIT key. This causes the program to scan backwards on the display screen. All the intervening data is transferred to the transmission buffer in Private RAM for eventual passage through the communication line.

KEYBOARD ROUTINE CONTINUED

TAB and RETURN may also set READ PENDING if they cause the program to encounter a Transmission Delimiter. In such a case, the program sequence acts like the TRANSMIT sequence.

KINPUT SUBROUTINE

This subroutine performs the manipulations required to input and process the encoded data from the keyboard. Once a key depression is recognized (through the Buffer 5A on Sheet 8 of the Logics), the character is shifted in a bit at a time by toggling a flip-flop that generates the keyboard clock. The most significant bit arrives first and represents the shift condition. The next 7 bits are the keyboard code - they are translated to ASCII for processing and display. All coded values translated to $80 or higher are recognized as control keys.

Characters are saved as received until the Repeat flag (initially cleared) is updated to reflect any upcoming repeat function.

Of the available control keys, KINPUT internally handles the following F2; SHIFT/F2; F3; LTRS; REPEAT; ALPHA MODE; and KANA MODE.

READ

A READ command from the main CPU is realized by the VT3 through a structured data sequence from the IOU-39Q. From the Main Control Loop, READ is entered whenever the READ IN PROGRESS flag is high. This flag is set during another routine, RECEIVE, which handles communicaiton line activities. Once the first three bytes of the formatted message stream are established by RECEIVE, the READ routine proceeds to continue transmission,

taking data from the Transmit Buffer, formatting it according to Qantel Standard Protocol, and releasing it onto the communications line. Compression and transparency of the data is taken care of during this process.

The message format in response to a READ command is as follows:

DEVICE	STX	STATUS	CURSOR X	CURSOR Y	TEXT	ETX	BCC

The cursor position is transmitted, both X and Y coordinates as positioned when the READ PENDING was encountered. (Cursor values are ORed with $80 so as not to be transparent.)

Each byte in the Transmit Buffer is then sent. When the data has been transmitted, the message format is concluded with a ETX character and BCC (Block Check Character) to ensure data integrity.

The READ PENDING state is maintained if the VT3 does not receive a positive acknowledgement (ACK -- $06). The entire sequence is then repeated when signaled by the IOU-39Q.

If the transmission succeeds, flags are reset (READ PENDING, F2, and F3) and the cursor is positioned to the next foreground field. The routine returns to the Main Control Loop.

WRITE

Characters coming in the UART's receive buffer are processed by the WRITE routine to be placed on the display screen. WRITE commands are received in formatted QSP message streams by RECEIVE routine at which time the WRITE PENDING flag is set. As the program is progressing through the Main Control Loop, detection of WRITE PENDING instigates the WRITE routine.

Characters are examined as they are inputted from the receive buffer for specific characteristics. After the write initialization sequence is performed, any characters between $00 and $0F are considered control commands; characters higher than $0F are data characters.

Each control character results in a program branch to accomplish the assigned task. Commands may consist of one, two or three-byte sequences. At the conclusion of processing the command, the program branches back to handle the next character in the receive buffer.

Data characters are stripped of their highest significant bit. Any resulting values between $00 and $03 are converted to $20. This prevents the user program from placing control characters onto the display screen directly.

Characters are placed on the screen in the position denoted by the cursor (which is incremented after each display). Foreground and background characters are distinguished when the character value is ORed with the mode of display. Whenever the cursor is extended beyond the edge of the screen, it is repositioned to the beginning of the screen. The exception to this is typewriter mode in which case the write is truncated when the cursor reaches the edge.

WRITE CONTINUED

Following character processing the routine performs a Write Cleanup if the Write Setup flag indicates the screen was modified for display. When in typewriter mode, a Transmit Mark is situated at the end of the data. The cursor is moved forward until it encounters a foreground field, where it is halted awaiting operator entry. The Write Pending flag is set to 0 and the program resumes in the Main Control Loop.

SCAN INTERRUPT HANDLER

The Z-8Ø utilizes its set of auxiliary registers (AF'; BC'; DE'; and HL') to keep track of horizontal and vertical trace progress across the CRT. When the Scan Interrupt routine is entered, these registers are immediately accessed and will contain the information to orient the Z-8Ø.

B	Raster Row Counter (0 through 8)
C	7 indicates odd scan; 8 indicates even scan
DE	Next Address to start scanning row
HL	Pointer for the Scan Address Table (used to find the address to be loaded into DE).

The hardware timing circuits initiate a Scan Interrupt every 64 microseconds. Each time this happens the Z-8Ø has 16 microseconds to load the correct address for the next starting horizontal row. Maskable Interrupts are disabled and the Z-8Ø, through a hardware buffer, recognizes the branch to address $0038 where the Scan Interrupt Routine is stored.

Each character is composed of 15 raster lines. Since interlacing is employed in VT3 scanning pattern, the character is

SCAN INTERRUPT HANDLER CONTINUED

"sketched in" in two subsequent passes of the entire display screen. A horizontal row address is presented for 7 or 8 times on an alternating basis. The signal ODDCOUNT obtained from the hardware dictates, if true, that the first row be presented 7 times. The next row will be presented 8 times followed by a row 7 times and so on. When ODDCOUNT is false, the first row is presented 8 times, the second 7 times, and so on.

A separate Scan Address table exists for 64 characters per line operation and one for 80 characters per line operation.

After delivering the correct address to the hardware, updating the data in the auxiliary registers, the program exchanges registers to the normal set, enables the interrupts, and resumes the program from the location indicated by the stack pointer.

TIMER INTERRUPT HANDLER

Roughly every 256 microseconds, a timer interrupt is generated from the hardware timing network. The Z-8Ø distinguishes this interrupt from the higher priority scan interrupt by reading a Tri-state buffer, 7B, seen on Sheet 1 of the Logic Drawings. This causes a RESTART 8 instruction; the program branches to location $008 where the Timer Interrupt Handler begins.

Interrupts are enabled during the Timer Interrupt sequence, allowing the Scan Interrupt to be generated and recognized at any time. This is necessary to ensure that the correct Scan Address will be delivered to the Scan RAM to start the refresh of a horizontal row on the display screen.

TIMER INTERRUPT HANDLER CONTINUED

The ININT flag is used to keep track of whether or not the Z-8Ø had begun processing a timing interrupt. If it had been processing the timing interrupt and was diverted by another timer interrupt, the flag would be true. In this case, the program would return so that interrupts would not be nested.

The ININT is set, otherwise, and the routine checks to see if data is arriving on the communications line. Incoming data is processed by the RECEIVE routine. Then the IO Flag Byte is checked for activity. If the flag contains any bits other than Ø the IOCHECK routine is entered. Following processing of this sequence, the program returns to the address stored in the stack register. The ININT flag is reset in preparation for the next Timer Interrupt.

RECEIVE

The QSP formatting of data transmissions and reception of incoming message strings is handled by this RECEIVE routine. An inputted data byte is dealt with according to what is expected next based on protocol sequences. An address is reserved to guide the program to the special purpose routine for handling the expected byte. This saves time in the processing of QSP sequences.

RECEIVE is entered out of the Timer Interrupt Handler whenever a byte has been received on the communication line.

IOCHECK SUBROUTINE

Modem control signals are monitored and manipulated by this subroutine. Three separate operations take place according to bits in the IO Flag signalling the state of activities.

One segment of the routine checks for the Clear to Send bit detected through the hardware. Once the CTS is detected, it is reset in the IO Flag.

While data is being transmitted, the IOCHECK subroutine monitors for the arrival of Transmit Service Request from the modem. Once received, the next byte in the IO buffer is fetched and outputted on the communication line. The total number of bytes in the buffer is stored in IOCOUNT, a location in Private RAM. When the bytes are all transmitted, the bit in the IO Flag denoted date ready to be transmitted is reset.

Ready to Send is dropped by this routine following the transmission of all data out of the UART. The combination of Transmit Service Request with the Transmit buffer empty causes the routine to drop Request to Send.

DATA PATHS and TRANSLATION

1) *A key position code is generated for each key pressed on the keyboard. This code must be translated to ASCII by the Z-80 before the character is stored in RAM or recognized as a control code.*

2) *The Display RAM is the ultimate storage location for all characters and graphic information that is to be placed on the screen. Since the character ROM responds to ASCII values placed at its address inputs, all display RAM characters must be ASCII encoded.*

3) *Data channeled over the communication line must be formated according to QSP requirements. This discipline increases efficiency of the communication process by structuring data compression, transparency, and maintaining message integrity by a block checking process.*

4) *The Video Signal is a serial bit stream. Dots are placed on the CRT during scanning representing slices of characters; the slices are interlaced to create the assembled character in two successive sweeps of the display screen. The visual representation of these characters is contained within the character ROM in the form of a dot matrix pattern.*

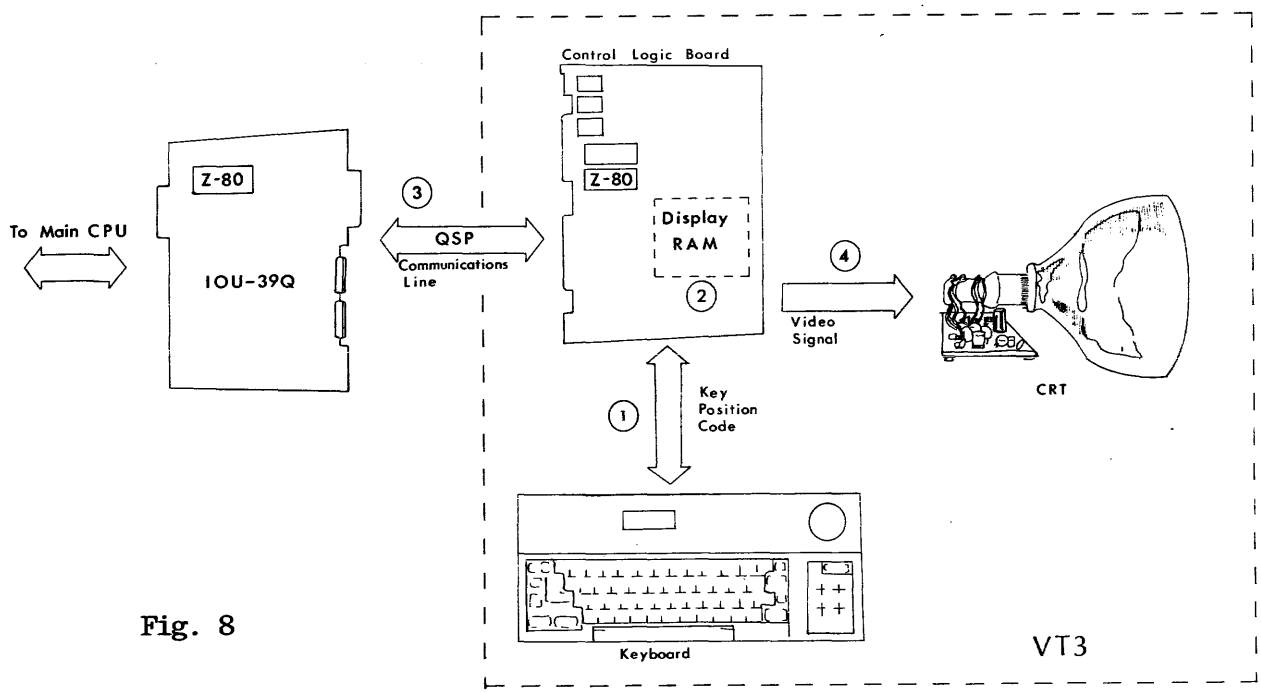


Fig. 8

TYPEWRITER MODE

Typewriter Mode provides a simplified means of writing to the VT3 when complicated screen formats are not required. The display screen mimics a typewriter; the lines of characters are entered as background at the bottom of the screen and "roll-up" as entry continues. The handling of the write process in Typewriter Mode is somewhat different and includes the following:

- As part of the Write Initialization, the display screen is rolled-up, the cursor is positioned at the beginning of the bottom line, and background display mode is set.
- $0D (Carriage Return) within the written data is an indication for the VT3 to roll-up the entire screen, clear the bottom line to blanks, and position the cursor at the beginning of the bottom line.
- A write is terminated if data characters run off the end of the display area. Use of Carriage Return ($0D) allows a number of lines to be written for one write command.
- Transmit Marks are placed at the end of the Write.

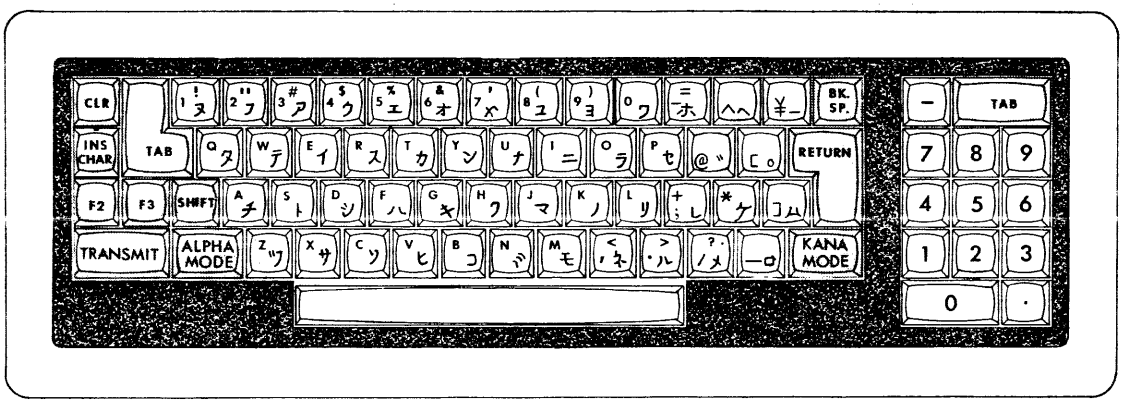


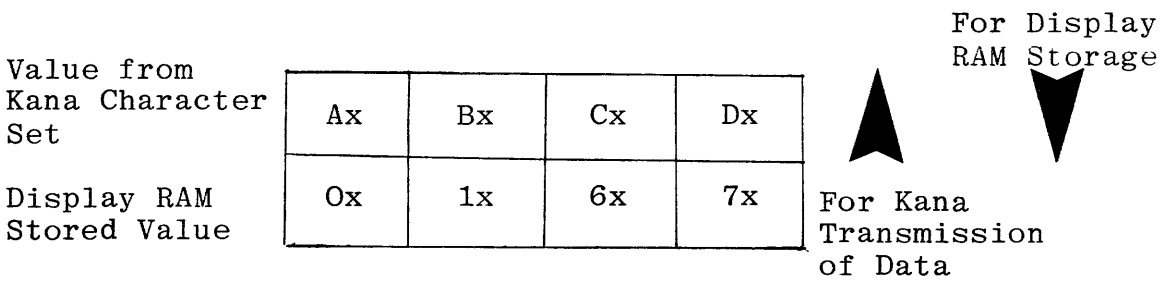
Fig.9
Katakana Keyboard

KATAKANA KEYBOARD

The Japanese character set consists of 124 characters including Katakana and uppercase English. During a write to the VT3, the Z-8Ø recognizes a $0F as the last background character before a field of Kana characters. This value is converted to a $83 for storage in the Display RAM. The cursor being positioned into a Kana field results in data entered from the keyboard being interpreted as Kana. The ALPHA key, once depressed, allows uppercase English characters to be entered.

The keyboard is equipped with both ALPHA and KANA mode keys -- the default value is ALPHA mode. Whenever KANA is depressed, subsequent keys are interpreted as KATAKANA code.

Because ASCII values as stored in the Display RAM are limited to seven bits (the eighth bit is used to identify foreground and background display), the values assigned to the KANA character set from $8F up must be translated to lower values for RAM storage. This translation takes place according to the following table:



x = Value between Ø and F as represented by vertical column on the character set chart.

DATA CONVERSION FOR STORAGE

Another type translation takes place with particular control code characters that are transmitted in one form and converted to another form for Display RAM storage. These characters are:

$80 SUPPRESSED BACKGROUND NULL	Used by the main CPU to write data in suppressed background mode.
$81 TRANSMIT MARK	Appears as $0C in a data stream.
$82 RIGHT-JUSTIFIED FIELD	Appears as $0B in a data stream.
$83 TRANSMIT STOP or KANA	Transmit Stop appears as $0409 in a data stream. In the KANA version, the same $83 means the following foreground field is KANA and appears as $0F in the data stream.

Applying these translations to a segment of a typical data transmission to a VT3 would result in the following conversions:

Sent through the IOU-39Q →	C5	AA	0C	20	20	0C	47
Display RAM Will Contain →	65	0A	81	20	20	81	47
Displayed on Screen →	+	I	Transit Mark	Space	Space	Transit Mark	G

Fig. 10

KATAKANA CONTINUED

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0			BLANK	0	@	P						ー	タ	ミ		
1			!	1	A	Q						ア	チ	ム		
2			"	2	B	R						イ	ツ	メ		
3			#	3	C	S						ウ	テ	モ		
4			$	4	D	T					ヽ	エ	ト	ヤ		
5			%	5	E	U					・	オ	ナ	ユ		
6			&	6	F	V					ヲ	カ	ニ	ヨ		
7			'	7	G	W					ア	キ	ヌ	ラ		
8			(	8	H	X					イ	ク	ネ	リ		
9			)	9	I	Y					ウ	ケ	ノ	ル		
A			*	:	J	Z					エ	コ	ハ	レ		
B			+	;	K	[					オ	サ	ヒ	ロ		
C			'	<	L	¥					ヤ	シ	フ	ワ		
D			−	=	M	]					ユ	ス	ヘ	ン		
E			.	>	N	^					ヨ	セ	ホ	゛		
F			/	?	O	−					ツ	ソ	マ	゜		

Fig. 11

KATAKANA CHARACTER SET

Configuration Information

VT3 CONFIGURATION GUIDE

VT3's attached to a single IOU-39Q may be arranged in the configurations described in the following section. A network involving one IOU-39Q may contain a maximum of 31 VT3's. All Baud rates should be identical within the network as set by jumper switches J1 through J7.

DIRECT STRING NETWORK

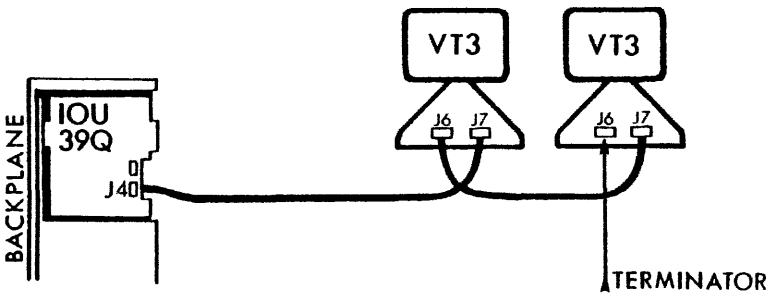


Fig. 12

- A string of 1 to 31 VT3's connected by 232/V24 cables.
- Total length of string no more than 250 feet.
- No more than 50 feet between individual VT3's.
- Communication speed: 19,200 bits per second.
- IOU-39Q timeout: 15 milliseconds.
- Terminator plug (M42540-001) should be attached to female connector of the last VT3 in the string.

HUB UNIT NETWORK

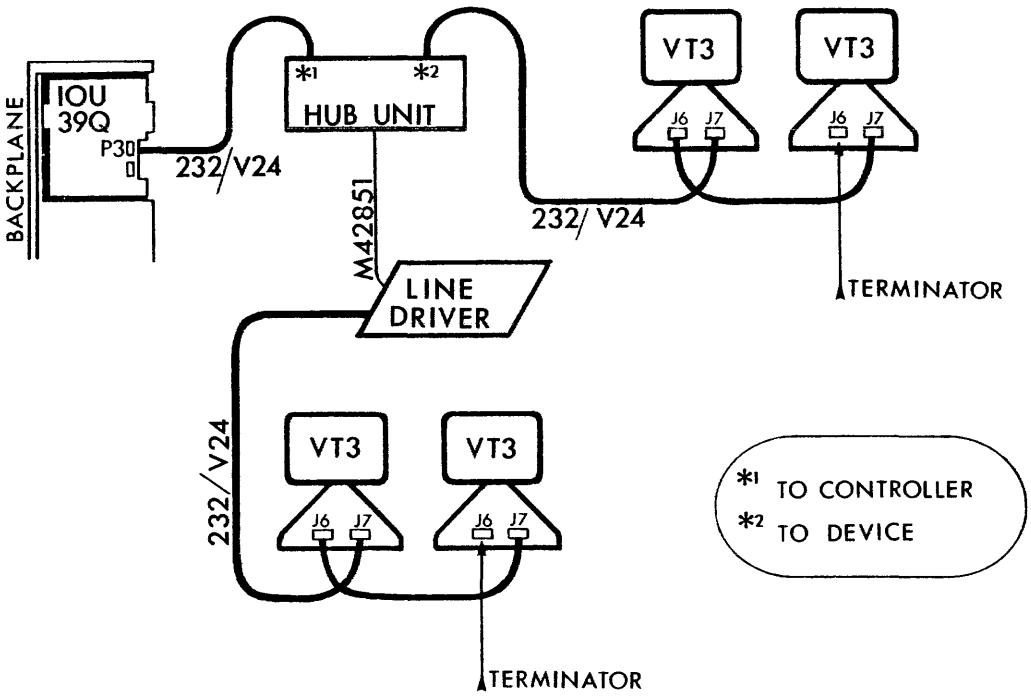


Fig. 13

- In conjunction with Line Drivers, the Hub Unit extends the range of direct strings (1 mile at 19,200 bps; 2 miles at 9600 bps).
- Allows more than one string of VT3's to be connected.
- Connection between Hub Unit and Line Driver should be 4-wire cable (M42851).
- A maximum of 7 Line Drivers may be attached to the Hub Unit.
- Additionally, a local string, without a Line Driver, may be attached.
- Maximum communication speed: 19,200 bps.
- IOU-39Q timeout: 15 milliseconds
- Terminator plugs should be attached to female connector of the last VT3 in any given string.

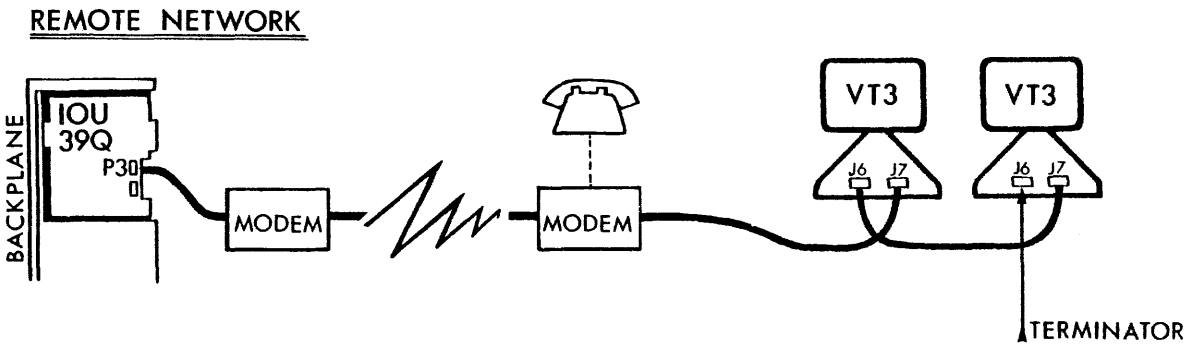


Fig. 14

- For longer distances than 1 mile (or 2 miles at 9600 bps), a Remote Network is necessary.
- Asynchronous modems supply the link between the IOU-39Q and the remote site.
- A local string of VT3's may be attached to modem.
- Communication speed is dependent on modem types and line conditions.
- IOU-39Q timeout is also dependent on a number of factors.
- Terminator plugs should be installed in the last VT3 in each string.

JUMPER SETTINGS FOR VT3 LOGIC BOARD

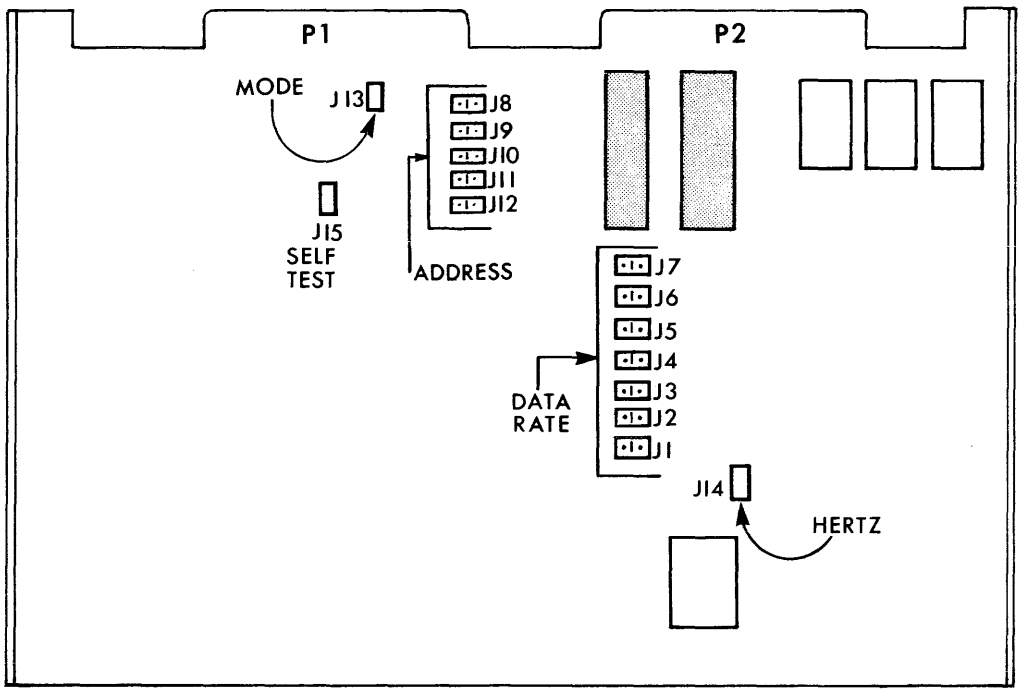


Fig. 15

Jumper J1 through J7 determine Baud rate. Install only one jumper. *Denotes typical jumper placement for USA, non-modem installations.

J1	19.2K Baud*	J5	1200 Baud
J2	9600 Baud	J6	600 Baud
J3	4800 Baud	J7	300 Baud
J4	2400 Baud		

The VT3 device address jumpers J8 through J12 determine the VT3 address. Allowable addresses are $00 to $1E. NEVER address a VT3 to $1F (all switches installed).

J8	$01	J11	$08
J9	$02	J12	$10
J10	$04		

The remaining jumpers J13 through J15 set mode control. *Denotes typical jumper placement for USA, non-modem installations. (See next page.)

JUMPER SETTINGS FOR VT3 LOGIC BOARD CONTINUED

J13	installed	=	Default is 64 char/line *
	removed	=	Default is 80 char/line
J14	installed	=	60 Hertz *
	removed	=	50 Hertz

J15 With J15 installed the VT3 will display a slash on the control line to indicate a completed polling sequence.

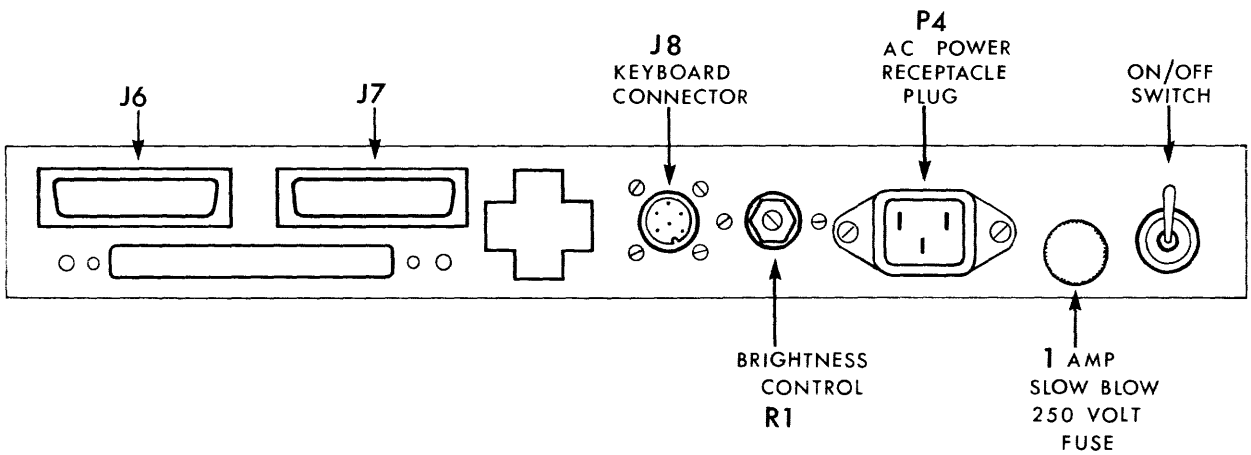


Fig. 16

VT3 Pedestal Back Panel

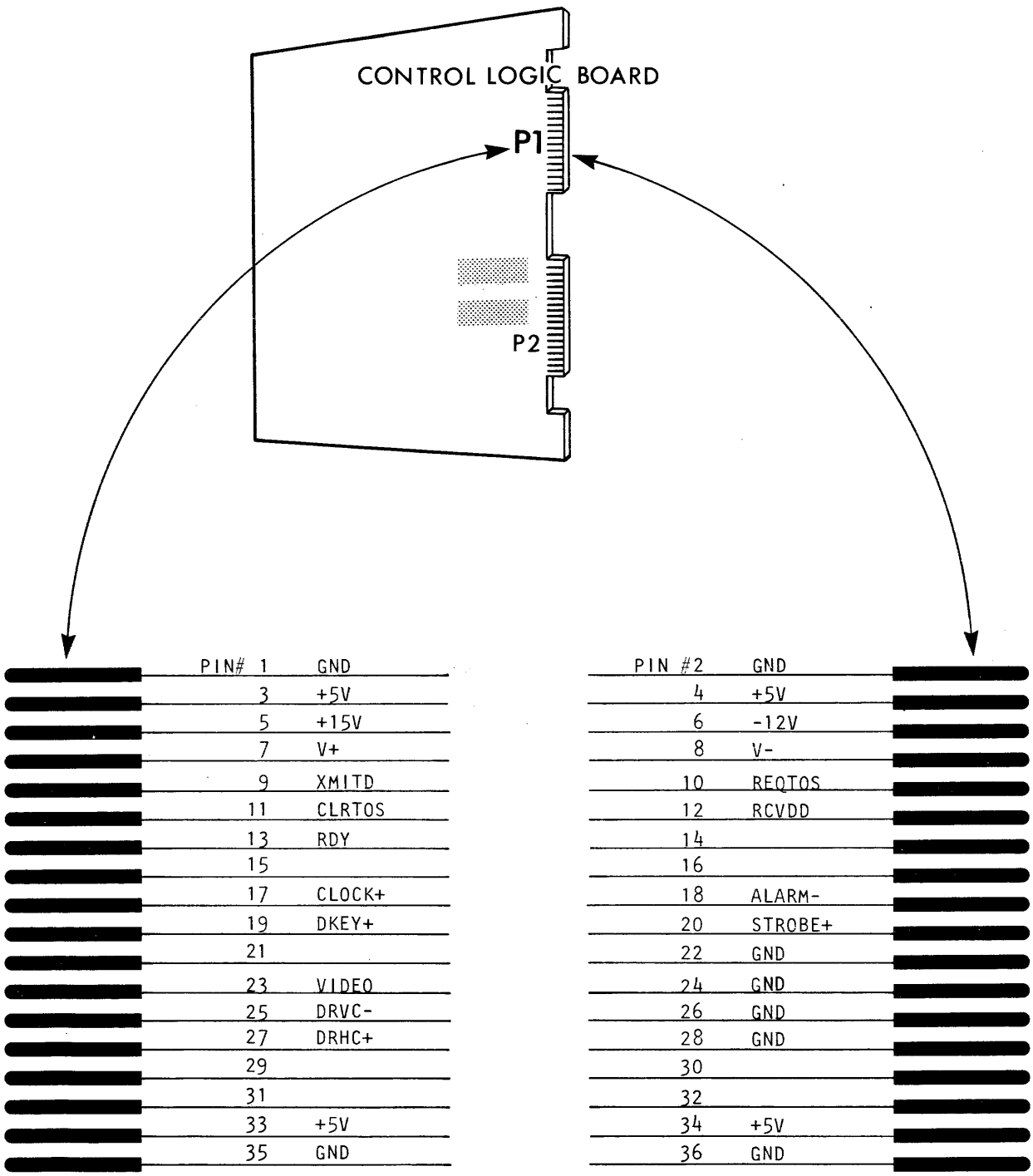

CONTROL LOGIC BOARD
P1
P2
PIN# 1 GND
3 +5V
5 +15V
7 V+
9 XMITD
11 CLRTOS
13 RDY
15
17 CLOCK+
19 DKEY+
21
23 VIDEO
25 DRVC-
27 DRHC+
29
31
33 +5V
35 GND
PIN #2 GND
4 +5V
6 -12V
8 V-
10 REQTOS
12 RCVDD
14
16
18 ALARM-
20 STROBE+
22 GND
24 GND
26 GND
28 GND
30
32
34 +5V
36 GND

Fig. 17

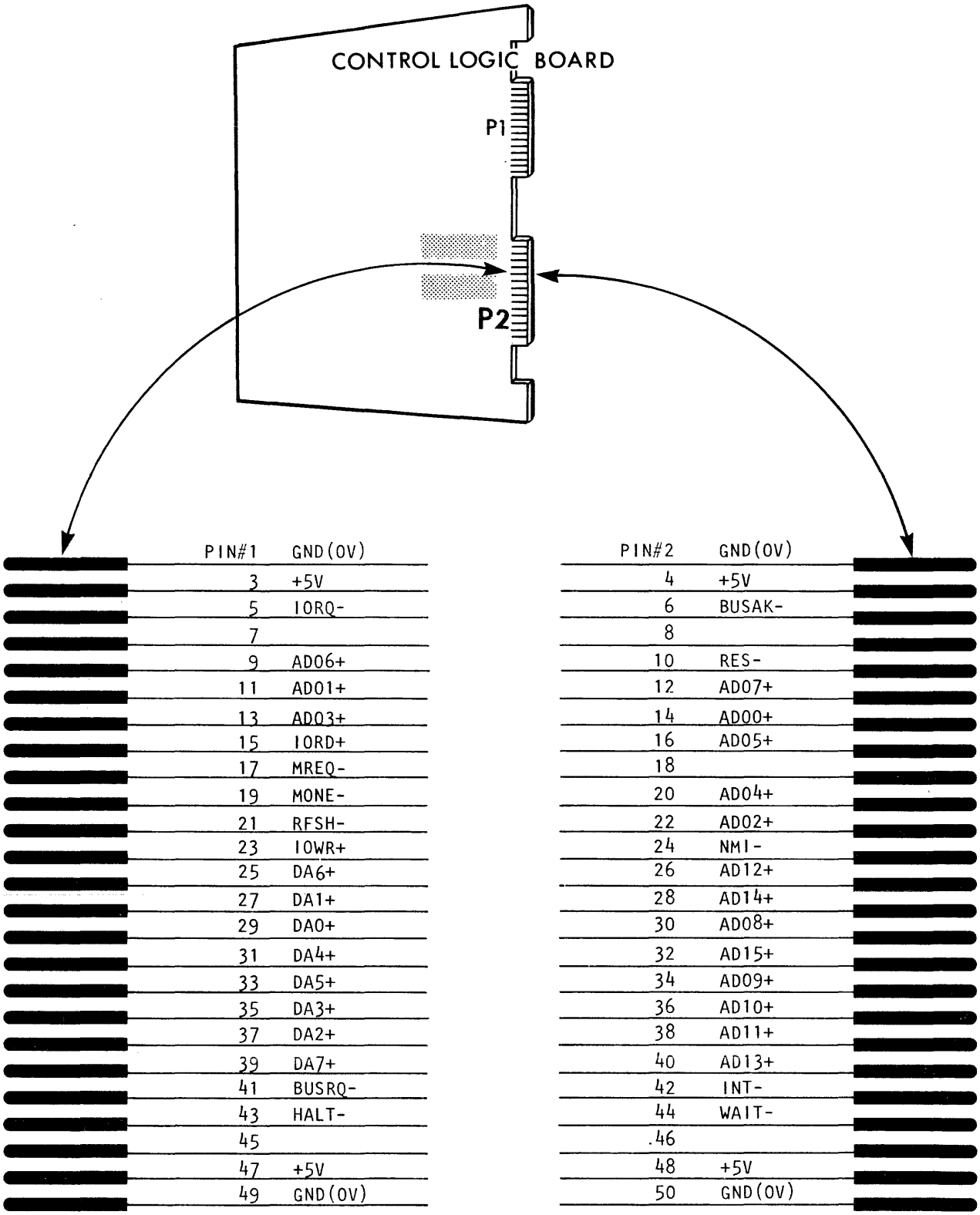

CONTROL LOGIC BOARD
P1
P2
PIN#1 GND(OV)
3 +5V
5 IORQ-
7
9 AD06+
11 AD01+
13 AD03+
15 IORD+
17 MREQ-
19 MONE-
21 RFSH-
23 IOWR+
25 DA6+
27 DA1+
29 DA0+
31 DA4+
33 DA5+
35 DA3+
37 DA2+
39 DA7+
41 BUSRQ-
43 HALT-
45
47 +5V
49 GND(OV)
PIN#2 GND(OV)
4 +5V
6 BUSAK-
8
10 RES-
12 AD07+
14 AD00+
16 AD05+
18
20 AD04+
22 AD02+
24 NMI-
26 AD12+
28 AD14+
30 AD08+
32 AD15+
34 AD09+
36 AD10+
38 AD11+
40 AD13+
42 INT-
44 WAIT-
46
48 +5V
50 GND(OV)

Fig. 18

Test Procedures

MANUAL TEST

The Manual Test (as described in the Engineering Test Procedures, Test 1, Document #A31022) provides a basic, overall test sequence to ascertain correct functioning of the VT3. The steps involved are shown in the following chart.

OPERATOR STEP	RESULT
Turn on VT3 using On/Off Switch on back panel.	VT3 beeps as switch is engaged. Following 30 seconds of warmup, the blinking cursor appears in the upper-left corner of the screen.
Press the letter 'A' on the keyboard.	The letter 'A' appears in the upper-left corner. Cursor moves one position right.
Press the 'RETURN' key on the keyboard.	Cursor drops one line below the 'A'.
Press F2 on the keyboard.	'F2' is displayed in background on the bottom screen line.
Press F2 again	'F2' disappears from screen.
Repeat the above sequence using F3.	'F3' will appear and then vanish as key is repressed.
Press TAB	Cursor disappears.
Press the letter 'A' on the keyboard.	VT3 beeps.
Press SHIFT and F2 simultaneously	VT3 beeps, clears the screen, and the cursor appears in the upper-left corner.

OPERATOR STEP	RESULT
Press each of the following keys and hold down to check repeat function: SPACE BACKSPACE SHIFT/BACKSPACE INS CHAR SHIFT/INS CHAR	After a short delay- repeating of the appropriate action occurs.
Press SHIFT and '.' in the numeric cluster simultaneously. Press the letter 'Q'.	A series of 'Q's' appears on the screen as long as the key is depressed.
Press the LTRS key and any alphabetic character.	Alphabetic characters should appear capitalized with LTRS depressed.
Press each non-control key in sequence. For KANA, verify both Alpha and Kana modes.	Verify that each displayed character correctly matches the character set being used.
Set Jumper J13 for 64-character mode. Press SHIFT/F2 and then enter a string of characters.	A string of 64 characters should fill each row.
Set Jumper J13 for 80-character mode. Press SHIFT/F2 and then enter a string of characters.	A string of 80 characters should fill each row.

AVAILABLE VT3 TEST PROGRAMS

The following tests are available for use with the VT3.
Refer to the appropriate literature for operating instructions of individual programs.

'CRT3': VT3 Acceptance Test

'ACRT3': VT3 Automatic Test

*VITTY: (REAL program running under BEST) Extensive Test

Appendix

1863B -- UART PIN DESIGNATIONS

PIN NUMBER	NAME	SYMBOL	FUNCTION
1	V_{ss} Power Supply	V_{ss}	+5 volts supply
2		NC	No Connection (Open)
3	Ground	GND	Ground = 0V
4	Receiver Register	RRD	A high level input voltage, V_{IH}, applied to this line disconnects the RECEIVER HOLDING REGISTER outputs from the RR_8 RR_1 data outputs (pins 5 12)
5-12	Receiver Holding Register Data	RR_8-RR_1	The parallel contents of the RECEIVER HOLDING REGISTER appear on these lines if a low level input voltage V_{IL} is applied to RRD for character formats of fewer than eight bits received characters are right justified with RR_1 (pin 12) as the least significant bit and the truncated bits are forced to a low level output voltage, V_{OL} .
13	Parity Error	PE	A high level output voltage, V_{OH}, on this line indicates that the received parity does not compare to that programmed by the EVEN PARITY ENABLE control line (pin 39). This output is updated each time a character is transferred to the RECEIVER HOLDING REGISTER. PE lines from a number of arrays can be bussed together since an output disconnect capability is provided by the Status Flag Disconnect line (pin 16).
14	Framing Error	FE	A high level output voltage, V_{OH}, on this line indicates that the received character has no valid stop bit, ie., the bit following the parity bit (if programmed) is not a high level voltage. This output is updated each time a character is transferred to the Receiver Holding Registar, FE lines from a number of arrays can be bussed together since an output disconnect capability is provided by the Status Flag Disconnect line (pin 16).
15	Overrun Error	OE	A high level output voltage, V_{OH}, on this line indicates that the Data Received Flag (pin 19) was not reset before the next character was transferred to the Receiver Holding Register. OE lines from a number of arrays can be bussed together since an output disconnect capability is provided by the Status Flag Disconnect line (pin 16).
16	Status Flags Disconnect	SFD	A high level input voltage, V_{IH}, applied to this pin disconnects the PE, FE, OE, DR and THRE allowing them to be buss connected.
17	Receiver Register Clock	RRC	The receiver clock frequency is sixteen (16) times the desired receiver shift rate.
18	Data Received Reset	DRR	A low level input voltage, V_{IL}, applied to this line resets the DR line.
19	Data Received	DR	A high level output voltage, V_{OH}, indicates that an entire character has been received and transferred to the RECEIVER HOLDING REGISTER.

UART PIN DESIGNATIONS CONTINUED

PIN NUMBER	NAME	SYMBOL	FUNCTION
20	Receiver Input	RI	Serial input data received on this line enters the RECEIVER REGISTER at a point determined by the character length, parity, and the number of stop bits. A high-level input voltage, V_{IH}, must be present when data is not being received.
21	Master Reset	MR	This line is strobed to a high level input voltage, V_{IH}, to clear the logic. It resets the Transmitter and Receiver Registers, the Receiver Holding Register, FE OE, PE, DRR and sets TRO, THRE, and TRE to a high level ouput voltage, V_{OH}.
22	Transmitter	THRE	A high level output Voltage V_{OH}, on this line indicates the TRANSMITTER HOLDING REGISTER has transferred its contents to the TRANSMITTER REGISTER and may be loaded with a new character.
23	Transmitter Holding Register Load	THRL	A low level input voltage, V_{IL}, applied to this line enters a character into the TRANSMITTER HOLDING REGISTER. A transition from a low level input voltage, V_{IL}, to a high level input voltage, V_{IH}, transfers the character into the TRANSFER REGISTER if it is not in the process of transmitting a character. If a character is being transmitted, the transfer is delayed until its transmission is completed. Upon completion, the new character is automatically transferred simultaneously with the initiation of the serial transmission of the new character.
24	Transmitter Register Empty	TRE	A high level output voltage, V_{OH}, on this line indicates that the TRANSMITTER REGISTER has completed serial transmission of a full character including STOP bit(s). It remains at this level until the start of transmission of the next character.
25	Transmitter Register Output	TRO	The contents of the TRANSMITTER REGISTER (START bit, DATA bits, PARITY bit, and STOP bits) are serially shifted out on this line. When no data is being transmitted, this line will remain at a high level output voltage, V_{OH}. Start of transmission is defined as the transition of the START bit from a high level output voltage, V_{OH}, to a low level output voltage, V_{OL}.
26-33	Transmitter Register Data Inputs	TR_1-TR_8	The character to be transmitted is loaded into the TRANSMITTER HOLDING REGISTER on these lines with the THRL Strobe. If a character of less than 8 bits has been selected (by WLS_1 and WLS_2), the character is right justified to the least significant bit, RR1, and the excess bits are disregarded. A high level input voltage, V_{IH}, will cause a high level output voltage, V_{OH}, to be transmitted.
34	Control Register Load	CRL	A high level input voltage, V_{IH}, on this line loads the CONTROL REGISTER with the control bits (WLS_1, WLS_2, EPE, PI SBS). This line may be strobed or hardwired to a high level input voltage, V_{IH}.
35	Parity Inhibit	PI	A high level input voltage, V_{IH}, on this line inhibits the parity generation and verification circuits and will clamp the PE output (pin 13) to V_{OL}. If parity is inhibited the STOP bit(s) will immediately follow the last data bit on transmission.
36	Stop Bit(s) Select	SBS	This line selects the number of STOP bits to be transmitted after the PARITY bit. A high level input voltage, V_{IH}, on this line selects two STOP bits, and a low level input voltage, V_{IL}, selects a single STOP bit. Selection of two STOP bits when programming a five (5) bit word generates 1.5 STOP bits.

UART PIN DESIGNATIONS CONTINUED

PIN NUMBER	NAME	SYMBOL	FUNCTION
37-38	Word Length Select	WLS_2-WLS_1	These two lines select the character length (exclusive of parity) as follows:

WLS_2	WLS_1	Word Length
V_{IL}	V_{IL}	5 bits
V_{IL}	V_{IH}	6 bits
V_{IH}	V_{IL}	7 bits
V_{IH}	V_{IH}	8 bits

39	Even Parity Enable	EPE	This line determines whether even or odd PARITY is to be generated by the transmitter and checked by the receiver. A high level input voltage, V_{IH}, selects even PARITY and a low level input voltage, V_{IL}, selects odd PARITY.
40	Transmitter Register Clock	TRC	The transmitter clock frequency is sixteen (16) times the desired transmitter shift rate.

74S/LS138

3-Line To 8-Line Decoder/Demultiplexer

FUNCTIONAL DESCRIPTION

The Am25LS138 is a 3-line to 8-line decoder/demultiplexer fabricated using advanced Low-Power Schottky technology. The decoder has three buffered select inputs A, B and C that are decoded to one of eight Y outputs.

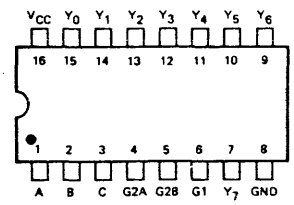
One active-HIGH and two active-LOW enables can be used for gating the decoder or can be used with incoming data for demultiplexing applications. When the enable input function is in the disable state, all eight Y outputs are HIGH regardless of the A, B and C select inputs.

The Am54LS/74LS138 is a standard performance version of the Am25LS138. See appropriate electrical characteristic tables for detailed Am25LS improvements.

DISTINCTIVE CHARACTERISTICS

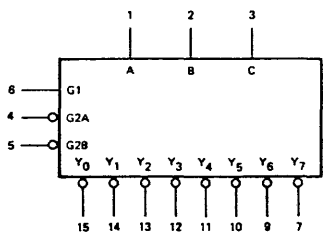
- Inverting and non-inverting enable inputs
- Am25LS devices offer the following improvements over Am54/74LS
  - Higher speed
  - 50mV lower V_{OL}
  - Twice the fan-out over military range
  - 440μA source current
- 100% product assurance screening to MIL-STD-883 requirements

CONNECTION DIAGRAM
Top View



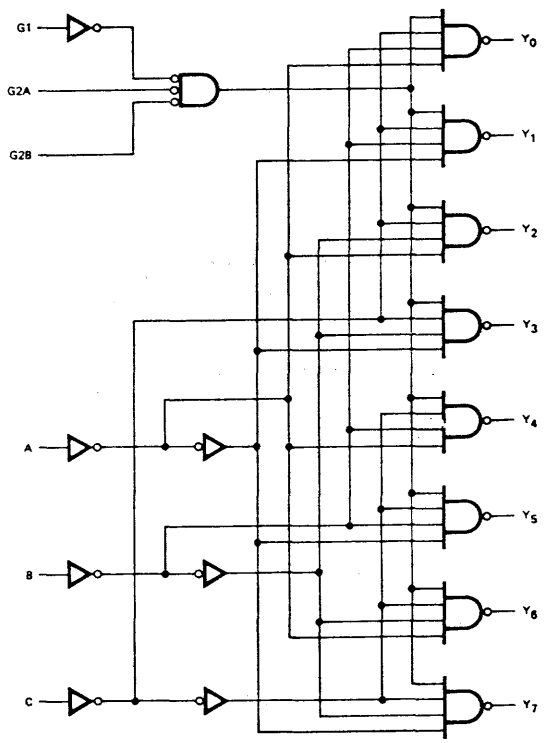
Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAM



74LS158

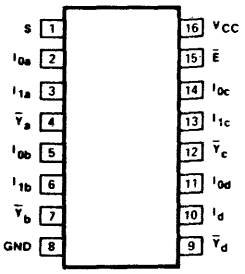
DESCRIPTION

The "158" is a high speed Quad 2-Input Multiplexer that selects 4-bits of data from two sources using the common Select and Enable inputs. The "158" presents inverted data. It can be used to generate any four of the 16 different functions of two variables.

FEATURES

- **Multifunction capability**
- **Inverting data path**
- **See "258" for 3-State version**
- **See "157" for non-inverting version**

PIN CONFIGURATION

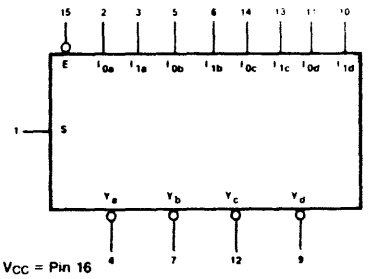


TRUTH TABLE

ENABLE	SELECT INPUT	DATA INPUTS		OUTPUTS
$\bar{E}$	S	I_0	I_1	$\bar{Y}$
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

FUNCTIONAL DESCRIPTION

The "158" is a Quad 2-Input Multiplexer which selects four bits of data from two sources under the control of a common Select input (S), presenting the data in inverted form at the four outputs ($\bar{Y}$). The Enable input ($\bar{E}$) is active LOW. When $\bar{E}$ is HIGH, all of the outputs ($\bar{Y}$) are forced HIGH regardless of all other input conditions.

Moving data from two groups of registers to four common output busses is a common use of the "158." The state of the Select input determines the particular register from which the data comes. It can also be used as a function generator. The device is useful for implementing gating functions by generating any four functions of two variables with one variable common.

The device is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select Input. Logic equations are shown below:

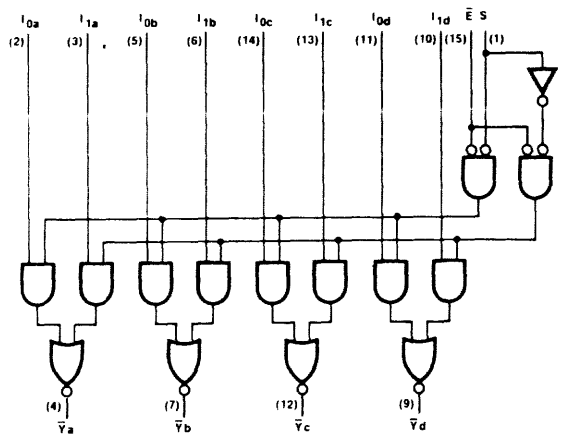
$$\bar{Y}_a = \bar{E} \bullet (I_{1a} \bullet S + I_{0a} \bullet \bar{S})$$

$$\bar{Y}_b = \bar{E} \bullet (I_{1b} \bullet S + I_{0b} \bullet \bar{S})$$

$$\bar{Y}_c = \bar{E} \bullet (I_{1c} \bullet S + I_{0c} \bullet \bar{S})$$

$$\bar{Y}_d = \bar{E} \bullet (I_{1d} \bullet S + I_{0d} \bullet \bar{S})$$

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

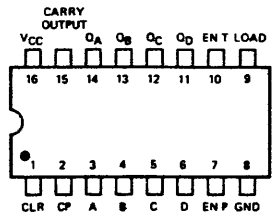
74LS161

Synchronous Four-Bit Counters

DISTINCTIVE CHARACTERISTICS

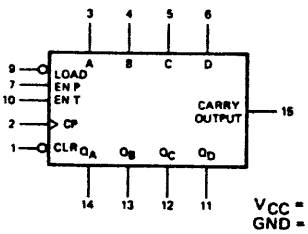
- Synchronous presettable counters
- Decade (LS160A and LS162A) and binary (LS161A and LS163A) counters
- Asynchronous (LS160A and LS161A) and synchronous (LS162A and LS163A) clear inputs
- Am25LS devices offer the following improvements over Am54/74LS
  - Higher speed
  - 50mV lower V_{OL}
  - Twice the fan-out over military range
  - 440μA source current
- 100% product assurance screening to MIL-STD-883 requirements

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

FUNCTIONAL DESCRIPTION

The Am25LS160A, Am25LS161A, Am25LS162A and Am25LS163A synchronous, presettable counters have internal look-ahead carry and ripple carry output for high-speed counting applications. The Am25LS160A and Am25LS162A are decade counters and the Am25LS161A and Am25LS163A are 4-bit binary counters. Counting or loading occurs on the positive transition of the clock pulse. A LOW level on the load input causes the data on the A, B, C and D inputs to be shifted to the appropriate Q outputs on the next positive clock transition. The load need meet only the set-up and hold time requirements with respect to the clock.

The Am25LS160A and the Am25LS161A feature an asynchronous clear. A LOW level at the clear input sets the Q outputs LOW regardless of the other inputs. The Am25LS 162A and Am25LS163A have a synchronous clear. A LOW level at the clear input sets the Q outputs LOW after the next positive clock transition regardless of the enable inputs.

Both count-enable inputs P and T must be HIGH to count. Count enable T is included in the ripple carry output gate for cascading connection. The enable P or T inputs need meet only the set-up and hold time requirements with respect to the clock.

The Am54LS/74LS160A series are standard performance versions of the Am25LS160A series counters. See appropriate electrical characteristic tables for detailed Am25LS improvements.

74LS166

DESCRIPTION

The "166" is a fully synchronous 8-bit serial or parallel-in, serial-out shift register. The Data and Parallel Enable inputs are edge triggered, and must be stable only one setup time before the LOW-to-HIGH transition of the clock. A gated clock is provided allowing one input to be used as a Clock Enable. The Master Reset is asynchronous and clears the register when LOW.

FEATURES

- **Synchronous parallel to serial applications**
- **Synchronous serial data input for easy expansion**
- **Clock enable for "do nothing" mode**
- **Asynchronous Master Reset**
- **See "165" for asynchronous parallel data load**

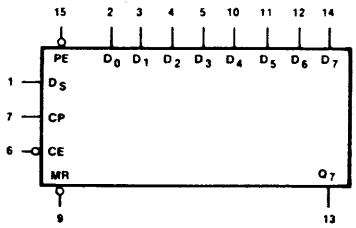
FUNCTIONAL DESCRIPTION

The "166" is an 8-bit shift register that has fully synchronous serial or parallel data entry selected by an active LOW Parallel Enable ($\overline{PE}$) input. When the $\overline{PE}$ is LOW one setup time before the LOW-to-HIGH clock transition, parallel data is entered into the register. When $\overline{PE}$ is HIGH, data is entered into internal bit position Q_0 from Serial Data input (D_S), and the remaining bits are shifted one place to the right ($Q_0 \rightarrow Q_1 \rightarrow Q_2$ etc.) with each positive-going clock transition. For expansion of the register in parallel to serial converters, the Q_7 output is connected to the D_S input of the succeeding stage.

The clock input is a gated OR structure which allows one input to be used as an active LOW Clock Enable ($\overline{CE}$) input. The pin assignment for the CP and $\overline{CE}$ inputs is arbitrary and can be reversed for layout convenience. The LOW-to-HIGH transition of $\overline{CE}$ input should only take place while the CP is HIGH for predictable operation.

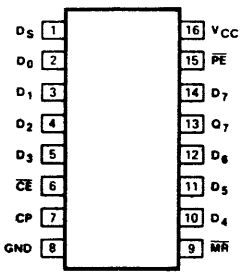
A LOW on the Master Reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all bit positions to a LOW state.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

PIN CONFIGURATION

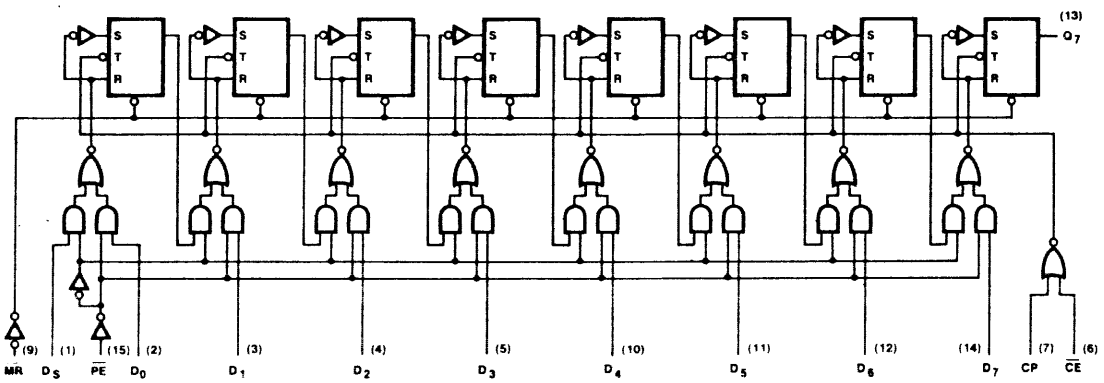


MODE SELECT-FUNCTION TABLE

OPERATING MODES	INPUTS					Qn REGISTER		OUTPUT
	$\overline{PE}$	$\overline{CE}$	CP	D_S	D_0-D_7	Q_0	Q_1-Q_6	Q_7
Parallel Load	l	l	↑	X	l - l	L	L - L	L
	l	l	↑	X	h - h	H	H - H	H
Serial Shift	h	l	↑	l	X - X	L	q_0 - q_5	q_6
	h	l	↑	h	X - X	H	q_0 - q_5	q_6
Hold (do nothing)	X	h	X	X	X - X	q_0	q_1 - q_6	q_7

H = HIGH voltage level.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
q_n = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW to HIGH clock transition.
X = Don't care.
↑ = LOW-to-HIGH clock transition.

LOGIC DIAGRAM



( ) = Pin numbers
V_{CC} = Pin 16
GND = Pin 8

74LS193

DESCRIPTION

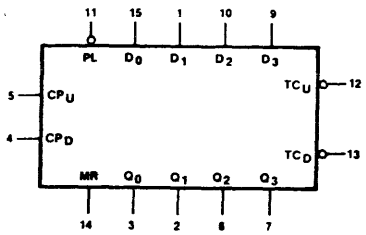
The "193" is an Up/Down Modulo-16 Binary Counter utilizing separate Count Up and Count Down Clocks. The individual circuits operate synchronously in either counting mode changing state on the LOW-to-HIGH transitions on the clock inputs.

To simplify multistage counter designs separate Terminal Count Up and Terminal Count Down outputs are provided which are used as clocks for subsequent stages without extra logic. Individual preset inputs allow the circuit to be used as a programmable counter. Both the Parallel Load ($\overline{PL}$) and the Master Reset (MR) inputs override the clocks and asynchronously load or clear the counter.

FEATURES

- **Synchronous reversible 4-bit binary counting**
- **Asynchronous parallel load**
- **Asynchronous reset (clear)**
- **Expandable without external logic**

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

FUNCTIONAL DESCRIPTION

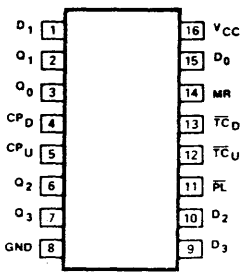
The "193" is an asynchronously presettable, Up/Down (reversible) 4-Bit Binary Counter. It contains four master/slave flip-flops with internal gating and steering logic to provide asynchronous Master Reset (clear) and Parallel load, and synchronous Count-up and Count-down operations.

Each flip-flop contains JK feedback from slave to master such that a LOW-to-HIGH transition on the clock inputs causes the Q outputs to change state synchronously. A LOW-to-HIGH transition on the Count Down Clock Pulse (CP_D) input will decrease the count by one, while a similar transition on the Count Up Clock Pulse (CP_U) input will advance the count by one. One clock should be held HIGH while counting with the other, because the circuit will either count by twos or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either clock input is LOW. Applications requiring reversible operation must make the reversing decision while the activating clock is HIGH to avoid erroneous counts.

The Terminal Count Up ($\overline{TC_U}$) and Terminal Count Down ($\overline{TC_D}$) outputs are normally HIGH. When the circuit has reached the maximum count state of "15", the next HIGH-to-LOW transition of CP_U will cause $\overline{TC_U}$ to go LOW. $\overline{TC_U}$ will stay LOW until CP_U goes HIGH again, duplicating the Count Up Clock although delayed by two gate delays. Likewise, the $\overline{TC_D}$ output will go LOW when the circuit is in the zero state and the CP_D goes LOW. The $\overline{TC}$ outputs can be used as the clock input signals to the next higher order circuit in a multistage counter, since they duplicate the clock waveforms. Multistage counters will not be fully synchronous, since there is a two gate delay time difference added for each stage that is added.

The counter may be preset by the asynchronous parallel load capability of the circuit. Information present on the parallel Data inputs (D_0-D_3) is loaded into the counter and appears on the outputs regardless of the conditions of the clock inputs when the Parallel Load ($\overline{PL}$) input is LOW. A HIGH level on the Master Reset (MR) input will disable the parallel load gates, override both clock inputs, and set all Q outputs LOW. If one of the clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that Clock will be interpreted as a legitimate signal and will be counted.

PIN CONFIGURATION



MODE SELECT-FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS		
	MR	$\overline{PL}$	CP_U	CP_D	D_0,D_1,D_2,D_3	Q_0,Q_1,Q_2,Q_3	$\overline{TC_U}$	$\overline{TC_D}$
Reset (clear)	H	X	X	L	X X X X	L L L L	H	L
	H	X	X	H	X X X X	L L L L	H	H
Parallel load	L	L	X	L	L L L L	L L L L	H	L
	L	L	X	H	L L L L	L L L L	H	H
	L	L	L	X	H H H H	H H H H	L	H
	L	L	H	X	H H H H	H H H H	H	H
Count up	L	H	↑	H	X X X X	Count up	H(b)	H
Count down	L	H	H	↑	X X X X	Count down	H	H(c)

H = HIGH voltage level
L = LOW voltage level
X = Don't care
↑ = LOW-to-HIGH clock transition

NOTES
b. $\overline{TC_U}$ = CP_U at terminal count up (HHHH)
c. $\overline{TC_D}$ = CP_D at terminal count down (LLLL)

74LS244

Octal Three-State Buffers

FUNCTIONAL DESCRIPTION

The LS241 and LS244 are octal buffers fabricated using advanced low-power Schottky technology. The 20-pin package provides improved printed circuit board density for use in memory address and clock driver applications.

Three-state outputs are provided to drive bus lines directly. The Am25LS241 and Am25LS244 are specified at 48mA and 24mA output sink current, while the Am54LS/74LS241 and Am54LS/74LS244 are guaranteed at 12mA over the military range and 24mA over the commercial range. Four buffers are enabled from one common line and the other four from a second enable line.

The LS241 has enable inputs of opposite polarity to allow use as a transceiver without overlap. The LS244 enables are of similar polarity for use as a unidirectional buffer in which both halves are enabled simultaneously.

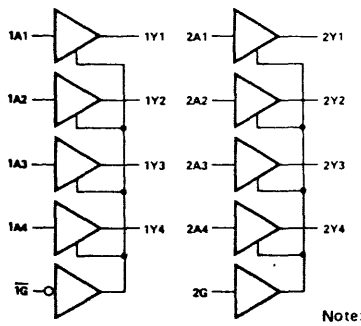
Improved noise rejection and high fan-out are provided by input hysteresis and low current PNP inputs.

DISTINCTIVE CHARACTERISTICS

- Three-state outputs drive bus lines directly
- Hysteresis at inputs improve noise margin
- PNP inputs reduce D.C. loading on bus lines
- Data-to-output propagation delay times – 18ns MAX.
- Enable-to-output – 30ns MAX.
- Am25LS241 and 244 specified at 48mA output current
- 20 pin hermetic and molded DIP packages
- 100% product assurance testing to MIL-STD-883 requirements

LOGIC DIAGRAMS

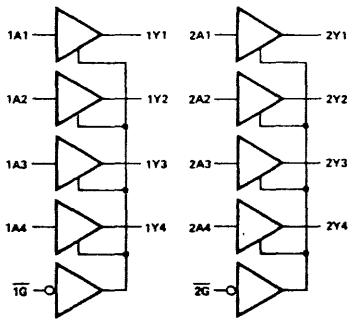
LS241



LS241

INPUTS			OUTPUTS
$\overline{1G}$	2G	A	Y
H	L	X	Z
L	H	H	H
L	H	L	L

LS244

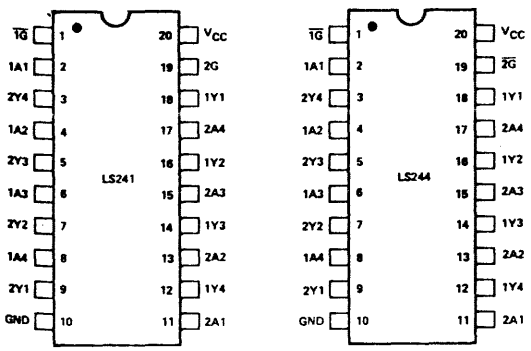


LS244

INPUTS		OUTPUT
$\overline{G}$	A	
H	X	Z
L	H	H
L	L	L

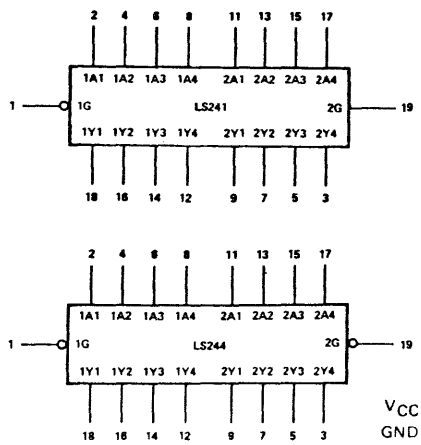
Note: All devices have input hysteresis.

CONNECTION DIAGRAMS
Top Views



Note: Pin 1 is marked for orientation.

LOGIC SYMBOLS



V_{CC} = Pin 20
GND = Pin 10

74LS273

DESCRIPTION

The "273" is an Octal D Flip-Flop used primarily as an 8-bit positive-edge-triggered storage register. Data on the D inputs is transferred to storage during the LOW-to-HIGH transition of the clock pulse. The Master Reset ($\overline{MR}$) input asynchronously clears all flip-flops when LOW.

FEATURES

- **Ideal buffer for MOS Microprocessor or Memory**
- **Eight edge-triggered D flip-flops**
- **High speed Schottky version available**
- **Buffered common clock**
- **Buffered, asynchronous Master Reset**
- **Slim 20-Pin plastic and ceramic DIP packages**
- **See "377" for Clock Enable version**
- **See "373" for transparent latch version**
- **See "374" for 3-state version**

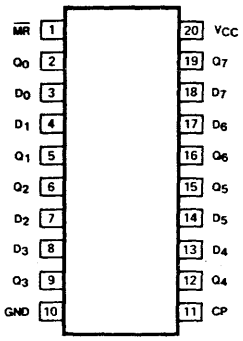
FUNCTIONAL DESCRIPTION

The "273" has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

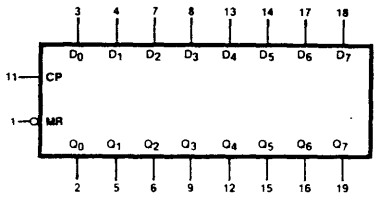
The register is fully edge triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

PIN CONFIGURATION



LOGIC SYMBOL



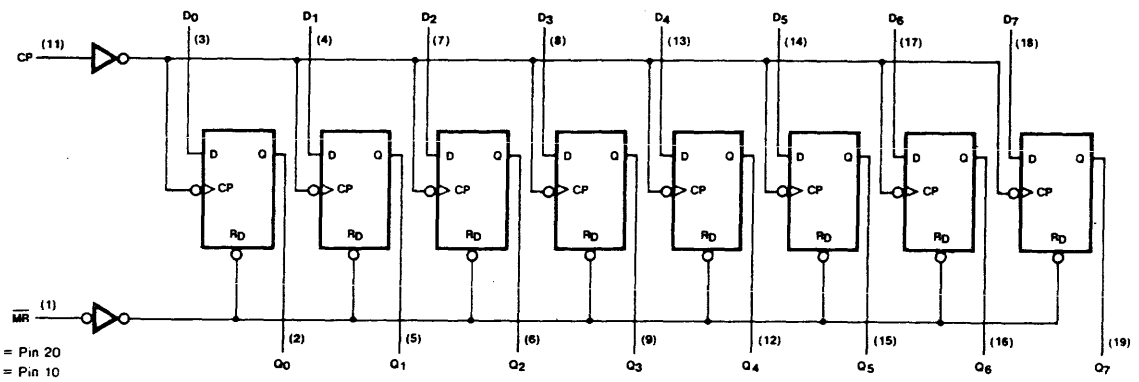
VCC = Pin 20
GND = Pin 10

MODE SELECT - FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS
	$\overline{MR}$	CP	D_n	Q_n
Reset (clear)	L	X	X	L
Load "1"	H	↑	h	H
Load "0"	H	↑	l	L

H = HIGH voltage level steady state.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition
L = LOW voltage level steady state.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition
X = Don't care.
↑ = LOW-to-HIGH clock transition.

LOGIC DIAGRAM



VCC = Pin 20
GND = Pin 10
( ) = Pin numbers

74LS373

OCTAL TRANSPARENT LATCH WITH 3-STATE OUTPUTS

FUNCTIONAL DESCRIPTION

The "373" is Octal Transparent Latch coupled to eight 3-state output buffers. The two sections of the device are controlled independently by Latch Enable (E) and Output Enable ($\overline{OE}$) control gates.

The data on the D inputs transferred to the latch outputs when the Latch Enable (E) input is HIGH. The latch remains transparent to the data inputs while E is HIGH, and stores the data present one setup time before the HIGH-to-LOW enable transition. The enable gate has about 400mV of hysteresis built in to help minimize problems that signal and ground noise can cause on the latching operation.

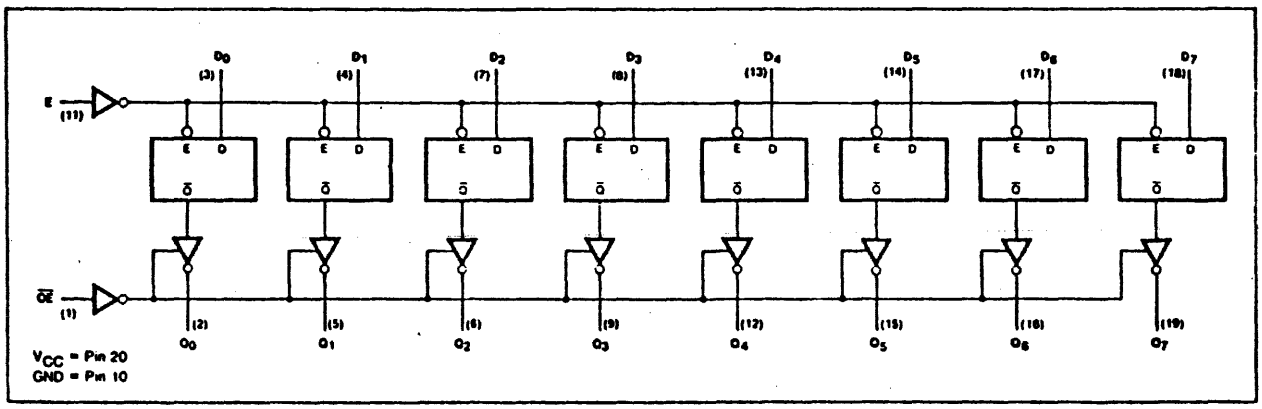
The 3-state output buffers are designed to drive heavily loaded 3-state buses, MOS memories, or MOS microprocessors. The active LOW Output Enable ($\overline{OE}$) controls all eight 3-state buffers independent of the latch operation. When $\overline{OE}$ is LOW, the latched or transparent data appears at the outputs. When $\overline{OE}$ is HIGH, the outputs are in the high impedance "off" state, which means they will neither drive nor load the bus.

MODE SELECT—FUNCTION TABLE

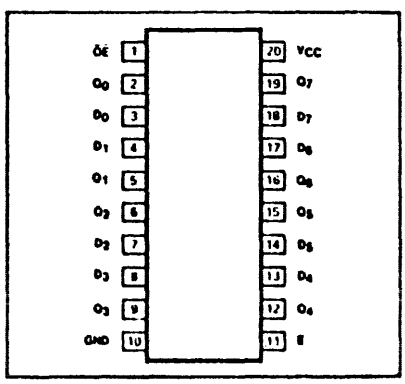
OPERATING MODES	INPUTS				OUTPUTS
	$\overline{OE}$	E	D_n	INTERNAL REGISTER	Q_0-Q_7
Enable & read register	L L	H H	L H	L H	L H
Latch & read register	L L	L L	l h	L H	L H
Latch register & disable outputs	H H	L L	l h	L H	(Z) (Z)

H = HIGH voltage level
h = HIGH voltage one setup time prior to the HIGH-to-LOW enable transition
L = LOW voltage level
l = LOW voltage level one setup time prior to the HIGH-to-LOW enable transition
(Z) = High impedance "off" state

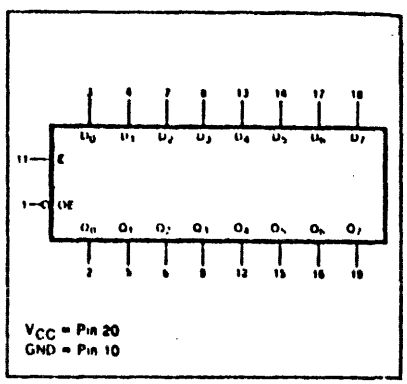
LOGIC DIAGRAM



PIN CONFIGURATION



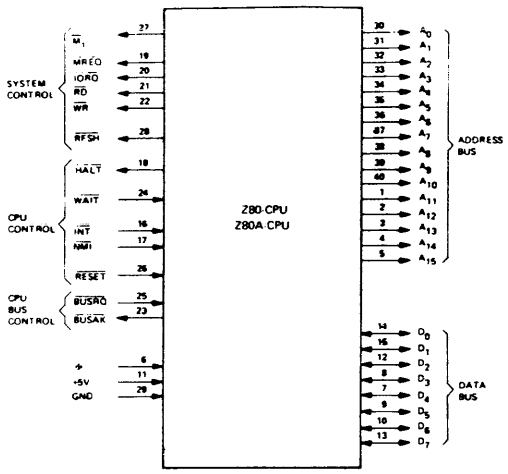
LOGIC SYMBOL



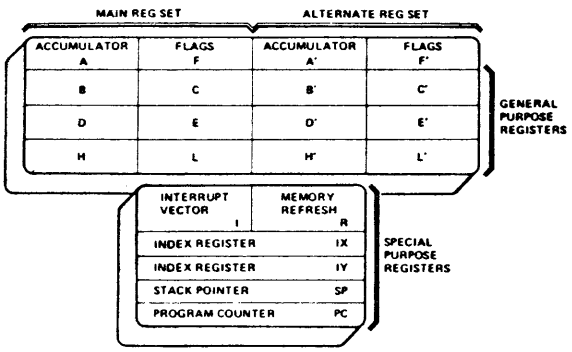
Z-80A

FEATURES

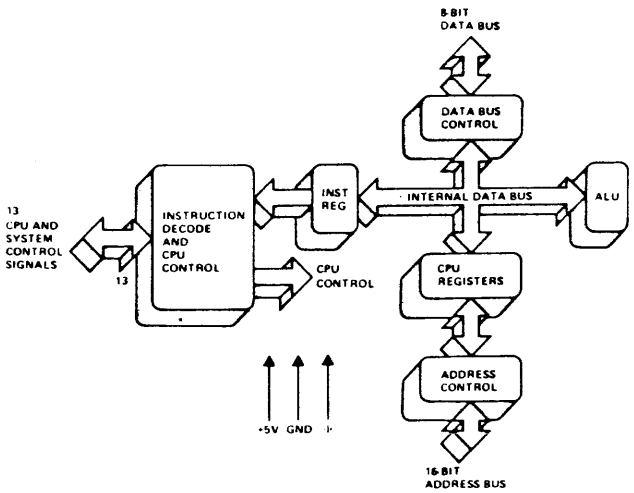
- Single chip, N-channel Silicon Gate CPU.
- 158 instructions–includes all 78 of the 8080A instructions with total software compatibility. New instructions include 4-, 8- and 16-bit operations with more useful addressing modes such as indexed, bit and relative.
- 17 internal registers.
- Three modes of fast interrupt response plus a non-maskable interrupt.
- Directly interfaces standard speed static or dynamic memories with virtually no external logic.
- 1.0 μs instruction execution speed.
- Single 5 VDC supply and single-phase 5 volt Clock.
- Out-performs any other single chip microcomputer in 4-, 8-, or 16-bit applications.
- All pins TTL Compatible
- Built-in dynamic RAM refresh circuitry.



Z80, Z80A CPU PIN CONFIGURATION



Z80, Z80A CPU REGISTERS



Z80, Z80A CPU BLOCK DIAGRAM

VT3 DOMESTIC CHARACTER SET

	0	1	2	3	4	5	6	7	8
0		▬	BLANK	0	@	P	`	p	
1		▌	!	1	A	Q	a	q	
2		▛	"	2	B	R	b	r	
3		▙	#	3	C	S	c	s	
4		▐	$	4	D	T	d	t	ϵ
5		▗	%	5	E	U	e	u	ζ
6		▄	&	6	F	V	f	v	η
7		▜	'	7	G	W	g	w	θ
8		▟	(	8	H	X	h	x	ι
9		▝	)	9	I	Y	i	y	κ
A		▞	*	:	J	Z	j	z	λ
B		—	+	;	K	[	k	{	μ
C		▏	,	<	L	\	l	¦	ν
D		┼	-	=	M	]	m	}	ξ
E		▔	.	>	N	^	n	~	ο
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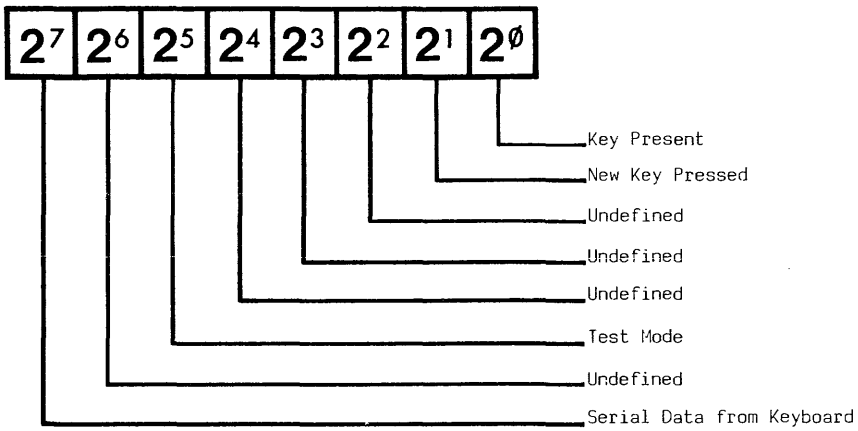
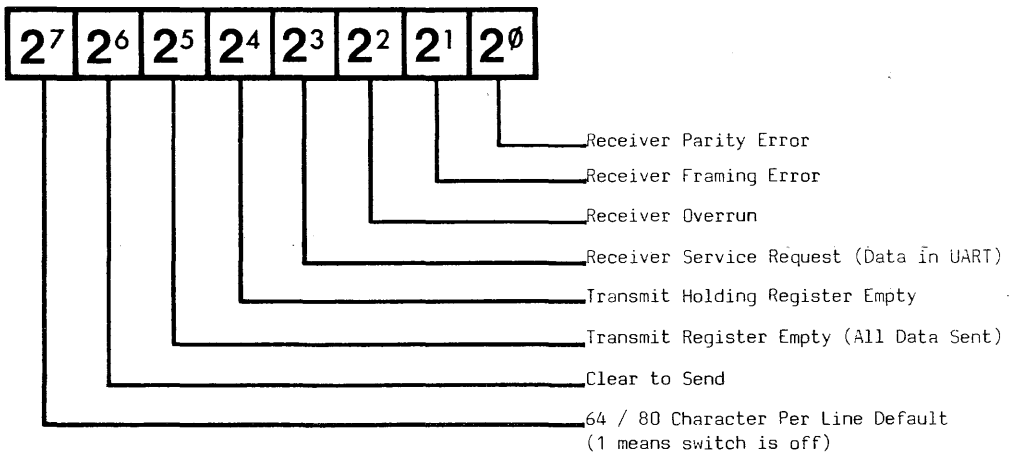
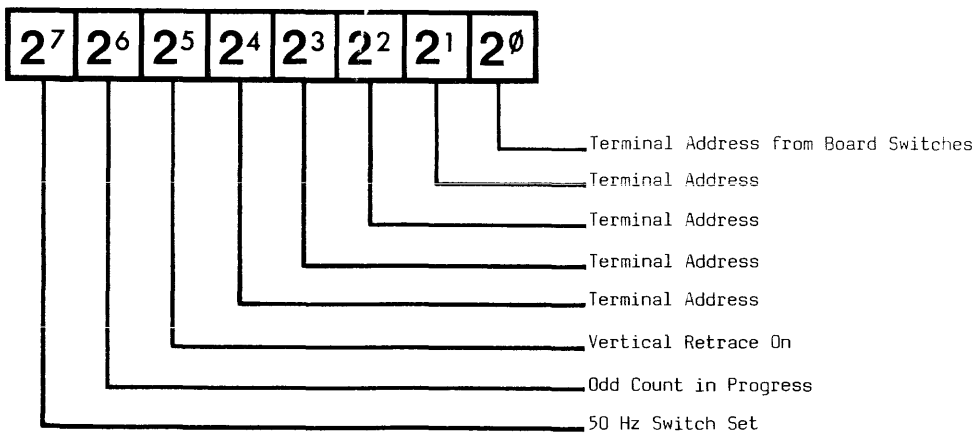
KEYBOARD STATUS



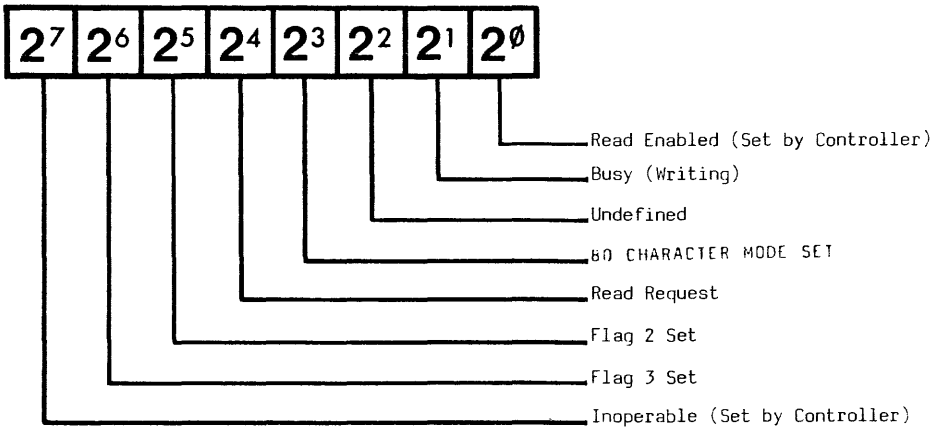
UART STATUS REGISTER AND 64 / 80 SWITCH



TERMINAL INFORMATION WORD



VT3 STATUS BYTE



This byte is produced during QSP exchanges by the VT3 to inform the IOU-39Q of status changes.

MEMORY DECODING

CHIP SELECT SIGNAL...	FOR SELECTING...	AD bus	Capacity
CSAØ	Program ROM	$0000 - 0FFF	4K
CSA1	Program ROM	$1000 - 1FFF	4K
CSA2	Display RAM	$2000 - 27FF	2K
CSA3	Initialize Scan Row	$3000 - 37FF	2K
CSA3	Blank Scan Row	* $38xx	
CSA4	Utility RAM	$4000 - 43FF	1K
CSA5	Utility RAM	$5000 - 53FF	1K
		* x = Don't care	

I/O DECODING

CHIP SELECT SIGNAL...	FOR SELECTING...	AD bus
CSC0	SELECT LINE LENGTH and CONTL-N - Load Status Register -	$8x
CSC1	STATE-N - Read UART Status Register -	$9x
CSC2	TRANL-N - Load Transmit Register	$Ax
CSC3	RECE-N - Read Receive Register -	$Bx
CSC4	CA - Set Request to Send	$Cx
CSC5	TERMINAL STATUS	$Dx
CSC6	KEYBOARD IN	$Ex
CSC7	KEYBOARD OUT	$Fx

Address Lines used: AD04 - AD07 and AD12 - AD15

D30807

NOTES
1. ALL RESISTORS IN OHMS UNLESS OTHERWISE SPECIFIED.
2. ALL CAP'S IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
3. RX - SELECTED FOR +5 ± .05V
4. RX - SELECTED FOR +15 ± .05V ON THE LOAD DURING INITIAL ADJUSTMENT.

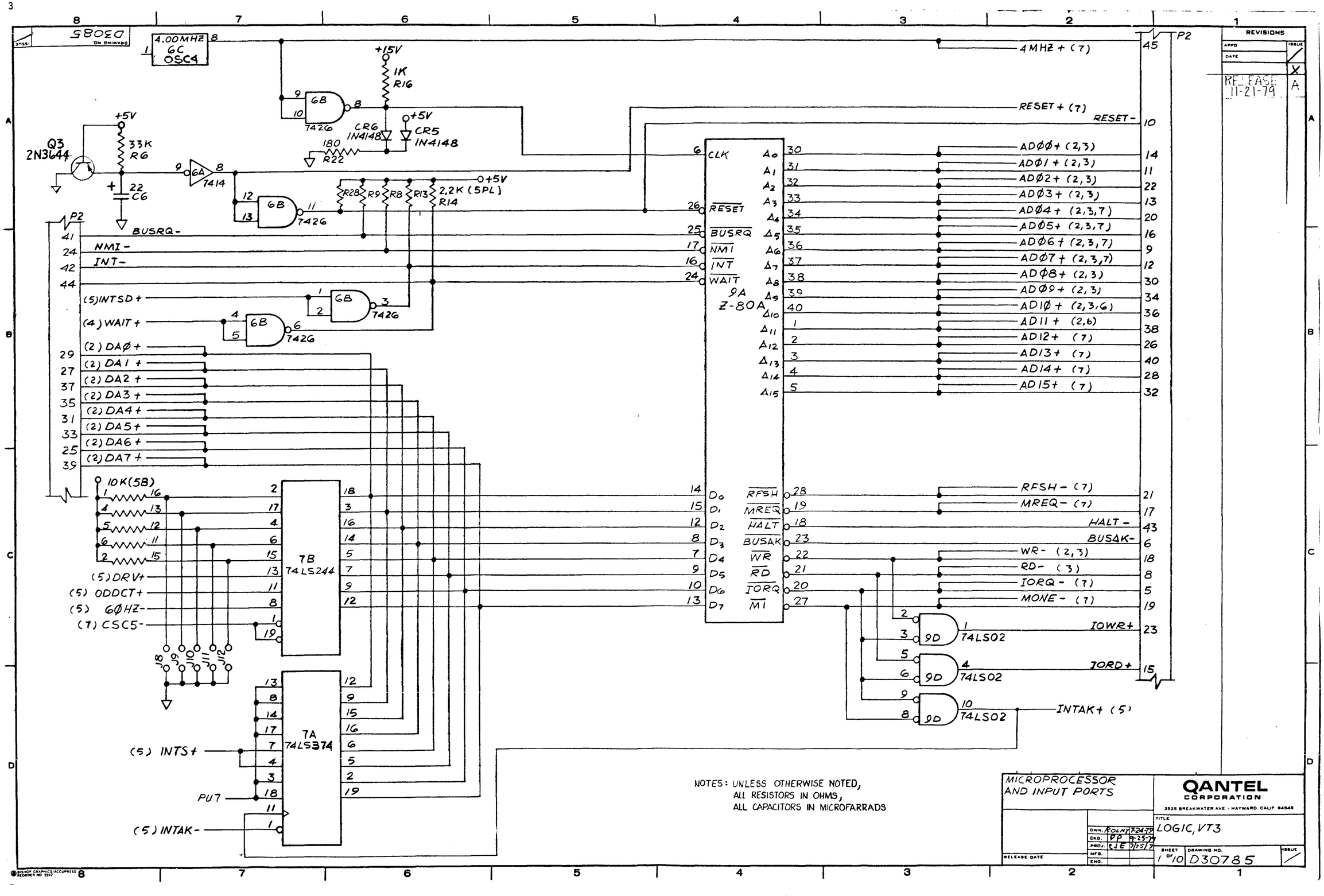
REVISIONS

APPD	DATE	BY	LTR
RELEASED			A
			B

J3
2
1
5
IN4002 D6
IN5401 D2
IN4002 D7
IN5401 D4
1000 C10, 35V
.001 C15
6,800 C9, 35V
6
3
4
IN5401 D5
IN5401 D3
15,000 C3, 16V
.001 C14
22 C11
1K R17
TIP34 Q1
475 R2 1%
.39 R16 3W
6.81K R3 1%
μA723 A
332 R1 1%
12.1K R7 1%
RX R6
12.1K R4 1%
10K R8 1%
.001 C1
2.2K R22
22 C4
.001 C16
+15V
J4
8
9
1K R20
Q2 TIP34
1K R14 1%
.10 R21 3W
22 C12
10K R10 1%
3.92K R13 1%
μA723 B
2.7K R15
RX R11
12.1K R12
.001 C2
100 R9
Q3 2N3642
47 R19
D1 5.6V
100 R5
1K R18
.1 C13
(2) 2N4441 SCR1 (1) (3)
2.2K R23
22 C5
.001 C17
+5V
1
2
3
GND
4
5
6
.1 C6
.1 C7
COM
IN
OUT
-12V
7912
2.2K R24
22 C8
-12V
12

POWER SUPPLY, VT3	QANTEL CORPORATION, 3525 BREAKWATER AVE · HAYWARD CALIF 94545		
	NEXT ASSY M42324	TITLE LOGIC, PS9, VT3	
	DWN. [illegible] 9/5/79		
	CKD [illegible] 9/5/79		
	PROJ [illegible] 9/5/79		
	MFG	SHEET 1 OF 1	DRAWING NO D30807
RELEASE DATE	ENG [illegible] 9/5/79		ISSUE A

BRUNOW GRAPHICS/ARTWORK/PRESS REORDER NO. 247



NOTES: UNLESS OTHERWISE NOTED,
ALL RESISTORS IN OHMS,
ALL CAPACITORS IN MICROFARRADS

MICROPROCESSOR AND INPUT PORTS

QANTEL CORPORATION
3525 BREAKWATER AVE. - HAYWARD, CALIF. 94545

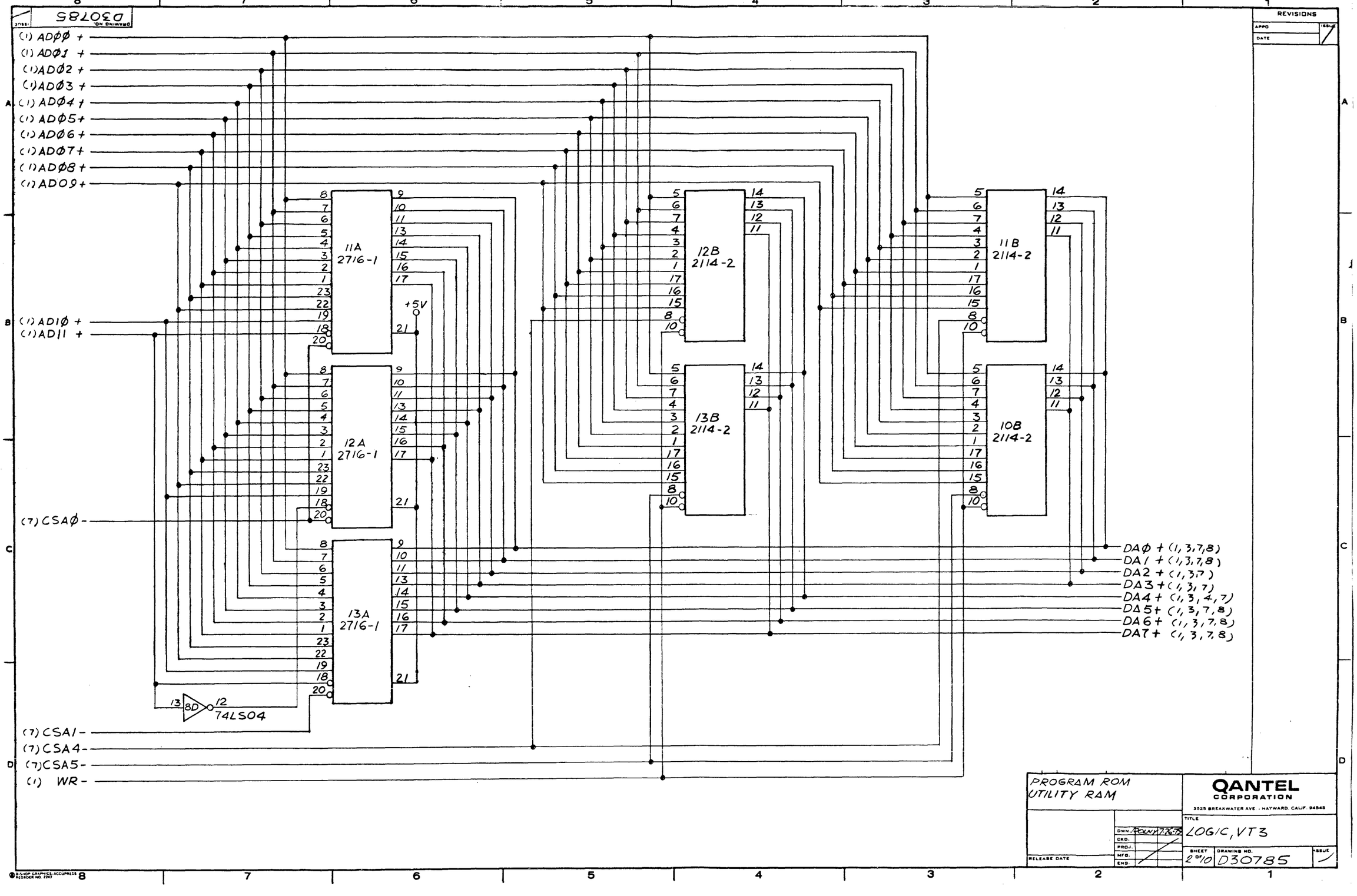
TITLE: LOGIC, VT3

DWN.	ROLNY	7-24-79
CKD.	PP	9-25-79
PROJ.	RJE	9-25-79
MFG.		
ENG.		

RELEASE DATE

SHEET 1 OF 10 | DRAWING NO. D30785 | ISSUE /

BISHOP GRAPHICS/ACCUPRESS REORDER NO 2267



REVISIONS

APPD	ISSUE
DATE	

PROGRAM ROM
UTILITY RAM

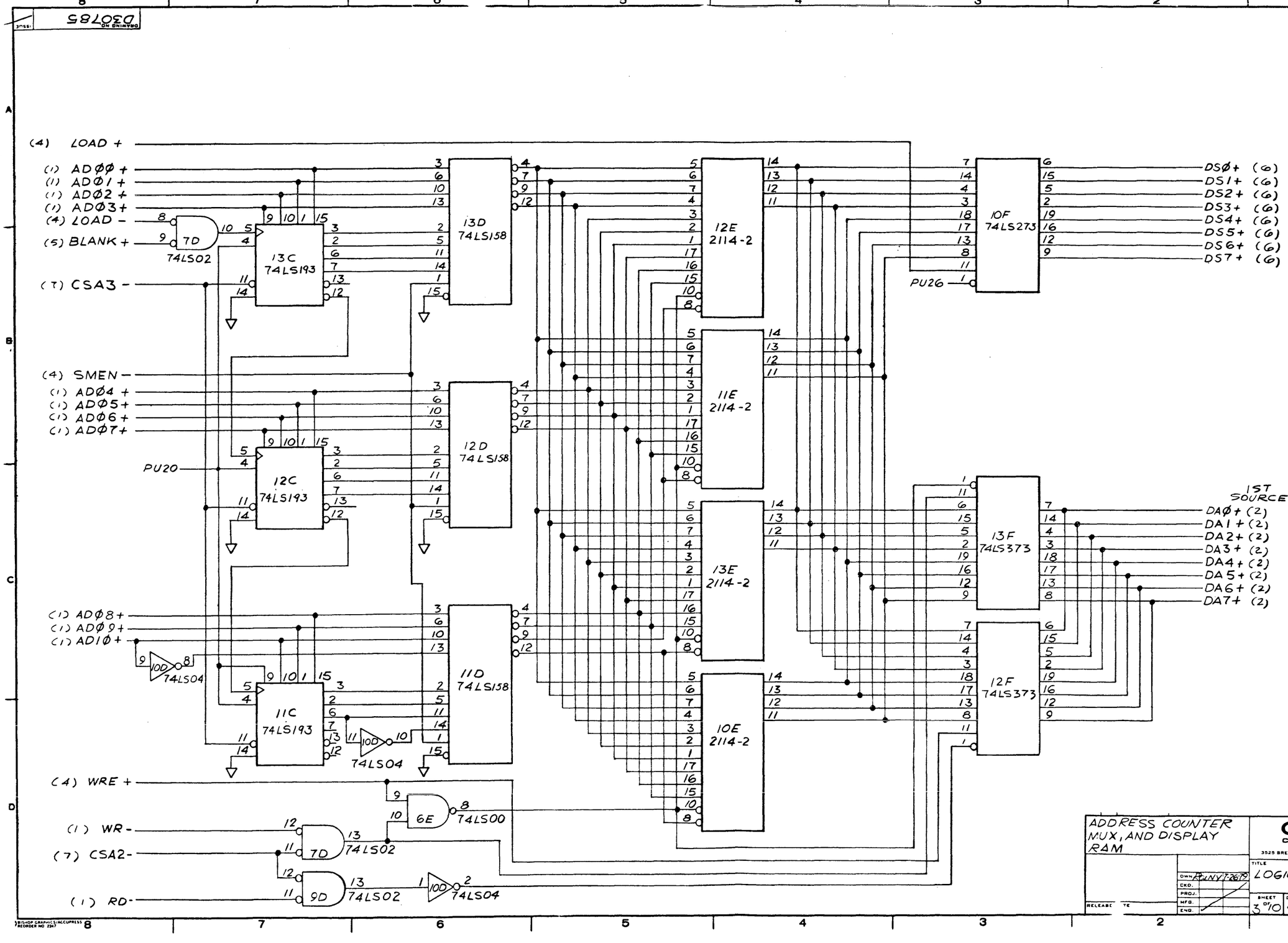
QANTEL CORPORATION
3525 BREAKWATER AVE. - HAYWARD, CALIF. 94545

TITLE: LOGIC, VT3

DWN.	
CKD.	
PROJ.	
MFG.	
ENG.	

RELEASE DATE

SHEET 2 OF 10 | DRAWING NO. D30785 | ISSUE 1



ISSUE	D30785
DRAWING NO.	

REVISIONS

APPD	ISSUE
DATE	

ADDRESS COUNTER MUX, AND DISPLAY RAM

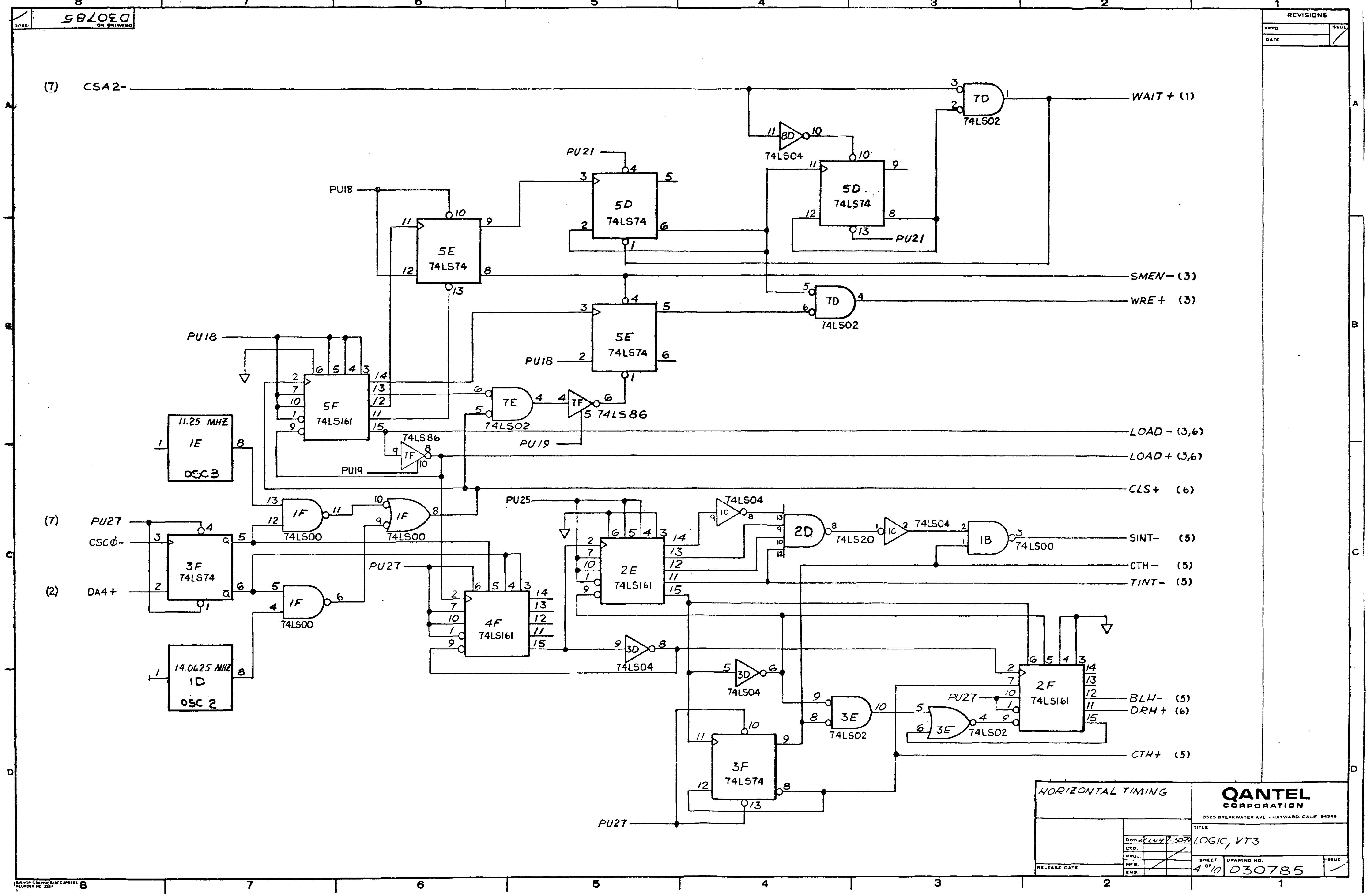
QANTEL CORPORATION
3525 BREAKWATER AVE · HAYWARD, CALIF. 94545

TITLE: LOGIC, VT3

DWN	RONNY 7-26-78
CKD.	
PROJ.	
MFG.	
ENG.	
RELEASE	

SHEET 3 OF 10 · DRAWING NO. D30785 · ISSUE /

BISHOP GRAPHICS/ACCUPRESS RECORDER NO. 2267



HORIZONTAL TIMING

QANTEL CORPORATION
3525 BREAKWATER AVE · HAYWARD, CALIF 94545

TITLE: LOGIC, VT3

SHEET 4 OF 10 · DRAWING NO. D30785

NOTE: J14 INSTALLED FOR 60 HZ OPERATION.

+5V
10K
R23
J14
10D 74LS04
7F 74LS86
6E 74LS00
60HZ- (1)
(4) CTH +
(4) CTH -
3C 74LS00
3E 74LS02
4E 74LS161
PU 25
3D 74LS04
6F 74LS74
PU19
PU21
6E 74LS00
IL-
3E 74LS02
ODDCT- (6)
4D 74LS161
3D 74LS04
4C 74LS74
PU17
4C 74LS74
DRV+ (1,6)
3C 74LS00
3C 74LS00
ODDCT +(1)
PU17
(4) BLH -
3C 74LS00
BLANK+(3)
3D 74LS04
BLANK-(6)
(1) INTAK+
3D 74LS04
INTAK- (1)
(4) SINT-
1B 74LS00
2C 74LS74
INTS+ (1)
1F 74LS00
(4) TINT -
2C 74LS74
PU17

REVISIONS
APPD | ISSUE
DATE

VERTICAL TIMING AND INTERUPT CONTROL

QANTEL CORPORATION
3525 BREAKWATER AVE - HAYWARD, CALIF 94545

TITLE: LOGIC, VT3
DWN: RONNY 73075
CKD.
PROJ.
MFG.
ENG.
RELEASE DATE
SHEET 5 OF 10
DRAWING NO. D30785
ISSUE 1

BISHOP GRAPHICS/ACCUPRESS REORDER NO. 2247

13

D30785

REVISIONS

APPD	ISSUE
DATE	

(5) DRV+
(5) ODDCT-
(4) DRH+
PU26
8E 74LS74
7E 74LS02
9E 74LS161
7E 74LS02
2D 74LS20
9F 2716-1
+5V
(3) DSØ+
(3) DS1+
(3) DS2+
(3) DS3+
(3) DS4+
(3) DS5+
(3) DS6+
(3) DS7+
(4) CLS+
(4) LOAD+
(4) LOAD-
1C 74LS04
1C 74LS04
1B 74LS00
PU19
8F 74LS166
INA
QH
7F 74LS86
7E 74LS02
8E 74LS74
1B 74LS00
1C 74LS04
+5V
470 R15
500 R24
VIDEO
P1
23
27
25
P1
DRHC+
DRVC-
(7) CSA3+
(1) AD11+
6F 74LS74
6E 74LS00
(5) BLANK-
1D 74LS04
1A 74LS273
2A 7437
2A 7437
PU1

CHARACTER GENERATOR AND CRT INTERFACE

QANTEL CORPORATION
3525 BREAKWATER AVE - HAYWARD CALIF 94545

TITLE	LOGIC, VT3	
DWN. PONY 7-30-79	SHEET 6 OF 10	DRAWING NO. D30785
CKD.		ISSUE
PROJ.		
MFG.		
ENG.		
RELEASE DATE		

BLUE-LINE GRAPHICS/ACCUPRESS REORDER NO. 2247

030785

REVISIONS

APPD		ISSUE
DATE		

(I) AD12+
(I) AD13+
(I) AD14+
(I) AD15+
(I) MREQ-
(I) RFSH-

10C 74LS138

CSAØ- (2)
CSA1- (2)
CSA2- (3,4)
CSA3- (3,6)
CSA4- (2)
CSA5- (2)

(I) ADØ4+
(I) ADØ5+
(I) ADØ6+
(I) MØNE-
(I) IORQ-
(I) ADØ7+

9C 74LS138

8D 74LS04

CSCØ- (4)
CSC1- (8)
CSC4- (8)
CSC5- (1)
CSC6- (8)
CSC7- (8)

P1 BB 12 — 680K R4 — 10K (5B) — .001 C8 — 2B 339 — +5V — 2.2K (3B)

(I) RESET+

8A 1863B

RI, RRC, TRC, CRL, SFD, THRL, RRD, DRR, MR, SBS, WLS2, WLS1, PI, EPE, TRI, TR2, TR3, TR4, TR5, TR6, TR7, TR8
TRO, TRE, PE, FE, OE, DR, THRE, RRI, RR2, RR3, RR4, RR5, RR6, RR7, RR8

PU7 — 8D 74LS04

+5V — 27K R10 — 10K (5B) — 2B 339 — 2.2K (3B) — +15V — Q1 2N3644 — CR3 IN4148 — 270 R11 — P1 9

BIAS+(8)
TRE+(8)

DAØ+ (2)
DA1+ (2)
DA2+ (2)
DA3+ (2)
DA4+ (2)
DA5+ (2)
DA6+ (2)
DA7+ (2)

PU21 — 4MHZ+ — 6D 74LS161 — 8D — J1 19.2K

7C 4040 — J2 9.6K, J3 4.8K, J4 2.4K, J5 1.2K, J6 600, J7 300

BAUD RATE GENERATOR AND USART

QANTEL CORPORATION
3525 BREAKWATER AVE. - HAYWARD, CALIF. 94545

TITLE: LOGIC, VT3

DWN. ROLNY 7-30-79
CKD.
PROJ.
MFG.
ENG.
RELEASE DATE

SHEET 7 OF 10 — DRAWING NO. 030785 — ISSUE

D30785

REVISIONS

APPD	ISSUE
DATE	

P1

20 STROBE+ R3 470 — C5 100pF — 3 6A 4 7414

19 DKEY+

11 680K R2 — 10K(5B) — .001 C7 — 5 2B 4 339 2

+5V 10K R5

J13

NOTE : J13 INSTALLED FOR 64 CHARACTER PER LINE DEFAULT CONDITION.

R29 +5V 10K J15

NOTE : J15 INSTALLED FOR SELF TEST

+5V 2.2K (3B) 10 7

5A 74LS244

6 8 4 2 1 13 15 11 17 19 → 14 12 16 18 7 5 9 3

1ST SOURCE

DAØ + (2)
DA1 + (2)
DA5+ (2)
DA6+ (2)
DA7+ (2)

PU1

4A 74LS74 — 3 4 5 — 2 6 — 1 10 9 — 11 12 8 — 13

2A 7437 — 1 2 3

2A 7437 — 12 13 11

ALARM— → P1 18

CLOCK + → 17

3A 74LS74 — 3 4 5 — 2 6 — 1

+15 V

3A 74LS74 — 11 12 9 — 10 8 — 13

2B 339 — 10 11 13

2.2K (3B) RP3 — 3 14 — 13 4

Q2 2N3644

IN4148 CR4

270 R12. 1/2W → 10

(7) CSC6-
(7) TRE +
(7) CSC1-
(7) CSC7-
(7) CSC4-
(7) BIAS +

P1 5 3 4 33 34 1 2 22 24 26 28 35 36 6

+15V
+5V
GND
-12 V

+ 22 15V C1,C2

.047 47 PL.

IN4001 CR1 +15 VT → 7 8

IN4001 CR2 -12 VT

+ 22 16V C4

+ 22 16V C3

P2 3 4 47 48 1 2 49 50

+5V
GND

R1 PU 1
R7 PU 7
R17 PU 17
R18 PU 18
R19 PU 19
R20 PU 20
R21 PU 21
R25 PU 25
R26 PU 26
R27 PU 27

KEYBOARD INTERFACE AND DC VOLTAGE

QANTEL CORPORATION
3525 BREAKWATER AVE - HAYWARD, CALIF 94545

TITLE: LOGIC, VT3

DWN.	JAN 3-1-79
CKD.	
PROJ.	
MFG.	
ENG.	
RELEASE DATE	

SHEET 8 OF 10 | DRAWING NO. D30785 | ISSUE 1

BISHOP GRAPHICS/ACCUPRESS REORDER NO 2247

D30785 ON ONIMYRO

REVISIONS

APPD	ISSUE
DATE	

J1

GND	1
GND	2
+5V	3
+5V	4
+15V	5
-12V	6
+5V	33
+5V	34
GND	35
GND	36
V+	7
V-	8
XMITD	9
REQTOS	10
CLRTOS	11
RCVDD	12
RDY	13
GND	24
CLOCK+	17
ALARM -	18
DKEY +	19
STROBE+	20
GND	22
VIDEO	23
DRVC -	25
GND	26
DRHC +	27
GND	28

CONTROL BOARD

P4

4	GND
1	+5V
3	+5V
9	+15V
12	-12V
2	+5V
5	GND
6	GND
8	+15V

POWER SUPPLY

RS232

J5: 7, 23, 24, 2, 4, 5, 3, 20, 1

J6: 23, 24, 2, 4, 5, 3, 20, 1, 7

J7: 3, 6, 1, 4, 2, 7, 5

KEYBOARD

J3: 8, 9, 10, 6, 1, 7, 5, 2, 3, 4

CRT

2	LEFT
3	RT
4	CNTR

POT

SIGNAL AND DC POWER DISTRIBUTION

QANTEL CORPORATION
3525 BREAKWATER AVE. - HAYWARD, CALIF. 94545

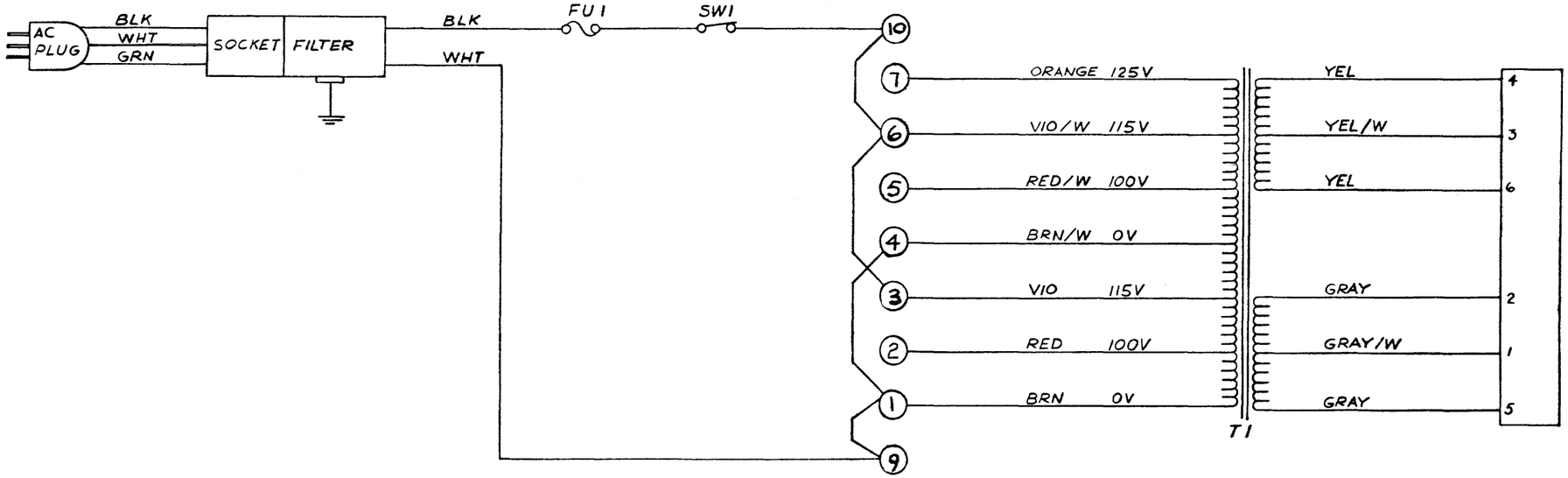
DWN.	RO&MT 7-31-79
CKD.	
PROJ.	
MFG.	
ENG.	
RELEASE DATE	

TITLE: LOGIC, VT3

SHEET 9 OF 10 | DRAWING NO. D30785 | ISSUE /

ISSUE	DRAWING NO.
/	D30785

INPUT VOLTAGE	JUMPERS			
	#1	#2	#3	#4
100	10-5	5-2	9-4	4-1
115	10-6	6-3	9-4	4-1
215	10-5	4-3	9-1	—
230	10-6	4-3	9-1	—
240	10-7	4-3	9-1	—



DATE /

TRANSFORMER WIRING DIAGRAM

QANTEL CORPORATION
3525 BREAKWATER AVE - HAYWARD, CALIF 94545

DWN ROLNY 7-3-79	TITLE	LOGIC, VT3
CKD.		
PROJ.		
MFG.	SHEET 10 OF 10	DRAWING NO. D30785
ENG.		ISSUE /
RELEASE DATE		