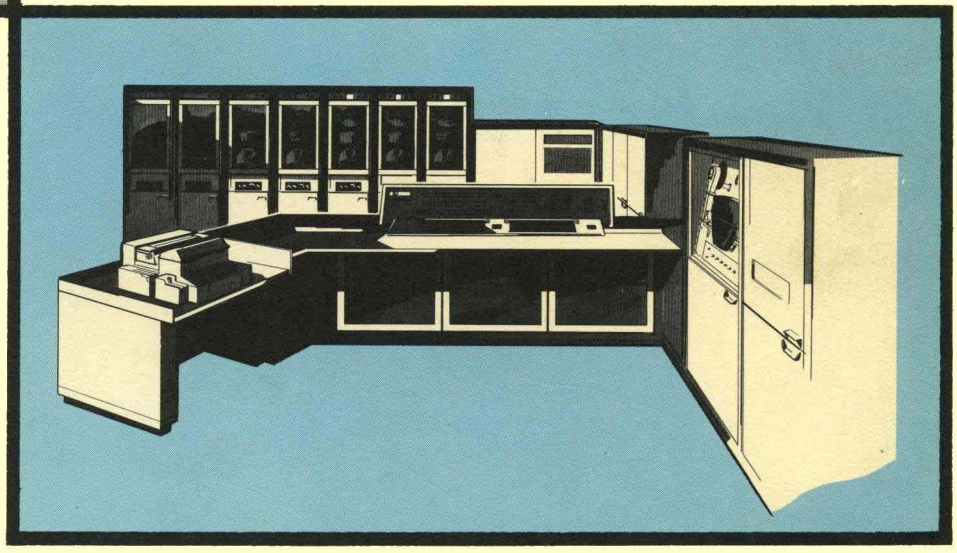
transac® S-2000

Systems Description



PHILCO®

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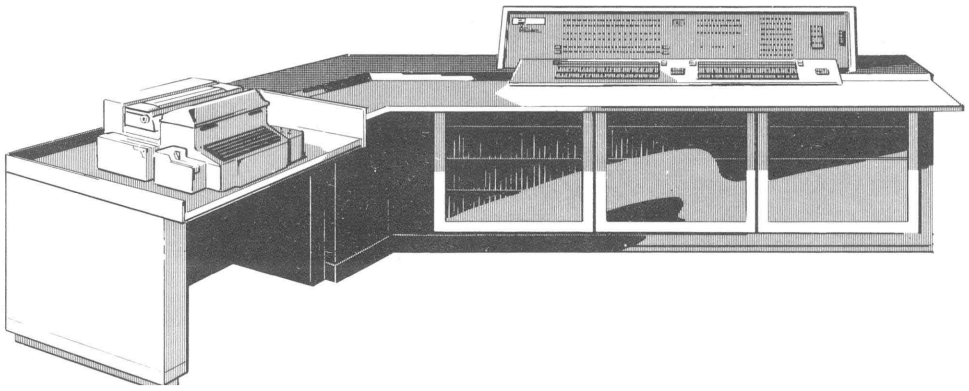
S-2000



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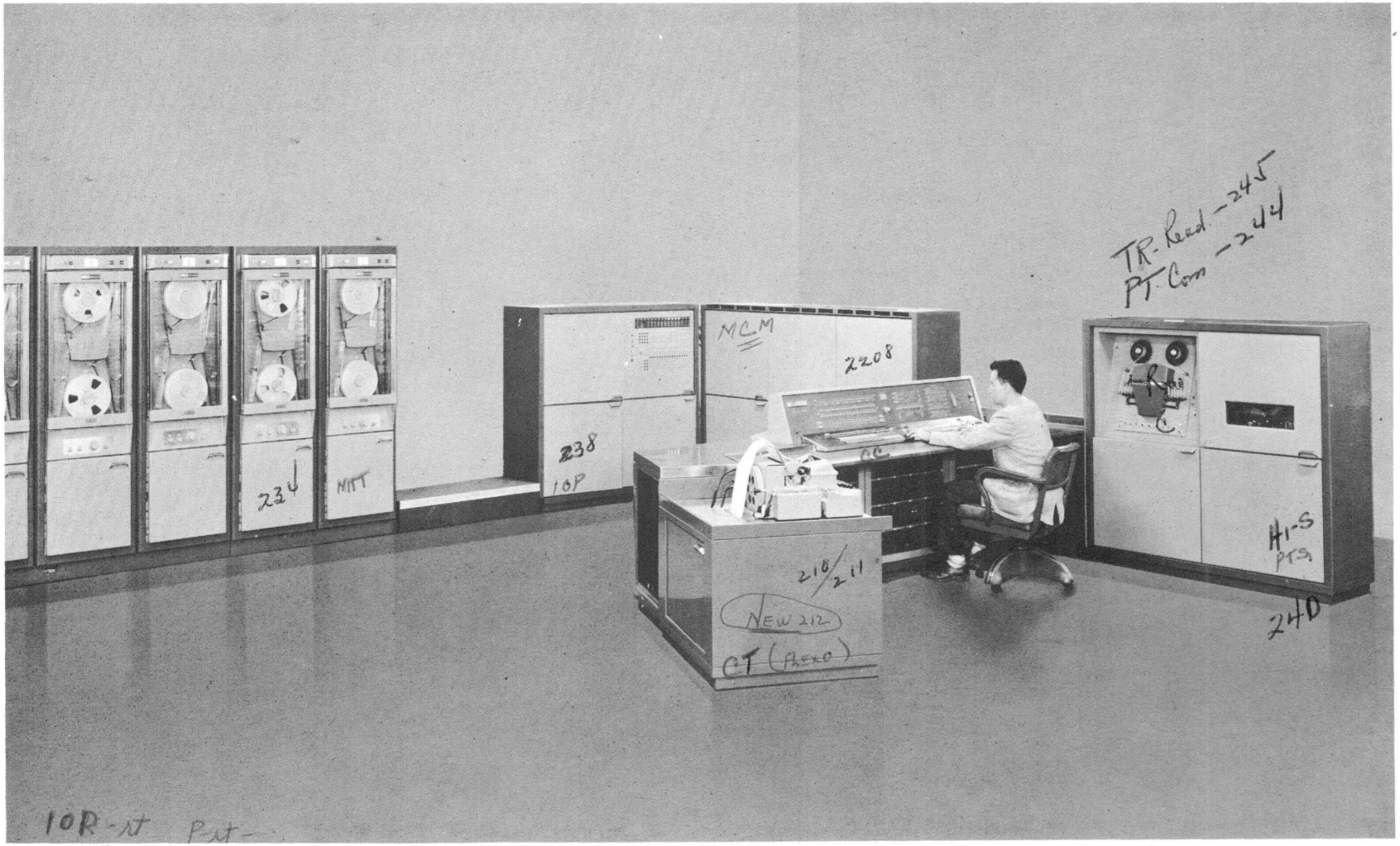

TRANSAC S-2000 System

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SECTION I

HIGHLIGHTS

There are many features which make the TRANSAC S-2000 the outstanding large-scale electronic data-processing system. One important fact to consider is that TRANSAC S-2000 is commercially-available today. A number of other TRANSAC features which are of general interest have been summarized in this section. These features should be compared with those of other systems existing or proposed, to realize the extent of the improvements and technological advances that exist in TRANSAC. Since Philco announced its design specifications, other companies have included similar features in their new, proposed systems. Philco, by producing the first large-scale transistorized EDP system, has opened the path to faster, more reliable, and more economical EDP systems which have revolutionized computer technology.

ECONOMY

No factor is more important in the consideration of a large-scale EDP system than the total of its various costs. TRANSAC was designed for maximum economy throughout the system and in all activities supporting the system.

1. In installation - minimum floor space, air conditioning, duct-work, false floors and ceilings; minimum rigging costs.

2. In programming - minimum coding through provision of complete automatic programming systems, easily-learned mnemonic code, large variety of instructions, many program checking techniques and routines.

3. In operation - fastest available system, low power consumption, fast tape loading and unloading, input-output devices switched on- or off-line by pushbuttons, off-line media conversions facilitated by electronic switching to connect the two units.

4. In maintenance - interchangeable and standardized logic cards, diagnostic routines, extremely reliable long-life components, derated circuits (operated at less than capacity), computer simulators to check logic cards.

5. In initial cost - fewer units needed due to high operating speeds and flexibility of each unit, prices based on mass-production methods, provision for constant expansion and modernization.

6. In storage - data compression reduces amounts of media to be stored, high character density reduces number of magnetic tapes.

NON-OBSOLESCENCE FACTOR

A number of EDP systems which were widely-publicized when they were designed became obsolete before the first few installations were completed. Subsequently, manufacture of these systems had to be discontinued. This situation, while caused by the planning of the manufacturer, may be disastrous for the customer who has invested several years and thousands of dollars into systems design, programming, installation, and training. TRANSAC contains numerous features which will prevent the TRANSAC system from becoming obsolete.

1. Modular construction

Throughout the system, a logical unit was adopted, standardized, and duplicated as many times as needed to accomplish its function. The smallest logical unit is the transistor module which holds four transistors and their supporting components. Up to eighteen transistor modules are mounted on a plug-in type printed circuit logic card which is manufactured in standard circuits. Up to 96 logic cards plug into a unit module. Each TRANSAC unit contains one or more unit modules. By packaging TRANSAC in these modular units, the thousands of components can be joined in standard units that fit together in an organized fashion to perform the functions of the system. Expansion, modification, and maintenance are greatly facilitated.

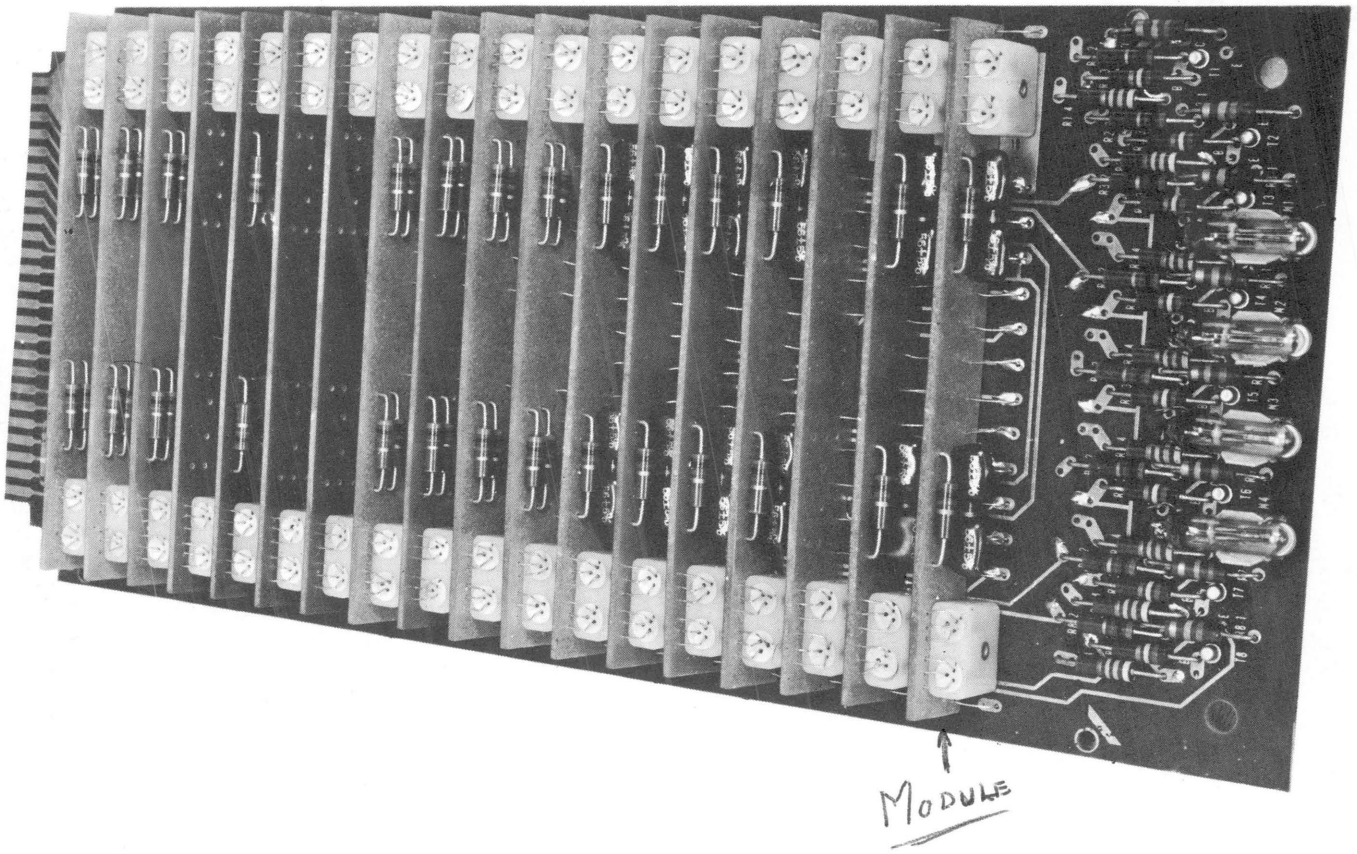
2. Automated Production

To make TRANSAC by mass-production methods, each logical unit must be interchangeable with any other similar unit. Mass production is not common in the large-scale EDP field; however, Philco has adopted automatic production methods and quality control techniques for TRANSAC. Philco transistor production techniques, for example, have been automated by such methods as the Fast Automatic Transfer (FAT) line which can produce 450 transistors per hour with nine operators. Experience in military systems production has greatly reduced the lead-time from design to production and enabled Philco to be the first to deliver a number of new developments to the field.

3. Modular expansion to large capacity

Each functional section of the TRANSAC system can be greatly expanded as illustrated by Figure 6-A. As the data-processing load increases, the installed TRANSAC system may be expanded. Only the capacity needed is provided, thus minimizing costs. New units can be installed during non-operating periods with little changeover time required. These new units may be for replacement, additional capacity or because of new developments.

Because of TRANSAC's asynchronous logic, new components, components now being developed, and design improvements may be



Arithmetic Register Chassis Card

incorporated without modifying existing systems. While it is not possible to mention all of the potential changes, a few of the more important ones are listed below.

a. Central Processor Unit - Faster transistors, developed by Philco, have already been incorporated in the system. There are now two central processors available, which differ only by the transistors used. One operates at a faster rate than the other.

b. Magnetic Core Storage Unit - Units with two microsecond access time may now be ordered. A complete description of these units will be found in another publication.

c. Input-output systems - Other input-output units are in development and may be added to the TRANSAC system easily. Many of these units such as data plotters, character generators, and character recognition devices may be ordered now as special units.

BALANCED SPEED AND FLEXIBILITY

For many data-processing applications, the EDP system is limited by the speed and capacity of its input-output equipment. In this case the high speed of its central processor may be dissipated. Therefore, increasing the input-output processing rates will substantially reduce the cost per unit of computer time for processing records.

TRANSAC's input-output and central processor speeds are among the highest available as may be seen by comparing the specifications listed in Section III with those of other systems. These speeds may be balanced for each application by selecting input-output equipment to correspond with the amounts of input-output processing and central computer processing. In this way TRANSAC can balance its high data-processing speeds with extreme system flexibility to produce maximum efficiency.

TRULY GENERAL PURPOSE

A TRANSAC system may be selected for commercial, scientific, real-time, and military applications. Each of these types has special characteristics which are often handled by four different systems. For example, commercial applications may require high input-output volumes, minimum and simple computations, and large permanent files. TRANSAC handles problems of this class by providing high input-output processing rates and a large number of magnetic tape units. The permanent files may be compressed and stored on magnetic tape reels using TRANSAC's data compression feature.

Scientific applications may require minimum input-output volumes but maximum and complex computations. A TRANSAC system with only paper tape input-output and the central processor's high speed will handle these problems very economically.

Real-time and military systems may need data-transmission facilities, provision for enormous internal and external storage, and maximum reliability. Many TRANSAC features contribute to make a system that is well adapted for these applications. Philco is a leader in the field of communications and transmission equipment. TRANSAC, itself, was an outgrowth of military computers designed and manufactured for the government. Reliability and storage capacity were of prime importance in its design.

A truly general purpose system may be ordered for a specific application and then expanded or modified for use in other applications. This allows one versatile system to service many departments of a company or agency. The fact that TRANSAC systems have been ordered for all these applications indicates that TRANSAC meets all the criteria for a truly general purpose system.

DESIGNED FOR AUTOMATIC PROGRAMMING

Instructions, controls, the library of routines, and automatic programs should make use of the most recent techniques for simplifying and speeding the programming task. In some types of problems, half of the operating cost may consist of the program preparation and checkout costs. In addition, long lead-times may cut down the flexibility of a system to the

point that some applications become impractical. Many of these problems can be minimized through advanced automatic programming techniques. These techniques are available to the TRANSAC user today. The computing system and its programming system are delivered together-- truly a first in the computer field.

The automatic programs and techniques used with TRANSAC are discussed in detail in Section IV. These techniques and programs minimize the length of the running program and eliminate machine coding. The short lead-time needed provides maximum flexibility of applications. Present user-personnel can easily learn to operate the TRANSAC system and management is afforded more direct communication with the system.

With these features in mind read the following sections and compare TRANSAC with your present or proposed systems. The specifications are conservative and represent actual machine experience - not estimates.

SECTION II

FUNCTIONAL DESCRIPTION

THE SYSTEM

The functional organization of the TRANSAC S-2000 may be divided into two main sections: the central computer, and the input-output sections. The Central Computer performs the functions of storage, processing, and operator control. TRANSAC contains both scheduled and real-time types of input-output equipment. In general the input-output equipments convert the data from media form into six-bit characters and then assemble these characters into words and blocks for quick transfer into storage. During an output operation the process is performed in reverse. Figure 2-A shows the TRANSAC systems by functional areas and types of equipment.

THE CENTRAL COMPUTER

Storage, processing, and operator controls are performed by the central computer. At present two types of storage equipment are furnished with the S-2000: internal-memory (magnetic core) and auxiliary (magnetic drum) storage. (The input-output systems provide an unlimited amount of external storage in the form of magnetic tape, punched cards, and paper tape). Processing is divided into program and data-processing while operator control is performed through the console typewriter, the manual switches and keyboards, and the display indicators.

Information moves through the central computer in word form. A TRANSAC word is composed of 48 bits, numbered left to right from 0 to 47 which are transferred throughout the central computer in parallel. The word may contain any of the types of representation shown in Figure 2-B, a combination of these, a 47-bit number with a sign bit, a constant, or an instruction word containing two instructions.

FUNCTIONAL ORGANIZATION

TRANSAC S-2000 ELECTRONIC DATA PROCESSING SYSTEM

MAIN FUNCTIONAL SECTIONS

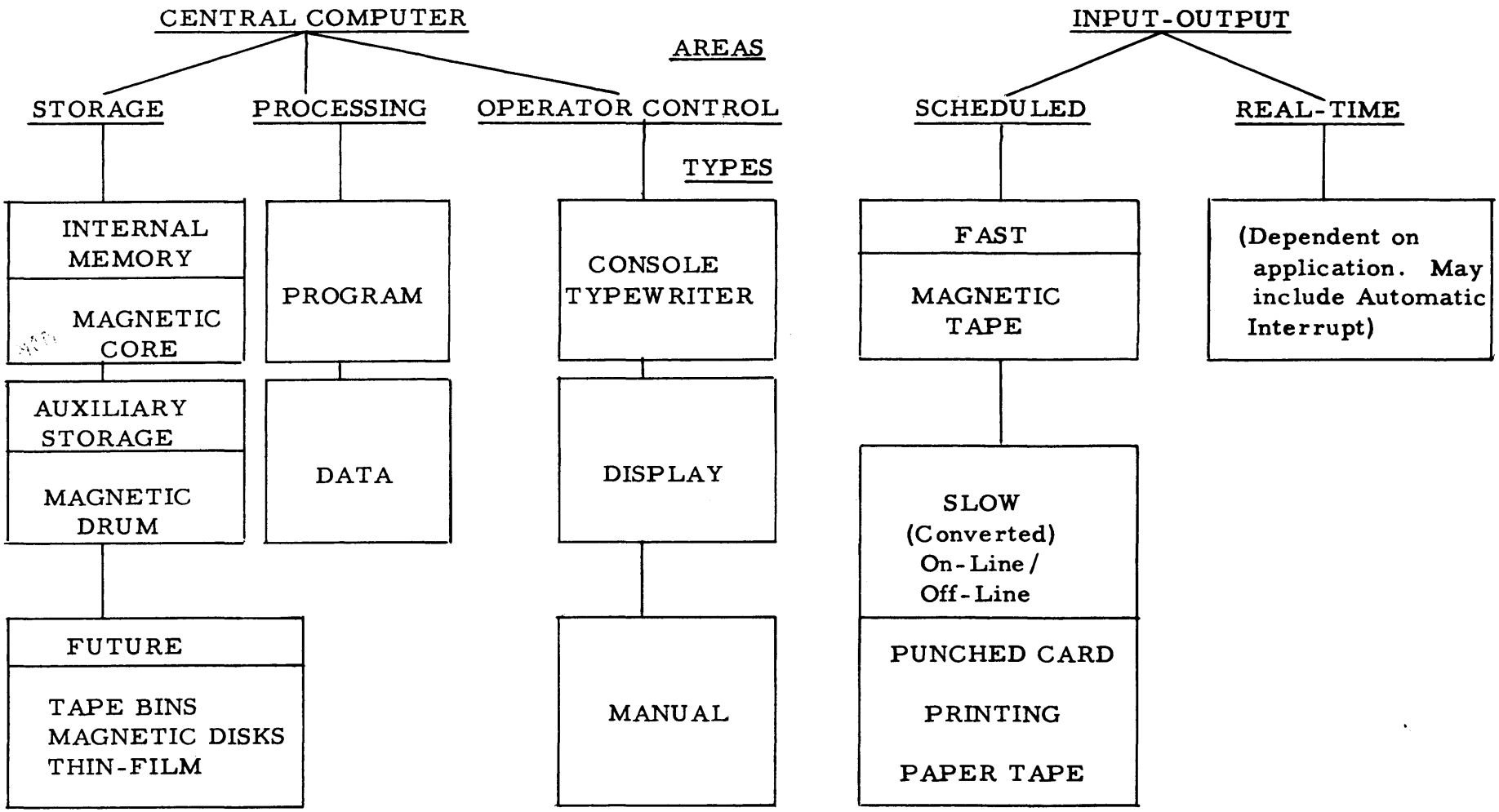
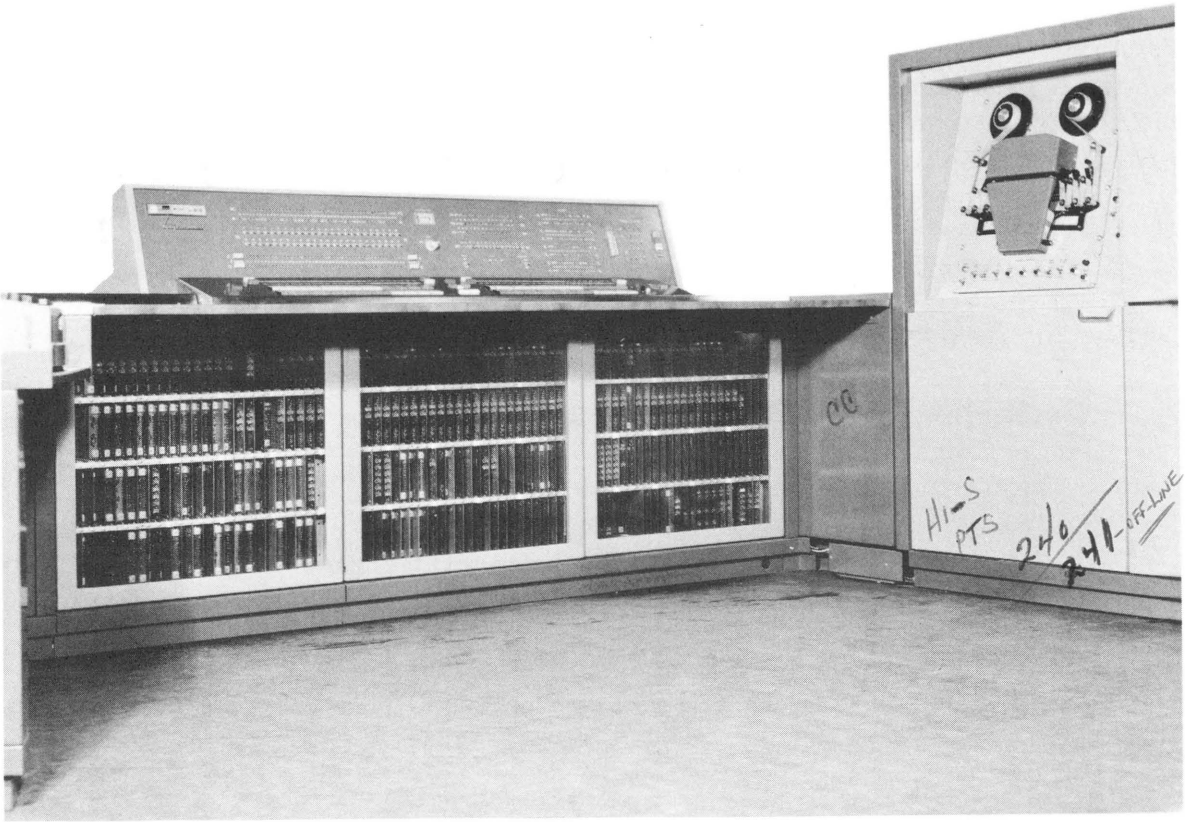


Figure 2-A



MODEL #210 SLOW TYPE "XSTOR"
#211 FASTER TYPE TRANSISTOR
#212

Central Computer and Paper Tape System

STORAGE

The storage functions, represented by internal memory and auxiliary storage, are shown in Figure 2-A. The input-output equipment also provides external storage.

Auxiliary storage differs from internal memory in use and access speed. It stores reference information, such as large tables and subroutines for a program. This information is then called into the internal memory, the highest speed storage, shortly before it is needed.

This facilitates fast information accessibility without slowing down the central computer.

MAGNETIC CORE STORAGE

The main internal storage or memory consists of up to eight magnetic core storage units. Each unit can store 4096 words, 48 binary digits in length, Each word may be individually addressed by its memory location.

With the flexibility in methods of representation shown below by Figure 2-B, each unit can store a maximum amount of data in the space available.

Figure 2-B

REPRESENTATION		STORAGE CAPACITY		
Type of Representation	Number of bits to represent one unit of each type	One TRANSAC Word	One Magnetic Core Unit	Eight Magnetic Core Units
Word	48 (bits/word)	1 (word)	4096 (words)	32,768 (words)
Alpha-Numeric Characters	6 (bits/character)	8 (characters)	32,768 (characters)	262,144 (characters)
Binary-Coded Decimal	4 (bits/digit)	12 (digits)	49,152 (digits)	393,216 (digits)
Hexadecimal	4 (bits/digit)	12 (digits)	49,152 (digits)	393,216 (digits)
Octal	3 (bits/digit)	16 (digits)	65,536 (digits)	524,288 (digits)
Pure Binary	1 (bits/bit)	48 (bits)	196,608 (bits)	1,572,864 (bits)
Decimal Equivalent of Binary (In digits)	3-4 (bits/digit)	14 + (digits)	57,344 + (digits)	458, 752+ (digits)

Memory Sharing

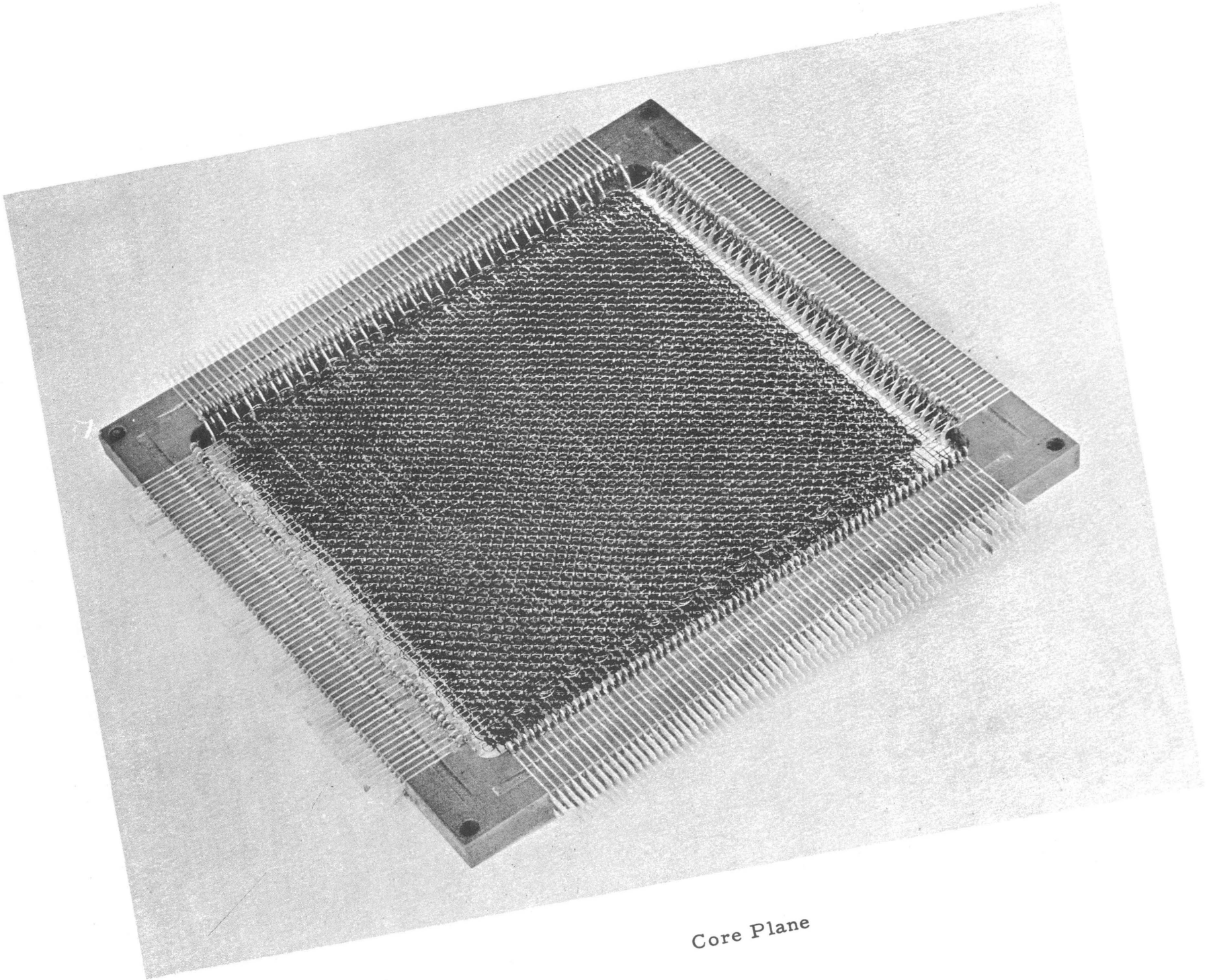
The magnetic core storage is shared by the central processor, the input-output processor, and the real-time or paper tape channel. This sharing process interweaves the memory accesses by the various units so that no unit must wait more than a few microseconds to use the memory. Therefore, with memory sharing, the program can run almost continuously without interruption by input-output operations.

Memory-sharing operates by assigning memory-access priorities to the input-output processor, real-time channel, central processor unit, and the magnetic drum system in this order. Since the input-output processor and the real-time channel operate dynamic (moving) devices, they are assigned priorities higher than the central processor which is a static and asynchronous unit. The magnetic drum system is assigned lowest priority because it does not participate in memory-sharing. A priority is assigned for each new input-output instruction or central processor request for memory access. Additional processing economy is achieved by allowing other units to access the memory (in the order of priority) during the time a high-priority unit is performing an input-output instruction.

For example, the input-output processor uses a standard 90,000 character per second transmission speed for all its input-output channels. At this speed 8 characters (alphanumeric) or one TRANSAC word is assembled in an input-output channel every 88 microseconds leaving the memory free for 78 out of every 88 microseconds. These 78 microseconds may be used in the sequence of the assigned priorities for 10-microsecond memory accesses by other multiplexed input-output channels, the real-time channel, and the central processor. Through this sharing procedure the memory may be accessed up to eight times during one 88-microsecond interval.

Memory Cycle

Words are read from or written into the magnetic core storage in two cycles: a 4-microsecond read cycle and a 6-microsecond restore cycle. So, for any location of magnetic core storage, a word may be transferred in or out within 10 microseconds.



Core Plane

When a word is read from memory, the read cycle reads and clears the memory location while the restore cycle restores the contents of the memory location accessed. When storing a word in memory, the read cycle clears the memory location and the restore cycle stores the word in the accessed memory location.

Substantial program running time is saved in TRANSAC because words read from memory may be operated on during the restore cycle. For example, if the operation is one that takes more than six microseconds, such as multiplication, the restore cycle is completely overlapped and the effective memory access time is only four microseconds. This is illustrated in the following diagram, Figure 2-C.

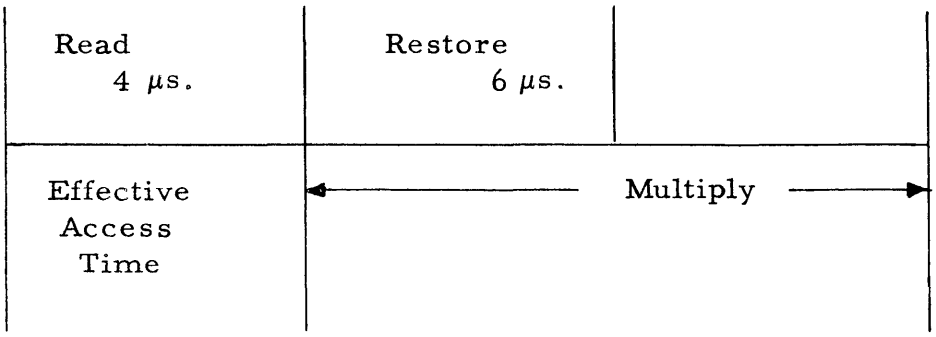


Figure 2-C

Note also that an input-output unit can access the memory while the multiplication is in progress, after the restore cycle.

Split Memory Cycle

Split memory cycling saves time when the operation requires that the result be replaced in the original memory location. The time to add a word from memory and replace it by the sum is 4 microseconds, plus the addition, plus 6 microseconds. The effective access time is therefore 5 microseconds. In contrast to this, unsplit memory cycle operations require two complete memory accesses plus the arithmetic operation. Therefore a saving of 10 microseconds is realized during every replace type operation as shown in Figure 2-D.

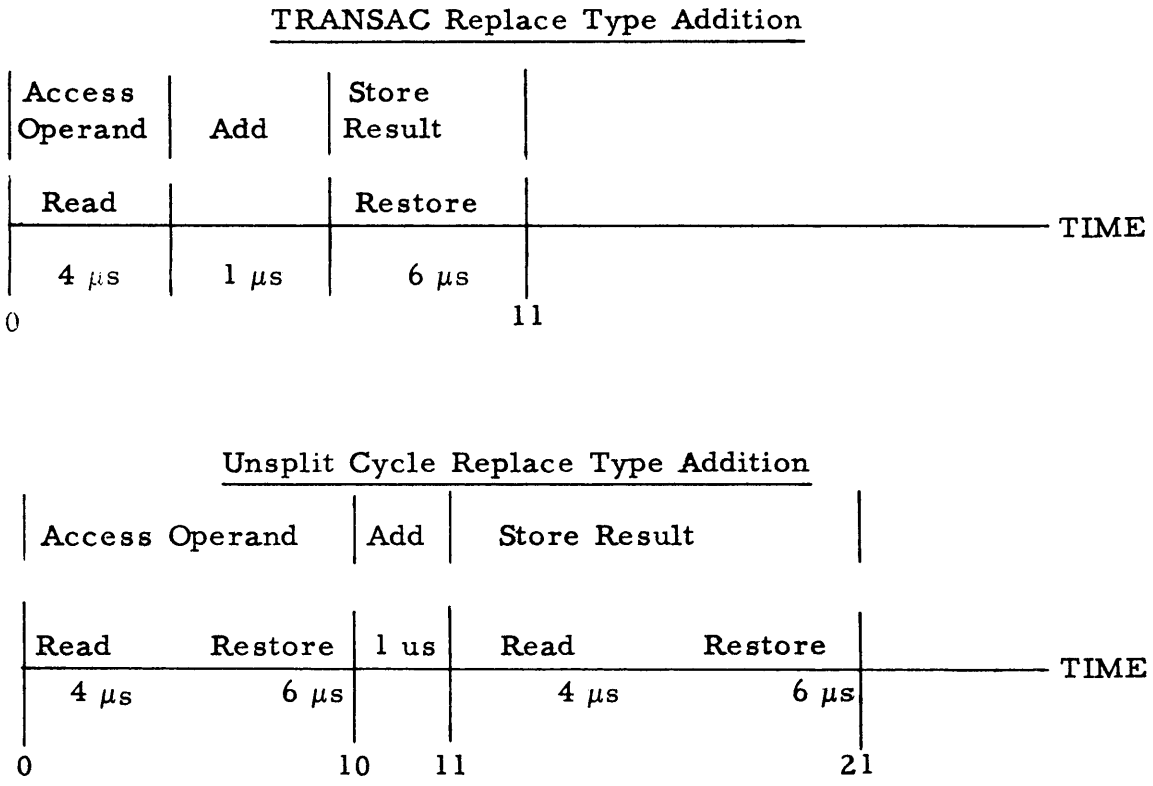


Figure 2-D

MAGNETIC DRUM STORAGE

The auxiliary internal storage stores 32,768 words in 8 bands on a magnetic drum. Up to 32 drums may be operated in one S-2000 system with only one controller required for every group of up to four drums. While the magnetic core system stores a maximum of 32,768 words, the magnetic drum system stores 32 times this amount or 1,048,576 words. TRANSAC's "write disable" feature guarantees permanent storage of tables, programs, and other constant data in the drum system. This feature prevents data from being accidentally erased or written over, thus providing a valuable available safeguard.

The magnetic drum system operates in random order for selection of drum and band addresses but sequentially within one band. Access time for the first location requested will average 17 milliseconds plus 8 milliseconds to operate the band select relays. However, once a starting address has been selected, up to 4096 words may be transferred between the drum system and memory at a rate of only 16 microseconds per word. A bulk transfer operation of this type is the most practical use for the drum system. The drum system is addressed by an input-output instruction (see Figure 4-F) which specifies the drum and band number, number of words, drum starting address, and whether it is a read or write command.

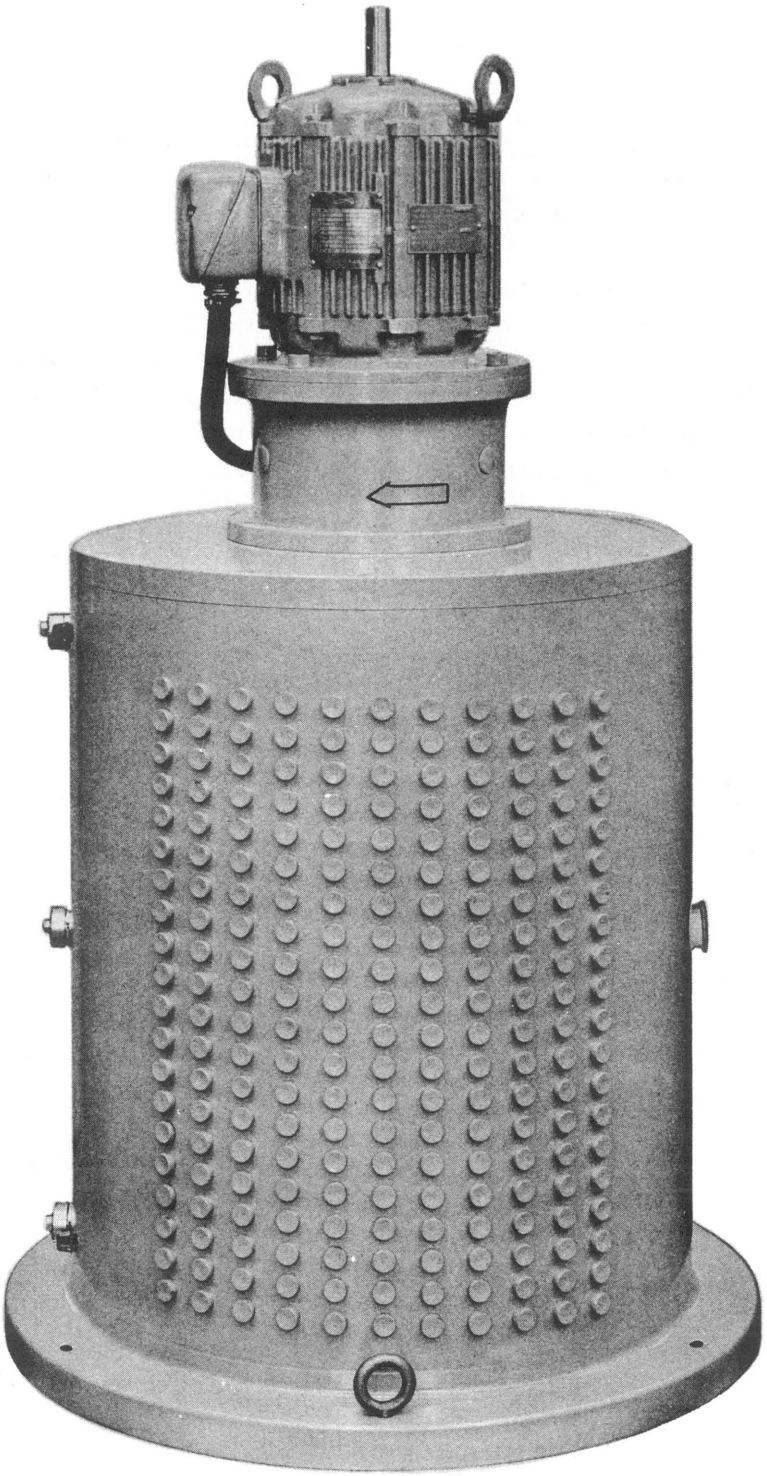
The magnetic drum system does not share the memory and is therefore assigned the lowest memory-access priority. Once the drum secures access to the memory, it retains access for the duration of its input-output instruction (a maximum of 66 milliseconds) since its purpose is to load or unload sections of the memory. The data transmission rate for the magnetic drum system is 500,000 characters per second or one TRANSAC word every 16 microseconds. This rate is so fast that there is not enough free memory access time to make memory-sharing feasible, without slowing down the data transmission rate of the magnetic drum system. In a program requiring both drum operations and memory-sharing, the number of words transferred during each drum input-output instruction may be chosen so as to allow optimum use of the memory-sharing feature.

CENTRAL PROCESSOR

Data processing, program processing and operator control are performed by the central processor unit (see Figure 3-A). The sections of the central processor are the arithmetic section, program section, console typewriter, and the display and manual control section.

Arithmetic Section

Data is processed in the arithmetic section by means of arithmetic, comparison, shifting, and extract operations. The information to be processed is transferred to the D or data register from either the memory or in some cases, the display and manual control section. The D



Magnetic Drum

#275

register is one of the three data registers in the arithmetic section. The others are the A or accumulator and Q or multiplier-quotient registers. The individual functions of these registers are outlined in Section III.

While the shifting and extract operations are performed in the registers, arithmetic and comparison operations utilize the adder network. This network acts extremely fast since it contains no storage registers and operates on all 48 bits of a word in parallel using pure binary notation. Subtraction occurs in the adder network by adding the two's complement of the D register to the contents of the A register. For floating point operations the adder network divides into two independent sections to handle the mantissa and exponent. Floating point arithmetic is optional and requires additional control circuitry.

Some of the flexible and timesaving additions to the basic types of arithmetic operations are: multiplication yielding double length or rounded products, division with double length dividends (all divisions are self-correcting in the case of overflow), and combinations of multiplication and addition or multiplication and subtraction. In all arithmetic operations the operands may be in absolute value and the results may be stored in memory. These additional operations add to the flexibility of TRANSAC and simplify the programming task.

The basic transfer time and minimum fixed point addition time are one microsecond. The average speeds of the arithmetic operations (including instruction and operand access), expressed in operations per second are:

	Fixed Point	Floating Point
Addition and Subtraction	66,700	66,700
Multiplication	20,300	24,900
Division	19,200	24,300

Under repeat control, the number of operations per second are increased by up to 50%.

Program Section

The central processor unit processes the stored data in accordance with the interpretation of the program instructions and, of course, manual actions by the operator. It is the function of the program section to interpret and execute the instructions.

Instructions are processed in the sequence that they appear in core storage except when under the control of a jump. Each memory location contains two instructions which are transferred simultaneously to the program register. Therefore the average storage access time per instruction is five microseconds.

225 instructions, including 59 floating point instructions, are recognized by the program section. The TRANSAC instructions were designed to provide maximum programming flexibility and to decrease the number of instructions required for each program.

Due to the variety of commands, the programmer is permitted to select from similar instructions the one which does precisely the operation desired. Therefore, one instruction often replaces several, thus shortening the program and its execution time.

Index Registers

The optional index registers may be selected in groups of 8, 16, and 32 registers. TRANSAC index registers are used for indirect addressing, address substitution, and address modification. Most TRANSAC instructions can utilize index registers for these purposes. The contents of the index registers may be automatically increased for counting or addressing sequential locations. Since the contents of the registers may be either increased or decreased, they may be used very conveniently for accumulating operations. The index registers are independent of the memory so do not require memory accesses when they are used. The program running time required to access an index register is infinitesimal.

Operator Control

The console typewriter and the display and manual control sections are the two means by which the operator may exercise control of the TRANSAC S-2000.

Console Typewriter Section

Through the console typewriter, the operator has direct immediate access to the magnetic core storage. He may furnish control information for the program or check intermediate results and control totals independently of the normal input-output circuitry. Input may be typed from the keyboard or read from a punched paper tape. In either case, a typed copy is prepared for checking purposes. Output may be either typed or punched or both. Some of the off-line uses of the console typewriter are: to prepare punched paper tape, edit or revise paper tape, or prepare hard copy from typing or paper tape.

The typewriter keyboard contains 67 keys which represent all 64 TRANSAC characters in either upper or lower shift. The three additional codes are the delete, upper, and lower case codes. The typewriter mechanism resembles a conventional electric typewriter and operates at a speed of 10 characters per second.

Display and Manual Control Section

Figure 2-E is a photograph of the console which contains all the displays and manual controls. The design followed advanced human-engineering standards to eliminate operator confusion and fatigue. Colors and placement of components were part of the overall design. No indicator or control was added to the console without careful consideration of its usefulness in simplifying operation without increasing its complexity. Section III describes the displays and controls according to their functions.

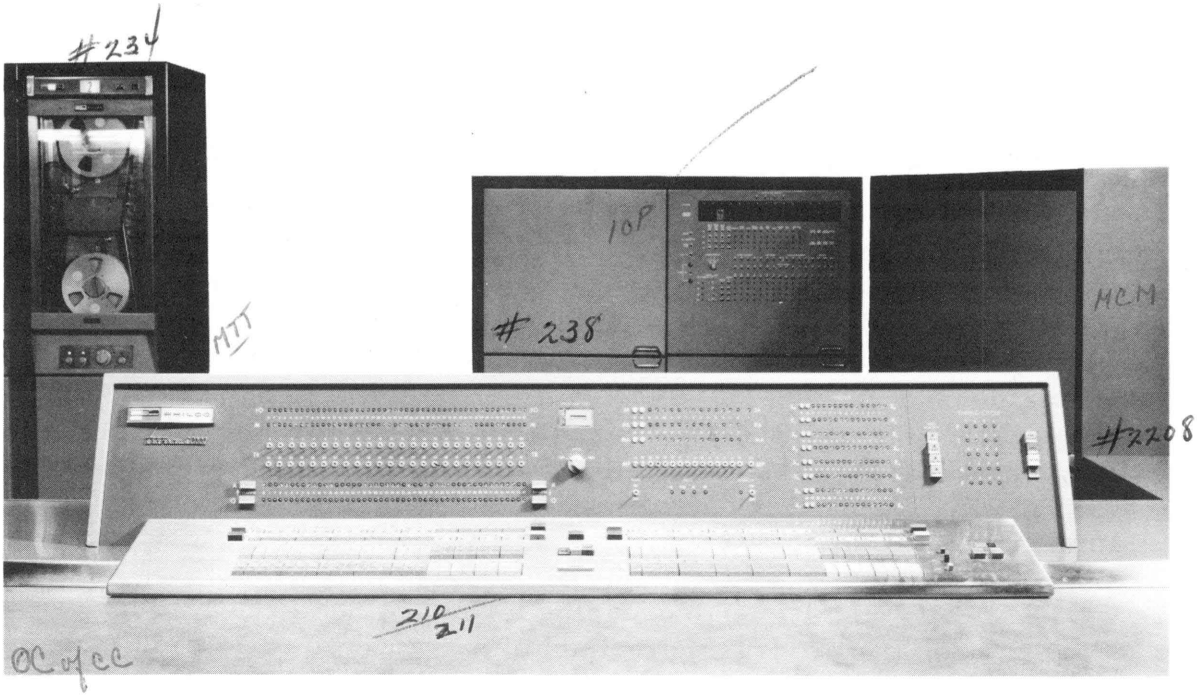


Figure 2-E Central Computer Operator's Console

TM-2 MTT

INPUT-OUTPUT

With the flexible TRANSAC input-output system (see Figure 2-F) effective use can be made of the high operating speed of the central computer. All input-output data that can be scheduled is funneled through the input-output processor unit. Random or high-priority input-output may be connected with the central computer through the real-time channel and may automatically interrupt a running program. When no real-time connections are needed, this channel may be used for paper tape input-output. Because of the TRANSAC design feature called Multiple Processing, many input-output units may be programmed for simultaneous operation.

MULTIPLE PROCESSING

TRANSAC's Multiple Processing technique has greatly improved and enlarged upon the processing method often referred to as simultaneous read/write/compute. While the central processor in TRANSAC is computing, as many as nine input-output devices may be processing data simultaneously. Four of the nine may be magnetic tape units and four may be punched-card systems, high-speed printers, and paper tape systems. The ninth may be either a real-time device or a paper tape system. Multiple processing is possible because of the Memory Sharing feature, which optimizes memory use, plus the advanced electronic design of both the input-output processor and theuniversal buffer-controller.

INPUT-OUTPUT PROCESSOR

The input-output processor is the interconnecting and control link between the central computer and the 16 input-output channels. Each channel couples either a magnetic tape unit or a universal buffer-controller to the central computer. The standard data transfer rate over a channel is 90,000 alphanumeric characters per second. By means of a multiplexing technique, the input-output processor can automatically connect any four of the sixteen channels to the central computer. Up to sixteen input-output processors may be used in a TRANSAC system to connect over 400 input-output systems to the central computer.

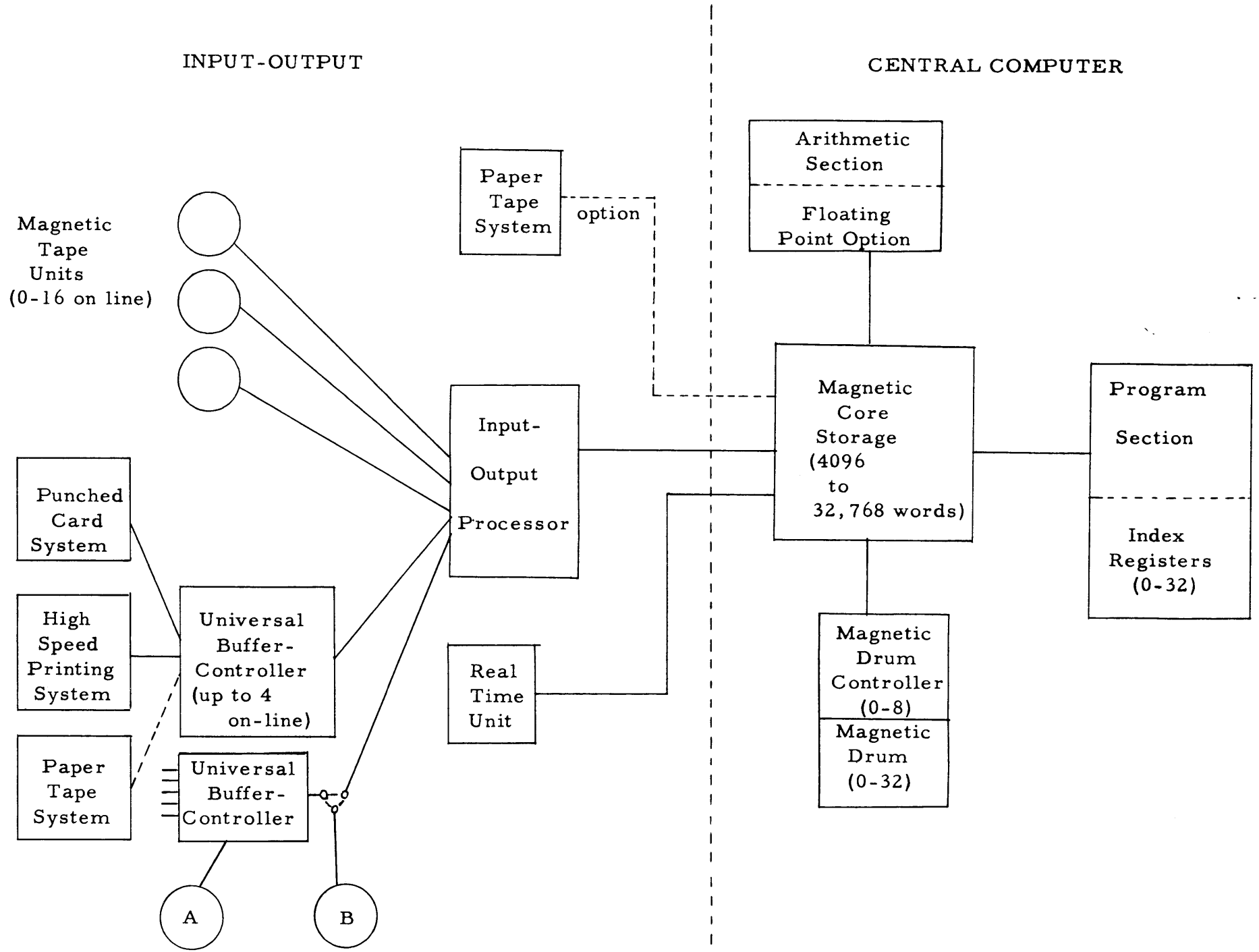


Figure 2-F Main Components of the TRANSAC S-2000 System

Each input-output processor also controls four universal buffer-controllers simultaneously. In this case, while transmission takes place between TRANSAC's memory and four tape units, any combination of four punched-card readers and punches, high-speed printers, and paper tape readers and punches may also be operating. Central computer time is only used when data is transferred between the memory and a buffer-controller. The operations of the punched-card, paper tape, and high-speed printing systems are essentially off-line when under the control of buffer-controllers.

UNIVERSAL BUFFER-CONTROLLER

The Universal Buffer-Controller adds greatly to the flexibility and economy of the TRANSAC System. This one unit controls off-line conversions between any two media, or on-line communication between the central computer and any medium except magnetic tape. In general, the buffer-controller acts as a buffering device between two input-output units or between one input-output unit and the central computer.

The input-output devices that may be operated with the buffer-controller include punched-card systems, magnetic tape units, paper tape systems, and high-speed printing systems. Up to seven devices, including five punched-card, paper tape, or high-speed printer units may be connected to a buffer-controller in addition to two magnetic tape units. In the future, any desirable input-output device may be easily added to a buffer-controller. A simplified diagram of a buffer-controller is shown in the following figure.

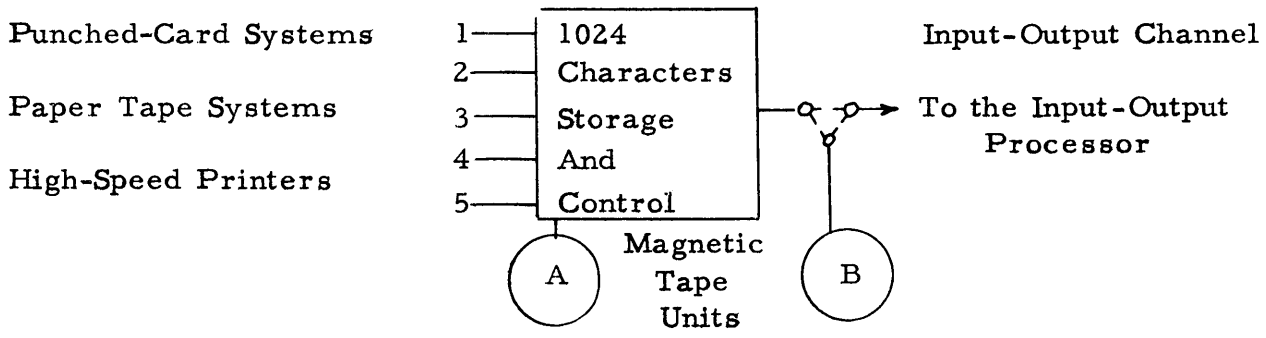


Figure 2-G Block Diagram of the Universal Buffer-Controller

When used off-line, the buffer-controller controls the conversion of data from any medium to any other medium. For example, the buffer-controller is used to convert data from punched cards to magnetic tape, from tape to printer, tape to tape, etc.

Data Select is an additional off-line feature. Using Data Select, only the data blocks containing selected control characters will be converted. Thus the data for up to 15 reports, for example, may be recorded on the same reel of magnetic tape or the same punched-card deck. Then with Data Select the universal buffer-controller may be used to segregate the data and prepare the reports in sequence from the single data source. Thus, Data Select simplifies and speeds up report preparation and allows the buffer-controller to perform an off-line function which in other systems requires central computer time.

The buffer-controller is switched on-line by a pushbutton for use as buffer storage for the intermediate speed input-output devices such as paper tape, punched-card, and high-speed printer systems. The transmission between the buffer-controller and an input-output device is essentially off-line and does not require central computer time or control. The transmission between a buffer-controller and the central computer, however, is the same as it is for magnetic tape and is at the same rate: 90,000 characters per second. Also, as for magnetic tape, the transmission is time-shared with other input-output operations and central computer processing.

The two magnetic tape units which may be connected to the buffer-controller are very flexible in their use. If tape unit A, as illustrated in Figure 2-G, is provided with the buffer-controller, it is permanently connected to permit off-line conversions to and from magnetic tape. If tape unit A is not provided with the buffer-controller, another input-output device may be substituted.

Tape unit B is extremely flexible in its connection and use. For maximum flexibility of the buffer-controller, an optional electronic switch may be set by a pushbutton to connect tape unit B either on-line to the input-output processor or off-line to the buffer-controller. Consequently, tape unit B may be used in one position as another on-line tape unit, retaining the capacity of the system when the buffer-controller

is engaged in an off-line operation. In the off-line position it may be used as an alternate of tape unit A for conversions to or from magnetic tape. For a magnetic tape to magnetic tape conversion, tape unit B is used with tape unit A.

Another use of tape unit B is to record the output data of a program. It may then be switched off-line to convert the output data to another medium through the buffer-controller. This operation avoids the handling of tape reels and speeds preparation of reports. The inverse of this operation, which converts data to magnetic tape off-line, is also very efficient.

For economy, tape unit B may be permanently connected to the buffer-controller in the same fashion as is tape unit A. Finally, tape unit B can be omitted entirely and be replaced by another input-output system. In any case the central computer cannot communicate with a tape unit through the buffer-controller, since this would result in poor utilization of the buffer-controller.

REAL-TIME CHANNEL

The real-time channel shares access to the magnetic core storage with the central processor, the input-output processor, and the magnetic drum system. The real-time channel may be used for paper tape input-output or for real-time input-output.

AUTOMATIC INTERRUPT

Two types of program interrupt may be employed in TRANSAC S-2000. The first type is a "programmed interrupt" under control of the program. By interposing a unique instruction into the program at selected intervals, the system can interrupt one program to perform another of higher priority, and then return to complete the first program.

The second interrupt is an "external" or "real-time" interrupt. The interrupt data and program may enter the S-2000 System through either the input-output processor or the real-time channel. The interrupt may take place immediately or within a few microseconds depending on the requirements of the specific installation.

The automatic interrupt feature is flexible enough to handle both the future centralized data processing requirements of industry and the real-time system needs of the military. The modular design of TRANSAC allows hardware to be furnished on an optional basis to suit the degrees of priority and speed required for the interrupt feature in a specific installation.

INPUT-OUTPUT SYSTEMS

TRANSAC is designed for a wide variety of input-output media and equipment. Additional types may be easily adapted to operate with TRANSAC. Current product line media include magnetic tape, punched-card, punched paper tape, and high-speed printing systems.

MAGNETIC TAPE SYSTEM

The TRANSAC magnetic tape system has been designed to provide the proper balance for the high operating speeds of the central computer. In addition to providing the fastest commercially available system, Philco has incorporated the most recent developments and advances in magnetic tape equipment.

The magnetic tape selected for the TRANSAC system has a one mil mylar base, is one inch wide, and comes in five reel sizes: 600, 1200, 1800, 2400, and 3600 feet. Data is recorded in fixed block form to provide for efficient peripheral operations, checking, and tape reading in both the forward and backward directions -- a significant feature for sorting operations. The size of the block is 128 words, recorded in 512 frames. Each frame contains 12 data bits, two parity bits, and two timing bits. In addition to the 512 data frames, a 513th frame adds to each of the 14 horizontal channels an even parity bit for parity-checking of the block.

Accuracy of reading and recording is ensured by the parity checks, frame counts, and use of separate read and write heads. While information is being recorded it is read back and checked for validity. When an error is detected, additional attempts are automatically made to rewrite the block. Similarly, when an error is detected during reading, the system automatically rereads the block.

To insure against unintentional loss of information, a physical snap ring is provided with each reel. Without the snap ring, recording cannot occur; a safety device can prevent the insertion of the snap ring. In any case the data on the tape may be read.

The density of recording on magnetic tape is 375 bits per inch and the tape speed is 120 inches per second. The instantaneous data transfer rate for one tape unit is, therefore, 45,000 bits per second. The data transfer rate may be represented in other terms because of the Data Compression feature.

DATA COMPRESSION

TRANSAC's design allows a user to compress the data recorded on magnetic tape so that instead of representing all information in alphanumeric form it will be compressed into binary coded decimal and pure binary forms. By taking advantage of this flexible feature, significant savings in magnetic tape, tape storage, tape handling, and computer time will be realized.

For example, when information is recorded in alphanumeric form, the data transfer rate is 90,000 characters per second, per tape unit in operation. Because of the Data Compression feature, numeric information, recorded in binary coded form, yields a rate of 135,000 decimal digits per second. Similarly, the rate for numeric information in binary form is 157,500 decimal digits per second. (Note that because four tape units may be operating simultaneously, the combined transfer rates are 360,000 alphanumeric characters, or 540,000 binary coded decimal digits, or 628,000 decimal digits per second).

Most data processing systems today are not strictly alphanumeric, although all can represent alphanumeric information. Unlike the other systems which can represent data in several forms, TRANSAC does not necessarily require time consuming conversion operations. Arithmetic can be performed in any of the data forms by flexible library routines. Therefore, even though some conversions may be necessary, the TRANSAC user will save up to 30% of his run time, plus the savings in tape handling time. In terms of actual tape needs, many thousands of dollars can be saved in a given installation because Data Compression reduces the total required amount of tape by a significant percentage.

PUNCHED-CARD SYSTEM

The punched-card system reads at the rate of 2000 cards per minute, by a new photoelectric reading technique, and punches at the rate of 100 cards per minute. The system may read 51- or 80-column cards and punch 80-column cards in either Hollerith or card image mode. The standard Hollerith code used in most punched-card installations has been expanded so that all 64 TRANSAC characters can be punched and read. The cards are translated from Hollerith code to TRANSAC code automatically by the punched-card system. The card image mode facilitates the handling of binary information and packs twelve bits or two TRANSAC characters in each column. The card image mode also is used to read punched cards prepared on different computers and in different codes.

The card format is controlled during reading and punching operations by two plugboards. Additional control is provided by editing symbols transmitted with the data. By plugboard wiring, fields may be rearranged and fixed fields may be inserted. During off-line operation the plugboards specify the amount of data to be read or punched for every card and block. Records of variable lengths are handled flexibly with editing symbols, such as the end-of-card and the end-of-block symbols.

The accuracy of the reading and punching operations is ensured by constant checking of the system components, parity, and card alignment (skew). The automatic card counter may be used by the operator to check whether any cards have been lost en route to the reader.

The punched-card system is extremely flexible in its use. The system may be used either on-or off-line in conjunction with a universal buffer-controller. Partial systems may be ordered for read-only or punch-only applications. These configurations allow a read-only system to be connected on-line and a punch-only system to be used off-line, for example. For some installations this will afford much better utilization of the punched-card equipment and the TRANSAC system.

HIGH-SPEED PAPER TAPE SYSTEM

Through the paper tape reader, data from 5- or 7-level punched paper tape may be read directly into the core memory at a rate of 1000 characters per second. Using the paper tape punch, data may be punched

Punched Card Reader with Card Controller
and Magnetic Tape Transport

into paper tape at a rate of 60 characters per second. Both reading and punching are controlled by the paper tape controller.

For long tape life and higher operating speeds, reading is accomplished photoelectrically; the tape speed is 100 inches per second. Up to 4096 words may be read with one instruction and provisions are made to pass blank tape. Operation of the reader is such that without reversing the tape or leaving a record or block gap, reading will begin with the character immediately following the last character read.

The Paper Tape System may be connected directly to the input-output buffer register or through the universal buffer-controller. The direct buffer register connection is necessary when no Universal Buffer-Controllers are included in a TRANSAC System. The direct connection may also be advantageous in a TRANSAC System since it allows the maximum number of input-output units to be operated simultaneously.

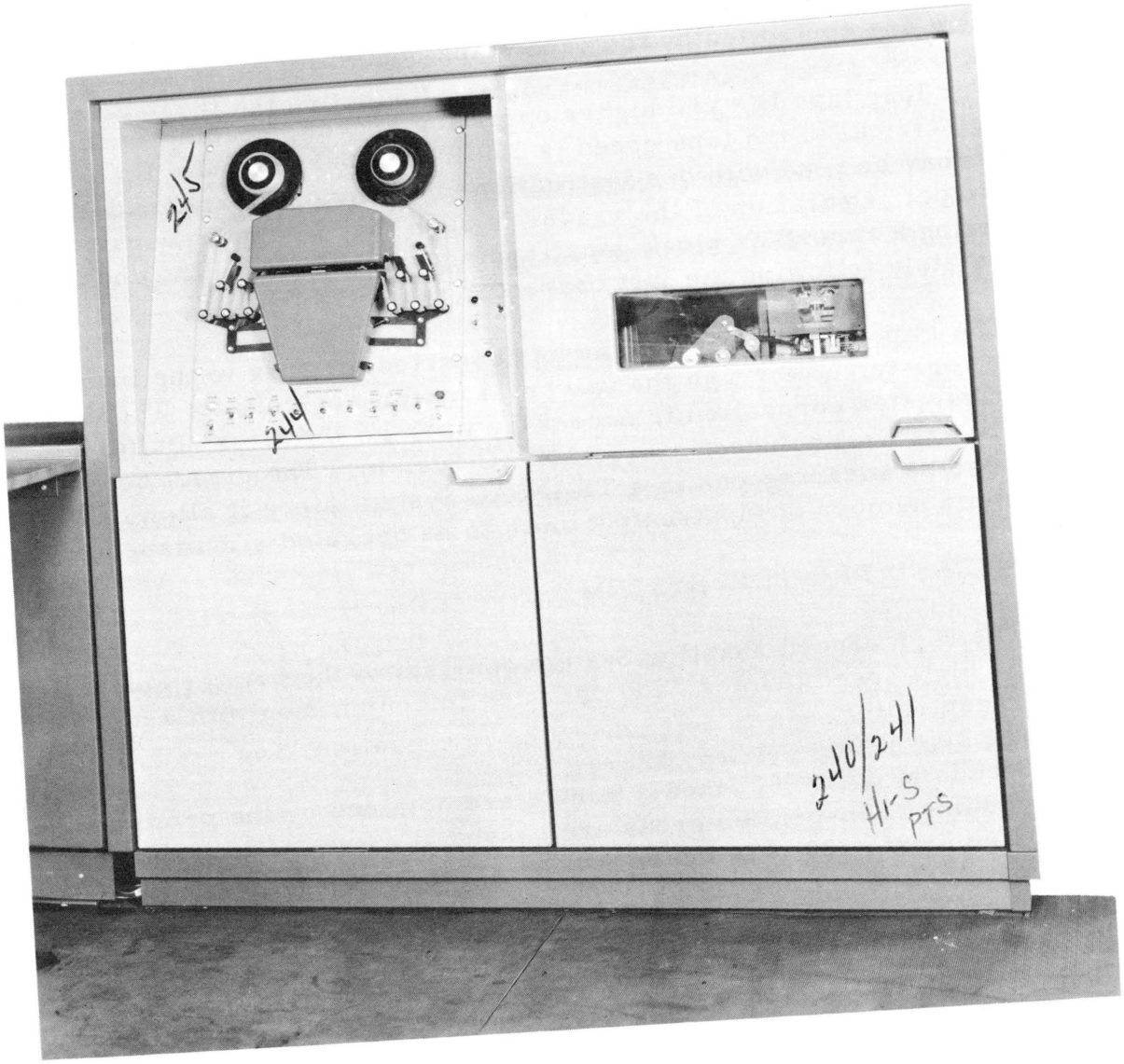
HIGH-SPEED PRINTING SYSTEM

The High -Speed Printing System consists of the printer controller and the high-speed printer, and operates in conjunction with a universal buffer-controller.

Speeds of up to 900 lines a minute are obtained by the printer. By skip-feeding, non-printed areas are passed at a rate of 25 inches a second. Each line prints 120 characters spaced at ten characters per inch horizontally and six per inch vertically. An optional paper feed mechanism, which can be attached by an operator, is available for 8 character per inch vertical spacing. This is especially useful when it is necessary to print between the rows of a punched card.

Information to be printed on-line is received from a buffer-controller in standard blocks of 1024 characters. The 64 TRANSAC characters fall into three major classes:

1. Decimal digits, 0 through 9.
2. Alphabetic characters, A through Z.
3. Twenty-eight special symbols



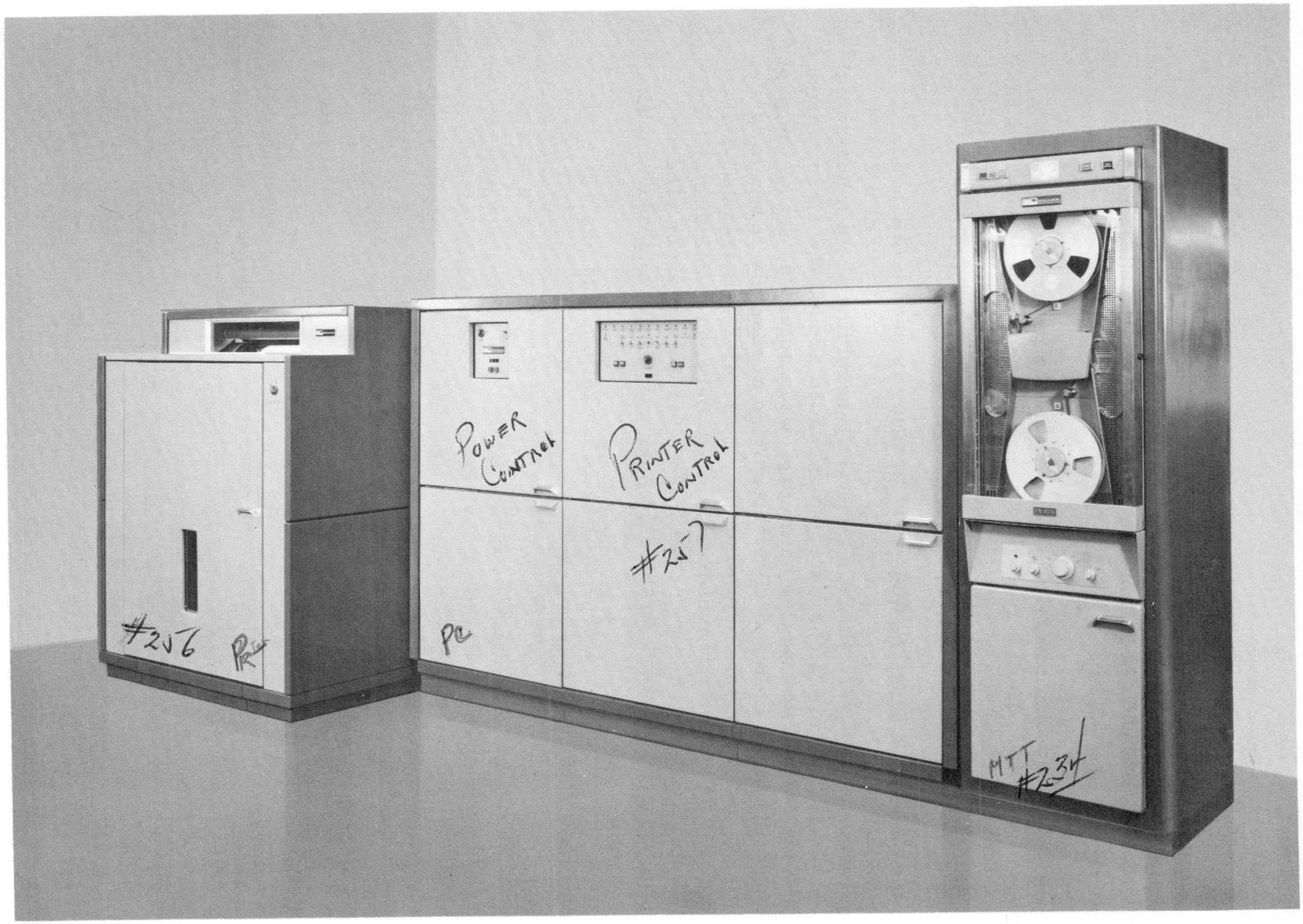
High-Speed Paper Tape System

In normal operating mode three of the special symbols are control characters and only the remaining 61 characters are printed. In memory dump mode all 64 TRANSAC characters (including the three control characters) are printed.

Horizontal format is controlled by computer programming and plugboard editing. The plugboard is used to repeat characters on a line, and to suppress and rearrange fields. Vertical format is accomplished by a paper tape control loop mounted on the print carriage mechanism.

The "print-on-the-fly" method of printing is used. One hundred and twenty hammers are arranged horizontally to be fired at a 2-3/4 inch diameter print roll which is constantly revolving about a horizontal axis. The 64 TRANSAC characters are spaced around the circumference of the print roll. The impulse hammers, when actuated, strike the paper and force it against an inked silk ribbon lying across the character face. One major feature of this printer is the "controlled penetration" of the hammer. The hammer travel is controlled between physical stops and never actually strikes the print roll. This feature produces clearer printing and reduces wear on the hammer, print roll, and inked ribbon.

The print ribbon is self reversing in operation, and has a life of approximately 100 printing hours.



High-Speed Printing System Including Printer, Printer Controller and Magnetic Tape Unit

SECTION III

PERFORMANCE SPECIFICATIONS

The preceding sections describe the major system concepts and equipment characteristics which are of most interest to a prospective user of a data processing system. This section summarizes the physical characteristics described and adds detailed performance specifications for quick reference and easy comparison with other systems.

I Central Computer

A. Magnetic Core Memory

1. Word size: 48 bits, equivalent to:

   a. 8 alphanumeric characters
   b. 14 decimal digits
   c. a combination of a and b
   d. 10-digit and sign floating point number

2. Capacity:

   a. 4,096; 8,192; 16,384; 32,768 words
   b. 32,768 - 262,144 characters
   c. 57,344 - 458,752 decimal digits

3. Access:

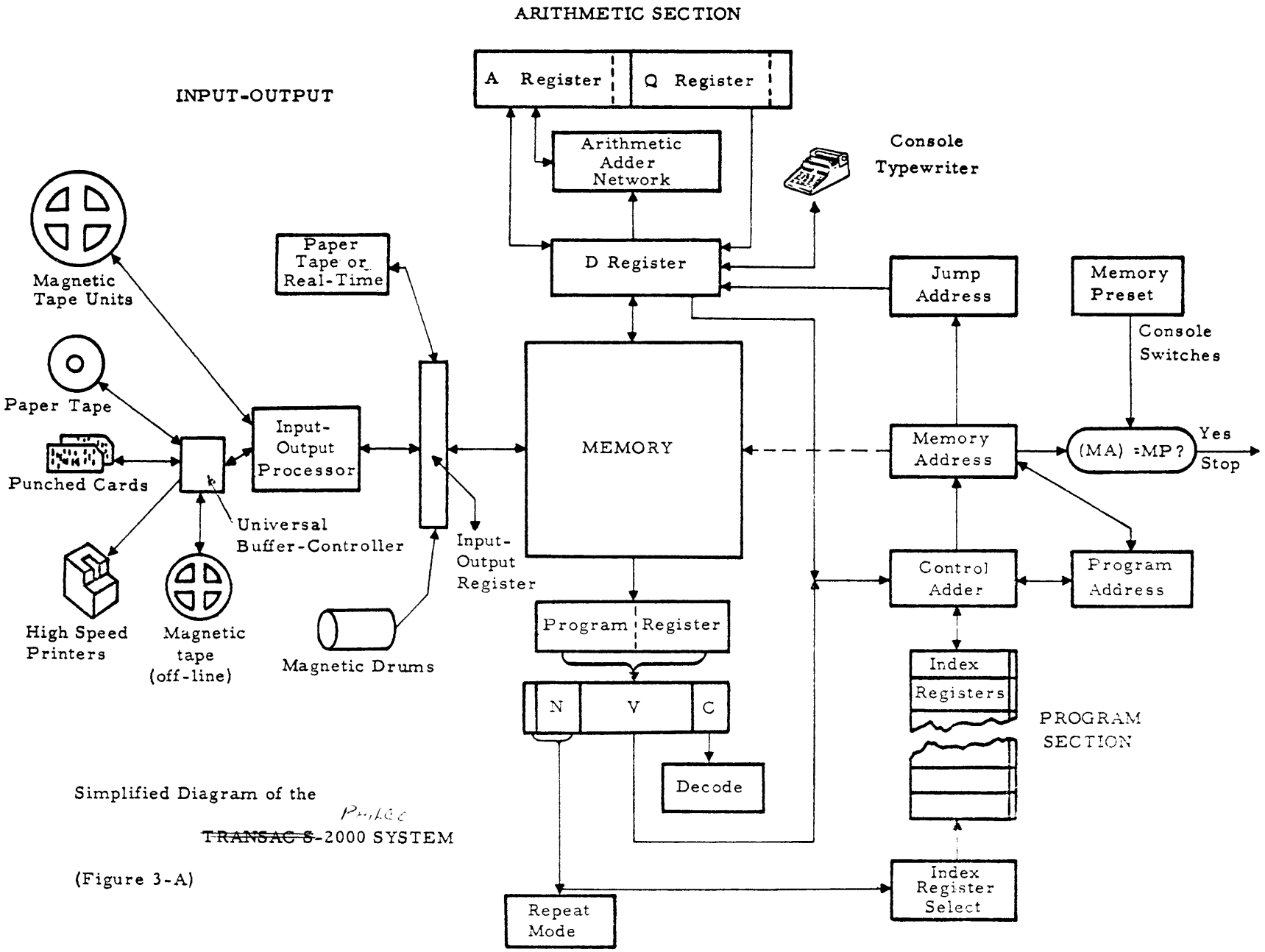
   a. Mode: parallel
   b. Time: 10 microseconds per cycle
   c. Priority: Use of memory is granted on a priority basis such as: - Automatic Interrupt, Input-Output Processor, Real-Time Channel, Central Processor Unit, and Magnetic Drum System.

4. Memory-sharing feature allows memory accesses of the various units to be interleaved in sequence according to the assigned priority. Therefore, multiple processing or simultaneous input-output and computing is practical.

5. Split Memory Cycle

   a. Words read from memory may be operated on during the restore cycle; saves up to 6 microseconds per access and reduces the effective memory access time to 4 microseconds in many cases.

   b. During a "store-type" instruction, the restore cycle is delayed so that only the result is stored. Saves 10 micro-



Simplified Diagram of the

~~TRANSAC S~~-2000 SYSTEM

(Figure 3-A)

seconds per instruction and reduces the effective memory access time to 5 microseconds.

B. Central Processor Unit

1. Arithmetic Section

a. Numbers

(1) Fixed point: 47 bits plus sign
(2) Floating point: 36-bit mantissa, 12-bit exponent; including sign bits.
(3) Binary
(4) Two's complement representation of negative numbers

b. Arithmetic mode: parallel

c. Registers: three storage registers accessible by program and operator console

(1) Data (D): Used as a buffer register for all arithmetic transfer operations and before an operation contains the addend, the subtrahend, the divisor, the multiplicand, or one factor of a comparison.
(2) Accumulator (A): Contains the augend, minuend, one factor of a comparison, and the dividend or its more significant half before an operation. After the operation stores the sum, difference, remainder, the product or its more significant half.
(3) Quotient (Q): Stores the multiplier, the quotient, a factor of a comparison, a masking pattern for an extract operation, or the less significant half of a product or a dividend.

d. Speed: The average arithmetic speeds, including operand and instruction access, expressed in operations per second, are:

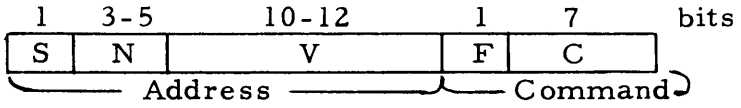
	FIXED POINT	FLOATING POINT
Addition and Subtraction	66,700	66,700
Multiplication	20,300	24,900
Division	19,200	24,300

Under Repeat Control, the number of operations per second are increased by up to 50%.

2. Program Section

a. Instructions

(1) Two instructions per word
(2) Automatically and sequentially accessed
(3) 225 instructions, including 59 floating point
(4) Single address
(5) Instruction format:



(a) 7-bit C field defines command
(b) F, or function bit, modifies command (e.g. specifies fixed or floating point mode for arithmetic)
(c) V, or variable field, may be an address, a number, or an index register modifier
(d) N specifies index register number
(e) S bit specifies index register use
(f) The size of N and V are determined by the number of index registers in a system. The V field is 15 bits if there are no index registers; the N field is not required in such a case.

b. Accesses memory via the Program Register.

c. Index Registers

(1) Available in groups of 8, 16 or 32 registers (not part of memory)
(2) Used for counting, accumulating, indirect addressing, and address modification or substitution.
(3) Contents may be automatically increased for counting and addressing sequential locations.
(4) Accumulating: contents may be increased or decreased.
(5) Access time: millimicroseconds

d. Other Registers

(1) Program (PR): stores the selected pair of instructions to be executed.
(2) Memory address (MA): holds the address of the memory location to be accessed.
(3) Program Address (PA): contains the address of the next instruction word.
(4) Jump Address (JA): stores the memory address of the instruction following the last jump instruction (for subroutine exit address). May be accessed by the program.

3. Console Typewriter Section

a. Contains typewriter keyboard (64 TRANSAC plus 3 control characters), seven-level paper tape reader and punch.

b. Used off-line as an electric typewriter, paper tape punch, to type hard copy from paper tape, or to reproduce and revise paper tape.

c. On-Line: manual or paper tape input to memory, typed copy and/or paper tape output.

d. Output speed: ten characters per second

e. Operates simultaneously with input-output operations.

4. Display and Manual Control Section

a. Three operating modes:

RUN for normal operation, STEP to perform one instruction at a time, and TEST which completes only one timing cycle of one instruction.

b. Programming Aids:

(1) Jump button simplifies execution of a jump instruction without altering the contents of the jump address register.
(2) Special Memory Preset register halts computer when specified memory location is accessed.
(3) Breakpoint and overflow switches cause the computer to stop before executing a breakpoint jump or after fixed point overflow.

c. Input Controls

(1) Toggle register to set up a word to be transferred to the data register by the running program
(2) Data and Program register keyboards to enter information into these registers when the central processor is stopped

d. Displays

(1) All arithmetic, index, and program registers
(2) Faults displayed are command, input-output, memory, exponent, and overflow.
(3) Clock displays program running time in seconds.

C. Magnetic Drum System

1. Size

a. Physical rotating drum

(1) Length: 24 inches
(2) Diameter: 18.5 inches

b. Capacity

(1) 32,768 words (48-bit word) per drum, arranged in eight 4096-word bands
(2) Up to 32 drums possible for a total capacity of 1,048,576 words or 8,388,608 alphanumeric characters
(3) One drum controller required for each group of one to four drums

2. Timing

a. 1800 rpm, 34 ms per revolution

b. Average access time for starting address is 17 ms plus 8 ms to operate band select relays; 9 ms are added when switching from one drum to another.

c. Transfer rate is 16 microseconds per word.

3. Mode of Operation

a. Parallel word by word transfer through the input-output register

b. Drum transmission waits until no other unit requires access to memory.

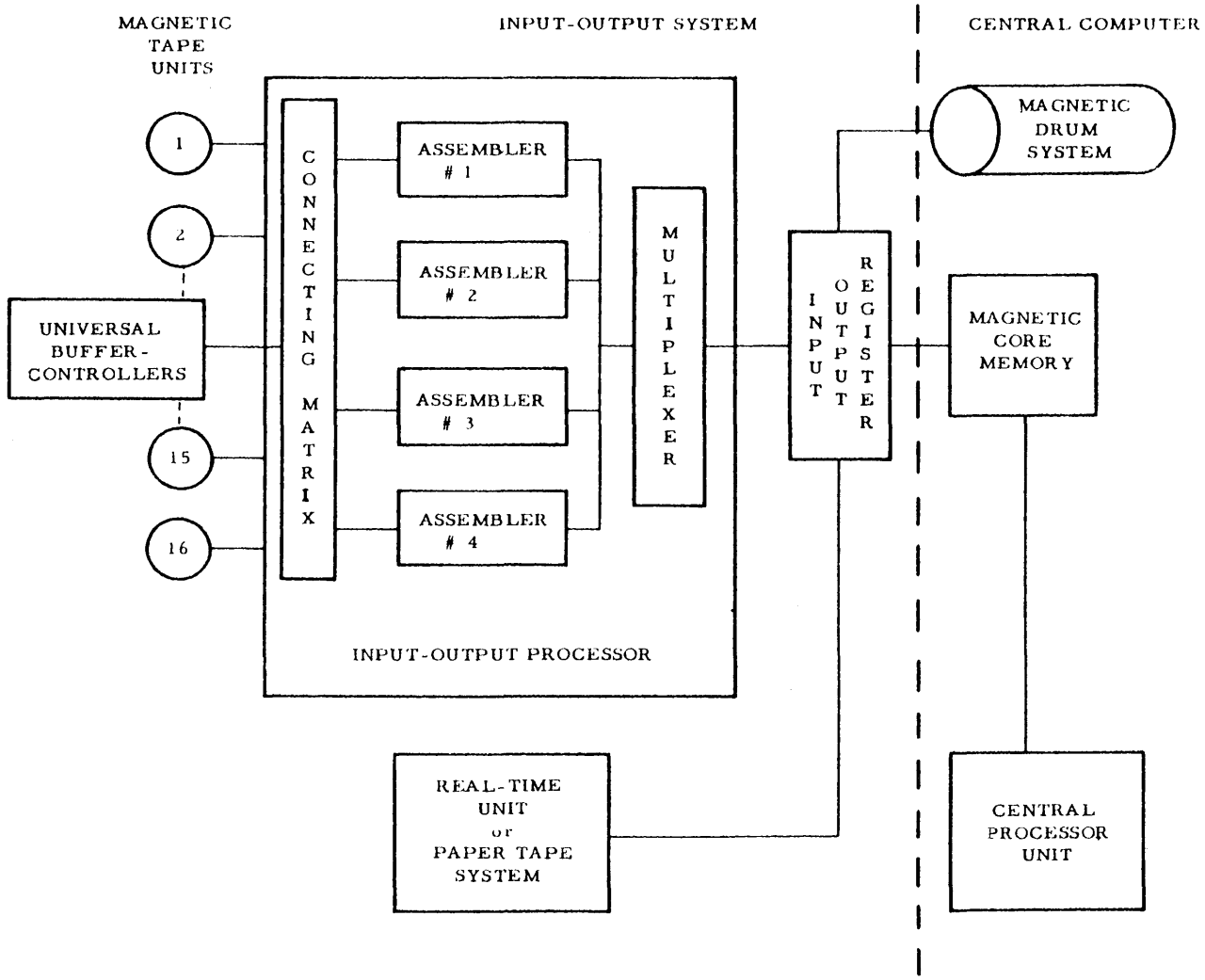
c. Transfers up to 4096 words per instruction.

d. A group of words to be transferred may span two bands.

e. "Write-disable" feature prevents accidental erasure of permanent information.

II Input-Output

All input-output units and the magnetic drum system communicate with the magnetic core memory through the input-output register, a one word, parallel, buffer register as shown in the following diagram.



INPUT-OUTPUT COMMUNICATION WITH THE MAGNETIC CORE MEMORY

Figure 3-B

A. Input-Output Processor

1. Controls and coordinates a total of 16 input-output channels each terminated by either a magnetic tape unit or a universal buffer-controller (Maximum number of buffer-controllers is four) as shown by the preceding diagram (Figure 3-B),

2. Multiplexes (provides simultaneous operation) up to four data transmissions (one per assembler) between magnetic core memory and the sixteen input-output channels.

3. Automatically switches any four input-output channels to the Central Computer.

4. Checks validity of all data-transmissions.

5. Up to 16 input-output processors possible in one TRANSAC system

B. Magnetic Tape System

1. Up to 16 magnetic tape units controlled by each input-output processor.

2. Data transfer rates per unit

   a. 90,000 characters per second

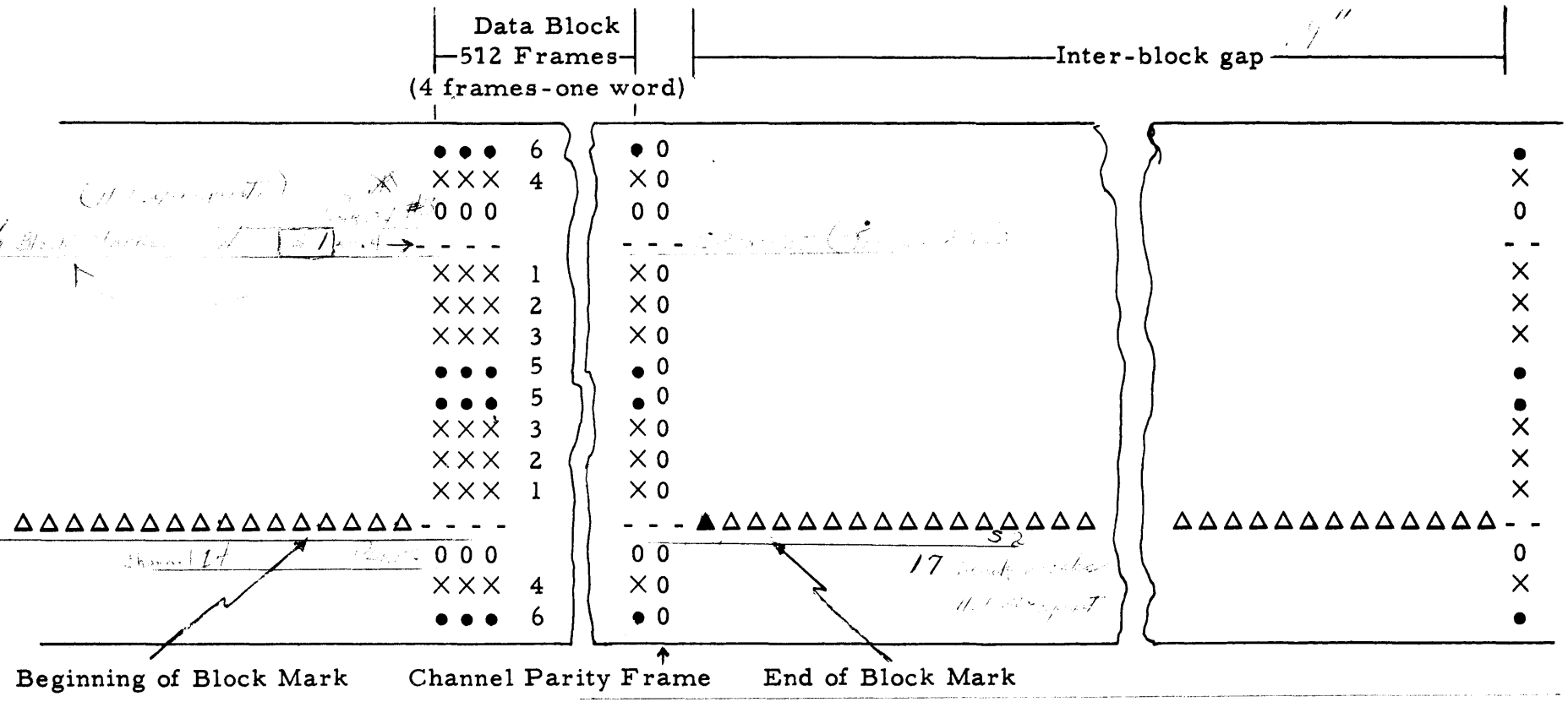
   b. 135,000 binary-coded decimal digits per second, or

   c. 157,500 decimal digits (pure binary) per second.

3. One tape frame contains twelve binary digits which may be two alphanumeric characters, three binary-coded decimal (or hexadecimal) digits, or four octal digits.

4. Tape format (See Figure 3-C)

TRANSAC S-2000 MAGNETIC TAPE FORMAT



● ... Zone bits
0 ... Parity bits
- ... Sprocket bits
Δ ... Block markers bits: 16 frames, recorded at double density
X ... Data bits

The numbers shown on the tape refer to the order of bits when alphanumeric data is recorded.
The six Bits of a character are numbered: 6, 5, 4, 3, 2, 1.

Figure 3-C

a. Block size: 128 words in 512 frames plus a channel parity frame 4

b. Tape frame: 12 data bits, 2 parity bits, and 2 timing bits = 16 channels

c. Recording density: 375 frames per inch, 750 alpha-numeric characters per inch, or 1300 decimal digits per inch

5. Tape Capacity: 19,000 blocks per 3600' tape

6. Tape passing speeds:

a. Read-write: 120 inches per second; 6.3 minutes per 3600' tape

b. Rewind: 225 inches per second; 3.25 minutes per 3600' tape

7. Tape dimensions: 1 inch wide, 1 mil mylar base, 600, 1200, 1800, 2400, or 3600 feet long.

8. End of tape sensing: both ends of tape coated with silver to electronically stop the tape when rewinding, reading, or writing beyond data.

9. Reliability

a. Independent read-head checks writing operation.

b. Horizontal and vertical parity check

c. Sprocket bits and block markers checked

d. Automatic reread or rewrite after detected error

e. All errors may be sampled by the program.

C. Universal Buffer-Controller

1. Maximum number per input-output processor: 4 on-line.

2. Functions:

   a. On-line, buffers all input-output media (except magnetic tape) for high-speed communication with the central computer.

   b. Off-line, converts data between any two input-output media.

   c. Off-line, the buffer-controller can switch a magnetic tape unit on-line to use the input-output channel or off-line for magnetic tape conversion.

3. Capacity: seven input-output systems; may include up to two magnetic tape units, paper tape, high-speed printing, and punched-card systems.

4. Data Select feature: allows off-line printing or punching of up to 15 separate reports from one reel of magnetic tape or other input medium.

5. Checking

   a. Validity check of instructions

   b. Error indicators on the input-output devices can be sampled by special program instructions. Instructions also check for completion of transmission.

   c. Parity check made for all data transmissions.

   d. Parity, frame count, and block marker checks made during magnetic tape transmission.

D. High-Speed Printing System

1. Function: Prints hard copy from any input media (Utilizing the universal buffer-controller).

2. Speed: 900 lines per minute (prints an original and at least five clear copies or an offset master)

3. Horizontal format

   a. Spacing: 120 characters per line, 10 characters per inch

   b. Form size: 4 to 20 inches

4. Vertical Format

   a. Spacing: 6 lines per inch; 8 lines per inch optional.

   b. Skip speed: 9000 lines per minute.

   c. Line advance: punched tape loop positions the lines to be printed.

5. Editing

   a. Data select characters control printing of up to 15 reports from one input medium (through universal-buffer controller).

   b. Horizontal format characters

      (1) Filler: Skipped over (not printed) without increasing the character count of the line.
      (2) End of line: indicates all characters to be printed on a line have been received.
      (3) Space character: skips a one-character space while advancing the character count of the line.

c. Plugboard

(1) Rearranges fields.
(2) Repeats characters up to four times per line.

6. Checking

a. Fault indications: audible tone, flashing light, and error signal sent to universal buffer-controller.

b. Error checks

(1) Characters counted to insure that no more than 120 printable characters occur before the end-of-line character (excluding data select and vertical format characters)

(2) The last character of a block is checked to ascertain if it is an end-of-line character.
(3) All print hammer circuits are checked to ensure proper action.

c. Halt Conditions

(1) Paper tears or supply is exhausted.
(2) Voltage varies out of limits.
(3) If more than 120 characters to be printed are received without an end-of-line character, an error signal is sent to the universal buffer-controller and the line is printed. (This stoppage is optional, depending on the setting of a switch)

d. Memory Dump Mode

For checking purposes prints all 64 characters (including the 3 control characters) at 64 characters per line. Prints out all characters sequentially from the universal buffer-controller.

E. Punched-Card System

1. Function

Provides punched-card input and output from the central computer.

a. May be operated on-line through the universal buffer-controller.

b. May be converted off-line through the universal buffer-controller to or from any other media.

c. Can read and transmit variable length data.

2. Card Size: 51-or 80-column Hollerith, rapid changeover by operator.

3. Reading

a. Speed-2000 cards per minute

b. Reading modes

(1) Code: cards are automatically translated from the Hollerith code (binary-coded characters) to TRANSAC code.

(2) Card Image: cards are read without translation. Each column contains 12 binary digits, which may be two alphanumeric characters, three binary-coded decimal digits, or four octal digits.

c. Format Control

(1) Reader plugboard

(a) Allows insertion of 8 columns of fixed data.
(b) Determines number of words per card, and cards per block to be read off-line.
(c) Rearranges fields.

(2) Special characters

(a) End-of-card and end-of-block characters facilitate handling variable length records and save time.
(b) Filler characters simplify editing.
(c) Blank columns may be read as zeros or spaces.

(3) On-line: instruction determines number of words per card and cards per block.

d. Capacity: Stacks 4000 cards in input or output bins.

Can be loaded or unloaded from either side. Visible counter indicates number of cards read.

4. Punching

a. Speed: 100 cards per minute

b. Punching modes

(1) Code: TRANSAC code is automatically translated and punched in the Hollerith mode.
(2) Card Image: twelve bits of a TRANSAC word are punched in one card column.

c. Format Control

(1) Punch plugboard

(a) Allows insertion of 8 columns of data.
(b) Determines number of words per card and cards to be punched per block off-line.
(c) Rearranges fields

(2) Special characters

(a) End-of-card and end-of-block characters facilitate handling variable length records, save time.

(b) Filler characters simplify editing.

(3) On-line: instruction determines number of words per card and cards per block.

d. Capacity: Input bin - 650 cards; output bin - 750 cards. Visible counter indicates number of cards punched.

5. Reliability

a. All photodiodes and preamplifiers are checked between each card reading.

b. Validity check on Hollerith code

c. Parity bits generated and checked between the punched-card controller and the buffer-controller, and after punching.

d. Checks made on format of data.

F. High-Speed Paper Tape System

1. Function:

Reads or punches paper tape as input or output from the central computer or the universal buffer-controller.

2. Control

May be controlled by the universal buffer-controller or operated directly through the real-time channel.

3. Operation with real-time channel

a. Transmission of up to 4096 words per instruction

b. Shares memory with input-output system and the central computer.

4. Tape specifications

   a. 5-or 7-channel tape, 11/16 or 7/8 inch widths

   b. Reader tape must be non-metalic, opaque, and non-oiled.

   c. Reel capacity: 350 or 700 feet

5. Operating characteristics

   a. Reading rate: 1000 characters per second (100 inches per second)

   b. Punching rate: 60 characters per second

   c. Photoelectric reading

   d. Starts and stops on one character.

   e. Stop character ends transmission (If switch is set).

   f. End-of-reel sensing, with automatic rewind option

   g. Blank tape is passed and ignored.

6. Checking

   a. Parity check for each character with 7-channel tape; bypass switch allows reading of 6 channels only.

   b. Tape tear or jam stops operation.

SECTION IV

PROGRAMMING TRANSAC S-2000

PROGRAMMING TOOLS

TRANSAC programming has been greatly simplified and shortened by the elimination of machine coding. Since the automatic programming system was developed in parallel with the design and production of the TRANSAC system, users may rely entirely on the automatic programs and never use machine coding methods. Basically, TRANSAC programming consists of linking instructions using simple mnemonic commands and symbolic addresses, with an extensive library of subroutines, generators, and macro-instructions.

Some of the programs already in existence are: TAC (TRANSAC Assembler and Compiler), ALTAC (Algebraic Translator into TAC), and IOPS (Input-Output Programming System). These programs insure a rapid mastery of TRANSAC programming techniques and fast coding of the user's applications.

The TRANSAC Assembler-Compiler operates on three levels of program automation represented by the mnemonic language, the subroutine library, and entire systems like ALTAC. The first of these, the mnemonic language, enables the programmer to take maximum advantage of TRANSAC's flexibility without the drudgery of coding in machine language. Two instructions written in the mnemonic language would appear on a coding form as shown in Figure 4-A. Of course the remarks would be omitted in an actual program.

Command	Address and Remarks	
TMA	DATA	Transfer from Memory to the A register, the contents of the memory location specified as DATA
JAZ	ZERO	Jump if the number in the A register is Zero. If a jump occurs, the next instruction will be taken from memory location ZERO.

Figure 4-A

Figure 4-A is merely an illustration of the instructions as they appear on the coding form. The explanation of how the instructions are written will be found later in this section.

The subroutine library is on the next level of program automation. A complete selection of scientific and commercial routines has been placed on a library tape for use in many different programs. The tape library is very useful in shortening the time required to program and checkout a problem. Through use of the tape library, the programmer may assemble a program quickly by incorporating into his program the tested routines furnished by Philco and the special routines developed by various TRANSAC users.

During compilation of the program, macro-instructions are placed in the program at the point where they are specified. To specify a macro-instruction, the programmer writes the name of the macro-instruction, such as TLUEQ (Table Look-Up for EQuality), in the command column of the coding form. The macro-instruction produces a number of machine instructions in the running program to accomplish a complete operation. Use of macro-instructions saves much coding time and insures that the operation is performed in an efficient manner.

Generators may be added to the TAC system at any time to increase its scope and power. Pseudo-code statements select a generator from the library tape. The statement is written by placing its name in the command column and defining its parameters in the address column of the TAC coding form. When the compiler (TAC) recognizes these statements, it defers action on them until the end of the program. Then the compiler generates the coding for all the statements and places it at the end of the program. The pseudo-statement in the program is then replaced by an instruction to jump to the generated coding. An advantage of a generator is that it provides only the amount of coding necessary for the specified parameters. In contrast, a subroutine is fixed, instead of variable and must always contain the same number of instructions.

IOPS, the input-output programming system, is an example of a TRANSAC generator. Its purpose is to create the necessary instructions to provide efficient input and output instructions for a program. In addition, the resulting instructions will convert and edit the input and output data into the desired form. When IOPS interprets a typical statement,

it will generate the coding to select a record, convert the fields (such as from decimal to binary) and place them in separate words, and initiate an input operation if the data in memory has been exhausted.

Subroutines differ from macro-instructions in that they follow the program, and from generators in that they are fixed or static. Subroutines, like macro-instructions and generators, are addressed by names such as SQRT (to compute square root) or EDIT (to edit a word for printing). The subroutine name is written on the coding form in the command column and its parameters are written in the address column.

The third level of automatic programming is represented by the ALTAC System. Using ALTAC, the programmer writes statements in an algebraic type of language. These statements are then translated by ALTAC into TAC language instructions, and further reduced by the TRANSAC Assembler-Compiler to machine code. During the process, TAC subroutines originally written in the basic TAC language are inserted where needed. For example, the formula, Y = nX + 5, is written in ALTAC language as; Y= N * X + 5$. ALTAC will convert this statement into TAC instructions, which will be converted in turn into TRANSAC instructions.

Mnemonic Instructions

After this general description of automatic programming with TRANSAC, the basic programming tools, the mnemonic instructions, must be described in more detail. A complete list of these instructions appears in Figure 4-B. The instructions are divided into ten functional classes which contain a total of 225 individual instructions.

Two main parts of an instruction are the command and address. The command part is composed of two to six letters, and is divided into three sections. The command part completely defines the operation to be performed, and specifies the origins of operands and the disposition of results.

For a specific example of how the command is written in the mnemonic code, the class of addition instructions is explained and shown in Figure 4-C.

NOMENCLATURE FOR FIGURE 4-G

M the specified memory location

A The A register
Q the Q register
D the D register
} one word arithmetic registers

I the instruction

X The selected index register

MA Memory Address register (the address of the currently accessed memory location)

PA Program Address register (the address of the next instruction word)

JA Jump Address register (the address of the instruction following the last jump instruction)

( ) Contents of

| | the absolute value of the contents of

→ is placed in

The following letters may be used as subscripts with the above letters.

L, R Left or Right half word

V Variable field of a word, usually the address part

F The function bit of a machine instruction

C The counter indicator of an index register

Examples of nomenclature usage:

D_{LV} The V part of the left half of (D)

JA_F The F bit associated with JA

$(X) = D_V$ The contents of the index register are equal to a V part of (D).

Figure 4-B

TRANSAC S-2000 INSTRUCTIONS

Instruction Class	Instruction	Mnemonic Code: Operation	Register or Condition	Option	Description of Operation	Notes	Code Example
Addition	Add	A	M Q	A, S	1. (A) + Operand ⟶ A 2. When result is stored: (A) ⟶ M (and D) The operand is from M or Q and may be in absolute value. Before step 1, A is cleared to zero for Clear Add.	Options: A = absolute operand S = result stored F = floating point Overflow: The overflow indicator is set when the result ≥ 1 or < -1.	AM AMA CAQS CAQAS
	Clear Add	CA					
	Add D	AD			(A) + (D) ⟶ A		
Subtraction	Subtract	S	M Q	A, S	1. (A) - Operand ⟶ A 2. When result stored: (A) ⟶ M (and D) The operand is from M or Q and may be in absolute value. Before step 1, A is cleared to zero for Clear Subtract.	Options: A = absolute operand S = result stored Overflow: The overflow indicator is set when the result ≥1 or < -1.	SM SMS SQA CSQAS
	Clear Subtract	CS					
	Subtract D	SD			(A) - (D) ⟶ A		
Multiplication	Multiply	M	A M	A R S	1. Operand x (Q) ⟶ A; Q or A rounded* 2. When result stored: (A) ⟶ M (and D) The operand is from M or A and may be in absolute value.	Options: A = absolute operand R = rounded product S = result stored Overflow: when the result = 1 * (Q) are unaltered when rounded.	MAR MMRS
	Multiply and Add	MAD			[(M) x (Q)] + (A) ⟶ A	The product is rounded. (Q) are unaltered.	
	Multiply and Subtract	MSU			[(M) x (Q)] - (A) ⟶ A		
Division	Divide A register	DA		S	1. [(A) or (A, Q)] ÷ (M) ⟶ Q, remainder ⟶ A 2. When result stored: (Q) ⟶ M (and D)	Option: S = result stored Potential overflow is detected if |M| ≤ |A|.	DA DAS DAQ DAQS
	Divide A and Q registers	DAQ					
Transfer	Clear	C	M, A, Q, D		0 ⟶ M or A or Q or D		CM
	Transfer	T	M, A, Q, D	M, A, Q, D	* Transfer [(M) or (A) or (Q) or (D)] to [M or A or Q or D]	*These are not optional. One letter must be selected. TMM, TAA, TQQ and TDD are not permitted.	TMA
Shift	Shift Left	SL	A AQ Q D	N	Shift the contents of the register (s) the number of places specified by the address. A numerical shift will preserve the sign of a word.	Option: N = numerical shift. No option specifies ordinary shift. (D) may only be shifted right	SLA SRQN
	Shift Right	SR					
	Shift Circular (D)	SCD			Shift (D) in circular mode right		
Jump	Jump	JMP		L‡ or R‡	Unconditional Jump	1. Address of next instruction ⟶ JA 2. Effective address ⟶ PA *Shift (Q) in circular mode left (for P or N) or right (for O or E) 1 position regardless of conditions. In these cases positive is defined as sign bit = 0; negative is sign bit = 1. ‡See notes for NOP and TJM. †JAGD treats words as alpha-numeric. For A and Q Comparisions, (Q) ⟶ D. Then (A) are compared to (D). In JAGQF the numbers should be normalized.	
	Breakpoint Jump	JBT			Stop if breakpoint switch set, jump if not		
	Jump if overflow	JOF			Jump if overflow indicator is set		
	Jump if no overflow	JNO			Jump if overflow indicator is not set		
	Jump if (D) are Positive	JDP			Jump if (D) are positive		
	Jump if (A) are + , -, 0	JA	P, N, Z		Jump if (A) are positive or negative, or zero		JAP
	*Jump if (Q) are + , -, odd, even	JQ	P, N, Q, E		Jump if (Q) are positive or negative, or odd or even		JQE
	Jump if (A) Equal (D) or (Q)	JAE	D, Q		Jump if (A) equal (D) or (Q)		JAED
	†Jump if (A) are Greater than or equal to (D) or (Q) or (Q)-floating point	JAG	D, Q, QF		Jump if (A) are greater than or equal to (D), or (Q), or (Q) if (A) and (Q) are floating point numbers.		JAGQ

Figure 4-B

TRANSAC S-2000 INSTRUCTIONS (Continued)

Instruction Class	Instruction	Mnemonic Code: Operation	Mnemonic Code: Operation or Half Word	Mnemonic Code: Option	Description of Operation	Notes
Index Register	Transfer Counter to Index	TCX	S, Z		$1 \rightarrow X_c$ if S, $0 \rightarrow X_c$ if Z	Option: C = Counter indicator is transferred. L and R specify left or right half of D register.
	Transfer Instruction address to Index	TIX			$I_v \rightarrow X$; $1 \rightarrow X_c$ if S, $0 \rightarrow X_c$ if Z.	
	Transfer from D to Index	TDX	L, R	C	D address $\rightarrow$ X	
	Transfer from Index to D	TXD			(X) $\rightarrow$ D address via JA	
	Add (D) to Index	ADX	L, R		(X) + D address $\rightarrow$ X	
	Subtract (D) from Index	SDX			(X) - D address $\rightarrow$ X	
	Add Instruction Address to Index and Jump	AIXJ			$(X) + I_v \rightarrow X$ } Jump to D right address if	
	Subtract Instruction Address from Index and Jump	SIXJ			$(X) - I_v \rightarrow X$ } (X) ≠ D left address	
	Add Instruction Address to Index and set Overflow	AIXO	L, R		$(X) + I_v \rightarrow X$ } Set Overflow if (X) = D address	
	Subtract Instruction address from Index and set Overflow	SIXO			$(X) - I_v \rightarrow X$ }	
	Repeat	RPT	N, A, S	N, A, S*	The next instruction or instruction pair is repeated the number of times specified by the address part of the RPT. If RPT is left half instruction, next instruction is repeated; if RPT is right half instruction, next pair of instructions is repeated.	*N, A, and S are not optional and specify no modification, add to and subtract from the index register(s) specified by the repeated instruction(s).
Extract	Extract from memory and: Transfer to D	ETD			Extract: bit by bit logical multiply (M) . (Q) $\rightarrow$ D; or mask (M) $\rightarrow$ D according to (Q)	Floating point mode is possible with EA and ES but is only in effect after the extraction.
	Transfer to A	ETA			1. e.g. M · Q $\rightarrow$ D: 1 0 0; 0 0 0; 1 1 1; 0 1 0	
	Add	EA			2. (D) $\rightarrow$ A or (A) ± (D) $\rightarrow$ A	
	Subtract	ES				
	Insert	EI			1. M Q A A after: 1 0 x x; 0 0 x x; 1 1 x 1; 0 1 x 0 — 2. When result stored (A) $\rightarrow$ D, (D) $\rightarrow$ M	After EI: (D) = (M) . (Q)
	Insert and Store	EIS				
Special	Larger Word	LWD			* If (M) > (A), (M) $\rightarrow$ A and M address $\rightarrow$ JA O $\rightarrow JA_F$	*Actually, (M) $\rightarrow$ D and (D) and (A) are compared in the alpha-numeric sense.
	Smaller Word	SWD			* If (M) < (A), (M) $\rightarrow$ A and M address $\rightarrow$ JA O $\rightarrow JA_F$	
	No Operation	†NOP		L or R	No operation	†L or R specifies I_F as 0 or 1
	Halt	†HLT			Stop Computation	
	Transfer (JA) to Memory	‡TJM			(JA) $\rightarrow$ M address, $JA_F \rightarrow M_F$ via D	‡L or R specifies the particular half word of M
	Transfer Instruction Address to JA	‡TIJ			Effective address $\rightarrow$ JA; $0 \rightarrow JA_F$ if L, $1 \rightarrow JA_F$ if R.	
	Increase Address in Memory	‡INCA			1 + M address $\rightarrow$ M address via D and JA; O $\rightarrow JA_F$	
	Inhibit Clearing of Overflow Indicator	ICO			Inhibits clearing of O.F. indicator before arithmetic.	#The skip instructions have a number of options described elsewhere in connection with the input-output instructions.
	Transfer from Console Typewriter to Memory	TCM			One character $\rightarrow$ 6 right bit positions of M and D	
	Transfer from D to Console Typewriter	TDC			Transfer left (6 bits) character of D $\rightarrow$ typewriter	
	Transfer from Toggle Register to D	TTD			Word set up with toggle switches $\rightarrow$ D	
	Transfer Control to Input Output	TIO			(D) $\rightarrow$ input-output control; execute this I/O instruction.	
	Skip Fault	#SKF			If no fault exists, the next instruction is skipped.	
	Skip Check	#SKC			Skip the next instruction if $I_V \geq$ the number in the specified input counter.	
	(D) or (M) bit by bit stored	DORMS			Binary ones from (D) or (M) $\rightarrow$ D, M (1+0=0+1=1 -=1;0+0=0)	
	Add without carry and store	AWCS			(M) + (A) without carries $\rightarrow$ D, M (1+1=0+0=0;0+1=1+0=1)	

OPERATION	LOCATION OF OPERAND	OPTIONS
Add or Clear Add	The operand from M or Q	in Absolute value and/or Store the result
A or CA	M or Q	A and/or S or blank

Figure 4-C

Thus the choice of operations is Add or Clear Add. The operand may either be in Memory or the Q register, and the possible options are: the operand may be in Absolute value, and the sum may be Stored. Some of the possible addition commands are listed in Figure 4-D.

MNEMONIC CODE	DESCRIPTION
AM	Add Memory
CAQ	Clear Add Q
AQS	Add Q and Store
CAMA	Clear Add Memory in Absolute value
AQAS	Add Q in Absolute value and Store

Figure 4-D

All arithmetic instructions will be executed in the floating point mode if an F is written as a prefix to the command. The commands in Figure 4-D would be written as follows to specify floating point mode: FAM, FCAQ, FAQS, FCAMA, and FAQAS.

The address part of the instruction tells the central processor where to locate the information desired. It may be written as an actual address, a symbolic address, or a relative address. Also this space may be used to write a number or a constant in place of an address, or to specify an index register with an increment or decrement. Different uses of the address part are shown in Figure 4-E. The command transfers a word from memory to the A register. The word transferred is shown to the right of the mnemonic instruction. A TAC coding form is shown on Page 65.

MNEMONIC CODING		WORD TRANSFERRED
TMA	1029	The contents of memory location 1029
TMA	29,3	The same word if index register 3 contains the number 1000
TMA	A/May, 1958	An alphanumeric constant
TMA	DATA	The contents of the memory location specified as DATA.

Figure 4-E

INPUT-OUTPUT INSTRUCTIONS

In addition to the central processor instructions shown on Figure 4-B there is a wide variety of input-output instructions. When a TIO (Transfer control to Input-Output) instruction is interpreted by the central processor, the input-output instruction which had been placed in the D register is transferred to the appropriate input-output controller. The TIO instruction is completed as soon as the transfer is completed and the central processor is free to proceed to other instructions while the input-output instruction is being executed. Figure 4-F shows the type of input-output instructions.

DESCRIPTION OF INSTRUCTION	QUANTITY OF DATA TRANSFERRED
Real-Time Device to Magnetic Core	Up to 4096 words
Magnetic Core to Drum	Up to 4096 words
Drum to Magnetic Core	Up to 4096 words
Magnetic Core to Paper Tape	Up to 4096 words
Paper Tape to Magnetic Core	Up to 4096 words
Magnetic Core to Buffered Output Unit	Up to 128 words
Input Device to Buffer-Controller	Up to 128 words
Buffer-Controller to Magnetic Core	Up to 128 words
Magnetic Core to Magnetic Tape - Forward	Up to 16 blocks
Magnetic Tape to Magnetic Core - Forward	Up to 16 blocks
Magnetic Tape to Magnetic Core - Backward	Up to 16 blocks

Figure 4-F

There are input-output instructions in addition to those in Figure 4-F which are used for rewinding tape, taking corrective action after error detection, and other routine work. It should be noted that the programmer using IOPS, ALTAC, and other subroutines and macro-instructions, will have little contact with the input-output instructions.

SPECIAL FEATURES OF TRANSAC INSTRUCTIONS

TRANSAC instructions contain a number of special features:

a. Arithmetic overflow cannot occur in fixed point division; it is detected before it occurs, the dividend is automatically shifted one place, and the program can attempt to divide again.

b. In floating point mode, an exponent overflow causes the program to jump to a diagnostic or corrective routine.

c. Information may be packed to save input-output time and efficiently manipulated by the flexible extract and shift instructions.

d. A wide variety of decision-making instructions allows words to be compared for magnitude and equality or to determine if individual numbers are zero, positive, negative, odd, or even.

e. Single bits may be examined.

f. When a jump occurs, the address of the next sequential instruction is automatically recorded in the JA register to be used for subroutine exits.

g. If any input-output instruction is not acceptable, it is bypassed so that a jump to a diagnostic routine can be effected. By this method, the central processor automatically determines if previous input-output operations have been completed correctly and interrupts the program if they have not. This procedure not only saves program steps and time, but also allows the input-output diagnostic instructions to be combined into one subroutine.

h. A group of special instructions (skip check) are used to determine when specific amounts of input-output data have been processed.

i. Another group of special instructions (skip fault) determines the nature of input-output faults so that the program may take corrective action without stopping the central processor.

SPECIAL INSTRUCTIONS

In addition to these features, there are some special instructions which are very valuable for many programs:

a. Repeat (RPT) - Repeats one or two instructions up to 4095 times. When the repeated instructions use index registers, the repeat instruction very efficiently transfers records, including variable-sized records, performs table look-ups; simplifies internal sorting and editing; and rapidly performs matrix multiplications.

b. Multiply and Add (MAD) -- Forms a product and adds it to the contents of the accumulator. Used with the Repeat instruction, it simplifies and rapidly forms the sum of the products of two sets of numbers, as in matrix multiplication.

c. Smaller Word (SWD) and Larger Word (LWD) - Compare a word in the A register with a word from memory. After the comparison the A register will contain the smaller, or larger, word and its address will be recorded in the JA register. Under Repeat control, SWD and LWD provide an extremely efficient method to sort records in memory.

SUMMARY

Programming TRANSAC is characterized by the lack of machine coding and the variety of programming aids in TAC, the TRANSAC Assembler-Compiler. The basic mnemonic language, which is simple to learn and easy to use, is supplemented by the complete library of macro-instructions, subroutines, and generators. In addition, the programmer may use the complete programming systems such as IOPS, for input-output, and ALTAC, for scientific applications.

1. Basic language

   a. English mnemonic commands

   b. Addresses may be absolute decimal addresses, symbolic addresses, or constants.

2. Macro-instructions

   a. One macro-instruction will insert many machine instructions in a program.

   b. Each macro-instruction needs to be specified only once.

3. Subroutine library

   a. Contains numerous mathematical and commercial routines.

   b. Specifications are provided each time a subroutine is executed, but each subroutine is included only once in a program.

4. Generators

   Provide only the number of instructions necessary to meet the programmer's specifications.

5. Other languages

   a. Other programming languages are being designed to meet future programming needs.

   b. ALTAC allows programmers to write scientific programs in algebraic form.

TRANSAC programming is in a state of constructive evolution. The modular expansion principle applies not only to the TRANSAC equipment but also to the automatic programs which are being developed. The data processing speed of TRANSAC and its large variety of instructions provide a good foundation for complete programming systems.

TRANSAC ASSEMBLER-COMPILER
CODING FORM

Page _____ of _____

Program:	Programmer:	Checked by:	Date:

IDENTITY & SEQUENCE (1)	L	LOCATION (10)	COMMAND (17)	ADDRESS AND REMARKS (25)

transac® s-2000

PHILCO®

FORM CS-658

SECTION V

INSTALLATION AND SERVICES

APPEARANCE

TRANSAC units have been styled to blend with any modern office decor. The pleasant blue-paneled units adjoin one another, minimizing the need for false flooring or concealed ductwork. Power is distributed by internal cabling and may be connected to the external source from any of several locations. The operating controls, indicators, and work positions have been designed and built according to the best human engineering standards.

FLOOR LAYOUT

A very large TRANSAC system (shown in Figure 5-A) occupies less than 1300 square feet, including working and access area, and room for expansion. If necessary, this system can be contained in a much smaller area without appreciably sacrificing convenience. This flexibility in the system floor layout is one result of the modular design. The modular design also enables the units to be packaged in sizes and weights which minimize rigging and other delivery costs. The floor loading is maintained under 55 lbs/sq. ft. Therefore, without raising other installation costs, the TRANSAC system can be contained in a minimum of valuable floor area with maximum operation and maintenance efficiency.

TEMPERATURE, HUMIDITY, and B.T.U. OUTPUT

Room temperature can vary from $60^{\circ}F$ to $80^{\circ}F$, with relative humidity between 40 to 60%. The heat dissipation varies with the number of operating units but a very large system will not exceed 136,000 BTU/hr. (40 KW system).

POWER REQUIREMENTS

The power required by a large TRANSAC installation is less than 40 KW. The 3-wire power input is 115 volts, single phase, 60 cycles, AC; or 4-wire 208 volts, three phase, 60 cycles, AC. The low power consumption of the TRANSAC System is an economy to be considered while estimating monthly operating costs.

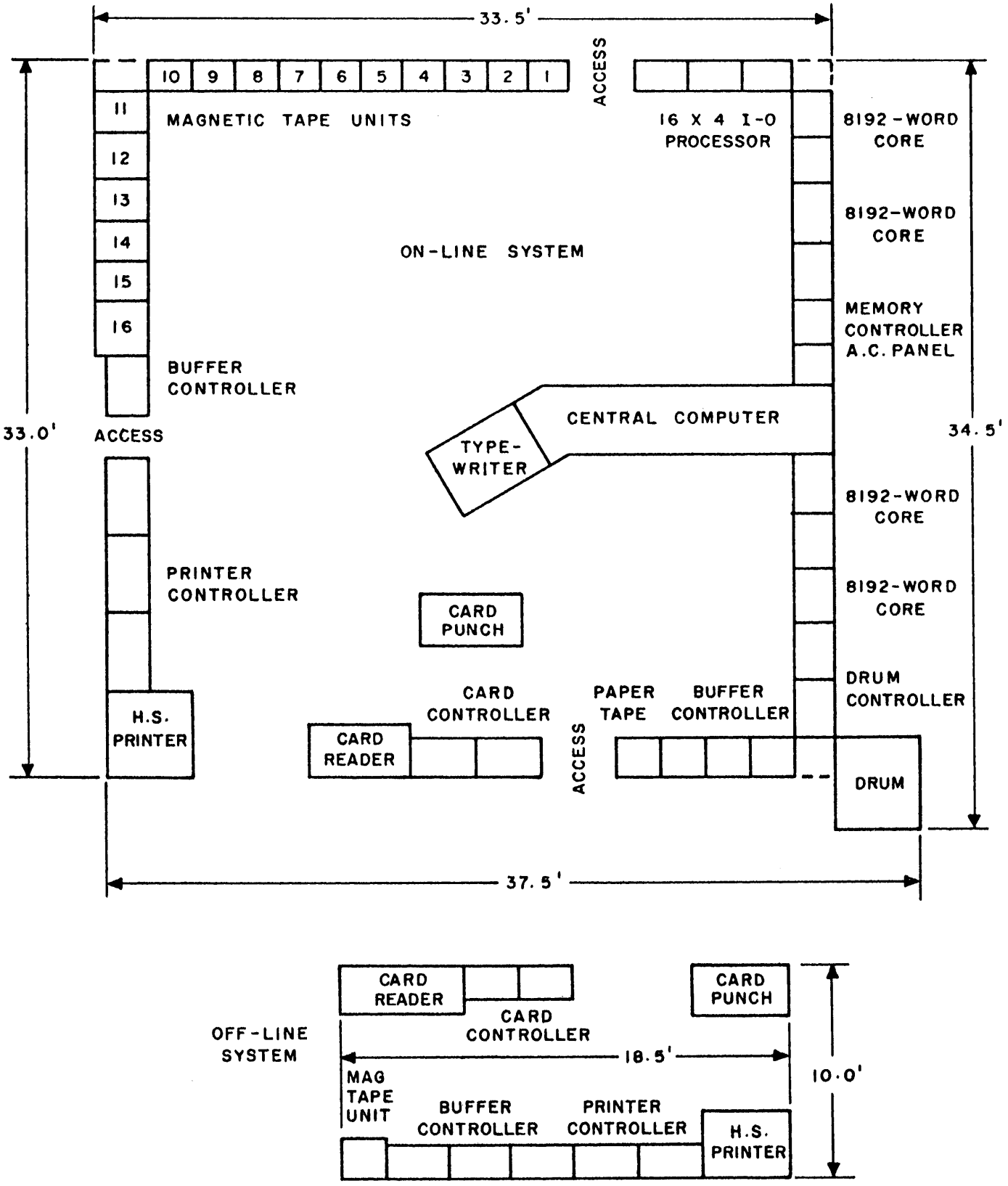


FIGURE 5-A. SUGGESTED FLOOR PLAN OF A TYPICAL LARGE SCALE TRANSAC S-2000 SYSTEM

AIR CONDITIONING

The TRANSAC System requires a minimum amount of air conditioning. In fact the present air conditioning plant at the installation site may have the capacity to carry the TRANSAC System. The number of tons of air conditioning equipment required is calculated from the B. T. U. /hour output. For the system shown in Figure 5-A, the tonnage is 136,000 B. T. U. 's/hour divided by 12,000 (12,000 B. T. U. 's/hour equals 1 ton of air conditioning) or 11.33 tons--which is rounded to twelve tons.

SERVICES

The Philco Corporation, as a result of its extensive experience in system design, manufacture, and maintenance of many types of complex electronic equipment, feels that the services described below are those required for optimum performance. Many problems that might otherwise arise after installation and during conversion are eliminated by thorough planning and provision of adequate service.

Throughout installation, conversion, and normal operation, management control remains with the customer. Philco's services are entirely advisory and auxiliary in nature. Each customer determines to what extent he requires these services. Philco will always supply the information and training to enable the customer to become self-sufficient in his own operation.

MANAGEMENT SEMINARS

For optimum utilization of the TRANSAC System, both middle and top-management need to understand the potentialities of this new management tool. Management support is vital to the success of the data processing effort. Therefore, Philco presents a continuing series of two-day seminars conducted either at the customer's facilities or at Philco's. These seminars are also open to companies still in the feasibility study phase.

Seminars are valuable to acquaint present management with the possible applications of TRANSAC in their departments, familiarize new executives with modern electronic data-processing methods, and update customer management from time-to-time on new applications and capabilities.

Seminars conducted at Philco give management an opportunity to discuss their systems and proposed applications with Philco's large staff of data-processing and management specialists. Some of these seminars are restricted to selected groups of executives on common levels from different companies who have similar applications. These groups offer an excellent opportunity for discussion of common problems in a relaxed and productive atmosphere.

TRAINING

Three types of training are available: programming, operation, and maintenance. Maintenance training, however, is usually provided only to a customer who purchases a TRANSAC System without a service contract. Normally, the classes are conducted at the most convenient location for the customer, but in some cases, Philco may suggest a location in order to make the best use of training personnel and facilities.

PROGRAMMING COURSE

A programming course can be started within thirty (30) days after a contractual agreement is made. The length of the course varies from 120 to 320 class-hours depending on the experience and learning ability of the class members. The complete programming course includes instruction in:

(1) Basic machine programming

(2) Program testing

(3) Use of automatic programming techniques

OPERATION

The operators course is usually scheduled to be completed at the same time as the installation of the TRANSAC System. The length of the course ranges from 80 to 240 hours depending on the variety of equipment in the customer's TRANSAC System and the varied backgrounds of the operators in the class. The operators are trained to operate all

the equipment in the system, to recognize errors, and to assist in program testing.

PROGRAMMING ASSISTANCE

Philco maintains an experienced staff of programmers for on-site assistance to a customer. Such assistance is provided to the extent needed by a customer, and includes:

(1) Detailed systems analysis

(2) Programming

(3) Program testing, and

(4) On-the-job training.

Constant research and development work on automatic programming methods is being performed by Philco. The results of this effort are apparent in the TRANSAC Assembler-Compiler (TAC), the Algebraic Translator (ALTAC) and the complete library of routines provided for TRANSAC users.

Philco will provide alternate facilities to meet a customer's data processing commitments in the event of power or other failure affecting the customer's TRANSAC System. During program testing and conversion operations, the customer may utilize the TRANSAC Installations at Philco's Western Development Laboratories in California or at the Corporate Headquarters in Philadelphia.

INSTALLATION AND MAINTENANCE

TRANSAC Customer Engineers install and maintain the TRANSAC Systems. Installation planning begins when the TRANSAC System is ordered and continues until the System is completely installed. This thorough planning results in a System being installed in the shortest possible time with minimum disruption of the customer's operations.

Philco's or the customer's engineers are trained to have a detailed

understanding of the logic of the TRANSAC System, complete knowledge of system circuitry, and a thorough understanding of the methods and techniques of efficient maintenance. Minimum course length varies from 800 to 1400 hours depending upon the equipment selected for the customer's installation. The customer engineers assigned to the customer's installation assist in the final check-out of the customer's system at the factory, perform the installation of the system, and remain on the site to insure optimum performance of the TRANSAC equipment.

Philco has been supplying engineers to maintain complex electronic equipment since 1933. Today over 3,500 Philco field and customer engineers throughout the world represent the pool of experience and manpower behind Philco's maintenance contracts.

SUMMARY

Any prospective customer is cordially invited to visit Philco, inspect our training facilities, review our training manuals, and discuss his service problems with our Training, Customer Engineering, and Customer Services Staffs. Since the services provided by the manufacturer can determine the success or failure of a customer's installation, Philco welcomes your inspection. We urge you to investigate thoroughly all services proposed by any manufacturer before investing in equipment as complex and as costly as a large-scale electronic data-processing system.

SECTION VI

EQUIPMENT LIST

The present product-line units are listed in Figure 6-A. The interconnection of these units is shown by Figure 2-F. Figure 6-A also indicates the minimum and maximum number or size of each unit possible in a specific TRANSAC system.

Many special units, such as data plotters and displays, are available by special order. Your special requirements should be discussed with your TRANSAC representative. He will include recommendations to satisfy these requirements in your TRANSAC proposal. Price lists will be furnished on request. Contractual agreements may be negotiated with firm delivery dates and specifications.

Figure 6-A

List of Equipment

List Number	Description	Minimum	Maximum
I	CENTRAL COMPUTER		
A	Central Processor Unit	1	1
	Includes: Arithmetic, Program, Console Typewriter, Display & Manual Control, Power Supply and Distribution Sections.		
B	Floating Point Components	0	1
C	Index Registers		
	Either, none, or one of the following groups may be selected.		
1	Index Registers (Group of 8)	0	1
2	Index Registers (Group of 16)	0	1
3	Index Registers (Group of 32)	0	1
D	Magnetic Core Storage System		
	One of the following units must be selected. The maximum size is not shown. Larger sizes may be obtained by special order.		
1	Magnetic Core Storage Unit (4,096 words/unit)	0	1
2	Magnetic Core Storage Unit (8,192 words/unit)	0	1
3	Magnetic Core Storage Unit (16,324 words/unit)	0	1

Figure 6-A (Continued)

List Number		Description	Minimum	Maximum
	4	Magnetic Core Storage Unit (32,768 words/unit)	0	as specified
E		Magnetic Drum System Consists of list No.'s E1 and E2		
	1	Magnetic Drum Unit	0	32
	2	Magnetic Drum Controller (Controls up to four drum units)	0	8
II		INPUT-OUTPUT (On-Line System)		
A		Input-Output Processor A minimal system without an input-output processor uses an input-output system connected through the real-time channel, and the console typewriter for input-output		
	1	Input-Output Processor (16 I-O channels; one operates simultaneously with processing)	0	16
	2	Input-Output Processor (16 I-O channels, 2 channels operate simultaneously)	0	16
	3	Input-Output Processor (16 I-O channels, 3 channels operate simultaneously)	0	16
	4	Input-Output Processor (16 I-O channels, 4 channels operate simultaneously)	0	16

For the following units, the maximum figures pertain to a system with one input-output processor and may be increased proportionally.

List Number		Description	Minimum	Maximum
B		Universal Buffer-Controller (any combination of B1 and B2 up to four on-line)		
	1	Universal Buffer-Controller (Magnetic tape unit operates off-line only)	0	4
	2	Universal Buffer-Controller (Electronic switching for on-line/off-line magnetic tape unit)	0	4
C		Magnetic Tape Unit (Maximum figure includes: 12 connected on-line to I-O channels; 8 connected to universal buffer-controllers)	0	20

(The total number of input-output systems connected to four buffer-controllers is 28.)

D		Punched-Card System Consists of list No.'s D1, D2, and D3.		
	1	Punched-Card Reader	0	28
	2	Punched-Card Punch	0	28
	3	Punched-Card Controller	0	28
E		High-Speed Printing System Consists of list No.'s E1 and E2		

List Number	Description	Minimum	Maximum
1	Printer Controller (High Speed)	0	28
2	High-Speed Printer	0	28
F	Paper Tape System Consists of list No.'s F1, F2, and either F3 or F4.		
	Connected through universal buffer-controller.	0	28
	Connected through real-time channel	0	1
	Total possible	0	29
1	Paper Tape Reader	0	29
2	Paper Tape Punch	0	29
3	Paper Tape Controller (Through real-time channel)	0	1
4	Paper Tape Controller (Through universal buffer-controller)	0	28