There are four pages of schematics:
1) Main power supply, sync conditioner, and video drive circuitry.
2) High voltage circuitry associated with the CRT.
3) Horizontal deflection circuitry.
4) Vertical deflection circuitry.

1) Main power supply, sync conditioner, and video drive circuitry.

1.1) Main power supply:

Note: Because the horizontal and vertical power circuitry are referenced to the NEGATIVE POWER rail, the convention NNrNEG is used to indicate that 'NN' is the voltage referenced to NEG PWR and not to GND.

Example: +18rNEG means +18VDC referenced to NEG PWR.

Monitor operates with two different DC input schemes:

1) POS POWER equal to +12VDC.
NEG PWR equal to -12VDC.
Both POS and NEG PWR returned to GND.
Power consumption:
Portrait = 50 watts.
Landscape = watts.

2) POS PWR equal to +24VDC.
NEG PWR and GND tied together.
Power consumption:
Portrait = 55 watts.
Landscape = watts.

Both schemes require +/- 10% voltage regulation.

The LM350/LM338 develops +18rNEG for the rest of the monitor. This +18rNEG can be adjusted +/- 1 Volt by using the WIDTH pot which changes the width of the raster.

1.2) Sync conditioner:

The incoming TTL levels for horizontal and vertical sync are sissored around +1.3VDC by the LM393 and converted to levels referenced to NEG PWR.

1.3) Video drive circuitry:

The video signal is connected by coax. This TTL level is terminated with 75 ohms to +3VDC, and drives a 74F04. The 74F04 direct drives the complimentary push-pull output stage consisting of a 2N5160 and a 2N3866. The CRT CATHODE drive voltage swings between +12VDC and +37VDC. The cathode drive is fixed; there is no contrast control.

A private 7805 voltage regulator makes +5VDC for the 74F04. The output stage requires +42VDC which comes from the TIP41 which in turn gets its input +67rNEG from the horizontal deflection circuit.

A TTL high level on Video In makes +12VDC at the cathode which is white on the CRT screen.

A TTL low level at Video In makes +37VDC at the cathode which is black on the CRT screen.

Note: Scope probe capacity will considerably degrade the CRT cathode signal rise and fall times.

2) High voltage circuitry associated with the CRT.
The horizontal and vertical deflection circuits provide signals to dynamically focus the CRT. Also, the horizontal deflection circuit provides +540rNEG, +1100rNEG, and -150VDC to the CRT circuitry.

2.1) The CRT FOCUS signal is a sumation of DYNAMIC FOCUS and STATIC FOCUS.

2.1.1) The DYNAMIC FOCUS amplifier sums H PARA (horizontal parabala) and V PARA (vertical parabala). Using the DYNAMIC FOCUS pot this combined waveform is typically adjusted to a slightly clipped 500 Vpp signal.

Note: Scope probe loads down this signal.

2.1.2) The STATIC FOCUS is typically set in the range of -100 to +500VDC using the FOCUS pot.

Note: Scope probe or DVM loads down this signal.

2.2) The CRT GRID2 is typically set at +700 to +900VDC using the GRID2 pot.

Note: Scope probe or DVM loads down this signal.

2.3) The CRT GRID1 is a combination of USER BRIGHTNESS and BRIGHTNESS RANGE, both of which are pot adjustable. Using these two pots CRT GRID1 can be adjusted from -35 to -105VDC. A less negative value makes the screen brighter.

2.4) The CRT FIL1 recieves +6.3VDC from the 7805 voltage regulator. The adjustment pin of the regulator also provides current to forward bias two diodes to +1.3VDC in the Sync conditioner circuitry.

3) Horizontal deflection circuitry.
This circuit consists of the horizontal oscillator chip, the horizontal driver, the horizontal output transistor and flyback transformer.

3.1) Horizontal oscillator chip
This chip is a TDA 1180. It consists of PHASE 1 (phase comparator), oscillator, and PHASE 2 (phase shifter) with its AMP. It is powered by the 7812 voltage regulator.

3.1.1) PHASE 1
The PHASE 1 (phase comparator) locks the oscillator to the H SYNC (horizontal sync) using the PLL (phase lock loop) components at pin 13.

3.1.2) Oscillator
The oscillator frequency is determined by the time constant of the components at pins 14 and 15. Using the H FREQ pot the free running frequency is adjusted to 64 KHZ.

3.1.3) PHASE 2

PHASE 2 compensates for the delay introduced by the horizontal output circuitry. The flyback pulses to pin 6 and the oscillator waveform are compared resulting in a control current which, after it has been filtered by the external capacitor at pin 5, is sent to the phase shifter portion of PHASE 2. This adequately regulates the phase of the output pulses at pin 3.

The H CENTERING pot injects current into the shifter at pin 5, thereby varing the delay between H SYNC and the flyback pulse on pin 6. This has the effect of centering the rastor horizontally.

3.2) Horizontal Driver

The phase shifter output pulses on pin 3 switch a MPS-U01A horizontal driver. The square wave at the collector of the MPS-U01A has a 4:1 voltage step-down as it is transformer-coupled to the horizontal output transistor. The primary has an RC snubber to control overshoot. Components on the secondary, and the transformer's own leakage inductance, insure hard switching of the horizontal output transistor.

3.3) Horizontal output transistor and flyback transformer

The transistor MJ16012 in conjunction with the yoke and flyback transformer make the sawtooth current through the yoke and act as a switching power supply to make all the voltages for the CRT as well as its own boost voltage.

3.3.1) The boost voltage of +67rNEG for the horizontal output transistor is stepped up from the main power supply voltage +18rNEG by the flyback transformer during the first part of the visible scan. This +67rNEG is applied across the yoke during the 12 micro second visible portion of the scan. The resulting yoke sawtooth current is about 10 amps peak. This current flows through the reverse diode MR2406 during the first half of the visable scan, and through the MJ16012 during the last half. The .01/.018 uF. flyback capacitor reverses the current flow during retrace.

The yoke current is slightly modified by the L1 asymetric linearity coil and the 0.82mf 'S' capicitor. The H PARA voltage for dynamic focus is generated across this capacitor.

The +67rNEG also powers the video circuitry.

3.3.2) CRT auxillary voltages.

3.3.2.1) +540rNEG

When the MJ16012 is initially biased off, a +540 volt flyback pulse is generated by the YOKE and appears across the flyback transformer. This pulse, which has a width of 3.0 micro seconds, is rectified to make +540rNEG for the dynamic focus circuitry.

3.3.2.2) +1100rNEG

The flyback transformer steps up the flyback pulse to +1100rNEG for the CRT GRID2 and for the static FOCUS circuit.

3.3.2.3) 17KVDC

The secondary of the flyback transformer has a winding to make 17KVDC for the CRT ANODE. The rectifier diode and bleeder resistor are molded into the flyback transformer.

3.3.2.4) -150VDC
Another secondary of the flyback transformer makes -150VDC which is used at the CRT GRID1 for BRIGHTNESS control.

4) Vertical deflection circuitry.
The main component of the vertical deflection circuit is the TDA 1670A. This chip contains:

4.1) 60 HZ oscillator
The oscillator is of sufficient accuracy to not require a vertical hold control. The V SYNC (vertical sync) signal syncronizes the oscillator at vertical retrace.

4.2) Ramp generator
The ramp at pin 10 is adjusted by the HEIGHT pot and the V LIN (vertical linearity) pot. The HEIGHT pot changes the vertical size of the rastor, while V LIN equalizes the top and bottom of the rastor.

The V PARA (vertical parabala) signal, used for DYNAMIC FOCUS, comes from the collector of the 2N5089 and is the integral of the ramp signal.

4.3) Ramp amplifier
The amplifier drives the yoke. The yoke current is sensed by a fractional ohm, current sampling resistor. This signal applies negative feedback to the AMP at pin 12. During vertical retrace, a flyback booster provides a 35 volt pulse to the yoke.

The V CENTERING (vertical centering) pot adjusts the vertical position of the rastor by varing a DC current through the yoke.

Alignment procedure for the 1k monitor - - revised 11 Apr 83 AFH+JSK

The purpose of this procedure is assure proper functioning of the UUT and to factory set the UUT to a standard baseline.

Equipment required;
1) Unit Under Test (CRT, PCB, yoke, flyback)
2) Power supply
3) Hatch pattern video generator
4) CRT mask grid
5) Oscilloscope
6) DVM

1) First, be sure that the initial test procedure has been completed, with the following setup:
1.1) Set all pots to midrange (there are 10 pots).
1.2) Power scheme:
POS PWR equal to +24VDC.
NEG PWR and GND tied together.
1.3) Plug in all connectors:
4.1) J1 - Input
4.2) J2 - CRT
4.3) J3 - CRT GND
4.4) J4 - YOKE
4.5) J5 - Flyback Transformer
1.4) Set User Brightness pot to 75% clockwise.
1.5) Apply power to UUT.
1.6) Adjust Grid2 pot upward until hatch pattern is visable on tube.

2) Adjust H Hold (horizontal hold).
2.1) Short H Sync (J1 pin 5) to GND (J1 pin 2 or 3).
2.2) Adjust H Hold for "stable" picture; the vertical lines of the hatch pattern should be essentially vertical rather than diagonal.
2.3) Remove H Sync short to GND; hatch pattern should be solid at this point.

3) Horizontal adjustment.
3.1) Move the centering rings on the yoke to be opposite each other. This is their minimum effect.
3.2) Adjust User Brightness pot to approximately 90% CW rotation.
3.3) Adjust Grid2 pot until the 'blanked' portion of the raster outside the hatch pattern is just visible.
3.4) Cock the yoke so that the raster runs diagonally across the tube. Verify that the H Cent pot will move the hatch pattern horizontally from one edge of the total raster scan to the other.
3.5) Return the yoke to its proper position and adjust both H Size and H Cent pots until the hatch pattern is properly positioned with respect to the CRT mask grid. Be sure yoke is snug against 'bell' of CRT or raster may become lopsided and have poor corner focus.
3.6) If the raster does not fit properly in the screen area, it may be necessary to 'pull' the raster with the yoke centering rings. Use only as much as necessary since the rings tend to distort the raster shape and focus
3.7) Check for 'bowing' of the hatch pattern, ie. both the left and right side (or top and bottom) bent the same direction. Adjust the yoke centering rings until opposite edges 'bow' in opposite directions about the same amount. This adjustment is somewhat of a fudge factor.
3.8) Recheck 3.5 and 3.6 if necessary.

4) Vertical adjustment.
The proper vertical alignment of the hatch pattern requires adjusting V Size, V Lin, and V Cent. These three pots are to be adjusted together so that:
4.1) The top and bottom of the hatch pattern matches the marks on the CRT mask grid.
4.2) The vertical centerline of the hatch pattern matches the centerline mark on the CRT mask grid.
4.3) Check for vertical 'bowing' as in 3.7.
4.4) It may be necessary to recheck 3.5, 3.6, 4.1, and 4.2 if the rings are moved.

5) Focus asjustment.
5.1) Dynamic focus.
5.1.1) Loosely couple scope probe with CRT focus lead (J2 pin 10; orange wire) by draping orange wire over the scope probe. Set scope to about 2 Volts/Div and time base to 5 Milliseconds/Div.

The picture on the oscilloscoope should be something like a very fat hour glass laying on its side.

5.1.2) Adjust the Dyn Focus pot so that the "waist" of the hour glass is about 75% the size of the hour glass "hip". This is the greatest amount of dynamic focus that can be generated.
5.2) Static focus.
Adjust the Static Focus pot for the best picture. If the dynamic focus is correct, all places on the picture should come into their best focus at the same setting of the Static Focus pot.

5.2.1) On occasional tubes, it may be noted that the Static Focus pot has one 'optimum' setting for the center of the screen, and a lower setting for the corners. If this is the case, reduce the dynamic focus and try again.
5.2.2) If it is noted that the corner 'optimum' setting seems higher that the center setting, then there is not quite enough dynamic focus. Since 5.1.2 produces the maximum available, try to adjust Static Focus for optimum focus in an area halfway between the screen center and a corner.
5.2.3) In general, all CRTs have one corner that is more poorly focused than the others. In adjusting Static Focus, pay special attention to the poor corner to bring it to its best focus. (Note: The yoke rings may affect the poor corner.)

6) Brightness Adjustment.
6.1) Note present brightness of display. Measure Grid2 voltage with DVM. Since DVM loads down Grid2 it is necessary to readjust Grid2 pot to get the same brightness as before; now note Grid2 voltage.

6.1.1) If Grid2 voltage is below 700 volts, turn Brightness Range pot down (less bright display) and readjust Grid2 to original brightness. Redo 6.1
6.1.2) If Grid2 voltage is above 900 volts, turn Brightness Range pot up (brighter display) and readjust Grid2 to original brightness. Redo 6.1.
6.2) Remove DVM and readjust Grid2 pot to original brightness.

7) Check video drive to CRT.
7.1) Check the CRT cathode drive with a scope. The voltage levels should be +12 volts and +37 volts within a few volts.

7.2) Disconnect the scope probe and set the hatch generator to make a black hatch on a white background. Turn down the User Brightness pot until the display is dim, and study the image quality. There should be a crisp edge of equal intensity on both the right and left side of the vertical lines. That is, the lines should not 'smear' black to their right, nor have an overly bright righthand edge, else the video waveform is misshapen.

7.3) Return the User Brightness to 90% ClockWise, and study the relative thickness of the vertical and horizontal lines. They should appear to be equally thick with both the black hatch and the white hatch.

8) Check horizontal drive timing.
Scope the voltage on the base of the horizontal output transistor. There should be at least 500 ns. between the spike at the end of the flyback pulse and the beginning of base drive.

10) Check vertical freerun frequency.
Short V Sync (J1 pin 6) to GND (J1 pin 2 or 3). Check the period of the vertical sweep (at the current sense resistor for instance) at 17.0 ms. to 22 ms.

11) With this, the functional test and factory setup of the UUT is complete.

Initial test procedure for the 1k monitor - - revised 11 Apr 83 AFH+JSK

The purpose of this test is to check for any gross problems, such as shorted track, components mispositioned, etc., before going on to final alignment.

Equipment required:
1) Unit Under Test (PCB, yoke, flyback, optional CRT).
2) Power supply.
3) Oscilloscope.
4) DVM.
5) High Voltage Tester.

1) Set all pots to mid-range (there are 10 pots).

2) Power scheme:
POS PWR equal to +24VDC.
NEG PWR and GND tied together.

3) Plug in all connectors except flyback:
3.1) J1 - Input
3.2) J2 - CRT (if available)
3.3) J3 - CRT GND
3.4) J4 - YOKE
3.5) J5 - DO NOT PLUG IN FLYBACK TRANSFORMER AT THIS TIME !!

4) Set USER BRIGHTNESS pot to 75% ClockWise.

5) Apply power to UUT and:
5.1) Listen for 60 HZ hum in YOKE.
5.2) Look for CRT FILAMENT becoming red hot (if CRT is available).

6) Using DVM check MAIN POWER regulator LM350/LM338 for about +18VDC output.

7) Using Oscilloscope check current sense resistor (0.47/0.68 Ohm) in vertical circuit for 1 Vpp sawtooth (with 17 millisecond period if a sync source is connected).

8) Using Oscilloscope check collector of MPS-U01A in horizontal drive for +18 Volt square wave with 16 microsecond period; 10 microseconds at +18 V, and 6 microseconds at 0 V.

9) TURN OFF POWER TO UUT !!

10) Plug in FLYBACK TRANSFORMER at J5.

BE SURE CRT IS GROUNDED at J3 !!

11) Apply power to UUT.

12) Using Oscilloscope check the collector of the MJ16012 for a +540 Volt, 3 microsecond pulse with a 16 microsecond period.

Observe knee of curve for sharp, linear rise time.

13) Using DVM check:
13.1) +540 Volts.
13.2) +1100 Volts.
13.3) -150 Volts.

14) Check current consumption of +24VDC with a CRT connected for about:
Portrait: 2.3 Amps.
Landscape: 3.1 Amps.

These values will be about 0.3 Amp lower if a CRT is not connected.

15) Turn up Grid2 until an image is visible on the screen (if CRT is available).

16) Using the High Voltage Tester, check the 17 KV.

17) Turn off power to UUT, it passes initial test.