DNA ICE

HARDWARE DESCRIPTION

The ICE Operating System will reside in memory space 60K - 63K. Space 63 - 64K will be operating system RAM. When power is applied or the ICE RESET pushbutton is pressed execution will go to location 60K. When the GAME RESET pushbutton is depressed execution will go to location 0.

The WP bit and RAM WRITE register control memory protection. The RAM WRITE register contains 16 bits and is at output ports FA and FB. Each bit corresponds to a 4K block of memory. Bit 0 of port FA corresponds to 0 - 4K, bit 7 of port FB corresponds to 60 - 64K. If a bit in the register is set to "1", its corresponding memory block will be write protected if the WP bit is set (bit 0 of output port FF). If WP is not set, then no memory will be write protected. Memory protection does not apply to external memory (memory in the Bally Arcade, Pinball, Add-On). The RAM WRITE register and WP bit are assumed to be in a random state when power is applied. The RESET pushbuttons have no effect on the register.

The RAM READ register controls which blocks of memory are internal to the ICE and which are external. The register is 16 bits long and each bit corresponds to a 4K block of memory. Bit 0 of output port F8 corresponds to 0 - 4K and bit 7of output port F9 correspondsto 60 - 64K. If a bit is set to "1", then the corresponding memory is considered to be external to the ICE (HVGSYS, screen memory.) The RAM READ register is assumed to be in a random state when power is applied. The RESET pushbuttons have no effect on the register.

Execution can be broken at a memory read or write at a specified address or an I/O read or write at a specified address. The break will occur after the instruction is executed. The address is specified by the BRK ADDRESS register, output ports FC and FD. The type of break, and whether or not a break is enabled is controlled by the BRL ENABLE register, output port FE.

FUNCTION	OUTPUT PORT FE
brk disable	00
brk on memory read	0A
brk on memory write	06
brk on input	09
brk on output	05

Execution can also be broken by pressing the BRK pushbutton. When execution is broken an NMI will occur, the PC will be saved in the PC register and execution will proceed to location F066. The PC can then be retrieved in the following manner:

1. Read from port F2.
2. Save in RAM (this is PC low).
3. Read from port F2.
4. Save in RAM (this is PC high).

Some time after reset and after breaks the operating system must jump to the upper 4K of memory and then execute an output instruction to the BRK ENABLE register. After this the system can access memory below 60K.

The system is capable of debugging user defined programs as large as 64K even though the operating system resides in memory space 60 - 64K. To do this the software must control three special control bits of output port FF. They are shown below, WP was described previously.

Bit

0 WRITE PROTECT (WP)
1 EXECUTIVE WITH 60 - 64K RAM (EX)
2 READ OR WRITE TO 60 - 64K RAM (RW)

The following are the procedures to be followed by the operating system in reading or writing from user RAM and executing programs from user RAM.

POWER UP ROUTINE

1. Set WP (01 to Port FF)

WRITE TO RAM

1. Disable brk point
2. Turn off WP and turn on RW (04-Port FF)
3. Do the Write (LMA)
4. Turn on WP (01 to Port FF)

READ FROM RAM

1. Disable brk point
2. Turn on RW (05 to Port FF)
3. Do the read (LAM)

EXECUTE FROM RAM

1. Turn on WP and EX (03 to Port FF)
2. JMP scratch pad RAM
3. Restore ACC
4. EI or DI
5. JMP to location

EXECUTE USING 60 - 64K AS OPERATING SYSTEM

1. Turn on WP (01 to Port FF)
2. Go to location In this mode breaks will not work.

There is no way to disable memory writing to external RAM (Bally Arcade screen or Magic RAM). If the Bally Arcade is connected to the system and the software writes to location 0 in internal memory, then location 16K on the screen will also be written to. If this is undesirable, the software must first read from 16K, save the result, write to 0, and then restore the value that was originally at 16K.

The Floppy Disc is controlled in the following manner:

1. Disable Arcade Interrupts by sending 05H to port 0EH.
2. Enable floppy interrupts by sending 04 (for drive 0) or
3. An interrupt will occur when data is to be read from the floppy.
4. During interrupt acknowledge a NOP will be placed on the data bus.
5. Interrupts will occur once every 25 usec.

The ICE hardware can be placed in any of three different configurations, depending upon the application. For doing asemblies and editing the internal Z-80 should be used. This Z-80 runs at 2.5 Mhz. The INT/EXT toggle switch should be placed in the INT position. When operating in this mode it does not matter whether or not an external system (ARCADE, PINBALL, ETC.) is connected to the ICE. However, it is impossible to access memory or I/O ports in an external device when operating in this mode.

If it is necessary to access memory or I/O in an external system, as in running a program for the system, then one of the final two configurations must be used. For both of the final two configurations the INT/EXT switch must be placed in the EXT position and the system clock is the clock of the external device. In one configuration the ICE Driver Board must be connected to the external device through the 50-pin DNA bus connector. This is possible only if the external device has a 50-pin DNA bus connector (ARCADE, COMMERCIAL ARCADE, ARCADE ADD-ON, or PINBALL). If the 50-pin connector is used, then chips U6 and U12 must be removed from the ICE Driver Board. If the ICE is plugged into an ARCADE or ARCADE ADD-ON, then the 1 uf Reset capacitor must be removed from the ARCADE. If plugged into a ADD-ON, the ADD-ON switch must be in ADD-ON mode. It is desirable to use the 50-pin connector when it is not appropriate to open the case of the external device.

If the device does not have a 50-pin connector, then the 40-pin twisted pair connector must be used. In this mode a 40-pin twisted pair cable is connected between the ICE Driver Board and Z-80 socket in the external device. If this mode is used, chips U6 and U12 must remain in the ICE Driver Board. The 40-pin connection can be used with any external device, whether or not it has or ARCADE ADD -ON if the 40-pin connector is used.

ICE PORT ASSIGNMENTS

PORT NO.	INPUT	OUTPUT
E0	UART CRT DATA	UART CRT DATA
E1	UART CRT STATUS	UART CRT CONTROL
E2	UART RS232C DATA	UART RS232C DATA
E3	UART RS232C STATUS	UART RS232C CONTROL
E4	FLOPPY	FLOPPY
E5	FLOPPY	FLOPPY
E6	FLOPPY	FLOPPY
E7	FLOPPY	FLOPPY
E8		
E9		
EA		
EB		
EC		
ED		
EE		
EF		
F0		ASSEMBLER ENABLE
F1		FLOPPY SELECT & ENABLE
F2	PC REGISTER	
F3		
F4		
F5		
F6		
F7		
F8		RAM READ (0-7)
F9		RAM READ (8-15)
FA		RAM WRITE (0-7)
FB		RAM WRITE (8-15)
FC		ADDRESS BRK (MSB)
FD		ADDRESS BRK (LSB)
FE		BRK ENABLE
FF		WP,EX,RW

BAUD RATE CONTROL

Switches 5,6,7,8 control the band rate for the CRT UART. Switches 1,2,3,4 control the band rate for the spare UART. The two band rates are independent and should be programmed as follows:

Band Rate	Switch 4 8	3 7	2 6	1 5
50	ON	ON	ON	ON
75	ON	ON	ON	OFF
110	ON	ON	OFF	ON
134.5	ON	ON	OFF	OFF
150	ON	OFF	ON	ON
300	ON	OFF	ON	OFF
600	ON	OFF	OFF	ON
1200	ON	OFF	OFF	OFF
1800	OFF	ON	ON	ON
2000	OFF	ON	ON	OFF
2400	OFF	ON	OFF	ON
3600	OFF	ON	OFF	OFF
4800	OFF	OFF	ON	ON
7200	OFF	OFF	ON	OFF
9600	OFF	OFF	OFF	ON
19200	OFF	OFF	OFF	OFF

ON means a closed switch.

RS232-C CONNECTORS

Connector J1 must be connected to the system CRT. It's pinout shown below. The baud rate for this interface is determined by switches 5,6,7,and 8 on the I/O Board.

Connectors J2 and J3 are wired to the same Uart and the baud rate is controlled by switches. 1,2,3,and 4 on the I/O Board. Both connectors cannot be used at the same time. J2 is used when the ICE is to be treatd as a terminal and the device it is talking to is to be treated as a Data Set. J3 is used when the ICE is to be treated as a Data Set and the device it is talking to is to be treated as a terminal. Pinouts are shown below.

RS232-C CONNECTOR PINOUTS

CONNECTOR	PIN	SIGNAL	SOURCE
J1	1	GND	ICE
J1	2	Transmitted Data	CRT
J1	3	Received Data	ICE
J1	7	GND	ICE
J2	1	GND	ICE
J2	2	Transmitted Data	ICE
J2	3	Received Data	DEVICE
J2	4	Request to Send	ICE
J2	5	Clear to Send	DEVICE
J2	6	Data Set Ready	ICE
J2	7	GND	ICE
J2	20	Data Terminal Ready	ICE
J2	24	Transmit Clock	ICE
J3	1	GND	ICE
J3	2	Transmitted Data	DEVICE
J3	3	Received Data	ICE
J3	4	Request to Send	DEVICE
J3	5	Clear to Send	ICE
J3	6	Data Set Ready	ICE
J3	7	GND	ICE
J3	17	Receive Clock	ICE
J3	20	Data Terminal Ready	DEVICE

Centronics S1 Microprinter

The following modification must be made in the printer cable to connector wiring.

1. Remove orange wire from pin 4.
2. Remove white wire from pin 20 and wire it to pin 4.
3. Remove grey wire from pin 11 and wire it to pin 20.

The printer cable can then be connected to the ICE's DCE RS232 Connector (J3).

BACKPLANE PINOUT

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	+5	31	A15	62	GND	92	~HALT
2	+5	32		63	GND	93	~INT
3	+5	33	A14	64	GND	94	~BUZOFF
4	MA0	34		65		95	D3
5	*~CAS	35	~WR	66		96	D1
6	MA6	36		67		97	D6
7	MA5	37		68		98	D4
8	MA4	38	~BUZOFF	69	~FAST	99	~RFSHCARD
9	MA3	39	D7	70	~RFSH	100	A12
10	MA2	40	D5	71		101	A13
11	MA1	41	D0	72	OSCS	102	~RD
12	0	42	D2	73	~RAMK1L	103	~MREQ
13	~IRESET	43	A9	74	~M1	104	
14	A3	44	A8	75	~GRESET	105	A5
15	A4	45	A6	76	~DBEN	106	A7
16	A2	46	TxDCRT	77		107	RxDSP
17	A1	47	~CARD3	78	~ZWAIT	108	TxDSP
18	A0	48	~CARD2	79	~NMI	109	CTSSP
19	~IRESETL	49	~CARD1	80	~GRESETL	110	RTSSP
20	ADDST	50	~CARD0	81	WP	111	DSRSP
21	A11	51	RxDCRT	82	~SEL0	112	RAMD1S
22	A10	52	~IDRQ	83	~SEL1	113	DTRSP
23	~IWEN	53	~INTR	84	~IREN	114	TxCSP
24	WS	54		85	~BUSREQ	115	+15V
25	~IORQ	55		86	~BUSACK	116	+15V
26	~BRK	56		87	IO	117	+15V
27		57	-5V	88	OSEN	118	
28		59	+5V	89	GO	120	GND
29		60	+5V	90		121	GND
30		61	+5V	91	~EXT	122	GND

*NOTE: ~ stands for inverted signal.