KPV-1180 LINE PRINTER INTERFACE

USER MANUAL

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(NOTE: An asterisk (*) indicates a registered trademark of the Digital Equipment Corporation)

netcom products, inc.

REPRESENTED BY
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DATA SHEET

LSI-11* SYSTEM BUILDING OPTIONS

KPV-1180 LINE PRINTER INTERFACE

STANDARD FEATURES

- Software Compatible with LAV-11
- Parallel Interface to Most Printers
- Switch Selectable Device and Interrupt Vector Addresses
- Low Cost

DESCRIPTION

The KPV-1180 LINE PRINTER INTERFACE is designed to provide a parallel interface between most popular Line Printers and the LSI-11 Microcomputer. The controller is compatible with RT-11 system software and DEC's line printer diagnostics. The KPV-1180 features switch selectable Device and Interrupt Vector addresses.

CONTROL AND STATUS REGISTER:

BIT 15	Read	Error (Paper Fault)
07	Read	Data Request, $\overline{\text{Error}}$ & $\overline{\text{Busy}}$
06	Read/Write	Interrupt Enable
02	Read	Off-Line
01	Read	Busy

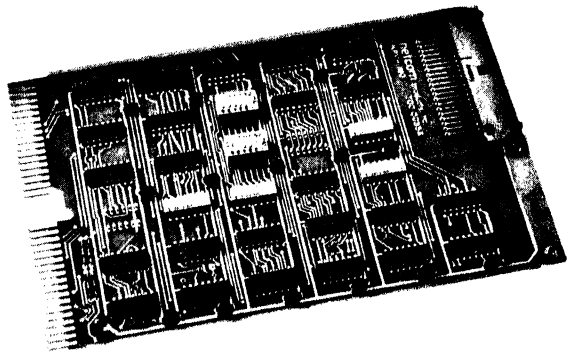
Interrupts are generated when an error or data request flag occurs and interrupt enable is set. Further interrupts are inhibited until after the interrupt condition is removed or Bit 06 is written into the CSR. A jumper is provided to set the error bit, if desired, when the printer goes off-line.

DATA BUFFER:

Bit 07 to 00	Write	Data to printer

The data buffer is write-only, but will respond to a DATI (returns zeroes) instruction. A write strobe is generated to the printer between the trailing edges of BDOUT and BSYNC. The data is presented to the printer exactly as it is programmed (no carriage return). Bit 07 may be optionally jumpered for 1, 0, odd parity, or even parity. Parity is an optional feature.

*TM - Digital Equipment Corporation



SPECIFICATIONS

Module Size: 22.8 x 13.2 cm.
8.9 x 5.2 inch

Environmental:
Temperature: 5°C - 50°C (41°F - 122°F)
Humidity: 10% to 90%, non-condensing

Power: +5 Volt ±5%, 500ma.

Options: Data Parity Logic

W-580, Line Printer Cable.
Interfaces to the LA-180 printer with 15 ft. flat cable

W-581, Line Printer Cable.
Interfaces to the LA-180 printer with 25 ft. round cable.

Ordering Information:

For further information contact:

netcom products, inc.
430 Toyama Drive
Sunnyvale, Ca. 94086
(408) 734-8732

1.0 Introduction

The Netcom Products KPV-1180 Line Printer Interface enables an LSI-11* microcomputer system to interface with an LA180 DECprinter or a Data Products-compatible line printer. An option is available which allows the KPV-1180 to be used with line printers that have a Centronic-compatible interface. If you have doubts about whether a specific line printer can be used with the KPV-1180, please contact Netcom Products.

This manual provides information that is required to use the KPV-1180. Device address and vector address switch settings, jumper settings, non-standard component selection and programming information are all provided.

2.0 Features

- Software compatible with the DEC* LAV11 Line Printer Interface. Compatible with RT-11 and other LSI-11* operating systems.

- Parallel Interface to most line printers.

- Switch selectable device and interrupt vector addresses.

- Jumper selectable signal levels (low or high).

  - ON-LINE (J1).
  - PAPER FAULT (J2).
  - Parity bit (Data bit 07) always low, always high, or data (J3).
  - DEMAND (J4).
  - BUSY (J5).
  - STROBE (J6).
  - ON-LINE (or other) signal sets the CSR Error bit (J1 and J2).

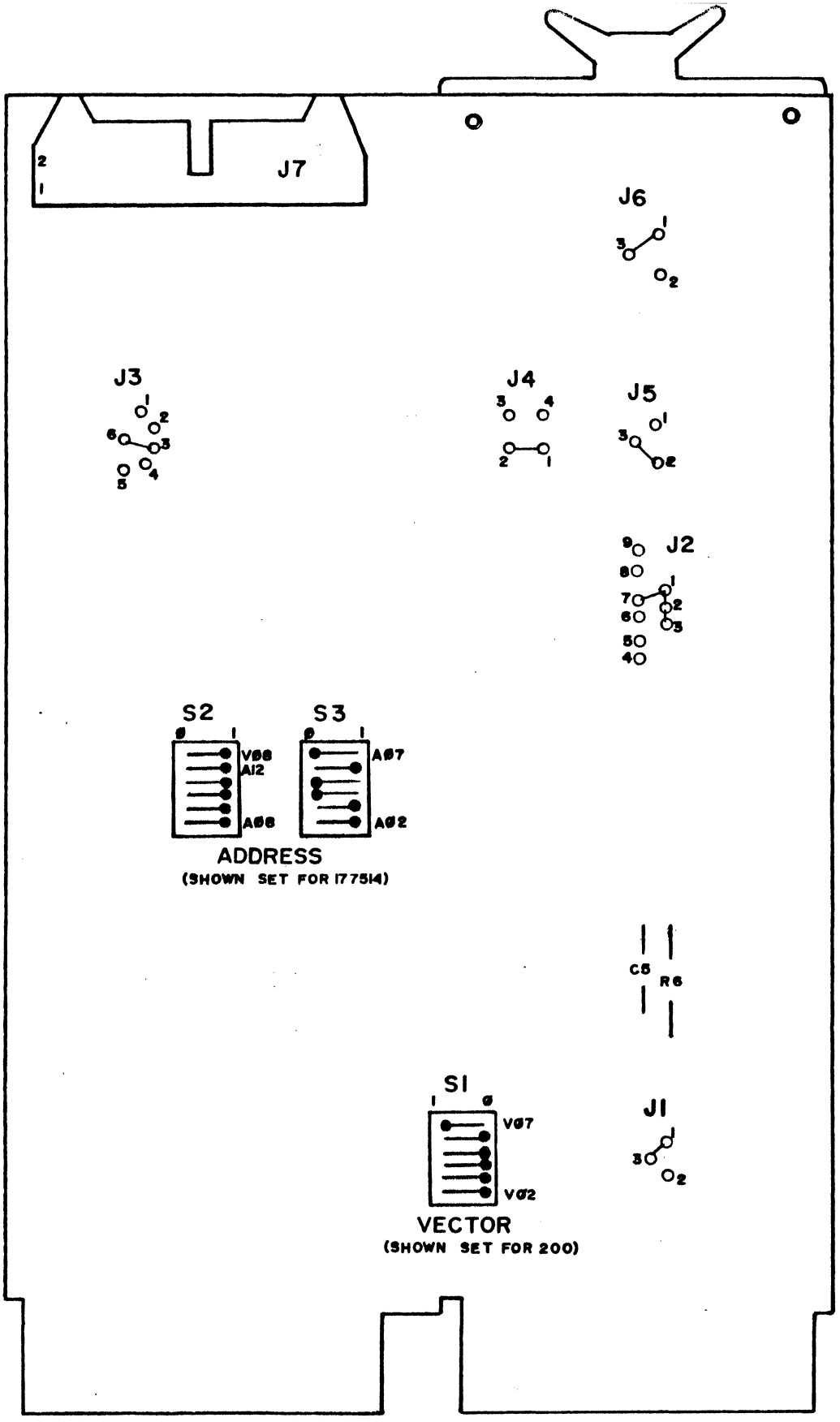


Figure 1. KPV-1180 switch and jumper locations.

3.0 Options

- Data parity logic option. Provides jumper-selectable odd or even parity on Data bit 07 via jumper J3.

- Fault option. Provides two additional signals from the line printer to the KPV-1180. The signals appear on jumper J2 and can be connected via jumper J2 to set the CSR Error bit.

- Centronics-compatible interface option.

- W-580 Line Printer Cable. A fifteen foot cable assembly for the LA180 DECprinter.

- W-581 Line Printer Cable. A twenty-five foot cable assembly for the LA180 DECprinter.

- Cables for other line printers are available. Contact Netcom for information.

4.0 Specifications

Model:	KPV-1180
Size:	Double (22.8 X 13.2 cm., 8.9 X 5.2 inch)
Power:	+5 Volts ±5%, 500 ma.

5.0 Configuration

This section describes the use of switches to set the device address and interrupt vector address, jumpers to set signal assertion levels, parity and Error bit setting, and selection of non-standard components C5 and R6.

5.1 Address Settings

As shipped from Netcom Products, the KPV-1180 is adjusted for the standard DEC* line printer device Control/Status Register (CSR) address 177514_8 and interrupt vector address of 200_8. If additional KPV-1180 modules are used in a system, they must be adjusted to use unique device and vector addresses. These addresses are set with switches S1, S2, and S3 as described below. Note: Switch settings may be altered thru handling or during shipping. User should check switch settings before installing KPV-1180 in system.

5.1.1 Device Address

Switches S2 and S3 are used to set the device address. The address on the switches is the address of the Control/Status Register (CSR). The Data Buffer Register (DBR) is located two bytes (one word) from the start of the CSR. If the CSR is located at the standard address of 177514_8, then the DBR is located at 177516_8. The first KPV-1180 module in a system should be set for the standard device address. Modules after the first should be adjusted for addresses in the floating address space.

Figure 2., below, shows the relationship between switch S2 and S3 settings and the device address.

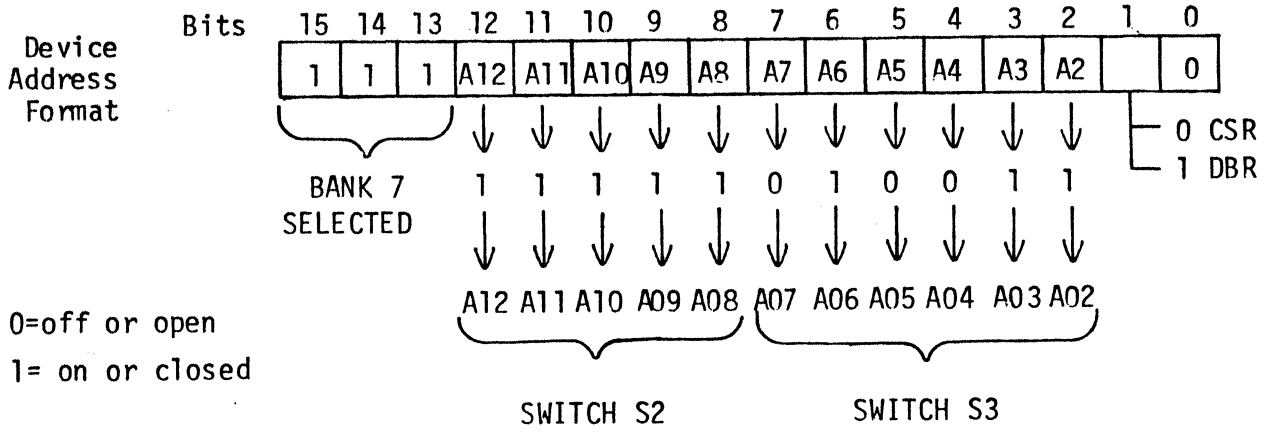


Figure 2. KPV-1180 Device Address Format (Shown set for 177514_8 as shipped for Netcom.)

5.1.2 Interrupt Vector Address

The KPV-1180, as shipped from the factory, is set for the DEC* standard Line printer interrupt vector address of 200_8. The first KPV-1180 in a system should be set for the standard interrupt vector address. If additional KPV-1180 modules are used in a system, each must be set for a unique vector address that is located in floating vector space.

Figure 3., below, shows the relationship between switches S1 and S2 and the interrupt vector address.

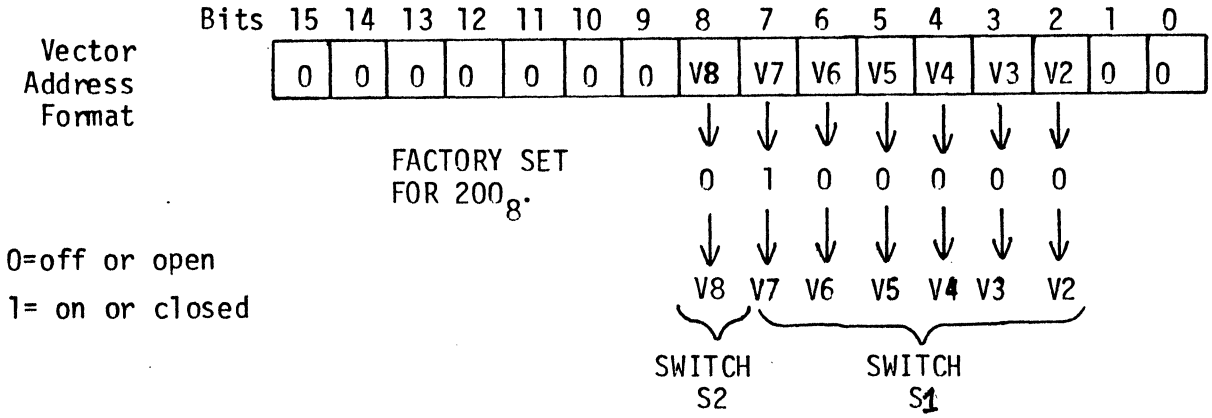


Figure 3. KPV-1180 Interrupt Vector Format.

5.2 Jumper Settings

Six jumpers, J1 through J6, are provided so that the KPV-1180 can be adjusted for different input and output signal assertion levels, parity bit (Data 07) handling and CSR Error bit setting. For example, jumper J1 allows the KPV-1180 to handle an ON-LINE signal from a printer that is asserted either low, J1(2-3), or high, J1(1-3). Jumper J3 controls parity bit (Data 07) handling. Jumper J2 allows the KPV-1180 to respond to printers that set the PAPER FAULT signal either low or high when a paper fault or other hardware error is detected. In addition, J2 allows signals other than PAPER FAULT to set the error bit in the Control/Status Register (CSR). Setting the CSR Error bit also initiates an interrupt sequence, if software has set the Interrupt Enable bit in the CSR.

The following table, Table 1., lists each jumper and the signal affected by that jumper. Table 2., shows the setting of each jumper as shipped from the factory with or without Centronics-compatible interface option. Finally, some additional information is given about the use of jumper J2 to allow input signals other then PAPER FAULT to set the Error bit in the CSR.

In addition to handling the assertion level of the PAPER FAULT signal, jumper J2 allows up to two other input (printer to KPV-1180) signals to set the Error bit in the CSR. As shipped from the factory, J2 pins 1, 2, and 3 are connected together. To have another input signal set the CSR Error bit, disconnect one of J2 pins 1, 2, or 3, leaving the other two pins connected, and connect that pin to the desired signal at one of the other jumpers.

5.3 Selection of Non-standard Components C5 and R6

For some printers it is necessary to increase the length of time that data is presented to the KPV-1180 and the printer. For this purpose, provision has been made for the insertion of an RC network, C5 and R6, that delays the BRPLY L signal. The BRPLY L signal terminates the transfer of output data from the LSI-11* to the KPV-1180, so delaying BRPLY L increases the time that data is presented to the KPV-1180 and line printer.

The LA180 DECprinter does not require the C5-R6 network and a jumper trace is provided on the board instead of R6. If a KPV-1180 is ordered with a Centronics-compatible interface, values of 330 pfd for C5 and 150 ohms for R6 are supplied. This provides around 50 NS delay in the BRPLY L signal.

(continued)

Table 1. Jumper Signals

Jumper	Signal	Meaning if installed	Signal Direction
J1 (2-3)	ON-LINE	asserted low	Printer to KPV-1180
J1 (1-3)	ON-LINE	asserted high	"
J2 (7-1-2-3)	PAPER FAULT	asserted low	Printer to KPV-1180
J2 (6-1-2-3)	PAPER FAULT	asserted high	"
J3 (5-6)	PARITY (DATA 07)	low	KPV-1180 to printer
J3 (4-6)	PARITY (DATA 07)	high	"
J3 (3-6)	NO PARITY	data on DATA 07	"
J3 (2-6)[1]	PARITY (DATA 07)	odd parity	"
J3 (1-6)[1]	PARITY (DATA 07)	even parity	"
J4 (1-3)	DEMAND	asserted low	Printer to KPV-1180
J4 (1-2)	DEMAND	asserted high	"
J4 (1-4)	C REQ L	Centronics connection	"
J5 (2-3)	BUSY	asserted low	Printer to KPV-1180
J5 (1-3)	BUSY	asserted high	"
J6 (1-3)	STROBE	asserted low	KPV-1180 to printer
J6 (2-3)	STROBE	asserted high	"

[1] PARITY OPTION must be installed to use these connections.

Table 2. Factory Jumper Settings[1]

Jumper	Setting as shipped from factory: For DEC* LA180 and Data Products printers[2]	With Centronics Option[3]	Meaning if installed:
J1 (2-3)	R	R	ON-LINE is asserted low.
J1 (1-3)	I	I	ON-LINE is asserted high.
J2 (7-1-2-3)	I	R	PAPER FAULT is asserted low.
J2 (6-1-2-3)	R	I	PAPER FAULT is asserted high.
J3 (5-6)	R	R	PARITY (DATA 07) bit is low.
J3 (4-6)	R	R	PARITY (DATA 07) bit is high.
J3 (3-6)	I	I	NO PARITY (DATA 07 is Data bit).
J3 (2-6)	R	R	Requires PARITY OPTION. Odd parity is transmitted on DATA 07 bit.
J3 (1-6)	R	R	Requires PARITY OPTION. Even parity is transmitted on DATA 07 bit.
J4 (1-3)	R	R	DEMAND is asserted low.
J4 (1-2)	I	R	DEMAND is asserted high.
J4 (1-4)	R	I	Centronics connection.
J5 (2-3)	I	R	BUSY is asserted low.
J5 (1-3)	R	I	BUSY is asserted high.
J6 (1-3)	I	I	STROBE is asserted low.
J6 (2-3)	R	R	STROBE is asserted high.

I=installed; R=removed. Removal of jumpers may require cutting traces on the PC board.

[2] For any line printer with a Data Products-compatible interface.

[3] For any line printer with a Centronics-compatible interface.

For some printers it may be necessary to experiment with the values of C5 and R6. If your printer prints garbage, it may be an indication that data isn't being presented to the printer long enough to latch into the printer's buffers. Installing C5-R6 or increasing their values may solve the problem.

6.0 Programming the KPV-1180

The KPV-1180 is programmed by means of the two device registers: the Control/ Status Register (CSR) and the Data Buffer Register (DBR). If the Interrupt Enable bit in the CSR is set, the interrupt vector address is used.

The CSR is located at the address set on switches S2, and S3. For use with RT-11 and other DEC* software, the CSR of the line printer interface is located at 177514_8. The CSR is a two byte (one word) register that has bits that indicate printer status (Error, Data Request, etc.) and the Interrupt Enable bit. A complete listing of CSR bits and their meanings is given in the following section, section 6.1.

The DBR is a two byte (one word) register that is located two bytes from the start of the CSR. With the CSR at 177514_8, the DBR is located at 177516_8. The most significant byte (bits 15-08) of the DBR is not used. Each character to be output to the line printer is placed in the low-order byte (bits 07-00) of the DBR. Bit 07 in the DBR can be used as a Parity bit, depending on the specific printer and jumper settings of the KPV-1180. DBR bit definitions are shown in section 6.2.

If interrupt processing is not used (Interrupt Enable bit in the CSR not set by software), software outputs data to the line printer by: 1) Checking the CSR Data Request bit (bit 7). If the bit is set, the printer is ready for the next character. 2) placing the character to be output in the low-order byte of the DBR. The KPV-1180 does not transmit any line-feed or other form-control characters to the printer. The user's program should check for error conditions, by checking the CSR Error bit, and perform appropriate functions to avoid loss of data.

If interrupt processing is used, the user's software should put the address of the line printer interrupt routine and the interrupt routine Processor Status Word (PSW) starting at the interrupt vector location set by switches S1 and S2, before setting the Interrupt Enable bit in the CSR. For use with DEC* software, the line printer interrupt vector is set at 200_8. Thus the address of the interrupt routine must be placed at 200_8 before setting the CSR Interrupt Enable bit. The PSW for the interrupt routine is generally 200_8 for LSI-11* systems. This PSW inhibits interrupts during execution of the printer interrupt routine.

Once the interrupt vector and PSW are set up, the user's program is ready to begin outputting data to the line printer. This is done by setting the CSR Interrupt Enable bit. An immediate interrupt to the user's line printer interrupt routine will occur. After checking the CSR for errors and making sure that the printer is ON-LINE, the interrupt routine can output a character to the printer by placing the character in the low-order byte of the DBR. At this point, the interrupt routine can issue a return from interrupt command and the user's main-line program can execute. When the printer is ready to accept another character, the user's main-line program will be interrupted and the above sequence repeated until all characters have been printed. The line printer interrupt routine will execute anytime the printer is ready to accept another character or an error (CSR bit 15 set) occurs. Because the interrupt routine will be executed when the printer is ready for another character or when an error occurs, the user's interrupt routine must check for and handle error conditions before trying to output a character. Since the error bit is read only, it can be reset only by correcting the error condition.

6.1 Control/Status Register (CSR)

The bit assignments of the CSR are as follows:

Table 3. KPV-1180 CSR Bit Assignments

Bit	Name	Description
15	Error	The Error bit is asserted high (to 1) when an error such as PAPER FAULT occurs. It can be jumpered so that ON-LINE signal sets this bit. This bit is read-only and can be reset only by correction of the error condition.
14-08	Unused	
07	Data Request	When asserted high, indicates that the printer is ready to accept another character. This bit is mutually exclusive with the Error bit. Data Request will never be set if an error condition exists and the CSR Error bit is set. Data Request is read only.
06	Interrupt Enable	This bit may be set or cleared under program control. It is cleared by the INIT signal on the LSI-11* bus. (INIT signal can be caused by the reset instruction, INIT console switch, power-up or power-down sequence). When the IE bit is set, an interrupt occurs if either Error or Data Request is set.
05-02	Unused	
01	ON-LINE	This read only bit is set when the printer is ON-LINE.
00	BUSY	The busy bit is set when the printer is performing a print or paper advance operation.

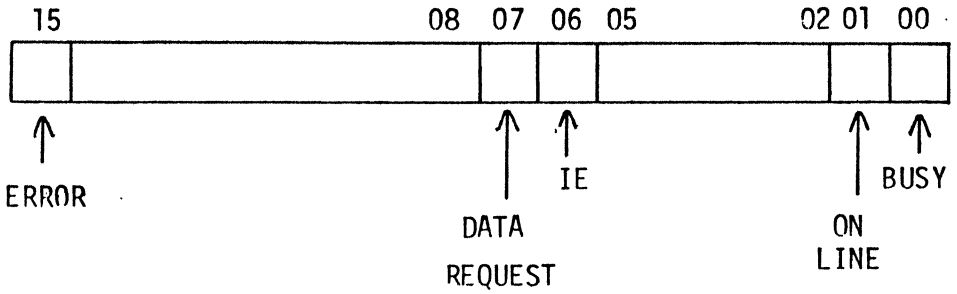


Figure 4. KPV-1180 CSR Bit Assignments

6.2 Data Buffer Register (DBR)

The bit assignments of the DBR are as follows:

Table 4. Data Buffer Register (DBR)

Bit	Name	Description
15-08	Unused	
07	Parity	A write-only bit that depends upon KPV-1180 jumper settings. Can be low, high, data, odd parity or even parity generated by the KPV-1180.
06-00	Data	Seven bit data character. Bit 06 is the most significant. This seven-bit character will be transferred to the line printer. All these bits are write-only.

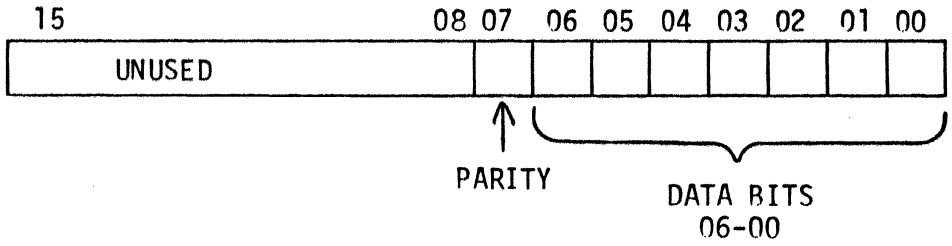


Figure 5. KPV-1180 DBR Bit Assignments.

Jumper Settings*

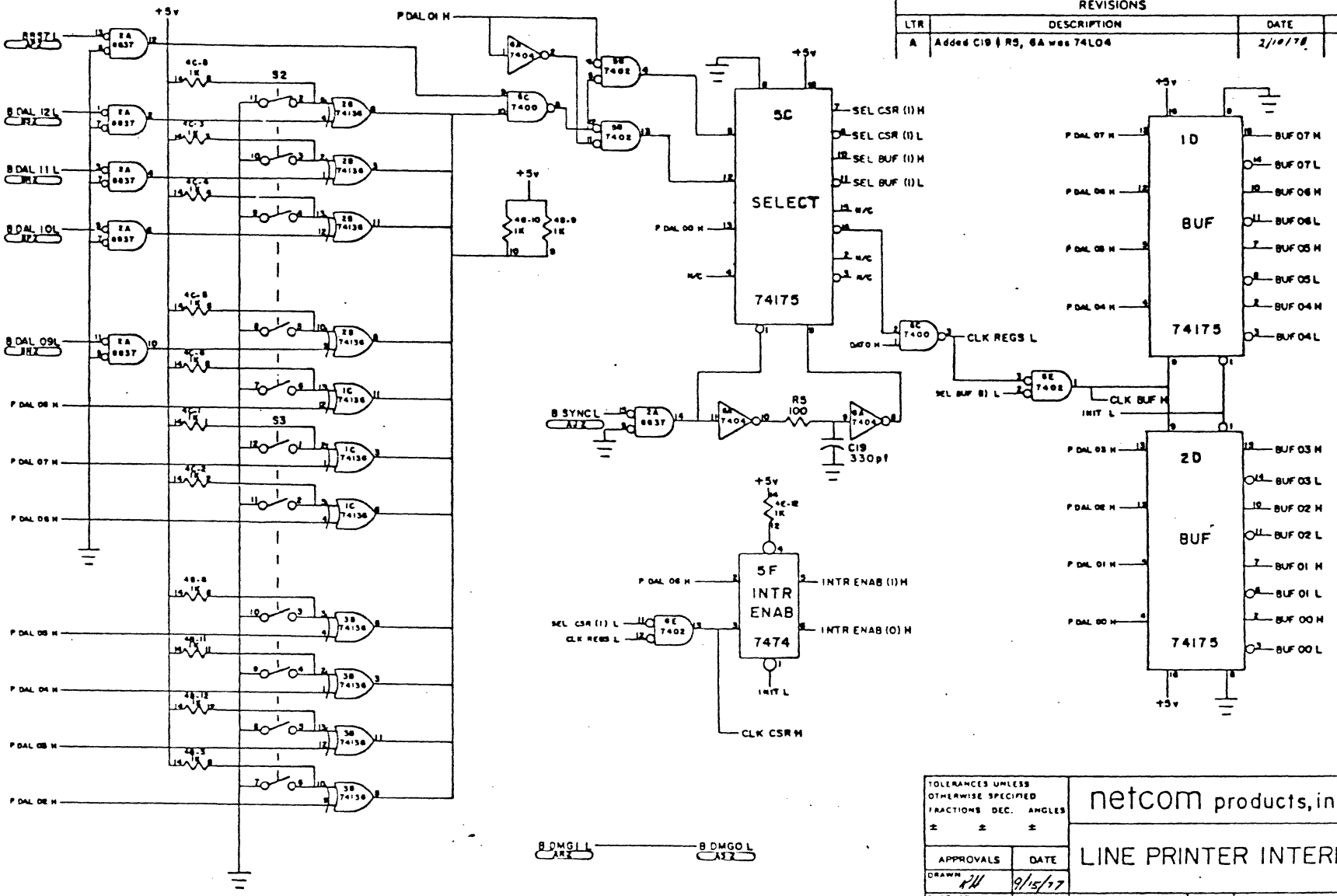
Jumper	Setting as shipped from factory: Without Centronics Option	With Centronics Option	Meaning if installed:
J1 (2-3)	R	R	ON-LINE is asserted low.
J1 (1-3)	I	I	ON-LINE is asserted high.
J2 (7-1-2-3)	I	R	PAPER FAULT is asserted low.
J2 (6-1-2-3)	R	I	PAPER FAULT is asserted high.
J3 (5-6)	R	R	PARITY (DATA 07) bit is low.
J3 (4-6)	R	R	PARITY (DATA 07) bit is high.
J3 (3-6)	I	I	NO PARITY (DATA 07 is Data bit).
J3 (2-6)	R	R	Requires PARITY OPTION. Odd parity is transmitted on Data 07 bit.
J3 (1-6)	R	R	Requires PARITY OPTION. Even parity is transmitted on Data 07 bit.
J4 (1-3)	R	R	DEMAND is asserted low.
J4 (1-2)	I	R	DEMAND is asserted high.
J4 (1-4)	R	I	Centronics connection.
J5 (2-3)	I	R	BUSY is asserted low.
J5 (1-3)	R	I	BUSY is asserted high.
J6 (1-3)	I	I	STROBE is asserted low.
J6 (2-3)	R	R	STROBE is asserted high.

*I=installed: R=removed. Standard board (without Centronics option column) jumpers are installed by means of traces printed on the board, with the exception of J4 (1-2). Removal of a jumper requires that a trace be cut. Remaining Jumpers are hard wired and are shown for information only

Centronics Option: In addition to above jumper connections for the centronics option: 1) cut trace on board for R6. 2) Install R6 = 150 ohms. 3) Install CS = 330 pfd.

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES			
APPROVALS	DATE	netcom products, Inc.	
DRAWN TR	7/20/79		
CHECKED		LINE PRINTER INTERFACE	
		SCALE —	SIZE B
DO NOT SCALE DRAWING		DRAWING NO AD KPV-1180	SHEET 2 of 2



REVISIONS			
LTR	DESCRIPTION	DATE	APPROV
A	Added C19 & R5, 6A was 74L04	2/10/78	R/K

TOLERANCES UNLESS OTHERWISE SPECIFIED		
FRACTIONS	DEC.	ANGLES
±	±	±

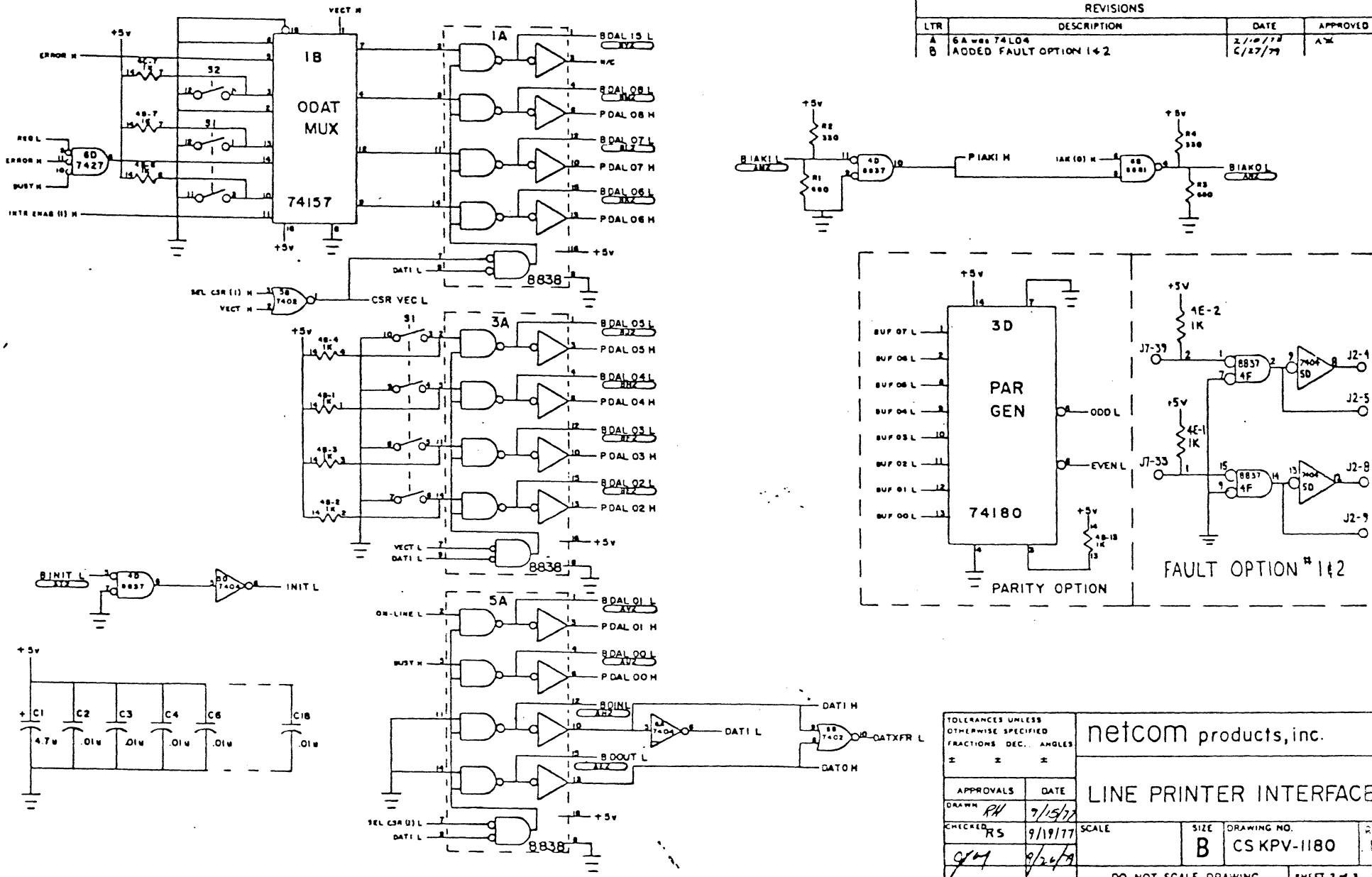
APPROVALS	DATE
DRAWN RH	9/15/77
CHECKED RS	9/19/77
	9/19/77

netcom products, inc.

LINE PRINTER INTERFAC

SCALE	SIZE	DRAWING NO.
	B	CS KPV-1180

DO NOT SCALE DRAWING — SHEET 1


REVISIONS
LTR | DESCRIPTION | DATE | APPROVED
A | 6A was 74L04 | 2/10/78 | AW
B | ADDED FAULT OPTION 1&2 | 6/27/79
1A
1B
ODAT MUX
74157
8838
3A
3D
PAR GEN
74180
PARITY OPTION
FAULT OPTION # 1&2
5A
BDAL 15 L
BDAL 08 L
PDAL 08 H
BDAL 07 L
PDAL 07 H
BDAL 06 L
PDAL 06 H
BDAL 05 L
PDAL 05 H
BDAL 04 L
PDAL 04 H
BDAL 03 L
PDAL 03 H
BDAL 02 L
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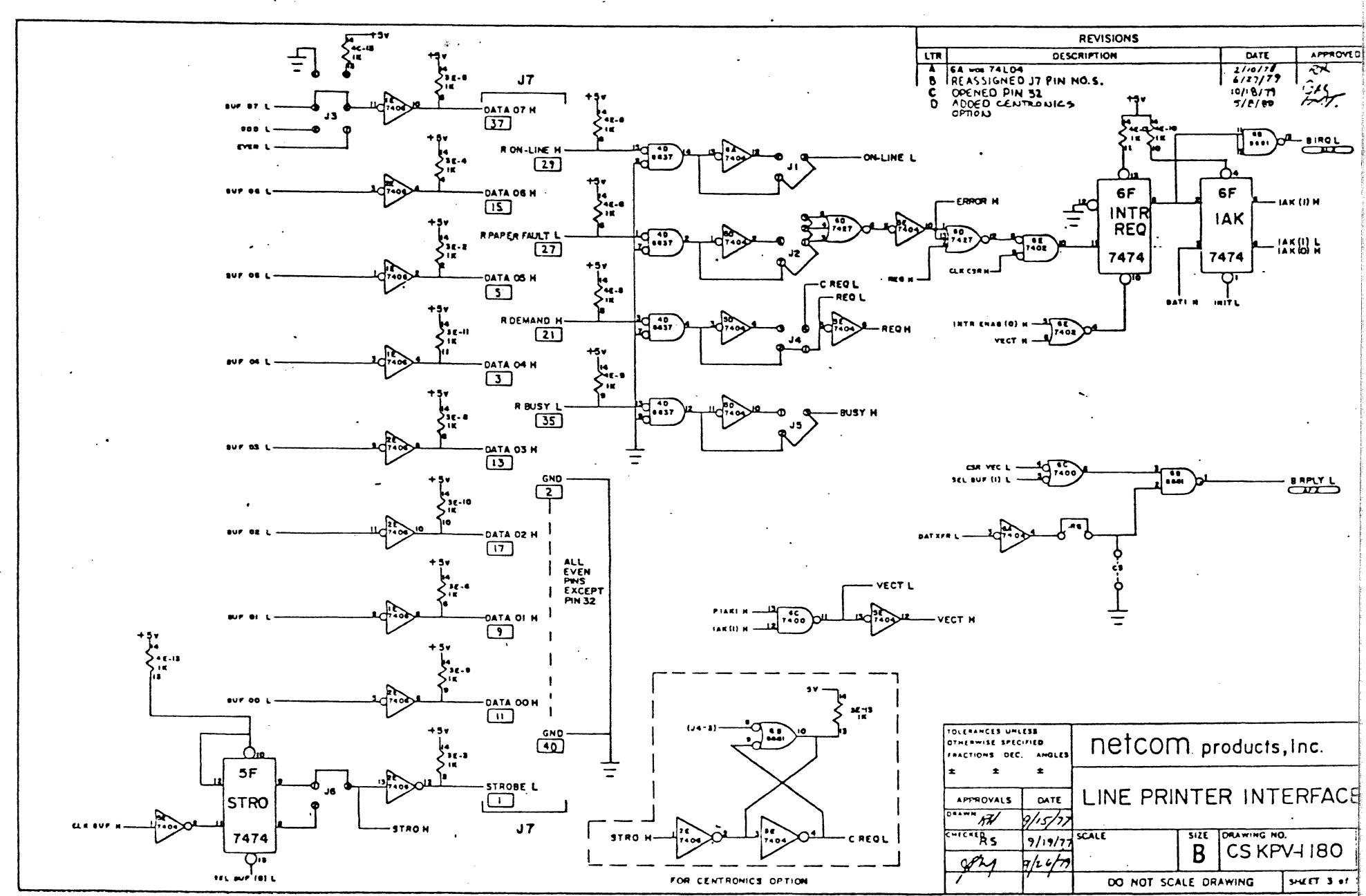
BDAL 01 L
PDAL 01 H
BDAL 00 L
PDAL 00 H
CSR VEC L
INIT L
DATI L
DATO H
DATXFR L
ODD L
EVEN L
BIAKI L
PIAKI H
BIAKO L
TOLERANCES UNLESS OTHERWISE SPECIFIED
FRACTIONS DEC. ANGLES
APPROVALS | DATE
DRAWN RH 9/15/77
CHECKED RS 9/19/77
9/26/79
netcom products, inc.
LINE PRINTER INTERFACE
SCALE
SIZE B
DRAWING NO. CS KPV-1180
DO NOT SCALE DRAWING
SHEET 2 of 3


REVISIONS
LTR DESCRIPTION DATE APPROVED
A 6A was 74L04 2/10/78
B REASSIGNED J7 PIN NO.S. 6/27/79
C OPENED PIN 32 10/18/79
D ADDED CENTRONICS OPTION 5/2/80
J7
DATA 07 H 37
DATA 06 H 15
DATA 05 H 5
DATA 04 H 3
DATA 03 H 13
DATA 02 H 17
DATA 01 H 9
DATA 00 H 11
STROBE L 1
GND 2
GND 40
ALL EVEN PINS EXCEPT PIN 32
R ON-LINE H 29
R PAPER FAULT L 27
R DEMAND H 21
R BUSY L 35
ON-LINE L
BUSY H
REQ H
C REQ L
REQ L
ERROR H
INTR ENAB (0) H
VECT H
VECT L
6F INTR REQ 7474
6F IAK 7474
IAK (1) H
IAK (1) L
IAK (0) H
BIRQ L
BRPLY L
CSR VEC L
SEL BUF (1) L
DAT XFR L
PIAK1 H
IAK (1) H
STRO H
C REQ L
CLK BUF H
SEL BUF (0) L
FOR CENTRONICS OPTION
TOLERANCES UNLESS OTHERWISE SPECIFIED
FRACTIONS DEC. ANGLES
APPROVALS DATE
DRAWN 9/15/77
CHECKED RS 9/19/77
9/26/79
netcom products, Inc.
LINE PRINTER INTERFACE
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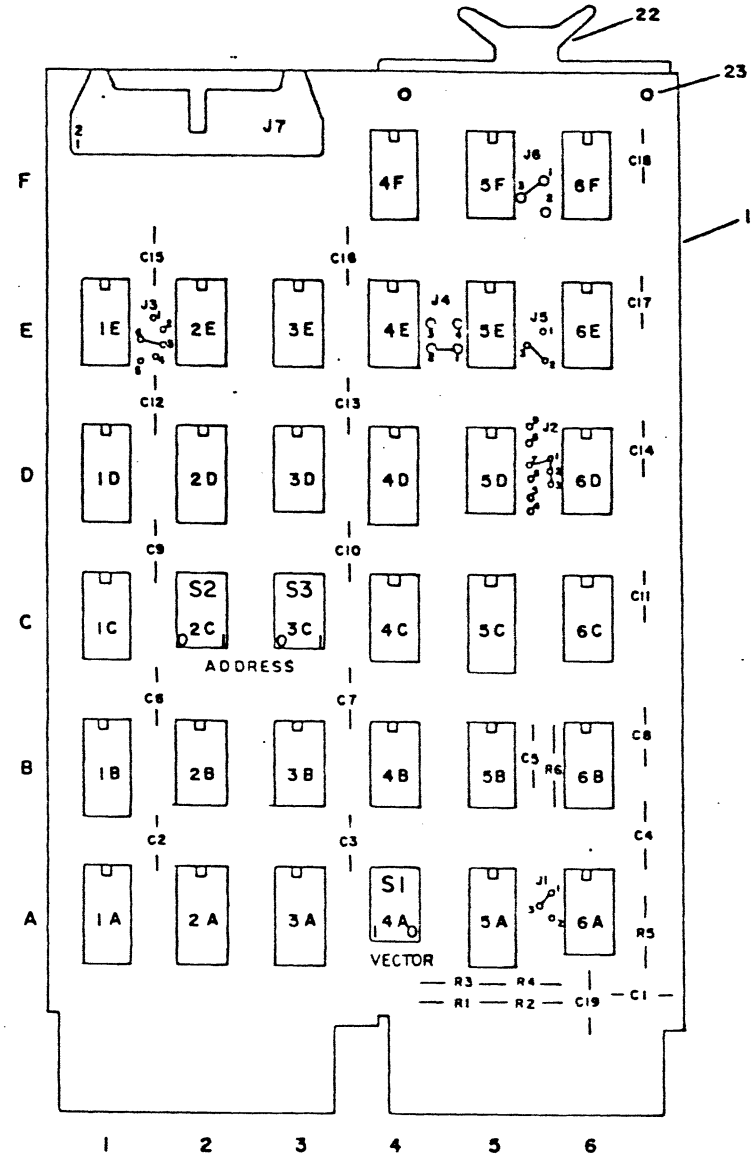
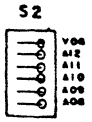
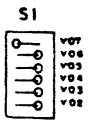
SIZE B
DRAWING NO. CS KPV-I 180
DO NOT SCALE DRAWING
SHEET 3 of





0-A-1

SWITCHES SHOWN SET FOR DEVICE ADDRESS 177514.



1-V-0

SWITCH SHOWN SET FOR VECTOR ADDRESS 200.

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
A	Added C19 | R5, 6A was 74L04	2/10/78	KH
B	ADDED PIN ASSIGNMENTS TO J7	6/27/79	
C	OMITTED PIN 32	10/8/79	
D	ADDED COLUMN FOR CENTRONICS OPTION	2/26/80	KH
E	DELETED J4(1-2) JUMPER FROM PARTS LIST.	5/1/80	D.T.
F	REMOVED 4F FROM FLOW STANDARD, 6 SWITCH POS "OFF" ON S2	5/28/80	D.T.

NOTES:

1. "I" QUANITY COLUMN IS FOR CENTRONICS OPTION.
2. WITH CENTRONICS OPTION INSTALL ITEMS 29(IC 4F), 25, AND 5.
   WITHOUT CENTRONICS OPTION REMOVE ITEMS 29(IC 4F), 25, AND 5.

QTY.	I	REF. DESIGNATION	DESCRIPTION	PART NO.
1	—	4F	I.C. 8837/8T37	MIS-8837-01
1	1	R5	RES. 100 ohm, 5%, 1/4 w	130-1015-00
1	1	C19	CAP. 330 pfd, 50v	104-3310-50
REF	REF	30 OPTIONAL	I.C. 74180	101-4180-00
1	—	R6	RES 150Ω, 5%, 1/4 w	130-1515-00
1	1	J7	CONNECTOR, 40 pin, 90° PCB	121-0012-04
2	2		RIVET	127-0004-22
1	1		HANDLE	127-0001-19
3	3	2C, 3C, 4A	SW-PAC, 8 pole DIP	124-0001-04
4	4	3E, 4B, 4C, 4E	RES-PAC 1K ohm DIP	132-10EE-14
2	2	R1, R3	RES 680 ohm, 5%, 1/4 w	130-6815-00
2	2	R2, R4	RES 330 ohm, 5%, 1/4 w	130-3315-00
1	1	6B	I.C. 8881	MIS-8881-00
3	3	1A, 3A, 5A	I.C. 8838/MSI2APC	MIS-8838-01
2	2	2A, 4D	I.C. 8837/8T37	MIS-8837-01
3	3	5C, 1D, 2D	I.C. 74175	TTL-4175-01
1	1	1B	I.C. 74197	TTL-4197-01
3	3	2B, 3B, 1C	I.C. 74136	TTL-4136-00
2	2	3F, 6F	I.C. 7474	TTL-7474-00
1	1	6D	I.C. 7427	TTL-7427-00
2	2	1E, 2E	I.C. 7406	TTL-7406-00
3	3	3D, 5E, 6A	I.C. 7404	TTL-7404-00
2	2	3B, 5E	I.C. 7402	TTL-7402-00
1	1	6C	I.C. 7400	TTL-7400-00
1	—	C5	CAP 330pf, 83v	100-331M-33
16	16	C2-C4, C6-C18	CAP .01mfd, 50v	100-1031-50
1	1	C1	CAP .47mfd, 35v	103-4731-35
REF	REF		SCHEMATIC	CSKPV-1180
1	1		PC BOARD	C0700-0035

TOLERANCES UNLESS OTHERWISE SPECIFIED
FRACTIONS ± DEC. ± ANGLES ±

APPROVALS	DATE
DRAWN AH	9/15/77
CHECKED RS	9/19/77
187	9/24/79

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