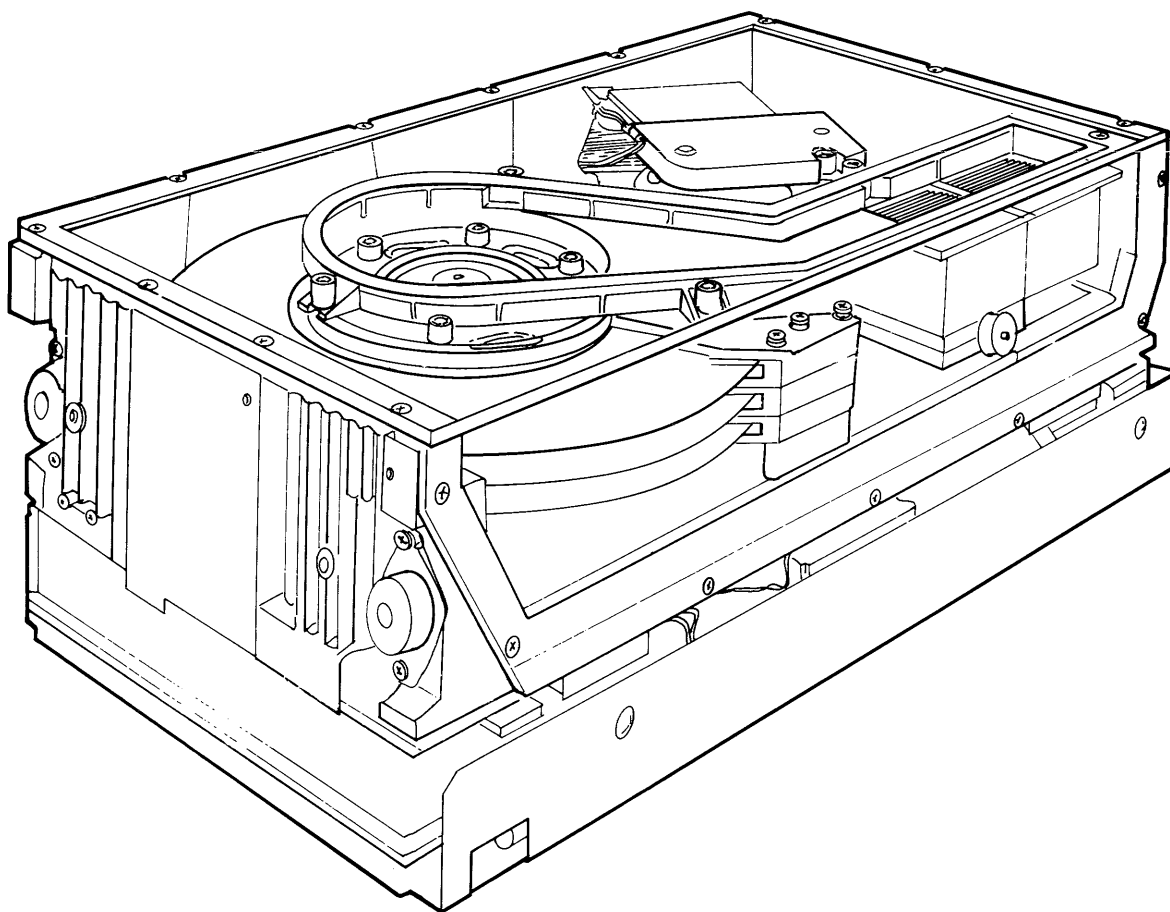


D2246 8-INCH WINCHESTER DISK DRIVE MAINTENANCE GUIDE



NEC
NEC Information Systems, Inc.

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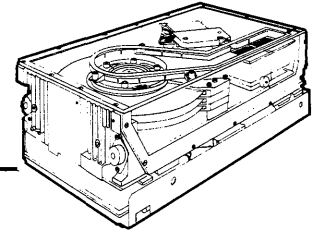
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Abbreviations

A	Ampere
ac	alternating current
AM	Address Mark
AWG	American Wire Gauge
CA	Cylinder Address
CRC	Cyclic Redundancy Check
dc	direct current
DE	Disk Enclosure
DIP	Dual-inline-packaged
DKC	Disk Controller
DKU	Disk Unit
ECC	Error Correction Code
EOR	End of Record
GND	Ground
HA	Head Address
HEX	Hexadecimal
IGB	Inner Guard Band
I/O	Input/Output
LED	Light emitting diode
m	meter
MB	Megabyte
MFM	Modified Frequency Modulation
MHz	Megahertz
mm	Millimeter
ms	Millisecond
mV	Millivolt
MTBF	Mean Time Between Failures
MTTR	Mean Time to Repair
NRZ	Non-Return-to-Zero
ns	Nanosecond
OGB	Outer Guard Band
PCB	Printed Circuit Board
PLO	Phase Locked Oscillator
RMS	Root-Mean-Square
ROM	Read only memory
RPM	Revolutions per Minute
R/W	Read/Write
SA	Sector Address
TTL	Transistor/Transistor Logic
V	Volt
μ s	microsecond

Chapter 1

System Overview



The D2246 is a new addition to the NEC D2200 series of disk drives. It is a compact, highly reliable, low-cost unit and is fully compatible with earlier D2200 models. It offers 85 megabytes (MB) of unformatted data storage on four 8-inch platters. Actual storage capacity depends upon the formatting method used.

1.1 D2246 SYSTEM DESIGN

The D2246 uses fixed-disk, Winchester-type technology, which provides the most advanced method of storing and retrieving large amounts of data. Each D2246 disk drive contains four 8-inch platters sealed within a protective, air-tight enclosure. This enclosure protects the recording platters from atmospheric dust and dirt to improve operational reliability. A spindle, a drive motor, a rotary actuator assembly, and movable read/write heads are also contained within the enclosure. Figure 1-1 shows the major components of the D2246.

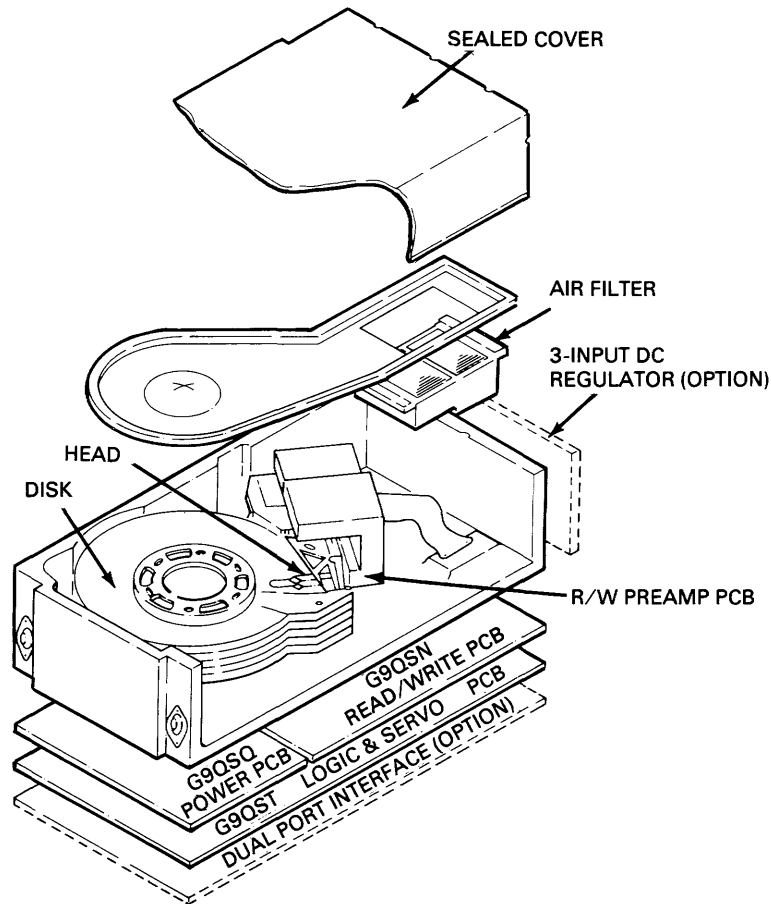


Figure 1-1 D2246 Major Components

Figure 1-2 shows the arrangement of recording platters and read/write heads within the D2246.

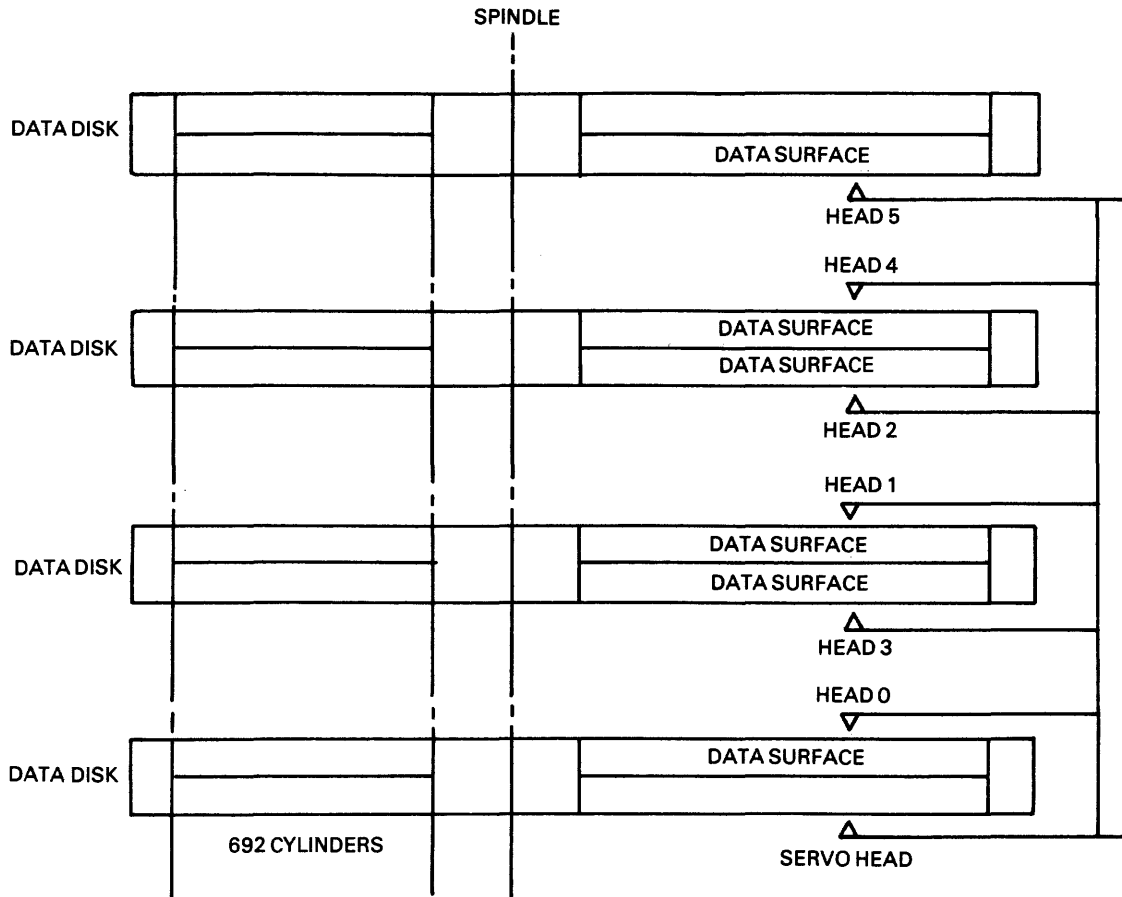


Figure 1-2 D2246 Disk and Read/Write Head Arrangement

The servo disk surface is shown in Figure 1-3.

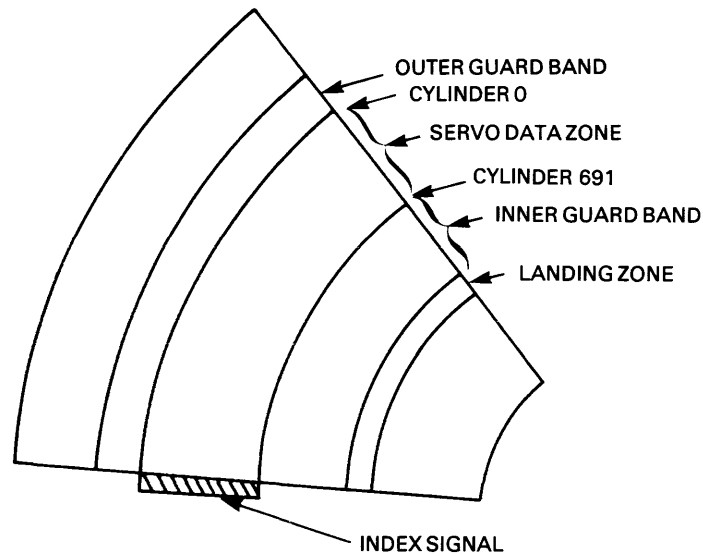


Figure 1-3 D2246 Servo Disk Surface

The Index signal is a six-bit pattern written along one radius of the servo surface. It identifies the beginning of a recording track. The index pattern repeats each time the radius intersects one of the recording tracks.

The servo data zone contains 692 concentric recording tracks. Each recording track contains prerecorded positioning data, including clock and synchronization signals, that provide information to place and maintain the read/write heads on track.

The inner and outer guard bands bracket the servo data zone. They contain recurring six-bit patterns to distinguish them from the servo data zone.

The landing zone is a silicon-coated surface where the read/write heads rest when the recording disks are not spinning. During read, write, and seek operations the heads “float” approximately 20 microinches above the surface of the disk.

1.2 DISK CIRCUITRY

A block diagram of a D2246 disk drive is shown in Figure 1-4. The functional components are the interface, the read/write circuits, the servo control, and the motor control circuits.

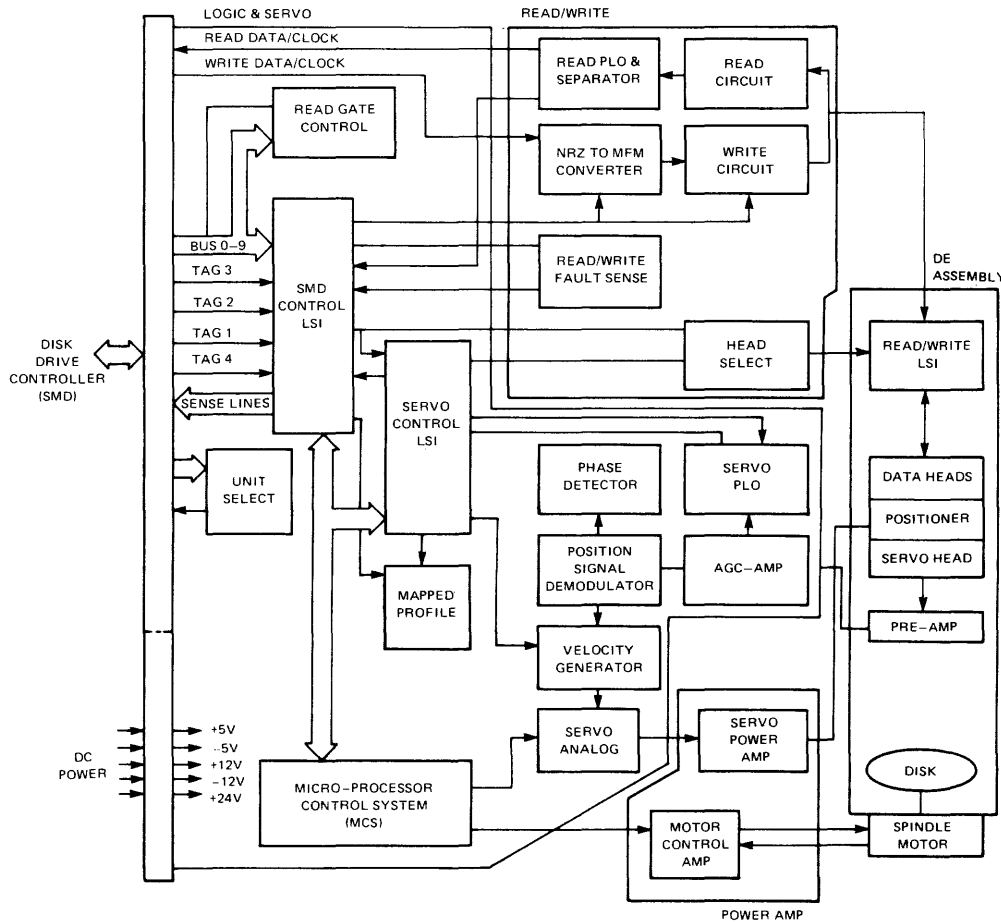


Figure 1-4 D2246 Functional Block Diagram

The interface circuits route data, addresses, status information, and control signals between the disk drive and the controller.

The read/write circuits control the transfer of data from the disk (read operation), and to the disk (write operation). During a write operation, the circuits receive serial nonreturn-to-zero (NRZ) format data from the controller and convert the data to a modified frequency modulation (MFM) format. The MFM data is then written on the disk. During a read operation, the circuits read and amplify the data from the disk, convert it from MFM to NRZ format, and send the NRZ data serially to the controller.

The servo control reads the data prerecorded on the servo disk. The servo control uses this data to position and maintain the read/write heads on the correct cylinder. The motor control circuits drive the spindle motor.

1.3 POWER REQUIREMENTS

D2246 disk drives operate on externally supplied dc power. DC power requirements are listed in Table 1-1.

Table 1-1 DC Power Requirements

REQUIRED VOLTAGE	TOLERANCE	DAMAGE THRESHOLD	CURRENT	RIPPLE (PEAK TO PEAK)
+5.0 V	±0.25 V	±10%	4.0 A	100 mV
-5.0 V	±0.25 V	±10%	0.5 A	100 mV
+12.0 V	±0.60 V	±10%	0.6 A	100 mV
-12.0 V	±0.60 V	±10%	0.5 A	100 mV
+24.0 V	±2.40 V	±10%	2.5 A* 5.0 A**	240 mV

*2.5 A — average running current

**5.0 A — peak starting current (25 seconds maximum duration)

All power line voltages must be established within 500 milliseconds (ms) of power on. Voltages must be enabled in the following order: +5 V, -5 V, ±12 V, +24 V. When power is turned off, lines must be disabled in the reverse order: +24 V, ±12 V, -5 V, +5 V.

1.4 FEATURES

Shorter access times, high-speed data transfers, and mechanical reliability are required for efficient computer network operations. To meet these demands the D2246 disk drive offers the following features.

1.4.1 Enhanced Seek Time

Seek time is the time required to find requested data on the disk. The D2246 has an average seek time of 25 milliseconds (ms), and a maximum of 50 ms.

1.4.2 Rapid Data Transfer Rate

The D2246 provides a data transfer rate of approximately 1.2 MB per second.

1.4.3 Compact Mounting

The compact size of the D2246 allows for either horizontal or vertical mounting in a limited space. The drive's lock mechanism is easily accessible even after the drive has been placed within a system cabinet.

The D2246 also features an integrated cooling fan that reduces space and power requirements.

1.4.4 Simplified Maintenance

The air-tight, sealed disk/head assembly and the D2246's simplified design produce a disk drive that requires no periodic maintenance. Neither installation nor field service requires special tools. Motor electronics are placed outside the head/disk assembly and do not need "clean room" repair facilities.

An optional diagnostic panel is available for test and maintenance purposes (see Appendix C).

1.4.5 Design Reliability

Lightweight, contact-type start/stop heads that reduce damage to the heads and disks are used within the D2246 disk drive. A simplified rotary actuator, a directly coupled, brushless dc motor, and a closed-loop air circulation system are the drive's major mechanical components. The control logic is microprocessor controlled and designed to minimize electronic components. This design strategy ensures high reliability and low cost.

1.4.6 Standard Interfaces

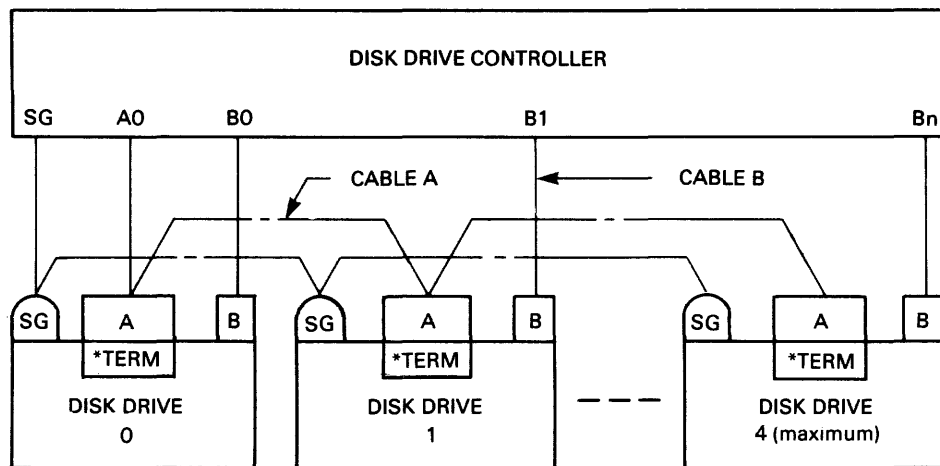
The D2246 uses standard original equipment manufacturer interfaces for connection to a disk controller and to a power supply.

1.4.7 Safety

The D2246 conforms to Underwriter's Laboratories Safety Regulation UL478.

1.4.8 System Configuration Flexibility

A maximum of four D2246 disk drives can be connected to a single controller in either a daisy-chain or radial system (see Figures 1-5 and 1-6).



* TERMINATING RESISTORS INSTALLED ON EACH DRIVE

Figure 1-5 Daisy-Chain System Configuration

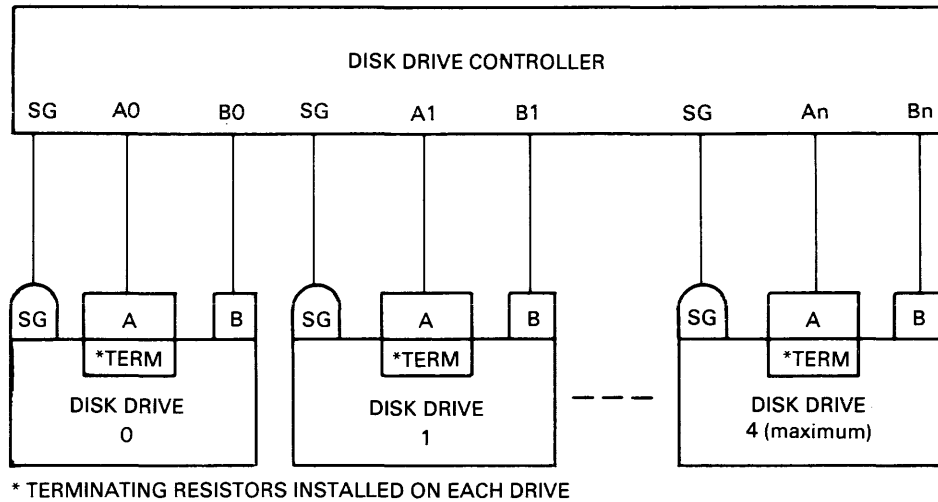


Figure 1-6 Radial System Configuration

1.5 RELATED DOCUMENT

For additional information on the D2246 disk drive, refer to the *D2246 8-Inch Winchester Disk Drive Product Description* (NEC document 819-000080-4001).

1.6 SPECIFICATIONS

Product specifications are listed in Appendix B.

1.7 OPTIONS

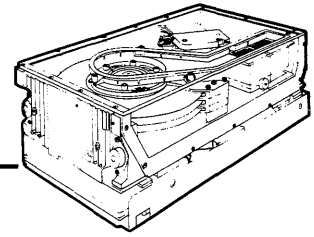
Table 1-2 lists available options for the D2246 disk drive.

Table 1-2 Available Options

OPTION	DESCRIPTION
3-Input DC Regulator Option	Supplies internal dc "power set" (+24 V, +12 V, +5 V, -5 V, -12 V) from external dc input of +24 V, +5 V, and -12 V.
Dual-Port Option	Enables disk drive interface with two controllers.
DC Power Supply	Supplies internal dc "power set" from ac input power. Provides power for two disk drives.
Diagnostic Panel	Tests and monitors disk drive operation.

Chapter 2

Installation Procedures



This chapter provides procedures for installing a D2246 disk drive. When preparing the installation site, refer to the environmental specifications listed in Appendix B.

2.1 UNPACKING/REPACKING

Before unpacking the disk drive, examine the shipping carton for damage. If damage has occurred, notify the carrier immediately. Do not open the carton until the carrier's representative is present.

If there is no damage to the shipping carton, use these procedures to unpack the disk drive. Failure to follow these procedures can void the product warranty.

1. Open the top of the shipping carton.
2. Remove the top packing brace (see Figure 2-1).
3. Carefully remove the disk drive from the shipping carton.
4. Remove the D2246 from the plastic shipping bag.
5. Save all packing material for reshipping.
6. Check all items against the bill of material to insure that no items are missing.
7. Check all items for shipping damage.

To repack the disk drive, reverse these procedures.

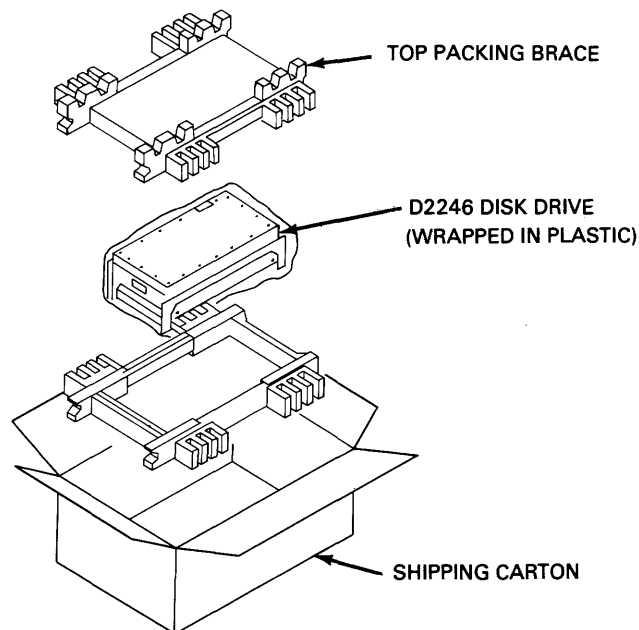


Figure 2-1 D2246 Packaging

2.2 TERMINATING RESISTORS

Terminating resistors are installed on the G9QST logic and servo printed circuit board (PCB) as shown in Figure 2-2.

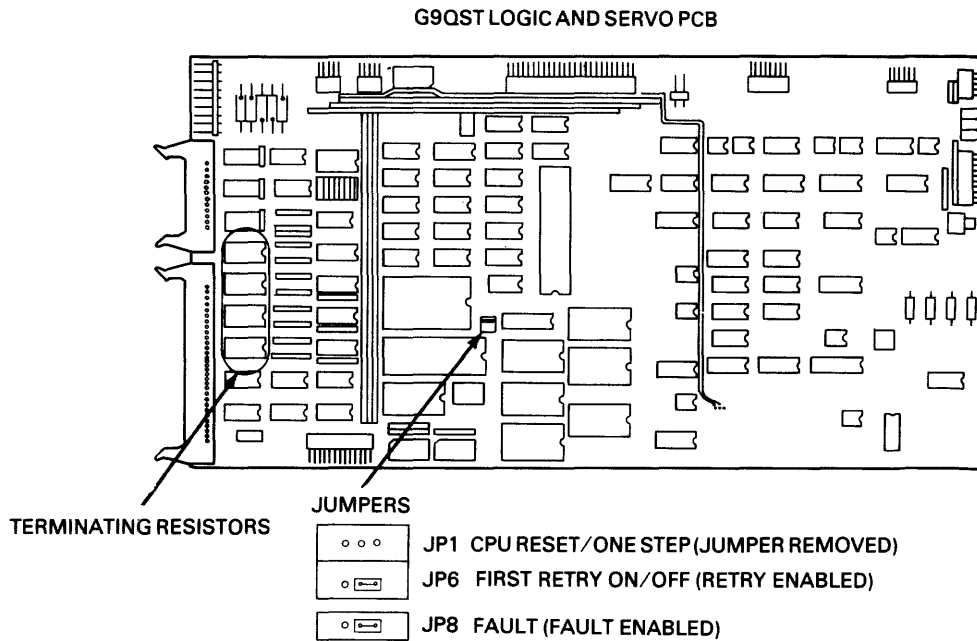


Figure 2-2 G9QST Terminating Resistor and Jumper Locations

If the D2246 drive is connected to the controller in a radial configuration, install a set of four terminating resistors in place as shown in Figure 2-3. Terminating resistors can be either 150Ω or 56 Ω.

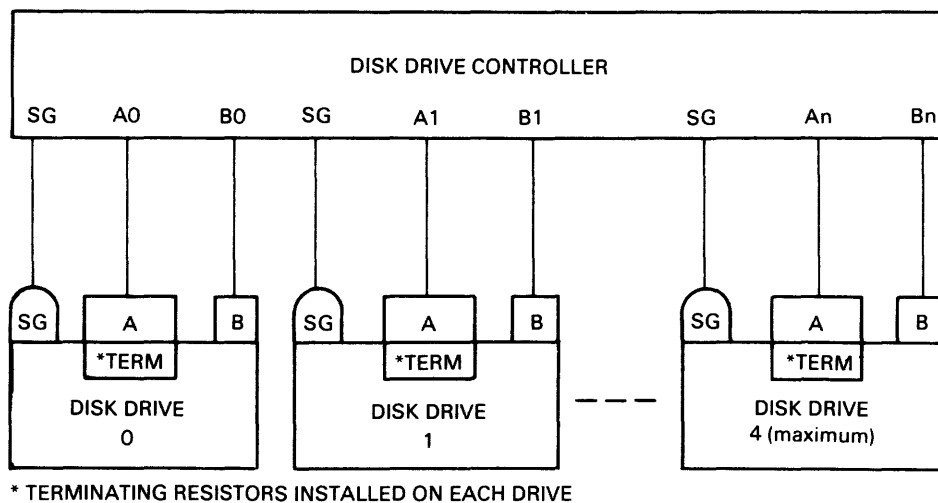


Figure 2-3 Terminating Resistors in Radial System

In a daisy-chain configuration, two types of termination methods can be used. To terminate individual drives, install a set of four 150Ω resistors in each drive as shown in Figure 2-4.

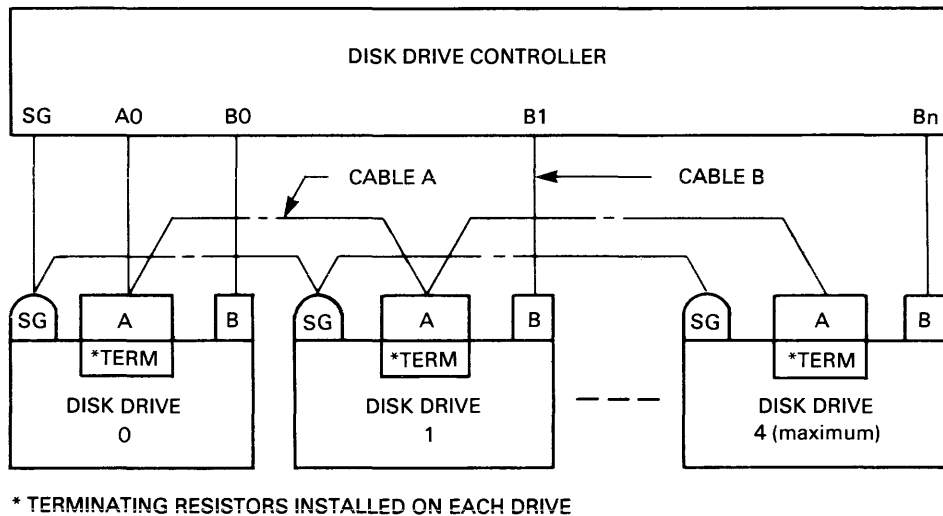


Figure 2-4 Individual Drive Termination/Daisy-Chain System

To terminate the last drive, install a set of four 56Ω resistors in the final drive of the chain as shown in Figure 2-5.

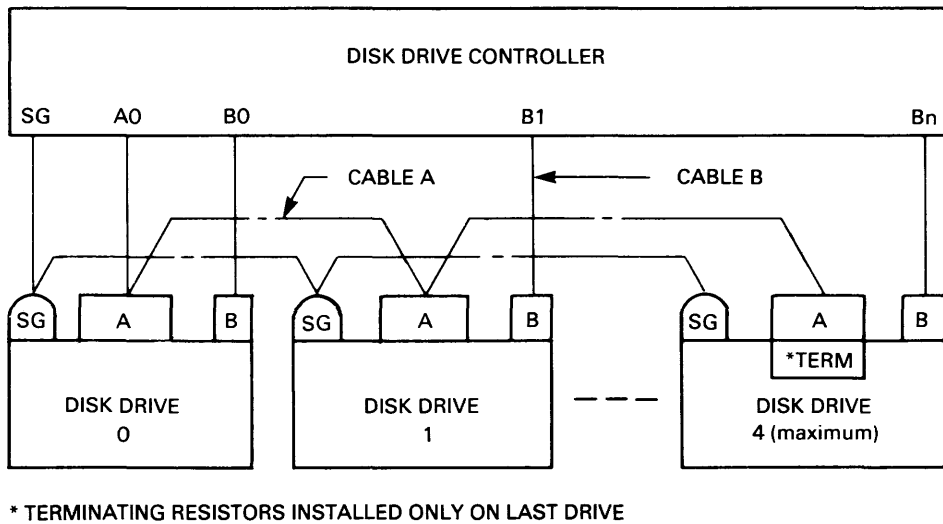


Figure 2-5 Last Drive Termination/Daisy-Chain System

2.3 JUMPER REQUIREMENTS

Three jumper settings must be verified before power is applied to the disk drive. The location of these three jumpers (JP1, JP6, and JP8) on the G9QST PCB is shown in Figure 2-2. Insure that settings match those shown in Figure 2-2.

CAUTION

Do not alter these jumper settings. They are intended for factory adjustments only.

2.4 SWITCH SETTINGS

Three eight-segment, dual-inline-packaged (DIP) switch assemblies on the G9QST logic and servo PCB configure the D2246 to communicate with the controller and set the sector count. DIP switch assembly locations are shown in Figure 2-6.

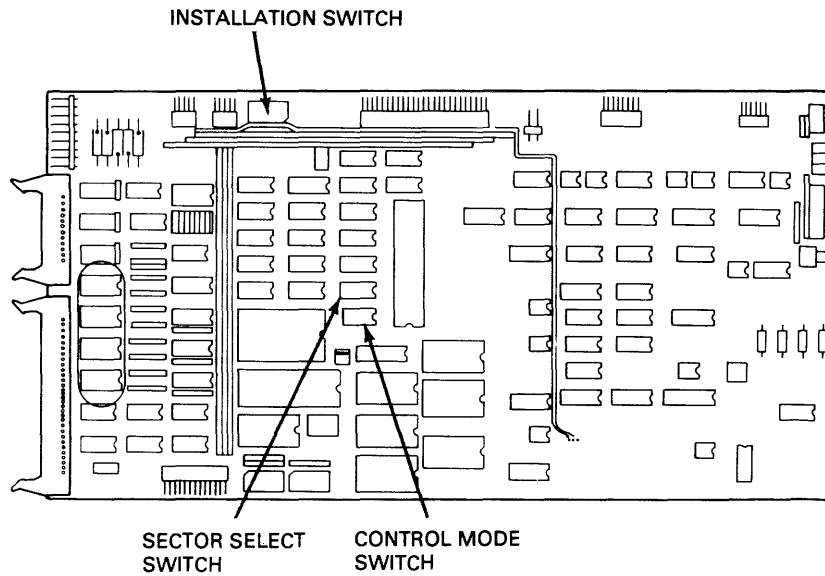


Figure 2-6 DIP Switch Assembly Locations

2.4.1 Installation Switch Assembly

The installation switch assembly, shown in Figure 2-7, sets the device address and controls the power-on sequence. Segments 1, 2 and 5 are set to 0.

Segments 3 and 4 assign the device address, a hexadecimal number from 0 to 3.

Segment 6 enables a 30-second delay in the start-up time of the spindle motor. This segment can be used in dual-drive systems to insure that both drives do not overload the power supply by simultaneously activating their power-up sequence.

Segment 7 is set to correspond to the mounting position of the drive.

Segment 8 places the D2246 in local or remote mode at power-on.

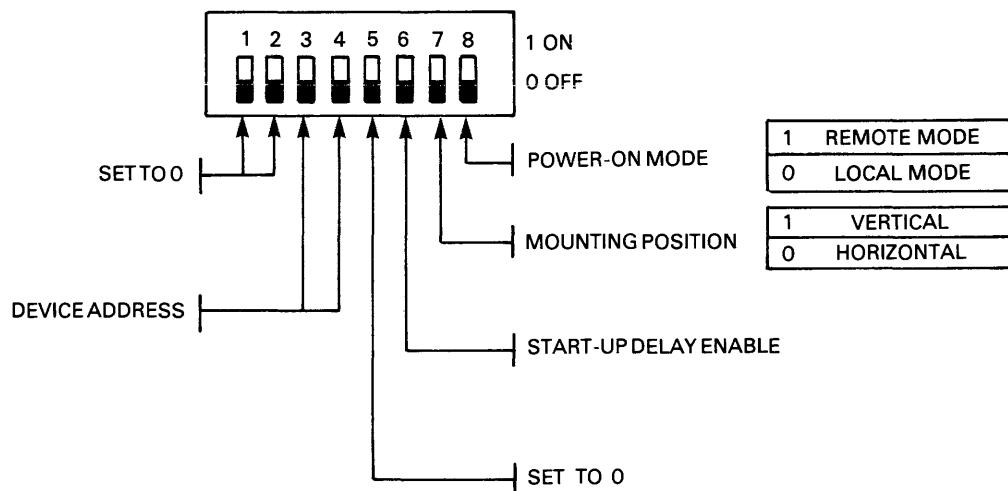


Figure 2-7 Installation DIP Switch

2.4.2 Control Mode Switch Assembly

The control mode switch assembly (shown in Figure 2-8) configures the D2246 to communicate with the disk controller and enables certain optional drive features.

Segment 1 is set to 1.

Segments 2 and 3 are set to 0.

Segment 4 enables the Address Mark function.

Segment 5 enables the Read Sector function. When segments 5 and 7 of the control mode switch assembly are set to 1, Tag 4 can be used with bus bits 8 and 9 to request the current sector address. The D2246 issues the current sector address across the sense lines.

Segment 6 enables the Format Write Release Option used with some controllers.

Segment 7 enables the Tag 4 line.

Segment 8 enables the controller interface.

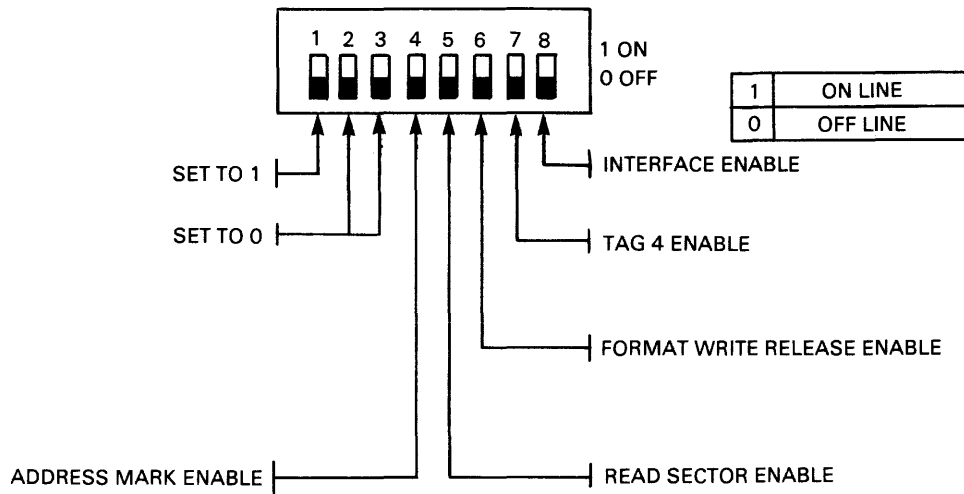


Figure 2-8 Control Mode DIP Switch

2.4.3 Sector Select Switch Assembly

The sector select switch assembly (see Figure 2-9) sets the number of sectors per track. Any number of sectors up to 128 can be selected.

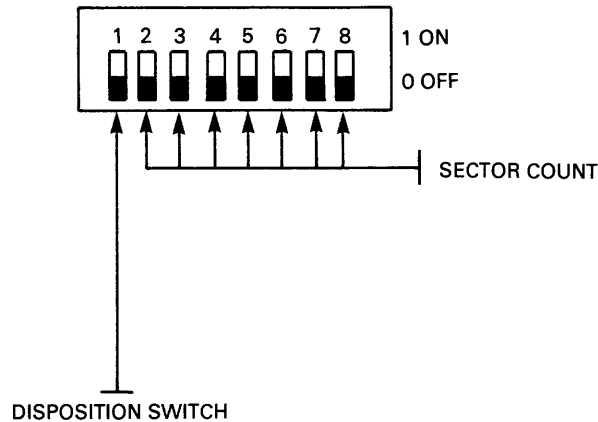


Figure 2-9 Sector Select Switch

Segment 1 of this assembly determines the disposition of odd or remainder bytes. These are extra bytes that must be allocated when the available bytes per track are not evenly divisible by the number of sectors per track. With segment 1 in the 0 position, odd bytes are grouped together in an extra sector at the end of the track. With this segment in the 1 position, the last sector is reduced to account for odd bytes.

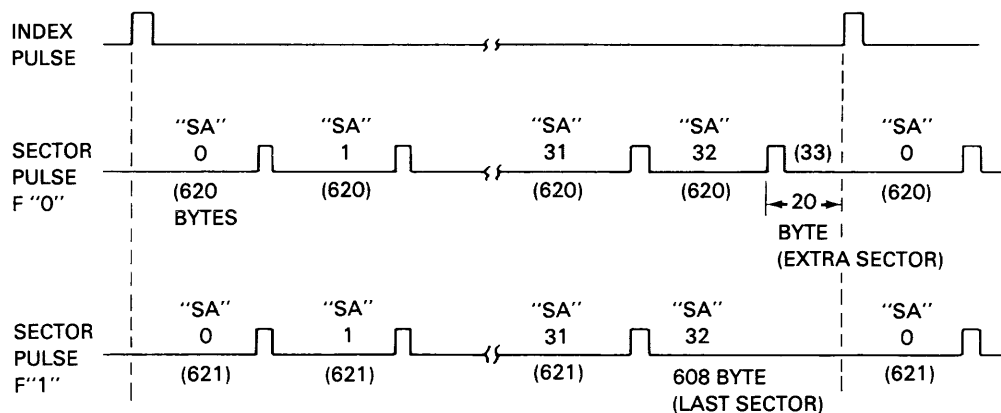


Figure 2-10 Sector Allocation

Figure 2-10 illustrates the allocation of 33 sectors with segment 1 of the sector select switch assembly in both the 0 and 1 positions.

Tables 2-1 and 2-2 list sector select switch settings and resulting sector allocations for the D2246 disk drive.

**Table 2-1 Sector Select Switch Settings
(Segment 1 = 0)**

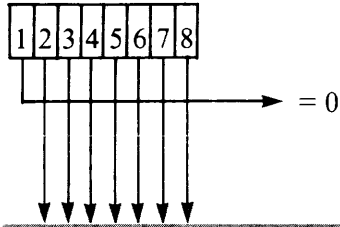
SECTOR SWITCH SETTING

1	2	3	4	5	6	7	8
---	---	---	---	---	---	---	---

				TRACK = 20,480 BYTES		
$2^6 2^5 2^4 2^3 2^2 2^1 2^0$	SECTORS PER TRACK	BYTES PER SECTOR	EXTRA SECTOR BYTES			
0000001	1	20480	0			
0000010	2	10240	0			
0000011	3	6826	2			
0000100	4	5120	0			
0000101	5	4096	0			
0000110	6	3413	2			
0000111	7	2925	5			
0001000	8	2560	0			
0001001	9	2275	5			
0001010	10	2048	0			
0001011	11	1861	9			
0001100	12	1706	8			
0001101	13	1575	5			
0001110	14	1462	12			
0001111	15	1365	5			
0010000	16	1280	0			
0010001	17	1204	12			
0010010	18	1137	14			
0010011	19	1077	17			
0010100	20	1024	0			
0010101	21	975	5			
0010110	22	930	20			
0010111	23	890	10			
0011000	24	853	8			
0011001	25	819	5			
0011010	26	787	18			
0011011	27	758	14			
0011100	28	731	12			
0011101	29	706	6			
0011110	30	682	20			

Table 2-1 Sector Select Switch Settings (cont'd)
(Segment 1 = 0)

SECTOR SWITCH SETTING



		TRACK = 20,480 BYTES	
$2^6 2^5 2^4 2^3 2^2 2^1 2^0$	SECTORS PER TRACK	BYTES PER SECTOR	EXTRA SECTOR BYTES
0 0 1 1 1 1 1	31	660	20
0 1 0 0 0 0 0	32	640	0
0 1 0 0 0 0 1	33	620	20
0 1 0 0 0 1 0	34	602	12
0 1 0 0 0 1 1	35	585	5
0 1 0 0 1 0 0	36	568	32
0 1 0 0 1 0 1	37	553	19
0 1 0 0 1 1 0	38	538	36
0 1 0 0 1 1 1	39	525	5
0 1 0 1 0 0 0	40	512	0
0 1 0 1 0 0 1	41	499	21
0 1 0 1 0 1 0	42	487	26
0 1 0 1 0 1 1	43	476	12
0 1 0 1 1 0 0	44	465	20
0 1 0 1 1 0 1	45	455	5
0 1 0 1 1 1 0	46	445	10
0 1 0 1 1 1 1	47	435	35
0 1 1 0 0 0 0	48	426	32
0 1 1 0 0 0 1	49	417	47
0 1 1 0 0 1 0	50	409	30
0 1 1 0 0 1 1	51	401	29
0 1 1 0 1 0 0	52	393	44
0 1 1 0 1 0 1	53	386	22
0 1 1 0 1 1 0	54	379	14
0 1 1 0 1 1 1	55	372	20
0 1 1 1 0 0 0	56	365	40
0 1 1 1 0 0 1	57	359	17
0 1 1 1 0 1 0	58	353	6
0 1 1 1 0 1 1	59	347	7
0 1 1 1 1 0 0	60	341	20

Table 2-1 Sector Select Switch Settings (cont'd)
(Segment 1 = 0)

SECTOR SWITCH SETTING

		TRACK = 20,480 BYTES	
$2^6 2^5 2^4 2^3 2^2 2^1 2^0$	SECTORS PER TRACK	BYTES PER SECTOR	EXTRA SECTOR BYTES
0 1 1 1 1 0 1	61	335	45
0 1 1 1 1 1 0	62	330	20
0 1 1 1 1 1 1	63	325	5
1 0 0 0 0 0 0	64	320	0
1 0 0 0 0 0 1	65	315	5
1 0 0 0 0 1 0	66	310	20
1 0 0 0 0 1 1	67	305	45
1 0 0 0 1 0 0	68	301	12
1 0 0 0 1 0 1	69	296	56
1 0 0 0 1 1 0	70	292	40
1 0 0 0 1 1 1	71	288	32
1 0 0 1 0 0 0	72	284	32
1 0 0 1 0 0 1	73	280	40
1 0 0 1 0 1 0	74	276	56
1 0 0 1 0 1 1	75	273	5
1 0 0 1 1 0 0	76	269	36
1 0 0 1 1 0 1	77	265	75
1 0 0 1 1 1 0	78	262	44
1 0 0 1 1 1 1	79	259	19
1 0 1 0 0 0 0	80	256	0
1 0 1 0 0 0 1	81	252	68
1 0 1 0 0 1 0	82	249	62
1 0 1 0 0 1 1	83	246	62
1 0 1 0 1 0 0	84	243	68
1 0 1 0 1 0 1	85	240	80
1 0 1 0 1 1 0	86	238	12
1 0 1 0 1 1 1	87	235	35
1 0 1 1 0 0 0	88	232	64
1 0 1 1 0 0 1	89	230	10
1 0 1 1 0 1 0	90	227	50

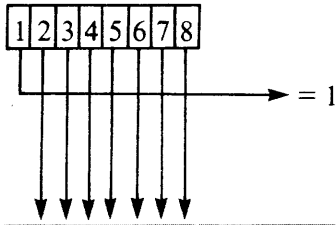
Table 2-1 Sector Select Switch Settings (cont'd)
(Segment 1 = 0)

SECTOR SWITCH SETTING

$2^6 2^5 2^4 2^3 2^2 2^1 2^0$	SECTORS PER TRACK	BYTES PER SECTOR	EXTRA SECTOR BYTES
1 0 1 1 0 1 1	91	225	5
1 0 1 1 1 0 0	92	222	56
1 0 1 1 1 0 1	93	220	20
1 0 1 1 1 1 0	94	217	82
1 0 1 1 1 1 1	95	215	55
1 1 0 0 0 0 0	96	213	32
1 1 0 0 0 0 1	97	211	13
1 1 0 0 0 1 0	98	208	96
1 1 0 0 0 1 1	99	206	86
1 1 0 0 1 0 0	100	204	80
1 1 0 0 1 0 1	101	202	78
1 1 0 0 1 1 0	102	200	80
1 1 0 0 1 1 1	103	198	86
1 1 0 1 0 0 0	104	196	96
1 1 0 1 0 0 1	105	195	5
1 1 0 1 0 1 0	106	193	22
1 1 0 1 0 1 1	107	191	43
1 1 0 1 1 0 0	108	189	68
1 1 0 1 1 0 1	109	187	97
1 1 0 1 1 1 0	110	186	20
1 1 0 1 1 1 1	111	184	56
1 1 1 0 0 0 0	112	182	96
1 1 1 0 0 0 1	113	181	27
1 1 1 0 0 1 0	114	179	74
1 1 1 0 0 1 1	115	179	10
1 1 1 0 1 0 0	116	176	64
1 1 1 0 1 0 1	117	175	5
1 1 1 0 1 1 0	118	173	66
1 1 1 0 1 1 1	119	172	12
1 1 1 1 0 0 0	120	170	80
1 1 1 1 0 0 1	121	169	31
1 1 1 1 0 1 0	122	167	106
1 1 1 1 0 1 1	123	166	62
1 1 1 1 1 0 0	124	165	20
1 1 1 1 1 0 1	125	163	105
1 1 1 1 1 1 0	126	162	68
1 1 1 1 1 1 1	127	161	33
0 0 0 0 0 0 0	128	160	0

**Table 2-2 Sector Select Switch Settings
(Segment 1 = 1)**

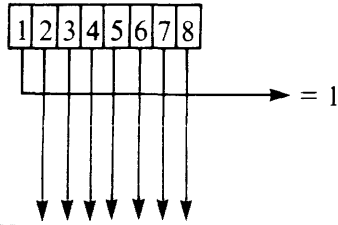
SECTOR SWITCH SETTING



		TRACK = 20,480 BYTES	
$2^6 2^5 2^4 2^3 2^2 2^1 2^0$	SECTORS PER TRACK	BYTES PER SECTOR	LAST SECTOR SHORTER
0 0 0 0 0 0 1	1	20480	0
0 0 0 0 0 1 0	2	10240	0
0 0 0 0 0 1 1	3	6827	-1
0 0 0 0 1 0 0	4	5120	0
0 0 0 0 1 0 1	5	4096	0
0 0 0 0 1 1 0	6	3414	-4
0 0 0 0 1 1 1	7	2926	-2
0 0 0 1 0 0 0	8	2560	0
0 0 0 1 0 0 1	9	2276	-4
0 0 0 1 0 1 0	10	2048	0
0 0 0 1 0 1 1	11	1862	-2
0 0 0 1 1 0 0	12	1707	-4
0 0 0 1 1 0 1	13	1576	-8
0 0 0 1 1 1 0	14	1463	-2
0 0 0 1 1 1 1	15	1366	-10
0 0 1 0 0 0 0	16	1280	0
0 0 1 0 0 0 1	17	1205	-5
0 0 1 0 0 1 0	18	1138	-4
0 0 1 0 0 1 1	19	1078	-2
0 0 1 0 1 0 0	20	1024	0
0 0 1 0 1 0 1	21	976	-16
0 0 1 0 1 1 0	22	931	-2
0 0 1 0 1 1 1	23	891	-13
0 0 1 1 0 0 0	24	854	-16
0 0 1 1 0 0 1	25	820	-20
0 0 1 1 0 1 0	26	788	-8
0 0 1 1 0 1 1	27	759	-13
0 0 1 1 1 0 0	28	732	-16
0 0 1 1 1 0 1	29	707	-23
0 0 1 1 1 1 0	30	683	-10

Table 2-2 Sector Select Switch Settings (cont'd)
(Segment 1 = 1)

SECTOR SWITCH SETTING

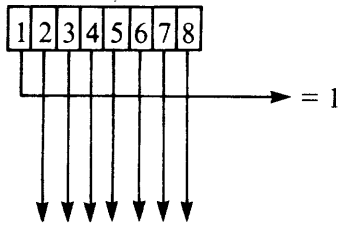


TRACK = 20,480 BYTES

$2^6 2^5 2^4 2^3 2^2 2^1 2^0$	SECTORS PER TRACK	BYTES PER SECTOR	LAST SECTOR SHORTER
0 0 1 1 1 1 1	31	661	-11
0 1 0 0 0 0 0	32	640	0
0 1 0 0 0 0 1	33	621	-13
0 1 0 0 0 1 0	34	603	-22
0 1 0 0 0 1 1	35	586	-30
0 1 0 0 1 0 0	36	569	-4
0 1 0 0 1 0 1	37	554	-18
0 1 0 0 1 1 0	38	539	-2
0 1 0 0 1 1 1	39	526	-34
0 1 0 1 0 0 0	40	512	0
0 1 0 1 0 0 1	41	500	-20
0 1 0 1 0 1 0	42	488	-16
0 1 0 1 0 1 1	43	477	-31
0 1 0 1 1 0 0	44	466	-24
0 1 0 1 1 0 1	45	456	-40
0 1 0 1 1 1 0	46	446	-36
0 1 0 1 1 1 1	47	436	-12
0 1 1 0 0 0 0	48	427	-16
0 1 1 0 0 0 1	49	418	-2
0 1 1 0 0 1 0	50	410	-20
0 1 1 0 0 1 1	51	402	-16
0 1 1 0 1 0 0	52	394	-8
0 1 1 0 1 0 1	53	387	-31
0 1 1 0 1 1 0	54	380	-40
0 1 1 0 1 1 1	55	373	-35
0 1 1 1 0 0 0	56	366	-16
0 1 1 1 0 0 1	57	360	-40
0 1 1 1 0 1 0	58	354	-52
0 1 1 1 0 1 1	59	348	-52
0 1 1 1 1 0 0	60	342	-40

Table 2-2 Sector Select Switch Settings (cont'd)
(Segment 1 = 1)

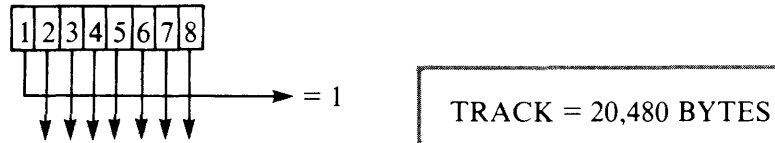
SECTOR SWITCH SETTING



		TRACK = 20,480 BYTES	
$2^6 2^5 2^4 2^3 2^2 2^1 2^0$	SECTORS PER TRACK	BYTES PER SECTOR	LAST SECTOR SHORTER
0 1 1 1 1 0 1	61	336	-16
0 1 1 1 1 1 0	62	331	-42
0 1 1 1 1 1 1	63	326	-58
1 0 0 0 0 0 0	64	320	0
1 0 0 0 0 0 1	65	316	-60
1 0 0 0 0 1 0	66	311	-46
1 0 0 0 0 1 1	67	306	-22
1 0 0 0 1 0 0	68	302	-56
1 0 0 0 1 0 1	69	297	-13
1 0 0 0 1 1 0	70	293	-30
1 0 0 0 1 1 1	71	289	-39
1 0 0 1 0 0 0	72	285	-40
1 0 0 1 0 0 1	73	281	-33
1 0 0 1 0 1 0	74	277	-18
1 0 0 1 0 1 1	75	274	-70
1 0 0 1 1 0 0	76	270	-40
1 0 0 1 1 0 1	77	266	-2
1 0 0 1 1 1 0	78	263	-34
1 0 0 1 1 1 1	79	260	-60
1 0 1 0 0 0 0	80	256	0
1 0 1 0 0 0 1	81	253	-13
1 0 1 0 0 1 0	82	250	-20
1 0 1 0 0 1 1	83	247	-21
1 0 1 0 1 0 0	84	244	-16
1 0 1 0 1 0 1	85	241	-5
1 0 1 0 1 1 0	86	239	-74
1 0 1 0 1 1 1	87	236	-52
1 0 1 1 0 0 0	88	233	-24
1 0 1 1 0 0 1	89	231	-79
1 0 1 1 0 1 0	90	228	-40

Table 2-2 Sector Select Switch Settings (cont'd)
(Segment 1 = 1)

SECTOR SWITCH SETTING



$2^6 2^5 2^4 2^3 2^2 2^1 2^0$	SECTORS PER TRACK	BYTES PER SECTOR	LAST SECTOR SHORTER
1 0 1 1 0 1 1	91	226	-86
1 0 1 1 1 0 0	92	223	-36
1 0 1 1 1 0 1	93	221	-73
1 0 1 1 1 1 0	94	218	-12
1 0 1 1 1 1 1	95	216	-40
1 1 0 0 0 0 0	96	214	-64
1 1 0 0 0 0 1	97	212	-84
1 1 0 0 0 1 0	98	209	-2
1 1 0 0 0 1 1	99	207	-13
1 1 0 0 1 0 0	100	205	-20
1 1 0 0 1 0 1	101	203	-23
1 1 0 0 1 1 0	102	201	-22
1 1 0 0 1 1 1	103	199	-17
1 1 0 1 0 0 0	104	197	-8
1 1 0 1 0 0 1	105	196	-100
1 1 0 1 0 1 0	106	194	-84
1 1 0 1 0 1 1	107	192	-64
1 1 0 1 1 0 0	108	190	-40
1 1 0 1 1 0 1	109	188	-12
1 1 0 1 1 1 0	110	187	-90
1 1 0 1 1 1 1	111	185	-55
1 1 1 0 0 0 0	112	183	-16
1 1 1 0 0 0 1	113	182	-86
1 1 1 0 0 1 0	114	180	-40
1 1 1 0 0 1 1	115	179	-105
1 1 1 0 1 0 0	116	177	-52
1 1 1 0 1 0 1	117	176	-112
1 1 1 0 1 1 0	118	174	-52
1 1 1 0 1 1 1	119	173	-107
1 1 1 1 0 0 0	120	171	-40
1 1 1 1 0 0 1	121	170	-90
1 1 1 1 0 1 0	122	168	-16
1 1 1 1 0 1 1	123	167	-61
1 1 1 1 1 0 0	124	166	-104
1 1 1 1 1 0 1	125	164	-20
1 1 1 1 1 1 0	126	163	-58
1 1 1 1 1 1 1	127	162	-94
0 0 0 0 0 0 0	128	160	0

2.5 CABINET/RACK INSTALLATION

The mounting bracket (see Figure 2-11) shipped with the D2246 secures the disk drive when it is installed in a cabinet or rack.

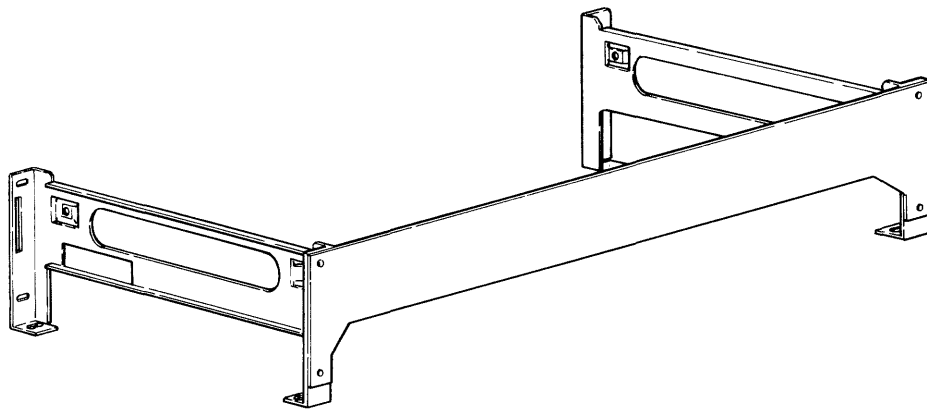


Figure 2-11 Mounting Bracket

The drive can be installed in either a horizontal or vertical position as shown in Figure 2-12. Figure 2-12 also shows the required ventilation for each mounting position. An air flow of 1.1 cubic yards per minute (1.1 yd³/min) is required on a 0.4-inch surface.

NOTE

Be certain that the segment 7 of the installation switch assembly is set according to the mounting position (see Section 2.4.1).

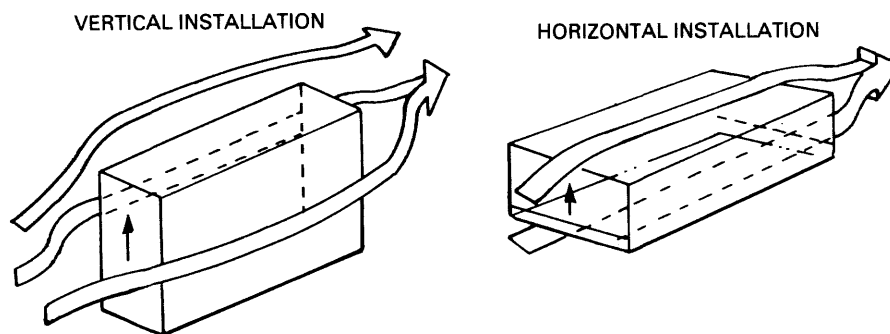


Figure 2-12 Horizontal and Vertical Installation

When installing the disk drive, first verify that the mounting holes in the rack or cabinet align with the holes in the mounting bracket. Refer to Appendix B for information on unit dimensions.

2.6 CABLE CONNECTIONS

This section describes the different connectors for the interface signal cables (cables A and B), for the system ground cable, and for the power cable.

2.6.1 Interface Cables

Interface cables A and B are connected to the G9QST PCB as shown in Figure 2-13.

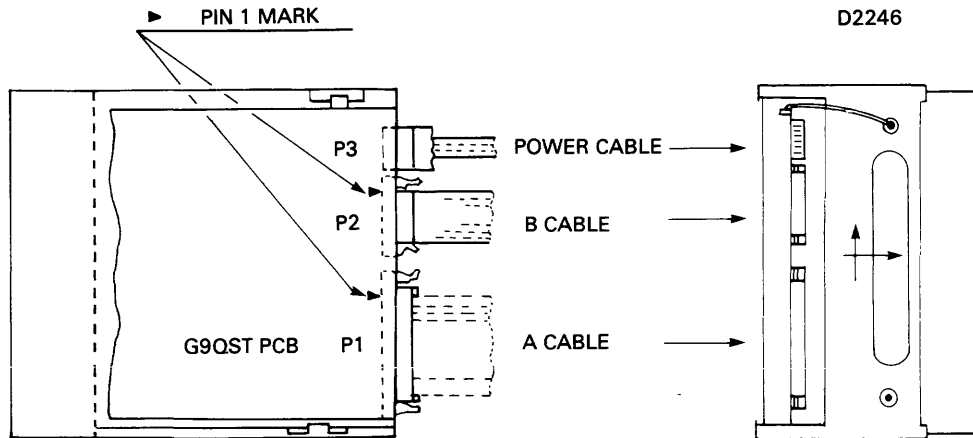


Figure 2-13 Interface Cable Connections

Cable B should not exceed 49.2 ft (15 m) in length. Cable A should not exceed 98.4 ft (30 m) in length. In a daisy-chain system, the total length of cable A (from the controller to the last drive) should not exceed 98.4 ft (see Figure 2-14).

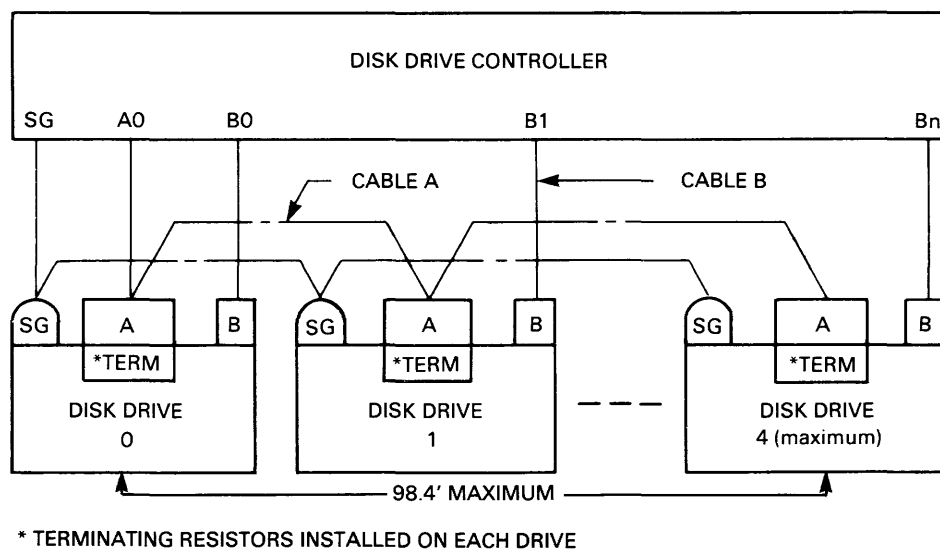


Figure 2-14 Cable A/Daisy-Chain System

2.6.2 System Ground Cable

Connect a system ground cable to the signal ground (SG) terminal at the rear of the disk drive (see Figure 2-15).

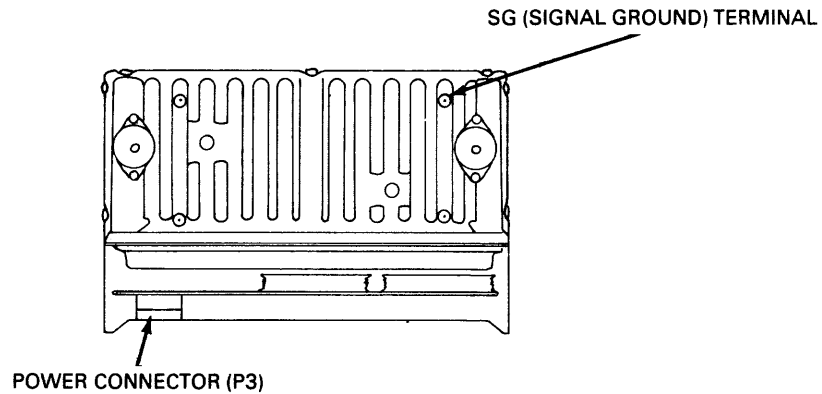


Figure 2-15 Signal Ground and Power Connections

2.6.3 Power Cable

Connect the power cable to connector P3 at the rear of the disk drive (see Figure 2-15).

2.7 LOCK CONTROL ASSEMBLY

When the disk drive is shipped, the spindle and actuator positioner are secured with a lock device to prevent movement. This lock must be released prior to operating the drive. To unlock the spindle and actuator, slide the lock control lever to the FREE position (see Figure 2-16).

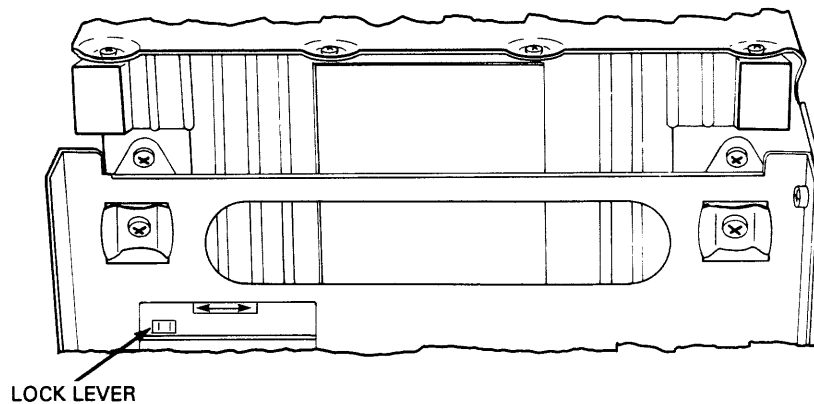
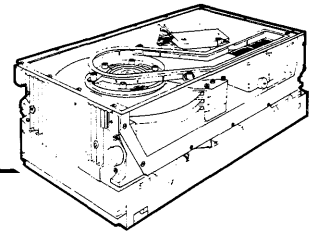


Figure 2-16 Lock Control Assembly

Chapter 3

Preventive Maintenance and Troubleshooting



This chapter outlines maintenance and troubleshooting procedures for the D2246 disk drive. It describes preventive maintenance, test operations and test points, and associated waveforms. Refer to Appendix C for information on how to use the optional diagnostic panel.

3.1 GENERAL MAINTENANCE RULES

Always observe the following general rules when replacing parts or servicing the disk drive.

- Turn off the disk drive and disconnect all ac power to the drive power supply before performing any maintenance procedure on the drive.
- Never remove or install any PCB, or disconnect any connector, plug, or wire while power is on.
- When removing any connector, grasp it firmly by its sides and pull it out. Do not remove any connector by pulling on the wire bundle.
- Do not remove any parts that are not specified in the replacement procedures.
- Package PCBs in an electrostatic-free envelope when they are transported.

3.2 MAINTENANCE TOOLS

Standard maintenance procedures require the following common hand tools.

- No. 1 Phillips screwdriver
- No. 2 Phillips screwdriver
- Small straight-tip screwdriver

The following instruments are also required.

- High impedance voltmeter
- Oscilloscope (Tektronics 465 or equivalent)

A rotor handler (NEC part number 134-233280) and a diagnostic panel (NEC part number 134-200267) are recommended.

3.3 PREVENTIVE MAINTENANCE

Preventive maintenance is limited to periodic dusting of the surface of the drive. No lubrication or further cleaning is required or recommended. D2246 disk drives contain no parts that require scheduled adjustment or replacement.

NOTE

The air filter in the sealed head/disk assembly cannot be replaced or cleaned.

As part of a periodic preventive maintenance routine, run system-specific (software) diagnostic programs or use the diagnostic panel to run offline test procedures (see Appendix C).

3.4 TROUBLESHOOTING

If a fault occurs, attempt to isolate the fault to the host, to the host controller, to the disk drive, or to another connecting component. For faults isolated to the disk drive, use the troubleshooting procedures outlined in the following flowcharts. These procedures localize the fault to a specific drive component.

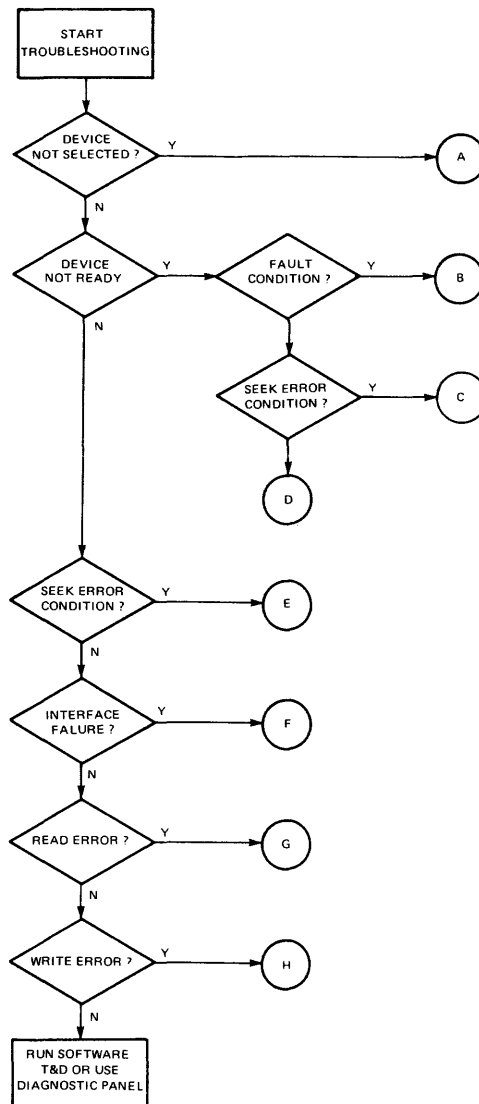


Figure 3-1 Troubleshooting Flowcharts

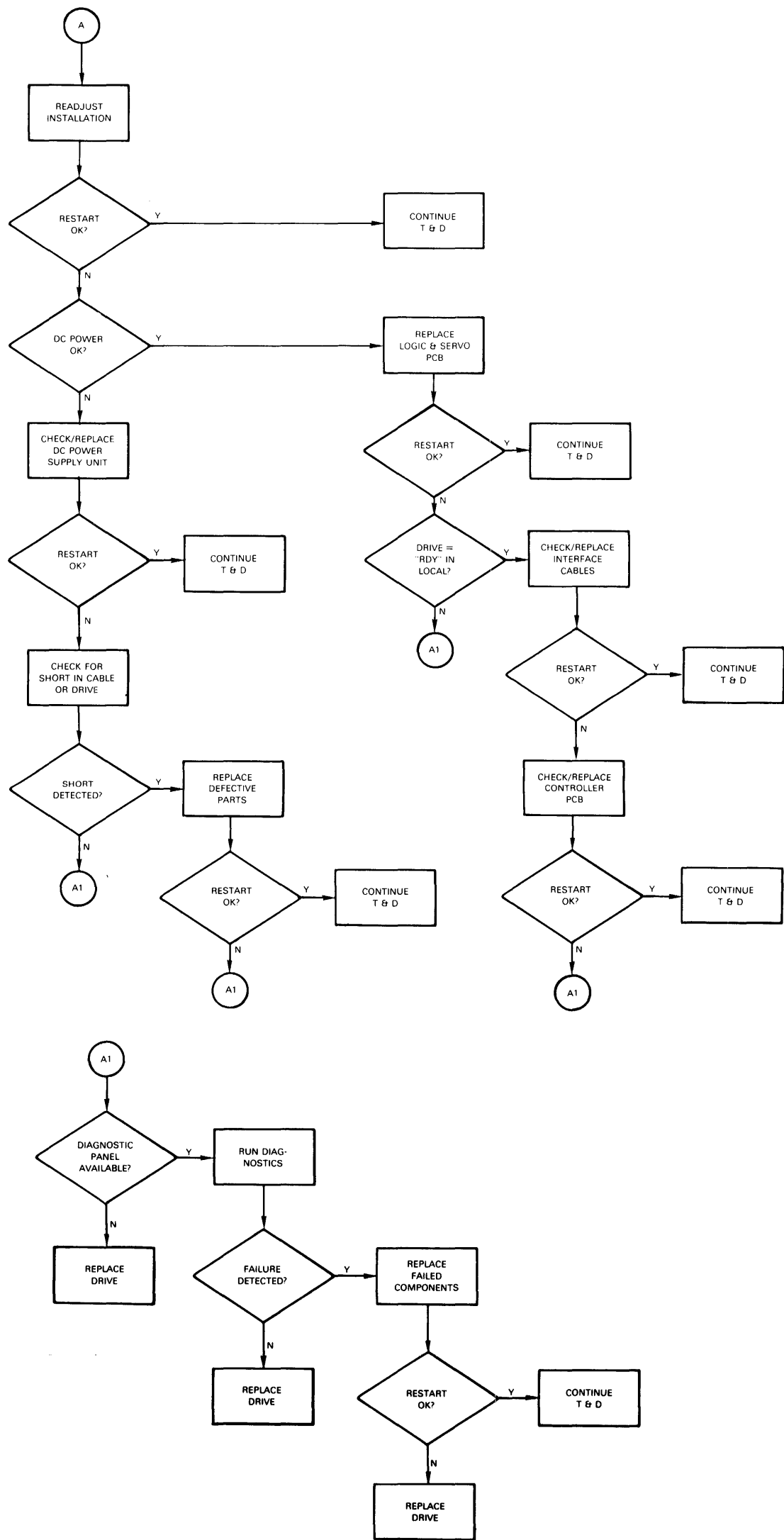


Figure 3-1 Troubleshooting Flowcharts (cont'd)

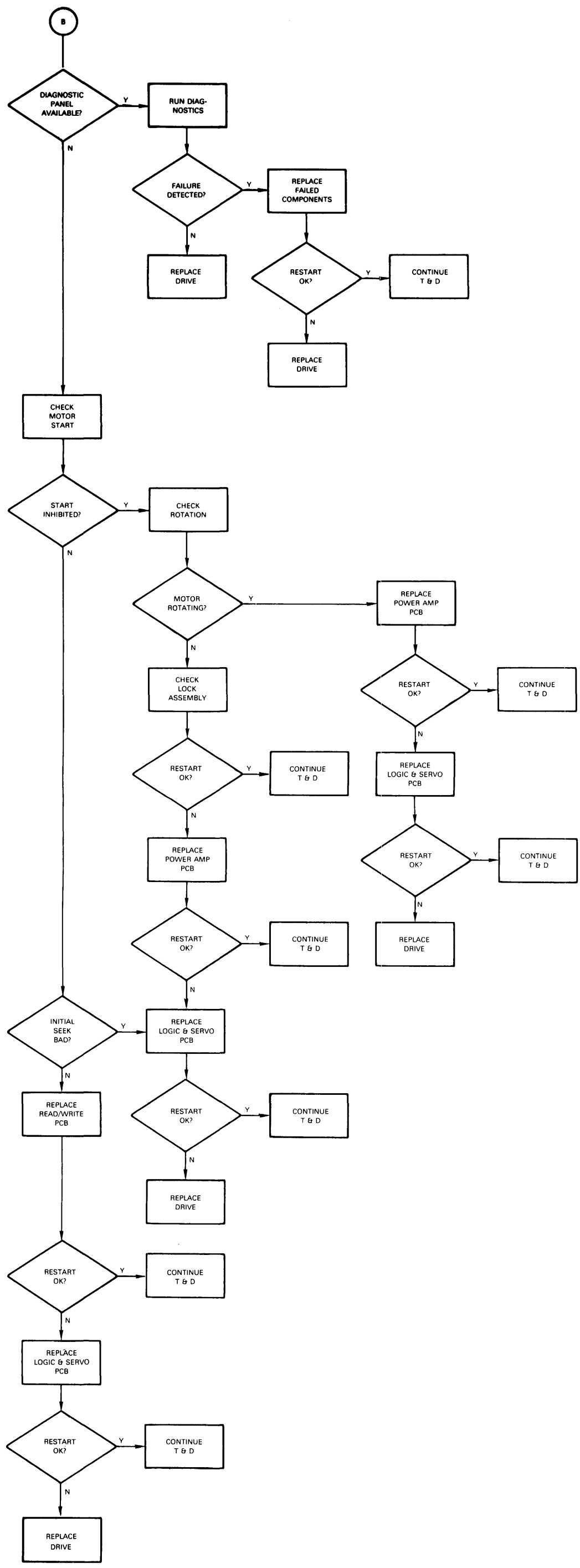


Figure 3-1 Troubleshooting Flowcharts (cont'd)

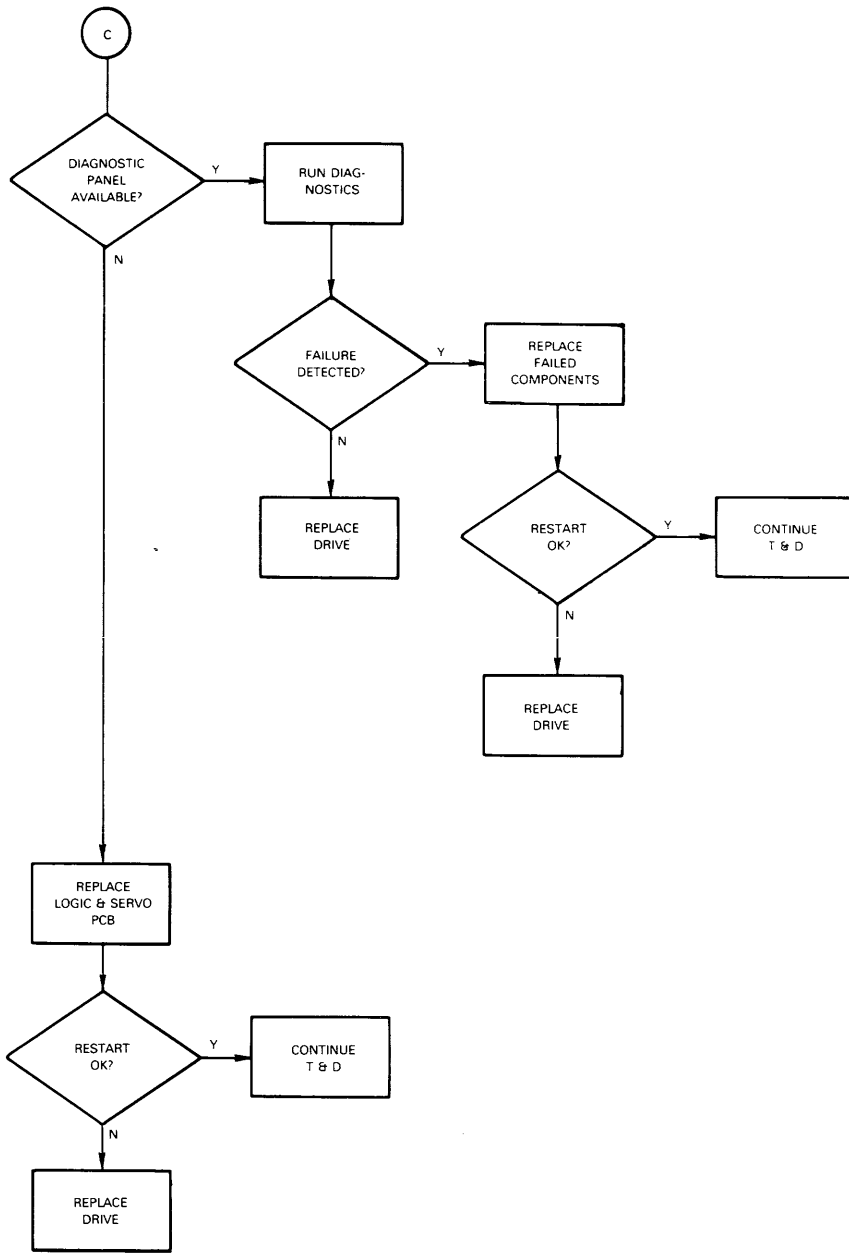


Figure 3-1 Troubleshooting Flowcharts (cont'd)

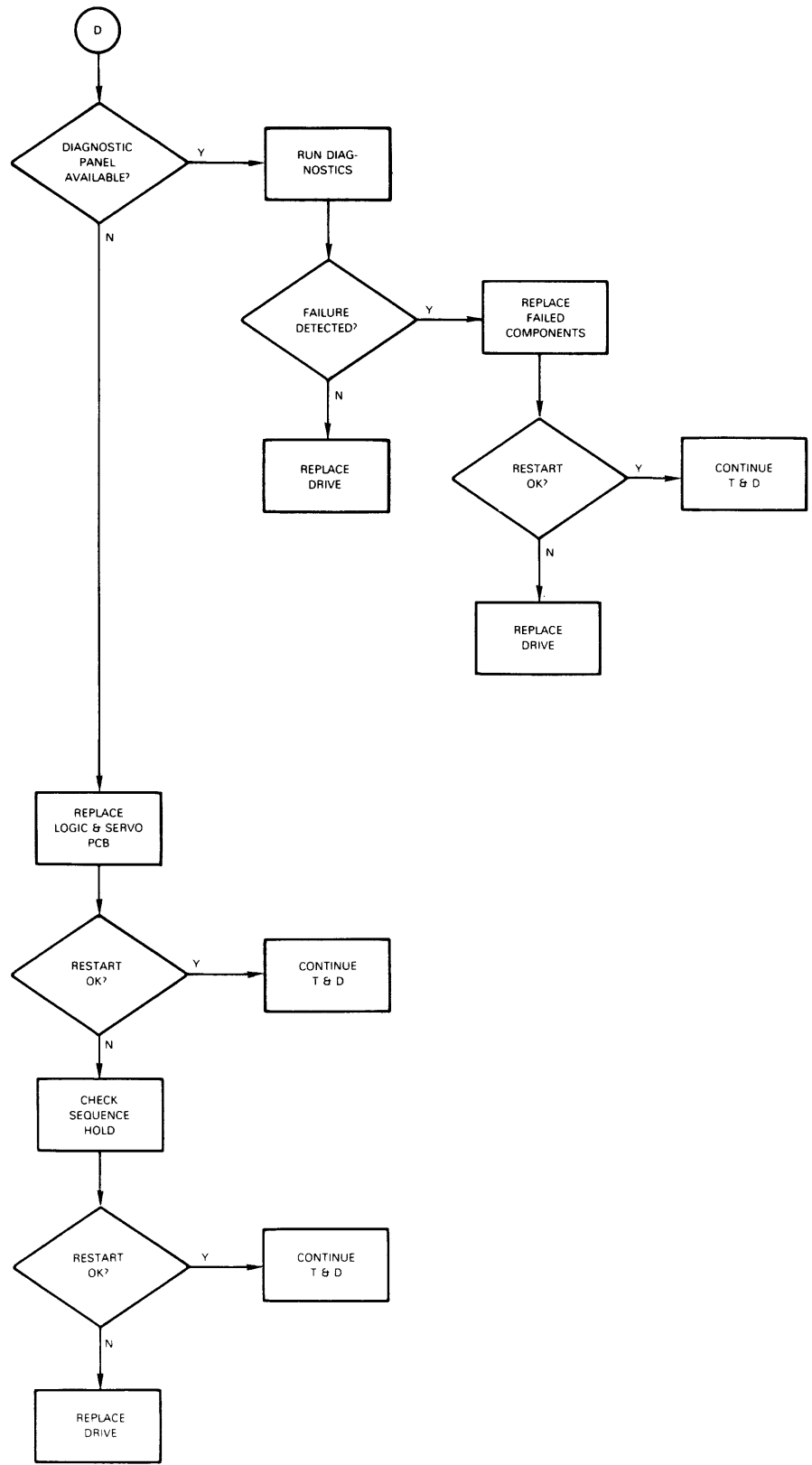


Figure 3-1 Troubleshooting Flowcharts (cont'd)

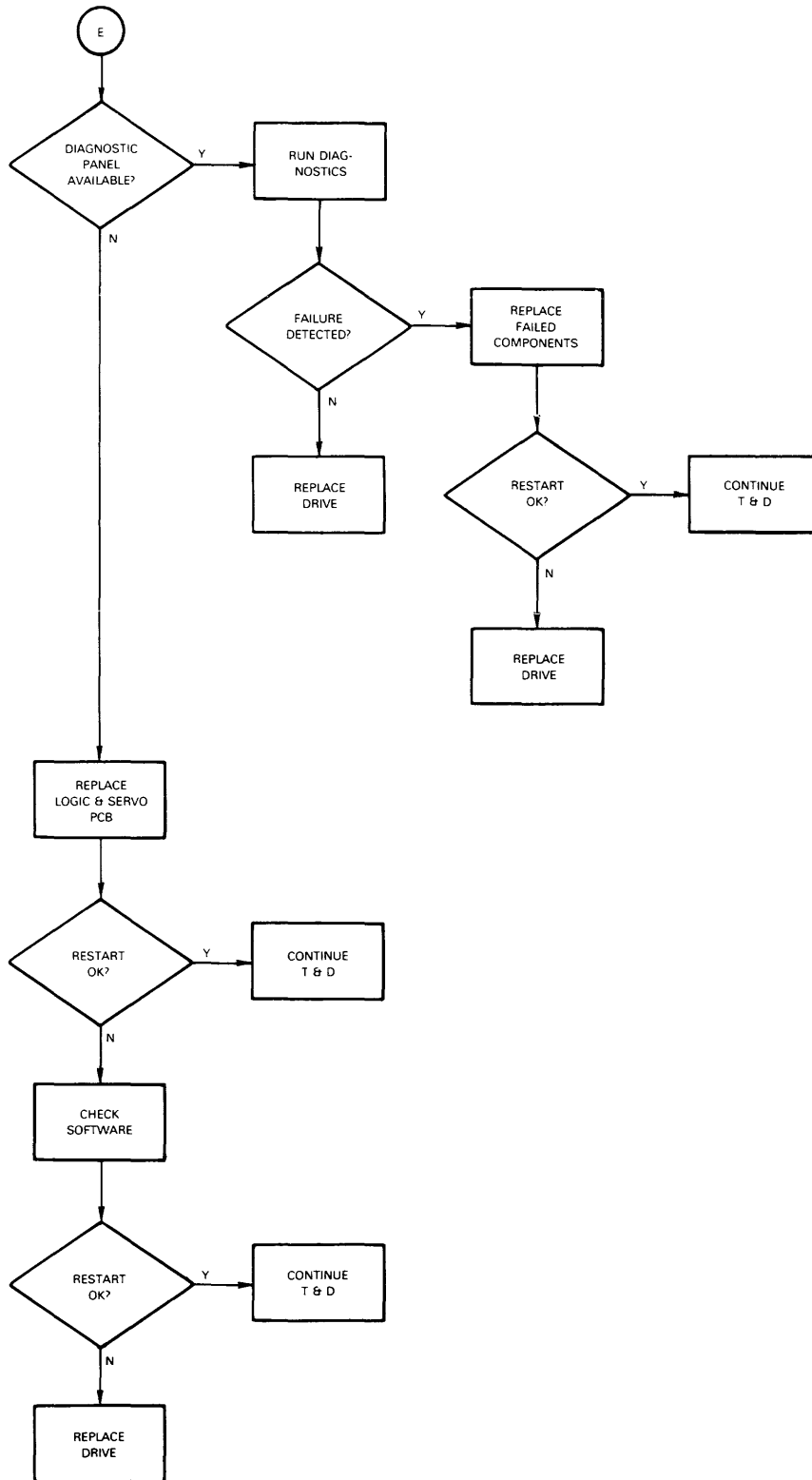


Figure 3-1 Troubleshooting Flowcharts (cont'd)

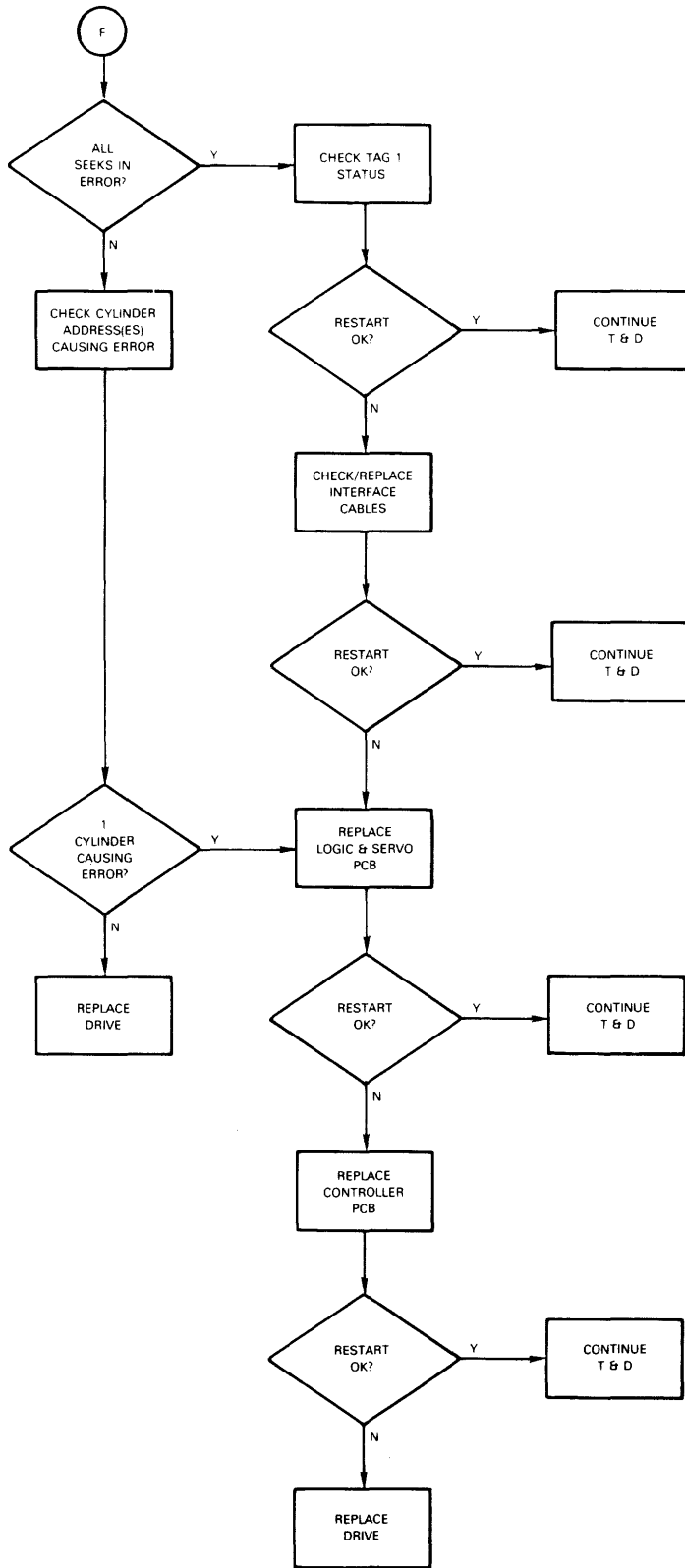


Figure 3-1 Troubleshooting Flowcharts (cont'd)

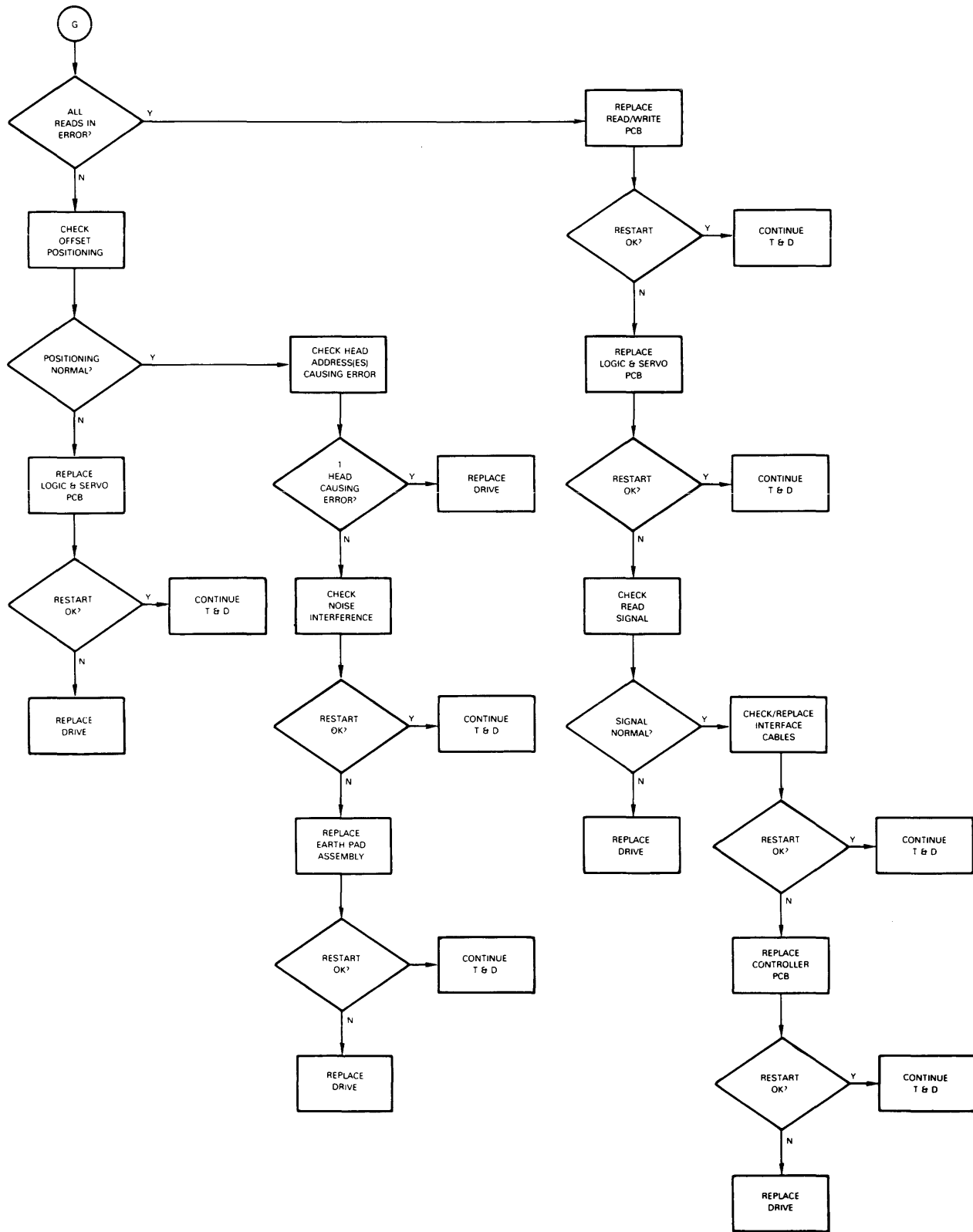


Figure 3-1 Troubleshooting Flowcharts (cont'd)

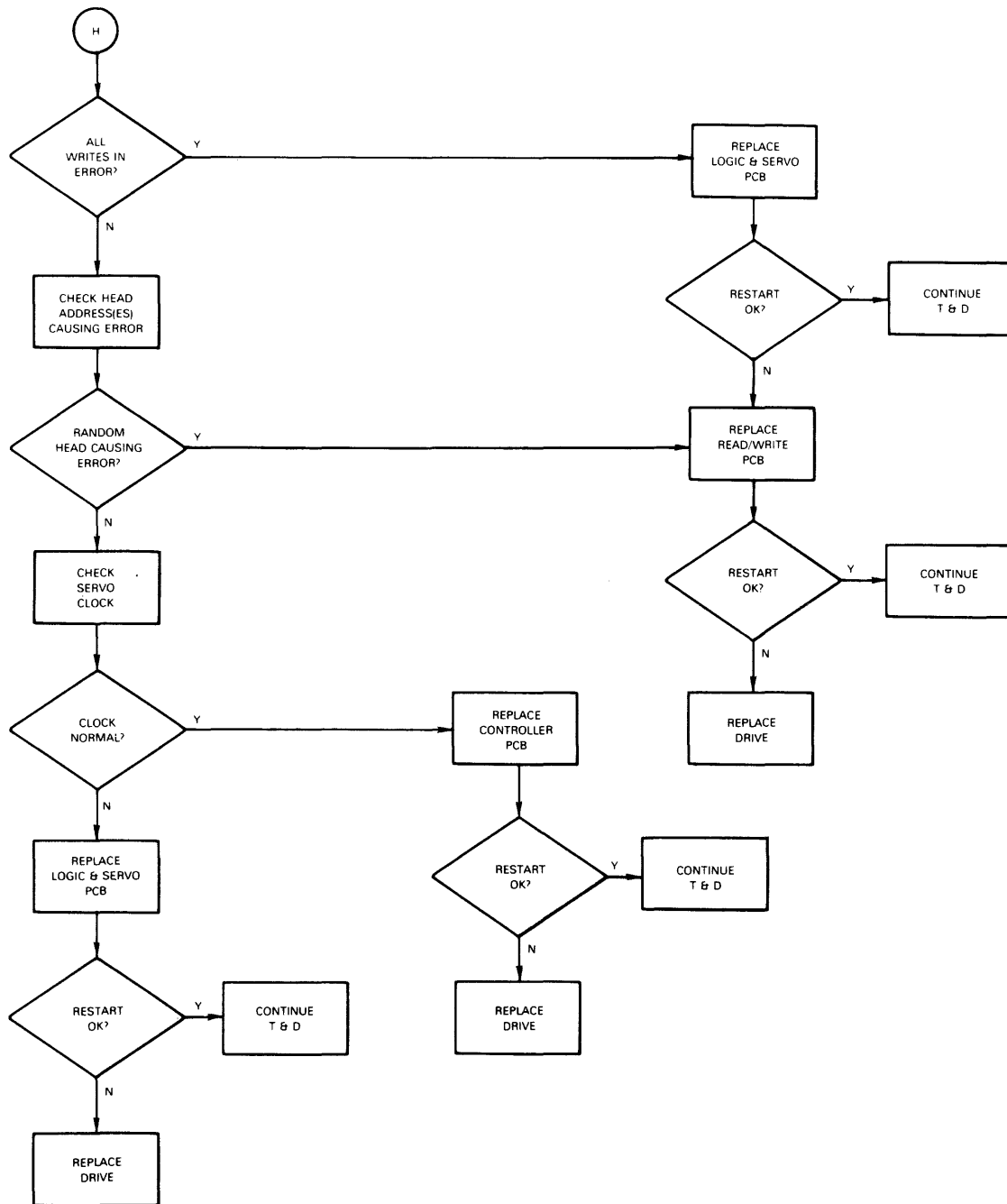


Figure 3-1 Troubleshooting Flowcharts (cont'd)

3.5 SERVO SYSTEM SIGNALS

Test point locations on the G9QST logic and servo PCB are shown in Figure 3-2. Table 3-1 lists the signal output and signal level from each test point.

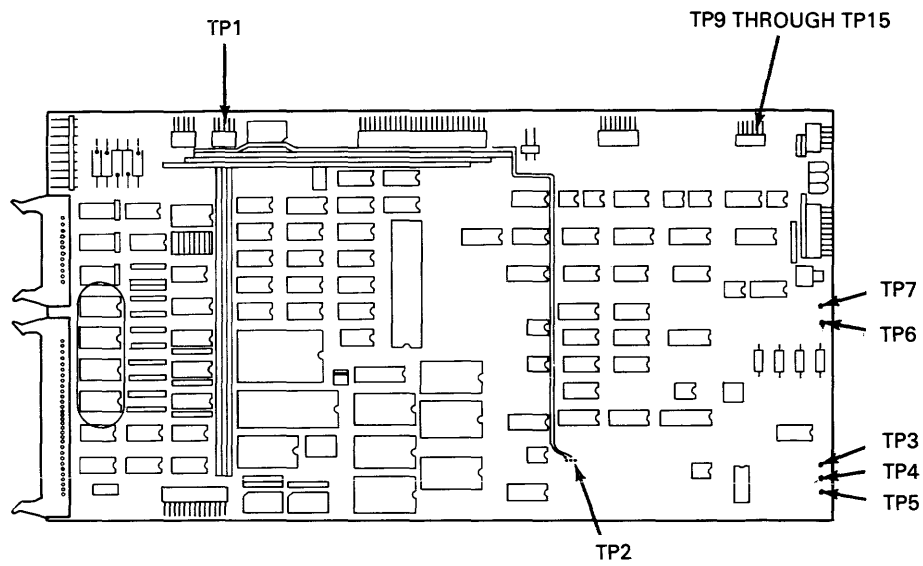


Figure 3-2 G9QST Test Point Locations

Table 3-1 Test Point Signal Outputs

TEST POINT	SIGNAL	LEVEL
TP2-2	Tripulse input (positive polarity)	20–75 mVpp
TP2-3	Tripulse input (negative polarity)	20–75 mVpp
TP3	Automatic gain control (AGC) standard voltage (regulated by RV1)	1.1 V (approx)
TP4	AGC control voltage	6.0 V (approx)
TP5	Tripulse output (AGC output)	4.0 Vpp (approx)
TP6	Q position signal	0 to ± 5.6 V
TP7	N position signal	0 to ± 5.6 V
TP8	Not used	
TP9	Connected to GND during offset adjustment (see Section 5.2)	2.0 V (approx)
TP10	Speed set signal	0 to +6.0 V
TP11	Speed signal (reverse polarity to TP10)	0 to -6.0 V
TP12	Noise injunction terminal	0 to 2.0 Vpp
TP13	Position loop phase compensation filter input	
TP14	Position loop secondary filter output	
TP15	Servo current (1.0 V corresponds to 1.0A)	0 to 3.0 Vpp

Normal servo system signals match the specifications and waveforms listed in Table 3-2.

Table 3-2 G9QST Servo Signals

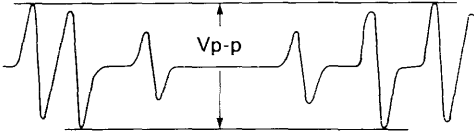
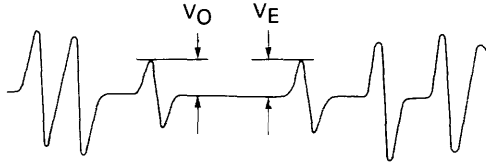
FUNCTION	TEST POINT	COMMENTS
Tripulse input amplitude	TP2-2, TP2-3	 <p data-bbox="873 730 1341 793">40mV_{pp} ≤ V_{pp} ≤ 150mV_{pp} at Cylinder 000 and Cylinder 691</p>
AGC output amplitude	TP5	 <p data-bbox="870 1209 1203 1245">V_O, V_E = About 1.0 V_{O-p}</p>
AGC standard voltage	TP3	DC about 1.0V

Table 3-2 G9QST Servo Signals (cont'd)

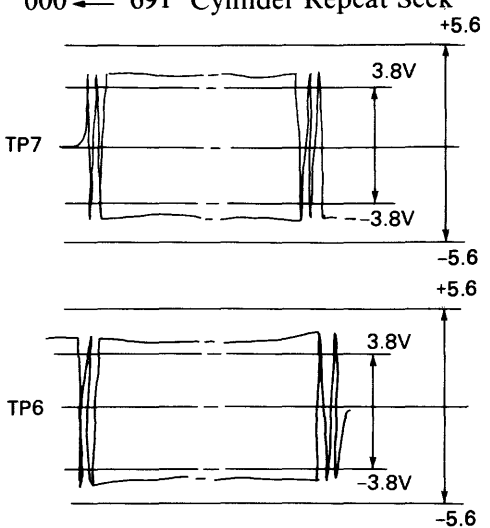
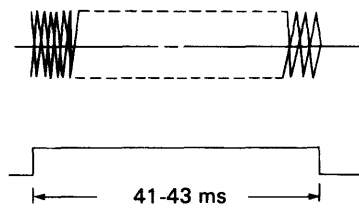
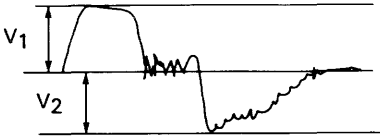
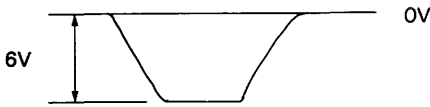
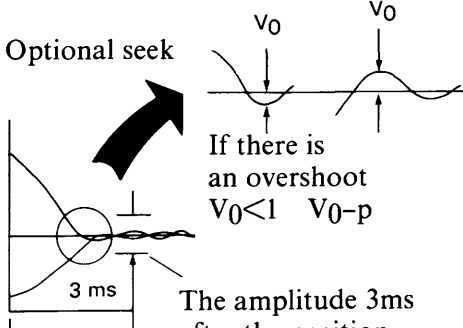
FUNCTION	TEST POINT	COMMENTS
Position signal amplitude	TP6, TP7 TP1-4 of G9QST is the trigger.	<p>000 ↔ 69I Cylinder Repeat Seek</p>  <p>TP7</p> <p>TP6</p>
Seek time	TP7 TP1-5	<p>000 ↔ 69I Cylinder Repeat Seek</p>  <p>41-43 ms</p> <p>*The settling time is not included.</p>

Table 3-2 G9QST Servo Signals (cont'd)

FUNCTION	TEST POINT	COMMENTS
<p>Current waveform</p>	<p>TP15</p> <p>The trigger is TP1-4 and TP1-3 of G9QST.</p>	<p>000 ⇌ 691 Cylinder Repeat Seek</p>  <p>$V_1 + 1.0 - 1.3 \text{ V}$ $V_2 < 1.3 \text{ V}$</p> <p>(The polarity changes according to the seek direction.)</p>
<p>Speed profile follows</p>	<p>TP10, TP11</p> <p>The trigger is TP1-4 and TP1-3 of G9QST.</p>	<p>000 ⇌ 691 Cylinder Repeat Seek</p>  <p>The speed set signal (TP10) is inverted and made to overlap the speed signal (TP11).</p>
<p>Position transient response</p>	<p>TP7</p> <p>The trigger is TP1-5 of G9QST.</p>	<p>Optional seek</p>  <p>If there is an overshoot $V_0 < 1$ $V_0 - p$</p> <p>The amplitude 3ms after the position mode is set shall be less than $0.5V_{0p}$.</p>

3.6 SEEK OPERATIONS TESTING

A repeat seek or a one-cylinder seek operation can be initiated by connecting strapping wire to TP1.

3.6.1 Repeat Seek Operation

A repeat seek operation seeks from the low cylinder (cylinder 000) to the high cylinder (cylinder 691), and then from the high cylinder back to the low cylinder. To perform a repeat seek operation, connect wires to TP1 as shown in Figure 3-3.

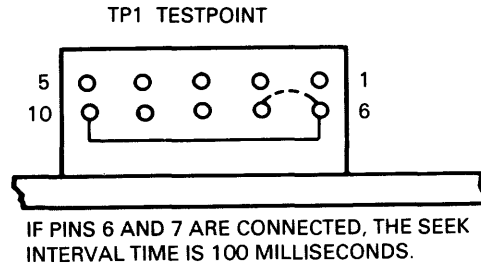


Figure 3-3 Repeat Seek Using TP1

3.6.2 One-Cylinder Seek Operation

A one-cylinder seek operation seeks from cylinder 000, to cylinder 001, to cylinder 002, and continues to the high cylinder. From the high cylinder, the unit seeks to cylinder 690, to cylinder 689, and continues back to the low cylinder. To perform a one-cylinder seek operation, connect wires to TP1 as shown in Figure 3-4.

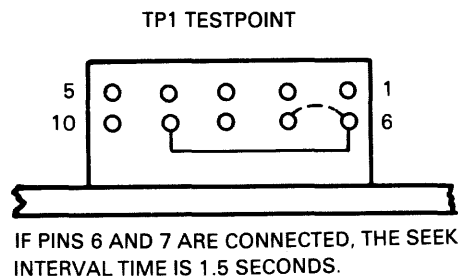
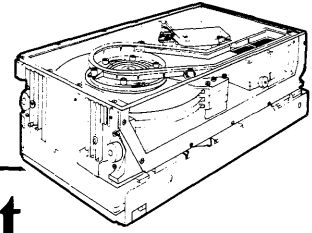


Figure 3-4 One-Cylinder Seek Using TP1

Chapter 4

Removal and Replacement Procedures



This chapter provides procedures for removing and replacing D2246 components and assemblies. Field-replaceable items are listed in Table 4-1.

Table 4-1 D2246 Field Replaceable Components

COMPONENT/ASSEMBLY	NEC PART NUMBER
G9QST Logic and Servo PCB	134-832954
G9QSQ Power Amplifier PCB	134-832951
G9QSN Read/Write PCB	134-832949
Earth Pad Assembly	134-232861-0
Motor Stator Assembly	806-942281-003-0

4.1 G9QST (LOGIC AND SERVO) PCB REMOVAL

Follow these steps to remove the G9QST logic and servo PCB.

1. Turn off the D2246.
2. Disconnect the dc power supply.
3. Loosen the two screws that secure the board cover to the drive unit (see Figure 4-1).
4. Lift the board cover straight up to remove it.
5. Disconnect cable connectors J55, J54, J53, and J41 (see Figure 4-2).
6. Remove the two screws that fasten the G9QST to the drive unit (see Figure 4-2).
7. Lift the G9QST PCB straight up to remove it.

When installing a new G9QST PCB, be sure that the DIP switch, jumper, and terminating resistor configurations on the replacement board match those on the old board.

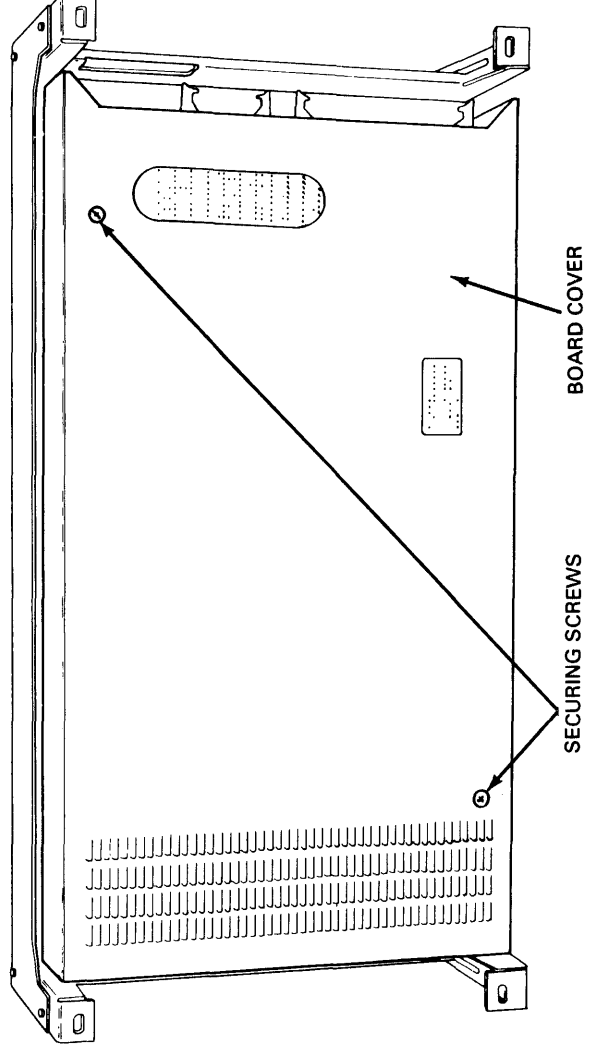


Figure 4-1 D2246 Board Cover

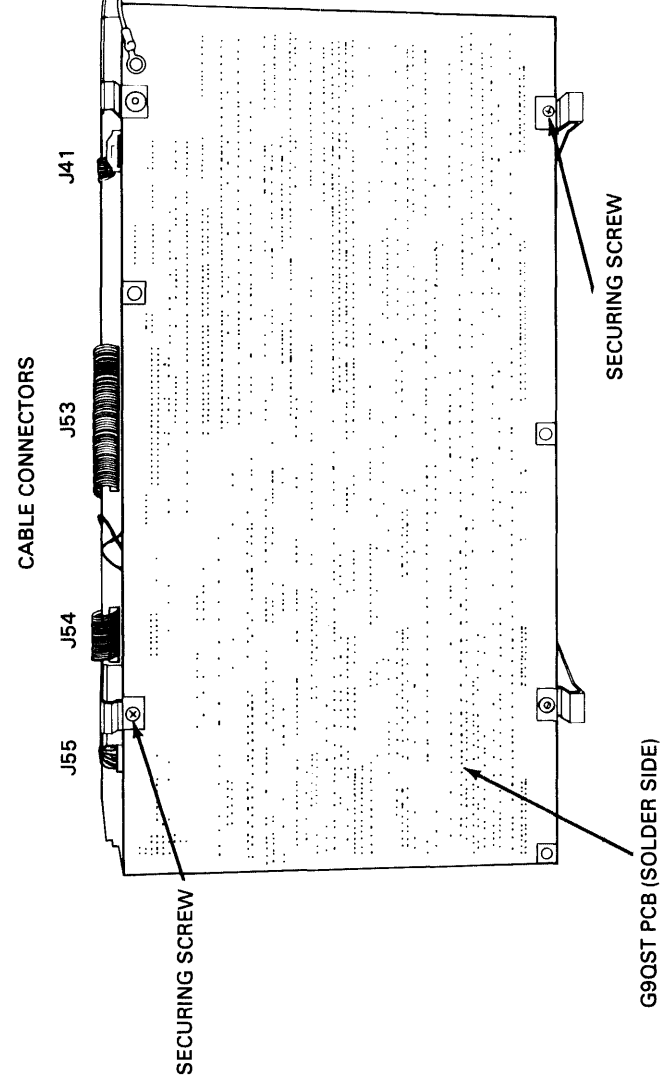


Figure 4-2 G9QST Cable Connectors

4.2 G9QSN (READ/WRITE) PCB REMOVAL

Follow these steps to remove the G9QSN read/write PCB.

1. Turn off the D2246.
2. Disconnect the dc power supply.
3. Remove the G9QST PCB (see Section 4.1).
4. Remove the four screws that secure the larger air separator (air separator A) to the drive unit (see Figure 4-3).
5. Lift air separator A straight up to remove it.
6. Disconnect cable connectors J31 and J32 (see Figure 4-4).
7. Lift the G9QSN PCB slightly and slide it away from the earth pad assembly to remove it (see Figure 4-4).

4.3 EARTH PAD ASSEMBLY REMOVAL

Follow these steps to remove the earth pad assembly.

1. Turn off the D2246.
2. Disconnect the dc power supply.
3. Remove the G9QST PCB (see Section 4.1).
4. Remove the screw that attaches the earth pad assembly to the smaller air separator (air separator B — see Figure 4-3).
5. Lift the earth pad assembly straight up to remove it.

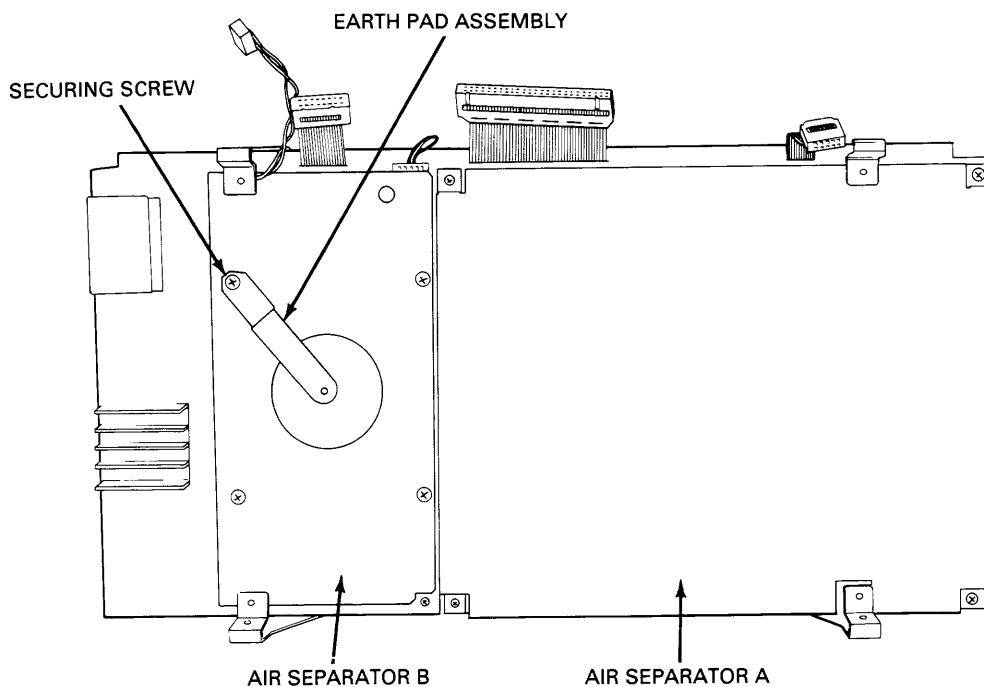


Figure 4-3 D2246 Air Separators

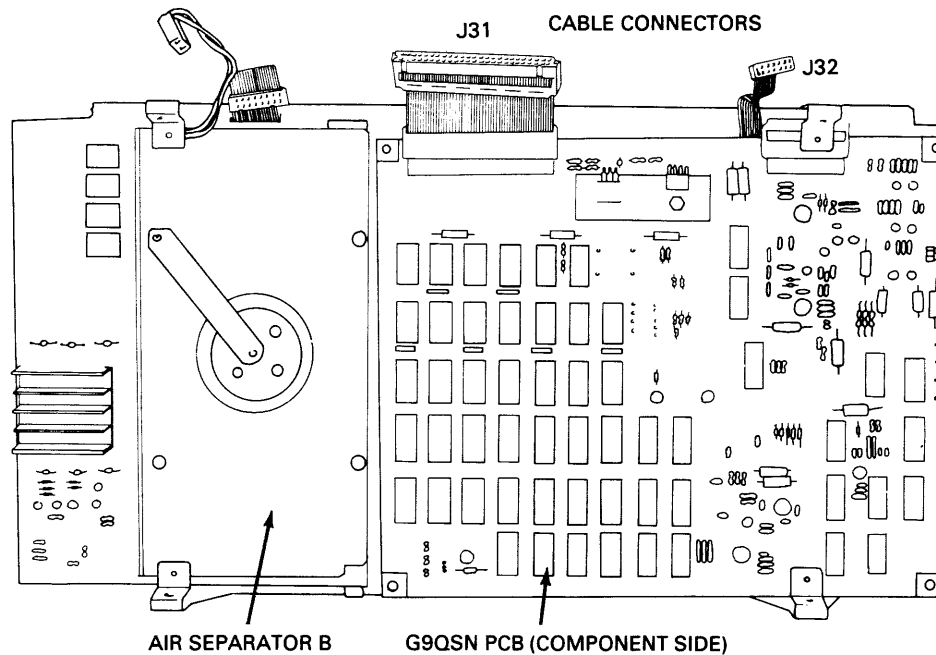


Figure 4-4 G9QSN Cable Connectors

4.4 G9QSQ (POWER AMPLIFIER) PCB REMOVAL

Follow these steps to remove the G9QSQ power amplifier PCB.

1. Turn off the D2246.
2. Disconnect the dc power supply.
3. Remove the G9QST PCB (see Section 4.1).
4. Remove the earth pad assembly (see Section 4.3).
5. Remove the three screws that secure air separator B to the drive unit (see Figure 4-4).
6. Lift air separator B and slide it to the side to remove it.
7. Disconnect cable connectors J22, J23, J24, and J44 (see Figure 4-5).
8. Remove the three screws that attach the G9QSQ PCB to the drive unit (see Figure 4-5).
9. Lift the G9QSQ PCB slightly and slide it to the side to remove it.

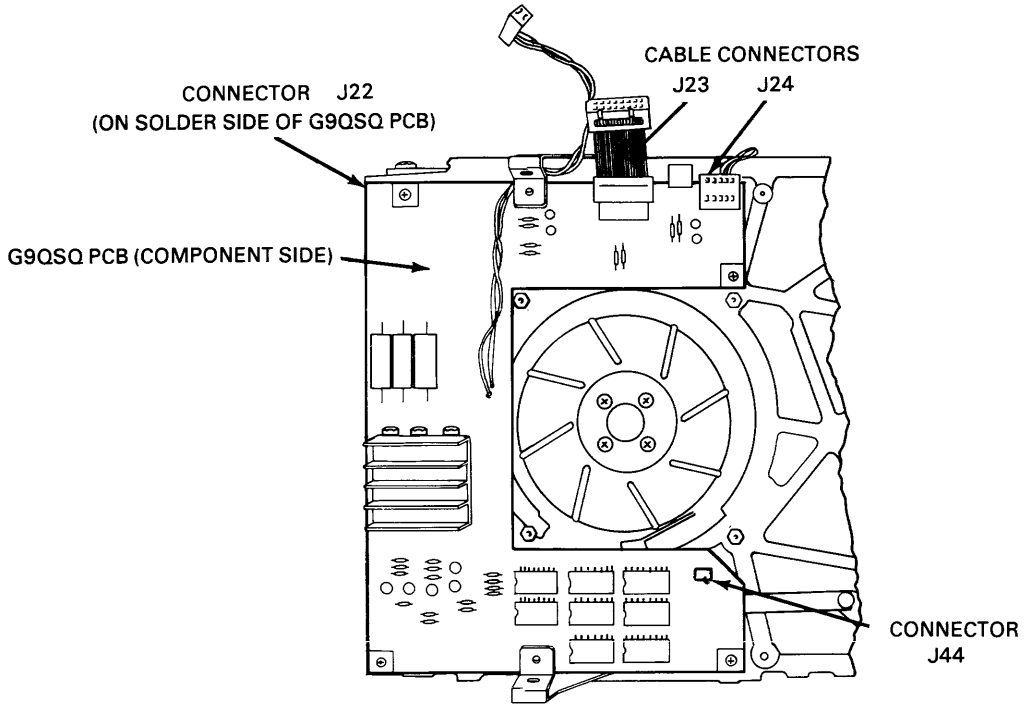


Figure 4-5 G9QSQ Cable Connectors

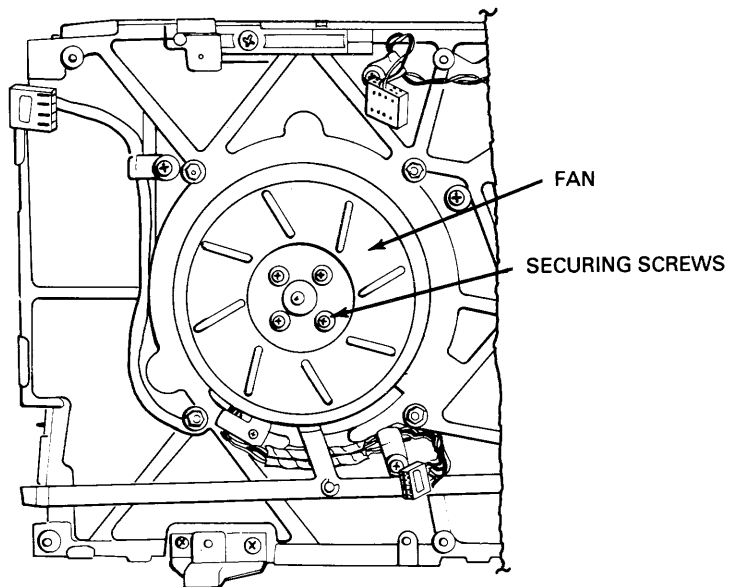


Figure 4-6 D2246 Fan

4.5 MOTOR STATOR ASSEMBLY REMOVAL

Follow these steps to remove the motor stator assembly.

1. Turn off the D2246.
2. Disconnect the dc power supply.
3. Remove the G9QST PCB (see Section 4.1).
4. Remove the earth pad assembly (see Section 4.3).
5. Remove the G9QSQ PCB (see Section 4.4).
6. Loosen the four screws that secure the fan (see Figure 4-6) and remove the fan by lifting it straight up.
7. Remove the rotor using the special rotor handling tool (see Figure 4-7).
8. Loosen the three screws that secure the claw stopper (see Figure 4-7) and remove the claw stopper.
9. Loosen the three screws that secure the motor shield and remove it.
10. Slide the motor stator assembly carefully along the spindle to remove it.

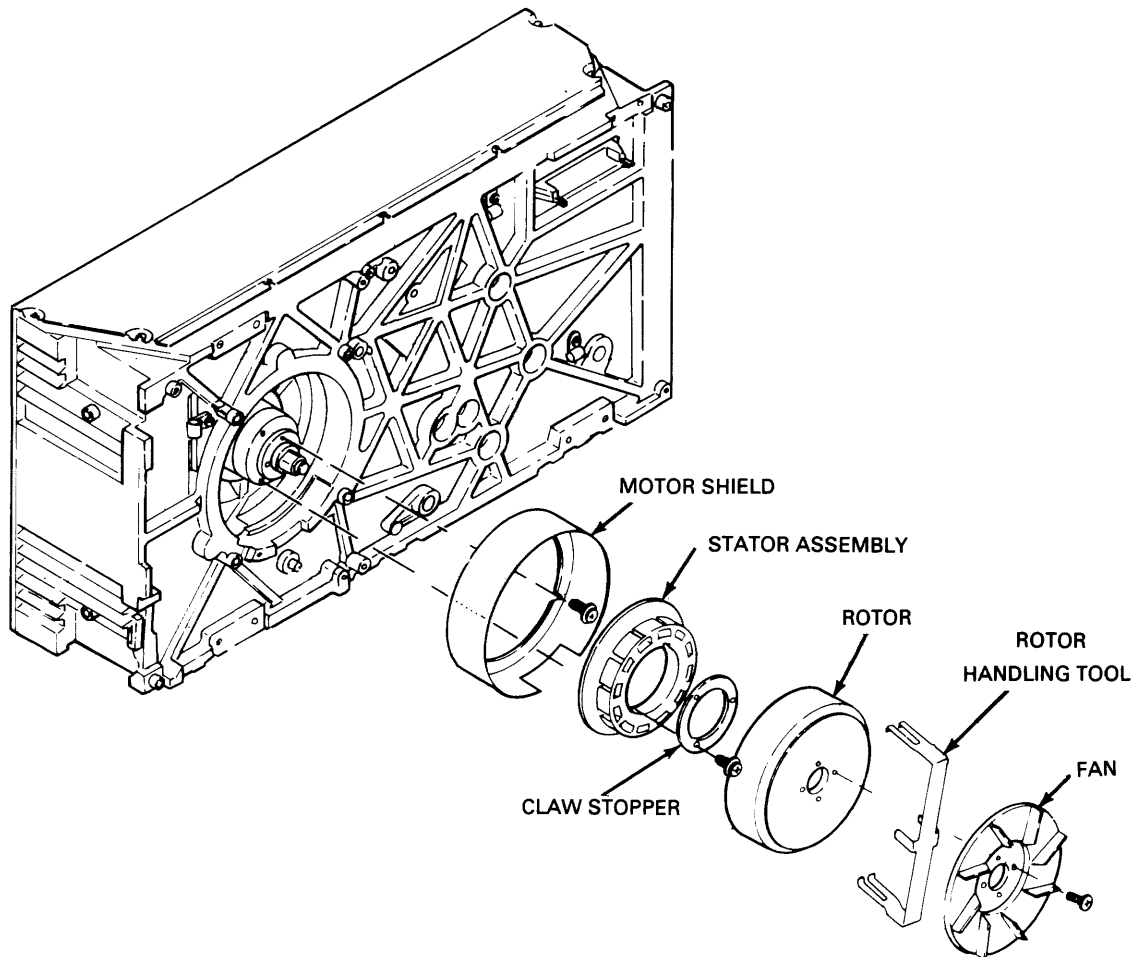
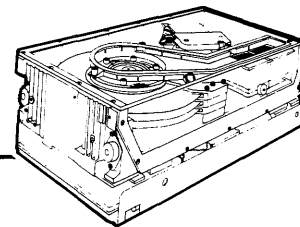


Figure 4-7 D2246 Stator Assembly

Chapter 5

Adjustments



This chapter describes how to adjust the servo offset and the seek speed circuits. These adjustments should always be performed when a new sealed head/disk module or a new logic and servo PCB has been installed. Adjustments can also be performed as part of a preventive maintenance routine.

5.1 REQUIRED TOOLS

Use the following tools to perform the adjustments described in this chapter.

- small straight-tip screwdriver
- oscilloscope
- strapping wire
- voltmeter

A diagnostic panel is recommended.

5.2 SERVO OFFSET ADJUSTMENT

Adjust the servo offset circuit whenever a new sealed head/disk module or a new G9QST logic and servo PCB has been installed. Follow these steps to adjust the servo offset circuit.

1. Place the D2246 in the vertical position (see Section 2.5).
2. Insure that segment 7 of the installation switch assembly is set to 1 (see Section 2.5).
3. Turn on power to the drive and wait until the Ready (RDY) light emitting diode (LED) lights.
4. Connect TP9 to ground (see Figure 5-1).
5. Trigger the oscilloscope at TP1-5.
6. Perform a repeat seek operation between cylinder 000 and cylinder 691, using either the diagnostic panel (see Appendix C) or the procedure described in Section 3.6.1.
7. Observe the waveform at TP7.
8. Adjust potentiometer RV4 (see Figure 5-1) to achieve the signal levels shown in Figure 5-2.

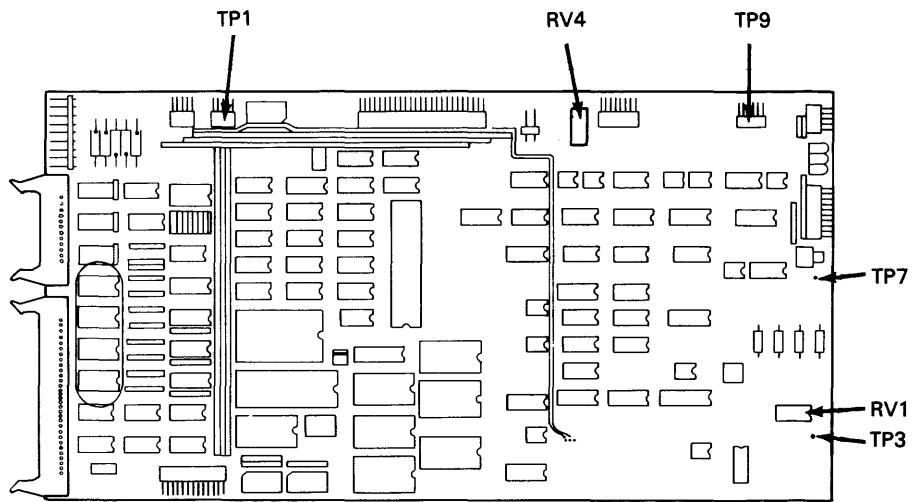


Figure 5-1 Servo Offset and Seek Speed Adjustment Test Points

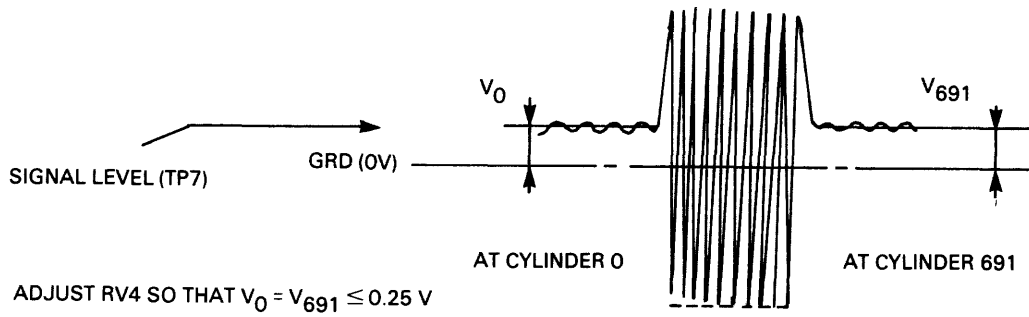


Figure 5-2 Servo Offset Waveform

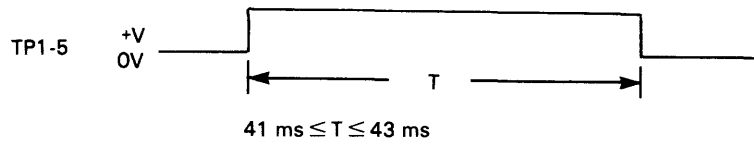


Figure 5-3 Seek Speed Waveform

5.3 SEEK SPEED ADJUSTMENT

Follow these steps to adjust the seek speed circuit.

1. Turn on power to the drive and wait until the RDY LED lights.
2. Trigger the oscilloscope at TP1-5.
3. Perform a repeat seek operation between cylinder 000 and cylinder 691, using either the diagnostic panel (see Appendix C) or the procedure described in Section 3.6.
4. Observe the waveform at TP7.
5. Adjust potentiometer RV1 to achieve a seek start to on-cylinder time of 41 to 43 milliseconds (see Figure 5-3).
6. Check that the voltage at TP3 measures approximately 1.0 volts.
7. Check that the transient response waveform matches the waveform shown in Figure 5-4.

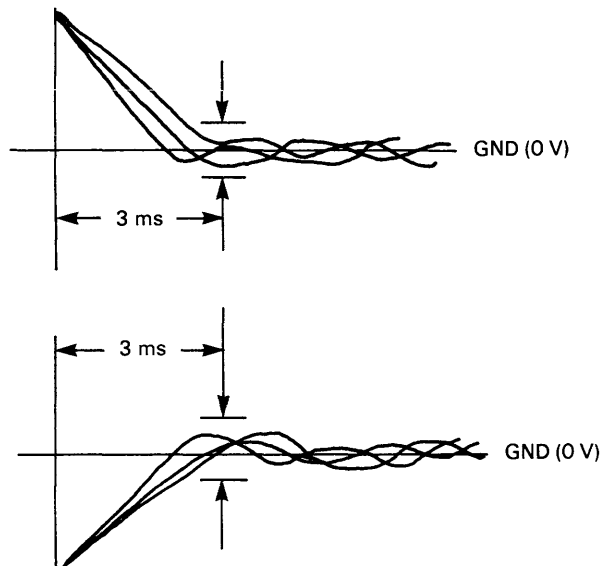


Figure 5-4 Transient Response Waveform

The following adjustment procedures require a diagnostic panel.

8. Perform an increment seek (see Table C-5) from cylinder 000 to cylinder 691.
9. Check that the oscilloscope waveform matches the waveform in Figure 5-5.
10. Repeat the increment seek for two or more sequences, and verify that there are no seek errors.

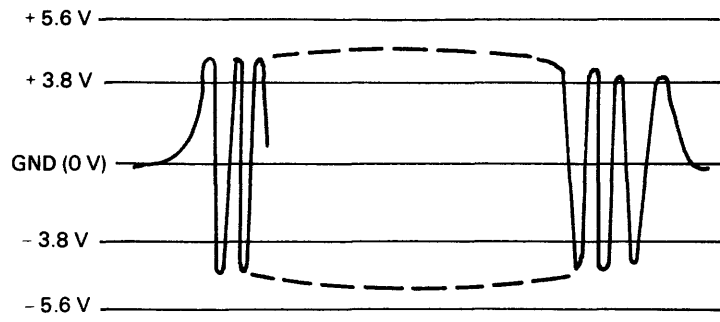
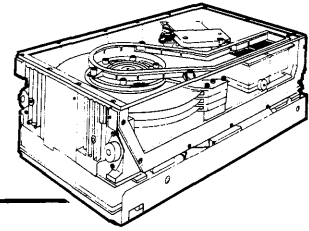


Figure 5-5 Increment Seek (Cylinder 000 to Cylinder 691) Waveform

Chapter 6



Illustrated Parts Breakdown

Figure 6-1 shows the D2246 standard assembly. Figure 6-2 shows the sealed head/disk enclosure with its external parts. Items are described in the accompanying tables.

Table 6-1 D2246 Standard Assembly

ITEM	DESCRIPTION	PART NUMBER	QUANTITY
1	042 Head/Disk Enclosure	134-200313-402	1
2	G9QSQ PCB	134-832951	1
3	G9QSN PCB	134-832949	1
4	G9QST PCB	134-832954	1
5	Air Separator (A)	134-247626-0	1
6	Air Separator (B)	134-248945-0	1
7	Earth Pad Assembly	134-232861-0	1
8	Spring Clamp	134-247779-0	1
9	Board Cover	134-248491-0	1
10	Collar	134-248476-001-0	2
11	Screw	134-248477-0	2
12	Cushion (Rubber)	806-937115-0	4
13	Bracket Frame	134-248488-0	2
14	Bracket Plate	134-247929-0	1
15	150Ω Terminating Resistor	806-921900-521-0	4
16	Head/Disk Enclosure Cable Assembly	134-232842-0	1
17	G9QSN PCB Cable Assembly	134-233133-0	1
18	G9QSQ PCB Cable Assembly	134-233134-0	1
19	Grounding Cable	134-232933-0	1

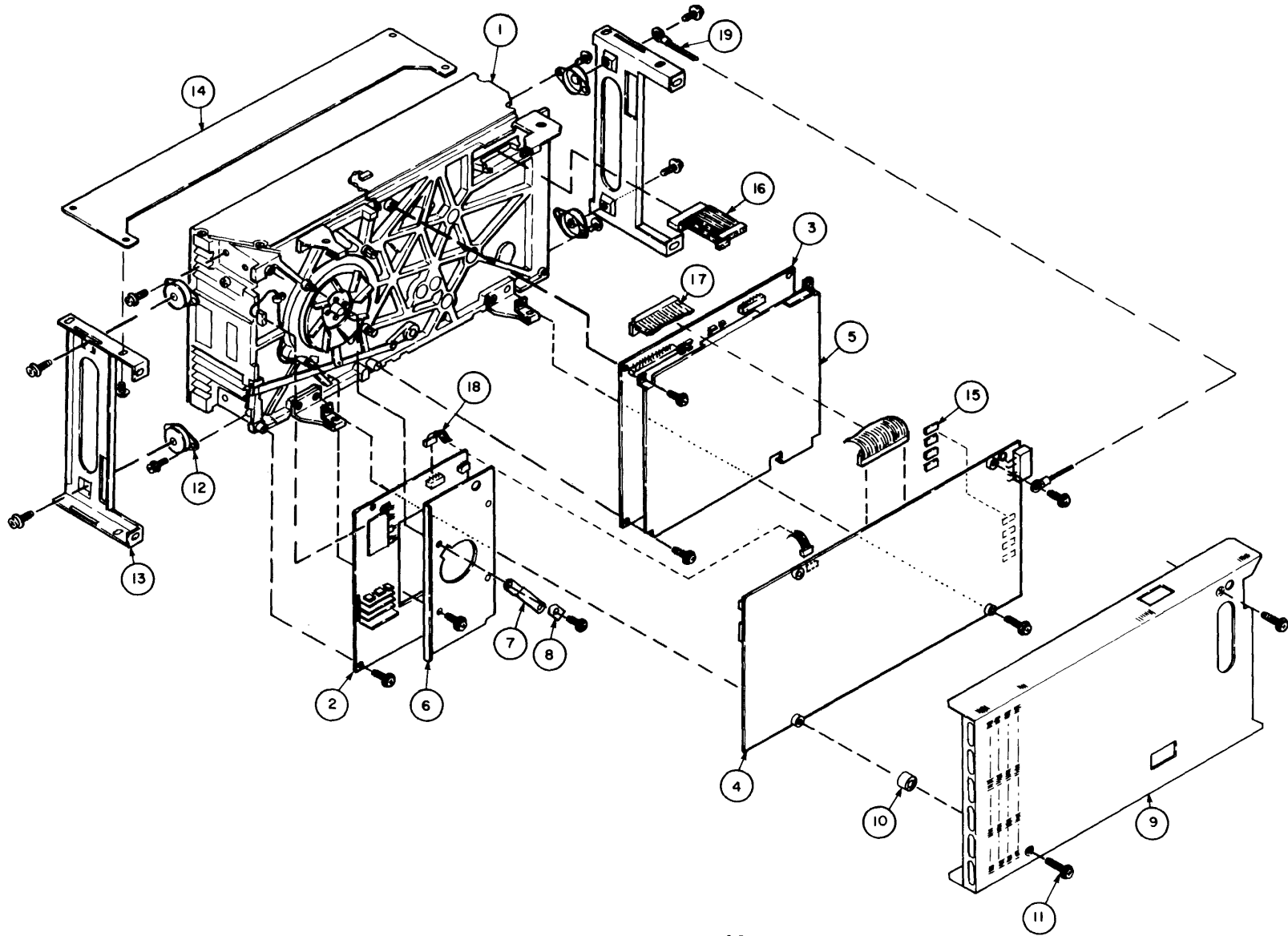


Figure 6-1 D2246 Standard Assembly

Table 6-2 Head/Disk Enclosure External Parts

ITEM	DESCRIPTION	PART NUMBER	QUANTITY
1	042 Head/Disk Enclosure	134-200313-402	1
2	Stator Assembly	806-942281-003-0	1
3	Claw Stopper	134-247662-0	1
4	Rotor	806-942281-002-0	1
5	Motor Shield	134-247782-0	1
6	Fan	134-247663-0	1
7	Pivot Spacer	134-247674-0	1
8	Stopper Link Assembly	134-233039-0	1
9	PCB Support A	134-247619-0	3
10	PCB Support B	134-247620-0	1
11	PCB Guide	134-248516-0	1
12	Stud	134-247621-0	4
13	Cable Clamp	134-248222-0	1
14	Nylon Clip HK-2N	803-070031-002-A	3
15	Nylon Clip HK-3N	803-070031-003-A	2
16	Washer	805-604205-0	4
17	Washer	806-931079-004-0	4
18	E-Ring	803-010001-030-A	1

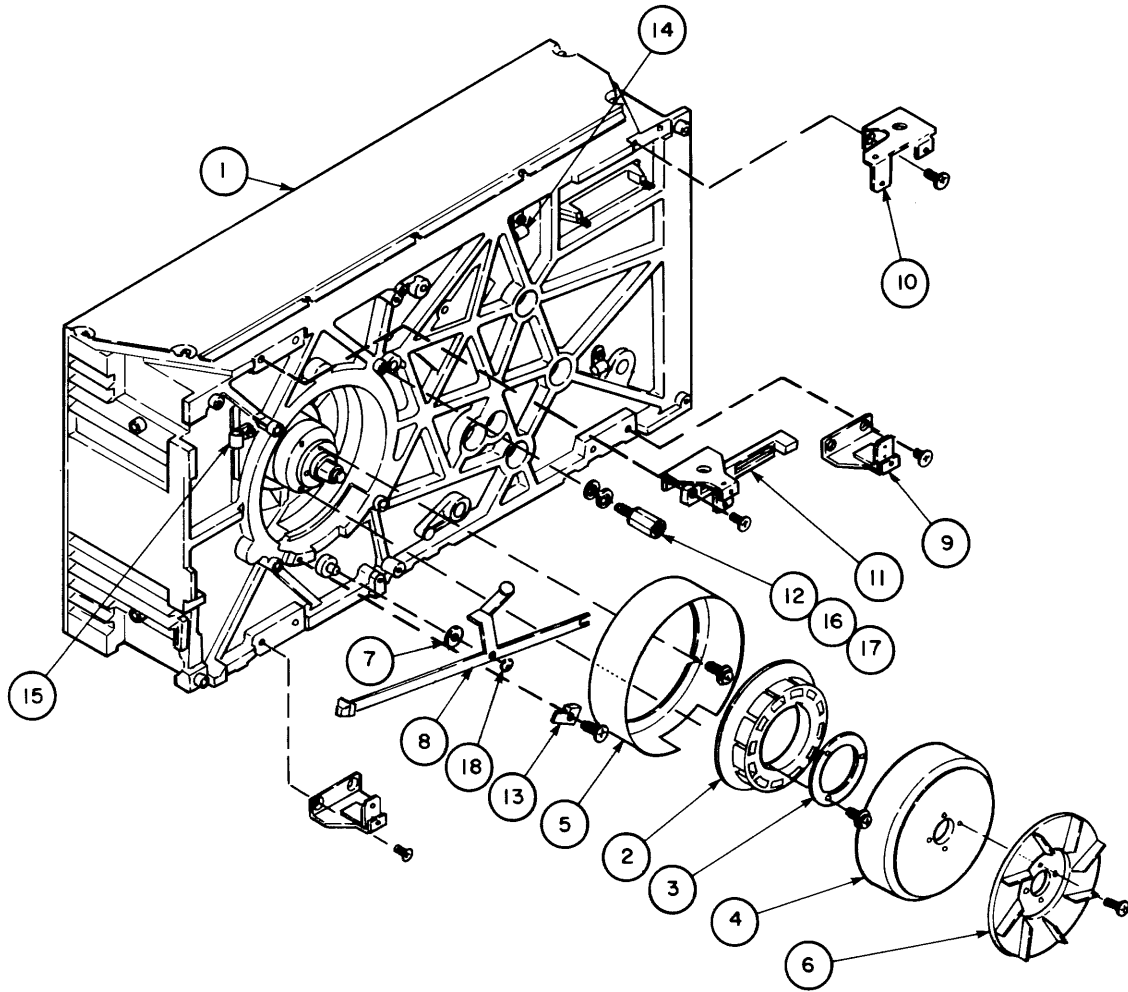
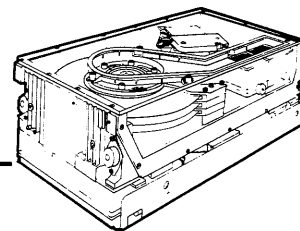


Figure 6-2 Head/Disk Enclosure External Parts

Chapter 7

DKU000-H3PM 3-Input DC Regulator Option



This chapter assumes familiarity with the operation of the 3-Input DC Regulator option. It describes only the regulator's electrical input requirements and its physical dimensions.

7.1 GENERAL DESCRIPTION

The 3-Input DC Regulator requires an input set of three dc voltages: +24V, +5V, and -12V. From this input set, the regulator supplies the power set of dc voltages required by the D2246 disk drive: +24V, +12V, +5V, -5V, and -12V.

The regulator contains an input connector, a signal ground terminal, voltage converters, and an output cable that connects to the D2246 disk drive. The 3-Input DC Regulator is mounted within the D2246 and does not affect its exterior dimensions.

Figure 7-1 diagrams the 3-Input DC Regulator and Figure 7-2 shows its physical dimensions.

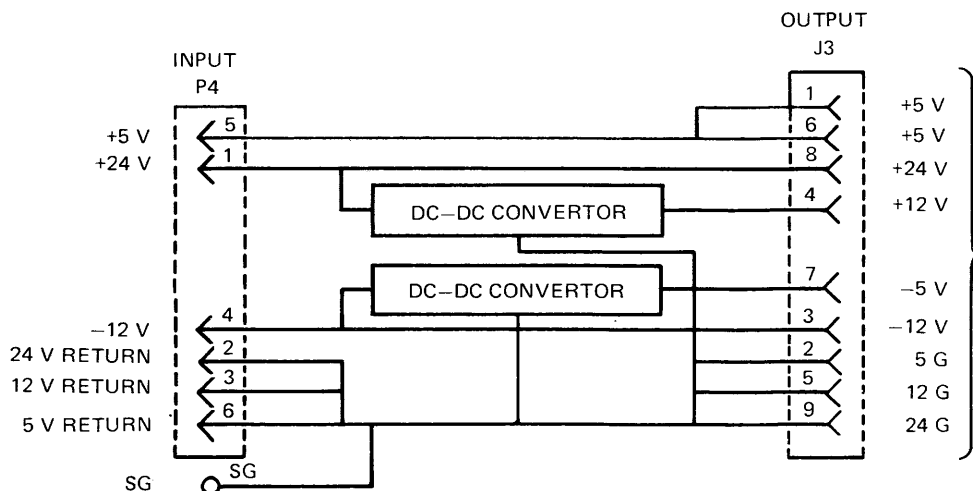


Figure 7-1 3-Input DC Regulator Block Diagram

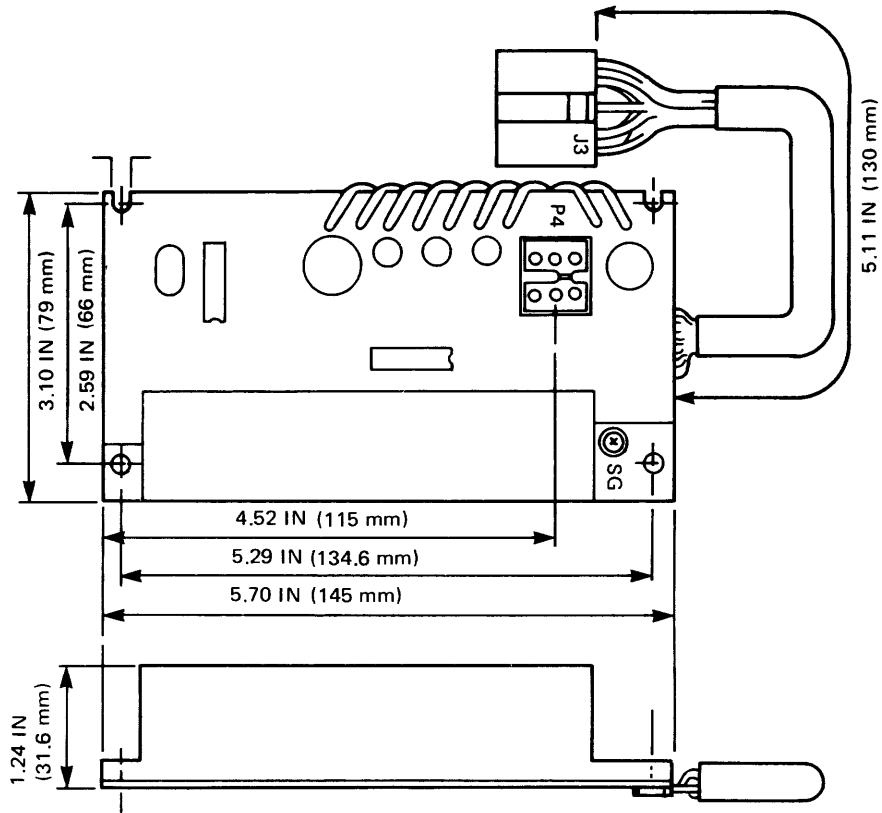


Figure 7-2 3-Input DC Regulator Dimensions

7.2 INTERFACE REQUIREMENTS

The following three sections describe specific interface requirements.

7.2.1 DC Power Connector (P4)

A six-pin AMP connector (No. 1-380999-0) is used for power input. Figure 7-3 shows this connector, and Table 7-1 lists its pin functions.

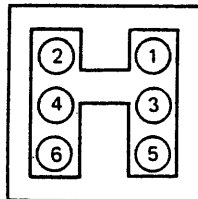


Figure 7-3 P4 Connector

Table 7-1 P4 Pin Assignments

PIN NUMBER	FUNCTION
1	+24 V dc
2	24 V return
3	12 V return
4	-12 V dc
5	+5 V dc
6	5 V return

The recommended mating connector for P4 is described below.

- Cable side housing— AMP P/N 1-480270-0
- Receptacle contact— AMP P/N 60617-4
AMP P/N 60619-4
- Cable wire — No. 18 AWG standard wire

7.2.2 Signal Ground Terminal

The signal grounding wire is connected to the SG terminal. The recommended mating connector for the SG terminal is described below.

- Cable side housing— AMP Plasti-Grip Terminal
- Receptacle contact— AMP P/N 170782-1
- Cable wire — No. 18 AWG standard wire

7.2.3 DC Power Input Requirement

Table 7-2 lists dc input requirements.

Table 7-2 DC Power Requirements

VOLTAGE (VOLTS-DC)	TOLERANCE (+VOLTS-DC)	CURRENT (AMPERES-DC)	RIPPLE (MILLIVOLTS P-P)
+5.0	0.25	4.0	100
-12.0	0.60	1.0	100
+24.0	2.40	3.0 average 5.5 peak	240

7.3 INSTALLING THE 3-INPUT DC POWER REGULATOR

Figure 7-4 shows how to install the regulator.

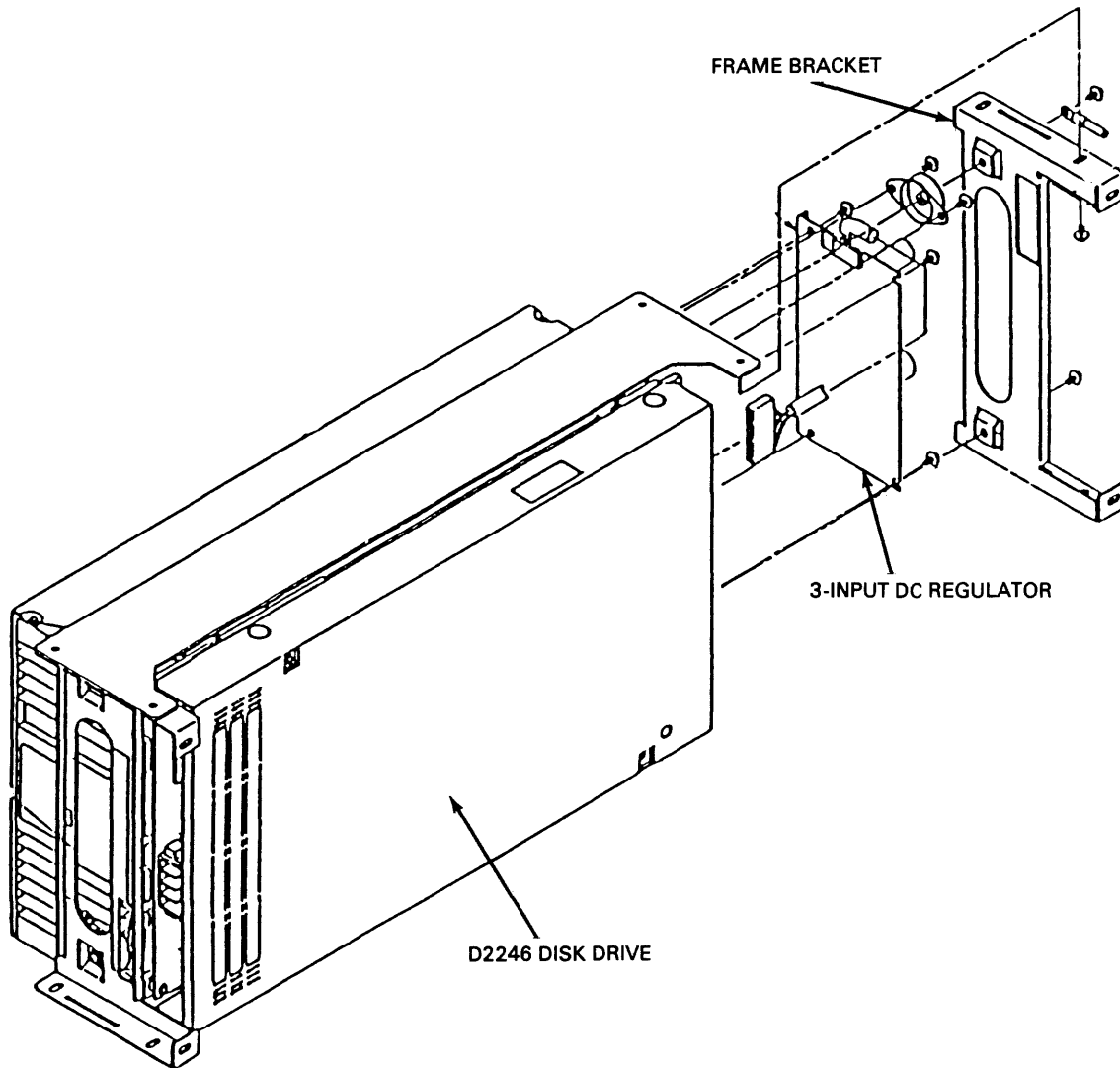
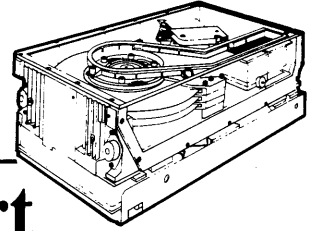


Figure 7-4 Installing the 3-Input DC Regulator

Chapter 8

DKU000-HDP1 Dual-Port Interface Option



This chapter assumes familiarity with the operation of the Dual-Port Interface, and describes only certain of its features.

8.1 GENERAL DESCRIPTION

The Dual-Port Interface allows access to one drive by two controllers. In allowing dual access, the interface functions as a switch that routes the necessary control and data signals to and from the correct controller.

The electrical specifications of the Dual-Port Interface (including line receivers and transmitters, cables and cable connectors, signal definitions, and pin assignments) are the same as those of a standard D2246. The only difference is that D2246 disk drives equipped with this option have two identical interfaces providing communications channels with two controllers.

These two identical interfaces are designated port A and port B. Communication links into and from port A are designated route 0; communication links into and from port B are designated route 1. Each port is physically connected to its controller by an A and a B cable.

Figure 8-1 shows a dual-port cabling diagram.

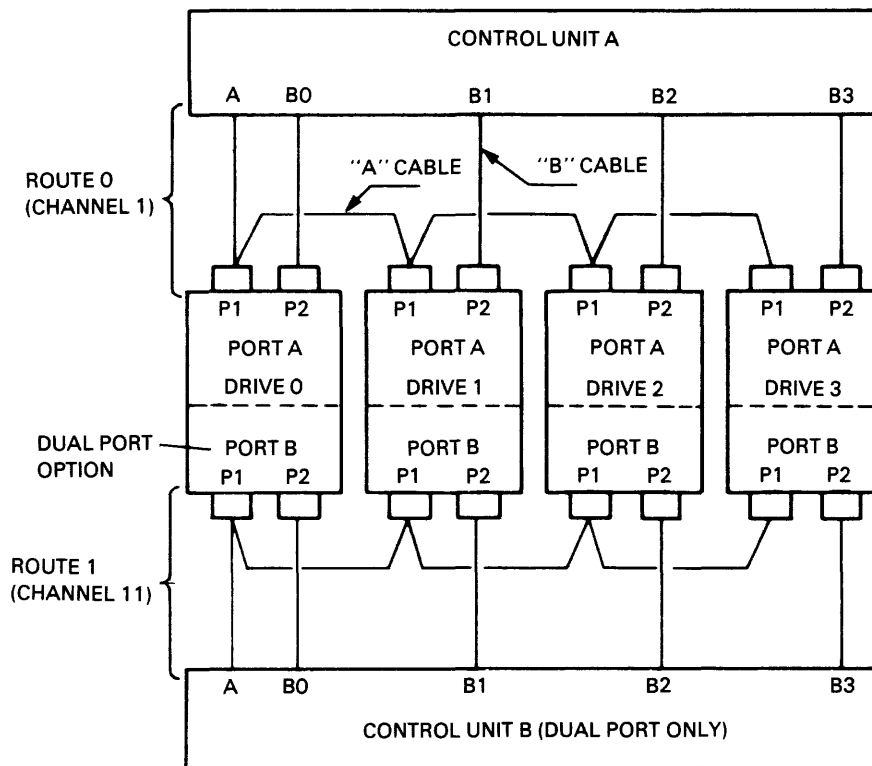


Figure 8-1 Dual-Port System Cabling

8.2 SWITCHES AND INDICATORS

Three switches and four LED indicators located on the interface G9QSW PCB control its functions and provide status information. These switches and indicators are shown in Figure 8-2.

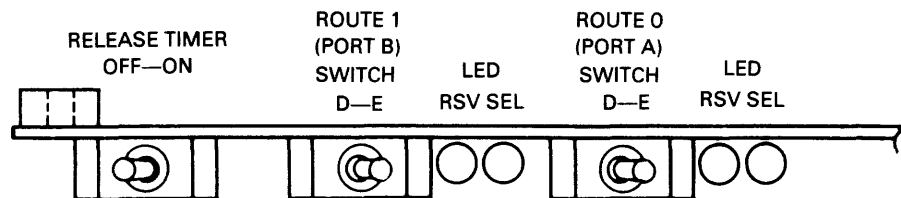


Figure 8-2 Dual-Port Control Switches and Indicators

8.2.1 Port A (Route 0) Switches and Indicators

- Toggle Switch In the “E” (Enable) position, this switch establishes a communications channel (route 0) between the disk drive and a drive controller.
In the “D” (Disable) position, no communications channel is established between the disk drive and the drive controller.
- RSV (LED) When lit, indicates that the D2246 is priority-selected by the route 0 controller.
- SEL (LED) When lit, indicates that the D2246 is selected by the route 0 controller.

8.2.2 Port B (Route 1) Switches and Indicators

- Toggle Switch In the “E” (Enable) position, this switch establishes a communications channel (route 1) between the disk drive and a drive controller.
In the “D” (Disable) position, no communications channel is established between the disk drive and the drive controller.
- RSV (LED) When lit, indicates that the D2246 is priority-selected by the route 1 controller.
- SEL (LED) When lit, indicates that the D2246 is selected by the route 1 controller.

8.2.3 Release Timer: ON/OFF Switch

This switch controls the release timer, a device that allows alternate controller access to the drive. With this switch in the OFF position, a drive remains selected until specifically released by the controller (see Section 8.5.1).

With this switch in the ON position, the release timer automatically manages controller access. Each controller is allowed approximately 500 milliseconds of disk time. After that period, the communications channel is disabled and drive access is granted to the other controller.

8.3 DRIVE SELECTION

Drive selection is controlled by the G9QSW PCB on the Dual-Port Interface. When no controller has the drive reserved, the drive is available and can be selected or reserved by either controller. The interface recognizes and engages with the first controller to complete a drive selection. The drive is reserved by the selecting controller, and remains reserved until a Release signal, a release timer function, or a dc power-down occurs.

If the drive is already reserved or selected, a Busy signal is issued on cable A of the controller attempting the select. This Busy signal is issued within 600 ns of the selection attempt and remains until the drive is no longer reserved or selected.

8.4 INTERFACE

The dual-port read/write cable (cable B) is identical to the standard D2246 cable B. The dual-port control cable (cable A), however, provides one additional status line. This line, Busy, issues a status response to a controller attempting to select a reserved or selected drive.

8.5 STATUS COMMANDS

The Dual-Port Interface provides two additional status commands.

8.5.1 Release Command

This command (bus bit 9 and Tag 3) is transmitted to the drive from the controller. It releases controller reserve and priority select, freeing the drive for use by the other controller.

8.5.2 Priority Select

The Priority Select signal (bus bit 9, Unit Select lines, and Unit Select Tag) is issued by a controller. This signal forces the drive to become unconditionally selected and absolutely reserved by the controller issuing the Priority Select signal. While this signal is active, the second controller is denied access to the drive. A Priority Select signal is not disabled by the release timer function.

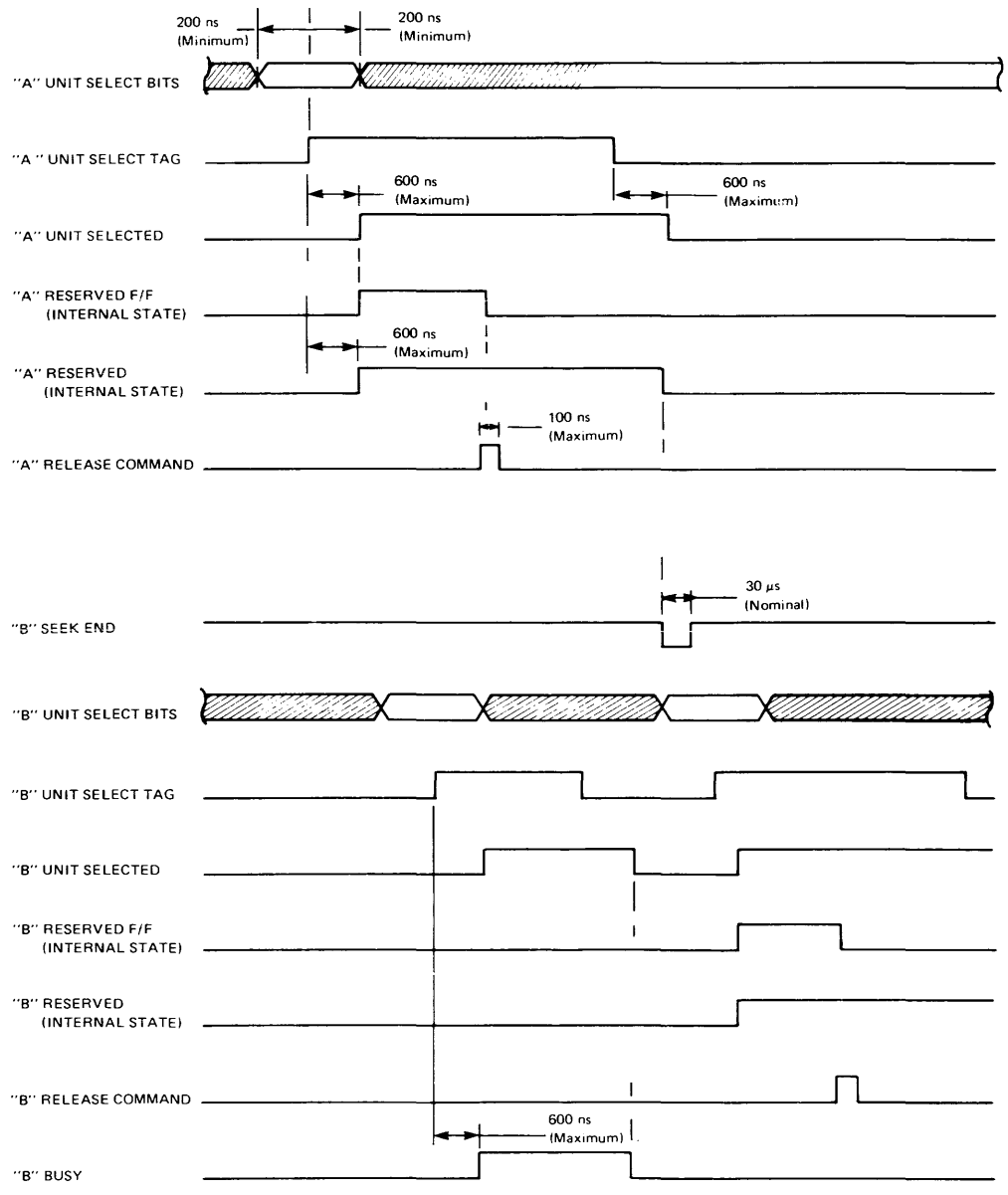


Figure 8-3 Unit Select Timing for Dual-Port Option

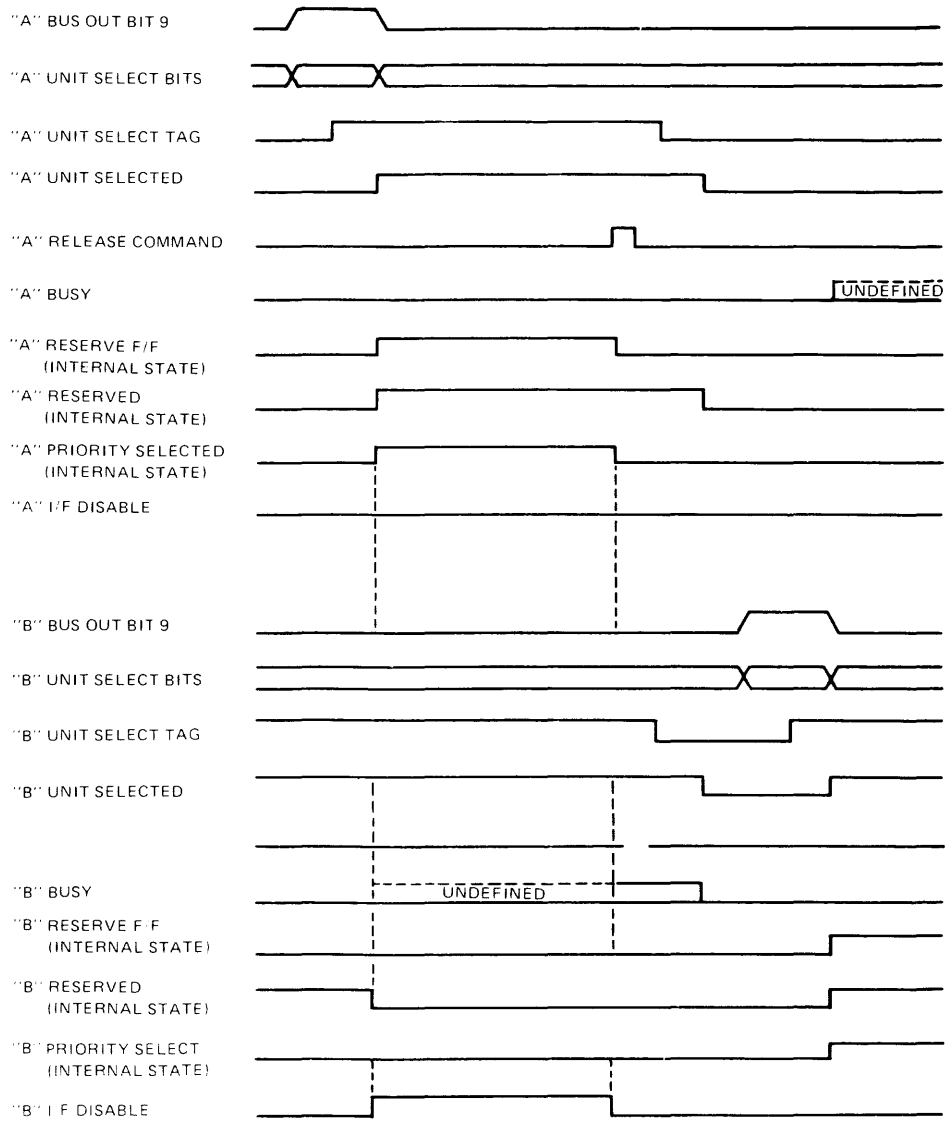


Figure 8-4 Sample Priority Select Timing

8.6 INSTALLING THE DUAL-PORT INTERFACE

Figure 8-5 shows how to install the interface.

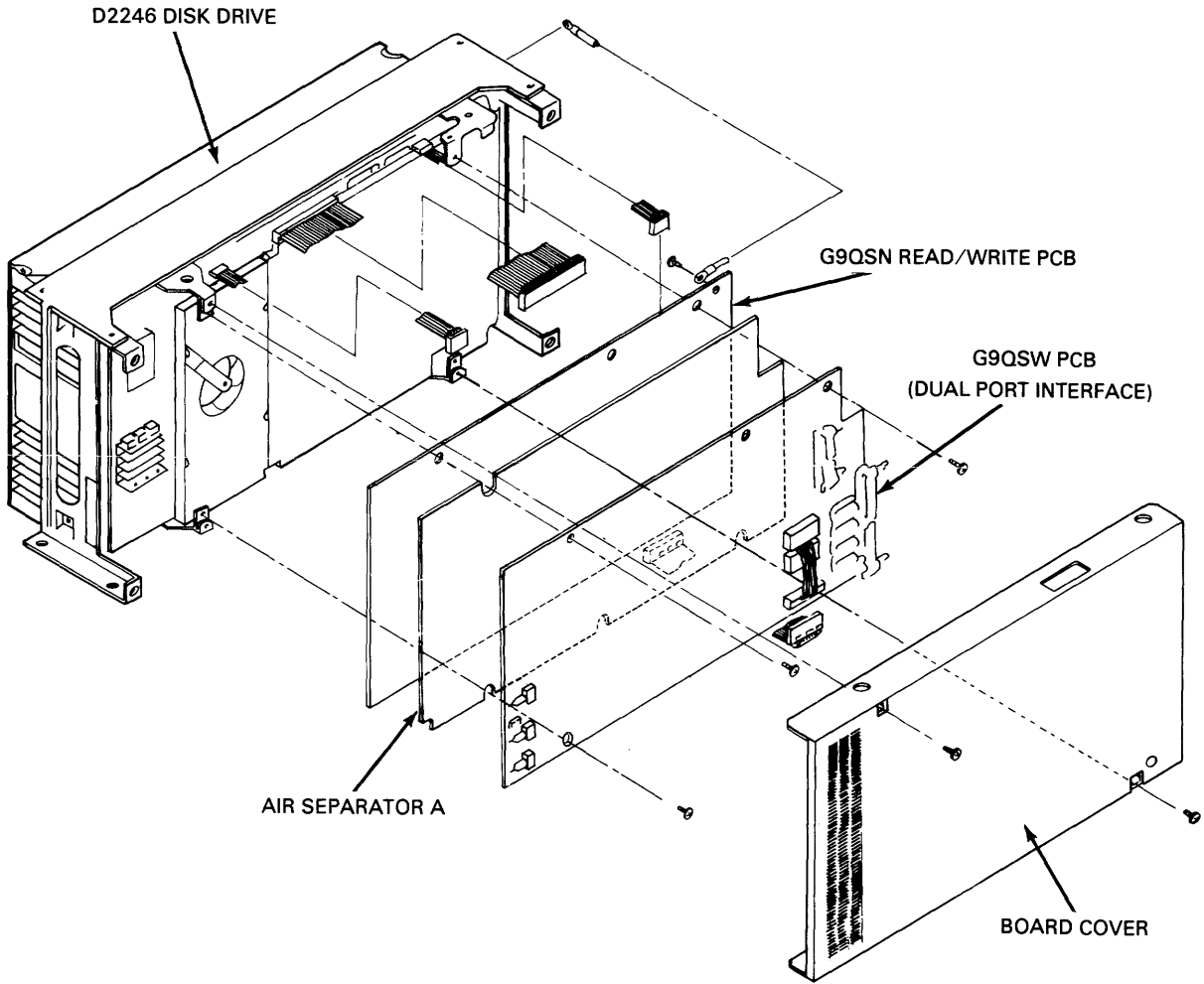
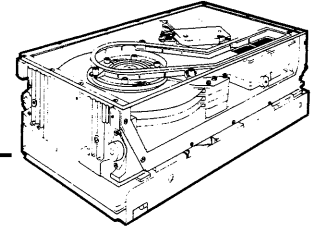


Figure 8-5 Installing the Dual-Port Interface

Appendix A

Schematic Diagrams



This Appendix includes the logic diagrams and schematics for each PCB in the D2246 disk drive. It also includes drawings illustrating the interface and cable connections between PCBs and the signal pin assignments for each connector.

A.1 SIGNAL TRACING SCHEME

The signal tracing scheme provides the ability to easily trace a signal from source to destination within the D2246 logic. Each individual drawing contains, in its lower right-hand corner, a page number, an identifier, and a drawing number as shown in Figure A-1.

Figure A-1 also shows the horizontal/vertical coordinates that are used to locate and identify a signal upon a specific page.

A.2 DRAWINGS

Table A-1 lists the drawings contained in this Appendix along with their drawing numbers.

Table A-1 Schematic Drawings

DIAGRAM	DRAWING NUMBER
I/O Connectors	134-296076-021
Interface and Power Connectors	134-296076-022
Head/Disk Assembly Internal Cabling Diagram	134-296076-011
Internal Cabling Diagram	134-296076-012
Route 0 (Port A) Interface	134-296077-051
Route 1 (Port B) Interface	134-296077-052
G9QSW PCB Schematic	134-296077-101/111
G9QST PCB Schematic	134-296077-201/226
G9QSN PCB Schematic	134-296077-301/309
G9QSQ PCB Schematic	134-296077-401/403
Head/Disk Assembly and Motor Circuit Diagram	134-296077-501
G9MRY PCB Schematic	134-296077-601

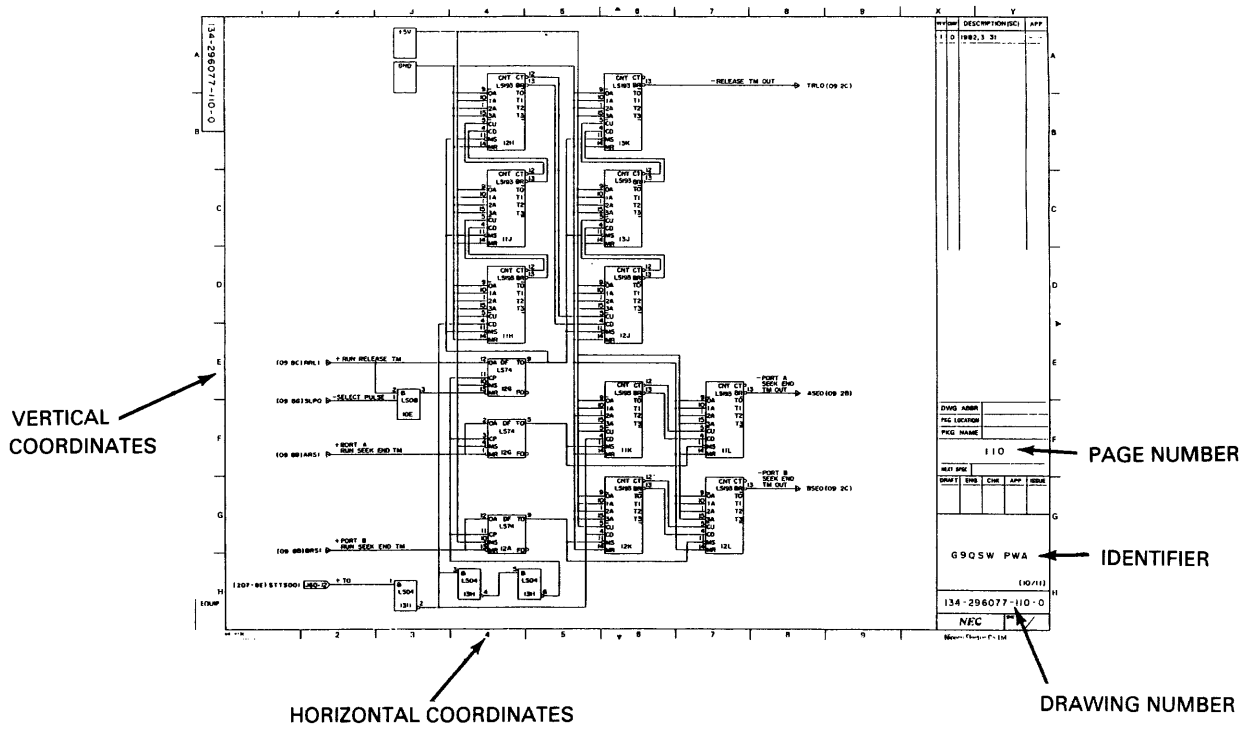
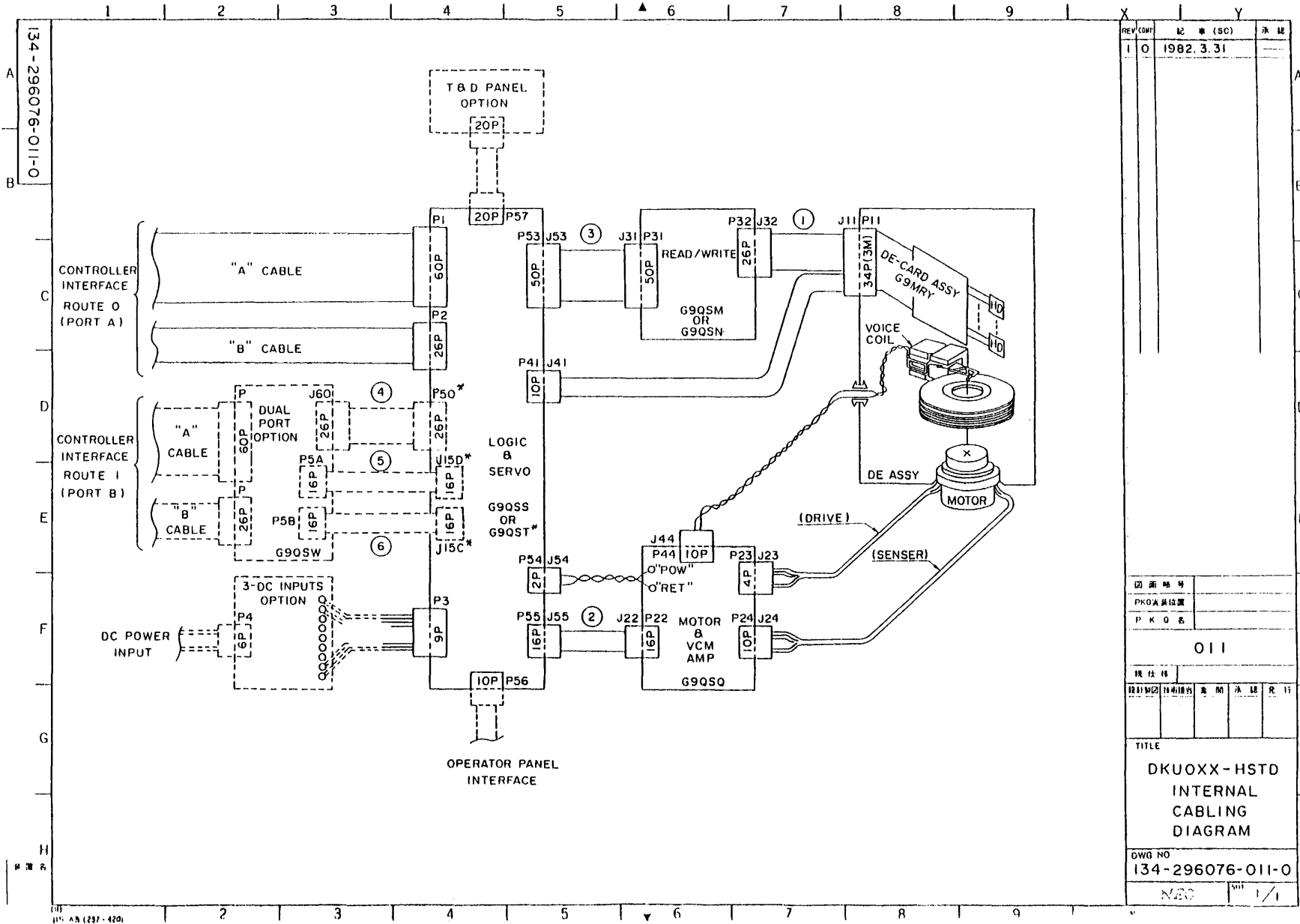


Figure A-1 Schematic Format



REV	COM	記 号 (SC)	承認
1	0	1982.3.31	

図 面 略 号	
PKO 実 装 位 置	
P K O 名	
011	
機 仕 様	
設 計 部 門	機 械 部 門
製 作 部 門	電 機 部 門
検 査 部 門	保 修 部 門
TITLE	
DKUOXX-HSTD INTERNAL CABLING DIAGRAM	
DWG NO	
134-296076-011-0	
製 作	1/1

134-296076-012-0

G9QST PWA (4)		G9QSW PWA	
J50	J60	J50	J60
(217-6F) 1	+5V	25	(111-2F1)
(217-6G) 2	+5V	25	(111-2F1)
(217-6G) 2	+5V	25	(111-2F1)
(217-6E) 15	+10	12	(110-2F1)
(217-6G) 3	-5V	24	(111-2H1)
(217-6H) 16	-5V	11	(111-2H1)
(217-80) 4	GROUND	23	(111-2F1)
(217-80) 17	GROUND	10	(111-2G1)
(217-80) 5	GROUND	22	(111-2G1)
(217-80) 18	GROUND	9	(111-2G1)
(202-7F) 6	+BUS OUT BIT 0	21	(102-8G1)
(202-7E) 7	+BUS OUT BIT 1	8	(102-8F1)
(202-7E) 7	+BUS OUT BIT 2	20	(102-8F1)
(202-7E) 20	+BUS OUT BIT 3	7	(102-8F1)
(202-7C) 21	+BUS OUT BIT 4	19	(102-8D1)
(202-7C) 21	+BUS OUT BIT 5	6	(102-8D1)
(202-7C) 9	+BUS OUT BIT 6	18	(102-8D1)
(202-7C) 22	+BUS OUT BIT 7	5	(102-8D1)
(202-7C) 10	+BIO / INDEX	17	(102-8C1)
(205-8H) 23	+B11 / SECTOR	4	(104-2E1)
(205-8H) 11	+B12 / FAULT	16	(104-2D1)
(205-8H) 24	+B13 / SEEK ERROR	3	(104-2D1)
(205-8C) 12	+B14 / ON CYLINDER	15	(104-2C1)
(205-8G) 25	+B15 / UNIT READY	2	(104-2C1)
(205-8G) 13	+B16 / ADDRESS MARK FOUND	14	(104-2B1)
(205-8G) 26	+B17 / WRITE PROTECT	1	(104-2A1)
(26P)		(26P)	
G9QST PWA (5)		G9QSW PWA	
P15D	P15A	P15D	P15A
(207-8A) 1	+PORT A BUS OUT BIT 9	1	(107-2F1)
(207-2A) 16	+BUS OUT BIT 9	16	(107-8F1)
(207-8A) 2	+PORT A BUS OUT BIT 8	2	(107-2F1)
(207-8A) 13	+BUS OUT BIT 8	13	(107-8F1)
(207-2A) 3	+PORT A COMPARED	12	(107-8F1)
(207-8B) 14	+PORT A SELECTED	3	(107-2A1)
(207-2B) 4	+SEEK END	4	(107-8G1)
(207-8C) 13	+PORT A SEEK END	13	(109-2A1)
(207-2C) 5	+PORT A WRITE DATA	5	(109-8A1)
(207-8B) 12	+WRITE DATA	12	(107-2F1)
(207-2B) 6	GROUND	6	(111-2G1)
(207-8C) 11	+BUSY	11	(108-8H1)
(207-2C) 7	+PORT A WRITE CLOCK	7	(107-2G1)
(207-8B) 10	+WRITE CLOCK	10	(107-8F1)
(204-8F) 8	-PORT A/B DISABLE	8	(109-2H1)
(204-2G) 9	-PORT A DISABLE	9	(106-8H1)
(16P)		(16P)	
G9QST PWA (6)		G9QSW PWA	
P15C	P15B	P15C	P15B
(203-6B) 1	-TAG 1	1	(103-8A1)
(203-6B) 16	-TAG 2	16	(103-8A1)
(203-6C) 12	-TAG 3	12	(103-8A1)
(203-6C) 15	-TAG 4	15	(103-8A1)
(204-6G) 3	+PORT A SEL INH	3	(103-8A1)
(203-2F) 14	-HOLD	14	(106-2G1)
(204-8D) 4	[SPARE]	4	(105-8F1)
(207-8D) 13	+INDEX	13	(105-2E1)
(204-8C) 5	+UNIT AD SW 3	5	(106-2B1)
(207-8E) 12	+SECTOR	12	(105-2E1)
(204-8C) 6	+UNIT AD SW 2	6	(106-2B1)
(207-8D) 11	+SERVO CLOCK	11	(109-2E1)
(204-8C) 7	+UNIT AD SW 1	7	(106-2D1)
(207-8D) 10	-READ DATA	10	(105-2C1)
(204-8D) 8	+UNIT AD SW 0	8	(106-2B1)
(207-8D) 9	-READ CLOCK	9	(105-2C1)
(16P)		(16P)	

DUAL PORT OPTION

G9QSS / G9QST PWA (3)		G9QSM / G9QSN PWA	
J53	J31	J53	J31
(217-8A) 1	GROUND	50	(309-2H1)
(217-6F) 26	+5V	25	(309-2G1)
(217-6F) 2	GROUND	49	(309-2G1)
(217-6F) 27	+5V	24	(309-2G1)
(217-6F) 3	GROUND	48	(309-2G1)
(217-6G) 28	-5V	23	(309-2H1)
(217-8A) 4	GROUND	47	(309-2F1)
(217-6G) 29	-12V	22	(309-2F1)
(217-8B) 5	GROUND	46	(309-2F1)
(217-6G) 30	-12V	21	(309-2F1)
(217-8B) 6	GROUND	45	(309-2E1)
(217-6C) 31	+12V	20	(309-2D1)
(217-8B) 7	GROUND	44	(309-2D1)
(217-6C) 32	+12V	19	(309-2D1)
(217-8B) 8	GROUND	43	(309-2E1)
(213-8D) 33	+HEAD SELECT 1	18	(309-2B1)
(213-8D) 34	+HEAD SELECT 0	17	(309-2B1)
(213-8C) 10	+CHIP SELECT 1 (NU)	17	(309-2B1)
(213-8C) 35	+CHIP SELECT 0	16	(309-2C1)
(213-8C) 11	GROUND	40	(309-2D1)
(212-8B) 36	+WRITE PROTECT	15	(309-2D1)
(212-8D) 12	-WRITE GATE	39	(308-2D1)
(212-8D) 37	GROUND	14	(301-2C1)
(212-8D) 13	+MARS UNSAFE	38	(308-9G1)
(208-2D) 38	+MARS UNSAFE!	13	(308-9F1)
(208-2E) 14	GROUND	37	(308-9G1)
(213-2A) 39	+SEPARATED READ DATA	12	(309-2H1)
(213-2A) 15	GROUND	36	(305-2H1)
(213-2B) 40	+READ CLOCK	11	(305-9E1)
(213-2B) 16	GROUND	35	(305-9E1)
(212-2B) 41	-DATA STROBE EARLY	10	(305-2E1)
(212-2A) 17	-DATA STROBE LATE	9	(305-2E1)
(212-8C) 42	GROUND	9	(304-2D1)
(212-8B) 18	+READ GATE	35	(303-2F1)
(212-2C) 43	+LOCK READ PLO	8	(305-2A1)
(217-8C) 19	GROUND	34	(304-2D1)
(212-8F) 20	+BIT CLOCK	31	(304-2F1)
(212-8F) 45	-WRITE CLOCK 2F	6	(301-2B1)
(212-9E) 21	GROUND	30	(301-2D1)
(212-8C) 46	+WRITE DATA	3	(301-2D1)
(212-8D) 22	GROUND	29	(301-2D1)
(212-8D) 47	+WRITE CLACK	4	(301-2D1)
(212-8D) 23	GROUND	28	(301-2E1)
(212-8B) 48	+AM ENABLE	3	(301-2E1)
(208-2E) 24	+AM FOUND	2	(303-9C1)
(212-8C) 49	GROUND	2	(301-2H1)
(212-8E) 25	-PAD IN PROGRESS OR NOT ALLOW WRITE	26	(301-2F1)
(212-8C) 50	GROUND	25	(301-2G1)
(50P)		(50P)	

DE ASSY (G9LDR PWB) (1)		G9QSS / G9QST PWA	
J11	J41	J55	J22
(601-2G) 1	-B2V	10	(218-9D)
(601-2H) 18	-B2V	5	(218-9D)
(601-2H) 2	GROUND	9	(218-9E)
(601-2H) 19	GROUND	4	(218-9E)
(601-2G) 3	SERVO SIGNAL B	8	(218-9C)
(601-2G) 20	GROUND	3	(218-1B)
(601-2G) 4	SERVO SIGNAL A	7	(218-1B)
(601-2F) 21	GROUND (NU)	2	(218-1B)
(601-2F) 5	GROUND (NU)	6	(218-9D)
(601-2F) 22	GROUND (NU)	1	(218-9C)
(10P)			
G9QSM / G9QSN PWA		G9QSS / G9QST PWA	
J32	J41	J55	J22
(601-2F) 6	-LC CHIP SELECT 2	2	(309-9D)
(601-2C) 23	-LC CHIP SELECT 1	15	(309-9C)
(601-2E) 7	-LC CHIP SELECT 0	3	(309-9C)
(601-2D) 24	GROUND	16	(309-9E)
(601-2D) 8	-LC HEAD SELECT 1	4	(309-9B)
(601-2D) 25	GROUND	17	(309-9E)
(601-2D) 9	-LC HEAD SELECT 0	5	(309-9B)
(601-2D) 26	GROUND	16	(309-9F)
(601-2D) 10	-4V	6	(308-9H)
(601-2C) 19	GROUND	19	(309-9F)
(601-2C) 27	GROUND	6	(308-9H)
(601-2C) 11	+5V	7	(309-9F)
(601-2C) 28	GROUND	20	(308-9E)
(601-2D) 12	UNSAFE	8	(309-9F)
(601-2E) 29	GROUND	21	(308-9G)
(601-2D) 13	WRITE CURRENT	5	(309-9F)
(601-2D) 30	GROUND	22	(308-9D)
(601-2E) 14	WRITE SELECT	10	(309-9F)
(601-2A) 31	GROUND	23	(308-9C)
(601-2E) 15	GROUND	11	(309-9G)
(601-2F) 32	GROUND	24	(309-9C)
(601-2F) 16	R/W DATA X	12	(307-2B)
(601-2B) 33	GROUND	25	(307-2B)
(601-2B) 17	R/W DATA Y	13	(307-2C)
(601-2B) 34	GROUND	26	(307-2B)
(34P)		(26P)	
G9QSS / G9QST PWA (2)		G9QSQ PWA	
J55	J22	J55	J22
(223-9E) 1	GROUND	16	(403-2G)
(223-9E) 9	-OUT DRIVE	6	(403-2F)
(226-9E) 2	GROUND	15	(402-1H)
(226-9E) 10	+5V	7	(402-1G)
(226-9E) 3	GROUND	14	(402-1G)
(226-9D) 11	-12V	6	(402-1G)
(226-9D) 4	GROUND	13	(402-1G)
(226-9D) 12	+12V	5	(402-1F)
(226-6G) 5	-SPEED PULSE	12	(401-9B)
(226-6F) 13	+SPEED PULSE POWER	4	(401-9B)
(226-9F) 6	-START MOTOR	11	(401-2H)
(226-9F) 14	+ZEND MODE	3	(403-2C)
(221-1F) 7	GROUND	10	(403-9H)
(221-1F) 8	-CURRENT SENSE	2	(403-9H)
(221-1F) 16	+CURRENT SENSE	9	(403-9G)
(221-1F) 1	GROUND	1	(403-9G)
(16P)		(16P)	

REV	DATE	DESCRIPTION (SC)	APP
1	0	1982.3.31	
DWG ABBR			
PKG LOCATION			
PKG NAME			
012			
NEXT SPEC			
DRAFT	ENG	CHK	APP
ISSUE			
INTERNAL CABLING DIAGRAM			
134-296076-012-0			
NEC			

134-296077-051-0

A-5

"A" CABLE INTERFACE

PIN NO.	FUNCTION	NAME	JUMP LOCATION
1	YSOTG1Z		203-2A
31	YSOTG1Y	TAG 1	203-2A
2	YSOTG2Z		203-2B
32	YSOTG2Y	TAG 2	203-2B
3	YSOTG3Z		203-2C
33	YSOTG3Y	TAG 3	203-2C
4	YSOBT0Z		202-2H
34	YSOBT0Y	BUS OUT BIT 0	202-2H
5	YSOBT1Z		202-2H
35	YSOBT1Y	BUS OUT BIT 1	202-2H
6	YSOBT2Z		202-2G
36	YSOBT2Y	BUS OUT BIT 2	202-2G
7	YSOBT3Z		202-2F
37	YSOBT3Y	BUS OUT BIT 3	202-2F
8	YSOBT4Z		202-2F
38	YSOBT4Y	BUS OUT BIT 4	202-2F
9	YSOBT5Z		202-2E
39	YSOBT5Y	BUS OUT BIT 5	202-2E
10	YSOBT6Z		202-2D
40	YSOBT6Y	BUS OUT BIT 6	202-2D
11	YSOBT7Z		202-2D
41	YSOBT7Y	BUS OUT BIT 7	202-2D
12	YSOBT8Z		202-2C
42	YSOBT8Y	BUS OUT BIT 8	202-2C
13	YSOBT9Z		202-2C
43	YSOBT9Y	BUS OUT BIT 9	202-2C
14	YSOOC0Z		202-2G
44	YSOOC0Y	OPEN CABLE DETECT	202-2G
15	YSOBI2Z		205-8E
45	YSOBI2Y	BUS IN BIT 2 (FAULT)	205-8E

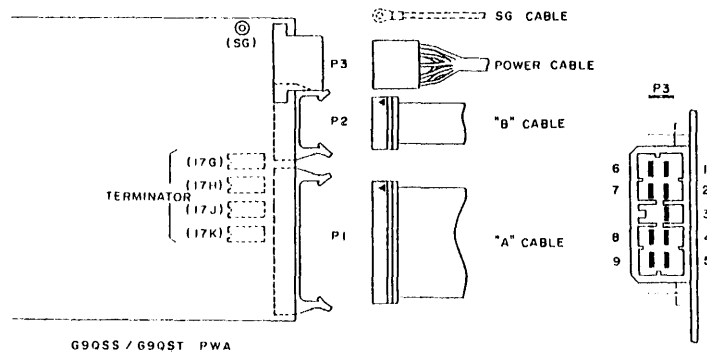
PIN NO.	FUNCTION	NAME	JUMP LOCATION
16	YSOBI3Z		205-8D
46	YSOBI3Y	BUS IN BIT 3 (SEEK ERROR)	205-8D
17	YSOBI4Z		205-8D
47	YSOBI4Y	BUS IN BIT 4 (ON CYLINDER)	205-8D
18	YSOBI0Z		205-8F
48	YSOBI0Y	BUS IN BIT 0 (INDEX)	205-8F
19	YSOBI5Z		205-8C
49	YSOBI5Y	BUS IN BIT 5 (UNIT READY)	205-8C
20	YSOBI6Z		205-8B
50	YSOBI6Y	BUS IN BIT 6 (ADDRESS MARK FOUND)	205-8B
21	YSOBSYZ		206-8B
51	YSOBSY	BUSY	206-8B
22	YSOUSTZ		201-2F
52	YSOUSTY	UNIT SELECT TAG	201-2F
23	YSOUS0Z		201-2E
53	YSOUS0Y	UNIT SELECT 2 ⁰	201-2E
24	YSOUS1Z		201-2D
54	YSOUS1Y	UNIT SELECT 2 ¹	201-2D
25	YSOBI1Z		205-8F
55	YSOBI1Y	BUS IN BIT 1 (SECTOR)	205-8F
26	YSOUS2Z		201-2C
56	YSOUS2Y	UNIT SELECT 2 ²	201-2C
27	YSOUS3Z		201-2B
57	YSOUS3Y	UNIT SELECT 2 ³	201-2B
28	YSOBI7Z		205-8B
58	YSOBI7Y	BUS IN BIT 7 (WRITE PROTECT)	205-8B
29	(YKSPCKO)	(POWER SEQUENCE PICK)	203-2F
59	YKSHLDO	POWER SEQUENCE HOLD	203-2F
30	YSOTG4Z		203-2D
60	YSOTG4Y	TAG 4	203-2D

"B" CABLE INTERFACE

PIN NO.	FUNCTION	NAME	JUMP LOCATION
1	X000	GROUND	206-8G
14	YSOSCKY	SERVO CLOCK	206-8B
2	YSOSCKZ		206-8B
15	X000	GROUND	206-8G
3	YSORDTZ		206-8C
16	YSORDTY	READ DATA	206-8C
4	X000	GROUND	206-8G
17	YSORCKY		206-8D
5	YSORCKZ	READ CLOCK	206-8C
18	X000	GROUND	206-8G
6	YSOWCKZ		202-2B
19	YSOWCKY	WRITE CLOCK	202-2A
7	X000	GROUND	206-8G
20	YSOWDTY		202-2A
8	YSOWDTZ	WRITE DATA	202-2A
21	X000	GROUND	206-8G
9	YSOUSDZ		206-8D
22	YSOUSDY	UNIT SELECTED	206-8D
10	YSOSKDZ		206-8E
23	YSOSKDY	SEEK END	206-8E
11	X000	GROUND	206-8G
24	YSOINXZ		206-8E
12	YSOINXZ	INDEX	206-8F
25	X000	GROUND	206-8H
13	YSOSECZ		206-8F
26	YSOSECY	SECTOR	206-8F

POWER INTERFACE

PIN NO.	VOLTAGE	JUMP LOCATION
9	+24V RETURN	217-2E
8	+24V	217-2E
7	-5V	217-2B
6	+5V	217-2A
5	GND	217-2C
4	+12V	217-2C
3	-12V	217-2D
2	GND	217-2B
1	+5V	217-2A



REV	COMP	DESCRIPTION (ISC)	APP
1	0	1982.3.31	

DWG ABBR				
PKG LOCATION				
PKG NAME	O51			
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
ROUTE 0 (PORT A) INTERFACE				
134-296077-051-0				
NEC				5/1

EQUIP

100 4130
06 81 1020-0410

Minom Electric Co Ltd

134-296077-052-0

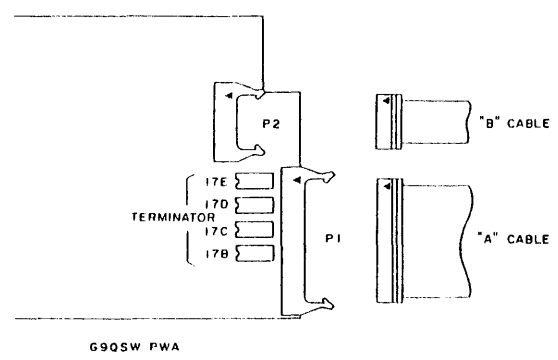
"A" CABLE INTERFACE

PIN NO.	FUNCTION	NAME	JUMP LOCATION
1	YSITG1Z	TAG 1	103-2A
31	YSITG1Y		103-2A
2	YSITG2Z	TAG 2	103-2B
32	YSITG2Y		103-2B
3	YSITG3Z	TAG 3	103-2C
33	YSITG3Y		103-2C
4	YSIBTOZ	BUS OUT BIT 0	102-2H
34	YSIBTOY		102-2H
5	YSIBTIZ	BUS OUT BIT 1	102-2H
35	YSIBTIY		102-2G
6	YSIBT2Z	BUS OUT BIT 2	102-2G
36	YSIBT2Y		102-2G
7	YSIBT3Z	BUS OUT BIT 3	102-2F
37	YSIBT3Y		102-2F
8	YSIBT4Z	BUS OUT BIT 4	102-2F
38	YSIBT4Y		102-2E
9	YSIBT5Z	BUS OUT BIT 5	102-2E
39	YSIBT5Y		102-2E
10	YSIBT6Z	BUS OUT BIT 6	102-2D
40	YSIBT6Y		102-2D
11	YSIBT7Z	BUS OUT BIT 7	102-2D
41	YSIBT7Y		102-2C
12	YSIBT8Z	BUS OUT BIT 8	102-2C
42	YSIBT8Y		102-2C
13	YSIBT9Z	BUS OUT BIT 9	102-2C
43	YSIBT9Y		102-2D
14	YSIOCDZ	OPEN CABLE DETECT	101-2G
44	YSIOCDY		101-2G
15	YSIB12Z		BUS IN BIT 2
45	YSIB12Y	(FAULT)	104-8E

PIN NO.	FUNCTION	NAME	JUMP LOCATION
16	YSIDI3Z	BUS IN BIT 3 (SEEK ERROR)	104-8D
46	YSIB13Y		104-8D
17	YSIB14Z	BUS IN BIT 4 (ON CYLINDER)	104-8D
47	YSIB14Y		104-8C
18	YSIB10Z	BUS IN BIT 0 (INDEX)	104-8F
48	YSIB10Y		104-8F
19	YSIB15Z	BUS IN BIT 5 (UNIT READY)	104-8C
49	YSIB15Y		104-8C
20	YSIB16Z	BUS IN BIT 6 (ADDRESS MARK FOUND)	104-8B
50	YSIB16Y		104-8B
21	YSIBSYZ	BUSY	105-8B
51	YSIBSY Y		105-8A
22	YSIUSTZ	UNIT SELECT TAG	101-2F
52	YSIUSTY		101-2E
23	YSIUS0Z	UNIT SELECT 2 ⁰	101-2E
53	YSIUS0Y		101-2D
24	YSIUS1Z	UNIT SELECT 2 ¹	101-2D
54	YSIUS1Y		101-2C
25	YSIB11Z	BUS IN BIT 1 (SECTOR)	104-8F
55	YSIB11Y		104-8E
26	YSIUS2Z	UNIT SELECT 2 ²	101-2C
56	YSIUS2Y		101-2B
27	YSIUS3Z	UNIT SELECT 2 ³	101-2D
57	YSIUS3Y		101-2A
28	YSIB17Z	BUS IN BIT 7 (WRITE PROTECT)	104-8D
58	YSIB17Y		104-8A
29	YKSPCKO	POWER SEQUENCE PICK	103-2F
59	YKSHLDO	POWER SEQUENCE HOLD	103-2F
30	YSITG4Z	TAG 4	103-2D
60	YSITG4Y		103-2D

"B" CABLE INTERFACE

PIN NO.	FUNCTION	NAME	JUMP LOCATION
1	X000	GROUND	105-8G
14	YSISCKY	SERVO CLOCK	105-8B
2	YSISCKZ		105-8B
15	X000	GROUND	105-8G
3	YSIRDYZ	READ DATA	105-8C
16	YSIRDZY		105-8C
4	X000	GROUND	105-8G
17	YSIRCKY	READ CLOCK	105-8D
5	YSIRCKZ		105-8C
18	X000	GROUND	105-8G
6	YSIWCKZ	WRITE CLOCK	102-2B
19	YSIWCKY		102-2A
7	X000	GROUND	105-8G
20	YSIWDYZ	WRITE DATA	102-2A
8	YSIWDZY		102-2A
21	X000	GROUND	105-8G
9	YSIUSDZ	UNIT SELECTED	105-8D
22	YSIUSDY		105-8D
10	YSISK0Z	SEEK END	105-8E
23	YSISK0Y		105-8E
11	X000	GROUND	105-8G
24	YSIINXY	INDEX	105-8E
12	YSIINXZ		105-8F
25	X000	GROUND	105-8H
13	YSISECZ	SECTOR	105-8F
26	YSISECY		105-8F



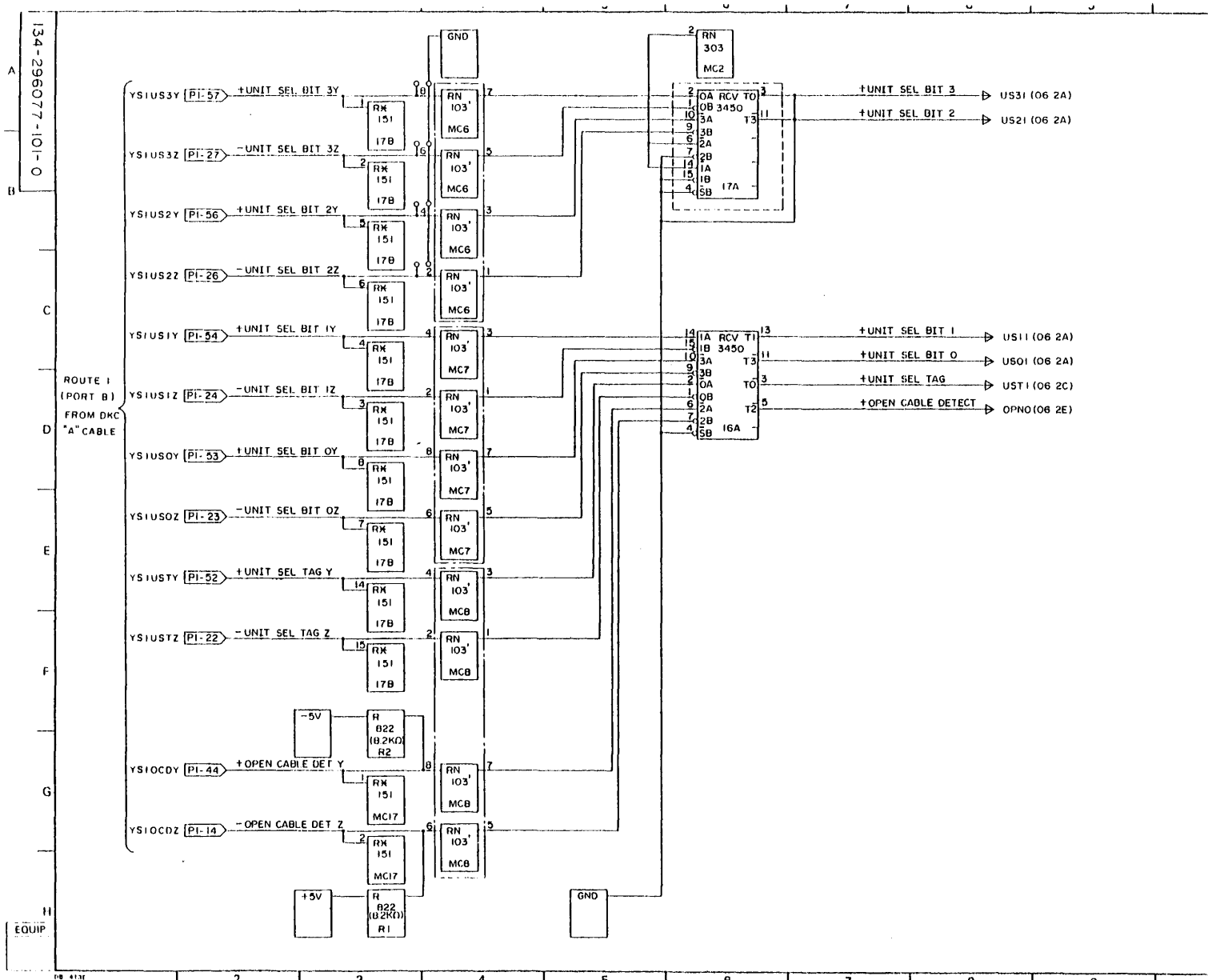
REV	DATE	DESCRIPTION(S)	APP
1	0	1982.3.31	

DWG ABBR	
PKG LOCATION	
PKG NAME	
052	
NEXT SPEC	
DRAFT	ENG
CHK	APP
ISSUE	
ROUTE 1 (PORT B) INTERFACE	
134-296077-052-0	
NEC	BIT 1/1

A-6

EQUIP

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REV	COMP	DESCRIPTION (SC)	APP
1	0	1982.3.31	

DWG ABBR	
PKG LOCATION	
PKG NAME	

101

NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE

G9QSW PWA

(1/11)

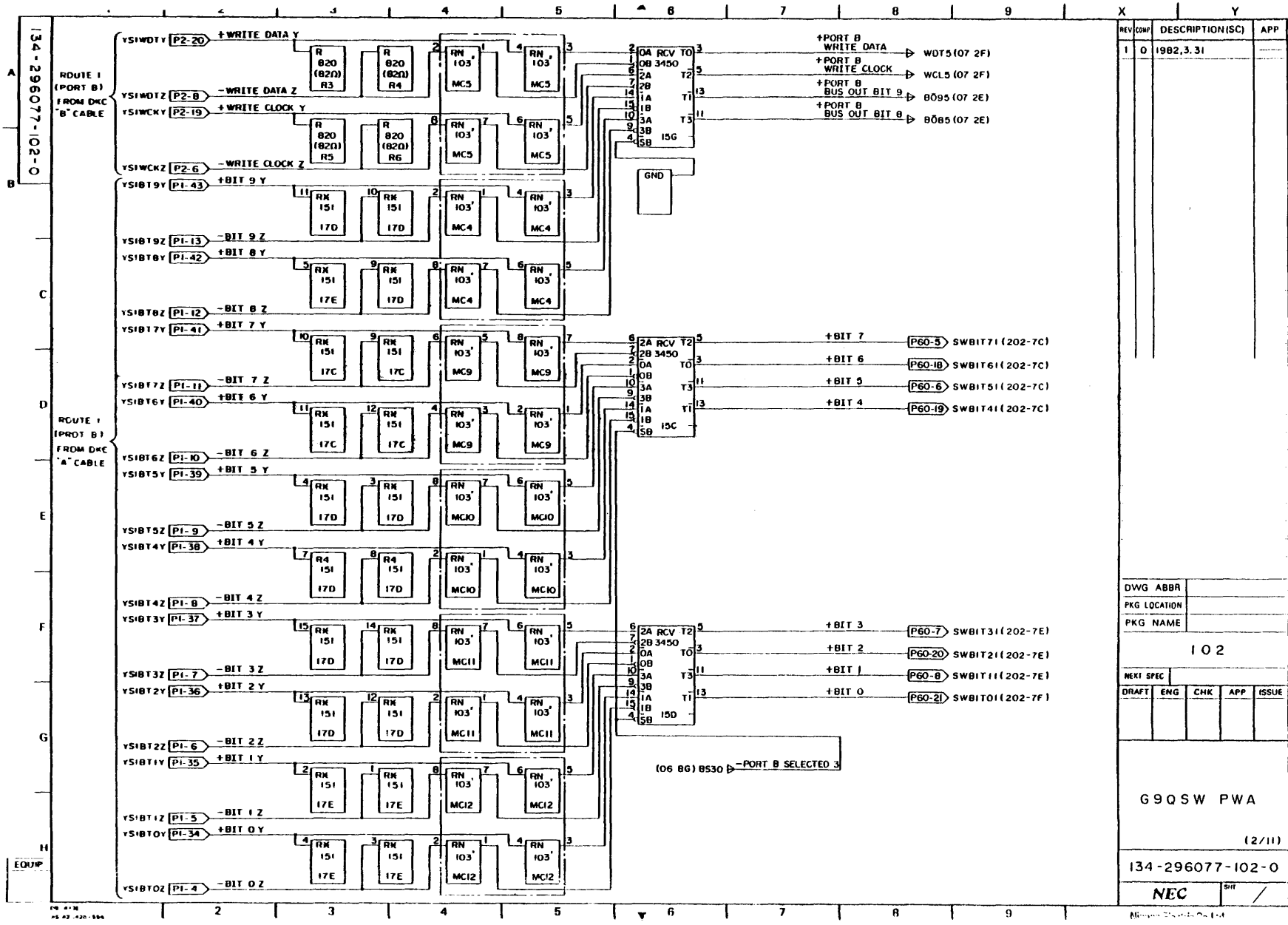
134-296077-101-0

NEC SHI

Nippon Electric Co. Ltd

IB 411E
IB 42 1410-514

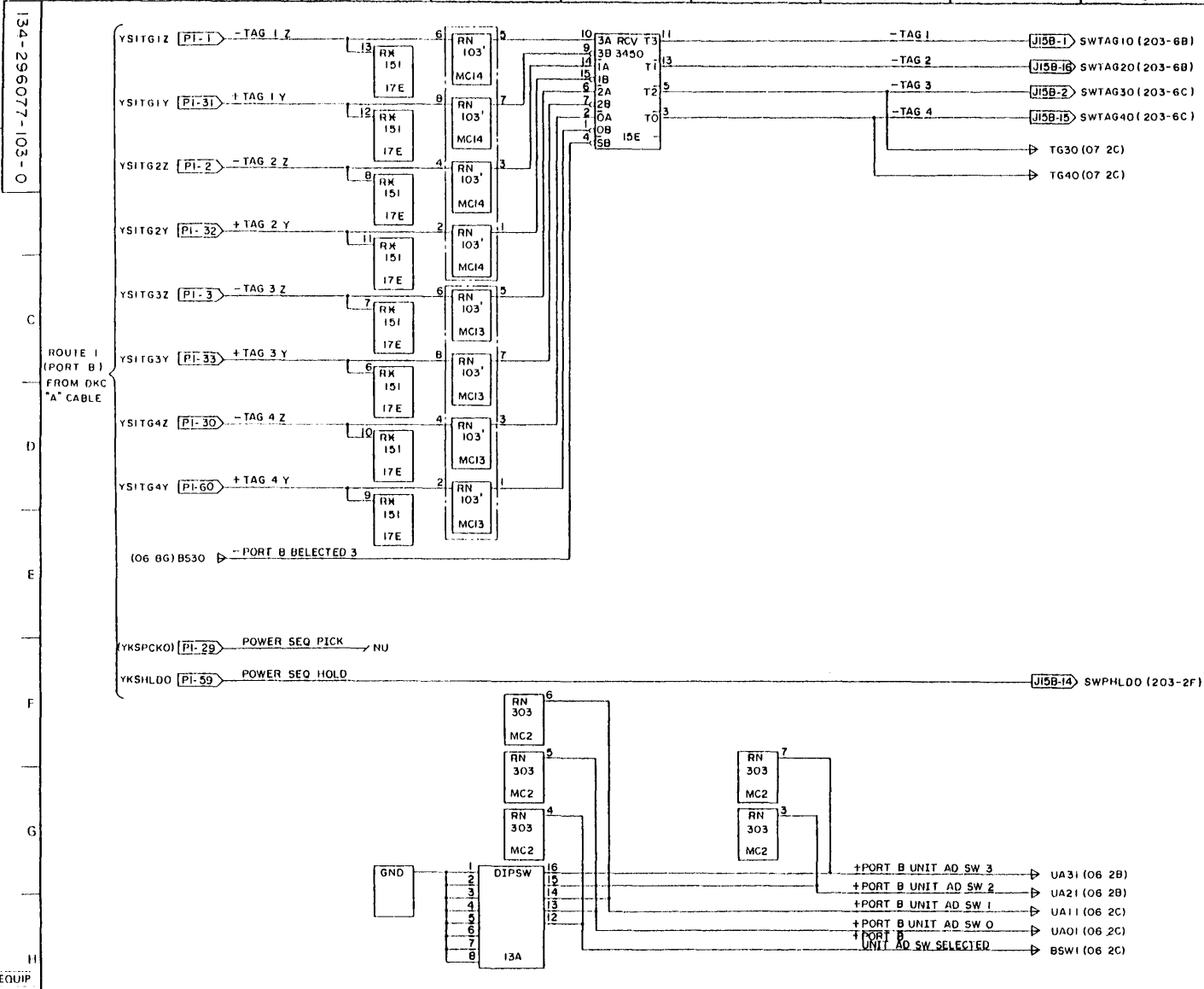
A-8



REV/CONF	DESCRIPTION (SC)	APP
1 0	1982.3.31	
DWG ABBR		
PKG LOCATION		
PKG NAME		
102		
MEKI SPEC		
DRAFT	ENG	CHK APP ISSUE
G90SW PWA		
(2/11)		
134-296077-102-0		
NEC		

14-0138
14-02-220-1004

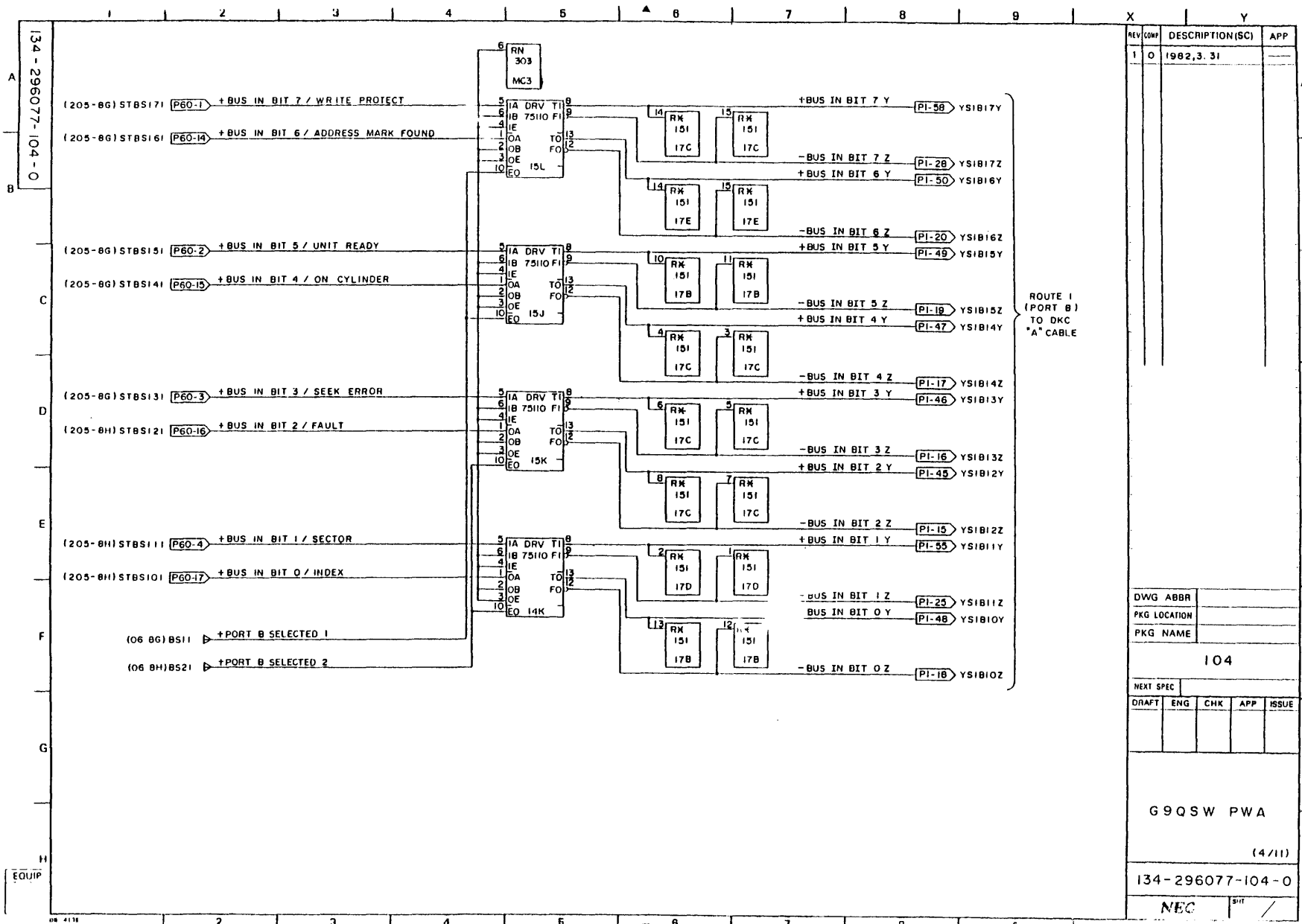
A-9



REV	COMP	DESCRIPTION (SC)	APP
1	0	1982.3.31	

DWG ABBR				
PKG LOCATION				
PKG NAME				
103				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
G9QSW PWA				
(3/11)				
134-296077-103-0				
NEC				SH

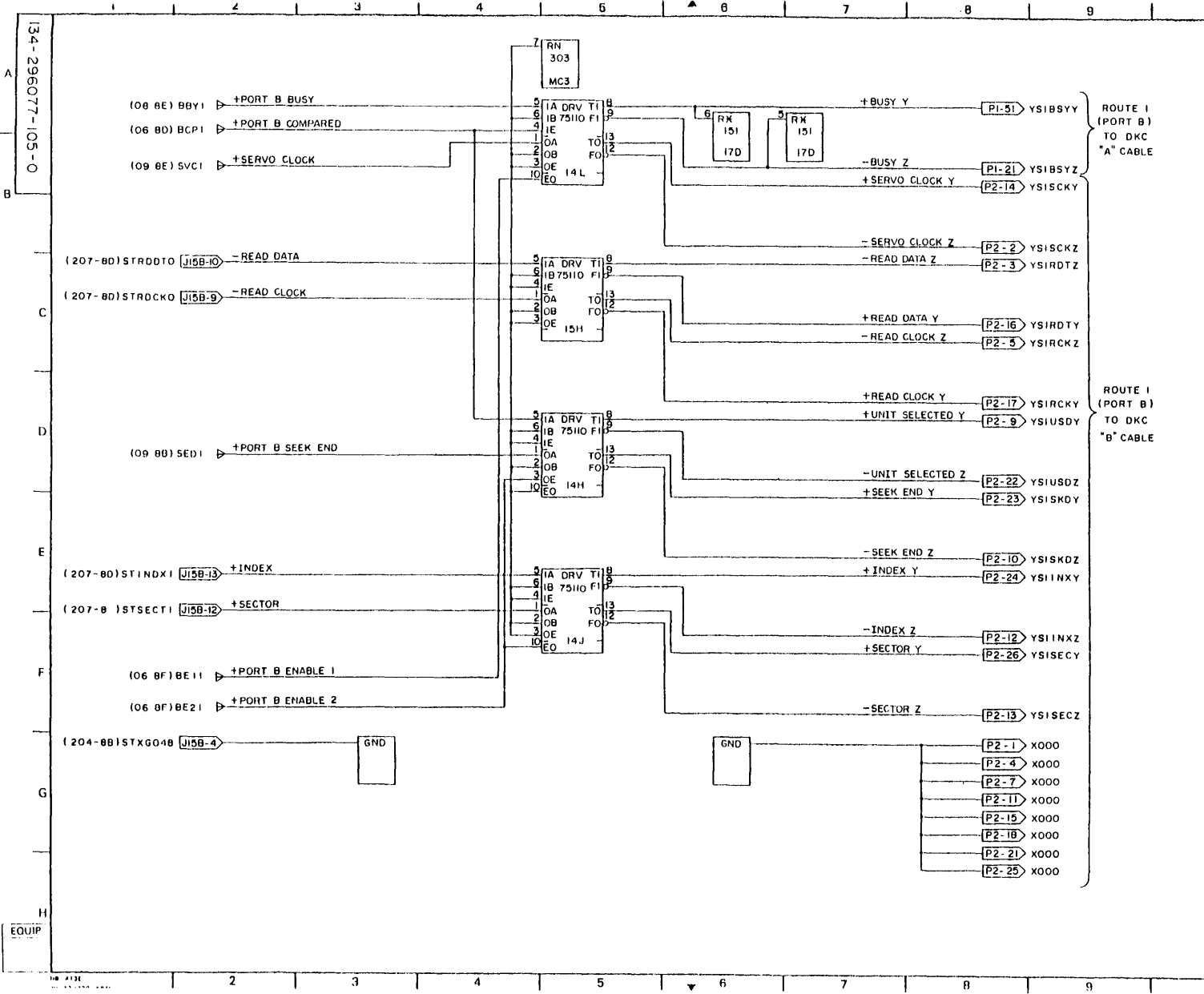
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REV	COMP	DESCRIPTION (SC)	APP
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DWG ABBR	
PKG LOCATION	
PKG NAME	
104	
NEXT SPEC	
DRAFT	ENG
CHK	APP
ISSUE	
G9QSW PWA	
(4/11)	
134-296077-104-0	
NEC	SHIT /

A-11



REV	COMP	DESCRIPTION(S)	APP
1	0	1982, 3, 31	

REV	COMP	DESCRIPTION(S)	APP
1	0	1982, 3, 31	

REV	COMP	DESCRIPTION(S)	APP
1	0	1982, 3, 31	

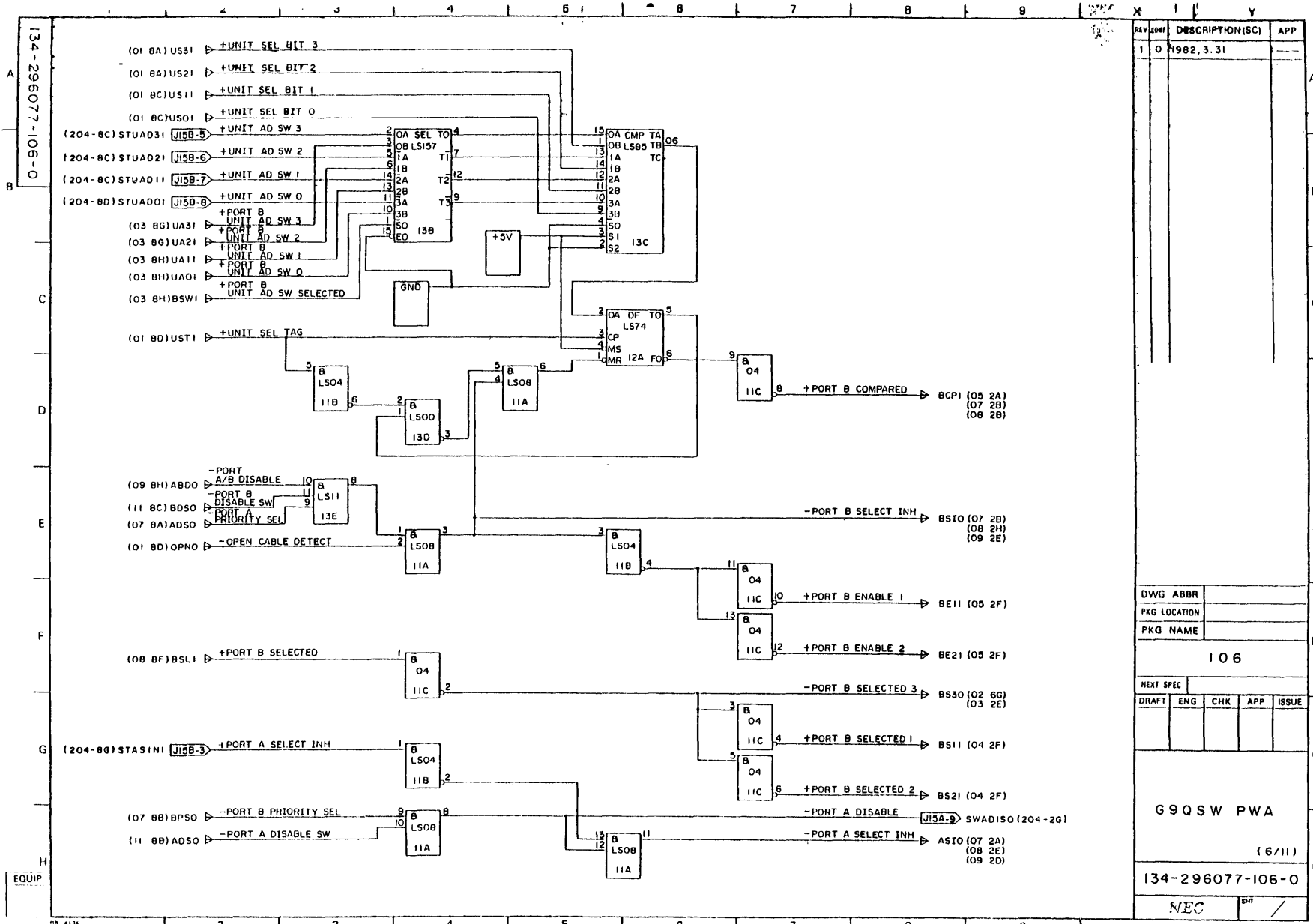
DWG ABBR	
PKG LOCATION	
PKG NAME	

105				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE

G9QSW PWA
(5/11)

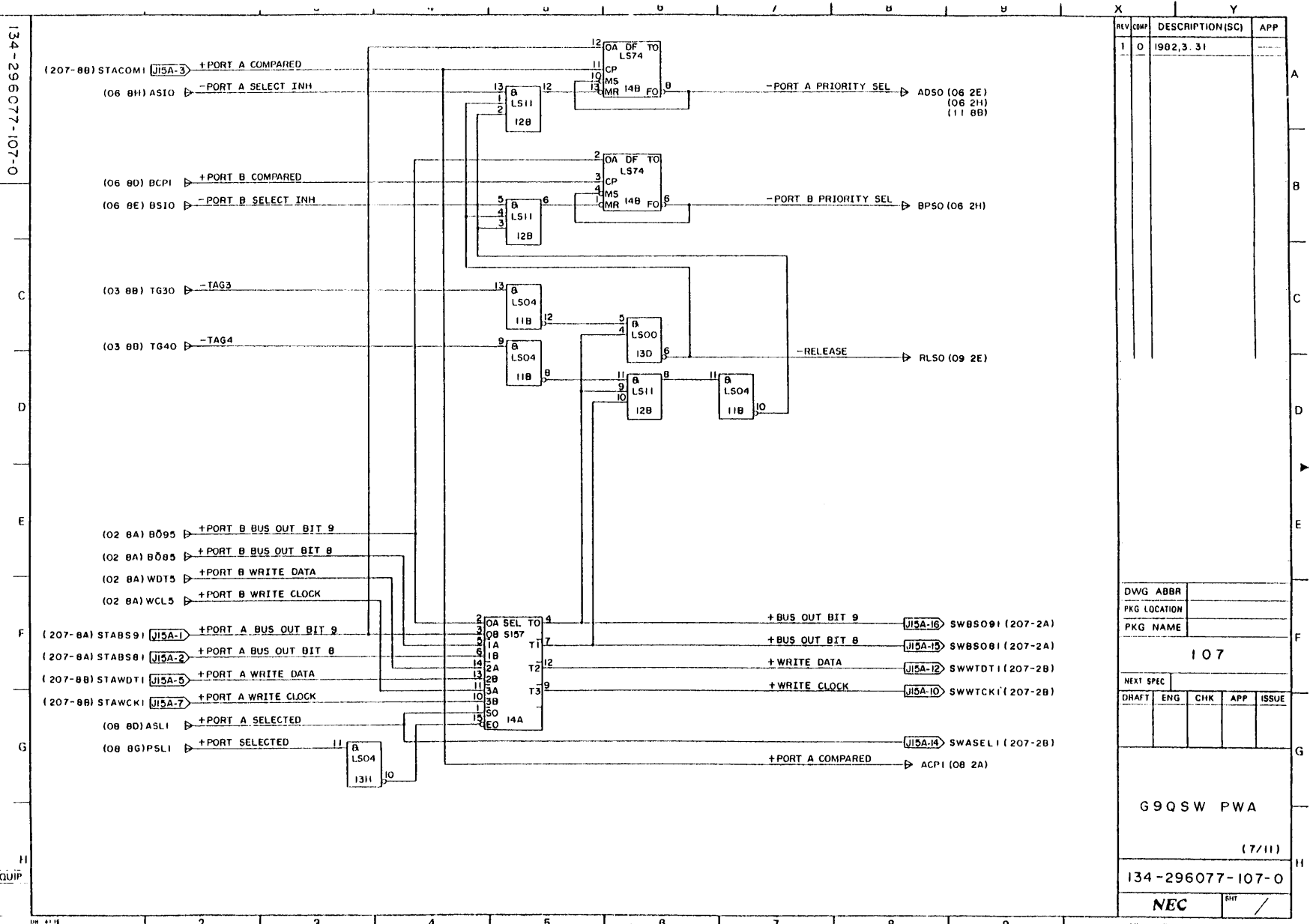
134-296077-105-0
NEC

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134-296077-107-0

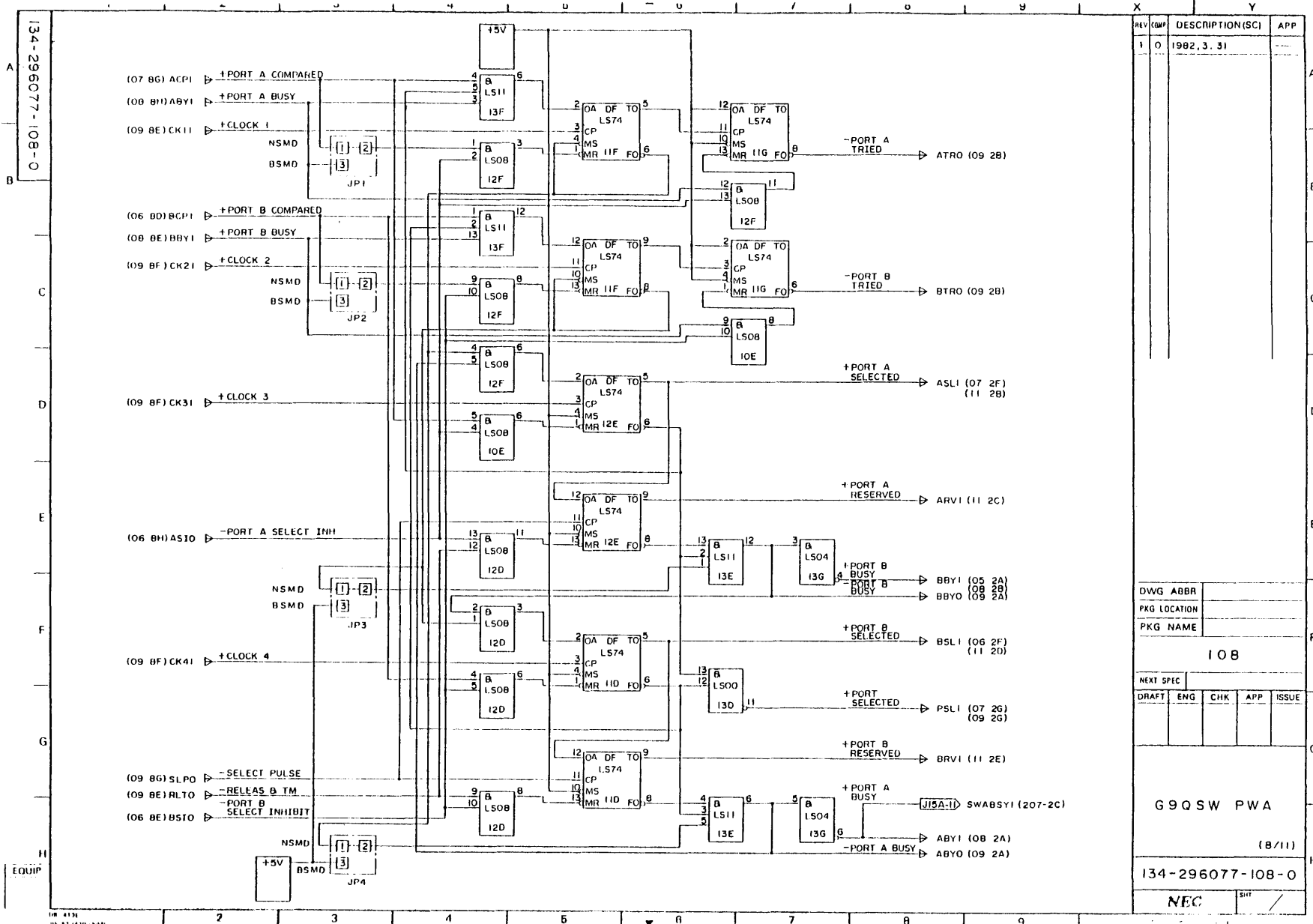
A-13



REV	COMP	DESCRIPTION (SC)	APP
1	0	1982.3.31	

DWG ABBR				
PKG LOCATION				
PKG NAME				
107				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
G9QSW PWA				
(7/11)				
134-296077-107-0				
NEC				RHT /

A-14

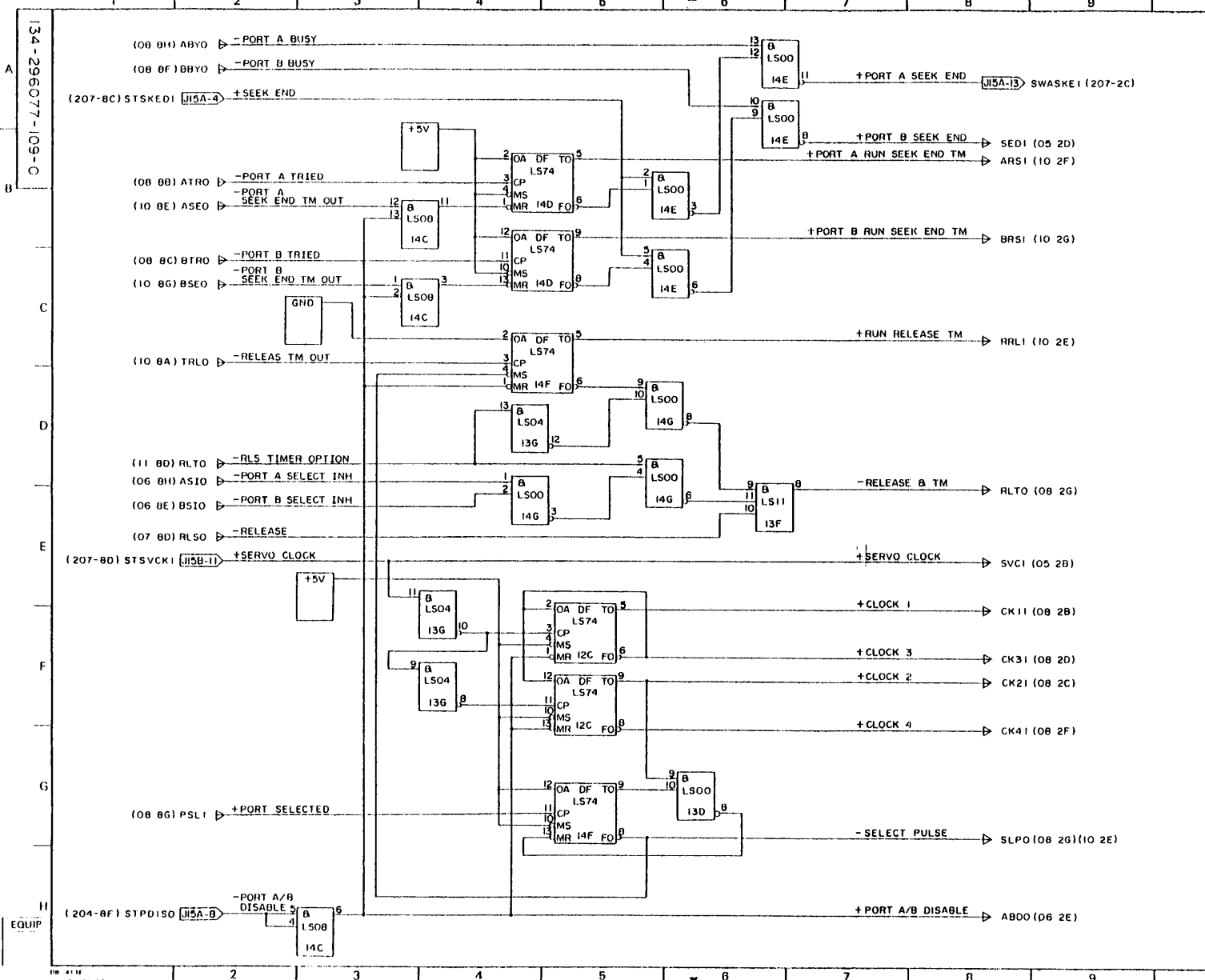


REV	COMP	DESCRIPTION (SC)	APP
1	0	1982, 3, 31	

DWG ABBR				
PKG LOCATION				
PKG NAME	IOB			
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
G9QSW PWA				
(8/11)				
134-296077-108-0				
NEC				SHT /

134-296077-108-0

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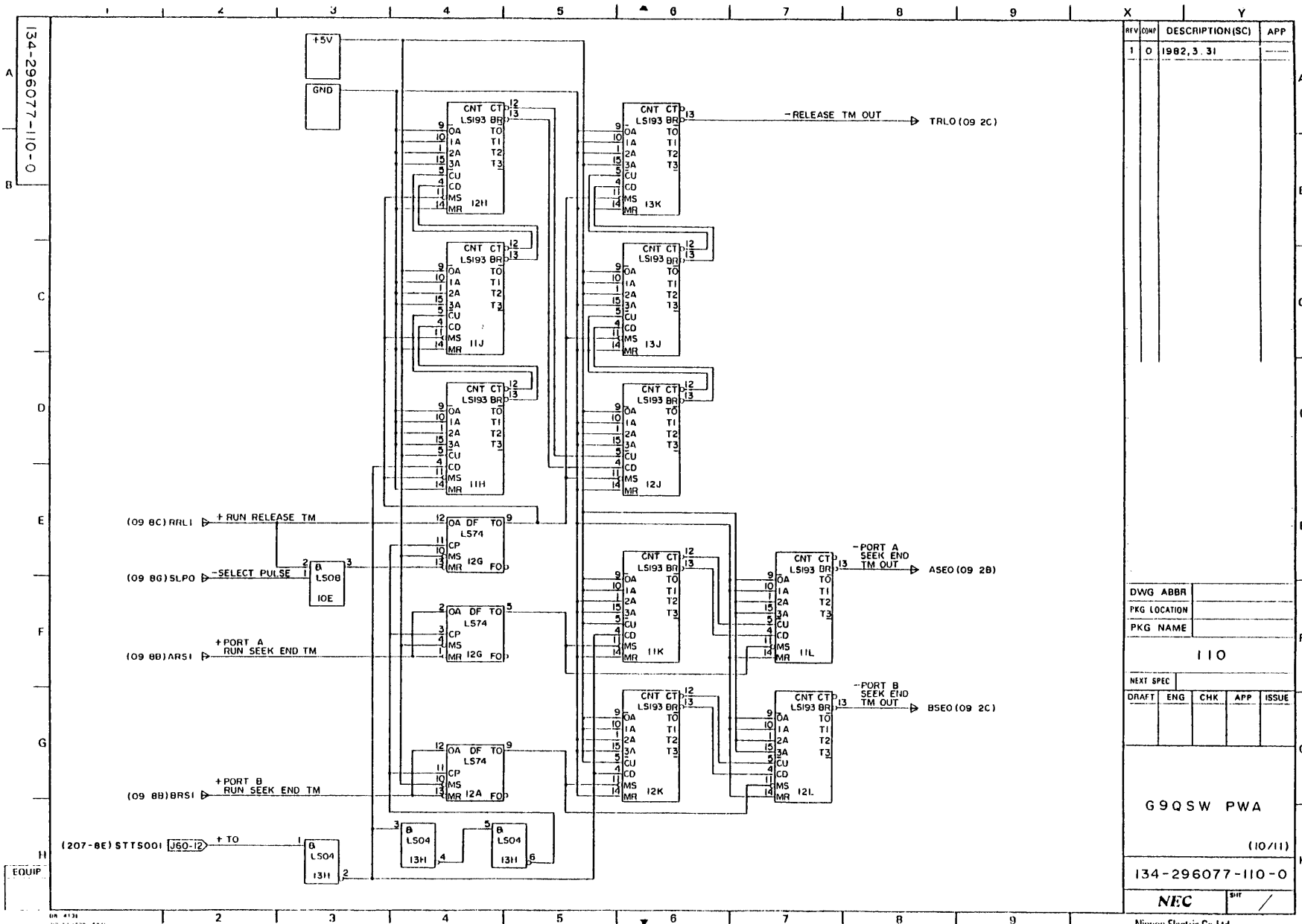
REV	COMP	DESCRIPTION (SC)	APP
1	0	1982.3.31	

DWG ABBR				
PKG LOCATION				
PKG NAME				
109				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
G9QSW PWA				
(9/11)				
134-296077-109-0				
NEC				REV

HW 411E
REV 42 (4/78)

Mitsubishi Electric Co. Ltd

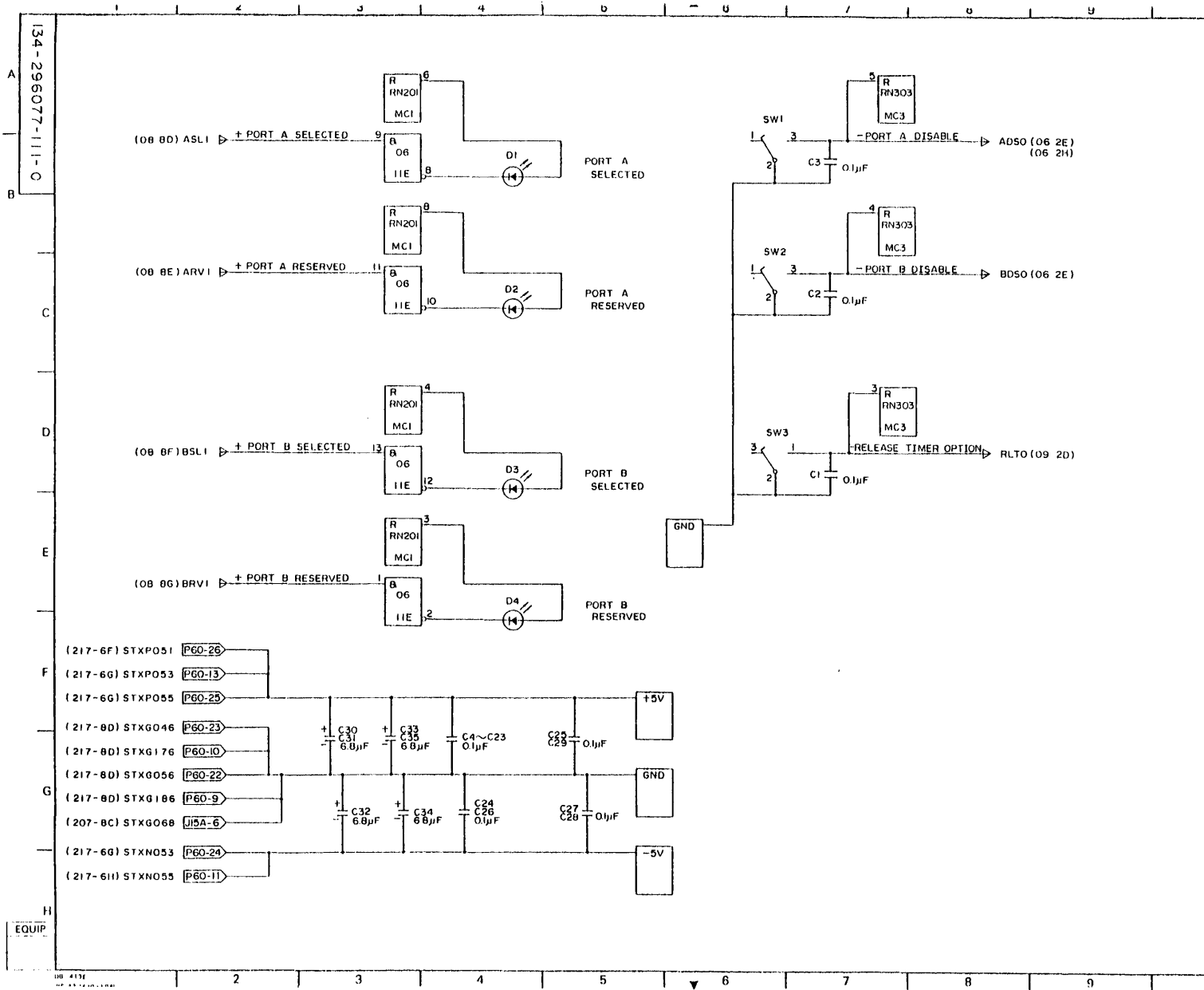
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REV	DATE	DESCRIPTION (SC)	APP
1	0	1982, 3 31	

DWG ABBR				
PKG LOCATION				
PKG NAME				
110				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
G9QSW PWA				
(10/11)				
134-296077-110-0				
NEC				SPT /

A-17



REV	COMP	DESCRIPTION (SC)	APP
1	0	1982.3.31	

DWG ABBR	
PKG LOCATION	
PKG NAME	

|||

NEXT SPEC	
DRAFT	ENG
CHK	APP
ISSUE	

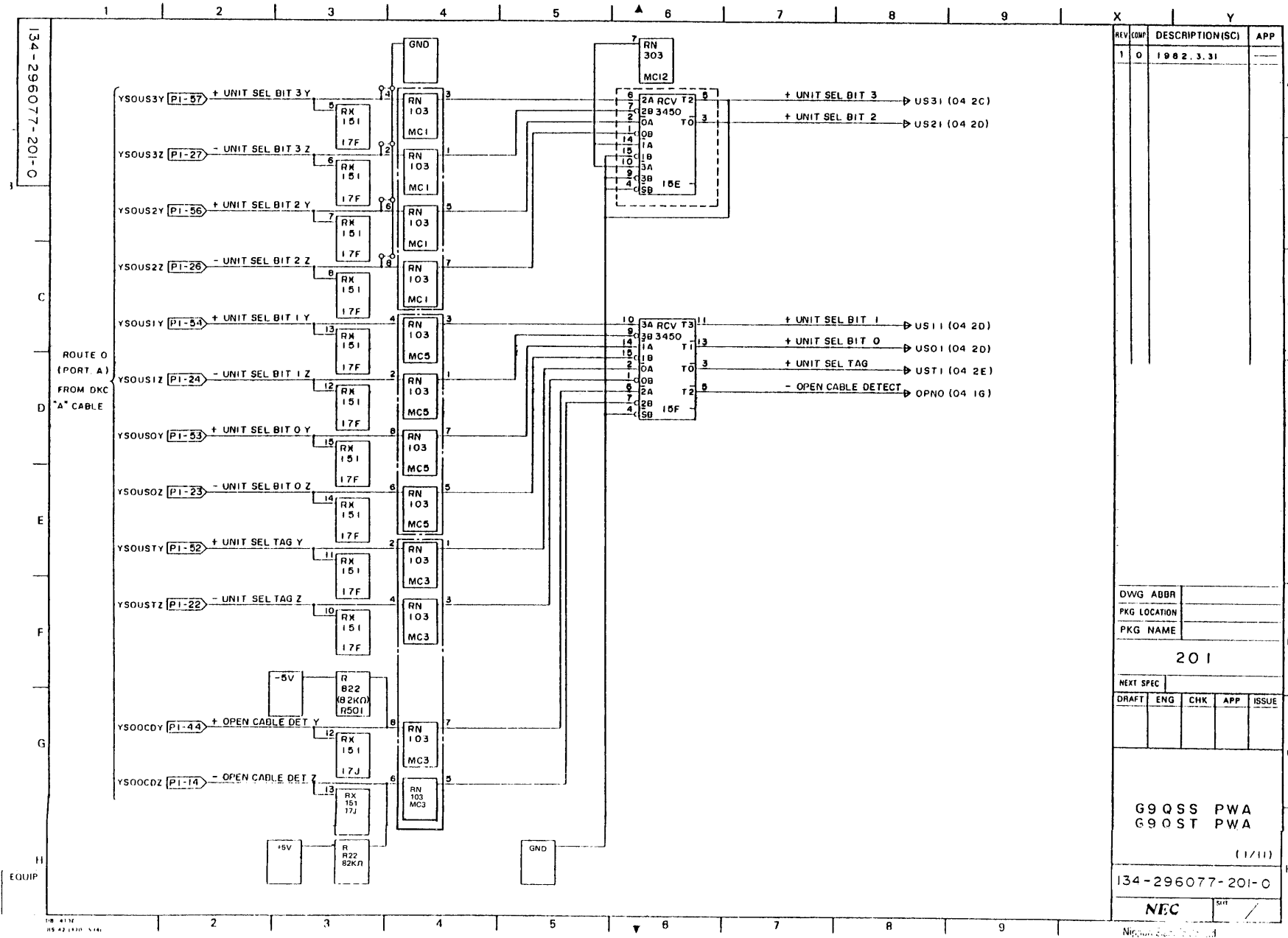
G9QSW PWA

(11/11)

134-296077-111-0

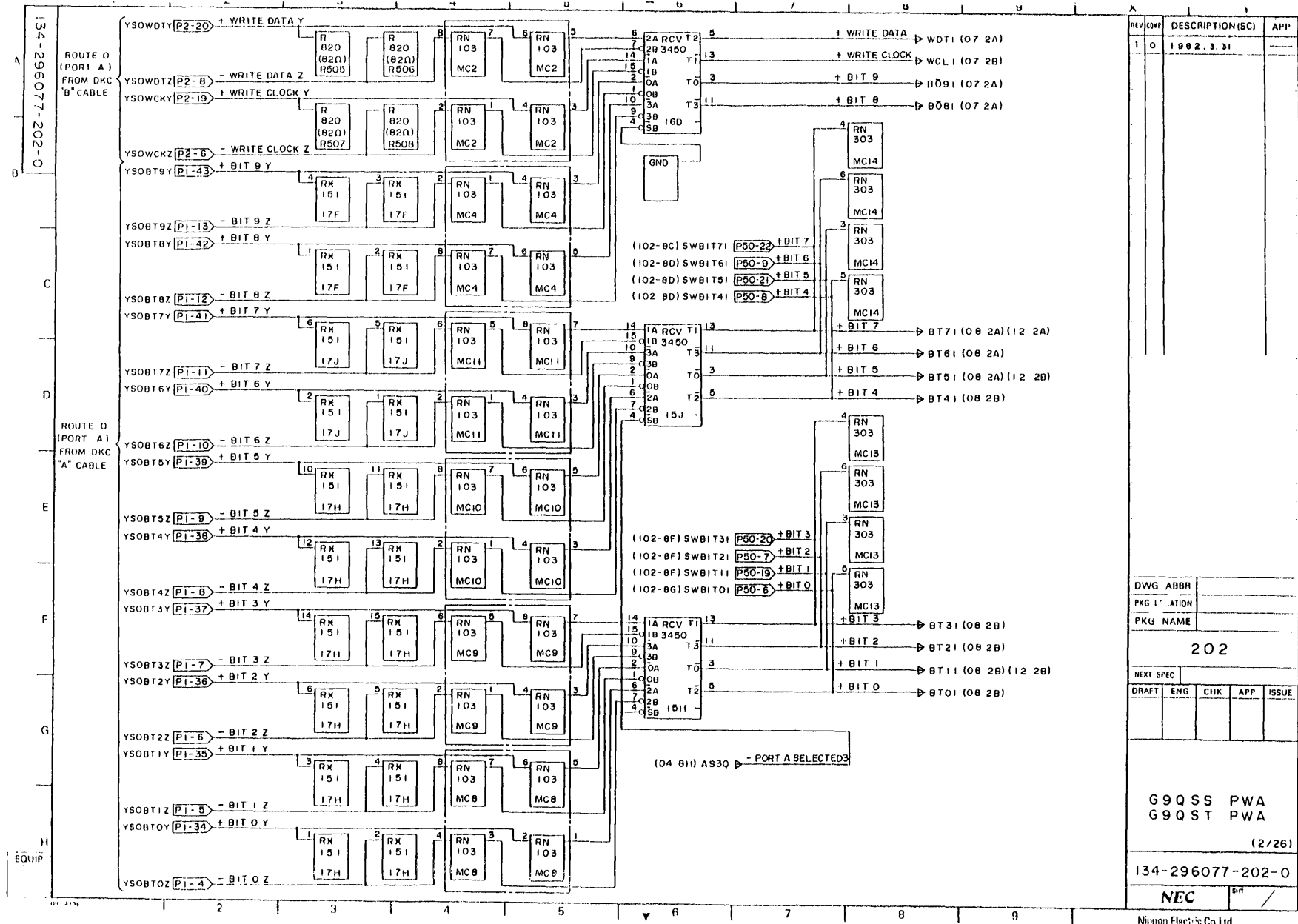
NEC

Northrop Grumman Co Ltd



REV	COMP	DESCRIPTION (SC)	APP
1	0	1992.3.31	

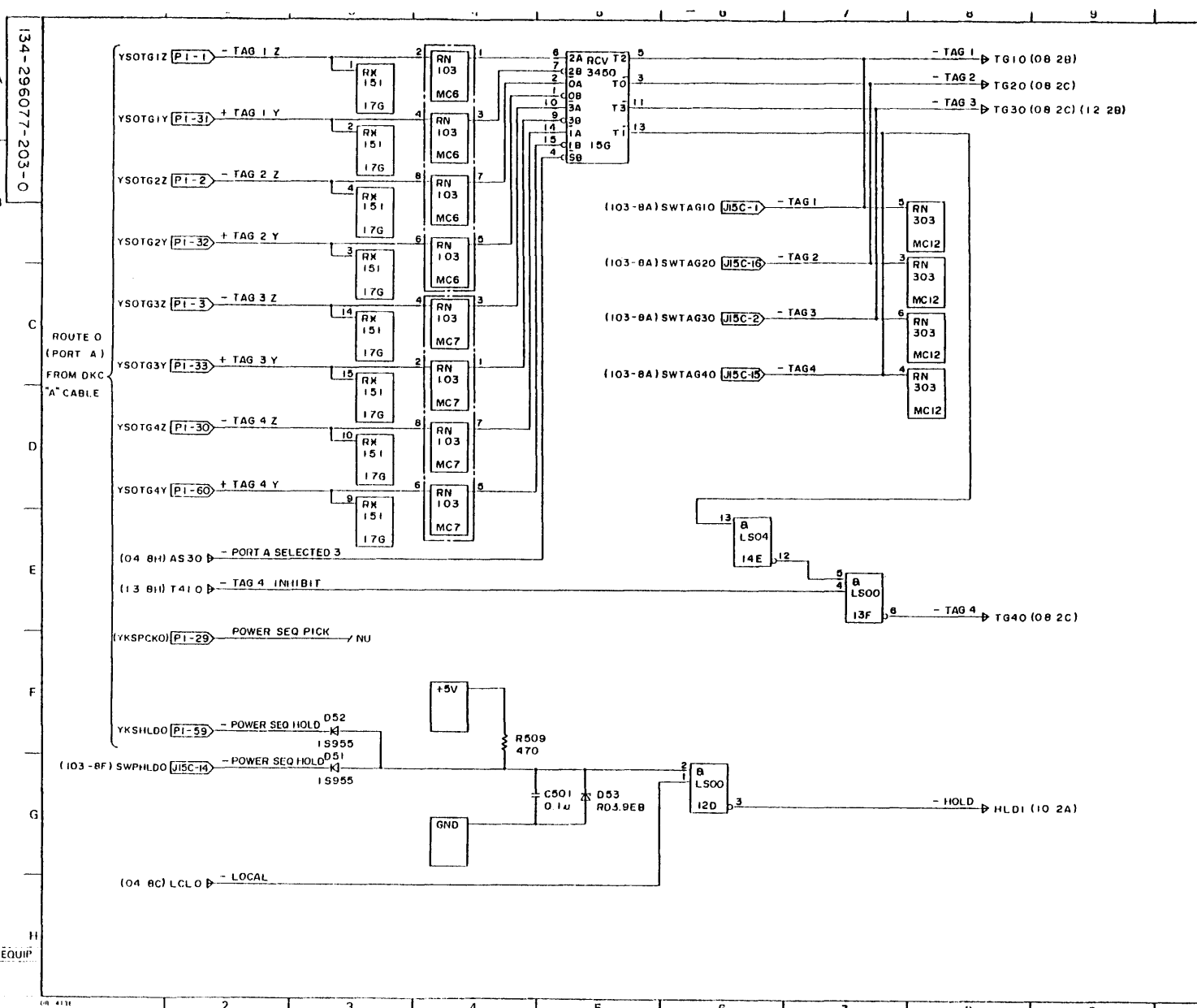
DWG ABBR				
PKG LOCATION				
PKG NAME				
201				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
G9QSS PWA G9OST PWA (1/11)				
134-296077-201-0				
NEC				



REV	COMP	DESCRIPTION (ISC)	APP
1	0	1982.3.31	

DWG ABBR				
PKG LOCATION				
PKG NAME				
202				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
G9QSS PWA G9QST PWA				
(2/26)				
134-296077-202-0				
NEC				5/11

Nippon Electric Co Ltd



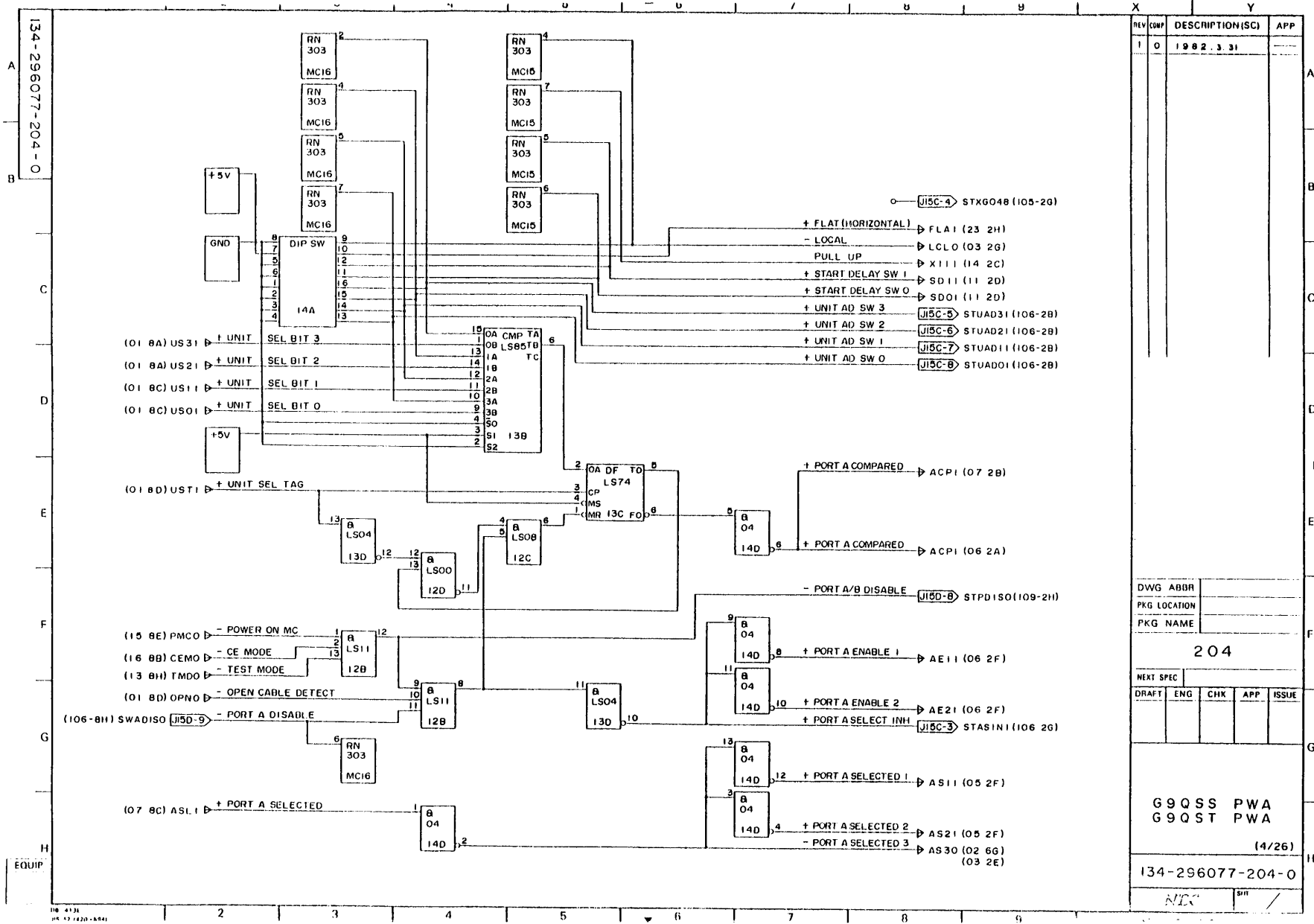
REV	DESCRIPTION(S)	APP
1 0	1982.3.31	

DWG ABBR	
PKG LOCATION	
PKG NAME	
203	
NEXT SPEC	
DRAFT	
ENG	
CHK	
APP	
ISSUE	
G9QSS PWA G9QST PWA (3/26)	
134-296077-203-0	
NEC	

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EQUIP

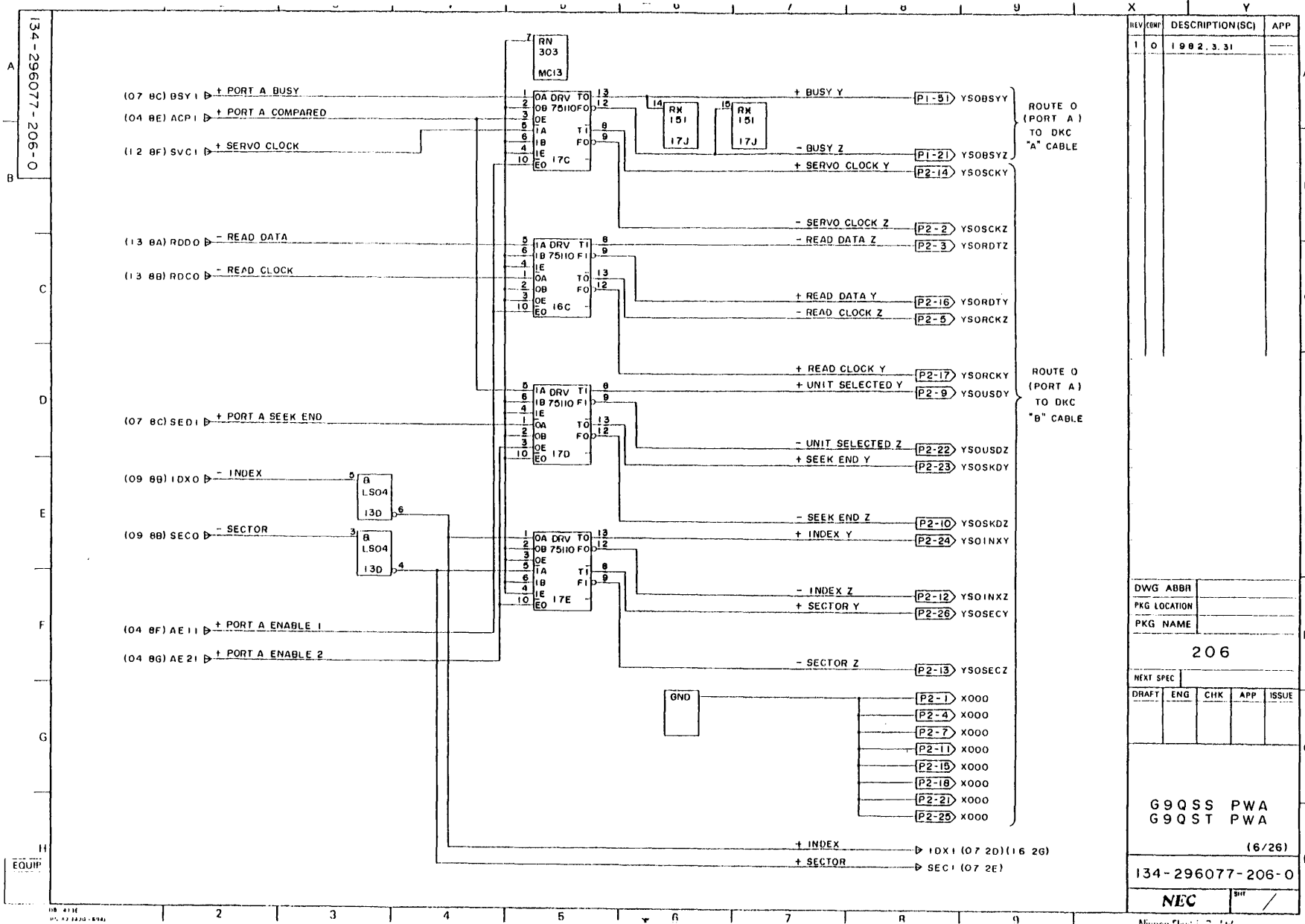
A-21



REV	COMP	DESCRIPTION (SC)	APP
1	0	1982.3.31	

DWG ABBR				
PKG LOCATION				
PKG NAME				
204				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
G9QSS PWA G9QST PWA (4/26)				
134-296077-204-0				
				SH

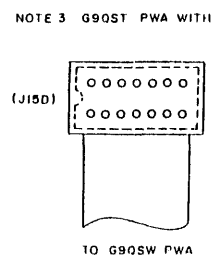
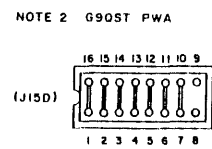
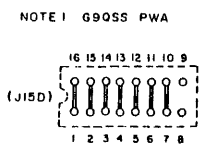
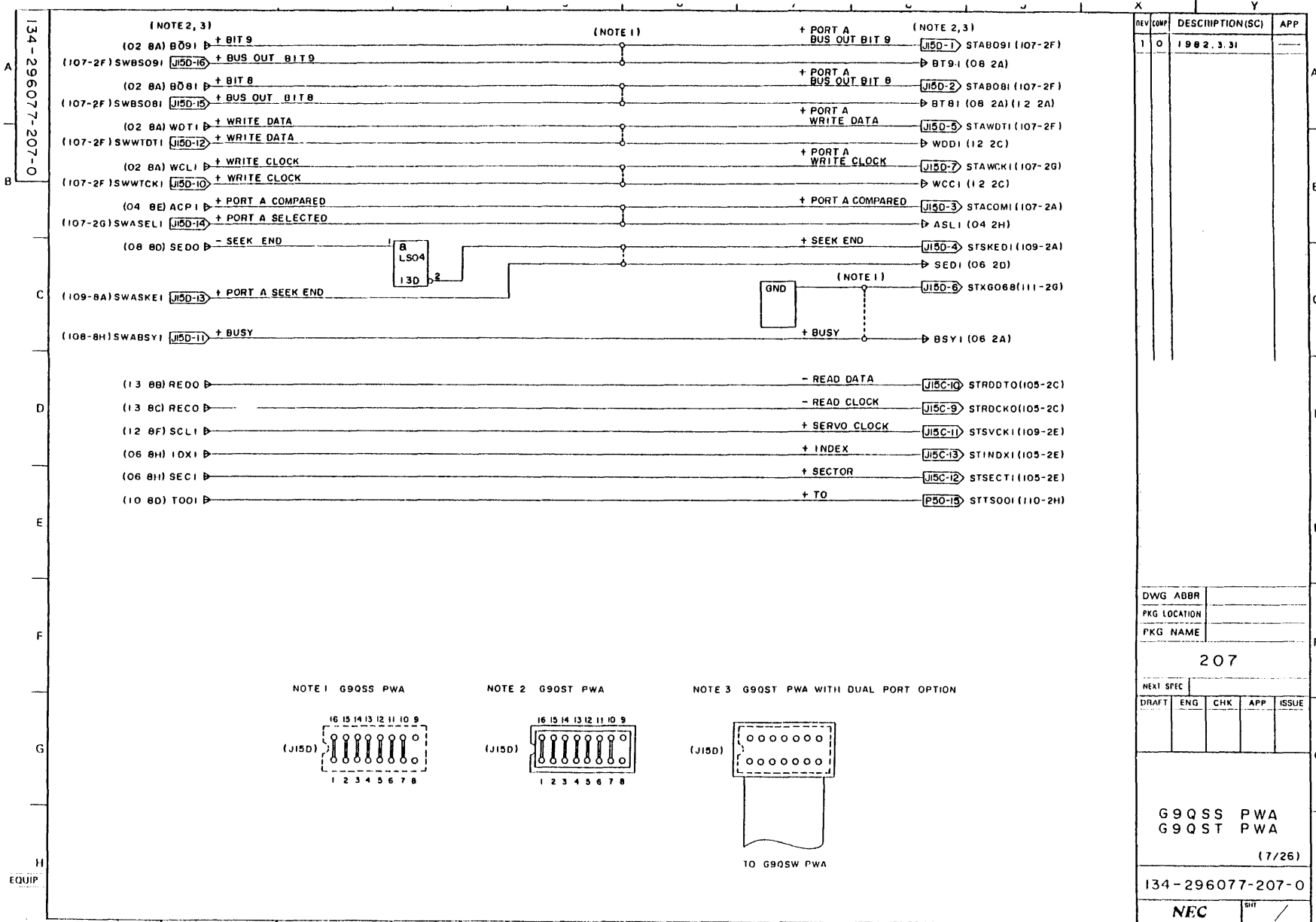
A-23



REV	COMP	DESCRIPTION (SC)	APP
1	0	1982.3.31	

DWG ABBR				
PKG LOCATION				
PKG NAME				
206				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
G9QSS PWA G9QST PWA (6/26)				
134-296077-206-0				
NEC				BHT

10 4131
MAY 82 (2220-874)



REV	COMP	DESCRIPTION(S)	APP
1	0	1982.3.31	

DWG ABBR	
PKG LOCATION	
PKG NAME	

207

NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE

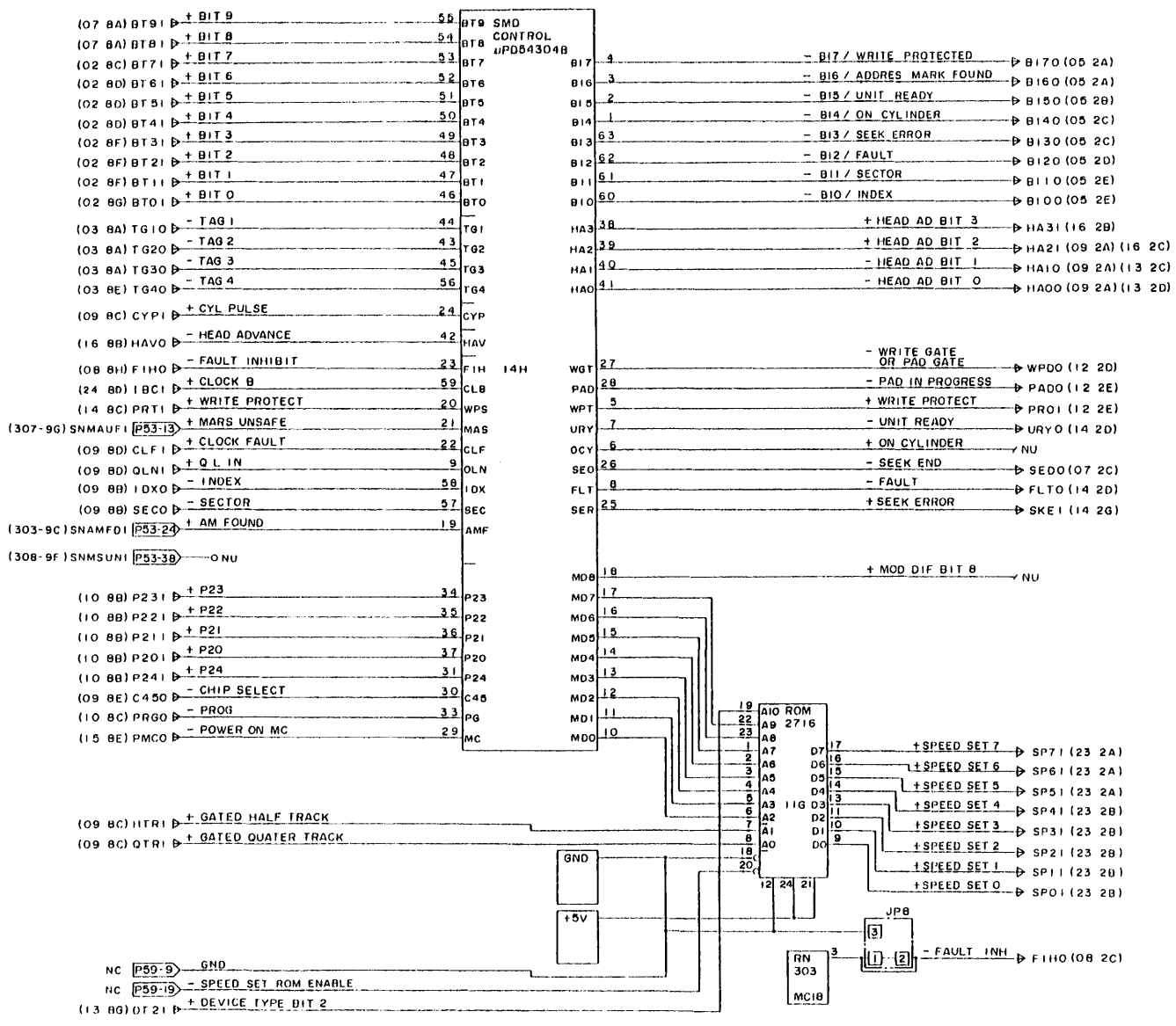
G9QSS PWA
G9QST PWA
(7/26)

134-296077-207-0

NEC

134-296077-208-0

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EQUIP



REV	COMP	DESCRIPTION (SC)	APP
1	0	1982.3.31	

DWG ABBR	
PKG LOCATION	
PKG NAME	

208

NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE

G9QSS PWA
G9QST PWA
(8/26)

134-296077-208-0

NEC

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134-296077-209-0

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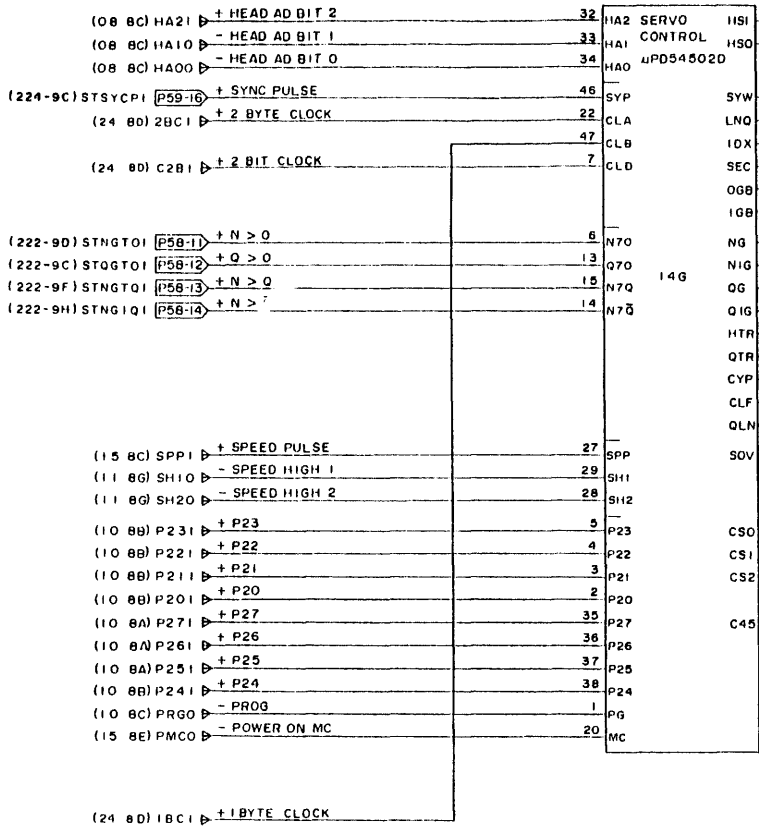
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REV	CONF	DESCRIPTION (SC)	APP
1	0	1 9 8 2 . 3 . 31	

DWG ABBR	
PKG LOCATION	
PKG NAME	
209	
NEXT SPEC	
DRAFT	ENG
CHK	APP
ISSUE	
G9QSS PWA G9QST PWA (9/26)	
134-296077-209-0	
NEC	SP1 /

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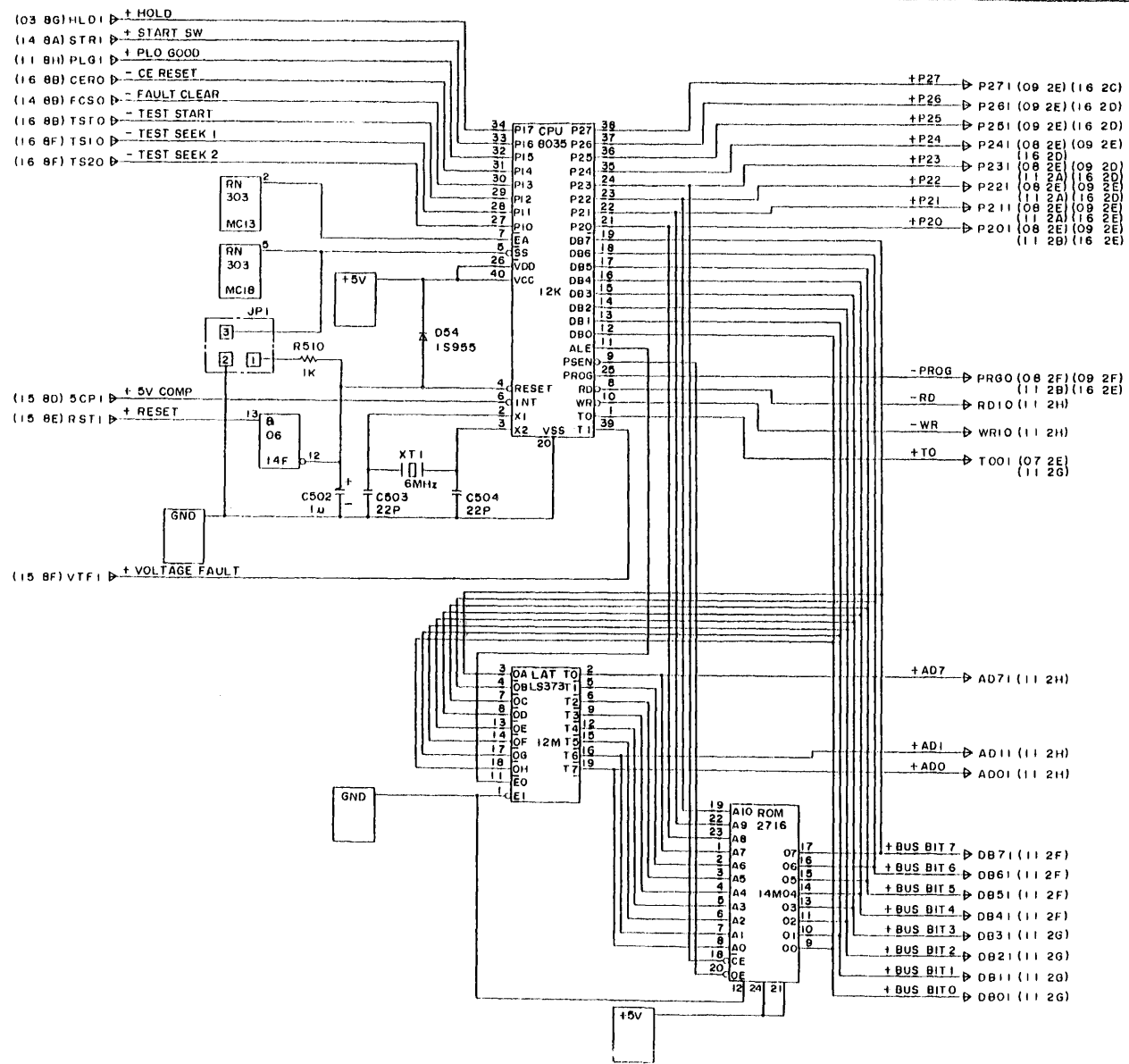
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A-26

134-296077-210-0



REV	COMP	DESCRIPTION (SC)	APP
1	0	1982.3.31	

DWG ABBR				
PKG LOCATION				
PKG NAME				
210				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
G9QSS PWA G9QST PWA (10/26)				
134-296077-210-0				
NEC				

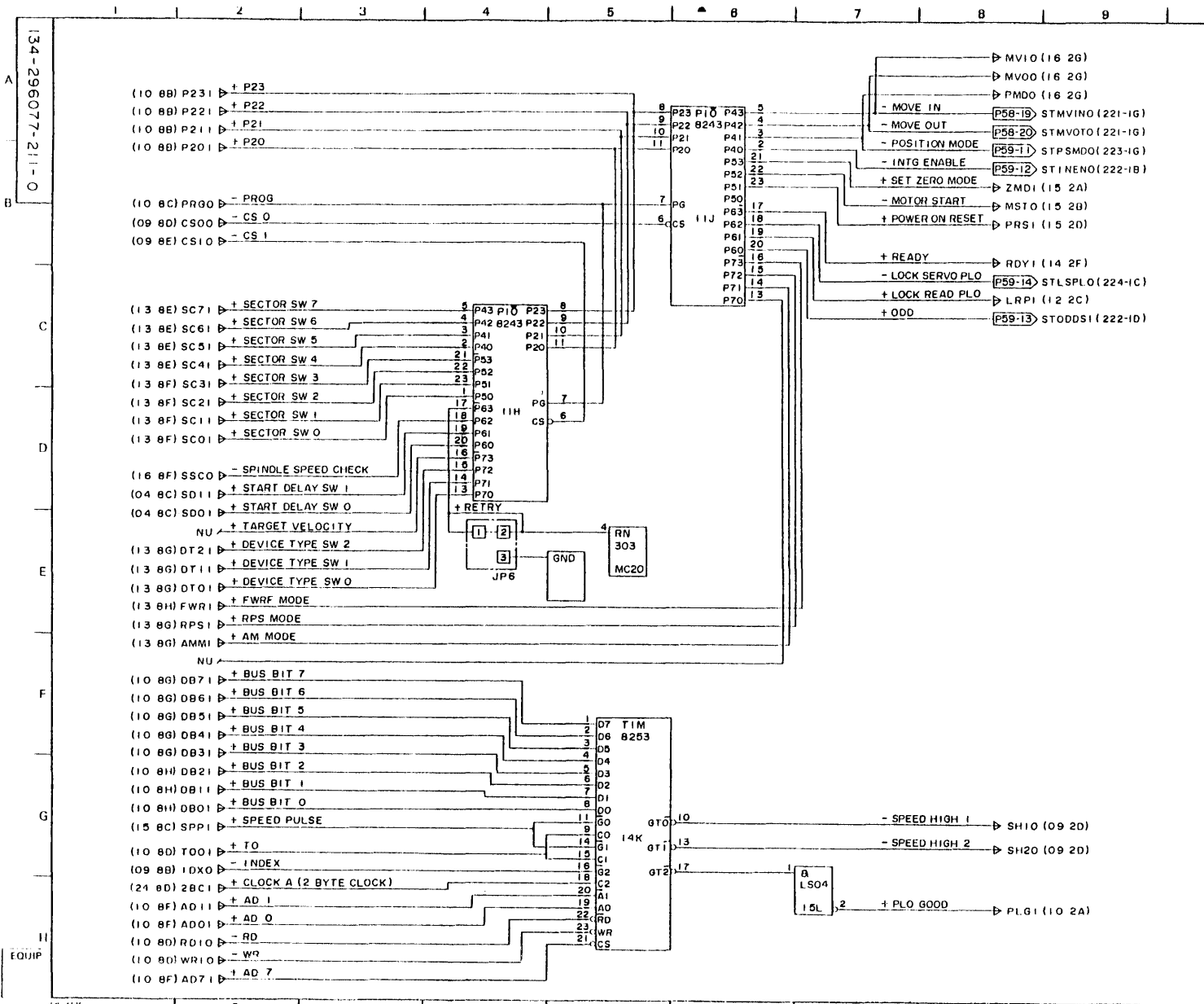
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100 1110
25 27 11/79-544

Number of Pages: 1

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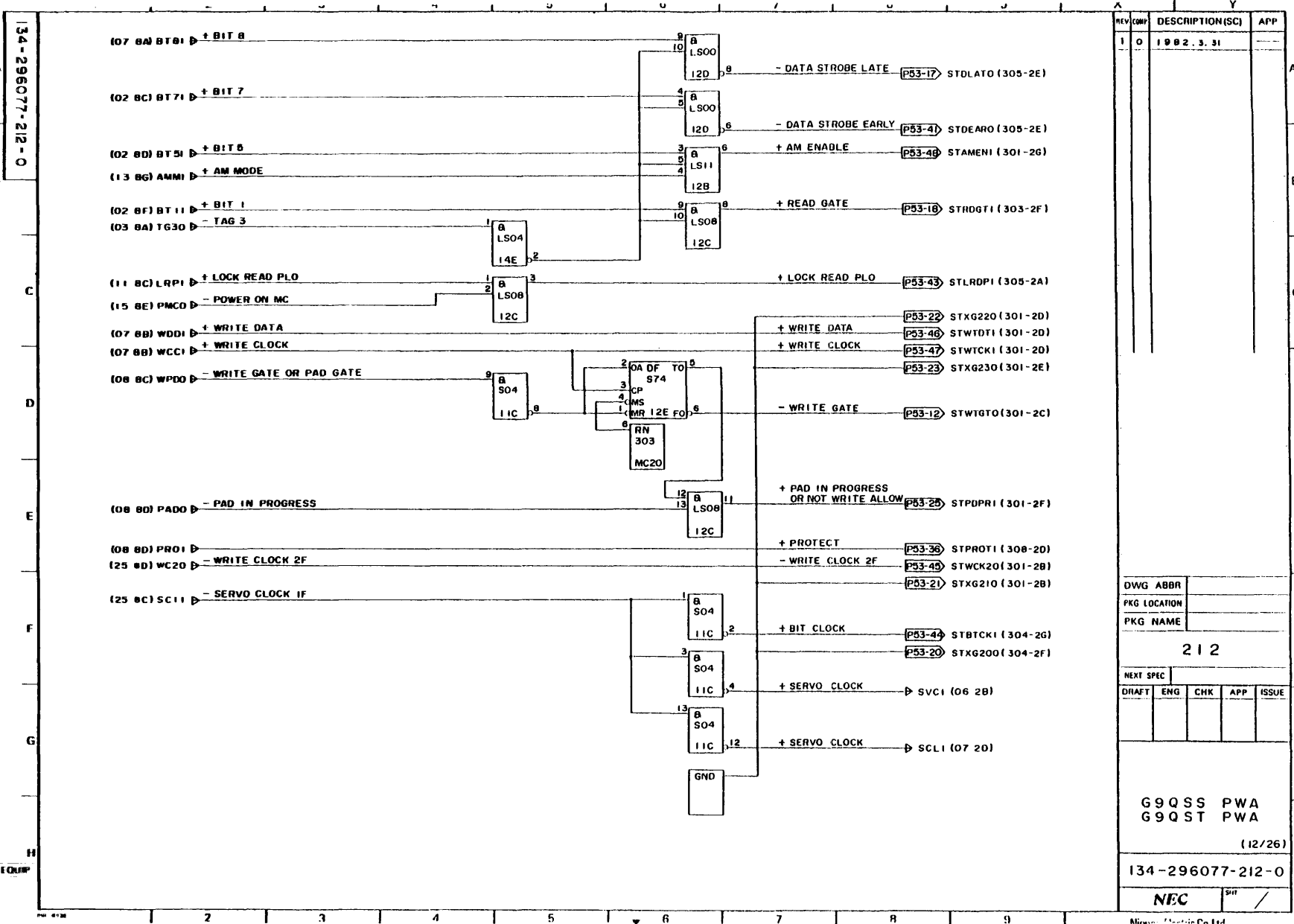


REV	COMP	DESCRIPTION (SC)	APP
1	0	1982.3.31	

DWG ABBR				
PKG LOCATION				
PKG NAME				
2 1 1				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
G9QSS PWA G9QST PWA (11/26)				
134-296077-211-0				
NEC				SH

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REV	COMP	DESCRIPTION (SC)	APP
1	0	1982.5.31	

DWG ABBR	
PKG LOCATION	
PKG NAME	
212	
NEXT SPEC	
DRAFT	ENG
CHK	APP
ISSUE	

G9QSS PWA G9QST PWA	
(12/26)	
134-296077-212-0	
NEC	SH /

134-296077-212-0

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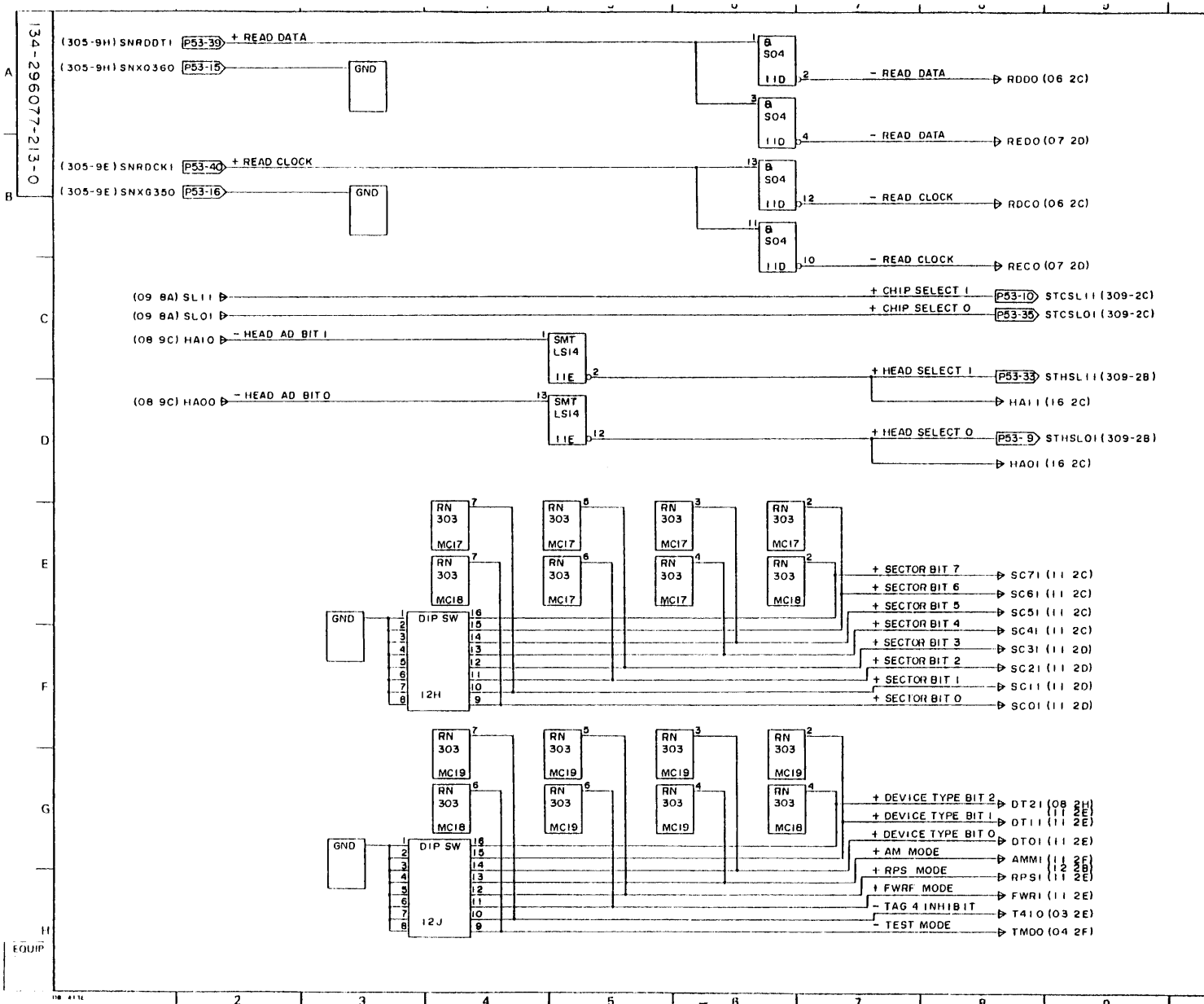
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REV	COMP	DESCRIPTION(S)	APP
1	0	1 9 8 2 . 3 3 1	

DWG ABBR	
PKG LOCATION	
PKG NAME	

2 1 3

NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE

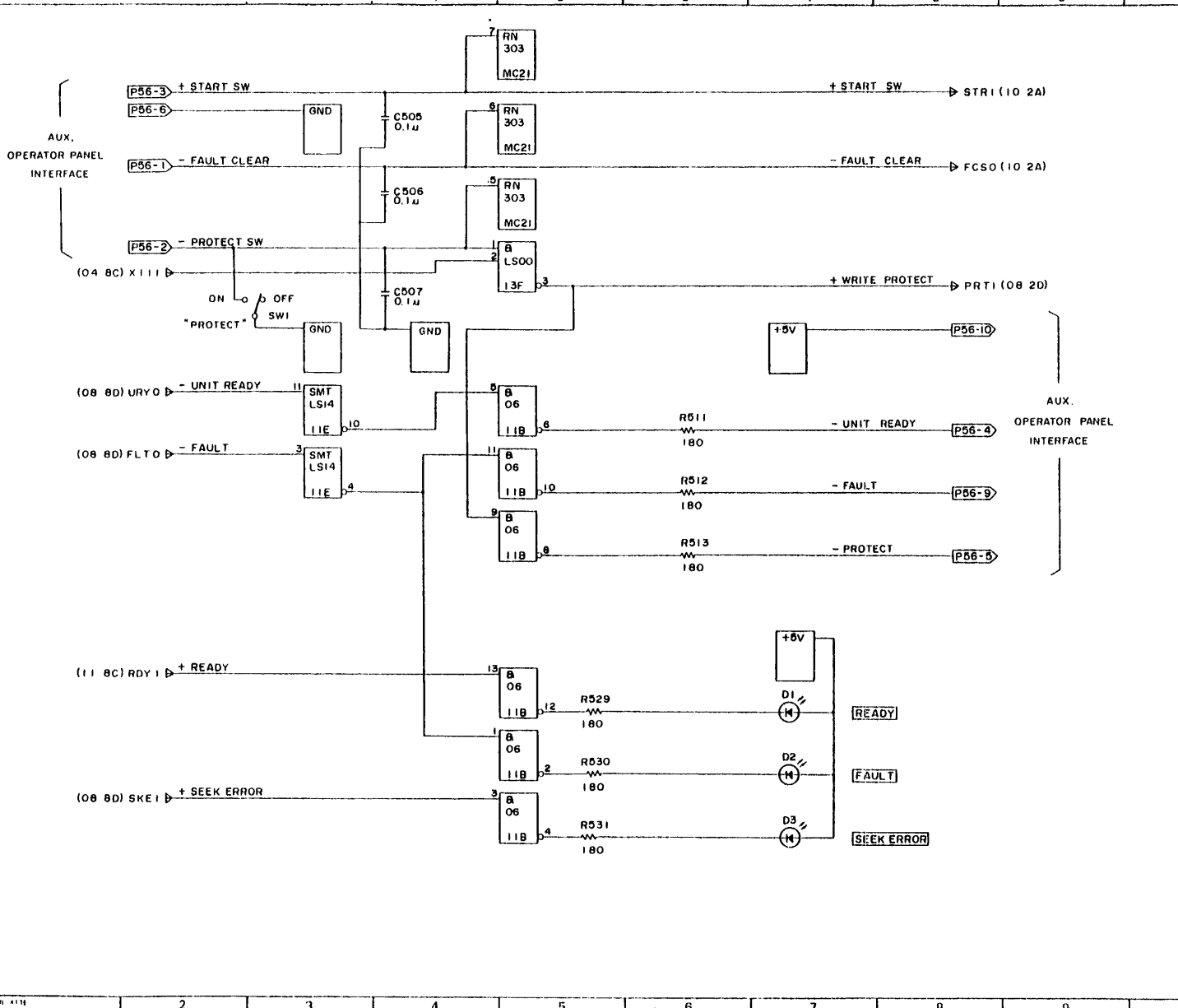
G9QSS PWA
G9QST PWA
(13/26)

134-296077-213-0

NEC MINI

Minneapolis Electric Co. Ltd.

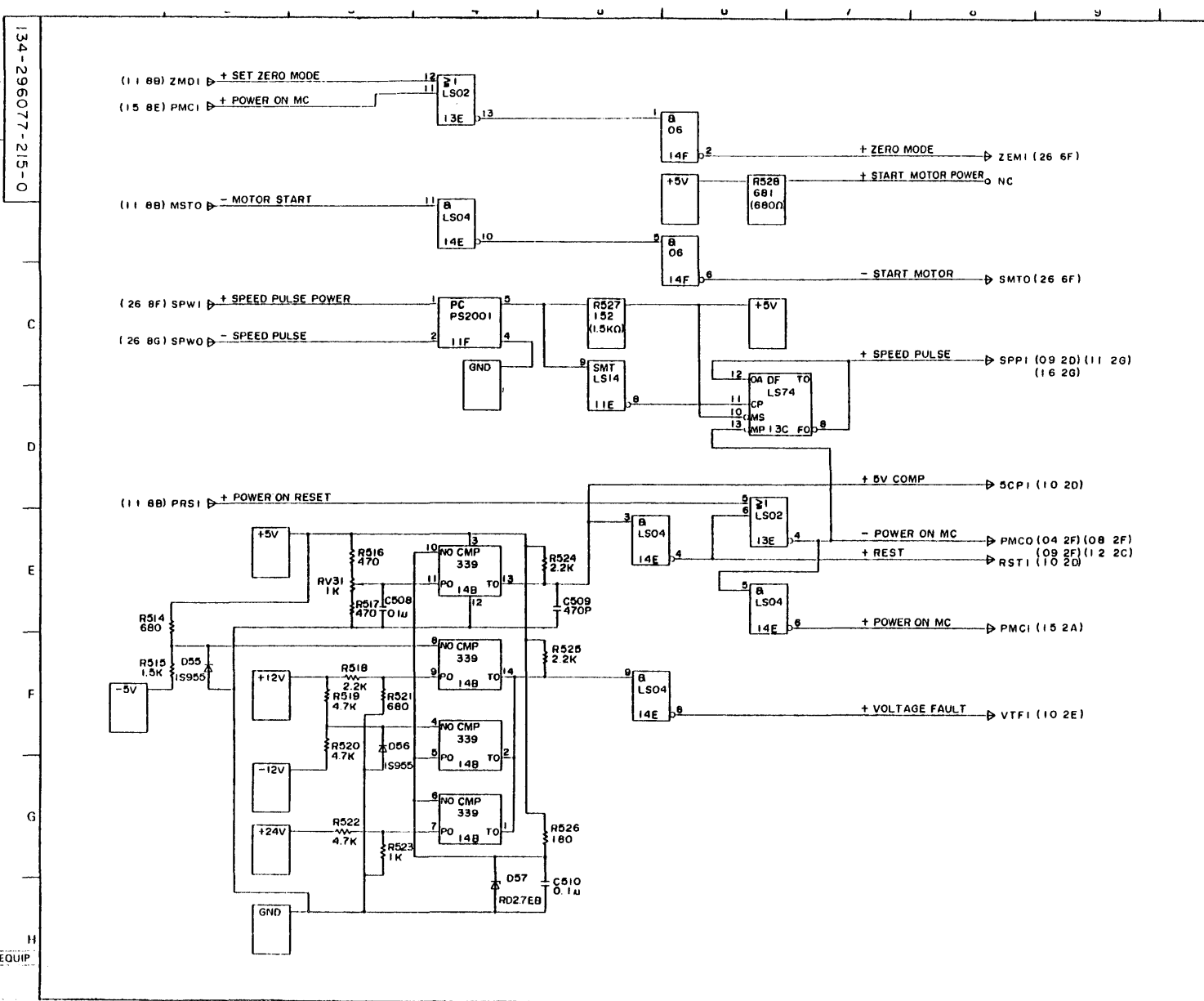
134-296077-214-0



REV	CONT	DESCRIPTION (SC)	APP
1	0	1982.3.31	

DWG ABBR	
PKG LOCATION	
PKG NAME	
214	
NEXT SPEC	
DRAFT	ENC
CHK	APP
ISSUE	
G9QSS PWA G9QST PWA (14/26)	
134-296077-214-0	
NEC	SMT /

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134-296077-215-0

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REV	COMP	DESCRIPTION (SC)	APP
1	0	1002.3.31	

DWG ABBR	
PKG LOCATION	
PKG NAME	
215	
NEXT SPEC	
DRAFT	ENG
CHK	APP
ISSUE	
G9QSS PWA G9OST PWA (15/26)	
134-296077-215-0	
NEC	SP

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134-296077-216-0

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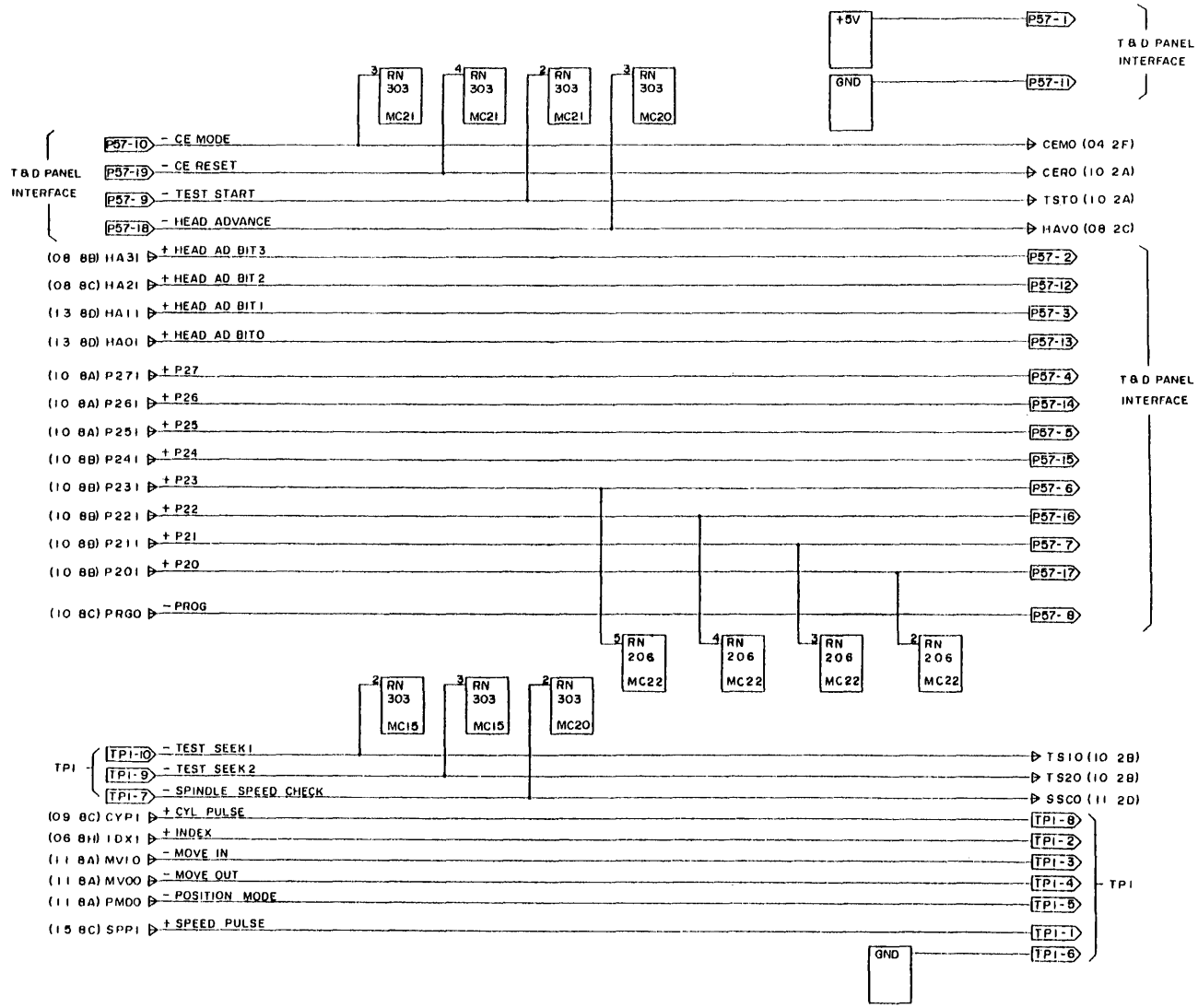
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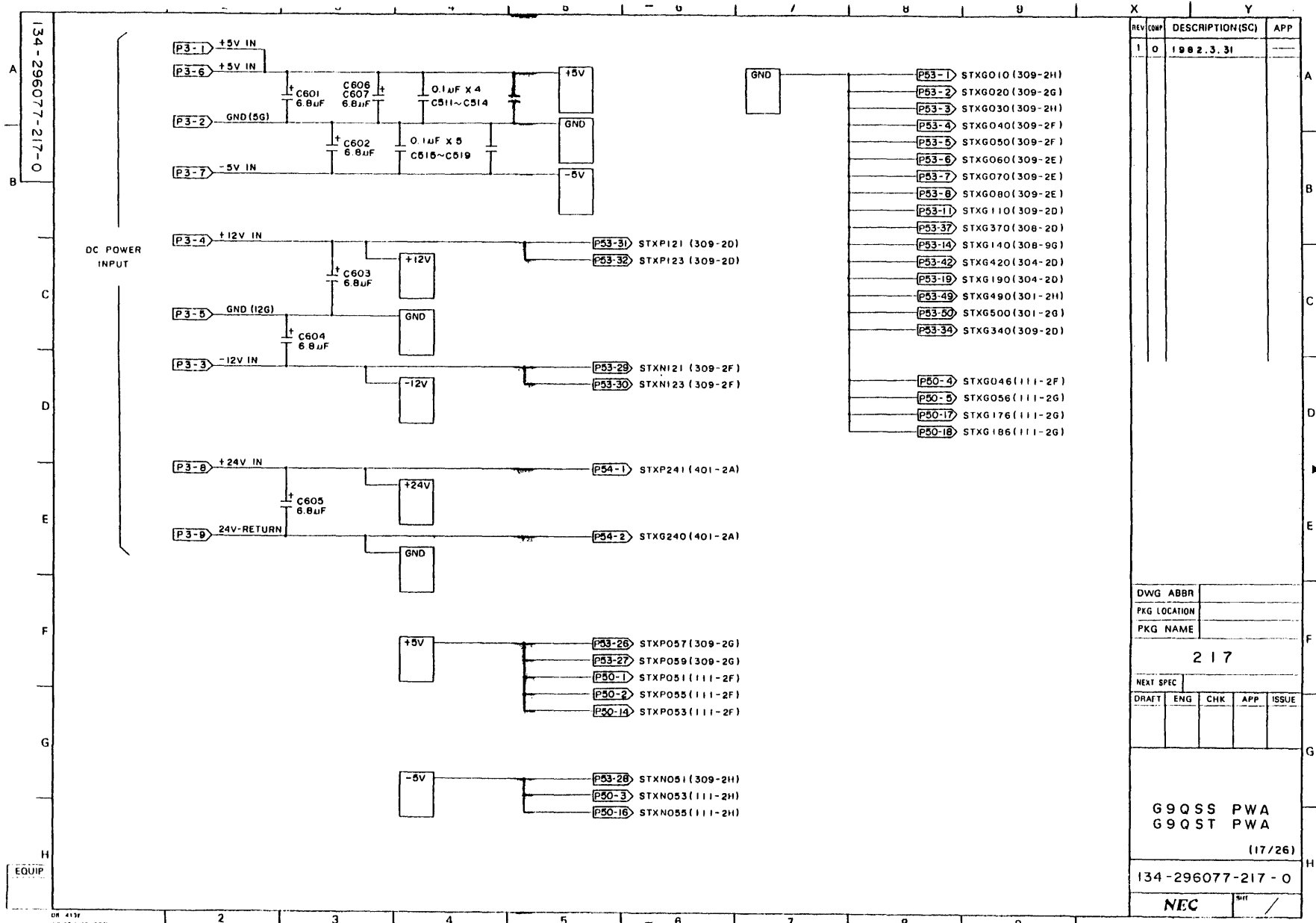


REV	DATE	DESCRIPTION (SC)	APP
1	0	1982.3.31	

DWG ABBR				
PKG LOCATION				
PKG NAME				
216				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
G9QSS PWA G9QST PWA (16/26)				
134-296077-216-0				
NEC				SWT

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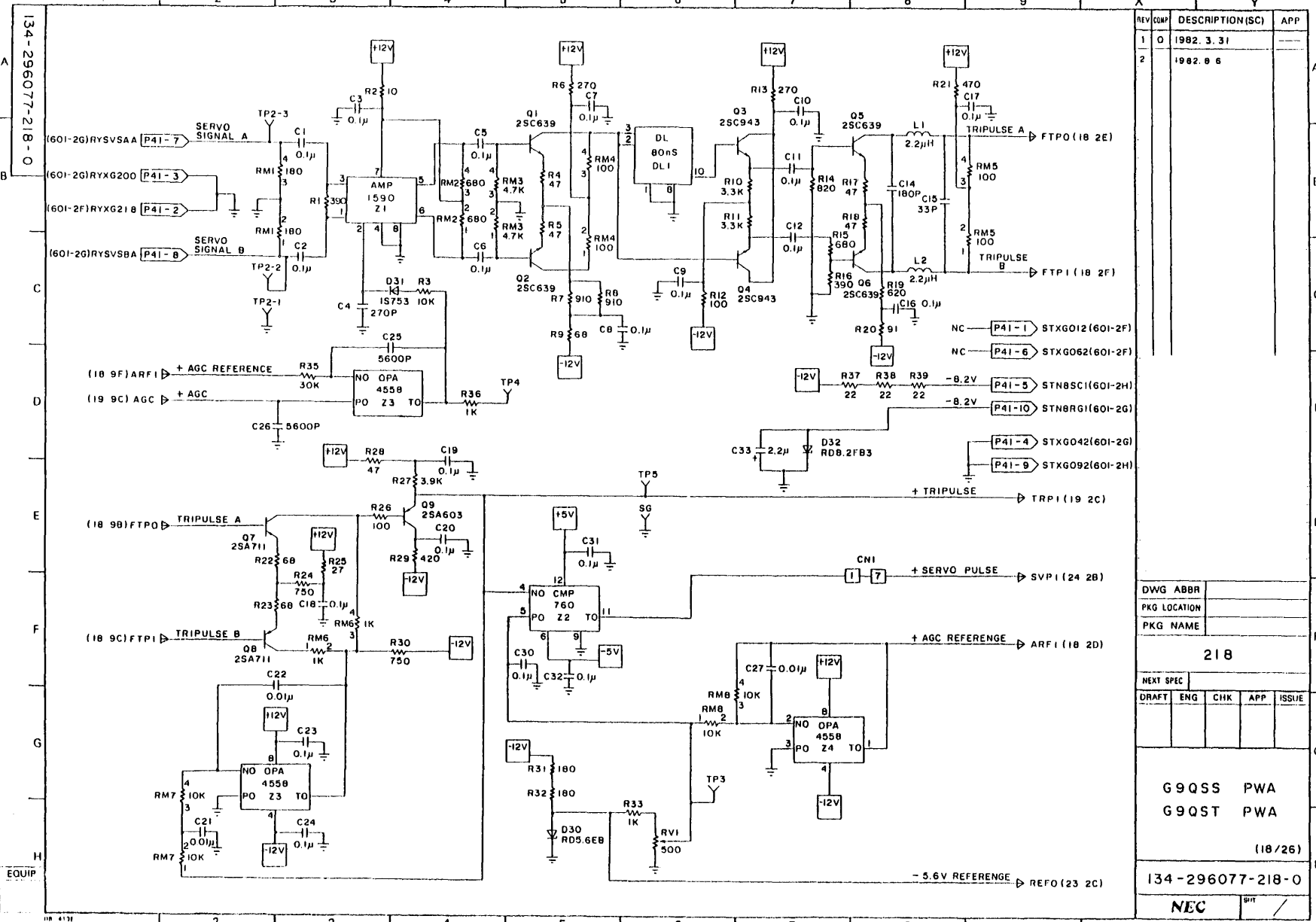


REV	COMP	DESCRIPTION (SC)	APP
1	0	1982.3.31	

DWG ABBR				
PKG LOCATION				
PKG NAME				
217				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
G9QSS PWA G9QST PWA (17/26)				
134-296077-217-0				
NEC				/

OR 4137
NS 42 (2/70-644)

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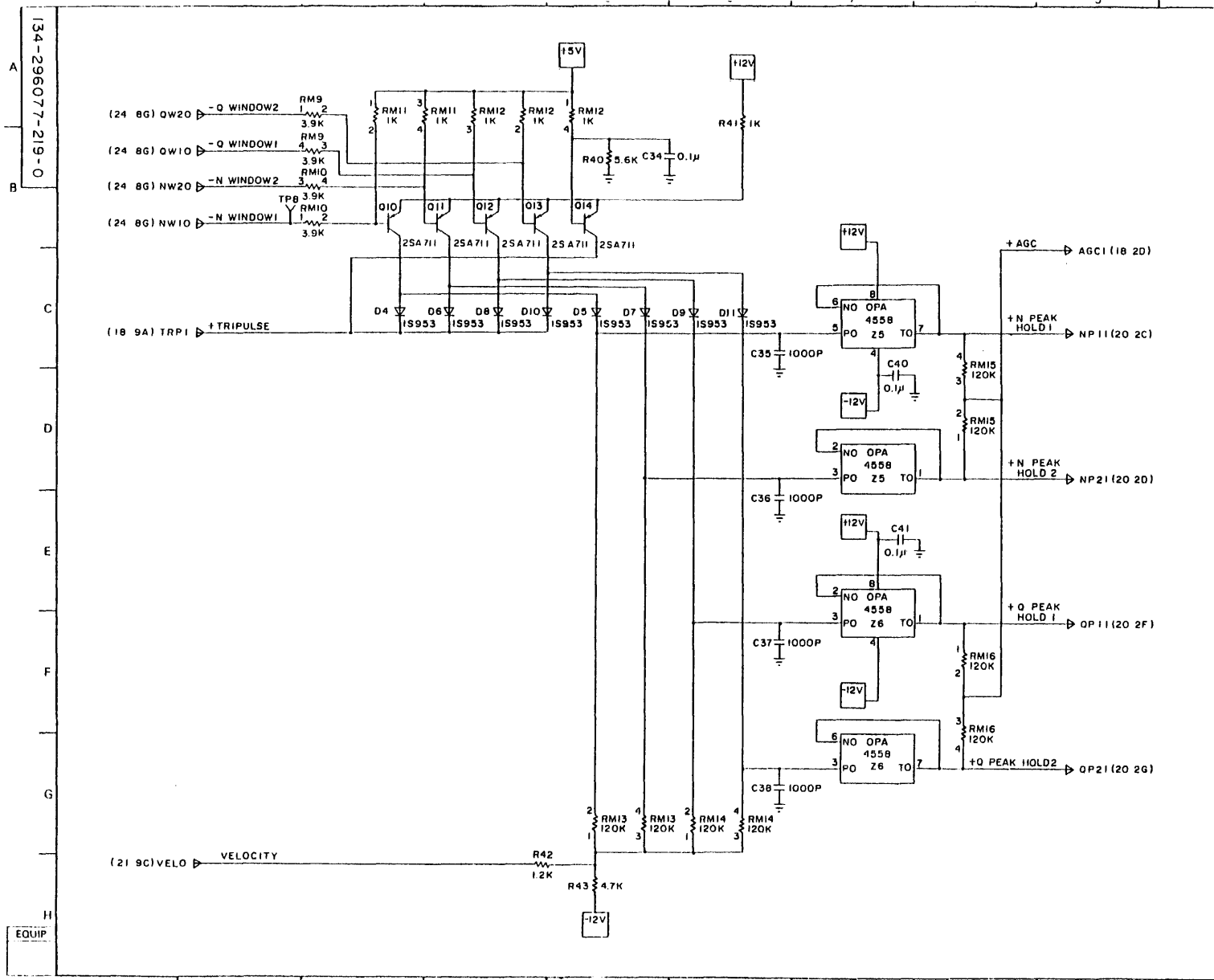


REV	COMP	DESCRIPTION (SC)	APP
1	0	1982. 3. 31	
2		1982. 8. 6	

DWG ABBR	
PKG LOCATION	
PKG NAME	
218	
NEXT SPEC	
DRAFT	ENG
CHK	APP
ISSUE	
G9QSS PWA G9QST PWA (18/25)	
134-296077-218-0	
NEC	

EQUIP

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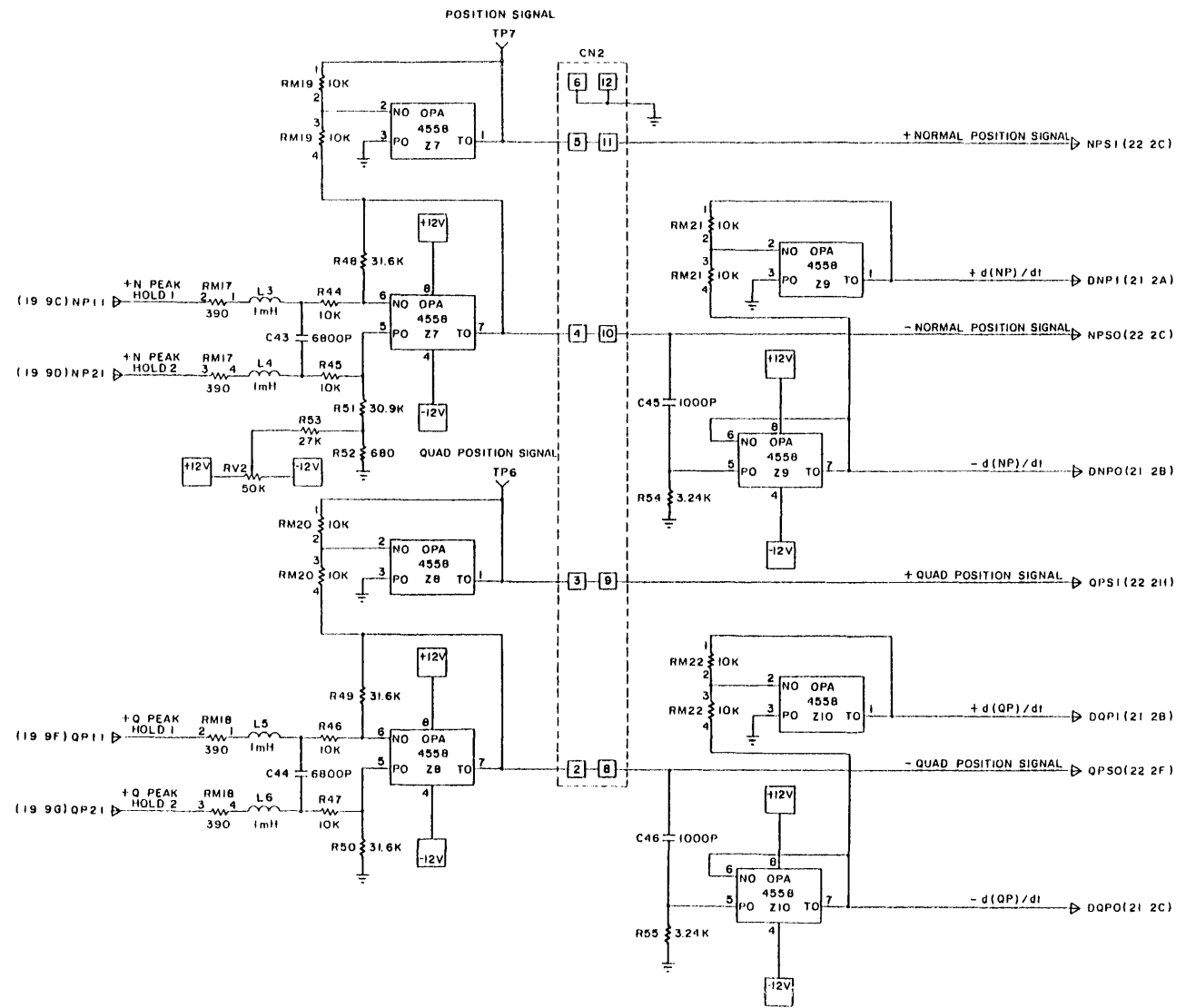
REV	COMP	DESCRIPTION (ISC)	APP
1	0	1982.3.31	

DWG ABBR	
PKG LOCATION	
PKG NAME	
219	
NEXT SPEC	
DRAFT	ENG
CHK	APP
ISSUE	
G9QSS PWA G9QST PWA (19/26)	
134-296077-219-0	
NEC	

Number Electric Co Ltd

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REV	DATE	DESCRIPTION (SC)	APP
1	0	1982 3 31	

DV '3	ABBR	
PKG	LOCATION	
PKG	NAME	

220

NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE

G9QSS	PWA
G9QST	PWA

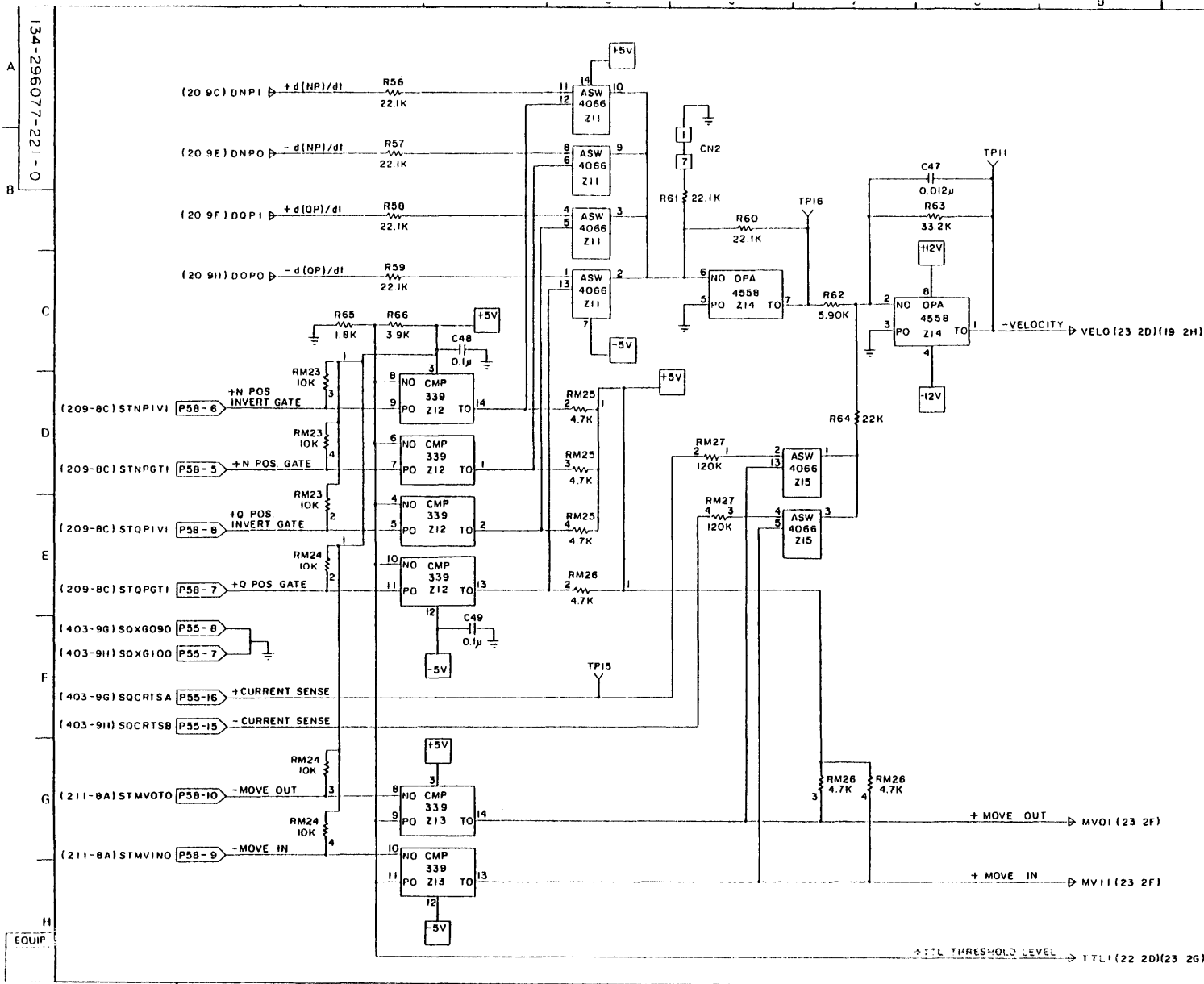
(20/26)

134-296077-220-0

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REV	COMP	DESCRIPTION(SC)	APP
1	0	1982.3.31	
2		1982.8.6	

DWG ABBR	
PKG LOCATION	
PKG NAME	
221	
NEXT SPEC	
DRAFT	
ENG	
CHK	
APP	
ISSUE	
G9QSS PWA G9QST PWA	
(21/26)	
134-296077-221-0	
NEC	SH

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EQUIP

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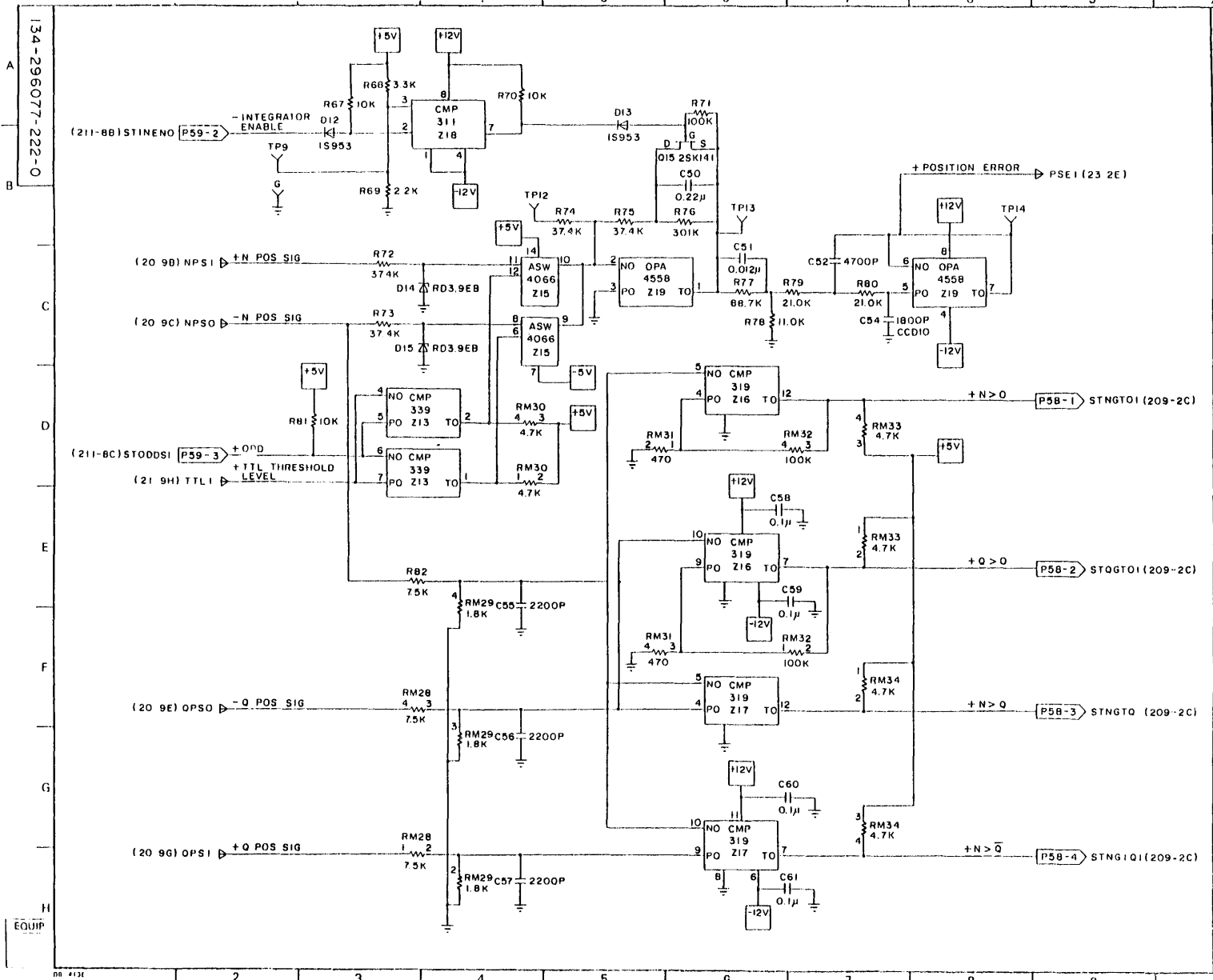
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134-296077-221-0

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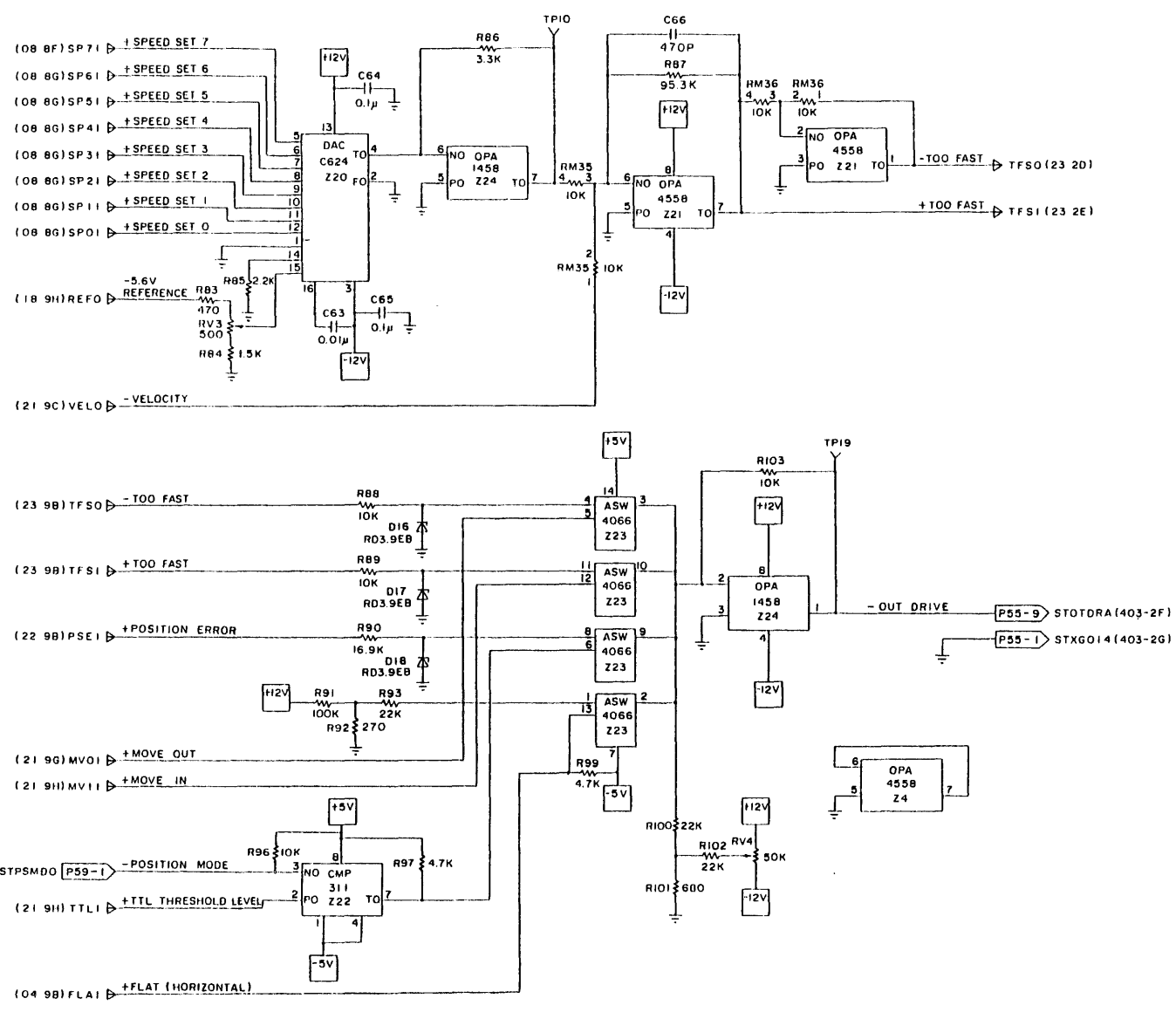
REV	COMP	DESCRIPTION (SC)	APP
1	0	1982.3.31	

DWG ABBR	
PKG LOCATION	
PKG NAME	
222	
NEXT SPEC	
DRAIT	ENG
CHK	APP
ISSUE	
G9QSS PWA G9QST PWA	
(22/26)	
134-296077-222-0	
MEC	

NO. 4130
REV. 12-1978

2 3 4 5 6 7 8 9

134-296077-223-0

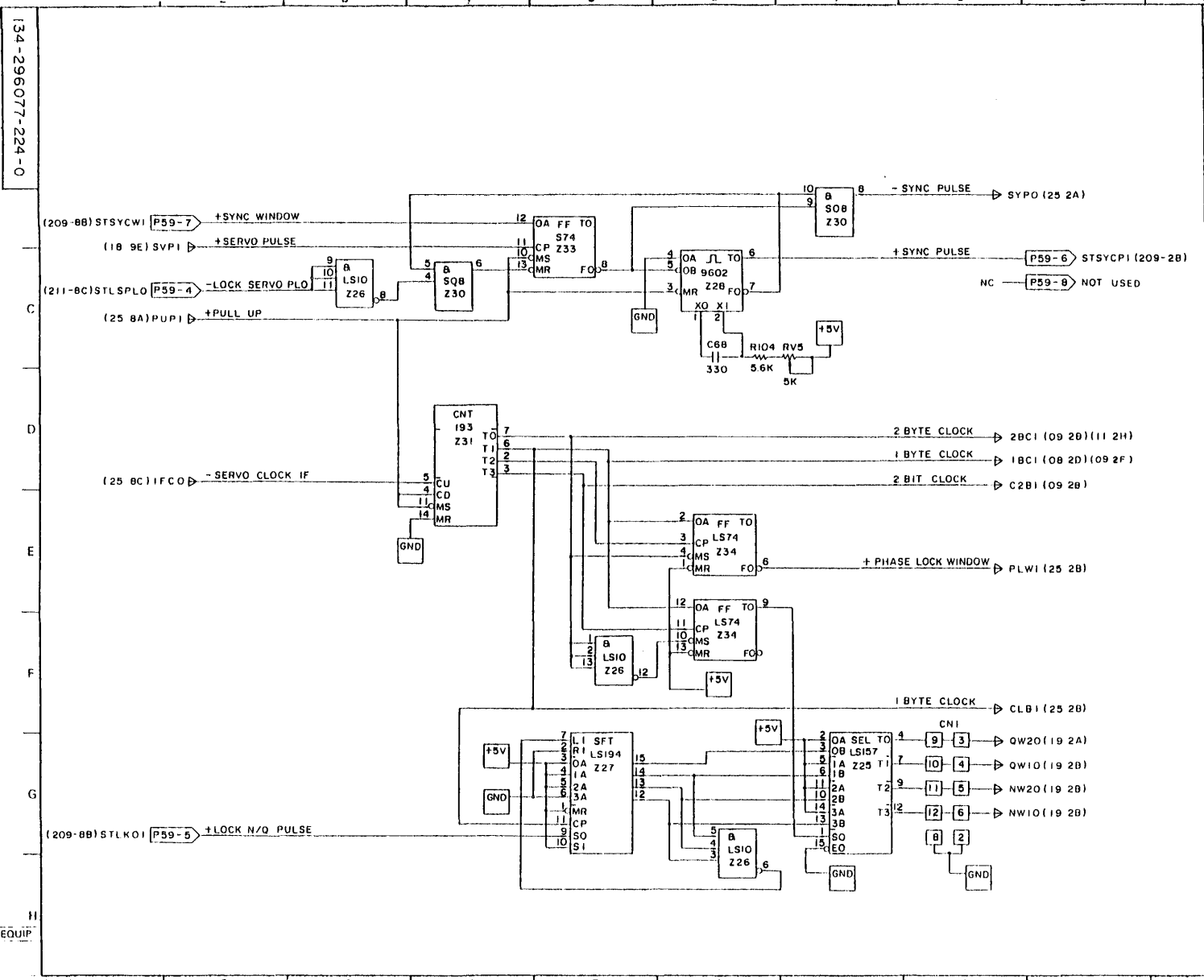


REV	COMP	DESCRIPTION (SC)	APP
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2		1982.8.6	

DWG ABBR	
PKG LOCATION	
PKG NAME	
223	
NEXT SPEC	
DRAFT	ENG
CHK	APP
ISSUE	
G9QSS PWA G9QST PWA	
(23/26)	
134-296077-223-0	
NEC	

A-40

A-41



REV	COMP	DESCRIPTION (ISC)	APP
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DWG ABBR	
PKG LOCATION	
PKG NAME	

224

NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE

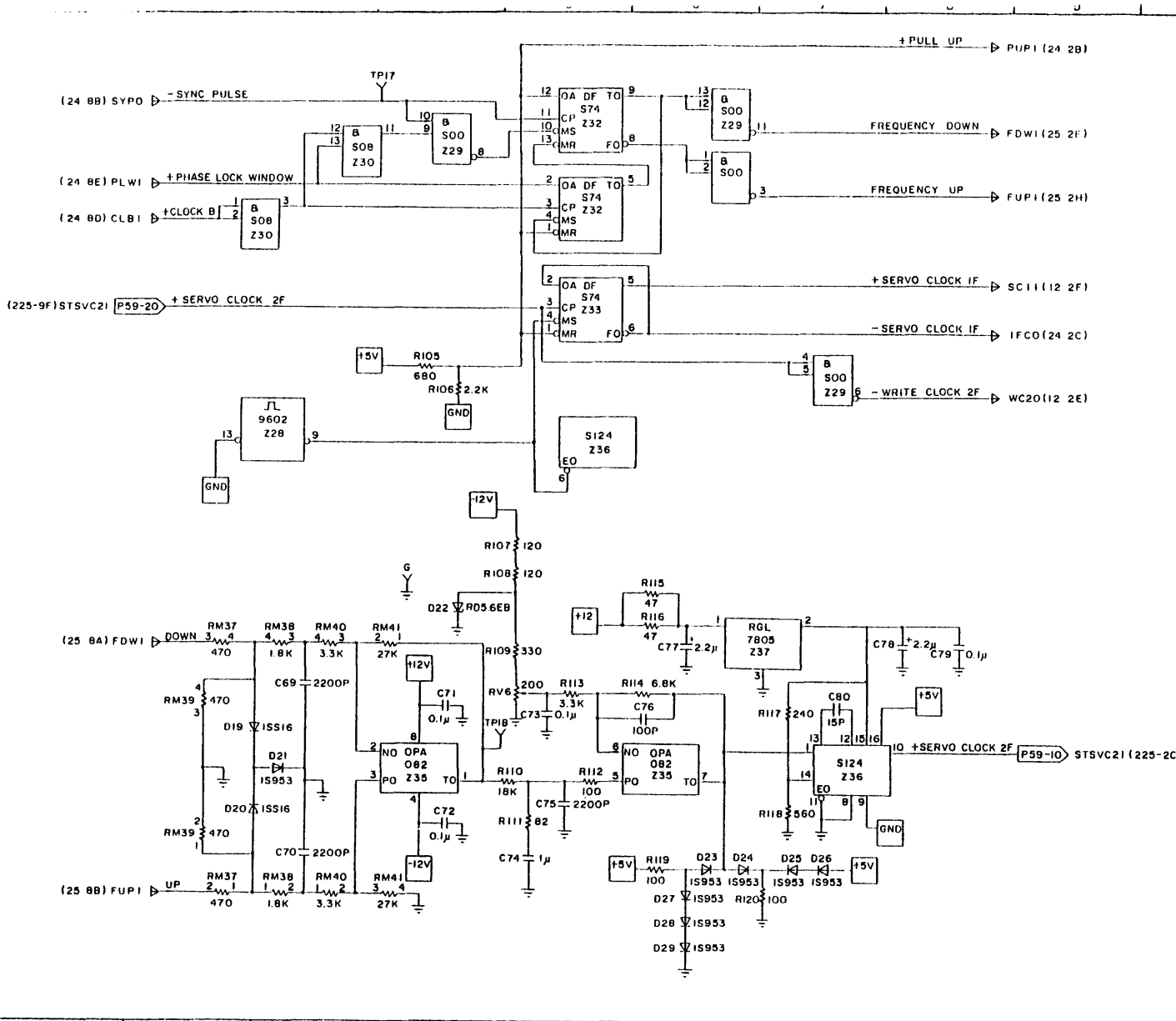
G9QSS	PWA
G9QST	PWA

(24/26)

134-296077-224-0

NEC

134-296077-225-0
A
B
C
D
E
F
G
H
EQUIP



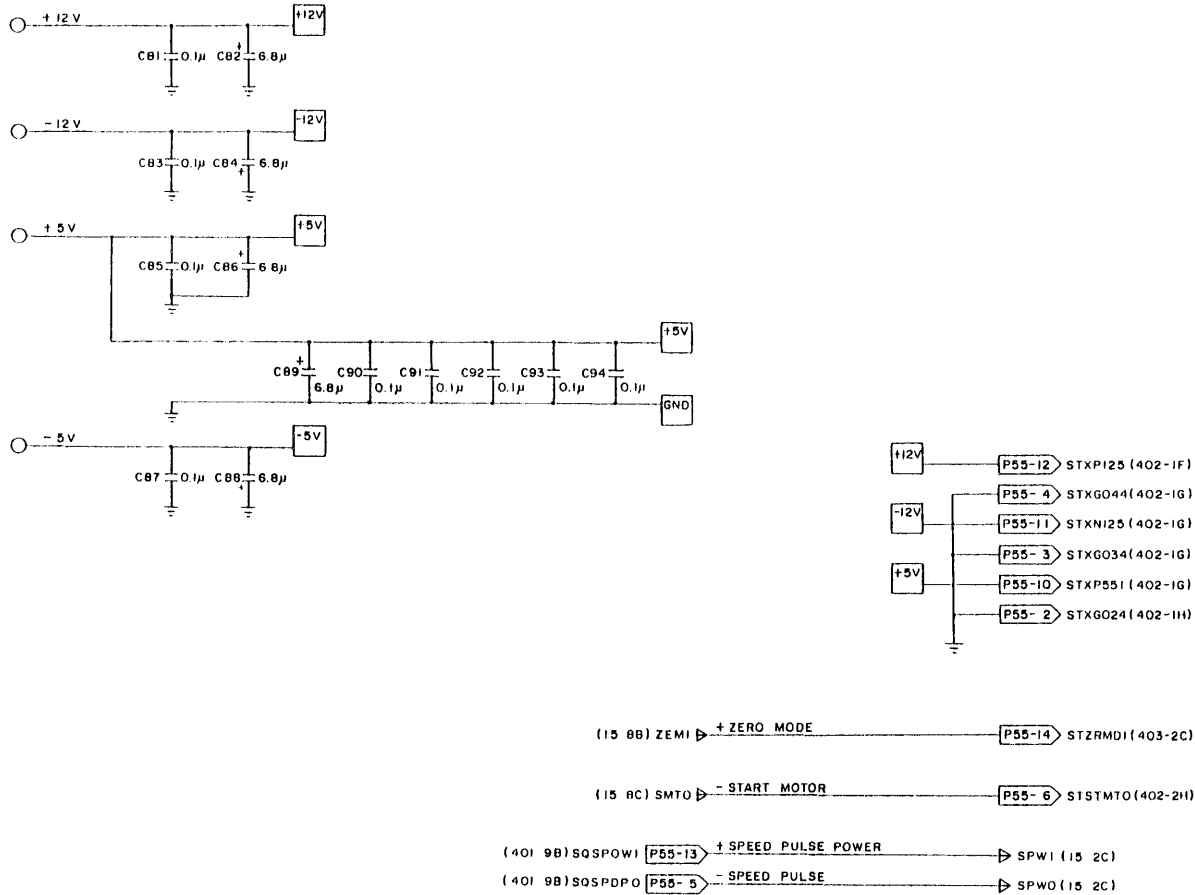
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PKG LOCATION	
PKG NAME	
225	
NEXT SPEC	
DRAFT	ENG
CHK	APP
ISSUE	
G9QSS PWA G9QST PWA (25/26)	
134-296077-225-0	
NEC	

A-42

DR 4134
DK 42 (25) 4461

134-296077-226-0



REV	DATE	DESCRIPTION (SC)	APP
1	0	1982.3.31	

DWG ABBR				
PKG LOCATION				
PKG NAME				
226				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
G9QSS PWA G9QST PWA				
(26/26)				
134-296077-226-0				
NEC				SMT /

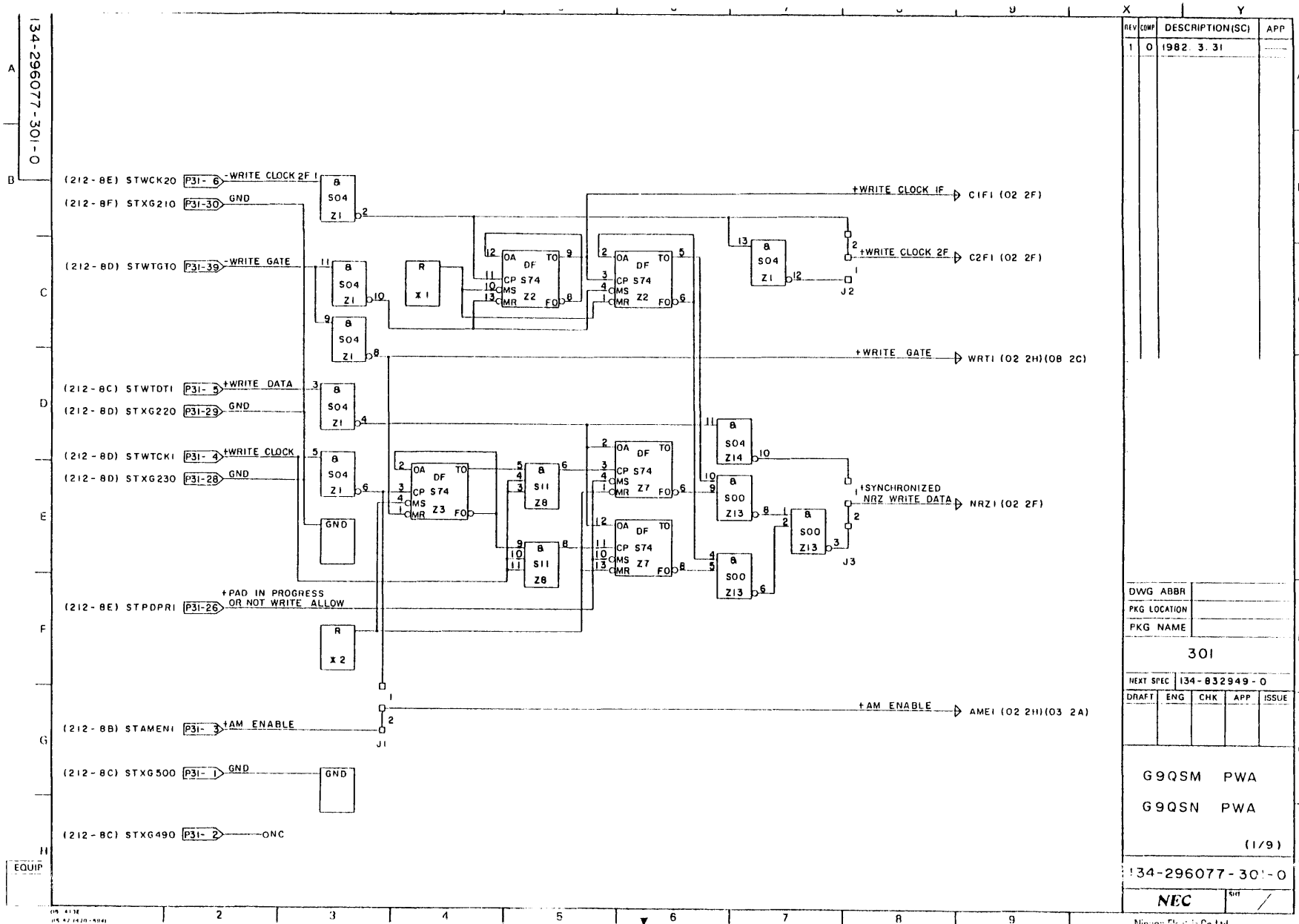
A-43

EQUIP

DATE: 1982.3.31

Revision: 1 of 1

A-44



REV	COMP	DESCRIPTION(S)	APP
1	0	1982 3 31	

DWG ABBR	
PKG LOCATION	
PKG NAME	

301

NEXT SPEC	134-832949-0			
DRAFT	ENG	CHK	APP	ISSUE

G9QSM PWA
G9QSN PWA
(1/9)

134-296077-301-0

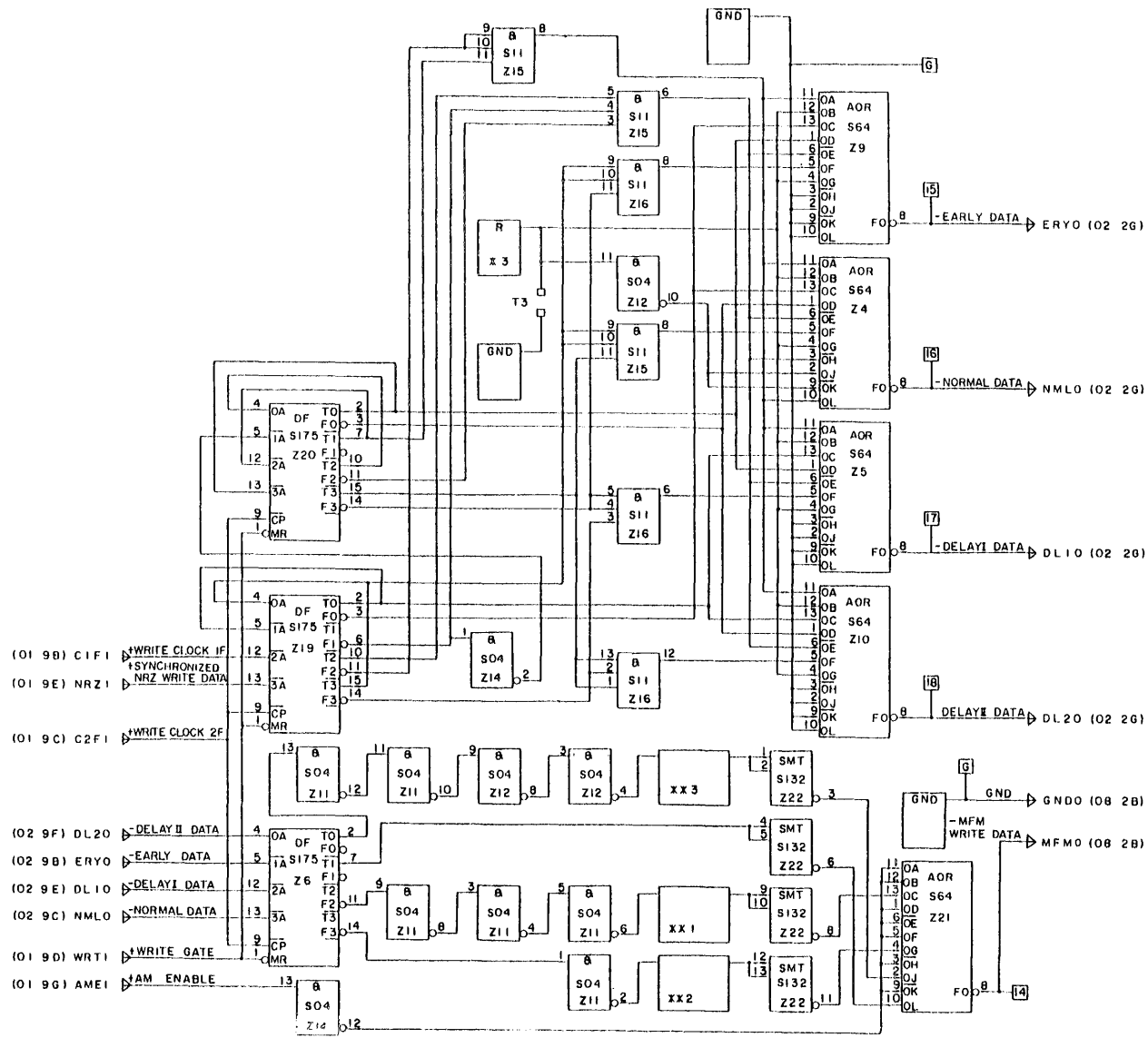
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OP 4134
10-82-1010-0001

Rev. 1.0

134-296077-302-0

A-45



REV	COMP	DESCRIPTION (SC)	APP
1	0	1982.3.31	
1		1982.8.6	

DWG ABBR	
PKG LOCATION	
PKG NAME	

302

NEXT SPEC	
DRAFT	ENG
CHK	APP
ISSUE	

G9QSM PWA
G9QSN PWA

(2/9)

134-296077-302-0

NEC

HW 4118
DL 43 2876, 4-72

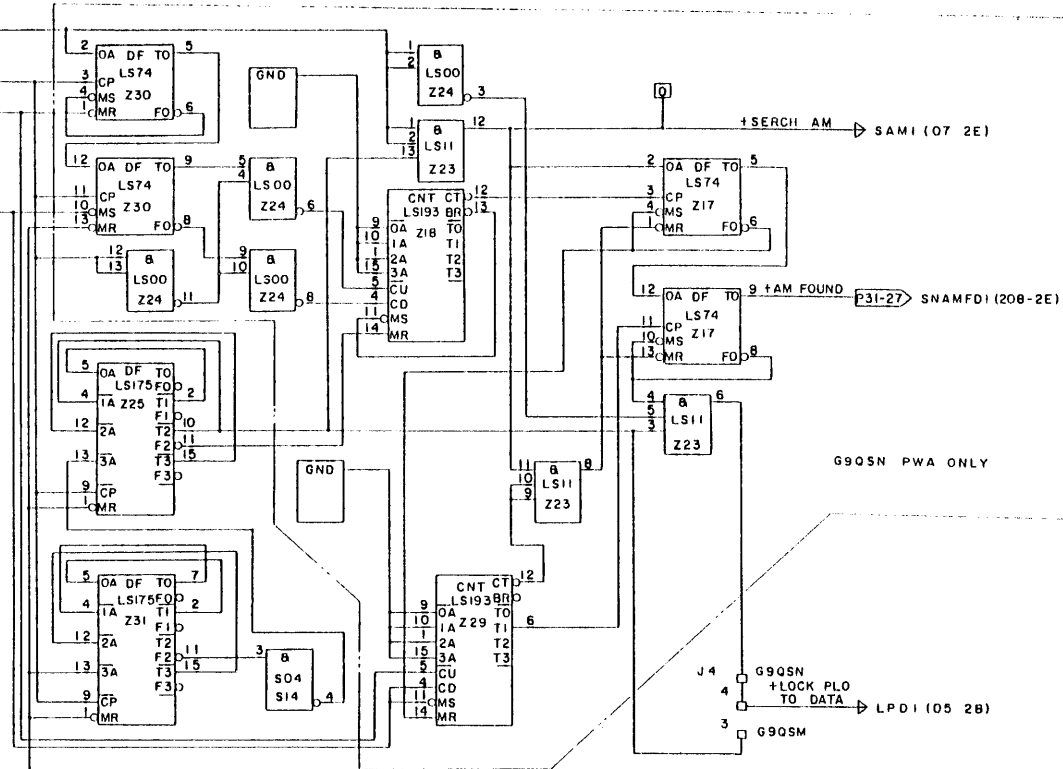
134-296077-303-0

A-46

(01 9G) AMEI ▷ + AM ENABLE
 (04 9G) BICO ▷ - BIT CLOCK
 (04 9A) RDTO ▷ - RAW READ DATA

R
x4

(212-88) STRDGT0 [P31-33] + READ GATE



J4
 4 G9QSN +LOCK PLO TO DATA
 4
 3 G9QSM

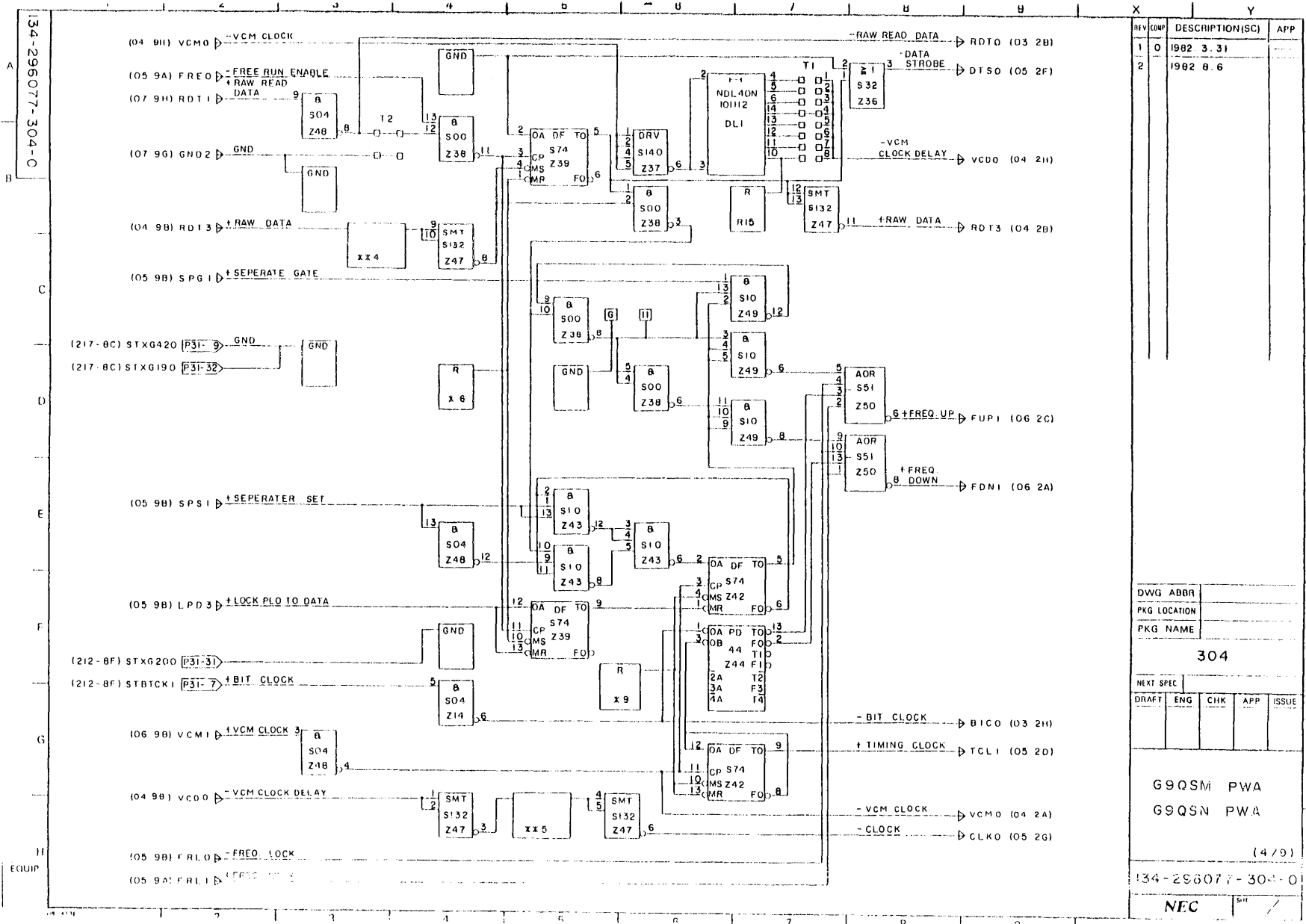
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1	0	1982.3.31	
2		1982.8.6	

DWG ABBR				
PKG LOCATION				
PKG NAME				
303				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
G9QSM PWA				
G9QSN PWA				
(3/9)				
134-296077-303-0				
NEC				

2 3 4 5 6 7 8 9

EQUIP

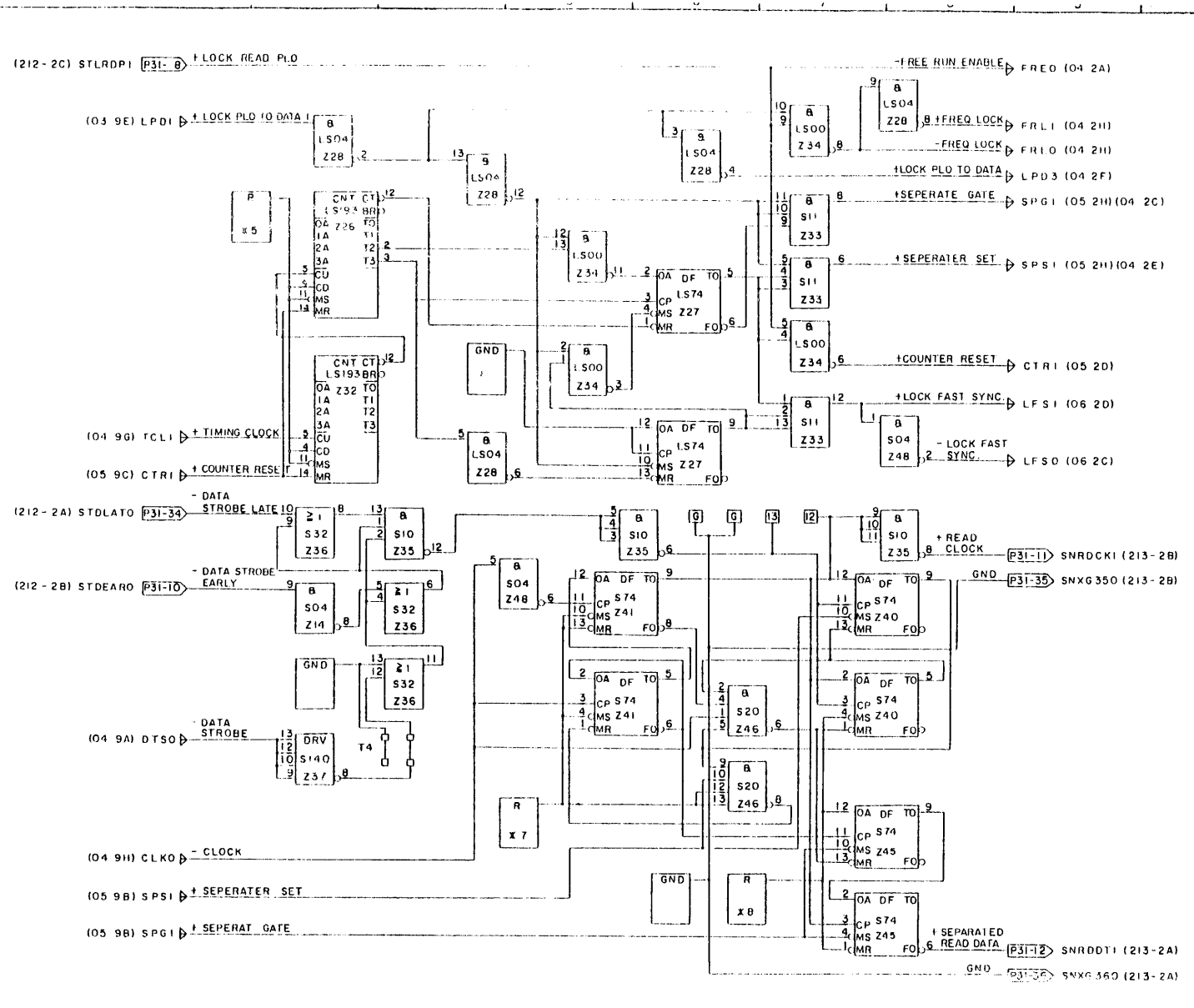
A-47



REV	COMP	DESCRIPTION (SC)	APP
1	0	1982 3. 31	
2		1982 8. 6	

DWG ABBR				
PKG LOCATION				
PKG NAME	304			
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
G9QSM PWA				
G9QSN PWA				
(4/9)				
134-296077-304-0				
NEC				

134-296077-305-0



REV	DATE	DESCRIPTION(S)	APP
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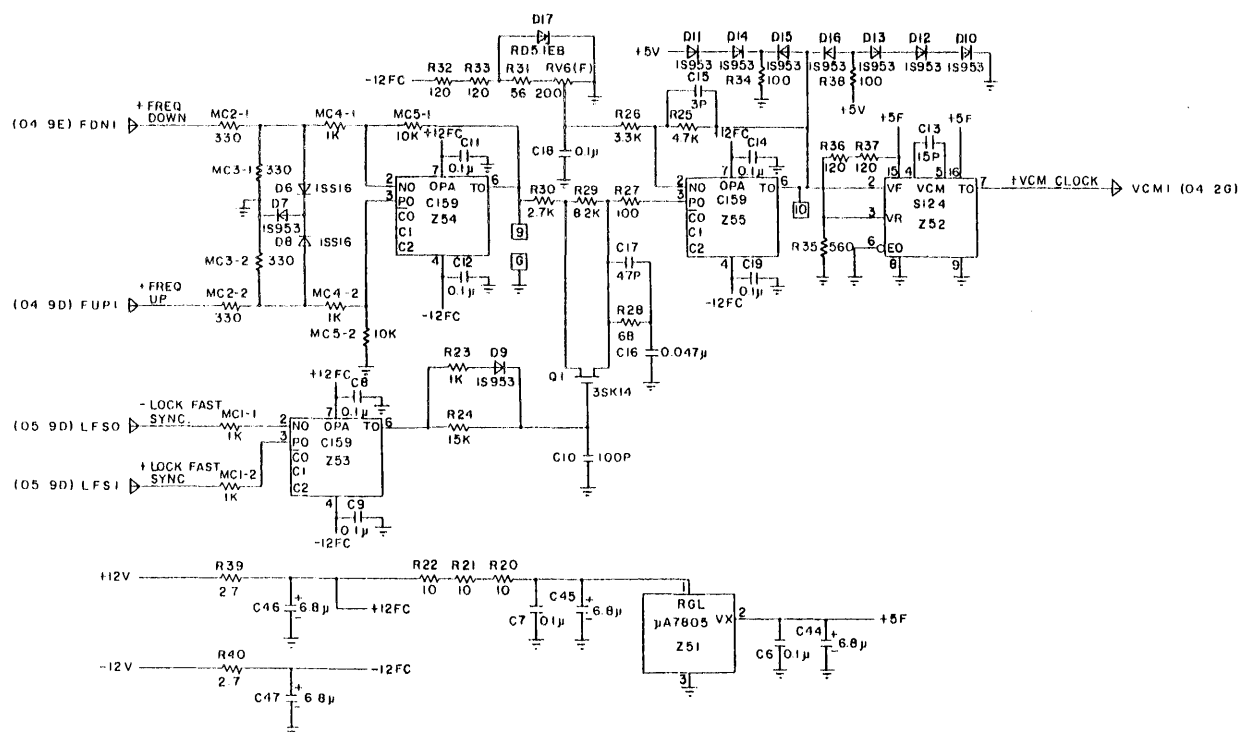
DWG ADDR				
PKG LOCATION				
PKG NAME	305			
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
G9QSM PWA				
G9QSN PWA				
(5/9)				
134-296077-305-0				
NEC				

Nihon Electric Co Ltd

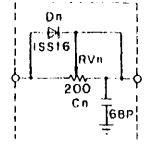
A-48

OR 4136
MS 47 1750-1441

134-296077-306-0

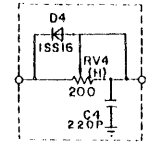


XX1~XX3 詳細図

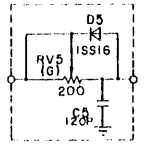


	Dn	RVn	Cn
XX1	D1	RV1	C1
XX2	D2	RV2	C2
XX3	D3	RV3	C3

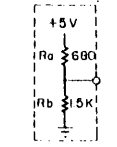
XX4 詳細図



XX5 詳細図

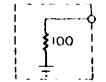


X1~X9 詳細図



	R0	Rb
X1	R2	R1
X2	R4	R3
X3	R6	R5
X4	R8	R7
X5	R10	R9
X6	R12	R11
X7	R14	R13
X8	R17	R16
X9	R19	R18

R15 詳細図



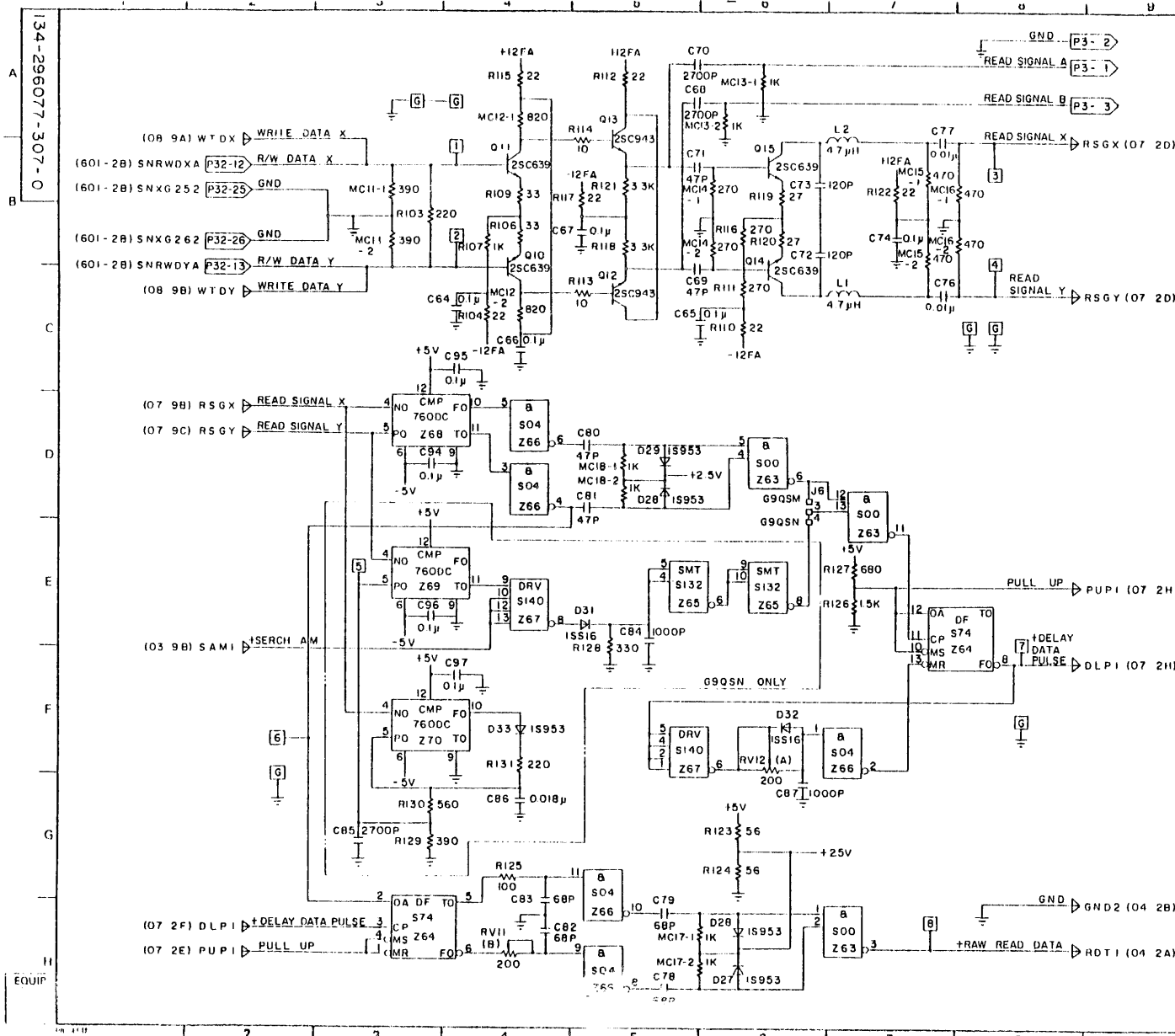
REV	COMP	DESCRIPTION (ISC)	APP
1	0	1982.3.31	

DWG ANBR				
PKG LOCATION				
PKG NAME				
306				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
G9QSM PWA				
G9QSN PWA				
(6/9)				
134-296077-306-0				
NEC				

A-49

EQUIP

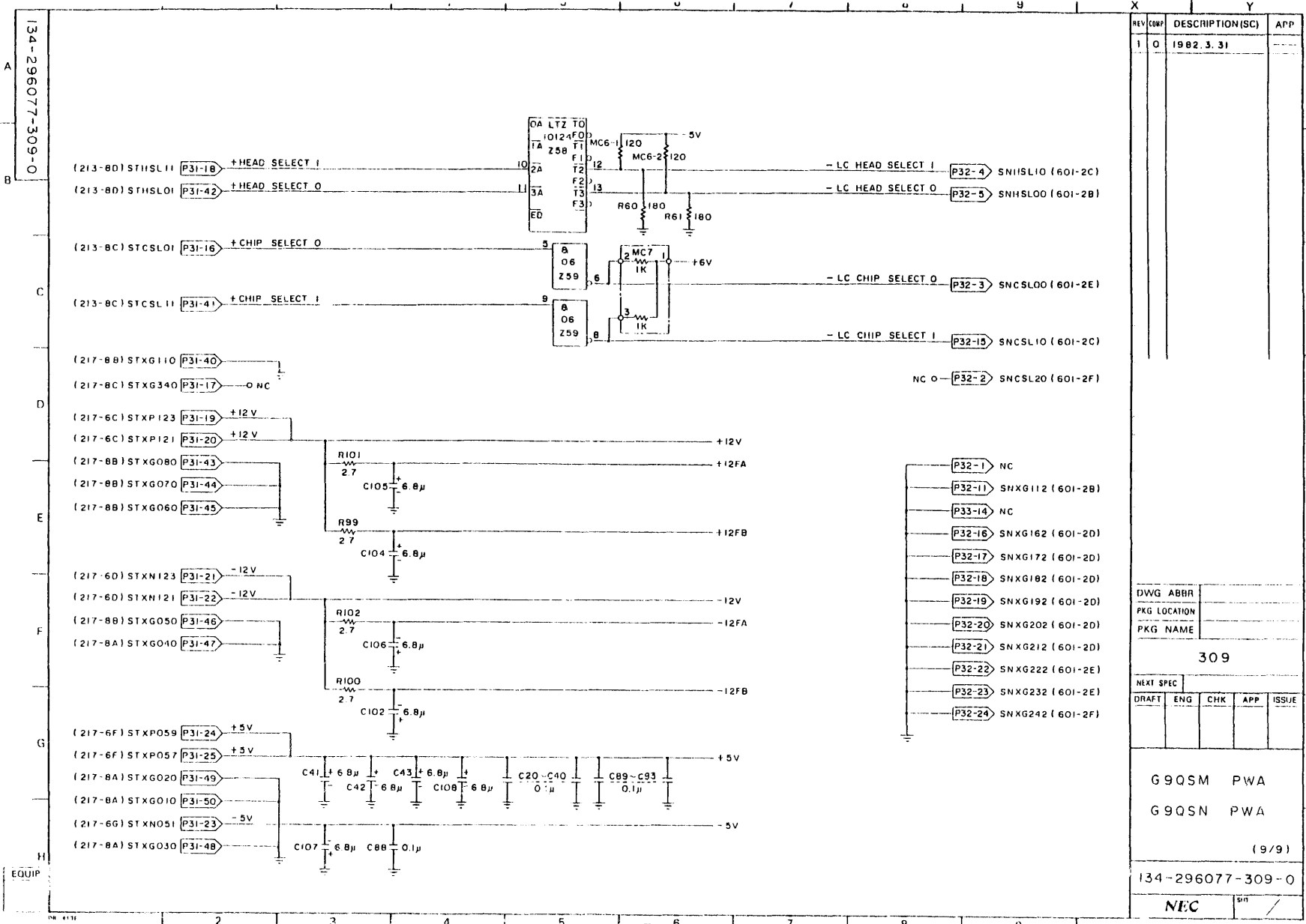
A-50



REV	COMP	DESCRIPTION (ISC)	APP
1	0	1982 3. 31	

DWG ABBR				
PKG LOCATION				
PKG NAME				
307				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
G9QSM PWA G9QSN PWA (7/9)				
134-296077-307-0				
NEC				511

A-52



REV	COMP	DESCRIPTION (SC)	APP
1	0	1982.3.31	

DWG ABBR	
PKG LOCATION	
PKG NAME	

309

NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE

G9QSM PWA
G9QSN PWA
(9/9)

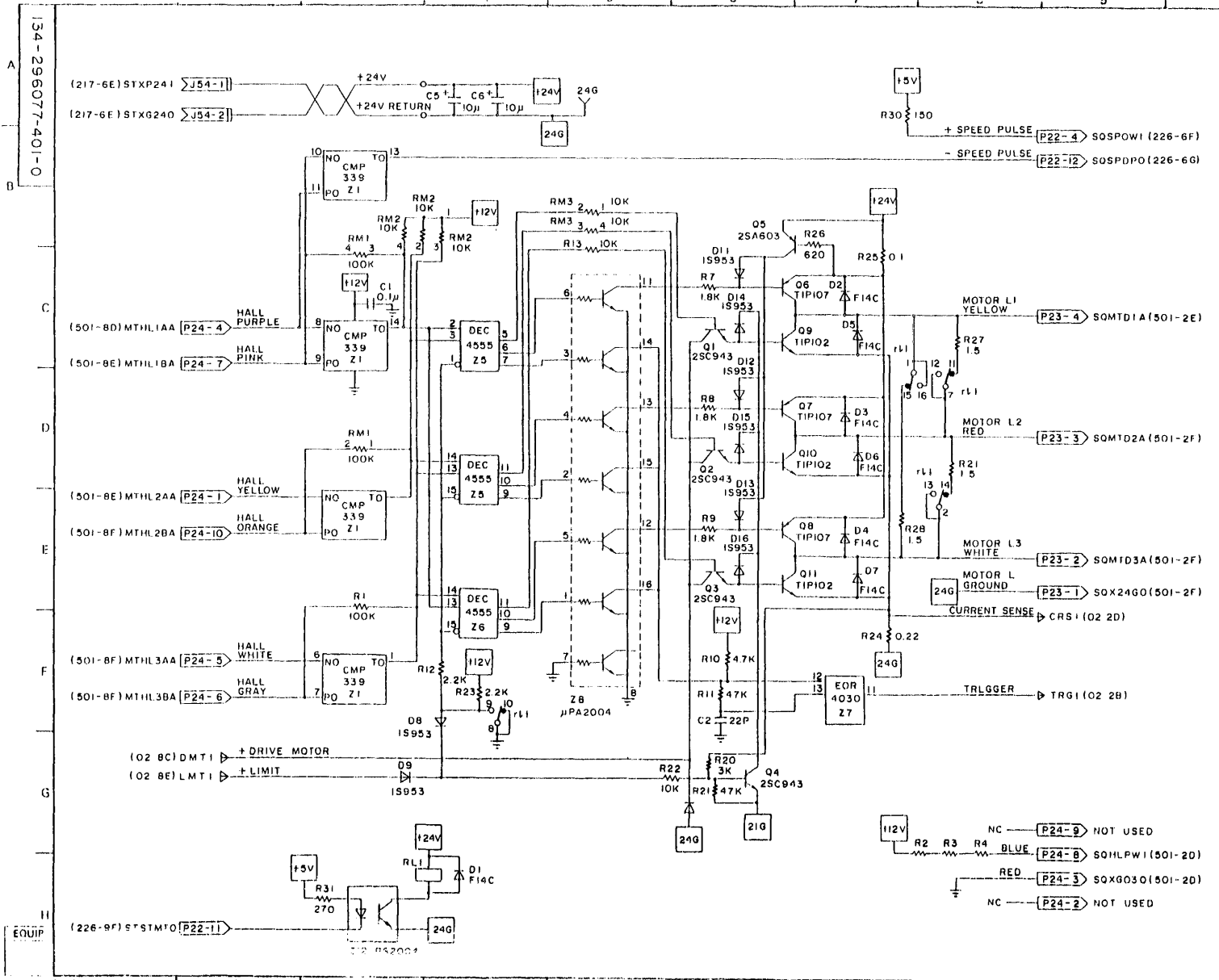
134-296077-309-0

NEC

134-296077-309-0

EQUIP

A-53



REV	DATE	DESCRIPTION (SC)	APP
1	0	1982.3.31	

DWG ABBR	
PKG LOCATION	
PKG NAME	

4 0 1

NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE

G9QSQ PWA

(1/3)

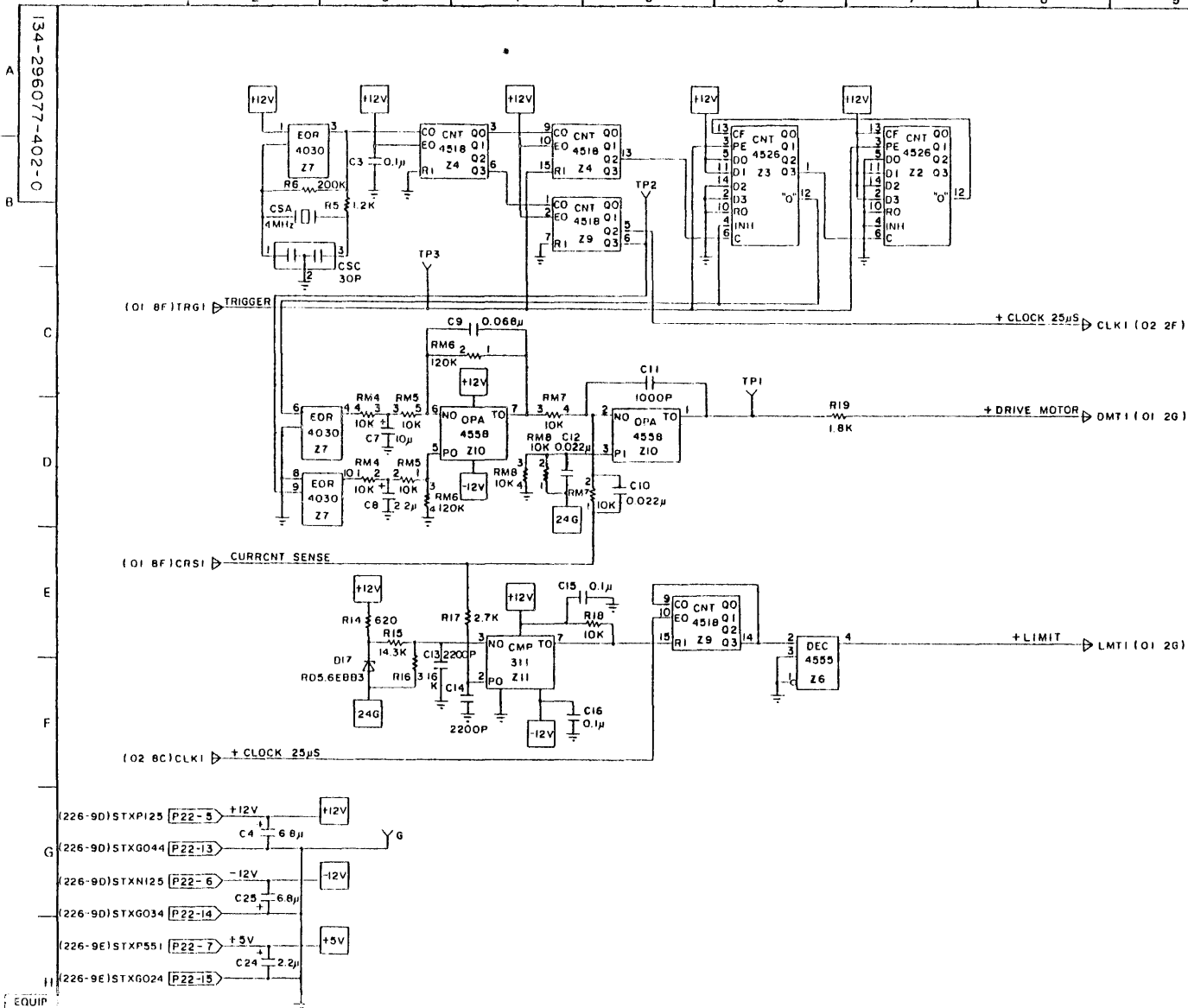
134-296077-401-0

NEC NEW ELECTRIC CO. INC.

08 4176
10 42 10/11/88

NEW ELECTRIC CO. INC.

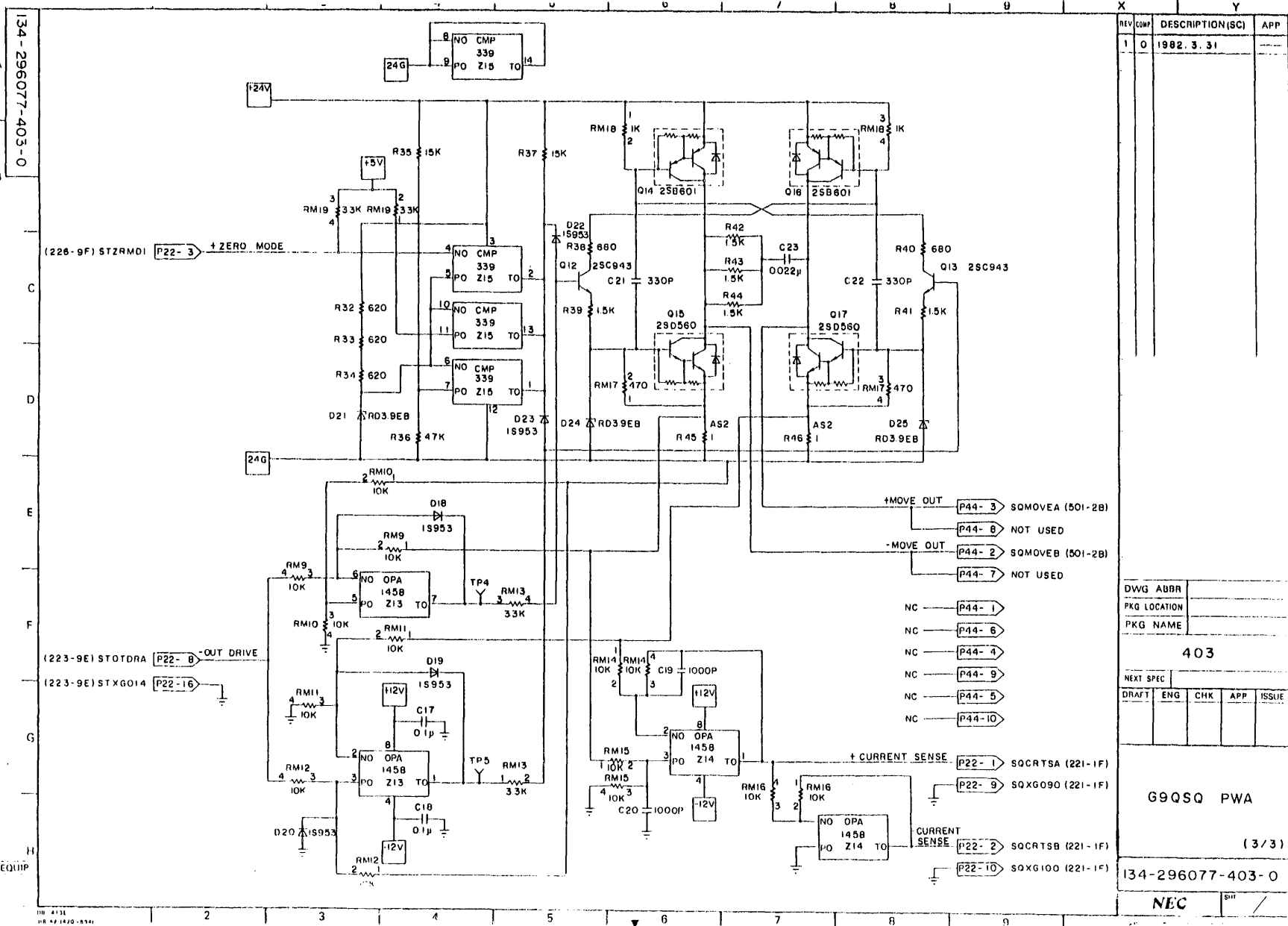
A-54



REV	DATE	DESCRIPTION (SC)	APP
1	0	1982.3.31	

DWG ABBR				
PKG LOCATION				
PKG NAME				
402				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE
G9QSQ PWA				
(2/3)				
134-296077-402-0				
				SHI /

A-55

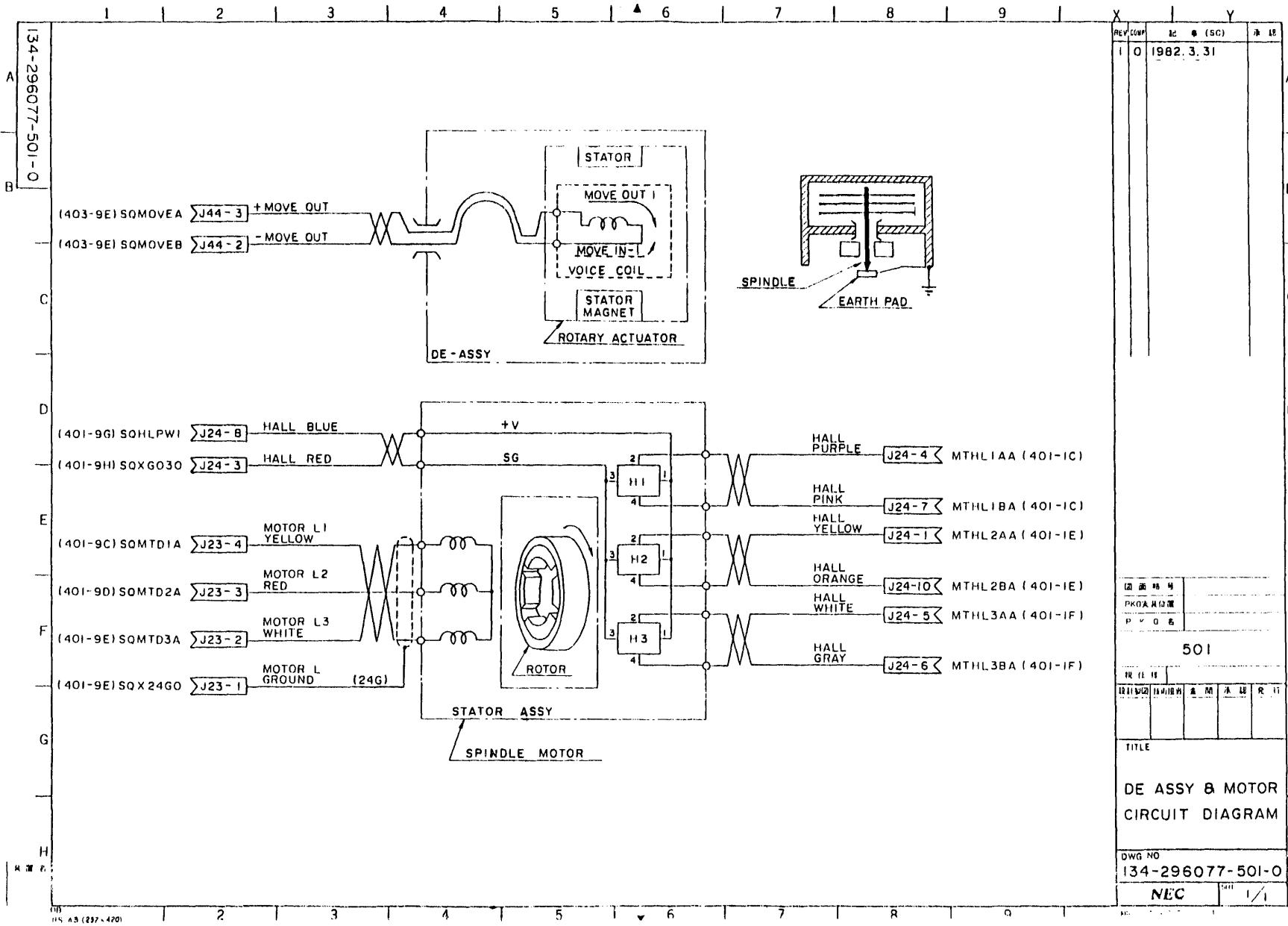


REV	COMP	DESCRIPTION (SC)	APP
1	0	1982.3.31	

DWG ABBR				
PKG LOCATION				
PKG NAME				
403				
NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE

G9QSQ PWA	
(3/3)	
134-296077-403-0	
NEC	SH

A-56



REV	COMP	DATE	BY (SO)	CHK
1	0	1982.3.31		

圖面號碼	501
PKDA 員位置	
P 0 6	

規 格 書	
材 質 表	
組 立 圖	
檢 查 表	
備 註	

TITLE

**DE ASSY & MOTOR
CIRCUIT DIAGRAM**

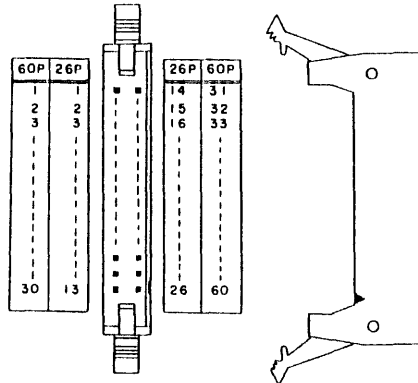
DWG NO
134-296077-501-0

NEC 1/1

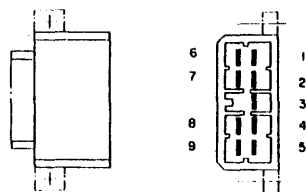
A-58

134-296076-022-0

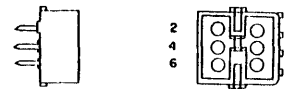
INTERFACE CONNECTORS



POWER CONNECTOR



3-DC INPUTS OPTION



REV	COMP	DESCRIPTION (SC)	APP
1	0	1982.3.31	
2		1982.8.6	

DWG ABBR	
PKG LOCATION	
PKG NAME	

NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE

INTERFACE CONNECTOR
a
POWER CONNECTOR

134-296076-022-0

NEC SHEET 1/1

EQUIP

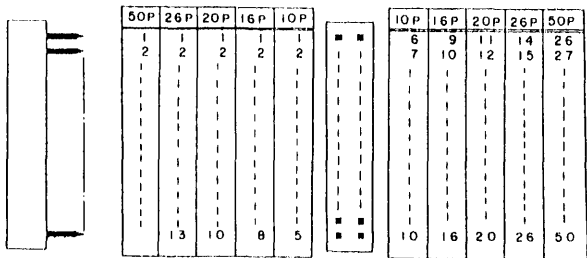
DRN 4134
REV 22-11-80-1060

2 3 4 5 6 7 8 9

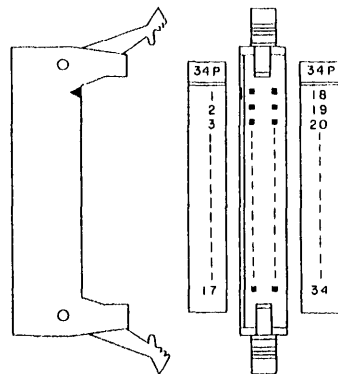
A-59

134-296076-021-0

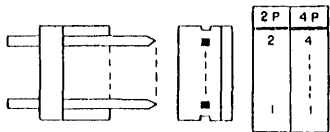
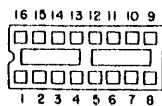
CONNECTORS PIN LAYOUT



PWA	10P	16P	20P	26P	50P
G9QSW				P60	
G9QSS	P56	P55	P59 P58 P57	P50	P53
G9QSM				P32	P31
G9QSQ	P24 P44	P22			



DE ASSY (PII)



PWA	2P	4P
G9QSS	P54	
G9QST		
G9QSQ		P23

PWA	16P
G9QST	J15C J15D
G9QSW	J15A J15B

REV	COMP	DESCRIPTION (SC)	APP
1	0	1982.3.31	

DWG ABBR	
PKG LOCATION	
PKG NAME	

NEXT SPEC				
DRAFT	ENG	CHK	APP	ISSUE

I/O CONNECTORS

134-296076-021-0

NEC SH 1/1

Appendix B

Specifications

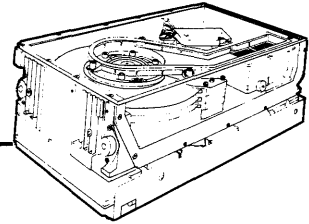


Table B-1 Operating Specifications

FEATURE	SPECIFICATION
General	
Start Time	Less than 30 seconds
Stop Time	Less than 20 seconds
Recording Mode	Modified Frequency Modulation (MFM)
Interface Mode	Nonreturn-to-Zero (NRZ)
Head Positioning	Closed servo rotary actuator using a tri-pulse pattern
Basic Power Requirements (No Options)	
Voltage and Current	+5 Vdc, 4.0 A -5 Vdc, 0.5 A +12 Vdc, 0.6 A -12 Vdc, 0.5 A +24 Vdc, 5.0 A (peak) 2.5 A (average running)
Power Dissipation	100W (average running) 150 W (peak starting, 20 seconds)
Heat Generation	86K calories/hour (average running)

Table B-1 Operating Specifications (cont'd)

FEATURE	SPECIFICATION
Environmental	
Temperature (Ambient) Operating Storage	41° to 104° F (5° to 40° C) 14° to 158° F (-10° to 70° C)
Temperature (Gradient/maximum) Operating Storage	18° F/hour (10° C/hour) 45° F/hour (25° C/hour)
Relative Humidity (No condensation) Operating Storage	20% to 80% relative humidity 10% to 90% relative humidity
Vibration Operating Storage	0.25 G 3.00 G
Shock Operating Storage	2 G (20 ms) 5 G (10 ms)

Table B-2 Design Specifications

MODEL D2246	
Unformatted Storage Capacity	
Per Unit (MB)	85.03
Per Cylinder (bytes)	122,880
Per Track (bytes)	20,480
Formatted Storage Capacity*	
Per Unit (MB)	68.02
Per Cylinder (bytes)	98,304
Per Track (bytes)	16,384
General	
Cylinders	692
Data Transfer Rate (MB/second)	1.198
Spindle Rotation (rpm)	3,510
Average Latency Time (ms)	8.55
Single Track Seek Time (ms)	7
Average Seek Time (ms)	25
Maximum Seek Time (ms)	50
Recording Density (bits/inch)	9,040
Track Density (tracks/inch)	720
Recording Disks	4
Data Heads	6
Servo Heads	1
*The capacity is calculated as: 256 bytes x 64 sectors x 692 cylinders x number of data heads	

Table B-3 Physical Dimensions

DIMENSIONS	BASIC UNIT	STANDARD ASSEMBLY*
Width	8.5 in. (217 mm)	8.8 in. (224 mm)
Height	5.5 in. (139 mm)	5.6 in. (143 mm)
Depth	16.5 in. (420 mm)	18.5 in. (470 mm)
Weight	28 lbs. (13 kg)	30 lbs. (14 kg)
*The standard assembly includes a frame bracket.		

Table B-4 Interface Cable Descriptions

FEATURE	CABLE A	CABLE B
Type	Flat cable, 30 twisted pairs	Flat cable, 26 conductor with ground plane and drain wire
Impedance	100Ω + 10Ω	130Ω + 15Ω
Wire Size	28 AWG, 7 strands	28 AWG, 7 strands
Propagation Delay Time	5.6 ns/m (nominal)	5.5 ns/m (nominal)
Maximum Cable Length	99 ft (30 m)	49.5 ft (15 m)
Voltage Rating	300 V rms	300 V rms
Part Number	Spectra strip SS-455-248-60	3 M 3476-26

Table B-5 Power Cable Descriptions

CABLE	DESIGNATION	NEC PART NUMBER	WIRE SIZE
DC Cable	DKU000-HDC1	134-232902-GRP-0	AWG 18
AC Cable	DKU000-HAC1	134-232903-GRP-0	AWG 18

Table B-6 Option Cable Description

CABLE	DESIGNATION	NEC PART NUMBER	WIRE SIZE
3-DC Option Cable	DKU000-H3PM	806-942333-100-0	
Operator Panel Cable			AWG 22-32

Table B-7 Interface Connector Descriptions

CABLE	I/O CABLE ASSEMBLY	LOGIC PRINTED WIRING ASSEMBLY
A	60-pin connector 3M #3334-6000 or equivalent	60-pin vertical adapter TPD #R60L NEC #802-710100-560 or equivalent
B	26-pin connector 3M #3399-3000 or equivalent	26-pin vertical adapter TPD #R26L NEC #802-710100-526 or equivalent

Table B-8 DC Power Cable Connector Description

CONNECTOR	NEC PART NUMBER	VENDOR/PART NUMBER
Disk Side Housing	806-927233-103-0	AMP Ltd./171892-1
Disk Side Contact	806-927191-0	AMP Ltd./170289-1
Power Supply Side Housing	802-710113-009-0	AMP Ltd./1-480706-0
Power Supply Side Contact	802-710114-002-0	AMP Ltd./350705-1

Table B-9 AC Power Cable Connector Description

CONNECTOR	NEC PART NUMBER	VENDOR/PART NUMBER
Distributor Side Housing	802-710113-503-0	AMP Ltd./350766-1
Distributor Side Contact	802-710114-002-0	AMP Ltd./350705-1
Power Side Housing	802-710113-503-0	AMP Ltd./350766-1
Power Side Contact	802-710114-102-0	AMP Ltd./350550-1

Table B-10 3-Input DC Rebulator Option Cable Connector Descriptions

CONNECTOR	NEC PART NUMBER	VENDOR/PART NUMBER
Disk Side Housing	806-927233-103-0	AMP Ltd./171892-1
Disk Side Contact	806-927191-0	AMP Ltd./170289-1
Power Supply Side Housing		AMP Ltd./1-480270-0
Power Supply Side Contact		AMP Ltd./60617-4

Table B-11 Operator Panel Cable Connector Descriptions

CONNECTOR	VENDOR	PART NUMBER
Disk Side Housing	Berg	65043-032
Disk Side Contact	Berg	47744 (for AWG 28, 30, 32)
	Berg	47745 (for AWG 22, 24, 26)

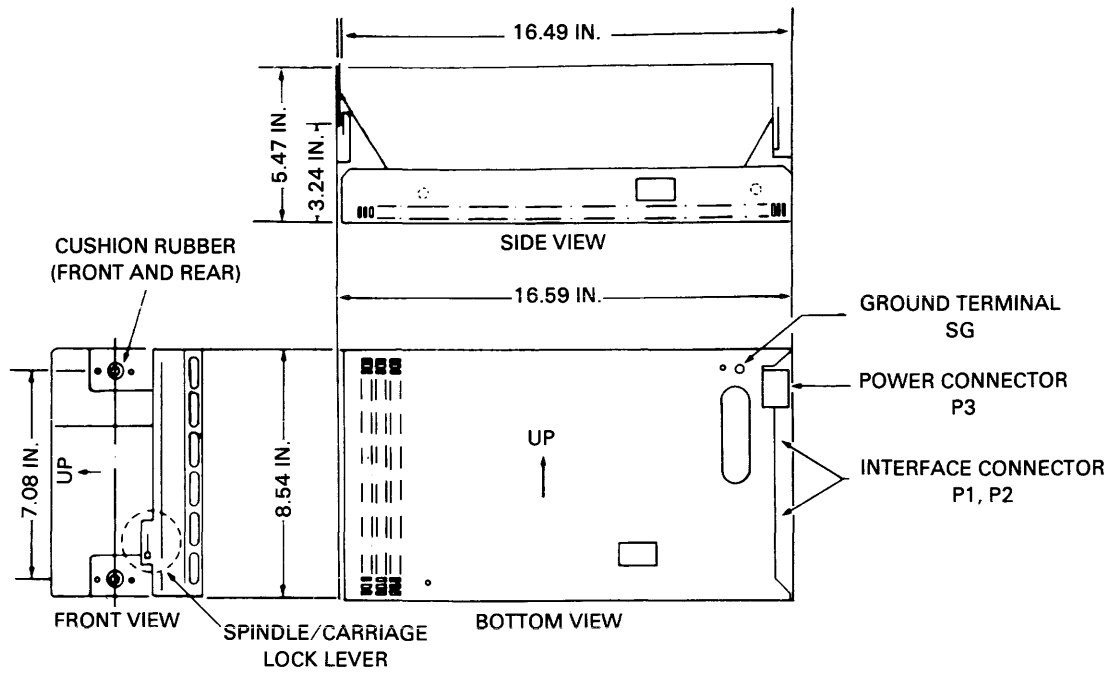


Figure B-1 D2246 Basic Assembly Dimensions

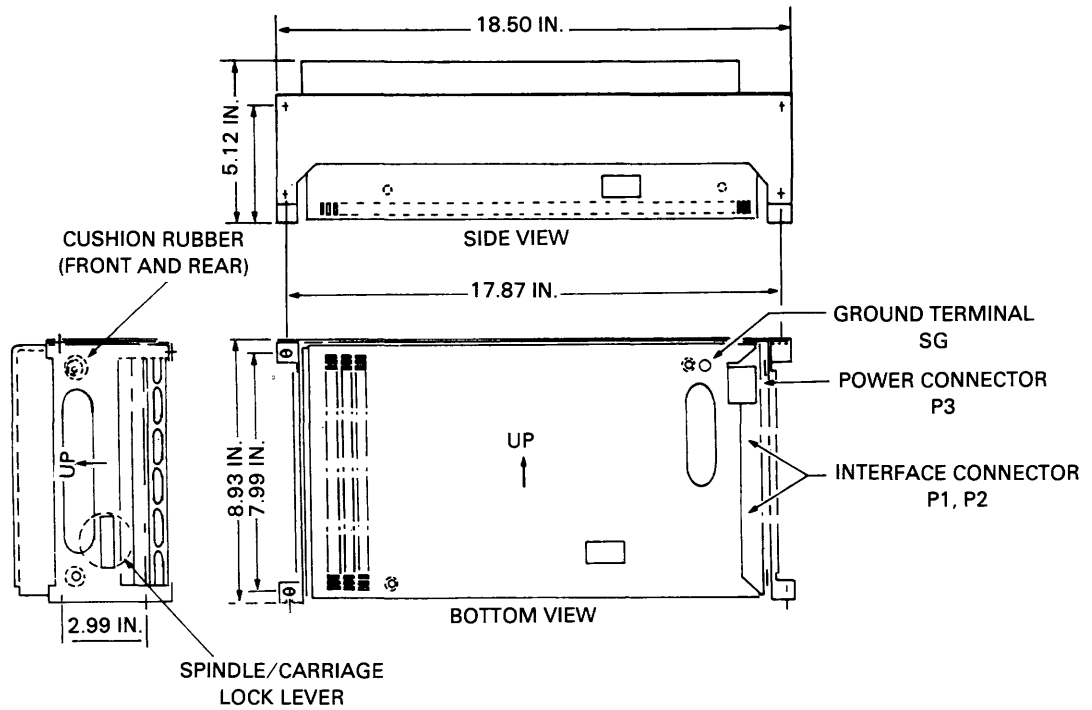


Figure B-2 D2246 Standard Assembly Dimensions

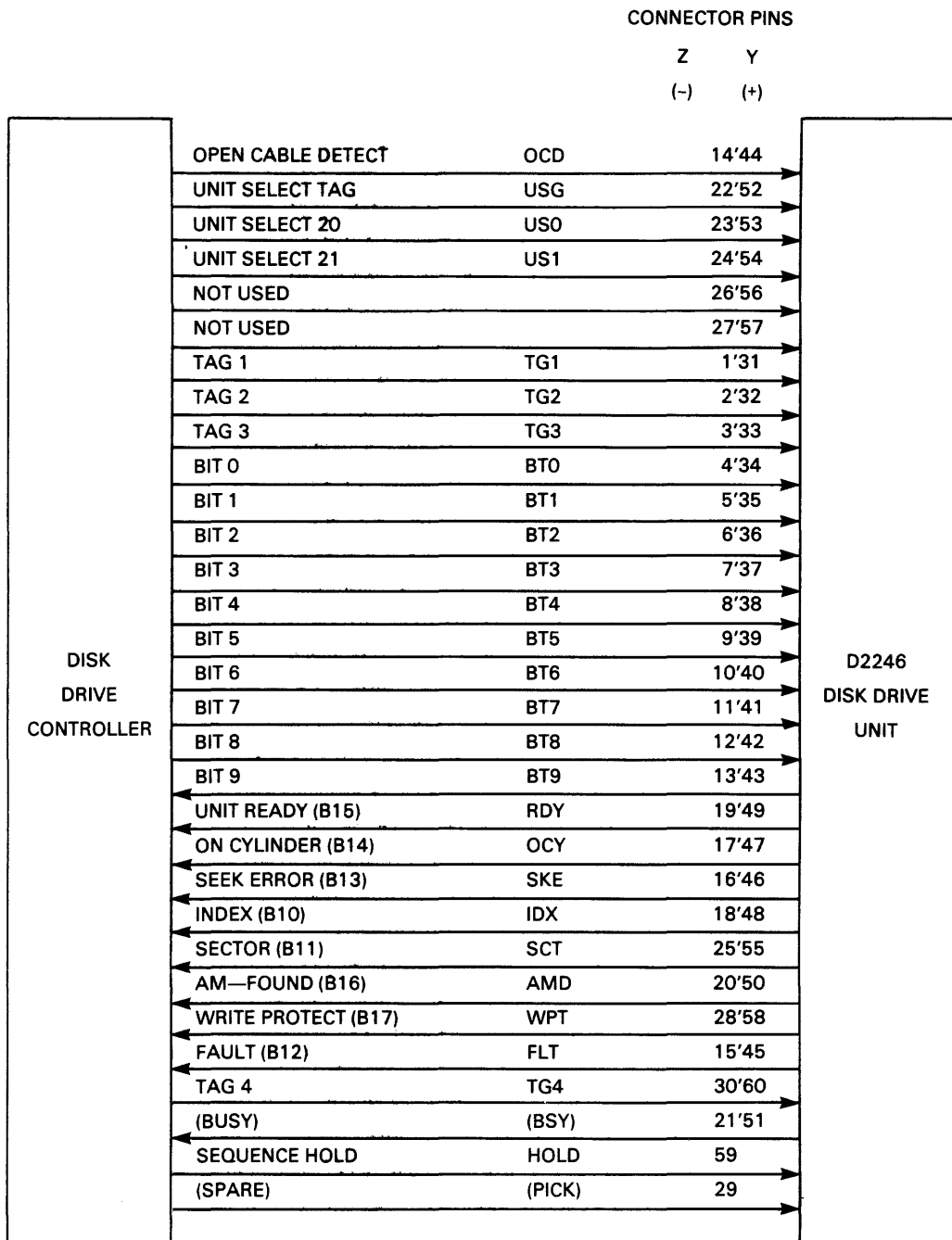


Figure B-3 Cable A Signals

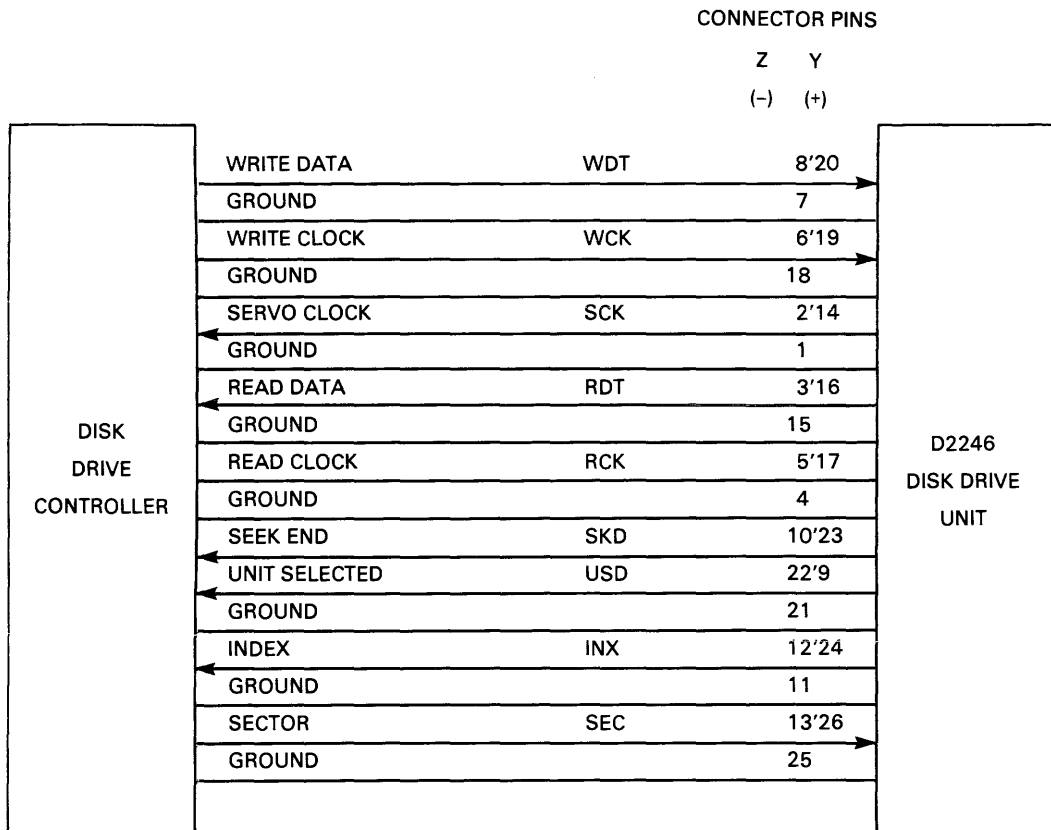
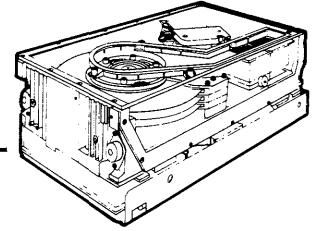


Figure B-4 Cable B Signals

Appendix C

DKU000-HLOG Diagnostic Panel



The DKU000-HLOG Diagnostic Panel tests disk drives. When the disk drive is offline, the panel simulates an interface controller and functions as a drive exerciser. When the disk drive is online, the panel functions as a status monitor. All errors detected by the panel are encoded and logged in its internal memory and retained for more than 100 hours after power has been turned off.

C.1 CONTROL PANEL

The diagnostic panel is shown in Figure C-1. The panel contains a 25-key keypad, five LED status indicators, a six-digit liquid crystal display (LCD) window, and two summary charts. A mounting spring on each end attaches the panel to the disk drive as shown in Figure C-2.

A 0.4 Farad capacitor provides nonvolatile memory for the logging function. The diagnostic panel is connected to the disk drive by an interface cable as shown in Figure C-3.

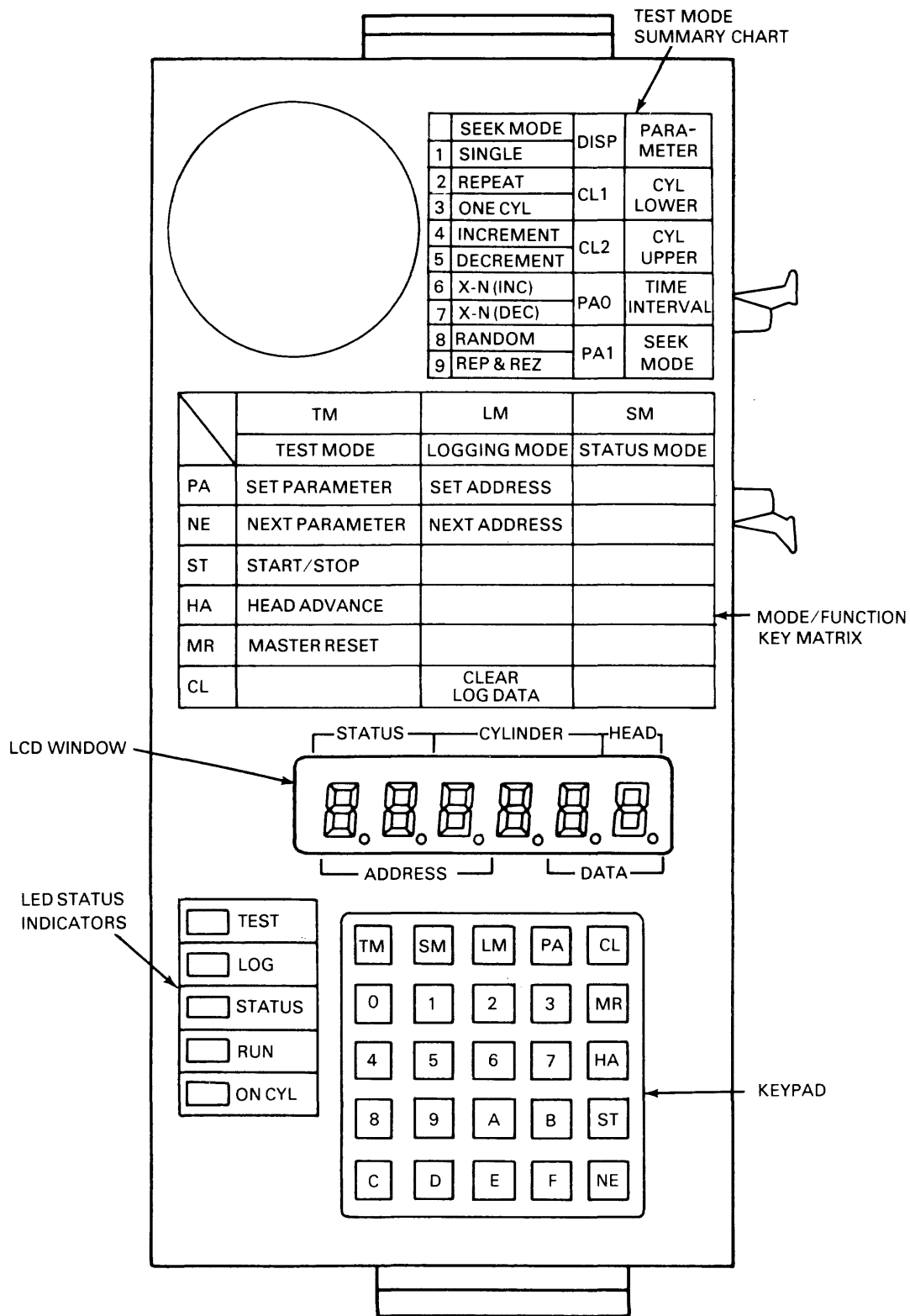


Figure C-1 Diagnostic Panel

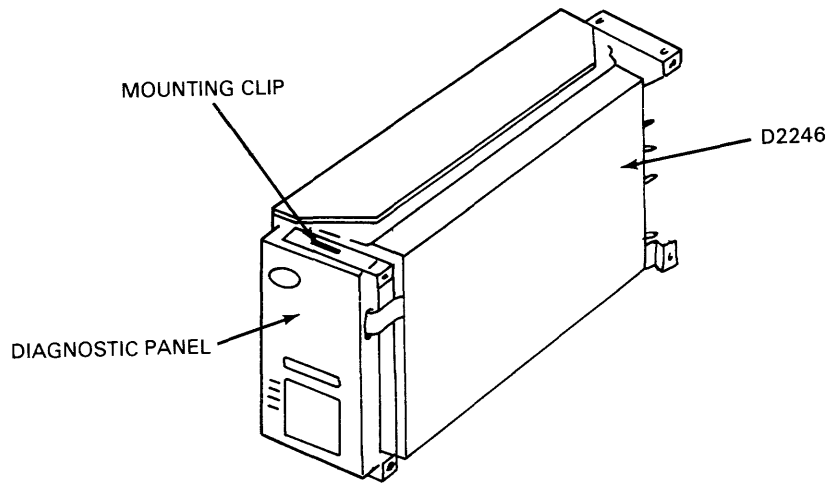


Figure C-2 Attaching the Diagnostic Panel to the Drive

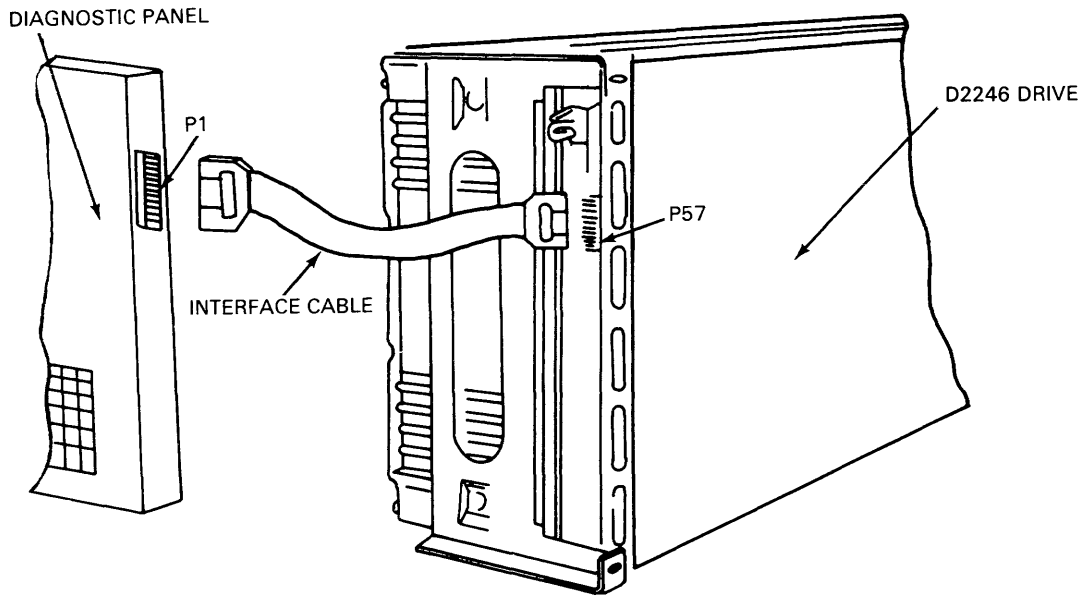


Figure C-3 Diagnostic Panel Cable and Connector

C.1.1 Keypad

The keypad contains 25 keys. Sixteen of these keys, representing hexadecimal digits 0 to F, are used to enter exercise parameters when Test mode is selected.

Three keys select the operational mode of the diagnostic panel. The functions of these keys are listed in Table C-1.

Table C-1 Mode Selection Keys

KEY	MODE SELECTED	DESCRIPTION
TM	Test Mode	Test mode places the disk drive offline. The diagnostic panel simulates an interface controller, and exercises the drive.
SM	Status Mode	Status mode monitors the online operation of the drive. The LCD window displays the current drive status, as well as the current head and cylinder address.
LM	Log Read Mode	Log Read mode provides a record of status or error information. Errors are logged sequentially and by type.

The six remaining keys enable specific diagnostic panel functions as listed in Table C-2.

Table C-2 Diagnostic Panel Functions

KEY	FUNCTION	MODE	DESCRIPTION
PA	Parameter Input	TM	Enables entry of seek test parameters from the panel keypad. See Section C.3.1.1.
		LM	Enables entry of sequential record address from the keypad. See Section C.4.2.
CL	Clear	LM	Clears the logging area. See Section C.4.3.
MR	Master Reset	TM	Performs a return-to-zero (RTZ) operation. See Section C.3.1.
HA	Head Advance	TM	Increases the head address by one each time the key is pressed. See Section C.3.1.
ST	Start/Stop	TM	Starts or stops the selected operation.
NE	Next Parameter	TM	Enters the parameter value selected by the PA key and brings up the next parameter. See Section C.3.1.1.
		LM	Initiates and advances search routine through error logs. See Sections C.4.1 and C.4.2.

C.1.2 LED Status Indicators

Three LEDs, labelled TEST, LOG, and STATUS, indicate the operational mode of the diagnostic panel. Two additional LEDs, labelled RUN and ON CYL, indicate the operational mode of the disk drive.

C.1.3 LCD Display Window

The six-digit LCD window displays status or error information. Depending upon the selected operational mode, the following information is displayed:

- cylinder address
- head address
- drive status
- error count.

C.1.4 Diagnostic Panel Summary Charts

Two charts, a Mode/Function Key Matrix and a Test Mode Summary, are included on the diagnostic panel. The Mode/Function Key Matrix lists the function performed by each of the six function keys in the three operational modes. The Test Mode Summary lists the nine seek operations and four parameters used in Test mode.

C.2 STATUS MODE

In Status mode, the diagnostic panel displays the current status of the disk drive. When an error occurs, data is logged in the diagnostic panel's internal memory and simultaneously displayed in the six-digit LCD window. Subsequent errors are logged in memory. The panel display, however, remains unchanged. Status information is formatted as shown in Figure C-4.

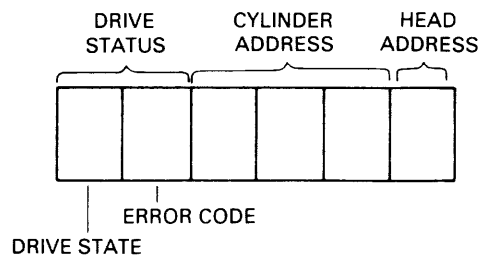


Figure C-4 Status Mode Display Format

C.2.1 Starting Status Mode

Pressing the SM key starts Status mode. When Status mode is selected, the STATUS and ON CYL LEDs light. The data window displays the drive status, consisting of the operational state of the disk drive and an associated error code, the current cylinder address, and the current head address.

C.2.1.1 DRIVE STATUS

The two-digit drive status display lists the operational state of the disk drive along with an encoded error report. Table C-3 lists the drive state displays and the corresponding state of operation.

Table C-3 Disk Drive Operational States

LCD DISPLAY	OPERATIONAL STATE
1	Power On/Initialization Sequence
2	Stop State
3	Start Delay
4	Motor Start (90% RPM attained)
5	Motor Speed Increase (97% RPM attained)
6	Full Motor Speed
7	Phase-Locked Oscillator
8	Recalibrate Out
9	Recalibrate In
A	Ready (On Cylinder)
B	Heads Out
C	Interface Check
D	Heads In
E	Not Used by D2246
F	Fault (Ready)

Table C-4 lists all drive status reports used with the D2246, along with suggested troubleshooting procedures.

Table C-4 Drive Status Reports

DISPLAY		ERROR CONDITION	SUGGESTED PROCEDURES
DRIVE STATE	ERROR CODE		
1	1	Voltage Fault	Check source voltage.
1	2	Read-only-memory (ROM) fault	Replace G9QST PCB.
1	4	Fault latch	Replace G9QST PCB.
2	1	Voltage fault	Check source voltage.
3	1	Voltage fault	Check source voltage.
4	1	Voltage fault	Check source voltage.
4	3	Insufficient motor speed	Check motor rotation. Replace G9QSQ PCB.

Table C-4 Drive Status Reports (cont'd)

DISPLAY DRIVE STATE	ERROR CODE	ERROR CONDITION	SUGGESTED PROCEDURES
4	4	No motor rotation	Check lock control lever. Replace G9QSQ PCB.
5	1	Voltage fault	Check source voltage.
5	2	Insufficient motor speed	Check source voltage. Check cable connector. Replace G9QSQ PCB. Replace G9QST PCB. Replace the unit.
5	3	Excessive motor speed	See Fault 52.
6	1	Voltage fault	Check source voltage.
6	2	Motor speed loss	Restart motor. If fault 43 or 44 occurs, replace G9QSQ PCB. Replace G9QST PCB. Replace the unit.
6	3	Excessive motor speed	See Fault 52.
7	1	Voltage fault	Check source voltage.
7	2	Motor speed loss	See Fault 62.
7	4	Loss of index	Check the tripulse output. If tripulse is available, replace G9QST PCB. Replace unit. If tripulse is not available, replace G9QSQ PCB. Replace unit.
7	5	Inner guard band (IGB) not found	Replace G9QST PCB. Replace unit.
8	1	Voltage fault	Check source voltage.
8	4	Loss of index	See Fault 74.
8	5	Outer guard band (OGB) not found	Check lock control lever. Verify current flow in the voice coil. Replace G9QST PCB. Replace unit.
8	6	No N linearity found	Replace G9QST PCB. Replace unit.
8	7	No half track found	Replace G9QST PCB.
8	8	No Q linearity found	Replace G9QST PCB.

Table C-4 Drive Status Reports (cont'd)

DISPLAY		ERROR CONDITION	SUGGESTED PROCEDURES
DRIVE STATE	ERROR CODE		
8	9	No zero difference found	Replace G9QST PCB.
8	A	Target velocity not obtained	Readjust the servo circuit. Replace G9QST PCB.
8	B	Servo circuit fault	See Fault 8A.
8	C	Over-shoot check	See Fault 8A.
8	D	Over-shoot check (time out)	See Fault 8A.
9	1	Voltage fault	Check source voltage.
9	4	Loss of index	See Fault 74.
9	5	Only OGB detected	Replace G9QST PCB. Replace unit.
9	9	No N linearity found	See Fault 86.
9	C	Over-shoot check	See Fault 8A.
9	D	Over-shoot check (time out)	See Fault 8A.
A	1	Voltage fault	Check the source voltage.
A	2	Motor speed loss	See Fault 72.
A	3	Excessive motor speed	See Fault 52.
A	4	Loss of index	Check the tripulse or cylinder concerned. If index signal found, replace G9QST PCB. If index signal missing, replace unit.
A	C	R/W positioner off track	See Fault 8A.
B	1	Voltage fault	Check the source voltage.
B	4	Loss of index	See Fault A4.
B	9	No zero difference found	Replace G9QST PCB.
B	C	Over-shoot check	See Fault 8A.
B	D	Over-shoot check (time out)	See Fault 8A.
B	E	OGB detected during seek	See Fault 8A.

Table C-4 Drive Status Reports (cont'd)

DISPLAY		ERROR CONDITION	SUGGESTED PROCEDURES
DRIVE STATE	ERROR CODE		
B	F	IGB detected during seek	See Fault 8A.
C	1	More than 692 cylinders detected	
C	3	Tag 1 received when not ready	
D	1	Voltage fault	Check the source voltage.
D	4	Loss of index	See Fault A4.
D	9	No zero difference found	Replace G9QST PCB.
D	C	Over-shoot check	See Fault 8A.
D	D	Over-shoot check (time out)	See Fault 8A.
D	E	OGB detected during seek	See Fault 8A.
D	F	IGB detected during seek	See Fault 8A.
F	1	Write protect violation	Check for defective interface.
F	2	Write gate while not ready	Check for defective interface. Replace G9QST PCB. Replace unit.
F	3	Write clock fault	Replace G9QST PCB. Replace unit.
F	4	Write head off track	Replace G9QST PCB.
F	5	Abnormal write operation	Replace G9QSN PCB. Replace G9QST PCB. Replace unit.
F	6	Abnormal read operation	See Fault F5.

C.2.1.2 CYLINDER AND HEAD ADDRESSES

When the diagnostic panel is in Status mode, the current cylinder address is displayed in three digit hexadecimal notation. The current head address is displayed as a single digit.

C.2.2 Using Status Mode

Status mode displays the current status of the disk drive. If an error occurs, the corresponding drive status report is displayed. Simultaneously, the displayed data is logged in the diagnostic panel's internal memory. The presence of a non-zero digit in the right position of the drive status display, or the presence of a "00" code in the drive status display indicates an error condition (see Figure C-5).

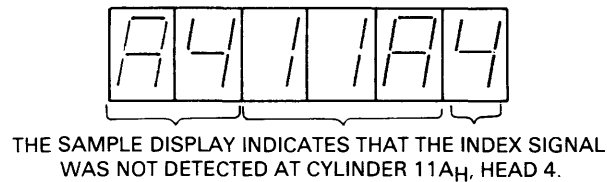


Figure C-5 Status Mode Error Display Format

The panel's internal memory records subsequent errors as they occur. The LCD display, however, remains unchanged until the SM key is pressed. Pressing the SM key displays the latest drive status report.

C.2.3 Ending Status Mode

Pressing the TM or LM key ends Status mode.

C.3 TEST MODE

In Test mode, the diagnostic panel places the disk drive offline; that is, the interface between the drive and the drive controller is disabled. The diagnostic panel simulates the drive controller, and enables nine different seek operations to test the drive.

C.3.1 Starting Test Mode

Select Test mode by pressing the TM key and then pressing the 9 key. Pressing the 9 key acts as a safety device that prevents the disk drive moving from an online to an offline condition when the TM key is accidentally pressed.

After Test mode is selected, press the MR key to perform a return-to-zero (RTZ) operation. This operation moves the read/write heads to Cylinder 000.

Press the HA key to select the desired read/write head. The head address appears in the rightmost character position of the LCD display. The address is incremented by one each time the HA key is pressed.

C.3.1.1 INPUT PARAMETERS

After the read/write head is selected, three parameters (low cylinder address, high cylinder address, and interval timing) are set. Press the PA key to begin setting parameters for seek operations. The resulting LCD display is shown in Figure C-6.

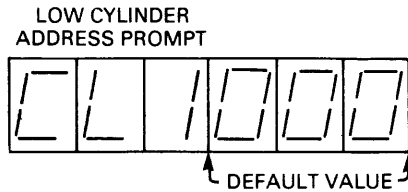


Figure C-6 Low Cylinder Parameter Display

The low cylinder address (CL1) default value (Cylinder 000) appears in the address field as shown. To set a new low cylinder address, enter three hexadecimal digits from the numeric keypad. Press the NE key to accept the default value or to accept the new value as entered from the keypad.

When the NE key is pressed, the LCD display appears as shown in Figure C-7.

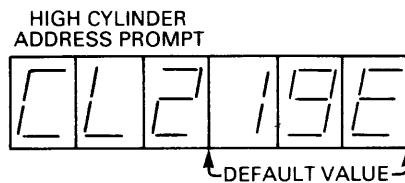


Figure C-7 High Cylinder Parameter Display

The high cylinder address (CL2) default value (Cylinder 19E) occupies the address field. To set a new high cylinder address, enter three hexadecimal digits from the keypad. The high cylinder address must be greater than the low cylinder address. Press the NE key to accept the default value or to accept the new value as entered from the keypad.

After pressing the NE key, the LCD display appears as shown in Figure C-8.

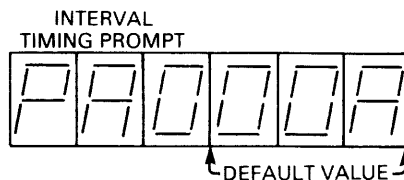


Figure C-8 Interval Timing Parameter Display

The interval timing default value, expressed in milliseconds, is recorded in the address field. To set a new interval timing, enter three hexadecimal digits from the keypad. Press the NE key to accept the default value or to accept the new value as entered from the keypad.

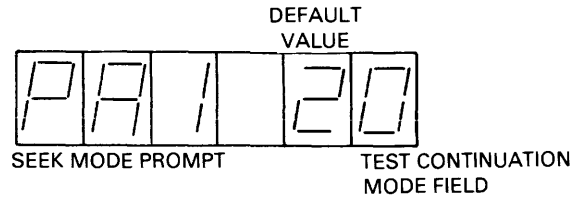


Figure C-9 Seek Mode Display

C.3.1.2 SEEK MODES

After the interval timing value is entered and the NE key pressed, the following display appears.

The seek mode digit selects one of the nine seek operations listed on the Test Mode Summary chart. The test continuation digit determines the conditions under which a seek test is halted. When a zero is displayed, seek operations are halted if an error occurs. When any other digit is displayed, seek operations continue to completion.

The seek mode default value is recorded in the address field. To set a new seek mode and test continuation condition, enter two digits from the keypad. Press the NE key to accept the default value or to accept the new value as entered from the keyboard.

Table C-5 summarizes the nine seek modes that can be selected.

Table C-5 Seek Modes

MODE NUMBER	SEEK MODE	DESCRIPTION
1	Single Seek	Seeks to destination cylinder (CL2) and stops. To repeat, press the MR key and wait until the read/write heads return to cylinder 000. Then press the ST key.
2	Repeat Seek	Seeks directly from the low cylinder address to the high cylinder address, and then from the high cylinder to the low cylinder. The cycle is repeated.
3	One Cylinder	Seeks one cylinder at a time from the low cylinder (CL1) to the high cylinder (CL2), and then from the high cylinder to the low cylinder. The cycle repeats. For example, with CL1 equal to 000 and CL2 equal to 100, seeks to 001, to 002, to ..., to 100. Then seeks to 099, to 098, to ..., to 000.

Table C-5 Seek Modes (cont'd)

MODE NUMBER	SEEK MODE	DESCRIPTION
4	Increment Seek	Seeks one cylinder at a time from the low cylinder (CL1) to the high cylinder (CL2), and then returns directly to the low cylinder to repeat the cycle. For example, with CL1 equal to 000 and CL2 equal to 100, seeks to 001, to 002, to ..., to 100. Returns to CL1 and repeats.
5	Decrement Seek	Seeks one cylinder at a time from the high cylinder (CL2) to the low cylinder (CL1), and then returns directly to the high cylinder to repeat the cycle. For example, with CL1 equal to 000 and CL2 equal to 100, seeks to 099, to 098, to ..., to 000. Returns to CL2 and repeats.
6	X + N (INC)	Seeks incrementally from the low cylinder (CL1) to the high cylinder (CL2), and then returns directly to CL1 to repeat the cycle. For example, with CL1 equal to 000 and CL2 equal to 100, seeks to 001 and returns to CL1; seeks to 002 and returns to CL1; seeks to ... and returns to CL1; seeks to 100. Returns to CL1 and repeats cycle.
7	X - N (DEC)	Seeks decrementally from the high cylinder (CL2) to the low cylinder (CL1), and then returns directly to CL2 to repeat the cycle. For example, with CL1 equal to 000 and CL2 equal to 100, seeks to 099 and returns to CL2; seeks to 098 and returns to CL2; seeks to ... and returns to CL2; seeks to 000. Returns to CL2 and repeats cycle.
8	Random	Seeks randomly within the parameters set by the low and high cylinder addresses.
9	Repeat and RTZ	Seeks to high cylinder (CL2), returns to cylinder 000, and repeats cycle.

C.3.2 Using Test Mode

When all parameters are set, press the ST key to enter Test mode. The RUN LED lights and the selected seek operation is performed. If an error occurs while a seek test is running, the diagnostic panel displays the status of the drive just as it does in Status mode (see Section C.2).

C.3.3 Ending Test Mode

Seek operations are halted before completion by a seek error (depending on the status of the test continuation condition), or by pressing the ST key. When seek operations stop, the RUN LED goes out. The panel remains in the Test mode. To end Test mode press the SM or LM key.

C.4 LOG READ MODE

The diagnostic panel stores specific information on each error that occurs during either Status or Test mode. Information is logged into a dedicated 640-byte memory that consists of two sections. The first section (memory addresses 000_H through 0FF_H) records the number of times a specific error occurs. The second section (memory addresses 100_H through 27F_H) provides a sequential log of drive operations. The Log Read mode provides access to both of these memory areas.

C.4.1 Error/Count Log

Press the LM key to start the Log Read mode. The LOG and the ON CYL LEDs light. When using the Error/Count Log, the LCD display is formatted as shown in Figure C-10.

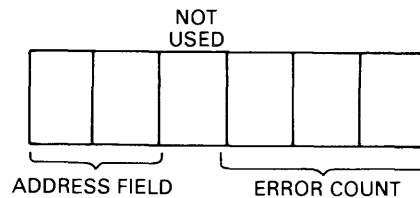


Figure C-10 Error/Count Log Display Format

When the LM key is pressed, the three-digit address field displays memory location 000 and the two-digit data field displays the total number of recorded errors.

Subsequent entries in the Error/Count Log are displayed by pressing the NE key. In most instances, pressing the NE key results in the following LCD display.

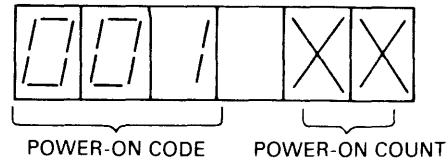


Figure C-11 Error/Count Log Power-On Count

The address field displays memory location 001 signifying power-on. The data field displays the power-on count.

Pressing the NE key again initiates a search through the Error/Count Log. When an error is detected, a drive status report (listed in Table C-3) is displayed in the address field. The number of times the error occurred is displayed in the data field. A sample LCD display is shown in Figure C-12.

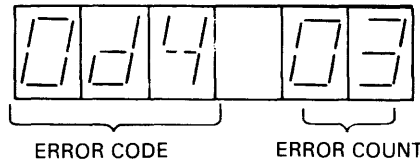


Figure C-12 Error/Count Log Error Display Format

The above display indicates that the d4 error (loss of Index signal) occurred three times.

Each time the NE key is pressed, the display advances to the next error. When all errors have been displayed, or if no errors have occurred, the display returns to the 000 memory address and the total count of logged errors.

C.4.2 Sequential Operations Log

Memory addresses 100 through 27F are assigned to the Sequential Operations Log. This log records errors and power-on and power-off operations. To access the Sequential Operations Log press the LM key to start Log Read mode, and then press the PA key.

Use the numeric keypad to initiate a search through the Sequential Operations Log. To examine the entire log, enter 100 from the keypad. Any other memory address from 101 through 27F can be entered. When the address has been entered, press the NE key to display the contents of the address location. The LCD display format is shown in Figure C-13.

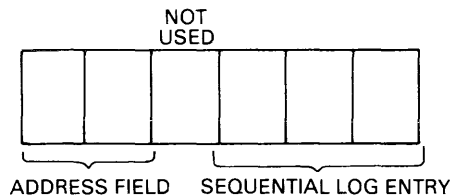


Figure C-13 Sequential Operations Log Display Format

Each time the NE key is subsequently pressed, the address field is incremented by one and the contents of that memory location are displayed in the data field. Figure C-14 shows sequential log entries.

C.4.3 Ending Log Read Mode

Press the CL key to clear both the error/count log and the sequential log. Press the LM or SM key to end Log Read mode.

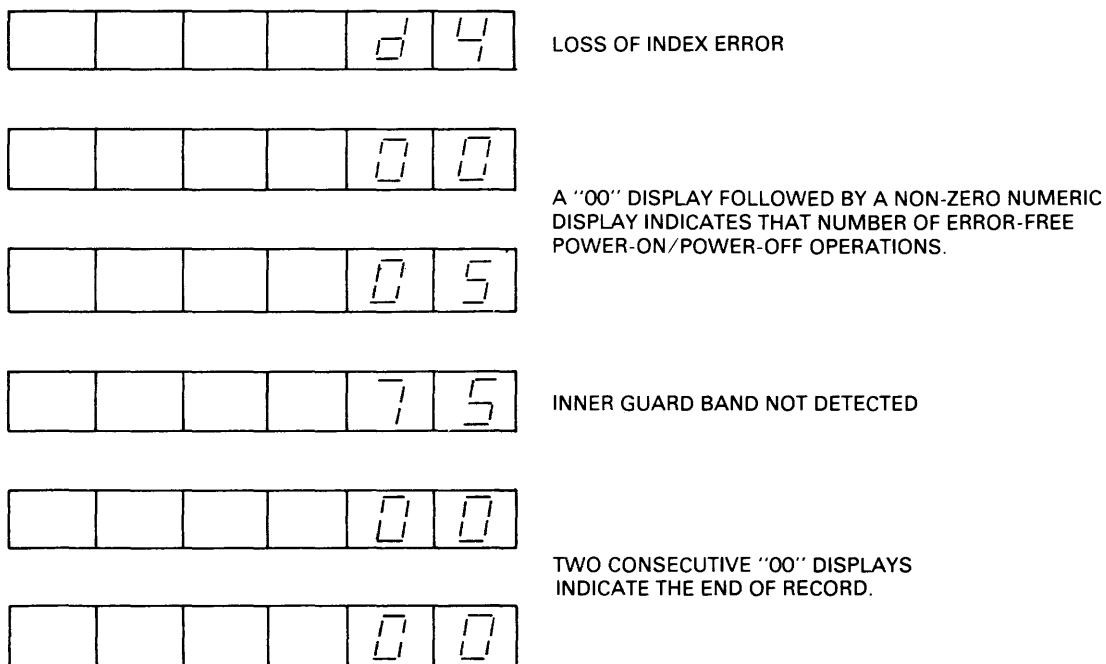
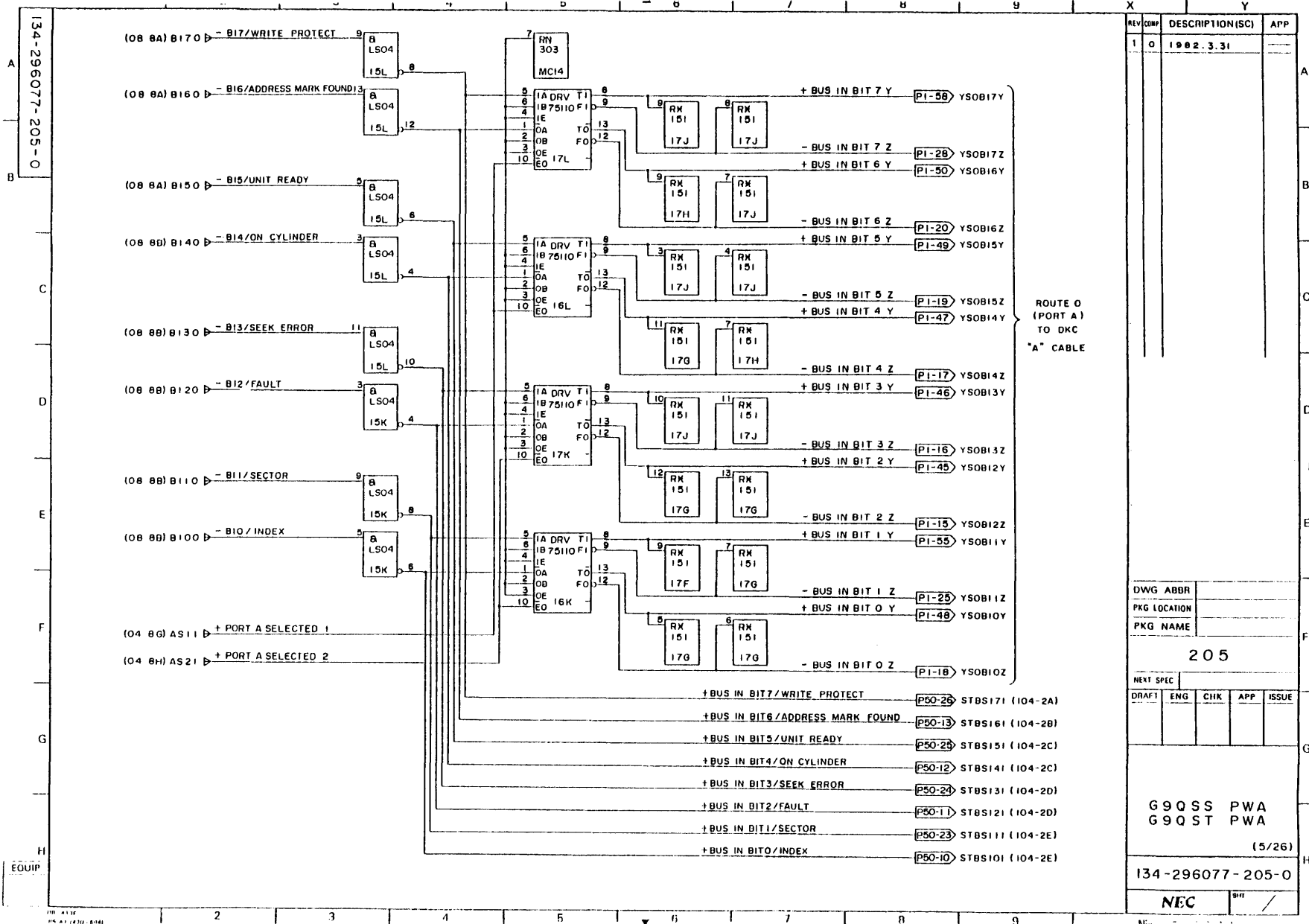


Figure C-14 Sequential Operations Log Entries

A-22



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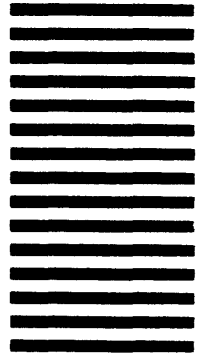


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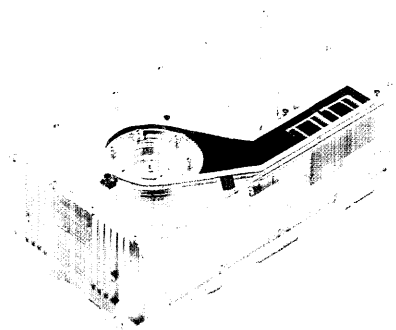
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