SWAC ENGINEERING MANUAL

NATIONAL BUREAU OF STANDARDS

May 1, 1951

Please Note:

This manual is not complete.

The following pages are missing:

A3.3-1
A6.1-1
A6.2-2
B.2.6-1
B2.7-1
C1.3-3
C1.1-1
C1.3-4
C1.3-6
C1.4-1

And probably more.

INA 51 - 4

U. S. DEPARTMENT OF COMMERCE

National Bureau of Standards

Los Angeles

ENGINEERING MANUAL FOR THE NATIONAL BUREAU OF STANDARDS WESTERN AUTOMATIC COMPUTER

prepared by

Machine Development Unit

Sponsored by the Office of Air Research

Project No. 1101-34-5103/49-1

Bloom

May 1, 1951

(This report is a working paper and has not been officially released by the National Bureau of Standards.)

PREFACE

This Engineering Manual is a working paper which has been prepared by the personnel of the Machine Development Unit of the Institute for Numerical Analysis in order to have available in convenient form pertinent information for the staff's own use. In this way the results of research of general interest carried on by any member of the group, as well as other useful information, is made available to all the staff. The present manual is incomplete; additional material will be issued as it becomes available.

Naturally not all the pages to be inserted in this manual will be issued at once. New chapters will be added as information becomes available. In some cases new pages may be issued to replace existing ones. Because of these facts a flexible numbering system has been adopted for use in this manual. In the upper right hand corner of each page will be found a number as, for example, A 3.1-1. The letter designates the Part of the manual in which the material is contained. In this instance the material is located in Part A, General Information. The first number to the left designates Chapter. In the example given the 3 means that this page is a part of Chapter 3, Test Equipment. The next number indicates what Section in Chapter 3 is concerned. The 1 in the example shows that this page is from Section 1, Crystal Checker. The number after the dash denotes the page number of the particular section. Thus, A 3.1-1 indicates that this page is to be found in Part A, Chapter 3, and is Page 1 of Section 1. This numbering system may seem complicated at first, but it does have the very distinct advantage of enabling new information to be added to the manual without reorganizing the existing material. An issuing date will be given in the upper left hand corner of each page. Thus, there will be no doubt as to which page has been issued last in the event changes are made and a new page is issued to replace one previously issued. (On pages issued after May 1, 1951 the number of this working paper, INA 51 - 4, will be typed directly above the page number.)

The Institute for Numerical Analysis is one of the four sections of the Applied Mathematics Laboratories of the National Bureau of Standards. It is located on the campus of the University of California at Los Angeles.

The Machine Development Unit of the Institute has designed and constructed an automatic digital computing machine known as the National Bureau of Standards Western Automatic Computer (SWAC). This machine was financed by the Office of Air Research of the United States Air Force.

The research program of the Institute is financed by the Office of Naval Research.

H. D. Huskey
Assistant Director
National Bureau of Standards
Los Angeles, California

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PART D. MAINTENANCE

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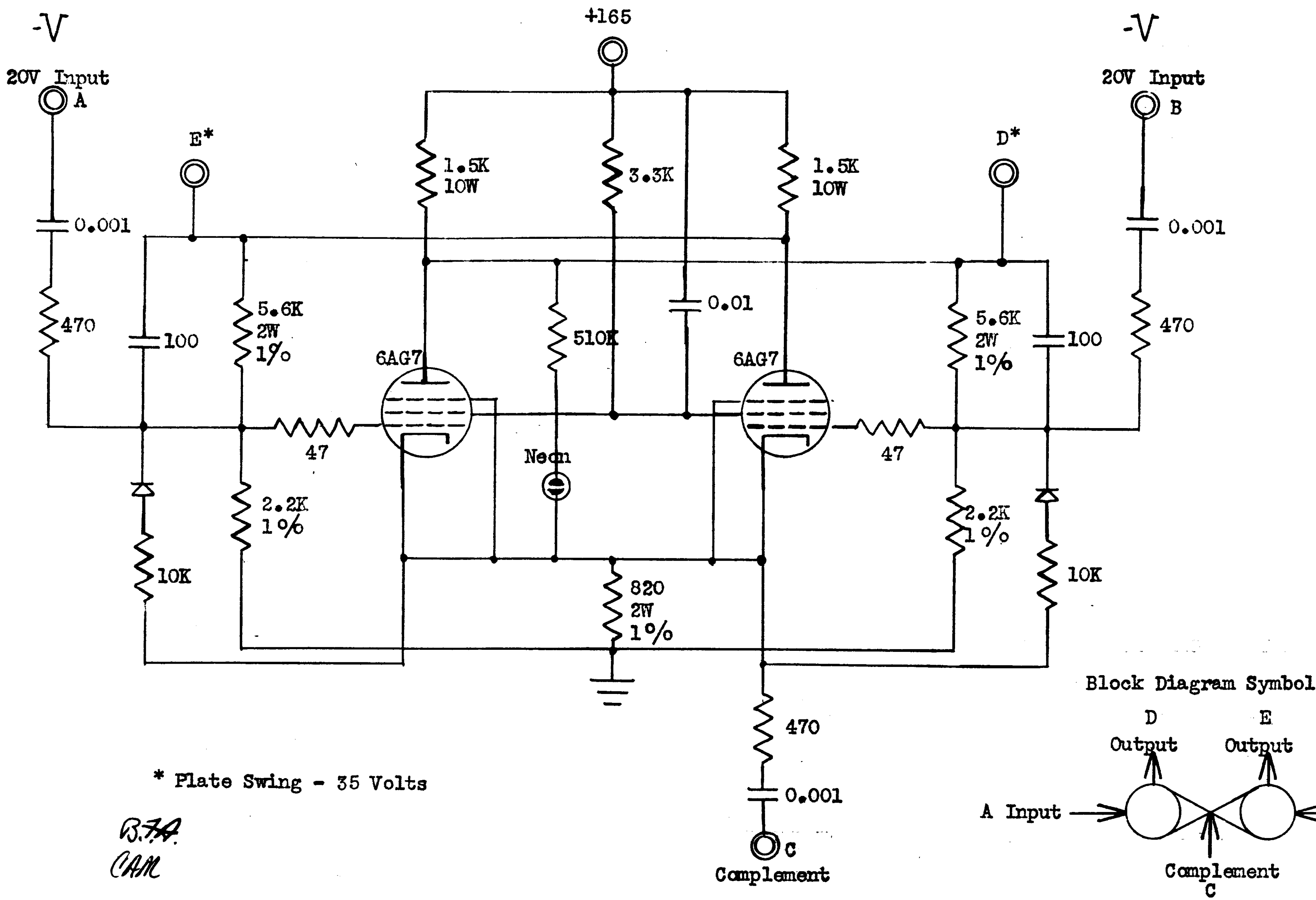
1.1 Flipflops and Binary Counters.

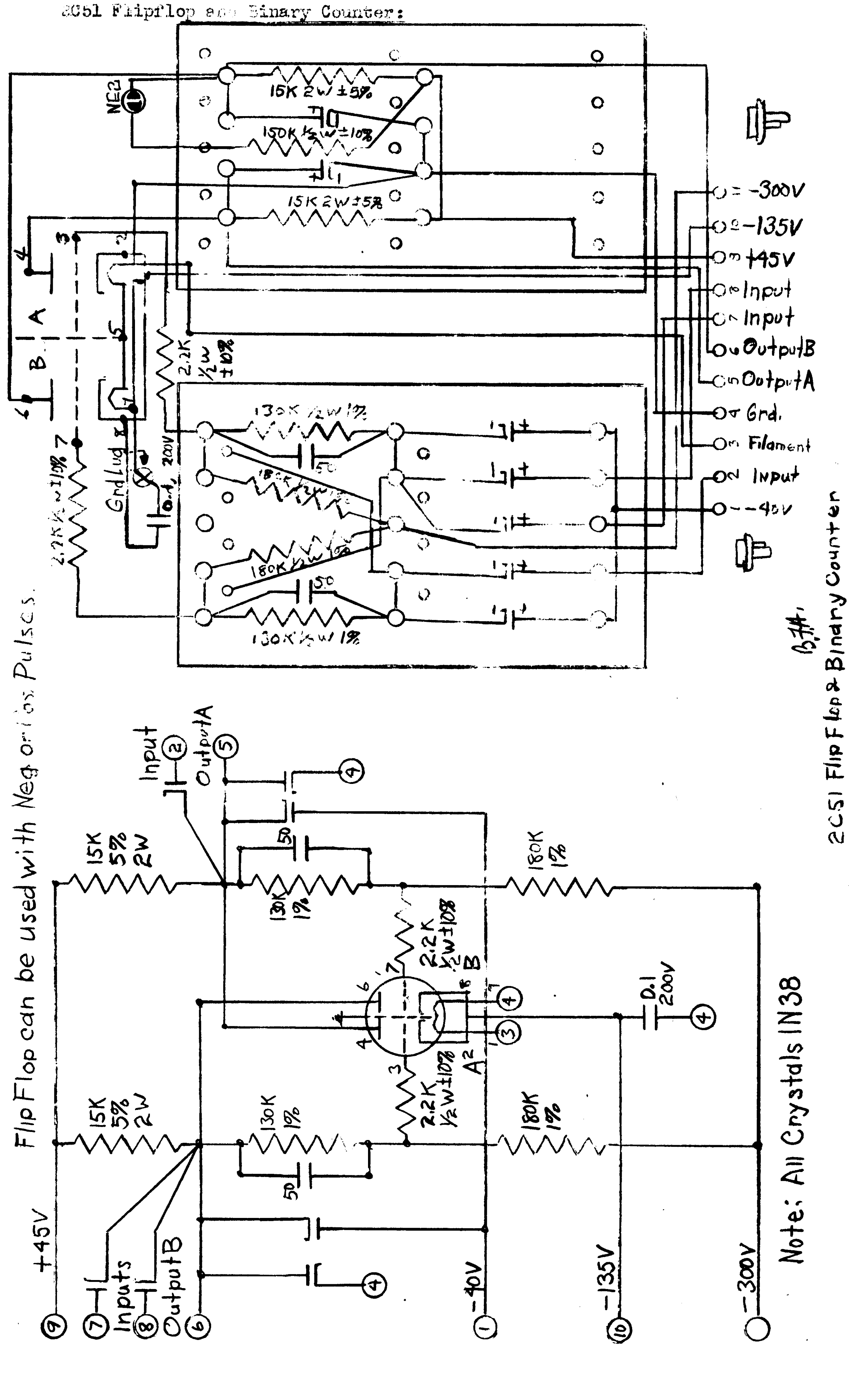
6AG7 Flipflop:



6AG7 FLIPFLOP

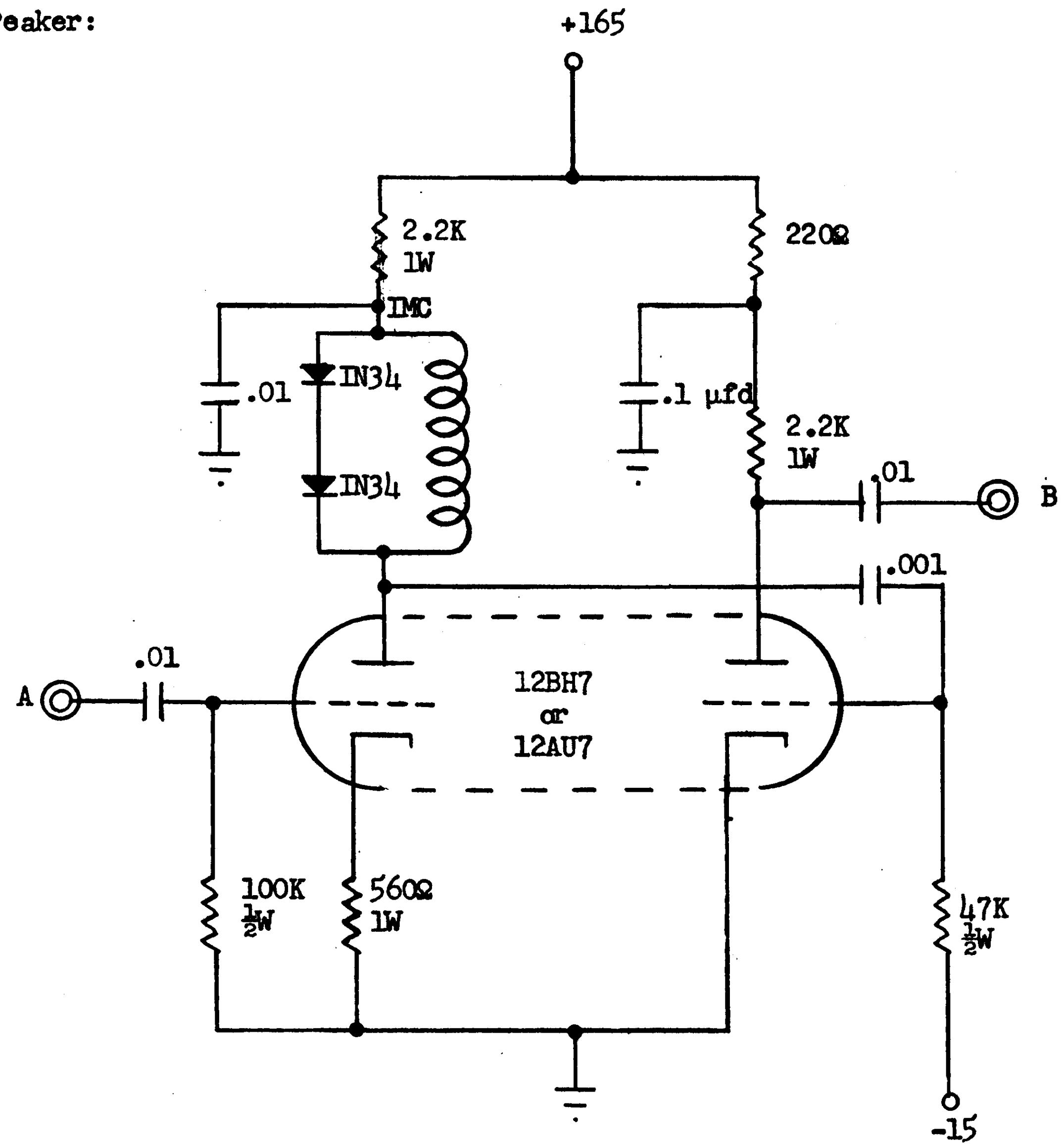
1.1 Flipflops and Binary Counters.

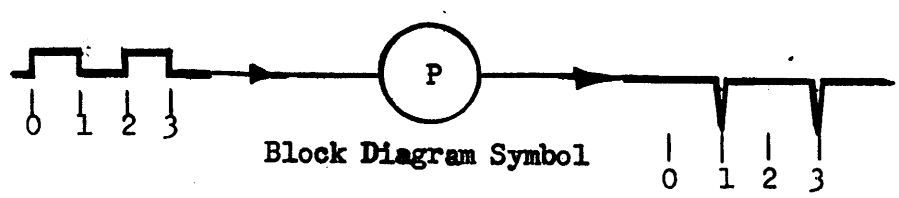
2C51 Flipflop and Binary Counter:



1.2 Pulse Shaping Circuits.

Peaker:



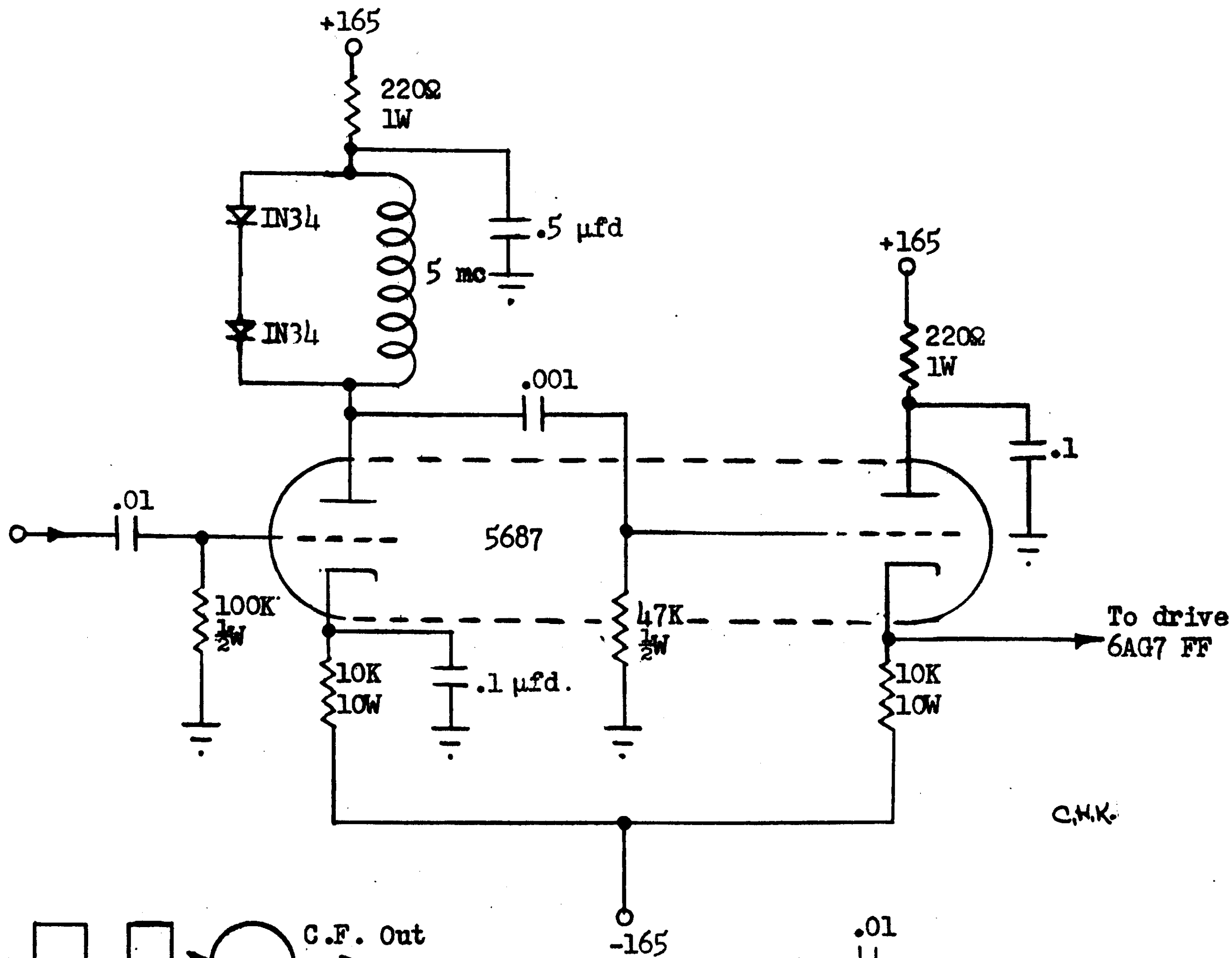


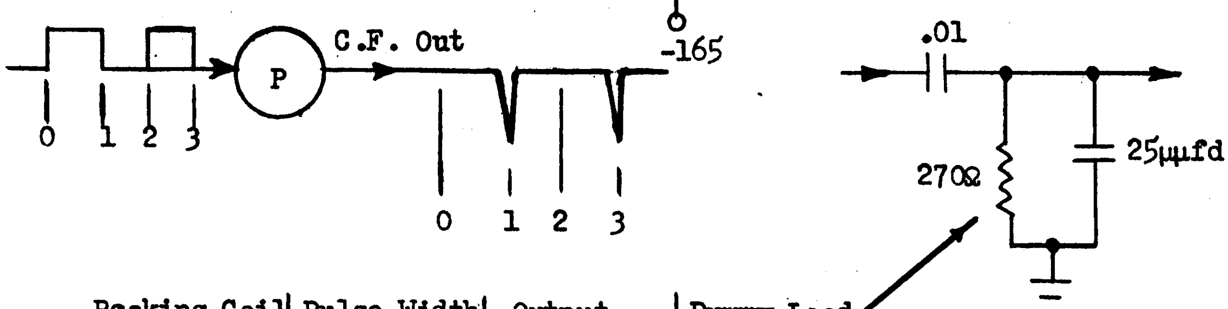
Block Diagram Symbol

Peaker Coil	Pulse Width at Base	Amplitude	Tube
1 Mc.	0.6 μsec.	125 Volts	12BH7
1 Mc.	0.5 μsec.	95 "	12AU7
5 Mc.	0.15 μsec.	70 "	12BH7
Condor 47μh	0.2 μsec.	60 "	12BH7

BFA

1.2 Pulse Shaping Circuits.





Peaking Coil	Pulse Width	Output	Dummy Load
1 Megacycle	.4 µsec.	150 Volts	70 Volts
5 "	.15 µsec.	50 "	35 "
Condor 47 µh.	.1 µsec.	45 "	30 "

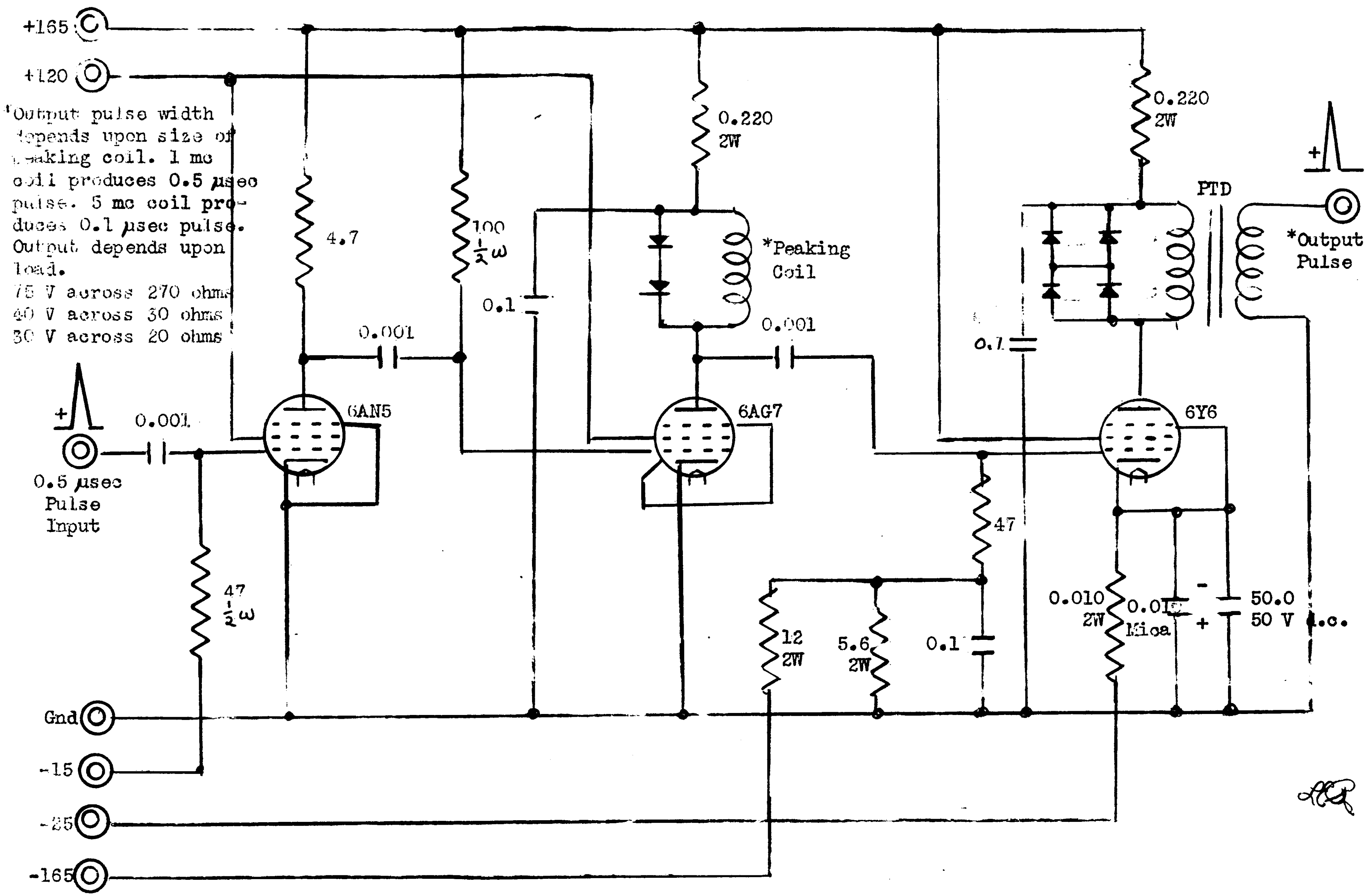
BFA

5687 PEAKER

Issued 9-23-49
Reissued 7-11-51

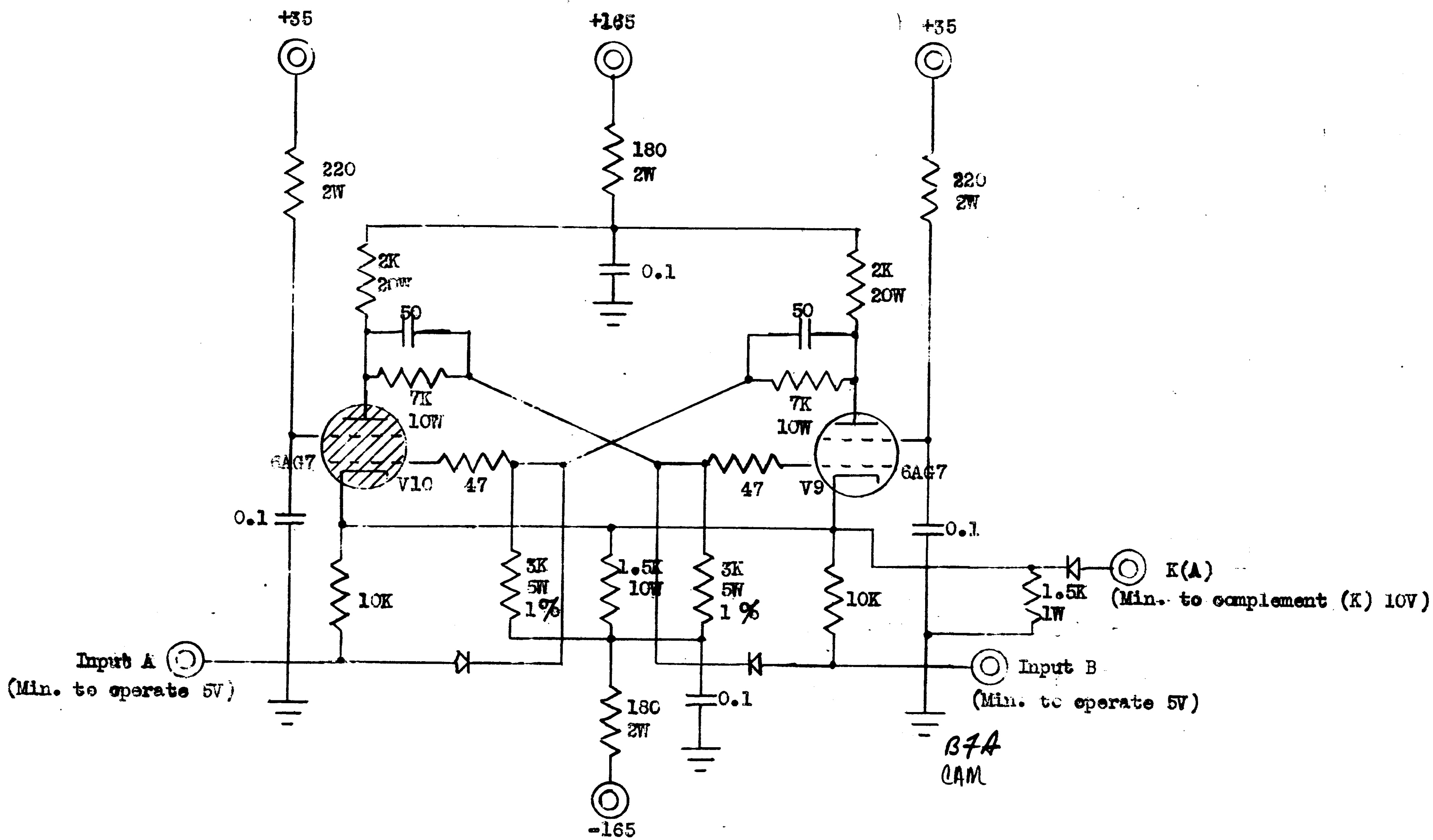
1.2 Pulse Shaping Circuits.

Peaker-Driver:



PEAKER-DRIVER

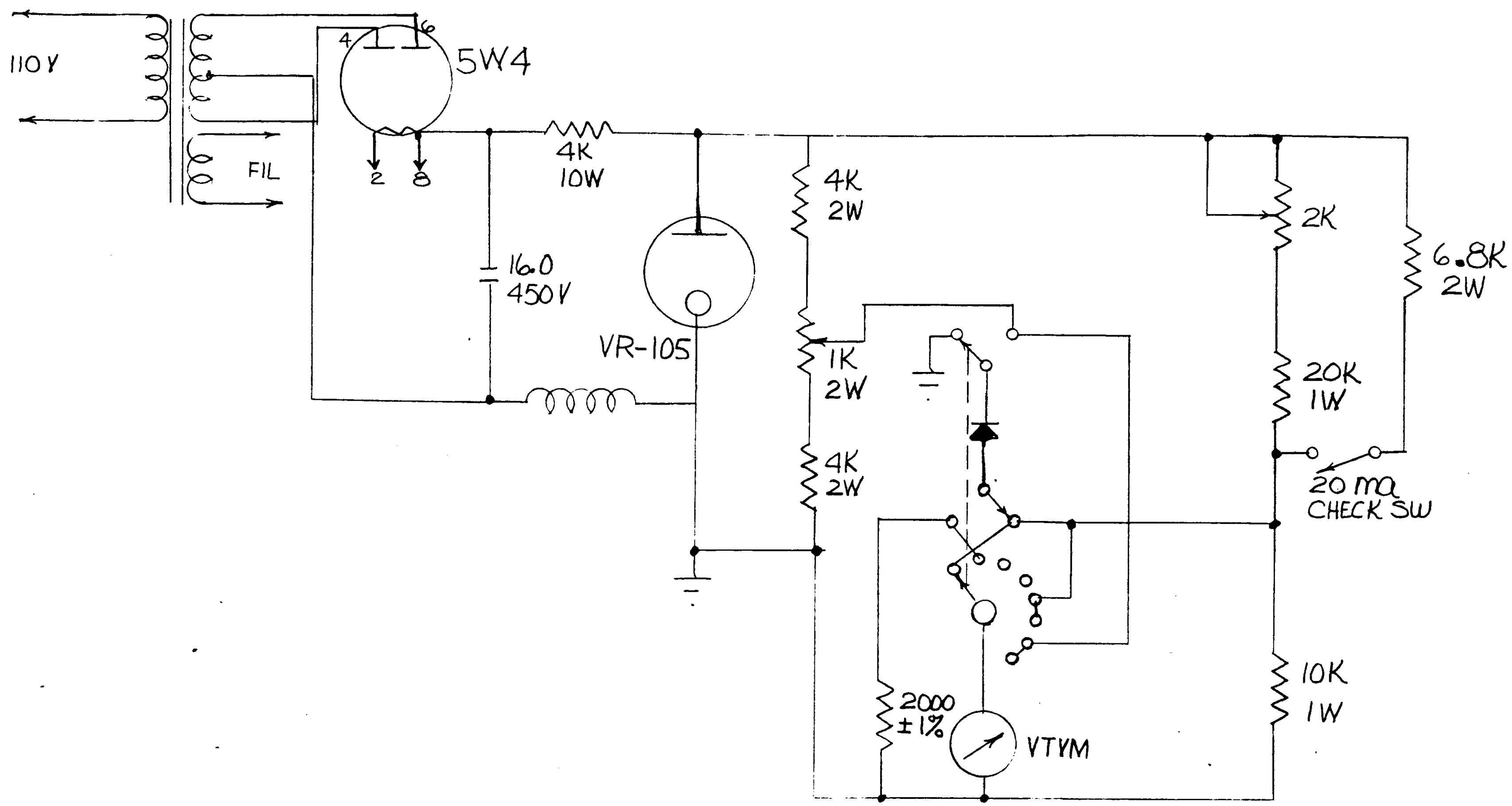
2.2 330V, 6AG7 Flipflop.



330V, 6AG7 FLIPFLOP

Issued 7-15-49
Reissued 4-20-51

3.1 Crystal Checker



Checks forward resistance at 5 ma and 20 ma.

Checks backward resistance at -50 V.

3.1 Crystal Checker

Explanation:

1. Connect Sylvania VTVM - set to +100 V scale - zero meter.
2. Set crystal checker selector switch to "Forward Res. Volt. Check" position.
3. With "Forward Res. Volt. Adj.", set voltage to +34.2 V.
4. Turn crystal selector switch to "Back Res. Volt. Check" position.
5. With "Back Res. Volt. Adj.", set voltage to +50 V.
6. Set checker selector switch to "OFF" - use Position No. 4 - insert crystal - observe polarity.
7. Set meter to +3 V scale - zero meter.
8. Set selector switch to "Forward Res. Position" - 1 V = 200 ohms*.
9. Press forward resistance 20 ma button - 2 V = 100 ohms**. Do not hold long at this position.
10. Set selector to "Back Res. Position" - 1 V = 100 K***.
11. Set selector switch to "OFF" - insert next crystal - repeat steps 7-11.

* 0-1 V = 0 ohms - 200 ohms

** 0-2 V = 0 ohms - 100 ohms

*** 0-1 V = INF - 100 K

3.2 CRT Memory Test Unit.

Introduction

The Cathode Ray Tube Memory Test Unit (hereafter referred to as the Test Unit) was designed and constructed primarily as a test unit for the electrostatic memory units of the SWAC and secondarily as a unit with which further development work on cathode ray tube memory devices might be performed.

This section of the manual describes the use and operation of the Test Unit. Information which may be used as a guide for maintenance of the memory units can be found in Section D2.1.

General

The Test Unit is divided into two racks, the Power Rack and the Test Rack. The Power Rack contains part of the power supplies (some of the voltages are obtainable from the main laboratory supply) and the voltage regulators necessary for operation of the Test Unit. Following is a list of voltages used in the Test Unit:

Test Unit Voltages

Unregulated Voltages	Location of Supply
+600	Power Rack
+350	Laboratory Supply
+165	" "
+120	" "
-15	" "
-165	" "
-300	Power Rack

Regulated Voltages	Derived From	Location of Regulator
+500	+600	Power Rack
+250	+350	Laboratory Supply
+110	+250 regulated	Power Rack
-200	-300	" "
- Hi Voltage		Laboratory Supply

3.2 CRT Memory Test Unit.

Power Rack

The power controls for the Test Unit are located on the Power Rack. The "AC" switch applies heater voltage to all tubes, and power to blowers and power supplies. A delay relay prevents other voltages from being applied until two minutes after the "AC" switch is operated. This is to allow the larger tubes adequate warm-up time. After this delay has elapsed the low d.c. voltages may be applied, followed by the high d.c. voltages. The presence of these voltages is indicated by neons. The voltages can be applied only in the sequence listed above.

If, during operation, any low d.c. voltage fuse blows or a low voltage d.c. supply fails, the alarm system will remove all d.c. voltages from the circuits of the Test Unit. If the a.c. power to the Test Unit should fail, the d.c. circuit will also be de-energized.

Located on the Power Rack are a voltmeter and a test point. The switch below the meter selects the voltage to be metered and also a.c. couples that supply voltage to the test point so that a measurement of the ripple or noise may be made. The meter should read 1.0 if the supply being metered is operating properly.

There are two convenience outlets available at the side of the Power Rack.

Note: All d.c. voltages should be off when inserting or removing a memory unit.

Test Rack

1) Front Panel:

The front panel of the Test Rack holds the flaw-tester controls, spillover control, fill and clear of memory unit control and the S register controls. The pulses most necessary for memory unit testing are made available at test points on the front panel. Some of the delay lines used in the Test Rack have been brought out to the front panel and spare lines of various electrical length have been provided.

The four input pulses to the memory unit are variable in amplitude and their controls are located on the front panel. These pulses are

3.2 CRT Memory Test Unit.

BP, GP, SP^{oo} and M → m. Their amplitude can be varied from normal to zero. See pages A3.2-4 and A3.2-5 for circuits.

2) Fill and Clear:

To fill a memory unit completely with dashes the Dot-Dash switch is placed in the dash position (up) and the Fill and Clear Memory switch pushed up (Fill Memory). To clear the memory unit completely (Store Dots) the Fill and Clear Memory switch is pushed down (Clear Memory). In clearing, GP to the CRT unit is interrupted. In filling, M → m_t is inverted and used to flip the CRT unit flip-flop.

3) Spillover Control:

The four S register controls select the address of the writing action used for spillover test or for writing a dash or dot in a particular address. The selection of a dot or dash input is made with the Dot-Dash switch. To read into the memory unit the switch labeled "write" is moved to "write". The number of times the dot or dash is read into the memory unit during a full regeneration cycle is determined by the switch marked "Spillover Control". See pages A3.2-6 and A3.2-7 for circuitry.

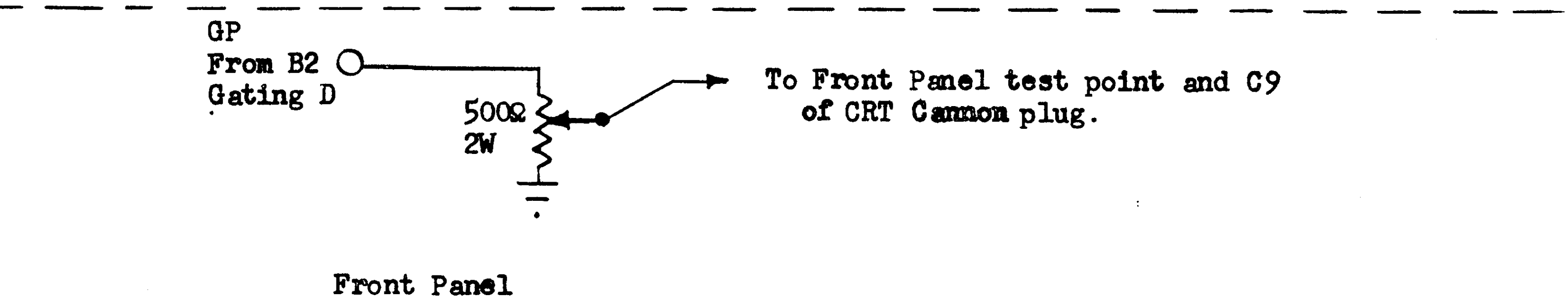
4) Flaw Tester:

To test for flaws on a memory unit, move the Normal-Flaw Test switch to "Flaw Test". Connect the "Sweep Output" of the 512 Tektronix Oscilloscope to the "Sweep Input" terminal on Test Rack. Set the oscilloscope sweep control to the desired frequency (use 50 μsec/cm preferably) and set the sweep to run free. Adjust the potentiometer, on the Test Rack, labeled "Sweep Control" until desired length of sweep is obtained. Move X and Y positioning controls and observe output of memory unit amplifier with 511A Tektronix Oscilloscope using "Gate Output" of 512 Oscilloscope as trigger for sweep of 511A oscilloscope.

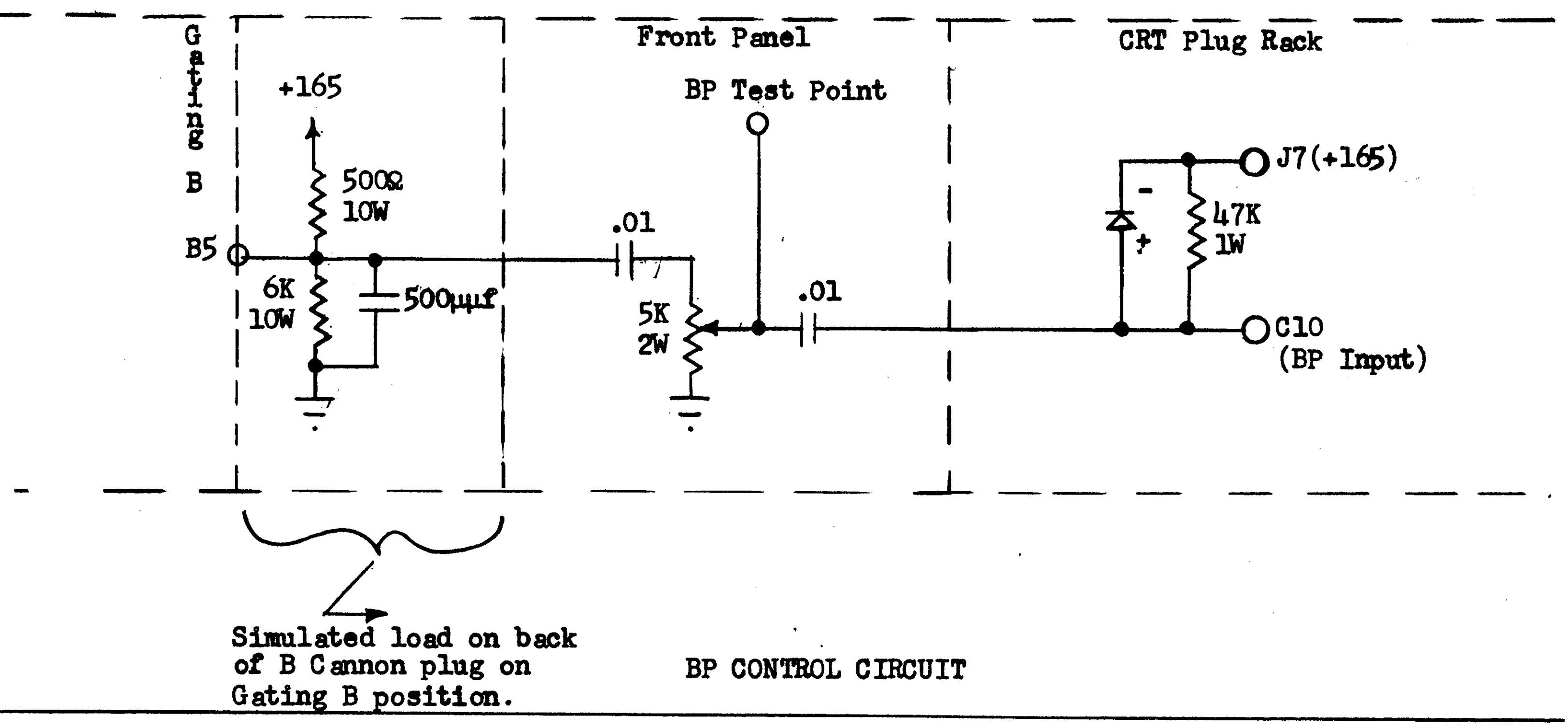
5) Oscilloscope Synch:

Provision has been made for selecting any of the pulses available at the front panel as an oscilloscope synch. The selected synch pulse is available at the bottom of the Test Rack at a coax connector. A special cable is provided for this purpose.

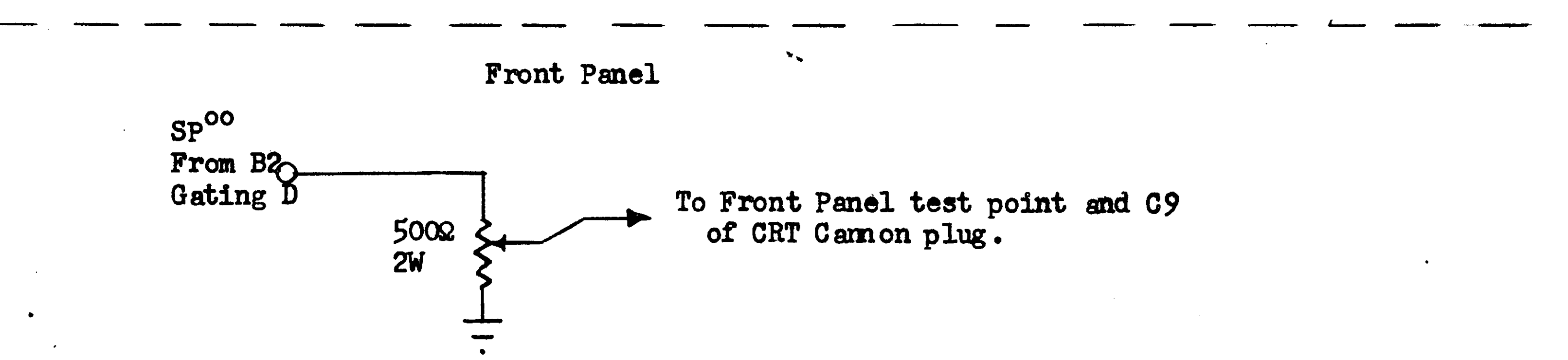
3.2 CRT Memory Test Unit.



GP CONTROL CIRCUIT



BP CONTROL CIRCUIT

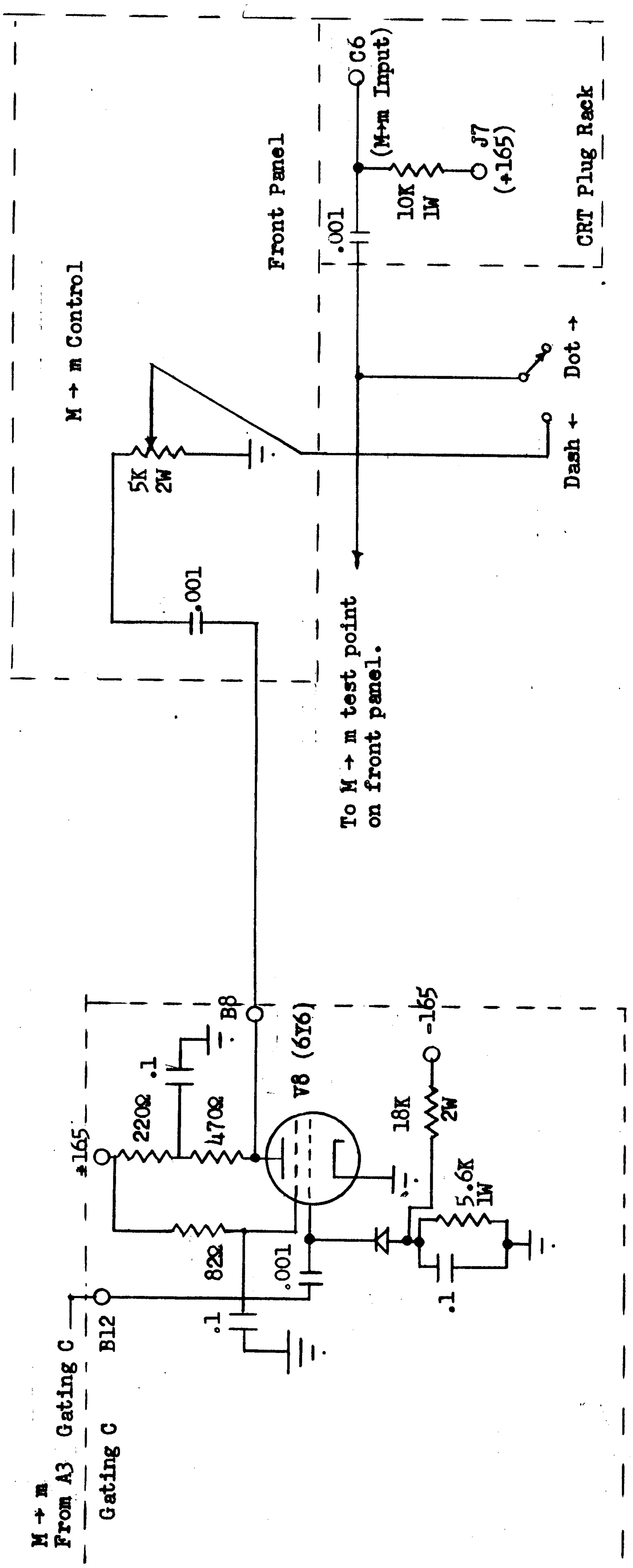


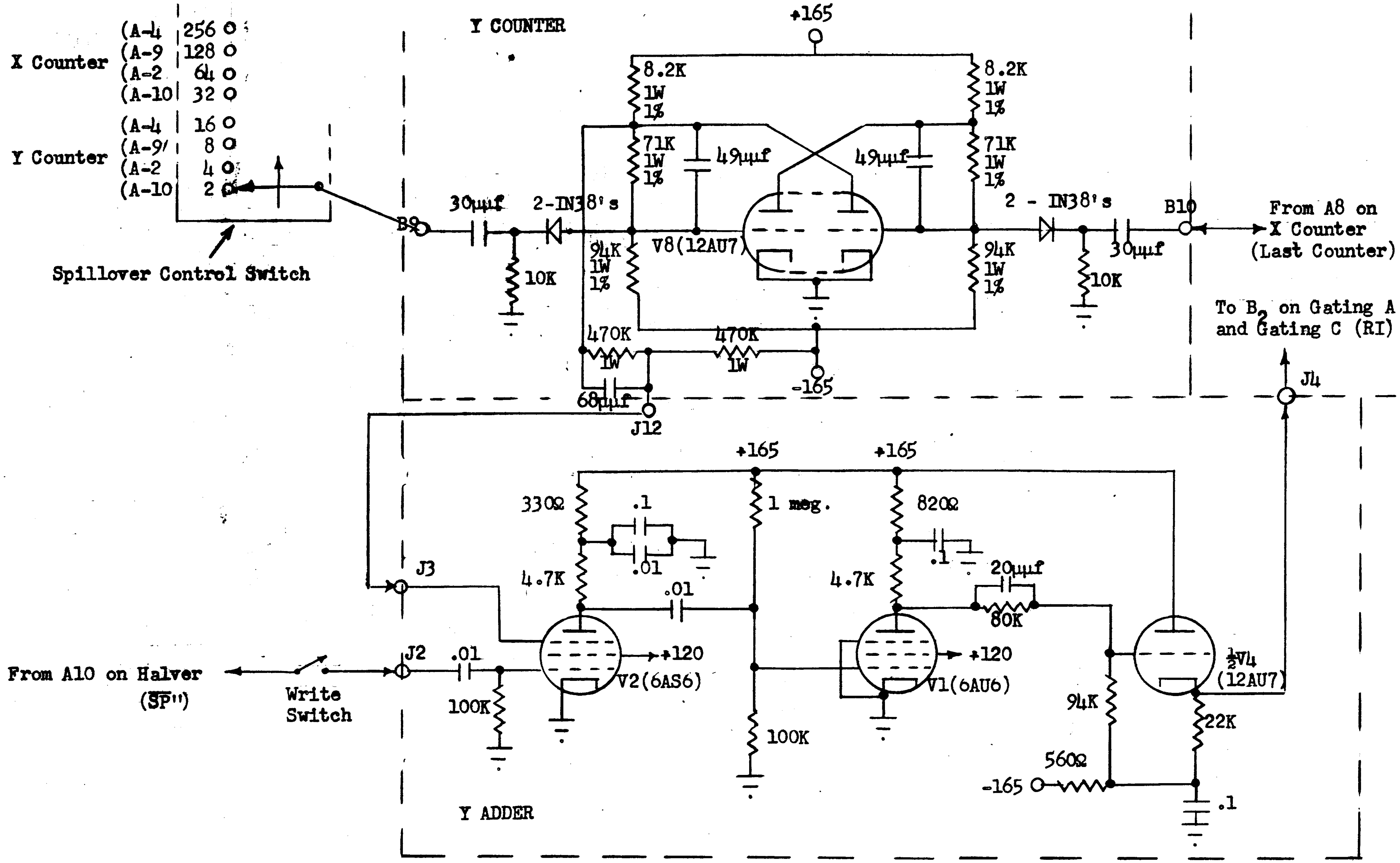
SP^{oo} CONTROL CIRCUIT

CHK

3.2 CRT Memory Test Unit.

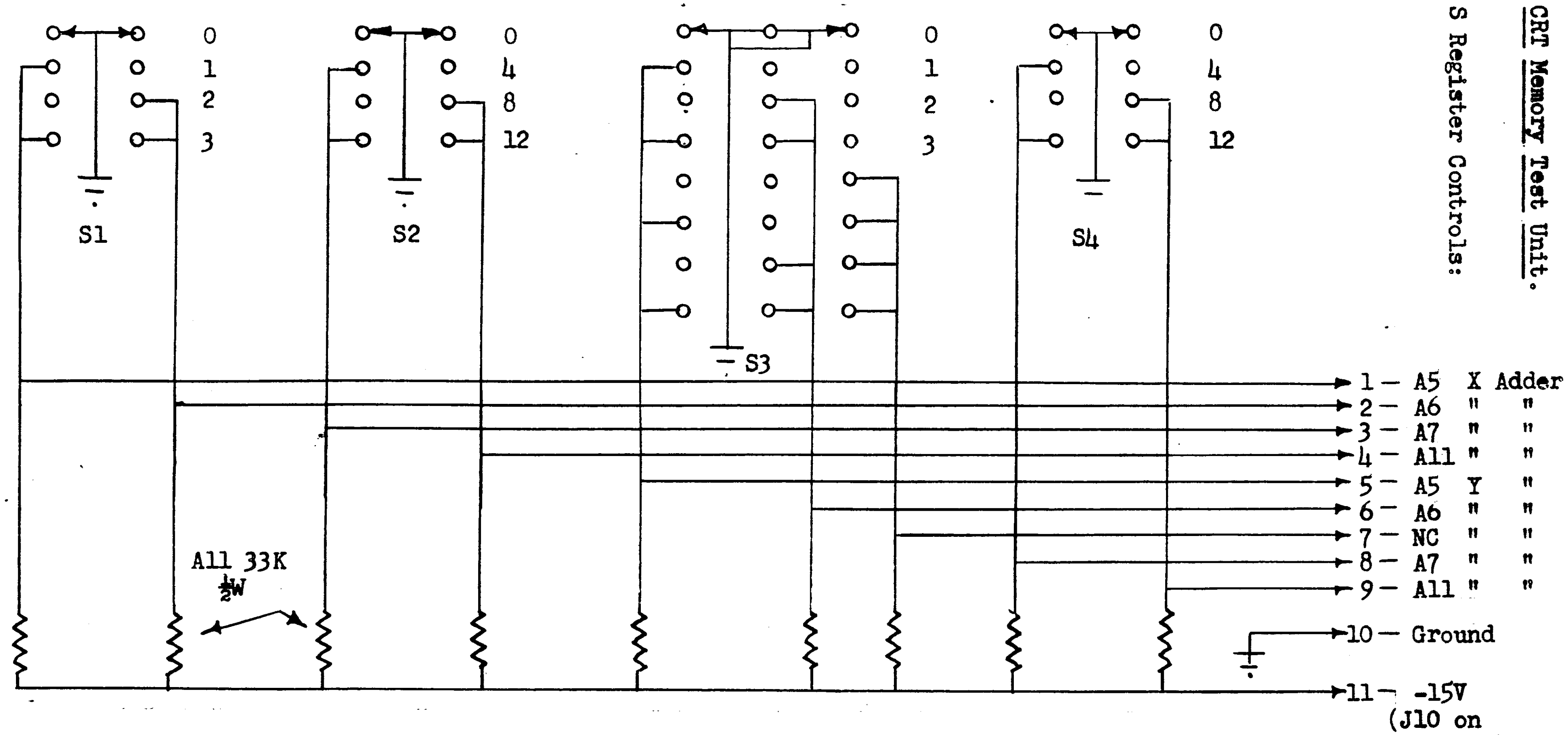
M → m Control Circuit and Dash-Dot Selector Switch:





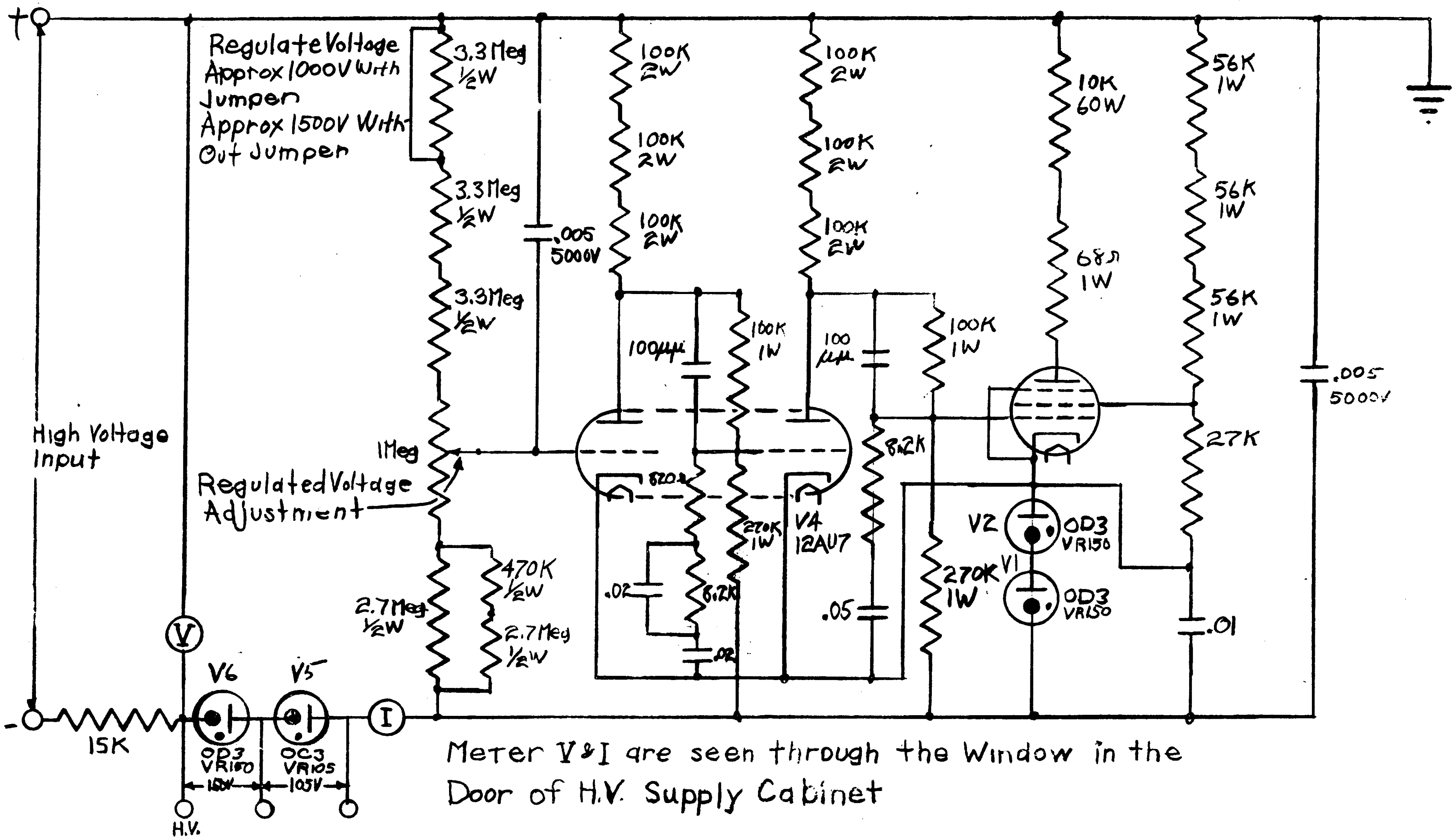
SPILLOVER TEST CIRCUITRY

S Register Controls (Switch positions as viewed from front of rack.)



Note: S3 has been wired so that expansion of memory capacity to 512 cells per CRT Unit is possible.

CHK



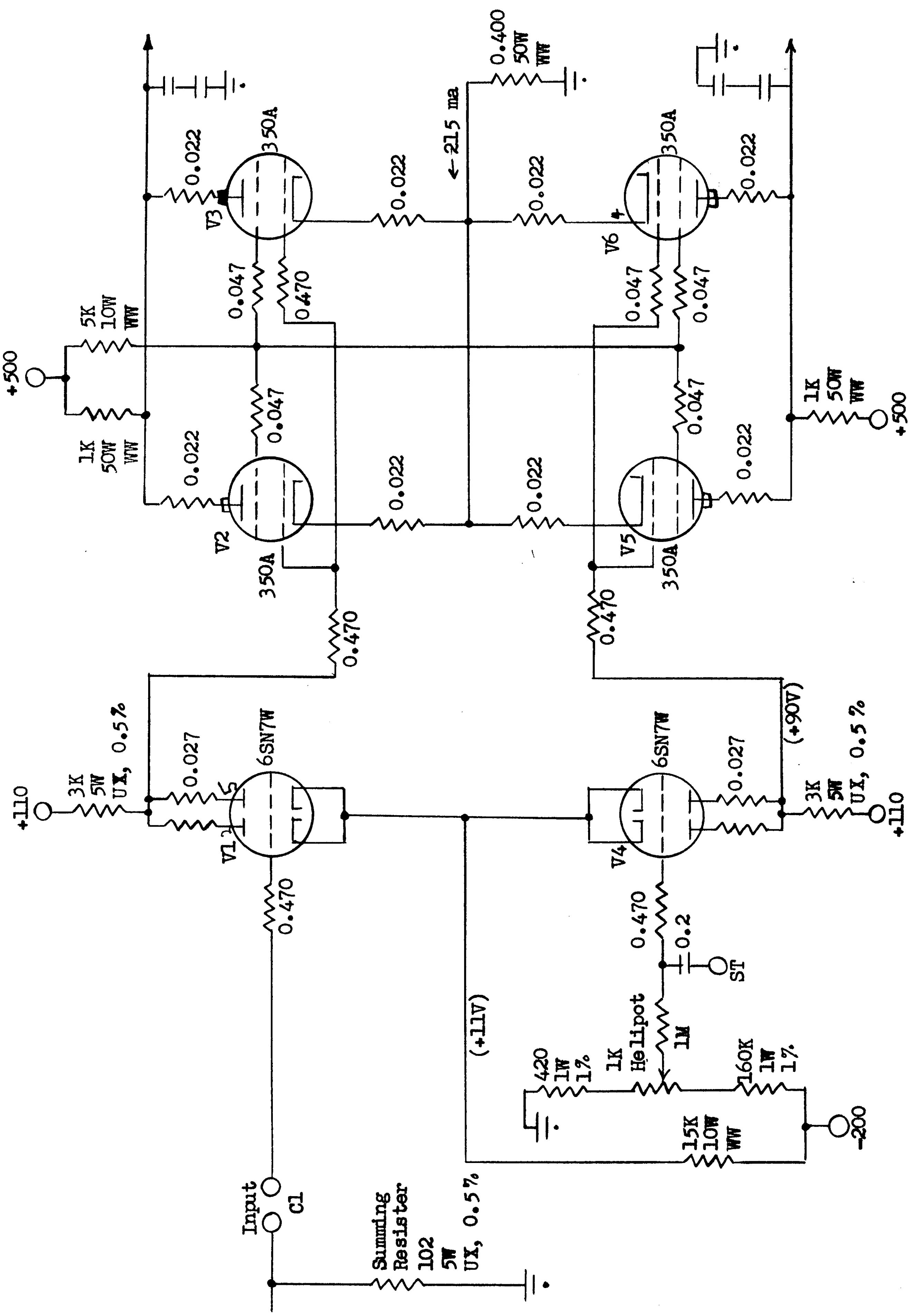
High Voltage Regulator System for CRT Test Unit

3.2 CRT Memory Test Unit.

NOTE: Information concerning Regulated Laboratory Power Supply 3, High Voltage Supply for CRT Memory Test Unit, will be found in Section A7.4 of this manual.

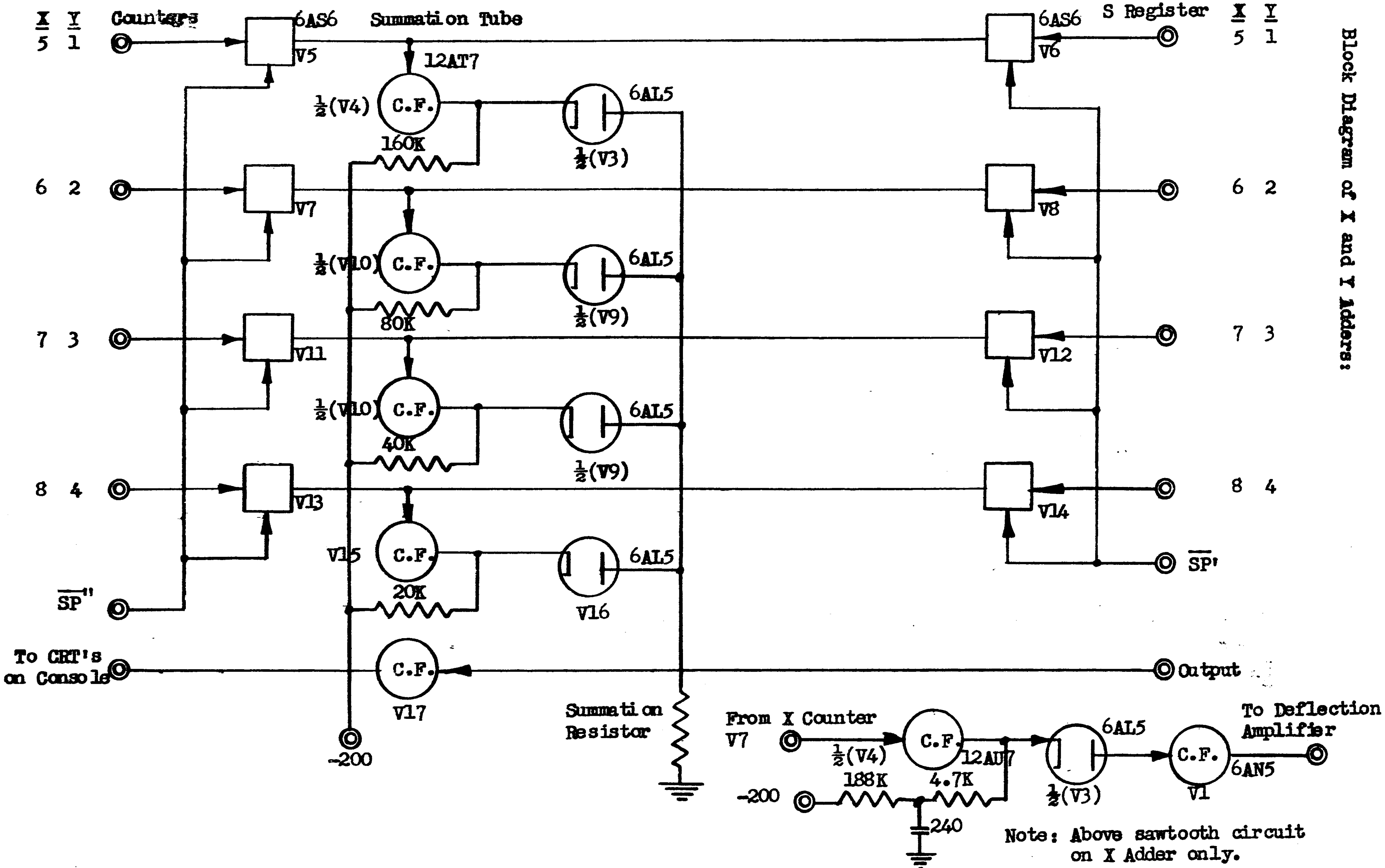
3.2 CRT Memory Test Unit

CRT DC Deflection Amplifier:



3.2 CRT Memory Test Unit

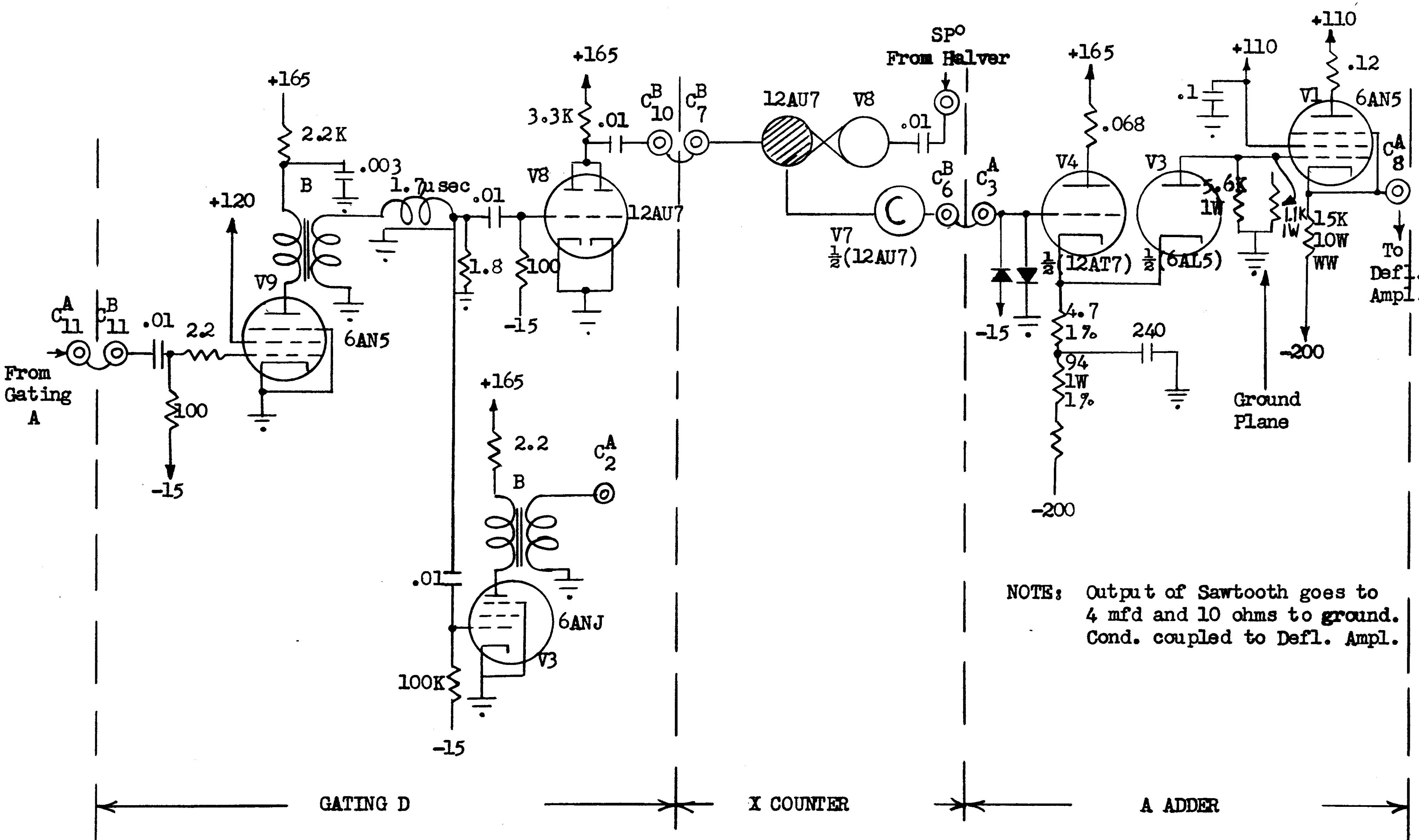
Block Diagram of X and Y Adders:



Issued 7-3-51
Reissued 10-27-53

3.2 CRT Memory Test Unit

Gating and Driving Circuitry:



NOTE: Output of Sawtooth goes to 4 mfd and 10 ohms to ground. Cond. coupled to Defl. Ampl.

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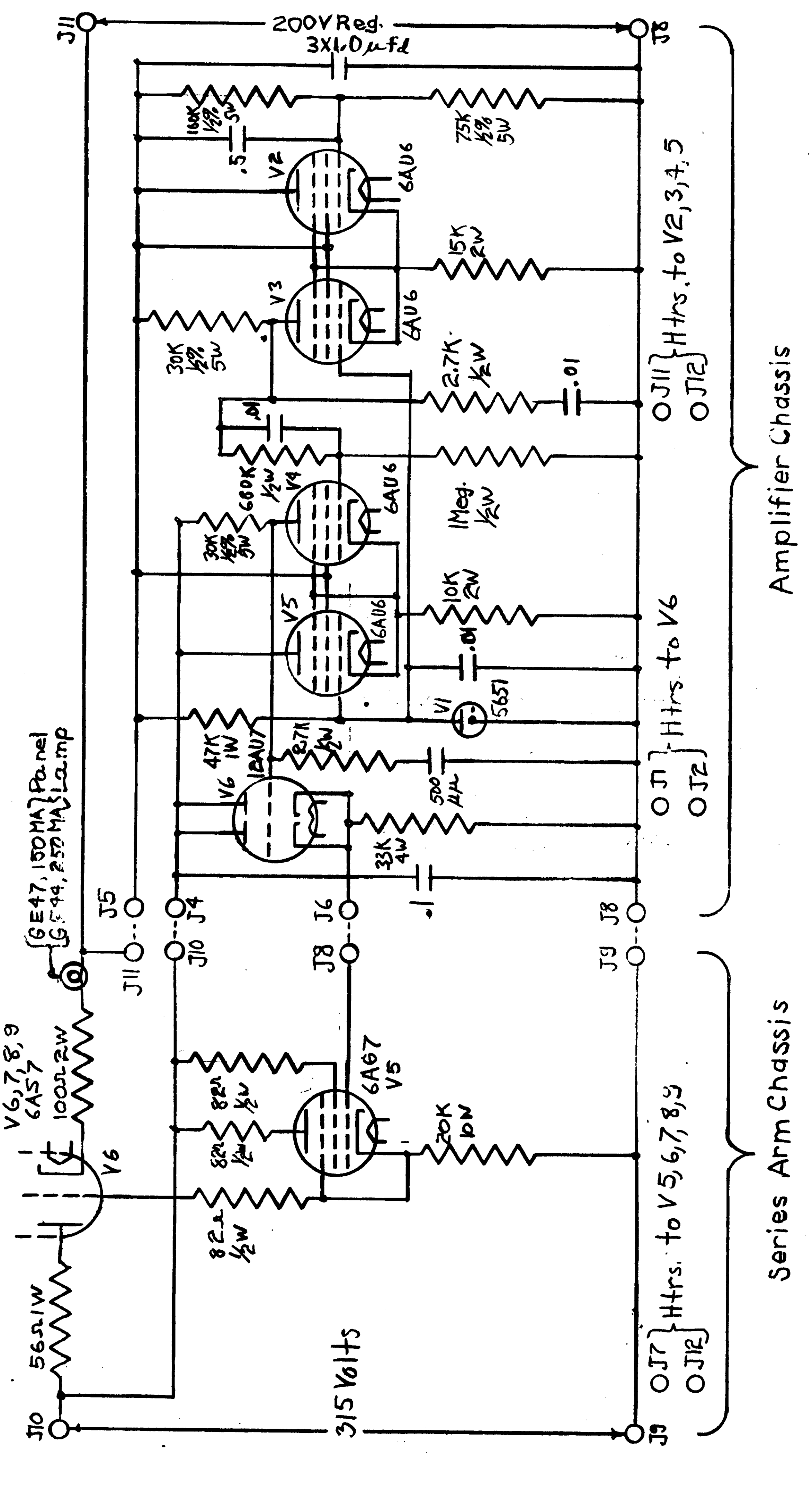
10-30-53

3. Test Equipment
~~4. POWER SUPPLY~~

INA 51 - 4
~~B 4.6-1~~
A 3.2-13

3.2 CRT Memory Test Unit
~~4.6~~ Regulators (Supersedes page A7.3-1 entitled 200V, 600 Ma. Voltage Regulator).

-200 Volt Regulator:



N.F.L.

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3. Test Equipment

~~4. POWER SUPPLY~~

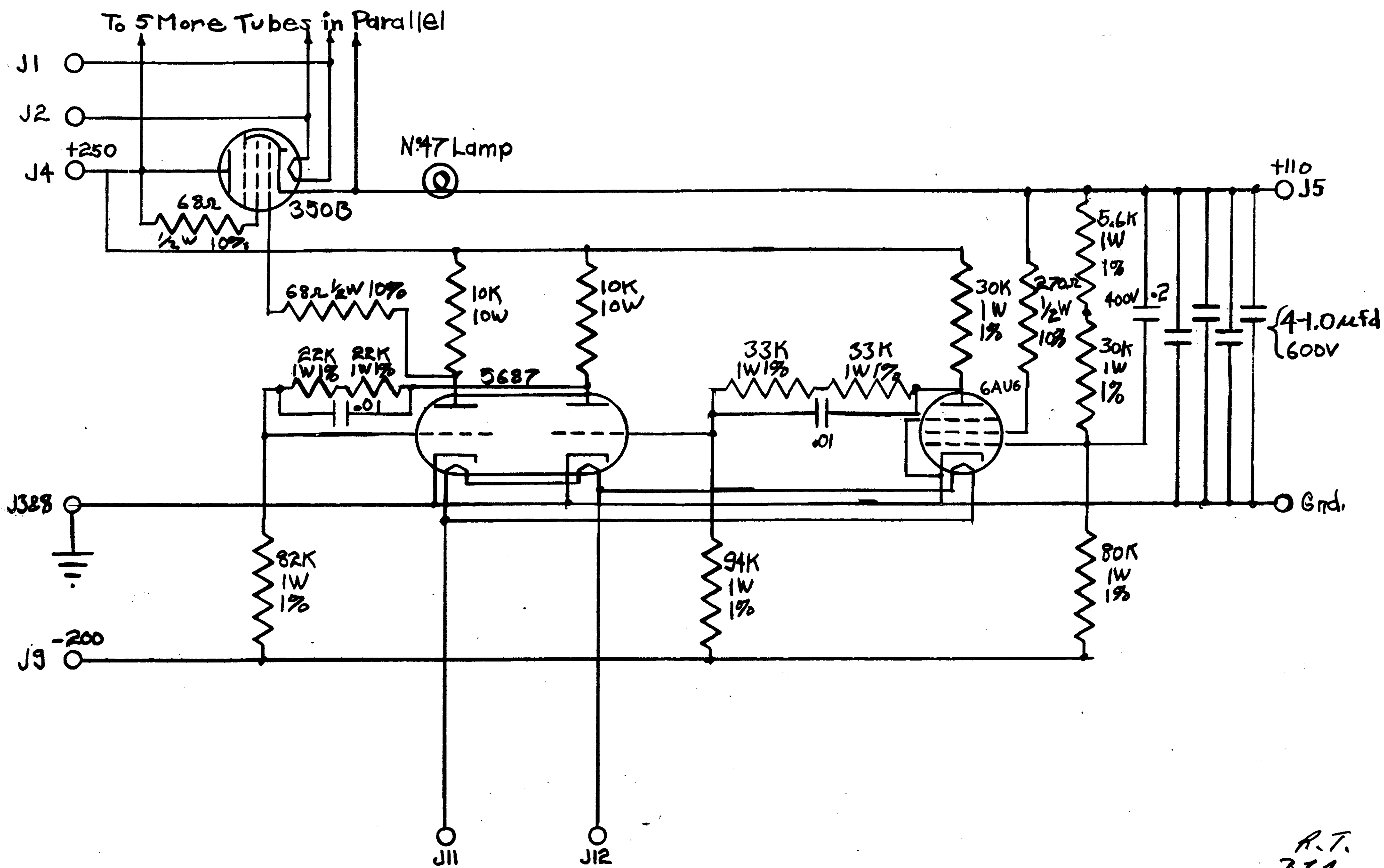
Issued 9-23-49
Reissued 2-15-52
Reissued 2-27-52
10-30-53

3.2 CRT Memory Test Unit

~~4.6~~ Regulators. (Supersedes page A7.3-3 issued 2-15-52.)

110 Volt Regulator for CRT Deflection Amplifiers:

INA 51 - 4
~~B 4.6-2~~
A 3.2-14



R.T.
J.F.A.

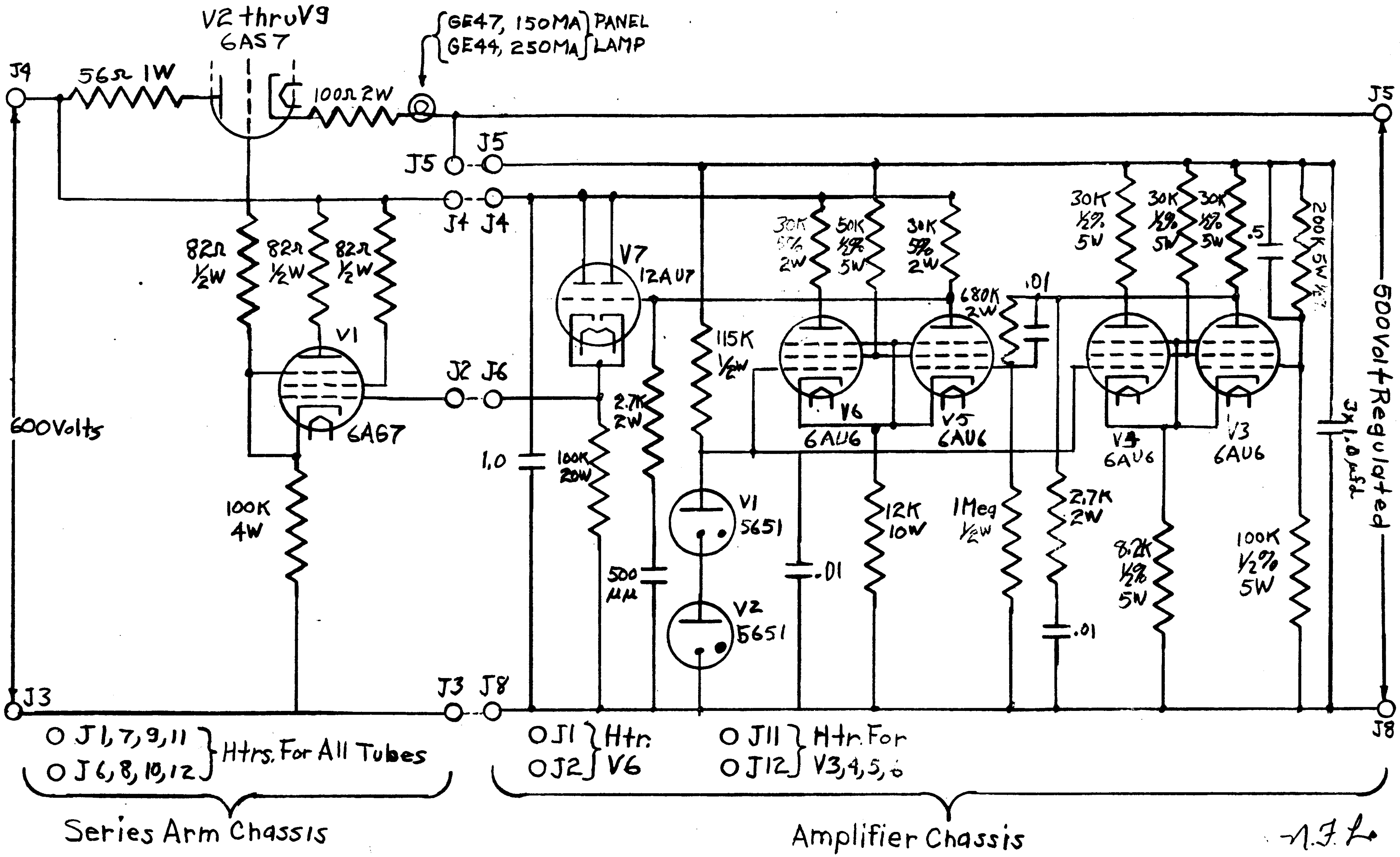
110 VOLT REGULATOR FOR CRT DEFLECTION AMPLIFIERS

3. Test Equipment ~~4. POWER SUPPLY~~

Issued 3-14-52

3.2 CRT Memory Test Unit
~~4.6~~ Regulators.

500 Volt Regulator:



INA 51 - 4
~~B 4.6-4~~
A 3.2-15

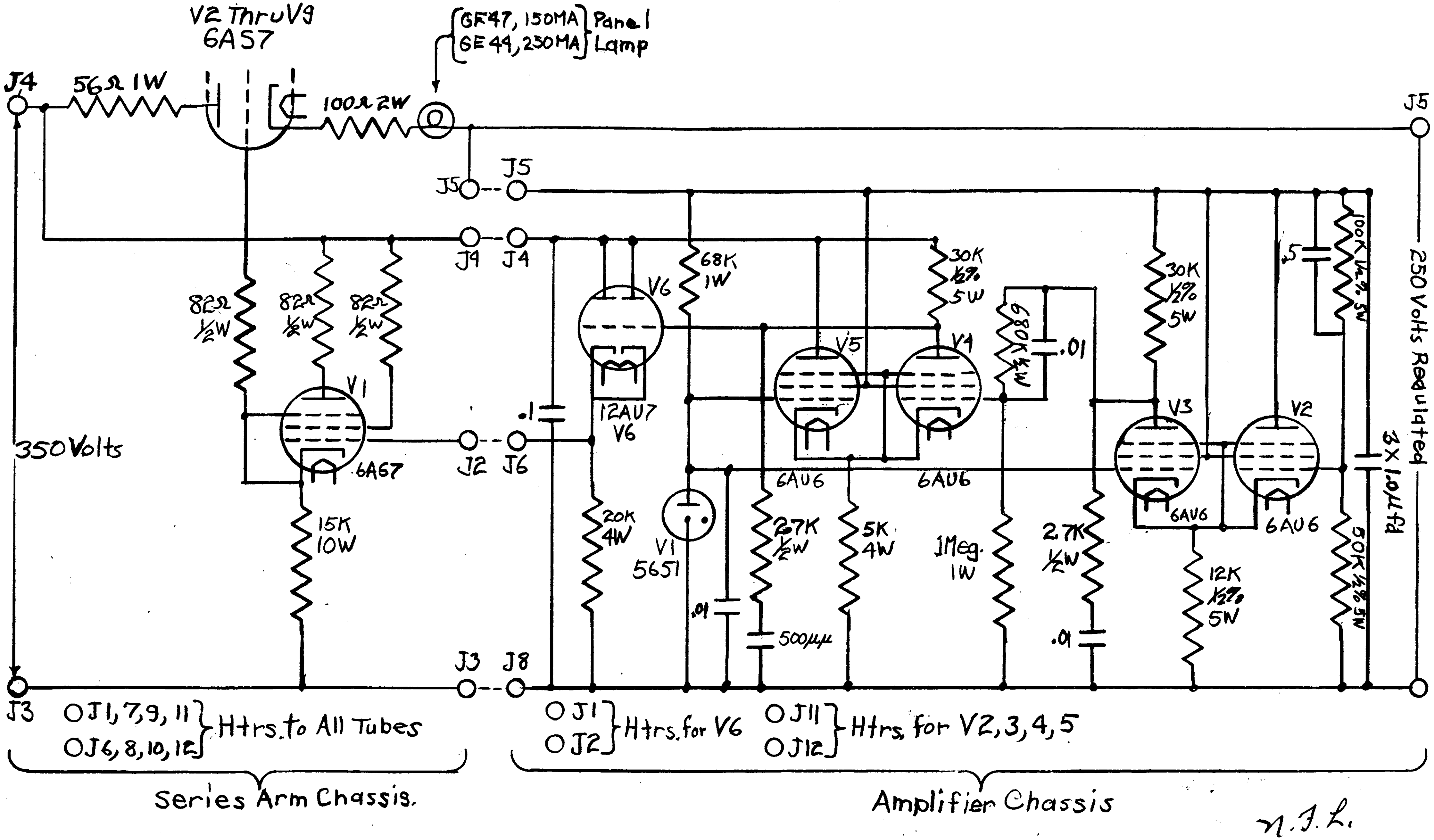
NATIONAL BUREAU OF STANDARDS

3. Test Equipment
~~4. POWER SUPPLY~~

Issued 3-17-52
10-30-53

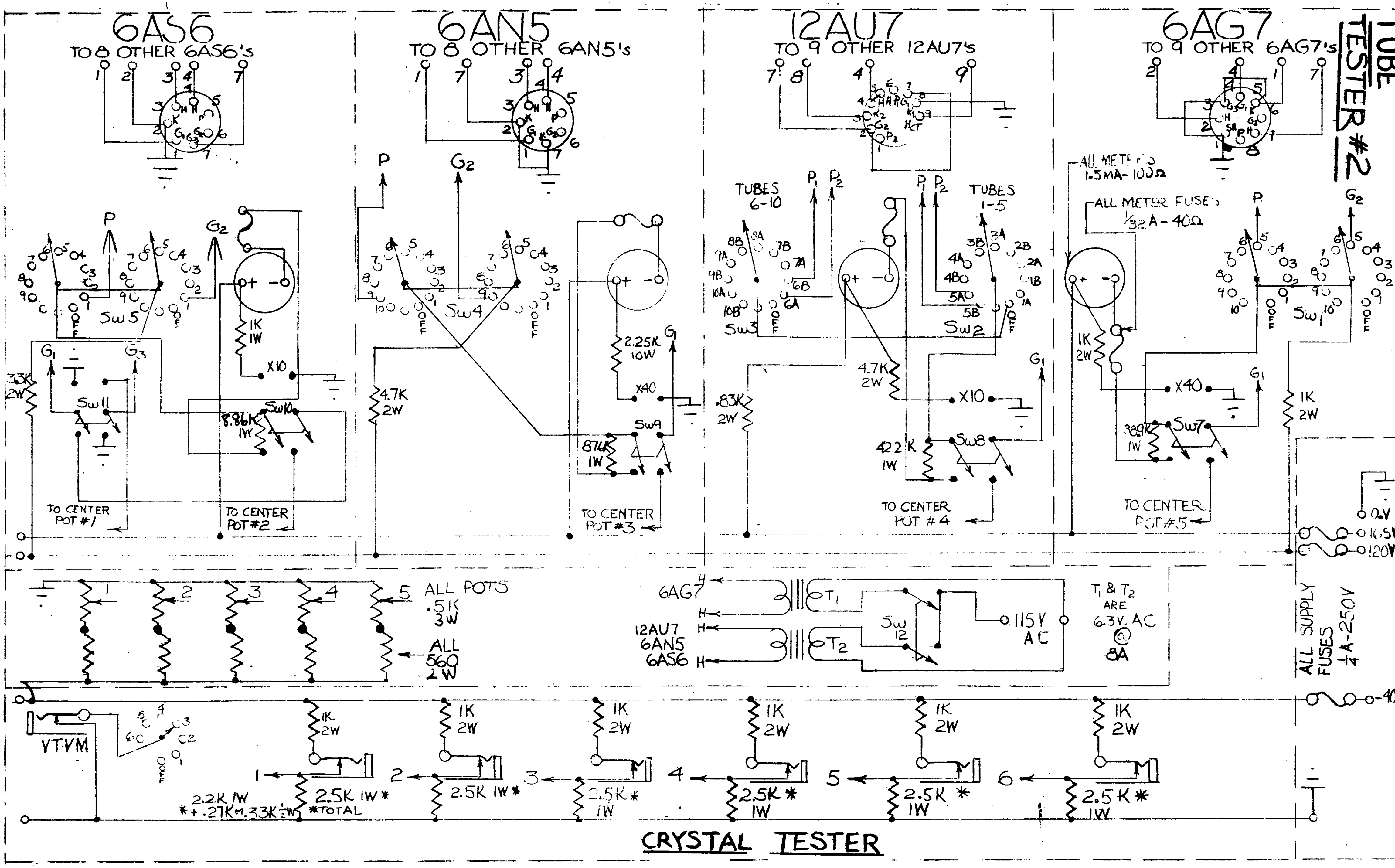
3.2 CRT Memory Test Unit
~~4.6~~ Regulators.

250 Volt Regulator:

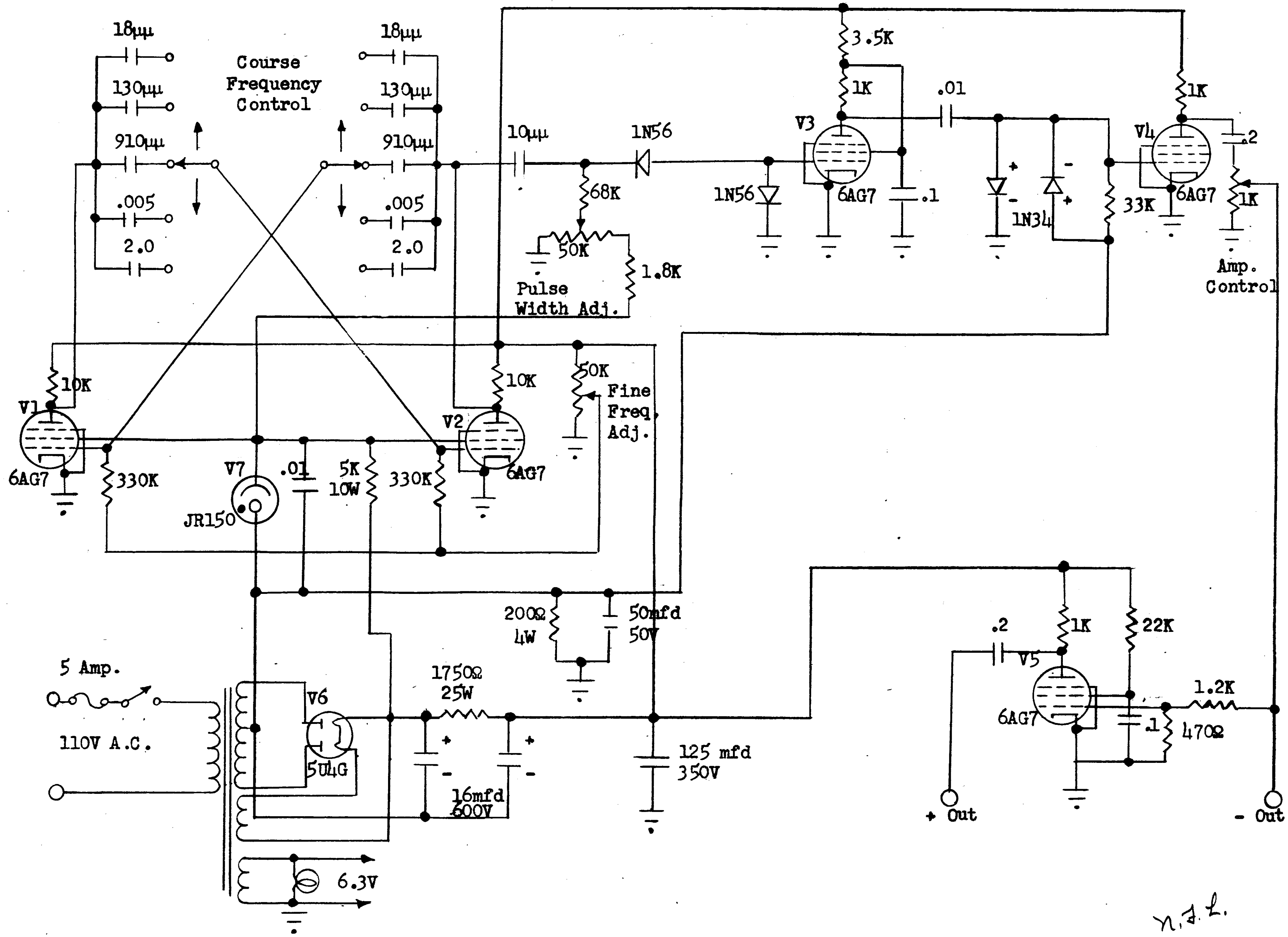


INA 51 - 4
~~B 4.5-5~~
A 3.2-16

3.4 Tube Tester No. 2 and Crystal Tester.



3.5 Pulse Generator No. 1



n.f.l.

3.6 Arithmetic Test Unit. (This supersedes pages A3.6-1 thru A3.6-10, dated 4-20-51.)

I. Description of the Test Unit.

The Arithmetic Test Unit provides a means of:

a) Testing three A chassis and three M chassis simultaneously,

b) Testing one A chassis and one M chassis individually.

Provisions have also been made to test C Register chassis (see Procedure for Testing C Register Chassis, page A3.6-25).

The positions into which the chassis are to be inserted for testing are labeled Positions 1, 2 and 3 for the A and M chassis and Position C for the C Register chassis.

A. The Control Section. (See Block Diagram, page A3.6-6)

The Control Section consists of an "Oscillator" chassis, a "Special Driver" chassis, an "A Driver" chassis, and a "B Driver" chassis.

1. Oscillator Chassis.

All pulses used in the test unit are derived originally from the Oscillator Chassis. The primary pulse produced is called the Timing Pulse. The timing pulse is initiated by one of three sources selected by the Timing Pulse Selector (see drawing on page A3.6-8). These sources are:

a) a 125 KC free running multivibrator,

b) a Schmitt Trigger driven by an external oscillator such as the Hewlett-Packard Oscillator,

c) the Schmitt Trigger of b) driven by a microswitch. When the switch is depressed one timing pulse is produced.

The outputs of the Schmitt Trigger and the multivibrator are differentiated to allow the peaker coil more time to recover before being pulsed again and to minimize noise pickup from V3 and V4 by permitting the tubes to conduct a shorter time following the triggering step voltage.

Also located on the oscillator chassis are five delay line drivers, the functions of which will be described later.

3.6 Arithmetic Test Unit.

2. Special Driver Chassis.

The output of the 125 kc multivibrator on the oscillator chassis is also used to drive the Special Driver. The outputs of this driver are connected to the Pulse Polarity Switch on the Control Panel and then to three flipflop switches labeled R-FF, M-FF and A-FF. With the Pulse Polarity Switch in the "Normal" position, pulses of the proper polarity are introduced on appropriate lines to the test positions to fill or clear the flipflops. To fill or clear the R, M or A flipflop, move the corresponding flipflop switch to the "one" or "zero" position respectively (only the flipflops in position 2 may be filled). With the Pulse Polarity Switch in the "Reverse" position, the polarity of all these pulses is reversed (see diagram on page A3.6-9)

3. The A and B Driver Chassis.

Located on the A and B Driver Chassis are all of the eight functional drivers. These are the drivers which produce all of the pulses used to check the operation of the chassis to be tested. The amplitudes of these pulses may be varied by the Driver Amplitude Controls located on the front panel.

CAUTION: The bias for all of the functional drivers is brought in to the chassis from the amplitude controls through a six pin Jones plug located on the tagboard of each driver chassis. Do not turn on the D.C. voltages unless these Jones connections are made.

FUNCTIONAL DRIVER	PULSE OUTPUT	
	WIDTH μSEC.	POLARITY
Driver No. 1	0.5	Positive
Driver No. 2	0.5	Negative
Driver No. 3	0.5	Negative
Driver No. 4	0.5	Positive
Driver No. 5	0.5	Positive
K(A) Driver	0.1	Positive
K(M) Driver	0.1	Positive
Add Driver	0.1	Negative

3.6 Arithmetic Test Unit.

B. The Control Panel.

On the Control Panel are located all of the controls necessary to operate the test unit.

1. Filament Control Panel.

At the top of the test unit is located the Filament Control Panel. Controls A and B vary the filament voltages supplied to the test positions. The filament voltmeter may be switched to monitor any one of these three filament voltages.

SWITCH POSITION	FILAMENT VOLTAGE MONITORED
1	Filaments at D.C. Ground At A and M Positions
2	All Filaments At C Position
3	Filaments at -165 volts D.C. At A and M Positions

2. D. C. Fuse Panel.

Immediately below the filament control panel is located the Fuse Panel. All D.C. voltages supplied to the test unit are fused at this panel with grasshopper alarm fuses (see table below).

D.C. VOLTAGE	FUSE SIZE (Amperes)
+ 165	3
+ 135	1-1/3
+ 25	.180
- 15	½
- 25	.180
- 165	1-1/3
- 180	.180

If a grasshopper fuse blows, the particular D.C. voltage supplied to that fuse is applied to the coil of one of two alarm relays (depending on whether the D.C. voltage is positive or negative). The alarm relay in turn disconnects the power to the D.C. holding relays which in turn disconnect the D.C. supply (see diagram on page A3.6-7). A neon lamp labeled "D.C. AVAILABLE"

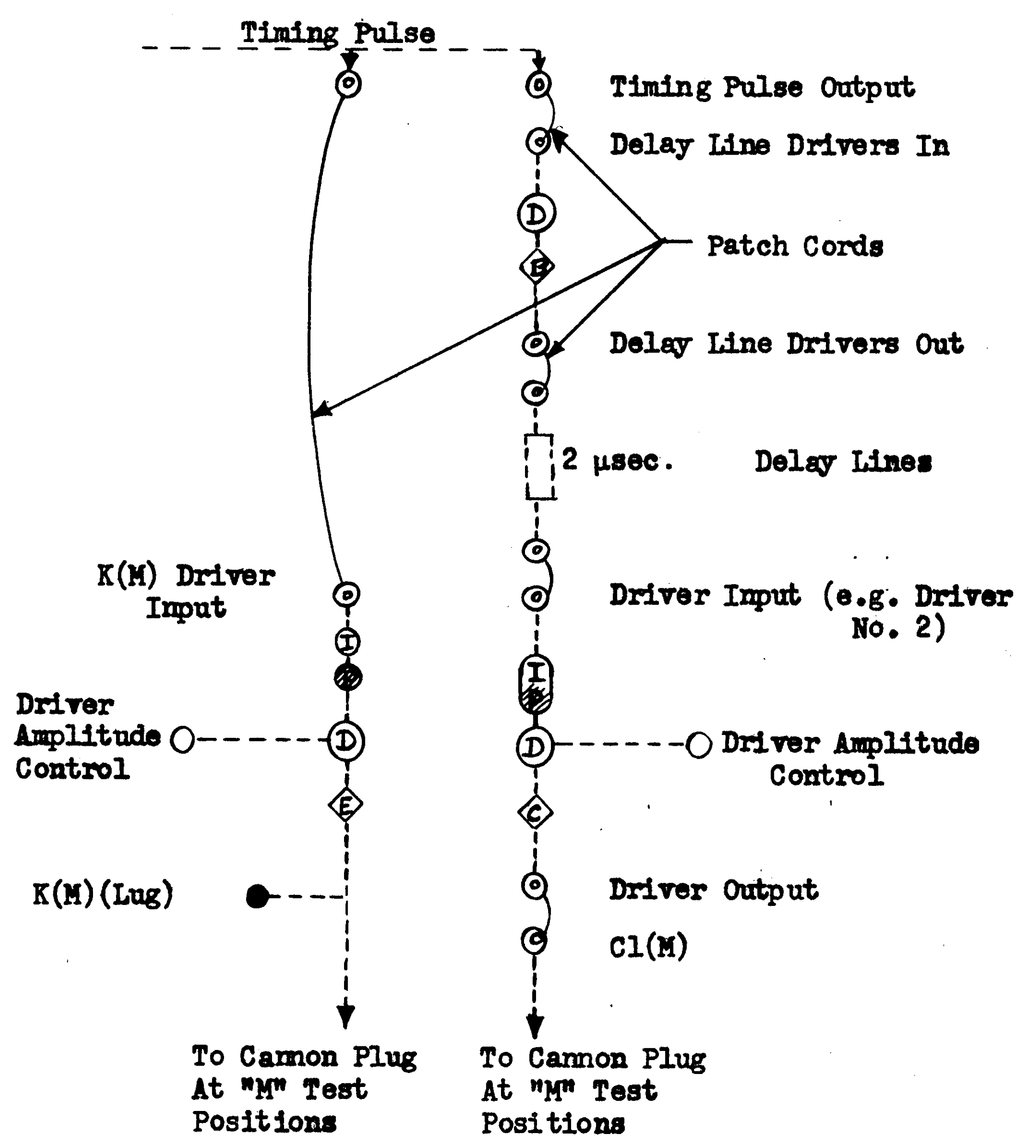
3.6 Arithmetic Test Unit.

is connected to the +165V D.C. input and indicates that the laboratory supply is on and that the test unit is connected to the supply.

3. The Patch Panel (see Drawing, page A3.6-10)

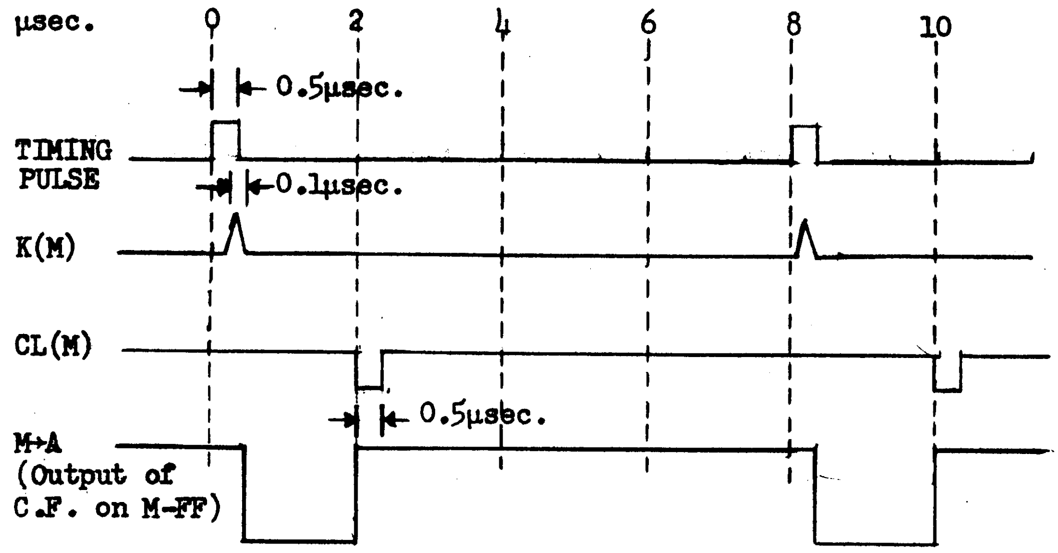
The Patch Panel is located directly below the fuse panel on the right-hand side of the test unit. At the top of the patch panel is located a row of eight paralleled banana jacks labeled "Timing Pulse Output". By means of patch cords the timing pulse and pulses of different delays may be used to drive the different functional drivers in the manner required to test the various logical circuits on the test chassis. A typical problem is illustrated below:

It is desired to complement the M flipflop and two microseconds later clear the M flipflop. It is also desired to perform this operation repeatedly so that operation of the flipflop may be observed with an oscilloscope. The connections on the patch panel required to do this are shown below:



3.6 Arithmetic Test Unit.

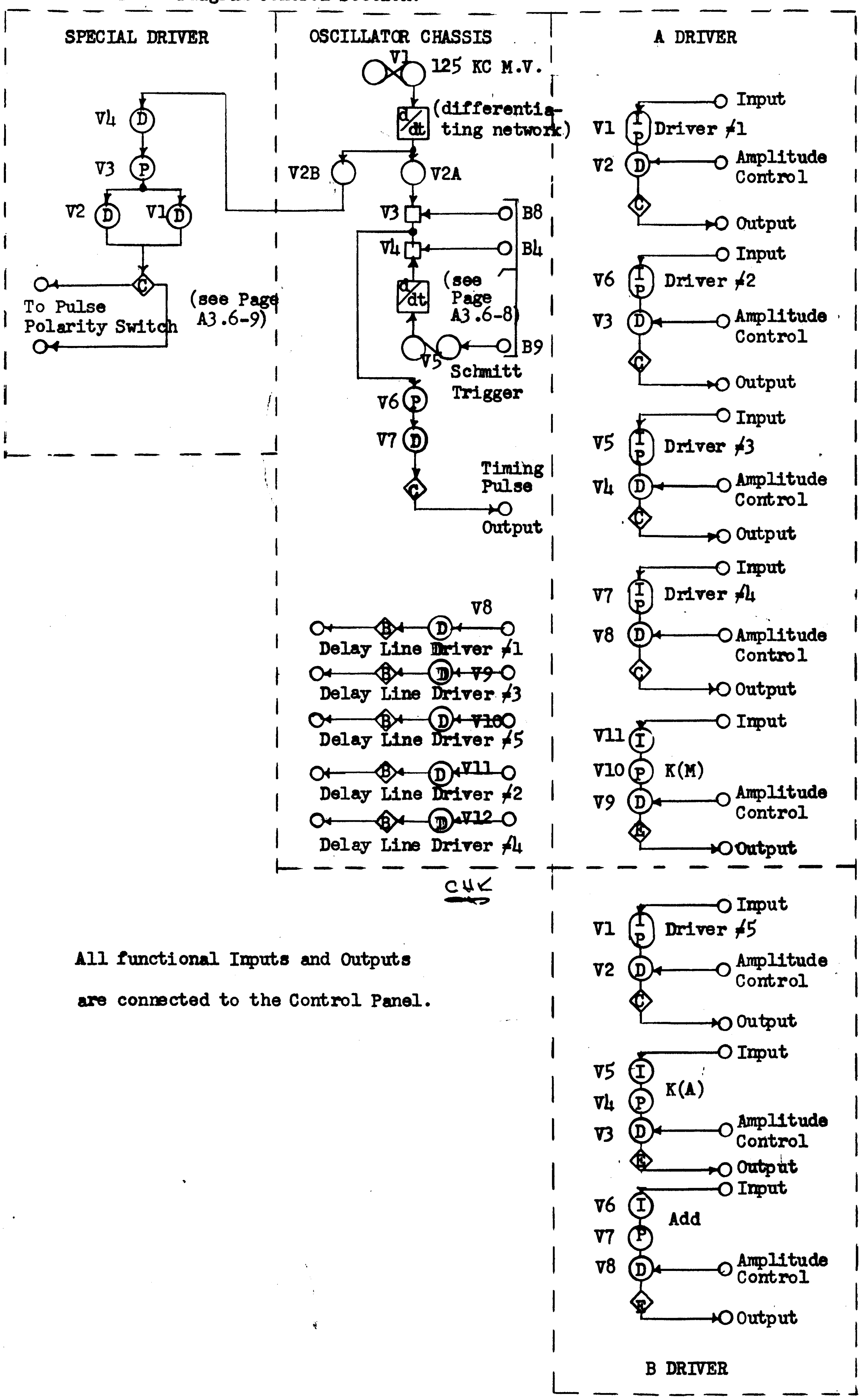
With the timing pulse selector switch on "Internal" the following timing will be observed:



Note the repetition rate as shown is 8 μsec. For a different repetition rate turn the timing pulse selector switch to "External" and connect the output of the Hewlett-Packard model 650A oscillator to the "External Osc." lug. With the 600 ohm load removed from the output of the Hewlett-Packard oscillator and with maximum output, the test unit may be reliably operated at frequencies from 10 cps to 130 kc.

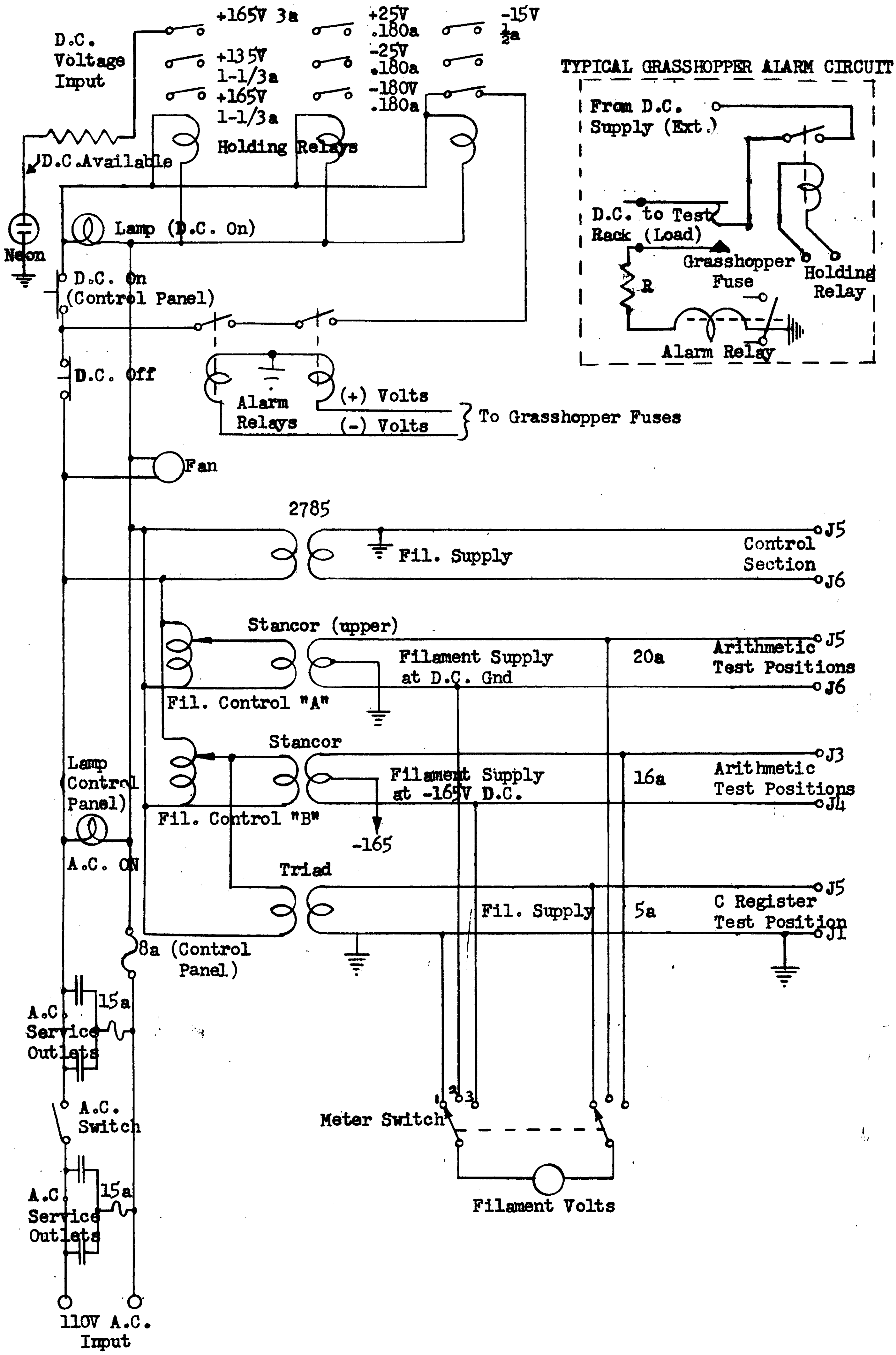
3.6 Arithmetic Test Unit.

Block Diagram Control Section:

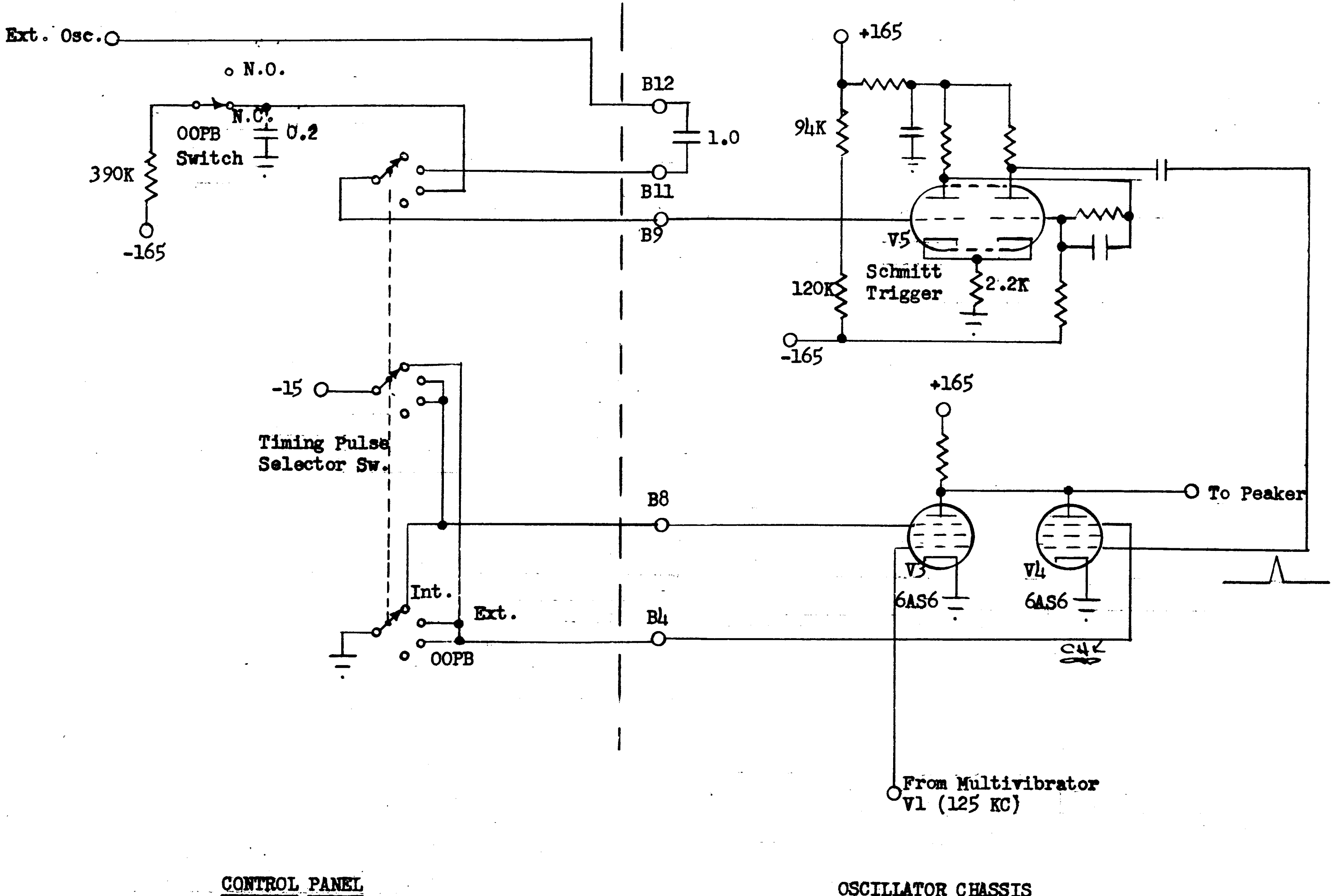


All functional Inputs and Outputs are connected to the Control Panel.

3.6 Arithmetic Test Unit.

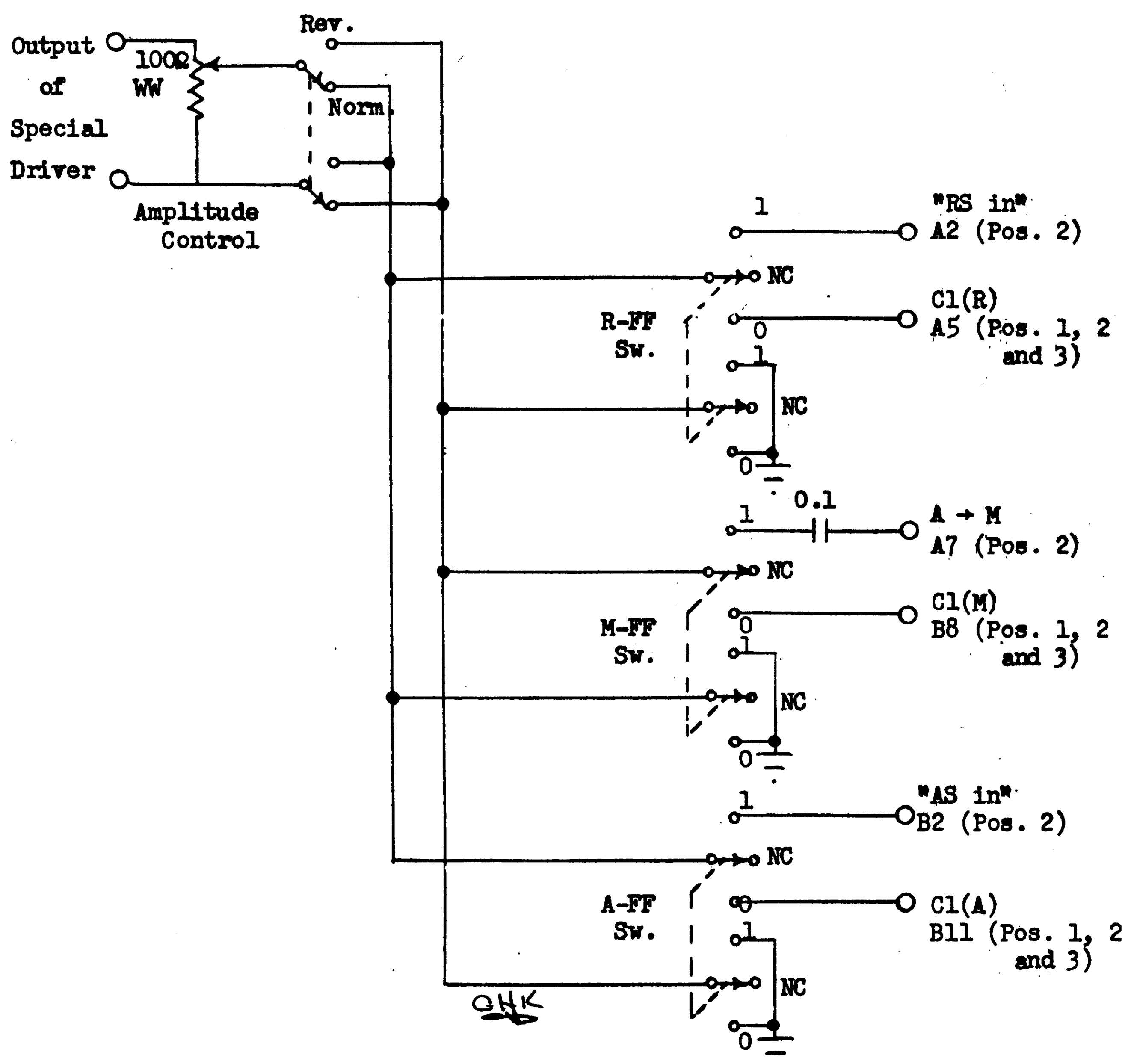


Timing Pulse Selector:



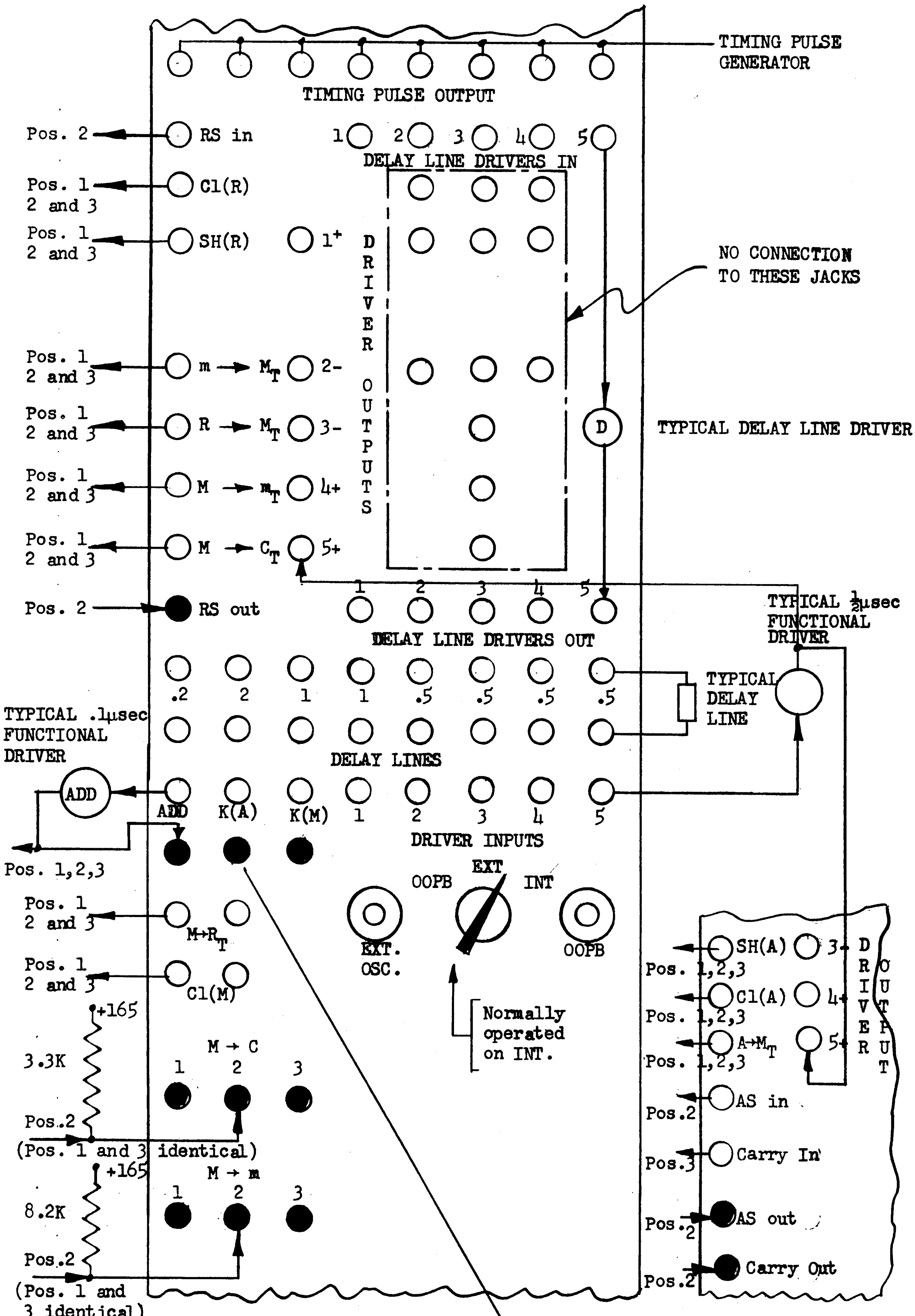
3.6 Arithmetic Test Unit.

Switching Circuit Utilizing the Special Driver:



3.6 Arithmetic Test Unit.

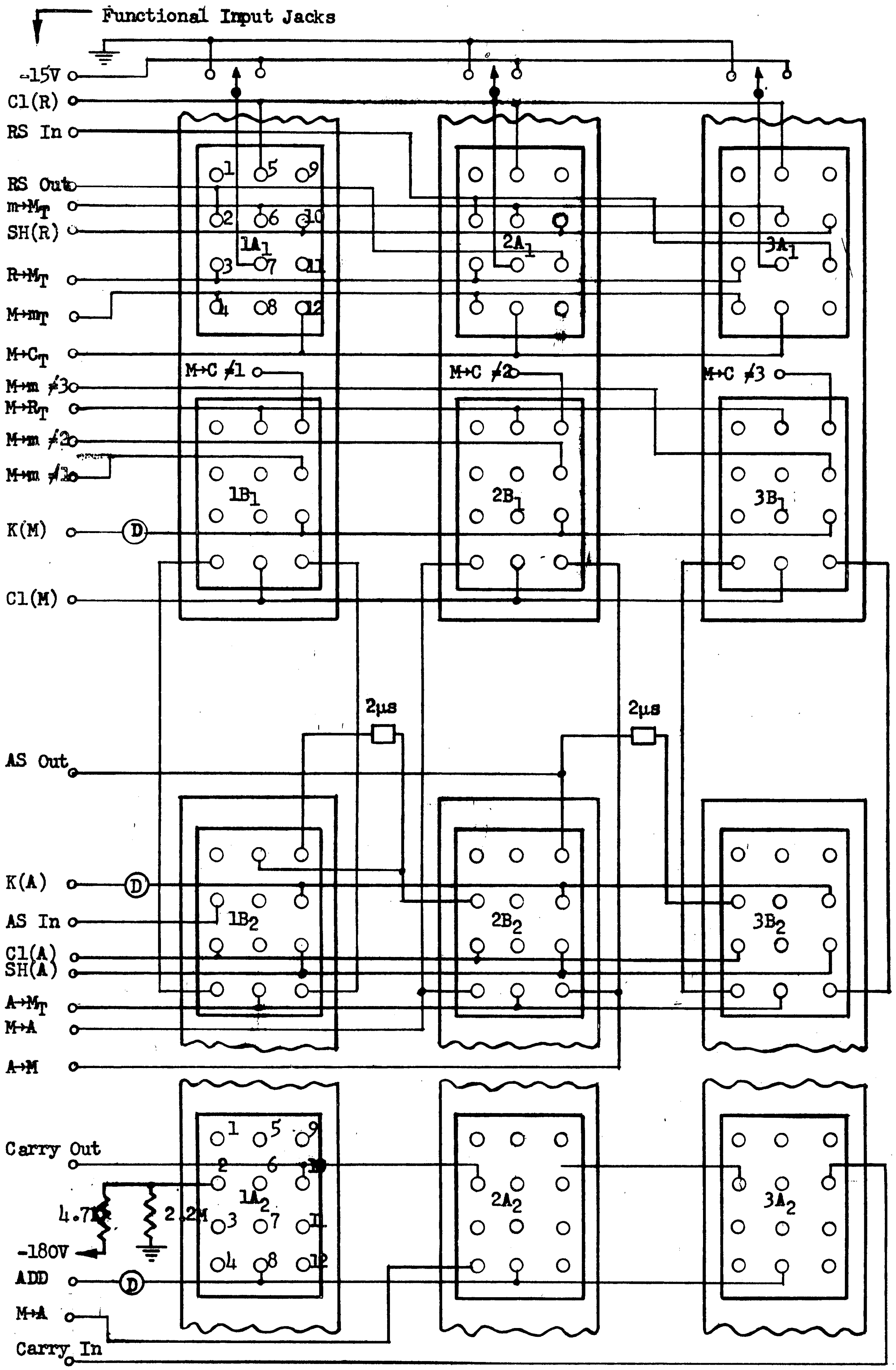
Plug Board of Arithmetic Test Unit:



Lugs carry the outputs of the ADD, K(A), and K(M) drivers for testing purposes.

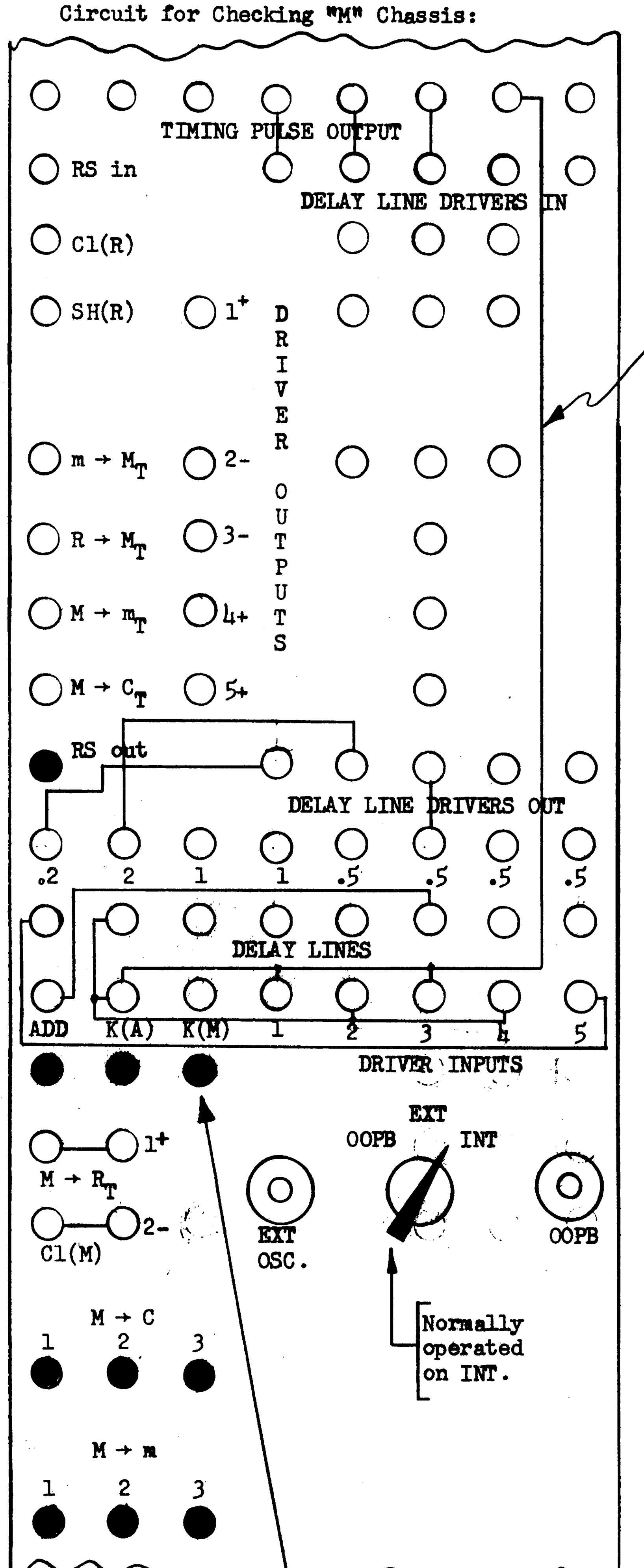
3.6 Arithmetic Test Unit.

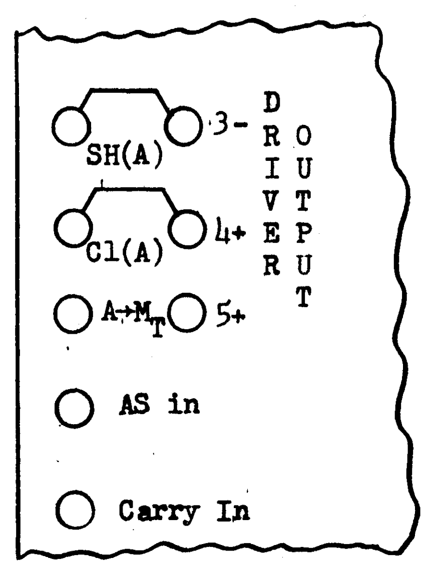
Cannon Plug Wiring on Arithmetic Test Unit (view from back of rack):



3.6 Arithmetic Test Unit.

Circuit for Checking "M" Chassis:

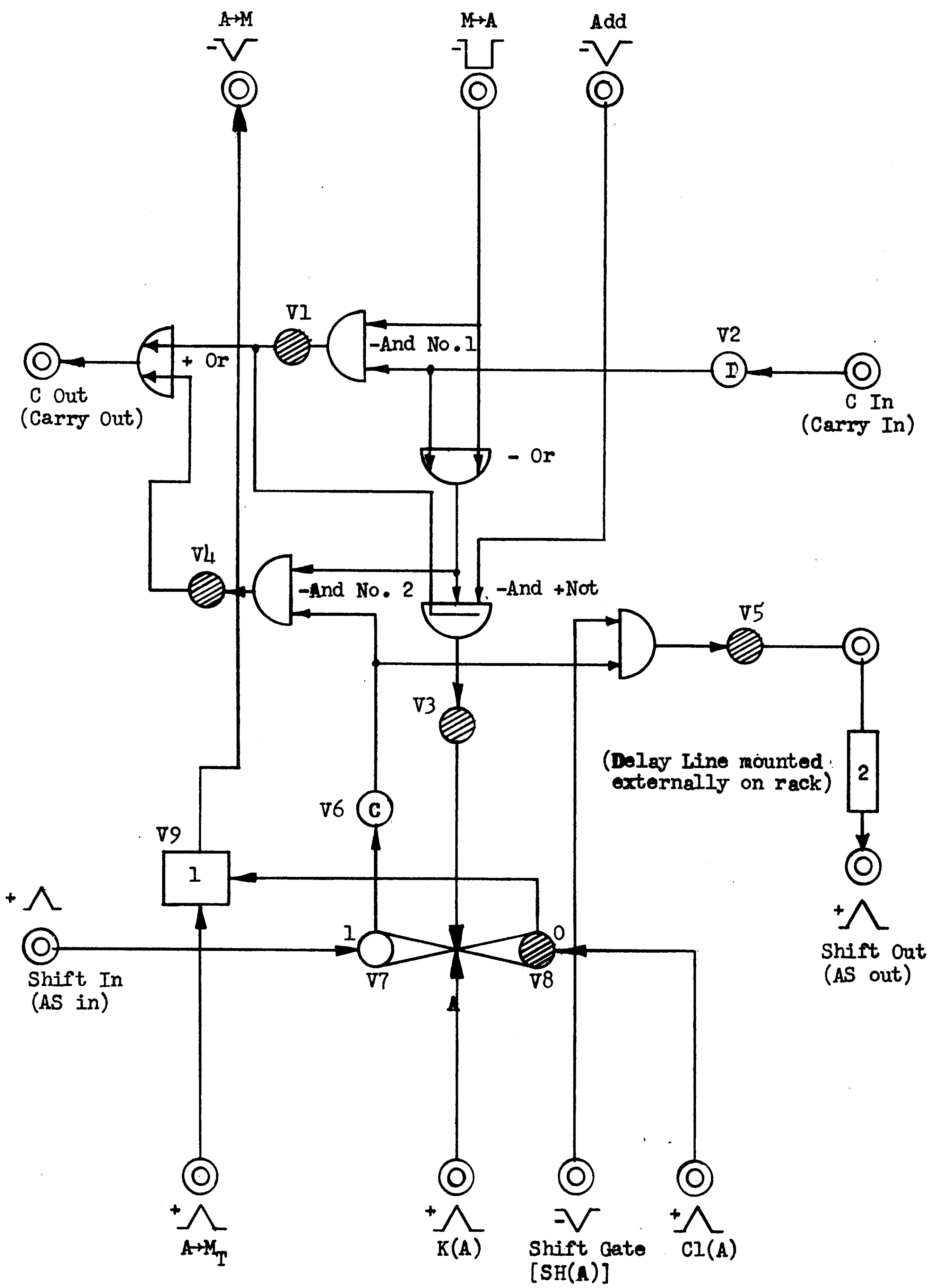




Lugs carry the outputs of the ADD, K(A), and K(M) drivers for testing purposes.

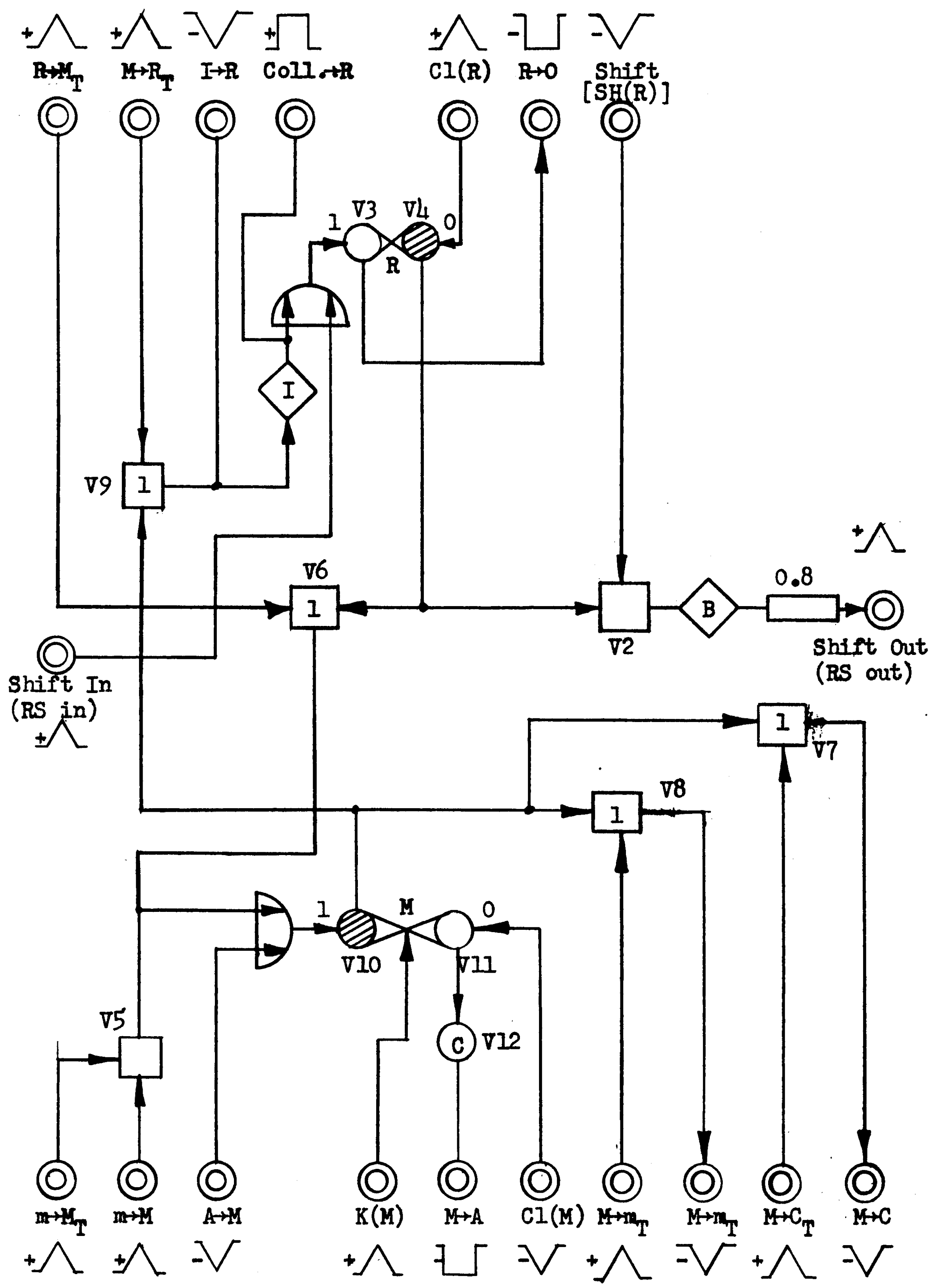
3.6 Arithmetic Test Unit.

A Register:



3.6 Arithmetic Test Unit.

M-R Register:



3.6 Arithmetic Test Unit.

II. Procedure for Testing "A" and "M" Chassis

Insert an M chassis in position 2 on the test unit and an A chassis directly below it.

When testing with one A chassis in position 2 special Cannon plugs need to be inserted in A chassis positions 1 and 3 as follows (see Drawing on page A3.6-11).

At Position $1A_2$*: a plug with a jumper between pin 2 and pin 10, to connect Carry-out of chassis in position 2 to terminating network and Carry-out lug on the control panel.

At Position $3A_2$: a plug with a jumper between pin 2 and pin 10, to connect Carry-input from the rack to the Carry-in on chassis in position 2.

At Position $1B_2$: a plug with a jumper between pin 2 and pin 5. Pin 2 is the "AS in" for that position, and derives an input from the rack. Pin 5 is a spare pin which has been wired directly to the "AS in" for position 2.

At Position $3B_2$: a plug with 1.2K between pin 1 (gnd) and pin 2. Pin 2 accepts an "AS in" from the chassis in position 2, so the resistor provides the proper termination for this signal.

CAUTION: Do not insert or remove chassis from the test unit with the D.C. voltages on.

* Explanation of notations such as "$1A_2$": The 1st number refers to the chassis digit position. The letter identifies the Cannon plug (eg., whether the "A" or "B" plug of a particular chassis). The subscript refers to the upper or lower rack; a "1" for the upper rack where M or C chassis are mounted, a "2" for the lower rack where "A" chassis are mounted. Thus, "$1A_2$" identifies the "A" Cannon plug of the lower chassis position 1. This happens to be the plug at the lower right of the rack. (The chassis positions are numbered from right to left, from most to least significant digit.)

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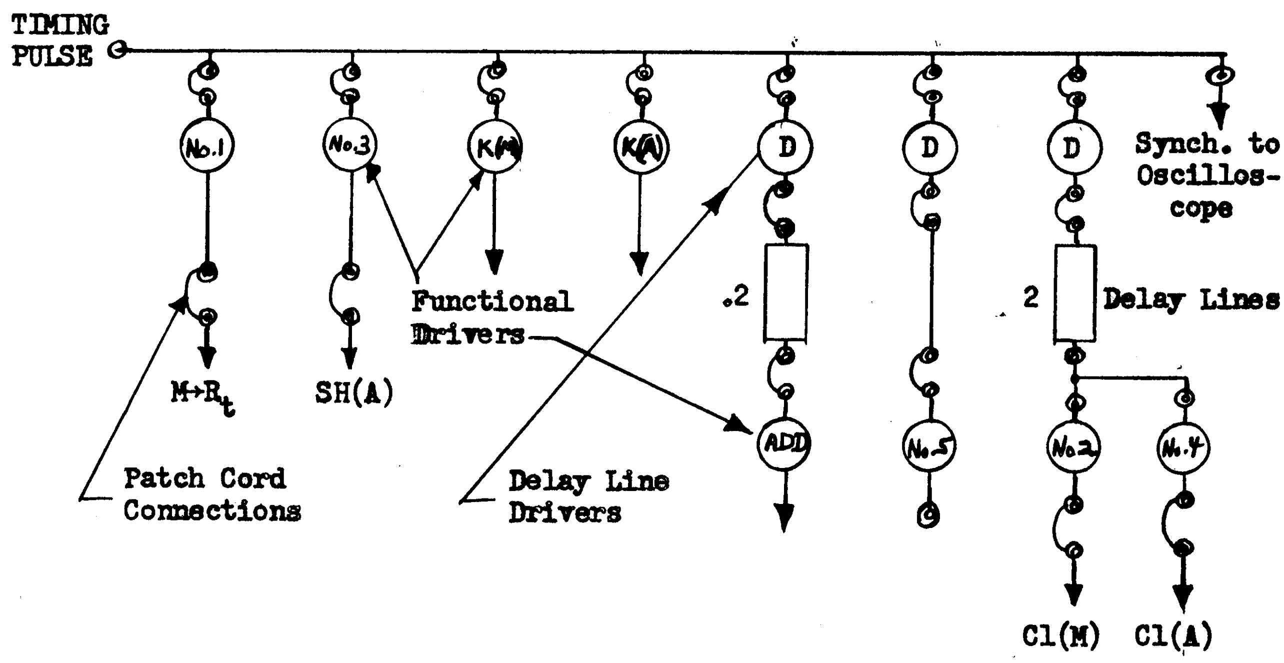
Interconnect the delay lines and drivers with patch cords as indicated below (a pictorial diagram is provided on page A3.6-12).



Other patch cord connections to the outputs of the functional drivers should be made only as needed. All functional driver amplitude controls should be turned down (counter-clockwise) except as needed, with the exception of the Stability Test Driver Amplitude Control which may be turned up at all times to allow convenient setting or clearing of the flipflops on the chassis to be tested.

In the suggested tests, notation of the following type is used: Pulses required Cl(A)-(4), "AS in"-(5). This means that the output of functional driver No. 4 should be patched into the Cl(A) jack and the output of functional driver No. 5 should be patched into the "AS in" jack on the patch panel. The pulse amplitude of the inputs may be measured at the functional input jacks on the control panel.

A. The "A" Chassis

1. A Register Flipflop.

a. Pulses required: "AS in"-(5) and Cl(A)-(4).

Under these conditions every 8μsec there will be an "AS in" pulse to set the flipflop to the "one" state, followed 2μsec later by a Cl(A) pulse which restores the flipflop to the "zero" state. The output of the flipflop can be observed at

3.6 Arithmetic Test Unit.

the cathode of V6 (cathode follower) as a negative 2μsec pulse of amplitude ≥ 25 volts.

Reduce the amplitude of the "AS in" pulse until the flipflop fails to trigger occasionally, marked by an intermittent trace across the base of the output pulse. Then slowly increase the amplitude until the trace just disappears, and measure the amplitude of the "AS in" pulse at that point. It should be between 10 and 15 volts. With the "AS in" back to maximum amplitude, repeat this sensitivity measurement for the "Cl(A)" input.

b. Pulses required: K(A) and Cl(A)-(4).

The behavior of the flipflop will be similar to that described in part a) above. (Though the K(A) pulse will change the state of the flipflop to the opposite state whether it stores a "zero" or a "one," in this case it always sets the flipflop to the "one" state because it is always preceded by a Cl(A).) Measure the sensitivity of the flipflop to the K(A) input in the same way that it was measured for the "AS in". The K(A) required for triggering should be between 10 and 15 volts.

2. The Adder.

a. Carry-Out.

1) -AND #2 Gate.

a) Pulses required: K(A) and Cl(A)-(4).

Put a "one" in the M flipflop. With the A flipflop thus being alternately set and cleared, a negative 2μsec pulse is presented to one input of -AND #2 gate. At the Carry-out lug on the control panel, observe a 2μsec positive pulse of at least 25 volts. Then set the M flipflop to "zero". The Carry-out pulse should be less than 5 volts.

b) Pulses required: K(M) and Cl(M)-(2).

Put a "one" in the A flipflop. At the Carry-out lug on the control panel, observe a 2μsec positive pulse of at least 25 volts. Then set the A flipflop to "zero". The Carry-out pulse should be less than 5 volts.

3.6 Arithmetic Test Unit.

c) Pulses required: "Carry-in"-(5) of 20V.
With a "zero" in M and a "one" in A, observe a Carry-out pulse of ½μsec and at least 20 volts.

2) -AND ≠1 Gate.

a) Pulse required: "Carry-in"-(5) of 20V.
Put a "one" in M and a "zero" in A. Observe a Carry-out pulse of ½μsec and at least 20 volts. With "zero" in M and Carry-in pulse turned up full, the Carry-out pulse should be less than 5 volts.

b. Addition.

1) -OR, -AND + NOT, -AND ≠1 Gates.

a) Pulses required: Add, Cl(A)-(4).
Put a "one" in M. Observe the output of the A flipflop at the cathode of V6. It should be a negative 2μsec pulse of at least 25 volts. Turn down the add pulse amplitude until the flipflop fails to trigger occasionally, as shown by a trace across the base of the output pulse. Then turn it back up until the trace just disappears, and measure the add pulse. It should be between 12 and 18 volts (0.1μsec negative pulse).

b) Pulses required: Add, Cl(A)-(4), "Carry-In"-(5).
With a "zero" in M observe the A flipflop output at the cathode of V6. It should be a negative 2μsec pulse of at least 25 volts. Repeat the measurement of sensitivity to add pulse which was made in procedure (a). The add pulse under these conditions should measure between 12 and 20 volts.

c) Pulses required: Add, Cl(A)-(4), "Carry-in"-(5).
Put a "one" in M. With the add pulse at maximum amplitude, the A flipflop should not trigger. Reduce the Carry-in to the magnitude at which the flipflop triggers occasionally (negative 2μsec pulse appearing intermittently at cathode of V6), then increase it until it

3.6 Arithmetic Test Unit.

barely inhibits addition all the time. The Carry-in to inhibit should be between 8 and 15 volts.

3. Shift A: -AND ≠3 Gate.

a. Pulses required: Sh(A)-(3) of 10V.

With a "one" in A observe the output at the "AS out" lug on the control panel. It should be a positive ½μsec pulse of at least 20 volts. With the Sh(A) output turned to maximum amplitude and a "zero" in A, the "AS out" pulse should be less than 5 volts.

b. Pulses required: "AS in"-(5), Cl(A)-(4).

With the flipflop running, a negative 2μsec pulse is presented to one input of the shift gate. The pulse appearing at the "AS out" lug should be less than 5 volts.

4. A → M: V9.

a. Pulse required: $A \rightarrow M_T$ -(5).

With a "one" in A observe the output at the A→M lug on the control panel. It should be a negative ½μsec pulse of magnitude greater than 30 volts. With a "zero" in A, this pulse should be less than 3 volts.

Resumé of Test Procedure for "A" Chassis

	INPUTS	OBSERVATION
1.a.	"AS in"-(5) Cl(A)-(4)	FF operation at K^6. (negative 2μs pulse ≥ 25 volts). Measure the minimum "AS in" required to trigger the FF reliably. It should be 10 to 15V. Repeat for Cl(A).
b.	K(A) Cl(A)-(4)	Same as a) above. Measure the minimum K(A) which will trigger FF. It should be 10 to 15 volts.
2.a. 1)a)	K(A) Cl(A)-(4)	With "one" in M: Carry-out = 2μs positive pulse ≥ 25V. With "zero" in M: Carry-out <5 volts.
1)b)	K(M) Cl(M)-(2)	With "one" in A: Carry-out = 2μs positive pulse ≥ 25V. With "zero" in A: Carry-out < 5 volts.
1)c)	Carry-in(5) of 20 volts	With "zero" in M and "one" in A: Carry-out = ½μs positive pulse ≥ 20 volts.
2)a)	Carry-in(5) of 20 volts	With "one" in M and "zero" in A: Carry-out = ½μs positive pulse ≥ 20 volts. With "zero" in M and Carry-in full: Carry-out < 5 volts.

3.6 Arithmetic Test Unit.

Resumé of Test Procedure for "A" Chassis (continued)

	INPUTS	OBSERVATION
2.b. 1)a)	Add Cl(A)-(4)	With "one" in M: FF operation at K^6. (negative 2µs pulse ≥ 25 volts). Measure the minimum "add" pulse which will trigger the FF reliably. It should be 12 to 18 volts.
1)b)	Add Cl(A)-(4) Carry-in(5)	With "zero" in M: FF operation at K^6. (negative 2µs pulse ≥ 25 volts). Measure the minimum "add" pulse which will trigger the FF reliably. It should be 12 to 20 volts.
1)c)	Add full Cl(A)-(4) Carry-in(5)	With "one" in M: FF should not trigger. Measure the minimum Carry-in required to inhibit. It should be between 8 and 15 volts.
3.a.	Sh(A)-(3) of 10 volts	With "one" in A: "AS out" = positive $\frac{1}{2}$ µs pulse ≥ 20V. With Sh(A) full and "zero" in A: "AS out" < 5 volts.
b.	"AS in"-(5) Cl(A)-(4)	"AS out" < 5 volts.
4.a.	$A \rightarrow M_T$ -(5)	With "one" in A: $A \rightarrow M$ = negative $\frac{1}{2}$ µs pulse ≥ 30V. With "zero" in A: $A \rightarrow M$ <3 volts.

Typical Failures, A Chassis

Any 6AG7:	low I_p, G-K short, poor cutoff, open filament, broken base or internal connection.
V1, V2, V3(6AG7):	G-K short.
V2(6AG7):	short, blows -165V fuse, tube left with no I_p.
V9(6AS6):	low I_p, short, broken pin.
Any diode:	low back resistance or drift, short, open, polarity accidentally reversed on replacement.
Critical diodes 31D, 37D, 31B, 32B, 30B, 34E, 35E, 32E, 33B:	low back resistance or drift.
Diode 30D (27E on some chassis)(IN56):	shorted, sometimes 34E shorted also.
Diode 37E(1N38):	open.
Diode 35B:	open, 35D shorted.
Diode 34E:	open.
Diode 27B:	shorted, 26B open.
Diode 42B:	shorted.
Any resistor:	overheated, changed in value, broken.
Flipflop precision resistors:	open, dropped in value.
Wiring:	shorted leads or components, especially in FF, poor solder joints, broken leads (especially running from tagboard to chassis).
Tube socket:	poor pin connection (especially miniature socket at V9 position).

3.6 Arithmetic Test Unit.

B. The "M" Chassis

1. R Register Flipflop.

a. Pulses requires: "RS in"-(1), Cl(R)-(4).

Under these conditions, every 8 μsec there will be an "RS in" pulse to set the flipflop to the "one" state, followed 2μs later by a Cl(R) pulse which restores the flipflop to the "zero" state. The output of the flipflop can be observed at G_3 of V2 (7AK7). It should be a positive 2μs pulse of at least 30 volts. Reduce the amplitude of the "RS in" pulse until the flipflop fails to trigger occasionally, marked by an intermittent trace across the base of the output pulse. Then slowly increase the amplitude until the trace just disappears, and measure the amplitude of the "RS in" pulse. It should be between 10 and 15 volts. With the "RS in" back to maximum amplitude, repeat this sensitivity measurement for the Cl(R) pulse.

2. Shift (R).

a. Pulses required: Sh(R)-(4).

Put a "one" in R. Observe the pulse at the "RS out" lug on the control panel. It should be a positive ½ μs pulse of at least 25 volts. Put a "zero" in R. The "RS out" pulse should be less than 3 volts.

3. M Register Flipflop and M → A.

a. Pulses required: K(M) and Cl(M)-(2).

Under these conditions, every 8μs there will be a K(M) pulse which sets the flipflop to the "one" state, followed 2μs later by a Cl(M) pulse which returns the flipflop to the "zero" state. (Though the K(M) pulse will change the state of the flipflop to the opposite state whether it stores a "zero" or a "one", in this case it always sets the flipflop to the "one" state because it is always preceded by a Cl(M).) The output of the flipflop can be observed at the M → A lug on the control

3.6 Arithmetic Test Unit.

panel. It should be a negative 2μs pulse of amplitude ≥ 30 volts. Next, reduce the amplitude of the K(M) pulse until the flipflop fails to trigger occasionally, marked by an intermittent trace across the base of the output pulse. Slowly increase the amplitude until the trace just disappears, and measure the amplitude of the K(M) pulse at that point. It should be between 10 and 15 volts. With the K(M) back to maximum amplitude, repeat this sensitivity measurement for the Cl(M) input.

4. M → C.

a. Pulses required: M → C_T-(5).

Put a "one" in M. Observe the output at the M → C lug on the control panel. It should be a negative ½ μs pulse of amplitude ≥ 40 volts. With a "zero" in M, this pulse should be less than 3V.

5. M → m.

a. Pulses required: M → m_T-(5).

Put a "one" in M. Observe the output at the M → m lug on the control panel. It should be a negative ½ μs pulse of amplitude ≥ 40 volts. With a "zero" in M, this pulse should be less than 3V.

6. R → M.

a. Pulses required: R → M_T-(5), Cl(M)-(2).

Put a "one" in R. Under these conditions, every 8 μs there is an R → M pulse which sets the M flipflop to the "one" state, followed 2 μs later by a Cl(M) which returns the flipflop to the "zero" state. The output of the M flipflop can be observed at the M → A lug on the control panel. It should be a negative 2μs pulse of amplitude ≥ 30 volts. Decrease the amplitude of the R → M_T pulse until the flipflop fails to trigger occasionally, marked by an intermittent trace across the base of the output pulse. Next, increase the amplitude of the R → M_T pulse until the trace just disappears and measure the amplitude of the R → M_T pulse at that point. It should be between 10 and 17 volts. With the amplitude of the R → M_T pulse back to maximum and a "zero" in R, the pulse

3.6 Arithmetic Test Unit.

appearing at the input (negative) end of crystal 3C should be ≤ 3 volts. (This point is the transfer input to the M flipflop, and derives a pulse from the R → M gate.)

7. M → R.

a. Pulses required: M → R_T-(1), Cl(R)-(4).
Put a "one" in M. Under these conditions, every 8 μs there is an M → R pulse which sets the R flipflop to the "one" state, followed 2μs later by a Cl(R) which restores the R flipflop to the "zero" state. The output of the R flipflop can be observed at G_3 of V2 (7AK7). It should be a positive 2μs pulse of amplitude ≥ 30 volts. Decrease the amplitude of the M → R_T pulse until the flipflop fails to trigger occasionally, marked by an intermittent trace across the base of the output pulse. Next, increase the amplitude until the trace just disappears, and measure the amplitude of the M → R_T pulse at that point. It should be between 12 and 19 volts.

b. Pulses required: M → R_T, Cl(R)-(4).
With the M → R_T pulse back to maximum amplitude and a "zero" in M, the pulse appearing at the input (positive) end of crystal 37B should be less than 3 volts.

Resumé of Test Procedure for "M" Chassis

	INPUTS	OBSERVATION
1.a.	"RS in"-(1) Cl(R)-(4)	R-FF operation at G_3^2 (7AK7)(positive 2μs pulse ≥ 30V). Measure the minimum "RS in" required to trigger the FF reliably. It should be 10 to 15V. Repeat for Cl(R).
2.a.	Sh(R)-(4)	With "one" in R: "RS out" = ½ μs positive pulse ≥ 25V. With "zero" in R: "RS out" < 3 volts.
3.a.	K(M) Cl(M)-(2)	M-FF operation at M → A lug (negative 2μs pulse ≥ 30V). Measure the minimum K(M) required to trigger the FF reliably. It should be 10 to 15V. Repeat for Cl(M).
4.a.	M→C_T-(5)	With "one" in M: M → C = negative ½ μs pulse ≥ 40V. With "zero" in M: M → C < 3 volts.
5.a.	M→m_T-(5)	With "one" in M: M → m = negative ½ μs pulse ≥ 40V. With "zero" in M: M → m < 3 volts.
6.a.	R→M_T-(5) Cl(M)-(2)	With "one" in R: M-FF operation at M→A lug. (negative 2μs pulse ≥ 30V). Measure the minimum R→M_T required to trigger the FF reliably. It should be 10 to 17V.

3.6 Arithmetic Test Unit.

Resumé of Test Procedure for "M" Chassis (continued)

	INPUTS	OBSERVATION
6.b.	$R \to M_T$ full Cl(M)-(2)	With "zero" in R: pulse at negative end of Xtal 3C should be ≤ 3 volts.
7.a.	$M \to R_T$-(1) Cl(R)-(4)	With "one" in M: R-FF operation at G_3^2. Measure the minimum $M \to R_T$ required to trigger FF reliably. It should be 12 to 19 volts.
b.	$M \to R_T$ full Cl(R)-(4)	With "zero" in M: pulse at positive end of Xtal 37B should be < 3 volts.

Typical Failures, M Chassis

Any 6AG7:	low I_p, G-K short, poor cutoff, open filament, broken base or internal connection.
Any 6AS6:	low I_p, shorts, broken pin.
Any diode:	low back resistance or drift, short, open, polarity accidentally reversed on replacement.
Any resistor:	overheated, changed in value, broken.
Flipflop precision resistors:	open, dropped in value.
Wiring:	shorted leads or components, especially in FF, poor solder joints, broken leads (especially running from tagboard to chassis).
6AS6 sockets:	poor pin connections.
Transformer 46C:	primary to secondary short (blows +165V fuse, usually burns 220Ω resistor at 46E).
Delay line:	shorted, open.

3.6 Arithmetic Test Unit.

C. C Register Test Procedure.

Plug the C Register chassis into position "C" on the Arithmetic Test Rack. The Cannon plugs A and B are wired to the set of jacks labelled "position C", and the individual jacks are labelled according to which Cannon plug pin they are connected . These jacks can then be connected via banana plugs to the outputs of any of the functional drivers.

The inputs and outputs to the C Register are as follows:

Pin	Plug A	Plug B
1	$\beta \rightarrow$ Transfer Reg.(out)	Gnd.
2	Cl(ε)(in) ᐯ	Cl(S)(in) ᐯ
3	$\delta \rightarrow$ P (out) ᐯ	D $\rightarrow$ S (in) ᐯ
4	$\delta \rightarrow$ O (out) ᐯ	$\gamma \rightarrow$ Channel Reg.(out) ⎍
5	ε Carry-in ᐱ	M $\rightarrow$ C (δ)(in) ᐯ
6	S to Adder (out) ⎍	M $\rightarrow$ C (γ)(in) ᐯ
7	$\delta \rightarrow \varepsilon_T$(in) ᐱ	Cl(C)(in) ᐯ
8	$\delta \rightarrow S_T$(in) ᐱ	M $\rightarrow$ C(β)(in) ᐯ
9	ε Carry-out ᐱ	$\gamma \rightarrow S_T$(in) ᐱ
10	$\varepsilon \rightarrow S_T$(in) ᐱ	$\beta \rightarrow S_T$(in) ᐱ
11	$\delta \rightarrow P_T$(in) ᐱ	$\alpha \rightarrow S_T$(in) ᐱ
12	$\delta \rightarrow O_T$(in) ᐱ	M $\rightarrow$ C(α)(in) ᐯ

In the following list of procedures, under each procedure are given the inputs required, with pin connection and driver to be used, and the outputs to be observed under the stated conditions. For example, in the first procedure the following information is given:

1. a.	D $\rightarrow$ S	B3	Driver ≠ 3
	Cl(S)	B2	Driver ≠ 2

This means that the output of driver ≠ 3 on the test rack should be patched into Cannon pin B3 at position C to produce a D $\rightarrow$ S input to the C Register, and that the output of driver ≠ 2 should be patched into Cannon pin B2 at position C to produce a Cl(S) input to the C Register.

3.6 Arithmetic Test Unit.

1. S Register, S → L, Output to Adder.

   a. D → S B3 Driver # 3
      Cl(S) B2 Driver # 2

      Observe a positive 2μs pulse at the S → L jack of at least 40 volts, and a positive 2μs pulse at A6 (output to adder) of at least 35 volts. The flipflop should continue to operate when the D → S input amplitude is reduced to 25 volts or less.

   b. Reverse the outputs of drivers #2 and #3, to give the following connections:

      D → S B3 Driver # 2
      Cl(S) B2 Driver # 3

      Under these conditions, the flipflop should continue to operate when the Cl(S) input amplitude is reduced to 25 volts or less.

2. ε Register, ε Carry-out, ε → S

   Using clip leads, connect the Carry-out through a .01 mfd. capacitor to the cathode of the S Register flipflop.

   a. ε Carry-in A5 Driver # 1

      Observe a voltage level which is up for 8μs and down for 8μs at G_3^1, with a swing of at least 40 volts. The ε flipflop should continue to trigger when the amplitude of the Carry-in pulse is reduced to 15 volts or less. It should not trigger on less than 8 volts.

   b. Cl(ε) A2 Driver # 3
      ε Carry-in A5 Driver # 4

      At G_1^3, observe a roughly triangular waveform of at least 30 volts swing, which drops in about 2μs and rises in about 6μs, indicating that the flipflop is being triggered by both pulses. The flipflop should continue to operate when the Cl(ε) pulse amplitude is reduced to 15 volts or less. It should not trigger on less than 8 volts.

   c. ε Carry-in A5 Driver # 1

      Observe the output of the S Register at S → L jack. It should be roughly a square wave up for 16μs and down for 16μs, with a swing

3.6 Arithmetic Test Unit.

of at least 45 volts. The S Register should continue to operate when the $\mathcal{E}$ Carry-in amplitude is reduced to 22 volts or less.

d. $\mathcal{E} \rightarrow S_T$ A10 Driver # 1
Cl(S) B2 Driver # 2

With a "one" in $\mathcal{E}$, observe S flipflop operation at S → L jack. The flipflop should continue to operate when $\mathcal{E} \rightarrow S_T$ is reduced to 25 volts or less. With a "zero" in $\mathcal{E}$, and $\mathcal{E} \rightarrow S_T$ at maximum amplitude, the pulse at the input crystal to the S Register (on G_2^5) should not exceed 3 volts.

3. α Register and $\alpha \rightarrow S$

a. M → C (α) B12 Driver # 3
Cl(C) B7 Driver # 2

Observe a positive 2µs pulse at G_3^{15}, of at least 30 volts. The flipflop should continue to operate when the M → C(α) pulse amplitude is reduced to 12 volts or less. It should not trigger on less than 5 volts (8 to 10 volts is normal).

b. Reverse the outputs of drivers #3 and #2, to give the following connections:

Cl(C) B7 Driver # 3
M → C (α) B12 Driver # 2

The flipflop should continue to operate when the Cl(C) pulse amplitude is reduced to 12 volts or less. It should not trigger on less than 5 volts.

c. $\alpha \rightarrow S_T$ B11 Driver # 1
Cl(S) B2 Driver # 2

With a "one" in α, observe S flipflop operation at S → L jack. Flipflop should continue to operate when $\alpha \rightarrow S_T$ pulse amplitude is reduced to 25 volts or less. With a "zero" in α and the $\alpha \rightarrow S_T$ pulse amplitude maximum, the pulse at the input crystal to the S Register (on G_2^5) should not exceed 3 volts.

4. β Register and $\beta \rightarrow S$

a. M → C (β) B8 Driver # 3
Cl(C) B7 Driver # 2

Observe a positive 2µs pulse at A1 of at least 30 volts. The flip-

3.6 Arithmetic Test Unit.

flop should continue to operate when the M → C (β) pulse amplitude is reduced to 12 volts or less. It should not trigger on less than 5 volts.

b. Reverse the outputs of drivers #2 and #3, to give the following connections:

Cl(C)	B7	Driver # 3
M → C (β)	B8	Driver # 2

The flipflop should continue to operate when the Cl(C) pulse amplitude is reduced to 12 volts or less. It should not trigger on less than 5 volts.

c.

$\beta \rightarrow S_T$	B10	Driver # 1
Cl(S)	B2	Driver # 2

With a "one" in β, observe S flipflop operation at the S → L jack. Flipflop should continue to operate when the $\beta \rightarrow S_T$ pulse amplitude is reduced to 25 volts or less. With a "zero" in β, the pulse at the input crystal to the S Register (on G_2^5) should not exceed 3 volts.

5. γ Register and $\gamma \rightarrow S$

a.

M → C (γ)	B6	Driver # 3
Cl(C)	B7	Driver # 2

Observe a positive 2µs pulse at B4 of at least 30 volts. The flipflop should continue to operate when the M → C(γ) pulse amplitude is reduced to 12 volts or less. It should not trigger on less than 5 volts.

b. Reverse the outputs of drivers #2 and #3, to give the following connections:

Cl(C)	B7	Driver # 3
M → C (γ)	B6	Driver # 2

The flipflop should continue to operate when the Cl(C) pulse amplitude is reduced to 12 volts or less. It should not trigger on less than 5 volts.

c.

$\gamma \rightarrow S_T$	B9	Driver # 1
Cl(S)	B2	Driver # 2

With a "one" in γ, observe S flipflop operation at the S → L jack.

3.6 Arithmetic Test Unit.

Flipflop should continue to operate when the $\gamma \to S_T$ pulse amplitude is reduced to 25 volts or less. With a "zero" in γ, the pulse at the input crystal to the S Register (on G_2^5) should not exceed 3 volts.

6. δ Register, $\delta \to S$, $\delta \to O$, $\delta \to P$, $\delta \to \mathcal{E}$

a. M → C (δ) B5 Driver ≠ 3
Cl(C) B7 Driver ≠ 2

Observe a positive 2μs pulse at G_3^9 of at least 30 volts. The flipflop should continue to operate when the M → C (δ) pulse amplitude is reduced to 12 volts or less. It should not trigger on less than 5 volts.

b. Reverse the outputs of drivers ≠2 and ≠3, to give the following connections:

Cl(C) B7 Driver ≠ 3
M → C (δ) B5 Driver ≠ 2

The flipflop should continue to operate when the Cl(C) pulse amplitude is reduced to 12 volts or less. It should not trigger on less than 5 volts.

c. $\delta \to S_T$ A8 Driver ≠ 1
Cl(S) B2 Driver ≠ 2

With a "one" in δ, observe S flipflop operation at the S → L jack. The flipflop should continue to operate when the $\delta \to S_T$ pulse amplitude is reduced to 25 volts or less. With a "zero" in δ, the pulse at the input crystal to the S Register (on G_2^5) should not exceed 3 volts.

d. $\delta \to O_T$ A12 Driver ≠ 1

Set the $\delta \to O_T$ pulse amplitude at 30 volts. With a "one" in δ, observe a negative ½ μs pulse at A4 ($\delta \to O$) of at least 75 volts. With a "zero" in δ, this pulse should be less than 3 volts.

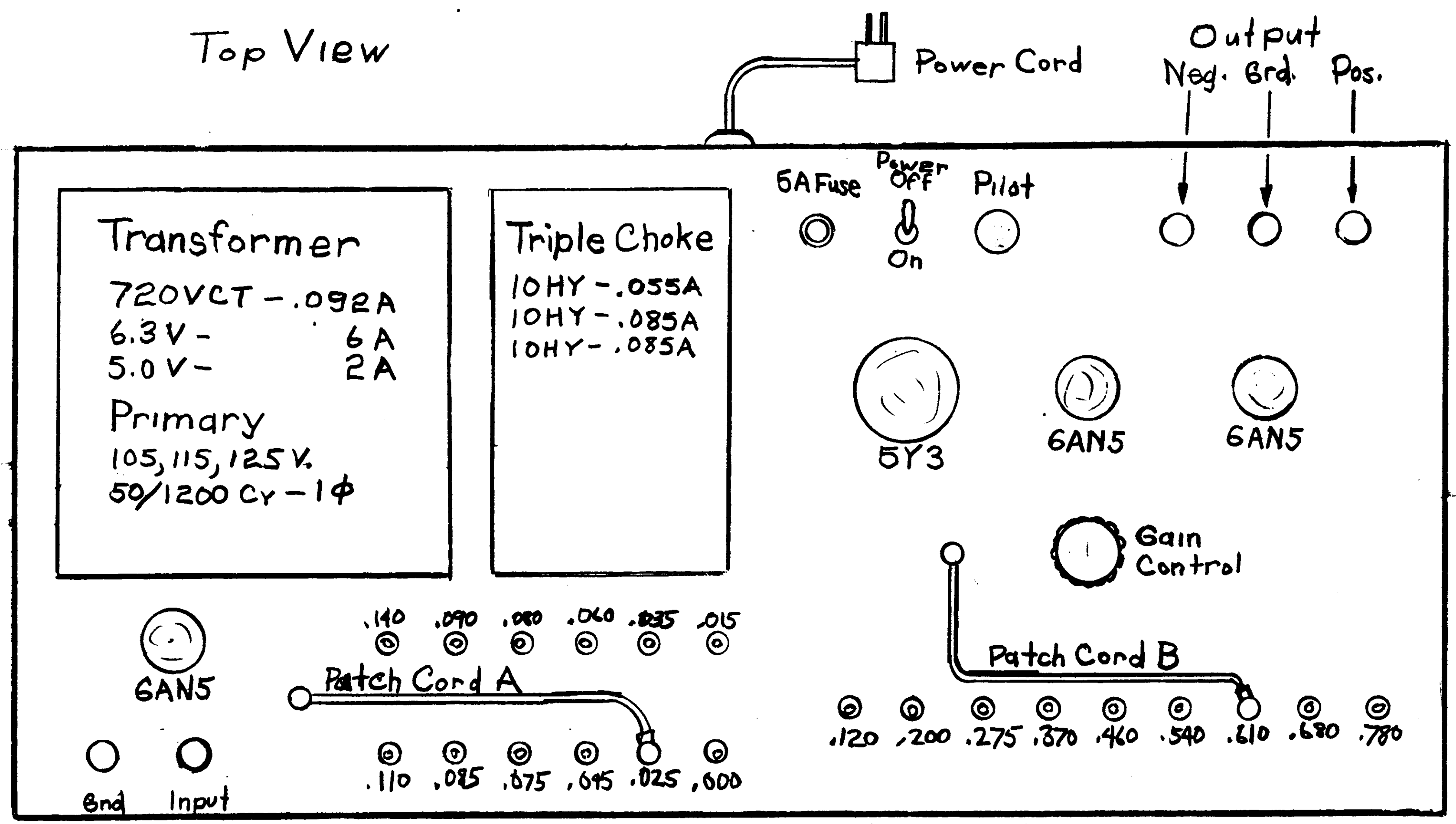
e. $\delta \to P_T$ A11 Driver ≠ 1

Set the $\delta \to P_T$ pulse amplitude at 30 volts. With a "one" in δ, observe a negative ½ μs pulse at A3 ($\delta \to P$) of at least 30 volts. With a "zero" in δ, this pulse should be less than 3 volts.

3.6 Arithmetic Test Unit.

f. $\mathcal{S} \rightarrow \mathcal{E}_T$ A7 Driver # 1
Cl($\mathcal{E}$) A2 Driver # 2

With a "one" in $\mathcal{S}$, observe $\mathcal{E}$ flipflop operation at G_3^1. The flip-flop should continue to operate when the $\mathcal{S} \rightarrow \mathcal{E}_T$ pulse amplitude is reduced to 25 volts. With a "zero" in $\mathcal{S}$, the pulse at the input crystal to the $\mathcal{E}$ Register (on G_2^3) should not exceed 3 volts.



Note: 1) Input Should Be Positive Pulse

2) Both cords must be used. Difference between Cords is Delay in Microseconds.

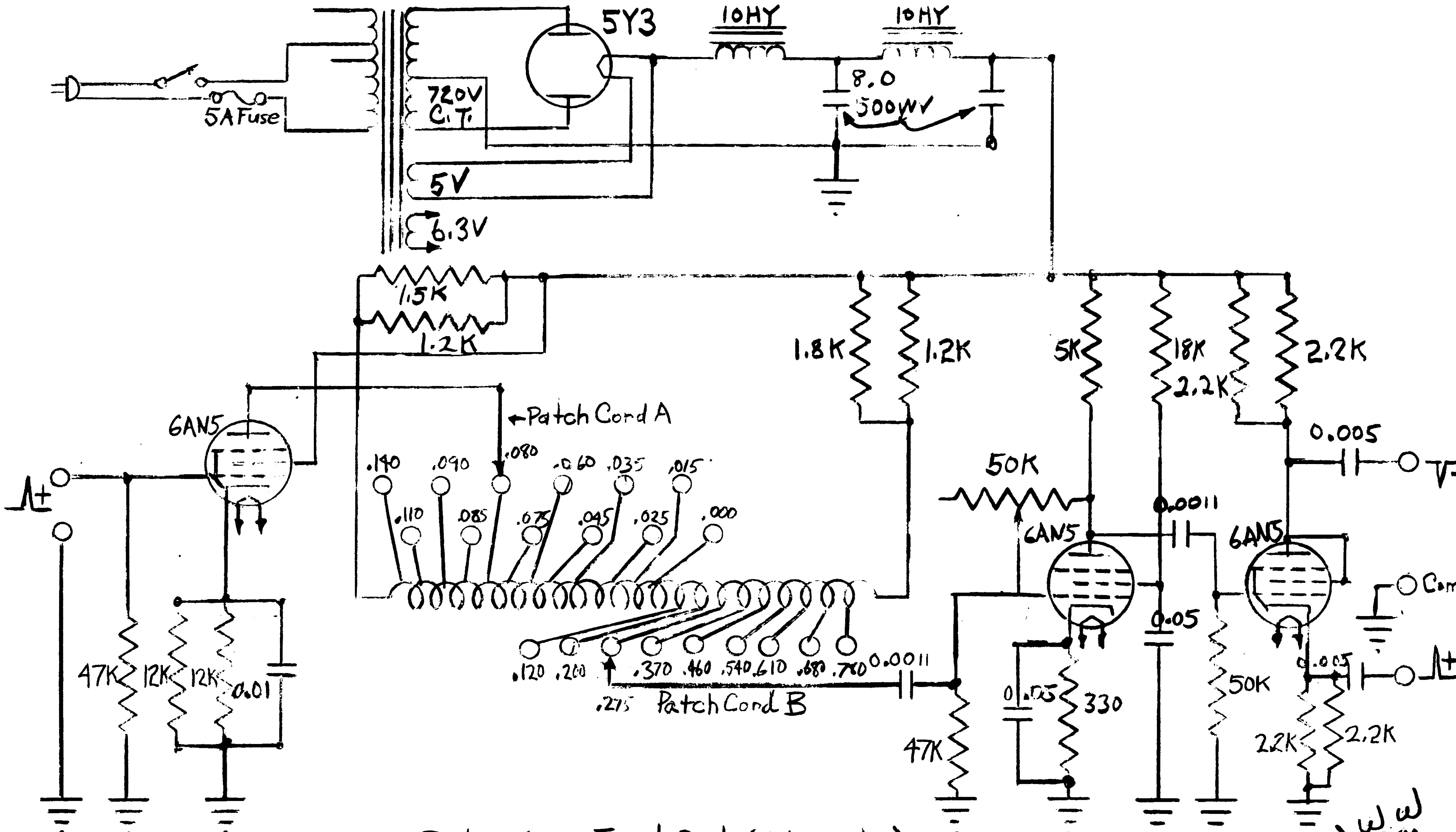
3) Output Impedance = 1000 ohms

J.W.W.

Delay Line Test Set

3.7 Delay Line Test Set

Schematic Drawing



Delay Line Test Set (Schematic)

JWW
EDM

3.8 Resistance Load Unit.

A. General Information:

The Resistance Load Unit has been developed to provide a means of loading power supplies and regulators for test. It provides a continuously variable resistance from 0 to 20,000 ohms. The maximum current and voltage are 1 ampere and 600 volts.

The load is composed of fixed resistors that may be cut in and out of the circuit except for the lowest range (0-350 ohms) which is continuously variable.

The load may be applied to, or removed from, the device being loaded by use of the LOAD-NO LOAD switch.

Current may be read on the built-in ammeter, and provision has also been made for use of an external ammeter. When an external ammeter is used, it is connected to the EXTERNAL AMMETER terminals and the AMMETER switch is set to EXTERNAL. Note that it is necessary to throw the AMMETER switch to INTERNAL to complete the circuit when not using an external ammeter.

Voltage may be read on an external voltmeter connected to the VOLTMETER terminals.

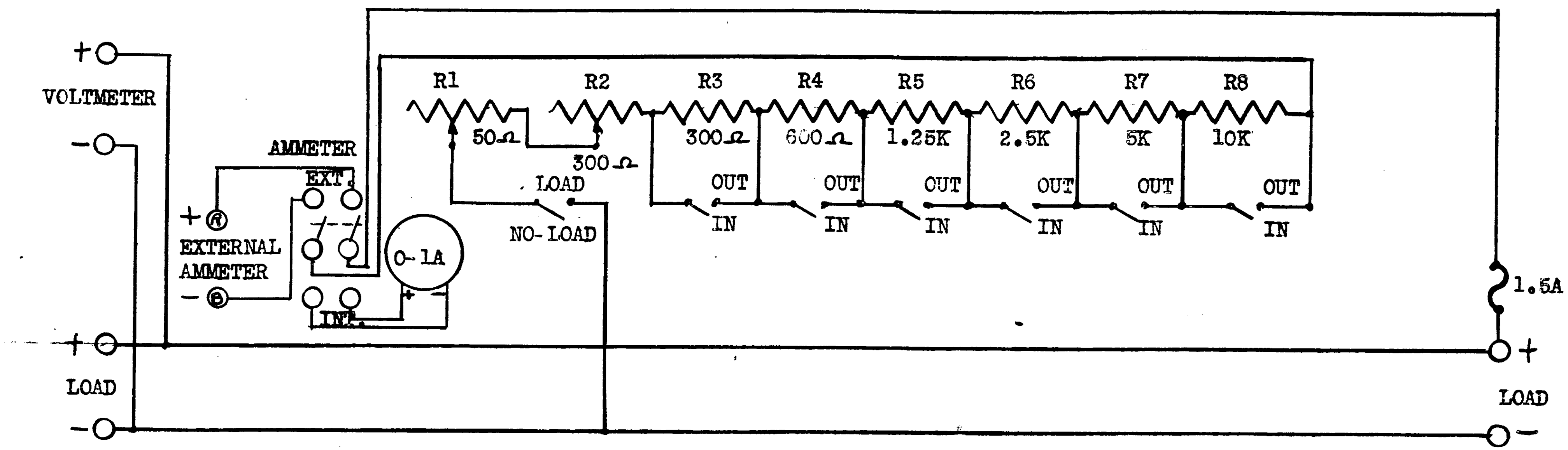
The two pairs of load terminals are provided for convenience and are wired in parallel.

The 1.5 ampere fuse will open the circuit upon excessive overloads.

A schematic drawing of the unit is shown on page A3.8-2.

3.8 Resistance Load Unit.

B. Schematic Drawing:



0 - 20,000 ohms
Max. Current = 1 amp.
Max. Voltage = 600V

EMR.

RESISTANCE LOAD UNIT

3.8 Resistance Load Unit.

C. Parts List:

R1 - 50 Ω, 50W rheostat

R2 - 300 Ω, 300W rheostat

R3 - 2-150 Ω, 160W, ww resistors in series

R4 - 4-150 Ω, 160W, ww resistors in series

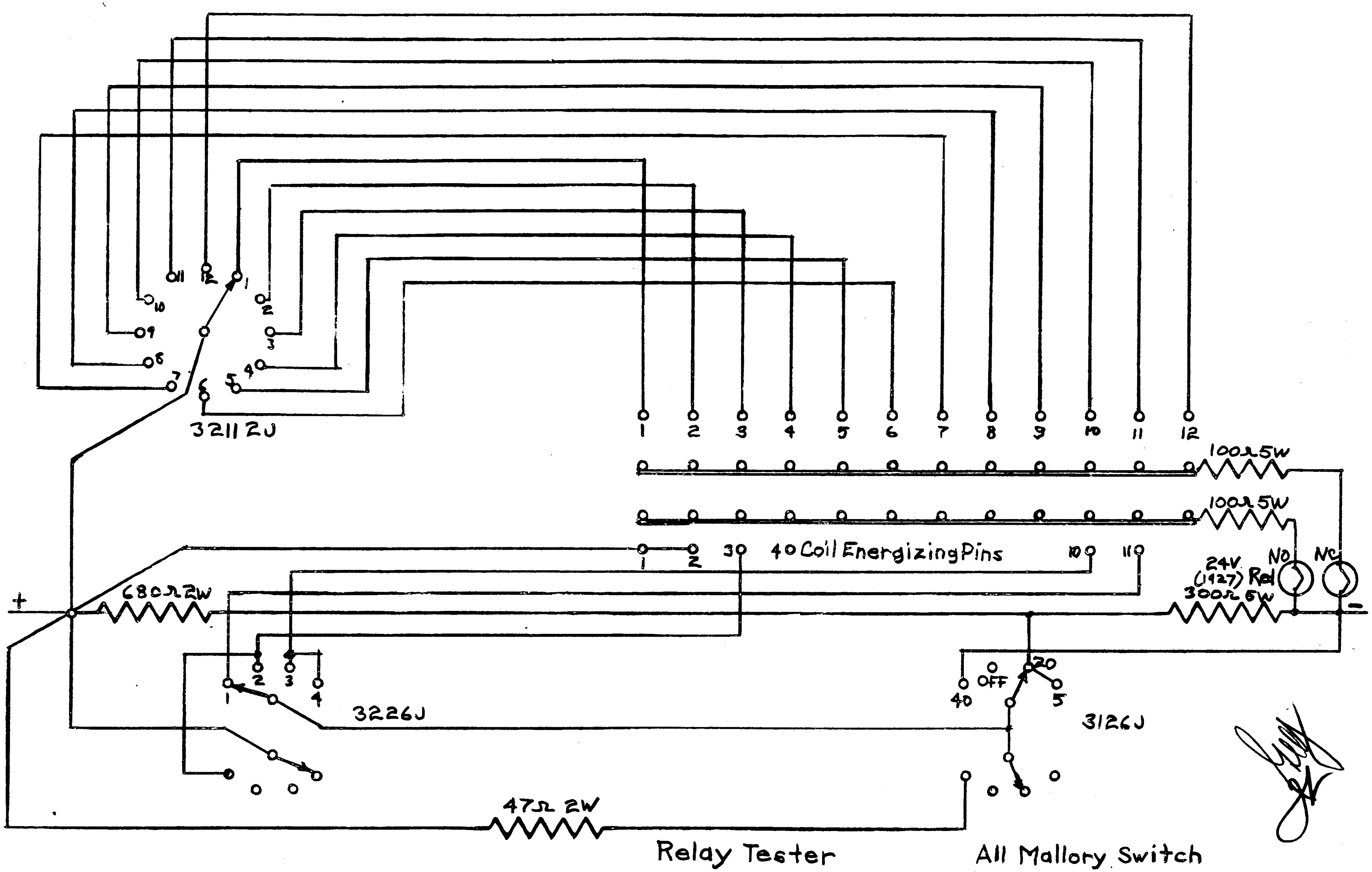
R5 - 2-2.5K, 160W, ww resistors in parallel

R6 - 2.5K, 160W, ww resistor

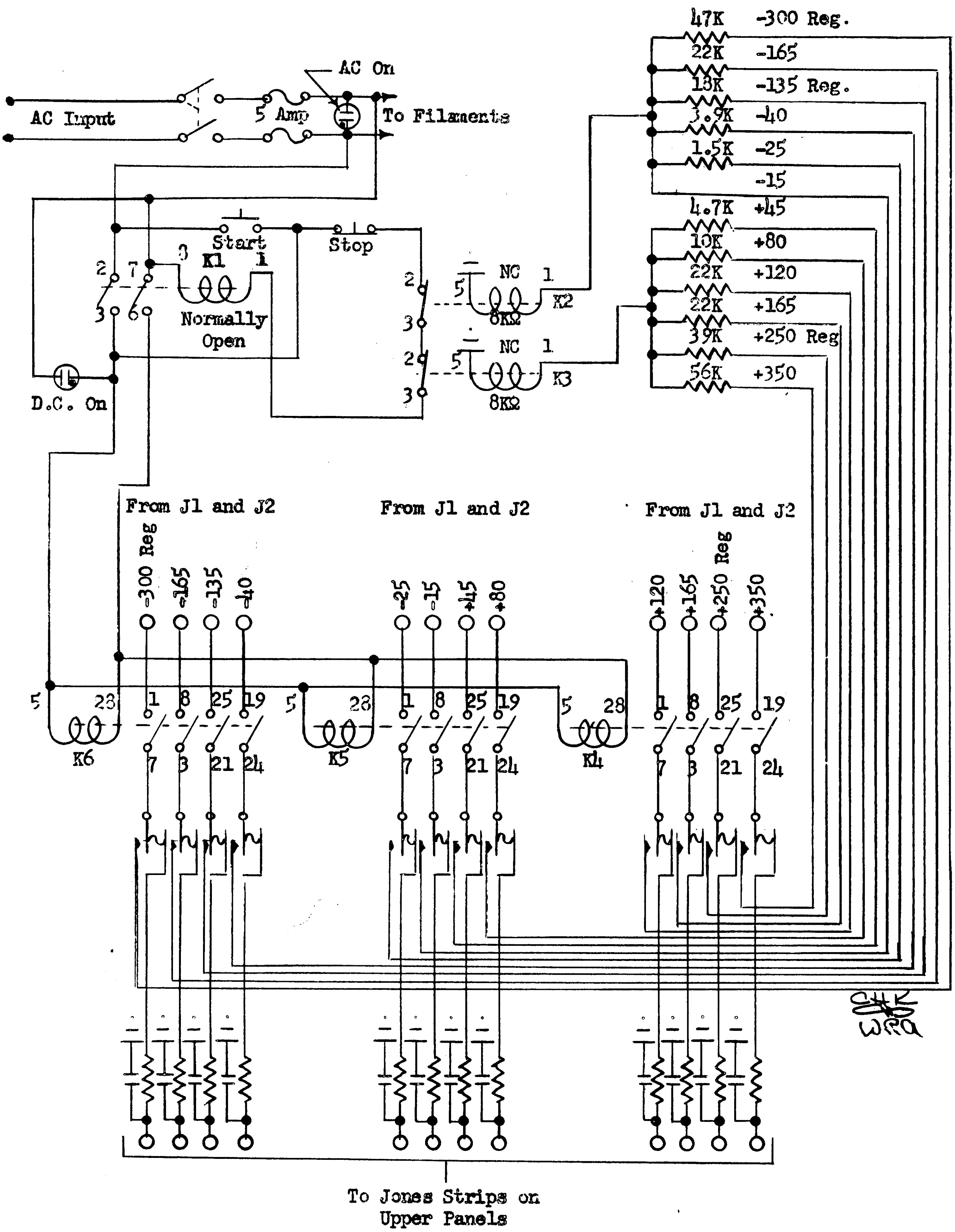
R7 - 2-2.5K, 160W, ww resistors in series

R8 - 10K, 100W, ww resistor

3.9 Relay Tester.



3.10 Protective System for Experimental Magnetic Drum.



J1 From Wall Plug

1	Grd	7	+165
2	+45	8	+120
3	+350	9	-165
4	-40	10	-15
5	-25	11	Not Used
6	Not Used	12	+80

J2 From Reg

1	-D Not Used	7	Grd -C
2	+D " "	8	+C +250 Reg
3	Not Used	9	-B -300 Reg
4	" "	10	Grd +B
5	" "	11	-A -135
6	" "	12	Grd +A

K1	Advance DPDT 115V AC
K2	Sigma 4A-2500
K3	Sigma 4A-2500
K4	Clare 6PDT 115V AC
K5	" " "
K6	" " . "

4.1 Standard Color Code.

+500 V to +650 V	Brown
+250 V to +350 V	Blue
+165 V to +200 V	Red
+120 V to +135 V	Orange
+110 V	Orange with tracer
+25 V	White with tracer
0 V	Black
-15 V to -25 V	Green
-165 V	Yellow
-200 V to -350 V	Yellow with tracer
All Heaters	Black
Ground	Black

4.2 Standard Connections on Jones Plugs.

A. For SWAC:

Pin	
1	0 V and Ground
2	Voltages above +165 V
3	Heaters at -165 V
4	Heaters at -165 V
5	Heaters at 0 V
6	Heaters at 0 V
7	+165 V
8	+120 V or +135 V
9	-165 V
10	-15 V
11	Indicator or Miscellaneous
12	Indicator or Miscellaneous

B. For Laboratory:

Pin	
1	0 V and Ground
2	+25 V
3	+350 V
4	-40 V
5	-25 V
6	+135 V
7	+165 V
8	+120 V
9	-165 V
10	-15 V
11	-180 V
12	+80 V

4.5 Standard Procedure Re Drawings.

A. General Procedure.

1. When drawings of new equipment or changes in existing drawings are desired, the sketches, drawings or corrected drawings should be made neatly, legibly and in an easy-to-understand form and presented to the draftsman.

2. Upon receipt of drafting work the draftsman will perform one of the following:

   a. If work is original, make tracing.

   b. If work is a correction, make correction on existing tracing.

   c. If changes are too numerous (and with the approval of the engineer in charge of maintenance), make new tracing.

3. Upon completion of tracing the draftsman will obtain one print of same, and submit it and the original working drawing to the initiating engineer for approval.

4. The engineer concerned will perform the following:

   a. Check print for correctness of work, including the drawing title and number.

   b. If there are corrections, mark in colored pencil and return print to draftsman.

   c. When drawing is satisfactory, initial print and tracing and return to draftsman.

5. The draftsman will send out the approved tracing for four copies which will be distributed as follows:

   a. Laboratory drawing board.

   b. File copy (located in SWAC Room).

   c. Engineers' office file.

   d. H. D. Huskey

   Any extra copies should be placed in the Engineers' office file.

B. Drawing Changes.

When engineers make changes on chassis or equipment these changes should appear on the drawings on the laboratory drawing boards or, for drawings not on these boards, on the file copy. When changes are

4.5 Standard Procedure Re Drawings.

made on the file copy or on board copies the engineer making the change must record this information in the engineering log. It is the responsibility of the draftsman to read the engineering log and make all changes on the tracings, and where needed obtain new prints.

It is the final responsibility of the person in charge of maintenance to see that drawings are kept up-to-date.

C. Drawing Notation.

1. The drawing title will be coded and will consist of two groups of letters and two groups of numbers with the following meaning:
   a. The first letter will designate location of the chassis or equipment, such as Arithmetic, Control, etc.
   b. The second letter, or group of letters, will designate the type of drawing, such as Block Diagram, Schematic, etc.
   c. The first number will give:
      1) For SWAC drawings the position of the chassis in the particular location designated in a).
      2) For all other drawings the drawing serial number, numbered in order of issue.
   d. The second number will designate the edition number of the drawing.
2. Code for chassis or equipment location, to be designated in first letter of drawing title [cf. 1a) above]:

A	Arithmetic	M	Memory
C	Control	O	Operating Console
D	Magnetic Drum	P	Power Unit
G	General	R	Charts and Rack Wiring
L	Laboratory Equipment	X	Auxiliary Equipment

3. Code for drawing type, to be designated in second letter, or group of letters, of drawing title [cf. 1b) above]:

B	Block Diagram	T	Tagboard Drawing
M	Mechanical Drawing	W	Wiring Diagram
S	Schematic Drawing		

4.5 Standard Procedure Re Drawings.

Note: Some drawings may consist of more than one of the above types. Their code will contain all of the letters for such types, but the drawing will be filed according to the first type designation only.

4. In addition to the drawing title described in 1, 2, and 3 above, descriptive titles will be given to drawings which will describe to some extent the function of the particular chassis or equipment.

4.7 Method of Molding Pulse Transformers, Delay Line Terminals, etc. with Liquid Plastic.

Molding is used to provide mechanical protection and to minimize humidity effects. It is considered feasible to mold almost any small piece of equipment. At the Institute for Numerical Analysis it has been found desirable to mold peaking coils, pulse transformers and delay line terminals.

The molds may be either wood or metal. Allowance for draft should be made to insure ease in removal of castings. If wooden molds are used, the mold cavity should be coated with a thin layer of beeswax to eliminate sticking.

The liquid plastic used is Claro-Cast Casting Plastic (Fry Plastics Company, Los Angeles 44, California) or equivalent; the liquid hardener is Claro-Cast Hardener for use with Claro-Cast Casting Plastic, or equivalent.

Three drops of hardener are added to two teaspoons of casting plastic, mixed well, and poured immediately. This one mixture is used for all castings. The castings are made at normal ambient temperature, pressure and humidity, with no special precautions taken to control these factors. The hardening process will take place at room temperature but is greatly accelerated by elevated temperatures.

When a wooden mold is used the liquid plastic is poured and allowed to stand for two to three hours before it is removed from the mold. The casting, which can at this stage be handled lightly without damage, is then baked for four hours at 120° F. When a metal mold is used the liquid plastic is poured and then immediately baked for five hours at 120° F, after which process the casting is removed from the mold.

Any flashings on the castings are removed with a file or sander after the baking process.

EMR

4.8 Standard Procedure Re Ordering Materials for MDU.

A. General Procedure:

1) Every purchase requisition sheet (orange colored ordering blank) must be filled out in duplicate for each item ordered. No order should ever be placed orally.

2) Each ordering blank must be signed by one of the following:

H. D. Huskey
E. Lacey
James W. Walsh

3) The purpose for which the purchase is intended should be indicated by the appropriate number followed by a dash. Only one purpose can be shown on each ordering blank. At the date of this issue one of the following categories should be chosen:

1. General (to be used for all items purchased for general use, such as machine shop tools, stock items not purchased for a specific project, and small miscellaneous purchases)
2. Maintenance (items purchased specifically for the SWAC should be included in this category, such as tube replacements and paper tape)
3. Development
   A. SWAC (items purchased specifically for further development work on the SWAC, exclusive of the magnetic drum and magnetic tape units)
   B. Magnetic Drum
   C. Magnetic Tape

4) After the use has been indicated the material should be classified into one of the main and, in most cases, one of the secondary categories shown on the chart (page A 4.8-3 of this report) attached to the back of the board holding the ordering blanks. The main and secondary classification should be separated by a period.

In the event that two or more items of different classification are to be ordered the classification of each different item should be noted, with a comma separating the two classifications. If necessary to designate more than one secondary classification the appropriate numbers can be written consecutively with no punctuation marks.

4.8 Standard Procedure Re Ordering Materials for MDU.

For example, assume an order is to be placed for stock items of 2W, 10 per cent, 10K resistors, and for terminal lugs. In the blank designated for Requisition No., a "1" should be entered as the first number since both items are for general stock. (If this were not the case, separate ordering blanks would have to be used.) The second number should be a "2" to indicate that resistors are being ordered. In this particular example, a third number indicating type of resistors (in this case "3") should be also noted. After the "3" a comma should be written, followed by 5.3, the main and secondary classification of the second item, terminal lugs. The entire number for this order, to be indicated in the space called "Requisition No." on the purchase requisition blank, would be 1-2.3,5.3.

6) The date of the order should also be entered in the appropriate space on the purchase requisition blank.

F. Justification for New System:

To simplify the whole process of keeping records it has been decided to punch the MDU budgetary records on IBM cards, beginning fiscal year 1951 (July 1, 1950). Indication of the use for which the material is intended is necessary as certain funds have been allotted for specific purposes. The main and secondary classification numbers are required, since it is desirable to know precisely what has been ordered in the past to assist with the reordering of items.

4.8 Standard Procedure Re Ordering Materials for MDU.

1. General 2. Maintenance	3. Development A. SWAC	B. Magnetic Drum C. Magnetic Tape

Breakdown of MDU Purchases

Main Classifications	Secondary Classifications 1	2	3	4	5	6	7	8	9
1. Tubes and Accessories	C.R.T.	Tubes-- All Other	Tube Shields	Tube Clamps	Tube Sockets				Misc. Tube Acces.
2. Resistors Potentiometers	¼W R.	1W R.	2W R.	5W R.	10W R.		Larger Resistors	All Potentio-meters	Misc. Resis-tors
Condensers									
4. Other Circuit Components	Crystals	Delay Lines	Neons	Indicators	Small Lights				Misc.
5. Hardware	Screws	Nuts, Bolts, Washers	Lugs	Terminal Strips	Solder	Posts	Coils, Coil Forms	Insula-tors	Misc.
6. Wire and Cable	All Types Cable	Pushback Wire	Building Wire	Copper Wire					Misc.
7. Fuses	Little-fuses	Circuit Breakers	Power Fuses	Grasshopper Fuses				Fuse Holders, Bases	Misc.
8. Metals	Sheet Metal	Channel, Angle	Bus bar, Metal Rod, Tubing	Hypersil		Screen and Cloth	Wiremold		Misc.
9. Plastics (Paper)	Phenol Rod, Tubing	Spaghetti	Tagboard	Bakelite, Lucite, Transite, etc.			Fish Paper		Misc.
10. Sockets, Plugs, Jacks	Jones	Cannon		Minature	Ass't Sockets	Ass't Plugs	Jacks		
11. Power Components	Trans-formers	Chokes	Rectifiers	Contactors	Relays	Switches	Batteries		Misc.
12. Photographic and Drafting	Prints	Tracing Paper	Misc. Drftg. Supplies	Film	Photo Paper	Misc. Photo Supplies			
13. Computer Accessories	Flexo-writer and Acces.	Mag. Drum and Acces.	Mag. Tape Unit and Acces.	Paper Tape	Magnetic Tape				Misc.
14. Misc. Supplies	Lubri-cants	Painting Supplies	Cement, Glue Products	Library Material	Belts and Pulleys	Bottle Goods			Misc.
15. Tools	Drills, Plug Taps, End Mills	Sawblades	Wrenches, Pliers	Screw-drivers	Chisel Sets, Punches, Dies	Soldering Irons and Replacements	Measuring Tools	Grinding, Sanding Tools	Misc.
16. Equipment	Furniture	Elect. Equip.	Power Tools and Acces.	Power Supplies	Motors	Photo-graphic Equip.			Misc. Equip.
17. Services	Contract	Small Misc.	Consultant						Misc.

4.9 Standard Procedure for Winding "Signal Pickup Grids" Used on Face of CRT Tubes.

A. Machine and Materials Necessary:

1) Lathe. Logan No. 211.

2) Mold. Phenolic tubing 3" OD x ¼" wall x 9" long, with slots at both ends on one (1) axis only. Slots are ¼" deep x saw blade width.

3) Wire. No. 40 round, bare, magnet.

4) Combination wire holder and tension device.

5) Tape. Electrical 1" wide, No. 7, Scotch.

6) Acetone.

7) Nokorode flux paste.

8) Rosin core solder, 60/40, Resin Five.

9) Soldering iron, wiping cloths, bench knife, 12" steel rule.

B. Machine Set Up:

1) Carriage travel is at the rate obtained by gear drive, using a 24 stud gear with left hand lever in position "A" and right hand lever in position "12". This gives 12 turns per inch.

2) Compound rest assembly should be away from operator towards rear. Wire holder and tension device should be mounted in tool post so as to obtain maximum clearance between end of brass mounting bar of device and mold. (cf. Fig. 4.9-1 on page 4.9-3)

3) Carriage should be as far towards head of lathe as is consistent with proper engagement of feed screw.

4) Mold should be held by jaws of chuck exerting pressure outwards on ID of mold.

5) Slots in mold should be so displaced in respect to jaws as to prevent interference with one another.

C. Winding Instructions:

1) Winding is started by fastening free end of wire to end of mold adjacent to lathe chuck. Start of winding should be kept away from slots. Grid is made by having mold rotate toward operator for a winding length of five (5) usable inches. End turn of winding should be fastened with tape before cutting wire.

2) Connecting wire. Pieces of same wire as used for winding are cut 15 inches long. Individual lengths are used. One end is placed in slot in mold, at head of machine, and fastened with tape. Wire is then pulled taut (this is important!), and fastened down at slot in opposite end of mold. Wire extending beyond end of mold is placed inside of mold.

4.9 Standard Procedure for Winding "Signal Pickup Grids" Used on Face of CRT Tubes.

3) Each joint or point of contact to be soldered should be touched lightly with the end of a finger on which a barely perceptible amount of Nokorode flux paste has been placed. Soldering is accomplished by using a 60 watt iron with a flat tip. Flux remaining after soldering is carefully and thoroughly removed with Acetone on a cloth.

4) Each connection is gently probed to determine if it is firmly joined. All points of contact must be connected.

5) Mold is then rotated 180° and above is repeated (2, 3, and 4).

6) Winding is then covered with tape, quarter lapped. First turn of tape must be firmly fastened on itself so as not to cause distortion of winding when taping.

7) Winding is removed from mold by cutting the winding lengthwise, end-to-end, with a sharp knife. Before cutting, mold should be rotated so that one set of slots are at top as this brings one of the signal leads to the top. A steel rule is placed about $\frac{1}{4}$" away but parallel to this lead, lengthwise along mold and above winding to serve as a guide when cutting. All wires must be severed.

Extreme care should be exercised at all times during the winding process.

If grids are not used immediately, they should be placed in proper container with adhesive side up.

JW
GMF
JHN.

4.9 Standard Procedure for Winding "Signal Pickup Grids" Used on Face of CRT Tubes.

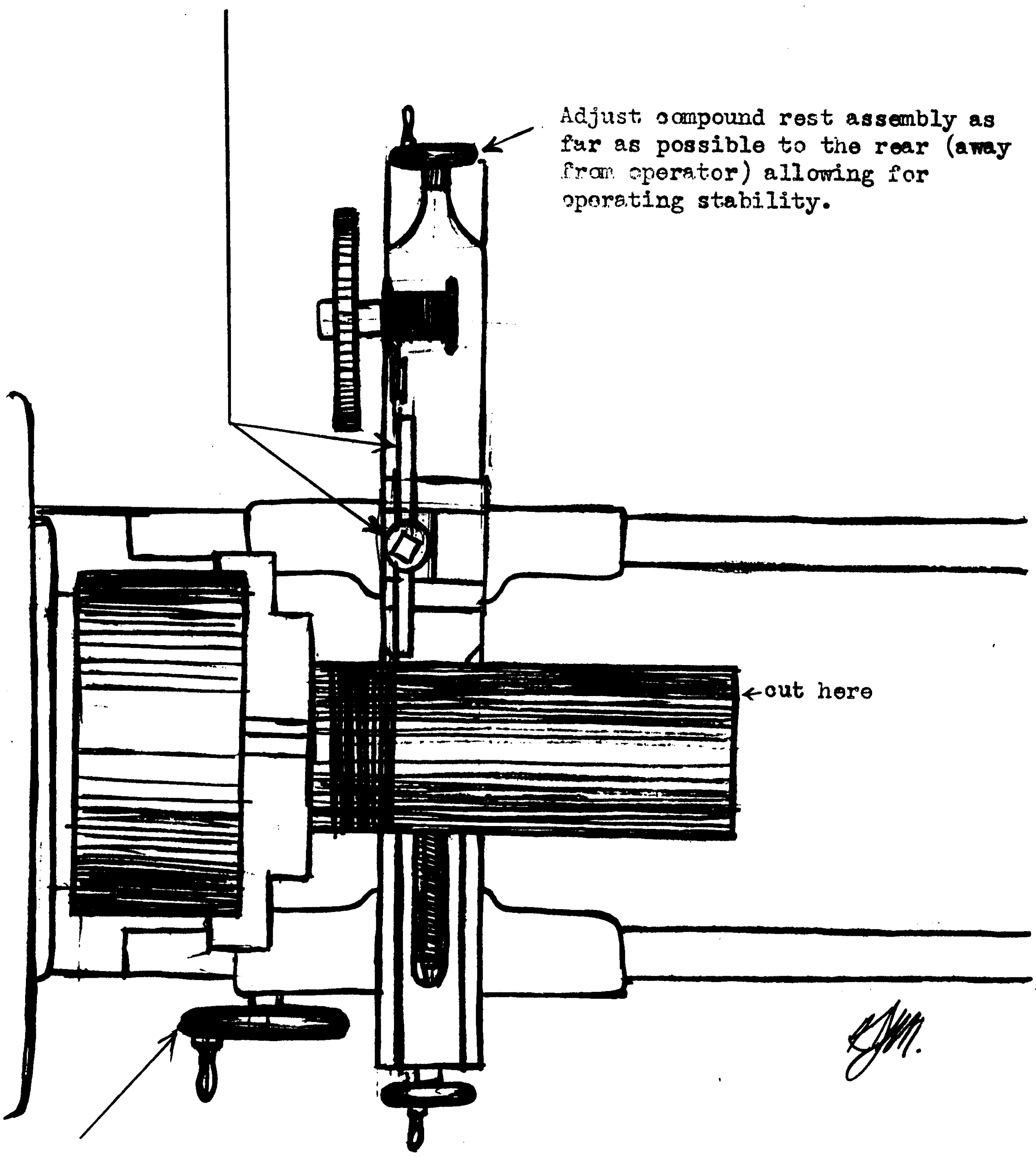


Figure 4.9-1 Lathe Set-Up

4.10 Conventions in the Assembly of Plug-in Turrets.

Place turret in such a manner that the bail is away from you and the hole for the neon lamp is to the left. The key in the 11-pin plug should be to the left, and pins 1 and 9 on the 9-pin socket on top. The bakelite card should be mounted so that in this position the top row of five lugs (lugs nearest to tube socket) is facing up.

R. T.

4.11 Numbering Procedure for New Tubes.

The following procedure has been adopted for numbering new vacuum tubes for use in the SWAC.

1) Tube types which have only a general purpose use will be numbered consecutively starting with one and going as far as necessary.

2) Tube types which have both general purpose and special purpose uses will be numbered as follows:

   The general purpose tubes will be numbered in odd-numbered-hundreds (100, 300, etc.) and the special tubes will be numbered in even-numbered-hundreds (200, 400, etc.).

   In addition, the general purpose tubes number will be preceded by the letter G.

   The special purpose tubes number will be preceded by a letter which will signify the primary use of the tube according to the following code: A - amplifier, C - cathode follower, F - flipflop, L - low noise.

   If the special purpose tube becomes no longer usable for its special purpose, but is still good for general use, the letter G will be added in front of the existing number to signify that it is a tube whose category has changed from special use to general use.

When new tubes are received, it will be the responsibility of the person in charge of the stock room to have the tubes numbered as above, tested (cf. A 4.12), and placed in stock.

4.12 Testing Procedure for New Tubes.

Following is a chart listing reject conditions in testing tubes used in the SWAC:

Tube Type	Discard if cut-off current registers more than:	Discard if 0 grid bias current registers less than:
6AG7 Flipflop	0.2 ma	40 ma
6AG7 General	0.7 ma	32 ma
6AG7 Cathode Follower	0.7 ma	50 ma
12AU7 Flipflop	0.2 ma	10 ma
12AU7 General	0.7 ma	8 ma
6AN5	0.7 ma	32 ma
6AS6	0.7 ma	8 ma

Note: The 2C51, 12AT7, and 6SN7 tubes must pass a noise test and gm test.

4.13 Procedure to be Followed on Receiving New Cathode Ray Tubes.

When cathode ray tubes are received, the serial numbers will be recorded on the invoice immediately. Then the tube will be checked for possible mechanical faults. Attention should be given to the deflection and post accelerator caps, if any, and the tube base. Also a continuity check of the filament should be made.

When the above has been done, grids must be made and attached to the face of the cathode ray tube. Also a band of tape should be wrapped around the base for the tube clamp to grip. The tubes should then be returned to their cartons and stored until put into use.

It will be the responsibility of the person in charge of the stock room to see that this work is done.

4.14 Procedure to be Followed on Receiving New Crystals.

Crystal color coding:

When new crystals are received they will be color coded. This is to be done in order to distinguish one shipment of crystals from another. The various shipments will be numbered in order according to the R.M.A. color code, starting with zero for the first shipment and proceeding from there.

It will be the responsibility of the person in charge of the stock room to see that this work is done.

4.15 Standard Procedure for Making Pulse Transformers.

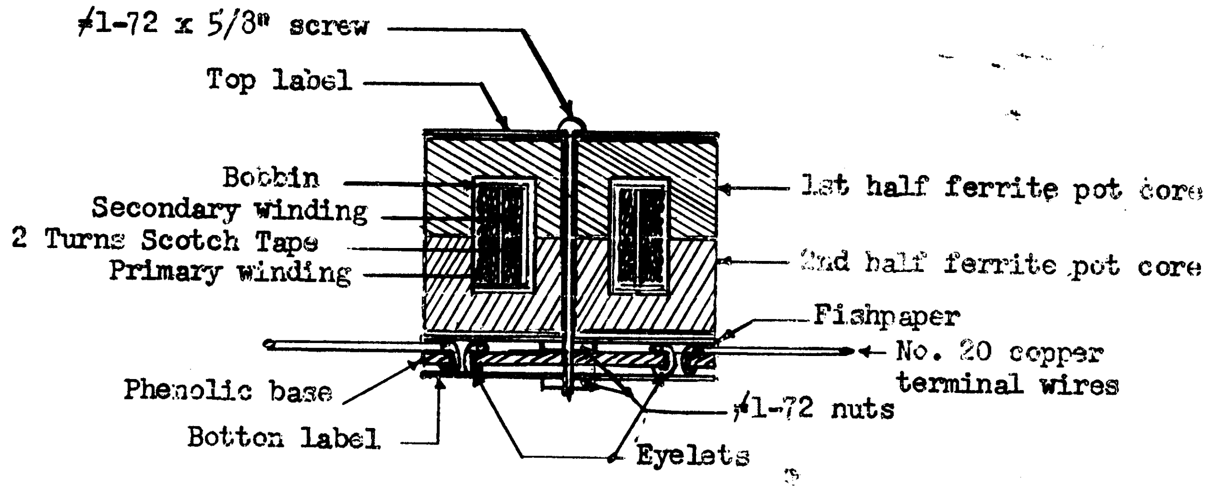
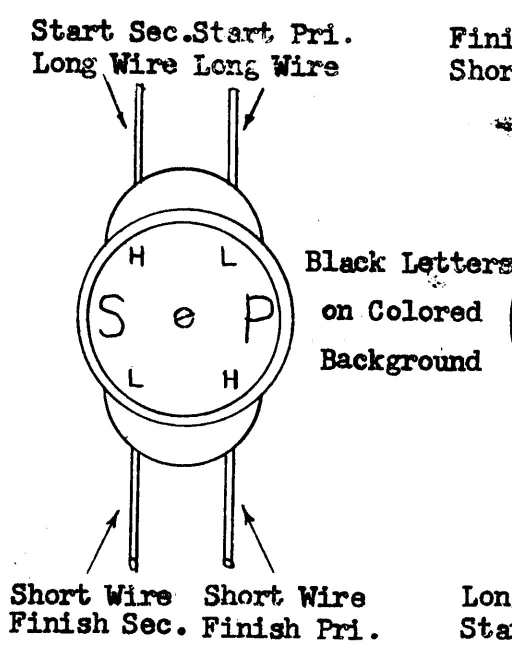
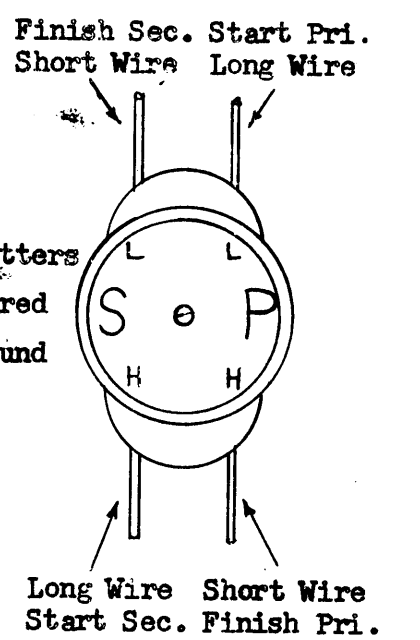


Figure 1. CROSS SECTION OF PULSE TRANSFORMER



Primary and Secondary Coils Wound in the Same Direction

Figure 2. REVERSING



Primary Wound in Opposite Direction from Secondary

Figure 3. NON-REVERSING

Trans.	Pri.	Wire	Sec.	Wire	Color Code
A	150	38	150	38	Brown
B	150	40	75	32	Red
BC	150	40	50	32	Orange
C	98	38	27	28	Yellow

Table I. WINDING DATA

4.15 Standard Procedure for Making Pulse Transformers.

Coil Winding:

The bobbin (see Item 2, Table II, page A4.15-4) is placed on the coil winder with slot facing to the left. The secondary winding is wound on first, leaving the finish end of the wire shorter than the starting end. Add one layer of scotch tape around secondary winding. NOTE: Do not put any polystyrene cement on the secondary winding as it adds capacity and causes the pulse to ring.

If winding a reversing transformer, leave the bobbin as is and continue with the primary winding.

If winding a non-reversing transformer, turn the bobbin with slot facing to the right before putting on the primary winding.

On the primary winding, the finish end of the wire is also left shorter than the starting end. After primary is wound, one drop of polystyrene cement is placed on the wire at the slot. To dry and remove the excess cement, spin the coil at top speed. Place scotch tape on lead wires of coil to identify non-reversing transformer.

Manufacturing of Transformer Parts:

Using 3/64" fabric base phenolic (see Item 4, Table II), cut out round base plate with 9/16" circular punch. Use special template for drilling holes in the base plate. For large holes use #43 drill and for the small hole in center use #49 drill. Use shank of #43 drill for bending terminal wires which are #20 solid copper tin coated. Insert eyelet (see Item 3, Table II) through terminal wires and base plate, and crimp with eyelet crimping pliers.

Use rubber stamps to print transformer terminal labels on proper colored paper (IBM cards), using color codes in Table I, page A4.15-1. Punch out with 9/16" circular punch and use template to drill center hole (#49 drill).

Punch 9/16" circular insulators out of .006" fishpaper and drill center hole with template (#49 drill).

4.15 Standard Procedure for Making Pulse Transformers.

Assembling:

Place a #1-72 NF x 5/8" round head brass screw through top terminal label. Add one-half of ferrite pot core (see Item 1, Table II, A4.15-4). Place coil in core with lead wires down and through slot. Put other half of core in place. On bottom of core place fishpaper insulator and tighten down with #1-72 brass hex nut. Place base plate on, with terminal wires closest to ferrite pot core and at right angles to slot. Place bottom terminal label on and tighten with second #1-72 hex nut. See Figures 2 and 3 for the correct terminal connections for the coil windings. Wrap coil leads loosely around the correct terminal wires and apply with eyedropper Turco #2489 (WARNING: do not get on hands). Let stand for approximately 15 minutes. Lightly brush off with brush dipped in acetone to remove Turco and insulation on lead wires. Rewrap wires close to base plate and solder.

Casting:

Set transformers on side with slot up. Mix thoroughly 1 teaspoon of Selectron Resin #5026 with ten drops of Duoprox hardener (see Item 5, Table II). Pour small amount of plastic mixture into slot of core until fully saturated. Let set for at least one hour.

Apply a film of mold release to the inside cavity of mold. Mix up plastic as above and pour small quantity in bottom of mold. Hold transformer over cup and pour plastic over transformer until covered. Put transformer in mold and tighten down mold ears. Fill to top with plastic and place a piece of cellophane over plastic so it will dry free from stickiness and have a smooth appearance.

Bake in oven at 150° F for about 30 minutes. Remove from oven. Let cool till room temperature. Remove cellophane and flashings. Release mold ears and gently lift transformer out.

4.15 Standard Procedure for Making Pulse Transformers.

Table II. Materials Used in Making Pulse Transformers

	Item	Source
1.	Cores, pot, using Ferroxcube 3C Potcore Type 7F154	Ferroxcube Corporation of America 11325 Washington Boulevard Culver City, California
2.	Spools, plastic, for Type 7F154 cores	Same source as Item 1 above.
3.	Eyelets, brass, 1/8" long x .069"ID x .088"OD	Andrews Hardware and Metal Company 334 South Main Street Los Angeles 13, California
4.	Panelyte, fabric base, phenolic, natural color, No. 900	Electrical Specialty Company 418 East Third Street Los Angeles, California
5.	Casting, plastic, Selectron Resin #5026 (made by Pittsburgh Plate Glass Company)	Thalco 765 South Harvard Boulevard Los Angeles 5, California

5.1 6AN5

DESCRIPTION

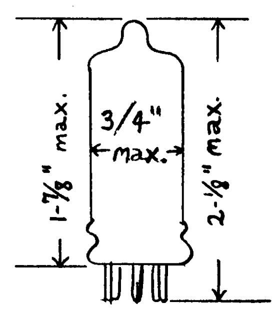
The 6AN5 is a heater-cathode type, pentode power amplifier of miniature construction. The design features of low triode mu, high transconductance, high plate current and relatively low interelectrode capacitances make it particularly suitable for service as a wide band, RF or video power amplifier in equipments with low plate supply voltages.

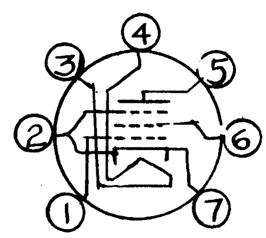
MECHANICAL DATA

ENVELOPE: T-5½ Glass
BASE: Miniature Button 7-Pin
TERMINAL CONNECTIONS: (JETEC Designation 7BD)

Pin 1	Grid # 1	Pin 5	Plate
Pin 2	Cathode, Grid # 3	Pin 6	Grid # 2
Pin 3	Heater	Pin 7	Cathode, Grid # 3
Pin 4	Heater		

MOUNTING POSITION: Any





Bottom View

ELECTRICAL DATA

DIRECT INTERELECTRODE CAPACITANCES: (μμfds)*

Grid # 1 to Plate	0.075 max.
Input	9.0
Output	4.8

DESIGN CENTER MAXIMUM RATINGS:**

Heater Voltage (a.c. or d.c.)	6.3	6.3	V
Plate Voltage	120	300	V
Grid # 2 Voltage	120	300	V
Plate Dissipation	4.2	1.70	W
Grid # 2 Dissipation	1.4	0.56	W
Cathode Current	50	20	ma
Bulb Temperature	140°	140°	C

CHARACTERISTICS AND TYPICAL OPERATION - CLASS A_1 AMPLIFIER:

Heater Voltage (a.c. or d.c.)	6.3 V
Heater Current	0.45 amps
Plate Voltage	120 V
Grid # 2 Voltage	120 V
Cathode Resistor***	120 ohms
Plate Resistance (approx.)	12500 ohms
Transconductance	8000 μmhos
Plate Current	35 ma
Grid # 2 Current	12 ma
Load Resistance	2500 ohms
Power Output (approx.)	1.3 W
Grid Voltage for Ib = 1.0 ma max.	-20 V

* Using JETEC shield #316 connected to cathode.

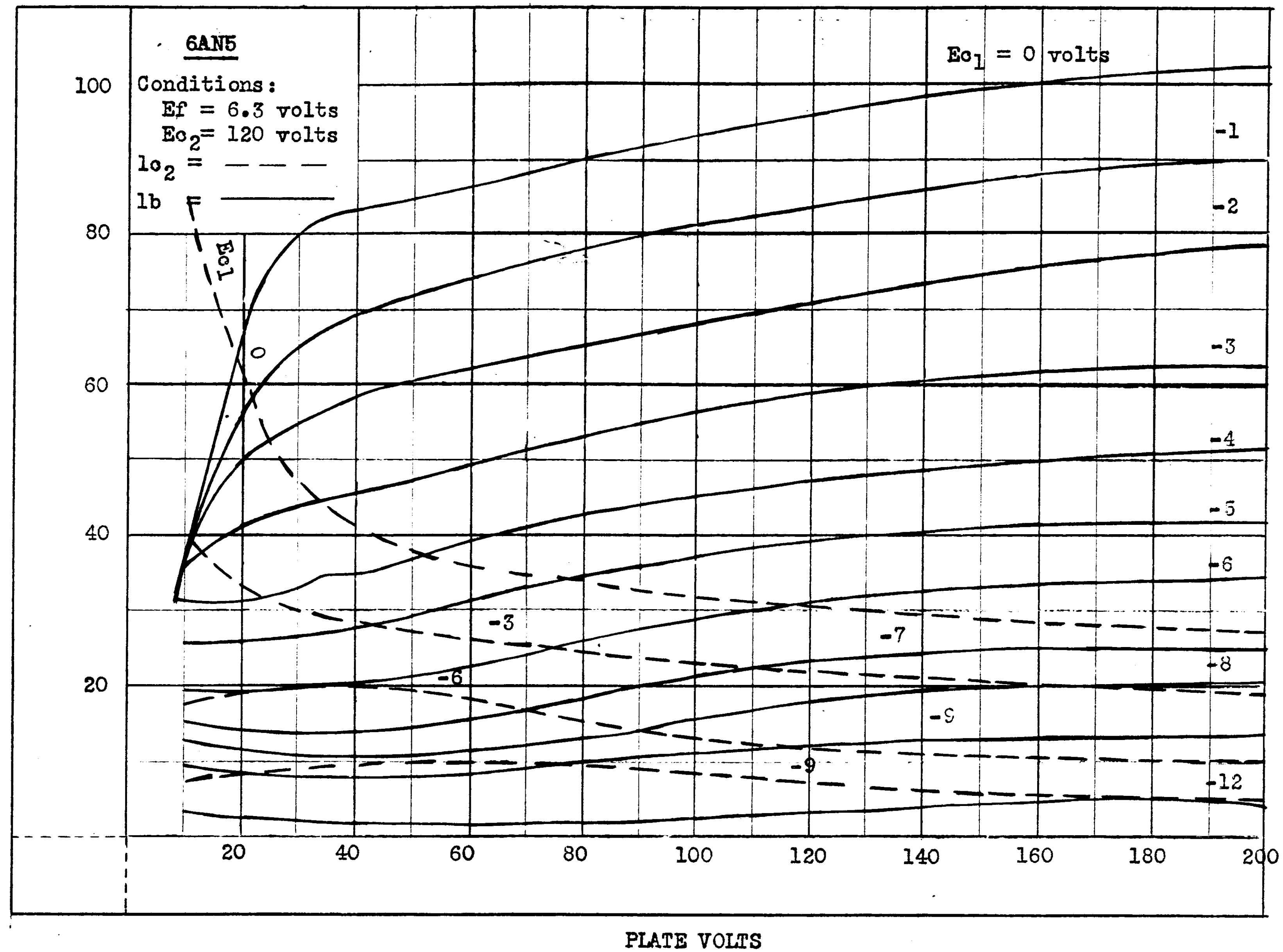
** The heater voltage should not deviate more than ± 10 percent from the rated value.

*** Fixed bias operation is recommended only when the plate and screen dissipation is less than 70 percent of the design center maximum ratings.
The d.c. grid circuit resistance should not exceed 100,000 ohms for self bias operation or for the limited fixed bias operation defined above.
The d.c. grid circuit resistance should not exceed 250,000 ohms for self bias operation in applications where the absolute maximum heater voltage is 6.6 volts.

Issued 7-28-49
Reissued 4-20-51

5.1 6AN5

AVERAGE PLATE CHARACTERISTICS



5.2 Technical Information on Western Electric 350A and 350B Vacuum Tubes

Classification

Beam power tetrodes with indirectly heated cathodes.
The 350A and 350B tubes have essentially identical static characteristics. The tubes differ in the way the leads are brought out and in basing arrangements.

Applications

The 350A tube is suitable for use as an audio frequency amplifier, radio frequency amplifier, oscillator, modulator or frequency multiplier.

The 350B tube may be used as an audio frequency amplifier or as a radio frequency oscillator.

Connections

Figures 1 and 2 show the arrangements of the electrode connections.

Basing

The 350A tube is provided with a medium, five-pin thrust type base.
The 350B tube is provided with a medium shell, seven-pin octal base.

Sockets

350A - Western Electric 141A or similar socket.
350B - Standard octal type socket.

Mounting Positions

These tubes may be mounted in any position. Provision should be made for free circulation of air to avoid overheating the glass.

Direct Interelectrode Capacitances

	350A	350B
Control-grid to plate (maximum)....................	0.3	0.5
Control-grid to heater, cathode and screen-grid....	18	18
Plate to heater, cathode and screen-grid...........	8	9

Heater Rating

Heater voltage .... 6.3 volts, a.c. or d.c.
Nominal heater current .... 1.6 amperes

The heaters of these tubes are designed to operate on a voltage basis and should be operated as near the rated voltage as possible.

The voltage between the cathode and heater should not exceed 150 volts.

5.2 Technical Information on Western Electric 350A and 350B Vacuum Tubes

Ratings

The 350A tube, having the plate terminal at the top of the bulb, is capable of withstanding higher plate voltages than the 350B tube. The 350A tube may withstand instantaneous voltages between plate and cathode as high as 7000 volts, provided the tube is operated in special circuits where its rated dissipations are not exceeded. The 350A tube may be used at maximum ratings at frequencies up to 60 megacycles.

The maximum operating conditions are given in Table 1.

Characteristics

Figures 3 and 4 show typical curves of plate current and screen-grid current as functions of control-grid voltage for several values of screen-grid and plate voltage. For these curves the screen-grid voltage is equal to the plate voltage.

Figures 5 and 6 show typical curves of plate current and screen-grid current as functions of plate voltage for a number of control-grid voltages. For these curves the screen-grid voltage was held constant at 250 volts.

Operating Conditions and Output

Nominal performance data are given in Tables 2 and 3 for a number of typical operating conditions. Less severe operating conditions should be selected in preference to maximum conditions wherever possible. The lives of the tubes at maximum conditions will be shorter than at the less severe conditions.

The performance data include the fundamental power output for the indicated values of load resistance and input voltage, and the corresponding second and third harmonic levels. The power output is given in watts and the harmonic levels in decibels below the fundamental.

5.2 350A and 350B Vacuum Tubes

TABLE 1

Maximum Operating Conditions

	A.F.Amp and Mod Class A	R.F.Amp Class B	R.F.Amp Plate Mod Class C	R.F.Amp and Osc Class C
			350A	
Direct plate voltage	600	600	475	600 volts
Direct screen voltage	300	300	300	300 volts
Negative direct grid voltage	-	-	200	200 volts
Direct plate current	*125	85	90	**105 milliamperes
Direct grid current	0	5	5	5 milliamperes
Plate input	65	45	45	62.5 watts
Screen dissipation	4	2.8	2.8	4 watts
Plate dissipation	30	30	20	30 watts
			350B	
Direct plate voltage	400	Not Suitable	Not Suitable	400 volts
Direct screen voltage	250			250 volts
Negative direct grid voltage	-			200 volts
Direct plate current	*125			**105 milliamperes
Direct grid current	0			5 milliamperes
Plate input	50			50 watts
Screen dissipation	4			4 watts
Plate dissipation	25			25 watts

* At maximum signal.

** Key down condition for intermittent service such as telegraphy. For continuous operation the direct plate current should be limited to 85 milliamperes.

5.2 350A and 350B Vacuum Tubes

TABLE 2

Single Tube

Plate Voltage	Screen-Grid Voltage	Control-Grid Voltage	Plate Current	Amplification Factor	Plate Resistance	Transconductance	Load Resistance	Input Voltage	Power Output
Volts	Volts	Volts	Milliamperes		Ohms	Micromhos	Ohms	Peak Volts	Watts
250	250	-14	94	287	35,000	8,200	1,500	14	8
							2,000	14	10
							2,500	14	10
300	250	-16	80	339	44,000	7,700	1,500	16	9
							2,000	16	12
							2,500	16	13
350	250	-18	65	364	52,000	7,000	2,000	18	13
							3,000	18	15
							4,000	18	15
400	250	-20	53	400	64,000	6,250	2,000	20	15
							3,000	20	18
							4,000	20	18
500*	250	-20	55	430	67,000	6,400	2,500	20	18
							3,500	20	22
							5,000	20	24

* Applies to 350A tube only. Maximum plate voltage for the 350B tube is 400 volts.

TABLE 3

2 Tubes

Push-Pull Amplifier - Class AB

Plate voltage........400 volts

Screen voltage.......250 volts

Grid voltage.........-22 volts

Input voltage - grid to grid........ 44 peak volts

Plate current......... 82 milliamperes

Load resistance.......6000 ohms

Power output.......... 40 watts

5.2 350A and 350B Vacuum Tubes

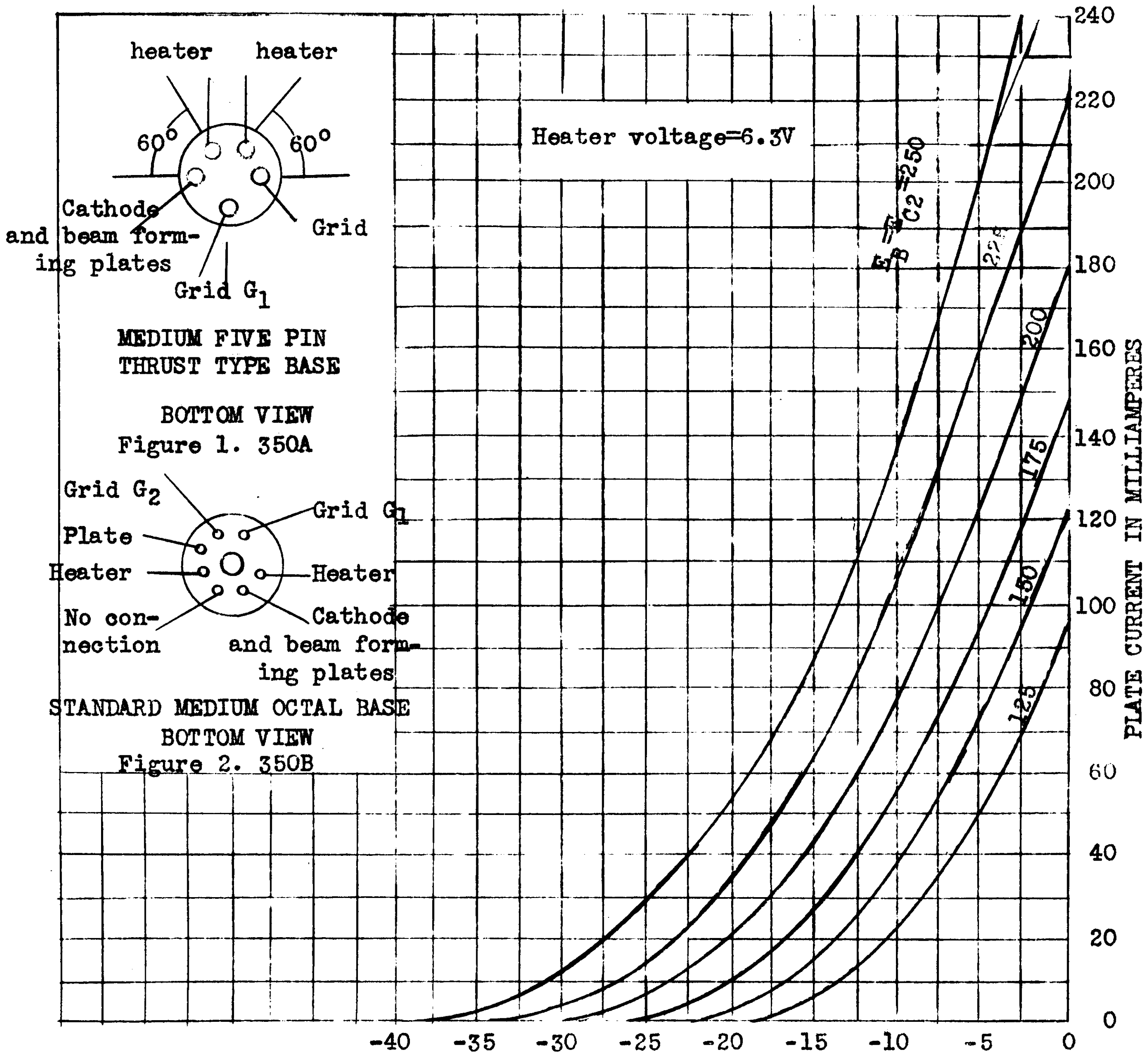


Figure 1. 350A

Figure 2. 350B

Figure 3

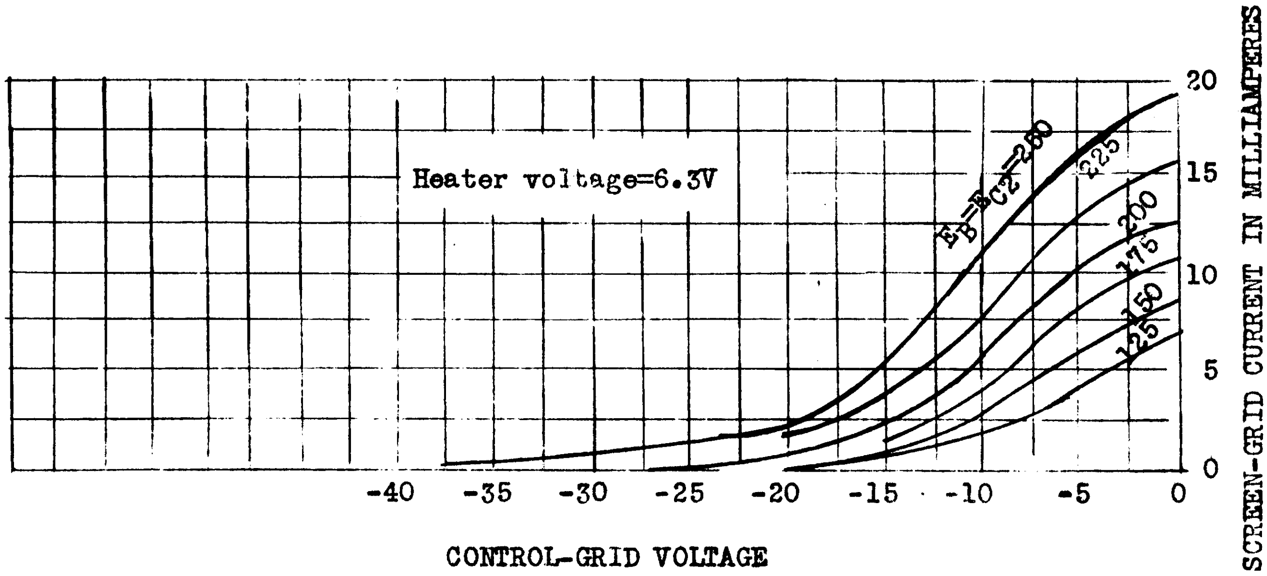


Figure 4

5.2 350A and 350B Vacuum Tubes

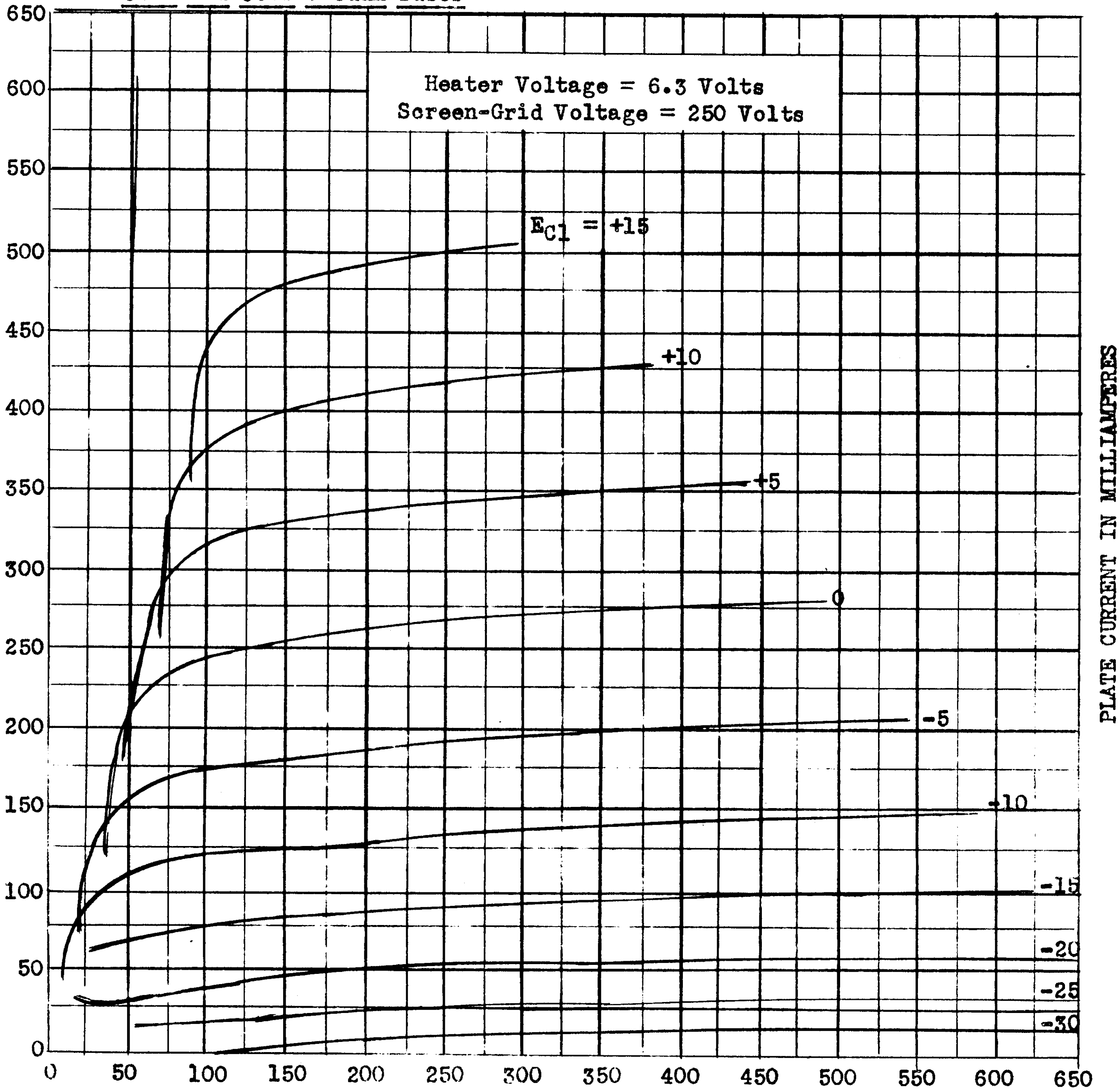


Figure 5

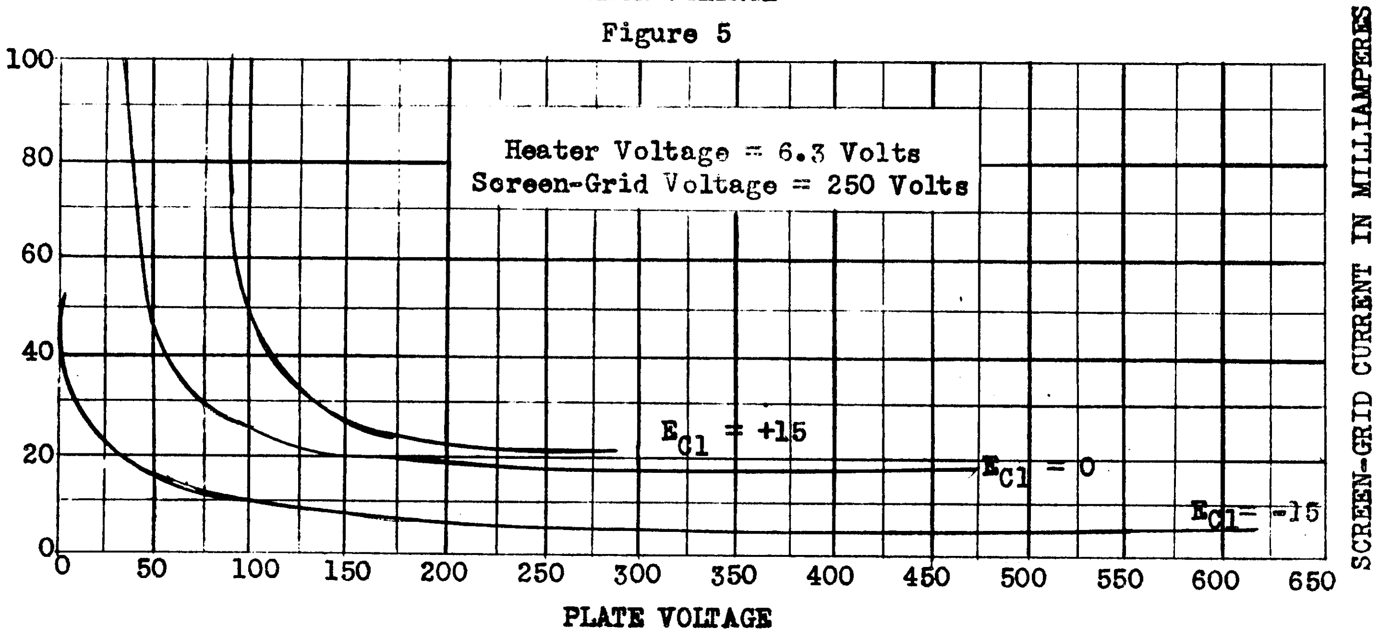
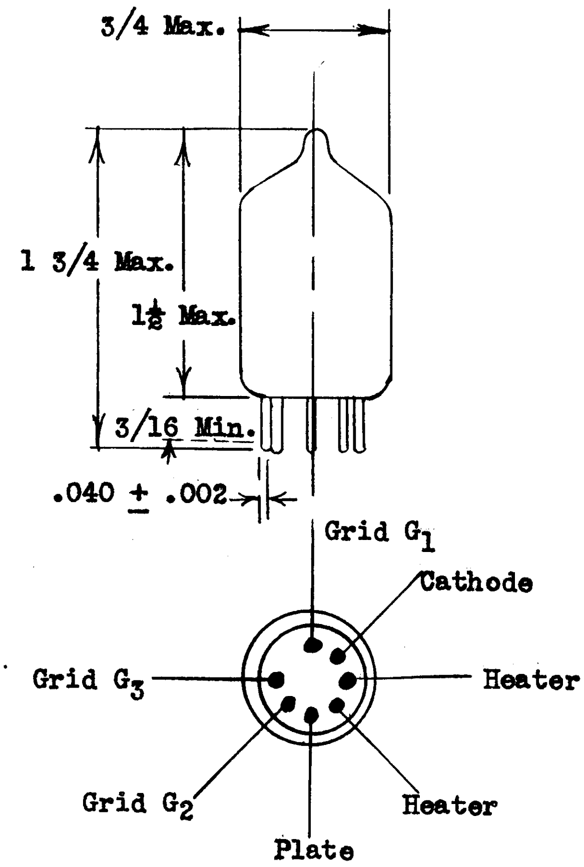


Figure 6

5.3 Technical Information on Western Electric 6AS6 Vacuum Tubes



Note: Tube pins shall by weight of tube be capable of entering a guage 1/4 thick, having 7 holes of .052 D. located on true centers of the pins. With tube seated in the pin gauge the glass envelope shall freely pass thru a .7551 D. cylinder which is coaxial with the specified pin circle.

Classification

The 6AS6 vacuum tube is a triple-grid pentode with an indirectly heated cathode. It is intended for low power applications at high and ultra-high frequencies. The usual control grid (grid No. 1) and the suppressor grid (grid No. 3) can be used as independent control elements. The tube is suitable for use in gated amplifiers, gain controlled amplifiers, delay circuits, and mixers.

Mounting

The dimensions and arrangement of terminal connections are shown in the above drawing. The tube may be mounted in any position.

Heater Rating

Heater voltage	6.3 volts, a.c. or d.c.
Nominal heater current	0.175 ampere

5.3 Technical Information on Western Electric 6AS6 Vacuum Tubes

Maximum Ratings (Design-center values)

Maximum plate voltage	180 volts
Maximum screen voltage	140 volts
Maximum positive suppressor voltage	27 volts
Maximum plate dissipation	1.7 watts
Maximum screen dissipation	0.75 watt
Maximum cathode current	18 milliamperes
Maximum heater-cathode voltage	90 volts
Maximum bulb temperature	120°C

Operating Conditions and Characteristics

Plate voltage	120	120 volts
Screen voltage (grid No. 2)	120	120 volts
Suppressor voltage (grid No. 3)	-3	0 volts
Control-grid voltage (grid No. 1)	-2	-2 volts
Plate current	3.6	5.2 milliamperes
Screen current	4.8	3.5 milliamperes
Transconductance, grid No. 1	1850	3200 micromhos
Transconductance, grid No. 3	810	470 micromhos

Grid No. 1 Plate Current Cut-Off Characteristics

Plate voltage	120 volts
Screen voltage	120 volts
Suppressor voltage	0 volts
Nominal cut-off, grid No. 1	-6 volts
Guaranteed cut-off, grid No. 1	-10 volts

Grid No. 3 Plate Current Cut-Off Characteristics

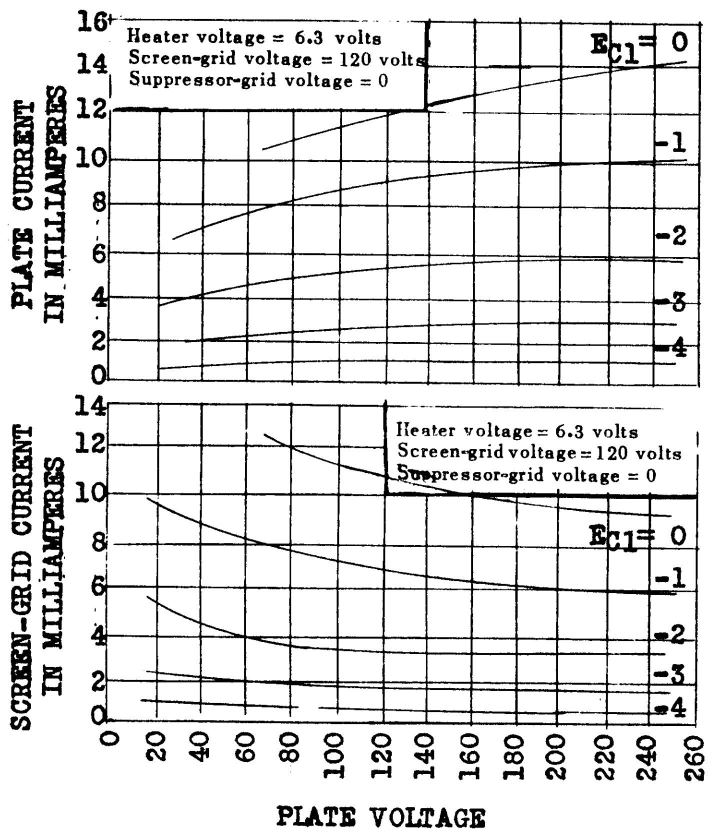
Plate voltage	120	120 volts
Screen voltage	120	60 volts
Control-grid voltage	-2	0 volts
Nominal cut-off, grid No. 3	-10	-8 volts
Guaranteed cut-off, grid No. 3	-15	-10 volts

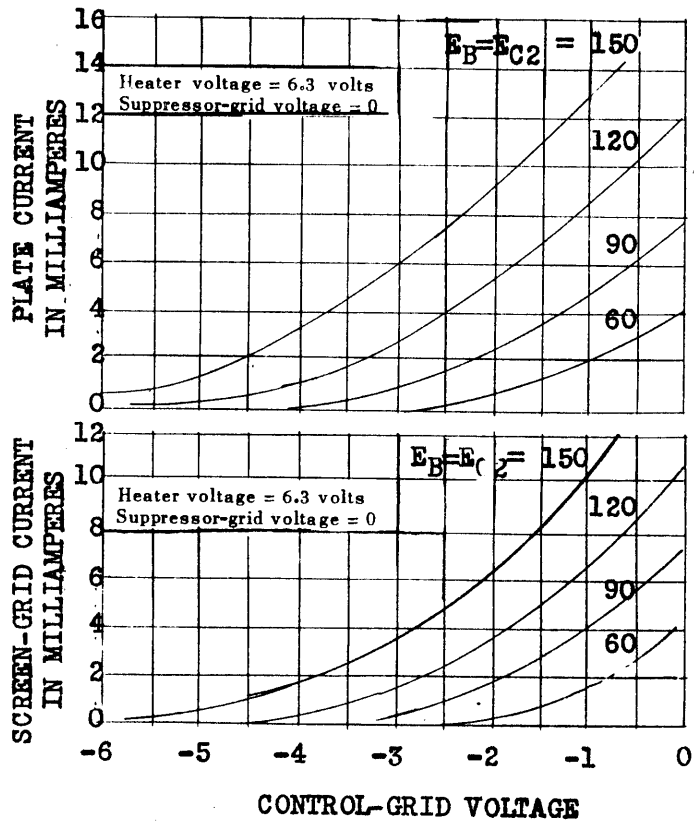
*Interelectrode Capacitances (With shield, connected to cathode)

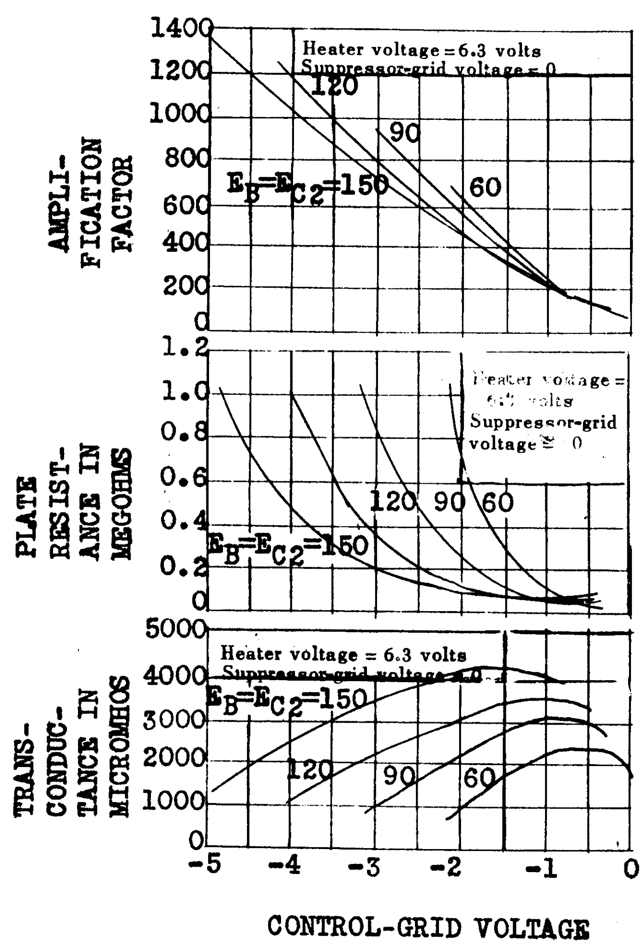
Control-grid to heater, cathode, screen-grid and suppressor-grid	3.9 micro-microfarads
Plate to control-grid	0.01 micro-microfarad
Plate to heater, cathode, screen-grid and suppressor-grid	2.8 micro-microfarads
Grid No. 1 to grid No. 3	0.1 micro-microfarad

* Measured with the pins shielded from each other and from the elements of the tube.

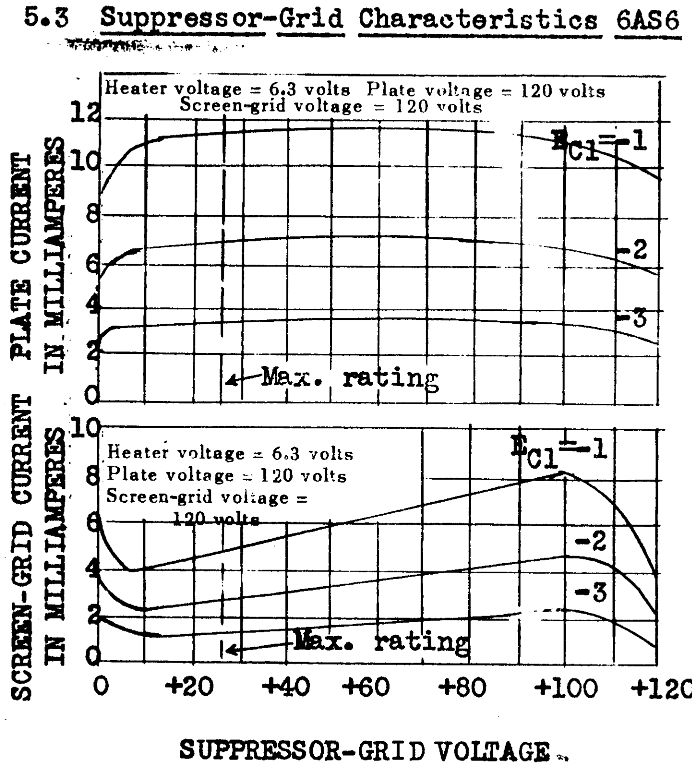
5.3 Normal Pentode Characteristics 6AS6

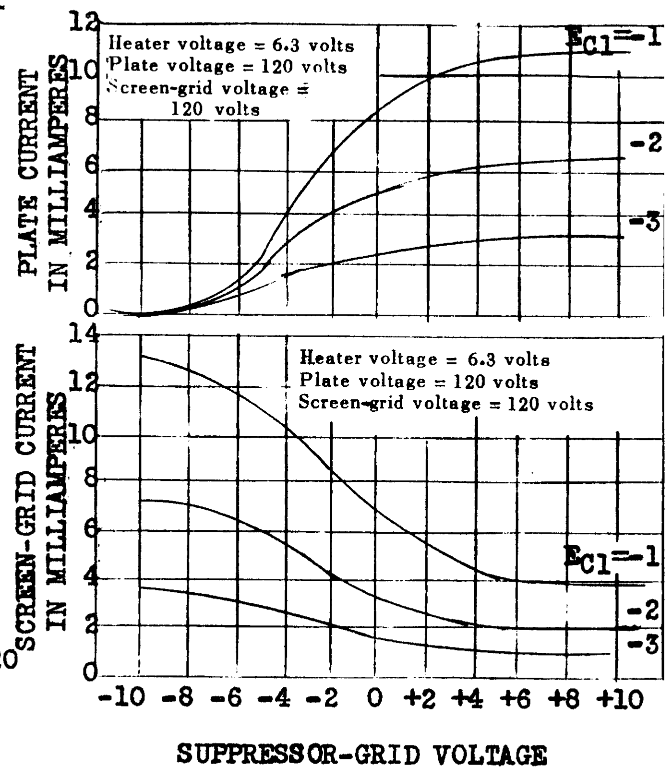


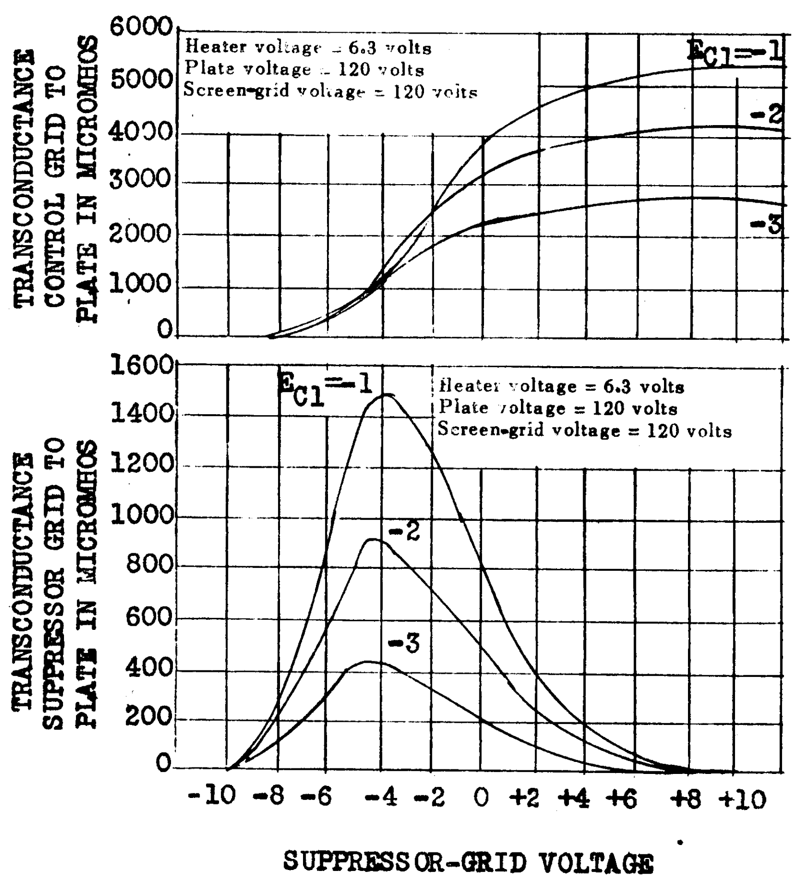




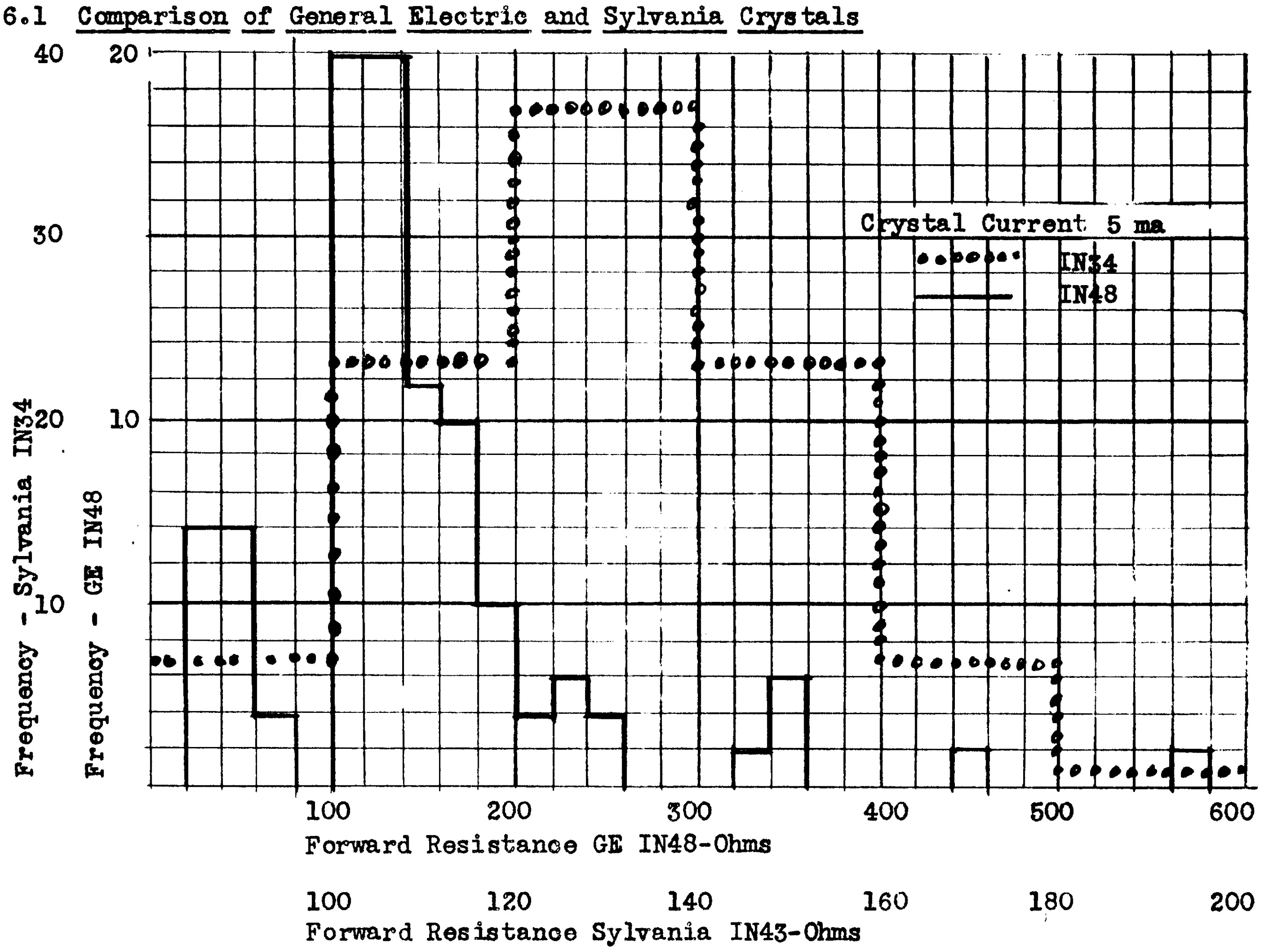
5.3 Suppressor-Grid Characteristics 6AS6

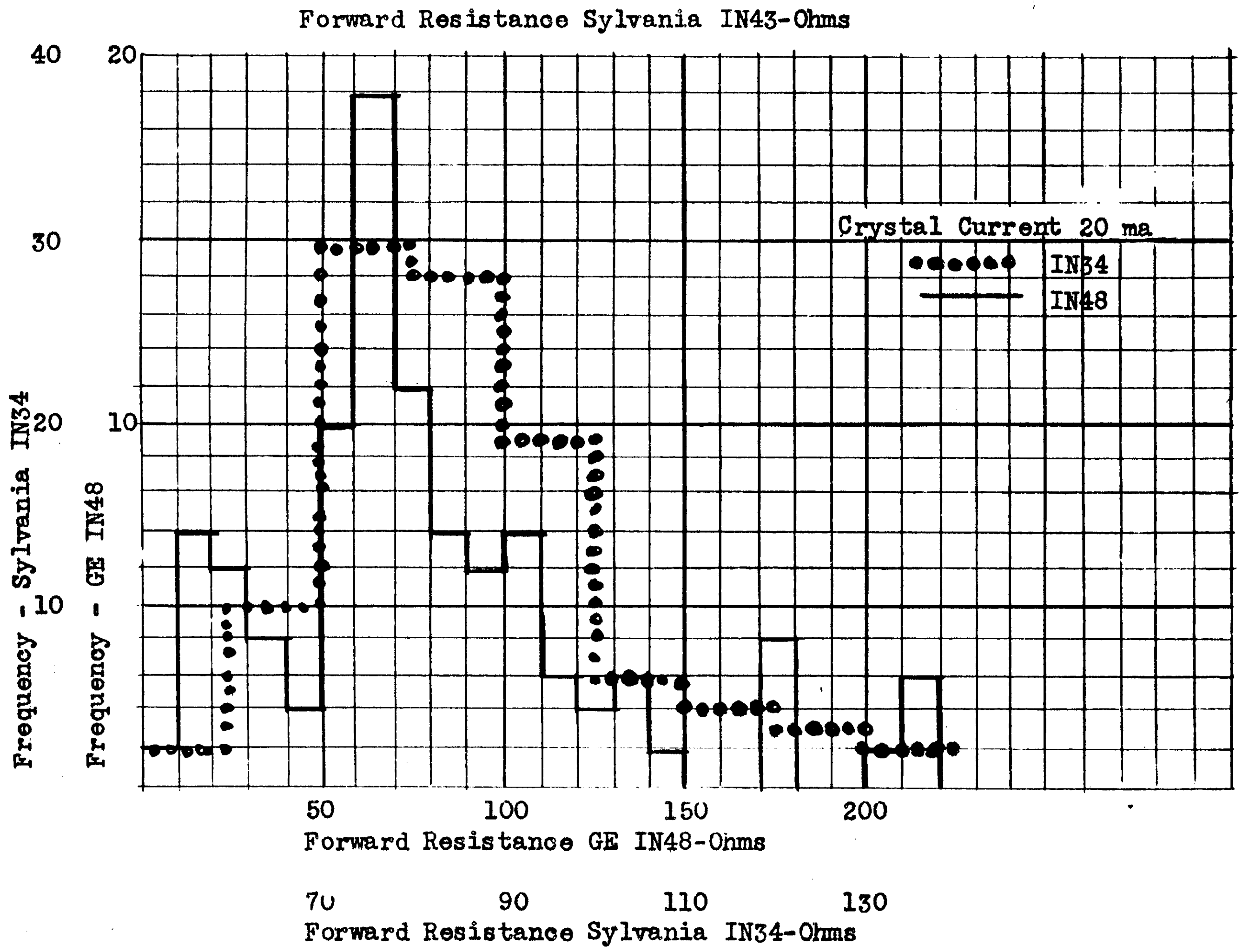






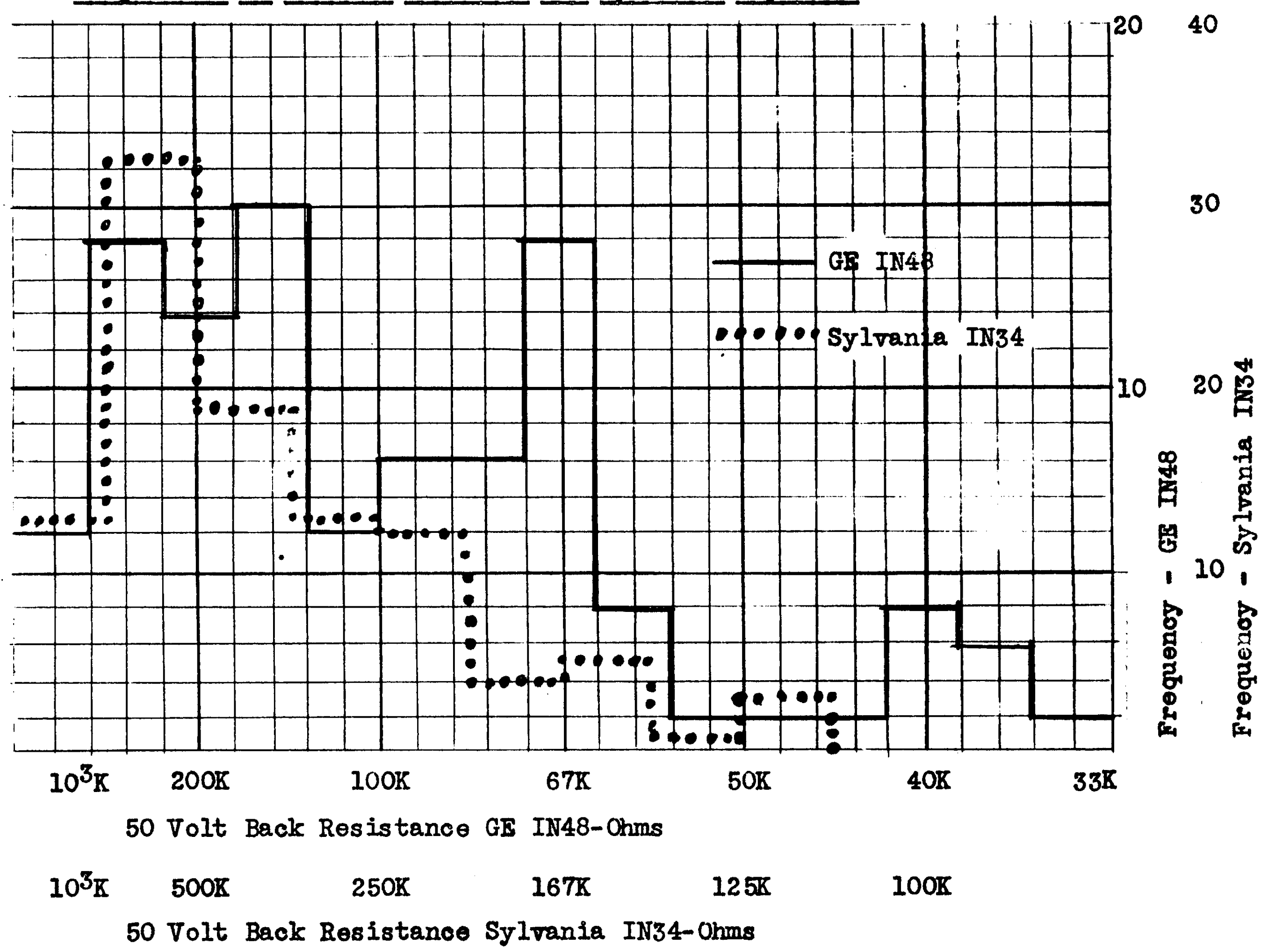
6.1 Comparison of General Electric and Sylvania Crystals





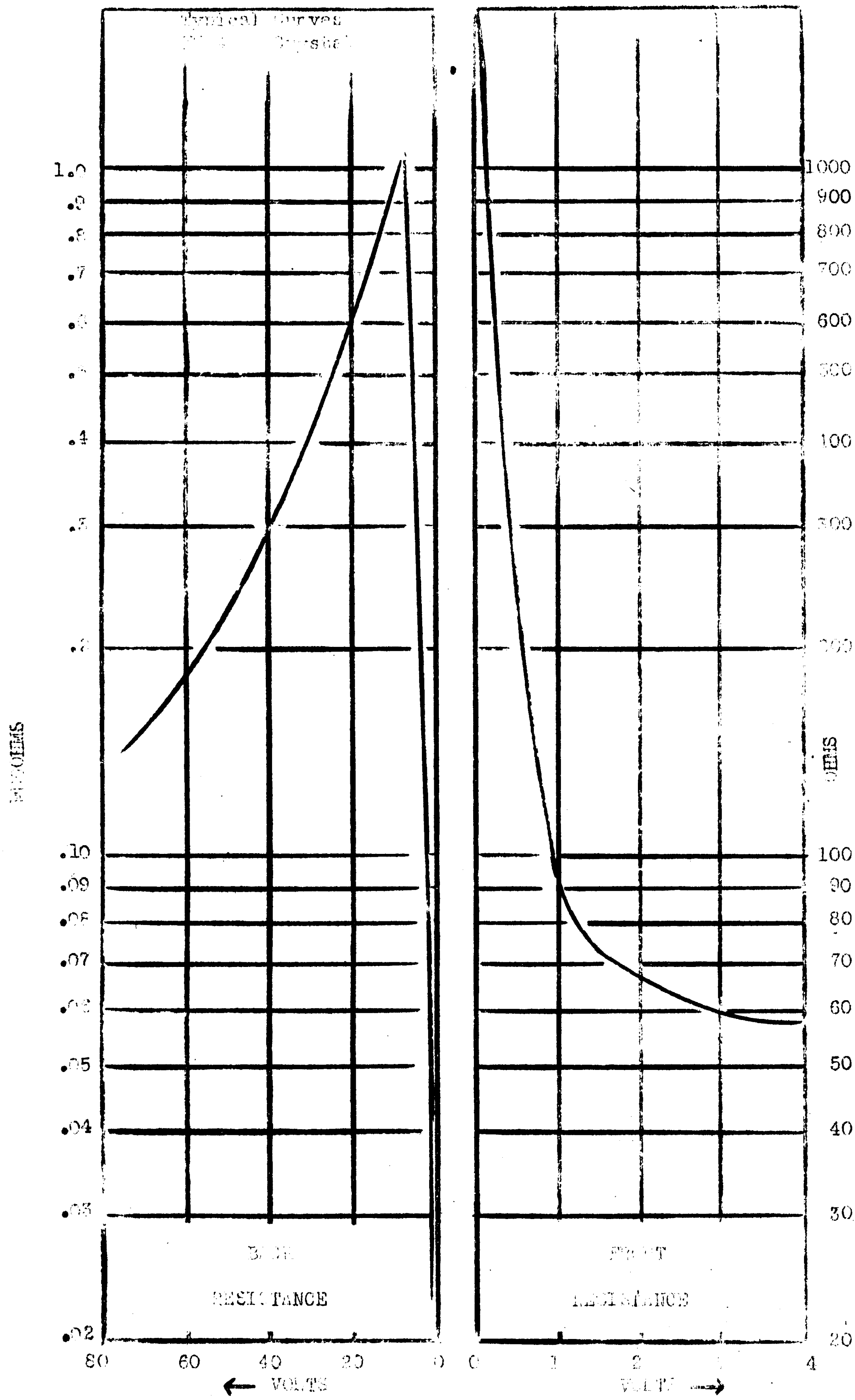
Resistance Distribution of 100 GE IN48 and 100 Sylvania IN34 Germanium Diodes

6.1 Comparison of General Electric and Sylvania Crystals



Resistance Distribution of 100 GE IN48 and 100 Sylvania IN34 Germanium Diodes

6.2 Static Characteristics of Sylvania IN34 Crystals.



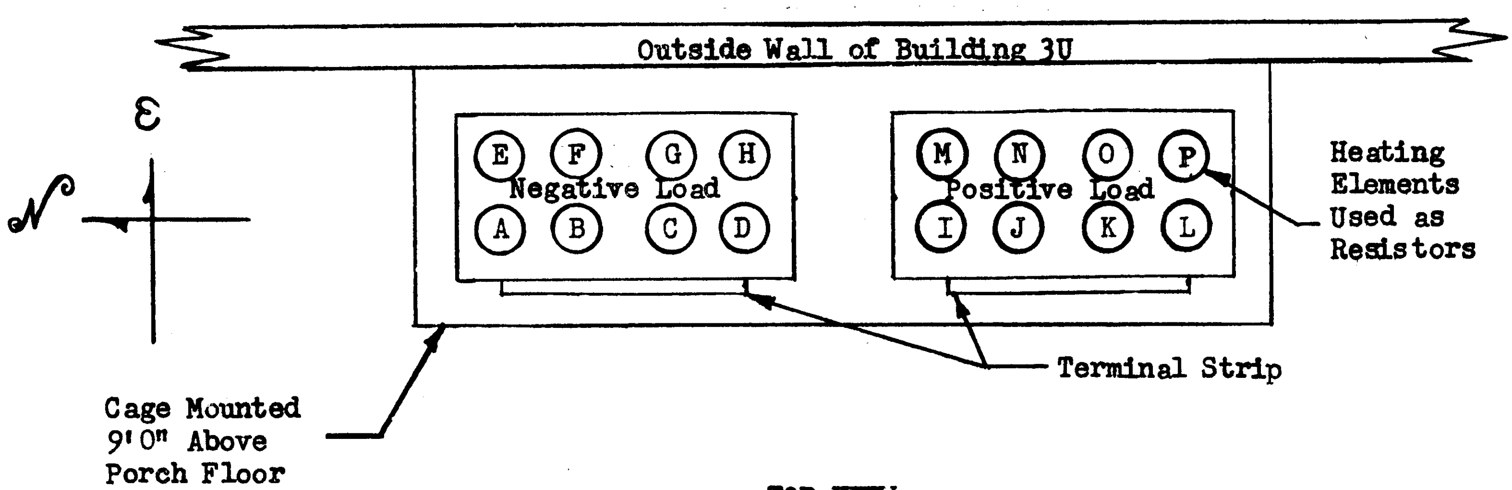
Static Resistance Characteristics of Sylvania IN34 Crystals.

7. POWER SUPPLIES

7.1 Laboratory Power Supply.

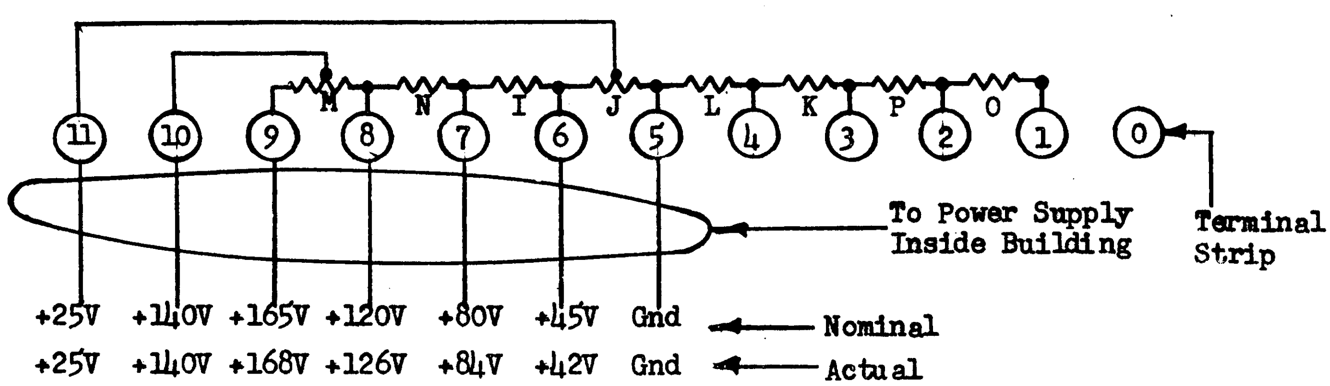
Resistance Load for ±165V:

PLAN DRAWING

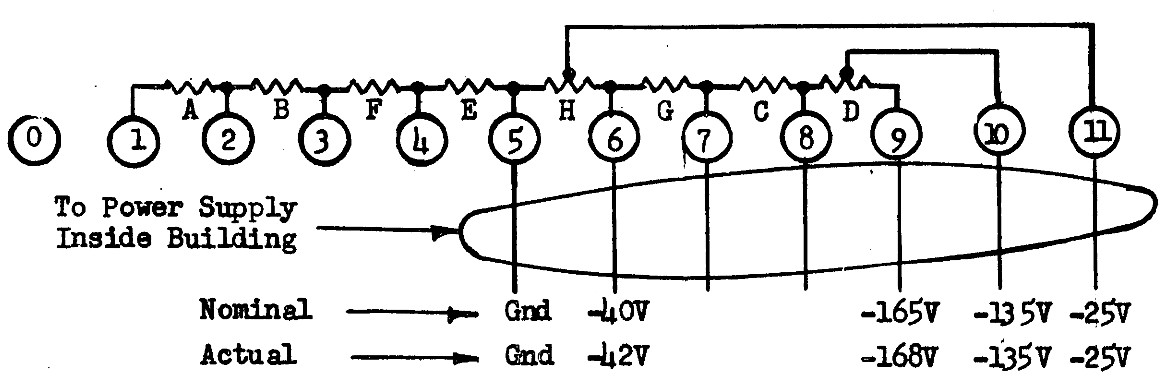


TOP VIEW

SCHEMATIC DRAWINGS



POSITIVE LOAD

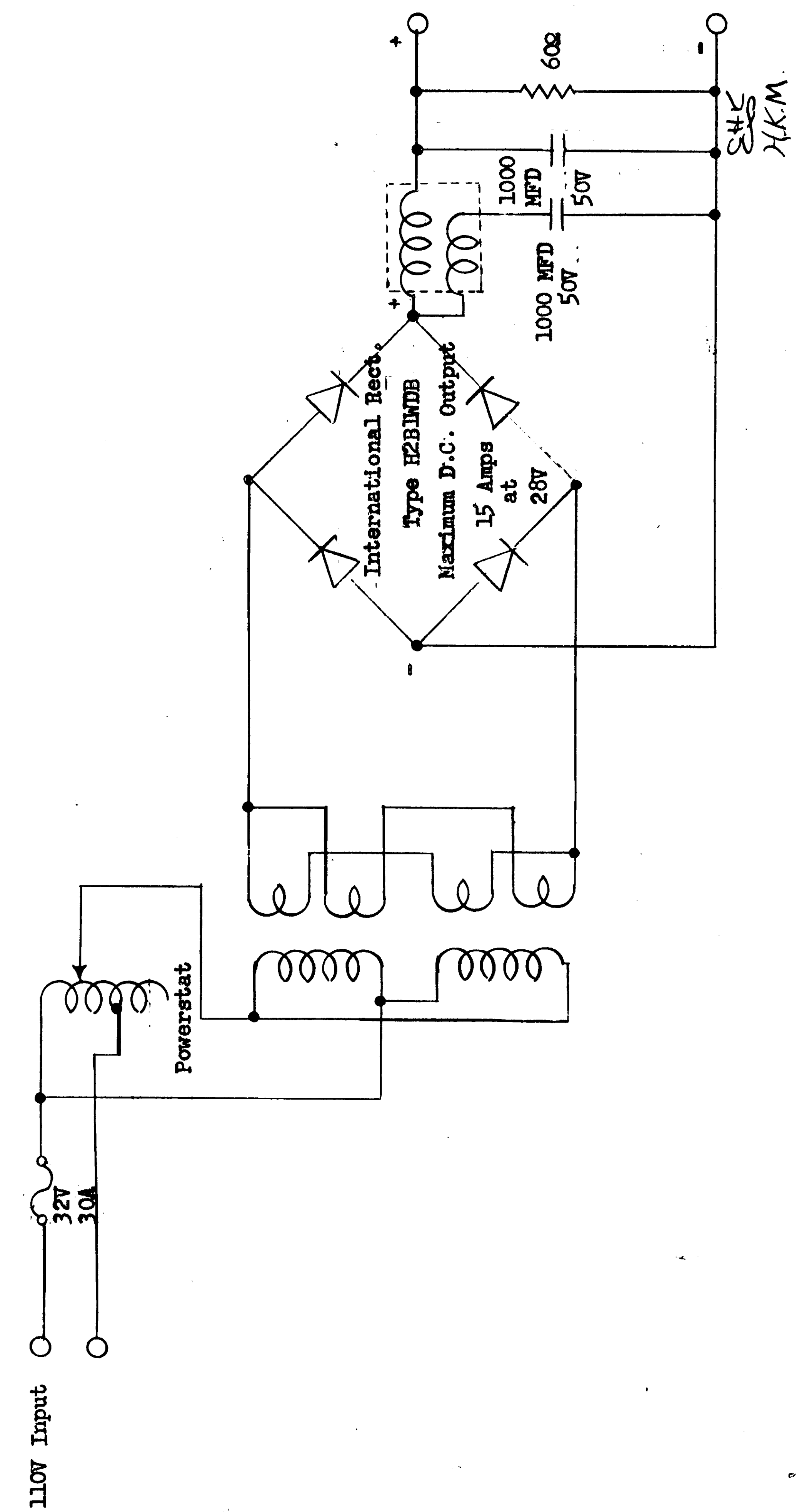


NEGATIVE LOAD

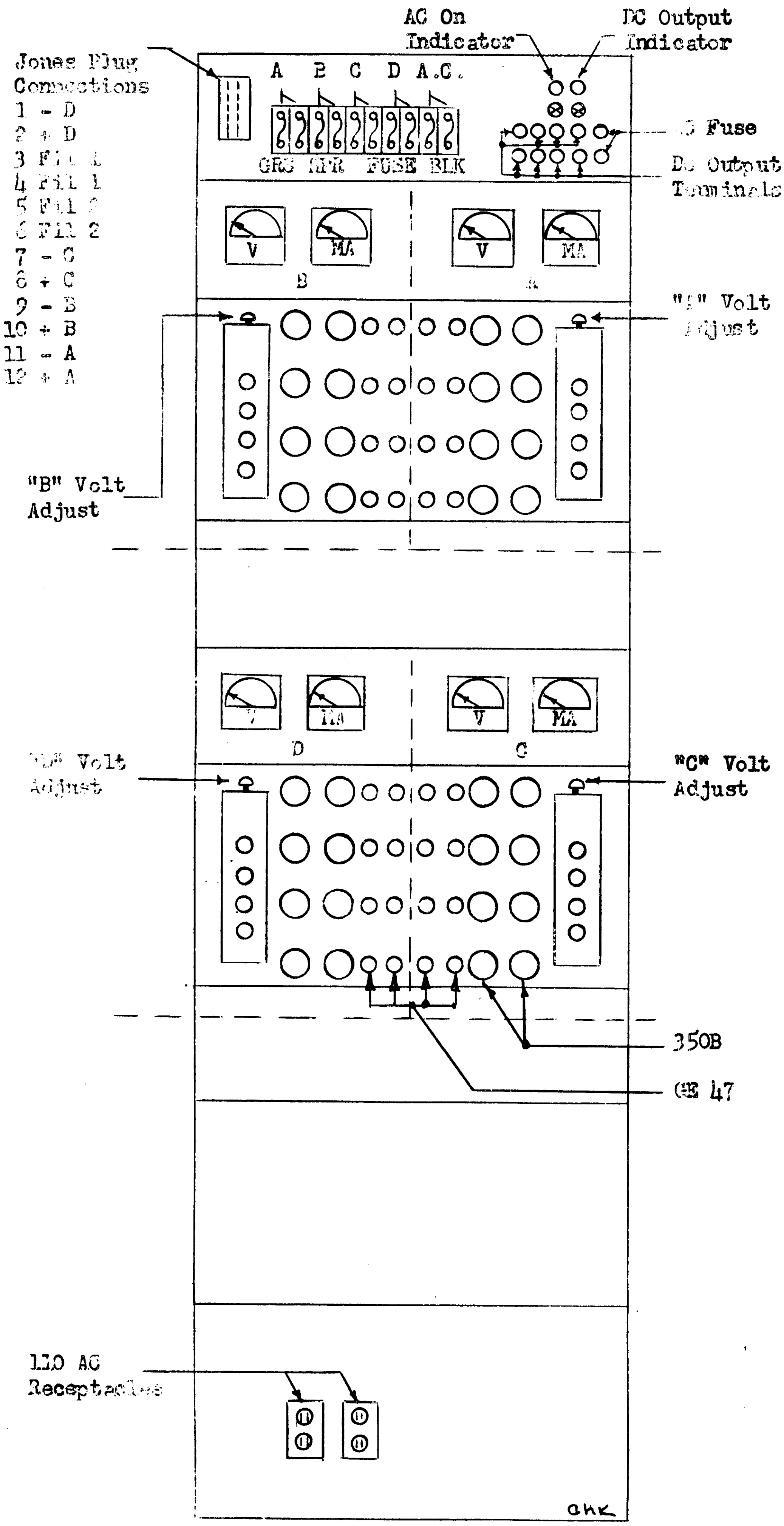
C.H.K.
EMR

7.1 Laboratory Power Supply.

-15V Power Supply:

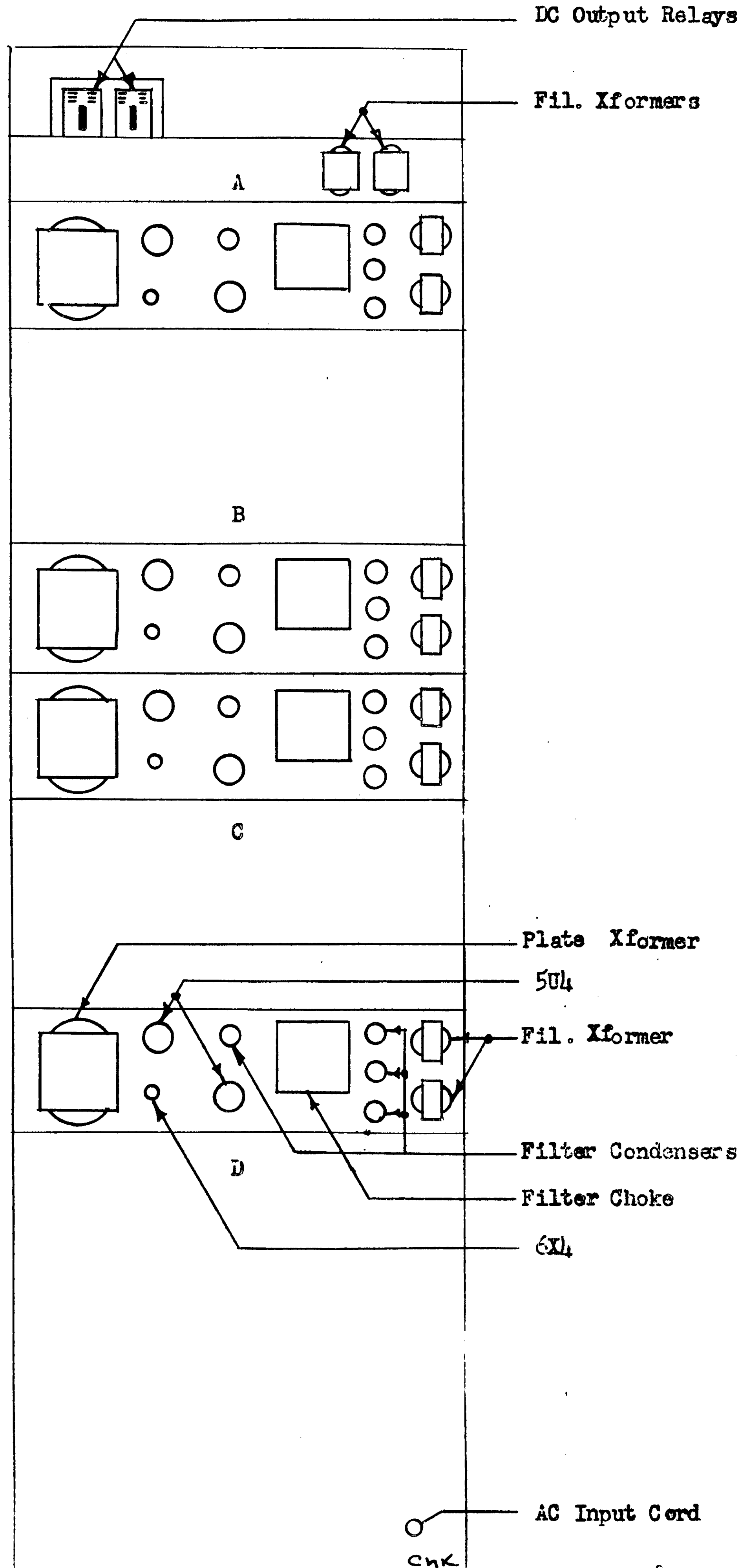


7.2 Regulated Laboratory Power Supply 1.



FRONT VIEW

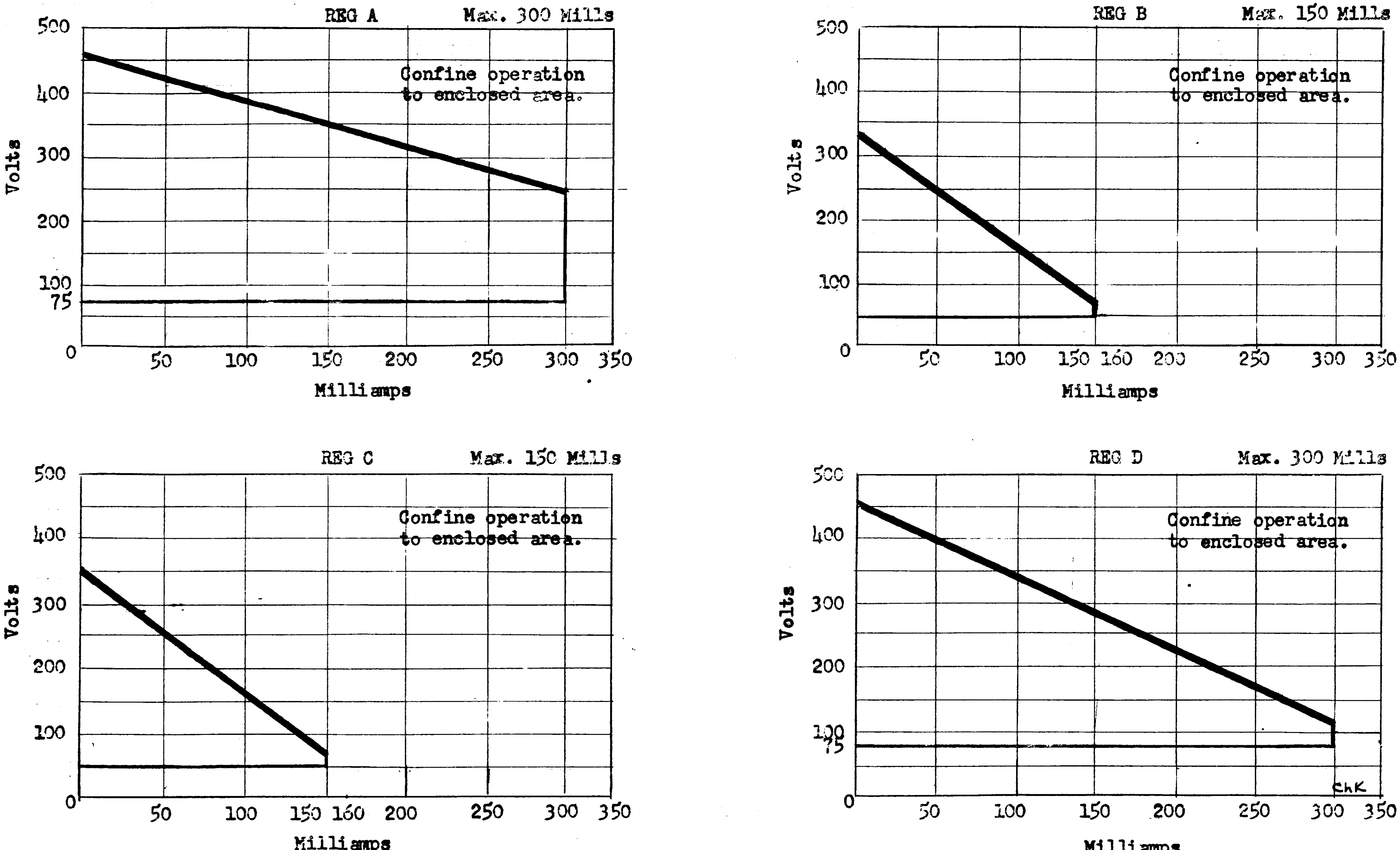
7.2 Regulated Laboratory Power Supply 1.



REAR VIEW

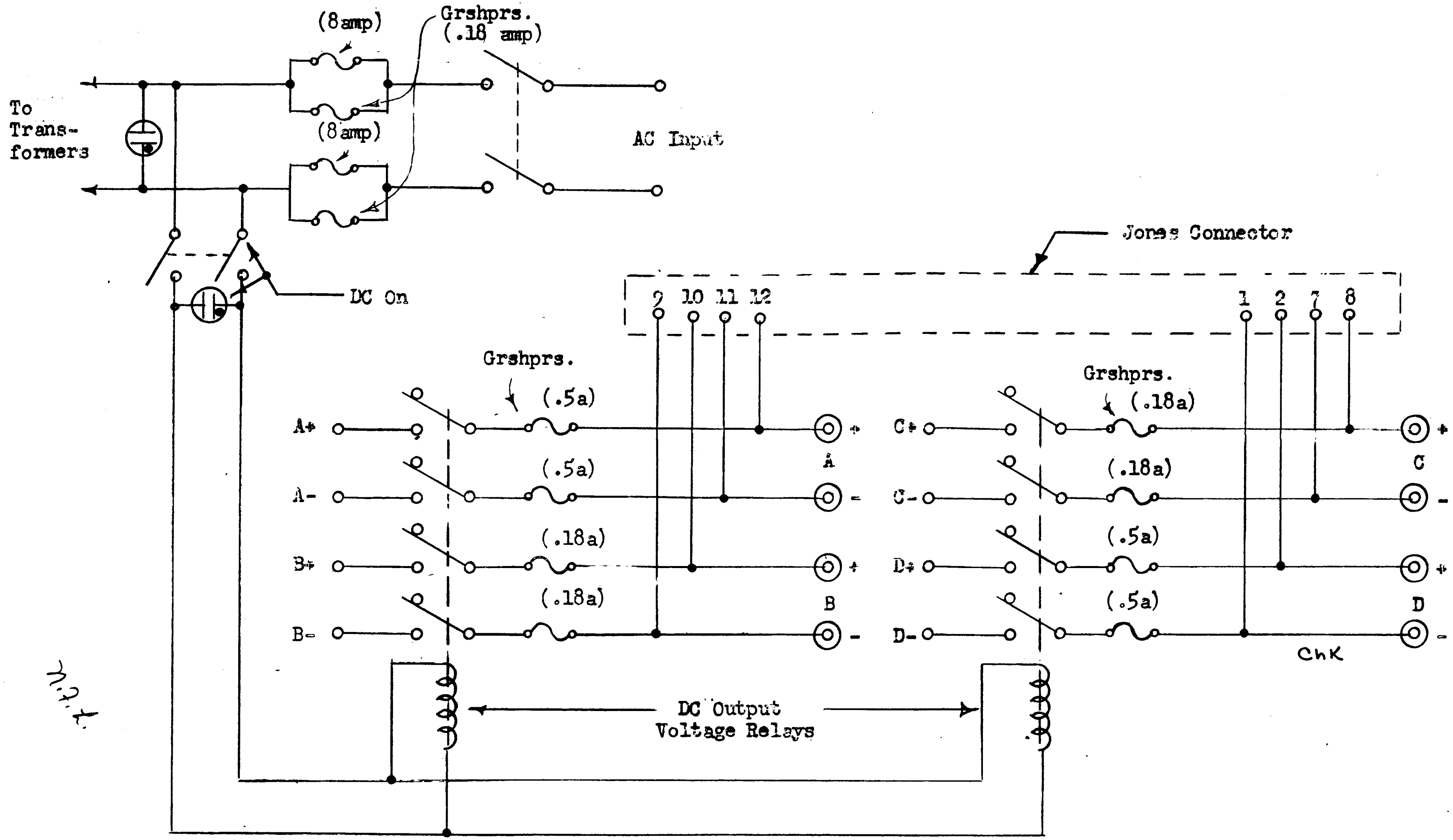
7.2 Regulated Laboratory Power Supply 1.

Regulator Curves:



REGULATOR CURVES

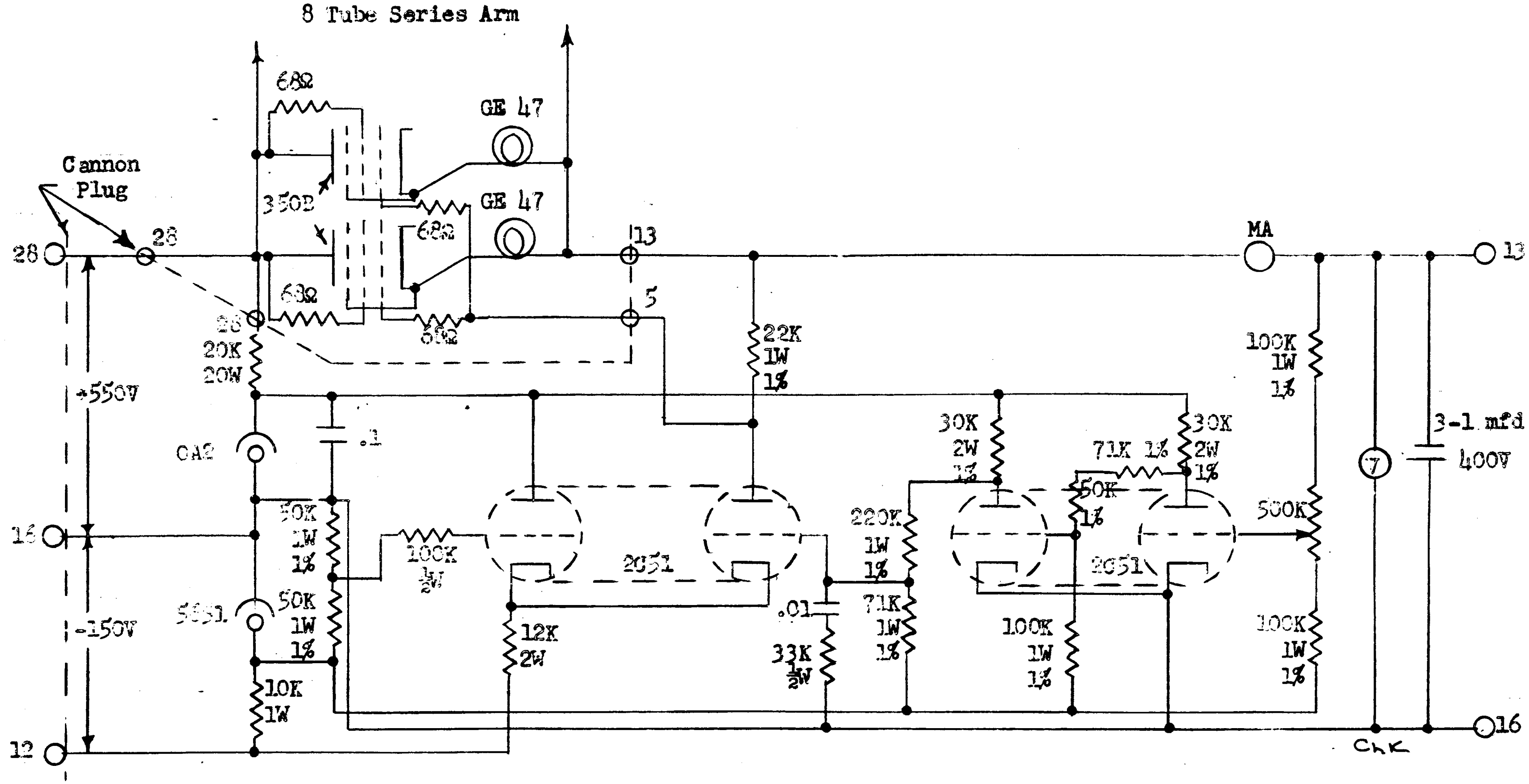
AC and DC Control Wiring:



AC AND DC CONTROL WIRING

7.2 Regulated Laboratory Power Supply 1.

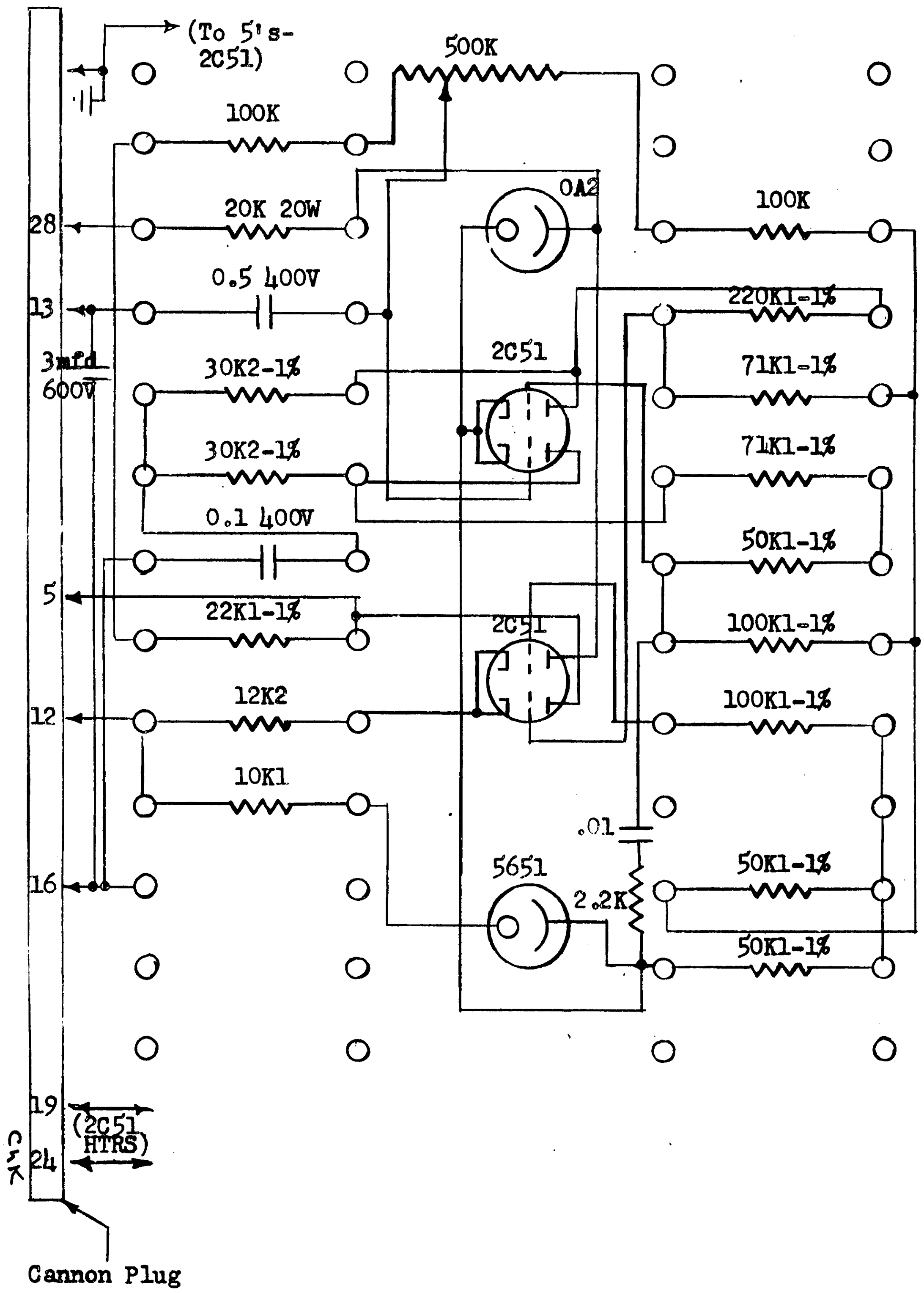
Amplifier for Variable Output Voltage Regulator (Schematic)



AMPLIFIER FOR VARIABLE OUTPUT VOLTAGE REGULATOR (Schematic)

7.2 Regulated Laboratory Power Supply 1.

Amplifier for Variable Output Voltage Regulator (Tagboard):



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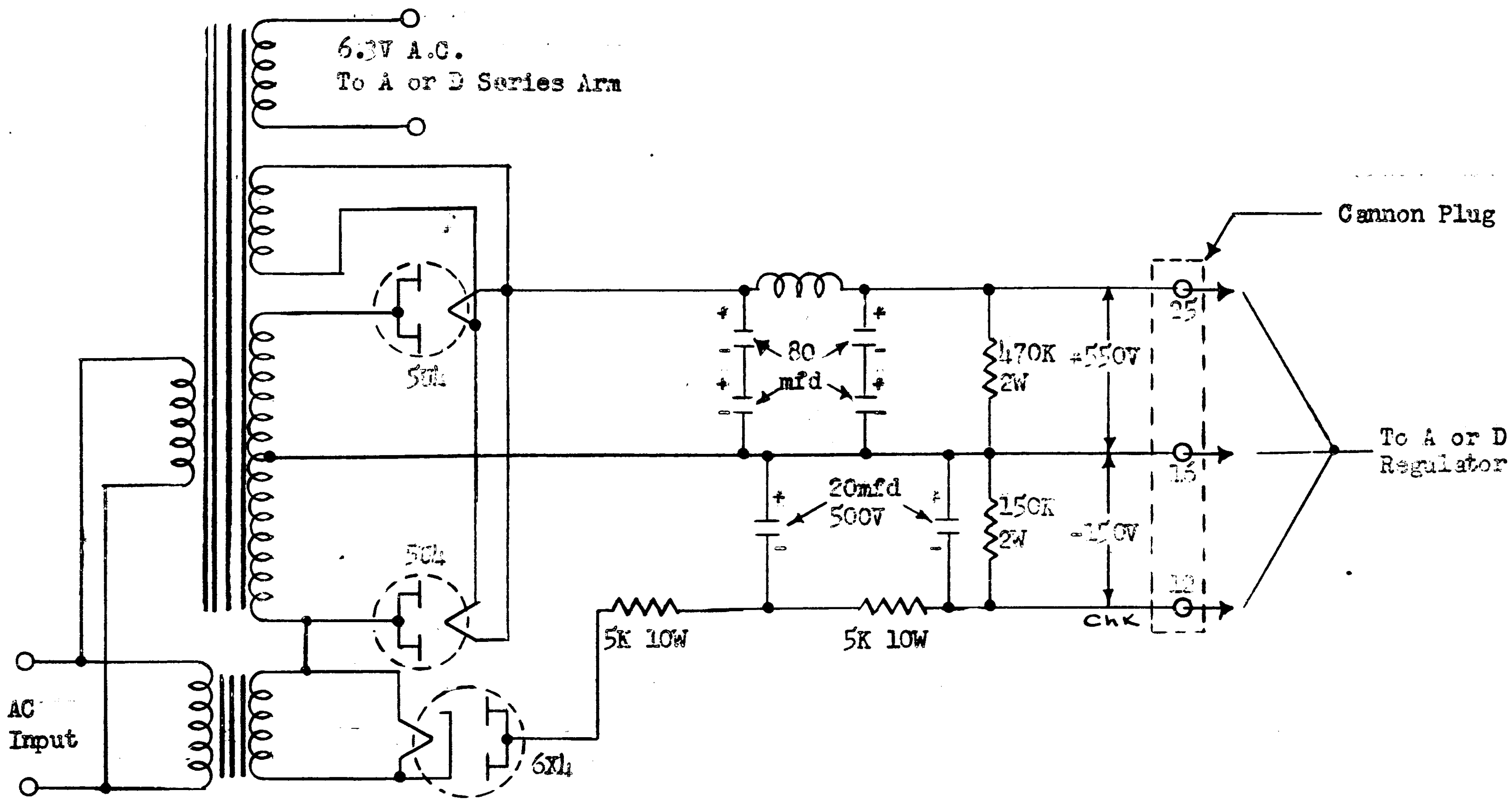
7.2 Regulated Laboratory Power Supply 1.

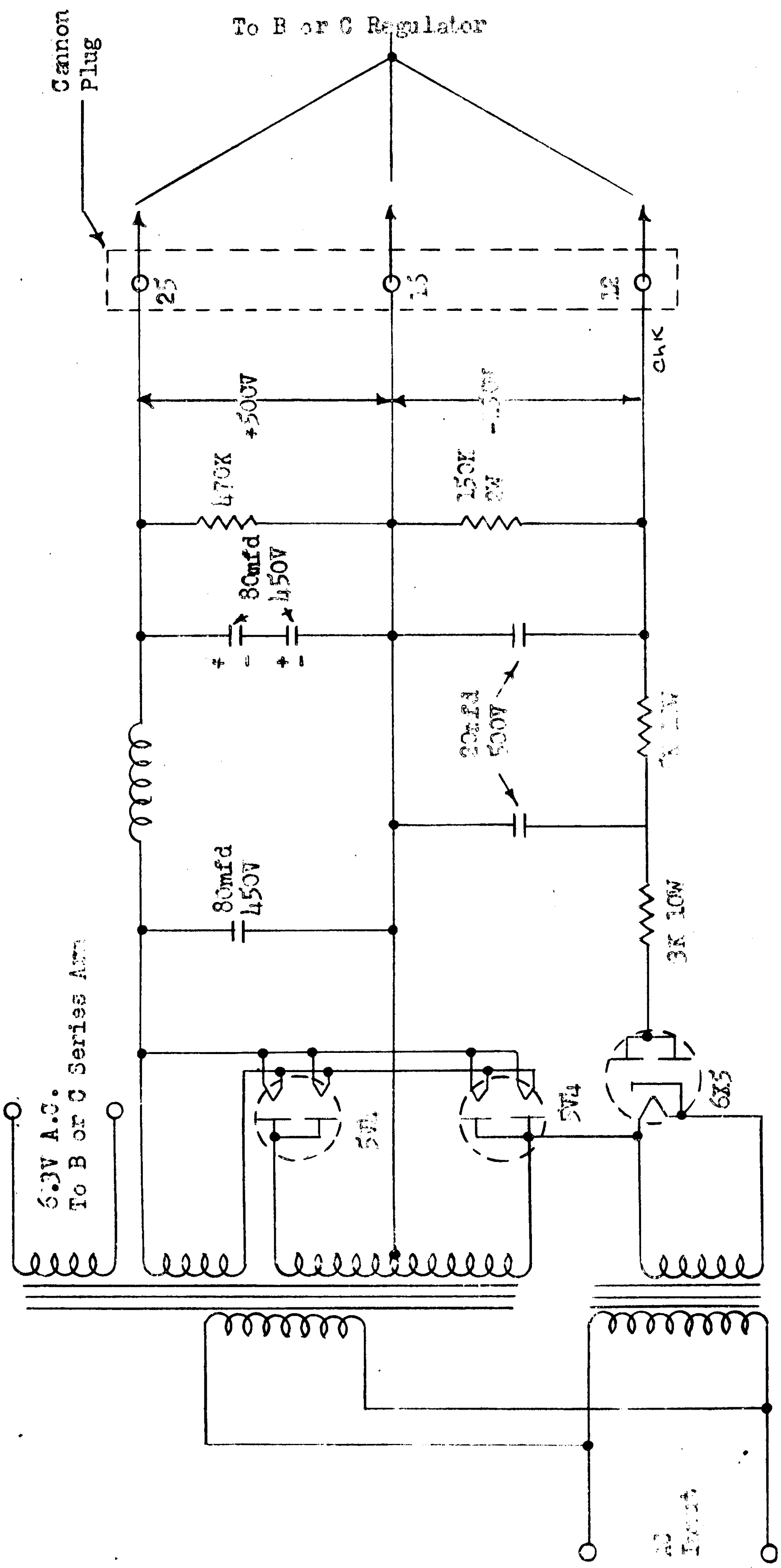
A and D Power Supply (Schematic):



A AND D POWER SUPPLY (Schematic)
(300 Ma)

7.2 Regulated Laboratory Power Supply 1.

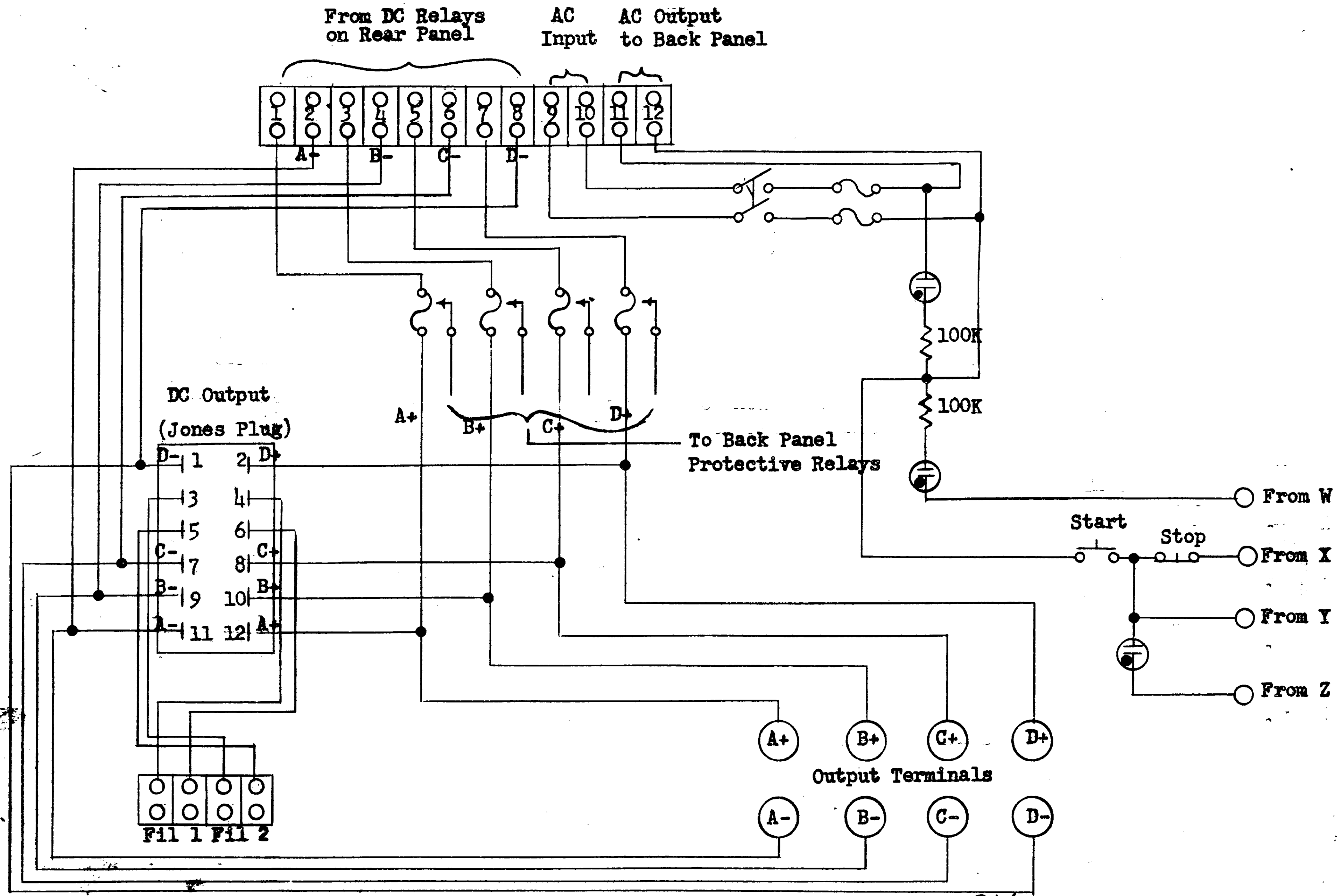
B and C Power Supply (Schematic):



B AND C POWER SUPPLY (Schematic)
(150 Ma)

7.3 Regulated Laboratory Power Supply 2.

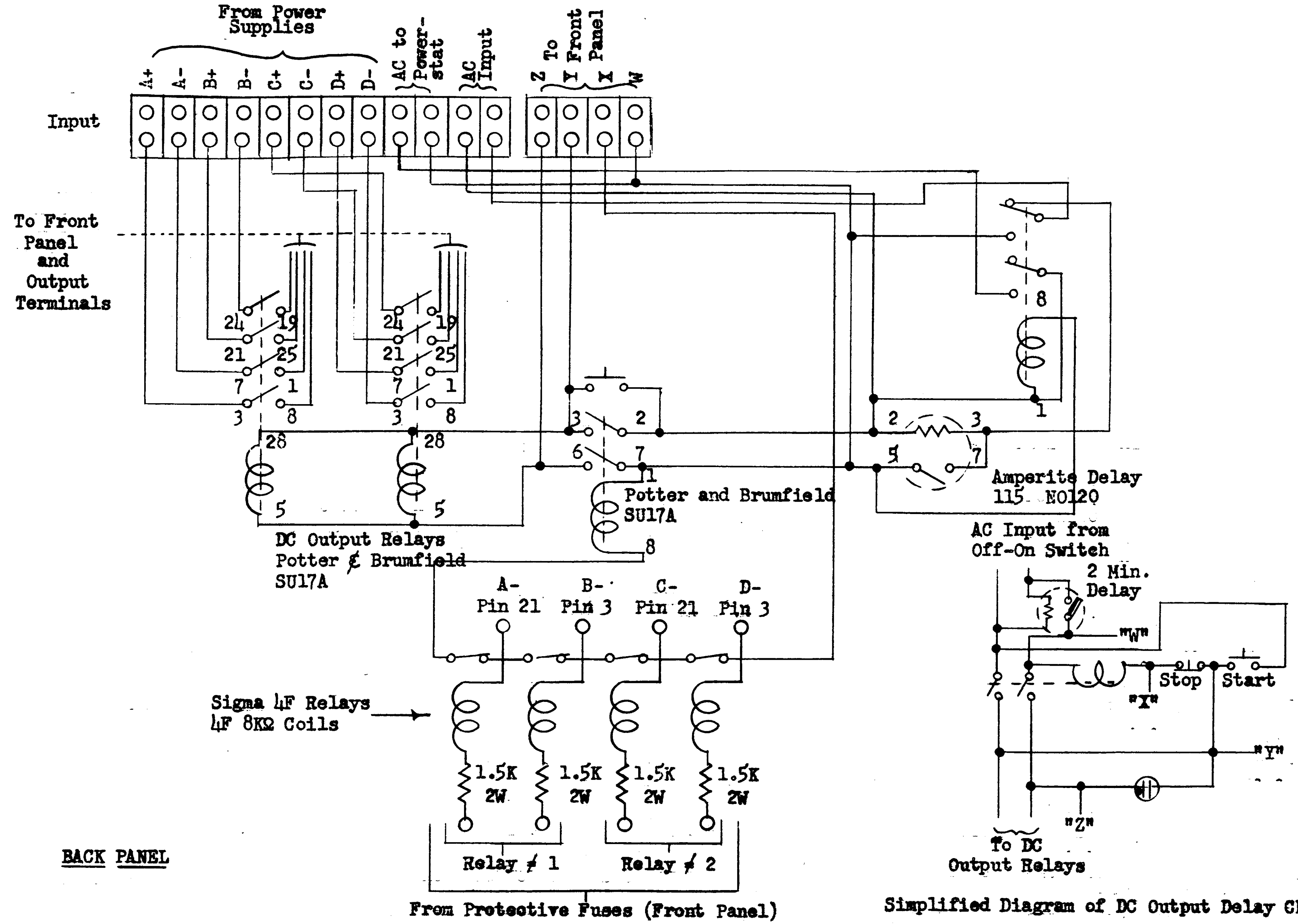
Front Panel:



FRONT PANEL

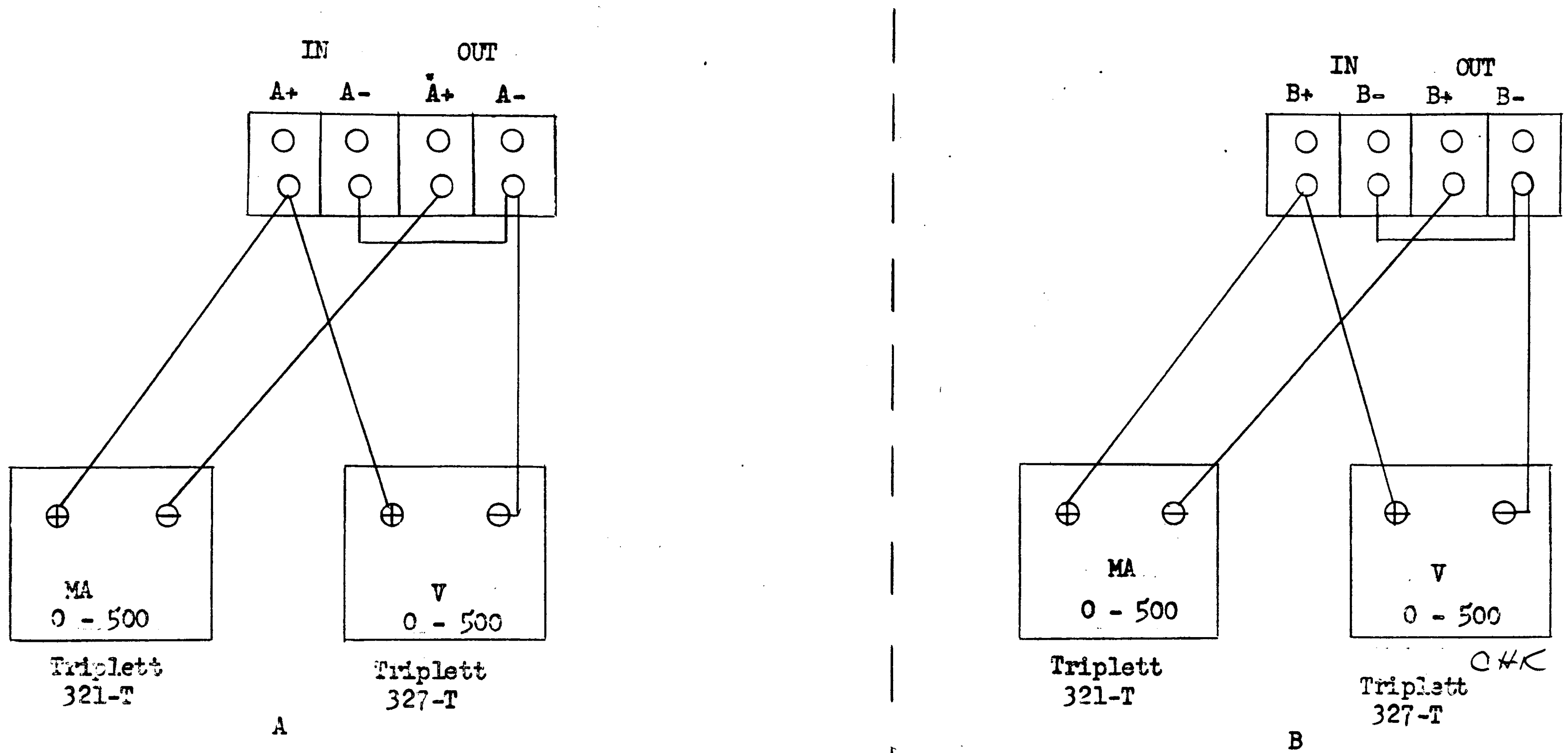
7.3 Regulated Laboratory Power Supply 2.

Back Panel:



Simplified Diagram of DC Output Delay Ckt.

Dwg. No. 2 - METER PANELS

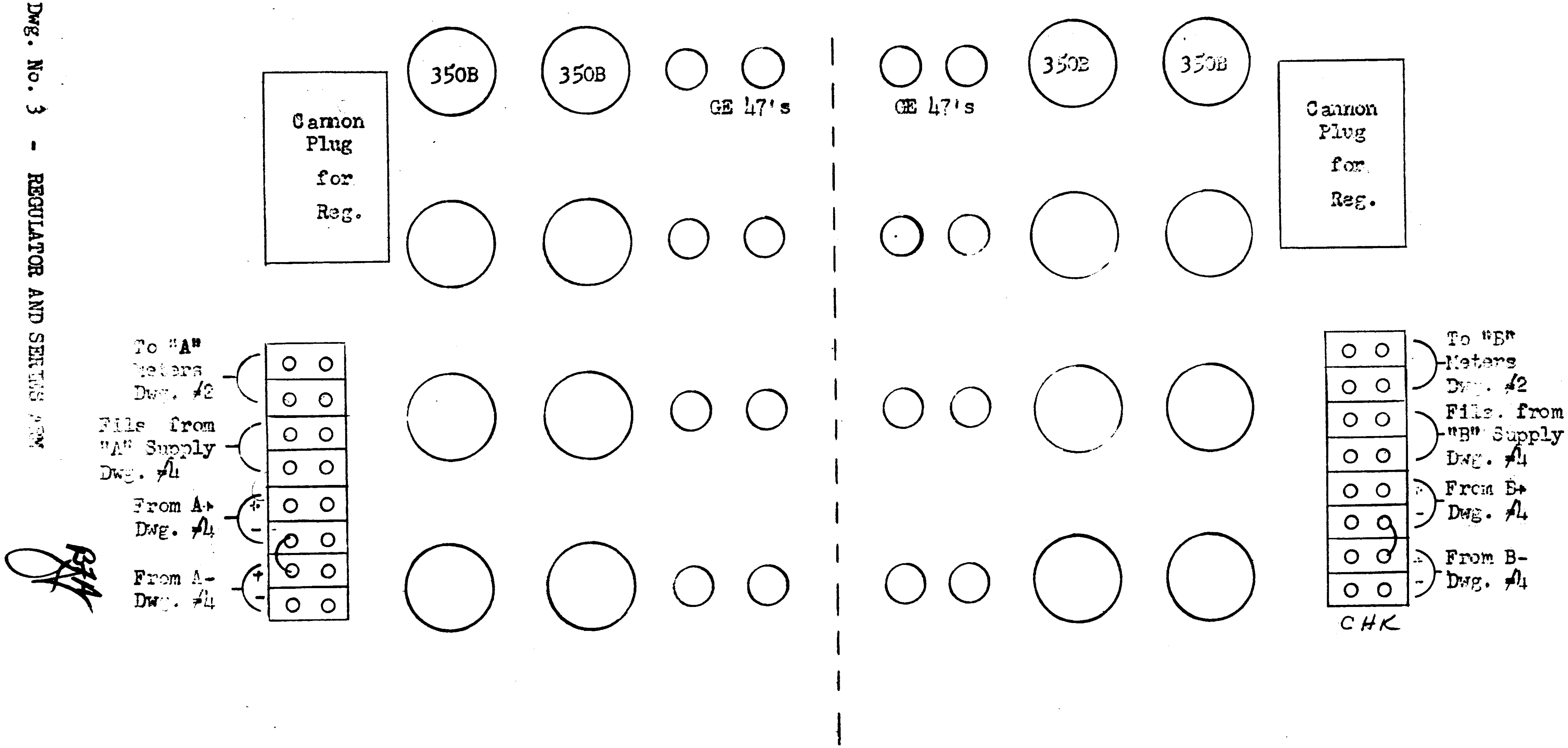


METER PANEL (make 2)

A+) A-) IN - FROM REGULATOR AND SERIES ARM DWG. NO. 3.

A+) A-) OUT - TO PROTECTIVE CIRCUIT 12 TERMINAL JONES STRIP DWG. NO. 1

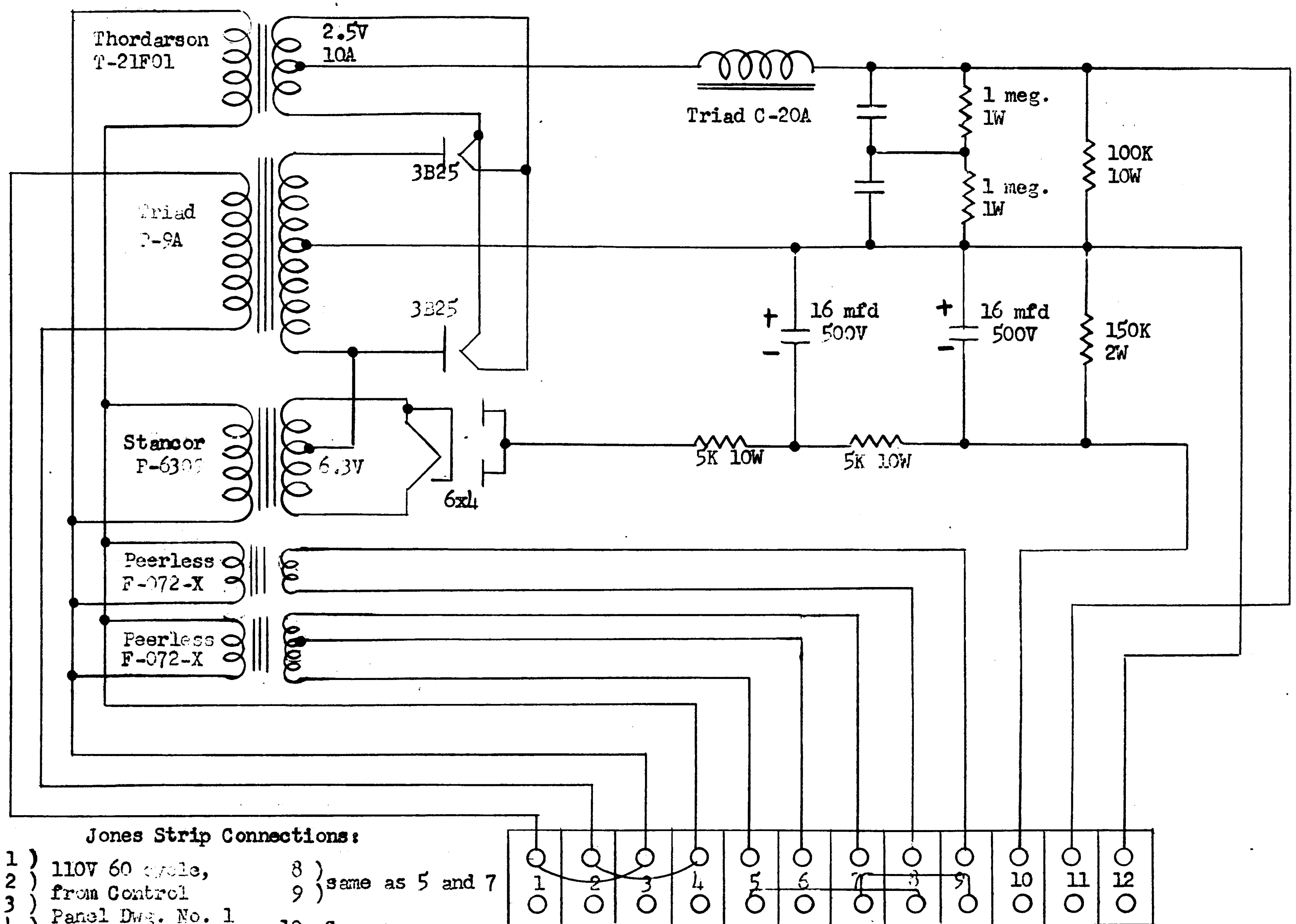
Dwg. No. 3 - REGULATOR AND SERIES ARM



REGULATOR AND SERIES ARM PANELS (make 2)

INPUT FROM A+, A-, B+, AND B- FROM RAW SUPPLY DWG. NO. 4.

7.3 <u>Regulated Laboratory Power Supply 2.</u>



Jones Strip Connections:

1) 110V 60 cycle,
2) from Control
3) Panel Dwg. No. 1
4)

5)
6) 6.3V a.c. CT
7) to Series Arm

8)
9) same as 5 and 7

10 Common

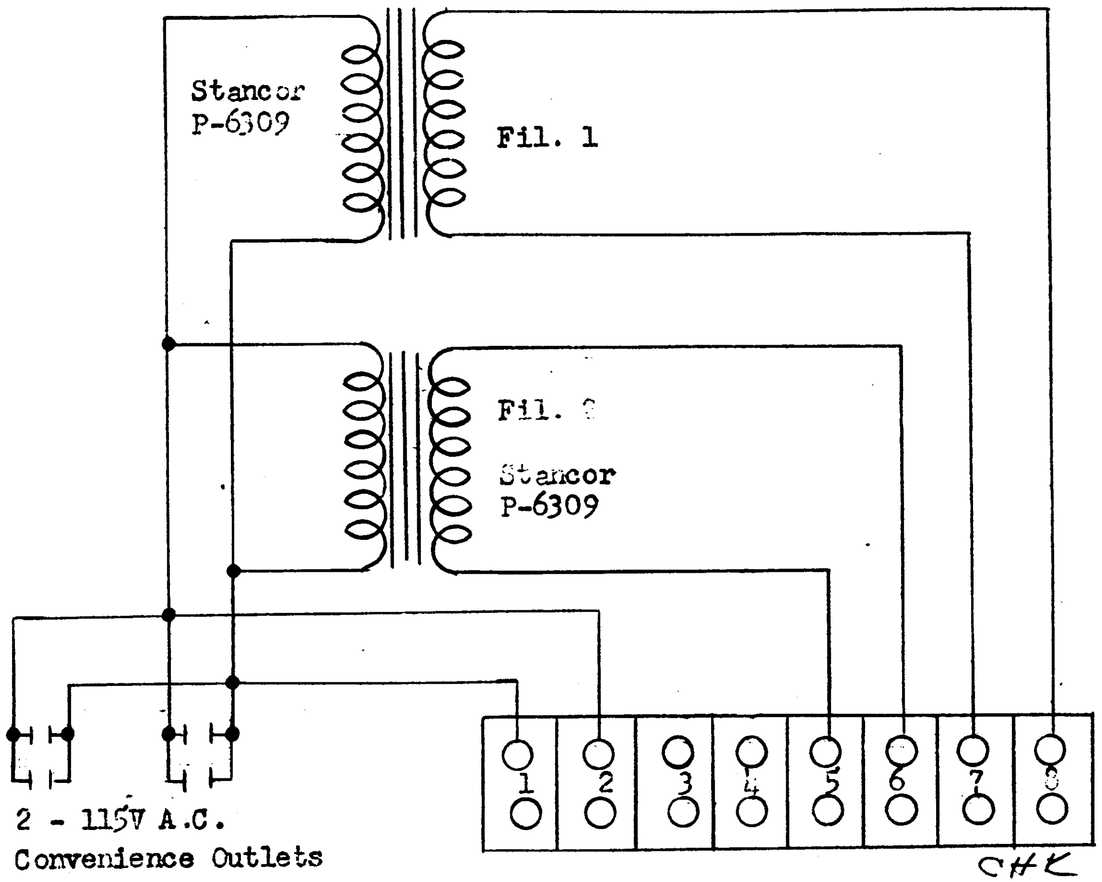
11 A+

12 A-

CHK

Dwg. No. 4 - POWER SUPPLY

7.3 Regulated Laboratory Power Supply 2.



Jones Strip Connections:

1)
2) From 115V Line.

3

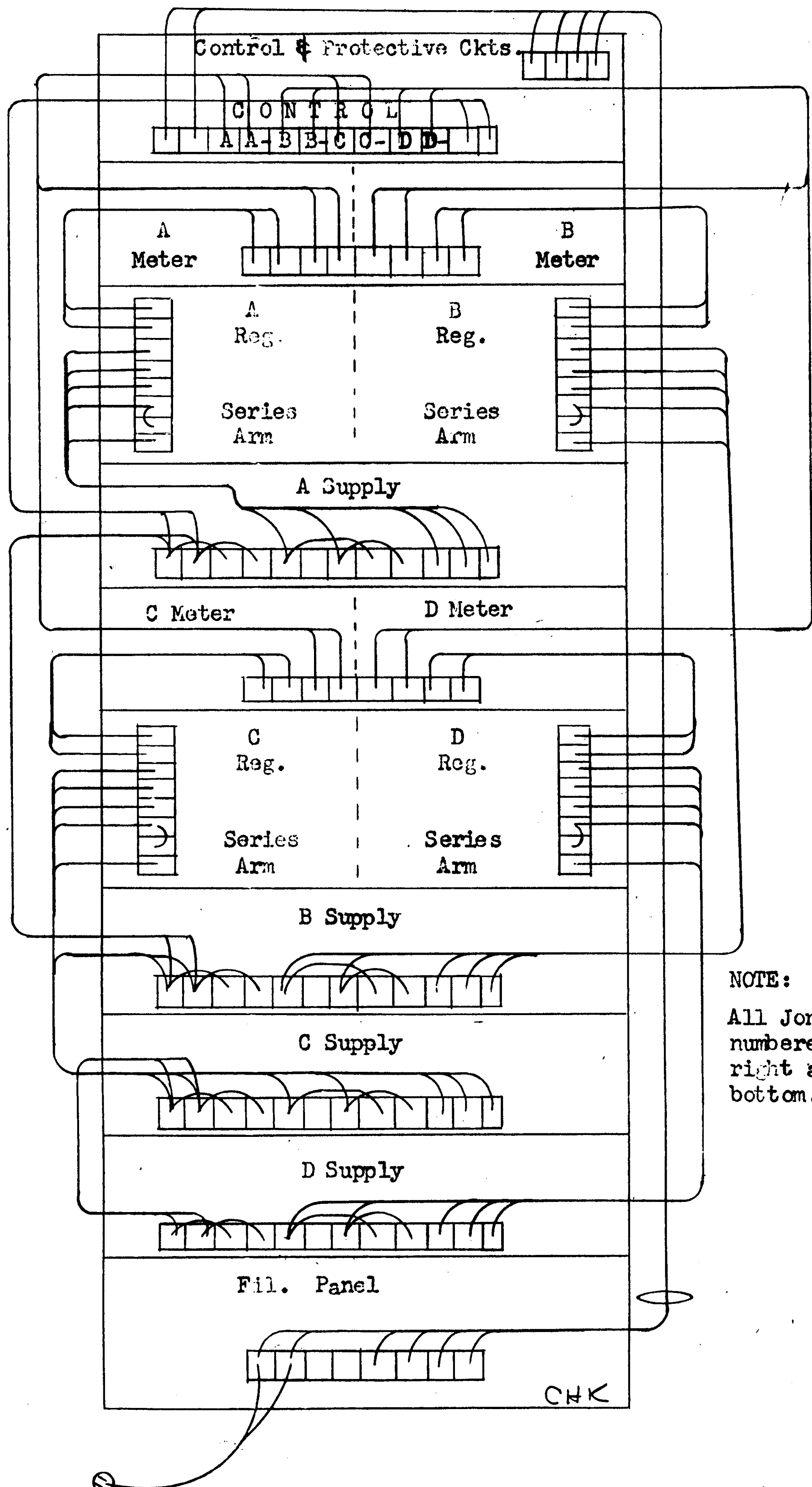
4

5)
6) 6.3V a.c. Fil. 1 to Control Dwg. No. 1.

7)
8) 6.3V a.c. Fil. 2 to Control Dwg. No. 1.

Dwg. No. 5 - FIL. PANEL

7.3 Regulated Laboratory Power Supply 2.



NOTE:
All Jones Strips numbered left to right and top to bottom.

BJA

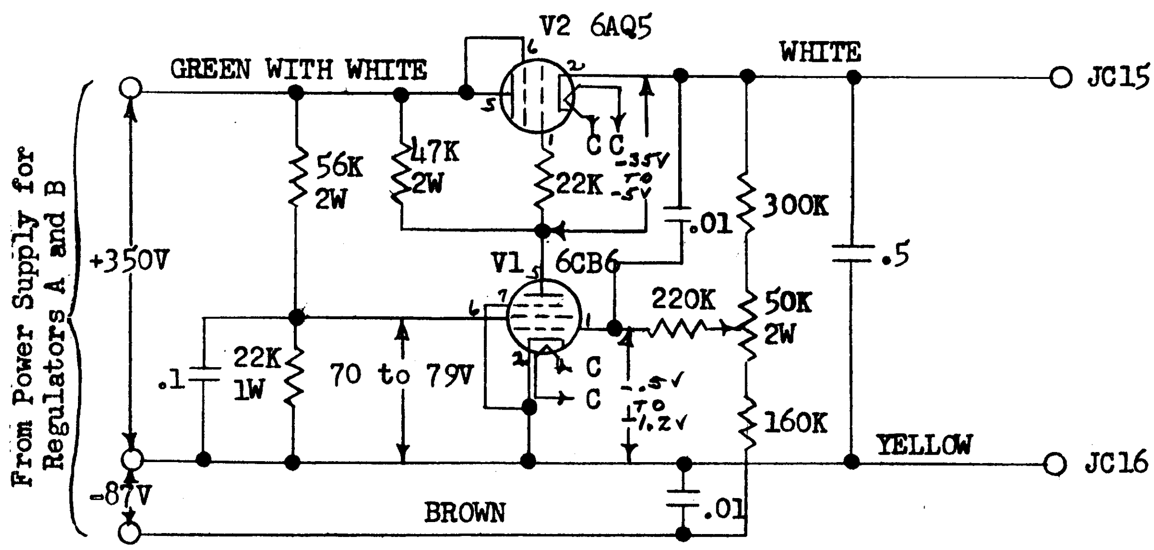
Dwg. No. 6 - CABLE DIAGRAM - FRONT VIEW

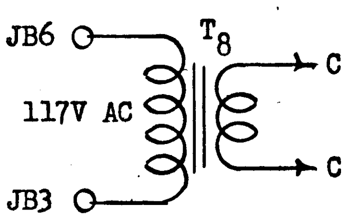
7.4 Regulated Laboratory Power Supply 3
<u>High Voltage Supply for CRT Memory Test Unit.</u>

Schematic Diagrams for Regulator A and Regulator B:

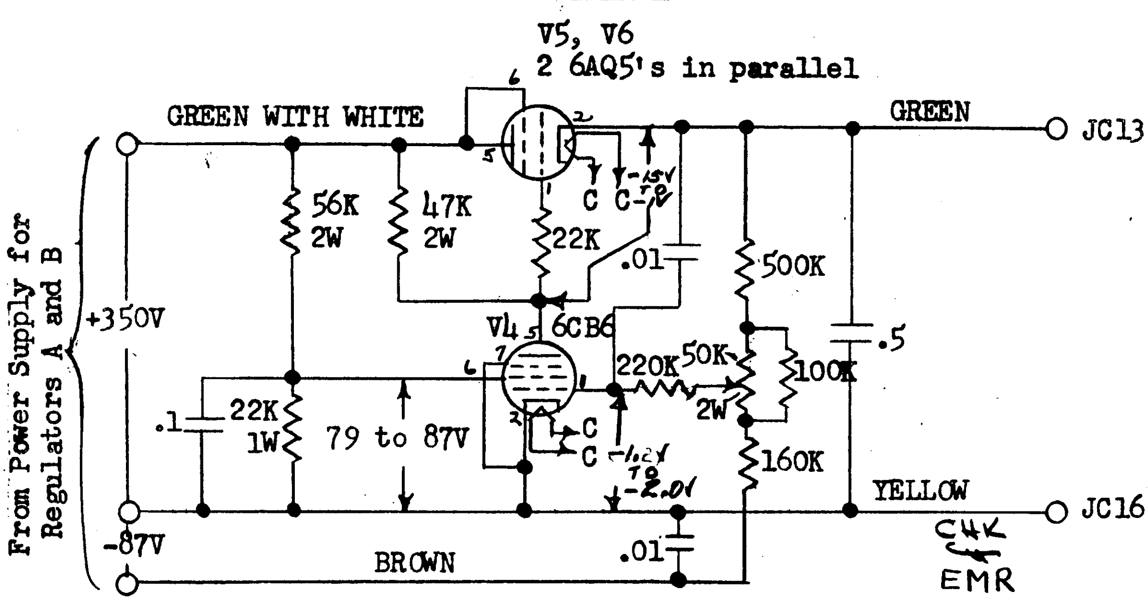
REGULATOR A (+125 to +175V)

V3 not used



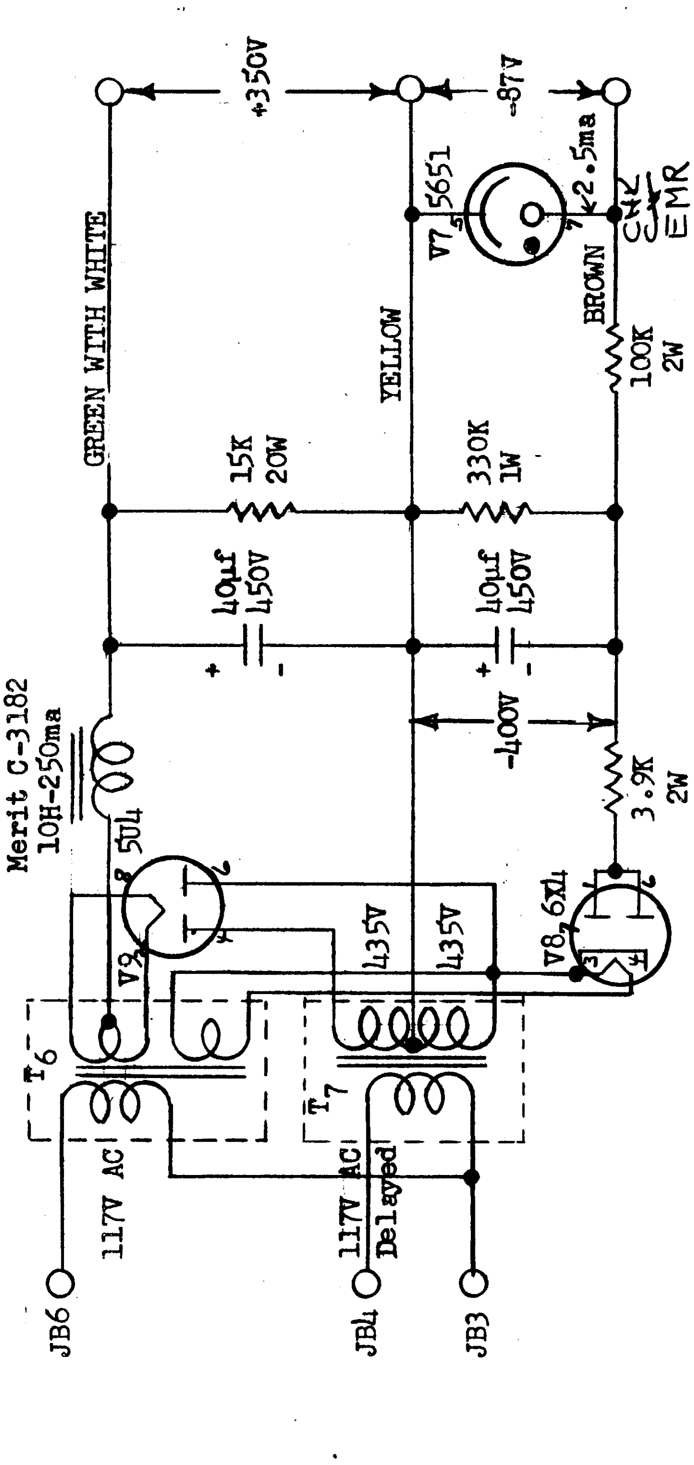


REGULATOR B (+225 to +275V)



7.4 Regulated Laboratory Power Supply 3
High Voltage Supply for CRT Memory Test Unit.

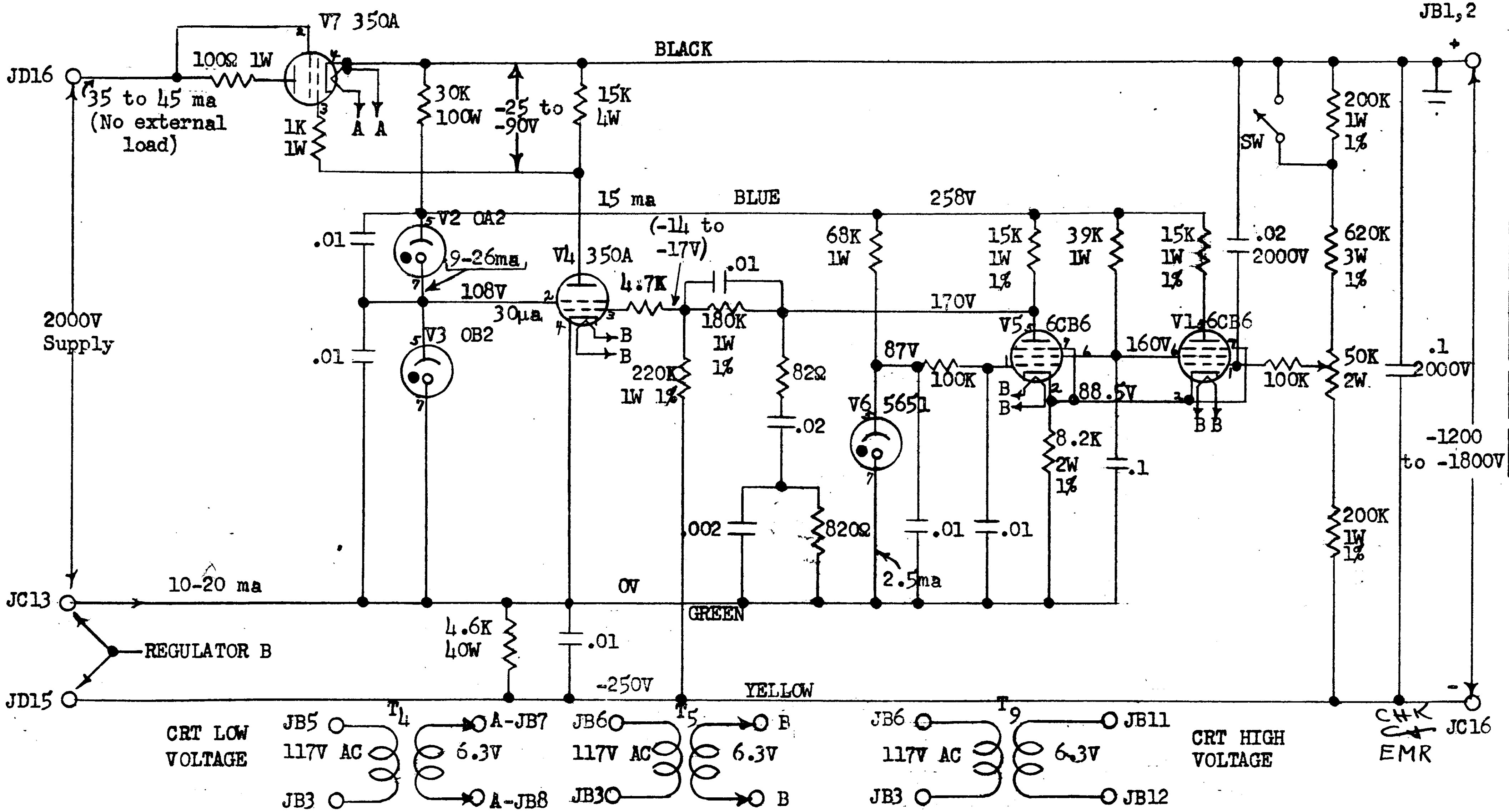
Power Supply for Regulators A and B (350V - 150ma):



7.4 Regulated Laboratory Power Supply 3
<u>High Voltage Supply for CRT Memory Test Unit.</u>

NOTES: 1) All voltages referred to green wire as 0V unless otherwise noted.

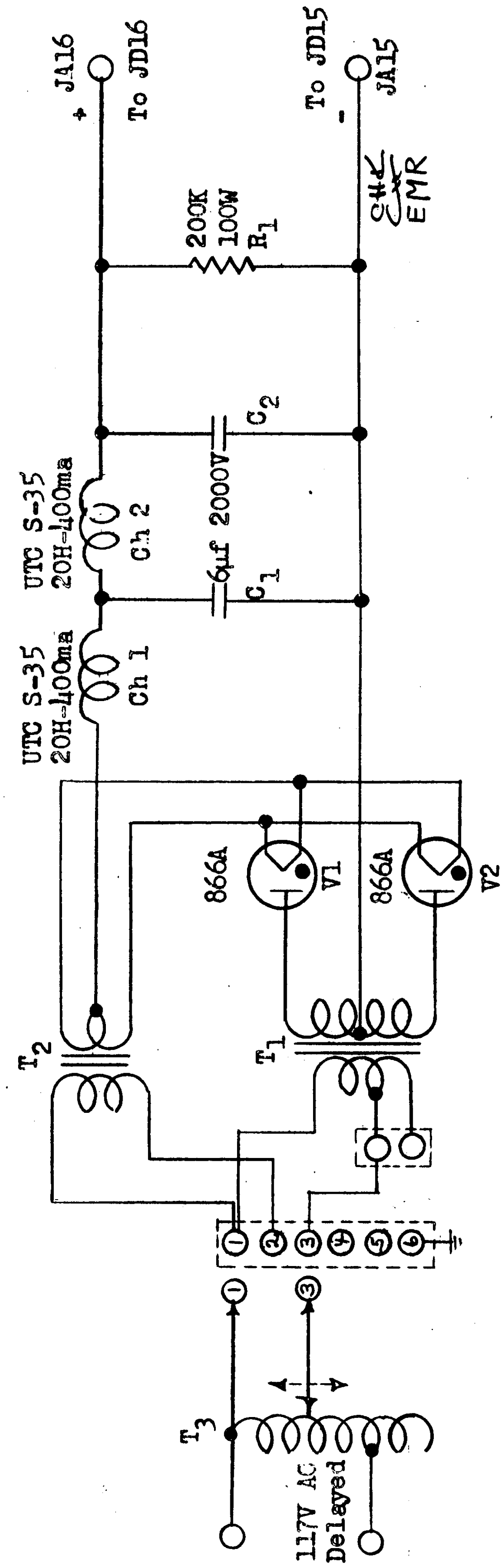
2) SW Open: Output = -1470 to -1800V SW Closed: Output = -1200 to -1490V



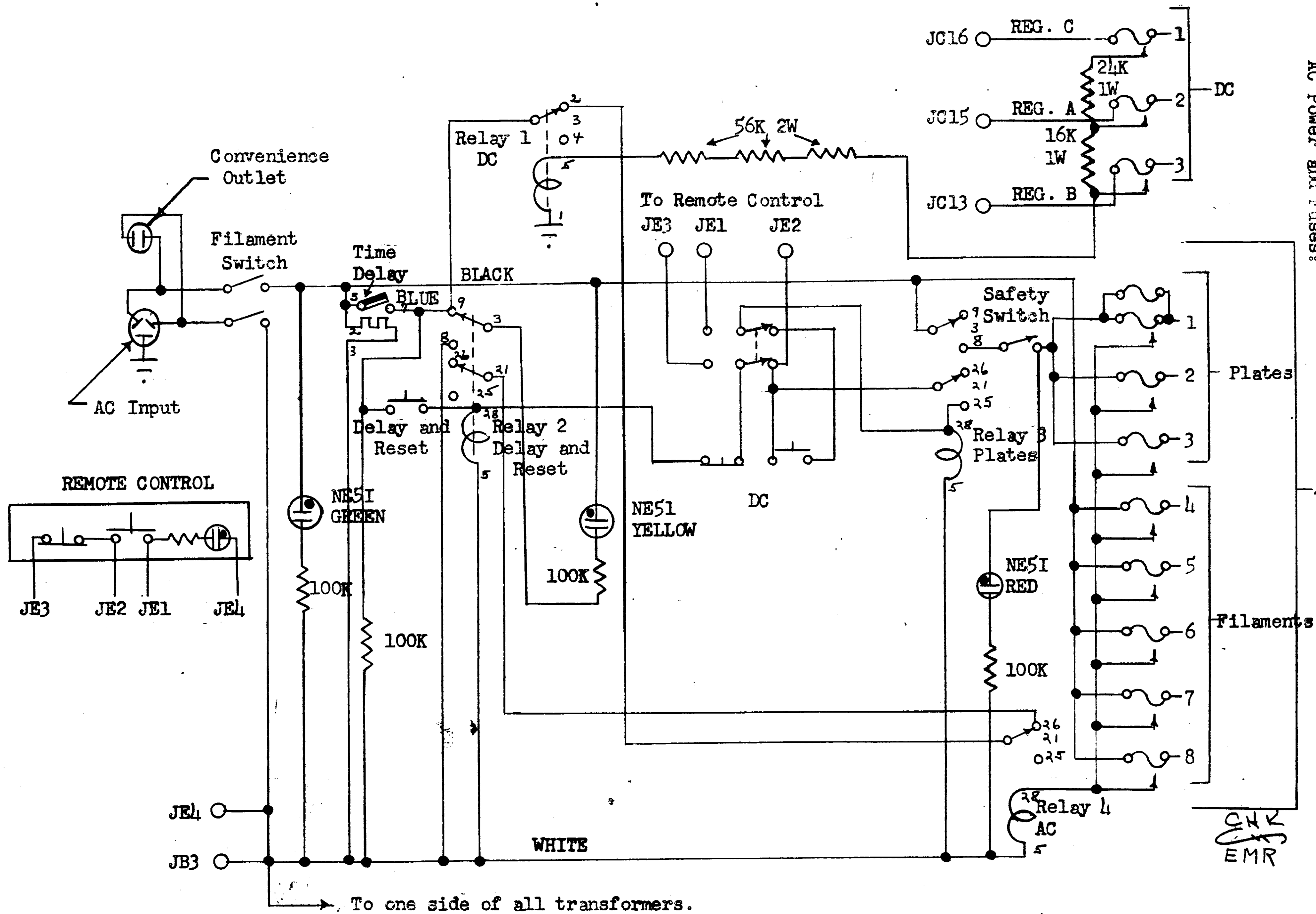
<u>SCHEMATIC DIAGRAM FOR REGULATOR C</u> (-1200 to -1800V)

7.4 Regulated Laboratory Power Supply 3
High Voltage Supply for CRT Memory Test Unit.

Power Supply for Regulator C (2000V - 300ma):



7.4 Regulated Laboratory Power Supply 3
<u>High Voltage Supply for CRT Memory Test Unit.</u>
Schematic Diagram for AC Power and Fuses.



7.4 Regulated Laboratory Power Supply 3
High Voltage Supply for CRT Memory Test Unit.

Fuse Schedule and Transformer and Plug Layout:

FUSE SCHEDULE

D. C. Fuses

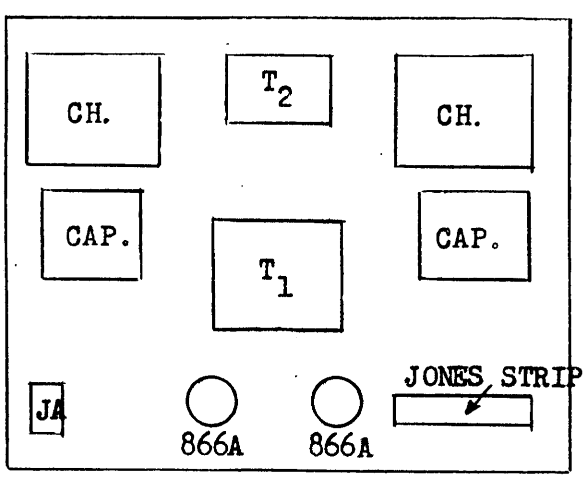
1. .180A - REG. C (-1200 to -1800V)
2. .180A - REG. C + REG. A (REG. A = +125 to +175V)
3. .180A - REG. C + REG. B (REG. B = +225 to +275V)

A. C. Fuses

1. 8A + .180A H.V. Plates T_1, T_3
2. 3A L.V. Plates T_7
3.
4. 1.3A H.V. Filaments T_2
5. 1.3A L.V. Filaments T_4
6. 1.3A L.V. Filaments T_5, T_6, T_8, T_9

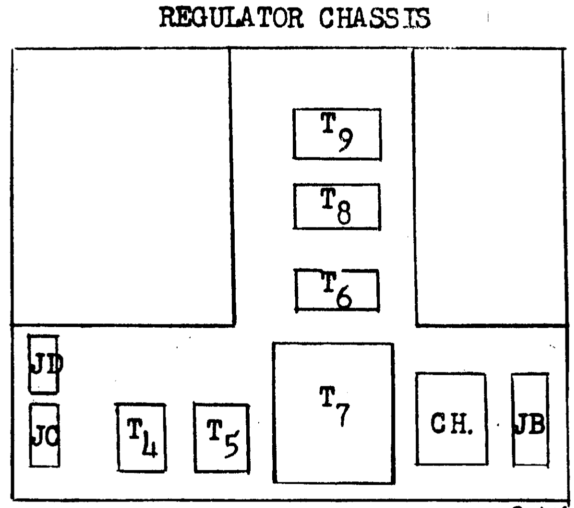
TRANSFORMER AND PLUG LAYOUT

POWER SUPPLY CHASSIS



TOP VIEW

REGULATOR CHASSIS



TOP VIEW

NOTE: Plug JE is located on side of Test Rack near AC Input.

7.4 Regulated Laboratory Power Supply 3 High Voltage Supply for CRT Memory Test Unit.

Transformer and Relay Schedule:

T_1 MERIT P-3168

PRIMARY
- Common - Black
- Low - Green
- High - Brown

SECONDARY
- Low Primary - 3600V CT
- High Primary- 4200V CT

T_2 STANCOR P-3060, 10 KV Insulation

PRIMARY - Black

SECONDARY - 2.5V, 10A

T_3 POWERSTAT 116

PRIMARY - 1KV, 7½A

T_4 MERIT P-2948, 2.5KV Insulation

PRIMARY - Black

SECONDARY - 6.3V, 10A Green-Green Yellow

T_5 STANCOR P-4019, 2.5KV Insulation

PRIMARY
- Common - Black
- 117V - Black Red
- 107V - Black Yellow

SECONDARY
- 6.3V, 4A CT, Green-Green(2 wires)

T_6 MERIT P-3041, 2.5KV Insulation

PRIMARY - Black

SECONDARY
- 6.3V, 3.6A CT, Green-Green Yellow
- 5V, 3A, Yellow-Red Yellow

T_7 MERIT P-3156

PRIMARY - Black

SECONDARY

870V, 250ma CT	Red-Red Yellow
80V Bias Tap	Red
6.3V, 3A CT	Green-Green Yellow
6.3V, 3A	Blue
5V, 3A	Orange
5V, 3A	Yellow
2.5V, 10A	Brown

T_8 MERIT P-2946, 2.5KV Insulation

PRIMARY - Black

SECONDARY - 6.3V, 3A CT, Green-Yellow

T_9 Same as T_8

RELAY 1 SIGMA 4A-2500G

Coil: Resistance - 2500Ω
Current
- Maximum - 20ma
- Operate - 4.0ma
- Release - 3.9ma

Contacts: 2A - 115V AC Non-Inductive

RELAY 2 POTTER and BRUMFIELD SU17A

Coil: 2W, 110V - 100ma, 50 to 60cps
Voltage
- Maximum - 100V
- Operate - 80V
- Release - 70V

Contacts: 4A - 110V AC Non-Inductive

RELAY 3 - same as Relay 2

RELAY 4 - same as Relay 2

EMR

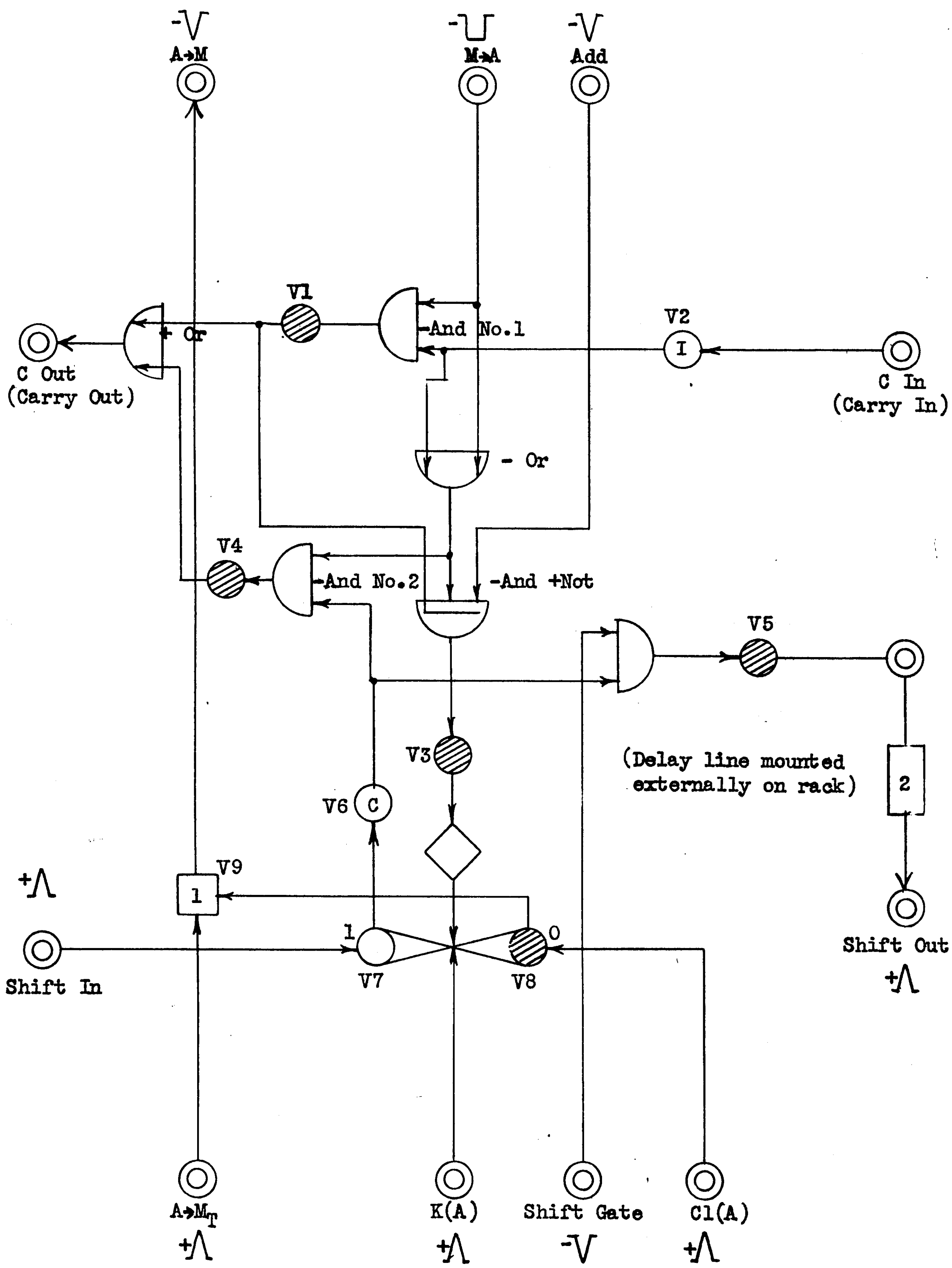
COMPARISON OF VARIOUS CHARACTERISTICS OF DCC AND BOC WITH BTS AND WITH APPLICABLE SPECIFICATIONS FIGURES SHOWN ARE AVERAGES *

Value	40°C Load Life 500 hrs.				70°C Load Life 200 hrs.				125°C Half Load 300 hrs	Humidity Bell Lab.			
	BTS	DDC	Mil Spec.	BOC	BTS	DCC	Mil Spec	BOC	DCC	BTS	DDC	Mil Spec	BOC
100 ohms	±1.8	-0.5	1.0	+0.1	±1.9	.2	3.0	.1	.3	+1.9	+0.6	5.0	+1.6
1,000 ohms	±1.4	-0.5	1.0	+0.2	+2.5	.2	3.0	.1	—	+1.3	+1	5.0	+1.7
10,000 ohms	-2.9	-0.5	1.0	+0.4	-3.6	.3	3.0	.1	.3	+2.8	+1	5.0	+1.8
100,000 ohms	±2.6	-0.5	1.0	+0.4	±1.9	.8	3.0	.6	.32	+2.9	+1	5.0	+1.9
500 K	—	-.8	1.0	0.8	—		3.0	.8		—	+1	5.0	+2
1 meg.	-1.8	-1.0			-2.8	1.4	3.0		9.7	+4.6	+2	5.0	—

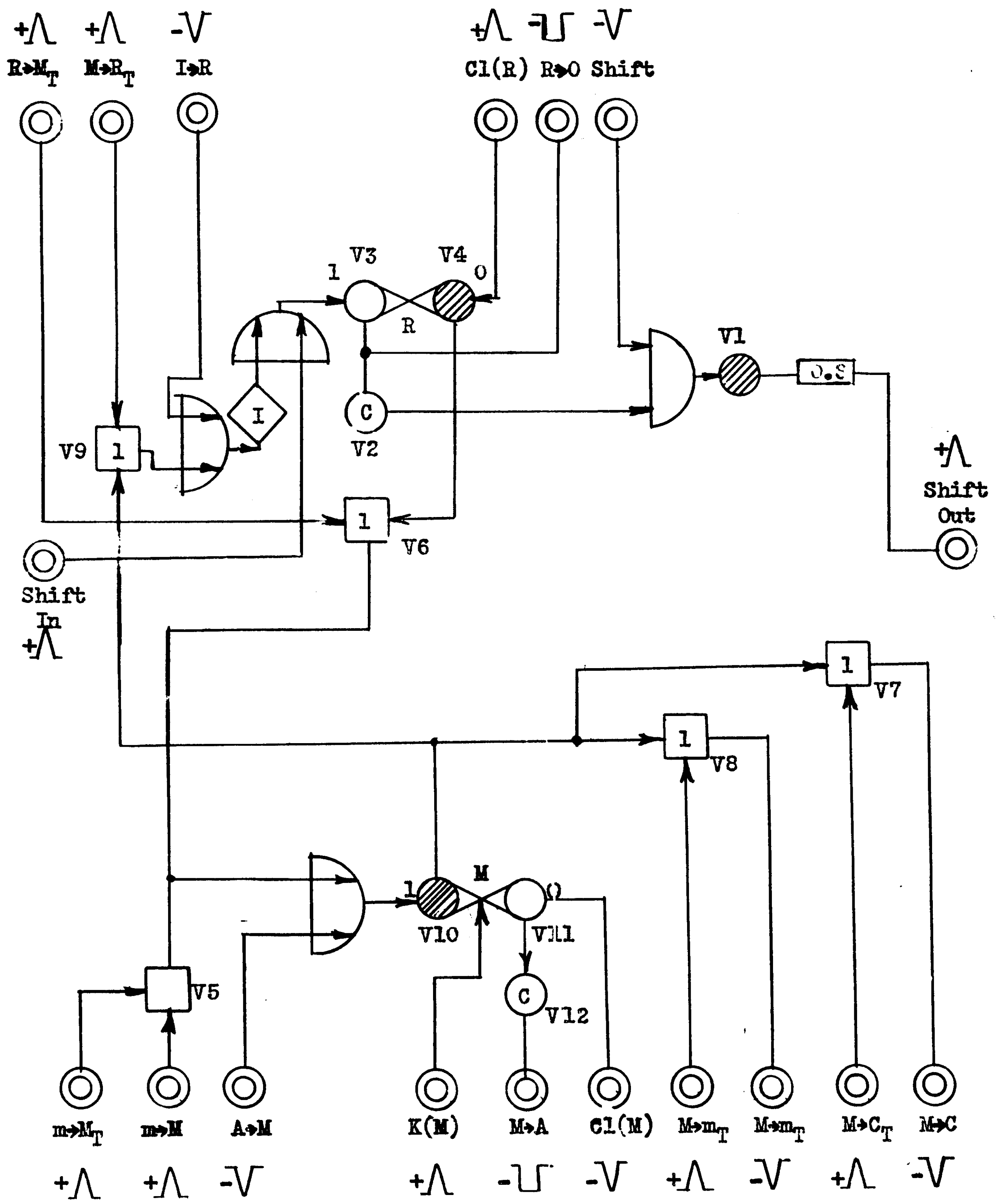
Value	Noise micro volts/volt			Temp. coeff. Parts/million					Solder Change				Temp Cycling -65°C to +125° -55 to 85°			
	BTS	DCC	BOC	BTS	Mil Spec.	DCC	Mil Spec.	BOC	BTS	DCC	Mil Spec.	BOC	BTS	DCC	Mil Spec.	BOC
100 ohms	—	0.1	0.1	-270	500	-270	100	-50	±0.7	-0.1	.5	+0.1	+0.4	-0.1	1.0	-0.1
1,000 ohms	1.3	0.2	0.2	-370	500	-300	100	-100	+0.6	-0.1	.5	+0.1	±0.2	+0	1.0	±0
10,000 ohms	2.3	0.3	0.3	-500	500	-325	100	-100	±0.5	-0.1	.5	+0.05	± .1	-0.1	1.0	-0.1
100,000 ohms	2.4	0.4	0.4	-180	500	-350	200	-150	±0.5	+0.1	.5	+0.1	+0.4	-0.2	1.0	-0.1
500 K	—	0.48	0.48	—	500	-385	200	-180	—	-0.1	.5	+0.1	—	-0.1	1.0	-0.1
1 meg	8.9	1.0	—	-250	500	400	—	—	± .4	-0.2	—	—	+ .4	-0.1	1.0	—

* DCC = Deposited Carbon Resistor, BOC = Boron Carbon Resistor, BTS = IRC Carbon Film Resistor.

1.1 A Register.



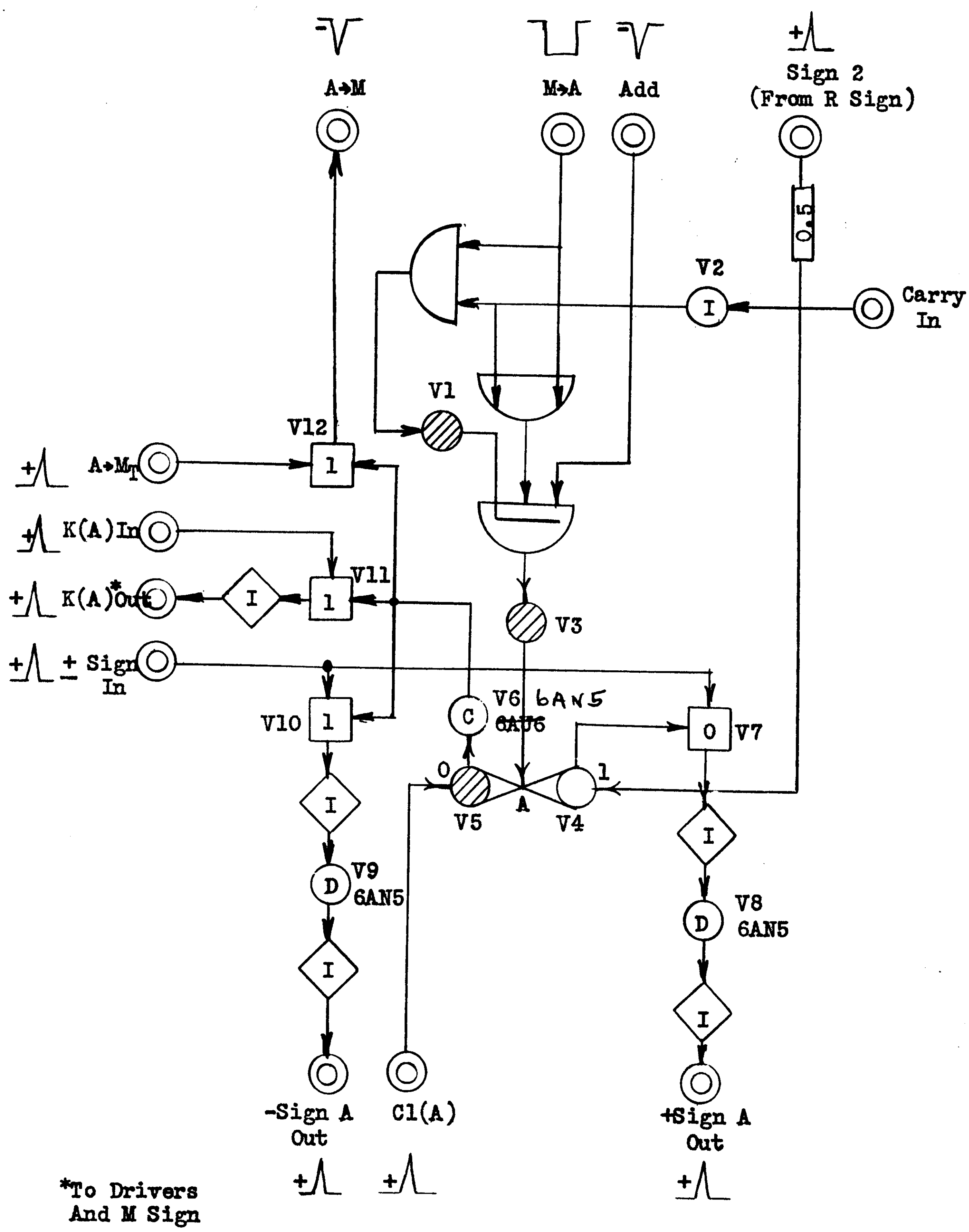
1.2 M-R Register.



OAM

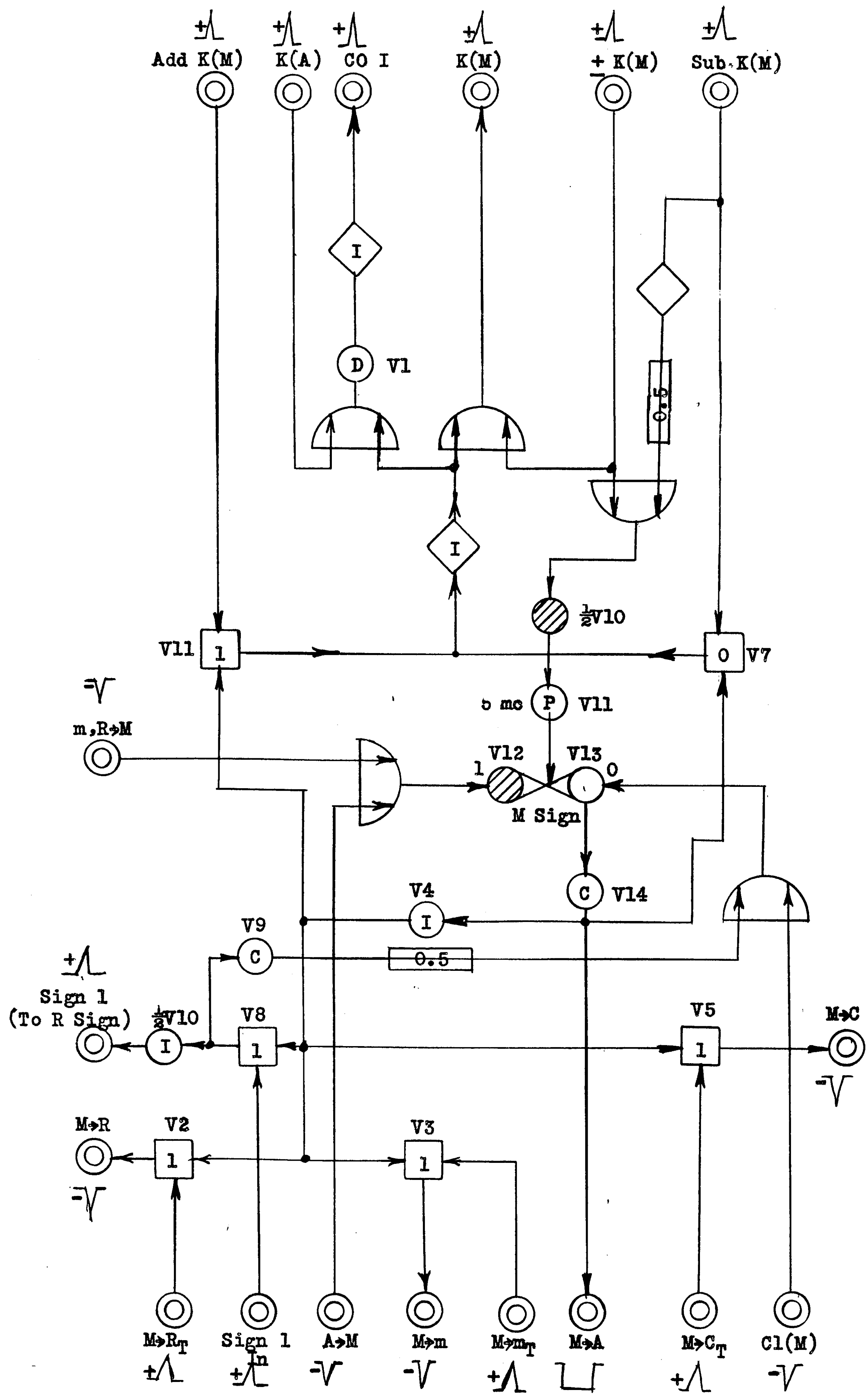
M-R REGISTER

1.3 A Sign Chassis (Supersedes 12-21-49 issue entitled A Sign Register).



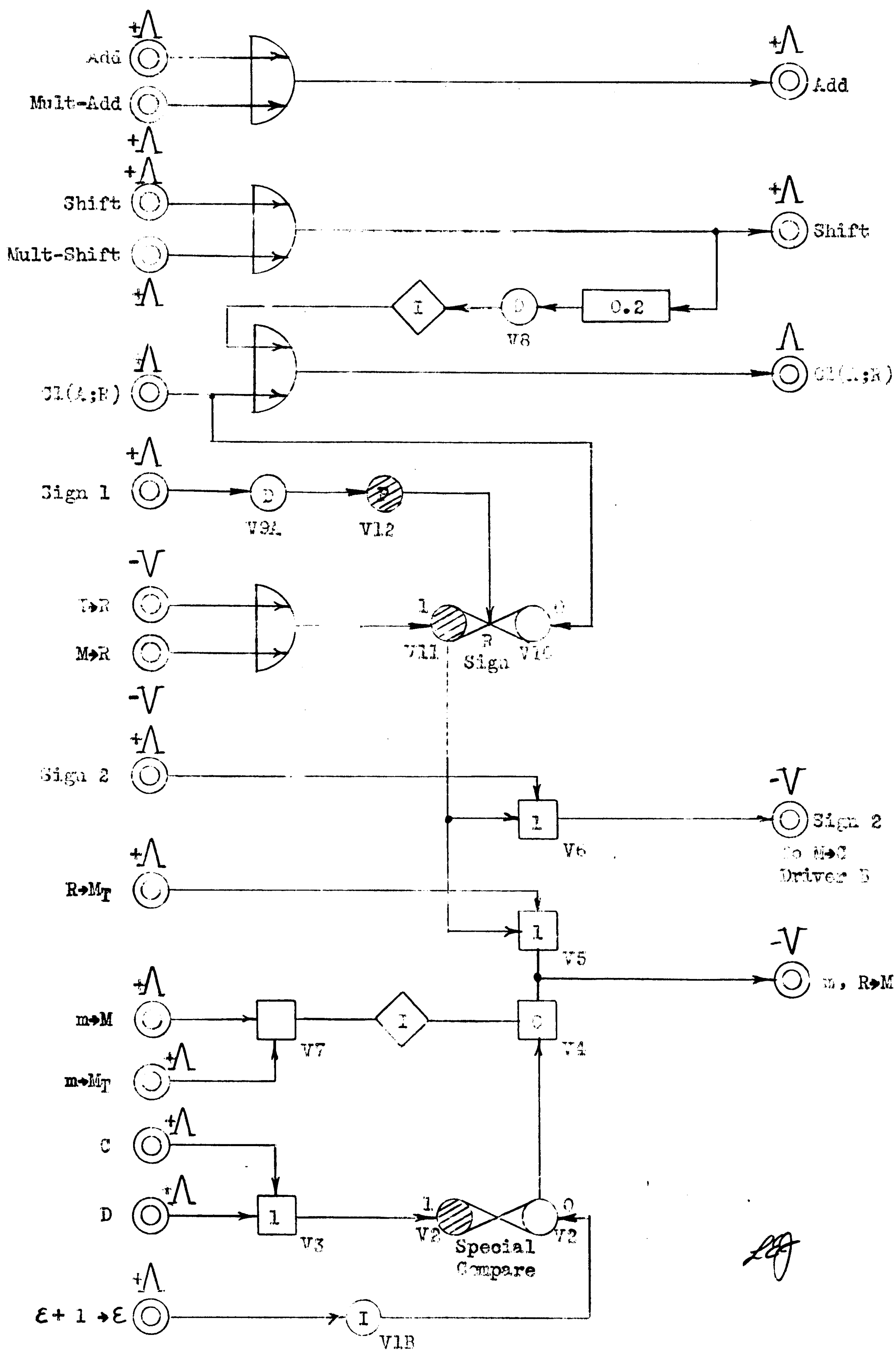
A SIGN CHASSIS

1.4 M Sign Chassis (Supersedes 12-21-49 issue entitled M Sign Register).



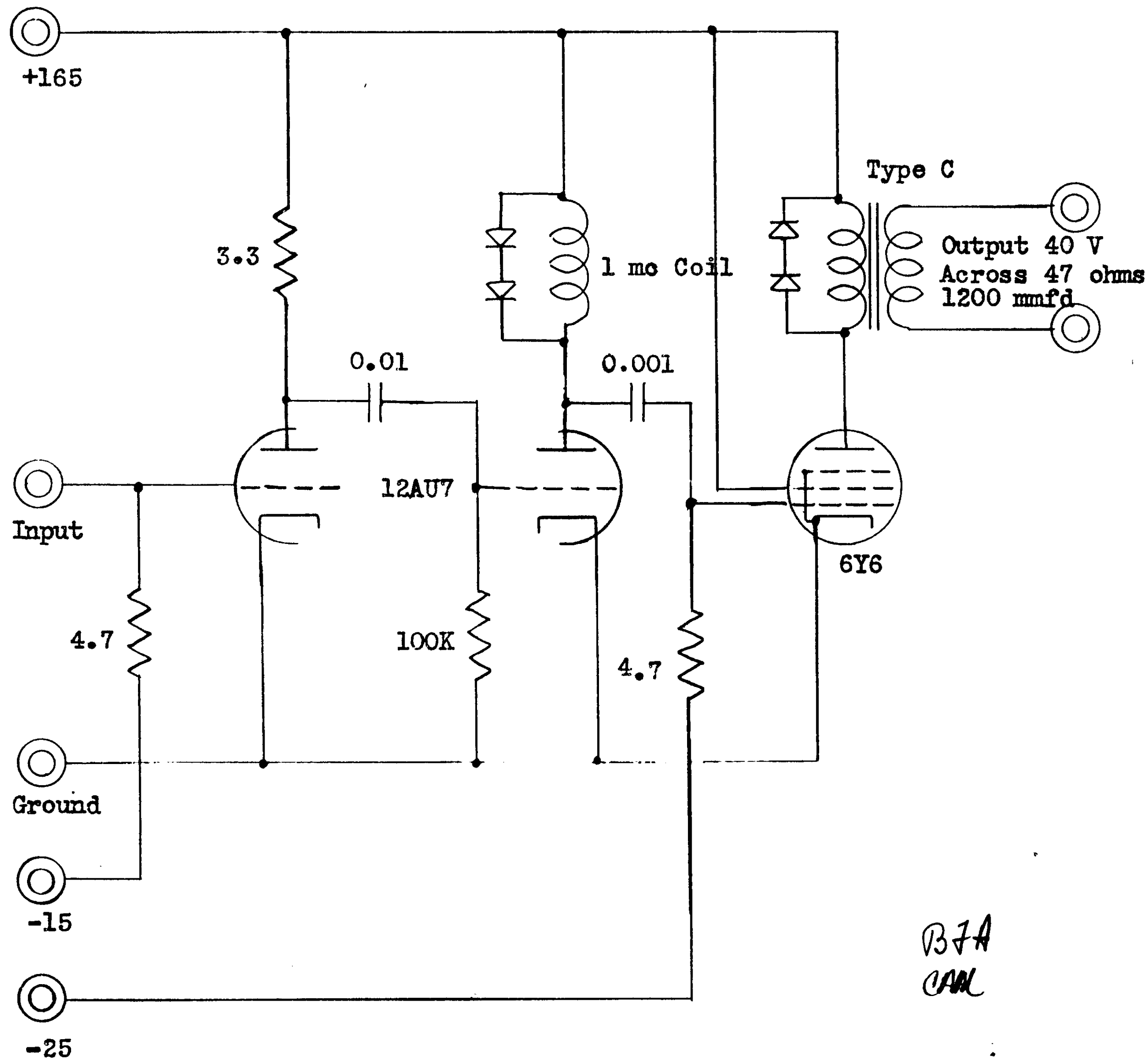
M SIGN CHASSIS

1.5 R Sign Chassis (Supersedes 11-21-49 issue entitled R Sign Register).



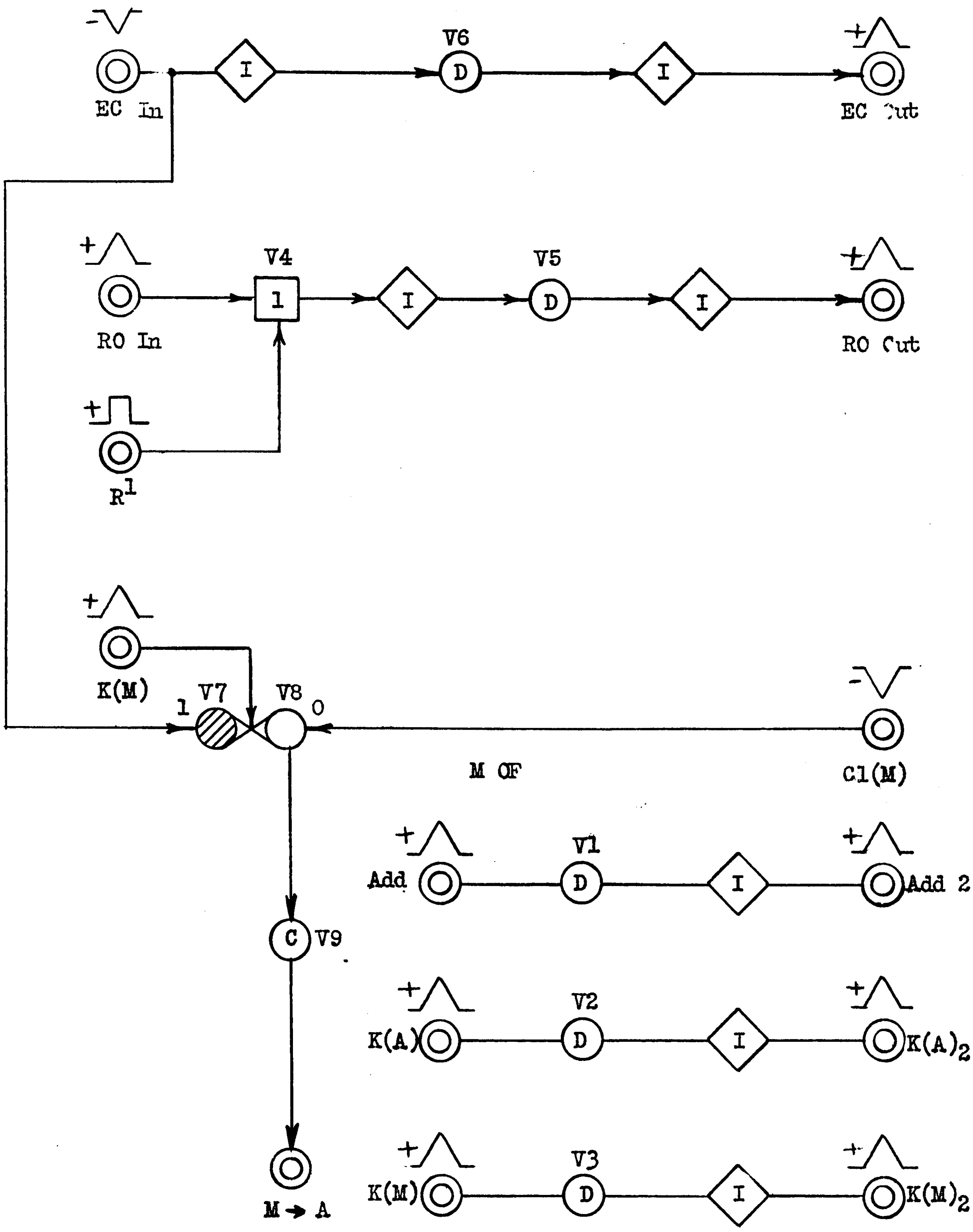
R SIGN CHASSIS

1.7 Broad Pulse Driver.



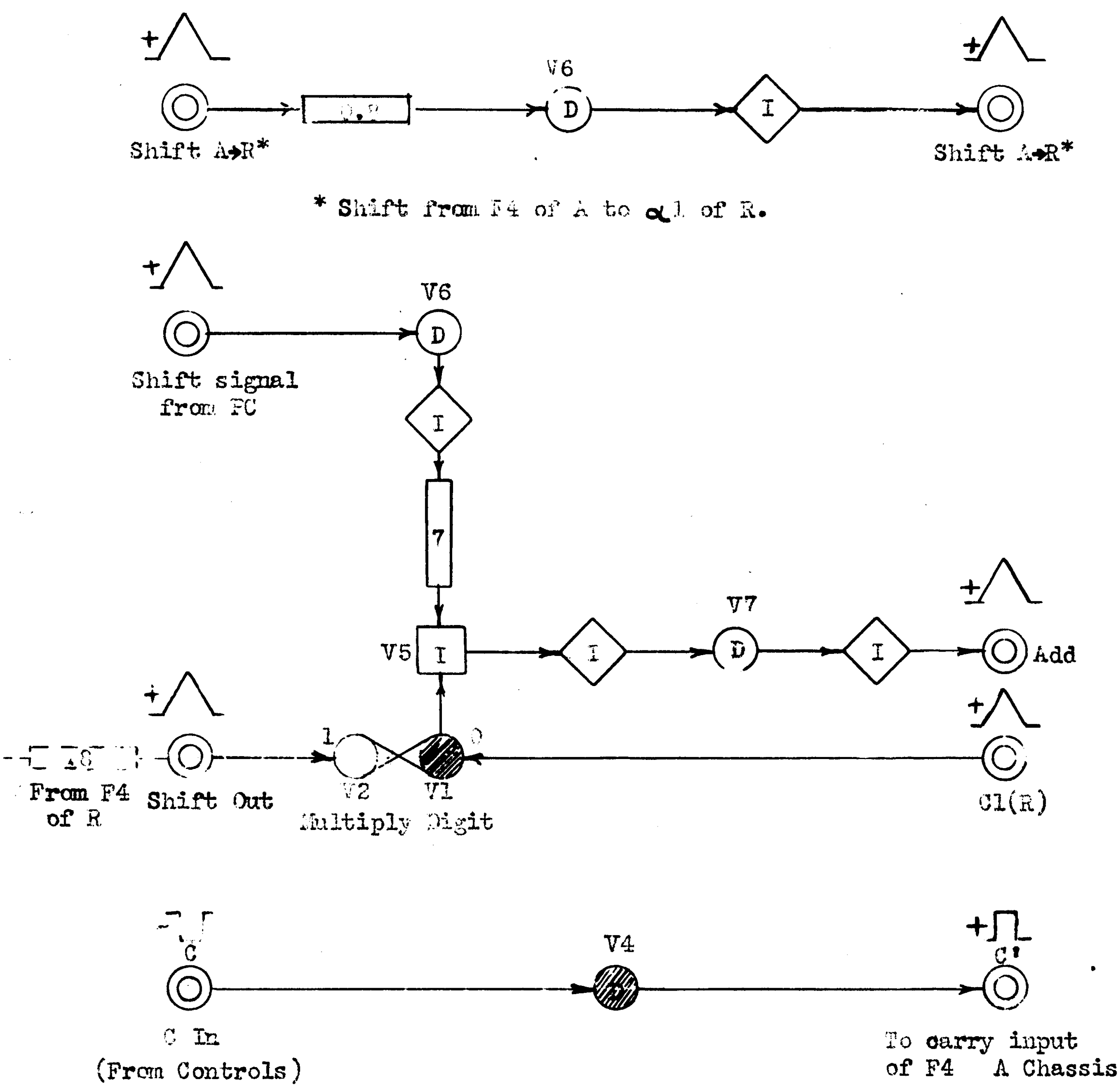
BROAD PULSE DRIVER

1.8 M Overflow.



M OVERFLOW

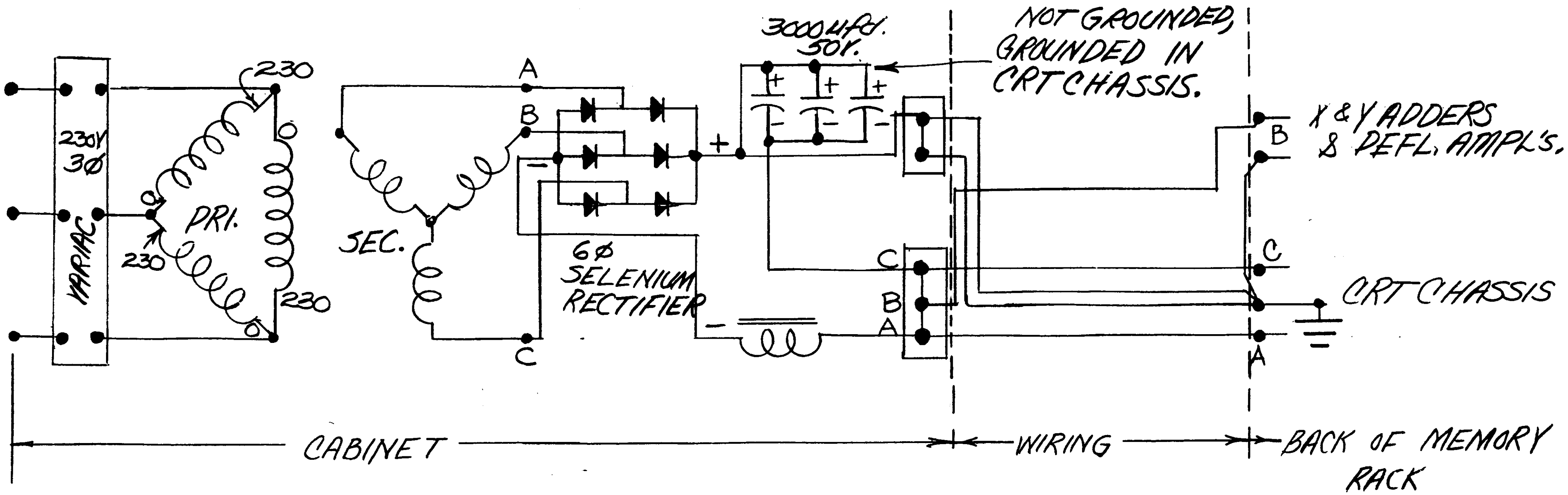
.9 Multiply Digit.



CAM

MULTIPLY DIGIT

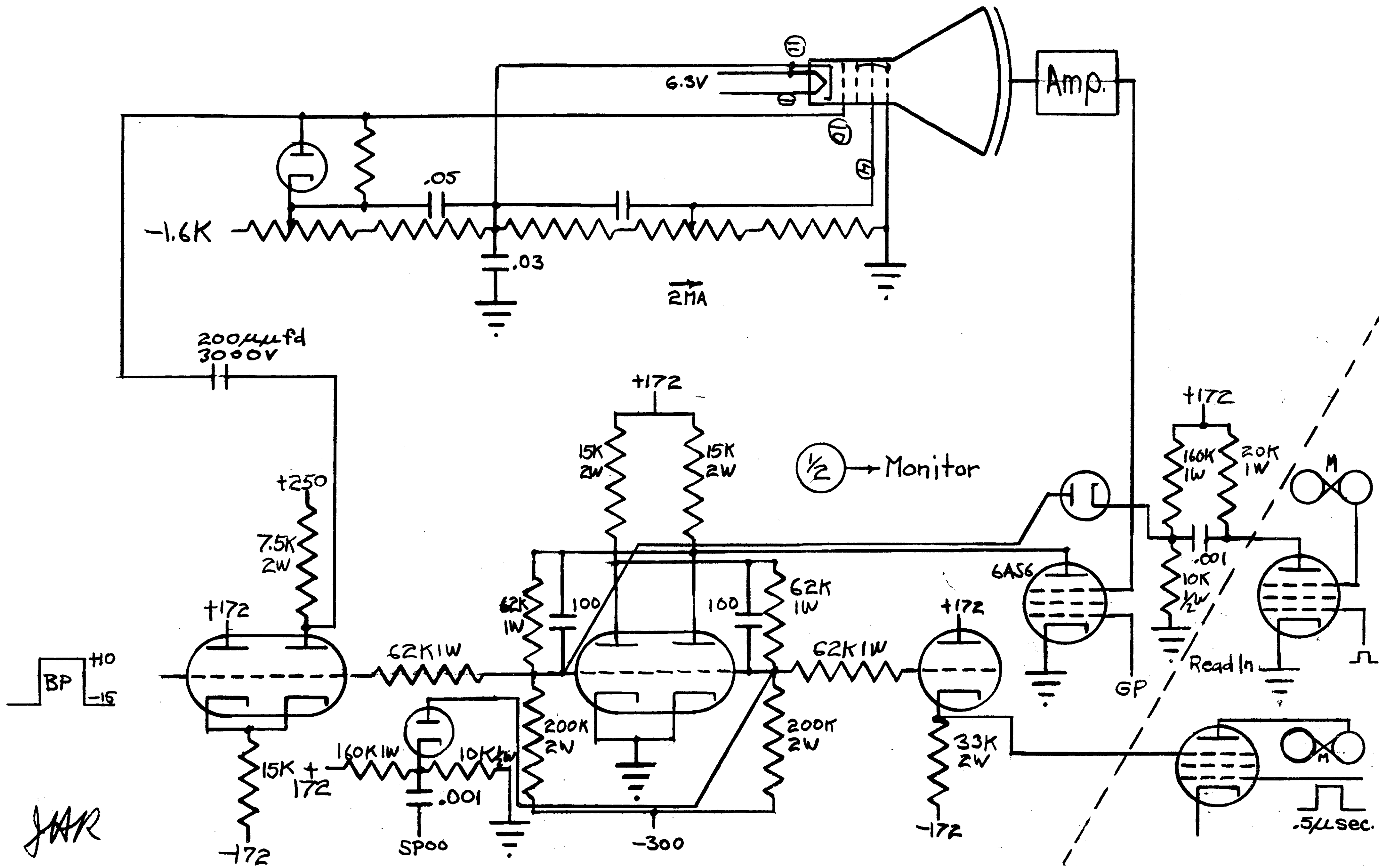
1.10 D.C. Filament Supply for Memory.



D.C. FILAMENT SUPPLY FOR MEMORY - 300 AMP.

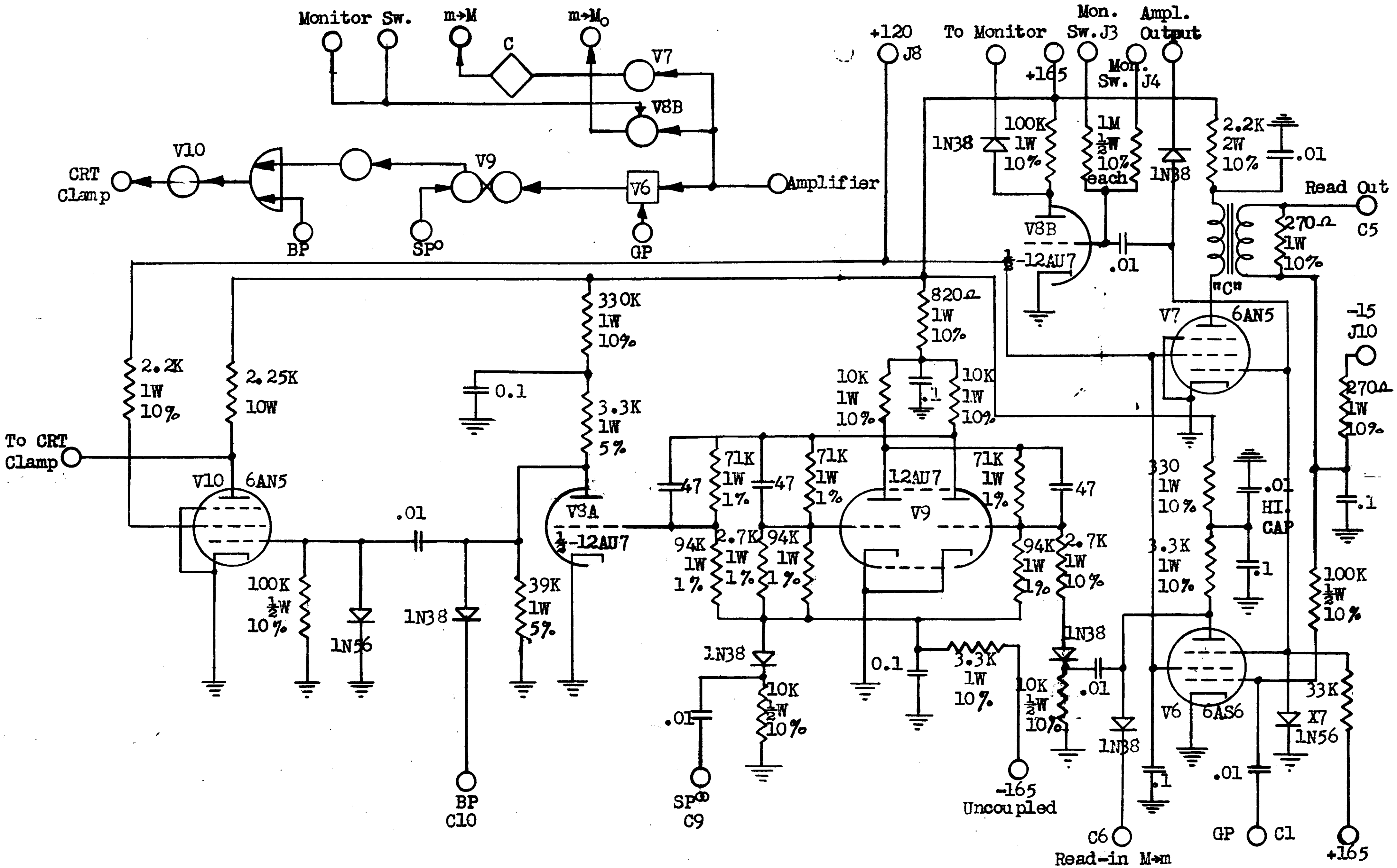
CAM

2.1 Gating and Driving Circuitry, and Clamping Circuit for CRT Unit.
(Experimental A)



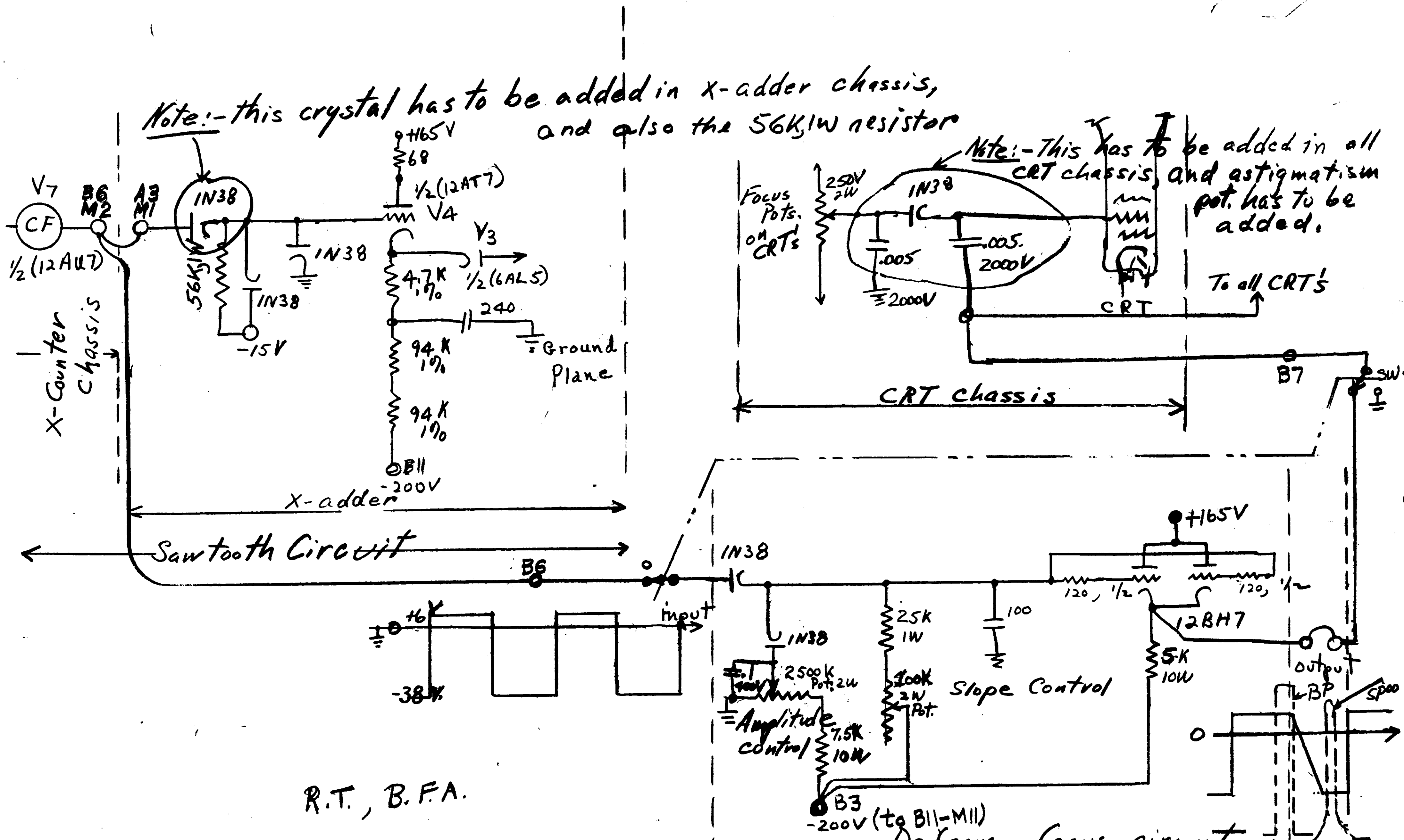
Issued 11-21-49
Reissued 3-1-54

2.1 Gating and Driving Circuitry for CRT Unit.



2.1 Gating and Driving Circuitry for CRT Unit.

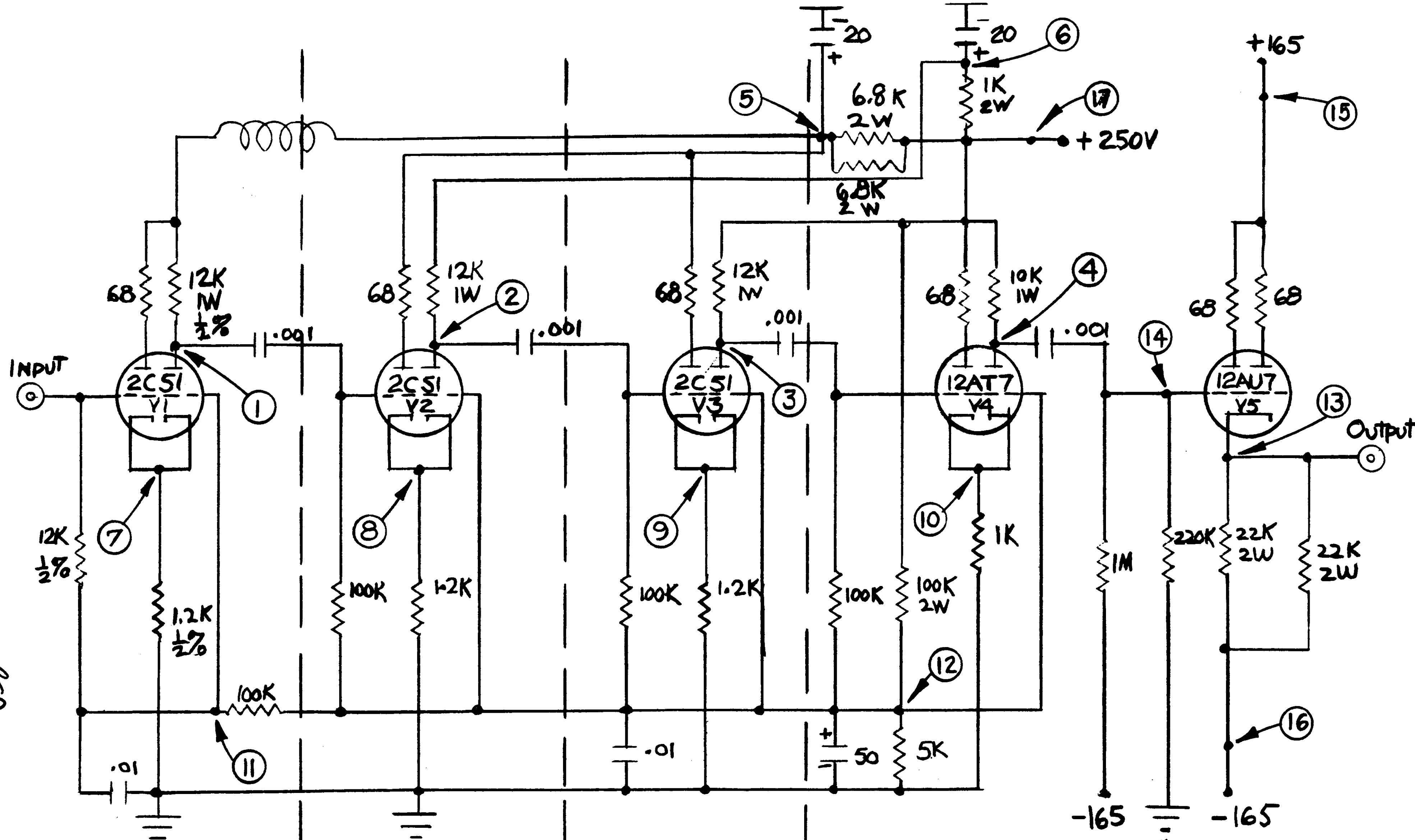
Defocus-Focus Circuitry for Driving CRT Units:



DEFOCUS-FOCUS CIRCUITRY FOR DRIVING CRT UNITS

2.2 CRT Amplifier

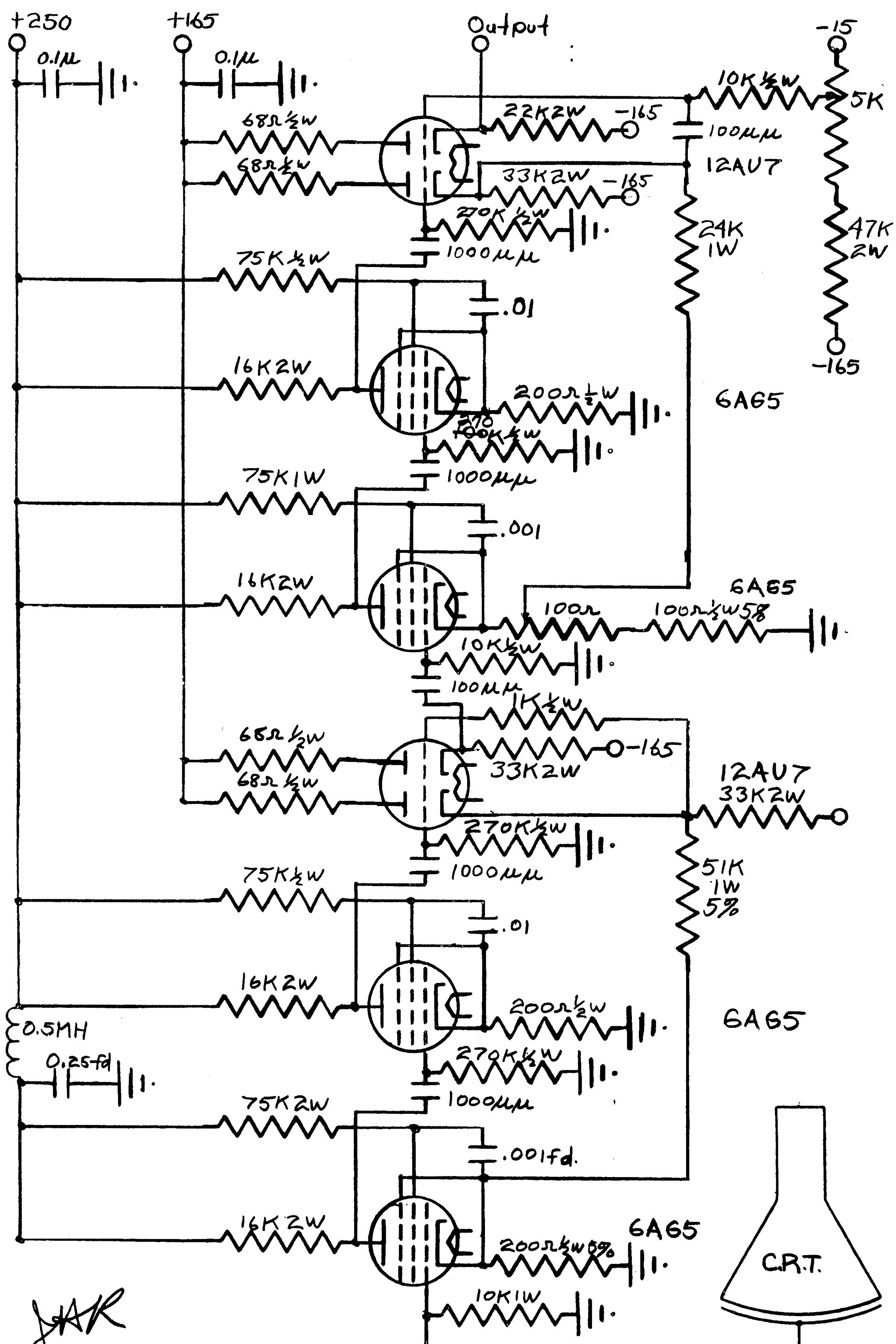
NOTE: TEST POINTS MARKED THUS ○→ SEE TEST PROCEDURE



CRT AMPLIFIER

CAM

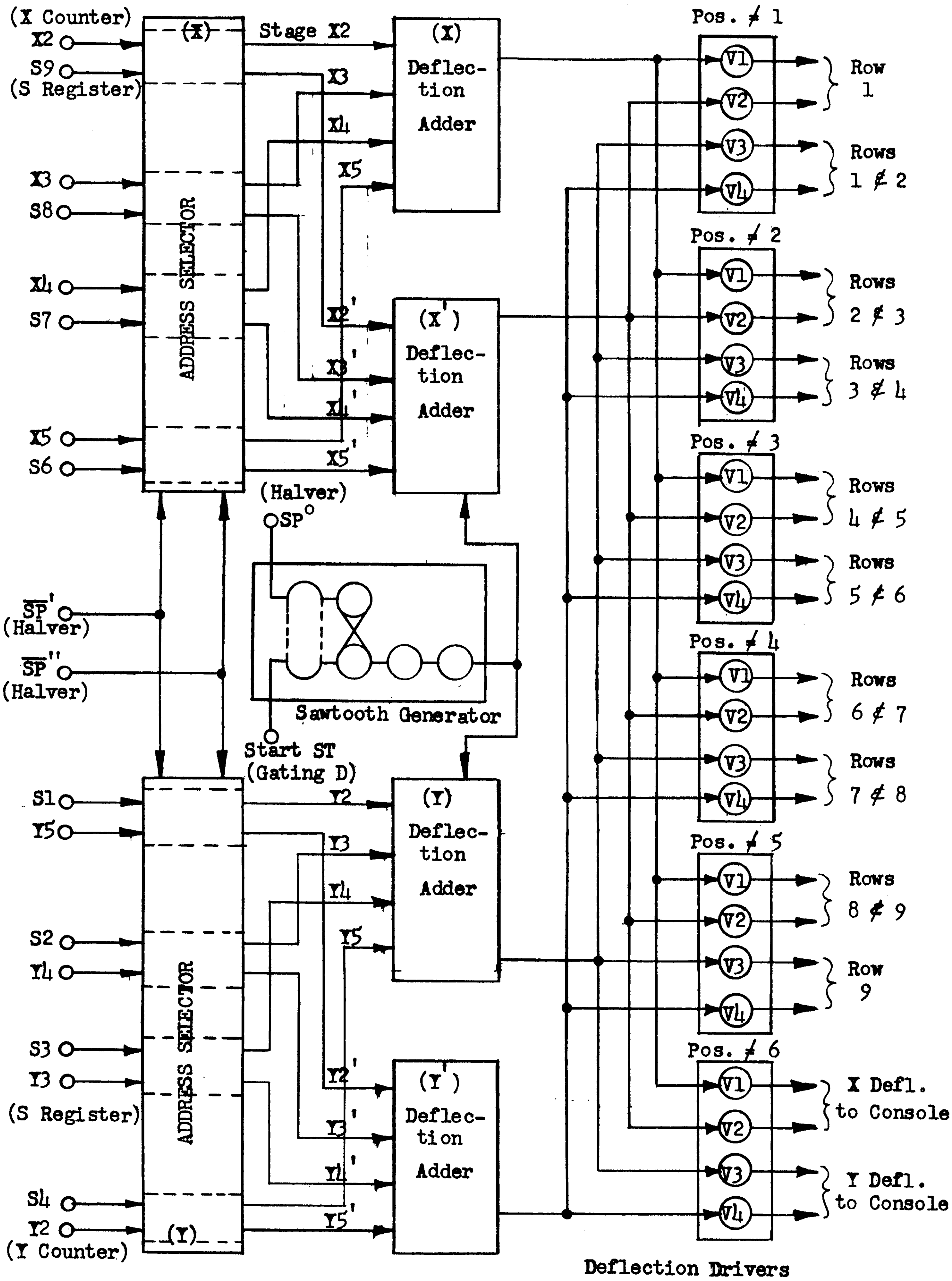
2.2 CRT Amplifier (Experimental)



CRT AMPLIFIER (Experimental)

2.3 CRT DC Deflection System

Block Diagram:

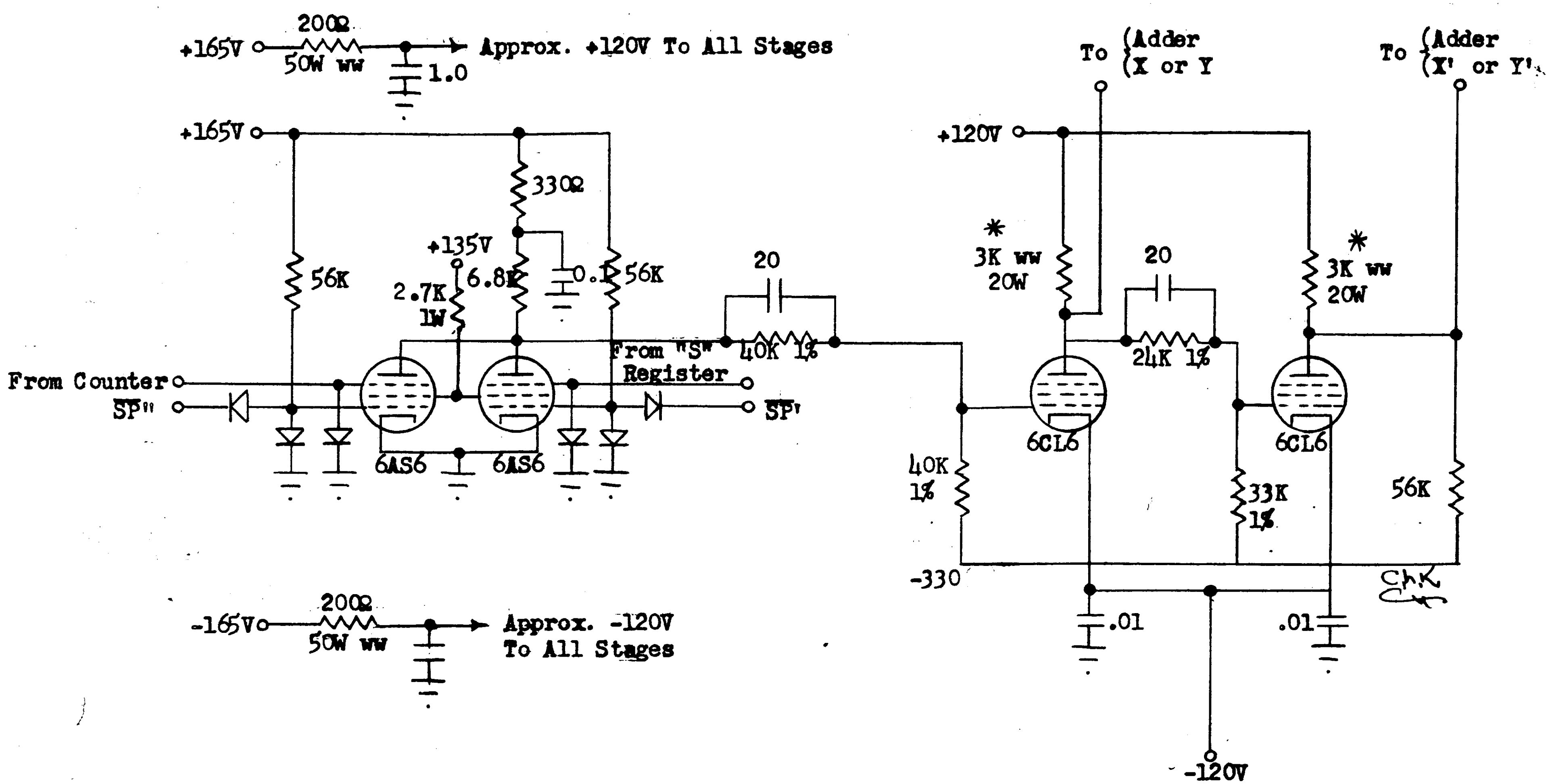


LEJ

BLOCK DIAGRAM

2.3 CRT DC Deflection System

Address Selector Chassis Type A (Schematic):



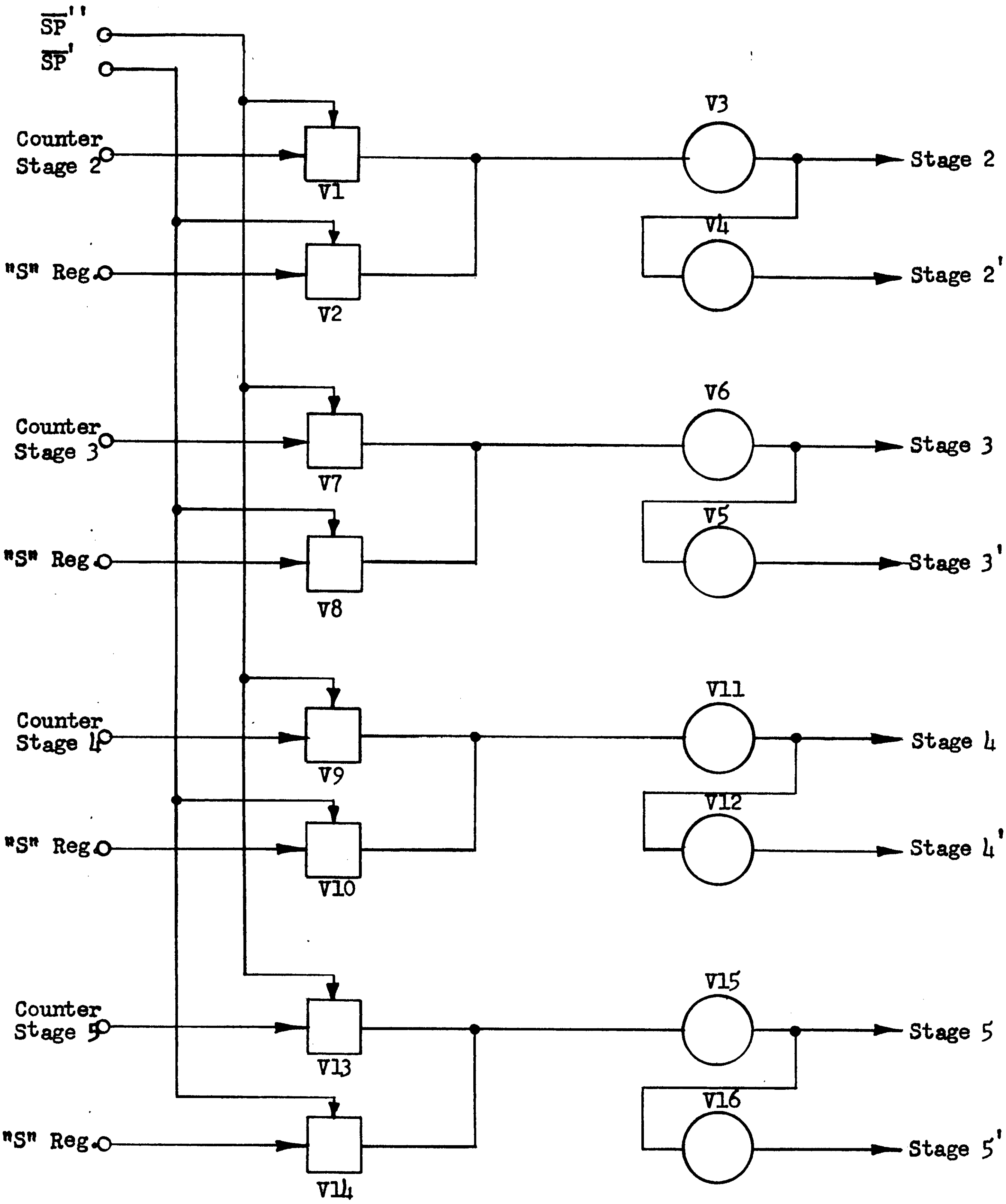
TYPICAL ADDRESS SELECTOR STAGE TYPE A

NOTE: 1) Four stages per chassis.
2) Stages 1, 2 and 3 identical to above schematic.
* 3) Stage 4 differs only in that plate resistors of 6CL6's are 3.5K.

Chk
637

2.3 CRT DC Deflection System

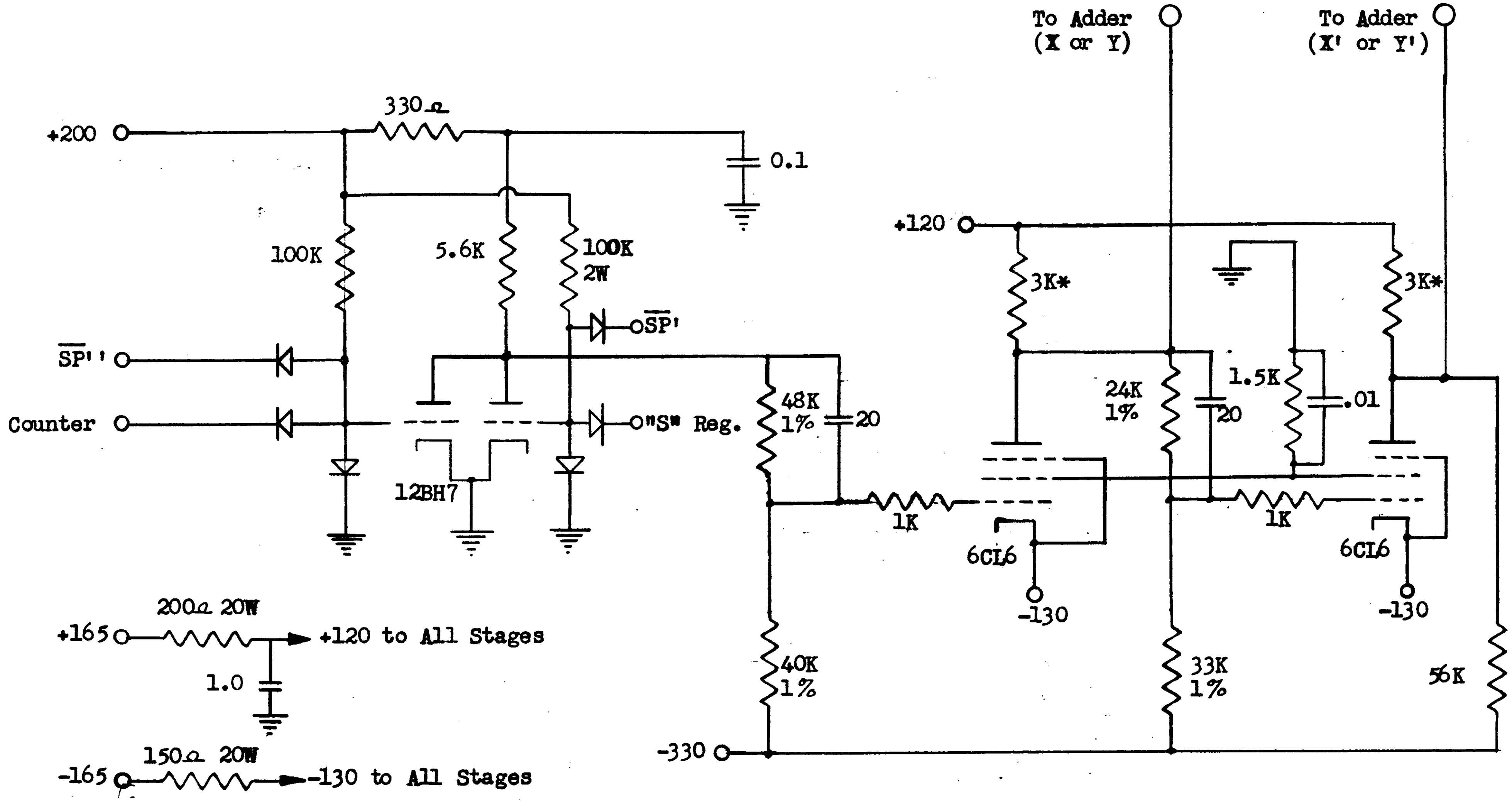
Address Selector Type A (Block Diagram):



ADDRESS SELECTOR TYPE A

2.3 CRT DC Deflection System

Address Selector Type B (Schematic):

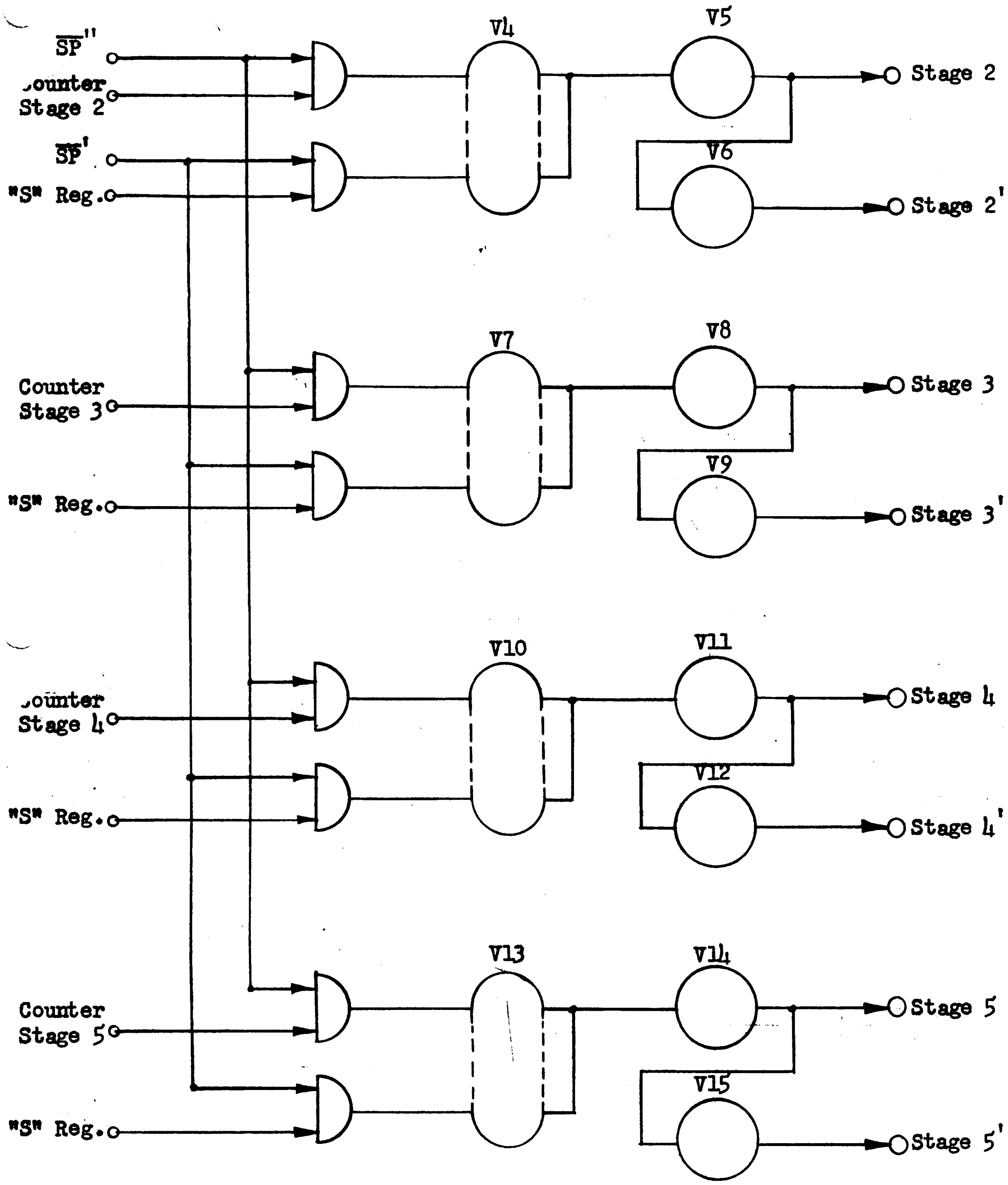


NOTE: 1) Four stages per chassis.
2) Stage 2, 3, and 4 identical to above schematic.
*3) Stage 5 differs only in that plate resistors of 6CL6's are 3.5K.

TYPICAL STAGE

2.3 CRT DC Deflection System

Address Selector Type B (Block Diagram):

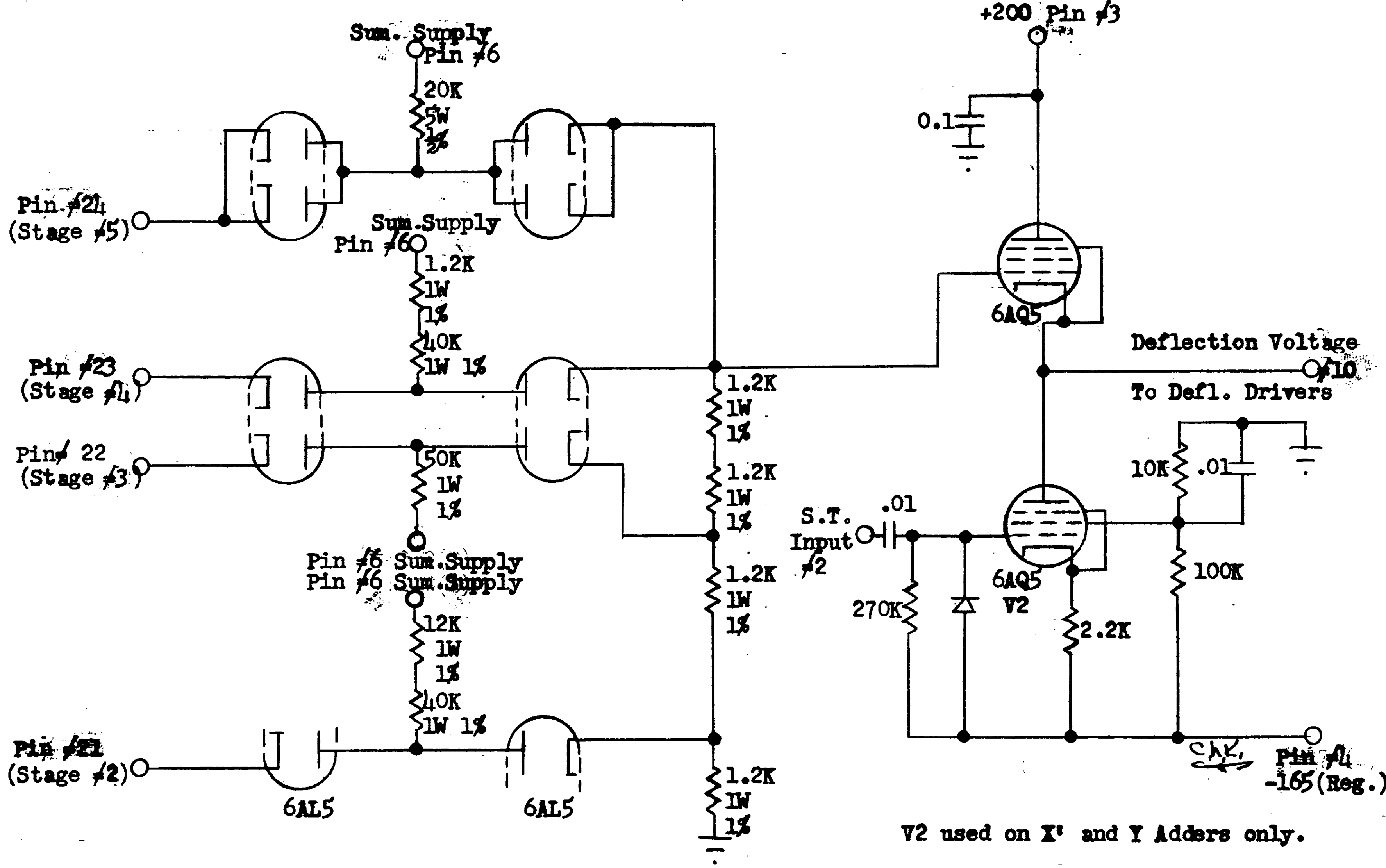


ADDRESS SELECTOR TYPE B

LEJ

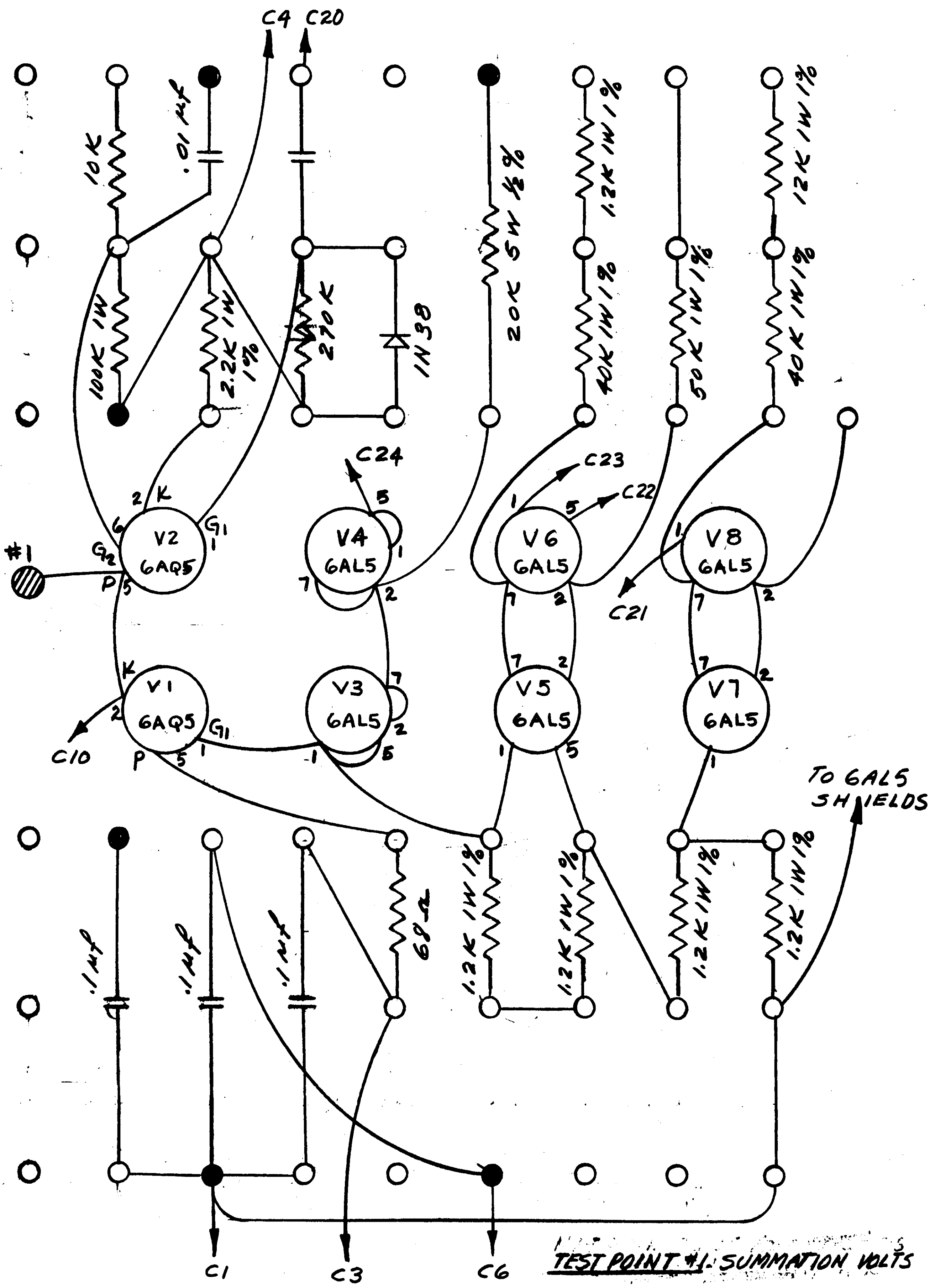
2.3 CRT DC Deflection System

Deflection Adder (Schematic):



2.3 CRT DC Deflection System

Deflection Adder (Tagboard):



TEST POINT #1. SUMMATION VOLTS

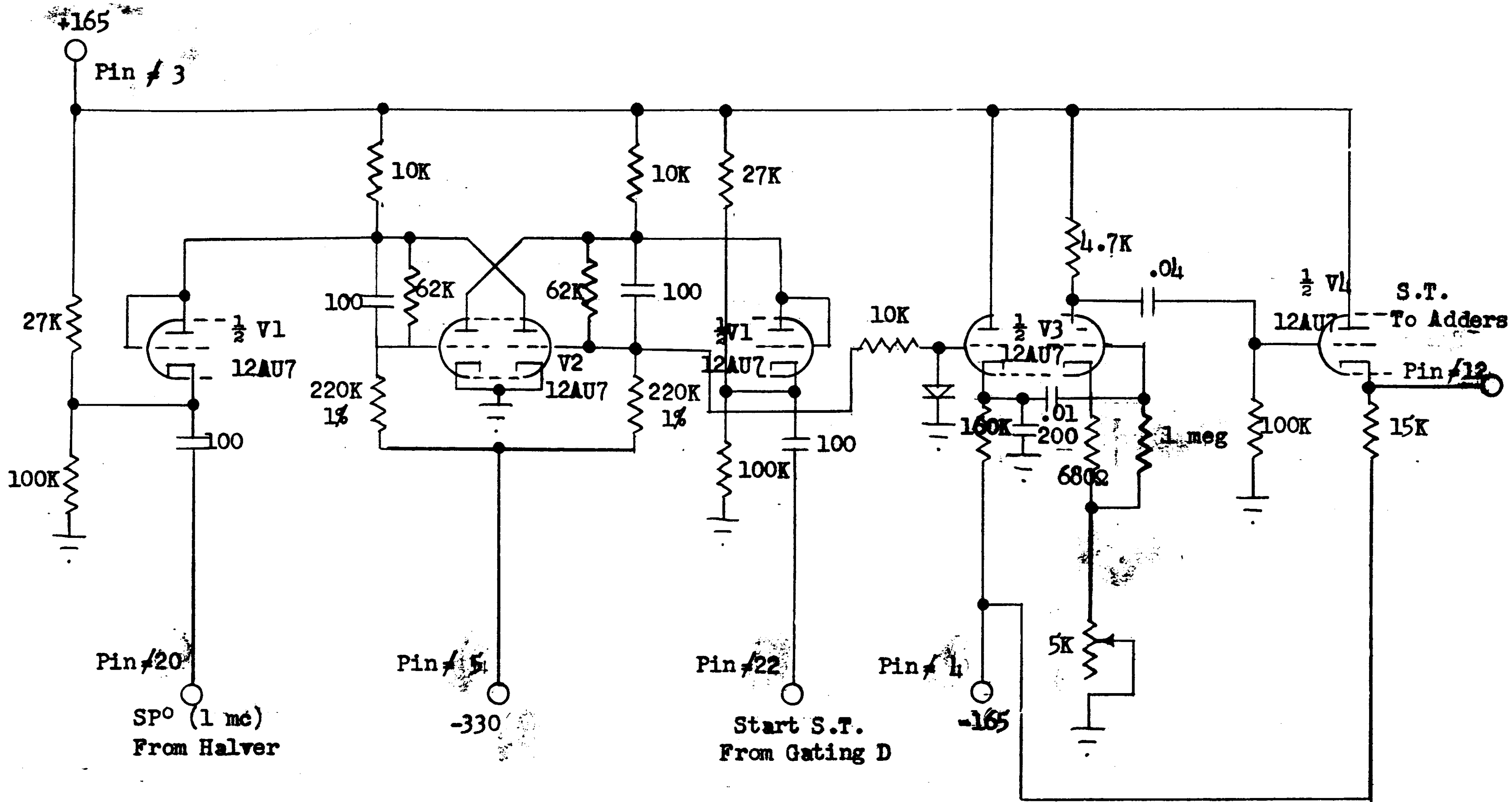
C1 GROUND	C7	C13 FIL. AT GND	C19
C2 GROUND	C8	C14 FIL. AT GND	C20 ST. INPUT
C3 +200 VOLTS	C9	C15 FIL AT -165	C21 STAGE #2 IN
C4 -165 VOLTS	C10 SUM. VOLT. OUT	C16 FIL AT -165	C22 STAGE #3 IN
C5	C11	C17	C23 STAGE #4 IN
C6	C12	C18	C24 STAGE #5 IN

NOTES 1. FIL OF V2 TO C15 & C16 - OTHERS C13 & C14 2. G_3 TO K ON V1 & V2 3. G2 TOP ON V1

Reissued 3-1-54
Issued 5-20-53

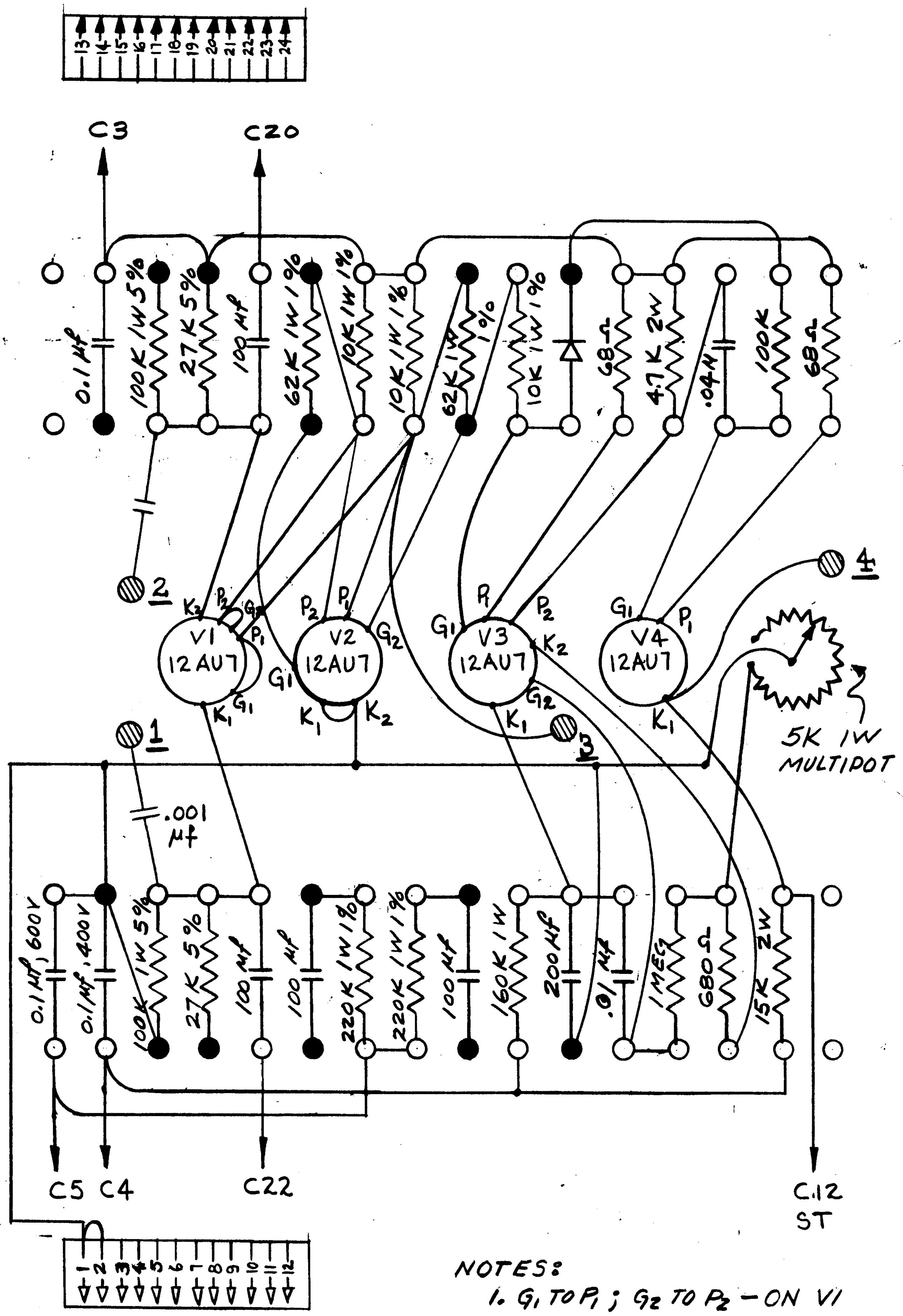
2.3 CRT DC Deflection System

Sawtooth Generator (Schematic):



2.3 CRT DC Deflection System

Sawtooth Generator (Tagboard):



NOTES:

1. G_1 TO P_1 ; G_2 TO P_2 — ON V1

C1 GROUND
C2 GROUND
C3 +165
C4 -165
C5 -330
C12 ST. OUT.
C13 FILAMENT
C14 FILAMENT
C20 SP°
C22 START S.T.

TEST POINTS:

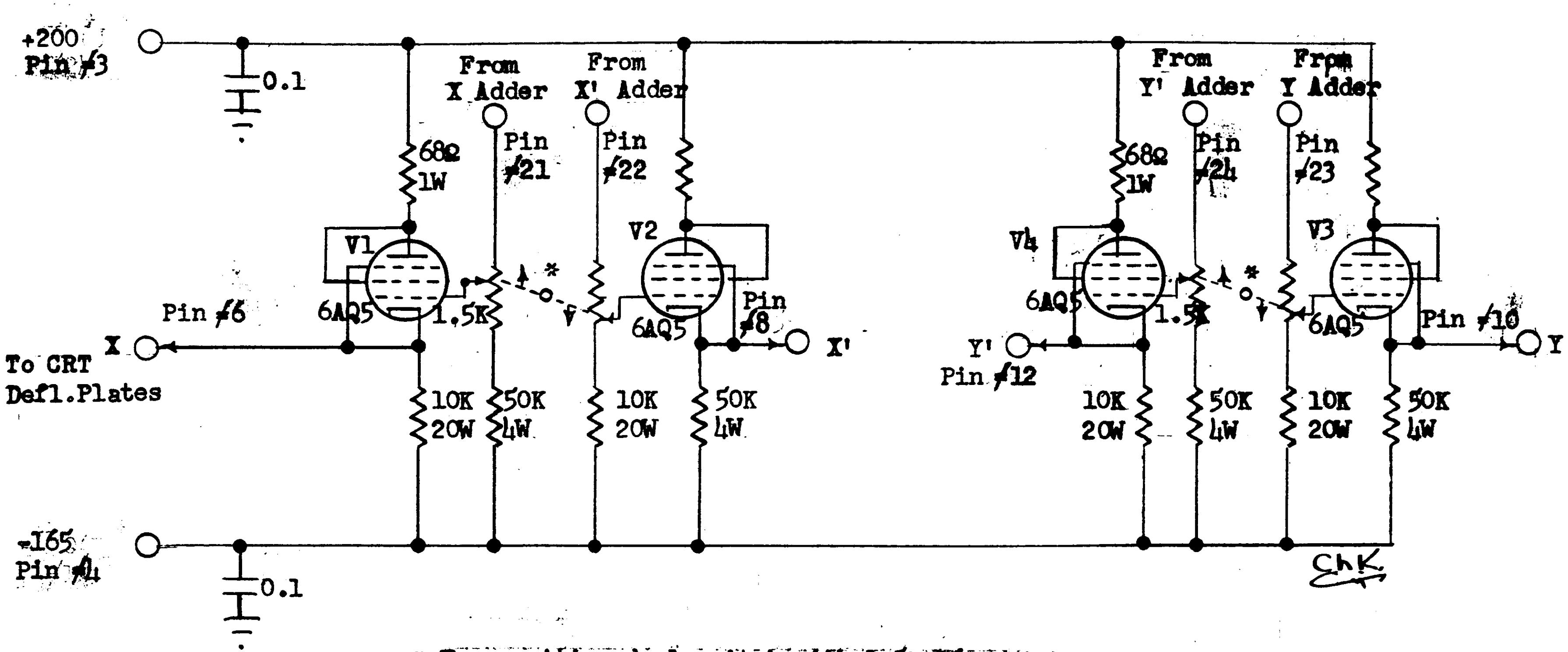
1. START S.T.
2. SP°
3. S.T. FLIPFLOP
4. S.T.

LEJ

Issued 5-20-53
Reissued 3-1-54

2.3 CRT DC Deflection System

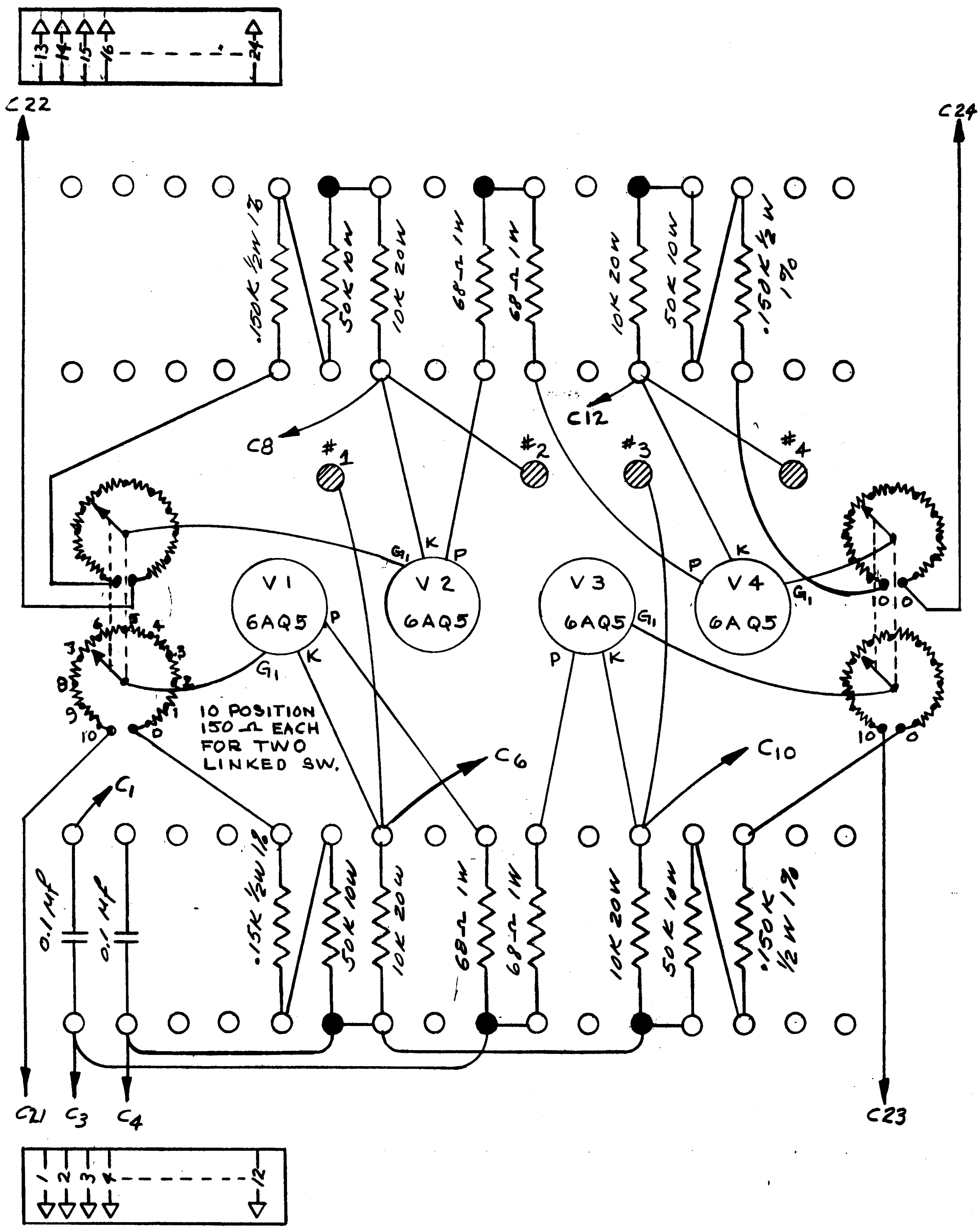
Deflection Driver (Schematic):



* Ten position dual switch with 1.5K 1% resistors between detents - for positioning raster.

2.3 CRT DC Deflection System

Deflection Driver (Tagboard):

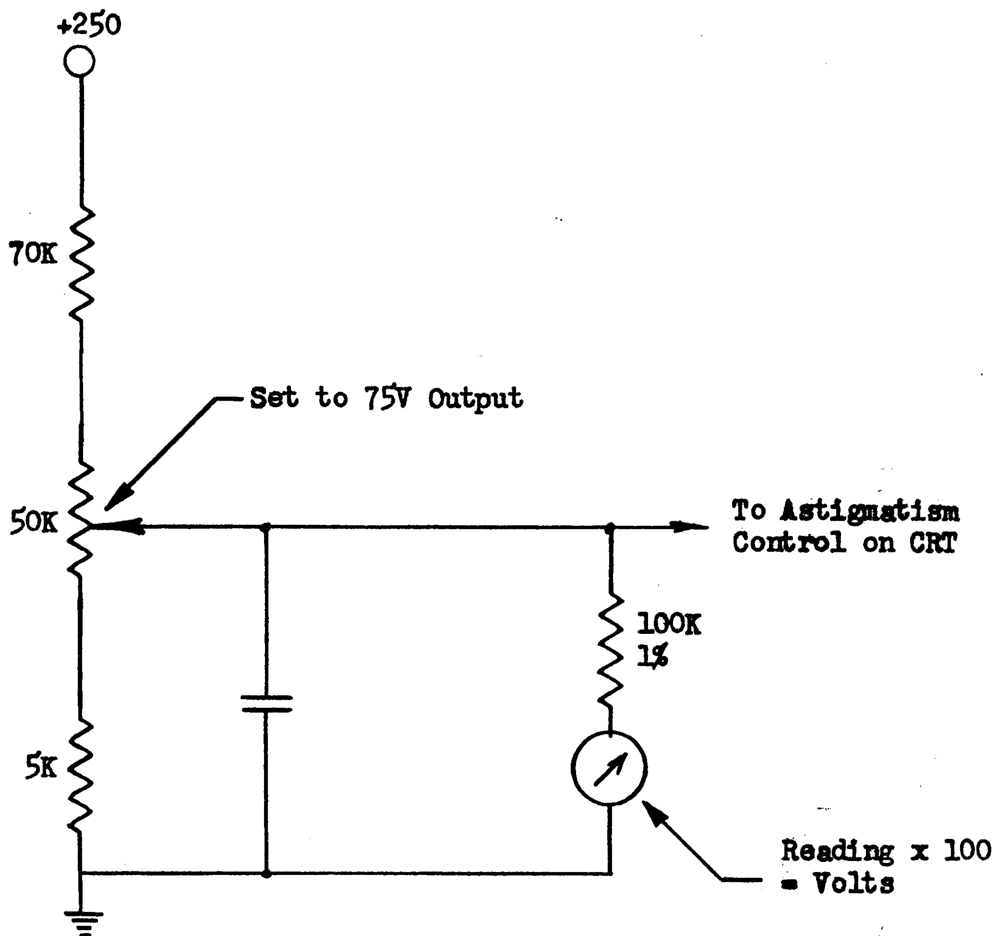


C1 GROUND
C2
C3 +200 VOLTS
C4 −165 VOLTS
C5 X TO CRT'S
C6
C7
C8 X' TO CRT'S
C9
C10 Y TO CRT'S
C11
C12 Y' TO CRTS
C13 FILAMENT
C14 FILAMENT
C15
C16
C17
C18
C19
C20
C21 X IN
C22 X' IN
C23 Y IN
C24 Y' IN

NOTES
FOR V1, V2, V3 & V4
G3 TO K, G2 TO P
TEST POINTS:
#1 X TO CRT'S
#2 X' TO CRT'S
#3 Y TO CRT'S
#4 Y' TO CRT'S

2.3 CRT DC Deflection System

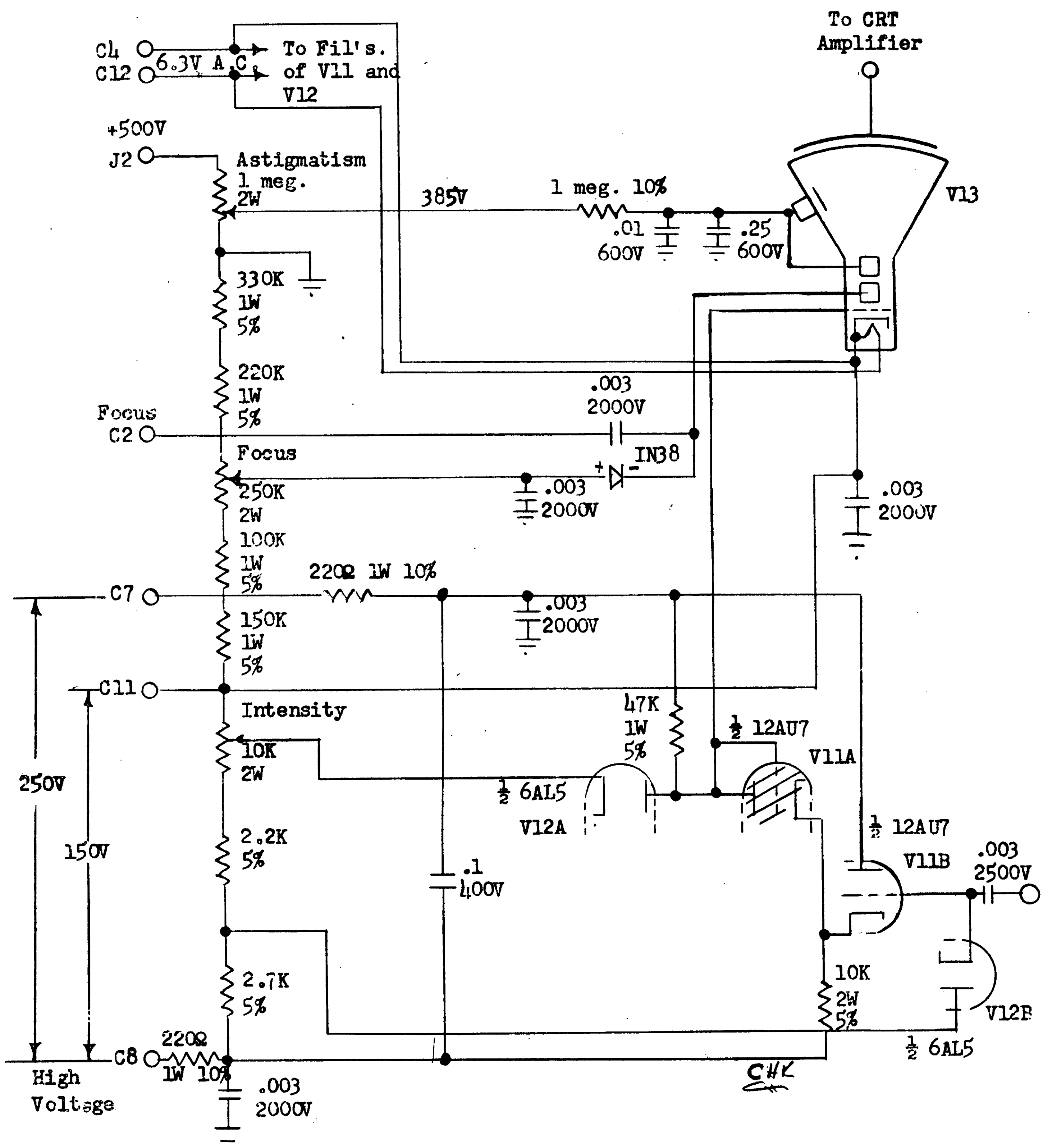
CRT Astigmatism Voltage Supply:



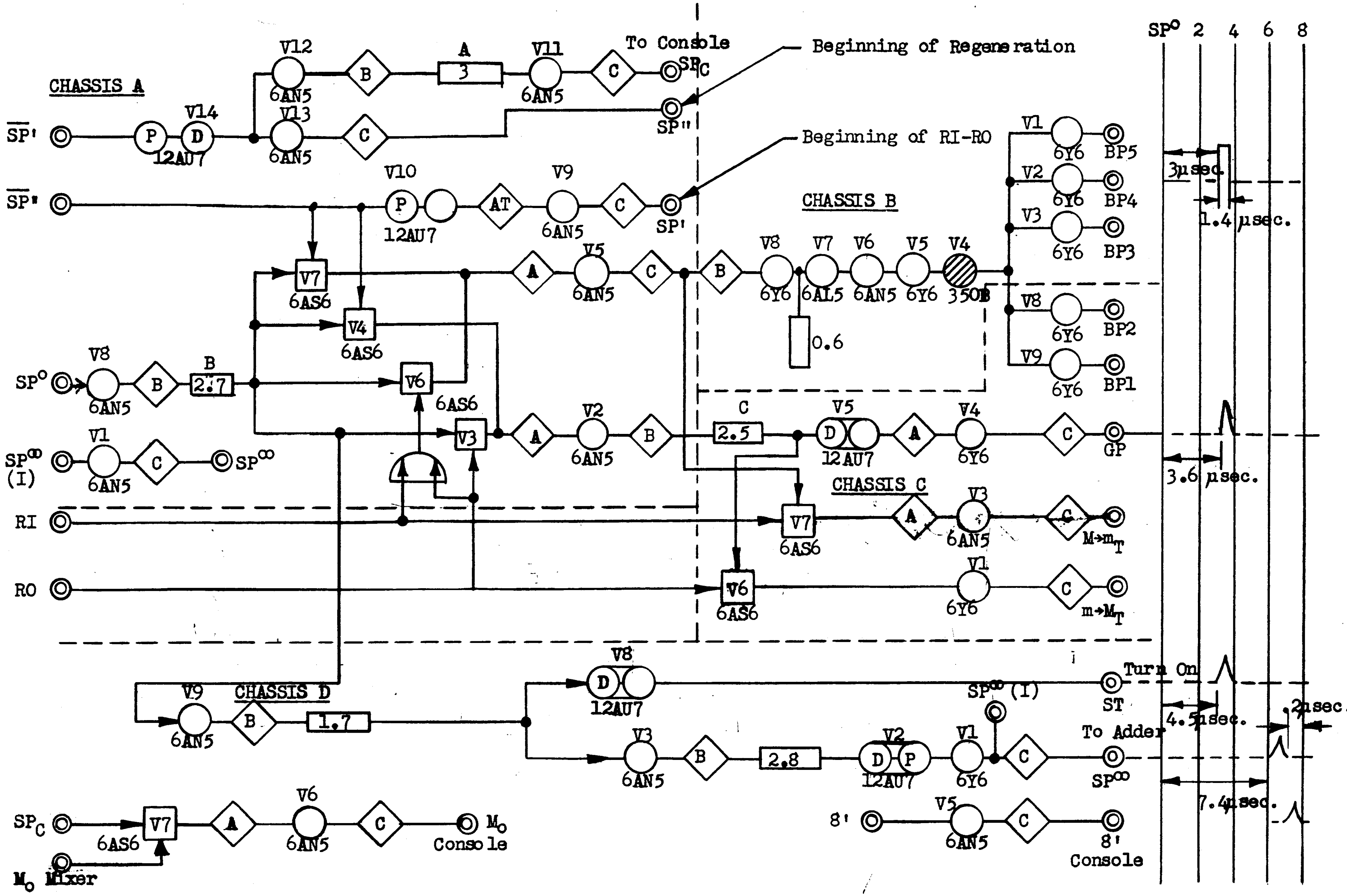
LOCATED ON MEMORY FUSE PANEL

LEJ

2.4 CRT Clamping Circuit.



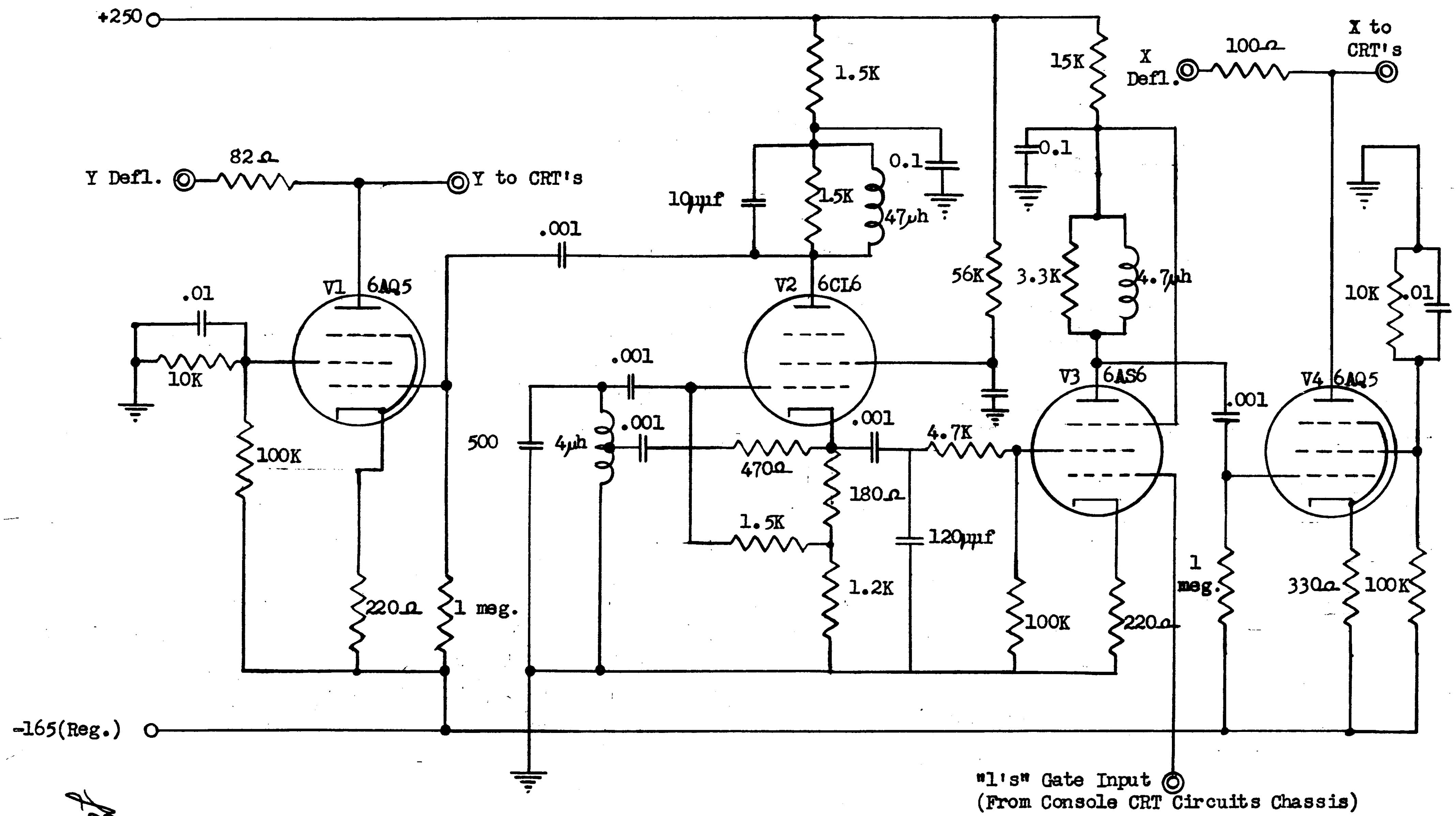
CRT CLAMPING CIRCUIT


CHASSIS A
CHASSIS B
CHASSIS C
CHASSIS D
Beginning of Regeneration
Beginning of RI-RO
To Console
SP'
SP"
SP°
SP∞
(I)
RI
RO
V14
12AU7
V12
V13
V11
6AN5
V10
V9
V8
V7
V6
V5
V4
V3
V2
V1
6AS6
6Y6
6AL5
350B
0.6
2.5
2.8
1.7
2.7
BP5
BP4
BP3
BP2
BP1
GP
M→m_T
m→M_T
Turn On
ST
To Adder
8'
8' Console
M_o Mixer
M_o Console
SP_C
3 µsec.
1.4 µsec.
3.6 µsec.
4.5 µsec.
2 µsec.
7.4 µsec.

Issued 3-1-54

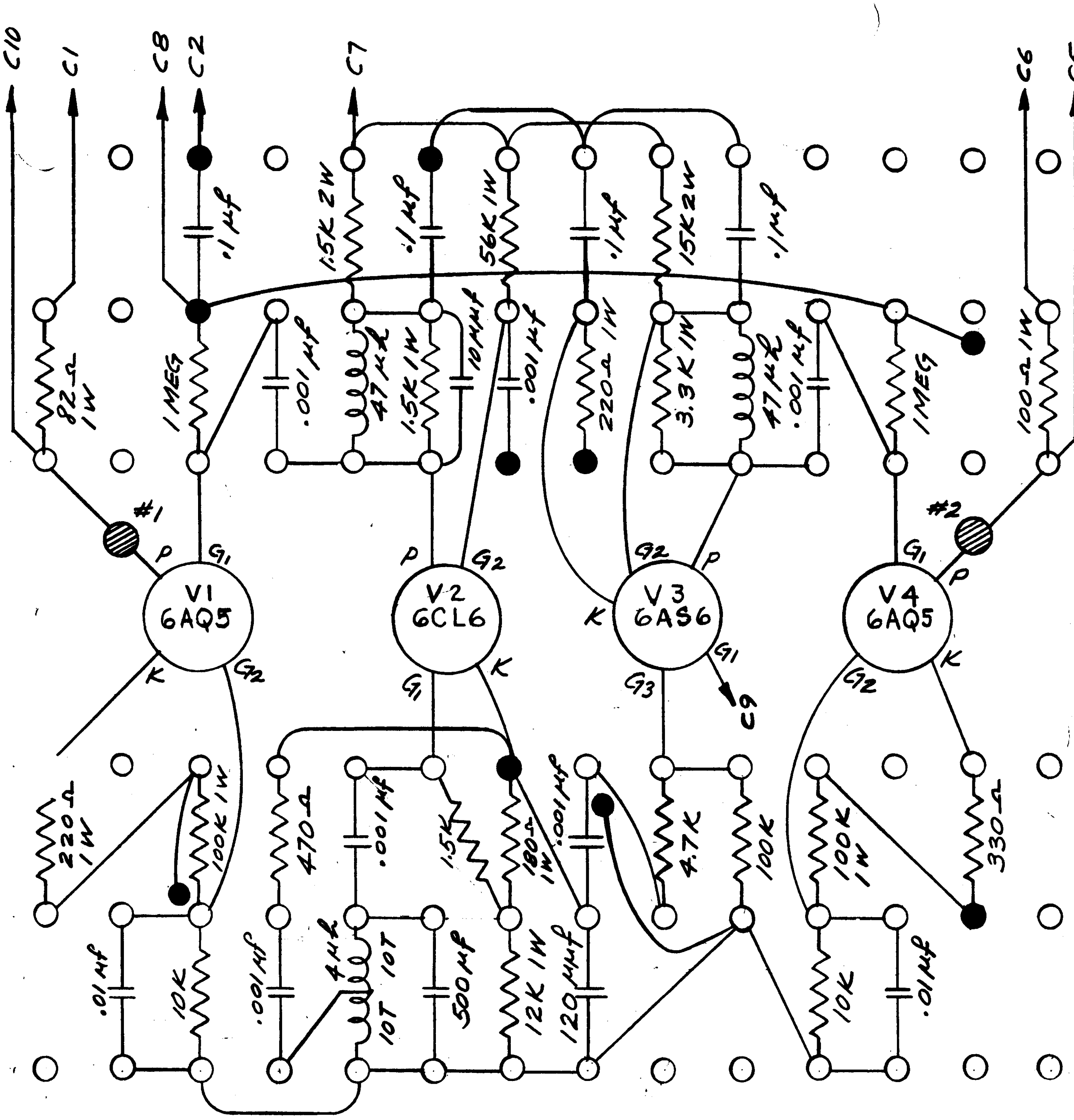
2.9 Console Circle Generator

Schematic:



2.9 Console Circle Generator

Tagboard:



C 1. Y DEFLECTION IN
2. GROUND
3 FILAMENT AT -165 VOLTS
4 FILAMENT AT GROUND
5 X DEFLECTION TO CRT'S
6. X DEFLECTION IN
7. +250 VOLTS
8. -165 VOLTS (REG)
Mo GATE INPUT
9. Y DEFLECTION TO CRT'S
11. FILAMENT AT -165 VOLTS
12. FILAMENT AT GROUND

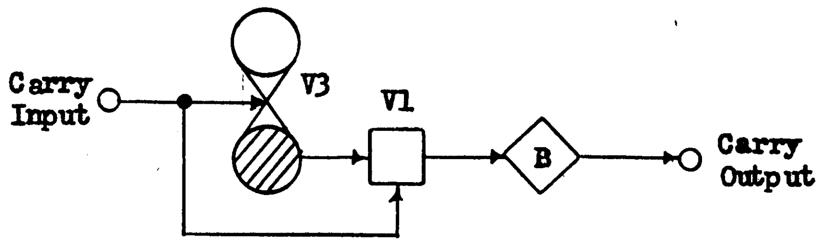
NOTES:
1. FILAMENTS OF V2 & V3 TO C4 & C12
2. FILAMENTS OF V1 & V4 TO C3 & C11
3. G_3 OF V2 TO K OF V2

TEST POINTS:
#1 Y DEFLECTION
#2 X DEFLECTION

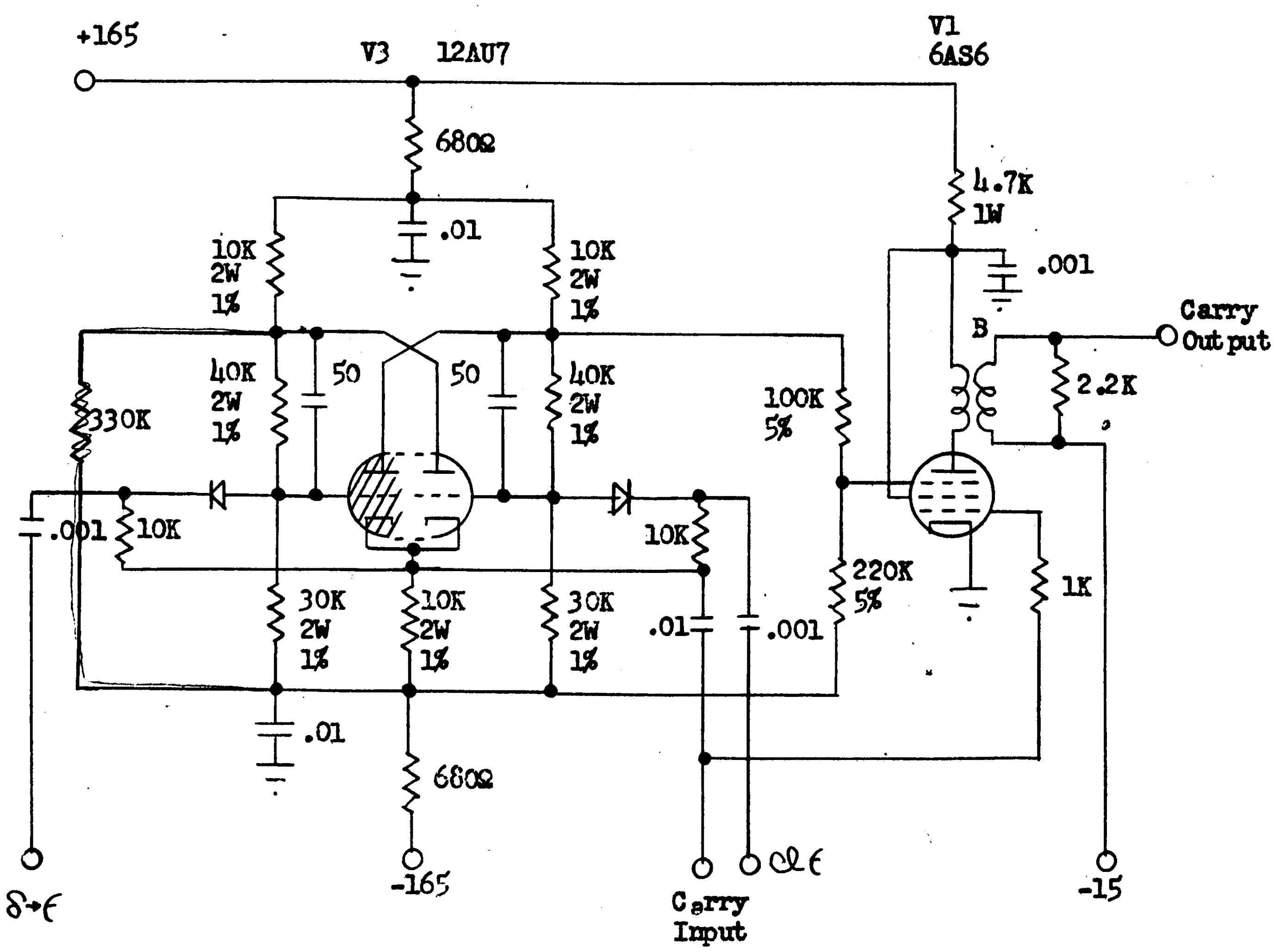
LEJ

3.1 $\mathcal{E}$ Counter. (Supersedes page B3.1-2 dated 5-15-52)

Block Diagram of Counter Stage:

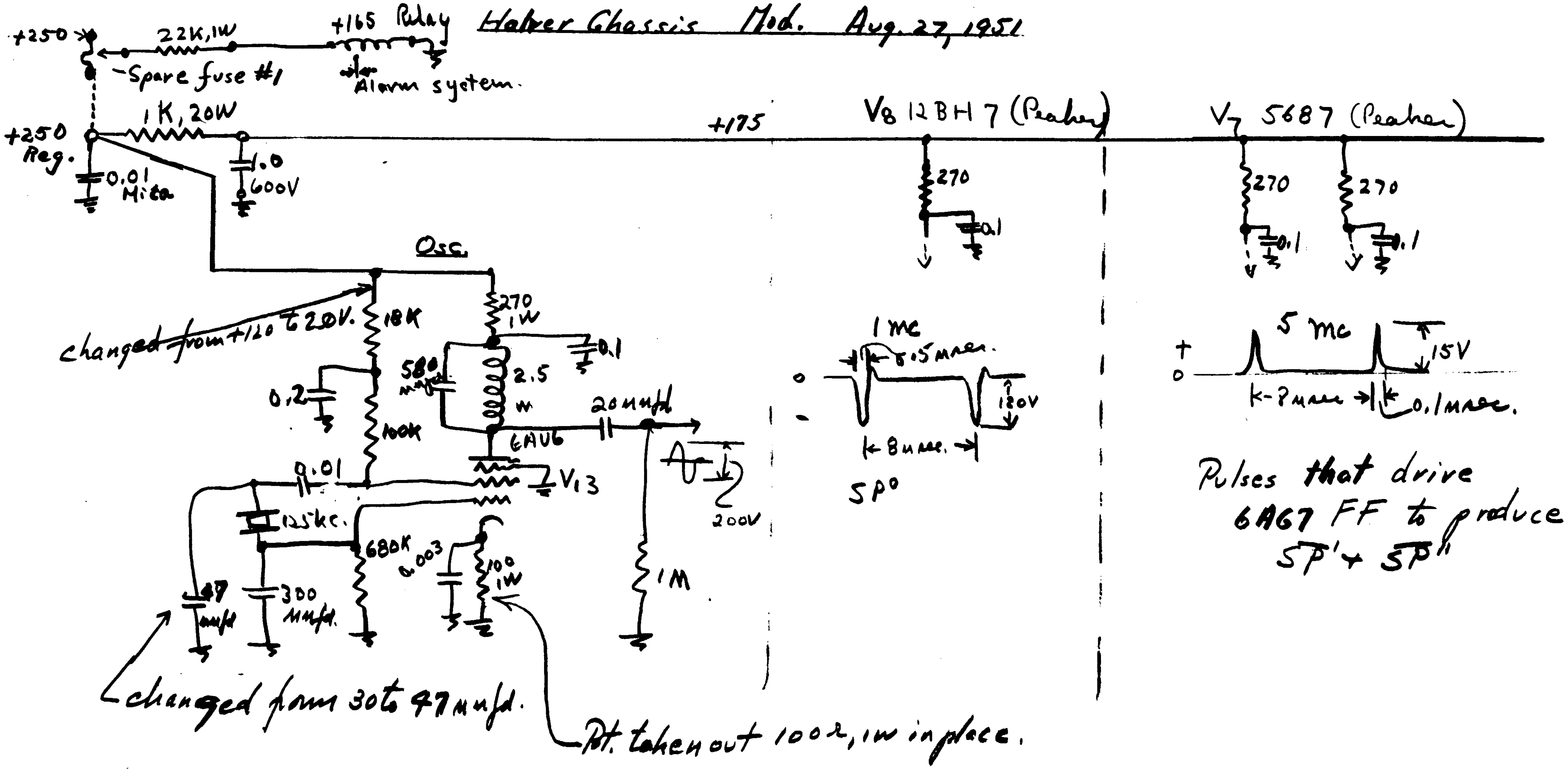


Schematic Diagram of Counter Stage:



H.F.R.
C.H.K.

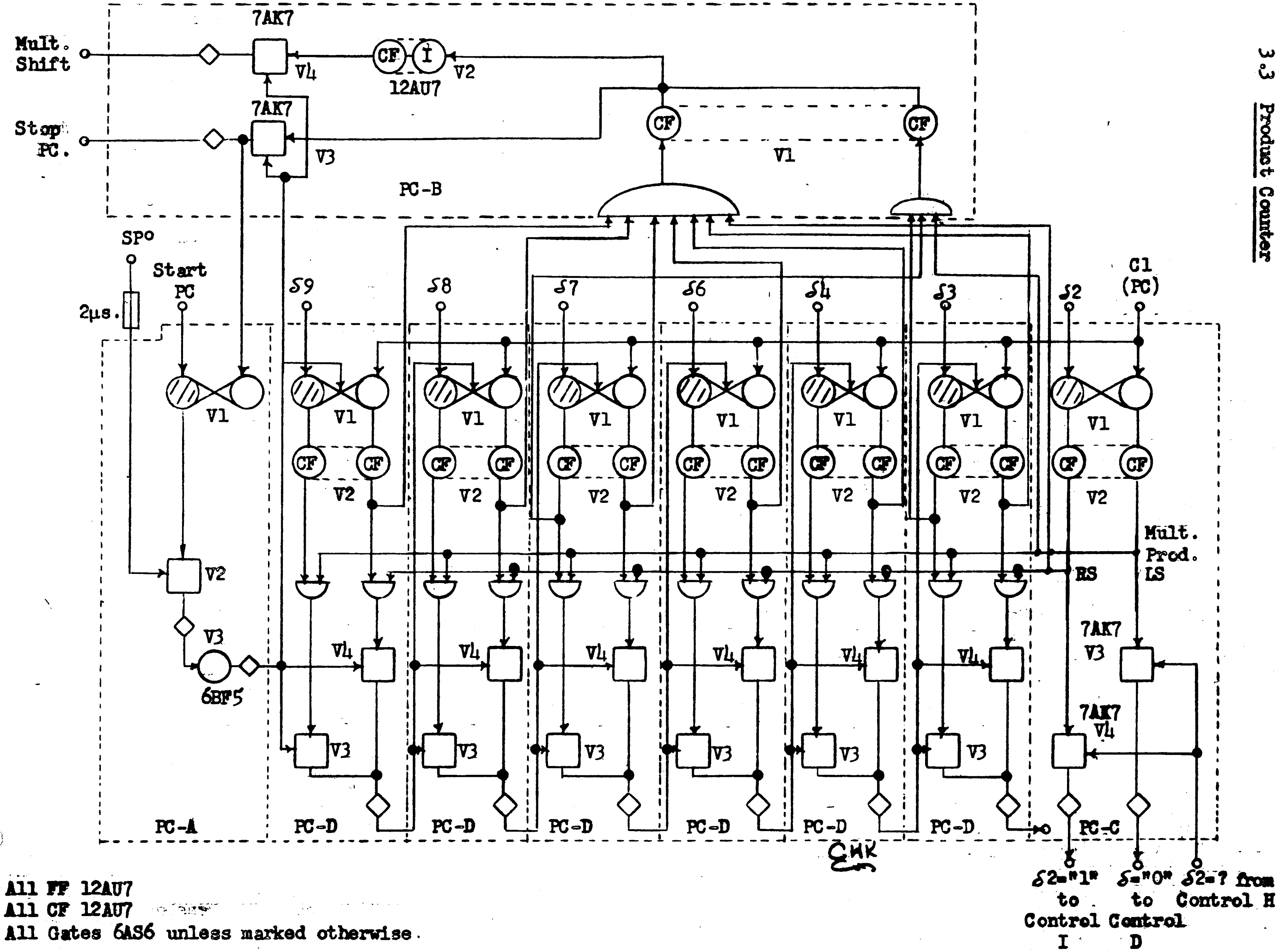
3.2 Halver Chassis Modification.



Modifications – Osc. (125 kc.), + two Peakers V7, + V8 run off +250 Reg. B.F.A. A.C.K.

3.3 Product Counter

BLOCK DIAGRAM



All FF 12AU7
All CF 12AU7
All Gates 6AS6 unless marked otherwise

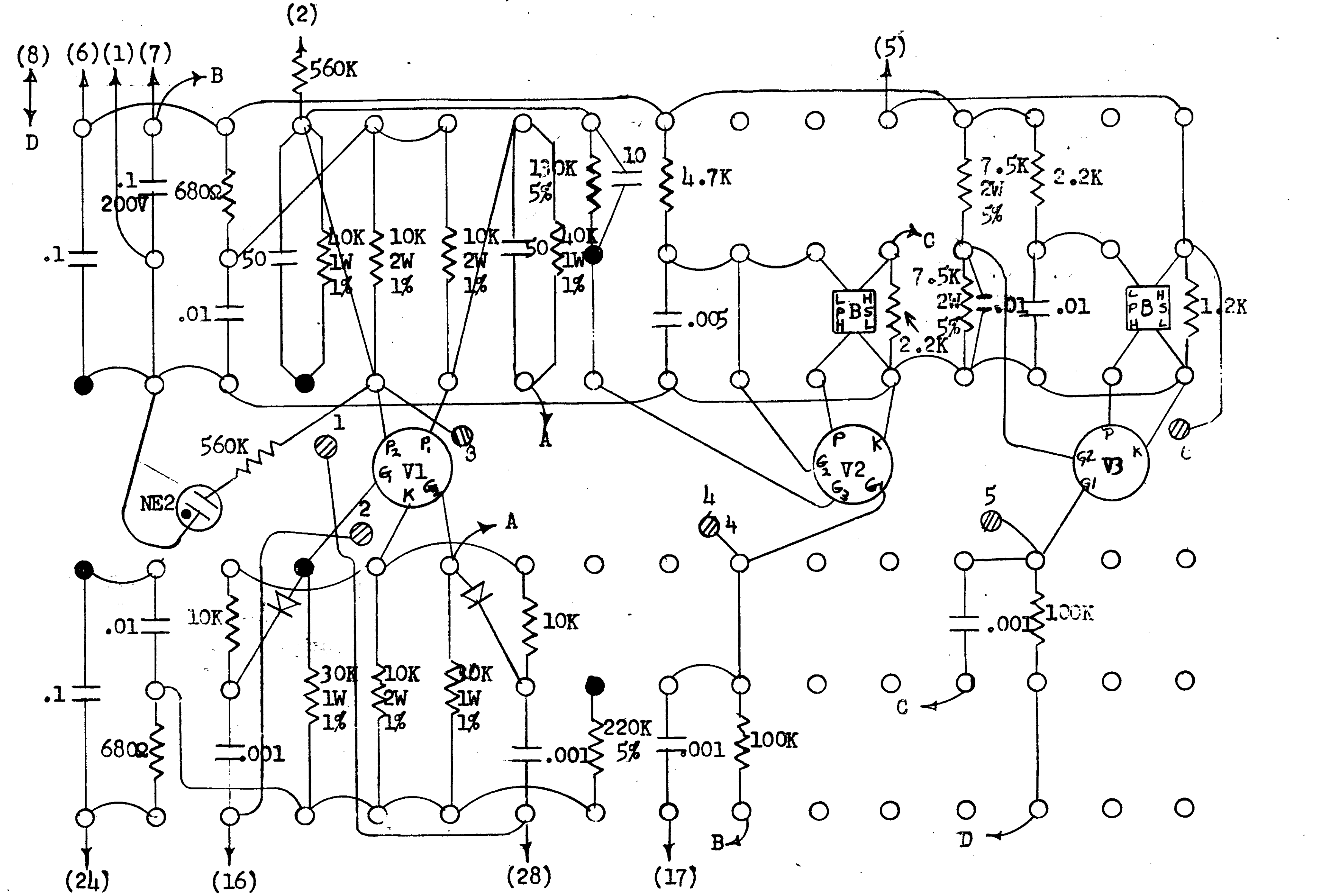
CHK

1.7.1

3.3 Product Counter

Plug-In Unit PC-A Layout:

(Note: this page supersedes page B3.3-2 dated 6-27-52 which is now obsolete)



CANNON PLUG CONNECTIONS:

1.	Ground	8.	-25V	15.	NC	22.	NC
2.	Neon	9.	NC	16.	Stop PC	23.	NC
3.	NC	10.	NC	17.	SP°	24.	-165V
4.	NC	11.	NC	18.	6.3V	25.	NC
5.	Counter Input	12.	6.3V	19.	NC	26.	NC
6.	+165V	13.	NC	20.	NC	27.	NC
7.	-15V	14.	NC	21.	NC	28.	Start PC

NOTES: V1 = 12AU7, V2 = 6AS6, V3 = 6BF5

Numbered shaded circles are test points:

1. Stop PC
2. Start PC
3. FF
4. SP°
5. G_1 V4
6. Counter Input

n.a.L.

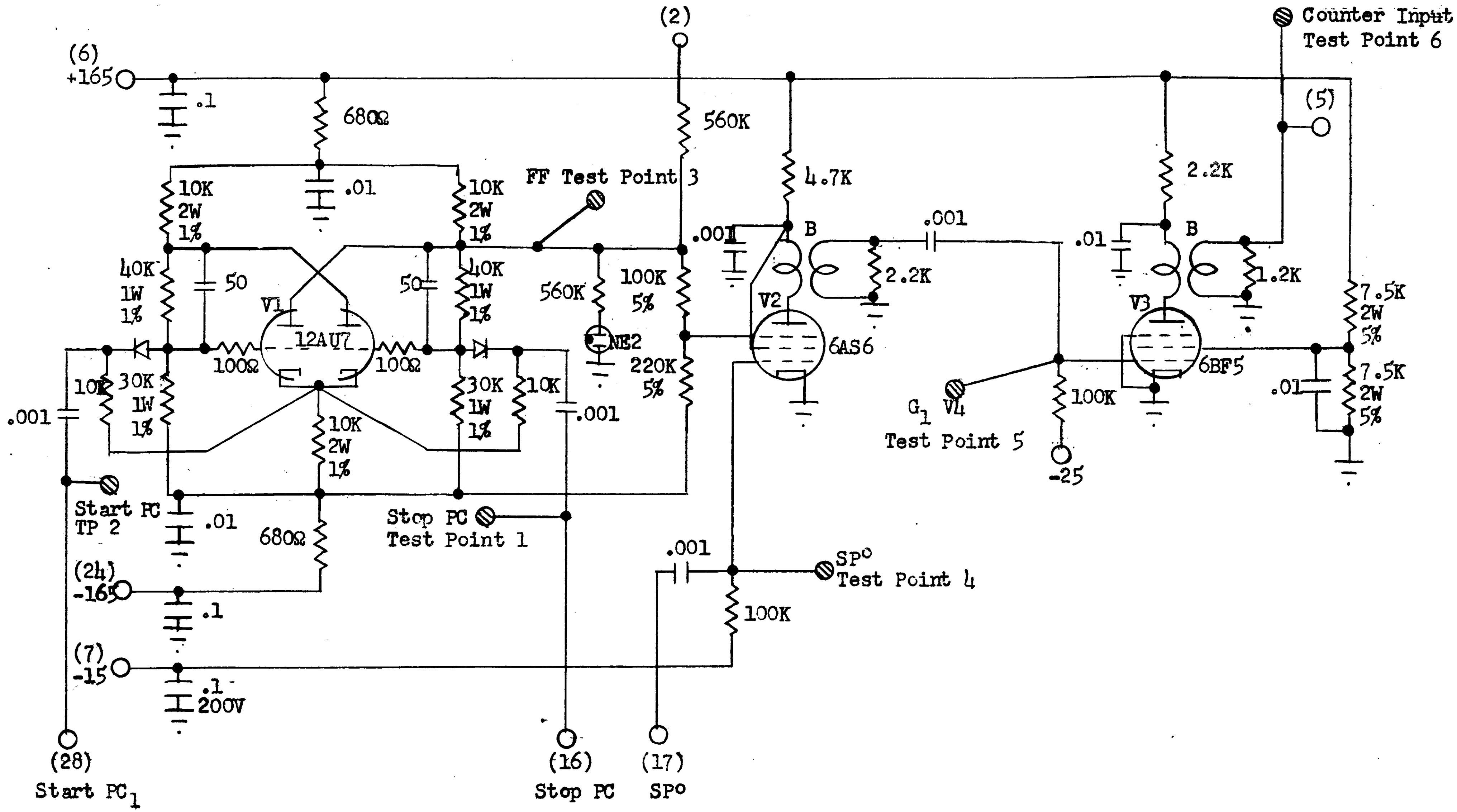
NATIONAL BUREAU OF STANDARDS

3. CONTROL UNIT

Issued 2-25-53

3.3 Product Counter

Plug-In Unit PC-A Schematic:



n.f.l.

INA 51-4
B 3.3-3

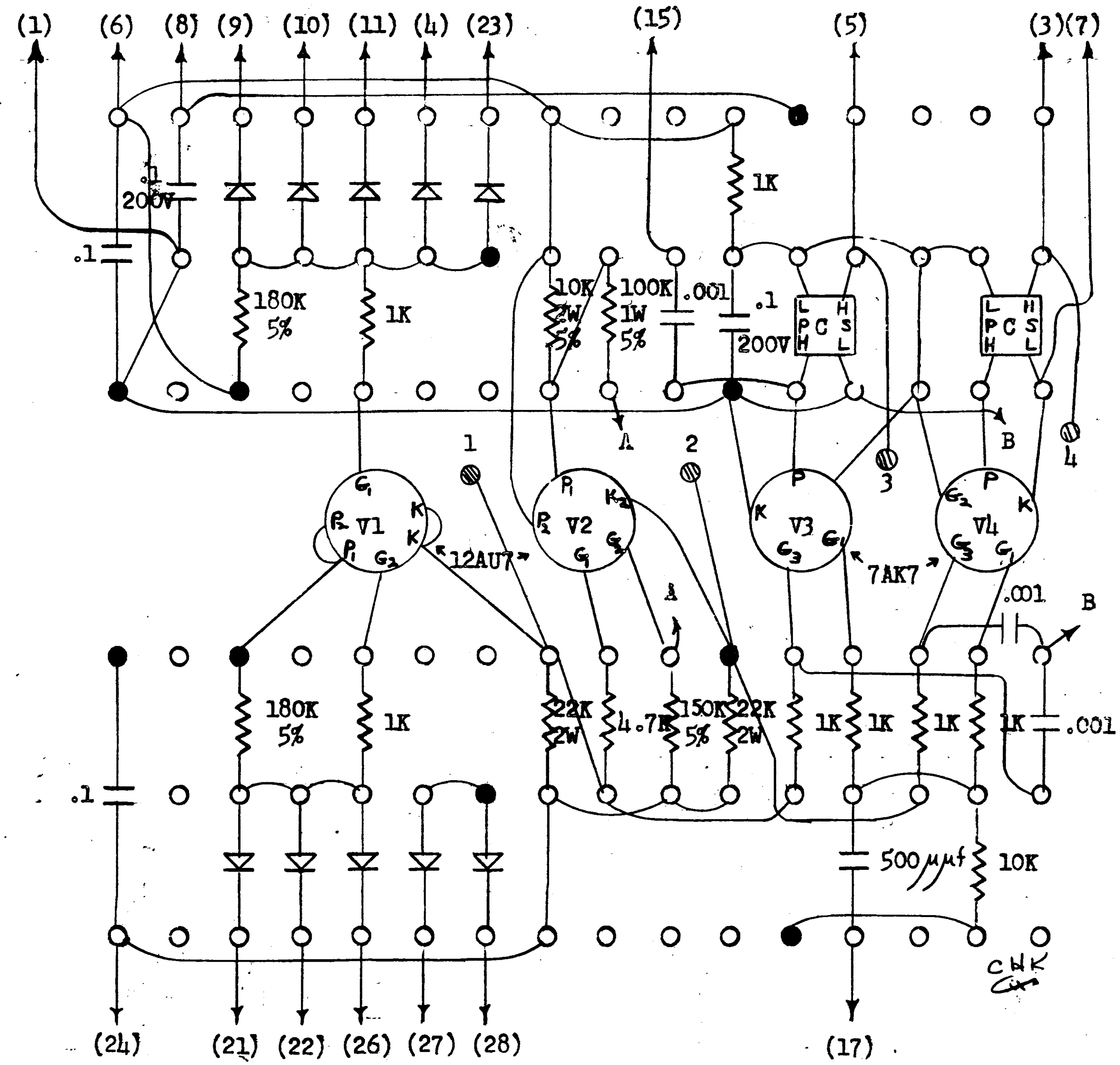
3.3 Product Counter

Plug-In Unit PC-B Layout:

CANNON PLUG CONNECTIONS:

1. Ground
2. NC
3. Shift
4. "0" from 8 Stage
5. Stop PC (positive)
6. +165V
7. -15V
8. -25V
9. "0" from 1 Stage
10. "0" from 2 Stage
11. "0" from 4 Stage
12. 6.3V
13. NC
14. NC
15. Stop PC (negative)
16. NC
17. Counter Input
18. 6.3V
19. NC
20. NC
21. "1" from 4 Stage
22. Left Shift
23. Right Shift
24. -165V
25. NC
26. "1" from 32 Stage
27. "0" from 16 Stage
28. "0" from 32 Stage

NOTE: V1, V2 = 12AU7
V3, V4 = 7AK7

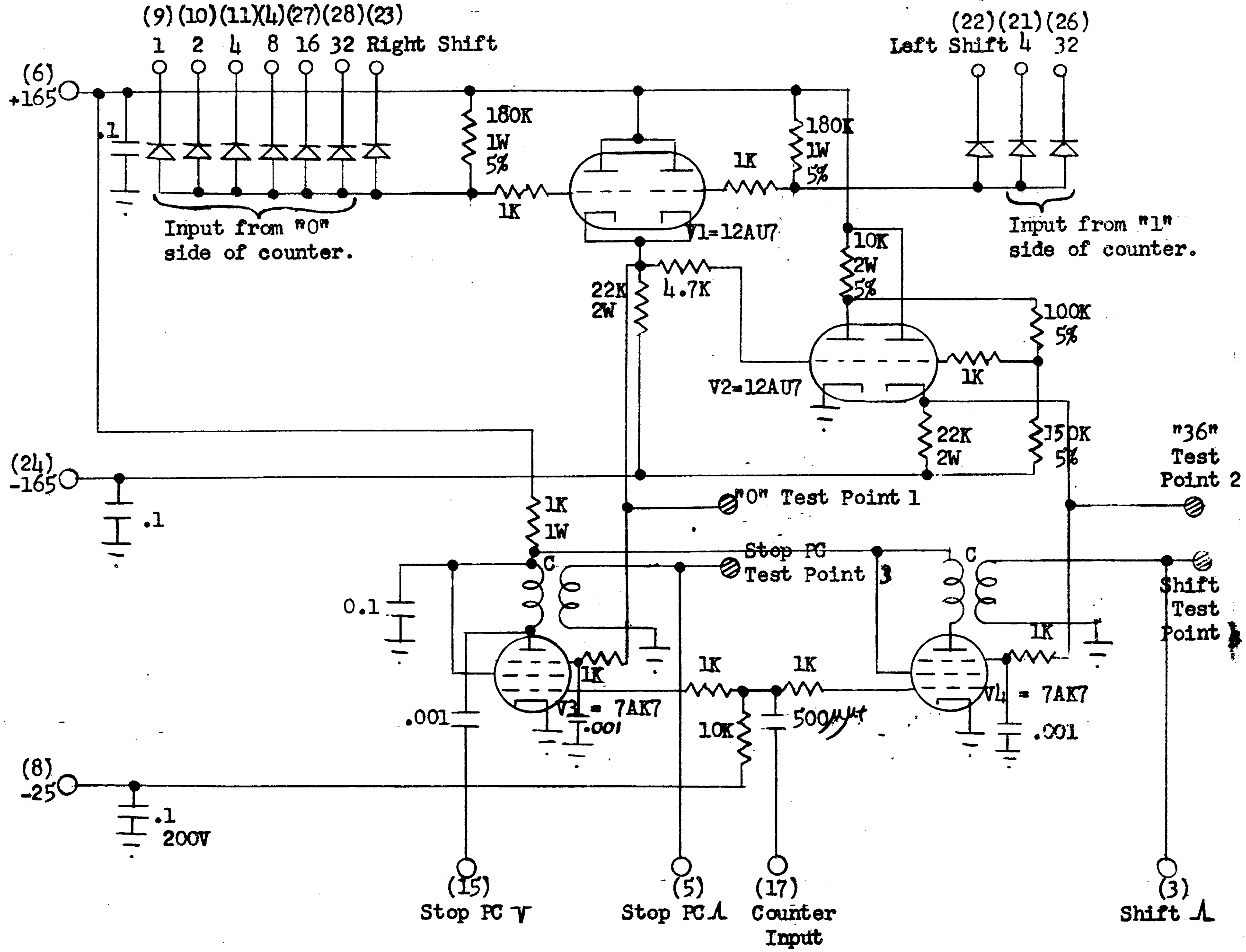


n.7.L

Issued 2-25-53
Reissued 6-26-53

3.3 Product Counter

Plut-In Unit PC-B Schematic:



Issued 2-25-53

3.3 Product Counter

Plug-In Unit PC-C Layout:

CANNON PLUG CONNECTIONS:

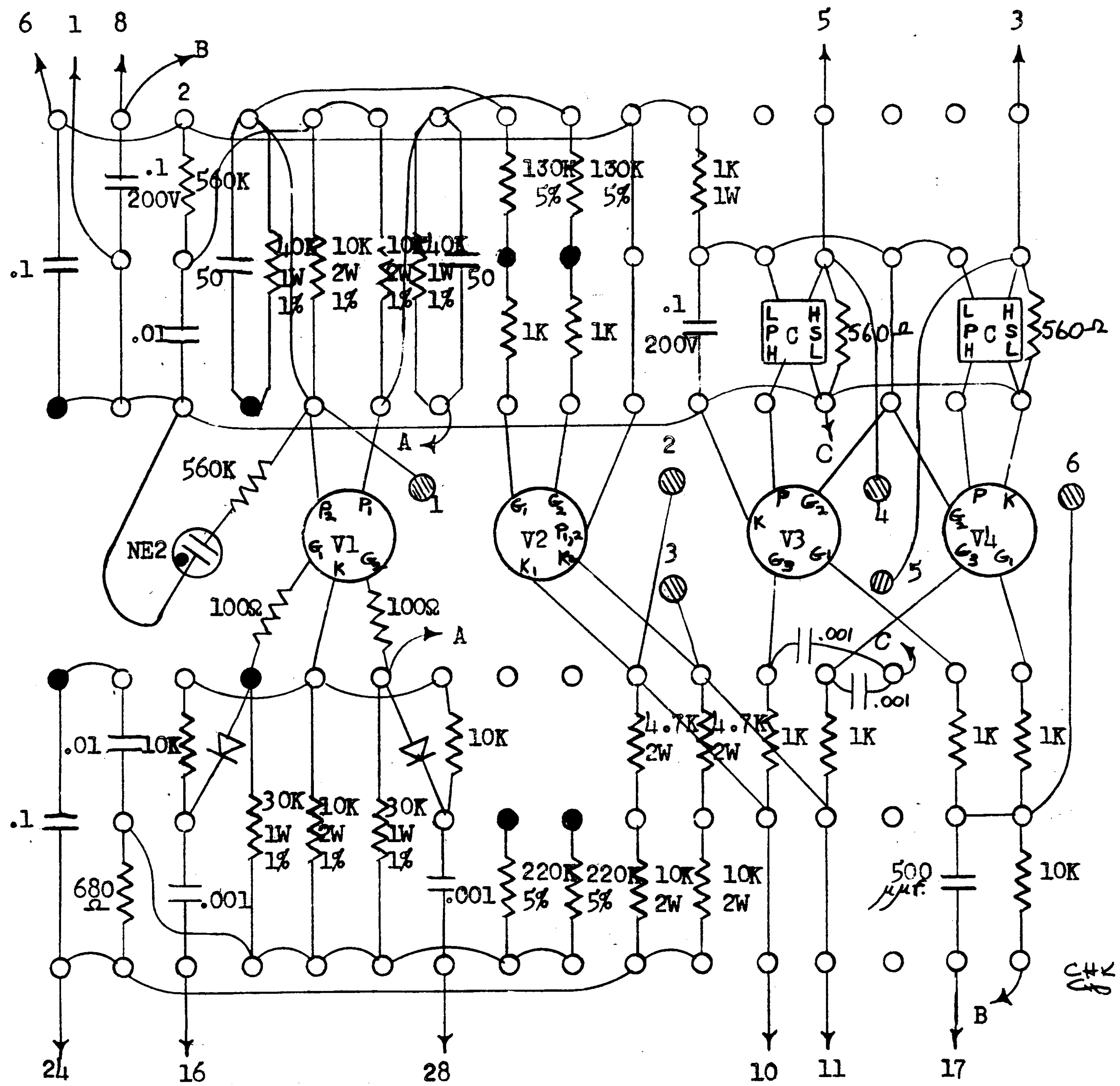
1. Ground
2. Neon
3. $\delta 2 = 1$
4. NC
5. $\delta 2 = 0$
6. +165V
7. -15V
8. -25V
9. NC
10. Right Shift
11. Left Shift
12. 6.3V
13. NC
14. NC
15. NC
16. C1(PC)
17. $\delta 2 = ?$
18. 6.3V
19. NC
20. NC
21. NC
22. NC
23. NC
24. -165V
25. NC
26. NC
27. NC
28. $\delta 2 \rightarrow$ PC

NOTES:

V1 = 12AU7
V2 = 12AU7
V3, V4 = 7AK7

Numbered shaded circles are test points:

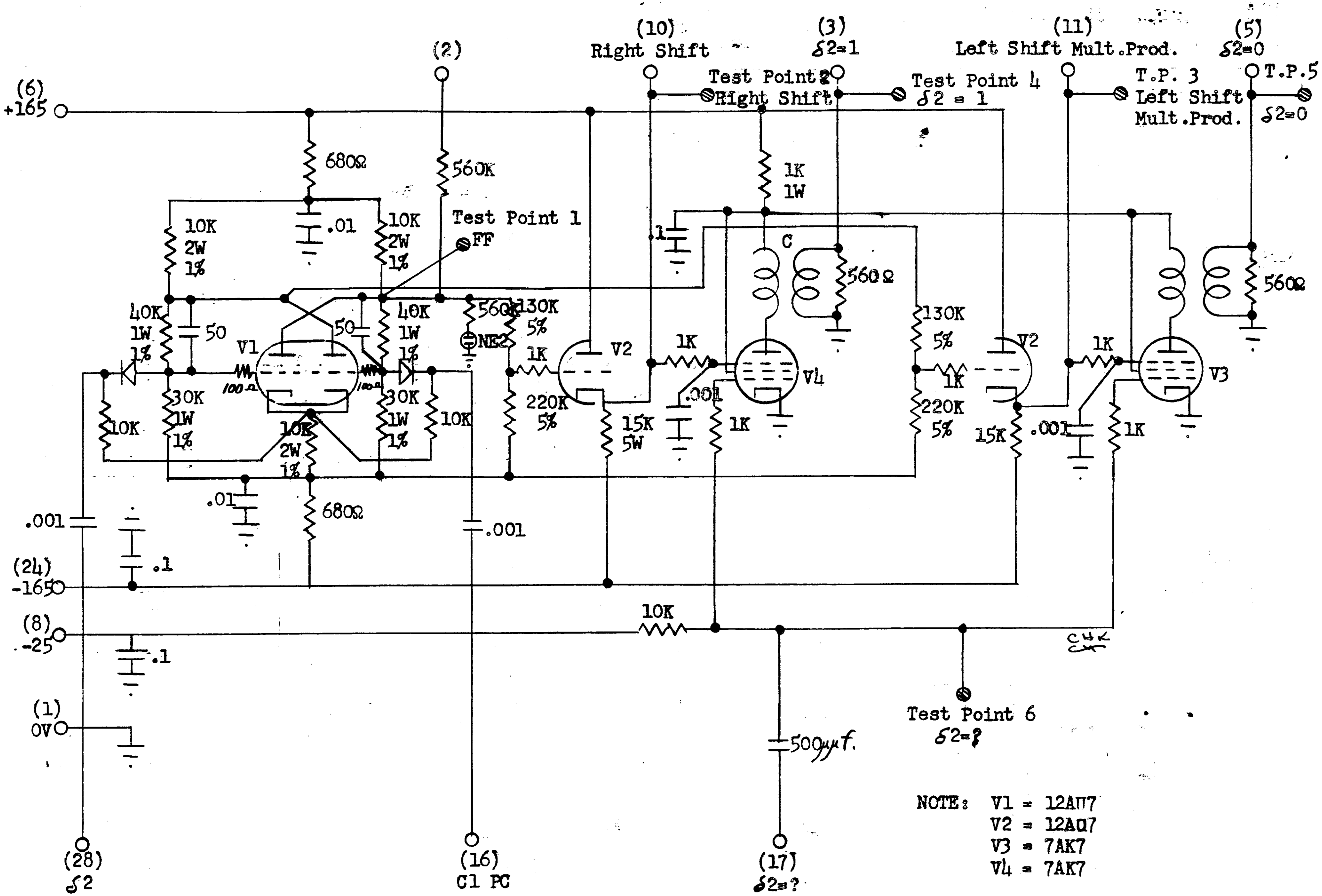
1. FF
2. Right Shift
3. Left Shift
4. $\delta 2 = 1$
5. $\delta 2 = 0$
6. $\delta 2 = ?$



Issued 2-25-53

3.3 Product Counter

Plug-In Unit PC-C Schematic:



Issued 2-25-53

3.3 Product Counter

Plug-In Unit PC-D Layout:

CANNON PLUG CONNECTIONS:

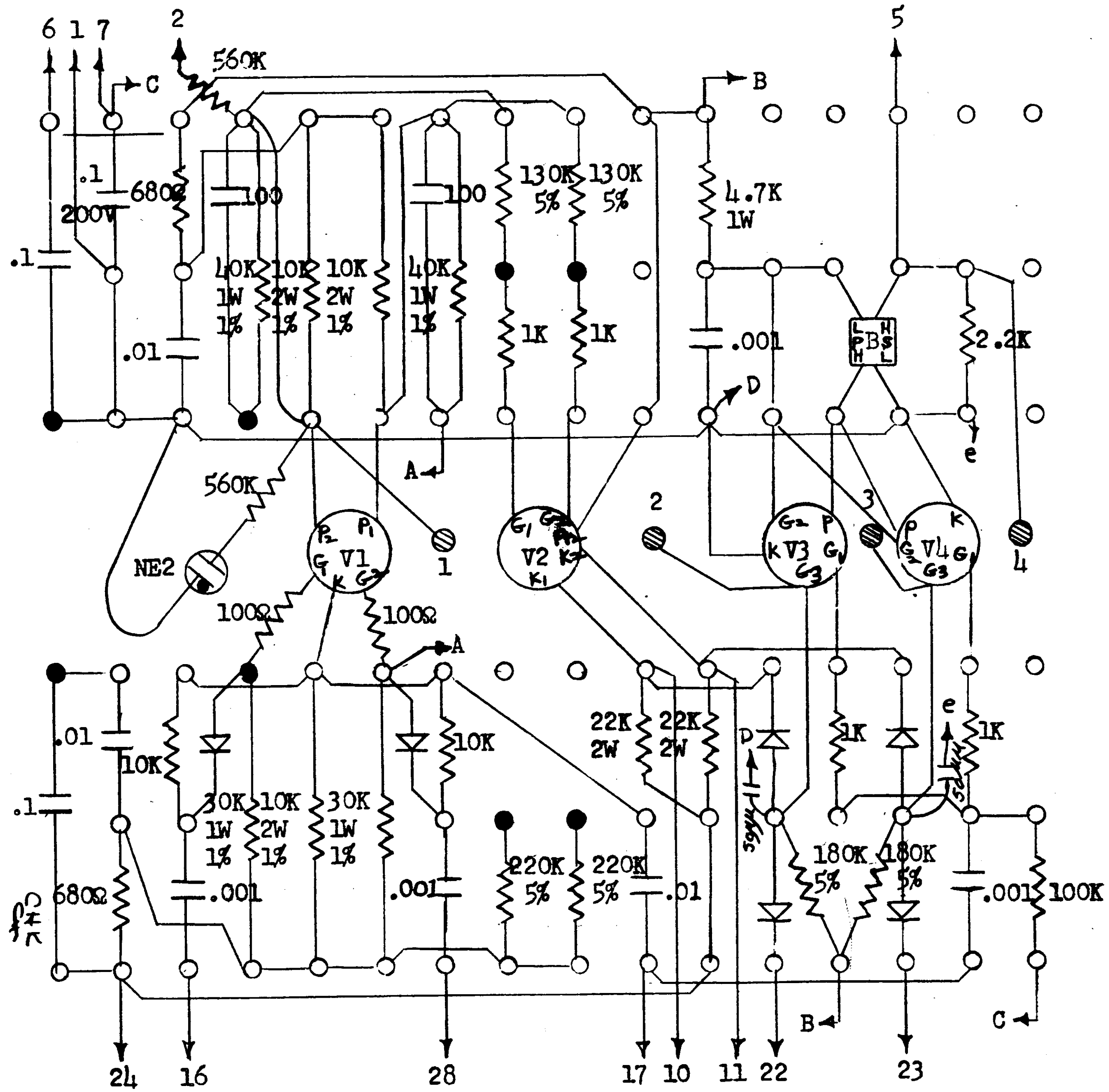
1. Ground
2. Neon
3. NC
4. NC
5. Carry Output
6. +165V
7. -15V
8. -25V
9. NC
10. Hi on "1" } To PC-B
11. Hi on "0"
12. 6.3V
13. NC
14. NC
15. NC
16. C1(PC)
17. Carry Input
18. 6.3V
19. NC
20. NC
21. NC
22. Mult, Prod, and Left Shift
23. Right Shift
24. -165V
25. NC
26. NC
27. NC
28. δ → PC

NOTES:

V1,V2 = 12AU7
V3,V4 = 6AS6

Numbered shaded circles are test points:

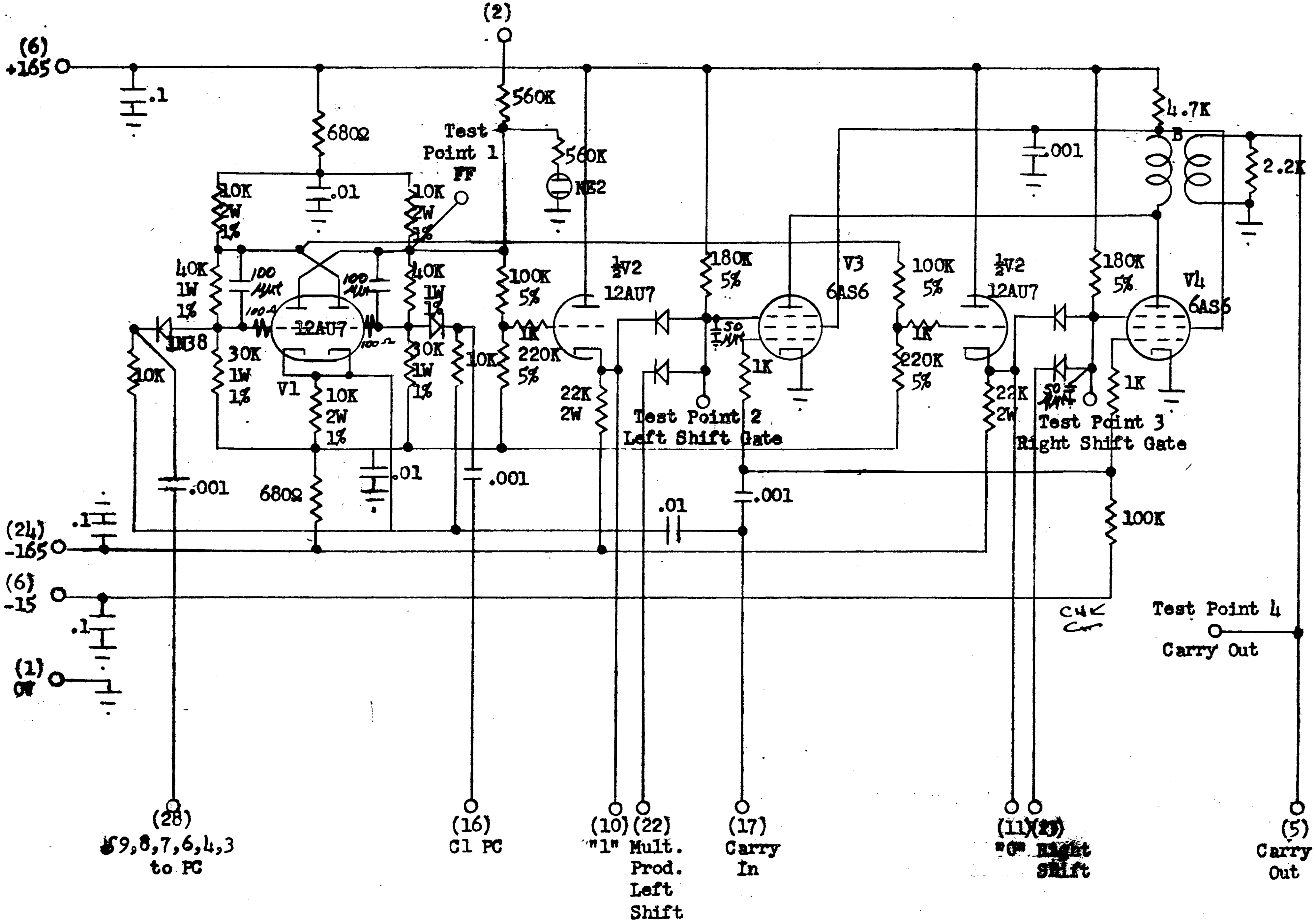
1. FF
2. Left Shift Gate
3. Right Shift Gate



3.3 Product Counter

Issued 2-25-53
Reissued 6-26-53

Plug-In Unit PC-D Schematic:



n.7.l.

3.3 Product Counter

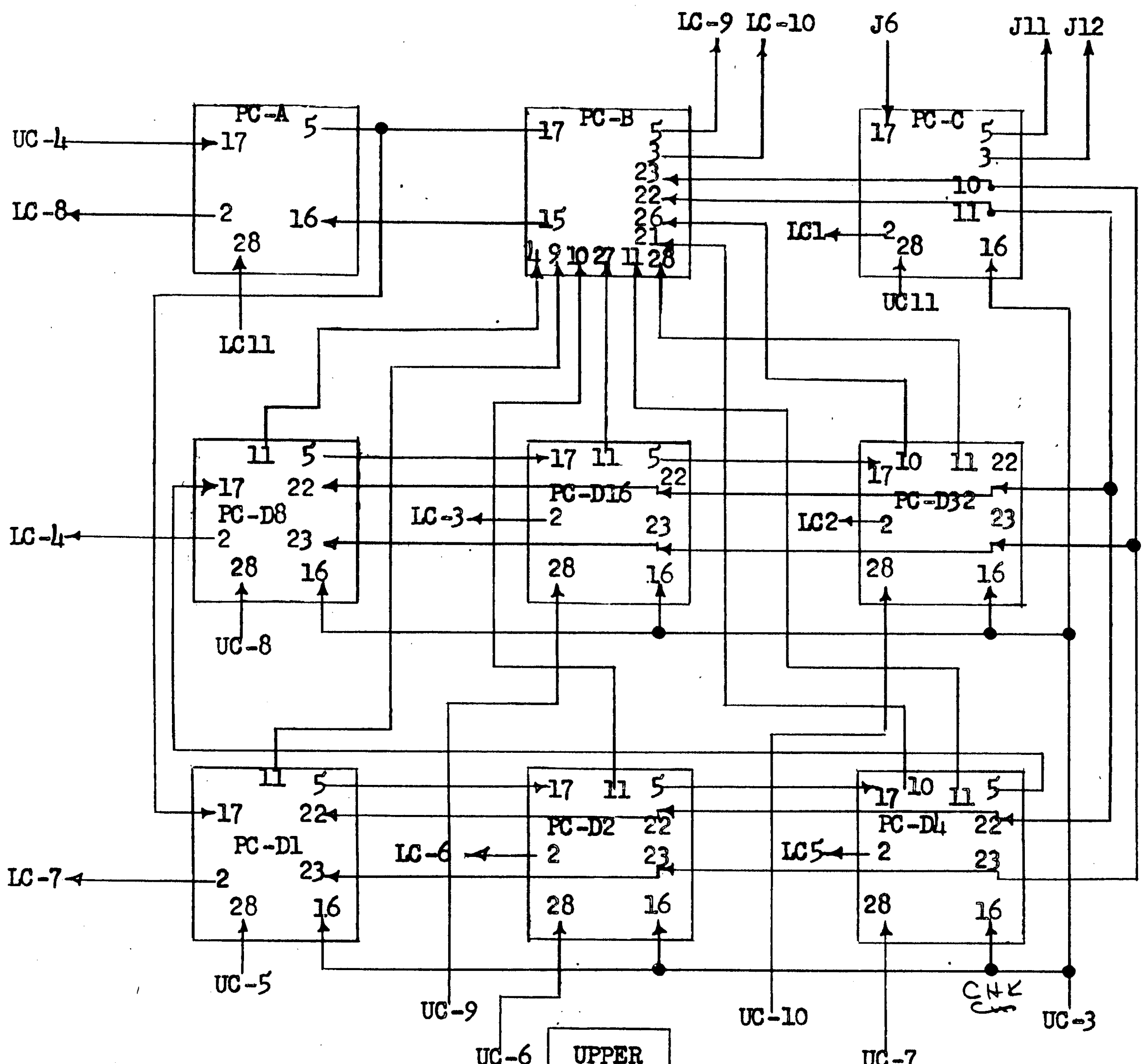
Wiring for Back of Product Counter Panel:

JONES PLUG CONNECTIONS:

1. 6.3V Gnd.Side
2. NC
3. NC
4. NC
5. 6.3V
6. $\delta 2=?$
7. +165V
8. -25V
9. -165V
10. -15V
11. $\delta 2=1$
12. $\delta 2=0$

Jones

11	12
9	10
7	8
5	6
3	4
1	2



UPPER CANNON PLUG-UC

LOWER CANNON PLUG-LC

UPPER CANNON PLUG CONNECTIONS:

1. NC
2. SP^0
3. C1(PC)
4. 2.0µs delay
5. $\delta 9 \to$ PC
6. $\delta 8 \to$ PC
7. $\delta 7 \to$ PC
8. $\delta 6 \to$ PC
9. $\delta 4 \to$ PC
10. $\delta 3 \to$ PC
11. $\delta 2 \to$ PC
12. Out to 2.0µs delay

LOWER CANNON PLUG CONNECTIONS:

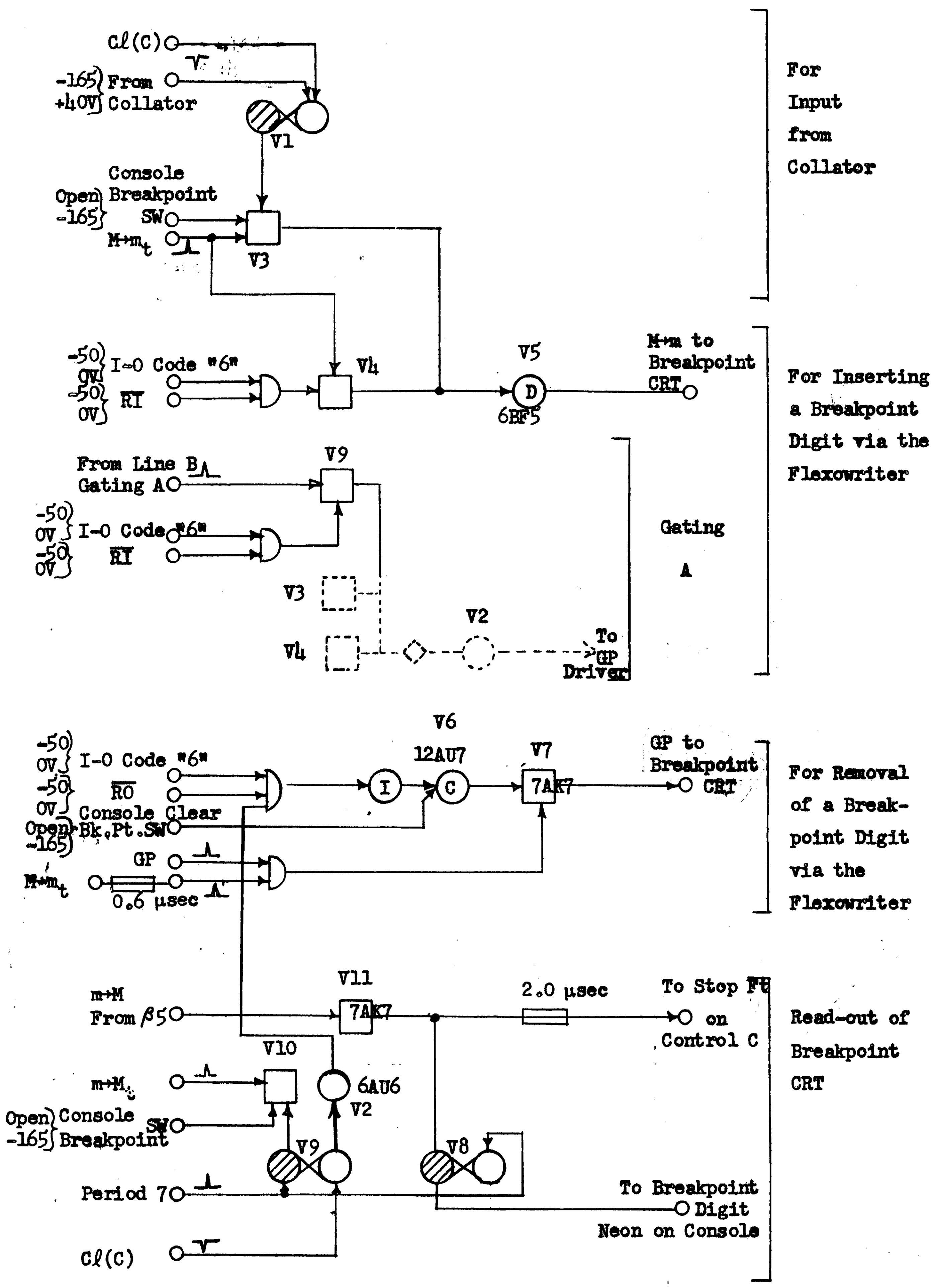
1. $\delta 2$ neon
2. $\delta 3$ neon
3. $\delta 4$ neon
4. $\delta 6$ neon
5. $\delta 7$ neon
6. $\delta 8$ neon
7. $\delta 9$ neon
8. Start neon
9. Stop PC
10. Shift and Add
11. Start PC
12. NC

NOTE: UC-2 connected to UC-12 on PC Panel.

N. J. L.

3.4 Breakpoint Operation.

Block Diagram for Breakpoint Control Chassis:



3.4 Breakpoint Operation.

A. Breakpoint Chassis.

The Breakpoint Chassis is located in position $A_3 - 18_2$ of the Arithmetic Section of SWAC and is shown in block diagram on page B3.4-1 of the Engineering Manual.

B. Collator Input.

When an IBM card has a hole punched in column 79 in the row being read by the collator, flipflop V1 is set allowing a $M \rightarrow m_t$ pulse to read a "one" into the Breakpoint CRT in position $\beta 5$. During the following machine cycle a Cl(C) pulse (Period 8) will clear the V1 flipflop preparing it for subsequent input. The action of the gate V3 is allowed or inhibited dependent upon the position of the Breakpoint switch located on the console.

C. Insertion of Breakpoint Digit.

To insert a Breakpoint Digit in an address an input breakpoint command (60 in δ) with the desired address in α is obeyed. V4 controls the input of a "one" to the Breakpoint CRT and V9 on Gating A allows for regeneration of the rest of the memory. This input breakpoint command is the only input command in which the contents of the address is regenerated.

D. Removal of Breakpoint Digit.

To remove a Breakpoint Digit from an address an output breakpoint command (60 in δ) with the desired address in α is obeyed. V7 and V6 inhibit GP for the read-out of the address in α, thus writing a "zero" in the Breakpoint CRT.

E. Read-out of Breakpoint CRT.

For read-out V11 senses the output of the CRT. The gate pulse to V11is derived from $m \rightarrow M_t$ but allowed only during Period 7. Thus, Breakpoint Digits will be affective only when in command words. This is controlled by V9 and V10. Flipflop V8 is set if a Breakpoint Digit is present in a command and lights the console Breakpoint neon. This

3.4 Breakpoint Operation.

flipflop is cleared by Cl(C) (Period 8). Read-out of the Breakpoint CRT can be inhibited by putting the console Breakpoint switch down in the OFF position.

The delay line which delays the Stop Ft 2.0 microseconds is located in back of the control rack.

F. Breakpoint Switch (on console).

The console switch marked "Breakpoint" inhibits collator input to the Breakpoint CRT (β5) and also inhibits read-out of the β5 CRT which causes the machine to halt if a "one" is stored. This switch has no affect on insertion or removal of Breakpoint Digits into β5 CRT. Breakpoint Digit action is inhibited when switch is down in the OFF position, allowed when switch is up in the ON position. The Breakpoint CRT β5 is cleared when the Breakpoint switch is pushed up to the momentary contact position marked "Clear".

G. Additional Information.

$M \rightarrow m_t$ delayed 0.6 μsec is mixed with GP so that the Breakpoint CRT will receive a regeneration gate pulse during a normal read-in. This prevents loss of Breakpoint Digits during normal read-in.

Flipflop V9 coupled through V2 is used to insure the presence of a GP during Period 7 read-out. If I-O code "6" and $\overline{RO}$ were present during Period 7, without V2 input as an inhibitor, a Breakpoint Digit in the command being read out would be removed.

4. POWER SUPPLY

4.1 SWAC Power Specifications.

SUMMARY OF FILAMENT SUPPLIES FOR SWAC

Item	Transf. Ser.No.	Volt. Ref.	Rated Breakdown	Rated Amps/Phase	K.W.
Arith. Units	9717	0	2500 V.	135	2.55
Arith. Units	9718	-165	2500 V.	100	1.89
Input-Output	9719	0	2500 V.	60	1.13
Control + "C" Reg. + CRT Control	9720	0	2500 V.	60	1.13
All 0 Volt Regulator Heaters	9721	0	2500 V.	75*	-
CRT Tube + 12AU7 + 6AL5	9722	-1800	5000 V.	70*	0.44
+165V Reg. Series Arm	9723	+165	2500 V.	60*	0.28
CRT Amplifier Regulator	9724	+250	2500 V.	60*	0.25
-330V Heaters in SWAC	9725	-330	2500 V.	8*	0.03
+200V Reg. Series Arm	9726	+200	2500 V.	20*	-
Summation Volt. Reg. Series Arm	9727	+250	2500 V.	20*	-
D.C. Supply for CRT Amplifiers, Deflection Drivers, Deflection Adders, Sawtooth Chassis		0	2500 V.	-	-
2-Thordarson Type T-21F10 for:					
-165V Reg. Amplifier		-165	1600 V.	3*	-
-330V Reg. Amplifier		-330	1600 V.	3*	-
2-Stancor Type 6309 (20 amp) -165V to Input-Output		-165	-	40*	-

* Single ∅ Transformer

NOTE: All transformers to be electrostatically shielded.

4. POWER SUPPLY

4.1 SWAC Power Specifications.

SUMMARY OF UNREGULATED D.C. POWER SUPPLIES FOR SWAC

Item	Volts	Amps.	Power Supply Capacity
Arith. Units	+165	24.30	
CRT Chassis		6.00	
Controls		0.85	
Product Counter		0.015	
Timing Chassis		1.40	
		32.565	40 amperes
Arith. Units	+135 S.G.	5.1	6 amperes
Controls	+120 S.G.	0.015	(Bleeder from +135V)
Arith. Units	+25	6.0	6 amperes
To +165 Reg.	+270		5 amperes
CRT Amplifier	+350	4.0	4.5 amperes
Arith. Units	-15	6.80	
CRT Chassis		0.03	
Controls		0.25	
Product Counter		0.10	
"C" Chassis		0.10	
Timing Chassis		0.20	
		7.48	10 amperes
Arith. Units	-25	4.1	5 amperes
Arith. Units	-165	12.90	
CRT Chassis		.60	
Controls		0.35	
Product Counter		0.18	
Timing Chassis		0.30	
		14.33	20 amperes
Arith. Units	-180	0.5	500 ma.
Controls and Arith.	-330	0.15	150 ma.
HV	0-2000		100 ma.
250 (HV)	350		500 ma.
150 (HV)	200		750 ma.
To -165 Reg.	-270		10 amperes
To -330 Reg.	-425		
Flexo. -165	-165		
" -35	-200		

NOTES: 1) All output leads (both the + and -) must be brought out and insulated from chassis and ground.

2) All supplies to have a regulation of 5% and a ripple voltage of ½%.

4.2 SWAC Power Wiring.

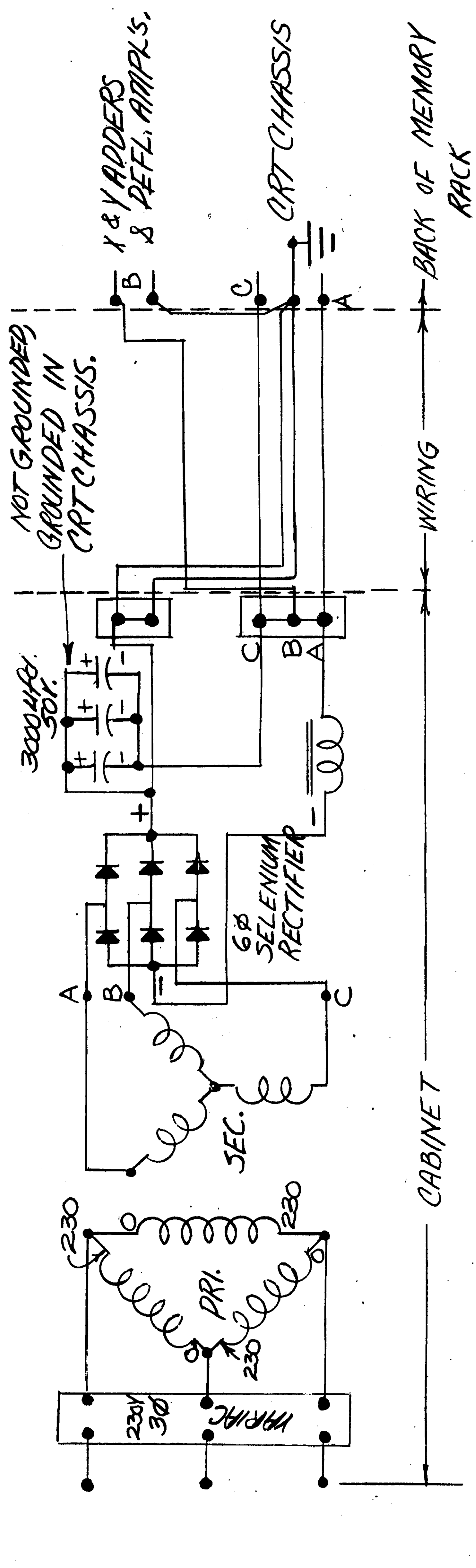
Jones Strip on Side Panel of CRT Section beside Memory Fuse Panel:

Terminal Nos. Start from Top	Voltage		
J1	-165	From: To:	Arithmetic Section Filter Choke back of Memory Control
J2	-25	From: To:	Arithmetic Section -25 Fuses on Memory Control Fuse Panel
J3	+165	From: To:	Power Shed 1) Control Section 2) Memory Control Fuse Panel 3) Memory Fuse Panel
J4	+135	From: To:	Arithmetic Section 1) Memory Fuse Panel 2) Console
J5	+120	From: To:	Power Cabinet 1) Control Section 2) Memory Control Fuse Panel
J6	+25	From: To:	Arithmetic Section Console
J7	-15 Bias	From: To:	Memory Control Switch on Memory Fuse Panel -15 on Memory Control Fuse Panel
J8	-15	From: To:	Arithmetic Section Bias Switches on Memory Fuse Panel
J9	-25	From: To:	-25 Fuse on Memory Control Fuse Panel 1) -15 Bias Pots on Memory Fuse Panel 2) Console
J10	-165	From: To:	-165 Filter Cond. back of Memory Control 1) Memory Fuse Panel 2) Control Fuse Panel 3) Memory Control Fuse Panel
J11	-180	From: To:	Arithmetic Section Console
J12	-330	From: To:	Power Shed 1) Control Fuse Panel 2) Memory Control Fuse Panel 3) Console 4) Arithmetic Fuse Panel A1

LEJ

Unregulated Power Supplies

4.4 D.C. ~~Heater~~ Supply for Memory. (Supersedes page Bl.10-1 issued 8-28-51.)

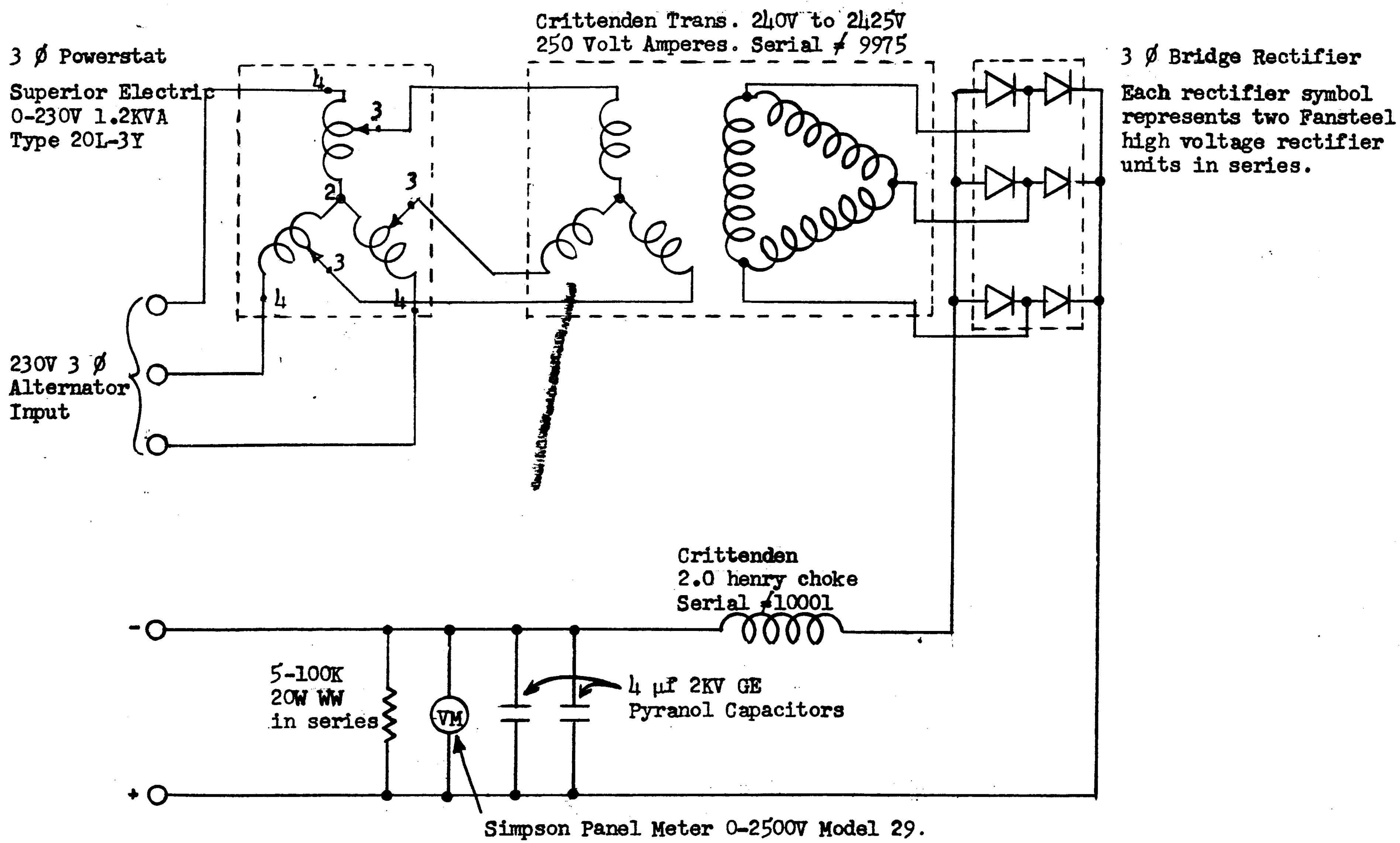


D.C. FILAMENT SUPPLY FOR MEMORY - 300 AMP.

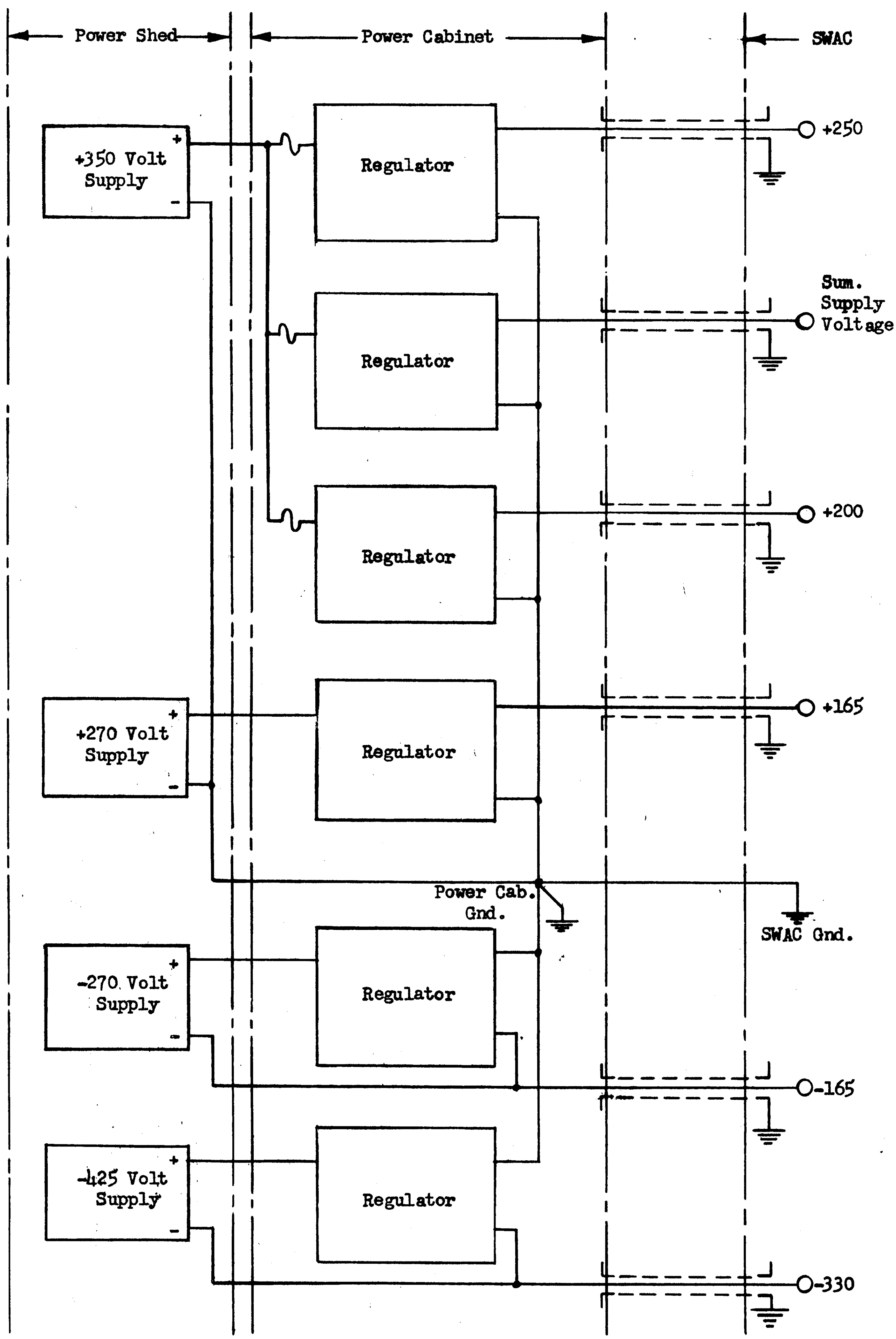
CAM
B.F.A.

4.4 Unregulated Power Supplies.

Memory High Voltage Supply (0-2000V at 0.1 amps):

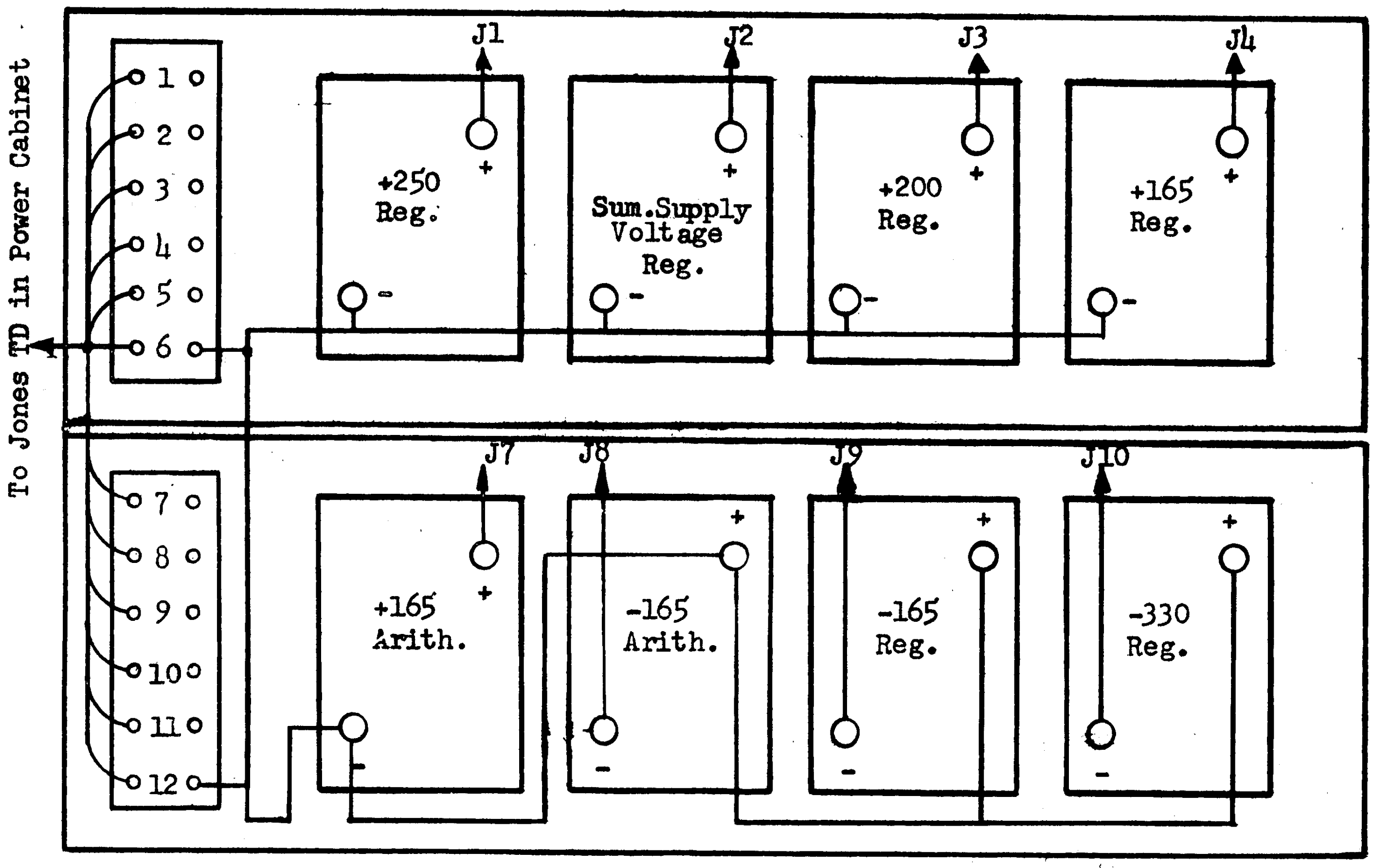


4.5 Voltage Regulator System.



4.5 Voltage Regulator System.

Voltmeters for SWAC Power Supplies:



This meter panel located next to power cabinet.

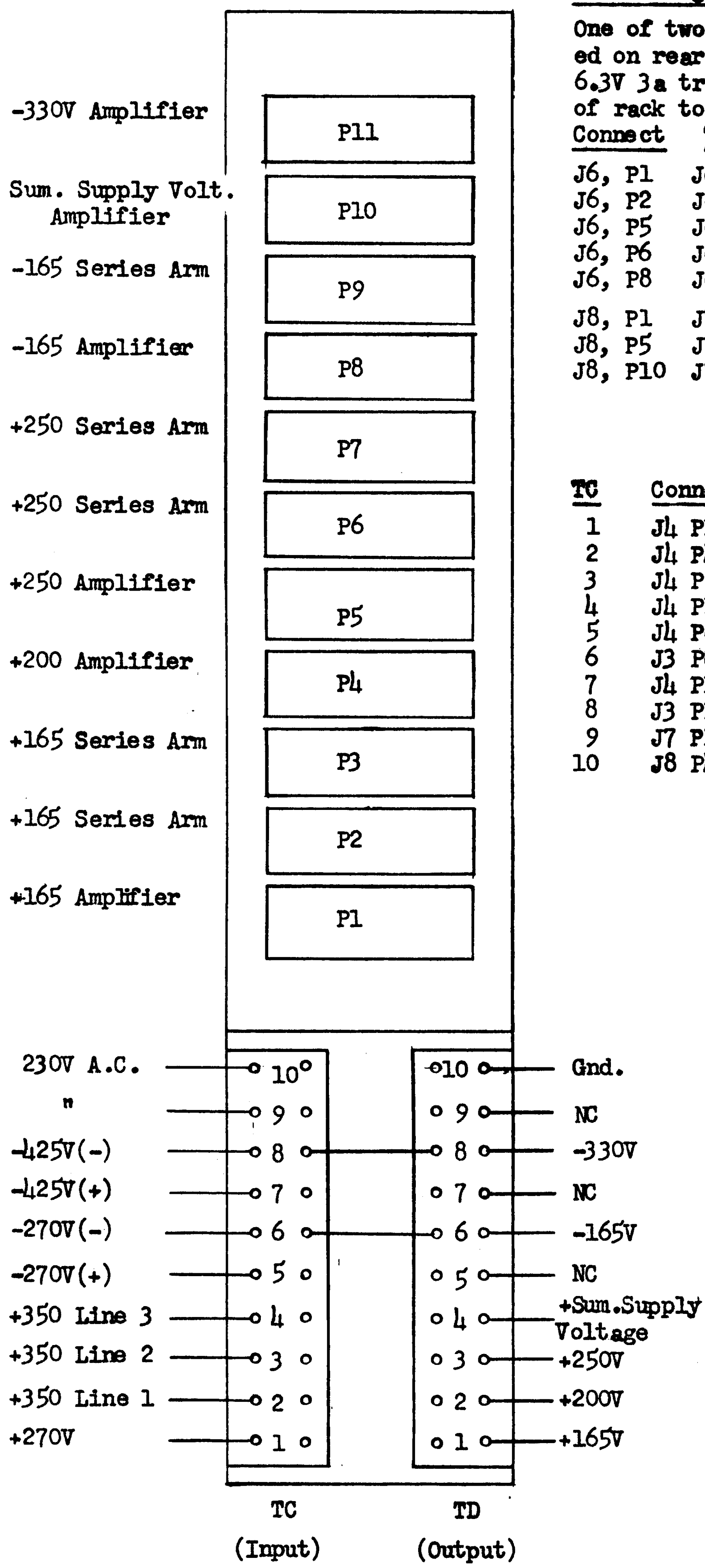
FRONT VIEW

Jones Strip Number	Voltage	Color Code	Connection to Jones Strip TD in Pwr. Cab.
1	+250	Brown	TD 3
2	+ Sum.Supply Volt.	White	TD 4
3	+200	Black	TD 2
4	+165	Large Red	TD 1
5	No Connection	-	-
6	0 V.	Black	TD 10
7*	+165 Arith.	Small Red	-
8*	-165 Arith.	Blue	-
9	-165	Yellow	TD 6
10	-330	Green	TD 8
11	No Connection	-	-
12	0 V.	Black	To J6

* These pins connect to + and - 165 supply busses in Power Cabinet.

4.5 Voltage Regulator System.

SWAC Regulator Rack in Power Cabinet:



Jones Plug Inter-Connections:

One of two 6.3V 3a transformers mounted on rear of rack to P8(J1,J2); other 6.3V 3a transformers mounted on rear of rack to P11(J1,J2).

Connect	To	Notes
J6, P1	J6, P2	Connections for control of Series Arm Chassis by Amplifier Chassis
J6, P2	J6, P3	
J6, P5	J6, P6	
J6, P6	J6, P7	
J6, P8	J6, P9	
J8, P1	J7, P4	Bias Transformers Interconnections. Bias trans. are 115V-prim. in series across 230V A.C.
J8, P5	J7, P8	
J8, P10	J7, P11	

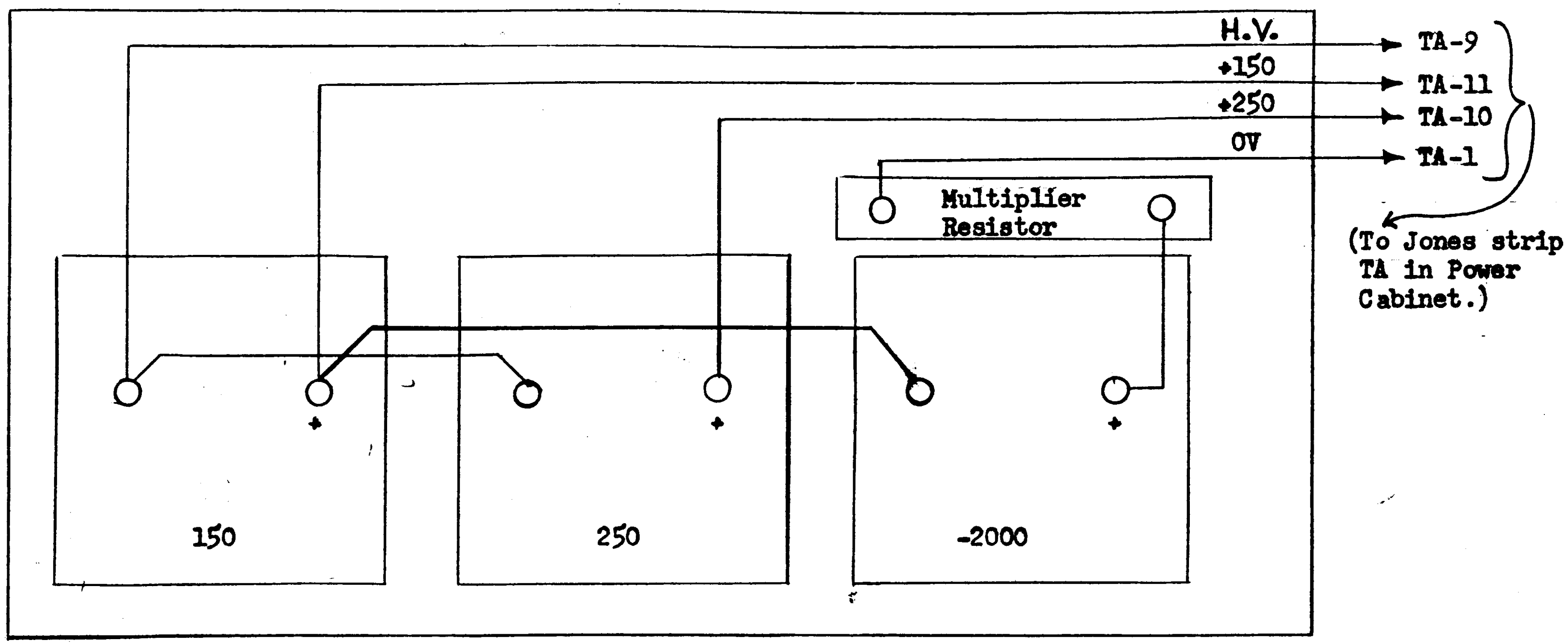
TC	Connected To
1	J4 P1,2,3
2	J4 P4
3	J4 P5,6,7
4	J4 P10
5	J4 P8,9
6	J3 P8
7	J4 P11
8	J3 P11
9	J7 P1,5,10 and to filament transformers - primaries in series
10	J8 P4,8,11

TD	Connected To
1	J5 P1,2,3
2	J5 P4
3	J5 P5,6,7
4	J5 P10
5	NC
6	TC-6
7	NC
8	TC-8
9	NC
10	J3 P1,4,5,10; J5 P8,9,11

Issued 11/24/52
Reissued 10-27-53

4.5 Voltage Regulator System.

Voltmeters for SWAC hi-voltage regulated power supplies:

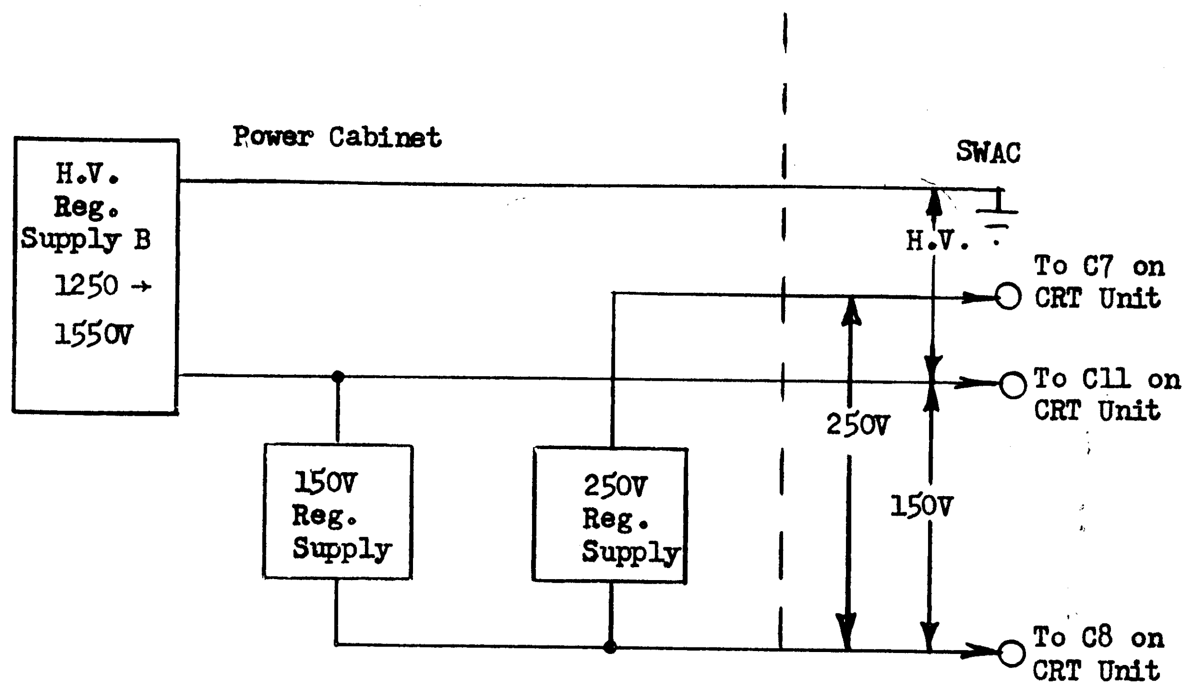


FRONT PHANTOM VIEW

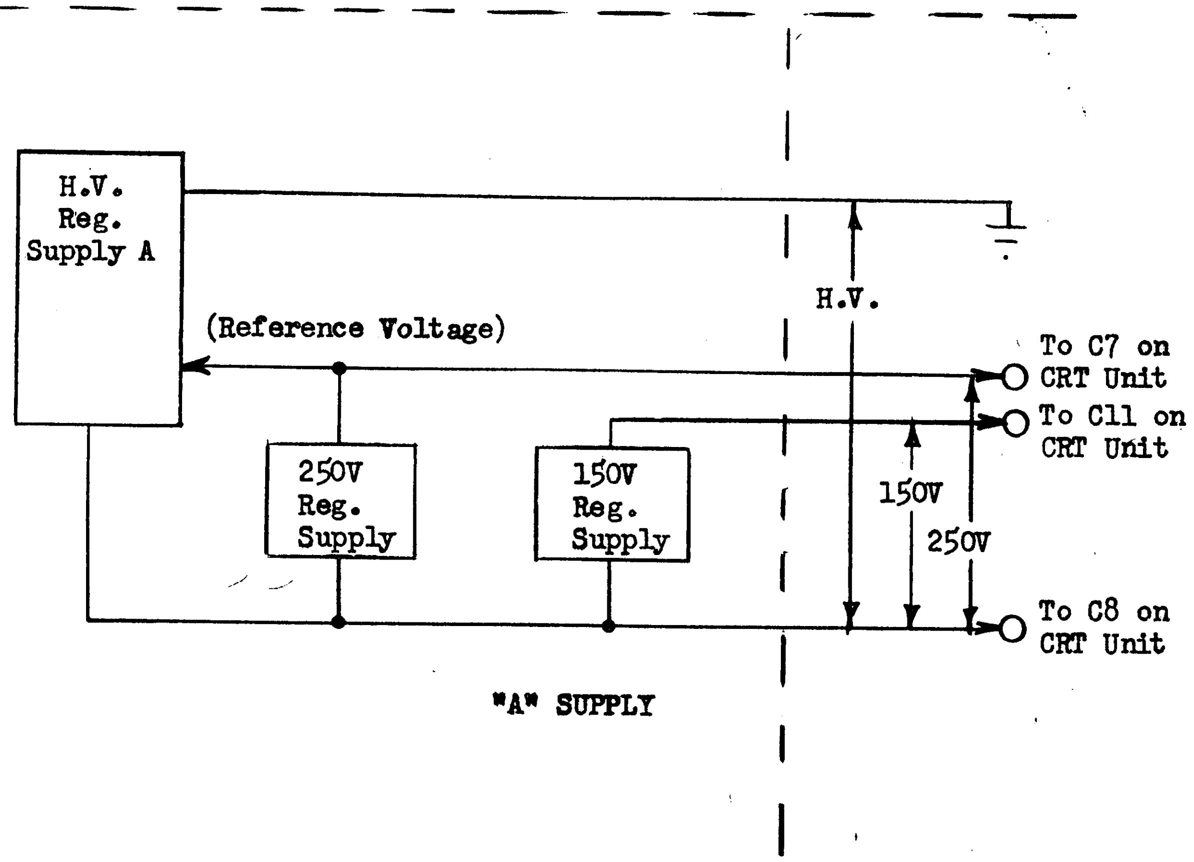
Note: These voltmeters are mounted on the front panel of the 200 volt supply in the high voltage power cabinet.

4.5 Voltage Regulator System.

Connection when using High Voltage Regulator:



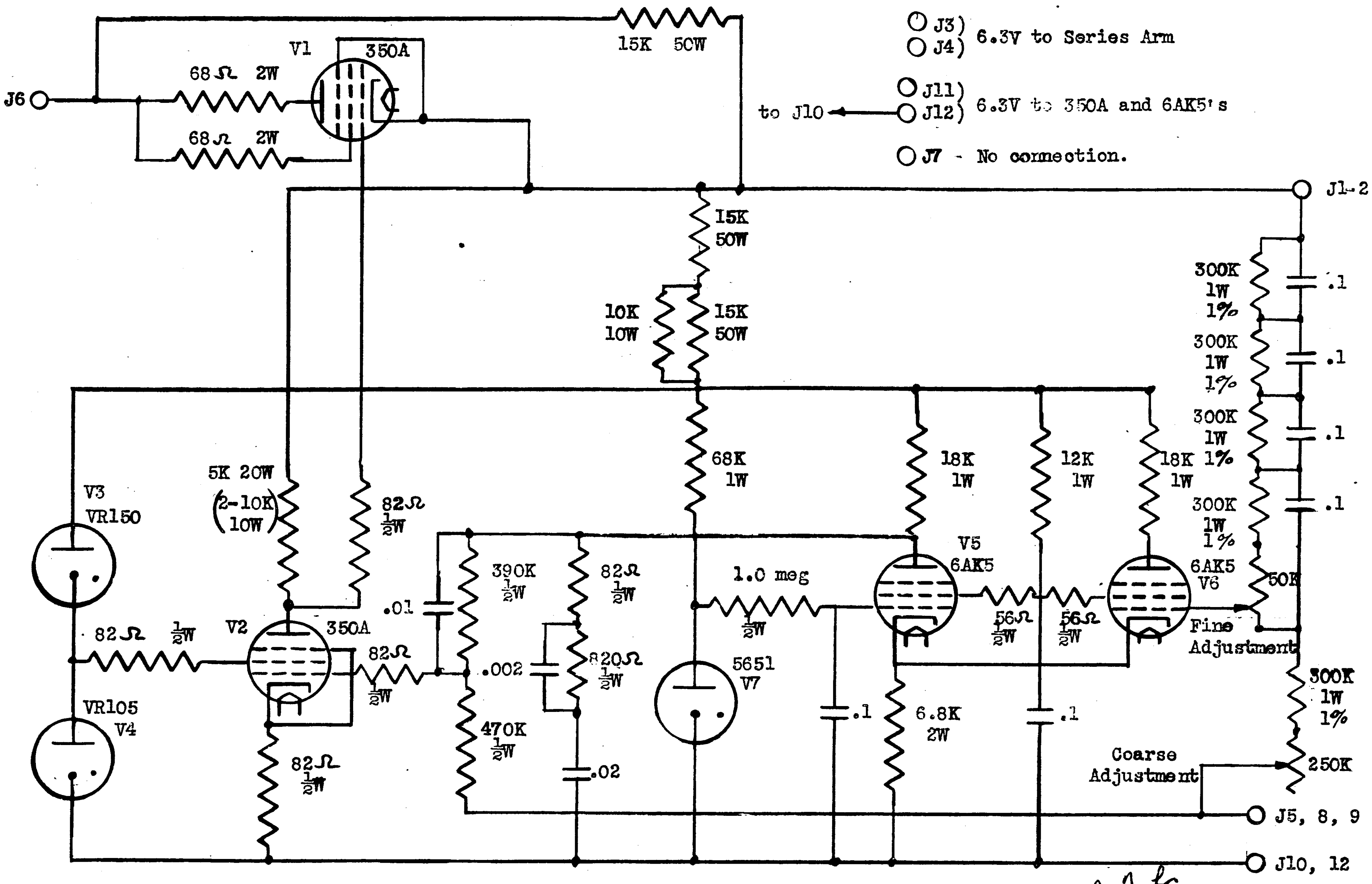
"B" SUPPLY



"A" SUPPLY

4.6 Regulators.

High Voltage Regulator Type A for Memory.

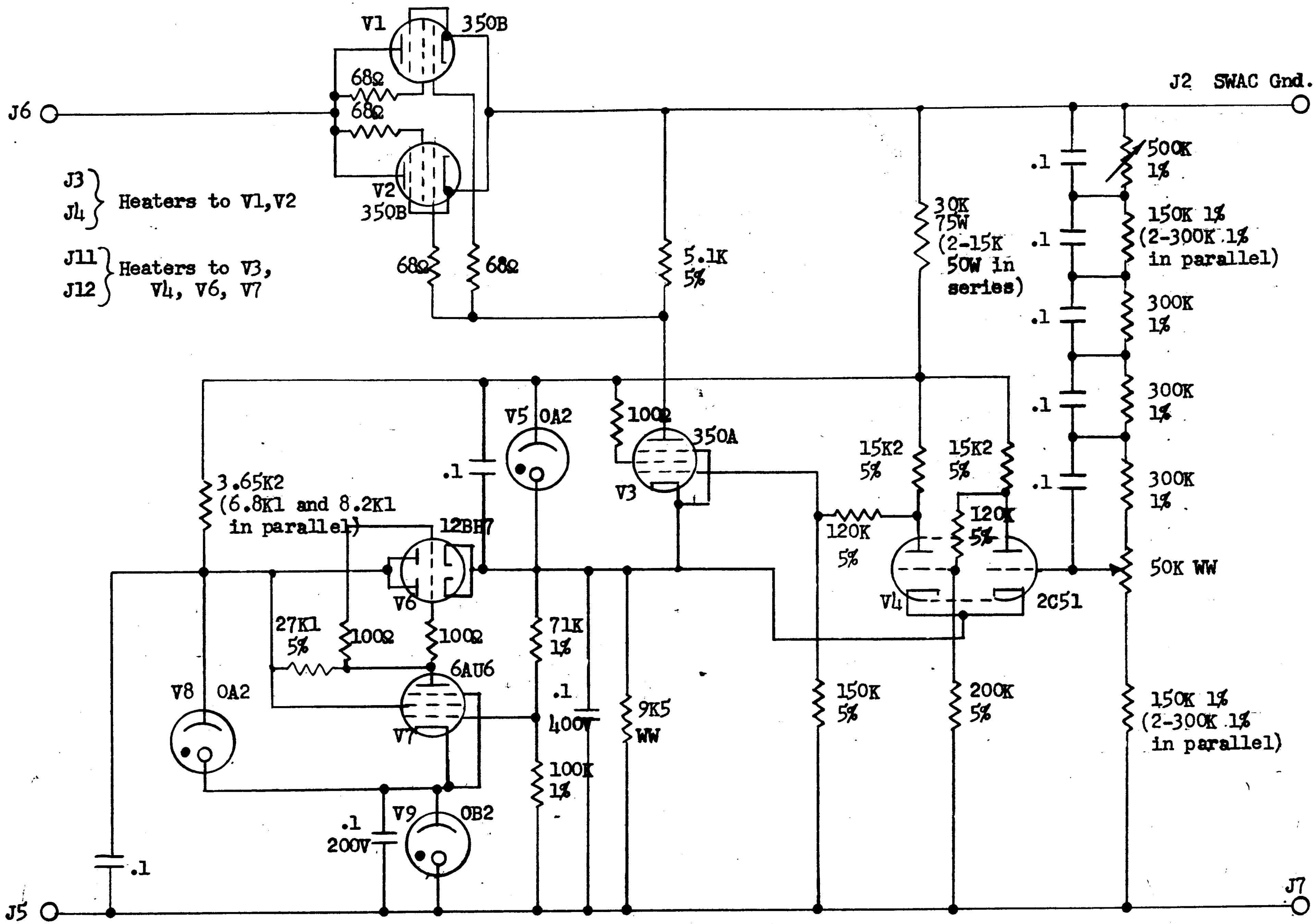


HIGH VOLTAGE REGULATOR FOR MEMORY

N. J. L.

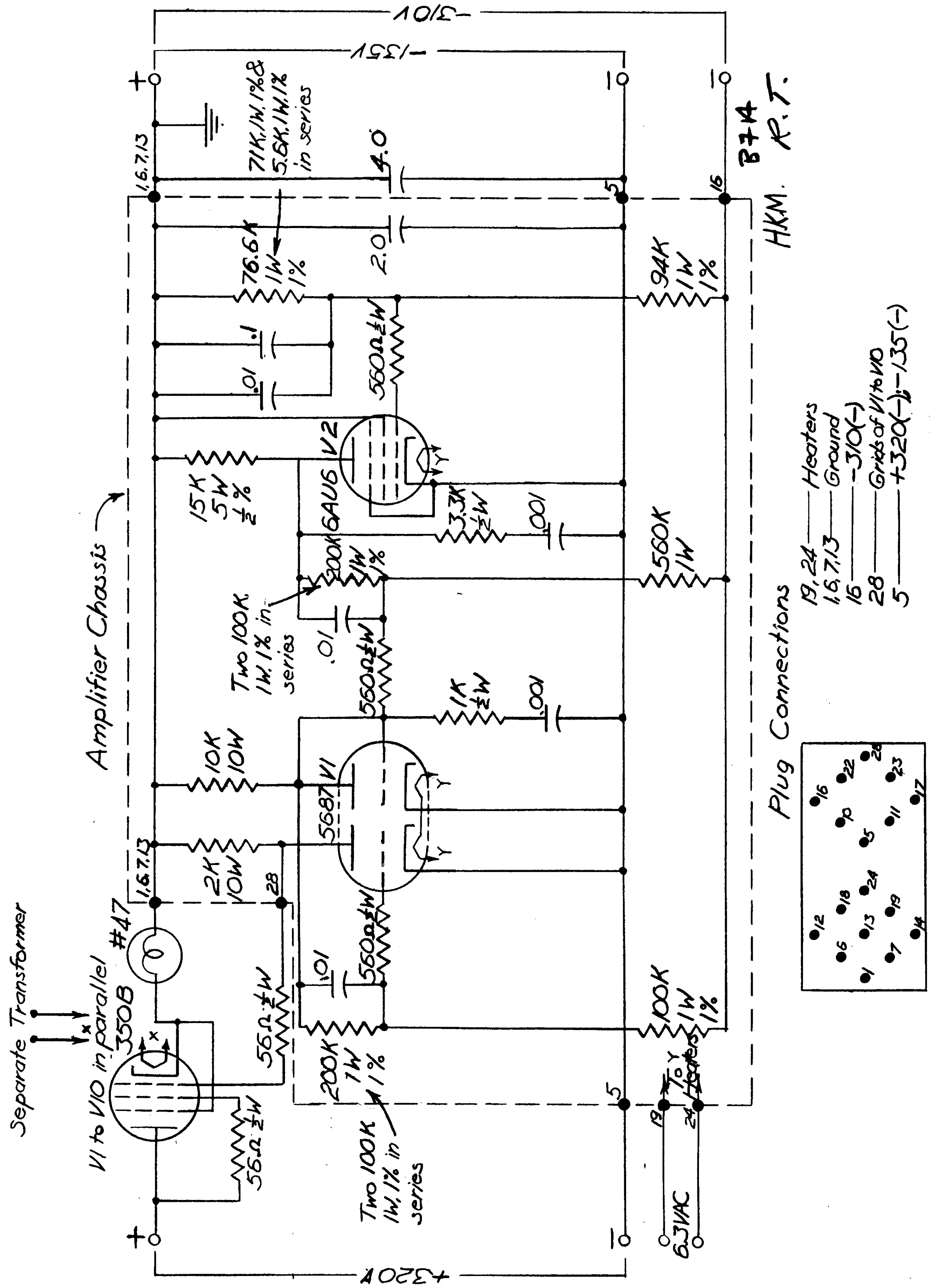
4.6 Regulators.

High Voltage Regulator Type B for Memory:



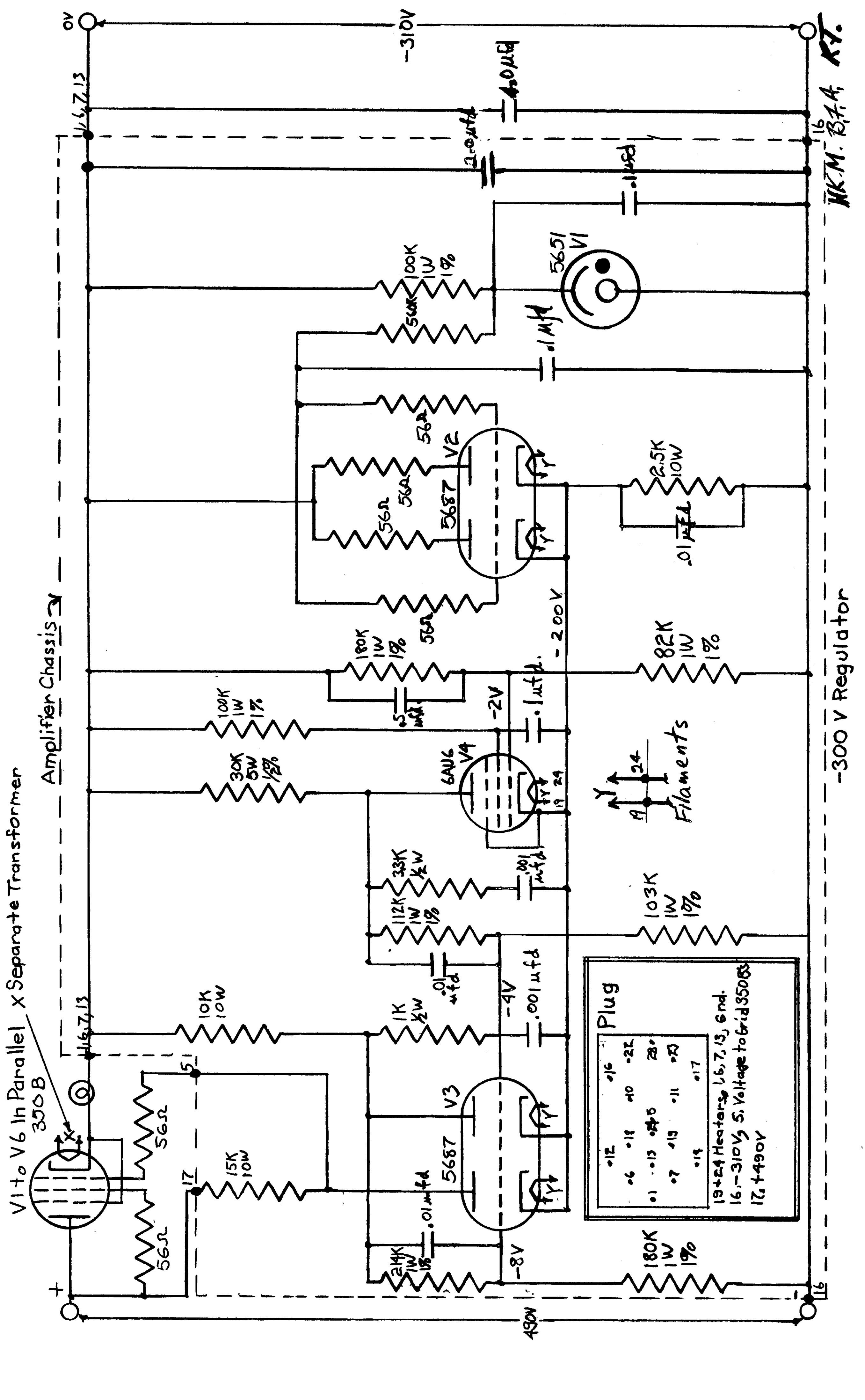
4.6 Regulators.

- 135 Volt Regulator for Magnetic Drum:



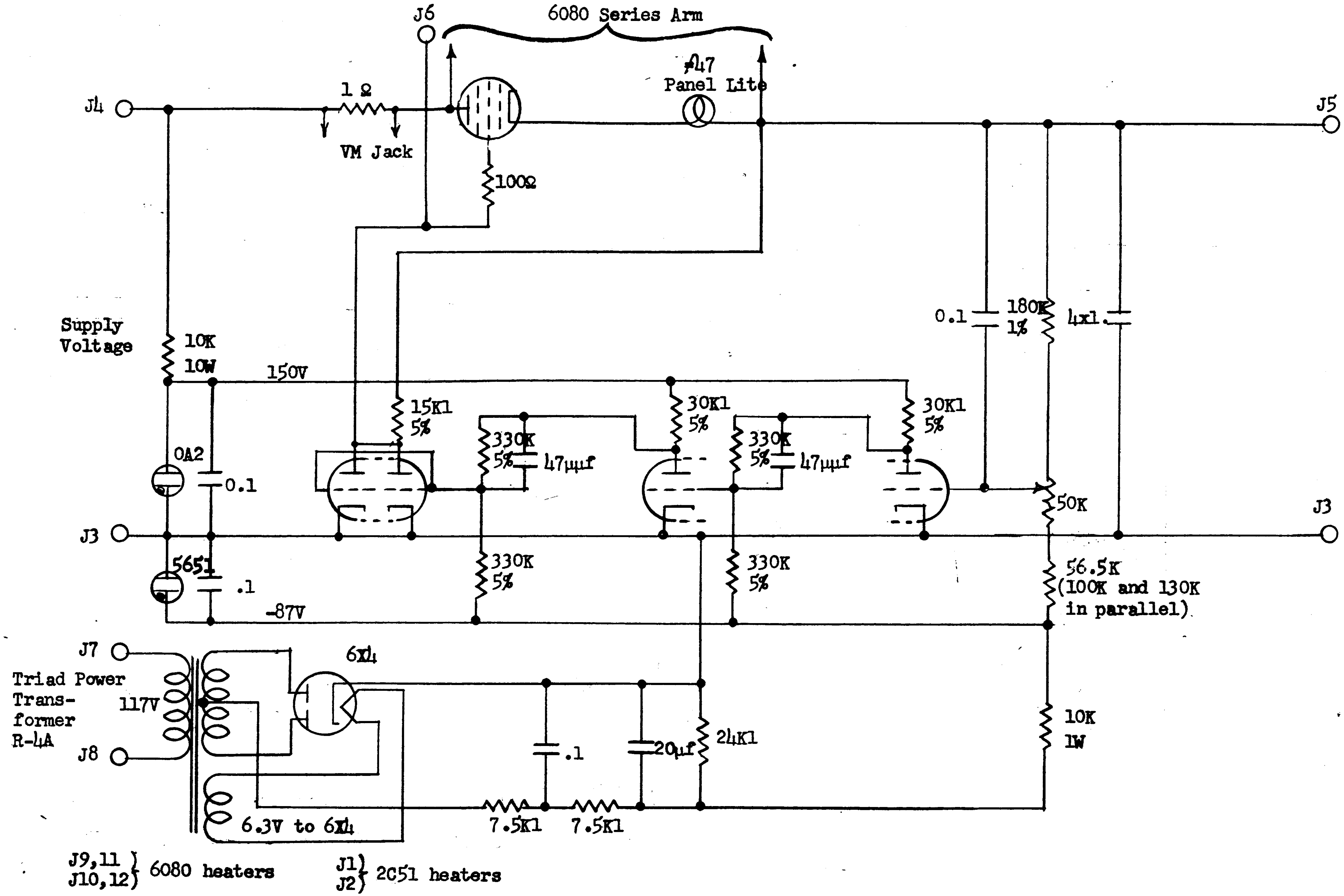
4.6 Regulators.

- 300 Volt Regulator for Magnetic Drum.

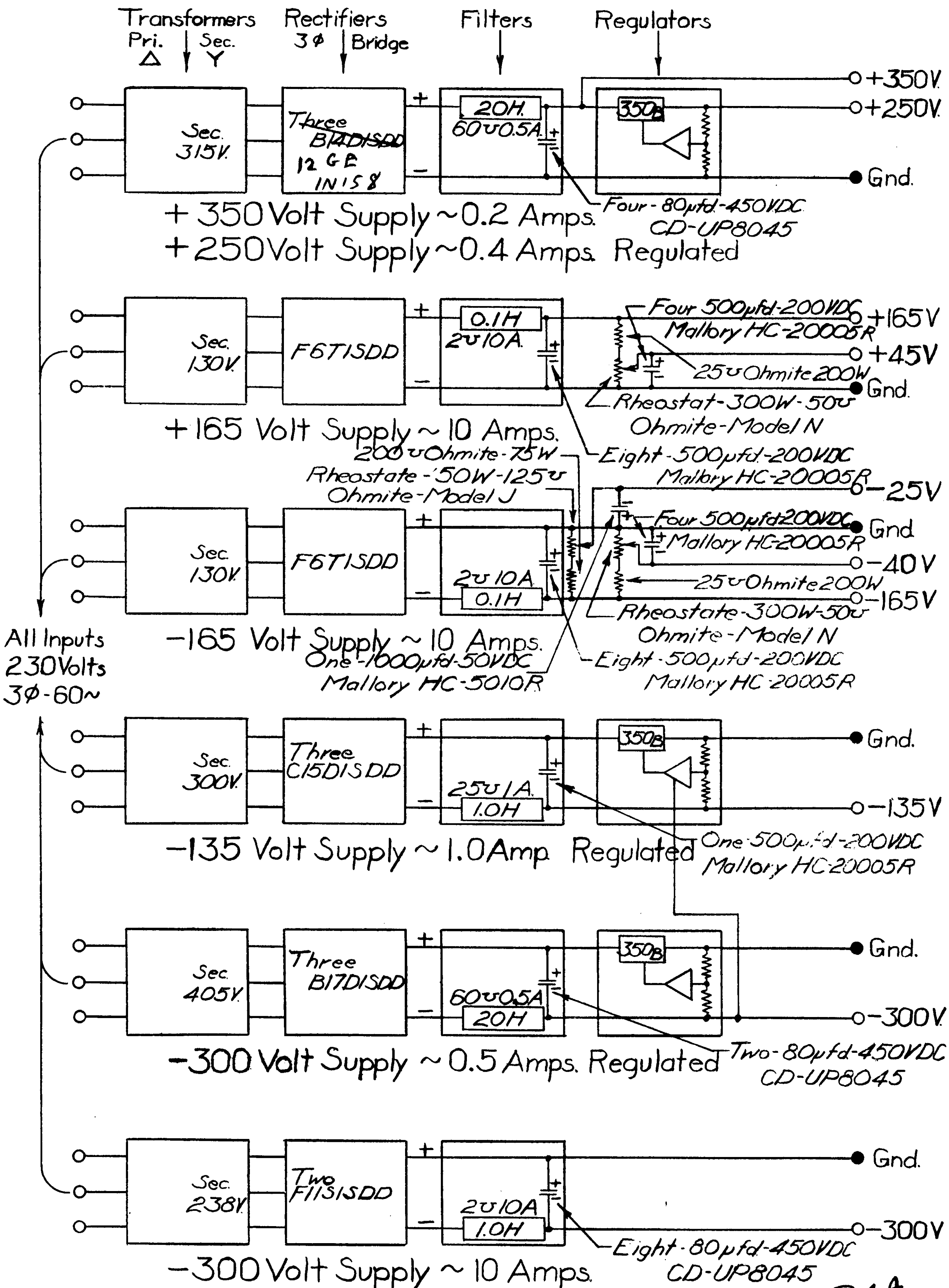


4.6 Regulators.

SWAC Regulator Type A:



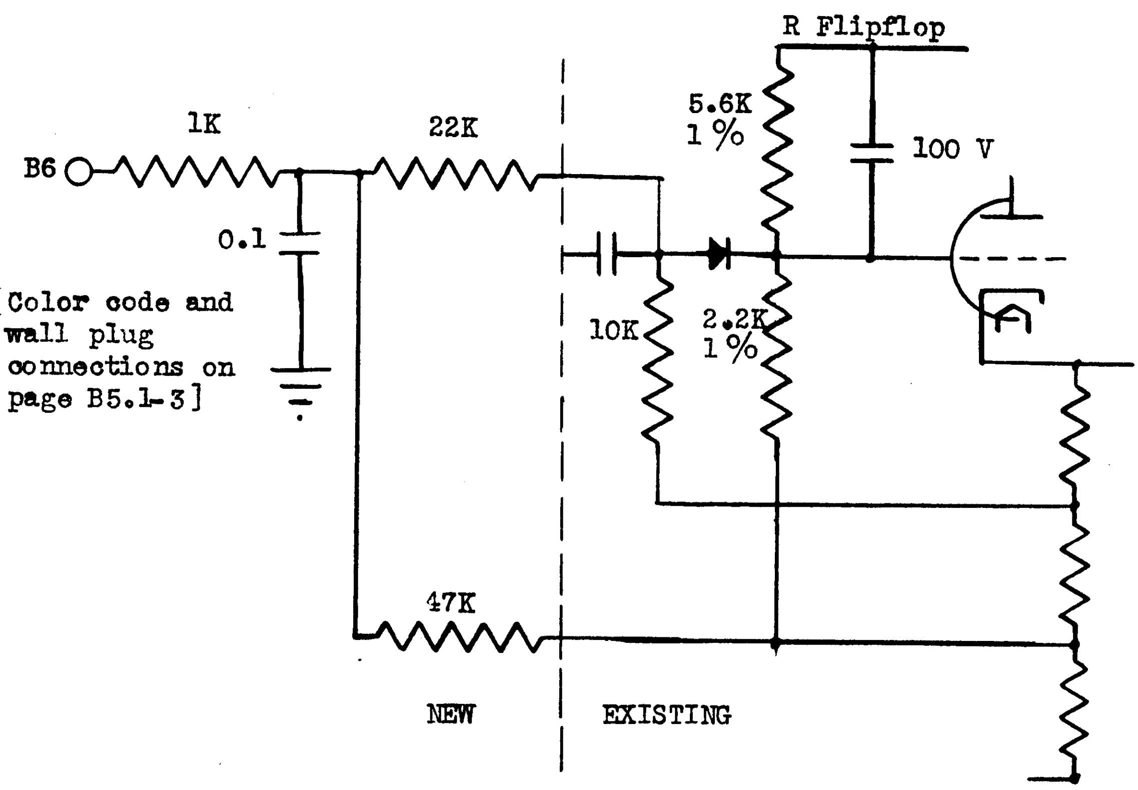
4.7 Block Diagram for Magnetic Drum Power Supply.



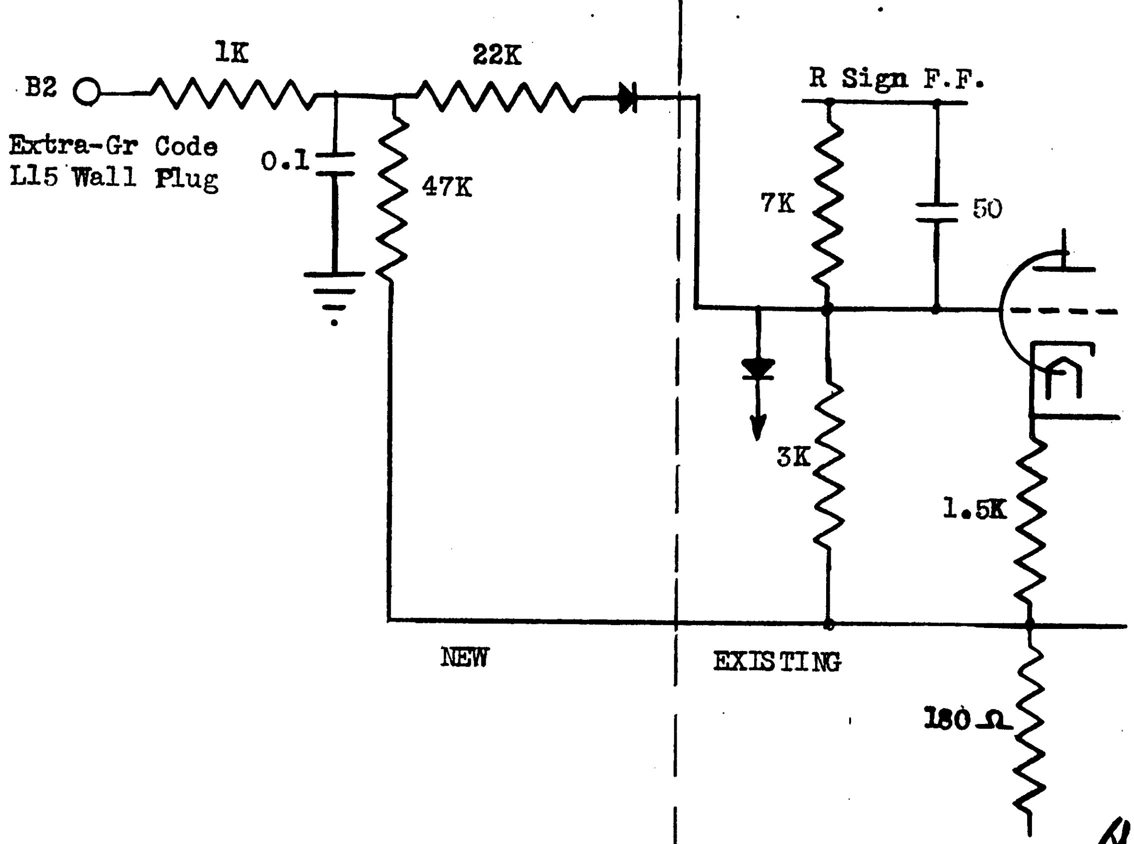
B.J.A.
R.T.

5.1 Collator ~~Modifications~~. Input System

On each M Chassis



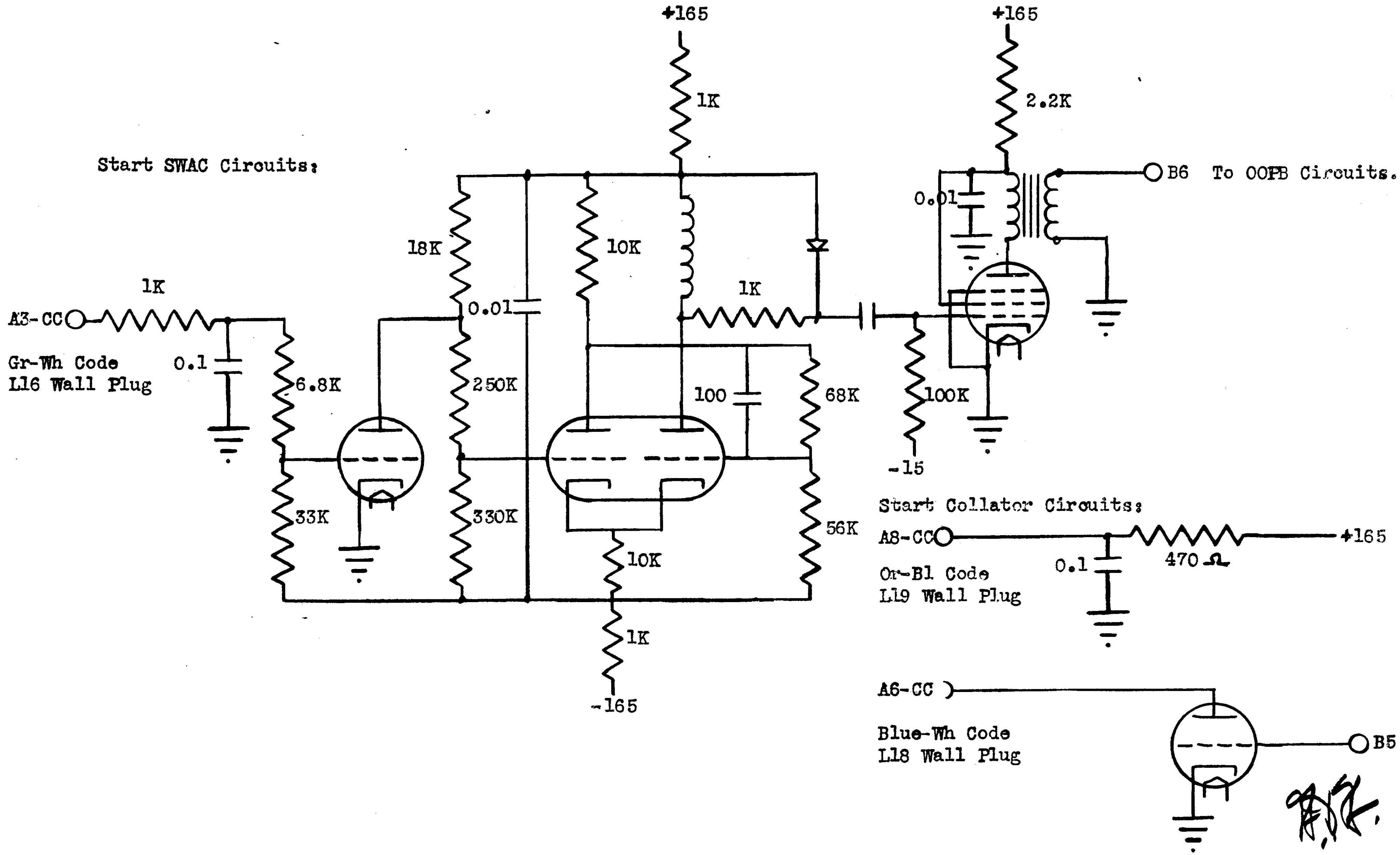
On R Sign Chassis



JRD

5.1 Collator Modifications.

On Input Selector Chassis



5.1 Collator Input System.

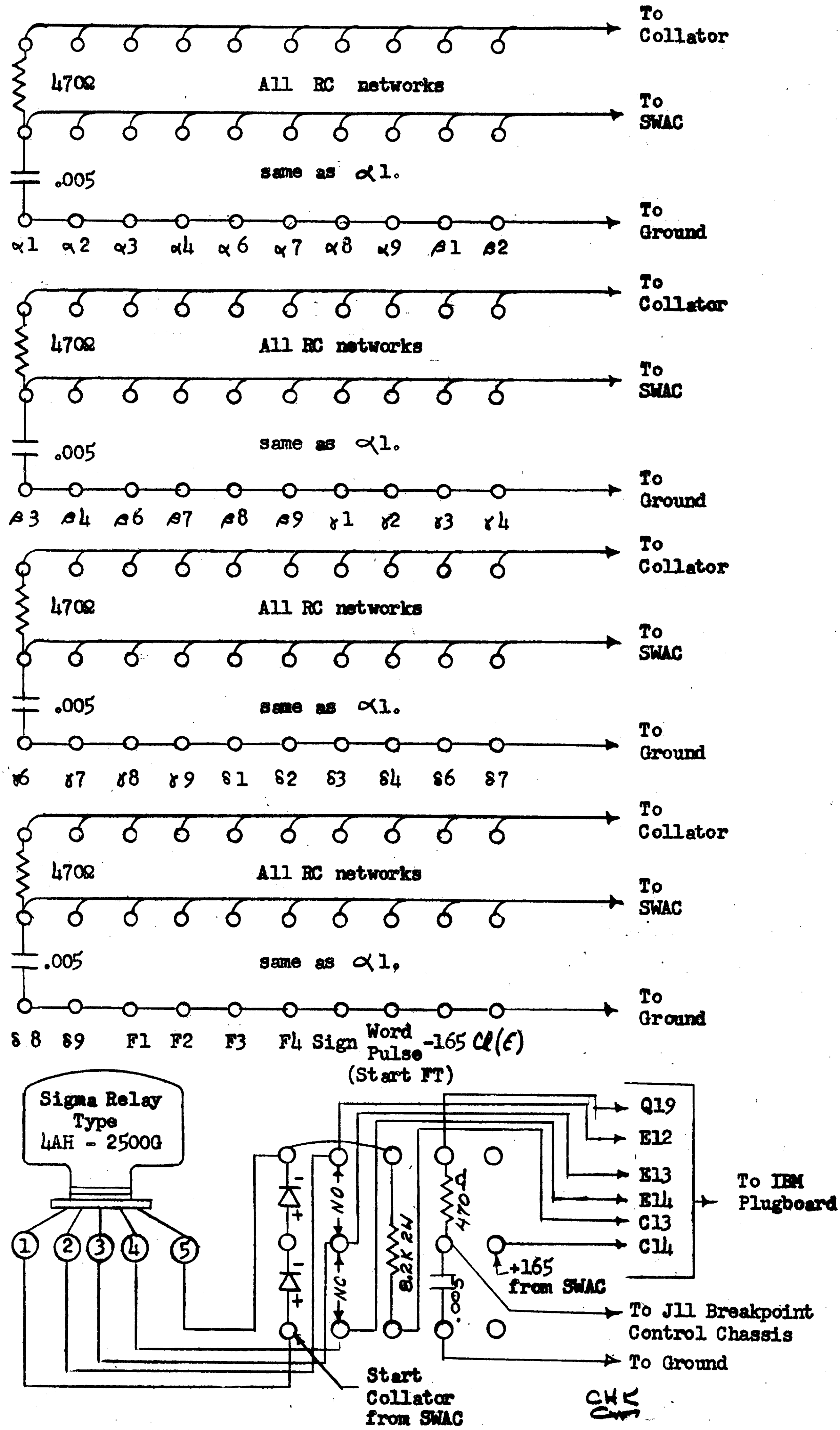
COLLATOR CONNECTIONS

Cable I			Cable II			Cable III		
Digit	Code	Wall Plug	Digit	Code	Wall Plug	Digit	Code	Wall Plug
	GND	D1,D17	β6	Br-Y	D14		GND	C1,C14
F4	Br-Gr	D2	β7	Br-Gr	D15	β4	Bl	C2
F3	Br-Y	D3	β8	Wh	D16	β3	Wh	C3
F2	Wh	D4	β9	Bl-Gr	D18	β2	Br	C4
F1	Bl	D5	γ1	Blue	D19	β1	Bl-Y	C5
δ9	Blue	D6	γ2	Bl-Br	D20	α9	Bl-P	C6
δ8	Br	D7	γ3	Bl	D21	α8	Y	C7
δ7	Gr	D8	γ4	Y	D22	α7	Bl-Gr	C8
δ6	Bl-P	D9	γ6	Br	D23	α6	Blue	C9
δ4	Bl-Y	D10	γ7	Gr	D24	α4	Gr	C10
δ3	Y	D11	γ8	Bl-P	D25	α3	Bl-Br	C11
δ2	Bl-Br	D12	γ9	Bl-Y	D26	α2	Br-Gr	C12
δ1	Bl-Gr	D13				α1	Br-Y	C13
						Sign	Extra-Gr	C15

INPUT SELECTOR CABLE TO CHASSIS CC 7

Function	Cannon Plug	Code	Wall Plug
Word Pulse (Start FT)	A3	Gr-Wh	C16
C1 (ε)	A4	Wh-Blue	C17
Start Collator	A6	Blue-Wh	C18
+ 165	A8	Or-Bl	C19
- 165	A12	Or-Wh	C20

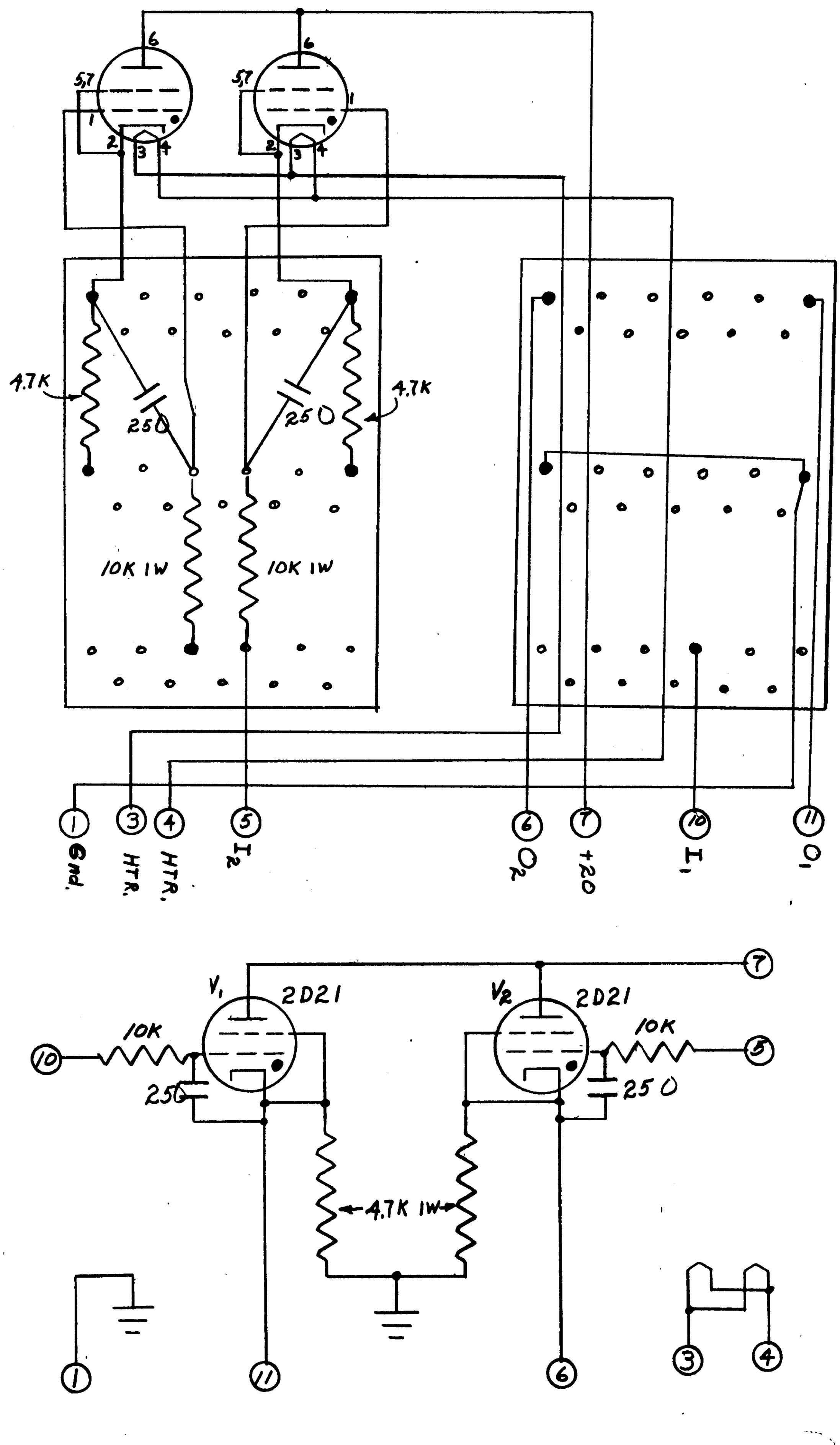
5.1 Collator Input System.



DECOUPLING AND CONTROL PANEL (IN COLLATOR)

5.2 IBM Punch Output.

IBM Punch Output Plug-In Unit:



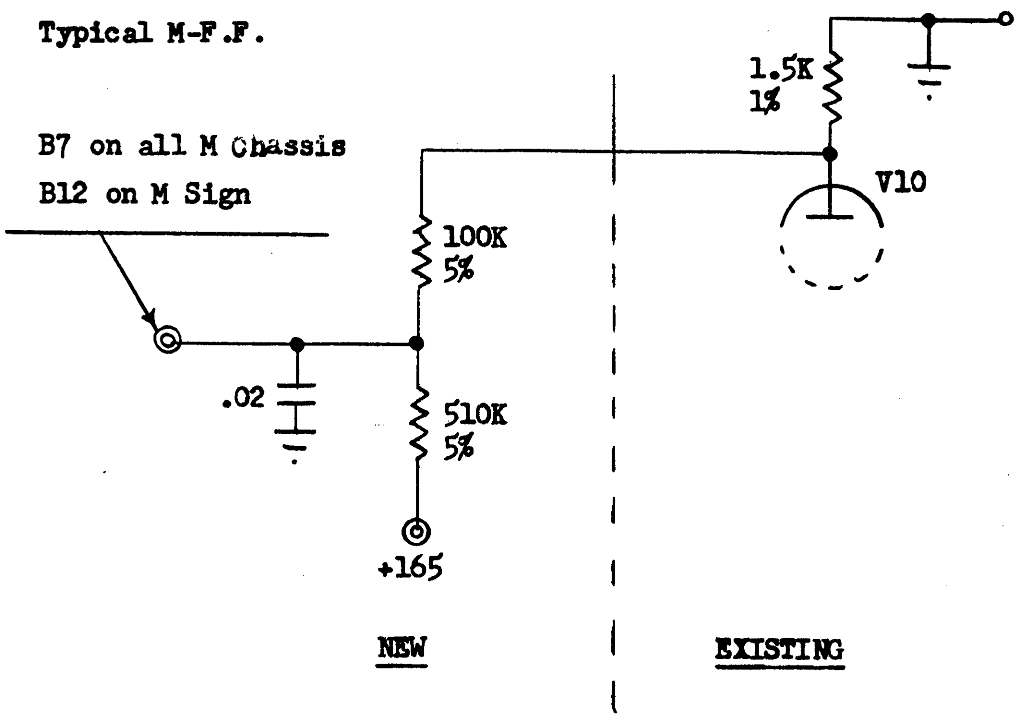
AEG

5.2 IBM Punch Output

M Chassis Modification for IBM Punch Output:

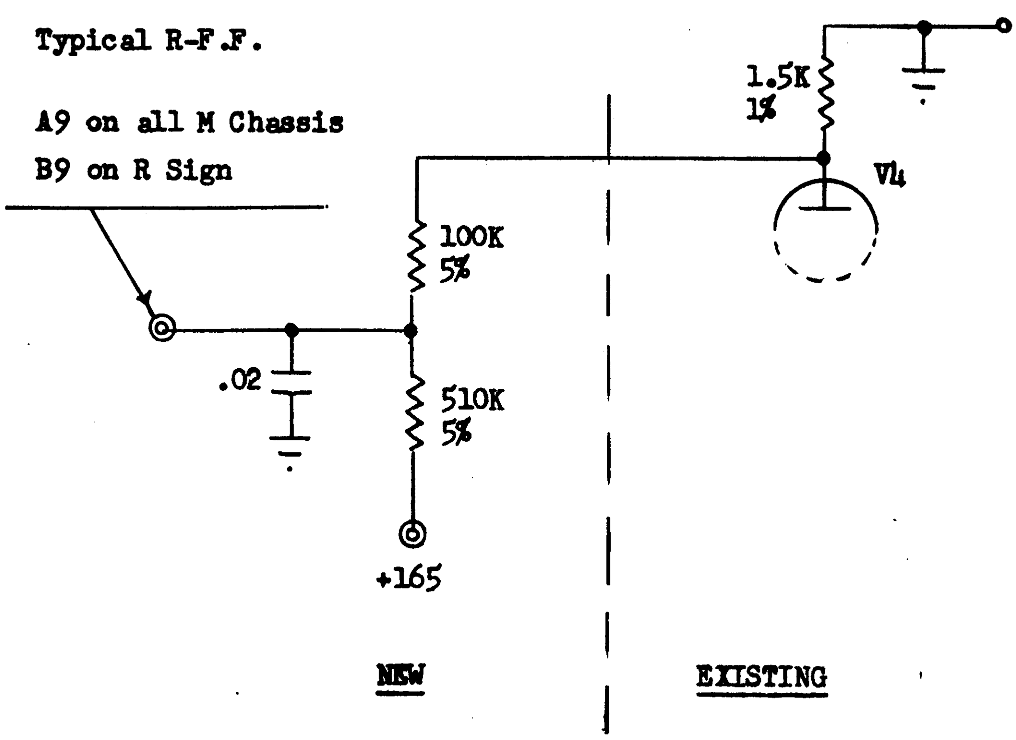
Typical M-F.F.

B7 on all M Chassis
B12 on M Sign



Typical R-F.F.

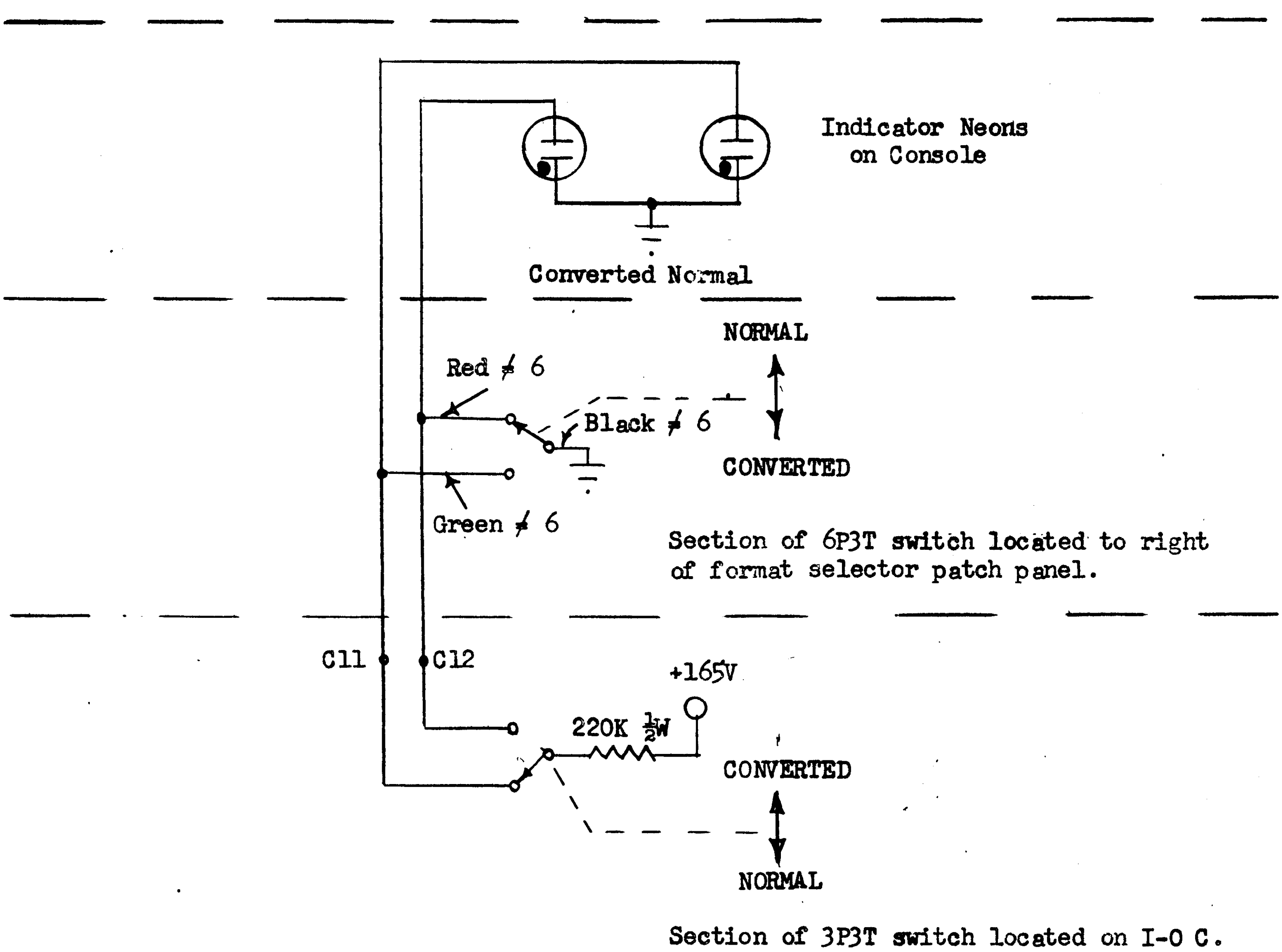
A9 on all M Chassis
B9 on R Sign



n.7.h

5.3 Converted Output

Converted-Normal Output Indicator Light Wiring:



Note:

Operation is such that if both switches are turned to "Normal" or "Converted" then the "Normal or "Converted" console neon respectively will be on. The above holds only if the center position of the three position switch is not used. If the center position of either switch is used, then erroneous indications and machine operation will result.

n.a.k.

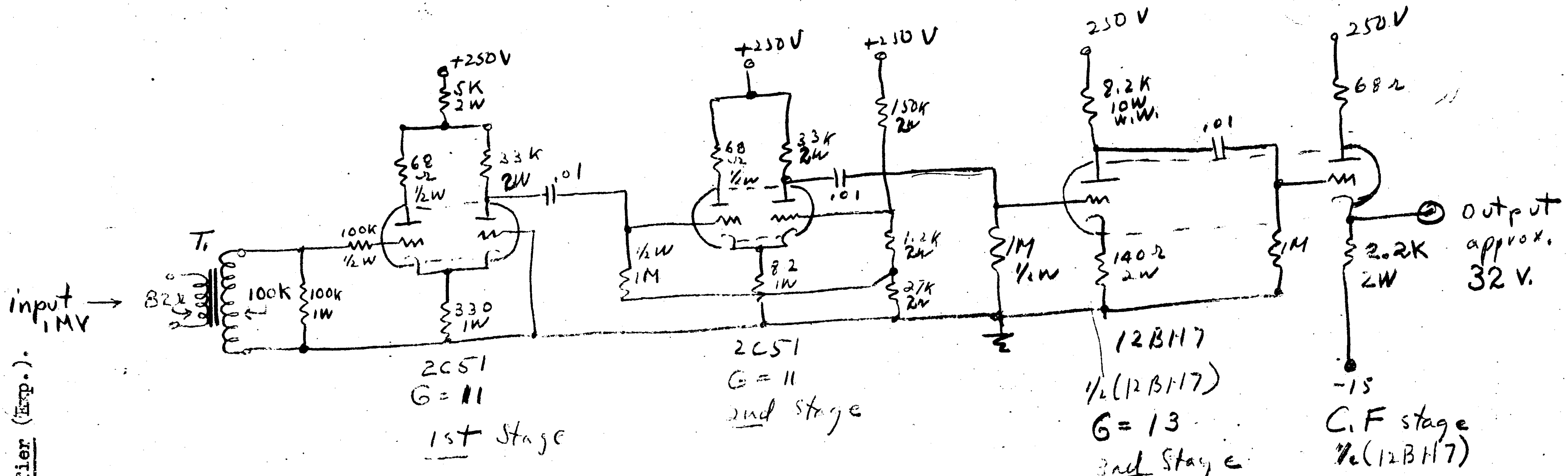
5. **Flexowriter Code.**

	543216		543216		543216
1	010001	I	110000	C.R.	100011
2	010010	J	110001	TAB	101000
3	010011	K	101001	SU	100100
4	010100	L	100001	SD	100101
5	010101	M	111010	PER	100010
6	010110	N	111011	SPACE	100000
7	010111	O	110010	-	001000
8	011000	P	111100	½	000100
9	011001	Q	111101	;	001011
0	010000	R	110011	'	000101
A	110100	S	110110	,	001010
B	110101	T	110111	/	001001
C	111000	U	101010	STOP	000010
D	111001	V	101011	BKSP	000001
E	111110	W	101100		
F	111111	X	101101		
G	100110	Y	101110		
H	100111	Z	101111		

DELAY CHASSIS SWITCH POSITION (Switch Down)	DELAY (μsec)
#1, #2, #3	512
#2, #3	448
#1, #3	384
#3	320
#1, #2	256
#2	192
#1	128
None	64

LEJ

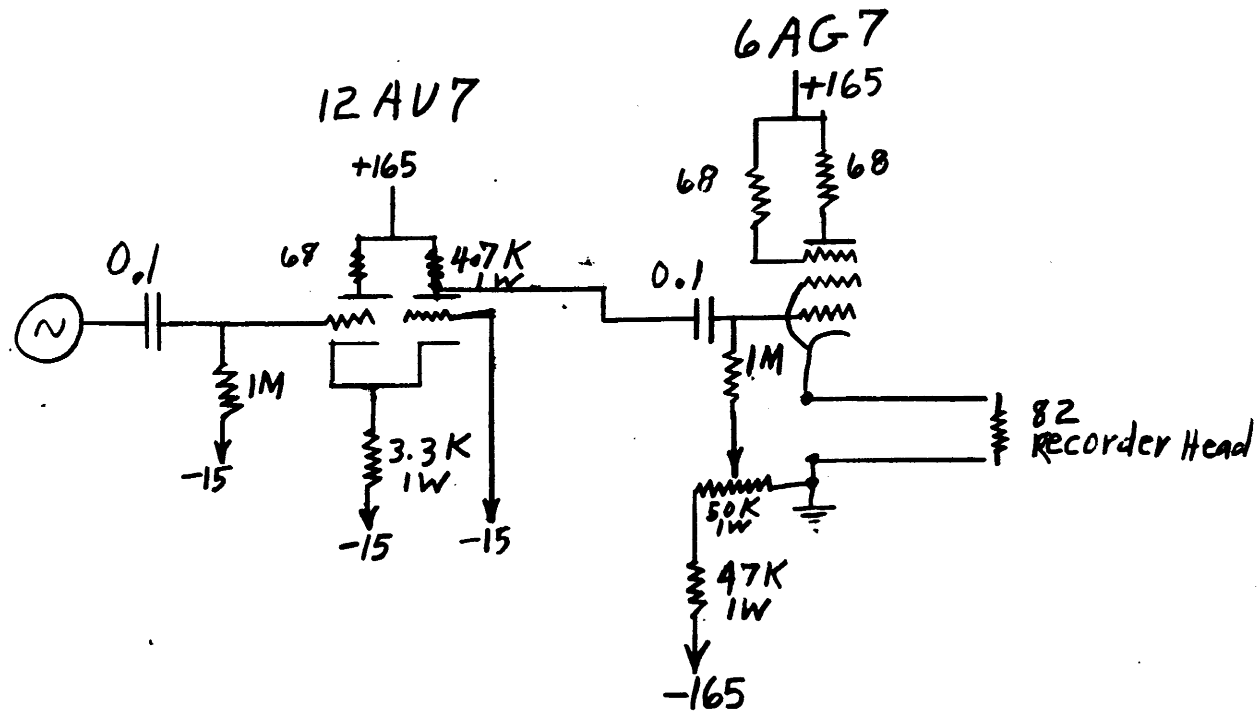
6.1 Magnetic Tape Amplifier (Exp.).



Magnetic Tape Amplifier (Exp.)

July 20, 1951 B.T.A. [illegible]
See Notebook pages 76, 77 + 80-82

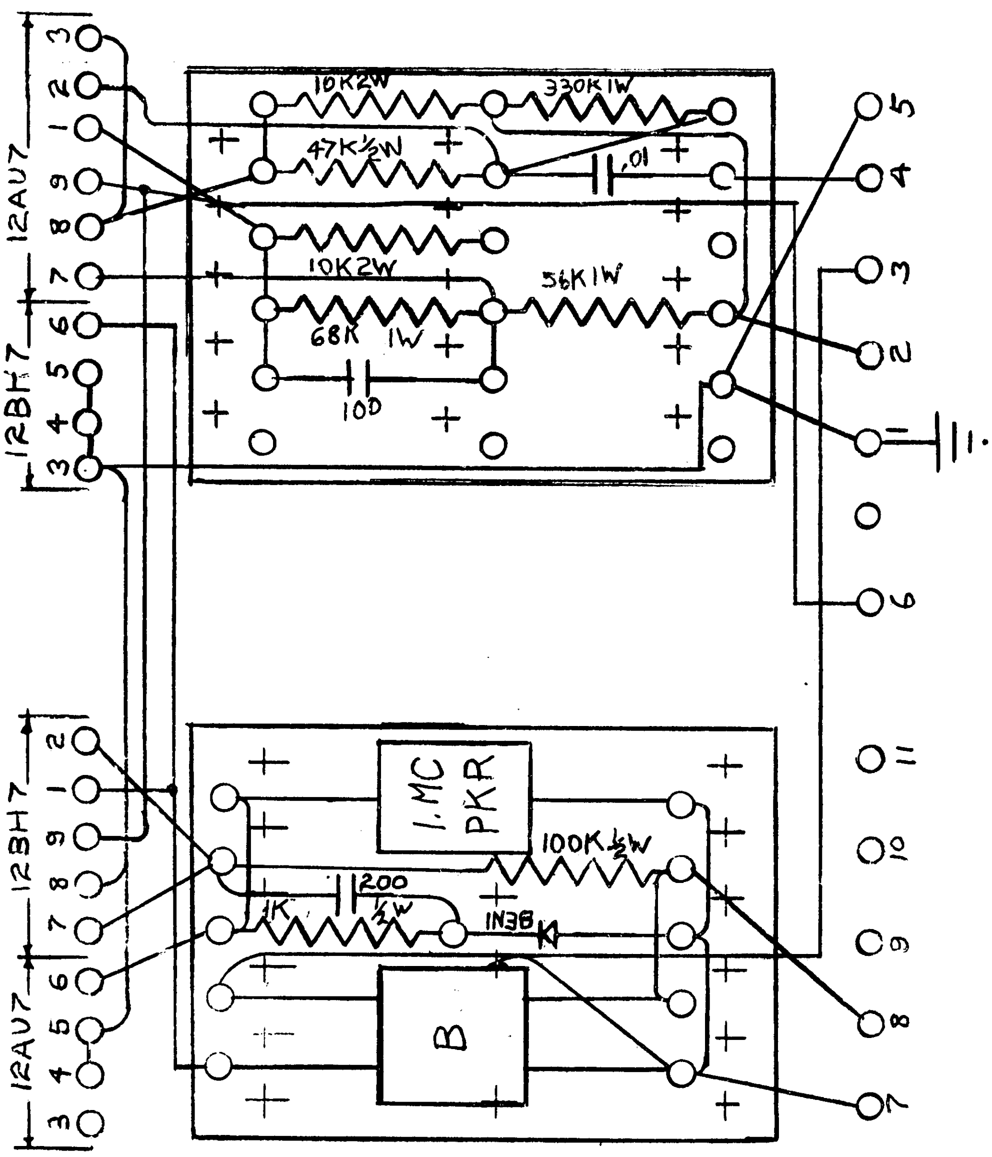
6.2 Magnetic Tape Driver (Experimental)

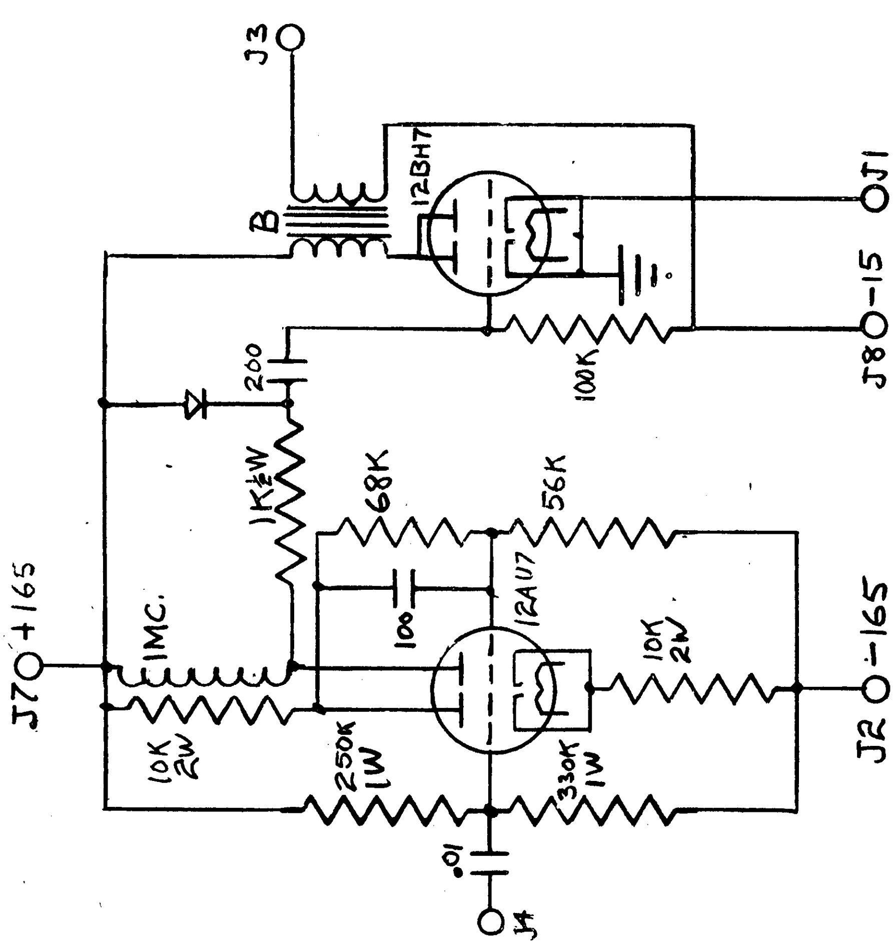


Magnetic Tape Driver (Exp.)

July 31, 1951 HK.M.

6.3 Magnetic Tape Pulse Former.



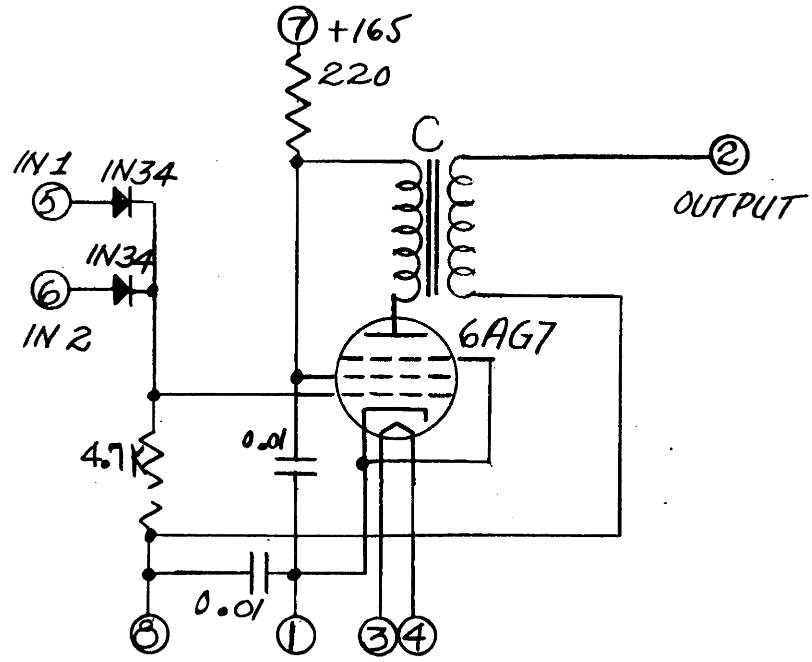


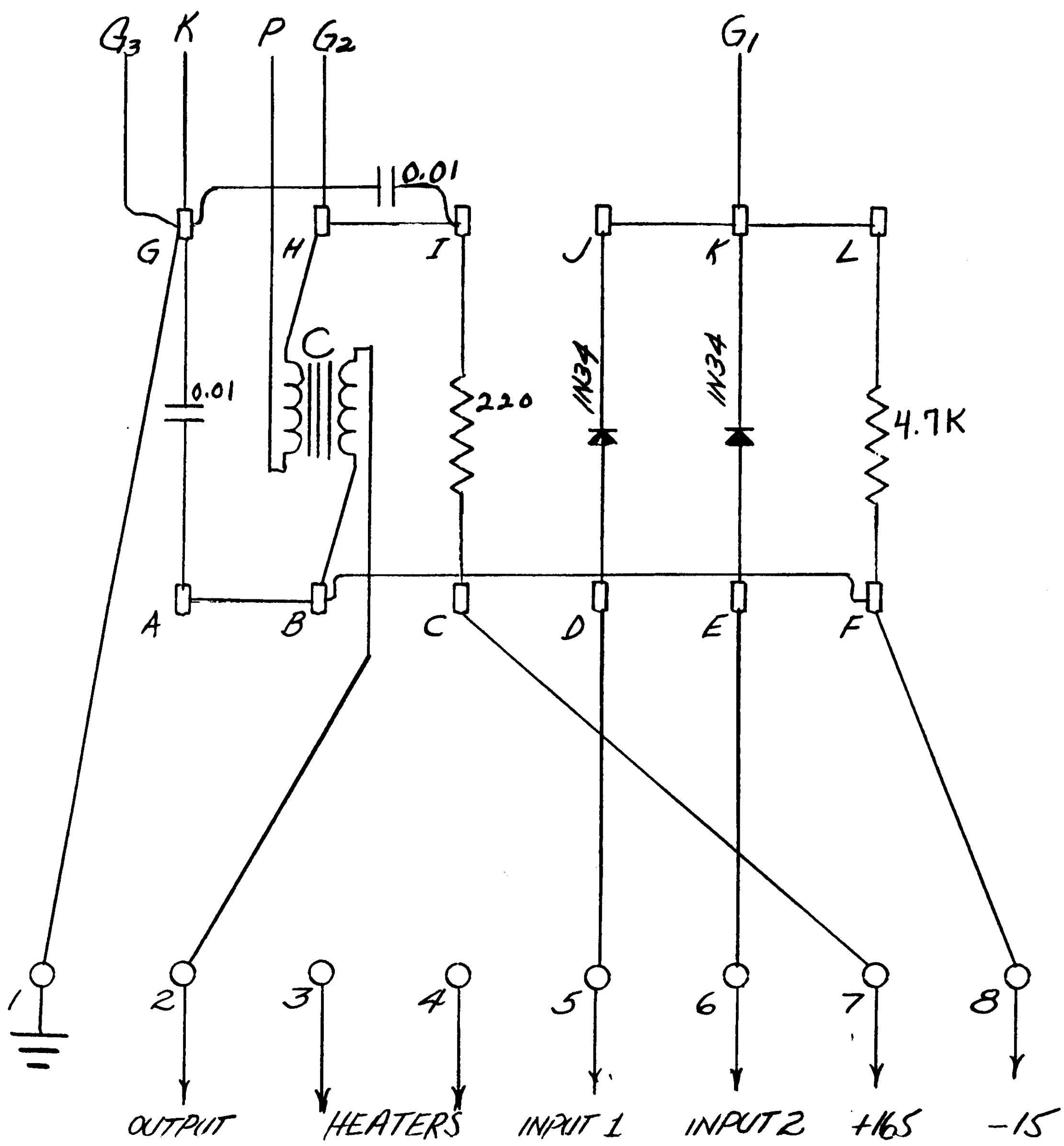
L.E.M.

6.4 Magnetic Tape 6AG7 Driver (Turret Plug In).

PLUG CONNECTIONS
1 CATHODE - GND
2 OUTPUT
3 HEATERS
4 HEATERS
5 INPUT 1
6 INPUT 2
7 +165
8 -15

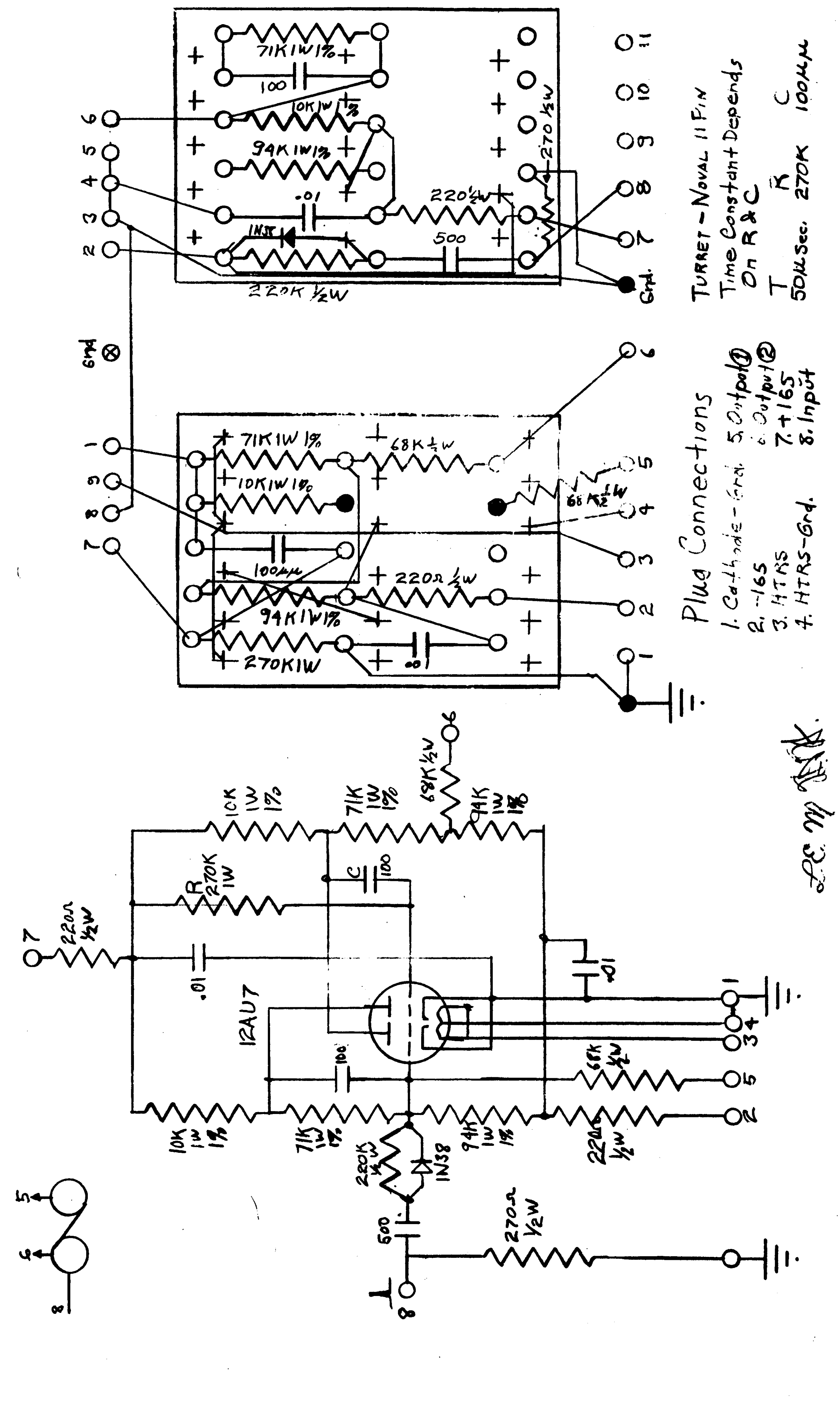
TURRET- OCTAL-OCTAL





CAM
HKM.

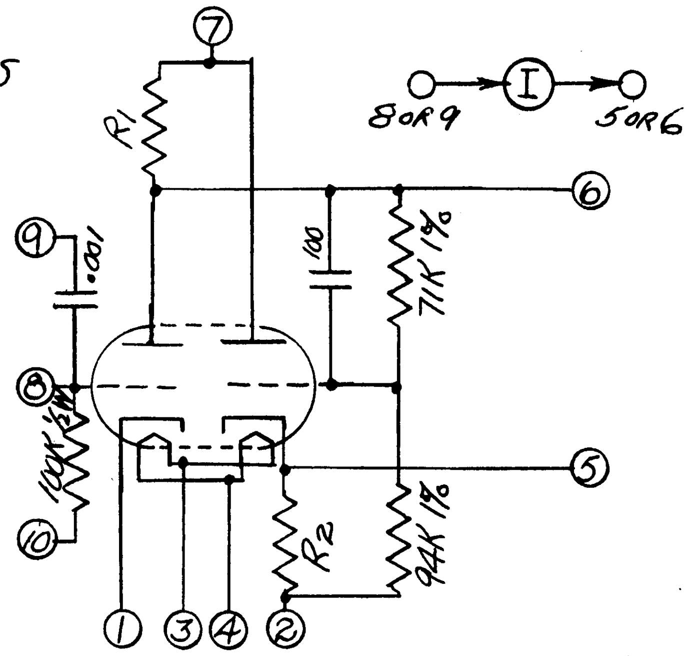
6.5 <u>Magnetic Tape One Shot</u> (Turret Plug-In).



6.6 Magnetic Tape Inverter-Cathode Follower (Turret Plug In).

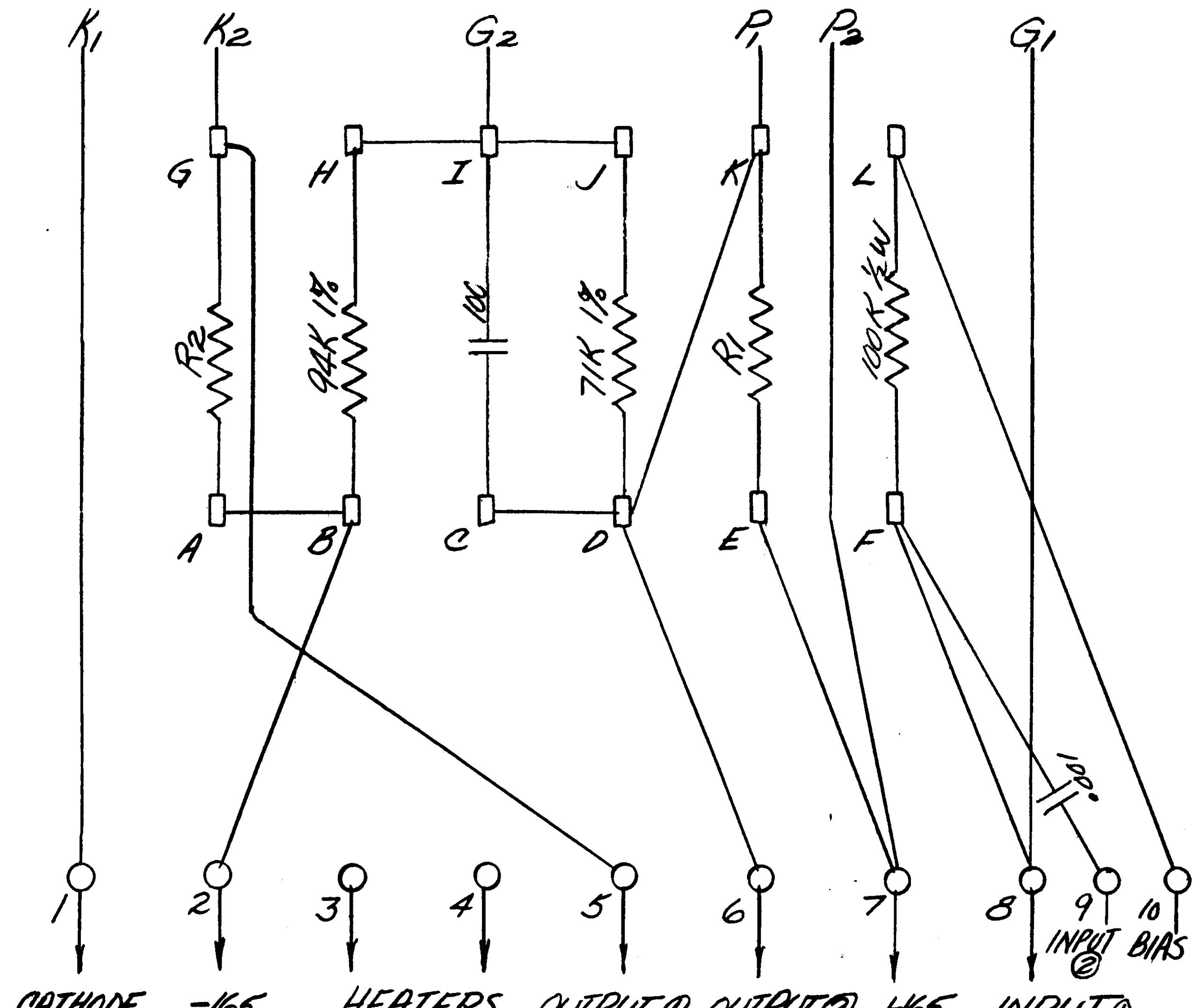
PLUG CONNECTIONS

1. CATHODE
2. -165
3. HEATERS
4. HEATERS
5. OUTPUT ①
6. OUTPUT ②
7. +165
8. INPUT ①
9. INPUT ②
10. BIAS



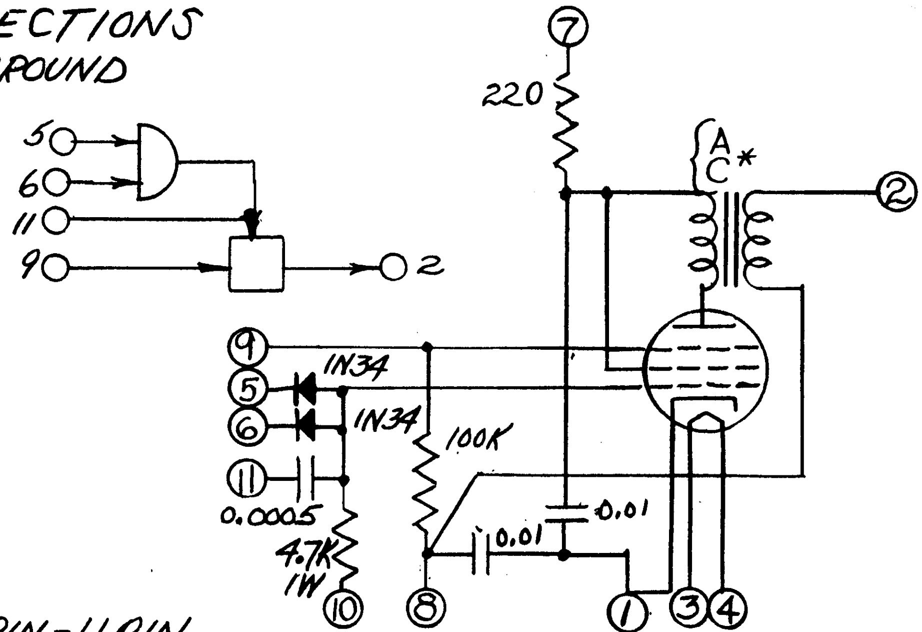
TURRET - NOVAL - 11PIN

	R_1	R_2
12AU7	3.3K(1W)	22K(2W)
12BH7	1.5K(1W)	15K(3W) → (10K. 2W IN SERIES WITH 5K, 1W)



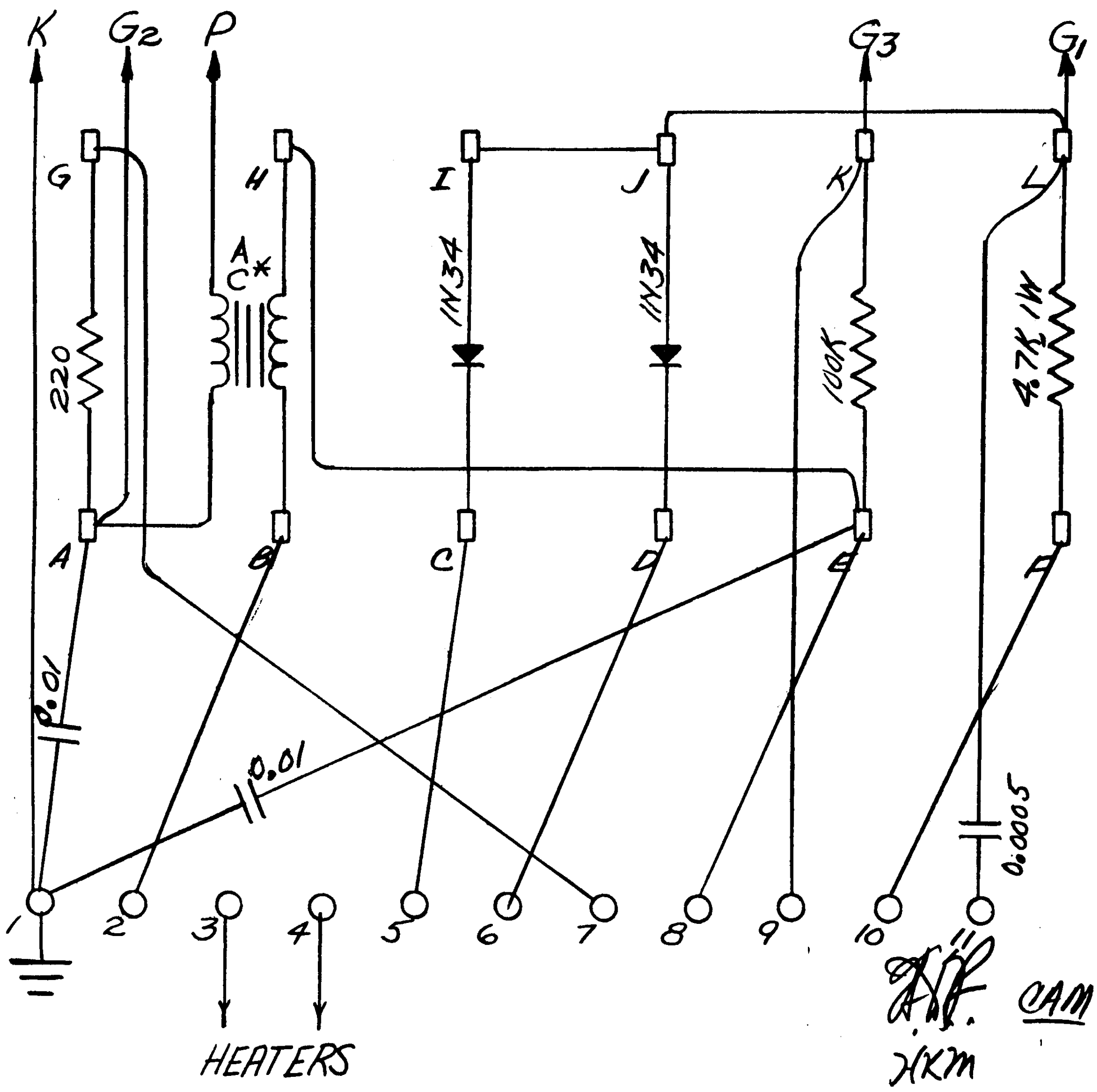
6.7 **Magnetic Tape Gate** (Turret Plug In).

PLUG CONNECTIONS
1. CATHODE-GROUND
2. OUTPUT
3. HEATERS
4. HEATERS
5. INPUT ①
6. INPUT ②
7. +165
8. -15
9. INPUT ③
10. G_1 BIAS
11. INPUT ④



TURRET - 7 PIN - 11 PIN *
LOCTAL - 11 PIN

* 6AS6
7AK7

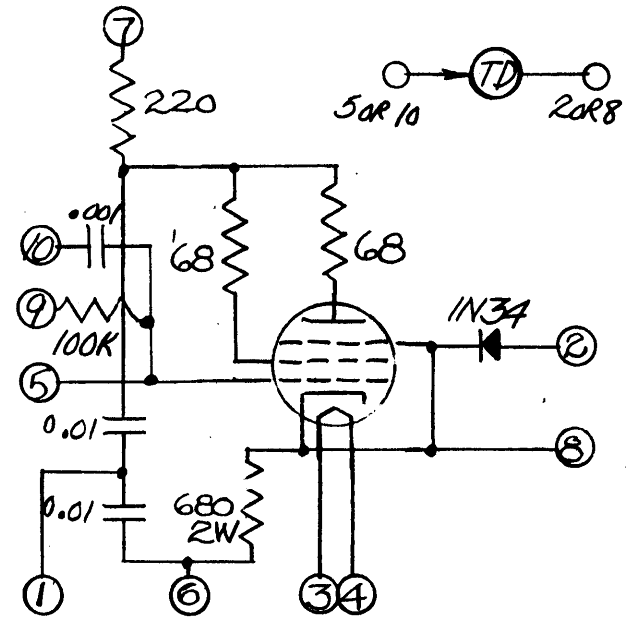


CAM
HKM

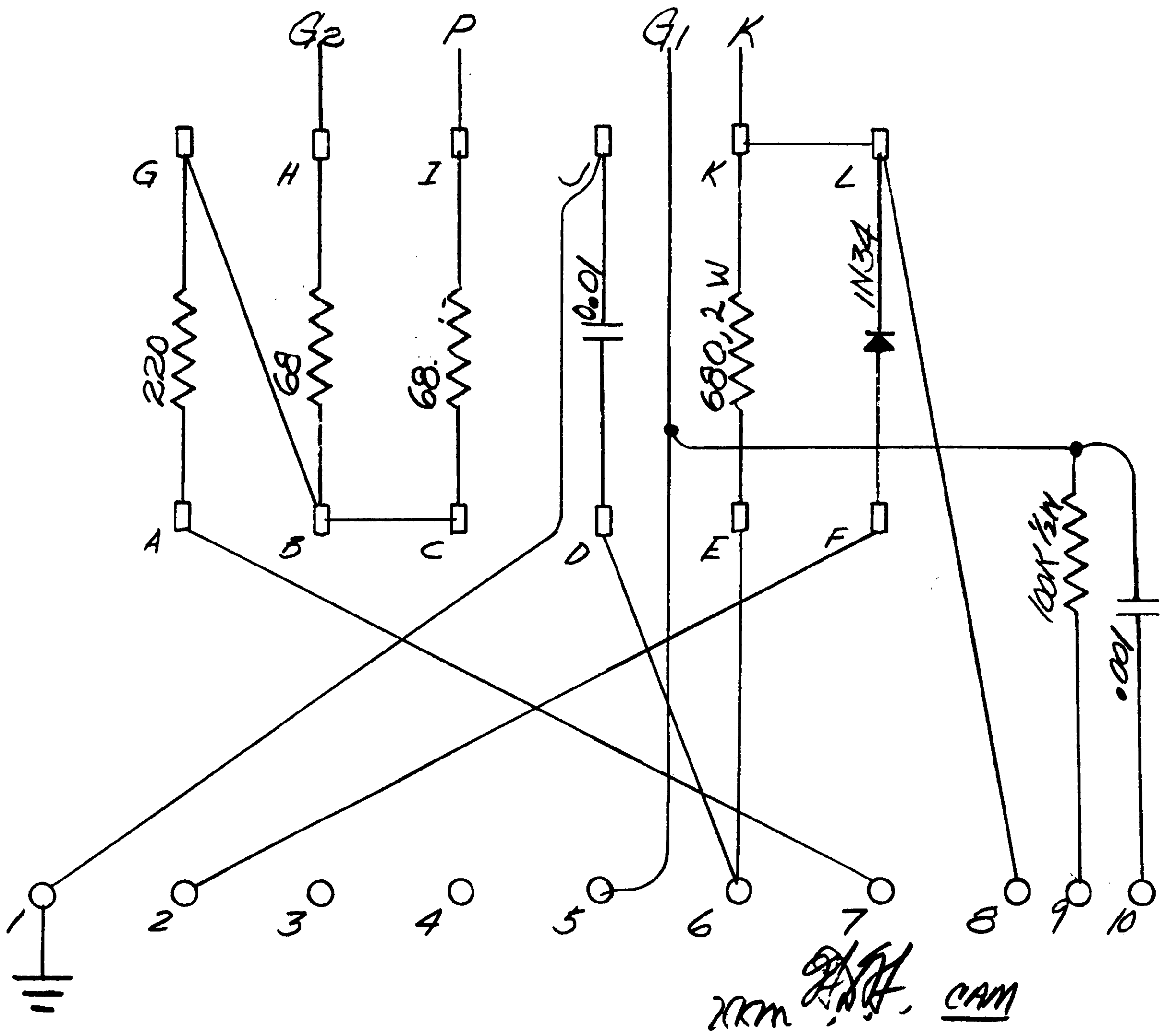
6.8 **Magnetic Tape - Tape Driver** (Turret Plug In).

PLUG CONNECTIONS

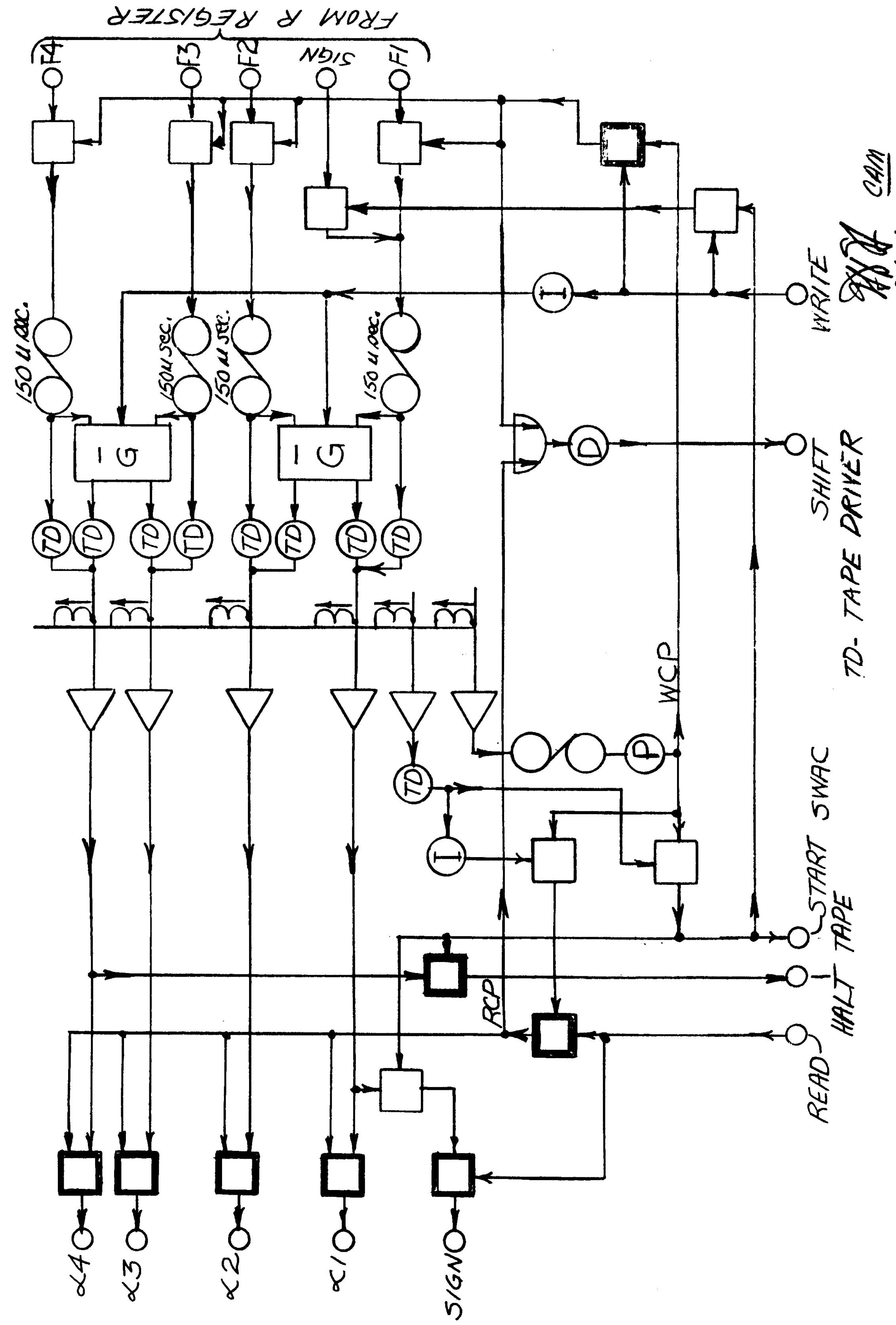
1. GROUND
2. OUTPUT ①
3. HEATERS
4. HEATERS
5. INPUT
6. CATHODE
7. +165
8. OUTPUT ②
9. BIAS
10. INPUT ②



TURRET-OCTAL-11 PIN



6.9 **Magnetic Tape Block Diagram.**



Issued 6-24-53

7.3 Component Location on Drum Panels.

Panel C1:

FRONT VIEW

TRANSFER REGISTER				CHANNEL REGISTER							
1.W F100	1.V F100	1.U F100	1.9 F100	1.8 F100	1.7 F100	1.6 F100	1.5 F100	1.4 F100	1.3 F100	1.2 F100	1.1 F100
2.W GD100	2.V GD100	2.U GD100	2.9 GD100	2.8 GD100	2.7 GD100	2.6 GD100	2.5 GD100	2.4 GD100	2.3 GD100	2.2 GD100	2.1 GD100
3.W Not Used	3.V Not Used	3.U Not Used	3.9 GD100	3.8 GD100	3.7 GD100	3.6 GD100	3.5 GD100	3.4 GD100 Not Used	3.3 GD100	3.2 GD100	3.1 GD100
4.W Not Used	4.V Not Used	4.U Not Used	4.9 Not Used	4.8 GD100	4.7 GD100	4.6 GD100	4.5 GD100	4.4 GD100 Not Used	4.3 GD100 Not Used	4.2 GD100	4.1 GD100

CODE: F100: 100 Series Flip-flop
GD100: 100 Series Direct Coupled Gate

7.3 Component Location on Drum Panels.

Panel C2:

FRONT VIEW

1.W Not Used	1.V Not Used	1.U GP200	1.9 GP200D	1.8 [illegible]	1.7 GP100D	1.6 F100	1.5 F100	1.4 F100	1.3 F100	1.2 F100	1.1 F100
2.W Not Used	2.V GP200D	2.U GP300D	2.9 GP300D	2.8 GD100	2.7 GD100	2.6 Not Used	2.5 GP100D	2.4 GP100D	2.3 GP100D	2.2 Not Used	2.1 GP100D
3.W I100	3.V GP200D	3.U GP200D	3.9 GP100D	3.8 GP100D	3.7 GP100D	3.6 GP100D	3.5 GP100D	3.4 [illegible]100	3.3 GP100D	3.2 GP100D	3.1 GP100D
4.W I100	4.V GP100D	4.U GP100D	4.9 GP100D	4.8 GP100D	4.7 GP100D	4.6 GP100D	4.5 GP100D	4.4 GP100D	4.3 Not Used	4.2 Not Used	4.1 Not Used

CODE:
- I100: 100 Series Inverter
- GP100: 100 Series Pulse Gate Using Inverting "B" Ferrite Transformer.
- GP200: 200 Series Pulse Gate Using Inverting "C" Ferrite Transformer.
- GP300: 300 Series Pulse Gate Using Non-inverting "C" Ferrite Transformer.
- GP100D, GP200D, etc.: Indicates that the 150μμ Delay Capacitor in the Second Control Grid Circuit is present.

WRA

7.3 Component Location on Drum Panels.

Panel C3:

TRANSFER COUNTER						ADDRESS COUNTER					
1.W F100 Not Used	1.V F100	1.U F100	1.9 F100	1.8 F100	1.7 F100	1.6 F100 Not Used	1.5 F100	1.4 F100	1.3 F100	1.2 F100	1.1 F100
2.W Not Used	2.V GP100D Not Used	2.U GP100D	2.9 GP100D	2.8 GP100D	2.7 GP100D	2.6 Not Used	2.5 GP100D Not Used	2.4 GP100D	2.3 GP100D	2.2 GP100D	2.1 GP100D
3.W F100	3.V GP100D	3.U GP100D	3.9 GD100	3.8 GD100	3.7 GP100D	3.6 GP300D Not Used	3.5 GP300D	3.4 GP300D	3.3 GP300D	3.2 GP300D	3.1 GP300D
4.W GP200D	4.V GP100D	4.U Not Used	4.9 Not Used	4.8 Not Used	4.7 Not Used	4.6 Not Used	4.5 Not Used	4.4 Not Used	4.3 Not Used	4.2 Not Used	4.1 Not Used

FRONT VIEW

WRA

7.3 <u>Component Location on Drum Panels.</u>

Panel M-1:

1.W Not Used	1.V Not Used	1.U Not Used	1.9 Not Used	1.8 Not Used	1.7 Not Used	1.6 Not Used	1.5 Not Used	1.4 Not Used	1.3 Not Used	1.2 Not Used	1.1 Not Used
2.W GW100	2.V GW100	2.U GW100	2.9 GW100	2.8 GW100	2.7 GW100	2.6 GW100	2.5 GW100	2.4 Not Used	2.3 GP100D	2.2 GP200D	2.1 Not Used
3.W 6BX7	3.V Not Used	3.U 6BX7	3.9 Not Used	3.8 6BX7	3.7 Not Used	3.6 6BX7	3.5 Not Used	3.4 Not Used	3.3 U100	3.2 U100	3.1 Not Used
4.W Not Used	4.V 6BX7	4.U Not Used	4.9 6BX7	4.8 Not Used	4.7 6BX7	4.6 Not Used	4.5 6BX7	4.4 Not Used	4.3 C100	4.2 C100	4.1 Not Used

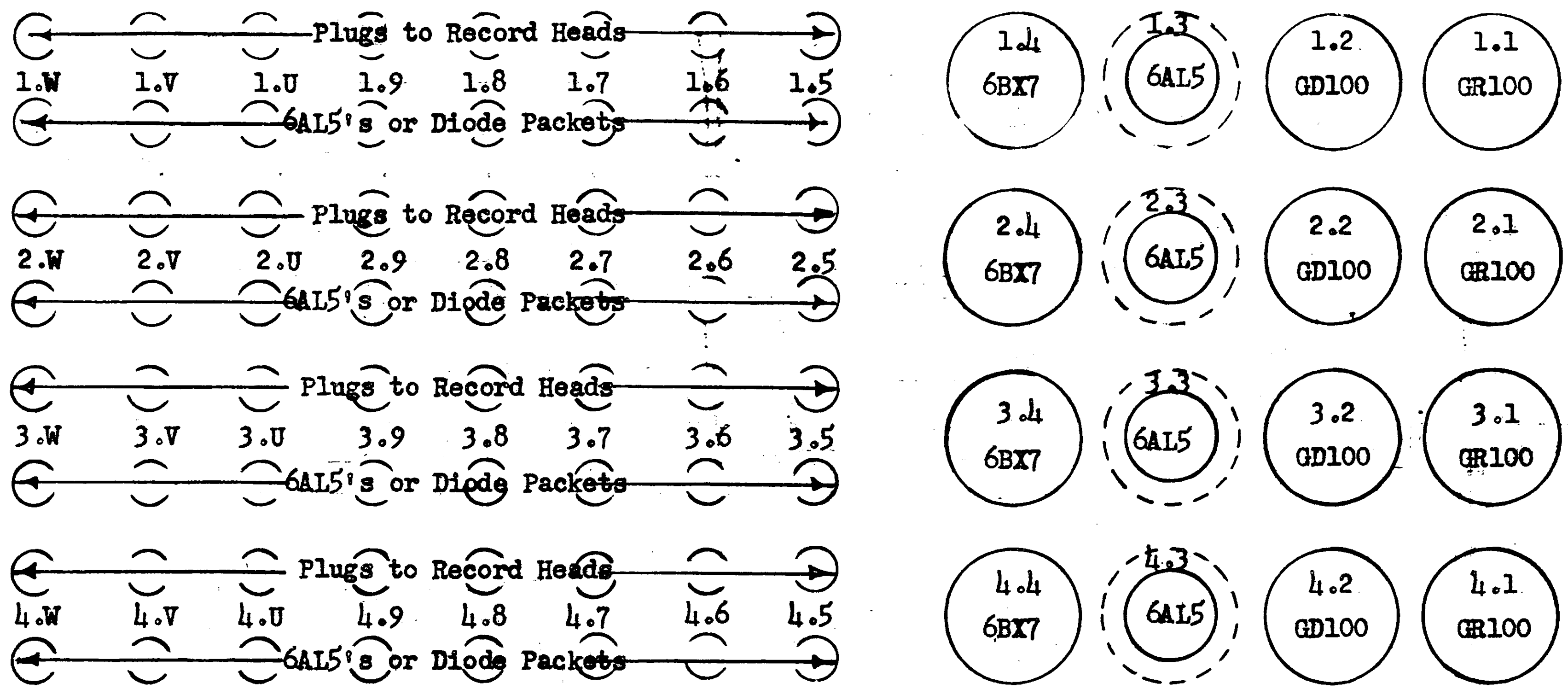
<u>FRONT VIEW</u>

WRQ

CODE: GW100: 100 Series Write Gate
U100: 100 Series Univibrator
C100: 100 Series Cathode Follower

7.3 Component Location on Drum Panels.

Panels S2, S3, S4, and S5.



FRONT VIEW

CODE: GR100: 100 Series Read Gate

WRA

7.3 <u>Component Location on Drum Panels.</u>

Panel S6:

1.W	1.V	1.U	1.9	1.8	1.7	1.6	1.5	1.4	1.3	1.2	1.1
P100	GP100D	GP100	GP100 Not Used	GP100	GP100	CL1	Not Used	Not Used	Not Used	Not Used	Not Used

FRONT VIEW

CODE: P100: 100 Series Peaker using 6AG7
CL1: Clamp Unit

WRA

7.3 Component Location on Drum Panels.

Panel S7:

Pos. 1.6	Pos. 1.5	Pos. 1.4	Pos. 1.3	Pos. 1.2	Pos. 1.1
AP100	AP100	AP100	AP100		
Clock Pulse Playback	Origin Pulse Playback	Word Pulse Playback	Information Playback	Spare	Spare

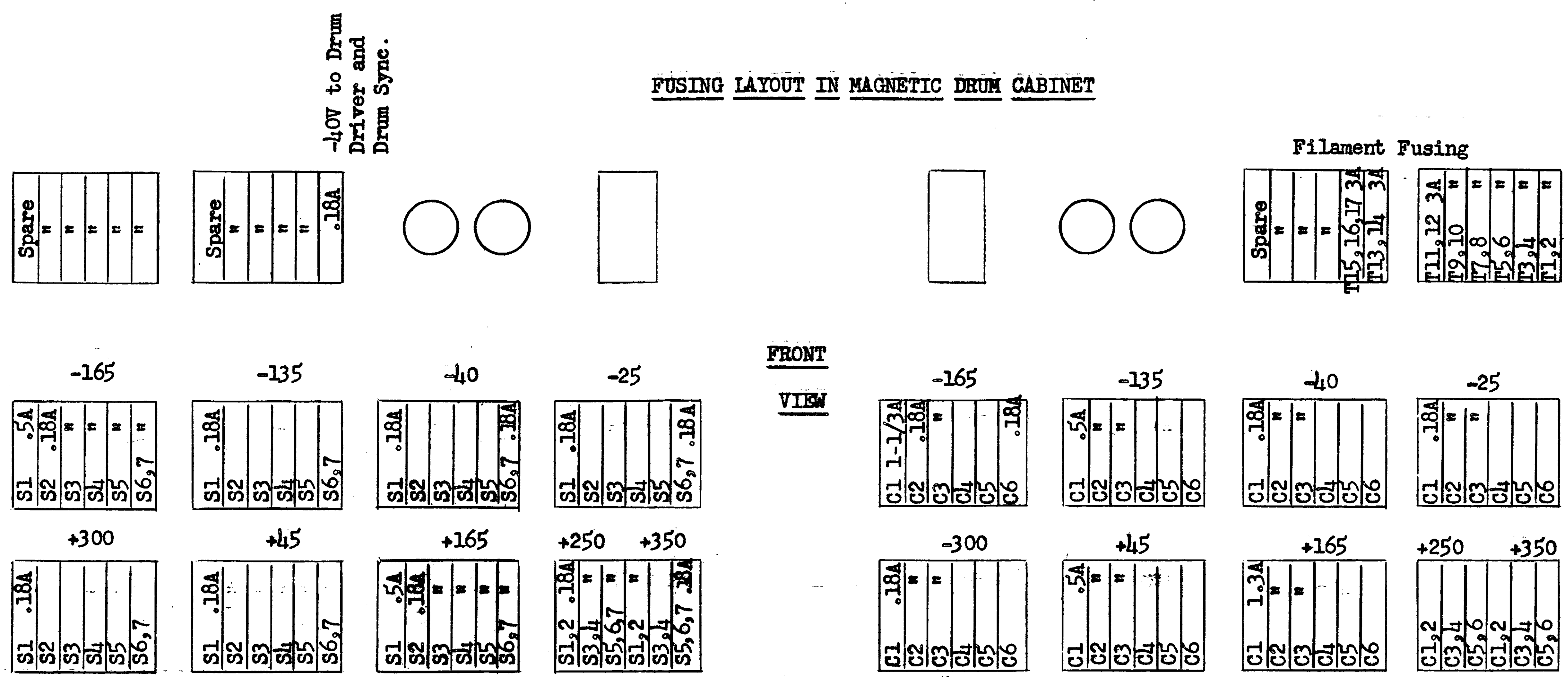
FRONT VIEW

CODE: AP100: 100 Series Playback Amplifier for RZ Recording System

wea

7.3 Component Location on Drum Panels.

FUSING LAYOUT IN MAGNETIC DRUM CABINET



Filament Transformers:
T1 - Panel C1 (-135 DC)
T2 - Panel S1 (-135 DC)
T3 - Panel C1 (DC Gnd)
T4 - Panel S1 (DC Gnd)
T5 - Panel C2 (DC Gnd)
T6 - Panel C2 (DC Gnd)
T7 - Panel C2 -135 Reg. Amp. and -300 Reg. Amp. (-135 DC)
T8 - Panel C3 (-135 DC)
T9 - Panel C3 (DC Gnd)
T10 - Panel S2 (DC Gnd)
T11 - Panel S3 +250 Reg. Amp. (DC Gnd)
T12 - Panel S4 (DC Gnd)
T13 - Series Arm -300V Reg. (DC Gnd)
T14 - Series Arm -135V Reg. (DC Gnd)
T15 - Series Arm 250V Reg. (250V DC)
T16 - Panel S5 (DC Gnd)
T17 - Panel S6, 7 (DC Gnd)

WRA

7.4 General Notes on Magnetic Drum.

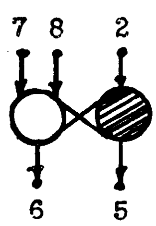
1) Numbers around plug-in unit symbols signify pin connections on 11-pin sockets on panels.

2) Numbers at side of plug-in unit symbols indicate location of unit on panel, from back view reading left to right.

3) All d.c. control lines (inputs and outputs) have voltage levels of 0 volts or -40 volts.

4) Block diagrams used for magnetic drum with 11-pin connections are shown below:

Flipflop

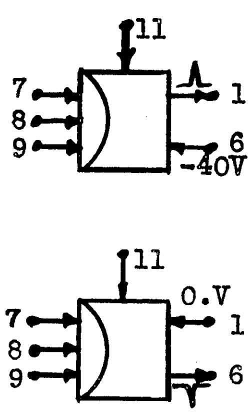


Output is 0 or -40 volts.

The flipflop is triggered by positive pulses applied to the plates.

Thus a pulse on 7 will make plate 6 high.

Pulse Gate

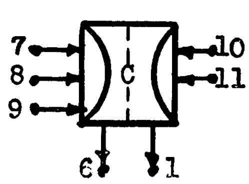


1 or 6 to be returned to voltage level.

Output on other line is positive or negative as indicated.

Terminals 7, 8 and 9 are inputs for d.c. control lines; 11 is for pulse input.

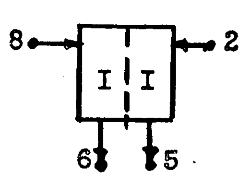
And/Or Circuit



Outputs 1 and 6 may be tied together to produce OR circuit.

D.C. control signals only.

Inverter



D.C. control signals only.

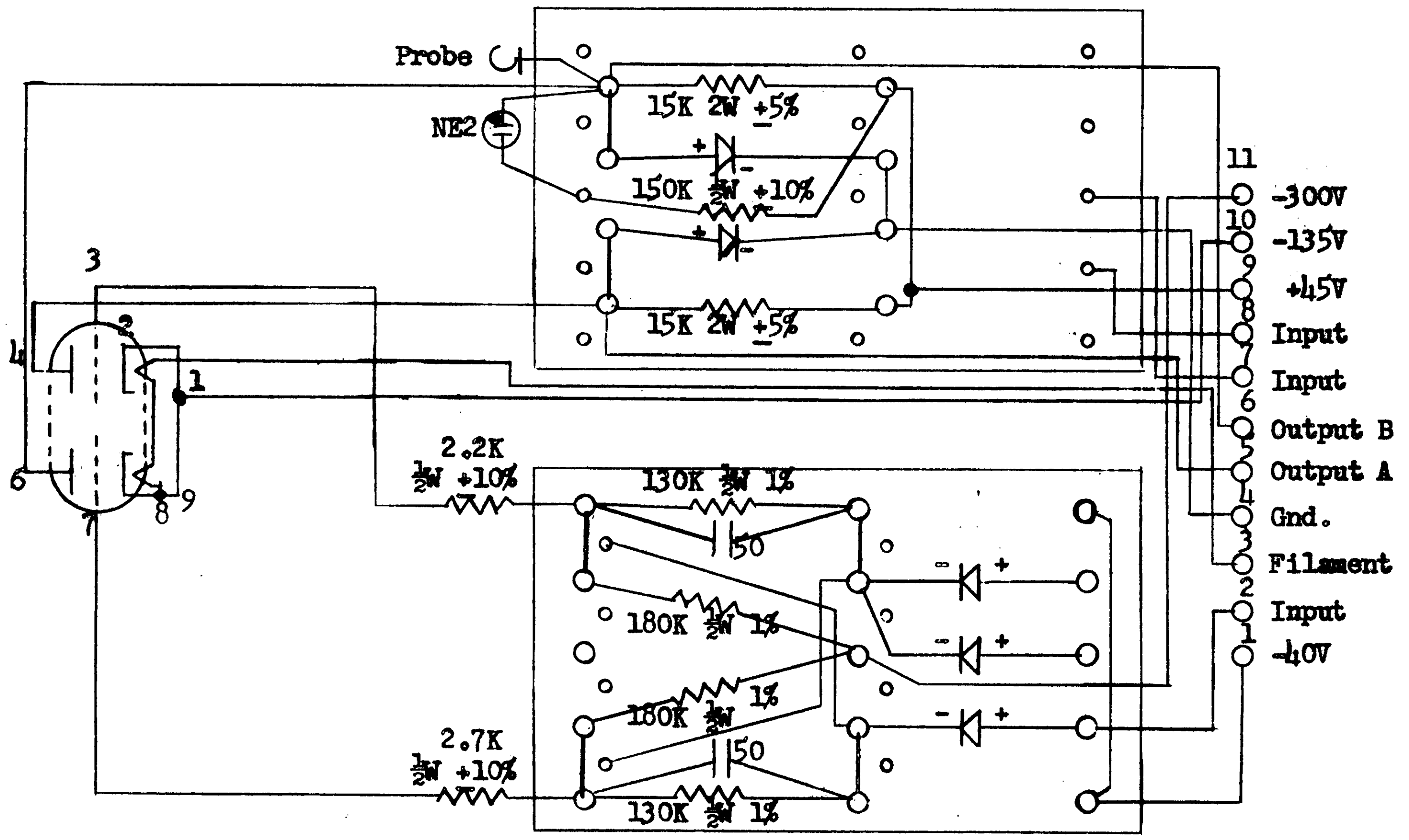
7.4 General Notes on Magnetic Drum.

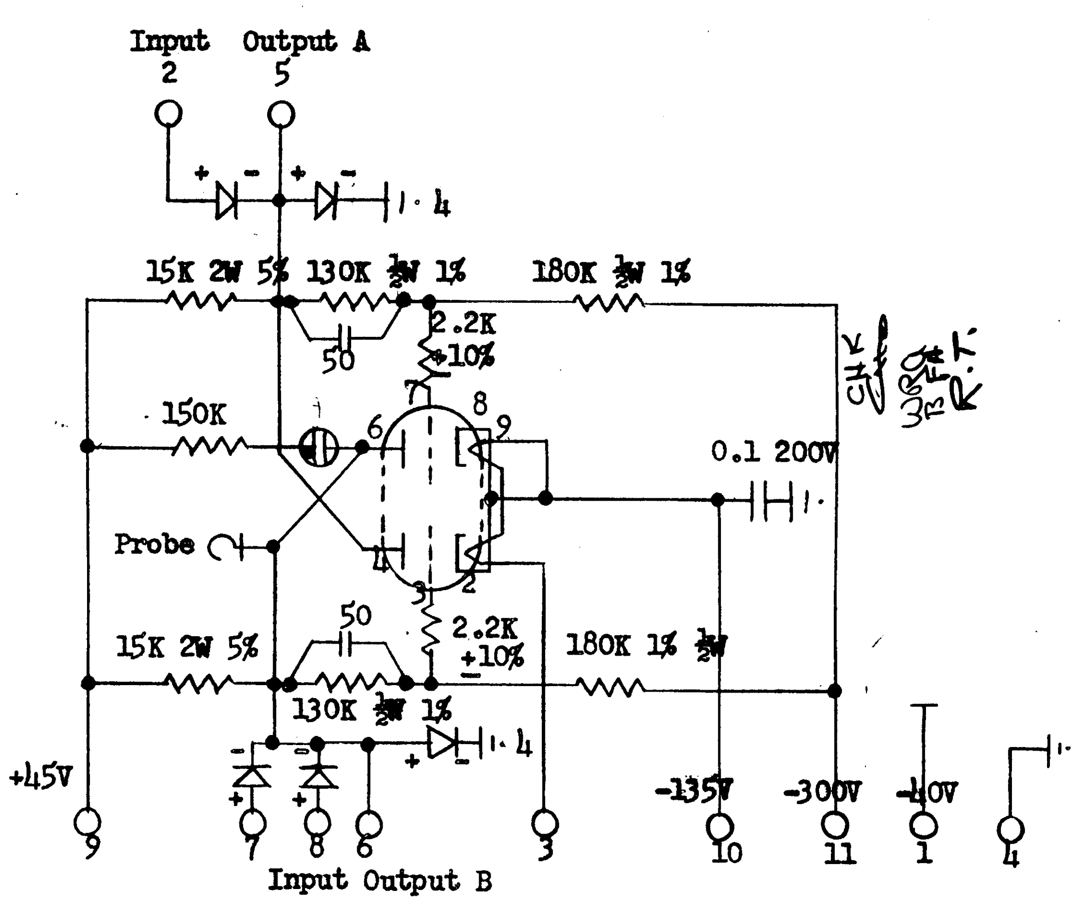
4) A pulse "and" gate will drive 4 flipflops; the pulse across the secondary of the transformer is down to 40 volts. When a pulse gate is used to drive one flipflop a 680 ohm, 1/2 watt resistor should be placed across pins 1 and 6 in back of panel. To drive two flipflops, a 4.7K, 1/2 watt resistor should be used. No resistor is used when driving three or four flipflops.

5) A flipflop can be loaded directly on each plate, or on each plate separately, with 1000 μμfd and a 60K load to the plus 165, and this will not affect the operation of the flipflop circuit. The flipflop has a static output impedance of approximately 50 ohms; while it is in its dynamic state of flipping, impedance is approximately 7K.

8.1 Flipflops and Binary Counters.

2C51 Flipflop and Binary Counter, F100 Series:

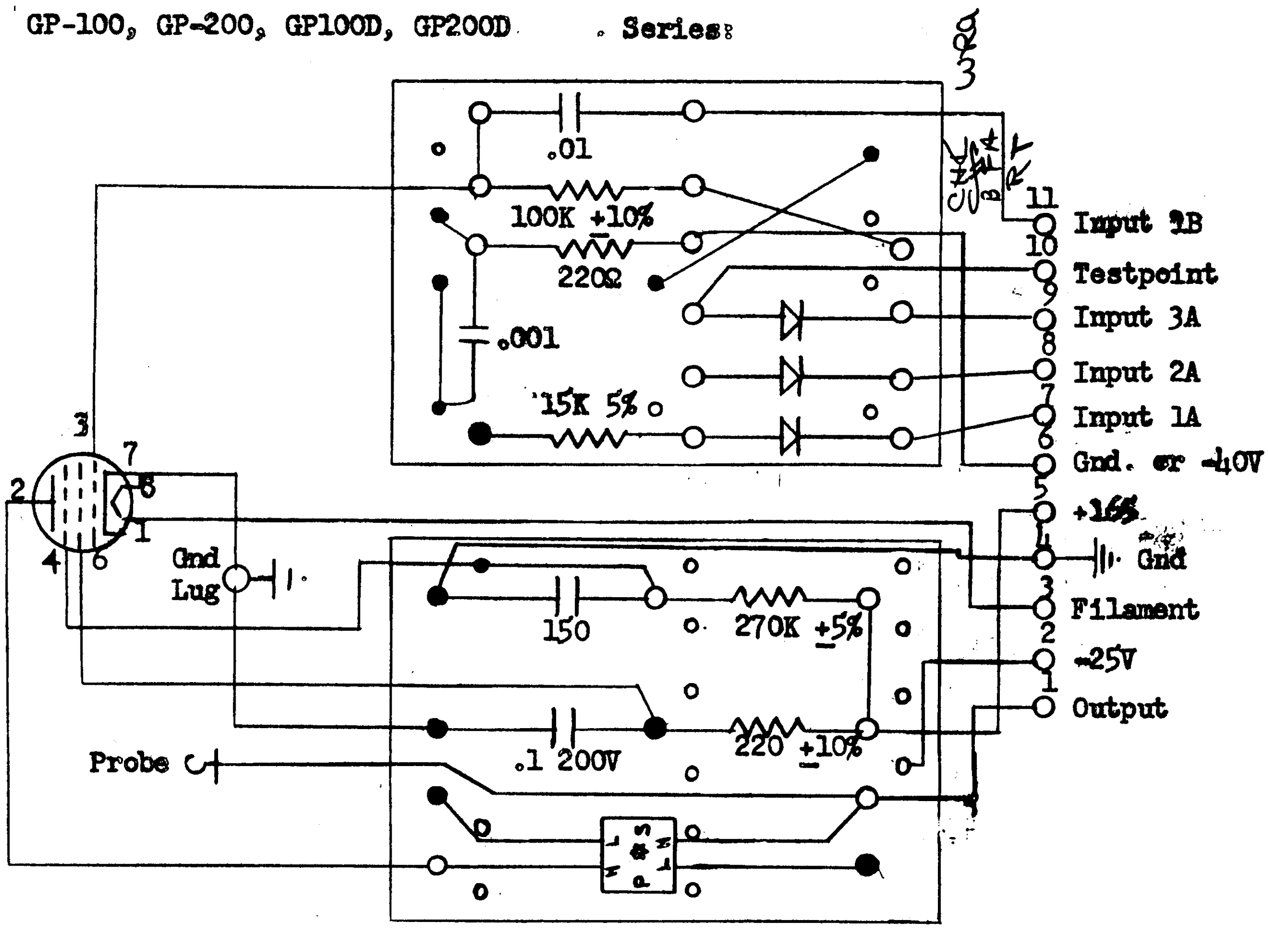




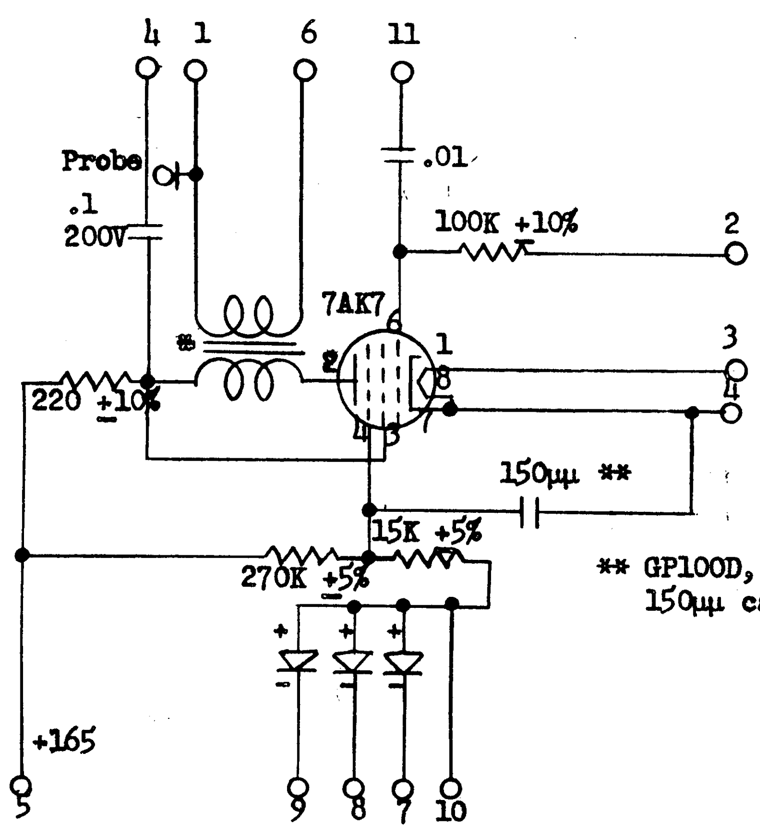
NOTE: All Crystals 1N38, and Filaments are at -135 volts.

8.2 7AK7 Gate.

GP-100, GP-200, GP100D, GP200D . Series:



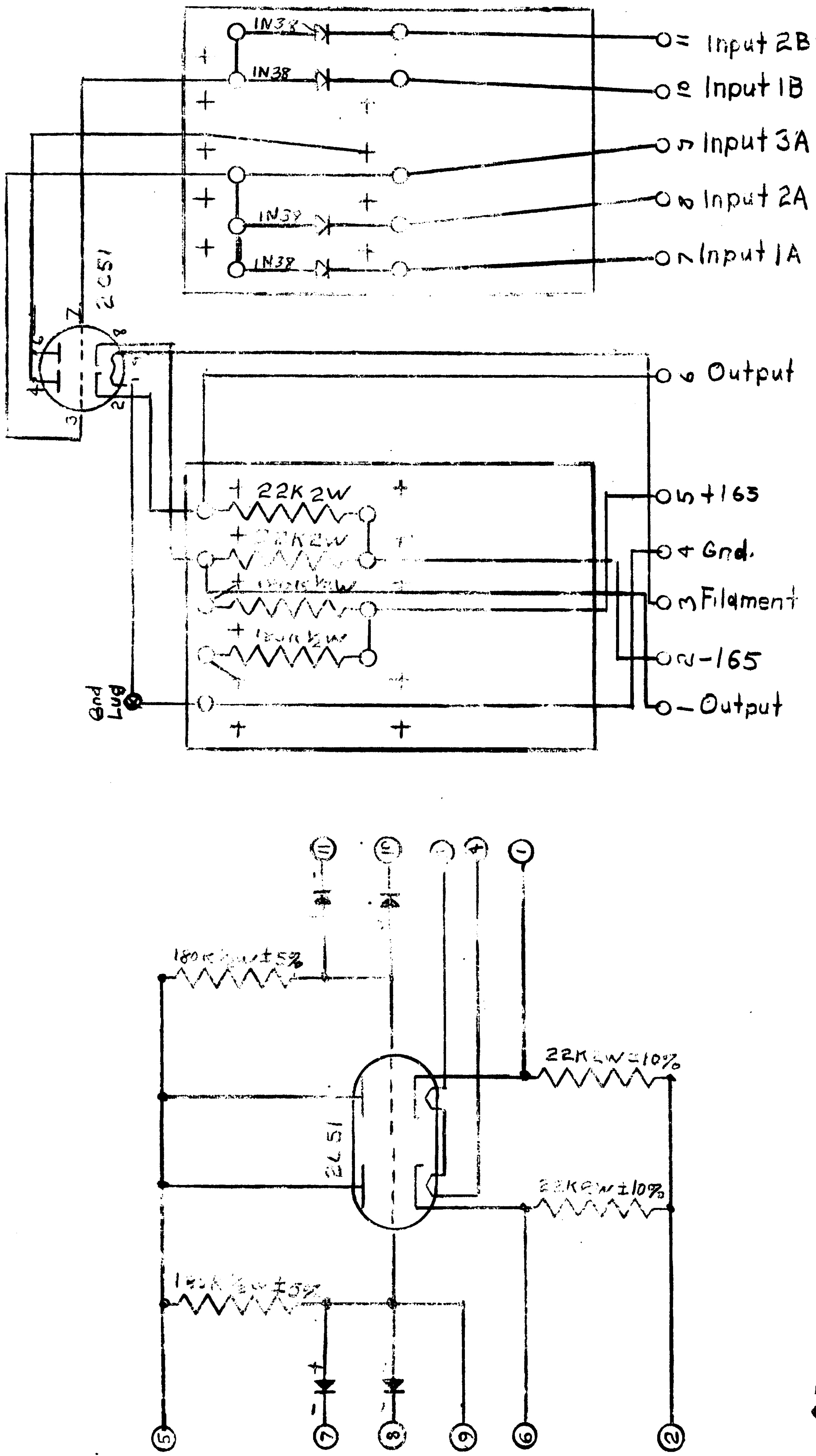
* Transformer: GP100 - Inverting "B"
GP200 - Inverting "C"



** GP100D, GP200D, etc. indicates 150μμ capacitor is present.

NOTE: All Crystals are IN38.

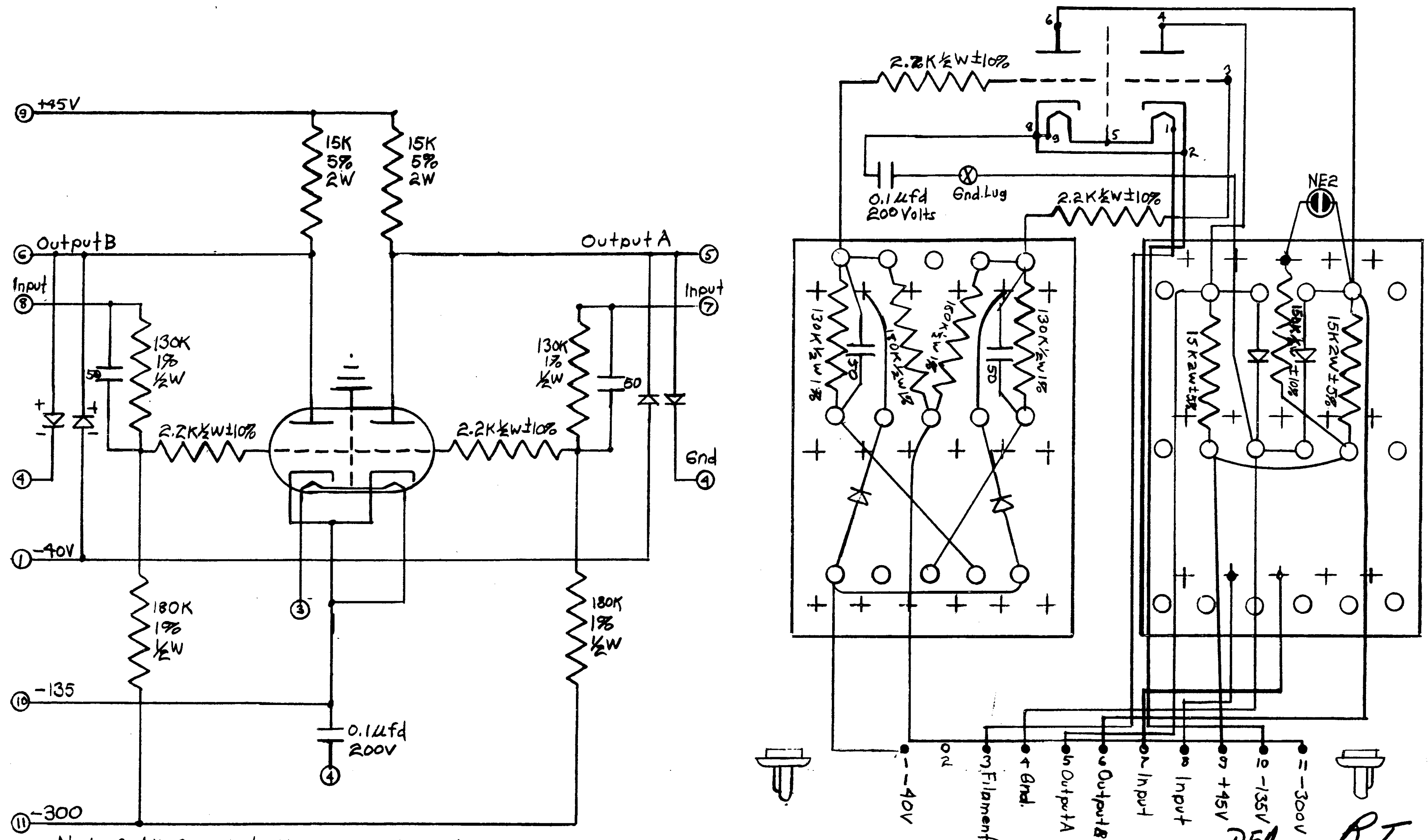
.3 D-C Switch.



D.C. Switch Plug-In Unit

R.T.

8.4 2C51 Inverter.



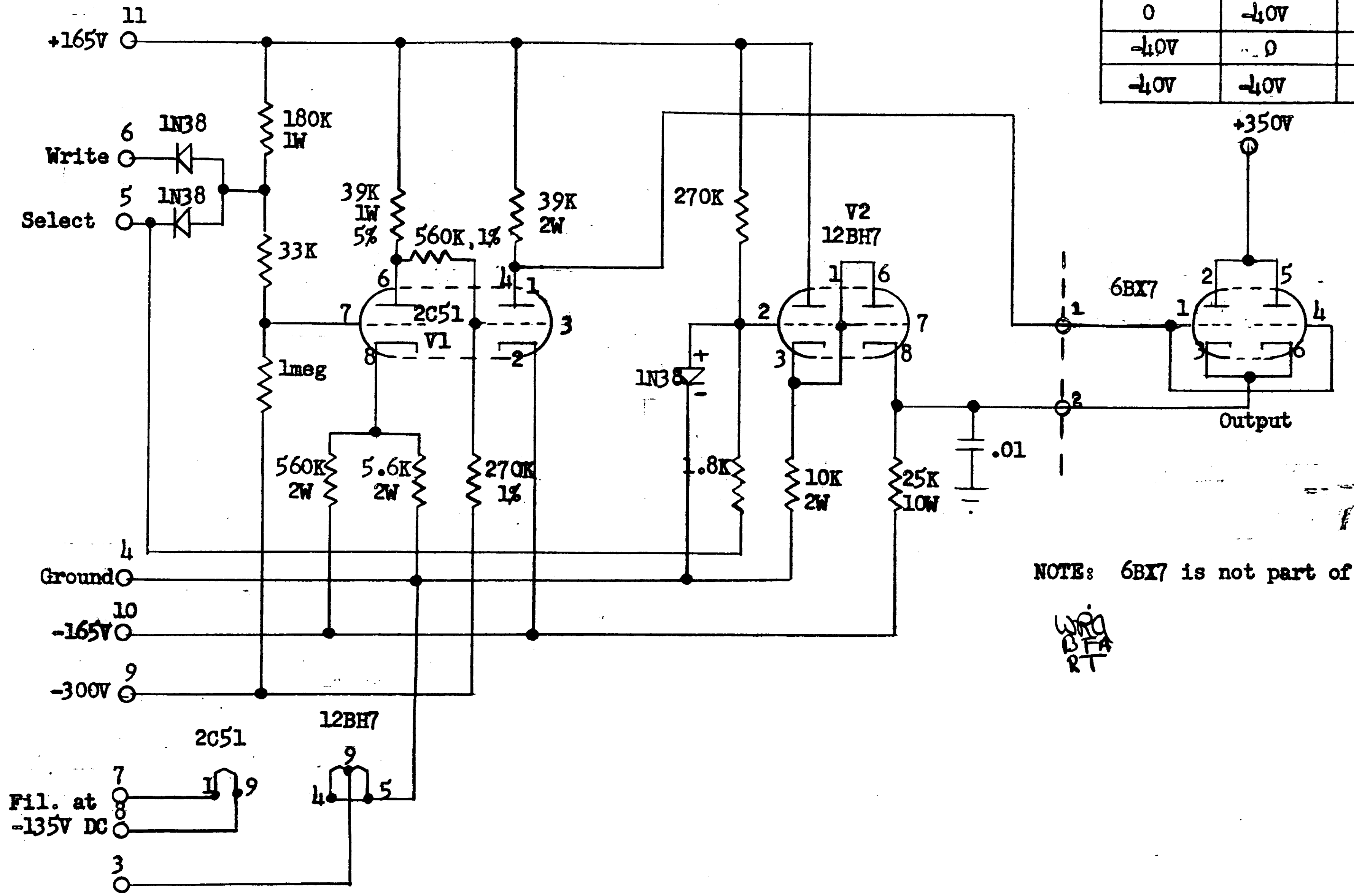
Note: All Crystals 1N38, + Fils. Are At -135 Volts.

Issued 11-6-52
Reissued 7-2-53

8.5 Read-Write Gate.

GW100 Series:

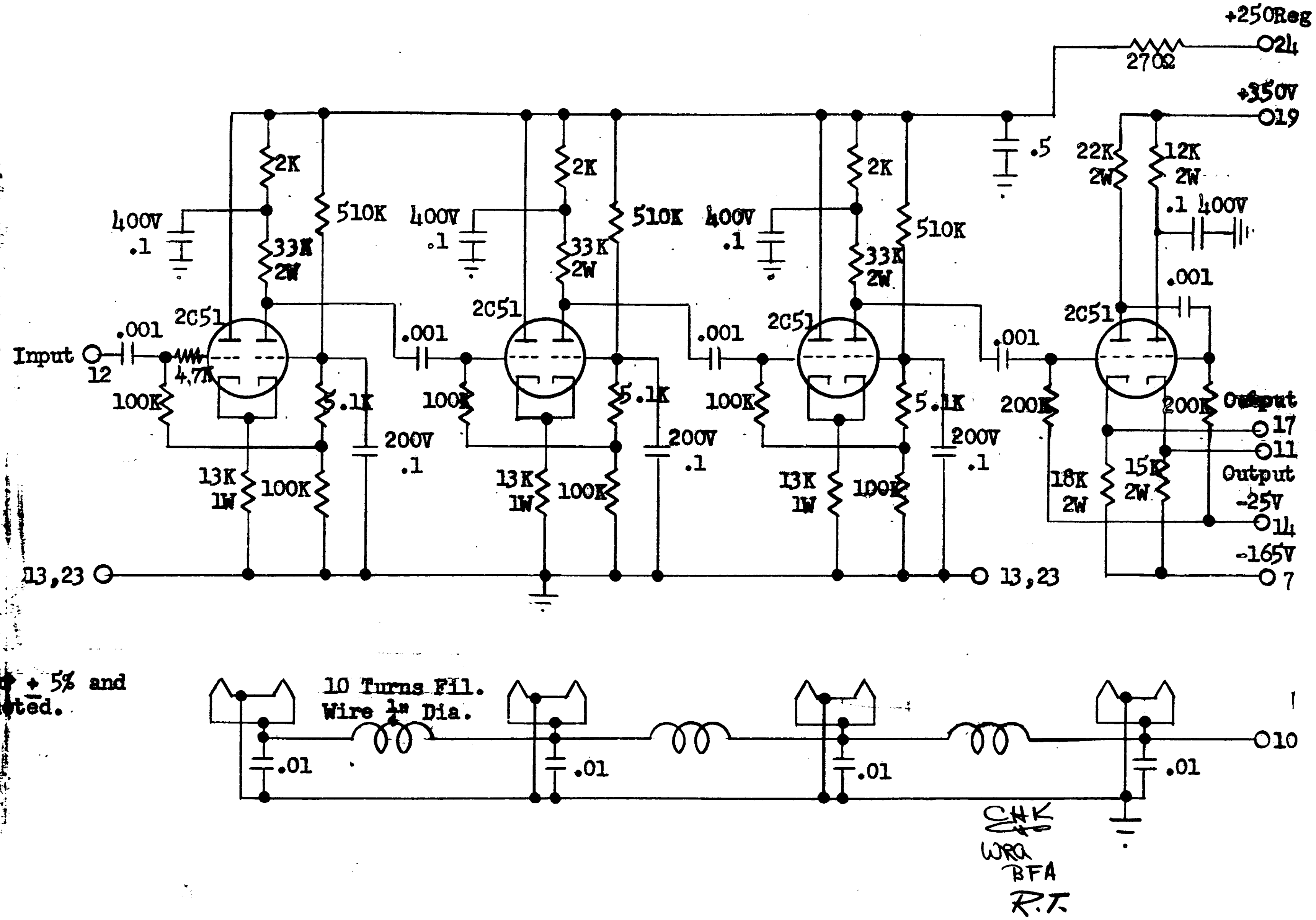
Input		Output
Select	Write	
0V	0V	+180V
0	-40V	+5V
-40V	0	-20V
-40V	-40V	-20V



NOTE: 6BX7 is not part of Plug-In Unit.

8.6 Magnetic Drum Playback Amplifier. (Formerly page B7.3-1)

AP-100 Series:

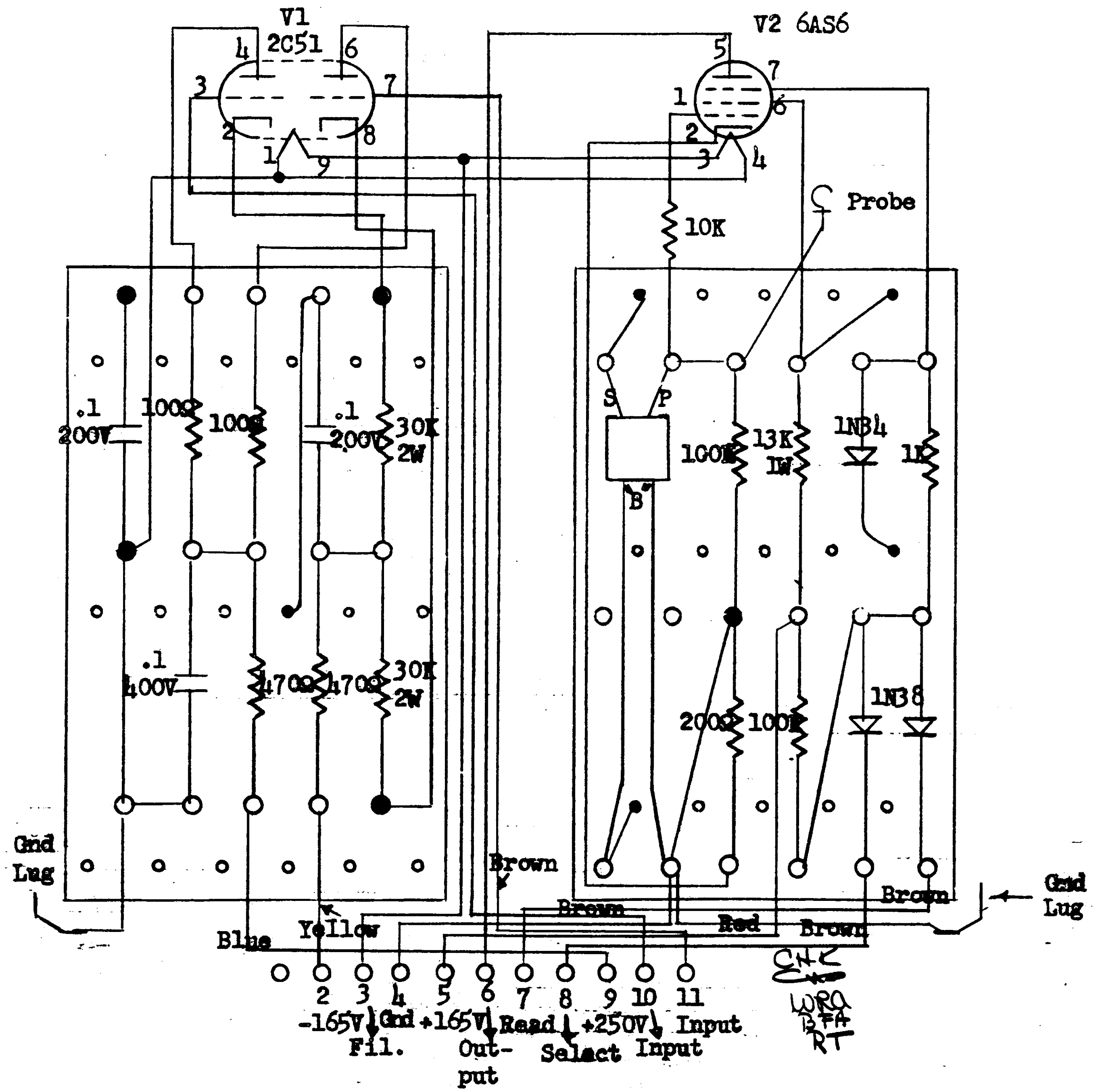


All Resistors ± 5% and ½W unless noted.

Issued 7-2-53

8.7 Read Gate.

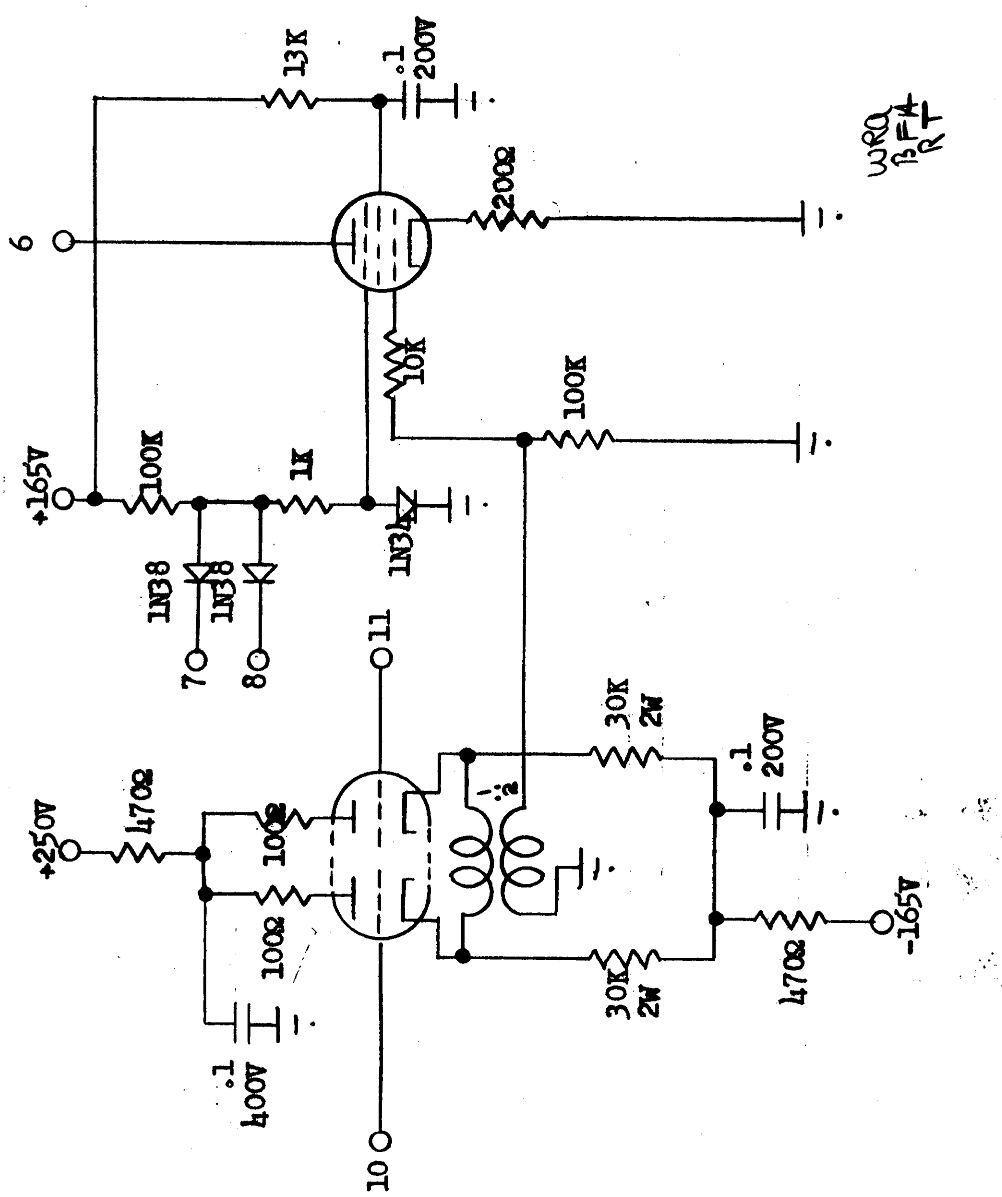
GR-100 Series:



Note: Transformer is connected 1:2 step-up.

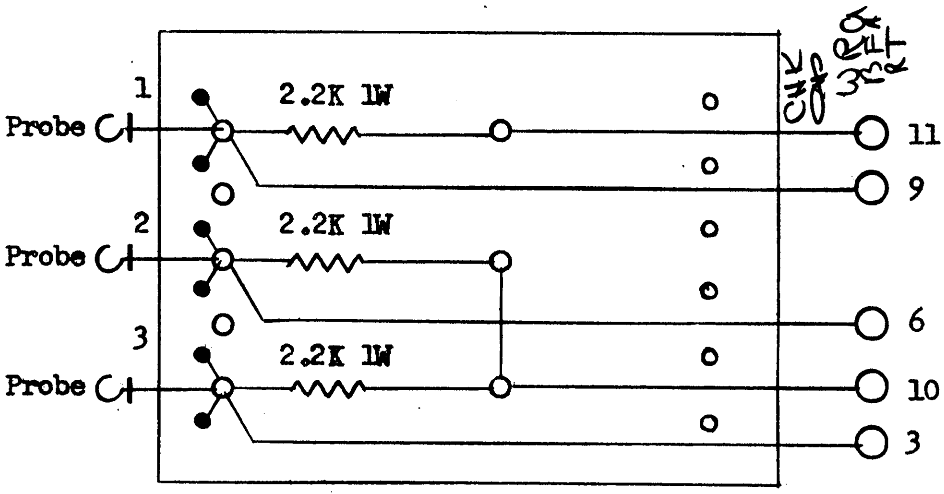
8.7 Read Gate (continued).

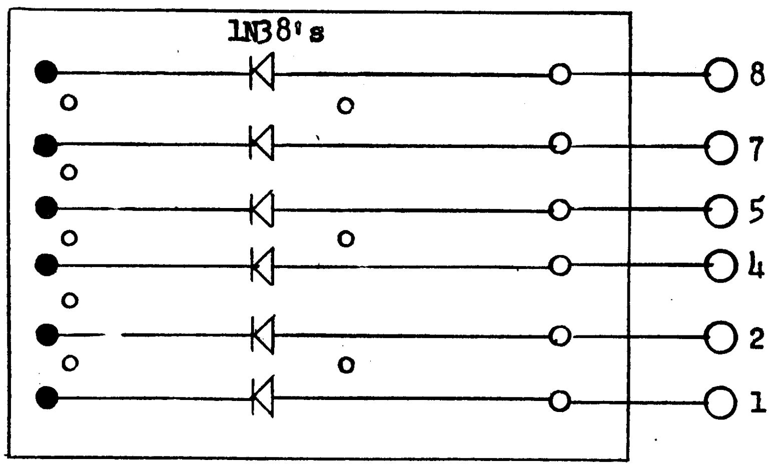
GR-100 Series:

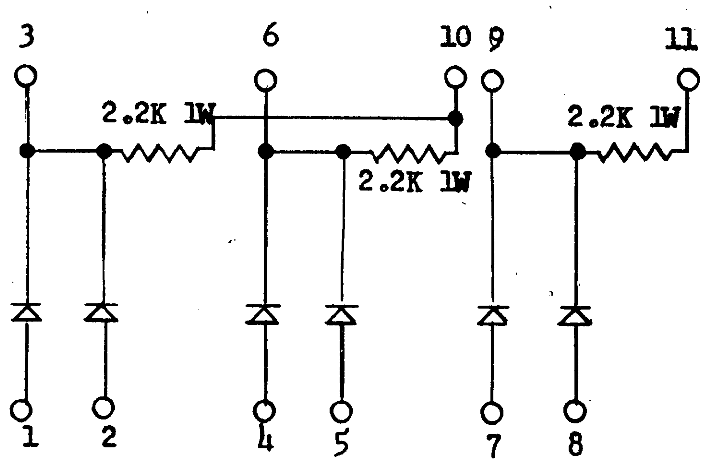


8.8 Positive Pulse Crystal "Or" Circuit.

GO-100 Series:



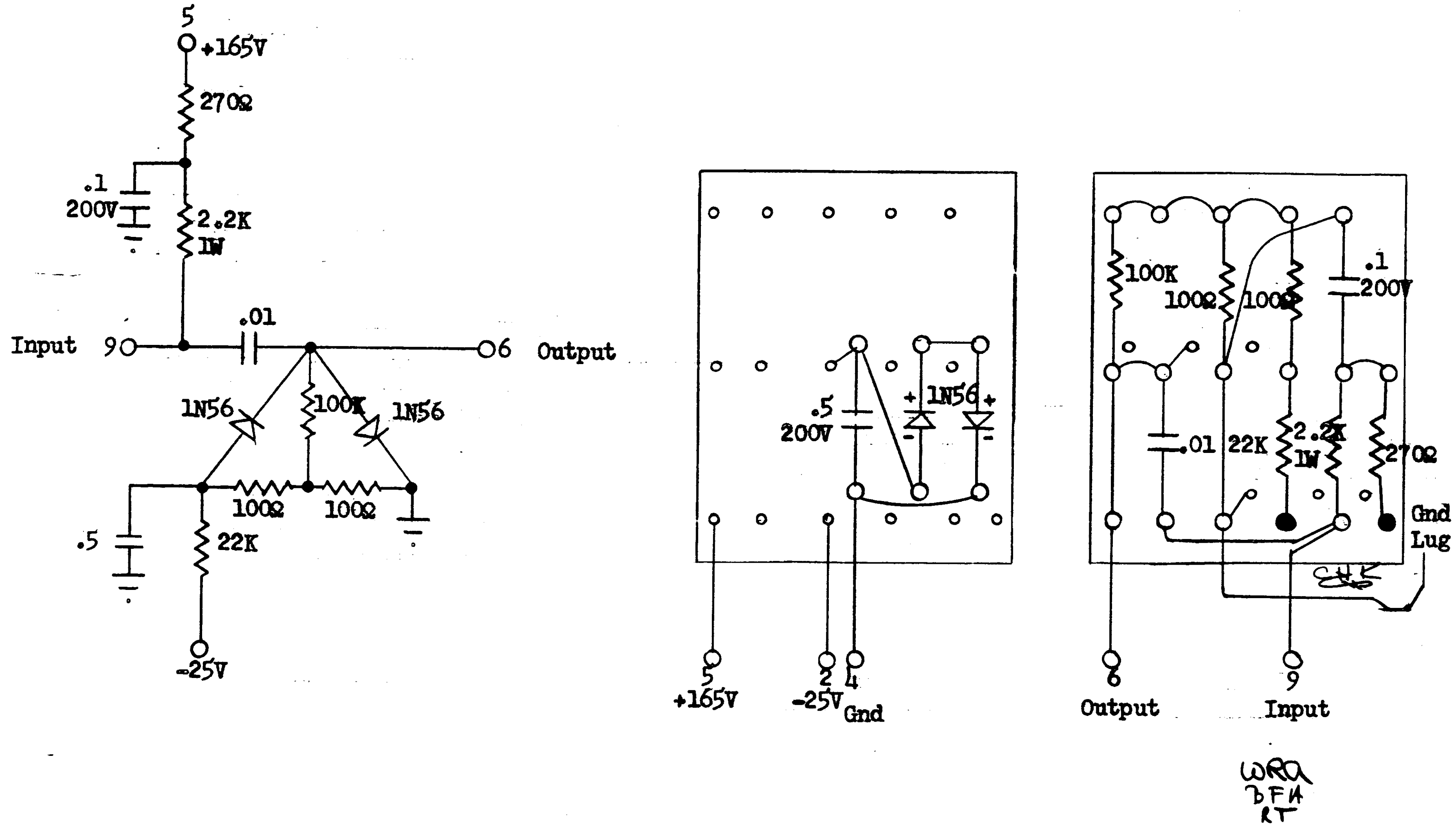




Issued 7-2-53

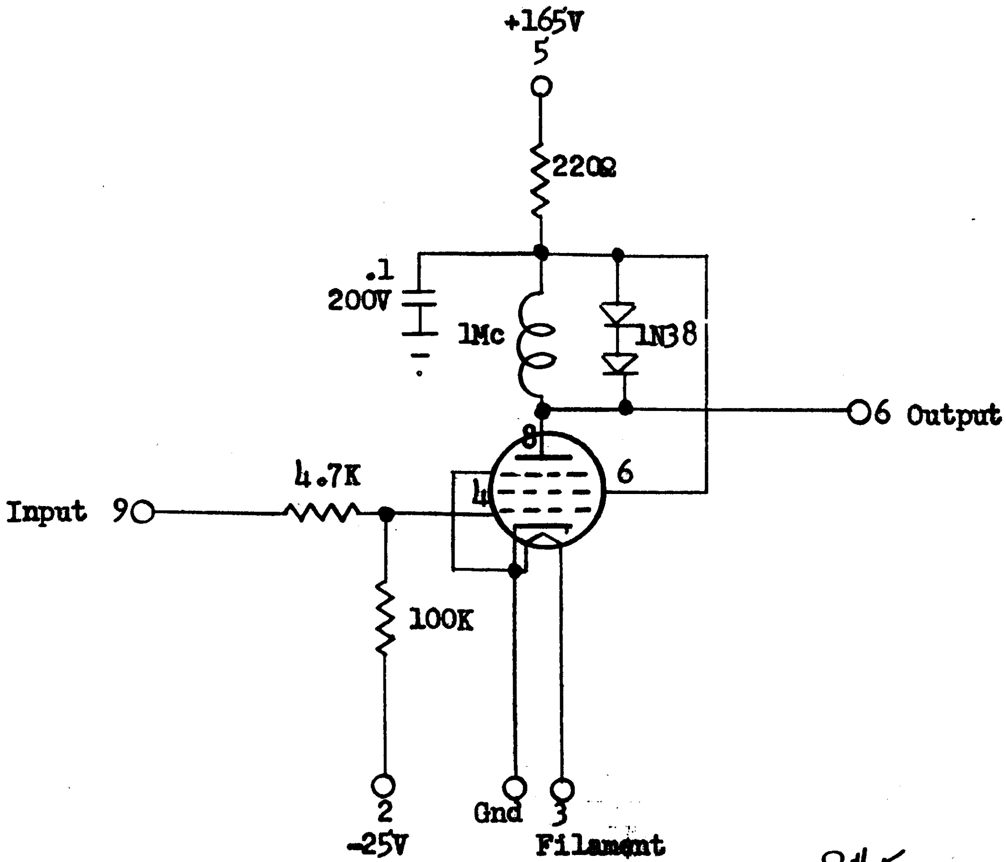
8.9 Voltage Clamping Unit.

CI 1:



8.10 6AG7 Peaker.

P-100 Series:



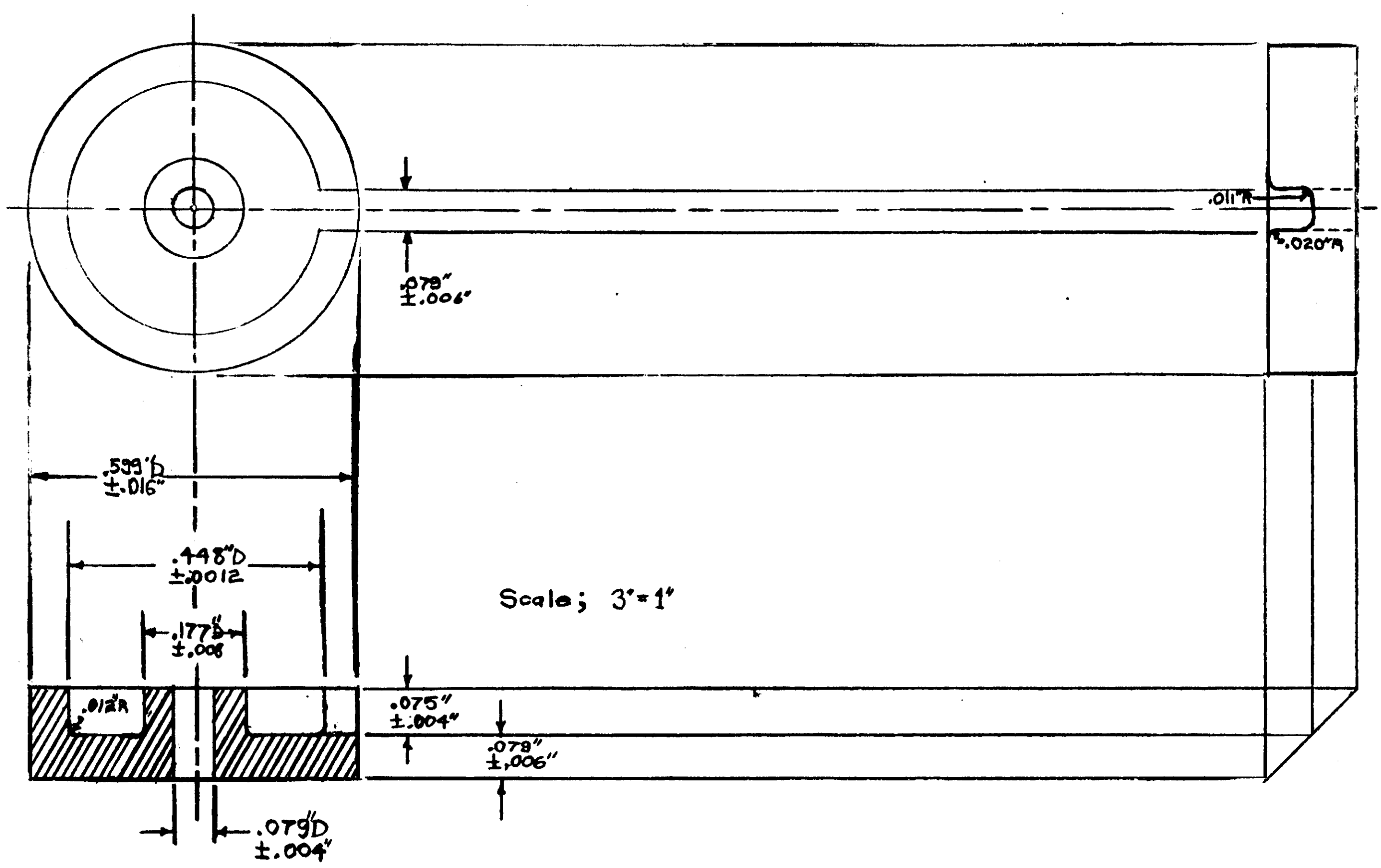
SHK
WRG
JFA
RT

1.2 Design of Pulse Transformers.

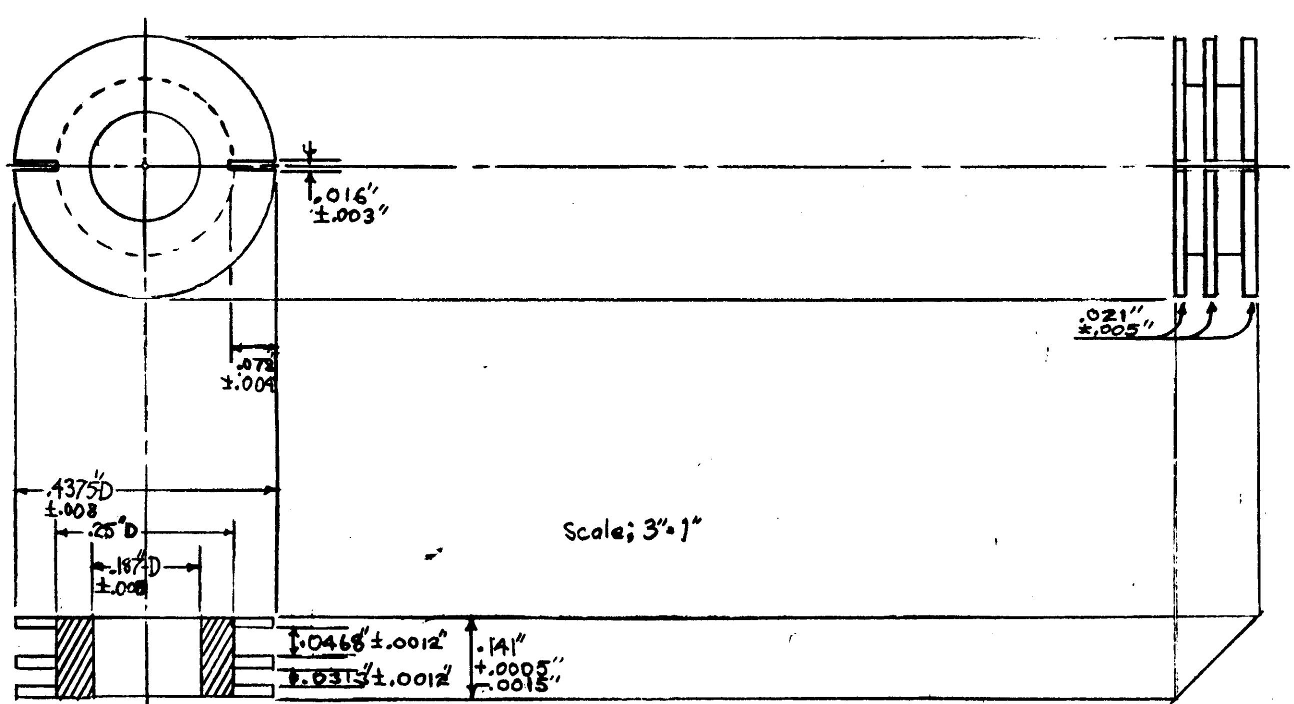
Core Material Used:

Ferroxcube 3C, Pot Core Type 7F154, made by Ferroxcube Corporation of America. Curie point is at 170 degrees centigrade. Permeability M_o is 900.

Core Dimensions:



Bobbin: Made out of a plastic such as vinyl, styrene copolymers, nylon or polzethylene.



B.F.A.

1.3 A Three Digit Accumulator.

An accumulator is the part of the arithmetic unit which is capable of performing the operation of addition. It is able to receive numbers, add them to numbers it already contains, and then transmit the sum to another part of the computer. It is called the accumulator as the sum of successive additions is sometimes accumulated in its A Register. The section of the accumulator which actually does the addition process is composed of circuits known as adders. A separate adder is necessary for each digit of the word (a number or order in digital form) used by the computer. Therefore, if the computer uses a 37 digit word, 37 adders are necessary. Similarly, if the word consists of 3 digits, 3 adders are all that are required.

In the Machine Development Unit Laboratory an accumulator capable of handling 3 digits in parallel fashion has been constructed. "In parallel" means that all digits are added simultaneously rather than in the familiar serial fashion in which the digits are added in sequence starting with the least significant digit. The binary number system is used. As this accumulator can not handle more than three digits, it can only take care of numbers which can be represented in the binary system with 3 binary digits. Decimal numbers which can be so represented are:

0 = 000

1 = 001

2 = 010

3 = 011

4 = 100

5 = 101

6 = 110

7 = 111

This three digit accumulator is composed of three adders operated in parallel as shown in Figure 1 on the following page.

1.3 A Three Digit Accumulator.

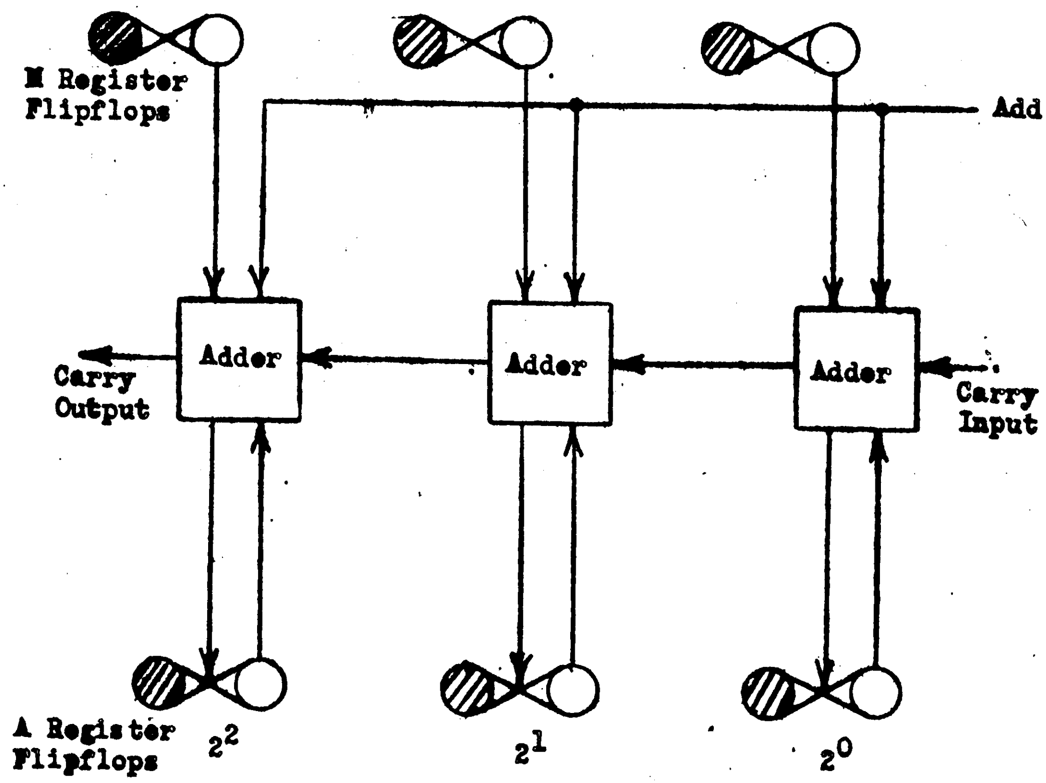


Figure 1. A Three Digit Accumulator

The adder when supplied with an add pulse adds the information in the M Register to that contained in the A Register. The following table lists conditions which may be given to the adder and the subsequent results:

Conditions	State of Registers			Results	
	M Reg.	A Reg.	Carry Input	A Reg.	Carry Output
1	0	0	1	Becomes 1	None
2	0	1	1	Becomes 0	Carry output produced
3	1	0	0	Becomes 1	None
4	1	1	0	Becomes 0	Carry output produced
5	1	0	1	Remains 0	" "
6	1	1	1	Remains 1	" "

Table 1. Conditions and Results

These operations are performed through the use of crystal coincidence and "or" circuits. A block schematic of a typical adder is shown in Figure 2.

1.3 A Three Digit Accumulator.

action of "-and +not" which would normally operate with M negative in the presence of an add pulse. Since there is no output from the "-and +not" gate the A Register is not triggered and remains in state "0".

Condition 6: M, negative output; A, negative output; Carry Input, positive pulse. Both the "-and" gates operate producing the carry output. The output from "-and #1" inhibits the action of the "-and +not" gate, thus the A Register remains in state "1".

Table 2 shows how the A Register accumulates the sum of the successive additions performed by the adders.

Add by	1's		2's		3's		4's		5's		6's		7's	
	Bin.	Dec.	Bin.	Dec.	Bin.	Dec.	Bin.	Dec.	Bin.	Dec.	Bin.	Dec.	Bin.	Dec.
M Reg. / A Reg.	001	1	010	2	011	3	100	4	101	5	110	6	111	7
A_0	000	0	000	[illegible]	000	0	000	0	000	0	000	0	000	0
A_1	001	[illegible]	010	[illegible]	011	3	100	4	101	5	110	6	111	7
A_2	010	2	100	[illegible]	110	6	000	8	010	10	100	12	110	14
A_3	011	3	110	[illegible]	001	9			111	15	010	18	101	21
A_4	100	4	000	8	100	12			100	20	000	24	100	28
A_5	101	5			111	15			001	25			011	35
A_6	110	6			010	18			110	30			010	42
A_7	111	7			101	21			[illegible]	35			001	49
A_8	000	8			000	24			000	40			000	56

Table 2. Accumulative Sum of Successive Additions

To explain the preceding table, let us consider as an example adding by 2's. The state of the A Register before the first addition pulse is supplied is signified by A_0. A_1 represents the condition or state of the A Register after the first addition has taken place, A_2 after the second, et cetera.

1.5 Temperature Sensitivity of Nobleloy and Phaostron Resistors.

PHAOSTRON, 180K, 1 %, 1/2W

Sample No.	Temperature and Time				Max. % Change
	76.5°	96° 5 minutes	96° 10 minutes	96° 15 minutes	
1	180,400	180,200	180,000	180,000	0.22
2	180,400	180,100	180,100	180,100	1.17
3	181,900	181,900	181,900		0.00
4	180,300	180,000	180,000		0.17
5	180,000	180,000	180,000		0.00
Average					0.11

NOBLELOY, 82K, 1 %, 1/2W

Sample No.	Temperature and Time				Max. % Change
	75.5°	95.5° 5 minutes	95.5° 10 minutes	95.5° 15 minutes	
1	82,660	81,800	81,990	82,040	1.04
2	82.530	82,350	82,350	82,350	0.22
3	82,530	82,330	82,330	82,330	0.24
4	82,820	82,220	82,220	82,220	0.72
5	82,720	82,540	82,540	82,540	0.22
Average					0.49

L. Mitchell

1.6 Peaking Coil Design Data.

Peaking Coil Characteristics

Type	Pulse Width	Inductance	DC Res.	Q at Oper. Frequence	Turns	Wire	O.D.	I.D.	Length
1 MC	.5 μS	.75 MH	20 Ohms	25	250	38 Silk	9/16"	3/8"	5/32"
5 MC	.1 μS	47 MH	2.5 Ohms	120	82	33 Ena.	1/2"	1/2"	3/4"

Coil Winder Set Up

Type	Drive Wheel	Idle Gear	Cam Gear	Cam	Coil Form			Turns	Type of Winding
					Diameter	Length	Material		
1 MC	76	60′ 60	74	.188	3/8"	3/4"	Phenolic	250	Universal
5 MC	100	50 50	90	* *	1/2"	7/8"	Polysterene	82	Single Layer

EPM

N.F.L.

1.7 Design Features of Magnetic Drum Memory.

The National Bureau of Standards Western Automatic Computer is a high speed electronic digital computer using a parallel electrostatic memory of the cathode ray tube type. The capacity of this memory is 256 words of 37 binary digits each with an access rate of one word per 16 microseconds. Due to the relatively limited size of this memory it is highly desirable to add an auxiliary memory such as a magnetic drum.

A drum memory, as contrasted with an electrostatic memory, may have an extremely large capacity. However, access to this memory is generally slow. In particular, if information is required from some small specific location on the drum, the computer may have to wait up to a maximum of one drum revolution before receiving any information. This waiting time, or access time, is measured in milliseconds as compared with only a few microseconds for the electrostatic memory. As an illustration: if memory cells were selected at random from the electrostatic memory and also from the drum memory, approximately 500 words could be read in or out of the electrostatic memory for every one word from the drum.

A high speed computer, solving a problem which requires a relatively large number of referrals to a magnetic drum memory may therefore be seriously slowed down if operated in this manner. This situation may be improved in two ways. In the first place, numbers could be transferred in sizeable blocks from the magnetic drum memory to the electrostatic memory of the computer, thus minimizing the total number of referrals. Secondly, these blocks of numbers could be so arranged in the drum memory as to cut down or even completely eliminate any dead waiting time for the drum, i.e., time taken for the drum to come to some specific position before read-out or recording of information begins. One manner in which this could be accomplished is to store the numbers of each block sequentially around the circumference of the drum (cf. Fig. 1, page C1.7-6) so that one block completely fills one band or a channel. When a transfer to or from the drum memory is made, the whole channel is handled at one time. Transfer of information starts immediately after the proper channel has been selected and continues for exactly one drum revolution, thus eliminating

1.7 Design Features of Magnetic Drum Memory.

all waiting time. By these means the average access time per word can be kept quite small and the previous speed ratio of 500:1 for electrostatic v.s. the drum memory may easily be reduced to 16:1 or less.

The magnetic drum memory for the SWAC has been designed along these lines. Information is stored serially on the drum in 40 binary digit words. The first 36 digits represent numerical information, the 37th digit the sign, while the remaining 3 digit positions are empty. Thirty-two words are stored in each channel and constitute a basic transfer block. A corresponding memory block in the cathode ray tube memory consists of two adjacent lines in the storage raster where each line contains 16 memory cells. A one-to-one correspondence is set up between the magnetic drum memory channel and the line-pair of the electrostatic memory so that to any word space on the channel corresponds one and only one definite storage cell in every line-pair of each storage tube. Thus word space number 9 on the drum always goes to memory cell 9 of a particular line-pair (see Figure 1). However, which line-pair goes with which channel is under the choice of the coder.

The main components of the magnetic drum memory and their relation to the SWAC are shown in the block diagram of Figure 2, page C1.7-7. The drum itself contains 192 information channels plus 4 timing channels. These timing channels feed a timing generator which generates a pulse for each digit space, a pulse for each word space, and a reference pulse for each revolution of the drum. The pulses marking each word space go to the Address Counter which counts from 0 through 31. This counter continuously keeps track of which word space is currently passing under the magnetic read-write heads. The reference pulse is used to initially synchronize this counter with the drum.

Read-out of information from the drum to the electrostatic memory involves the following main components of the SWAC proper.

1. The Function Table

   This element is a diode matrix which decodes the operation digits of an instruction.

1.7 Design Features of Magnetic Drum Memory.

2. The C Register

This register is used for storing an instruction and connects with such control circuitry as is necessary for the instruction to be carried out.

3. The R Register

This register communicates with all types of input-output equipment connected to the machine.

4. The S Register

The function of this register is to select a memory cell in the electrostatic memory.

5. The Electrostatic Memory

The read-out operation proceeds as follows:
The function table of the SWAC control unit first indicates an input from the drum. The C register of the SWAC stores the information as to which drum channel is to be mapped onto which line-pair of the electrostatic memory. That portion which specifies the drum channel is transferred to the channel selection register in the drum control which then operates the selection matrix and connects the correct channel through proper amplifiers and gates to the SWAC.

The remaining information in the C register is transferred to the S register (within the SWAC) which selects the proper line-pair in the electrostatic memory.

The particular address that happens to be in the drum address counter at the beginning of the next complete word is also transferred to the S register. This information is used to pick out the particular memory cell of the selected "line-pair" corresponding to the word space that is just about to be read-out from the drum. The drum address counter thus has complete control over selecting the particular cells within the line-pair whereas the line-pair itself is selected by the SWAC control circuitry. If the address counter happens to read 9 when the first transfer is made it will start with point 9 of the line-pair and proceed through 31; then come back to zero and proceed through 8. The transfer counter counts

1.7 Design Features of Magnetic Drum Memory.

the number of transfers from the address register to the S register and thus insures that only the 32 words or the information occupying one channel are transferred.

The electrostatic memory operates in parallel and asynchronously from the serial magnetic drum memory. Therefore, direct communication between the two is not possible. Information from the drum must first be played back into a vacuum tube shifting register and then transferred in parallel to the electrostatic memory. The R register of the SWAC is used for this purpose. The A register can also shift and both registers may be used if a higher rate of information transfer is desired. After the information has arrived in the R register it must wait there until access to the electrostatic memory is available. Arrival of further information from the drum must be halted until this transfer has been completed and the R register cleared again. Access to the electrostatic memory however can be had within 16 microseconds and the maximum time required for the complete transfer operation from the R register to the electrostatic memory is less than 24 microseconds. Transfer of information from the drum to the R register has therefore to be suspended for only 24 microseconds between any two words. This is best accomplished by leaving a blank space on the drum between words. It is now apparent why each word on the drum consists of 37 information spaces plus 3 blank digits. Each digit takes 13 microseconds to play back so the three empty digit spaces give a total delay of 39 microseconds between words. This delay is more than adequate for transferring a number from the R register to the electrostatic memory and clearing R for receiving new information.

The timing generator, the address and transfer counters, and the memory control circuits (see Fig. 2) have all been constructed of simple single tube plug-in units. Only four basic circuits have been used to build up all of the required operations. These are: a flipflop, an inverter, a pulse gate, and a d.c. gate. A good deal of development was carried out to make these units as independent as possible of the vacuum tube characteristics. In addition, all circuits had to pass satisfac-

1.7 Design Features of Magnetic Drum Memory.

emission and poor cut-off, before any given design was accepted as a standard unit. To give an idea of how insensitive these circuits have been made to tube characteristics, our flipflop which is designed around the 2C51 operates equally well with any of the double triodes 5687, 12BH7, 12AU7 or 12AT7 without any circuit changes whatever. Moreover, the plate outputs of all of these flipflops are identical, and it is not possible to tell which tube type is being used by simply inspecting the output voltages.

The magnetic memory selection system features a high level gating system as shown in Figure 3, page C1.7-8. For writing, a 6L6 cathode follower supplies power to a single row of 16 record heads. A pair of 6Y6's are used to drive a single column of 12 record heads. The particular head selected is one at the intersection of a row and a column. In this manner only 44 power tubes are required to drive the total of 192 record heads. The diodes shown in series with these heads are two IN38's connected in series to withstand a transient back voltage of some 150 volts. The record windings on these heads are also used for playback. A read signal applied to the 2C51 cathode follower determines which particular row is selected. The selection of a specific column (one out of 16) is done by a second set of gates (not included in Fig. 3).

The entire magnetic drum memory with a capacity of over 6000 words will when completed contain only some 250 vacuum tubes.

1.7 <u>Design Features of Magnetic Drum Memory</u>.

One to One Correspondence Between Single Channel on Drum and Pair of Lines in CRT Memory:

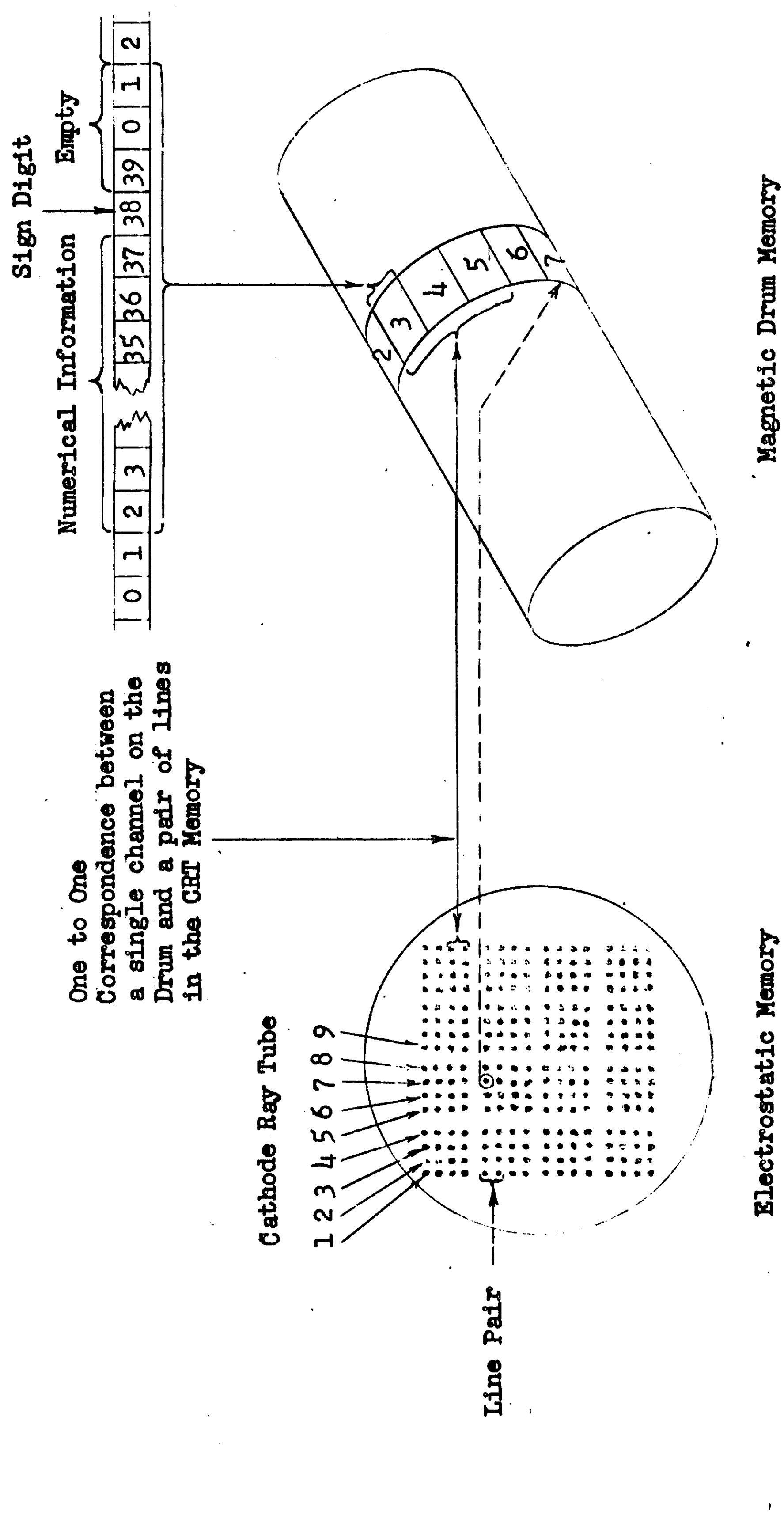


FIGURE 1

1.7 <u>Design Features of Magnetic Drum Memory</u>.

Block Diagram of Component Relationship Between Magnetic Drum and SWAC:

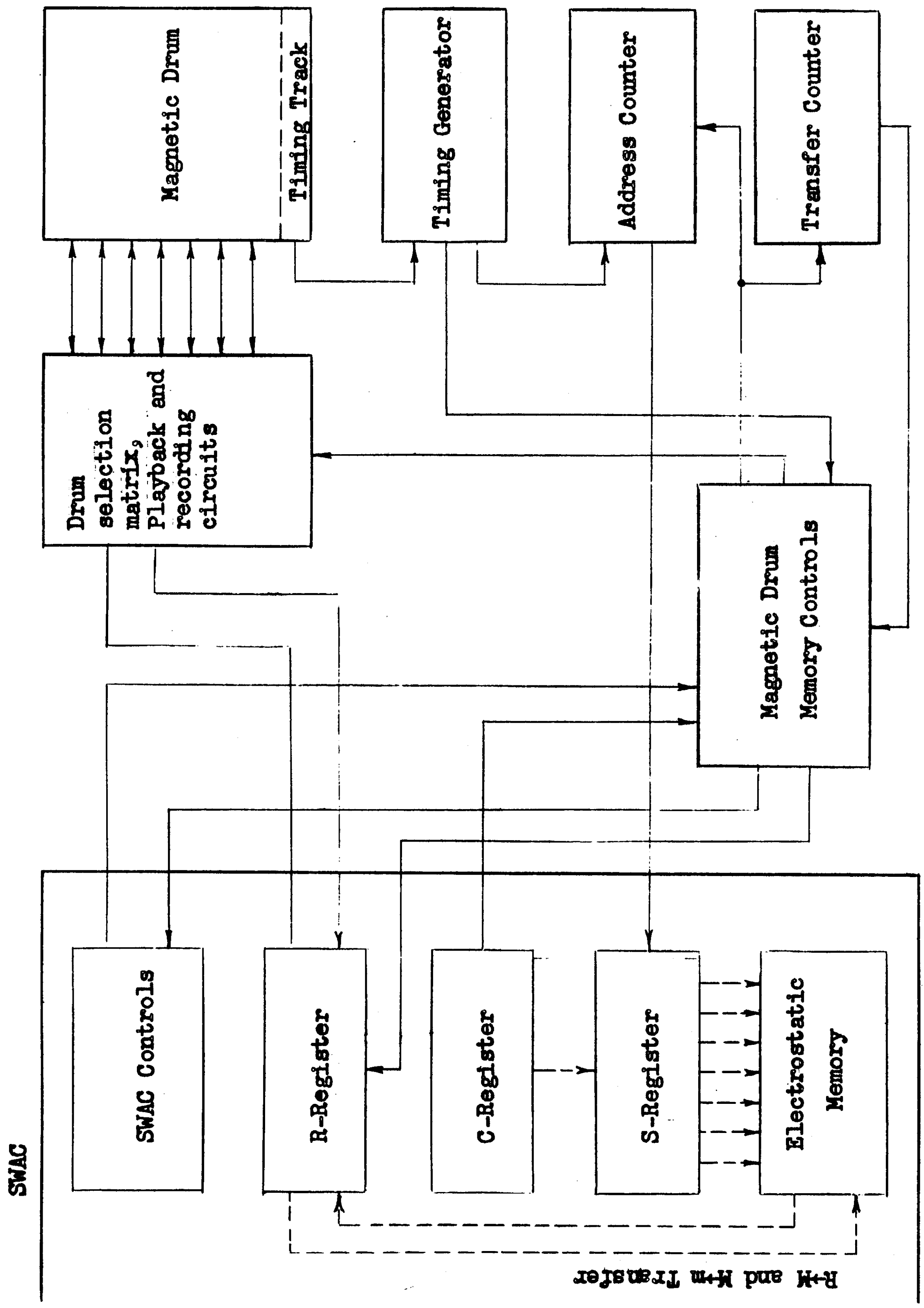


FIGURE 2

1.7 Design Features of Magnetic Drum Memory.

Magnetic Drum Memory Selection System:

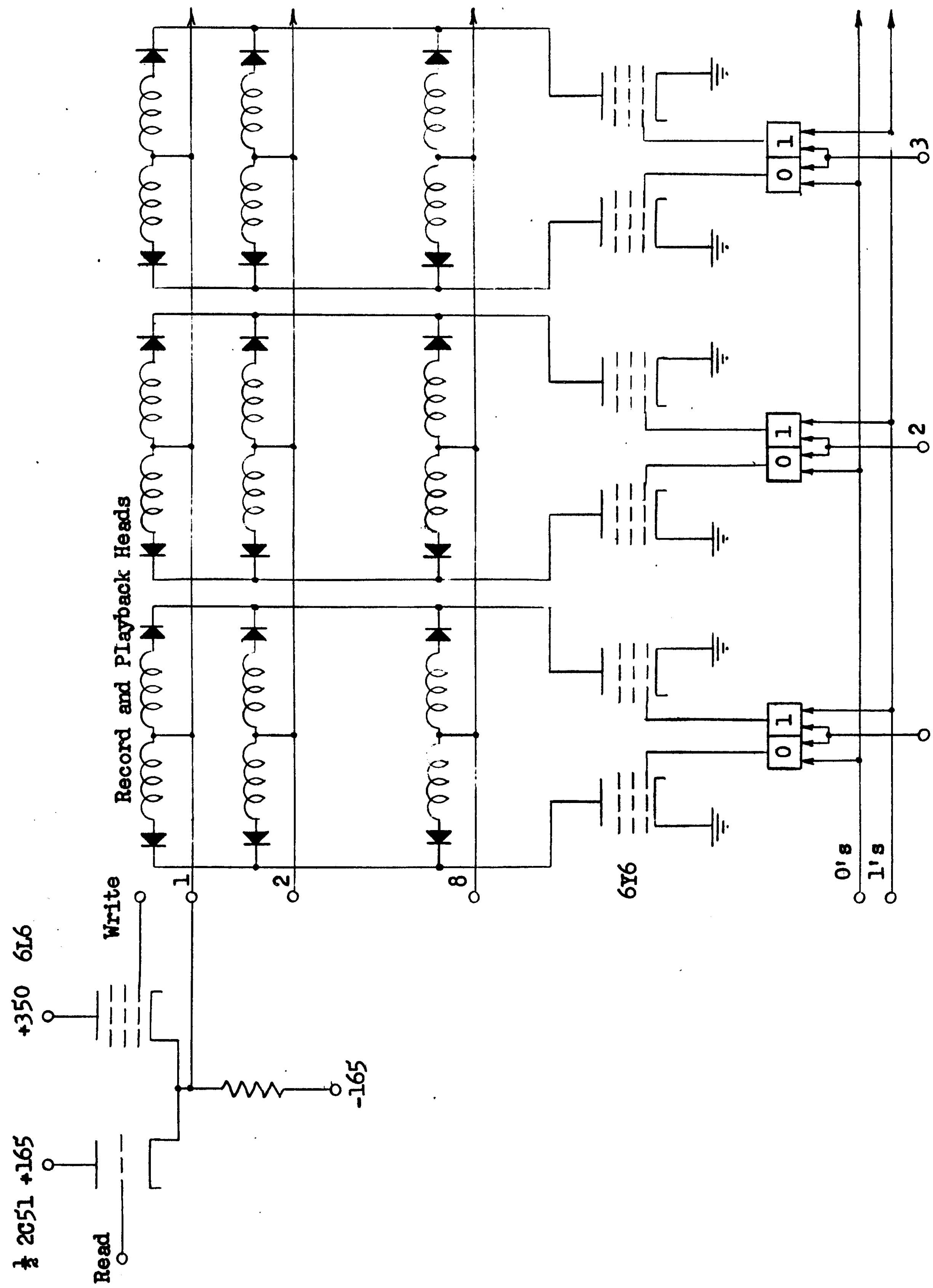


FIGURE 3

2.1 Systematic Preventative Maintenance.

A. General.

The schedule should be such that the entire memory is checked over once every 90 days. Maintenance is important as a well-planned program can go far towards insuring reliable operation.

B. Records.

1. Circuit Changes

In case of an approved circuit change the proper procedure is as follows:

a. Issue (or reissue) the circuit drawing, labelling it experimental and incorporating the changes, for the Engineering Manual.

b. Make change on appropriate CRT units.

c. If change proves satisfactory, correct appropriate drawings according to standard procedure (cf. Section A4.5 this manual).

d. Record data of change in CRT Memory Log Book as each chassis is modified.

2. Maintenance Records

Fill in two cards for each CRT chassis:

a. Top card. Record comments on condition of CRT unit, e.g. whether all right for SWAC, reason for removal from SWAC, etc.

b. Bottom card. Record following information:

1) Date CRT installed and serial number.

2) Read-around ratio as tested on Test Rack.

3) Read-around ratio as obtained in SWAC.

4) Amplifier gain at 100 KC; type of amplifier.

5) Any special circuit changes.

3. CRT Unit Records

a. Daily Engineering Log. Record all information about movement of unit listing any trouble it caused while in SWAC.

b. Daily Component Replacement Log. Record all component replacement such as tubes, resistors, condensors, and crystals.

c. CRT Memory Log. Record information on unit troubles and how fixed.

2.1 Systematic Preventative Maintenance.

C. Cleaning.

1. Remove dust and dirt from insulating surfaces with pure carbon-tetrachloride using small brush. (Be sure bristles from brush are not left on tagboards.)
   Important as high voltage may break down when dirt and moisture accumulate between lugs resulting in arcing.
2. Clean other parts with vacuum or use blower to remove dust and dirt.
3. Clean Jones, Cannon, and banana plugs with Walsco No-Ox Contact Cleaner.
4. Inspect all parts after cleaning as outlined in D.

D. Inspection.

Always combine inspection with cleaning, since in cleaning every point of equipment is exposed, and even more important the very act of cleaning may inadvertently break or loosen a connection. In particular:

1. Carefully examine, and if faulty resolder or fix, all exposed connections such as:
   a. Banana plugs
   b. Jones plugs
   c. Cannon plugs
   d. Tube sockets
   e. Solder joints
   f. Crystal connections
2. Look for evidence of heating or breakdown such as:
   a. Carbonized surfaces
   b. Overheated resistor with charred or discolored surface
   c. Condenser loosing wax.

   Change all such parts and record change even though no serious damage or potential trouble is indicated.

E. Mechanical.

1. Tighten knobs.
2. Tighten screws, replace if missing, or if stripped replace using a larger size.

2.1 Systematic Preventative Maintenance.

F. CRT Unit Voltage.

1. Check weekly on Monday morning and record.

2. Voltage should be within tolerance shown below:

Table 1. CRT Unit Voltage

Note: All voltage measured in Regulator Cabinet unless otherwise specified.

NAME OF VOLTAGE	NOMINAL VOLTAGE with Reference to Gnd. Using GR Meter	RIPPLE MEASUREMENT Using High Gain D.C. Scope
CRT Clamping and Accelerating Potentials (cf. Engineering Manual page B2.4-1)		
2nd Anode and Intensity At Fuse Panel in SWAC	+ 522 ± 1% + 521 ∓ 1%	Should be less than 20 M.V. Should be less than 50 M.V.
Meas. diff. between Gnd. and cathode of CRT	- 1000 ± 1%	Should be less than 400 M.V.
Clamping Voltage	- 252 ± 1%	Should be less than 400 M.V.
Intensity Voltage	- 154 ± 1%	Should be less than 400 M.V.
CRT Gating and Driving Circuitry Voltage (cf. Engr. Man. B2.1)	All of these voltages measured at Fuse Panel in SWAC	
"B" Plate Supply, measurement	+ 172 ± 4%	Should be less than 3 Volts with machine idle.
Negative Voltage for F.F. V9 and ½V8	- 172 ± 4%	Should be less than 1 Volt with machine idle.
Screen Voltage for V10, V7	+ 132 ± 4%	Should be less than 3 Volts with machine idle.
Bias Voltage	- 15.5 ± 4%	Should be less than 1 Volt with machine idle.
CRT Amplifier (cf. Engr. Man. B2.2-1)		
C.F. V5 Plate Voltage	Same as "B" Plate Sup.	Same as "B" Plate Supply
C.F. V5 return of Cathode Follower + Grid	Same as Negative Voltage for F.F.	Same as Neg. Voltage for F.F.
"B" Plate Supply for V1, V2, V3, and V4 At Fuse Panel in SWAC	+ 256 ± 1% + 255 ± 1%	Should be less than 50 M.V. Should be less than 400 M.V.
Filament Voltages		
For All Filaments except CRT	- 6.5 Volts D.C.	Should be less than 250 M.V.
CRT Filament at -1100V	6.3 Volts A.C.	

2.1 Systematic Preventative Maintenance.

G. Testing and Servicing of CRT Unit.

This is divided into following three parts:

1. CRT Amplifier and Cathode-Follower

2. CRT Gating and Driving Circuitry

3. CRT Clamping and Accelerating Potential

Selected test points on each part are marked as circled numbers on pages B2.2-1, B2.4-1, and section B2.1 of the Engineering Manual. Detailed instructions on each part follows:

1. CRT Amplifier and Cathode-Follower Driver

a. Test tubes according to general test procedure, before making voltage measurements in Table 2 on following page.

b. Take measurement at test points (cf. Engineering Manual, page B2.2-1) 1 to 17 which appear on Table 2, with only +250, +165, -165, -15 volts, and filament voltages feeding into CRT unit. (These voltages are supplied by a plug and cable from the CRT Memory Test Rack.)

2.1 Systematic Preventative Maintenance.

Table 2. CRT Amplifier Voltage

Note: Measurements are made with amplifier having 2C51 and 12, 12, 12, and 20K in plate of second triode and .001, .001, and .50 μμfd coupling condensers in between 1st and 2nd, 2nd and 3rd, 3rd and 4th stages.

TEST POINT NOS.	TEST POINTS	VOLTAGE LIMIT	REMARKS
1	2nd plate of V1	+ 125 ± 10%	
2	" " " V2	+ 165 ± 10%	
3	" " " V3	+ 175 ± 10%	
4	" " " V4	+ 175 ± 10%	
5	Feeds V1 and C.F.'s of V2 and V3	+ 172 ± 10%	
6	Feeds BV2 plate	+ 250 ± 10%	
7	Cathode potential V1	+ 15 ± 10%	
8	" " V2	+ 15 ± 10%	
9	" " V3	+ 15 ± 10%	
10	" " V4	+ 15 ± 10%	
11	Grid potential of V1	- 13 ± 10%	
12	Grid potential of V2, V3 and V4	- 13 ± 10%	
13	Output of C.F. V5	- 22 ± 10%	
14	Grid of C.F. V5	- 28 ± 10%	
15	Plate of C.F. V5	+ 172 ± 4%	
16	C.F. V5 return	- 172 ± 4%	
17	Plate supply voltage	+ 255 ± 1%	

2.1 Systematic Preventative Maintenance.

c. If voltages are within proper tolerance, the next step is to take gain measurements of amplifier including V5 cathode-follower (cf. Table 3, page D2.1-7). The gain measurements should be made as follows:

1) H.P. oscillator with 6 ohm, 100 to 1, output pad is used to supply a 1.0 millivolt r.m.s. signal to amplifier. This is a.c. coupled with a 0.01 μfd condenser, and is fed into input of amplifier's first stage, well shielded.

2) The D.C. Scope Tektronix Type 512 is used to measure peak-to-peak, or a H.P. vacuum tube voltmeter can be used to measure both input and output r.m.s. voltages. (See Figure 1 below.)

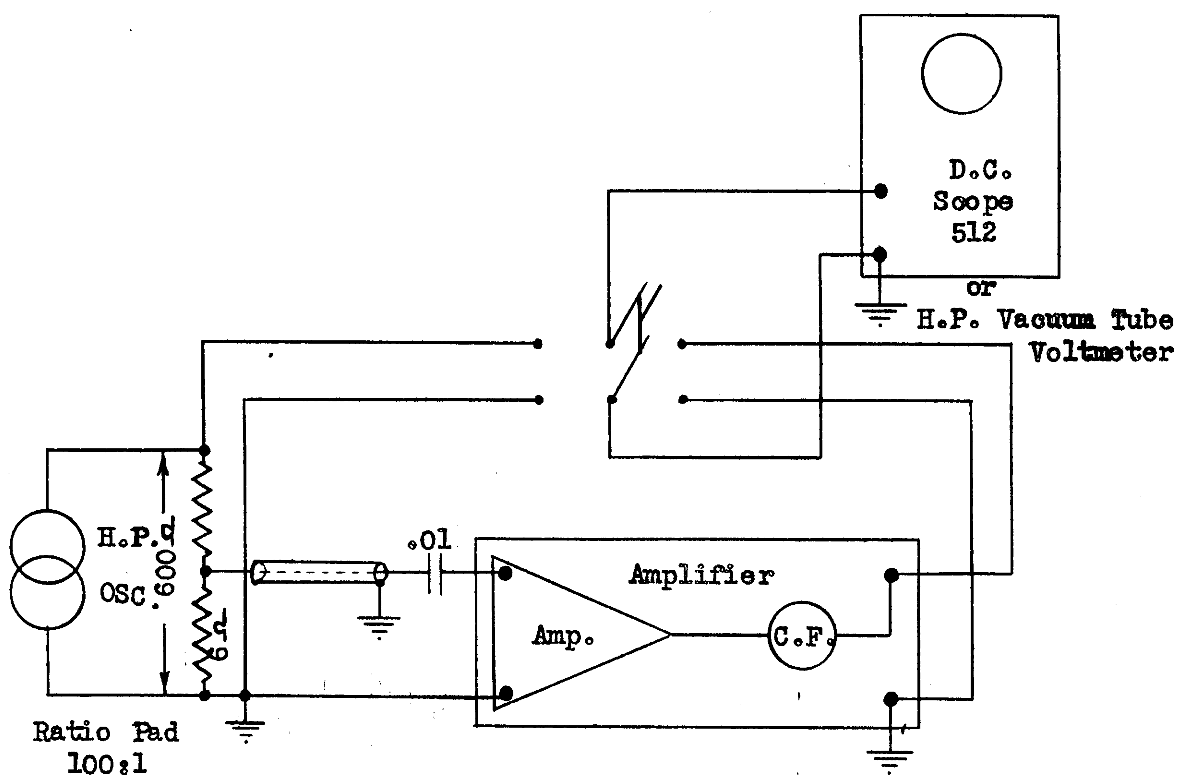


Figure 1.

2.1 Systematic Preventative Maintenance.

Table 3. Gain Measurements of CRT Amplifier

FREQUENCY CHECK POINTS	INPUT	OUTPUT VOLTS	GAIN (Min.)
5 KC	1.0 M.V., r.m.s.	5.0	5,000
10 KC	"	15.0	15,000
100 KC	"	32.0	32,000
500 KC	"	22.0	22,000
1000 KC	"	12.0	12,000

3) The gains given in the preceding Table 3 are the minimum gains that an amplifier should have.

4) Amplifiers should be checked for noise and 60 cycle ripple by turning off H.P. oscillator, or by grounding the first grid of V1, which is the input to the amplifier. With the D.C. Scope 512 across the output of V5 (cathode-follower), and maximum gain in scope, the noise + 60 cycle ripple should be less than 30 millivolts.

This completes the checking of the CRT Amplifier and Cathode-Follower output.