Superram™

16k-A

USER'S MANUAL

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Thinker Toys™

SuperRam™ 16K-A

INTRODUCTION

The SuperRam 16K-A utilizes the MM5257/4044 4096 x 1 static memory I.C. As with other memories from Thinker Toys, all data and address lines are fully buffered for enhanced data integrity. The board is designed to give the user maximum flexibility by splitting the memory into four independent 4K blocks which can be separately write protected. Each 4K block may be independently addressed at any 4K boundary in memory.

The $\overline{\text{PHANTOM}}$ line can be conditionally enabled to turn off the board during power-up procedures. The board uses DIP switches located at the top of the board so that address selection is easy to accomplish. Finally, SIP (single-in-line package) resistor networks have been utilized throughout the board to keep the parts count down. A lower parts count means higher reliability and quicker assembly for the end user.

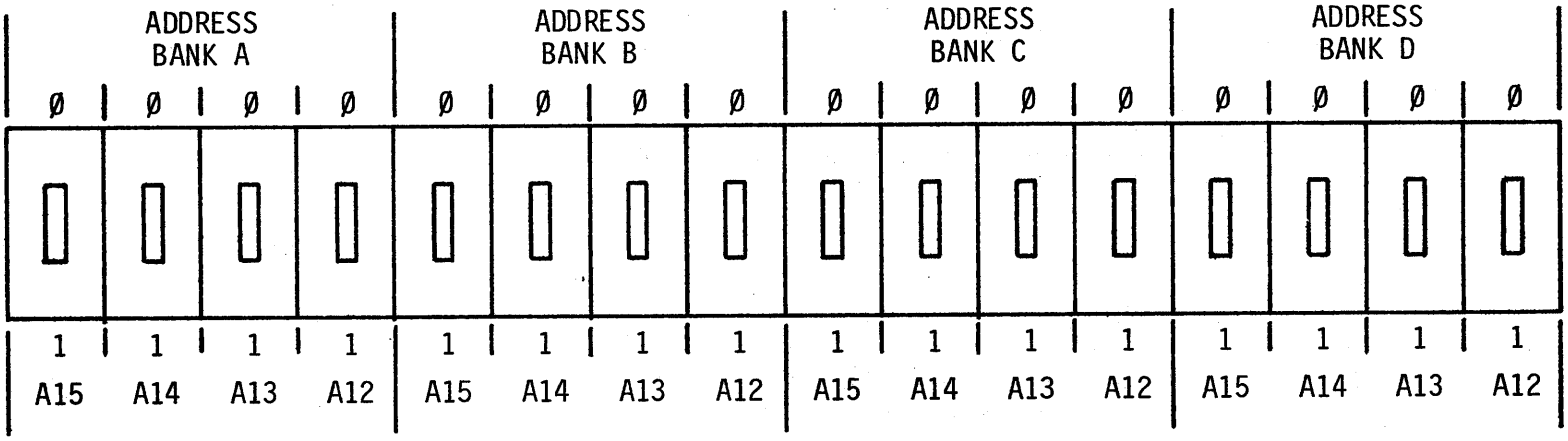
We at Thinker Toys have tried to make this manual clear and accurate. Comments on improving this document are welcome. Thank you for purchasing the SuperRam 16K-A memory. We hope it will serve your needs.

OPERATING INSTRUCTIONS

> NOTE: TURN OFF THE POWER IN YOUR COMPUTER BEFORE PLUGGING IN OR REMOVING THE SUPERRAM! YOU MAY DAMAGE ONE OR MORE OF THE RESIDENT CIRCUIT BOARDS IF YOU DO NOT FOLLOW THIS PROCEDURE.

ADDRESSING

At the top of the circuit board, there are three eight-position DIP switches. The left two determine the addressing of the memory. The DIP switch on the right is for write protection and PHANTOM enabling. The two switches on the left are illustrated below:



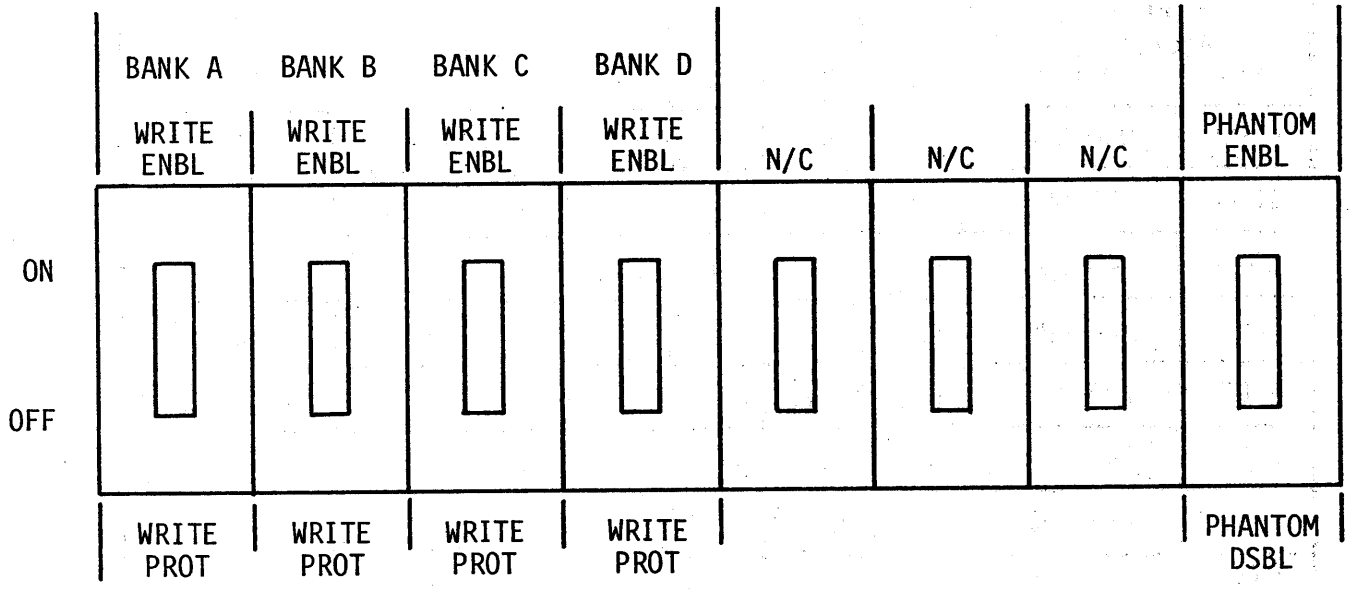
In the 64K bytes of address space of the S-100 bus, there are sixteen 4K blocks. The positions of the four switches associated with blocks A, B, C and D as illustrated above determines which 4K segment of address space a particular block will occupy. For example, if the switches associated with block A are all ON (up), block A will occupy locations 000:000 through 17:377 octal or 0000 through 0FFF hex. If the switches associated with block B are ON (15 through 13) and OFF (12), block B will occupy memory locations 20:000 through 37:377 octal or 1000 through 1FFF hex.

Note that in the illustration above there is an address bit above each switch. Block positions are formed by making a hex digit pattern with each group of four switches. The high order bit of this hex digit is to the left as is the high order address bit. These hex digits represent the starting address of the block associated with the switches (when followed by three hex zeros). Following is a table of switch positions and corresponding starting addresses

Starting Address Hex	Starting Address Octal	A 15	A 14	A 13	A 12	Corresponding Hex Digit	Corresponding Binary Number
0000	000:000	up	up	up	up	0	0000
1000	020:000	up	up	up	down	1	0001
2000	040:000	up	up	down	up	2	0010
3000	060:000	up	up	down	down	3	0011
4000	100:000	up	down	up	up	4	0100
5000	120:000	up	down	up	down	5	0101
6000	140:000	up	down	down	up	6	0110
7000	160:000	up	down	down	down	7	0111
8000	200:000	down	up	up	up	8	1000
9000	220:000	down	up	up	down	9	1001
A000	240:000	down	up	down	up	A	1010
B000	260:000	down	up	down	down	B	1011
C000	300:000	down	down	up	up	C	1100
D000	320:000	down	down	up	down	D	1101
E000	340:000	down	down	down	up	E	1110
F000	360:000	down	down	down	down	F	1111

Note: up = on; down = off.

WRITE PROTECTION LOGIC



The left most four switches of the DIP switch on the far right (DIP switch array #3) are devoted to write protection for the four blocks A, B, C and D. If the switch associated with a particular block is OFF (down), that block of memory is write protected. For example, if the left most switch above is OFF, it is impossible for the CPU, i.e., the 8080 processor, to alter any of the 4096 memory locations spanned by block A. The switches have been arranged in the same order as the address selection switches (A to the left, D to the right) to help minimize errors when these switches are manipulated.

PHANTOM ENABLE

The right most switch of DIP switch #3 is used to enable or disable the $\overline{\text{PHANTOM}}$ line on the S-100 bus (pin #67). The $\overline{\text{PHANTOM}}$ signal is used to disable normal memory during power-up situations or other emergencies. Typically, special purpose ROM is enabled on the bus during the time the $\overline{\text{PHANTOM}}$ signal is active and so normal memory is disabled. If your mainframe has logic which utilizes the PHANTOM line as described above, the PHANTOM switch should be up (ON). If the $\overline{\text{PHANTOM}}$ line is not used in your system or used for some other purpose, the switch should be down (OFF).

MEMORY DIAGNOSTIC

The memory test described below was designed by Phil Meads of William Brobeck Associates to exercise the most sensitive circuitry of the memory chips -- the address buffers. The test starts from the middle and works its way outward alternately to the top and bottom of memory. This type of test inverts the address lines more often than sequential ones. This continual inversion process punishes and eventually breaks down weak or faulty address buffers in the device.

USING THE TEST

The test itself must be placed in an area which is different than the location of the board(s) to be tested. The test starts on a page boundary to make the task of relocating the binary code easier.

There are two parameters in the test to be set by the user:

(1) The number of 4K blocks to be tested -- keep in mind that there are four 4K blocks per board. This constant is called BLKCNT and is located at the eleventh byte of the test.

(2) The starting page number of the lowest 4K block to be tested is called PAGENO and is located at the ninth byte of the test.

When testing more than one 4K block of memory, be sure that they occupy contiguous memory.

The page number of the position of the test itself must be entered wherever a $(YYY)_8$ or $(YY)_{16}$ occurs in the test listing. This is necessary because JMP and CALL need both the page number and the location within the page to execute correctly.

The only other thing to remember when loading the test is that it must be placed at the starting address of a page.

Start the test at the first instruction. Once started, the test will run continuously unless an error is detected. If the test encounters an error, all the data pertinent to this error is stored in the last ten locations of the test. After storing this data, the test comes to a dynamic halt at the label STALL. The test may be restarted by stopping the computer and restarting it at the POP PSW instruction following JMP STALL. The user may also restart the test from the beginning. If errors indicate the board is malfunctioning, return it as soon as possible for service.

MEMORY TEST PROGRAM FOR 4K NMOS RAMS

Octal

```
YYY  000 061 175 YYY     START  LXI   SP,STACK   INITIALIZE STACK POINTER
     003 001 000 000            LXI   B,0        INITIALIZE CYCLE COUNT
     006 305            NEWCYL  PUSH  B          UPDATE CYCLE COUNT
     007 006 100                MVI   B,PAGENO   STARTING ADDR OF TEST MEM
     011 016 004                MVI   C,BLKCNT   # OF 4K BLOCKS TO TEST
     013 041 377 007    LOOP    LXI   H,7:377Q   HALF SIZE OF MEMORY -1
     016 170                    MOV   A,B
     017 204                    ADD   H          CALCULATE MIDDLE
     020 147                    MOV   H,A          OF CURRENT BLOCK
     021 345                    PUSH  H          SAVE INITIAL ADDRESS
     022 315 114 YYY    WRITE   CALL  TWORD      GET TEST WORD
     025 167                    MOV   M,A        STORE
     026 315 123 YYY            CALL  COMP       COMPLEMENT ADDRESS
     031 315 114 YYY            CALL  TWORD      GET TEST WORD
     034 167                    MOV   M,A        STORE
     035 315 134 YYY            CALL  INCR       COMPLEMENT & DECREMENT
     040 302 022 YYY            JNZ   WRITE        ADDRESS
     043 341                    POP   H          RECOVER INITIAL ADDRESS

YYY  044 315 114 YYY    READ    CALL  TWORD      GET TEST WORD
     047 256                    XRA   M          COMPARE
     050 304 145 YYY            CNZ   ERROR
     053 315 123 YYY            CALL  COMP       COMPLEMENT ADDRESS
     056 315 114 YYY            CALL  TWORD      GET TEST WORD
     061 256                    XRA   M          COMPARE
     062 304 145 YYY            CNZ   ERROR
     065 315 134 YYY            CALL  INCR       COMPLEMENT & DECREMENT
     070 302 044 YYY            JNZ   READ         ADDRESS

YYY  073 076 020                MVI   A,20Q     ADVANCE
     075 200                    ADD   B            THE
     076 107                    MOV   B,A          BLOCK
     077 015                    DCR   C          DECREMENT BLOCK COUNT
     100 302 013 YYY            JNZ   LOOP
     103 173                    MOV   A,E        CALCULATE NEW
     104 306 207                ADI   135          BASE FOR
     106 137                    MOV   E,A          TEST WORD
     107 301                    POP   B
     110 003                    INX   B          INCREMENT CYCLE COUNT
     111 303 006 YYY            JMP   NEWCYL

     114 175            TWORD   MOV   A,L        GET LOWER BYTE OF ADDRESS
     115 007                    RLC              ROTATE
     116 207                    ADD   A          SHIFT
     117 204                    ADD   H          ADD HIGHER BYTE OF ADDR
     120 203                    ADD   E          ADD BASE
     121 127                    MOV   D,A        SAVE TEST WORD
     122 311                    RET
```

```
YYY  123 174           COMP   MOV   A,H      COMPLEMENT THE UPPER
     124 356 017              XRI   17Q        BYTE ADDRESS
     126 147                  MOV   H,A        WITH RESPECT TO MEM SIZE
     127 175                  MOV   A,L      COMPLEMENT THE LOWER
     130 356 377              XRI   377Q       BYTE OF THE
     132 157                  MOV   L,A        ADDRESS
     133 311                  RET

YYY  134 315 123 YYY  INCR   CALL  COMP     RESTORE ADDR TO NORMAL SIZE
     137 053                  DCX   H        DECREMENT
     140 300                  RNZ            TEST IF LOWER BYTE ZERO
     141 170                  MOV   A,B      TEST UPPER BYTE EQUAL
     142 075                  DCR   A          TO BLOCK
     143 274                  CMP   H          BOUNDARY
     144 311                  RET

YYY  145 345           ERROR  PUSH  H        SAVE ERROR ADDRESS
     146 305                  PUSH  B        SAVE CURRENT BLOCK
     147 325                  PUSH  D        SAVE TEST WORD
     150 365                  PUSH  PSW      SAVE ERROR BITS
     151 303 151 YYY  STALL  JMP   STALL    DYNAMIC HALT
     154 361                  POP   PSW      RESTORE
     155 321                  POP   D          THE
     156 301                  POP   B          STATE OF
     157 341                  POP   H          THE CPU
     160 311                  RET

YYY  161 000           TABLE  DB    0        FLAGS
     162 000                  DB    0        ACC - ONES ARE ERROR BITS
     163 000                  DB    0        E - CURRENT RANDOM OFFSET
     164 000                  DB    0        D - CURRENT TEST WORD
     165 000                  DB    0        C - CURRENT BLOCK COUNT
     166 000                  DB    0        B - CURRENT BLOCK PAGE
     167 000 000              DW    0        HL - ERROR ADDRESS
     171 000 000              DW    0        RETURN ADDRESS
     173 000 000              DW    0        CYCLE COUNT
     175 000 000       STACK  DW    0
```

MEMORY TEST PROGRAM FOR 4K NMOS RAMS

Hex

```
YY  00    31 7D YY      START  LXI   SP,STACK
    03    01 00 00             LXI   B,0
    06    C5           NEWCYL  PUSH  B
    07    06 40                MVI   B,PAGENO
    09    0E 04                MVI   C,BLKCNT
    0B    21 FF 07     LOOP    LXI   H,7:377Q
    0E    78                   MOV   A,B
    0F    84                   ADD   H
    10    67                   MOV   H,A
    11    E5                   PUSH  H
    12    CD 4C YY     WRITE   CALL  TWORD
    15    77                   MOV   M,A
    16    CD 53 YY             CALL  COMP
    19    CD 4C YY             CALL  TWORD
    1C    77                   MOV   M,A
    1D    CD 5C YY             CALL  INCR
    20    C2 12 YY             JNZ   WRITE
    23    E1                   POP   H

YY  24    CD 4C YY     READ    CALL  TWORD
    27    AE                   XRA   M
    28    C4 65 YY             CNZ   ERROR
    2B    CD 53 YY             CALL  COMP
    2E    CD 4C YY             CALL  TWORD
    31    AE                   XRA   M
    32    C4 65 YY             CNZ   ERROR
    35    CD 5C YY             CALL  INCR
    38    C2 24 YY             JNZ   READ

YY  3B    3E 10                MVI   A,20Q
    3D    80                   ADD   B
    3E    47                   MOV   B,A
    3F    0D                   DCR   C
    40    C2 0B YY             JNZ   LOOP
    43    7B                   MOV   A,E
    44    C6 87                ADI   135
    46    5F                   MOV   E,A
    47    C1                   POP   B
    48    03                   INX   B
    49    C3 06 YY             JMP   NEWCYL

YY  4C    7D           TWORD   MOV   A,L
    4D    07                   RLC
    4E    87                   ADD   A
    4F    84                   ADD   H
    50    83                   ADD   E
    51    57                   MOV   D,A
    52    C9                   RET
```

```
YY  53   7C          COMP   MOV    A,H
    54   EE OF              XRI    17Q
    56   67                 MOV    H,A
    57   7D                 MOV    A,L
    58   EE FF              XRI    377Q
    5A   6F                 MOV    L,A
    5B   C9                 RET

YY  5C   CD 53 YY    INCR   CALL   COMP
    5F   2B                 DCX    H
    60   C0                 RNZ
    61   78                 MOV    A,B
    62   3D                 DCR    A
    63   BC                 CMP    H
    64   C9                 RET

YY  65   E5          ERROR  PUSH   H
    66   C5                 PUSH   B
    67   D5                 PUSH   D
    68   F5                 PUSH   PSW
    69   C3 69 YY    STALL  JMP    STALL
    6C   F1                 POP    PSW
    6D   D1                 POP    D
    6E   C1                 POP    B
    6F   E1                 POP    H
    70   C9                 RET

YY  71   00          TABLE  DB     0        FLAGS
    72   00                 DB     0        ACC - ONES ARE ERROR BITS
    73   00                 DB     0        E - CURRENT RANDOM OFFSET
    74   00                 DB     0        D - CURRENT TEST WORD
    75   00                 DB     0        C - BLOCKS LEFT TO TEST
    76   00                 DB     0        B - CURRENT BLOCK PAGE
    77   00 00              DW     0        HL - ERROR ADDRESS
    79   00 00              DW     0        RETURN ADDRESS
    7B   00 00              DW     0        CYCLE COUNT
    7D   00 00          STACK  DW     0
```

PARTS LIST

O	1	8" x 10" photo
O	1	5" x 10" printed circuit board
O	3	SIP resistor packs
O	21	by-pass capacitors*
O	5	39 µfd tantalum capacitors
O	10	14-pin low profile sockets
O	3	16-pin low profile sockets
O	32	18-pin low profile sockets
O	3	8-position DIP switches
O	4	heat sinks
O	4	6-32 x 5/16 machine screws
O	4	6-32 hex nuts
O	1	74LS00/74LS132 quad 2 input NAND gate
O	2	74LS04/74LS14 hex inverters
O	1	74LS20 dual 4 input NAND gate
O	1	74LS02 quad 2-input NOR gate
O	1	74LS32 quad 2 input OR gate
O	4	74LS266 quad EXCLUSIVE NOR gates
O	3	74LS367/74LS368 hex tristate** buffer
O	32	MM5257/4044 4096 x 1 static RAMS
O	4	7805/LM340.5 5 volt regulators

*by-pass capacitors will vary in value between .01 µfd and .1 µfd.

**tristate is a trademark of National Semiconductor.

ASSEMBLY INSTRUCTIONS

DO NOT INSTALL OR SOLDER ANY PARTS UNTIL YOU HAVE READ THE INSTRUCTIONS AND UNDERSTAND THEM!

CAUTION -- DO NOT SOLDER OR CLIP COMPONENT LEADS WITHOUT USING SAFETY GLASSES!

INSPECTION

Use the Parts List to make sure that there are no missing items in your kit. Please notify us of any shortages. Be sure to check for missing parts before you start assembling.

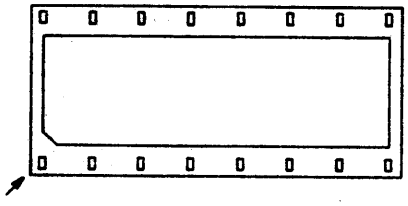
SOCKETS

A socket is furnished for every integrated circuit. It is important that you use the sockets; otherwise, a defective part will be extremely difficult to replace.

NO REPAIR OR SERVICE WILL BE PERFORMED ON A CIRCUIT BOARD WHICH HAS HAD INTEGRATED CIRCUITS SOLDERED TO IT.

PARTS ORIENTATION

In all references throughout the instructions, the convention used is that the gold edge connector is the bottom of the board. Orientation identification is molded into the plastic of the sockets either with numbers or in the manner illustrated below.



This orientation or an embossed "1" identifies where pin #1 of the integrated circuit is to be positioned when inserted into the socket. The sockets should be inserted in the board so that the orientation mark is in the lower left hand corner.

The tantalum capacitors should be oriented so that the red strip or positive mark is to the left when the part is inserted in the board. The three DIP switches at the top of the board should be positioned so that switch #1 is to the left.

The SIP resistor packs have an orientation dot at one end. The pin associated with this dot is the common point of the nine resistors in this package and must be to the left when the parts are soldered to the board.

SOLDERING AND SOLDER IRONS

The most desirable soldering iron for complex electronic kits is a constant temperature soldering iron with an element regulated at 650° F. The tip should be fine so that it can be brought in intimate contact with the pads of the circuit board. Both Unger and Weller have excellent products which fit the above requirements.

There are three important soldering requirements for building this kit:

1. Do not use an iron that is too cold (less than 600° F) or too hot (more than 750°).

2. Do not apply the iron to a pad for extended periods.

3. Do not apply excessive amounts of solder.

The proper procedure for soldering components to the circuit board is as follows:

1. Bring the iron in contact with both the component lead and the pad.

2. Apply a small amount of solder at the point where the iron, component lead, and pad all make contact.

3. After the initial application of solder has been accomplished with the solder flowing to the pad and component lead, the heat of the iron will have transferred to both the pad and the lead. Apply a small amount of additional solder to cover the joint between the pad and the lead. DO NOT PILE SOLDER ON THE JOINT! EXCESSIVE HEAT AND SOLDER CAUSE PADS AND LEADS TO LIFT FROM THE CIRCUIT BOARD. EXCESSIVE SOLDER IS THE PRIMARY CAUSE FOR BOARD SHORTS AND BRIDGED CONNECTIONS.

PARTS INSTALLATION

Install:

- ☐ Sockets 1A-8A, 1B-8B, 1C-8C, 1D-8D. 18-pin low profile. Pin #1 to the lower left.
- ☐ Sockets 1E-5E, 1F-5F. 14-pin low profile. Pin #1 to the lower left.
- ☐ Sockets 6E-8E. 16-pin low profile. Pin #1 to the lower left.
- ☐ C1-C5 39 µfd tantalum capacitors. Orientation mark to the left. Bend leads .6" wide before insertion.
- ☐ SIP resistor packs. RN1, RN2, and RN3. Orientation dot to the left.
- ☐ By-pass capacitors (21 each) as shown by the silk screen legend on the circuit board.
- ☐ DIP switches 1, 2 and 3. Switch #1 of each switch array should be to the left when inserted.
- ☐ 7805/LM340.5 5 volt regulators (4 each) by bending the leads, inserting and hand tightening the nut and bolt through the circuit board, heat sink and regulator, in that order. Solder the leads. If heat sink grease is available, apply a <u>thin</u> film between the board and heat sink and between the heat sink and the regulator before inserting the parts and soldering the leads. Finally, tighten the nut firmly.

For parts placement, please see the silk screen legend on the printed circuit board and the 8" x 10" photograph.

POWER SUPPLY/VOLTAGE REGULATOR CHECK OUT

Voltage requirements: (reference to ground - pins 50 and 100)

Pins 1 and 51: not less than 7 volts approx. 1700 ma
not more than 10 volts

Before installing any of the integrated circuits, apply power to pins 1 and 51 as specified above. Power can come from external supplies or from a host S-100 mainframe. After applying power, perform the following measurements:

(1)	1F pin 14	+ 5 volts
(2)	2F pin 14	+ 5 volts
(3)	3F pin 14	+ 5 volts
(4)	4F pin 14	+ 5 volts
(5)	5F pin 14	+ 5 volts
(6)	6E pin 16	+ 5 volts
(7)	7E pin 16	+ 5 volts
(8)	8E pin 16	+ 5 volts

If the voltage at any of the check points differs by more than 5% if the required value, return the board for service.

POWER-UP CHECK OUT

Install the integrated circuits. Be very careful not to bend pins of the ICs under the package. Frequently, a pin which is bent under appears to be inserted in the socket.

BENT PINS ARE THE MOST COMMON REASON FOR A MALFUNCTIONING BOARD!

After the parts have been installed, repeat the eight voltage measurements specified above. If the test points differ from the required values, return the board for service. UNDER NO CIRCUMSTANCES SHOULD THE SOCKETS BE REMOVED FROM THE BOARD. Such abuse will void the warranty under which repair and service is performed.

SYSTEM CHECK OUT

Select four different bank positions for the four blocks of memory on the board. Make sure that the write protect/enable switches are all on. Select the position of the PHANTOM switch that is appropriate for your system. Next with power OFF, plug the board into an empty slot of main frame and apply power. Examine several locations in each of the four different blocks and verify that all zeros and all ones can be written into and read from each of the four blocks.

Finally, a memory test (either the one included in this manual or one of your choosing) should be run for several hours over the entire 16K. After completion of these steps, the memory is ready for use in your mainframe.

THEORY OF OPERATION

ADDRESS SELECT LOGIC

The SuperRam 16K-A is configured as four 4K blocks of memory. The board has circuitry which allows each of these four blocks to be independently addressed. Each block uses a 74LS266 open collector quad exclusive-NOR pack and four switches of an eight position DIP switch to select one of sixteen possible 4K boundaries at which the block is to be located.

One input of each of the four gates is connected to address lines A15, A14, A13 and A12, respectively. The other input is connected to an address select switch and pull-up resistor. If the switch is open, the pull-up resistor forces a logic "1" to the input. The output transistor will then be in the OFF state if and only if the corresponding address line connected to the other input is also a logic "1". If the switch is closed, the input will be grounded (logic "0"). In this case, the output transistor will be in the OFF state if and only if the corresponding address line connected to the other input is also a logic "0". The four outputs of these exclusive-NOR gates are connected together along with a pull-up resistor.

If all four of the output transistors are in the OFF state, the common output node will be pulled up to +5 volts through the resistor and will be at a logic "1". This common output node will be at a logic "1" when the logic level on each address line A15-A12 independently matches the logic level determined by the switch associated with the address line. If there are any mismatches, one or more of the output transistors of the exclusive-NOR gates will be ON (i.e., conducting to ground) and the common output node of the four gates will be at a logic "0". There are four of these common output nodes. They are labeled SELECT A, SELECT B, SELECT C and SELECT D. When one of these select lines is high, the 4K block of memory associated with this line will be selected if the status signals $\overline{\text{SWO}}$, SOUT, SMEMR and (conditionally) $\overline{\text{PHANTOM}}$ are at the appropriate levels to signal a memory reference.

BOARD SELECTION LOGIC

In order to reference one of the four 4K blocks on the board, one or more of the select signals discussed above must be at a logic "1". But this is not enough. The only bus cycle which the board will respond to are memory references.

$\overline{\text{SWO}}$ is a status signal which is active (logic "0") during bus cycles which transfer data from the CPU to a bus slave (memory, I/O, etc.). SOUT is active (logic "1") when the CPU is transferring data to an I/O device. Thus the CPU is writing into memory when SOUT and $\overline{\text{SWO}}$ are both in a logic "0" state. When the CPU is reading memory SMEMR is active (logic "1").

$\overline{\text{PHANTOM}}$ is active (logic "0") when phantom ROM or other exceptional memory must usurp the bus and lock out normal to furnish the CPU with special instructions. This is most common during power-up when the CPU's program counter is forced to zero.

We shall define memory write cycle to be a bus cycle during which $\overline{\text{PHANTOM}}$ is a logic "1" and SMEMR is a logic "1". The SuperRam 16K-A board is selected whenever a memory read or a memory write is in progress and at least one of the select lines SELECT A, SELECT B, SELECT C, or SELECT D is at a logic "1" level. During memory reads or writes, SELECT A activates $\overline{\text{BANK A}}$, SELECT B activates $\overline{\text{BANK B}}$, etc.

DATA TRANSFER LOGIC

PDBIN is the data input strobe signals. The CPU drives this line high during the period of a bus cycle when an addressed peripheral is to place its data on the input lines. On the 16K-A board, the PDBIN signal turns on the tri-state** buffers to the CPU's input lines whenever one of the banks on the board is selected. This logic is implemented with a pair of 4-input NAND gates at position 1E of the circuit board and appears at the upper left hand corner of page 2 of the schematics.

Both $\overline{\text{PWR}}$ and MWRITE are strobe signals active when the CPU transfers data to a peripheral device. $\overline{\text{PWR}}$ is the logic "0" strobe for both memory and I/O writes while MWRITE is the logic "1" strobe for memory writes only. However, not all CPUs generate the MWRITE signal. On both the original ALTAIR and IMSAI machines, the MWRITE signal is generated by the front panel.

The only time information can be written into the MM5257/4044 memory chips when both the chip select ($\overline{\text{CS}}$) and the write enable ($\overline{\text{WE}}$) inputs are at a logic "0" level. The $\overline{\text{CS}}$ inputs are connected to the BANK A, BANK B, BANK C or BANK D signals on page 1 of the schematics and is low only when the proper block of memory on the board is selected. The $\overline{\text{WE}}$ inputs are connected to the $\overline{\text{WRITE A}}$, $\overline{\text{WRITE B}}$, $\overline{\text{WRITE C}}$, or $\overline{\text{WRITE D}}$ signals also on page 1 of the schematics. These signals are low whenever either of the data output strobes is active and the write enable switch corresponding to the proper block of memory is closed. Thus, memory must be write enabled and selected before it can be written into.

Morrow Designs, Inc.

Thinker Toys™ 5221 Central Avenue, Richmond, CA 94804 (415) 524-2101

LIMITED WARRANTY

Morrow Designs Inc. warrants its products to be free from defects in workmanship and material for the period indicated. This warranty is limited to the repair or replacement of parts only and liability is limited to the purchase price of the product. The warranty is void if, in the sole opinion of Morrow Designs Inc., the product has been subject to abuse, misuse, unauthorized modification, improper assembly, non-conformance to assembly directions, or if the unit is used in any other manner than intended.

KITS - Parts, including the printed circuit boards, purchased in kit form are warranted for a period of ninety (90) days from the invoice/purchase date. If a board, which was purchased in kit form, is returned for testing or repair, a minimum service charge of $35. will be assessed.

ASSEMBLED BOARDS - Parts, including the printed circuit boards, purchased as factory assebmlies, are warranted for a period of six (6) months from the invoice/purchase date. Out-of-Warranty boards returned for testing of repair will be assessed a minimum of $35. service charge. If the charge to repair will exceed $35., the customer will be notified prior to the actual repair.

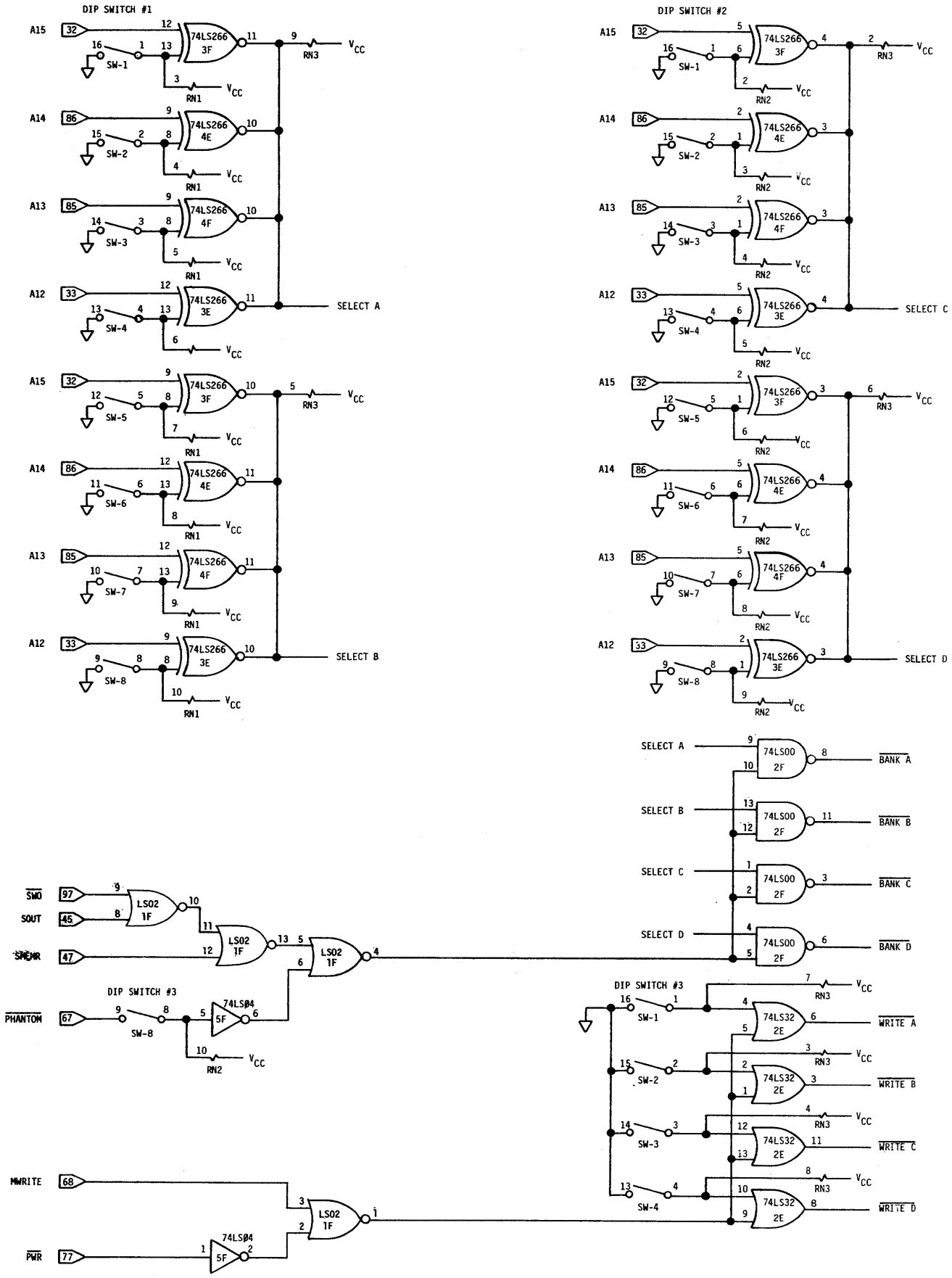
ELECTROMECHANICAL PERIPHERALS - Peripheral equipment, such as floppy disk drives, hard disk drives, etc., not manufactured by Morrow Designs Inc. have warranties which vary according to the manufacturer. In most cases, Morrow Designs Inc. provides a warranty equal to or greater than the original manufacturer. Please contact the factory for individual warranty information. Warranty information for each device is included with the equipment when it is shipped.

RETURN PROCEDURE - A COPY OF THE INVOICE OR PROOF OF ORIGINAL PURCHASE IS REQUIRED AND MUST ACCOMPANY THE ITEM FOR IN-WARRANTY SERVICE. Items returned without proof of original purchase will be sent back, shipping charges collect. A description of the problem must accompany the returned item. Shipment must be made prepaid to Morrow Designs, Inc. Repaired items will be shipped via U.P.S. surface. Shipment by air requires payment of the additional charges. Morrow Designs Inc. is not responsible for any consequential damages of for damage incurred in transit.

The foregoing warranty is in lieu of all other warranties either expressed or implied and, in any event, is limited to product repair or replacement.

Effective February 1, 1980

Specifications, terms, and pricing are subject to change without notice.



SUPERRAM 16K-A STATIC S-100 MEMORY

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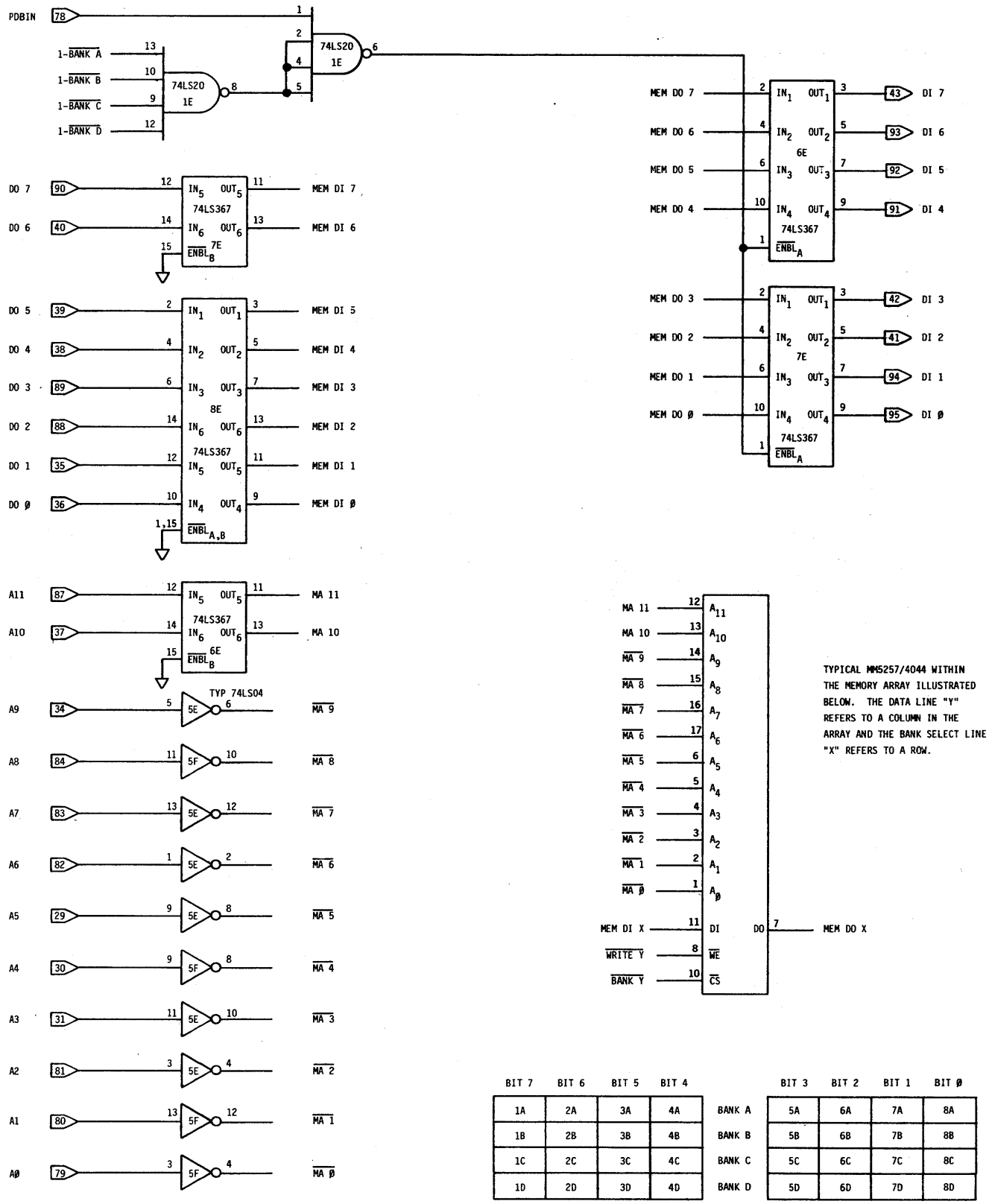
BANK SELECT & WRITE ENABLE LOGIC



TYPICAL MM5257/4044 WITHIN THE MEMORY ARRAY ILLUSTRATED BELOW. THE DATA LINE "Y" REFERS TO A COLUMN IN THE ARRAY AND THE BANK SELECT LINE "X" REFERS TO A ROW.

	BIT 7	BIT 6	BIT 5	BIT 4		BIT 3	BIT 2	BIT 1	BIT Ø
BANK A	1A	2A	3A	4A		5A	6A	7A	8A
BANK B	1B	2B	3B	4B		5B	6B	7B	8B
BANK C	1C	2C	3C	4C		5C	6C	7C	8C
BANK D	1D	2D	3D	4D		5D	6D	7D	8D