

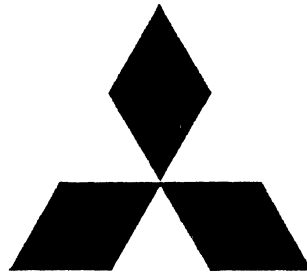
# **VLSI MOS MEMORY RAM/ROM & MEMORY CARDS**

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January 1991

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# mitsubishi

VLSI    MOS    Memory

## RAM / ROM

## New package

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January 1991

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## NOTE



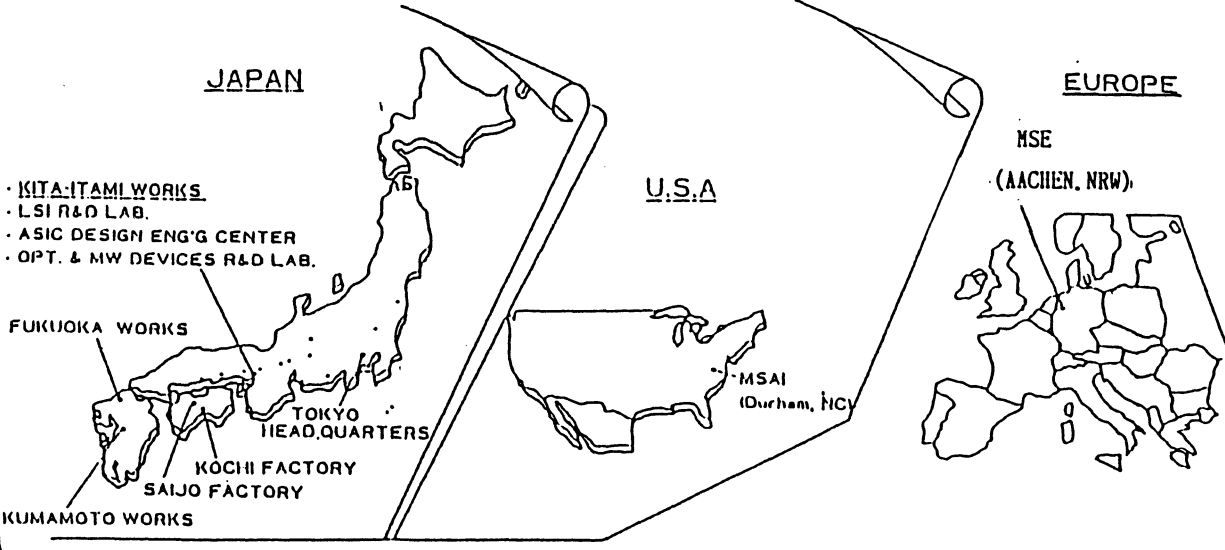
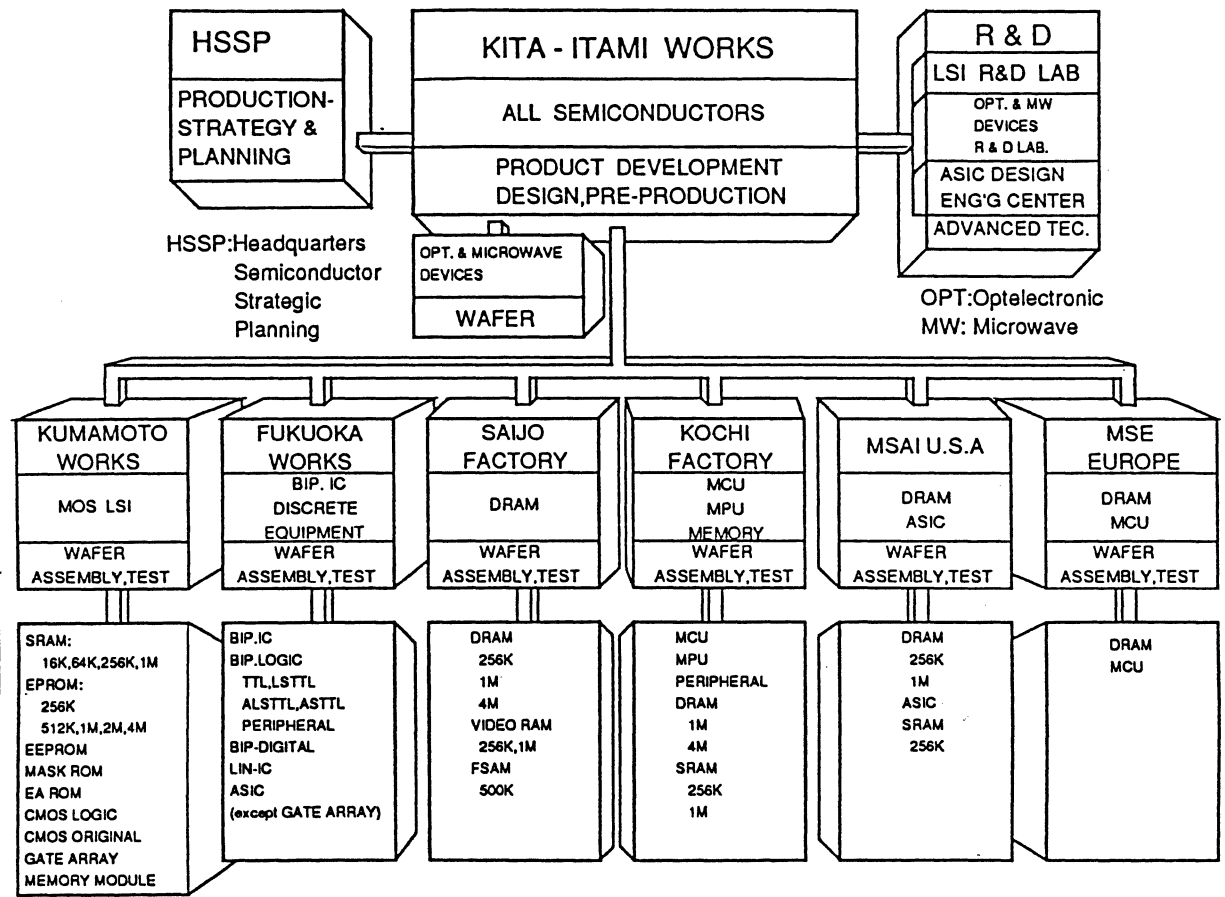
..... NEW INFORMATION



..... REVISION



## SEMICONDUCTOR TECHNOLOGY DEVELOPMENT and MANUFACTURING FACILITIES



# MITSUBISHI MOS Memory LSI (1)

		Products	Type name	I Ref	Access(ns)	Sample	Production	Page
D y n a m i c		256KX1NMOS	M5M4256A,7A,P,L,J		85,100,120	-	Yes	
		64KX4NMOS	M5M4464AP,L,J		80,100,120	-	Yes	
		1MX1CMOS	M5M41000BP,J,L	L	70,80,100	-	Yes	38~44
		1MX1CMOS	M5M41000BP,J,L		60	-	91-2	◆
		1MX1CMOS	M5M41001BP,J,L	L	70,80,100	-	Yes	◆
		1MX1CMOS	M5M41002BP,J,L	L	70,80,100	-	Yes	◆
		1MX1CMOS	M5M41000BVP,RV	L	70,80,100	-	Yes	◆
		256KX4CMOS	M5M44256BP,J,L	L	70,80,100	-	Yes	◆
		256KX4CMOS	M5M44256BP,J,L		60	-	91-2	◆
		256KX4CMOS	M5M44258BP,J,L	L	70,80,100	-	Yes	◆
		256KX4CMOS	M5M44266BP,J,L	L	70,80,100	-	Yes	◆
		256KX4CMOS	M5M44268BP,J,L	L	70,80,100	-	Yes	◆
		256KX4CMOS	M5M44256BVP,RV	L	70,80,100	-	Yes	◆
		4MX1CMOS	M5M44100J,L	L	80,100	-	Yes	12~26
		4MX1CMOS	M5M44101J,L		80,100	-	Yes	◆
		4MX1CMOS	M5M44102J,L		80,100	-	Yes	◆
		1MX4CMOS	M5M44400J,L	L	80,100	-	Yes	◆
		1MX4CMOS	M5M44402J,L		80,100	-	Yes	◆
		4MX1CMOS	M5M44100AWJ,J,L,TP,RT	L	60,70,80,100	-	91-1	◆
		4MX1CMOS	M5M44101AWJ,J,L,TP,RT		60,70,80,100	-	91-1	◆
		4MX1CMOS	M5M44102AWJ,J,L,TP,RT		60,70,80,100	-	91-1	◆
		1MX4CMOS	M5M44400AWJ,J,L,TP,RT	L	60,70,80,100	-	91-1	◆
		1MX4CMOS	M5M44402AWJ,J,L,TP,RT		60,70,80,100	-	91-1	◆
		1MX4CMOS	M5M44410AWJ,J,L,TP,RT	L	60,70,80,100	-	91-1	◆
		1MX4CMOS	M5M44412AWJ,J,L,TR,RT		60,70,80,100	-	91-1	◆
		512KX8CMOS	M5M44800AJ,L,TP,RT	L	60,70,80,100	91-2	91-4	27~35
		512KX9CMOS	M5M44900AJ,L,TP,RT	L	60,70,80,100	91-7	91-10	◆
		256KX16CMOS	M5M44260AJ,(L),TP,RT		(60,70),80,100	91-2	91-4	◆
		256KX16CMOS	M5M44170AJ,(L),TP,RT	L	60,70,80,100	91-2	91-4	◆
		256KX18CMOS	M5M44280AJ,(L),TP,RT	L	(60,70),80,100	91-7	91-10	◆
	256KX18CMOS	M5M44190AJ,(L),TP,RT	L	60,70,80,100	91-7	91-10	◆	
Video RAM		64KX4CMOS	M5M4C264L		100,120,150	-	Yes	53~54
		64KX4CMOS	M5M4C264AJ,L		80,100,120,	90-9	90-11	◆
		256KX4CMOS	M5M442256J,L		100,120	-	Yes	46~49
		256KX4CMOS	M5M442256AJ,L		70,80,100	90-12	91-2	◆
		128KX8CMOS	M5M482128J		100,120	-	Yes	50~52
		128KX8CMOS	M5M482128AJ		70,80,100	90-12	91-2	◆
Field SAM		80KX6CMOS	M5M4C500L		50,60,100	-	Yes	57~58
		80KX6CMOS	M5M4C500AL		30,50	90-6	90-12	◆
		261KX4CMOS	M5M4C900L		30(50)	-	TBD	55
S t a t i c	S t d.	8kX8 CMOS	M5M5165P,FP	Isb L	70,100,120	-	Yes	
		32KX8 CMOS	M5M5256BP,FP,KP	L/L	70,85,100,120	-	Yes	75~76
		32KX8 CMOS	M5M5255BP,FP,KP	L/L	70,85,100,120	-	Yes	◆
		32KX8 CMOS	M5M5256BVP,RV	L/L	70,85,100,120	-	Yes	◆
		128KX8 CMOS	M5M51008P,FP,VP,RV	L/L	70,85,100,120	-	Yes	69~74
	F a s t	64KX1 CMOS	M5M5187AP,J		25,35,45,55	-	Yes	
		16KX4 CMOS	M5M5188AP,J		25,35,45,55	-	Yes	64
		16KX4 CMOS	M5M5189AP,J (OE)		25,35,45,55	-	Yes	69
		64KX1 CMOS	M5M5187BP,J		15,20,25	-	Yes	68
		16KX4 CMOS	M5M5188BP,J		15,20,25	-	Yes	69
	16KX4 CMOS	M5M5189BP,J (OE)		15,20,25	-	Yes		
	8KX8 CMOS	M5M5178P,KP,J		35,45,55	-	Yes	64~65	
	8KX9 CMOS	M5M5179P,J		35,45,55	-	Yes	◆	
	8KX8 CMOS	M5M5178AP,FP,J		15,20,25	-	Yes	◆	
	8KX9 CMOS	M5M5179AP,FP,J		15,20,25	-	Yes	◆	
	8KX8 CMOS	M5M5180AP,FP,J (Latch)		20,25	-	Yes	◆	

# MITSUBISHI MOS Memory LSI (2)

	Products	Type name	Access(ns)	Sample	Production	Page
S t a t i c	256KX1 CMOS	M5M5257P,J	35,45	-	Yes	67~68
	64KX4 CMOS	M5M5258P,J	35,45	-	Yes	•
	256KX1 CMOS	M5M5257AP,J	25,30	-	Yes	•
	64KX4 CMOS	M5M5258AP,J	25,30	-	Yes	•
	256KX1 CMOS	M5M5257BP,J	15,20	90-12	91-3	67~68
	64KX4 CMOS	M5M5258BP,J	15,20	90-12	91-3	•
	64KX4 CMOS	M5M5259BP,J,(OE)	15,20	91-2	91-3	•
	32KX8 CMOS	M5M5278P,J	(15),20,25	91-1	91-3	66
	32KX9 CMOS	M5M5279P,J	(15),20,25	91-1	91-3	•
	1MX1 CMOS	M5M51001P,J	25,35,45	-(25:91-1)	Yes(25:91-4)	63~65
	256KX4 CMOS	M5M51004P,J	25,35,45	-(25:91-1)	Yes(25:91-4)	•
	256KX4 CMOS	M5M51014,J,(I/O Sepa)	25,35,45	-(25:91-1)	Yes(25:91-4)	•
E P R O M	32KX8 NMOS	M5L27256K	200,250	-	Yes	•
	64KX8 NMOS	M5L27512K	170,200,250	-	•	•
	32KX8 CMOS	M5M27C256AK	85,100,120,150	-	•	•
	64KX8 CMOS	M5M27C512AK	100,120,150	-	•	•
	128KX8 CMOS	M5M27C100K	120,150,200,250	-	•	84
	128KX8 CMOS	M5M27C101K,J,K	120,150,200,250	-	•	•
	64KX16 CMOS	M5M27C102K,J,K	120,150,200,250	-	•	•
	256KX8 CMOS	M5M27C201K,J,K	100,120,150	-	•	•
	128KX16 CMOS	M5M27C202K,J,K	100,120,150	-	•	80
	512KX8 CMOS	M5M27C401K	120,150	-	•	•
	256KX16 CMOS	M5M27C402K	120,150	-	•	•
O T P	32KX8 NMOS	M5M27256P,FP	200,250	-	Yes	•
	64KX8 NMOS	M5M27512P,FP	250	-	•	•
	32KX8 CMOS	M5M27C256AP,FP,VP,RV	(120),150	-	•	•
	64KX8 CMOS	M5M27C512AP,FP	150	-	•	•
	128KX8 CMOS	M5M27C100P	150	-	•	86
	128KX8 CMOS	M5M27C101P,J,FP,VP,RV	150	-	•	•
	64KX16 CMOS	M5M27C102P,J,FP,VP,RV	150	-	•	83
	256KX8 CMOS	M5M27C201P,J,FP,VP,RV	(120),150	-	•	•
	128KX16 CMOS	M5M27C202P,J,FP,VP,RV	(120),150	-	•	•
	512KX8 CMOS	M5M27C401P	150	-	91-2	•
256KX16 CMOS	M5M27C402P	150	-	91-2	•	
M a s k R O M	512KX8 / 256KX16 CMOS	M5M23400AP,FP,VP,RV	150	-	Yes	92~95
	512KX8 CMOS	M5M23401AP,FP,VP,RV	150	-	Yes	•
	1MX8 / 512KX16 CMOS	M5M23800P,FP,VP,RV	150	Yes	91-4	•
	1MX8 CMOS	M5M23801P,FP,VP,RV	150	Yes	91-3	•
	2MX8 / 1MX16 CMOS	M5M23160P,FP,VP,RV	150	Yes	91-3	•
EEPROM	8KX8 CMOS	M5M28C64AP,FP,VP,RV	150,200	-	Yes	90~91
Flash EEPROM	128KX8 CMOS 64KX8 CMOS	M5M28F101P,J,FP,VP,RV M5M28F102P,J,FP,VP,RV	100,120,150 100,120,150	Yes 91-2	91-2 91-5	88 •
Versatile Memory	256KOTP+16KSRAM	M6M72561J	ROM / SRAM	-	Yes	96
		M6M72561J-I	200 / 150	-	Yes	•



# MITSUBISHI ELECTRIC

## MITSUBISHI Memory Module



	Products	Type name	Access(ns)	Sample	Production	Page
1 M D R A M  M o d u l e	1MX8 CMOS Fast Page mode	MH1M08B0J,JA	60,70,80,100	-	Yes	
	1MX9 CMOS Fast Page mode	MH1M09B0J,JA	60,70,80,100	-	Yes	
	1MX8 CMOS Nibble mode	MH1M08B1J,JA	70,80,100	-	Yes	
	1MX9 CMOS Nibble mode	MH1M09B1J,JA	70,80,100	-	Yes	
	1MX8 CMOS Static column mode	MH1M08B2J,JA	70,80,100	-	Yes	
	1MX9 CMOS Static column mode	MH1M09B2J,JA	70,80,100	-	Yes	
	1MX8 Double sided 25PIN	MH1M08BCJA	70,80,100	-	Yes	
	1MX9 Double sided Fast Page mode	MH1M9B0DJA	70,80,100	-	Yes	
	1MX9 Double sided Nibble mode	MH1M9B1DJA	70,80,100	-	Yes	
	1MX9 Double sided Static column mode	MH1M9B2DJA	70,80,100	-	Yes	
	2MX4 CMOS Fast Page mode	MH2M04B0J,JA	70,80,100	-	Yes	
	2MX4 CMOS Nibble mode	MH2M04B1J,JA	70,80,100	-	Yes	
	2MX4 CMOS Static column mode	MH2M04B2J,JA	70,80,100	-	Yes	
	256KX32 CMOS Fast Page mode	MH25632BJ	70,80,100	-	Yes	
	512KX32 CMOS Fast Page mode	MH51232BJ	70,80,100	-	Yes	
	256KX36 CMOS Page mode	MH25636BJ	85,100,120	-	Yes	
	512KX36 CMOS Page mode	MH51236BJ	85,100,120	-	Yes	
	1MX36 TSOP,CMOS Fast Page	MH1M36BBJ	70,80,100	-	Yes	
	256KX8 CMOS Fast Page mode	MH25608BAJ,JA	70,80,100	-	Yes	
	256KX9 CMOS Page mode	MH25609BAJ,JA	85,100,120	-	Yes	
1MX36 Double sided 72PIN	MH1M36BJ	70,80,100	-	Yes		
256KX16Pseudo-Pseudo SRAM Module	MH25616PNA	8MHz,10MHz	-	Yes		
512KX8Pseudo-Pseudo SRAM Module	MH51208PNA	8MHz,10MHz	-	Yes		
M 4 o M d D u R I A e M	1MX9 CMOS Fast Page mode	MH1M09A0AJ,JA	60,70,80,100	-	Yes	
	4MX9 CMOS Fast Page mode	MH4M09A0J	80,100	-	Yes	102
	4MX9 Double Sided Fast Page mode	MH4M90DJA	80,100	-	Yes	
	1MX36 CMOS Fast Page mode	MH1M36CJ	80,100	-	Yes	
	1MX36 Double Sided Fast Page mode	MH1M36DJ	80,100	-	Yes	102
	1MX36 CMOS Low profile	MH1M36EJ	60,70,80,100	Yes	91/2	
	2MX36 Double Sided	MH2M36CJ	80,100	-	Yes	103
	2MX36 Double Sided Low profile	MH2M36EJ	60,70,80,100	Yes	91/2	103
	2MX8 Pseudo-Pseudo SRAM Module	MH2M08PNA	8MHz,10MHz	91/2	91/4	104
	2MX40 Double Sided Fast Page	MH2M40AJ	80,100	91/2	91/4	
4MX36 Double Sided Fast Page	MH4M36AJ	80,100	91/2	91/4		
M 5 6 o K S u R I A M	128KX8 CMOS (30PIN N-C)	MH12808TNA	85,100,120	-	Yes	
	128KX8 CMOS (30PIN CS2)	MH12908TNA	85,100,120	-	Yes	
	256KX8 CMOS (30PIN,NC,TSOP)	MH25608TNA	85,100,120	-	Yes	
	256KX8 CMOS (30PIN CS2,TSOP)	MH25708TNA	85,100,120	-	Yes	
	256KX8 CMOS 35PIN SIM	MH25608SIN	70,85,100,120	-	Yes	
	512KX8 CMOS (TSOP)	MH51208TNA	85,100,120	-	Yes	
	512KX8 CMOS 64PIN SIM	MH51208SN	70,85,100,120	-	Yes	106
	256KX9 CMOS 35PIN SIM	MH25609ASN	100,120	-	Yes	
M o d u l e  M S R A M	512KX8 CMOS (TSOP,32PIN DIP)	MH51208ANA	85,100,120	-	Yes	
	512KX8 CMOS (SOP,32PIN DIP)	MH51208UNA	85,100,120	-	Yes	
	1MX8 CMOS (TSOP,36PIN DIP)	MH1M08TNA	85,100,120	91/1	91/4	
	2MX8 CMOS (TSOP,36PIN DIP)	MH2M08TNA	85,100,120	91/1	91/4	105
M o d u l e  M S R A M	64KX32 CMOS (64PIN ZIP)	MH6432NZ	15,20	91/3	91/6	105
M o d u l e  R O M	256KX16 CMOS	MH25616RNA	150,200,250	-	Yes	106
	512KX16 CMOS	MH51216RNA	150,200,250	-	Yes	
M o d u l e  R A M o I D e	128KX16 CMOS	MH12816JZ	80,100,120	-	Yes	104
	128K X 16 CMOS	MH12816AJZ	70, 80, 100	91/2	91/3	

MITSUBISHI DRAM PLAN

	89	90	91	92	93	94	95
256KD	Shrink X1/X4						
Dual Port	X4		2nd X4				
FSAM(500K)	X6		2nd X6				
1MD	2nd	3rd	X1/X4				
Dual Port		X4	2nd				
		X8	2nd				
FSAM			X4				
4MD	1st		2nd X1/X4			3rd	
			X8/X16				
Dual Port			X9/X18				
			X8				
			X16				
4MCDRAM							
FSAM							
16MD							
Dual Port							
16MCDRAM							
FSAM							
64MD							

New product / Under Development DRAM

Memory cap	1M					4M			
Organization	1M X 1	256K X 4	256K X 4 (Dual port)	128K X 8	261K X 4 (FSAM)	4M X 1	1M X 4	512K X 8	256K X 16
Type name	M5M 41000B	M5M 44256B	M5M 442256	M5M 482128	M5M 4C900	M5M 44100A	M5M 44400A	M5M 44800A	M5M 44260A
Access time (n s)	70 80 100		100(30) 120(40)		30	60.80 70,100		60 70 80 100	(60) (70) 80 100
Pd. (mW) max.	Active	440 385 330	660 550	770	550 467.5 412.5 357.5	550 467.5 412.5 357.5	550 490 413	660 550 490 413	(1045) (908) 770 660
	St. by	2.75		27.5	33	5.5		5.5	5.5
Pins/Pkg*/W (mil)	18P(300) 26J 20L 24VP	20P(300) 26J 20L 24VP	28L(400) 28J(400)	40J(400)	28L	26WJ(350)26J(300) 20L(400)26TP(300) 26RT(300)		28J(400) 28L(400) 28TP,RT	40J(400) 44TP,RT
Chip size (mm <sup>2</sup> )	3.88 X 11.39		5.08 X 13.54		4.94 X 13.85	5.36 X 14.45		5.81 X 14.80	5.81 X 14.80
Process technology	CMOS 0.9 μ		CMOS 1.0 μ			CMOS 0.7 μ		CMOS 0.7 μ	CMOS 0.7 μ
Sample availability	Already		Already	Already	TBD	Already		91-2	91-2

\*P=DIP, J=SMD, L=ZIP, VP=TSOP type I, TP=TSOP type II RT=reverse bend type TSOP



### MITSUBISHI SRAM PLAN

	'89	'90	'91	'92	'93	'94	'95	
Fast	16Kx1 4Kx4 64Kx1 16Kx4	45 / 55 ns		A ver, 25 ~ 55 ns		B ver, 15 / 20 ns		
	8Kx8 8Kx9	35 ~ 55 ns		A ver, 15 / 20 ns		(15) / 20 ns / 25		
	32Kx8 x9 256Kx1 64Kx4	35 ~ 55 ns		A ver, 25 / 35 ns		B ver, 15 / 20 ns		
	1Mx1 256Kx4	35 ~ 45 ns		25 / 45 ns				
	Slow	8Kx8	70 ~ 120 ns		70 ~ 120 ns Shrink chip		70 ~ 120 ns	
		32Kx8						
		128Kx8						
	4M							



### NEW Product / Under Development SRAM

Process	B				C		D		E		
Memory cap	64K / 72K		256K		64K	256K	1M	64K / 72K	1M	256K / 288K	
Organization	64Kx1 16Kx4	8Kx8 8Kx9	32Kx8	256Kx1 64Kx4	64Kx4 16Kx4	256Kx1 64Kx4	128Kx8	8Kx8 8Kx9	1Mx1 256Kx4	256Kx1 64Kx4	32Kx8 32Kx9
Type name	M5M5187A M5M5188A M5M5189A	M5M5178 M5M5179	M5M5256B M5M5255B	M5M5257 M5M5258	M5M5187B M5M5188B M5M5189B	M5M5257A M5M5258A	M5M51008	M5M5178A M5M5179A M5M5180A	M5M51001 M5M51004	M5M5257B M5M5258B M5M5259B	M5M5278 M5M5279 M5M5269
Access time(ns)	25 35 45 55	35 45 55	70 85 100 120	35 45	15 20 25	25 30	70 85 100 120	15 20 25	25 35 45	15 20	(15) 20 25
Power(mw)											
Active											
Stand by (MOS)	550 11	660 11	385 0.55 0.15	660 11	550 55	660 55	385 0.55 0.15	660 55	660 55	660 55	660 55
Stand by (3V)											
Pins/Pkg/ Width(mil)	22P(300) 24P(300) 24J(300)	28P(300) 28J(300)	28P(300, 600) 28FP(450) 28TSOP	24P(300) 24J(300)	22P(300) 24P(300) 24J(300)	24P(300) 24J(300)	32P(600) 32FP(525) 32TSOP	28P(300) 28J(300) 28FP(450)	28P(400) 28J(400)	24P(300) 24J(300)	28P(300) 28J(300) 32P(300) 32J(300)
Chip Size(mm)	6.35x3.69	7.12x4.29	8.33x4.72	10.68x4.60	5.73x3.33	11.01x4.66	15.72x6.01	5.53x3.53	15.84x6.10	10.69x4.54	11.89x4.6
Channel length	1.1 μm 1.6 μm	1.1 μm 1.6 μm	1.1 μm 1.6 μm	1.1 μm 1.6 μm	1.1 μm 1.2 μm	1.1 μm 1.2 μm	0.9 μm 1.1 μm	0.9 μm 1.1 μm	0.8 μm 1.0 μm	0.8 μm 1.0 μm	0.8 μm 1.0 μm
Design rule	1.3 μm	1.5 μm	1.0 μm	1.0 μm	1.1 μm	1.0 μm	0.8 μm	0.8 μm	0.8 μm	0.8 μm	0.8 μm
Process	CMOS,LDD,MoSi tox=220A				CMOS,LDD MosI,tox=180A		CMOS,LDD Wsl 3-poly		CMOS,LDD Wsl 3-poly 2-Al		
Availability	Already	Already	Already	Already	Already	Already	Already	Already	Already (25-91-1)	90-12	91-1



# MITSUBISHI ROM PLAN

		'89	'90	'91	'92	'93	'94	'95
EPROM(OTP)	NMOS 256K	[Timeline bar]						
	NMOS 512K	[Timeline bar]						
	CMOS 256K	[Timeline bar]			Shrink			
	CMOS 512K	[Timeline bar]						
	1M	[Timeline bar]						
	2M	[Timeline bar]						
	4M	[Timeline bar]						
Flash EEPROM	1M		[Timeline bar]					
	4M			[Timeline bar]				
	16M				[Timeline bar]			
EEPROM	64K	[Timeline bar]						
Mask ROM	4M	[Timeline bar]		Shrink				
	8M		[Timeline bar]					
	16M		[Timeline bar]					
	32M			[Timeline bar]				



# New Product / Under Development ROM

Device	EPROM / OTP**						EEPROM	MASK ROM					Flash EEPROM		
	1M		2M		4M			64K	4M		8M	16M	1M		
Memory cap.	128Kx8	64Kx16	256Kx8	128Kx16	512Kx8	256Kx16	8Kx8	512Kx8 256Kx16	512Kx8	1Mx8 512Kx16	1Mx8	2Mx8 1Mx16	128Kx8	64Kx16	
Organization															
Type name	M5M 27C100 / 101	M5M 27C102	M5M 27C201	M5M 27C202	M5M 27C401	M5M 27C402	M5M 28C64A	M5M 23400A	M5M 23401A	M5M 23800	M5M 23801	M5M 23160	M5M 28F101	M5M 28F102	
Access time (ns)	120 150** 200 250	120 150** 200 250	100 120 150**	100 120 150**	120 150**	120 150**	150 200	150	150	150	150	150	100 120 150	100 120 150	
Pd. (mW)	Active	263	263	165	165	165	165	165	165	165	275	275	275	165	275
	Standby	0.55	0.55	0.55	0.55	0.55	0.55	5.5	0.55	0.55	0.55	0.55	0.55	0.55	0.55
Chip size(mm <sup>2</sup> )	45.0	48.6	50.9	53.5	87.5	91.5	34.2	58.5	58.5	73.2	73.9	128.7	38.1	TBD	
Process technology	CMOS 1.2 μm	CMOS 1.2 μm	CMOS 0.9 μm	CMOS 0.9 μm	CMOS 0.9 μm	CMOS 0.9 μm	CMOS 1.2 μm	CMOS 1.1 μm	CMOS 1.1 μm	CMOS 0.8 μm	CMOS 0.8 μm	CMOS 0.8 μm	CMOS 0.9 μm	CMOS 0.9 μm	
Pins Package* Width(mil)	32K(600) 32P(600) 32FP(525) 32J 32JK 40VP,RV	40K(600) 40P(600) 40FP(525) 44J 44JK 40VP,RV	32K(600) 32P(600) 32FP(525) 32J 32JK 40VP,RV	40K(600) 40P(600) 40FP(525) 44J 44JK 40VP,RV	32K(600) 32P(600)	40K(600) 40P(600)	28P(600) 28FP(450) 28VP,RV	40P(600) 40FP(525) 40VP,RV	32P(600) 32FP(525) 40VP,RV	42P(600) 44FP(600) 48VP,RV	32P(600) 32FP(525) 40VP,RV	42P(600) 44FP(600) 48VP,RV	32P(600) 32FP(525) 32J 32VP,RV	40P(600) 40FP(525) 44J 40VP,RV	
Sample availability	Already	Already	Already	Already	Already	Already	Already	Already	Already	Already	Already	Already	Already	'91-2	
Note															

Package \* : K: Ceramic DIP, P: DIP, FP: SOP, J: PLCC, VP / RV: TSOP, JK: Ceramic LCC(CLCC)



# MITSUBISHI ELECTRIC

## New package series for MOS Memory



		Organization	DIP	ZIP	PLCC	SOP	TSOP	SOJ	QFP	CLCC	Page
DRAM		256KX1	⊙(16)	⊙(16)	⊙(18)	—	—	—	—	—	
		64KX4	⊙(18)	⊙(20)	⊙(18)	—	—	—	—	—	
		1MX1	⊙(18)	⊙(20)	—	—	⊙(24)	⊙(26)	—	—	
		256KX4	⊙(20)	⊙(20)	—	—	⊙(24)	⊙(26)	—	—	
		4MX1	—	⊙(20)	—	—	⊙(26)	⊙(26)	—	—	
		1MX4	—	⊙(20)	—	—	⊙(26)	⊙(26)	—	—	
		512KX8	—	⊙(28)91-4	—	—	⊙(28)91-4	⊙(28)91-4	—	—	
		512KX9	—	⊙(28)91-10	—	—	⊙(28)91-10	⊙(28)91-10	—	—	
		256KX16	—	△(40)	—	—	⊙(44)91-4	⊙(40)91-4	—	—	
	256KX18	—	△(40)	—	—	⊙(44)91-10	⊙(40)91-10	—	—		
VRAM		64KX4	—	⊙(24)	—	—	△	⊙(24)	—	—	
		256KX4	—	⊙(28)	—	—	△	⊙(28)	—	—	
		128KX8	—	—	—	—	△	⊙(40)	—	—	
FSAM		80KX6	—	⊙(28)	—	—	△	△	—	—	
		261KX4	—	△(28)	—	—	—	—	—	—	
SRAM	SLOW	8KX8	300mil	—	—	—	—	⊙(28)	—	—	—
			600mil	—	—	—	—	—	—	—	—
		32KX8	⊙(28)	⊙(28)	—	—	⊙(28)	⊙(28)	—	—	—
	128KX8	—	⊙(32)	—	—	⊙(32)	⊙(32)	—	—	—	
	FAST	64KX1	⊙(22)	—	—	—	—	—	⊙(24)	—	—
			16KX4	⊙(22)	—	—	—	—	⊙(24)	—	—
			16KX4(OE)	⊙(24)	—	—	—	—	⊙(24)	—	—
		8KX8	⊙(28)	⊙(28)	—	—	⊙(28)	—	⊙(28)	—	—
		8KX9	⊙(28)	—	—	—	⊙(28)	—	⊙(28)	—	—
		256KX1	⊙(24)	—	—	—	—	△(24)	⊙(24)	—	—
		64KX4	⊙(24)	—	—	—	—	—	⊙(24)	—	—
		32KX8	⊙(28)91-3	—	—	—	△(28)	—	⊙(28)91-3	—	—
		32KX9	⊙(32)91-3	—	—	—	△(32)	—	⊙(32)91-3	—	—
	1MX1	400mill	—	—	—	—	△(32)	⊙(28)	—	—	
	256KX4	⊙(28)	—	—	—	—	△(32)	⊙(28)	—	—	
256KX4 I/O separate	400mill	—	—	—	—	—	⊙(32)	—	—		
EPROM	1M	128KX8	⊙(32)	—	—	—	—	—	—	⊙(32)	
		64KX16	⊙(40)	—	—	—	—	—	—	⊙(44)	
	2M	256KX8	⊙(32)	—	—	—	—	—	—	⊙(32)	
		128KX16	⊙(40)	—	—	—	—	—	—	⊙(44)	
	4M	512KX8	⊙(32)	—	—	—	—	—	—	△	
		256KX16	⊙(40)	—	—	—	—	—	—	△	
OTP	1M	128KX8	⊙(32)	—	⊙(32)	⊙(32)	⊙(40)	—	—	—	
		64KX16	⊙(40)	—	⊙(44)	⊙(40)	⊙(40)	—	—	—	
	2M	256KX8	⊙(32)	—	⊙(32)	⊙(32)	⊙(40)	—	—	—	
		128KX16	⊙(40)	—	⊙(44)	⊙(40)	⊙(40)	—	—	—	
	4M	512KX8	⊙(32)	—	—	—	—	—	—	—	
		256KX16	⊙(40)	—	—	—	—	—	—	—	
MASK ROM	4M	512KX8	⊙(32)	—	—	⊙(32)	⊙(40)	—	—	—	
		512KX8/256KX16	⊙(40)	—	—	⊙(40)	⊙(40)	—	—	—	
	8M	1MX8	⊙(32)91-3	—	—	⊙(32)91-5	⊙(40)91-6	—	—	—	
		1MX8/512KX16	⊙(42)91-4	—	—	⊙(44)91-7	⊙(48)91-8	—	—	—	
16M	2MX8/1MX16	⊙(42)91-3	—	—	⊙(44)91-6	⊙(48)91-8	—	—	—		
Flash EEPROM	1M	128KX8	⊙(32)91-1	—	⊙(32)91-4	⊙(32)91-4	⊙(32)91-4	—	—	—	
		64KX16	⊙(40)91-5	—	⊙(44)91-6	⊙(40)91-6	⊙(40)91-6	—	—	—	

⊙:Production, ○:Development, Production start time  
 △:Market Survey, —:No plan

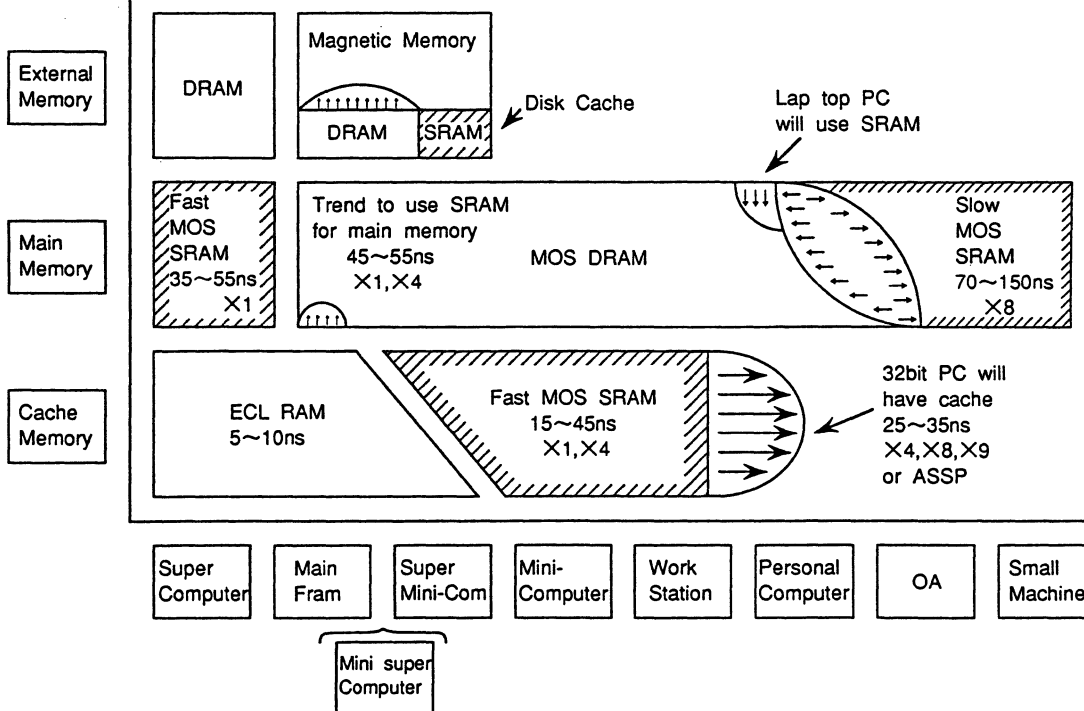


## Semiconductor Devices in Computer

Functional Block	Personal Computer		EWS	Small & Medium Computer	Large Computer	Super Computer
	Book Type Lap top	Desk Top				
CPU	Standard MPU			Custom and semicustom LSI MPU Permeation	Semicustom LSI	
Other Control Unit	Custom & Semicustom LSI ASSP			Semicustom LSI		
Main Memory	DRAM Mainly	DRAM			DRAM Mainly	SRAM
	SRAM Partially				SRAM Partially	
Cache Memory	—	SRAM			—	
Display Memory	DRAM Mainly VRAM Partially		VRAM		—	

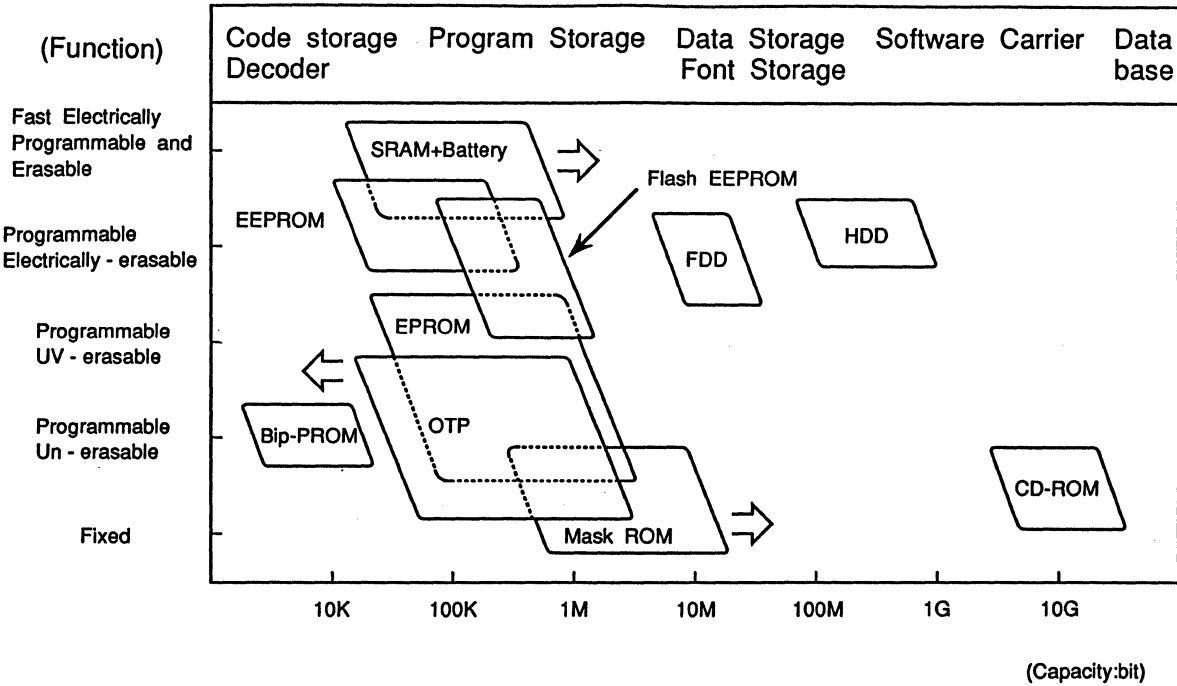
Semicustom LSI : Gate Array and Standard Cell

## Application of DRAM/ SRAM





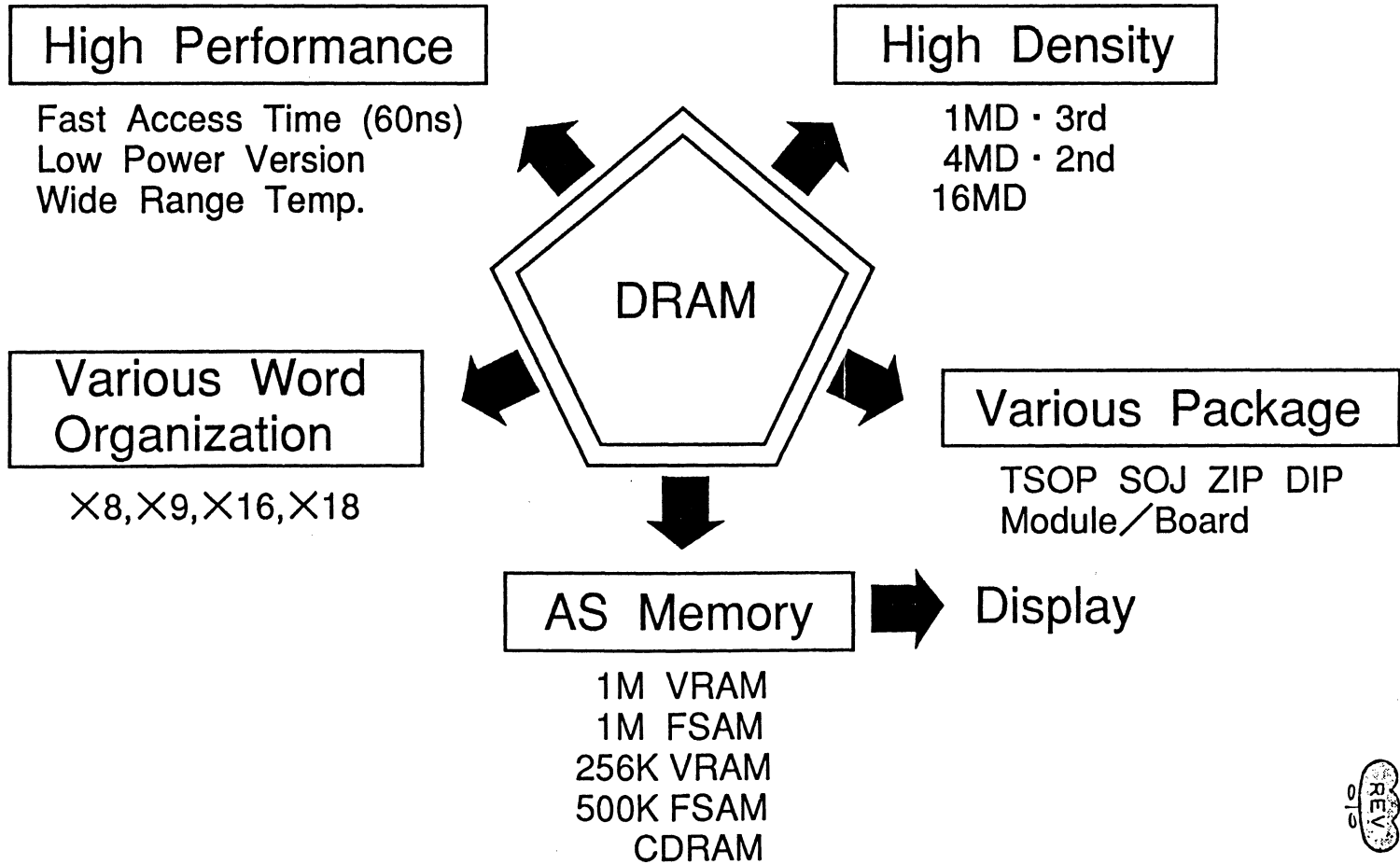
## Application of ROM



## Quality & Reliability of MITSUBISHI MOS Memory

Type of device		Incoming Inspection ppm		Field Data FIT	
		Target 1991	Results 1990	Target 1991	Results 1990
DRAM	M5M44100J, M5M44400J	100	—	100	—
	M5M41000BP	100	30~150	50	50~100
	M5M44256BP	100	30~150	50	50~100
SRAM	M5M51008P	100	—	100	—
	M5M5256BP	100	50~100	100	50~100
	M5M51001P	100	50~100	100	50~100
	M5M5257P/AP, M5M5258P/AP	100	50~100	100	50~100
EPROM	M5M27C401K	100	100~200	100	50~100
	M5M27C201K	100	100~150	100	50~100
	M5M27C101K	100	100~150	50	50~80

# Technical Strategy of DRAM

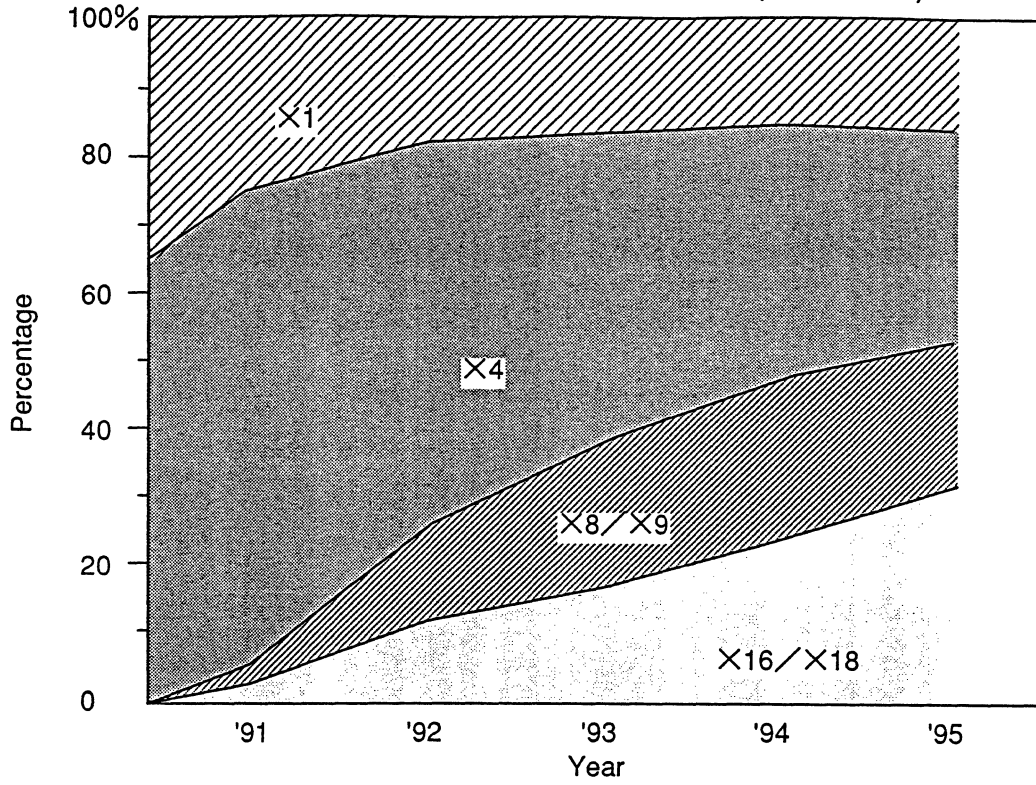


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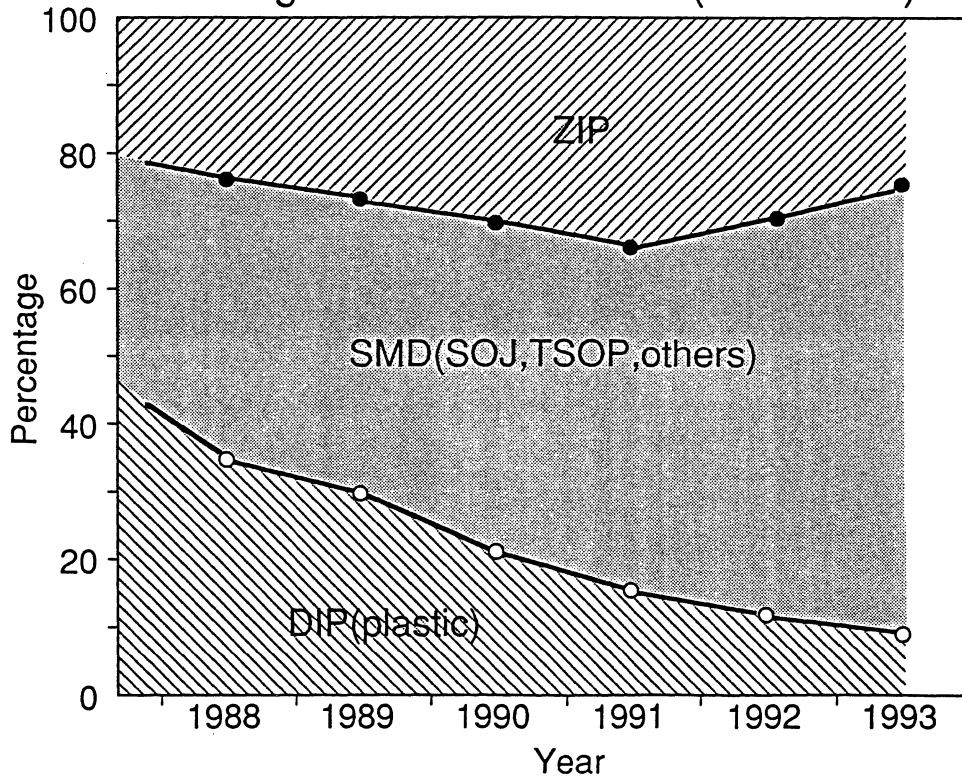


DRAM

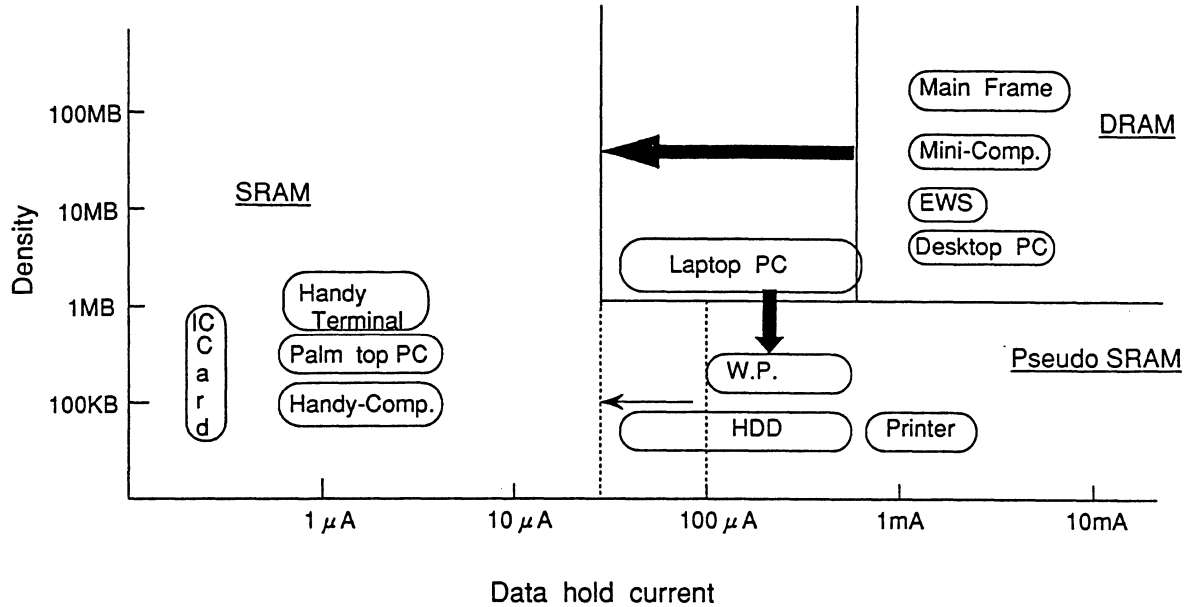
Organization Trend of 4MDRAM(Mitsubishi)



Package Trend of DRAM (Mitsubishi)



### Application of DRAM, PSRAM and SRAM



### Mitsubishi 1st Generation 4M DRAM Series

Type Name	Description	Package	Speed item	Low Power Version*	Production
M5M44100J,L	4M×1, Fast page mode	SOJ,ZIP	-8,-10	Yes	Yes
M5M44101J,L	4M×1, Nibble mode	SOJ,ZIP	-8,-10	—	Yes
M5M44102J,L	4M×1, Static column mode	SOJ,ZIP	-8,-10	—	Yes
M5M44400J,L	1M×4, Fast page mode	SOJ,ZIP	-8,-10	Yes	Yes
M5M44402J,L	1M×4, Static column mode	SOJ,ZIP	-8,-10	—	Yes

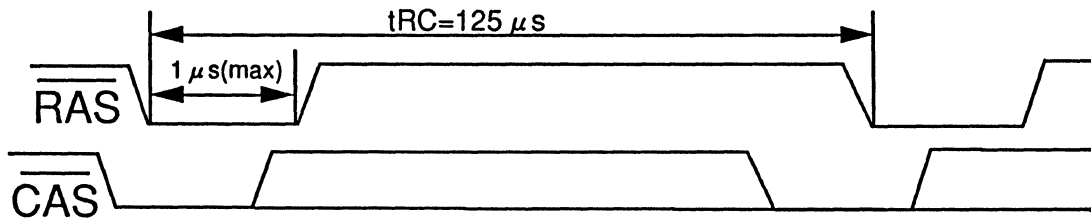
• Organization (X1/X4)---Al mask masterslice  
 • Function mode (Fast page/Nibble/Static Column)---Wire bonding option  
 \* Icc2 (MOS) = Icc8 = 500 μA (Max) at tREF = 128msec



# LOW POWER DRAM SERIES

Device	tREF	tRC	lcc2(MOS)	lcc8
1M X 1 (B) 256K X 4 (B) F.P.	64ms /512cycle	125 $\mu$ s	200 $\mu$ A	200 $\mu$ A
4M X1 1M X4 F.P.	128/1024	125	LL 300 L 500	LL 300 L 500
4M X 1 (A) 1M X 4 (A) F.P.	128/1024	125	200 (300)	200 (300)
512K X 8 (A) X 9 (A) F.P.	128/1024	125	100	250 (Future Target 200)
256K X 16/ 18 (A) 2 CAS / 1 WE F.P.	64/512	125	100	350 (F.T.300)
256K X 16/ 18 (A) 1 CAS / 2 WE F.P.	128/1024	125	100	250 (F.T.200)
64K X 4 VRAM (A)	32/256	125	200	300

lcc8 : CBR Extended (Slow) Refresh Current



$\overline{\text{CAS}}$  = 0.2V or CBR Cycling

$\overline{\text{OE}}$  =  $V_{cc} - 0.2V$

$\overline{\text{WE}}$  =  $V_{cc} - 0.2V$  or 0.2V

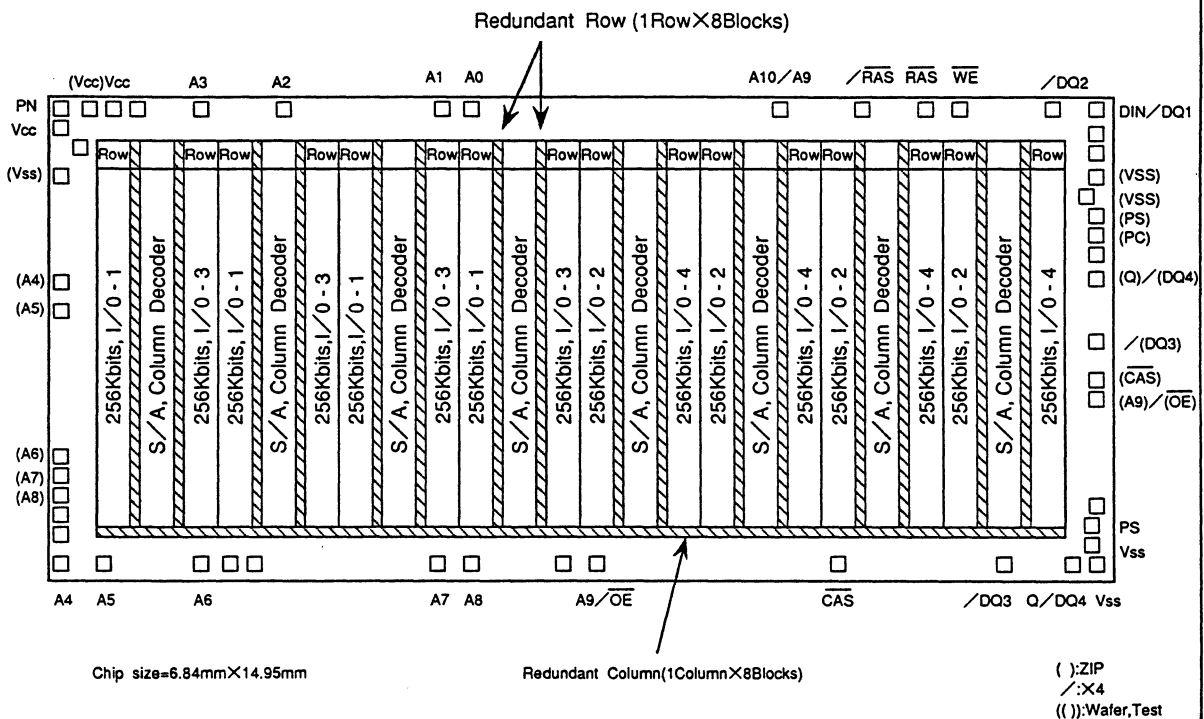
Add =  $V_{cc} - 0.2V$  or 0.2V

DQi =  $V_{cc} - 0.2V$  or 0.2V or O pen

## Features of 1st Generation 4MDRAM

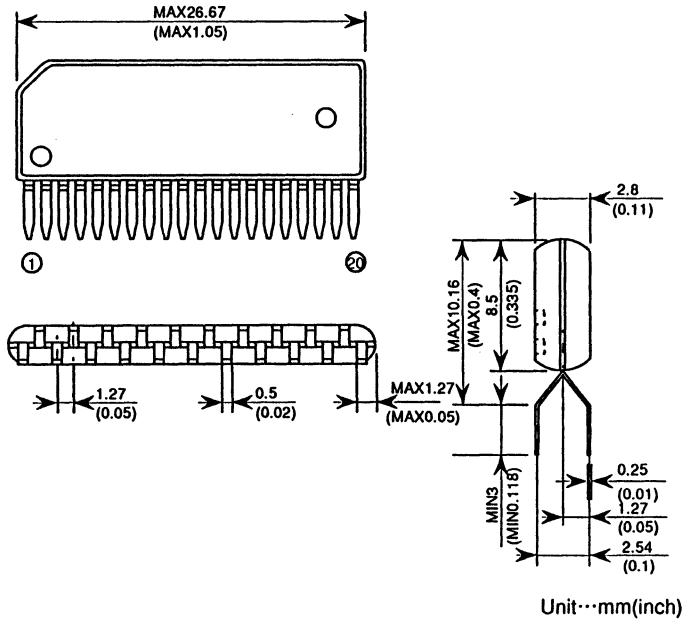
- 4M×1/1M×4 organization
- Package ----- 26pin 350mil SOJ  
20pin 400mil height ZIP
- Additional Function ----- Fast Page, Nibble, Static Column.
- Single 5volt power supply
- Test mode ----- JEDEC Standard (External Timing Induced)
- High speed / Low power, 80nsec access time at 523 mW  
100nsec access time at 468 mW
- Twin - well CMOS
- 0.8 μm minimum feature size : chip size 102mm<sup>2</sup>  
cell size 12.3 μm<sup>2</sup>
- Stacked cell structure

## Chip Architecture of 1st Generation 4MDRAM

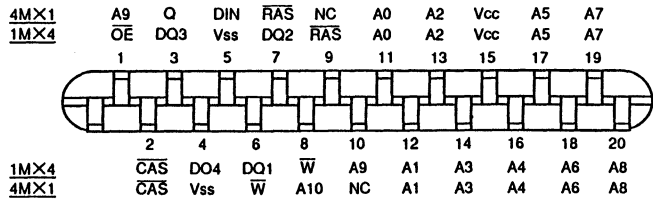


20Pin ZIP for 4M×1 and 1M×4 DRAM

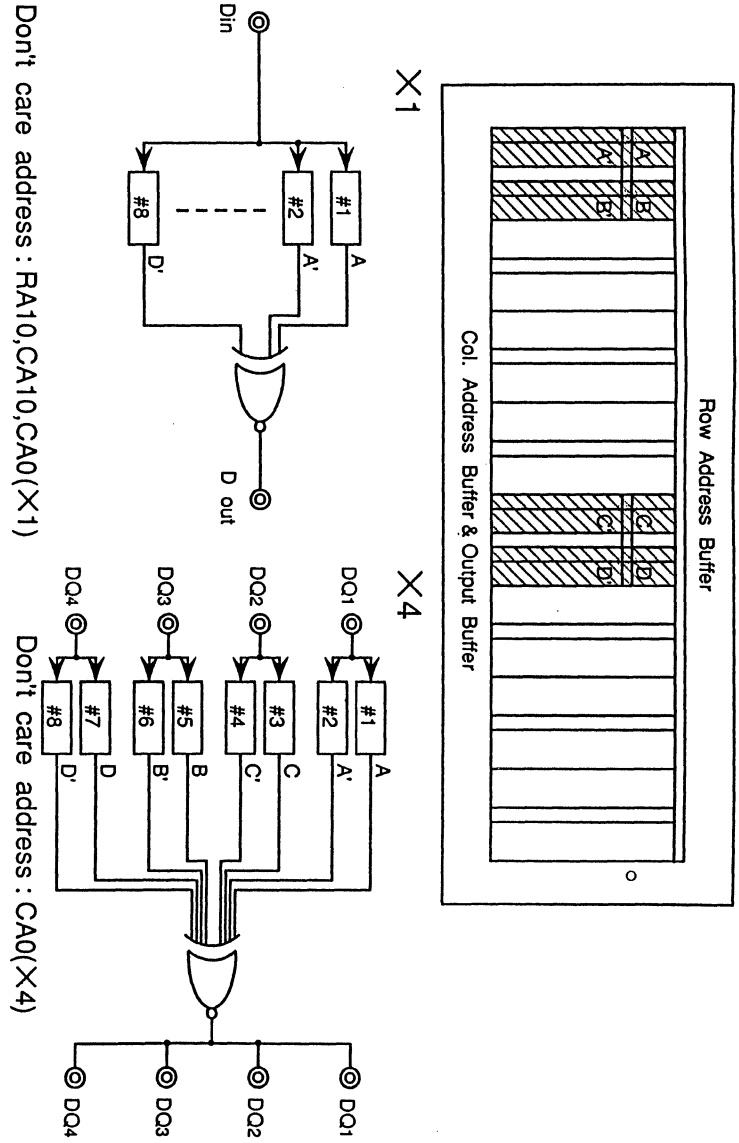
Outline Drawing



Pin configuration(Bottom view)



Configuration of Test Mode





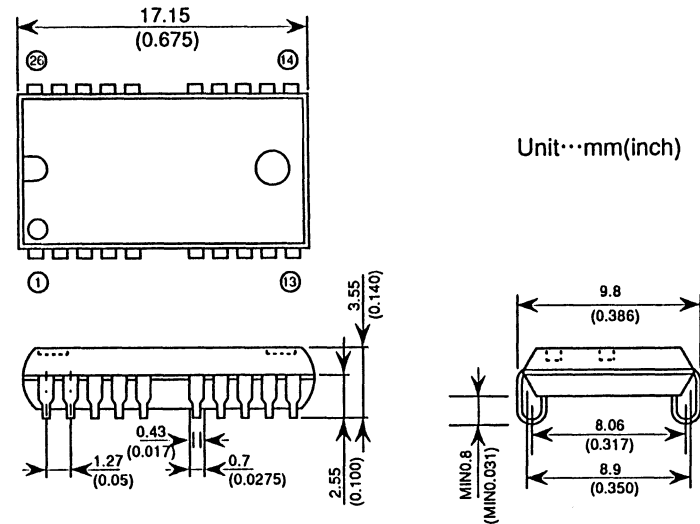
### Long Term Life Test Data for 4MDRAM SOJ and ZIP

Test	Condition	Item tested	Failures/Sample size	
			SOJ	ZIP
High temperature operating life test	Ta=125°C Vcc=7.5V t=1000hrs	• DC and function • Stability of electrical margins	0 120	1* 120
	Ta=150°C Vcc=7.0V t=1000hrs	• DC and function • Stability of electrical margins	1* 120	—
Low temperature operating life test	Ta=-20°C Vcc=8.0V t=1000hrs	• DC and function • Stability of electrical margins	0 50	0 30
High temperature storage test	Ta=175°C t=1000hrs	• DC and function • Stability of electrical margins	0 80	0 80
Soldering heat test	260°C 10sec	• DC and function	0 10	0 10
Thermal shock test	-55/125°C 15cycles			
Temperature cycling test	-65/150°C 1000cycles	• DC and function	0 120	0 120
Pressure cooker test	121°C 100%RH t=240hrs	• DC and function • Stability of electrical margins	0 140	0 180
Pressure cooker test with DC bias	140°C 85%RH Vcc=5.5V t=1000hrs	• DC and function • Stability of electrical margins	2** 82	0 160
Humidity test with DC bias	85°C 85%RH Vcc=5.5V t=2000hrs	• DC and function • Stability of electrical margins	0 230	0 230

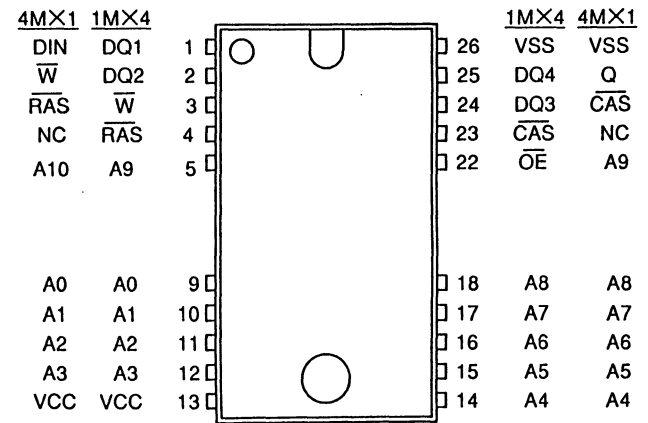
\* : Single bit failure, \*\* : DC failure

### 26Pin SOJ for 4M×1 and 1M×4 DRAM

#### Outline Drawing (Tentative)



#### Pin configuration(Top view)



### Package Reliability Data for 4MDRAM

Test	Condition	Failures/Sample size	
		SOJ	ZIP
Solderability	230°C, 5sec	0/50	0/50
Resistance to solvent	Solvent Aceton Isopropyl alcohol Trichloroethane	0/30	0/30
Lead pull	230g, 30sec	0/30	0/30
Lead bend	230g, 90°C, 3times	0/30	0/30
Radiography	Check of Lead frame Die attach Au wire Resin void	0/100	0/100
Salt atmosphere	35°C, 5wt% salt, 48hrs	0/30	0/30
Package crack	85°C, 85%RH, 72hrs→ Soldering(260°C, 30sec)	0/30	0/30

### Results of Infant Mortality Study for 4MDRAM

Sample	Condition	Sample size	Failures
M5M44100J	Dynamic burn-in Ta=125°C Vcc=7V t=100hours	5,102	9 { Single bit : 7 Bit line : 1 Word line : 1
M5M44100L		3,645	6 { Single bit : 5 Bit line : 1
Total		8,747	15

\* In case the field condition of Ta=55°C and Vcc=5V  
 $=15 / (8,747 \times 100 \times 100 \times 9.4)$   
 =18FIT

\* In case the field condition of Ta=70°C and Vcc=5V  
 $=15 / (8,747 \times 100 \times 100 \times 5.3)$   
 =32FIT



MITSUBISHI ELECTRIC



## Mitsubishi 2nd Generation 4M DRAM Series

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Type Name	Description	Package	Speed Item	Low Power Version	Sample	Production
M5M44100AWJ,J,L,TP,RT	4M×1, Fast Page mode	SOJ(300), ZIP SOJ(350), TSOP	-6,-7,-8,-10	YES	—	'91/1
M5M44101AWJ,J,L,TP,RT	4M×1, Nibble mode	SOJ(300), ZIP SOJ(350), TSOP	-6,-7,-8,-10	—	—	'91/1
M5M44102AWJ,J,L,TP,RT	4M×1, Static Column mode	SOJ(300), ZIP SOJ(350), TSOP	-6,-7,-8,-10	—	—	'91/1
M5M44400AWJ,J,L,TP,RT	1M×4, Fast Page mode	SOJ(300), ZIP SOJ(350), TSOP	-6,-7,-8,-10	YES	—	'91/1
M5M44402AWJ,J,L,TP,RT	1M×4, Static Column mode	SOJ(300), ZIP SOJ(350), TSOP	-6,-7,-8,-10	—	—	'91/1
M5M44410AWJ,J,L,TP,RT	1M×4, Fast Page mode Write Per Bit	SOJ(300), ZIP SOJ(350), TSOP	-6,-7,-8,-10	YES	—	'91/1
M5M44412AWJ,J,L,TP,RT	1M×4, Static Column mode Write Per Bit	SOJ(300), ZIP SOJ(350), TSOP	-6,-7,-8,-10	—	—	'91/1
M5M44800AJ,L,TP,RT	512K×8, Fast Page	SOJ(400), ZIP(400) TSOP(400)	-6,-7,-8,-10	YES	'91/2	'91/4
M5M44900AJ,L,TP,RT	512K×9, Fast Page	ditto	ditto	YES	'91/7	'91/10
M5M44260AJ,(L),TP,RT	256K×16, Fast Page (2CAS, 1W)	SOJ(400), TSOP(400) (ZIP(475))	-8,-10 (-6,-7)	YES	'91/2	'91/4
M5M44170AJ,(L),TP,RT	256K×16, Fast Page (1CAS, 2W)	ditto	-6,-7,-8,-10	YES	'91/2	'91/4
M5M44280AJ,(L),TP,RT	256K×18, Fast Page (2CAS, 1W)	ditto	-8,-10 (-6,-7)	YES	'91/7	'91/10
M5M44190AJ,(L),TP,RT	256K×18, Fast Page (1CAS, 2W)	ditto	-6,-7,-8,-10	YES	'91/7	'91/10

- Organization (X1/X4) ----- Wire Bonding option
- Fast Access Mode (Fast Page/Nibble/Static Column) ----- Wire Bonding option
- Write Per Bit Function (With/Without) ----- Wire Bonding option
- TSOP Package (Type II) ----- Normal bend type (TP) & Reverse bend type (RT)
- X8/X16 . . . Metal mask option
- X9/X18 . . . Metal mask option



## Spec. Comparison between 1st and 2nd Generation 4MDRAM

Spec.	Gen.	1st Generation	2nd Generation
Organization		×1,×4 (AI Masterslice)	×1,×4 (Bonding option)
Package		350mil SOJ 400mil ZIP	350mil SOJ 300mil SOJ 400mil ZIP 300mil TSOP (II)
Access Time		80/100ns	60/70/80/100ns
Power Supply Current	Operating	95/85mA	100/85/75/65mA
	Stand - by	2mA (TTL) 1mA (MOS)	2mA (TTL) 1mA (MOS)
Fast Access Mode		Fast Page Nibble (×1 Only) Static Column (Bonding Option)	Fast Page Nibble (×1 Only) Static Column (Bonding Option)
Write Per Bit Function (×4 Only)		No	Yes (Bonding Option)
Test Mode		8-bit Parallel	16-bit Parallel
Low Power Version Refresh Current (t <sub>ref</sub> =128ms)		Yes 500 μA	Yes 200 μA*

\*: Target Spec.

## Comparison of 4M DRAM Design Technology

	1st Generation	2nd Generation
Chip Size	102mm <sup>2</sup>	77.5mm <sup>2</sup>
Memory Cell Size	12.3 μm <sup>2</sup>	9.0 μm <sup>2</sup>
Minimum Feature Size	0.8 μm	0.7 μm
Inter-Connection Layer	Metal:1 (Word Line) Poly-silicon:3 (Tr. Cell Capacitor) Poly-cide:1 (Bit Line)	Metal : 2 (Word Line, Column Select Line) Poly-silicon : 3 (Tr., Cell Capacitor) Poly-cide : 1 (Bit Line)
Partial Activation	1/4	1/8
Memory Cell/Bit Line	128	64
Redundancy	8 Rows, 8 Columns	32 Rows, 16 Columns
Metal Masterslice	×1/×4	—
Wire Bonding Option	Fast Access Mode SOJ/ZIP	×1/×4 Fast Access Mode Write Per Bit SOJ&TSOP/ZIP

## Comparison Process Design between 1st and 2nd Generation 4MDRAM

	1st Generation	2nd Generation
Isolation	Single Locos	Single Locos
Well	Twin-well	Twin-well
Cell structure	Stacked Tox (eff) = 100 Å	Stacked Tox (eff) = 80 Å
Transistor	Nch : 0.9 μm(LDD) Pch : 1.1 μm(S.W)	Nch : 0.8 μm(LDD) Pch : 1.0 μm(LDD)
1st Poly-Si	Transistor(Poly-Si) Tox = 200 Å	Transistor(Poly-Si) Tox = 180 Å
2nd Poly-Si	Storage Node	Storage Node
3rd Poly-Si	Capacitor(Poly-Si) Tox (eff) = 100 Å	Capacitor(Poly-Si) Tox (eff) = 80 Å
4th Poly-Si	Bit line WSi <sub>2</sub> /Poly-Si	Bit line WSi <sub>2</sub> /Poly-Si
1st Metal layer	Word line Pile Al-Si-Cu/TiN	Word line Pile Al-Si-Cu/TiN
2nd Metal layer	None	Column Select line Al-Si-Cu/TiN
Passivation	P-SiN	P-SiN
Coating	Polyimide (10 μm)	Polyimide (10 μm)

## Comparison between 1st and 2nd Generation 4M DRAM -SOJ/ZIP Package-

	1st	2nd
Plastic material	Epoxy-resin	same
Lead frame material	Fe-Ni 42 Alloy	same
Die attach	Soft solder	same
Wire bonding material	Au 30 μm φ	same
Wire bonding method	Thermosonic	same
Lead frame finish	Sn/Pb plating	same
α Flux of Plastic material	<0.001 CpH	same
Marking	Ink	Laser

## 2nd Generation 4M DRAM Thermal Resistance

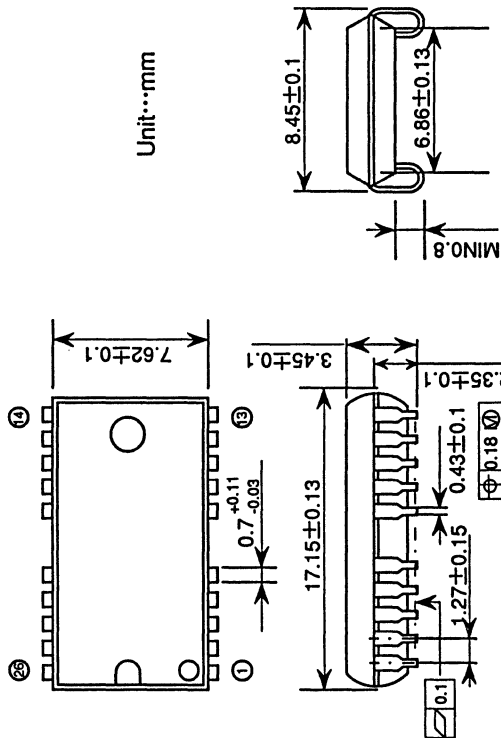
Package Type	$\theta_{JA}$ ( $^{\circ}\text{C}/\text{W}$ )			$\theta_{JC}$ ( $^{\circ}\text{C}/\text{W}$ )
	Hanging	Mounted on standard PCB		
	0 (f/m)	0 (f/m)	200 (f/m)	In Fluorinert Liquid
SOJ (300mil)	95	75	55	16
SOJ (350mil)	90	75	55	16
ZIP (400mil)	85	70	50	16
TSOP (Type II)	120	85	70	16

Note

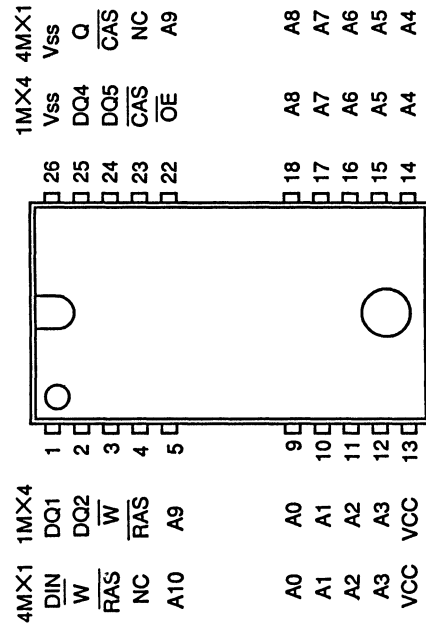
- (1) Standard PCB
  - Material .....glass epoxy(one side face Cu Pattern)
  - Size.....70mmX70mm,1.6mm(thickness)
  - Cu thickness...18  $\mu\text{m}$
- (2) f/m...feet/minute  
(200f/m=1m/s)

### 26Pin 300mil SOJ for 4MX1 and 1MX4DRAM

Outline Drawing

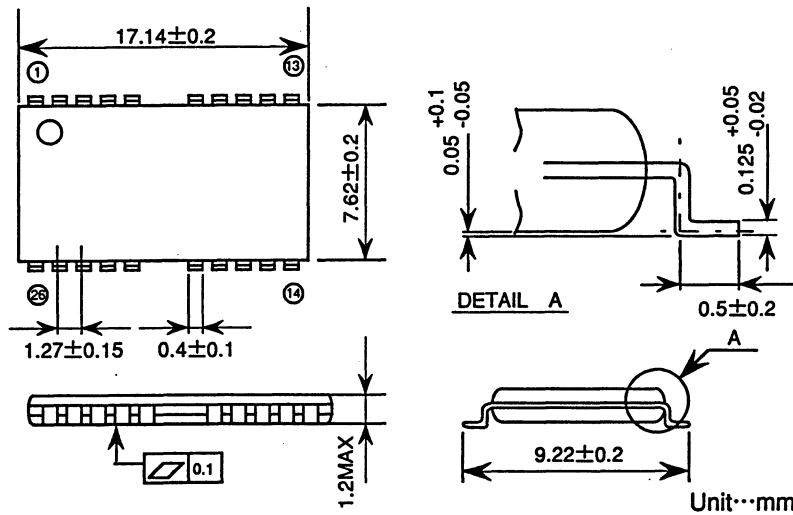


Pin Configuration (Top View)

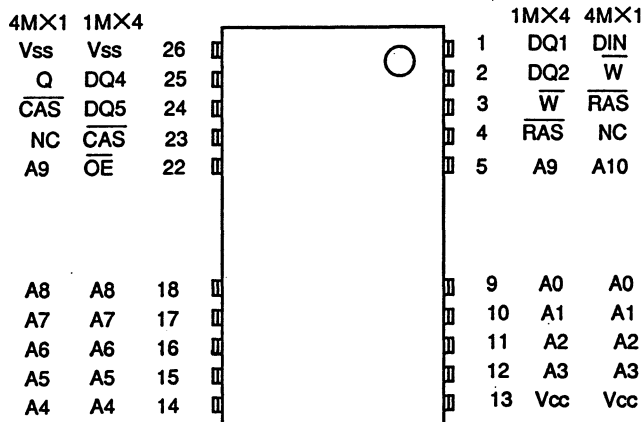


26Pin TSOP for 4M×1 and 1M×4 DRAM  
(Reverse Bend Type)

Outline Drawing

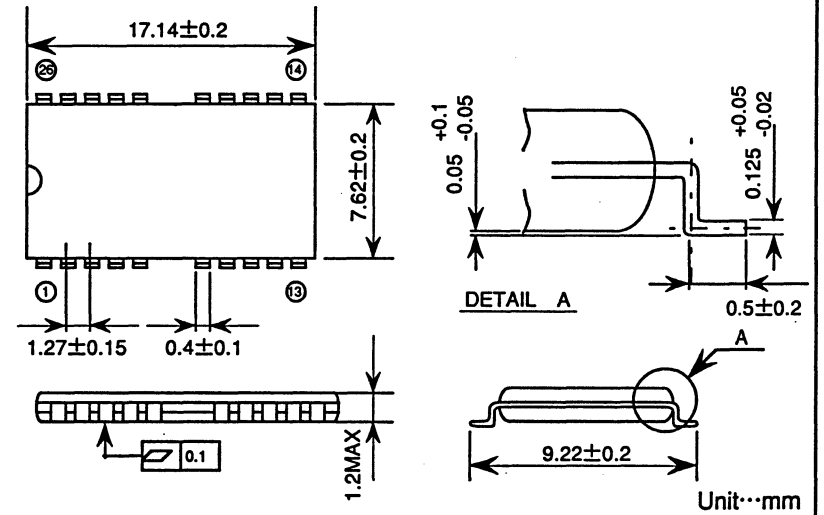


Pin Configuration (Top View)

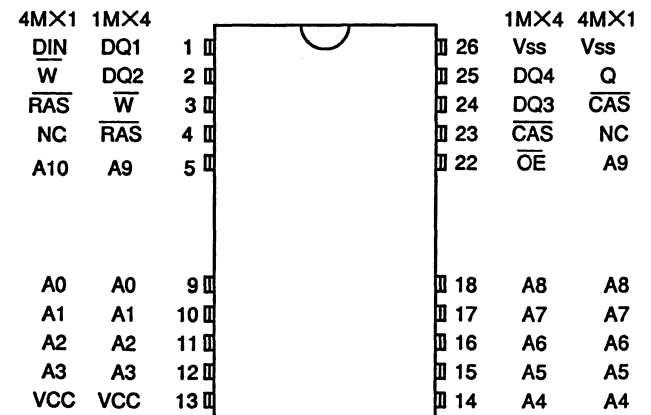


26Pin TSOP for 4M×1 and 1M×4 DRAM  
(Normal Bend Type)

Outline Drawing



Pin Configuration (Top View)





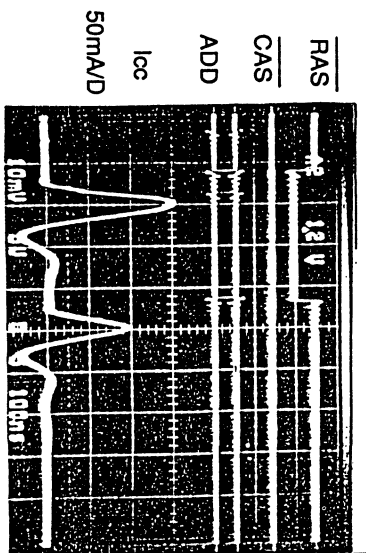
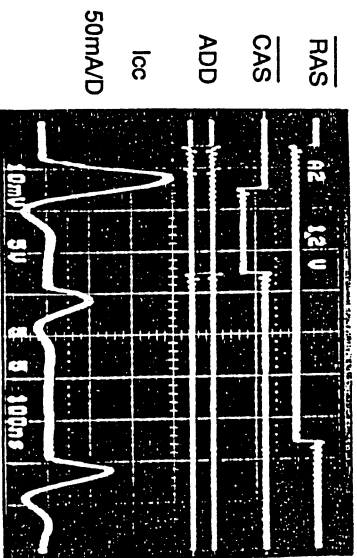
## Electrical Characteristics of 2nd Generation 4MDRAM

### SUMMARY (for 80ns device)

Electric Characteristics	Data Mean	Sigma	Limit	Test Condition
lcc1	62.5mA	0.65	75mA	V <sub>cc</sub> =5.5V, T <sub>c</sub> =160ns, T <sub>a</sub> =25° C
lcc2(MOS)	55.5 μA	3.10	1.0mA	V <sub>cc</sub> =5.5V, T <sub>a</sub> =25° C
lcc2(TTL)	1.12mA	0.02	2.0mA	ditto
lcc3	62.9mA	0.61	75mA	V <sub>cc</sub> =5.5V, T <sub>c</sub> =160ns, T <sub>a</sub> =25° C
lcc4	62.6mA	1.26	75mA	V <sub>cc</sub> =5.5V, T <sub>c</sub> =50ns, T <sub>a</sub> =25° C
TRAC	61.9ns	1.22	80ns	V <sub>cc</sub> =4.5V, T <sub>a</sub> =80° C
TCAC	11.8ns	0.23	20ns	ditto
TAA	34.0ns	0.90	40ns	ditto
TRAH	3.8ns	0.12	10ns	ditto
TASR	-4.8ns	0.12	0ns	V <sub>cc</sub> =5.5V, T <sub>a</sub> =25° C
TCAH	8.9ns	0.21	15ns	V <sub>cc</sub> =4.5V, T <sub>a</sub> =80° C
TASC	-7.8ns	0.16	0ns	V <sub>cc</sub> =5.5V, T <sub>a</sub> =25° C
TRP	26.1ns	0.51	70ns	V <sub>cc</sub> =4.5V, T <sub>a</sub> =80° C
TREF(Pause)	507.5ms	136.4	16.4ms	V <sub>cc</sub> =5.5V, T <sub>a</sub> =80° C
TREF(Disturb)	372.6ms	104.7	16.4ms	ditto

Sample Size=20pcs


### Power Supply Current Waveforms of 2nd Generation 4MDRAM




**MITSUBISHI ELECTRIC**  
**RELIABILITY TEST RESULT of 300mil SOJ**  
**2nd Generation 4MDRAM**

TESTING ITEM	CONDITION	CHECKING ITEM	FAILURES SAMPLE SIZE	
			X1	X4
High temperature operating life test	Ta=125°C Vcc=7.5V t=1000hrs	Function and DC Stability of electrical margins	$\frac{0}{72}$	$\frac{1^{*1}}{284}$
	Ta=150°C Vcc=7.5V t=1000hrs	Function and DC Stability of electrical margins	$\frac{0}{36}$	$\frac{0}{72}$
Low temperature operating life test	Ta=-20°C Vcc=8.0V t=1000hrs	Function and DC Stability of electrical margins	$\frac{0}{30}$	$\frac{0}{30}$
High temperature storage test	Ta=175°C t=1000hrs	Function and DC Stability of electrical margins	$\frac{0}{52}$	$\frac{0}{160}$
Temperature cycling test	-65/150°C 1000cycles	Function and DC	$\frac{0}{68}$	$\frac{0}{125}$
Thermal shock test	-55/125°C 1000cycles	Function and DC	$\frac{0}{25}$	$\frac{0}{50}$
Soldering heat test	260°C 10sec	Function and DC	$\frac{0}{50}$	$\frac{0}{50}$
Humidity test with DC bias	85°C 85%RH Vcc=5.5V t=2000hrs	Function and DC Stability of electrical margins	$\frac{0}{36}$	$\frac{0}{65}$
Pressure cooker test with DC bias	140°C 85%RH Vcc=5.5V t=1000hrs	Function and DC Stability of electrical margins	$\frac{1^{*2}}{36}$	$\frac{1^{*3}}{135}$
Pressure cooker test	121°C 100%RH t=240hrs	Function and DC Stability of electrical margins	$\frac{0}{64}$	$\frac{0}{96}$

\*1:Single bit failure \*2,3:DC failure


**MITSUBISHI ELECTRIC**

**RESULTS OF INFANT MORTALITY STUDY for**  
**2nd Generation 4MDARM**



Sample	Condition	Sample size	Failures
M5M44400AJ	Dynamic burn-in Ta=125°C Vcc=7.5V t=100 hours	2.653	<div style="display: flex; align-items: center;"> <div style="font-size: 2em; margin-right: 5px;">{</div> <div style="margin-right: 5px;">7</div> <div style="margin-right: 5px;">}</div> <div style="margin-right: 10px;">Single bit : 5</div> </div> <div style="margin-left: 10px;">Bit line : 2</div>

\* In case the field condition of Ta=55°C and Vcc=5.0V  
 $=7/(2.653 \times 10^3 \times 10^2 \times 2.970 \times 10^3)$   
 $=8.9FIT$

\* In case the field condition of Ta=70°C and Vcc=5.0V  
 $=7/(2.653 \times 10^3 \times 10^2 \times 1.702 \times 10^3)$   
 $=15FIT$



## MITSUBISHI BYTE WIDE DRAMs

Specifications for BYTE WIDE 4M DRAM are not final. Some specifications are subject to change.

1. 512K×8/×9

2. 256K×16/×18

(Note)

2  $\overline{\text{CAS}}$ , 1 $\overline{\text{W}}$  ..... FOR COMPUTERS

1  $\overline{\text{CAS}}$ , 2 $\overline{\text{W}}$  ..... FOR GRAPHICS

(Note)

Part number of 2  $\overline{\text{CAS}}$  type has been changed from M5M44160A to M5M44260A.



## 512K ×8/9 4Mbit DRAM Proposed Spec.

- Same Package : 512K×8 and 512K×9
- Fast Page Mode Support
- Refresh Period : 1024cycles/16ms  
(Refresh Address : A9~A0)
- Package : 28pin 400mil SOJ  
28pin 400mil ZIP  
28pin 400mil TSOP TypeII

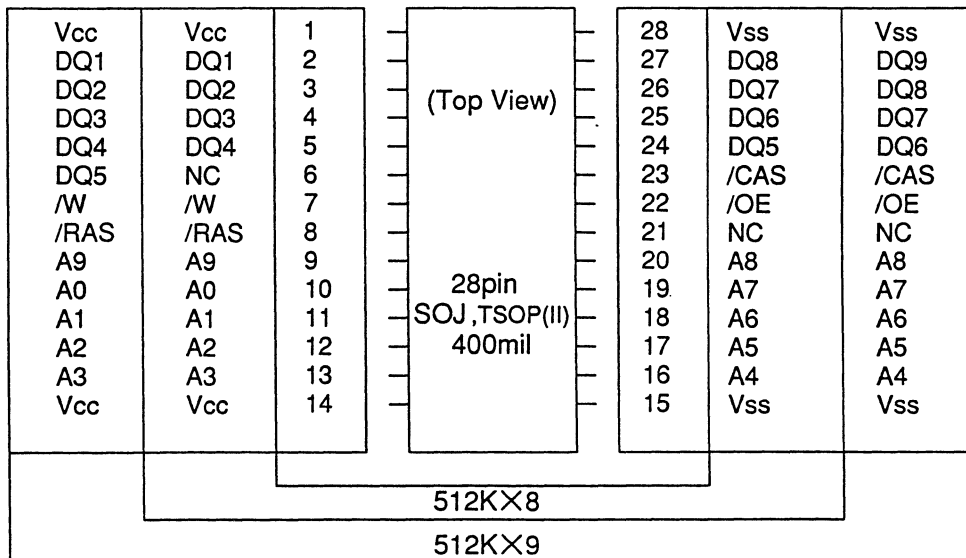


## 512K X8 4M DRAM Target Spec.

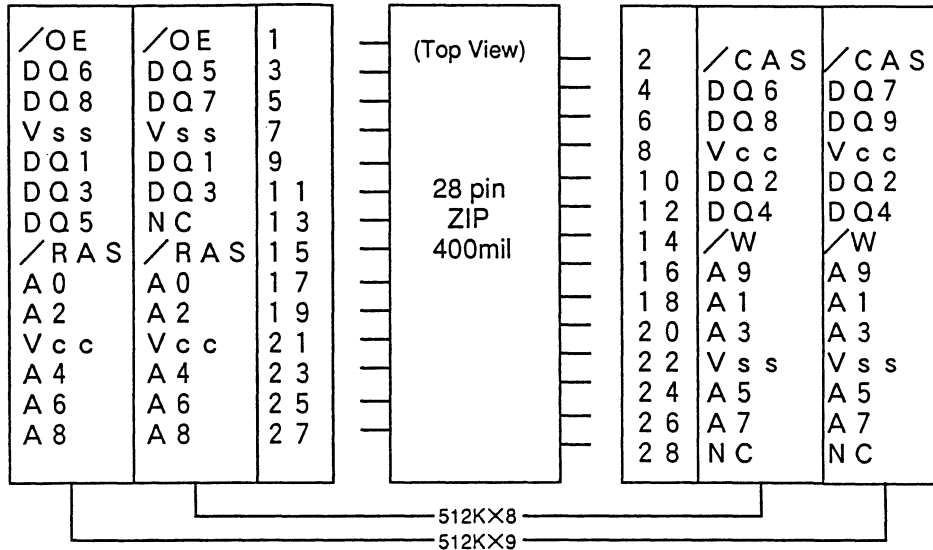
Access Time/Cycle Time	: 60ns/120ns, 70ns/140ns, 80ns/160ns, 100ns/190ns
Power Dissipation* (max)	Operating : 660mW, 550mW, 490mW, 413mW (120mA) (110mA) (90mA) (75mA) Stand by : 5.5mW(1mA)
Fast Access Mode	: Fast Page Mode
Refresh Cycle	: 1024cycles /16ms (Refresh Address A9~A0)
Package	: 28pin 400mil SOJ 28pin 400mil ZIP 28pin 400mil TSOP(II)
Technology	: Based on 2nd Generation 4M DRAM chip Twin-well CMOS 0.7 $\mu$ m minimum feature size Stacked cell structure Double Aluminum layers

\* Low power version with extended CBR refresh being considered.  
Icc8=250  $\mu$ A, Icc2=100  $\mu$ A, tREF=125  $\mu$ s

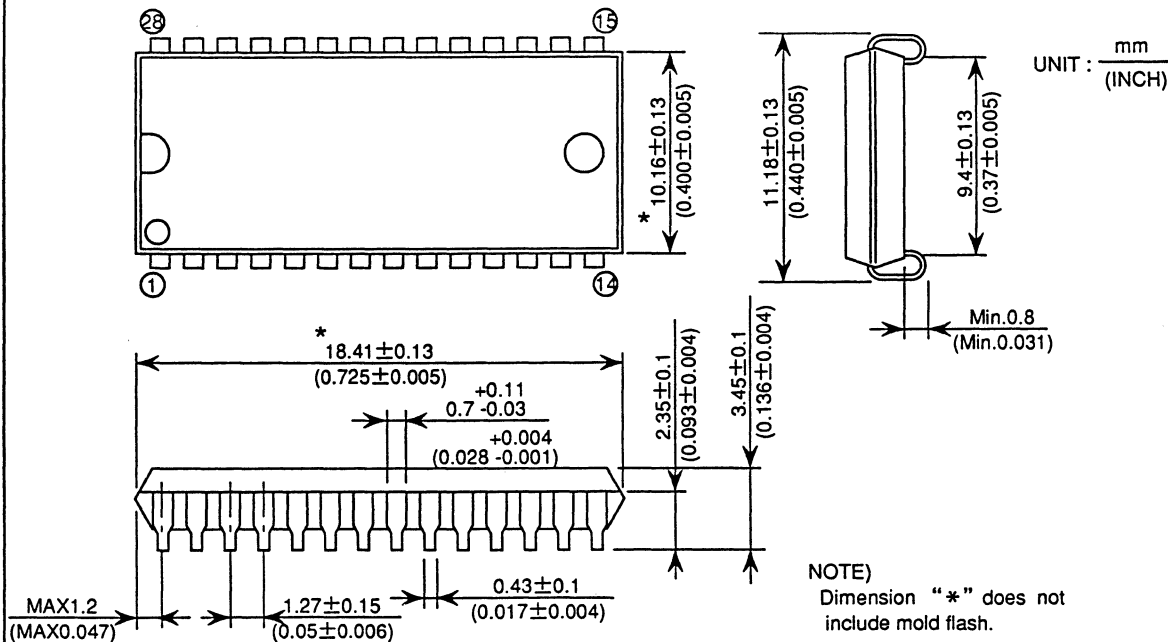
## 512K X8/9 4Mbit DRAM Pin Configuration



### 512KX8/9 4Mbit DRAM Pin Configuration

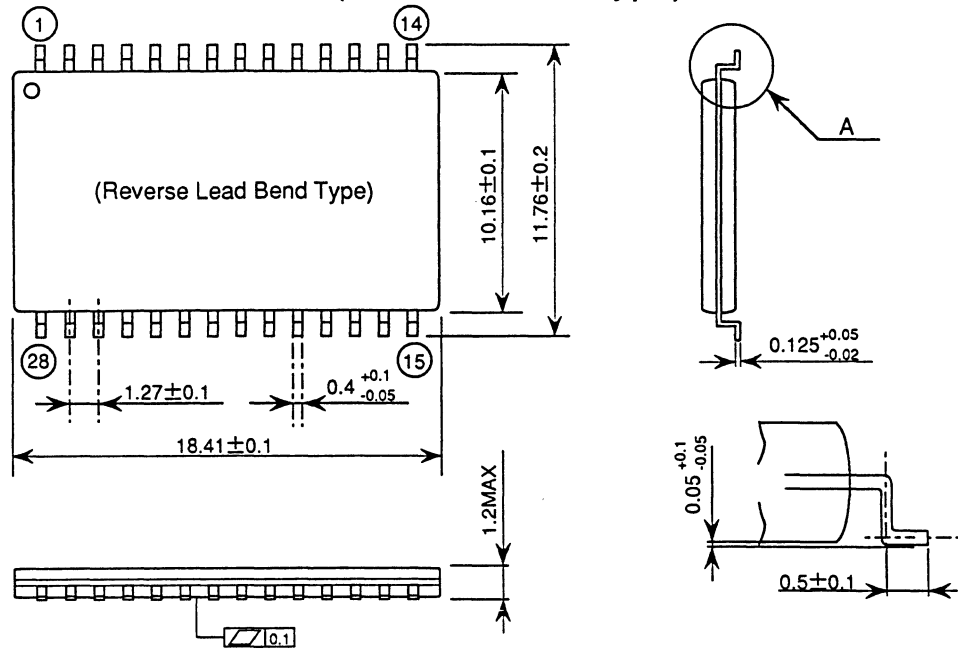


### 28Pin SOJ For 512KX8 DRAM





28pin TSOP(Typell) For 512KX8 DRAM  
(Reverse Bend Type)



256K X16/18 4MbitDRAM Proposed Spec

- Same Package : 256KX16 and 256KX18
- Byte and Word Operation
  - 2CAS,1W : Byte/Word Read,Byte/Word Write
  - 1CAS,2W : Word Read,Byte/Word Write
- Fast Page Mode Support
- Refresh Period
  - 2CAS,1W : 512cycles/8ms  
(Refresh Address : A8~A0)
  - 1CAS,2W : 1024cycles/16ms  
(Refresh Address : A9~A0)
- Package : 40pin 400mil SOJ  
44pin 400mil TSOP Typell



## 256K×16 4M DRAM Target Spec.

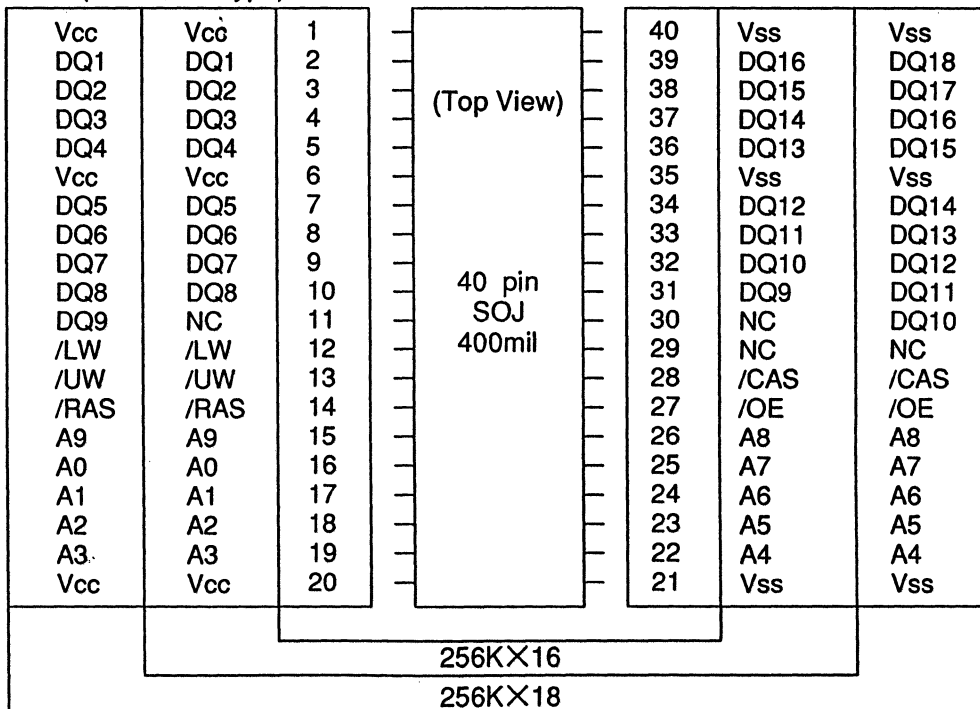
		M5M44260A *1) (2CAS,1W)	M5M44170A (1CAS,2W)
Access Time /Cycle Time (ns)		(60/120,70/140*),80/160,100/190	60/120,70/140,80/160,100/190
Power Dissipation (ma x)	Operating mW (mA)	{(1045, 908)*} 770, 660 (190, 165,) 140, 120	770, 660, 578, 495 (140, 120, 105, 90)
	Stand by mW(mA)	5.5(1.0)	5.5(1.0)
Refresh Cycle (Refresh Address)		512cycles/8ms (A8~A0)	1024cycles/16ms (A9~A0)
Package		40pin 400mil SOJ 44pin400mil TSOP(II)	
Technology		Same as 512K×8 4M DRAM	
Low Power Version Refresh Current(μA) (tc=125μs)		Yes 350	Yes 250

\*1) Depend on maximum allowable power dissipation

\*2) Part number of 2 CAS type has been changed from M5M44160A to M5M44260A

## 256K×16/18 4Mbit DRAM Pin Configuration

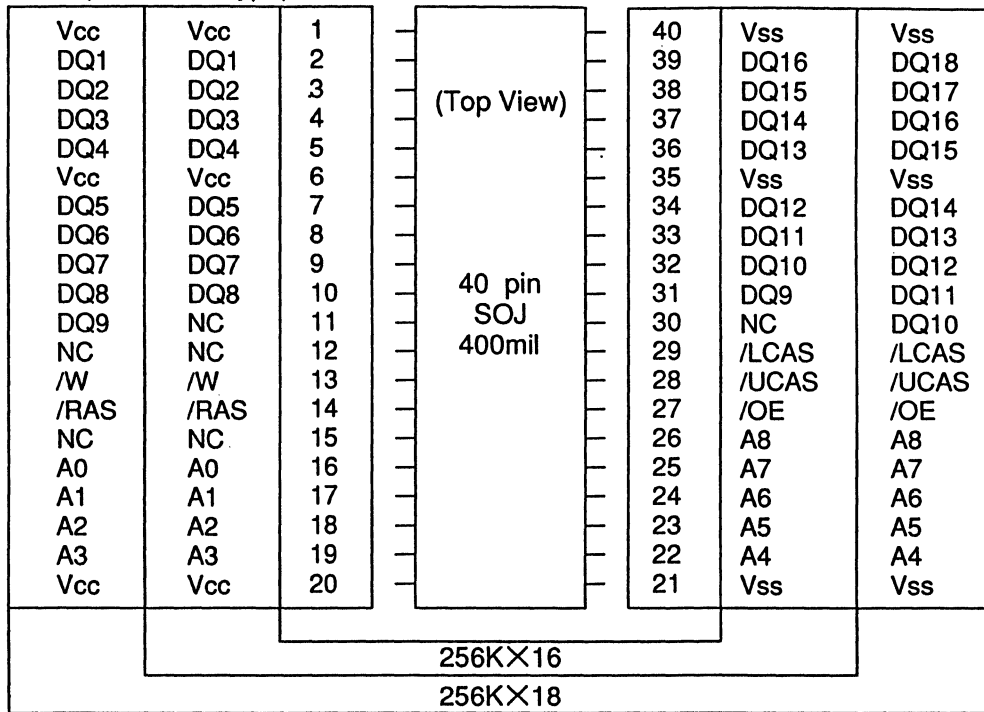
(1CAS,2W Type)





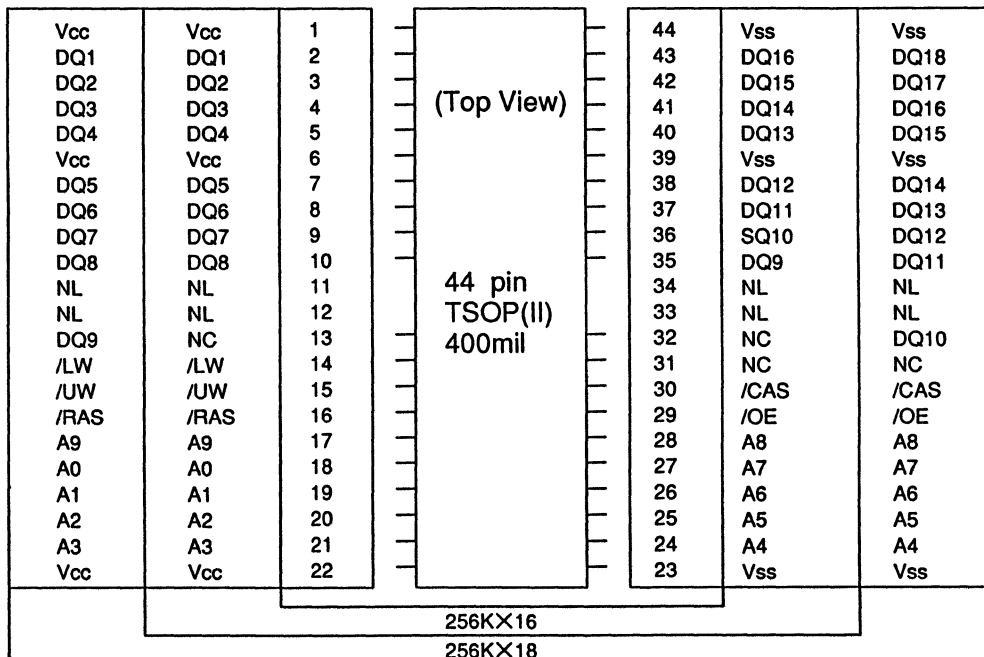
## 256K×16/18 4Mbit DRAM Pin Configuration

(2CAS,1W Type)



## 256K×16/18 4Mbit DRAM Pin Configuration

(1CAS,2W Type)

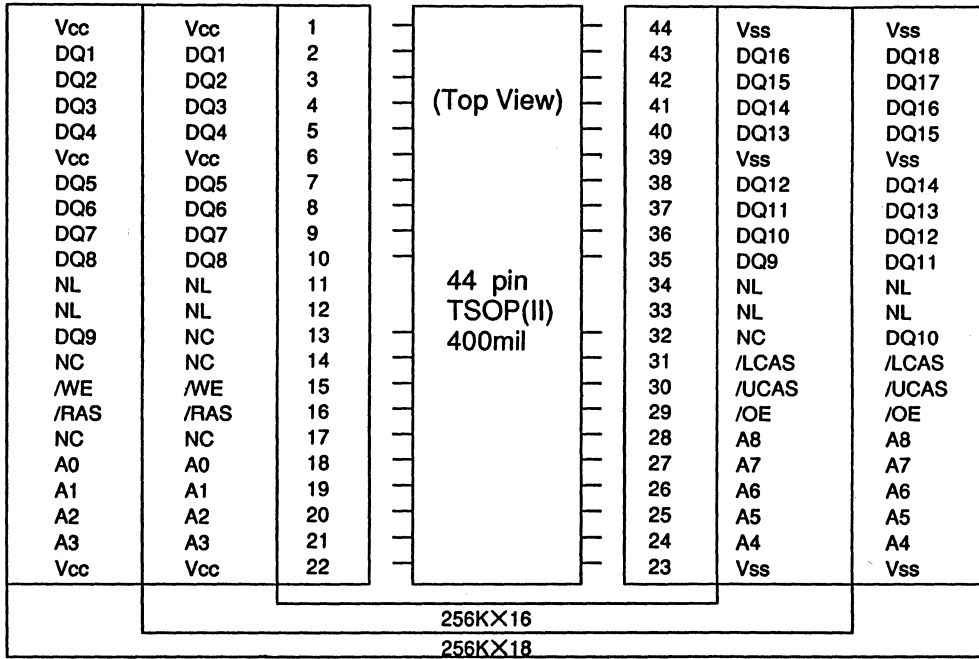


NL=NO LEAD

# 256K×16/18 4Mbit DRAM Pin Configuration



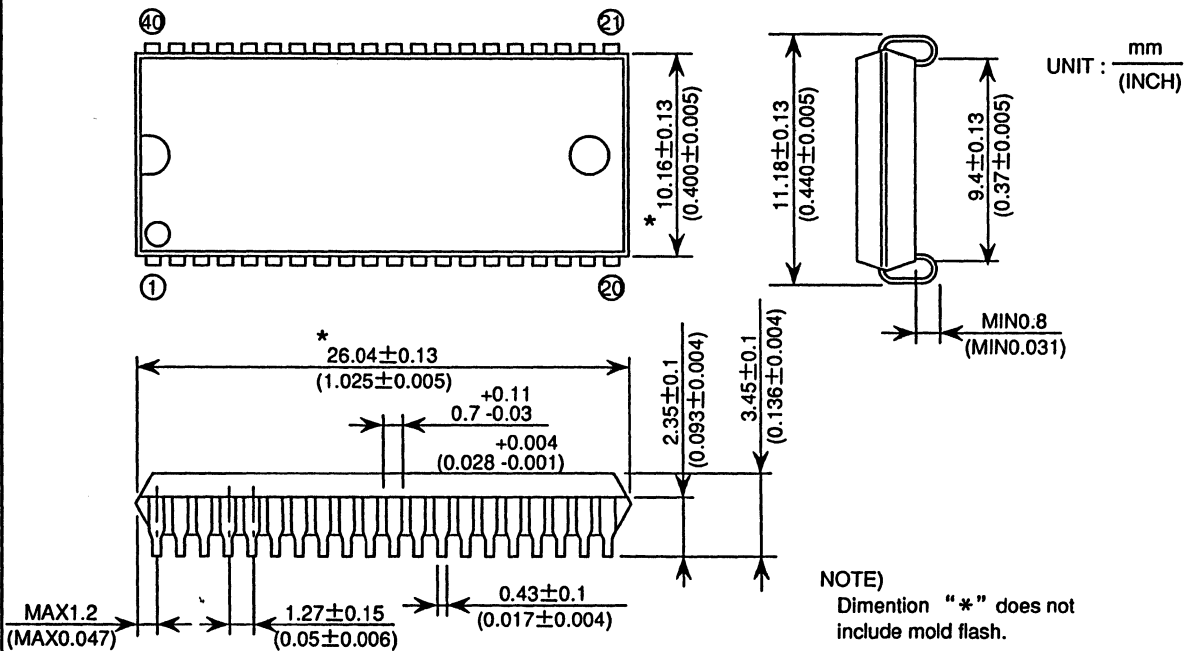
(2CAS,1W Type)



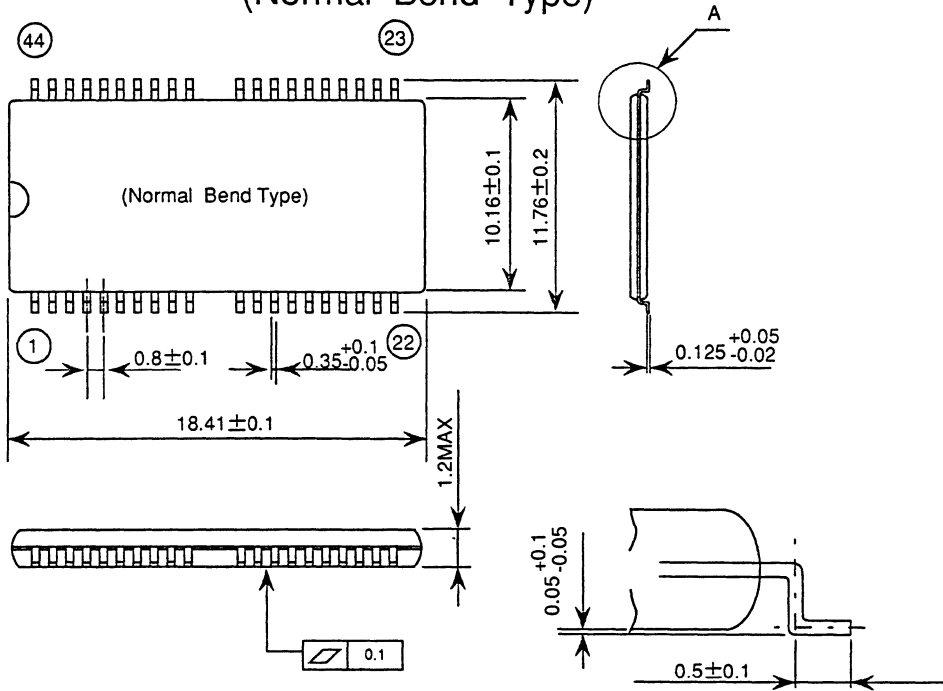
NL=NO LEAD

Advanced Information

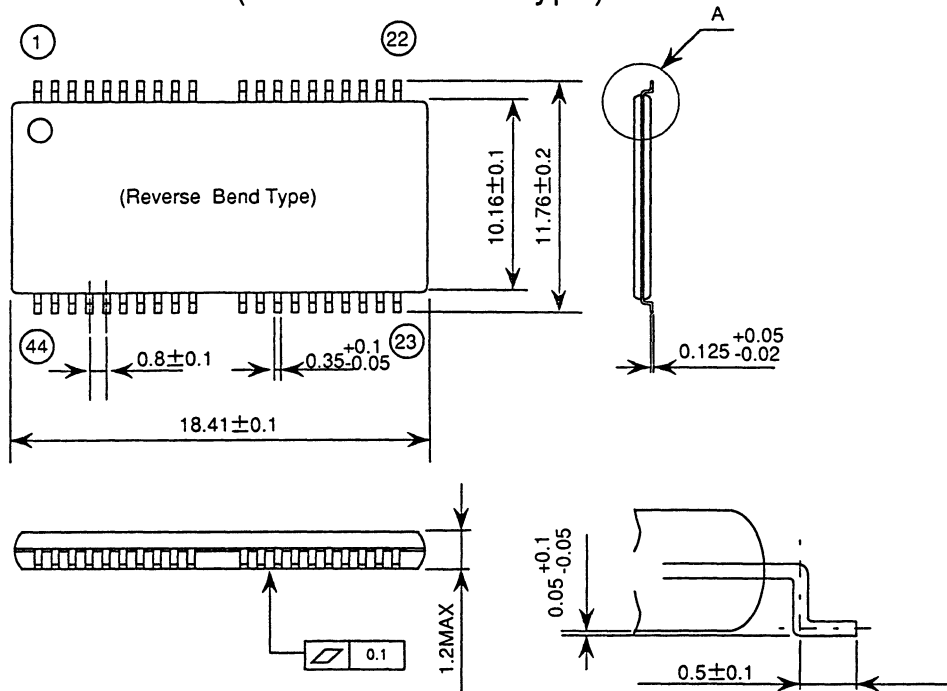
## 40Pin SOJ For 256K×16 DRAM



44pin TSOP (TypeII) For 256K×16DRAM  
(Normal Bend Type)



44pin TSOP (TypeII) For 256K×16 DRAM  
(Reverse Bend Type)





## 4M SILICON FILE

- 1.Ultra Low Power ; Battery Drive / Back Up
- 2.4Mx1 / 1Mx4
- 3.Pin Compatible with Existing Standard 4M
- 4.Fast Access Time
- 5.Fast Page Mode Support
- 6.Entering into Self Refresh Mode by RAS Clock Toggling at Slow Frequency



## 4M SILICON FILE TARGET SPEC

4Mx1 /1Mx4	26pin 300mil SOJ
Power Dissipation	I <sub>cc 1</sub> =90mA (t <sub>c</sub> =160ns) I <sub>cc 2</sub> =0.5mA
Ultra Low Self Refresh Current	I <sub>cc 8</sub> = 30 μA(T <sub>a</sub> =50°C ) 60 μA(T <sub>a</sub> =60°C ) 120 μA(T <sub>a</sub> =70°C )
Fast Access	t <sub>RAC</sub> /t <sub>C</sub> =80ns / 160ns t <sub>CAA</sub> =40ns t <sub>CAC</sub> /t <sub>PC</sub> =20ns / 50ns (Fast Page)
Refresh	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh, $\overline{\text{RAS}}$ only Refresh Hidden Refresh
Normal Refresh	1024 cycles / 32ms
Sample	1992 / M



### 4M SILICON FILE Self Refresh

- RAS clock Toggling by Maintaining  $\overline{\text{CAS}}$  Low to Stabilize Substrate Voltage
- Different from Existing  $\overline{\text{RAS}} = \overline{\text{CAS}} = \text{Low}$  Self Refresh
- Power Dissipation / pcs Consumed by  $\overline{\text{RAS}}$  Clock Generator is Small
- Ideal to the Systems where Low Power is Essential at Data Hold Period

Battery Drive, Battery Back UP

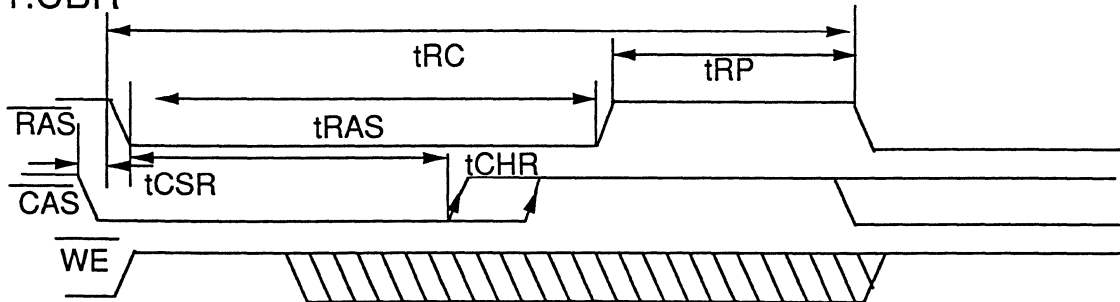
- Development of the DRAM controller being Considered.

MPU : 80286, 80386SX

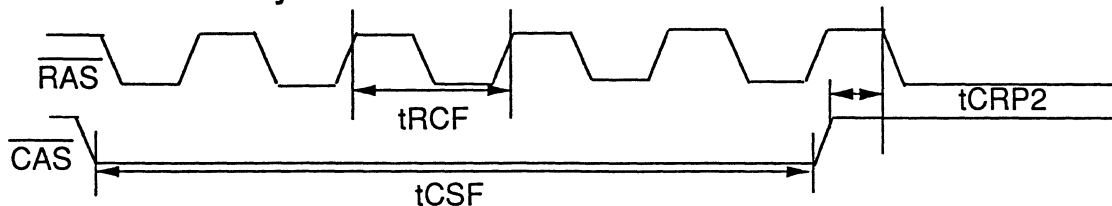


### 4M SILICON FILE Refreshing

#### 1.CBR



#### 2. Self Refresh Cycle



$t_{RCF} = 32 \mu s$	$T_a = 50 \text{ }^\circ\text{C}$
$16 \mu s$	$60 \text{ }^\circ\text{C}$
$8 \mu s$	$70 \text{ }^\circ\text{C}$

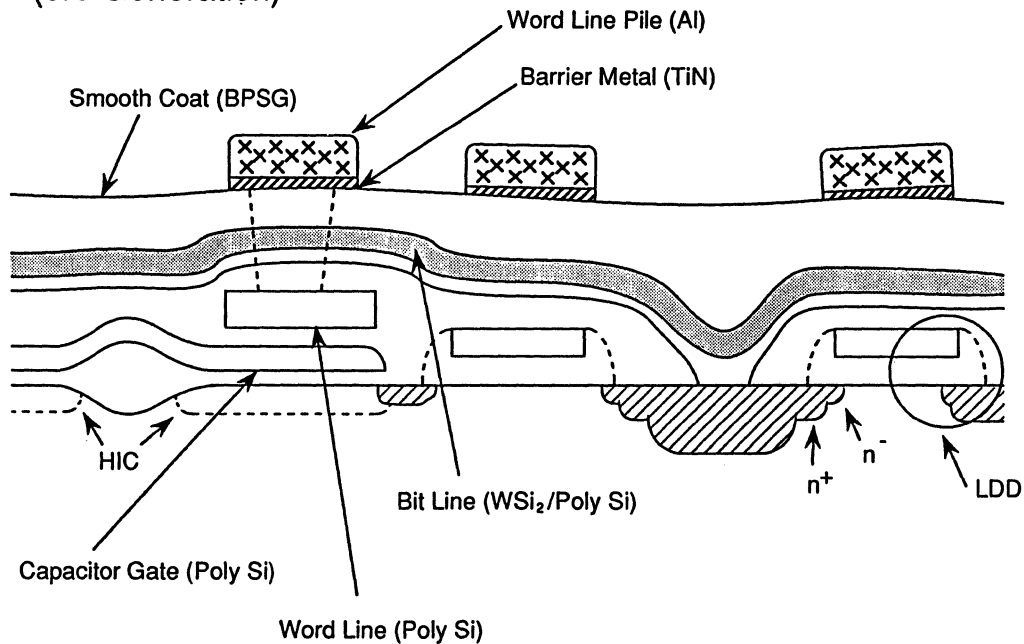
## SPEC of 3rd Generation 1M DRAM

( M5M41000B )  
( M5M44256B )

- |                          |                   |   |                     |
|--------------------------|-------------------|---|---------------------|
| <input type="checkbox"/> | Organization      | X1, X4 (Al-mask masterslice)  | } bonding<br>Option |
| <input type="checkbox"/> | Optional Function | Fast Page<br>Nibble (only X1)<br>Static Column<br>Write per bit (only X4) |                     |
| <input type="checkbox"/> | Characteristics   | Access time 70ns/80ns (/100ns)<br>80mA/70mA (/60mA)                       |                     |
| <input type="checkbox"/> | Chip Size         | 44.2mm <sup>2</sup>   |                     |

## Memory Cell Structure of 1M DRAM

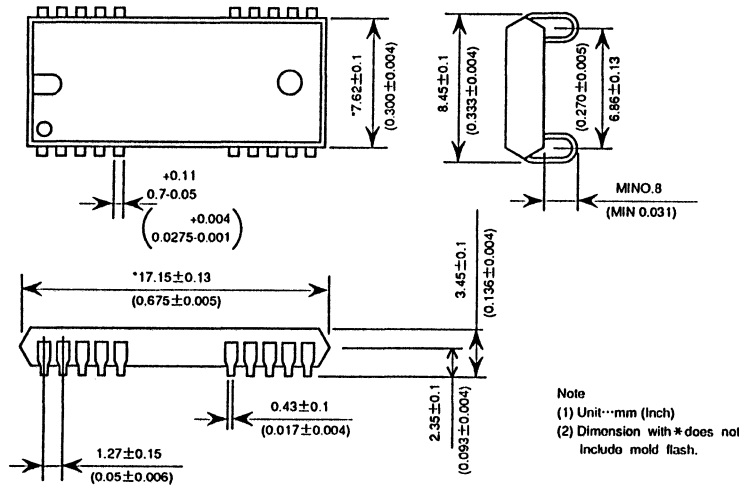
(3rd Generation)



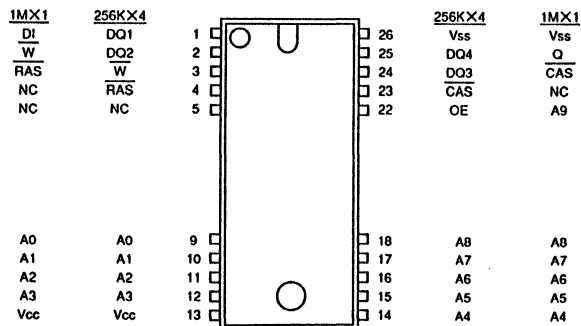


### 26Pin SOJ for 1M×1 & 256K×4

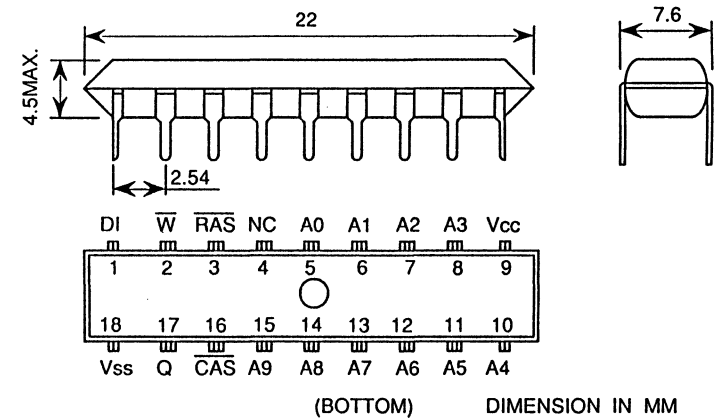
#### Outline Drawing (Final)



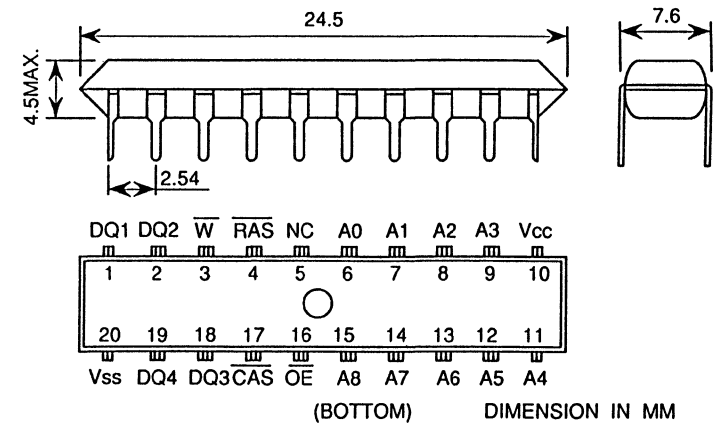
#### Pin Configuration



### PACKAGE DIMENSION and PIN CONFIGURATION OF 1M×1 DRAM



### PACKAGE DIMENSION and PIN CONFIGURATION OF 256K×4 DRAM



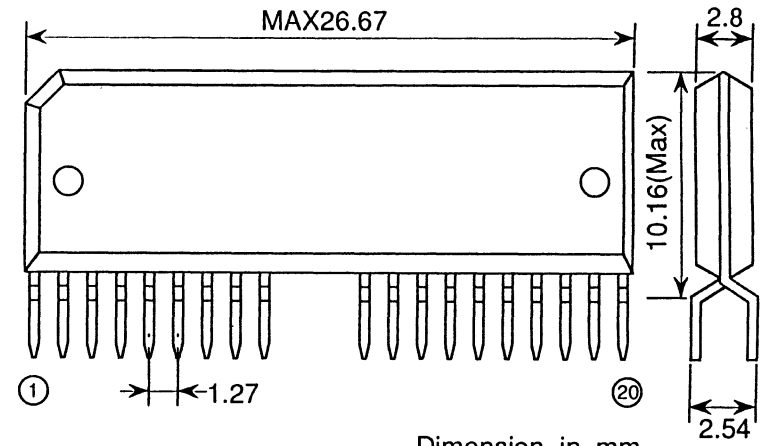


Comparison between P-DIP, SOJ and ZIP for M5M41000A and M5M41000B

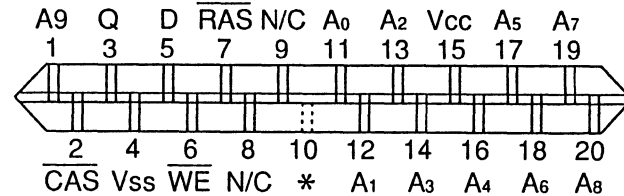
Package	P-DIP	SOJ	ZIP
Pin number	18 (20*)	20	20
Plastic material	Epoxy - resin	Same	Same
Lead frame material	Fe - Ni 42alloy	Same	Same
Die attach	Soft solder	Same	Same
Wire bonding material	Au 30 μm φ	Same	Same
Wire bonding method	Thermosonic	Same	Same
Lead frame finish	Sn/Pb plating	Same	Same
α Flux of plastic material	<0.001 CpH	Same	Same

\* : M5M44256A and M5M44256B

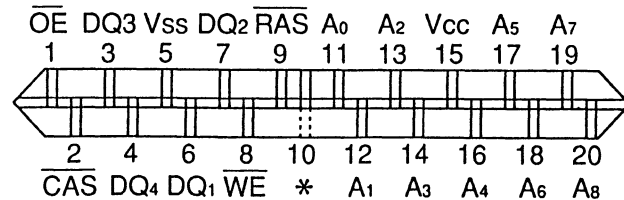
Package dimension and pin configuration (Bottom view) of 20 pin ZIP



M5M41000BL (1M×1 DRAM)



M5M44256BL (256K×4 DRAM)



Note : \* means no lead

1M DRAM DIP,SOJ,ZIP,TSOP  
Thermal Resistance (3rd generation)

1. 1M×1 (CMOS)

Package Type	Package Name	$\theta_{JA}$ (°C/W)			$\theta_{JC}$ (°C/W) In fluorinert liquid
		Hanging	Mounted on standard PCB		
		0 (f/m)	0 (f/m)	200 (f/m)	
DIP	18P4 Y	100	76	60	19
SOJ	26P0 J	113	81	64	18
ZIP	20P5 L	98	75	60	19
TSOP	24P3 B	150	94	74	17

2. 256K×4

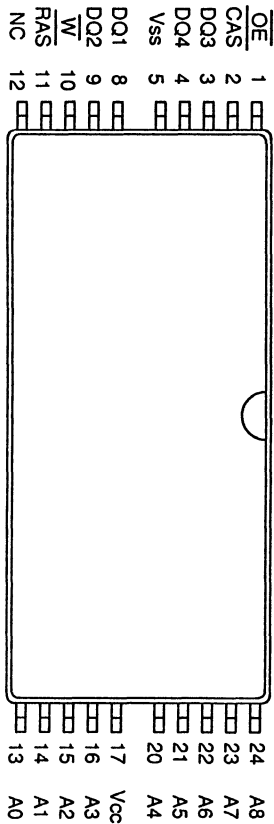
Package Type	Package Name	$\theta_{JA}$ (°C/W)			$\theta_{JC}$ (°C/W) In fluorinert liquid
		Hanging	Mounted on standard PCB		
		0 (f/m)	0 (f/m)	200 (f/m)	
DIP	20P4 Y	96	74	59	19
SOJ	26P0 J	113	81	64	18
ZIP	20P5 L	98	75	60	19
TSOP	24P3 B	150	94	74	17

Note

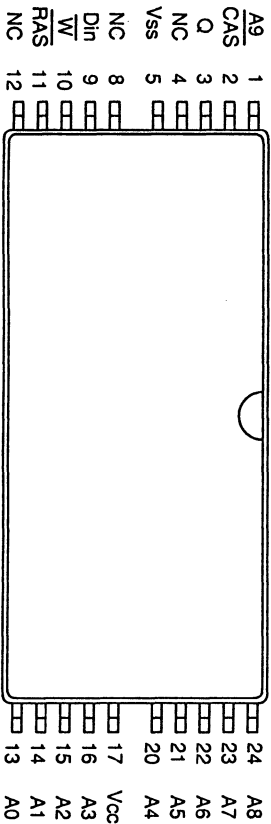
- (1) Standard PCB  
Material...glass epoxy (one side face Cu pattern)  
size...70mm×70mm,1.6mm (thickness)  
Cu thickness...18 μm
- (2) f/m...feet/minute  
(200f/m=1m/s)

Pin configuration (Top view) of 256K×4 & 1M×1DRAM TSOP

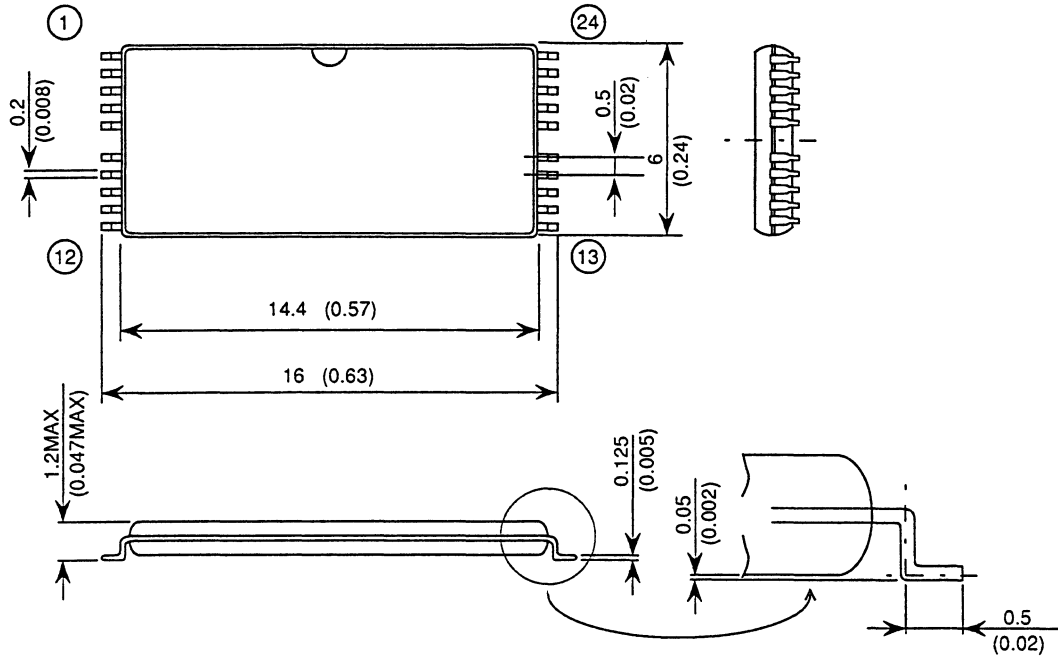
1. 256K×4 (M5M44256BVP,M5M44266BVP)



2. 1M×1 (M5M41000BVP)



### Dimension of 24pin TSOP



Unit ... mm (inch)

### Comparison of TSOP and SOJ package for 1M DRAM

Items		TSOP	SOJ
Package size	Plane(mm <sup>2</sup> )	16.0×6.0* (96.0)	17.15×8.45 (144.9)
	Height(mm)	1.2	3.45
Lead pitch (mm)		0.5	1.27
Standard memory Module 1M×9 (mm <sup>3</sup> )		88.9×25.4×2.54 (5735)	88.9×20.3×5.08 (9167)
Reliability		Care (Thermal Stress)	Very Good
Weight (g)		0.22	0.75
Production cost (Ratio)		1.1	1.0
Sample Schedule		Yes	Production

\*Need the chip - capacitor area

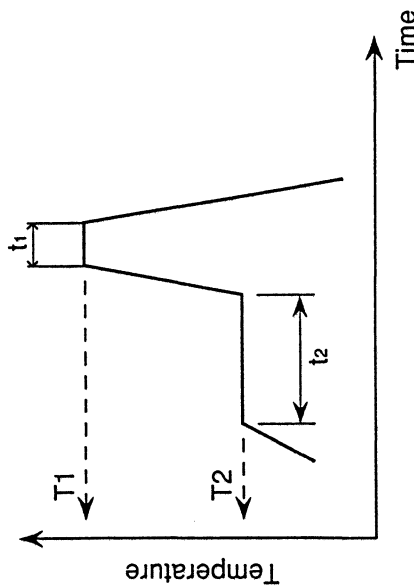
## Package Reliability in 1M DRAM

Test	Condition	Failures/Sample Size		
		DIP	ZIP	SOJ
Solderability	230°C , 5sec	0/10×5	0/10×5	0/10×5
Resistance To Solvent	Solvent (Acetone Isopropyl Alcohol Trichloroethane)	0/10×3	0/10×3	0/10×3
Lead Pull	230g , 30sec	0/10×3	0/10×3	0/10×3
Lead Bend	230g ,90°C, 3Times	0/10×3	0/10×3	0/10×3
Radiography	Check of Lead Frame Die Attach Au - Wire Resin Void	0/20×5	0/20×5	0/20×5
Salt Atmosphere	35°C , 5% , Solt 48 hours	0/10×3	0/10×3	0/10×3

### Recommendation For Solder Reflow

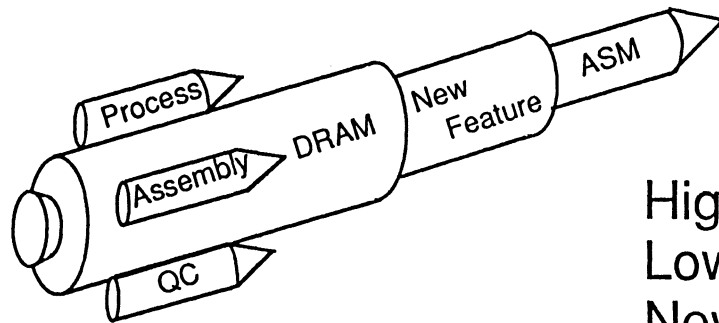
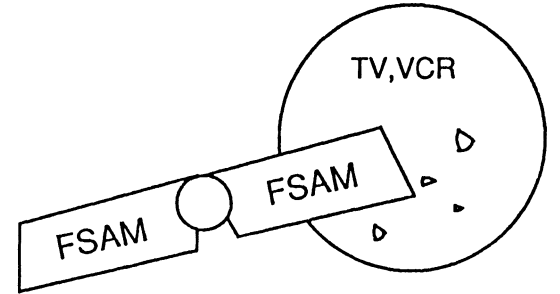
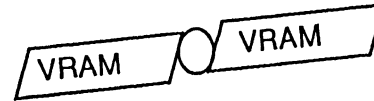
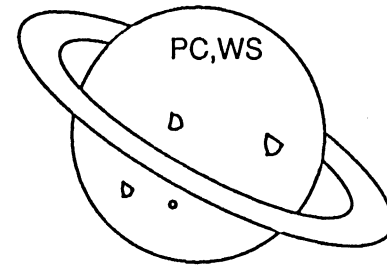
1. Baking before Solder Reflow  
Baking condition ; Ta = 125°C  
Duration = 20 ~ 24hrs

### 2. Temperature Profile of VPS



T1 : 215°C max.  
T2 : 150°C ±10°C  
t1 : 20sec max.  
t2 : approx. 2min.  
Slope = 1°C ~ 4°C/sec.

AS Memory



High Speed  
Low Power  
New Function  
Multi Bit

Video Memory

# 1M BIT DUAL - PORT DYNAMIC RAM 2nd Generation (A.ver)

## Design Concepts

- Based on the 256K VRAM Architecture
- High Speed      tRAC = 70nsMAX  
                              tSCC = 30nsMAX
- Low Power      CMOS
- Relaxed Real Time Transfer Timing  
    (Split SAM Architecture)
- High Performance
  - Flash Write (X4/X8)
  - Block Write (X4/X8)
- High Density Package
  - 28pin ZIP/SOJ (X4)
  - 40pin SOJ (X8)
- Productivity
  - Aluminum Master Sliced X4/X8
- High Quality
  - Based on the 1M DRAM (III)  
Process/Memory Cell

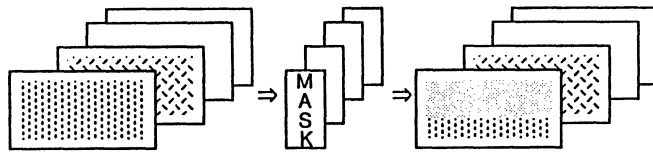


## 1M bit Dual Port DRAM Feature 2nd Generation (Aver.)

	M5M442256A	M5M482128A
RAM Size	256K X 4	128K X 8
SAM Size	512 X 4	256 X 8
Serial IN/OUT	YES	YES
Write per Bit	YES	YES
Split SAM	YES	YES
Flash Write	YES	YES
Block Write	YES	YES
Fast Page Mode	YES	YES
ZIP Package (400Mil)	YES (28 Pin)	-----
SOJ Package (400Mil)	YES (28 Pin)	YES(40 Pin)
DIP Package	-----	-----

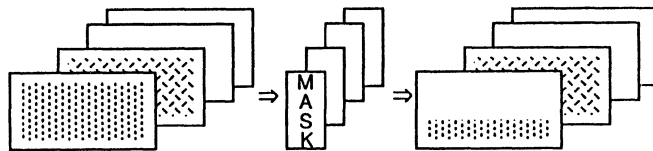
## Dual Port DRAM Feature

Write per bit



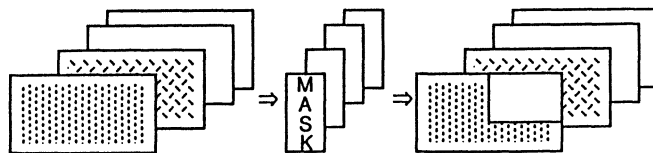
Masked Write

Flash Write



Fast Clear

Block Write



Window Clear



## M5M442256A 256K×4bit Dual Port DRAM

Feature

Dual Port RAM

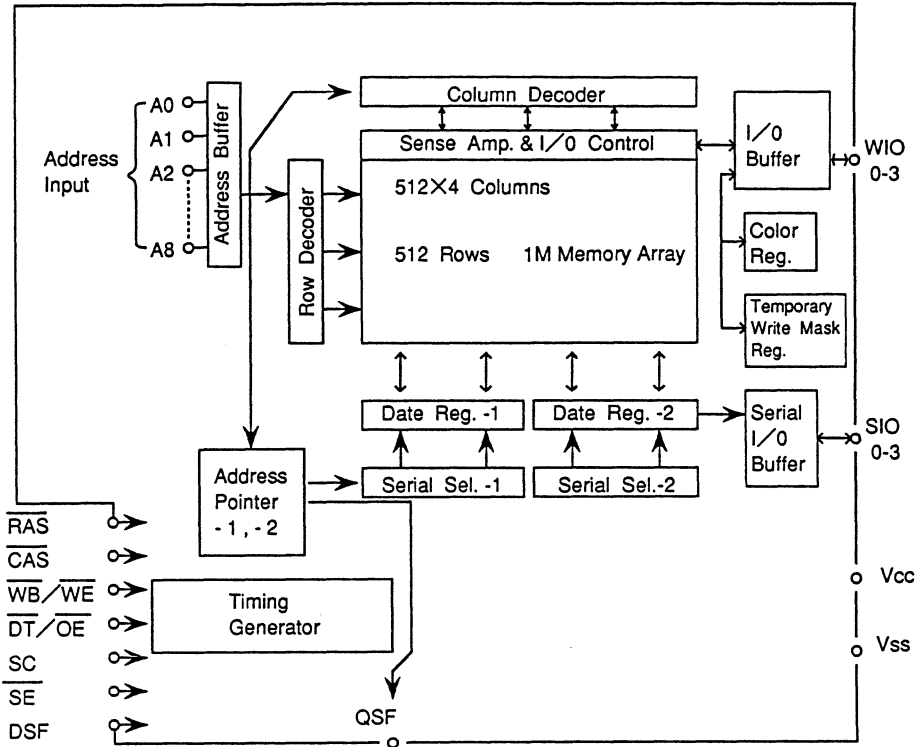
RAM Port 256K×4bit  
tRAC 70/80/100ns Max  
SAM Port 512×4bit  
tSCC 30/30/30ns Max

- Bi-directional Data Transfer between RAM and SAM
- Bi-directional SAM Port
- Addressable Start Pointer of SAM
- Fully Asynchronous Dual Port Accessibility
- Write per Bit Function
- Relaxed Real Time Data Transfer (Split SAM architecture)
- Flash Write Function
- Block Write Function
- Fast Page Mode, Hidden Refresh and CAS before RAS Refresh
- 512 cycle/8ms Refresh
- Low Power (CMOS)
 

RAM Port/SAM Port	100ns Ver.
Standby/Standby	5mA Max.
Active/Standby	60mA Max.
Standby/Active	35mA Max.
Active/Active	90mA Max.
- 28pin 400mil ZIP/SOJ

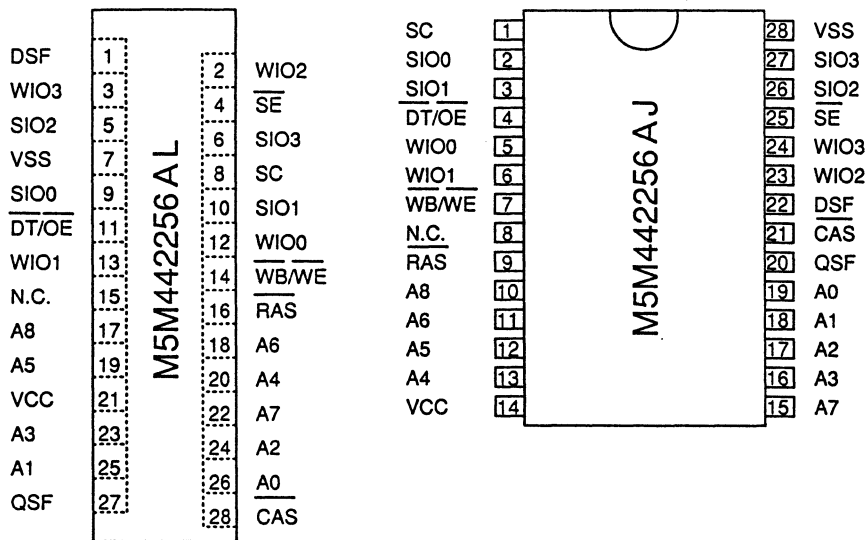
M5M442256 A

256KX4bit Dual Port DRAM BLOCK DIAGRAM



M5M442256 A

256KX4 BIT DUAL - PORT DRAM  
PIN CONFIGURATION



400mil 28pin ZIP  
28P5L

400mil 28pin SOJ  
28P0K



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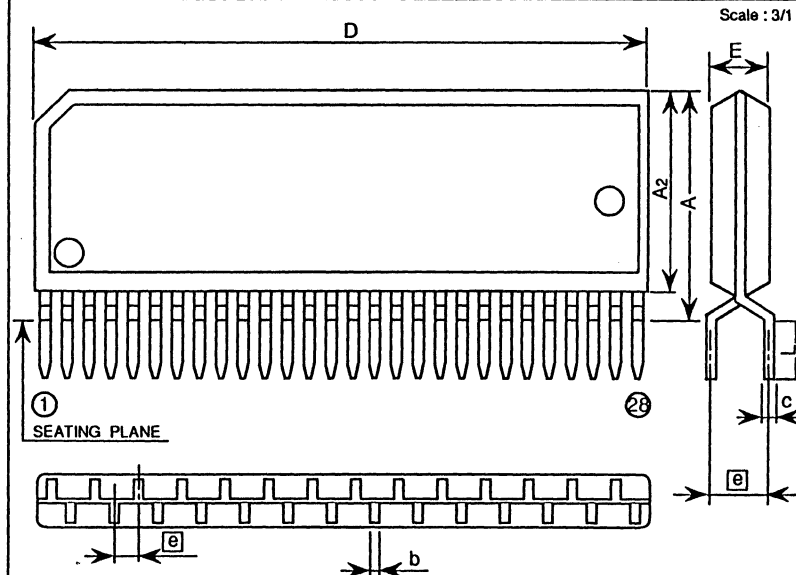
M5M442256 A  
256KX4bit Dual Port DRAM



MITSUBISHI SEMICONDUCTOR PACKAGES  
28P5L

Plastic 28Pin ZIP

Package Name	Lead Treatment	Weight(g)	EIAJ Code No.	JEDECCode No.
28P5L	Solder plating			



Symbol	Dimension in Millimeters			Dimension in Inches		
	Min	Nom	Max	Min	Nom	Max
A	-	-	10.16	-	-	0.400
A <sub>2</sub>	8.3	8.5	8.7	0.327	0.335	0.343
b	0.4	0.5	0.6	0.016	0.020	0.024
c	0.2	0.25	0.32	0.008	0.010	0.013
D	35.35	35.55	35.75	1.392	1.400	1.407
E	2.6	2.8	3.0	0.102	0.110	0.118
[e]	-	1.27	-	-	0.050	-
[e]	-	2.54	-	-	0.100	-
L	3.0	-	-	0.118	-	-

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MITSUBISHI ELECTRIC

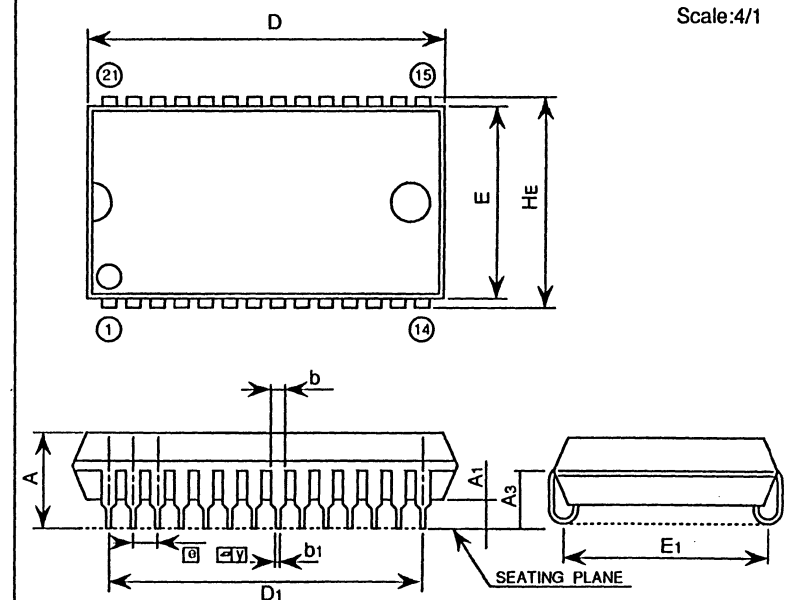
M5M442256 A  
256KX4bit Dual Port DRAM



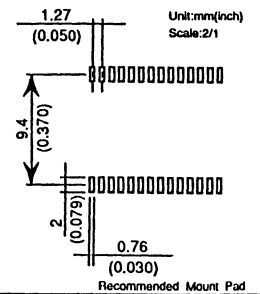
MITSUBISHI SEMICONDUCTOR PACKAGES  
28POK

Plastic 28pin 400mil SOI

Package Name	Lead Treatment	Weight(g)	EIAJ Code No.	JEDECCode No.
28POK	Solder plating			



Symbol	Dimension in Millimeters			Dimension in Inches		
	Min	Nom	Max	Min	Nom	Max
A	-	-	3.55	-	-	0.140
A <sub>1</sub>	0.8	-	-	0.031	-	-
A <sub>2</sub>	2.25	2.35	2.45	0.089	0.093	0.096
b	0.67	0.7	0.81	0.026	0.028	0.032
b <sub>1</sub>	0.33	0.43	0.53	0.013	0.017	0.021
D	18.28	18.41	18.54	0.720	0.725	0.730
D <sub>1</sub>	-	16.51	-	-	0.65	-
E	10.03	10.16	10.29	0.395	0.400	0.405
E <sub>1</sub>	9.27	9.4	9.53	0.365	0.370	0.375
[e]	-	1.27	-	-	0.050	-
HE	11.05	11.18	11.31	0.435	0.440	0.445
y	-	-	0.1	-	-	0.004





MITSUBISHI ELECTRIC

M5M442256 A 256K X 4bit Dual port DRAM

M5M482128 A 128K X 8bit Dual port DRAM



Table

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code mnemonic	/RAS falling edge						CAS falling edge					Write Mask Op.	Raster Op.	Register		color	
	CAS	DT/ OE	WB/ WE	DSF	SE	Addr.	WIO	WB/ WE	DSF	Addr.	WIO			WM1 temporary	WM2 persistant		
option	0	0	0	0	-	-	-	-	-	-	-	-	-	-	-	-	None Use
	0	0	0	1	-	-	-	-	-	-	-	-	-	-	-	-	C.B.R
CBR	0	0	1	0	-	-	-	-	-	-	-	-	-	-	-	-	C.B.R
	0	0	1	1	-	-	-	-	-	-	-	-	-	-	-	-	C.B.R
CBR	0	1	1	0	-	-	-	-	-	-	-	-	-	-	-	-	C.B.R
	0	1	1	1	-	-	-	-	-	-	-	-	-	-	-	-	C.B.R
MWT/ PWT	1	0	0	0	0/1	Row	WM1	-	0	TAP	-	Yes per Row	-	Lord Use	-	-	Wr. Transfer(/SE=0) Pseudo Wr. Transfer(/SE=1)
	1	0	0	0	0/1	Row	WM1	-	1	TAP	-	Yes per Row	-	Lord Use	-	-	Split Write Transfer with New Mask
SWT	1	0	0	1	-	Row	WM1	-	0	TAP	-	Yes per Row	-	Lord Use	-	-	Read Transfer
	1	0	0	1	-	Row	WM1	-	1	TAP	-	-	-	-	-	-	Split Read Transfer
RT	1	0	1	0	-	Row	-	-	0	TAP	-	-	-	-	-	-	Read Write with New Mask
	1	0	1	0	-	Row	-	-	1	TAP	-	-	-	-	-	-	Block Write with New Mask
SRT	1	0	1	1	-	Row	-	-	0	TAP	-	-	-	-	-	-	Flash Write with New Mask
	1	0	1	1	-	Row	-	-	1	TAP	-	-	-	-	-	-	Read/ Write with No Mask
RWNM	1	1	0	0	-	Row	WM1	*E/L	0	Col	DQin	Yes	-	Lord Use	-	-	Block Write with No Mask
BWNM	1	1	0	0	-	Row	WM1	-	1	Col	Sel.	Yes	-	Lord Use	-	Use	Load Color Reg.
FWT	1	1	0	1	-	Row	WM1	-	0	-	-	Yes per Row	-	Lord Use	-	-	
	1	1	0	1	-	Row	WM1	-	1	-	-	-	-	-	-	-	
RW	1	1	1	0	-	Row	-	*E/L	0	Col	DQin	-	-	-	-	-	
BW	1	1	1	0	-	Row	-	-	1	Col	Sel.	-	-	-	-	Use	
LCR	1	1	1	1	-	Ref	-	*E/L	0	-	CLR.	-	-	-	-	Lord	
	1	1	1	1	-	Ref	-	*E/L	1	-	CLR.	-	-	-	-	Lord	

\*E/L:Early write/Late write



## M5M482128A 128K×8bit Dual - Port DRAM

### Feature

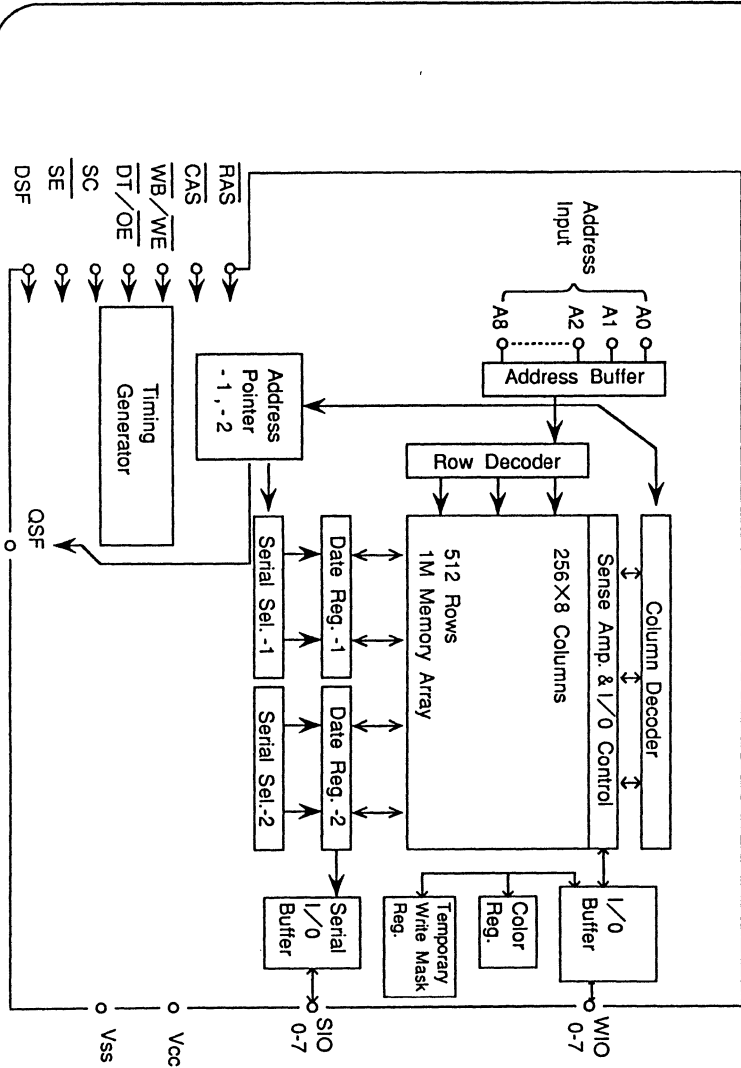
- Dual Port RAM
  - RAM Port 128K×8bit
  - tRAC 70/80/100ns Max.
  - SAM Port
  - tSCC 30/30/30ns Max
- Bi - directional Date Transfer between RAM and SAM
- Bi - directional SAM Port
- Addressable Start Pointer of SAM
- Fully Asynchronous Dual Port Accessibility
- Write per Bit Function
- Relaxed Real Time Data Transfer (Split SAM architecture)
- Flash Write Function
- Block Write Function
- Fast Page Mode,Hidden Refresh and/CAS before/RAS Refresh
- 512 cycle/8ms Refresh
- Low Power (CMOS)
 

RAM Port/SAM Port	100ns Ver.
Stand-by/Stand-by	5mA Max.
Active/Stand-by	60mA Max.
Stand-by/Active	35mA Max.
Active/Active	90mA Max.
- 40pin 400mil SOJ

MITSUBISHI ELECTRIC

M5M482128A

128K×8bit Dual Port DRAM Block Diagram





**MITSUBISHI ELECTRIC**  
**1M VRAM (Dual Port RAM)**



2nd Generation (A ver)  
M5M442256A / M5M482128A

What New are : "High Performance"

COMPARISON between 1st and 2nd Generation

Generation	1st	2nd (Target)
Feature	Fast Page Split SAM Flash Write Block Write	Same Same Same Same
Access Time RAM Port		
tRAC	120/100	100/ 80 /70
tCAC	35/ 30	30/ 25/ 20
SAM Port		
tSCA	40/ 30	25/ 25/25
tSCC	40/ 30	30/ 30/30
Power Dissipation		
lcc1 (RAM)	60/ 70	60/ 75/ 85
lcc8 (SAM)	40/ 50	35/ 35/ 35
lcc12 (Xfer)	100/120	90/110/120
Package		
256K×4	400mil ZIP/SOJ	Same
128K×8	400mil SOJ	Same
		{ T S O P }
		{ (planning) }
Design Rule	1.0 μm	0.9 μm
Gate Oxide(Call)	SiO <sub>2</sub> 80 Å	SiO <sub>2</sub> 75 Å
Gate Length(NMOS)	1.1 μm	0.9 μm
Gate Length(PMOS)	1.5 μm	1.2 μm

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**MITSUBISHI ELECTRIC**



**256K VRAM (Dual Port RAM)**  
2nd Generation (A ver.)  
M5M4C264AL/J (64KX4)

What New are ;

Function  
Upper Compatible with M5M4C264L

Write per Bit

Characteristics

High Speed

Fast (Enhanced) Page Mode

tRAC 80ns Max. ← 100ns

tCAC 25ns Max. ← 50ns

tSCA 25ns Max. ← 35ns

tSCC 30ns Max. ← 35ns

Low Power Dissipation

35% Decreased from M5M4C264

RAM/SAM

lcc1 Act/Stb 60mA Max. ← 70mA Max.

lcc8 Stb/Act at tRC = 160ns ← at tRC = 200ns

30mA Max. 45mA Max.

at tRC = 30ns at tRC = 40ns

Package

400mil 24pin ZIP

300mil 24pin SOJ

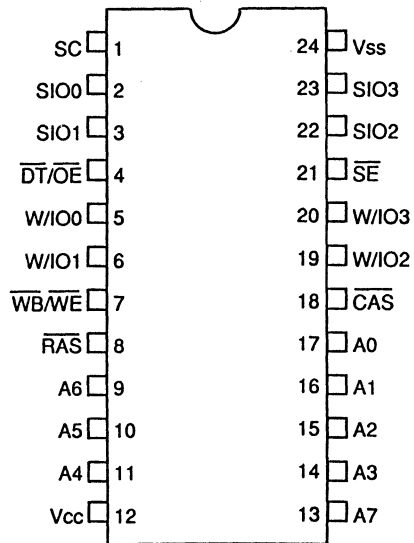
Production Plan (SOJ)

ES 90/9

CS 90/11

256K VRAM (Dual Port RAM)  
2nd Generation (A ver.)  
M5M4C264AL/J (64KX4)

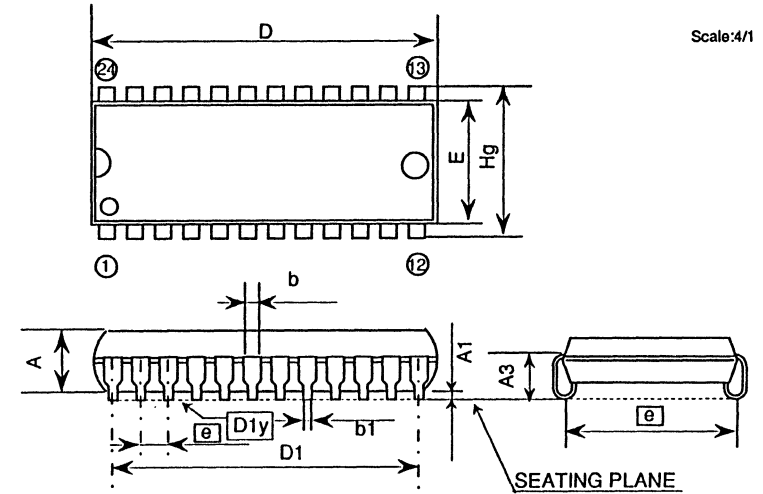
300mil 24Pin SOJ Pinout



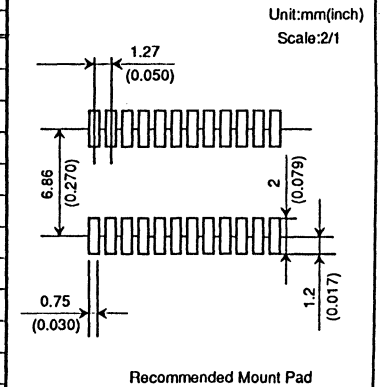
54

256KVRAM (Dual Port RAM)  
2nd Generation(AVer.)  
M5M4C264AJ(64KX4)

Package Name	Lead Treatment	Weight (g)	EIAJ Code No.	JEDEC Code No.
24POJ	Solder Plating			



Symbol	Dimension in Millimeters			Dimension in Inches		
	Min	Non	Max	Min	Non	Max
A	-	-	3.55	-	-	0.140
A1	0.8	-	-	0.031	-	-
A3	2.25	2.35	2.45	0.089	0.093	0.096
b	0.67	0.7	0.81	0.026	0.028	0.032
b1	0.33	0.43	0.53	0.013	0.017	0.021
D	15.74	15.87	16.0	0.620	0.625	0.630
D1	-	13.97	-	-	0.550	-
E	7.52	7.62	7.72	0.296	0.300	0.304
e	6.73	6.86	6.99	0.265	0.270	0.275
e	-	1.27	-	-	0.050	-
Hg	8.35	8.45	8.55	0.330	0.333	0.337
Y	-	-	0.1	-	-	0.004



Recommended Mount Pad

Unit:mm(inch)  
Scale:2/1



## 261Kx4bit Field SAM (M5M4C900L)

### Feature

#### Memory Size

Field Memory	(FMEM)	288ROWx928COLx4bit
Serial Input Memory	(SIM)	928x4bit
Serial Output Memory	(SOM)	928x4bit

#### Cycle Time

Serial Input Memory (SIM)	tc=50nsMin
Serial Output Memory (SOM)	tc=30nsMin

Asynchronous Operatable SIM and SOM  
Split SAM Architecture

Bidirectional Data Transfer between SIM and FMEM

Addressable SIM/SOM Tap

Simple Timing Controlability with Triple Multi BUS  
ROW Add./COL.Add./Command

Package 28pin ZIP (400mil)

### Application

Field Memory for TV/VCR/Video Printer  
NTSC/PAL/SECAM/ID/ED/HD TV System

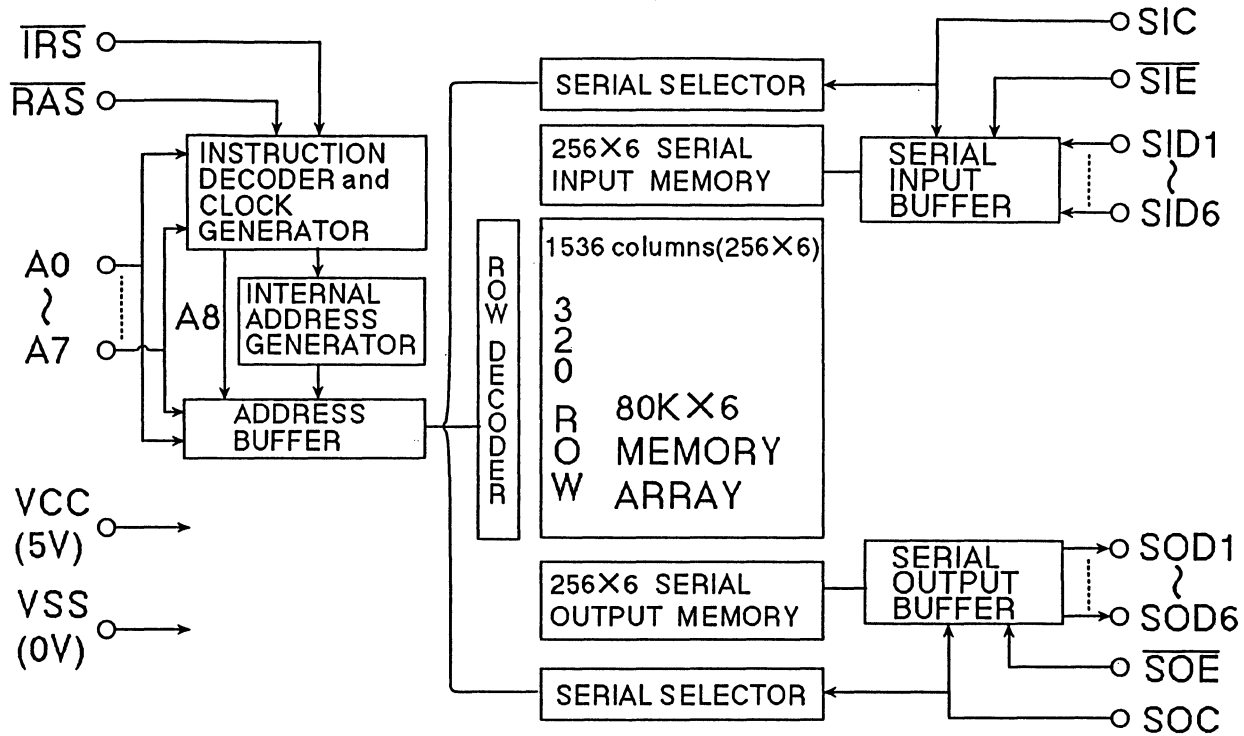
Band Memory for Page Printer  
LBP,PPC,FAX

High Speed Buffer Memory





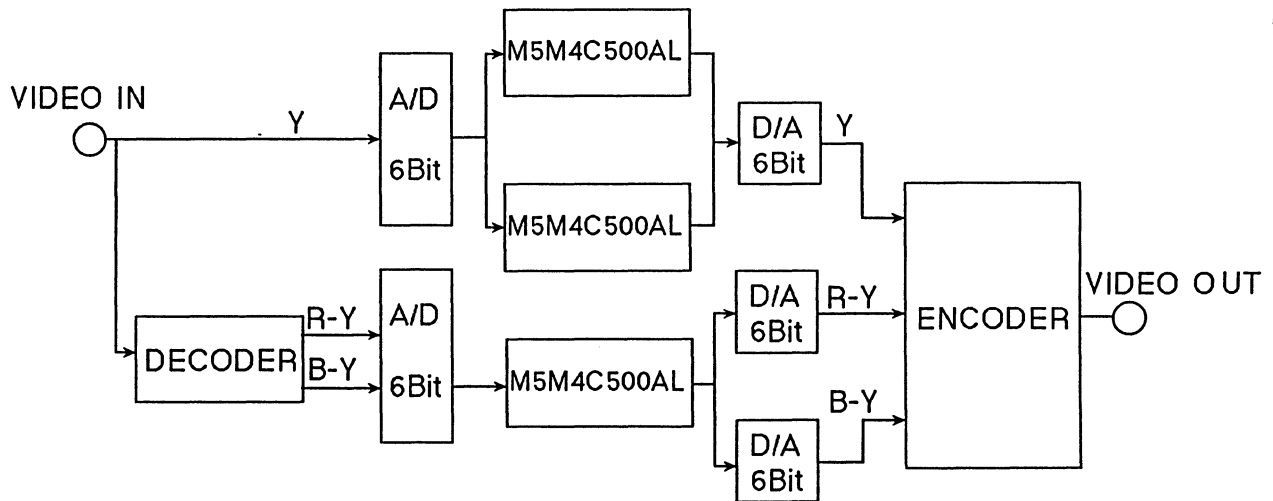
### BLOCK DIAGRAM of M5M4C500AL



### Field SAM (M5M4C500AL) for TV/VCR

#### Application 1

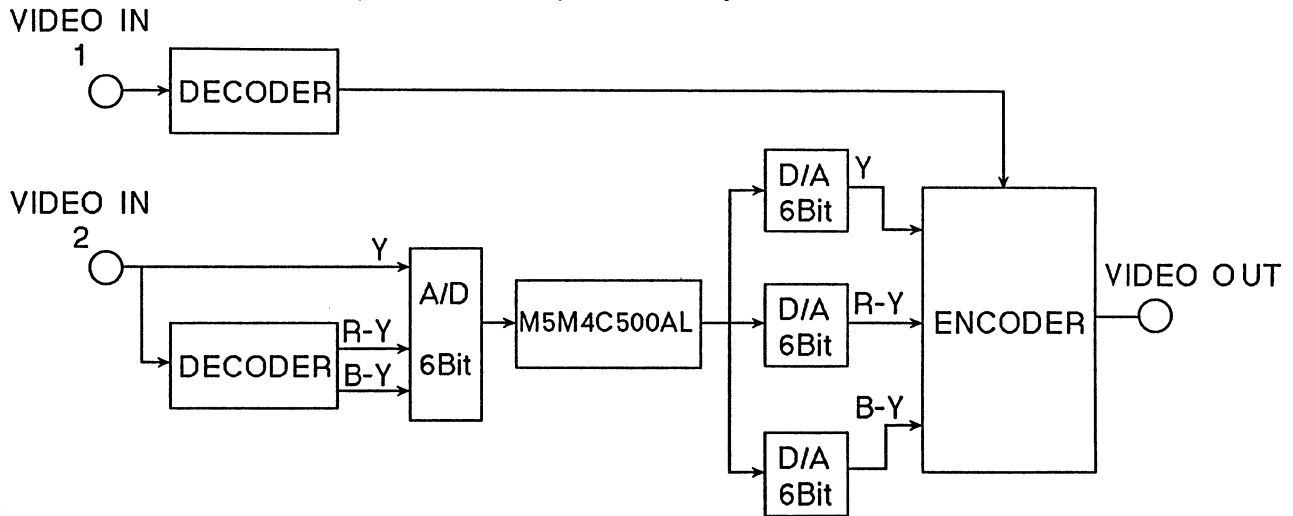
TV/VCR Full digital play system.



## Field SAM (M5M4C500AL) for TV/VCR

### Application 2

TV/VCR picture in picture system.



## FSAM — FEATURES of PRODUCTS —

		M5M4C500	M5M4C500A	M5M4C900
SAMPLE SCHEDULE		MP NOW 500K/M	ES N O W CS 90-12	ES TBD CS TBD
MEMORY SIZE		480K bits		1.02M bits
ORGANIZATION		320×256×6		288×928×4
SAM CYCLE	TSCC	50ns	30ns	30ns
PACKAGE OPTIONS		28PIN ZIP	28PIN ZIP	28PIN ZIP
APPLI-CATIONS		Picture In Picture Multi Screen Video Printer		IDTV,EDTV HDTV Video Printer



## 4M bit Cached DRAM (M5M44409TP)

### What's New!

- High Band width Memory                      100M Words/sec.
- High Speed Cache SRAM on DRAM.

### Target Applications

- High Speed Cache & Main Memory for PC,WS.
- 2nd/3rd Cache for Main Frame.



## 4M bit Cached DRAM

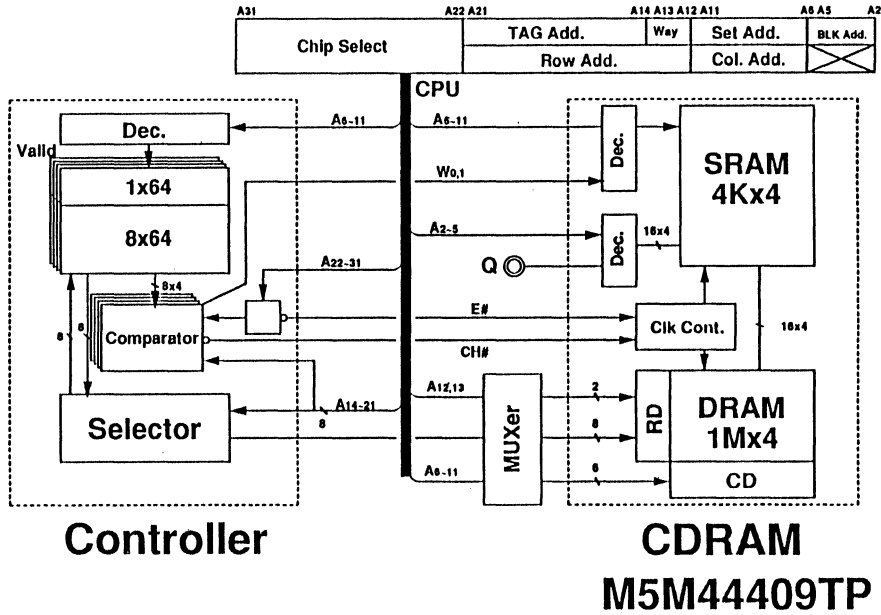
### Feature

- 1M× 4 bit DRAM and 4K×4bit High Speed Cache SRAM are integrated
- High Speed Cache Access    : 10ns max
- Block(16×4bit) Transfer Capable between DRAM and SRAM
- Support to the Direct Map/Associative System



# 4M bit Cached DRAM

## Block Diagram in a 4Way Set Associative System

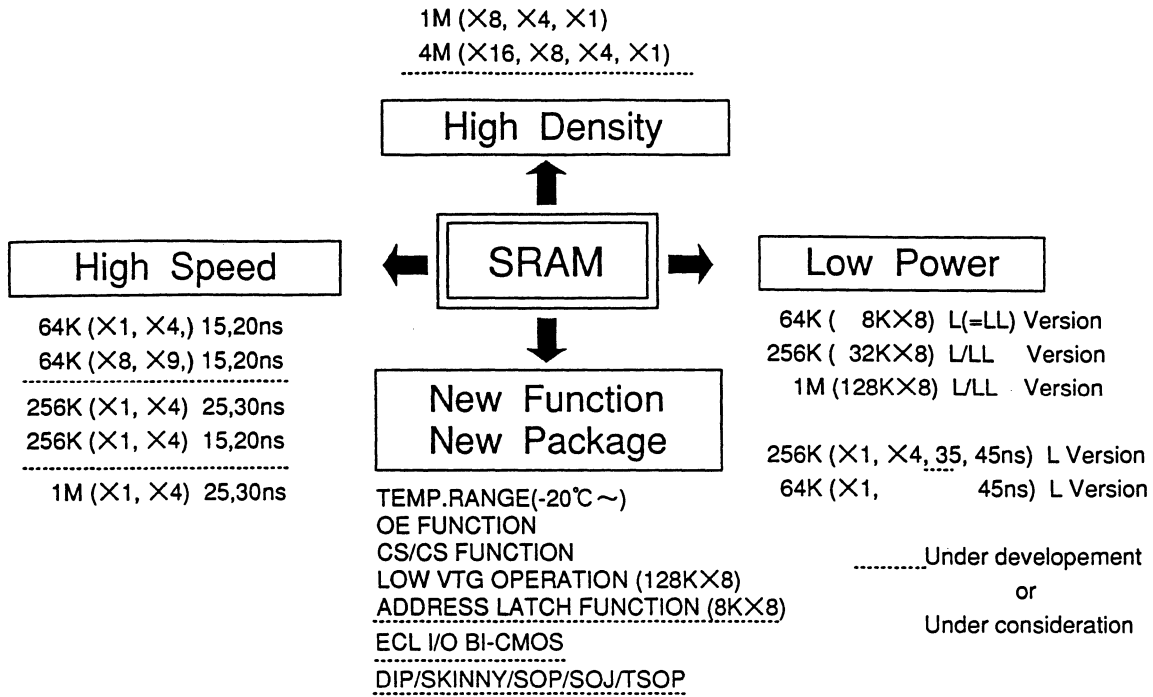


# 4M bit Cached DRAM

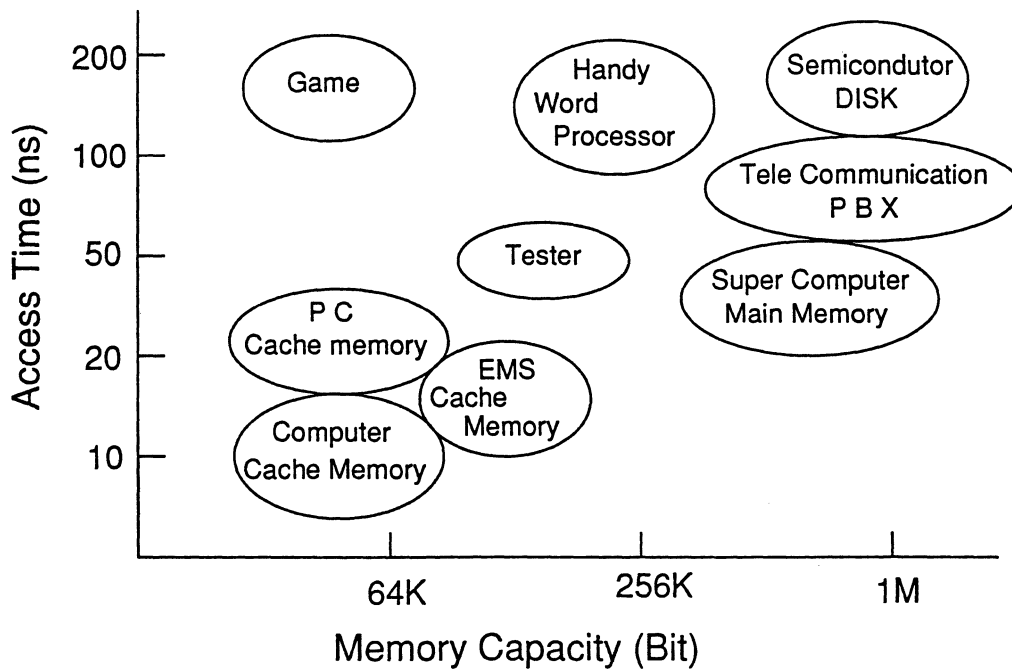
## TARGET PERFORMANCE

Type name	Cache Hit Access/cycle	Array Access/cycle	Cache Fill Time with Copy Back	Power Dissipation
M5M44409TP-10	10ns/10ns	70ns/140ns	210ns	Cache:550mW Array:413mW
M5M44409TP-15	15ns/15ns	70ns/140ns	210ns	Cache:440mW Array:413mW
M5M44409TP-20	20ns/20ns	80ns/160ns	240ns	Cache:385mW Array:358mW

Technical Strategy of SRAM



Application of Static RAM



### Mitsubishi Fast SRAM Selection

Super Computer Main Frame	1M×1	M5M51001-25/35/45	DIP,SOJ
	256K×4	M5M51004-25/35/45,M5M51014-25/35/45(I/O Sepa.)	DIP,SOJ
Mini Computer EWS	256K×1	M5M5257B-15/20,M5M5257A-25/30,M5M5257-35/45	DIP,SOJ
	64K×4	M5M5258B-15/20,M5M5258A-25/30,M5M5258-35/45	DIP,SOJ
	64K×4(OE)	M5M5259B-15/20	DIP,SOJ
Personal Computer	32K×8	M5M5278-15/20/25	DIP,SOJ
	32K×9	M5M5279-15/20/25,M5M5269-15/20/25	DIP,SOJ
	64K×1	M5M5187B-15/20,M5M5187A-25/35	DIP,SOJ
	16K×4	M5M5188B-15/20,M5M5188A-25/35	DIP,SOJ
	16K×4(OE)	M5M5189B-15/20,M5M5189A-25/35	DIP,SOJ
	8K×8	M5M5178A-15/20/25,M5M5178-35/45	SOJ, DIP,SOP
	8K×8(Latch)	M5M5180A-20/25	SOJ, DIP,SOP
8K×8	M5M5179A-15/20/25,M5M5179-35/45	SOJ, DIP,SOP	

### MITSUBISHI SRAM Selection



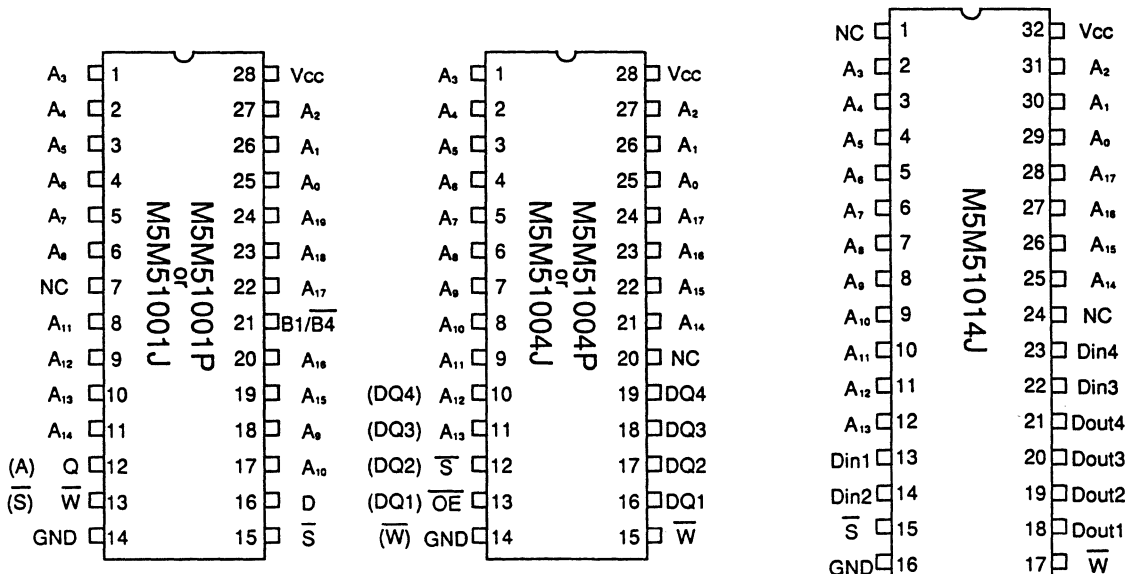
Memory Capacity	Access time (ns)	Access time (ns)												
		15	20	25	30	35	45	55	70	85	100	120	150	
16K	16K×1						M5M21C67P							
	4K×4						M5M21C68P							
64K	8K×8	M5M5178AP					M5M5178P							
	8K×9	M5M5179AP					M5M5179P							
	64K×1	M5M5187BP,J					M5M5187AP,J							
	16K×4	M5M5188BP,J						M5M5188AP,J						
		M5M5189BP,J						M5M5189AP,J						
256K	32K×8	M5M5278P,J												
	256K×1	M5M5257BP,J		M5M5257AP,J			M5M5257P,J							
		M5M5258BP,J		M5M5258AP,J			M5M5258P,J							
	64K×4													
1M	128K×8													
	1M×1					M5M51001P,J								
	256K×4					M5M51004P,J								
	256K×4 I/F sepa					M5M51014J								

## MITSUBISHI 256KX4 / 1MX1 Static RAM

### TARGET FEATURES

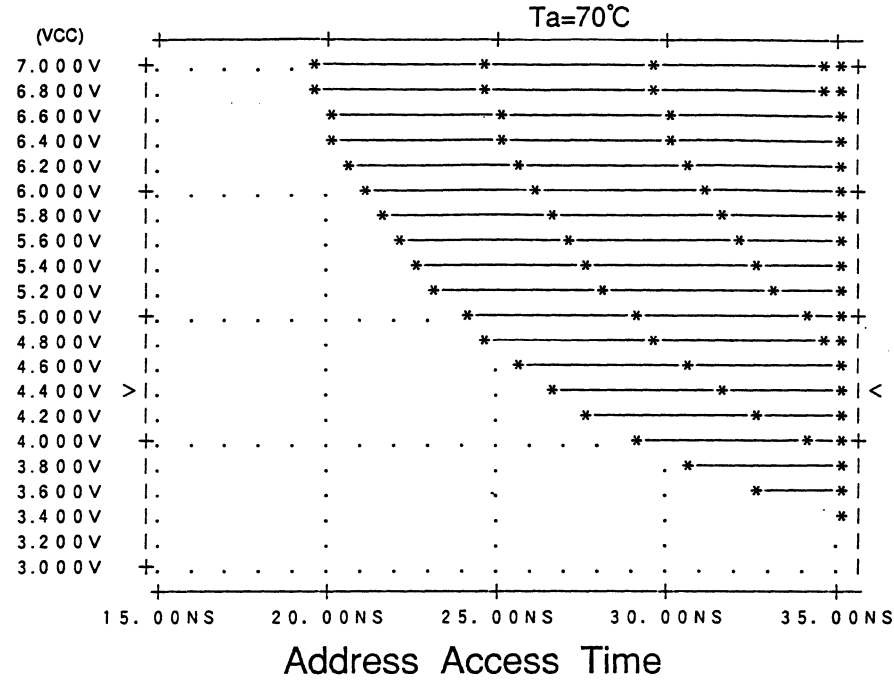
Organization	256KX4 / 1MX1
Design Rule	0.8 $\mu$ m
Process technology	CMOS, Triple poly-Si Double Al
Access time	25ns / 35ns / 45ns
Active current	120mA(max.)
Standby current	40mA(max.)
Chip size	6.10X15.84(96.6)mm <sup>2</sup>
Cell size	5.875X8.5(49.9) $\mu$ m <sup>2</sup>
Package	28-pin / 400mil DIP, SOJ
Sample Availability	NOW 25ns Jan.'91
Production	NOW 25ns Apr.'91

## 1M Fast SRAM PIN CONFIGURATION



1M×1 / 256K×4 FAST SRAM  
(M5M51001 / M5M51004 / M5M51014)

Access Time Shmoo Plot



8K×8 / 8K×9 SRAM  
(M5M5178A / 79A / 80A)

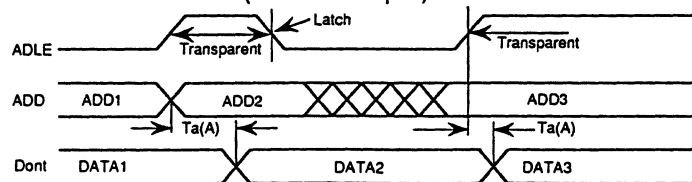


TARGET FEATURES

- Organization 8K×8(78A/80A)  
8K×9(79A)
- Design Rule 0.8 μm
- Process CMOS, Triple poly-Si,  
Single Al
- Access time 78A/79A 15ns/20ns/25ns  
80A 20ns/25ns Ta(OE)=8ns/10ns
- Active current 120mA(max)
- Standby current(AC) 30mA(max)
- Chip size 5.53×3.53mm<sup>2</sup>
- Cell size 10.5×8.0 μm<sup>2</sup>

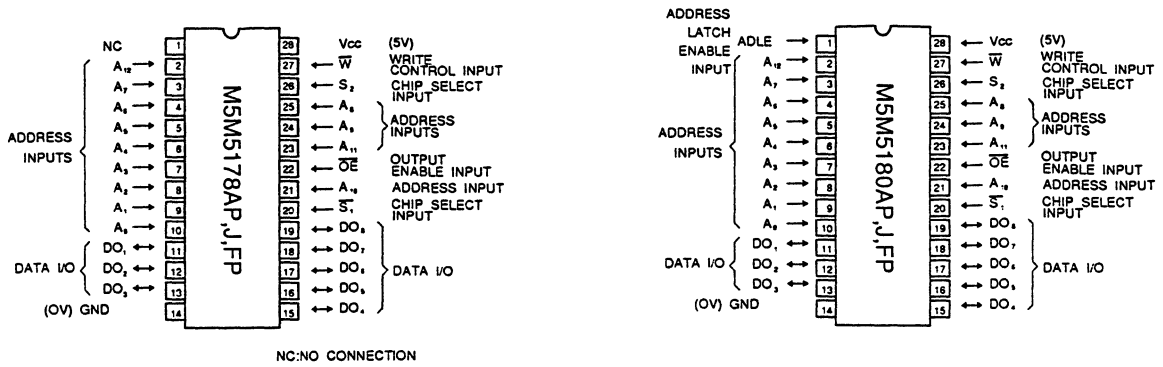
M5M5180A FEATURES

- Address Latch Function (with ADLE pin)

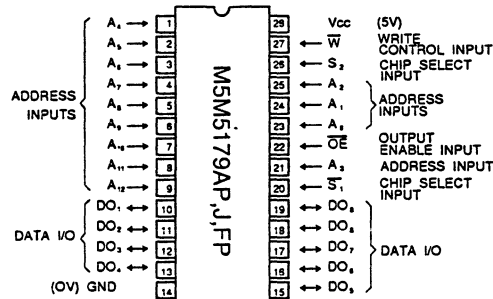




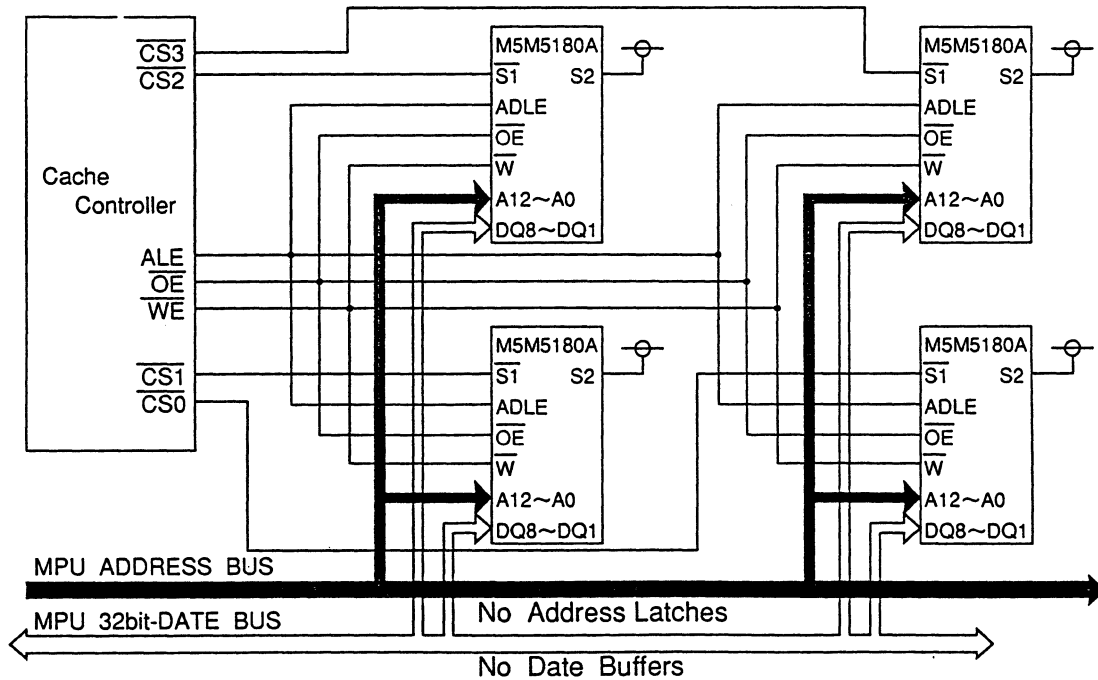
MITSUBISHI ELECTRIC  
**8K×8,8K×9 FAST SRAM PIN CONFIGURATION**  
 (TOP VIEW)



NC:NO CONNECTION



MITSUBISHI ELECTRIC  
**Example of Cache with M5M5180A**  
 — 32KB Direct Mapping —

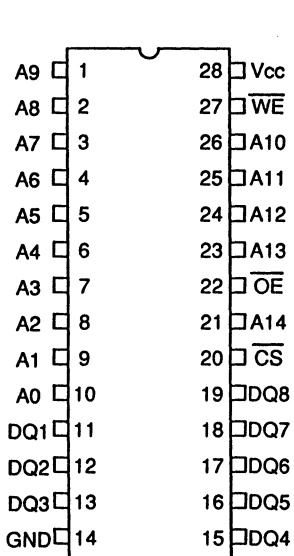


### 32KX8 / 32KX9 FAST SRAM (M5M5278/M5M5279/M5M5269)

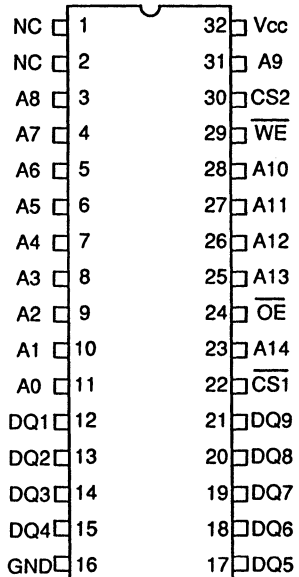


Organization	32KX8 / 32KX9
Design Rule	0.8 $\mu$ m
Process Technology	CMOS Double Al Triple Poly-Si
Access Time	(15ns) / 20ns/25ns
Active Current	140mA(max)
Standby Current	30mA(max)
Chip Size	4.6X11.89mm <sup>2</sup>
Cell Size	6.3X10.0 $\mu$ m <sup>2</sup>
ESD(@1.5Kohm, 100pf)	>3000V
Soft Error Rate	<300fit
Latch-up(@Vcc=5V)	Free
Package	300mil DIP, SOJ 32KX8 28pin 32KX9 32pin
Sample Availability	Jan '91
Production	Mar'91

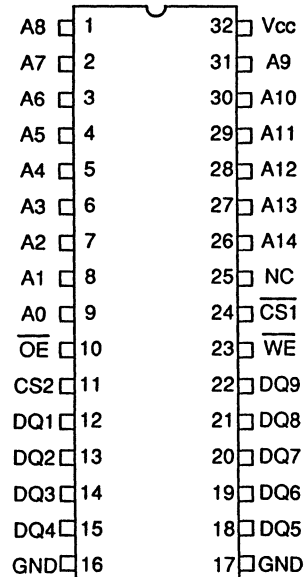
### 32KX8/32KX9 Fast SRAM Pin Out



M5M5278P,J  
32KX8



M5M5279P,J  
32KX9



M5M5269FP  
32KX9



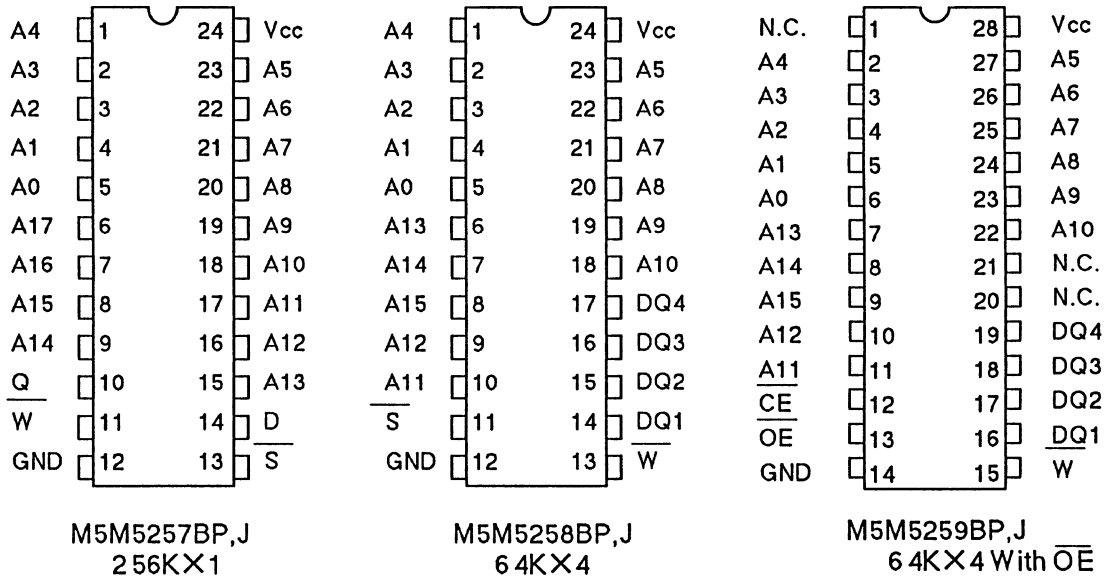
## 256KX1 / 64X4 FAST SRAM (M5M5257B / 58B / 59B)

### TARGET FEATURES

Organization	64KX4/256KX1
Design Rule	0.8 $\mu$ m
Process technology	CMOS, Triple poly-Si Double Al
Access time	15ns/20ns
Active current	120mA(max)
Standby current(AC)	30mA(max)
Chip size	4.54X10.69mm <sup>2</sup>
Cell size	6.3X10.0 $\mu$ m <sup>2</sup>
ESD(@1.5K $\Omega$ , 100pf)	>3000V
Soft error rate	<300fit
Latch-up(@Vcc=5V)	Free
Package	24pin/300mil DIP, SOJ (5259B 28pin)
Sample Availability	'90-12 (5259B '91-2)
Production	'91-3 (5259B '91-3)



## 256K X 1/64K X 4 Fast SRAM Pin Out



### Design Objective of 256K Fast SRAM

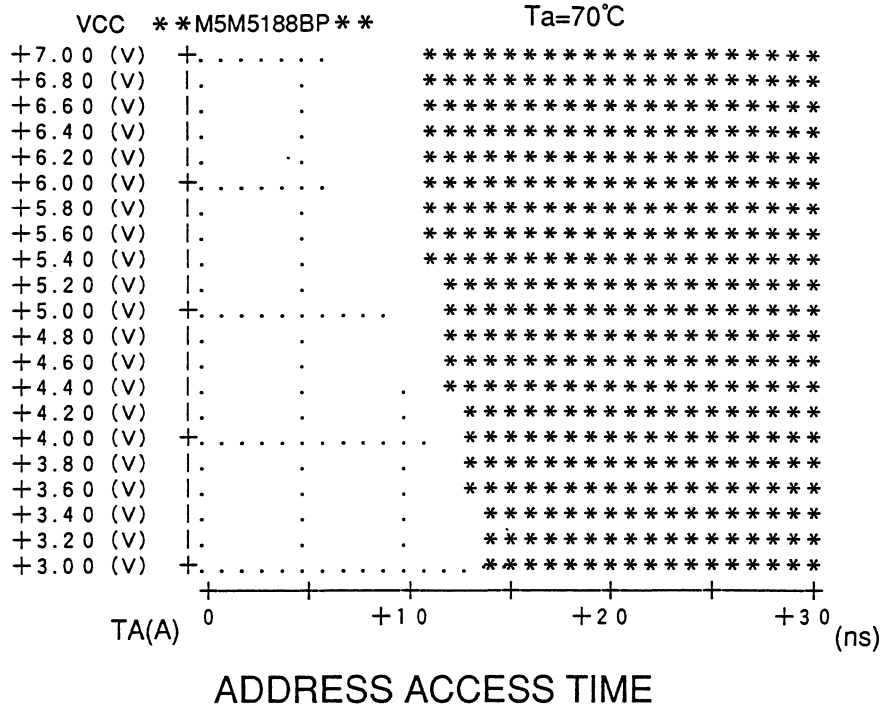
	M5M5257AP	256K word × 1 bit
	M5M5258AP	64K word × 4 bit
Package	300 mil 24pin plastic DIP	
Power supply	single 5V	
Access time	25,30	
Power Dissipation	active	660mW max.
	stand by (TTL level)	165mW max.
	stand by (MOS level)	55mw max.
Process technology	scaled CMOS 1.0 μm design rule	

### Design Objective of 64K Fast SRAM

Organization	M5M5187BP	65536 word × 1 bit
	M5M5188BP	16384 word × 4 bit
	M5M5189BP	16384 word × 4 bit with $\overline{OE}$ pin
Package	M5M5187BP/5188BP	300 mil 22 pin plastic DIP
	M5M5189BP	300 mil 24 pin plastic DIP
Power supply	single 5V	
Access time	15ns,20ns,25ns	
Power dissipation	active	660mW max
	stand by (TTL level)	165mW max
	stand by (MOS level)	55mW max
Process technology	scaled CMOS 1.1 μm design rule	
Chip size	19.1mm <sup>2</sup>	

SOJ package is available (24P 300mil)

## 64K FAST SRAM (M5M5188BP, 16K×4) Access Time Shmoo Plot



## 1M bit SRAM (128K×8) M5M51008P/FP/VP/RV

131072 word×8bit CMOS RAM

### Features

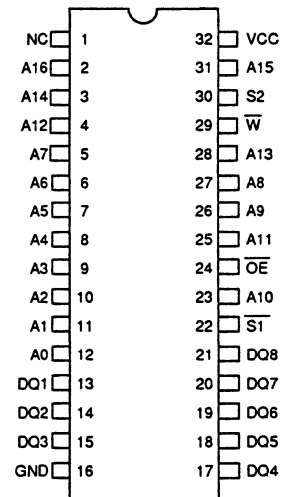
- High speed 70/85/100/120ns
- Low power
  - Low power\* Standby 10 μW (typ)
  - Operation 200mW (typ) 10MHz
- Single 5V Supply
- Completely static...No clock is required.

### Process

- 0.8 μm Mixed CMOS
- Tripple poly Si

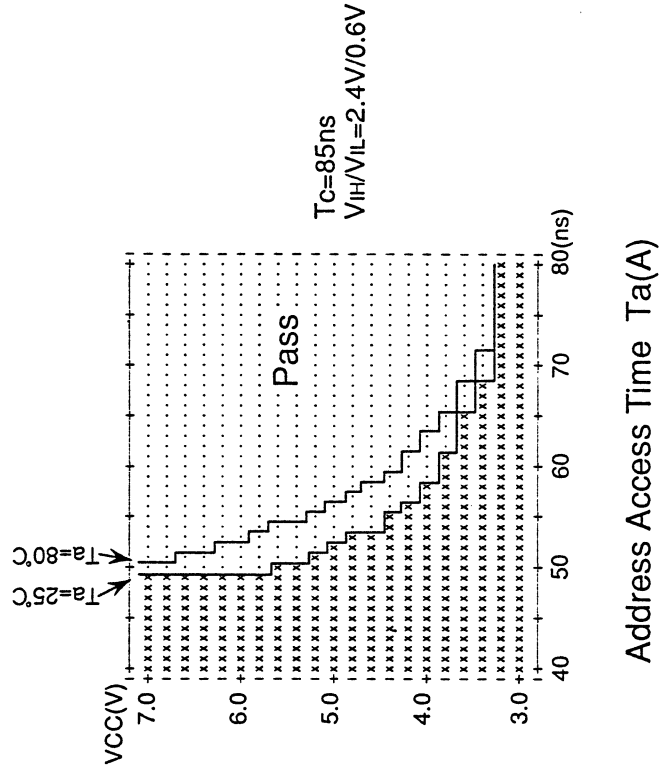
### Package

- 600 mil DIP
- 525 mil SOP
- 8×20mm<sup>2</sup> TSOP

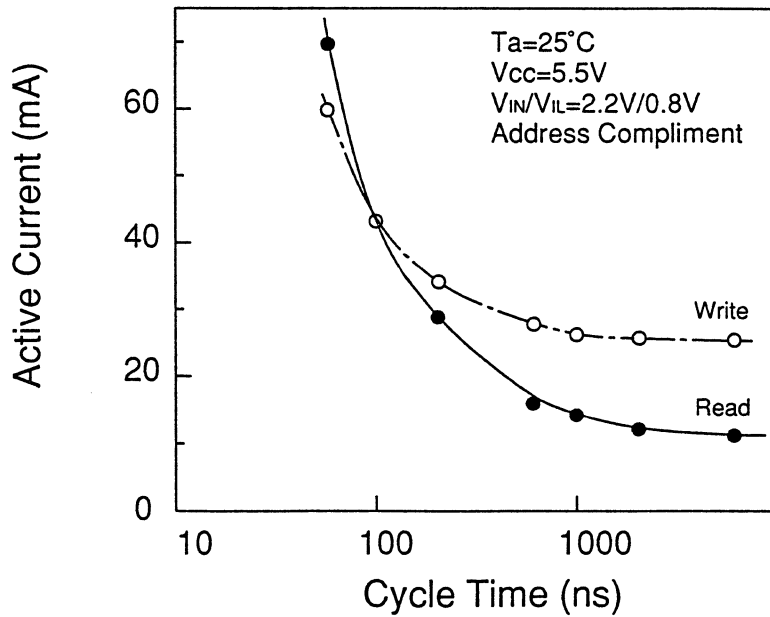


32 PIN Package  
P/FP Outline

M5M51008P/FP/VP/RV  
Address Access Time



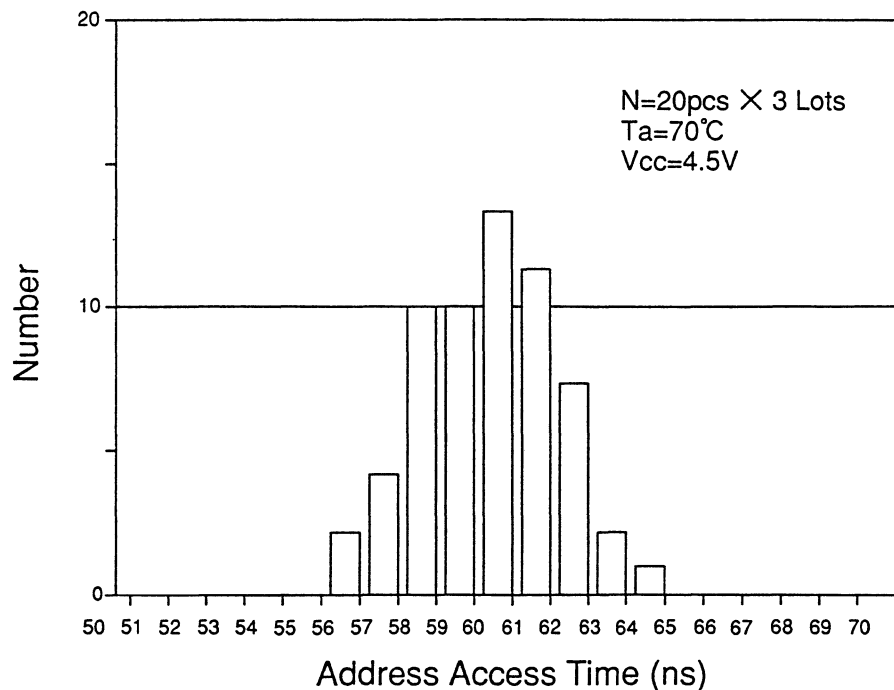
M5M51008P/FP/VP/RV Power Supply Current



### MITSUBISHI 1M SRAM Series

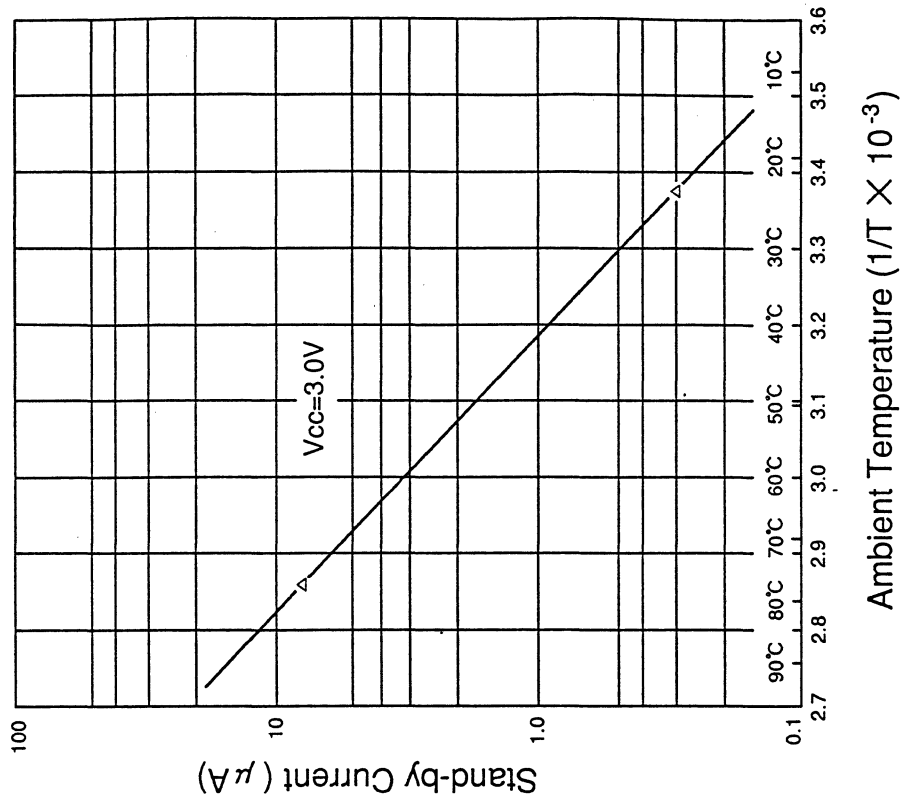
Part NO.	Item	Access Time	Stand by Current	Package
M5M51008P	70,85,10,12	70ns,85ns,100ns,120ns	2mA	600mil DIP
	70L,85L,10L,12L	70ns,85ns,100ns,120ns	50 $\mu$ A(3V,70°C)	
	70LL,85LL, 10LL,12LL	70ns,85ns,100ns,120ns	10 $\mu$ A(3V,70°C)	
M5M51008FP	70,85,10,12	70ns,85ns,100ns,120ns	2mA	525mil SOP
	70L,85L,10L,12L	70ns,85ns,100ns,120ns	50 $\mu$ A(3V,70°C)	
	70LL,85LL, 10LL,12LL	70ns,85ns,100ns,120ns	10 $\mu$ A(3V,70°C)	
M5M51008VP RV	70,85,10,12	70ns,85ns,100ns,120ns	2mA	8X20mm TSOP
	70L,85L,10L,12L	70ns,85ns,100ns,120ns	50 $\mu$ A(3V,70°C)	
	70LL,85LL 10LL,12LL	70ns,85ns,100ns,120ns	10 $\mu$ A(3V,70°C)	

### 1MSRAM Distribution of Access Time M5M51008P/FP/VP/RV



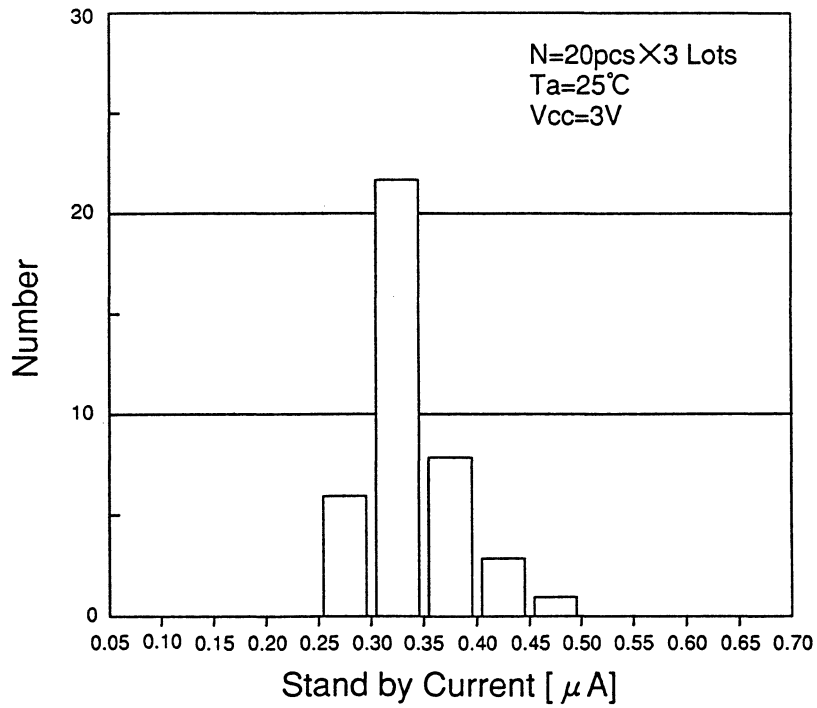
M5M51008P/FP/VP/RV

Stand by Current



1MSRAM Distribution of Stand by Current

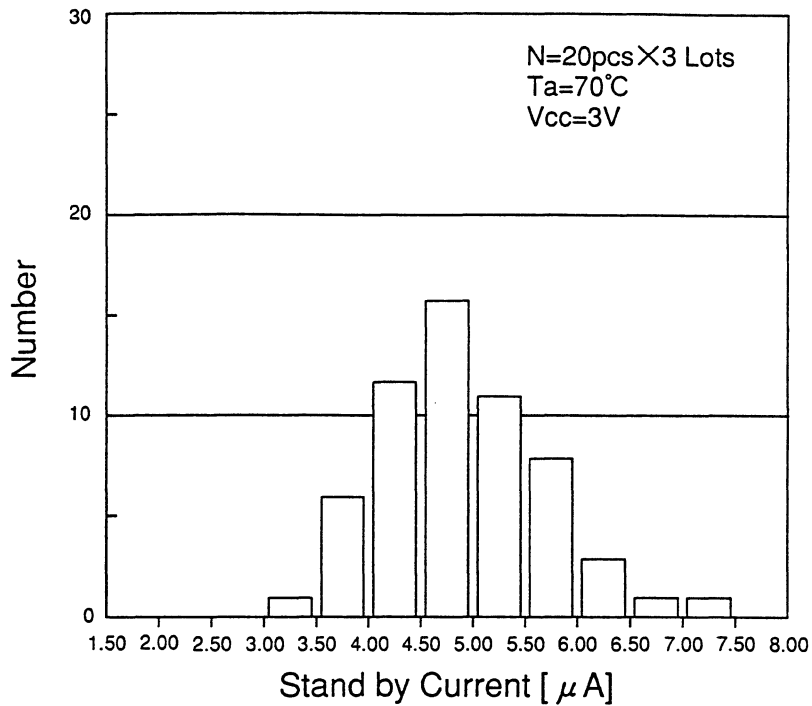
M5M51008P/FP/VP/RV





### 1MSRAM Distribution of Stand by Current

M5M51008P/FP/VP/RV

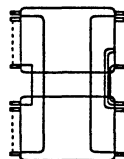


### M5M51008VP/RV TSOP (Thin Small Outline Package)

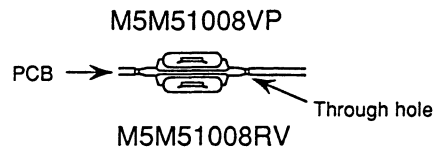
#### Advantage of TSOP

- Very Small . . . . . 1/2 area of SOP, comparable size as TAB  
1/4 volume of SOP
- High reliability . . . . . 100% burn in & full test can be done
- Short lead length . . . . . Low inductance, Low capacitance  
(DIP 10nH → 2nH) (DIP 1.5pF → 0.5pF)
- Uniform lead length . . . . . Uniform electric characteristics
- Easy PCB layout . . . . . Normal lead type and reverse bend type are available

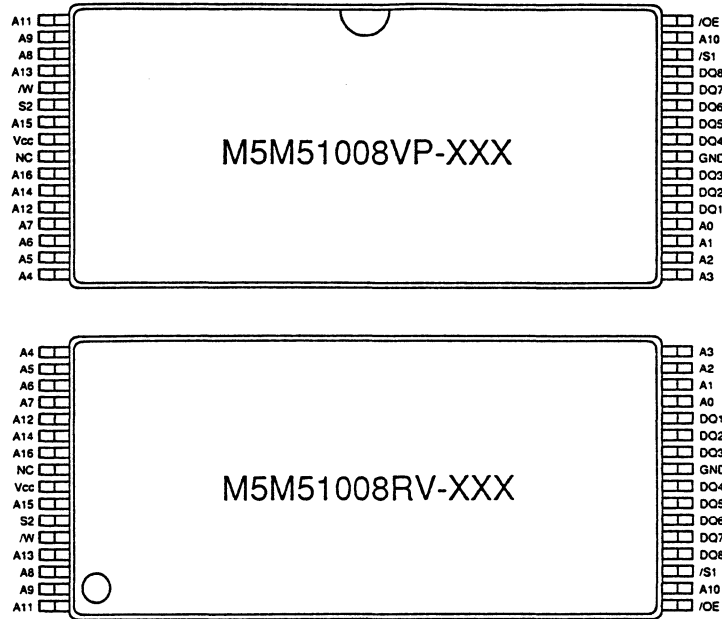
M5M51008VP



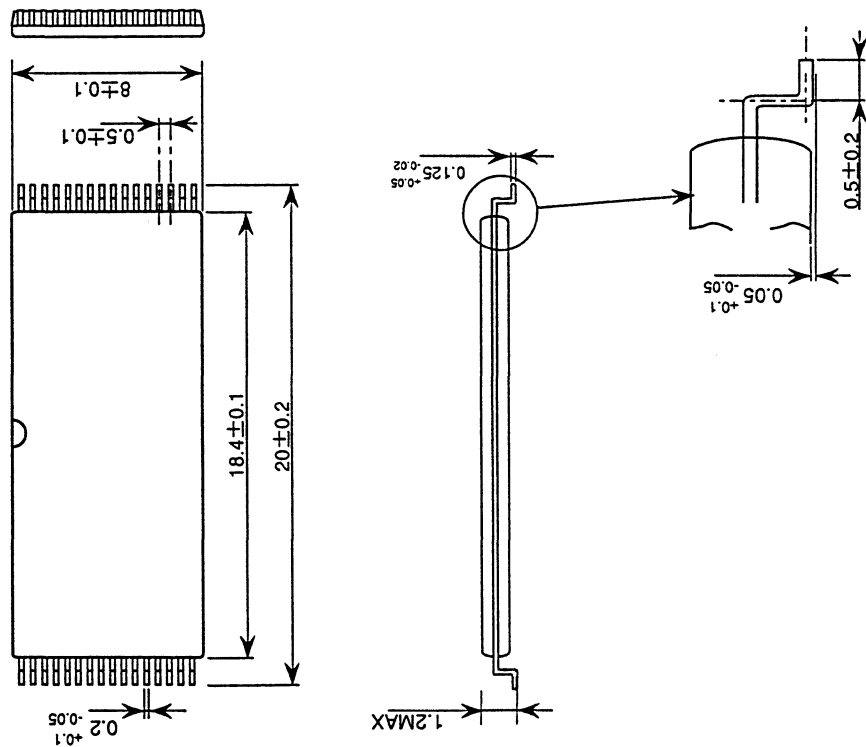
M5M51008RV



### M5M51008VP/RV TSOP Outline



### 1M SRAM TSOP Dimensions





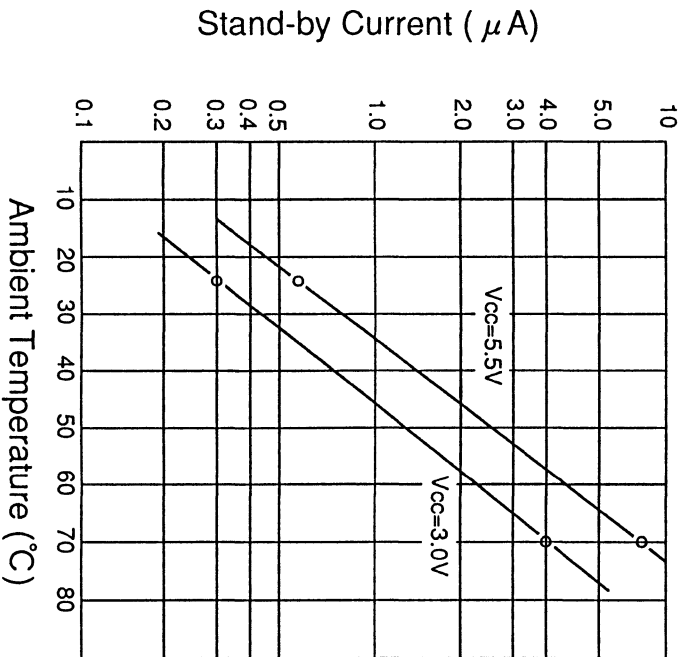
## MITSUBISHI ELECTRIC 256K SRAM Shrink Chip Series

Part No.	Item	Access Time	Stand-by Current	Package	Remark
M5M5256BP	70,85,10,12	70ns,85ns,100ns,120ns	2mA	600mil DIP	
	70L,85L,10L,12L	70ns,85ns,100ns,120ns	100 $\mu$ A		
	70LL,85LL,10LL,12LL	70ns,85ns,100ns,120ns	20 $\mu$ A		
M5M5256BKP	70,85,10,12	70ns,85ns,100ns,120ns	2mA	300mil DIP (Skinny package)	
	70L,85L,10L,12L	70ns,85ns,100ns,120ns	100 $\mu$ A		
	70LL,85LL,10LL,12LL	70ns,85ns,100ns,120ns	20 $\mu$ A		
M5M5256BFP	70,85,10,12	70ns,85ns,100ns,120ns	2mA	SOP	
	70L,85L,10L,12L	70ns,85ns,100ns,120ns	100 $\mu$ A		
	70LL,85LL,10LL,12LL	70ns,85ns,100ns,120ns	20 $\mu$ A		
M5M5256BVP BRV	70L,85L,10L,12L	70ns,85ns,100ns,120ns	100 $\mu$ A	TSOP	
	70LL,85LL,10LL,12LL	70ns,85ns,100ns,120ns	20 $\mu$ A		
M5M5255BP	70,85,10,12	70ns,85ns,100ns,120ns	2mA	600mil DIP	S1,S2
	70L,85L,10L,12L	70ns,85ns,100ns,120ns	100 $\mu$ A		
	70LL,85LL,10LL,12LL	70ns,85ns,100ns,120ns	20 $\mu$ A		
M5M5255BKP	70,85,10,12	70ns,85ns,100ns,120ns	2mA	300mil DIP	S1,S2
	70L,85L,10L,12L	70ns,85ns,100ns,120ns	100 $\mu$ A		
	70LL,85LL,10LL,12LL	70ns,85ns,100ns,120ns	20 $\mu$ A		
M5M5255BFP	70,85,10,12	70ns,85ns,100ns,120ns	2mA	SOP	S1,S2
	70L,85L,10L,12L	70ns,85ns,100ns,120ns	100 $\mu$ A		
	70LL,85LL,10LL,12LL	70ns,85ns,100ns,120ns	20 $\mu$ A		

MITSUBISHI ELECTRIC

256KSRAM(M5M5256B)

Stand-by Current V.S.Ambient Temperature

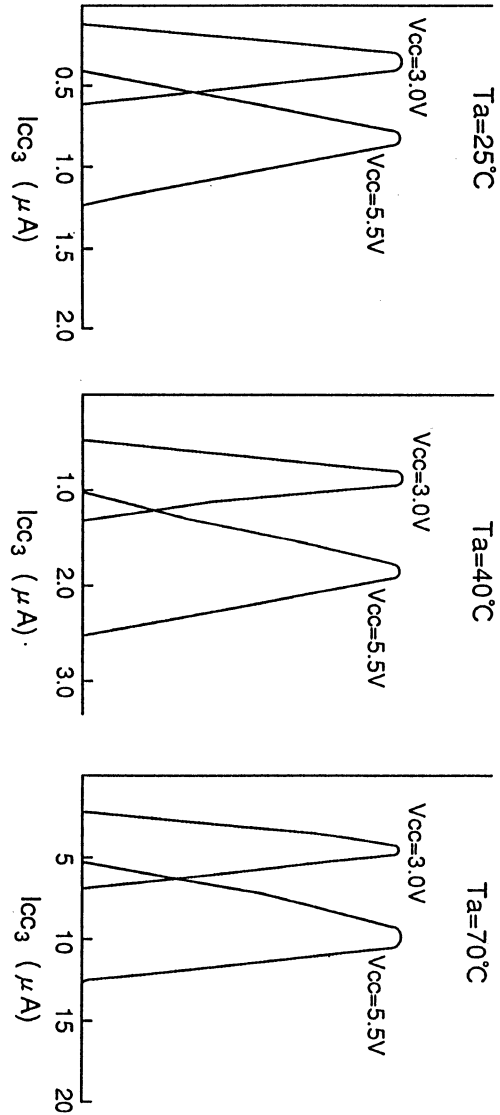


General Reliability Evaluations for M5M5256BKP

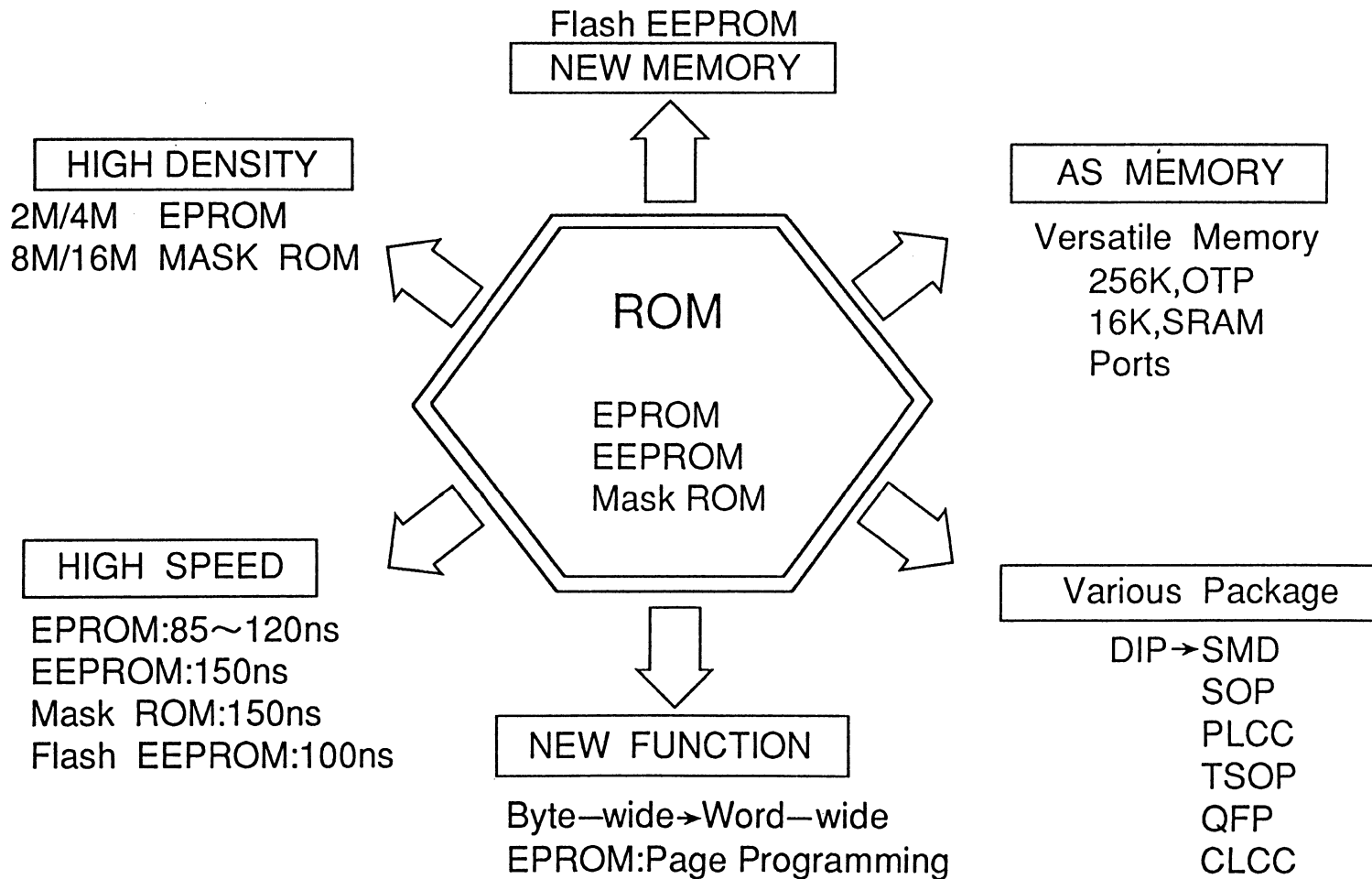
Test Item	Test Condition	Failure Identification	Sample Size	Failures
Dynamic Life Test (1)	Ta = 125°C Vcc = 6.0V t = 2000 Hrs	DC and Function Stability of electrical margins	200	0
Dynamic Life Test (2)	Ta = -40°C Vcc = 7.0V t = 1000 Hrs	DC and Function Stability of electrical margins	50	0
Thermal Stress	Soldering Heat	260°C, 10 sec	100	0
	Thermal Shock	-55°C/125°C 15 cycles		0
	Temperature cycling	-65°C/150°C 100 cycles		0
Moisture Resistance	Ta = 85°C Relative Humidity =85% Vcc = 5.5V t = 2000 Hrs	DC and Function Stability of electrical margins	200	* 1
Pressure Cooker Test (1)	Ta = 121°C Relative Humidity =100% t = 200 Hrs	DC and Function Stability of electrical margins	150	0
Pressure Cooker Test (2)	Ta = 140°C Relative Humidity =85% Vcc = 5.5V t = 500h	DC and Function Stability of electrical margins	100	0
High Temperature Storage	Ta = 150°C t = 1000 hrs	DC and Function Stability of electrical margins	100	0

\* ; AL Corrosion

256K SRAM (M5M5256B)  
Distribution of stand-by current



# ROM Technology Trend



## MITSUBISHI ROM Selection



Device			Access Time (ns)				
			50	100	150	200	250
E P R O M	32K×8	NMOS					M5L27256K
	32K×8	CMOS		M5M27C256AK			
	64K×8	NMOS				M5L27512K	
	64K×8	CMOS		M5M27C512AK			
	128K×8	CMOS			M5M27C100K		
	128K×8	CMOS			M5M27C101K,JK		
	64K×16	CMOS			M5M27C102K,JK		
	256K×8	CMOS		M5M27C201K,JK			
	128K×16	CMOS		M5M27C202K,JK			
	512K×8	CMOS			M5M27C401K		
256K×16	CMOS			M5M27C402K			
R a s k	512K×8/256K×16	CMOS			M5M23400AP,FP		
	512K×8	CMOS			M5M23401AP,FP		
	1M×8/512K×16	CMOS			M5M23800P	*	
	1M×8	CMOS			M5M23801P	*	
	2M×8/1M×16	CMOS			M5M23160P	*	
EEPROM	8K×8	CMOS					M5M28C64AP,FP,VP,RV
Flash EEPROM	128K×8	CMOS			M5M28F101P	*	
	64K×16	CMOS			M5M28F102P	*	

\* :under development

## Mitsubishi EPROM

### General Features

#### 1) High Performance

- High Speed.....85ns(27C256A), 100ns(27C512A,2M EPROM)  
120ns(1M EPROM, 4M EPROM)
- Low Power.....30mA(Active)/100 μ A(Standby) (27C256A, 2M,4M EPROM)  
50mA(Active)/100 μ A(Standby) (1M EPROM,27C512A)

#### 2) High Quality

- High reliability ..... <100fit
- Low incoming failure rate..... <100ppm
- ESD Endurance ..... >1000V(100PF, 1.5K Ω), >300V(200PF, 0 Ω)

#### 3) Complete screening and test procedure

- Data retention test for all bits of all devices
- AC/DC characteristics test for all devices

#### 4) Many varieties and Large volume production capacity

- Pioneer of EPROM in JAPAN (from 2K bit)
- Main EPROM supplier from 256K bit to the current devices

### Comparison Table of Mitsubishi EPROM

Memory capacity	256K	512K	1M		2M		4M	
Organization	32K×8	64K×8	128K ×8	64K ×16	256K ×8	128K ×16	512K ×8	256K ×16
Type name	M5M 27C256AK	M5M 27C512AK	M5M 27C100/ 101K	M5M 27C102K	M5M 27C201K	M5M 27C202K	M5M 27C401K	M5M 27C402K
Process technology	CMOS 1.2 μm	CMOS 1.2 μm	CMOS 1.2 μm	CMOS 1.2 μm	CMOS 0.9 μm	CMOS 0.9 μm	CMOS 0.9 μm	CMOS 0.9 μm
Access time (ns)	85 100 120 150	100 120 150	120 150 200 250	120 150 200 250	100 120 150	100 120 150	120 150	120 150
Active current(mA)	30	50	50	50	30	30	30	30
Standby current(mA)	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1
Read	Vcc(V) Vpp(V)	5	5	5	5	5	5	5
Program	Vcc(V) Vpp(V)	6 12.5	6 12.5	6 12.5	6 12.5	6 12.5	6.25 12.75	6.25 12.75
Pins/Package*/ Width (mil)	28K (600)	28K (600)	32K (600) 32JK	40K (600) 44JK	32K (600) 32JK	40K (600) 44JK	32K (600)	40K (600)
Note								

Package \*...K:CERDIP,JK:CLCC

### Comparison Table of Mitsubishi OTPROM

Memory capacity	256K	512K	1M		2M		4M	
Organization	32K×8	64K×8	128K ×8	64K ×16	256K ×8	128K ×16	512K ×8	256K ×16
Type name	M5M 27C256AP	M5M 27C512AP	M5M 27C100/ 101P	M5M 27C102P	M5M 27C201P	M5M 27C202P	M5M 27C401P	M5M 27C402P
Process technology	CMOS 1.2 μm	CMOS 1.2 μm	CMOS 1.2 μm	CMOS 1.2 μm	CMOS 0.9 μm	CMOS 0.9 μm	CMOS 0.9 μm	CMOS 0.9 μm
Access time ( ) Special Spec (ns)	(120) 150	(120) 150	150	150	(120) 150	(120) 150	150	150
Active current(mA)	30	50	50	50	30	30	30	30
Standby current(mA)	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1
Read	Vcc(V) Vpp(V)	5	5	5	5	5	5	5
Program	Vcc(V) Vpp(V)	6 12.5	6 12.5	6 12.5	6 12.5	6 12.5	6.25 12.75	6.25 12.75
Pins/Package*/ Width (mil)	28P(600) 28FP(450) 28VP,RV	28P(600) 28FP(450)	32P(600) 32FP(525) 32J 40VP,RV	40P(600) 40FP(525) 44J 40VP,RV	32P(600) 32FP(525) 32J 40VP,RV	40P(600) 40FP(525) 44J 40VP,RV	32P(600)	40P(600)
Note								

Package \*...P:DIP,FP:SOP,J:PLCC,VP/RV:TSOP

## 4M CMOS EPROM (M5M27C401K, M5M27C402K)

### Feature

1) Organization and pinout	M5M27C401K 512Kx8bit, 32pin DIP, JEDEC
	M5M27C402K 256Kx16bit, 40pin DIP, JEDEC
2) High speed access time	120ns/150ns (max.)
3) Low power supply current	30mA (Active)/0.1mA (Standby)
4) Vcc tolerance	5V±10%
5) Programming voltage	12.75V

### Technology

- 1) High performance Si-gate twin well CMOS      0.9 μm design rule
- 2) Low resistance material
- 3) Redundancy circuit for high yield

## 2M CMOS EPROM (M5M27C201K, M5M27C202K)

### Feature

1) Organization and pinout	M5M27C201K 256Kx8bit, 32pin DIP, JEDEC
	M5M27C202K 128Kx16bit, 40pin DIP, JEDEC
2) High speed access time	100ns/120ns/150ns (max.)
3) Low power supply current	30mA (Active)/0.1mA (Standby)
4) Vcc tolerance	5V±10%
5) Programming voltage	12.5V
6) Page programming algorithm	4-byte or 2-word programming

### Technology

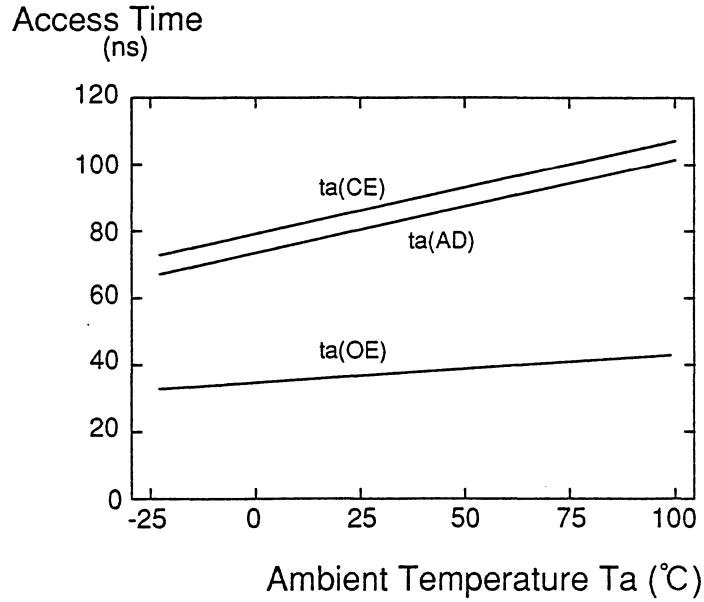
- 1) High performance Si-gate twin well CMOS      0.9 μm design rule
- 2) Low resistance material
- 3) Redundancy circuit for high yield



### CMOS EPROM M5M27C202K

Access Time vs Ambient Temperature

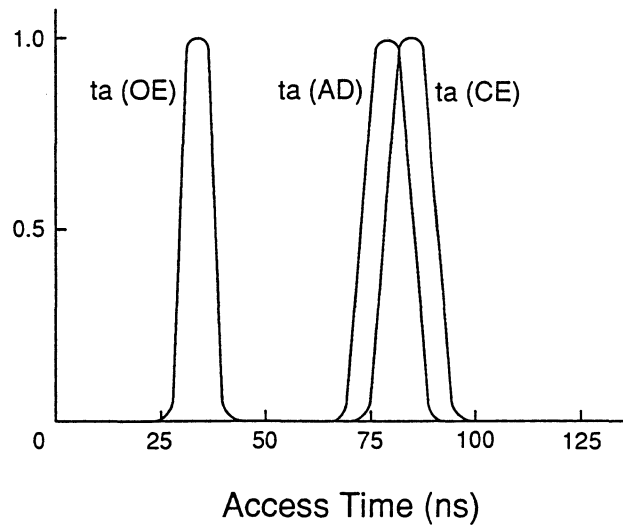
( $V_{CC}=5V$ )



### CMOS EPROM M5M27C202K

Normalized Distribution of Access Time

( $V_{CC}=5.0V, T_a=25^{\circ}C$ )

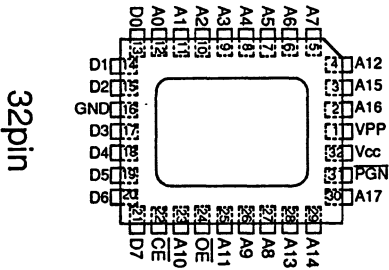




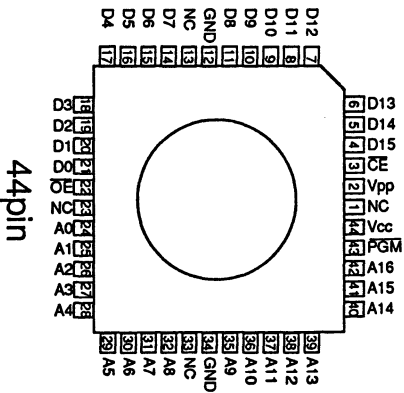
## 2M CMOS EPROM (CLCC)

### Features

- 1) Varieties of organization and pinout  
 M5M27C201JK ----- 256KX8bit, 32pin, JEDEC pin out  
 M5M27C202JK ----- 128KX16bit, 44pin, JEDEC pin out
- 2) High speed access time 100/120/150ns(max)
- 3) Pin compatible with PLCC(OTPROM)

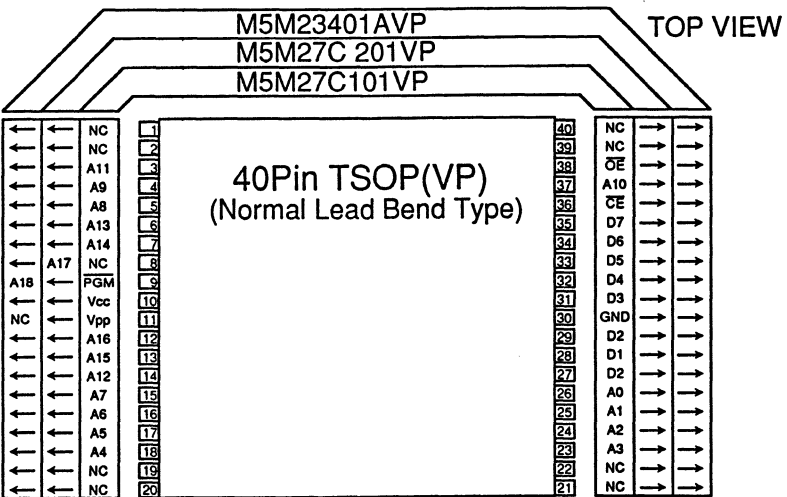


32pin

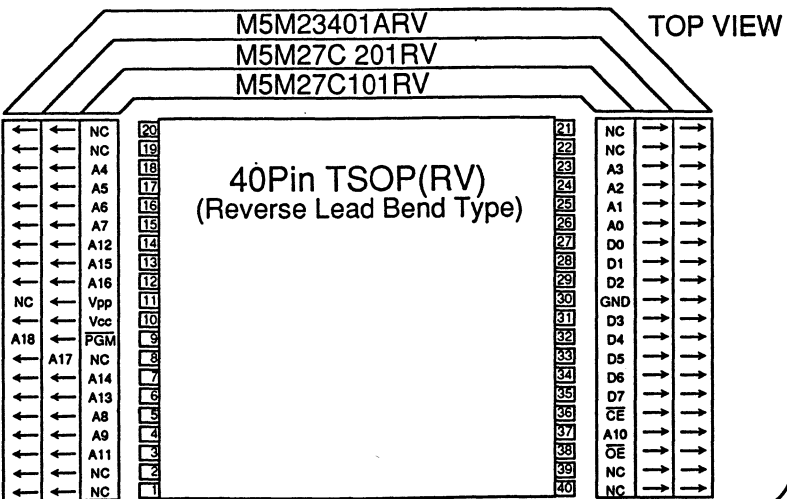


44pin

## 1M,2M OTP ROM / 4M Mask ROM Pin configuration (TSOP)



40Pin TSOP(VP)  
(Normal Lead Bend Type)



40Pin TSOP(RV)  
(Reverse Lead Bend Type)

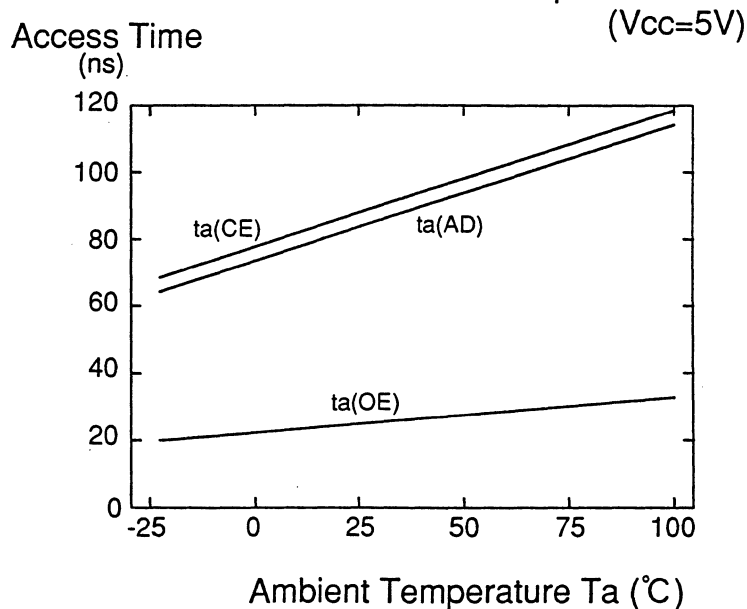
### CMOS 1.2 $\mu\text{m}$ EPROM/OTP Series

#### Technology

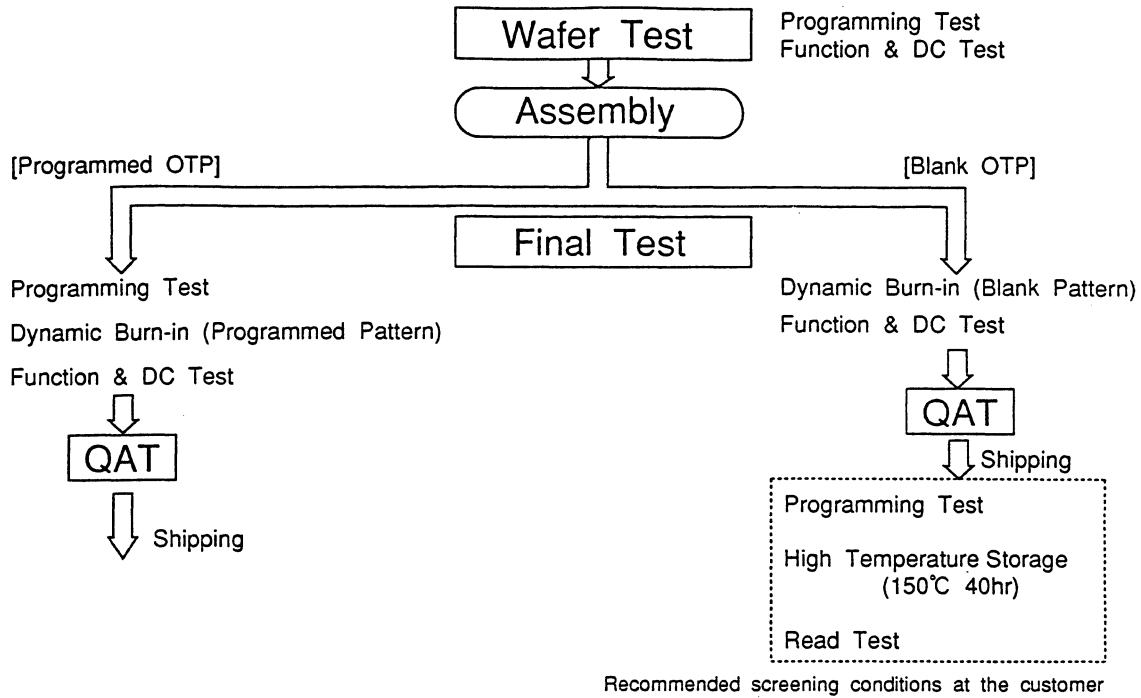
- 1) High performance Si-gate N-well CMOS  
1.2  $\mu\text{m}$  design rule  
Memory Cell size:  $4.5 \times 4.5 \mu\text{m}$   
Channel length:  $1.5 \mu\text{m}$ (N),  $2.0 \mu\text{m}$ (P)
- 2) Low resistance material  
MoSi
- 3) Redundancy circuit for high yield  
1M EPROMs/OTPs
- 4) High speed circuit  
High speed differential sense amplifier
- 5) CMOS 1.2  $\mu\text{m}$  EPROM/OTP Series:  
M5M27C256A, M5M27C512A, M5M27C100,  
M5M27C101, M5M27C102

### — CMOS EPROM M5M27C100K — M5M27C101K

Access Time vs Ambient Temperature



### OTP Test Flow



### APPROVED EPROM PROGRAMMER



EPROM PROGRAMMER MAKER	PROGRAMMER TYPE	
	GANG	SINGLE
ADVANTEST CORPORATION	R4951 R4952 R4949	R4945 R4944/A
ANDO ELECTRIC CO.,LTD	AF9720 AF9721 AF9722*	AF9703 AF9704
AVAL DATA CORPORATION	PKW-1600	PKW-1100/A PKW-3100
DATA I/O CORPORATION	S1000 280 288	UNIPAK2B UNISITE40 201
MINATO ELECTRONICS INC	MODEL-1870A MODEL-1910	MODEL-1900 MODEL-1890/A

\* Plan to approve

# MITSUBISHI FLASH EPROM, EPROM & EEPROM CELL

	Flash EEPROM	EPROM	EEPROM
Top View			
Cross Section			
Program	Hot Electron Injection	Hot Electron Injection	Tunneling
Erase	Tunneling	UV light	Tunneling

Advanced Information

## 1M FLASH EEPROM (M5M28F101P)

### Target Features

- |                            |                             |
|----------------------------|-----------------------------|
| 1) Organization            | 128k x 8bit                 |
| 2) High Speed Access Time  | 100ns/120ns/150ns(max.)     |
| 3) Power Supply            | V <sub>cc</sub> =5v±10%     |
|                            | V <sub>pp</sub> =12.0v±0.6v |
| 4) Low Power               | 50mA(Active)/0.1mA(Standby) |
| 5) Program/Erase Operation | Software Command Control    |
| 6) Program Time            | 10 μs Typical Byte-Program  |
|                            | 2sec Typical Chip-Program   |
| 7) Erase Time              | 1sec Typical Chip-Erase     |
| 8) Endurance               | 10000 Cycles                |
| 9) Package                 | 32 Pin DIP                  |
|                            | 32 Pin SOP                  |
|                            | 32 Pin PLCC                 |
|                            | 32 Pin TSOP                 |

### Technology

- 1) High Performance Si-Gate Twin-Well CMOS 0.9 μm Design Rule
- 2) Self-Aligned Stacked Gate (EPROM Base)

## 1M FLASH EEPROM MODE SELECTION TABLE

Mode		Pins	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	VPP	Data I/O
Read-Only	Read		VIL	VIL	VIH	VPPL	Data Out
	Output Disable		VIL	VIH	VIH	VPPL	Floating
	Standby		VIH	X	X	VPPL	Floating
Read/Write	Read		VIL	VIL	VIH	VPPH	Data Out
	Output Disable		VIL	VIH	VIH	VPPH	Floating
	Standby		VIH	X	X	VPPH	Floating
	Write		VIL	VIH	VIL	VPPH	Data In

VPPL=0~VCC+2.0V

VPPH=12.0±0.6V

X can be VIL or VIH

## 1M FLASH EEPROM SOFTWARE COMMAND DEFINITION

Command	Bus Cycles Req'd	First Bus Cycle			Second Bus Cycle		
		Mode	Address	Data I/o	Mode	Address	Data I/o
Read memory	1	write	X	00H	—	—	—
Set-up program/program	2	write	X	40H	write	PA	PD
Program verify	2	write	X	C0H	Read	X	PVD
Set-up erase/erase	2	write	X	20H	write	X	20H
Erase verify	2	write	EVA	A0H	Read	X	EVD
Reset	2	write	X	FFH	write	X	FFH
Read device identifier code	2	write	X	90H	Read	DIA	DID

PA = Programmed Address

EVA = Erase-Verified Address

DIA = Device Identifier Address : 0000H for manufacturer code,0001H for device code.

PA and EVA are latched on the falling edge of the  $\overline{WE}$  pulse.

PD = Programmed Data : Data is latched on the rising edge of the  $\overline{WE}$  pulse.

PVD = Program-Verified Data

EVD = Erase-Verified Data

DID = Device Identifier Data : 1CH for manufacturer code,D0H for device code.



## 1M Flash EEPROM (M5M28F102P,FP,J,VP,RV)

### Target Features

- |                            |   |
|----------------------------|---|
| 1) Organization            | 64Kx16bit   |
| 2) High Speed Access Time  | 100ns/120ns/150ns(max.)   |
| 3) Power Supply            | V <sub>cc</sub> =5V±10%<br>V <sub>pp</sub> =12.0V±5%                  |
| 4) Low Power               | 50mA(Active)/0.1mA(Standby)   |
| 5) Program/Erase Operation | Software Command Control<br>Erase / Program Pulse Controlled by Timer |
| 6) Program Time            | 10 μs Typical Byte-Program<br>1 sec Typical Chip-Program              |
| 7) Erase Time              | 1 sec Typical Chip-Erase  |
| 8) Program/Erase Cycles    | 10000 Cycles  |
| 9) Package                 | 40 pin DIP, SOP, TSOP, 44pin PLCC                                     |

### Technology

- 1) High performance Si-Gate Twin-well CMOS (0.9 μm Rule)
- 2) Self-Aligned Stacked Gate(EEPROM Base)
- 3) Redundancy Circuit for High Yield



## 1M(64K x 16) Flash EEPROM Software Command Definition

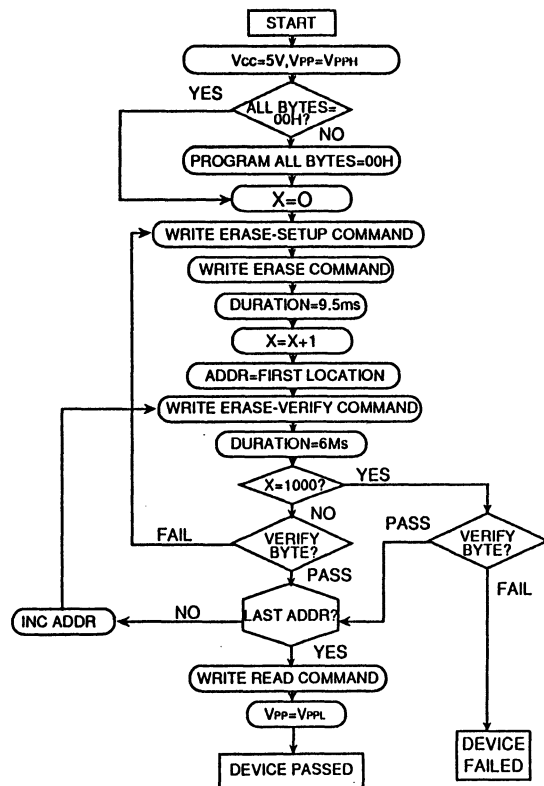
Command	Bus Cycles Req'd	First Bus Cycle			Second Bus Cycle		
		Mode	Address	Data	Mode	Address	Data
Read Memory	1	Write	X	0000H	—	—	—
Set-up Program/Program	2	Write	X	0040H	Write	PA	PD
Program Verify	2	Write	X	00C0H	Read	X	PVD
Set-up Erase/Erase	2	Write	X	0020H	Write	X	0020H
Erase Verify	2	Write	EVA	00A0H	Read	X	EVD
Reset	2	Write	X	FFFFH	Write	X	FFFFH
Read Device Identifier Code	2	Write	X	0090H	Read	DIA	DID

PA = Programmed Address : Address is latched on the falling edge of  $\overline{WE}$ .  
 EVA=Erase-Verified Address : Address is latched on the falling edge of  $\overline{WE}$ .  
 DIA= Device Identifier Address  
 PD= Programmed Data : Data is latched on the rising edge of  $\overline{WE}$ .  
 PVD= Program-Verified Data  
 EVD= Erase-Verified Data  
 DID= Device Identifier Data





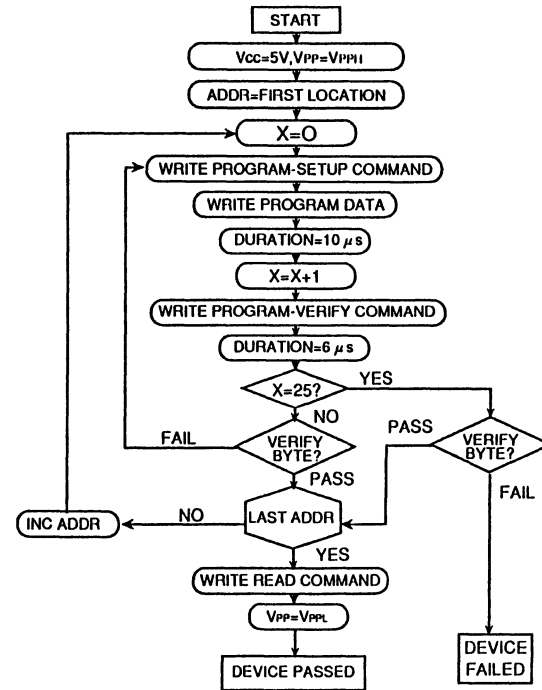
### Flash EEPROM Erase Algorithm Flowchart



68



### Flash EEPROM Programming Algorithm Flowchart



## 64K CMOS EEPROM (M5M28C64AP)

### Features

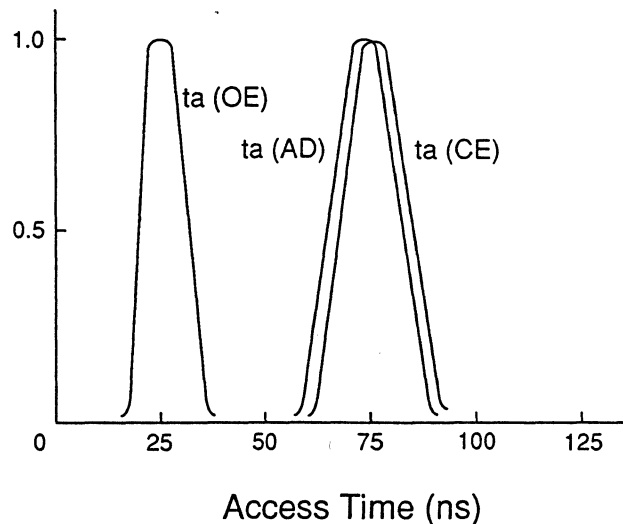
- |                           |  |
|---------------------------|--|
| 1) Organization           | 8Kx8bit, 28pin DIP (JEDEC pinout)  |
| 2) High Speed access time | 150ns/200ns (max.)   |
| 3) Low Power              | 165mW (Active)/5.5mW (Standby)   |
| 4) Write Operation        | 32 Byte Page Mode Write<br>Data Polling  |
| 5) High Endurance         | 10000 Erase/Write<br>10Years Data Retention  |
| 6) Package                | M5M28C64AP ..... 28pin DIP<br>M5M28C64AFP ..... 28pin SOP<br>M5M28C64AVP,RV ..... 28pin TSOP |

### Technology

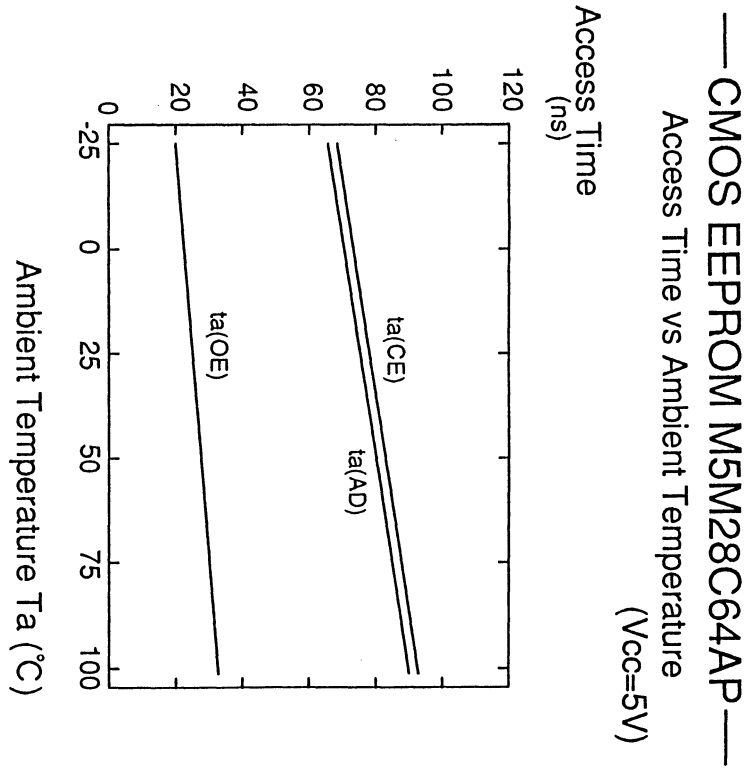
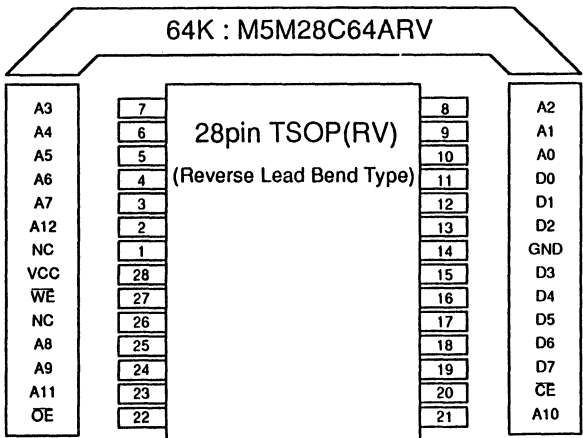
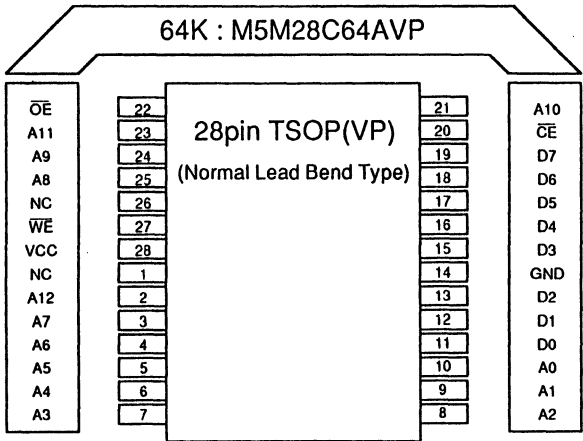
- |  |                         |
|--|-------------------------|
| 1) High performance Si-gate N-well CMOS      | 1.2 $\mu$ m design rule |
| 2) Low resistance material                   | MoSi                    |
| 3) Built-in ECC circuit for high reliability |                         |

## — CMOS EEPROM M5M28C64AP —

Normalized Distribution of Access Time  
(V<sub>cc</sub>=5.0V, T<sub>a</sub>=25°C)



### EEPROM Pin Configurations (TSOP)



**Comparison Table of Mitsubishi Mask ROM**

Memory capacity	4M		8M		16M
Organization	512k×8/ 256k×16	512k×8	1M×8/ 512k×16	1M×8	2M×8/ 1M×16
Type name	M5M23400A	M5M23401A	M5M23800	M5M23801	M5M23160
Process technology	CMOS 1.1 μm	CMOS 1.1 μm	CMOS 0.8 μm	CMOS 0.8 μm	CMOS 0.8 μm
Access time (ns)	150	150	150	150	150
Supply voltage (V)	5	5	5	5	5
Active current (mA)	30	30	50	50	50
Stand by current (mA)	0.1	0.1	0.1	0.1	0.1
Pins/ Package * Width(mil)	40P(600) 40FP(525) 40VP,RV	32P(600) 32FP(525) 40VP,RV	42P(600) 44FP(600) 48VP,RV	32P(600) 32FP(525) 40VP,RV	42P(600) 44FP(600) 48VP,RV
Note					

Package\* ---- P:DIP , FP:SOP , VP/RV:TSOP

**16M Mask ROM**
**Target Features**

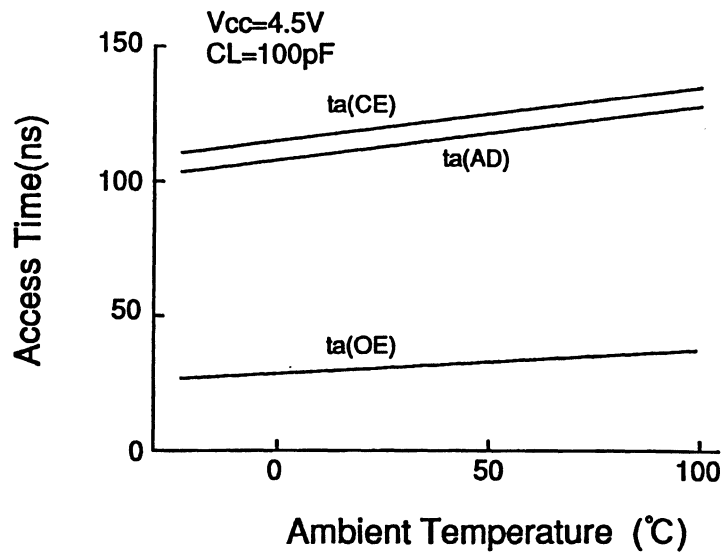
- 1) Organization M5M23160 . . . 2M×8/1M×16
- 2) High Speed Access Time 150ns(max.)
- 3) Low Power 50mA(Active)  
0.1mA(Standby)
- 4) Package M5M23160P . . . 42pin DIP(600mil)  
M5M23160FP . . . 44pin SOP(600mil)  
M5M23160VP/RV . . . 48pin TSOP(12×18mm)

**Technology**

- 1) High performance Si-gate twin well CMOS
- 2) Design rule 0.8 μm
- 3) Built-in ECC circuit for high yield

## 16M bit Mask ROM M5M23160P,FP,VP,RV

### Access Time vs Ambient Temperature



## 8M Mask ROM

### Target Features

1) Organization	M5M23800	• • • 1M×8/512K×16
	M5M23801	• • • 1M×8
2) High Speed Access Time		150ns(max.)
3) Low Power		50mA(Active) 0.1mA(Standby)
4) Package	M5M23800P	• • • 42pin DIP(600mil)
	M5M23800FP	• • • 44pin SOP(600mil)
	M5M23800VP/RV	• • • 48pin TSOP(12×18mm)
	M5M23801P	• • • 32pin DIP(600mil)
	M5M23801FP	• • • 32pin SOP(525mil)
	M5M23801VP/RV	• • • 40pin TSOP(10×14mm)

### Technology

- 1) High performance Si-gate twin well CMOS
- 2) Design rule 0.8 μm
- 3) Built-in ECC circuit for high yield



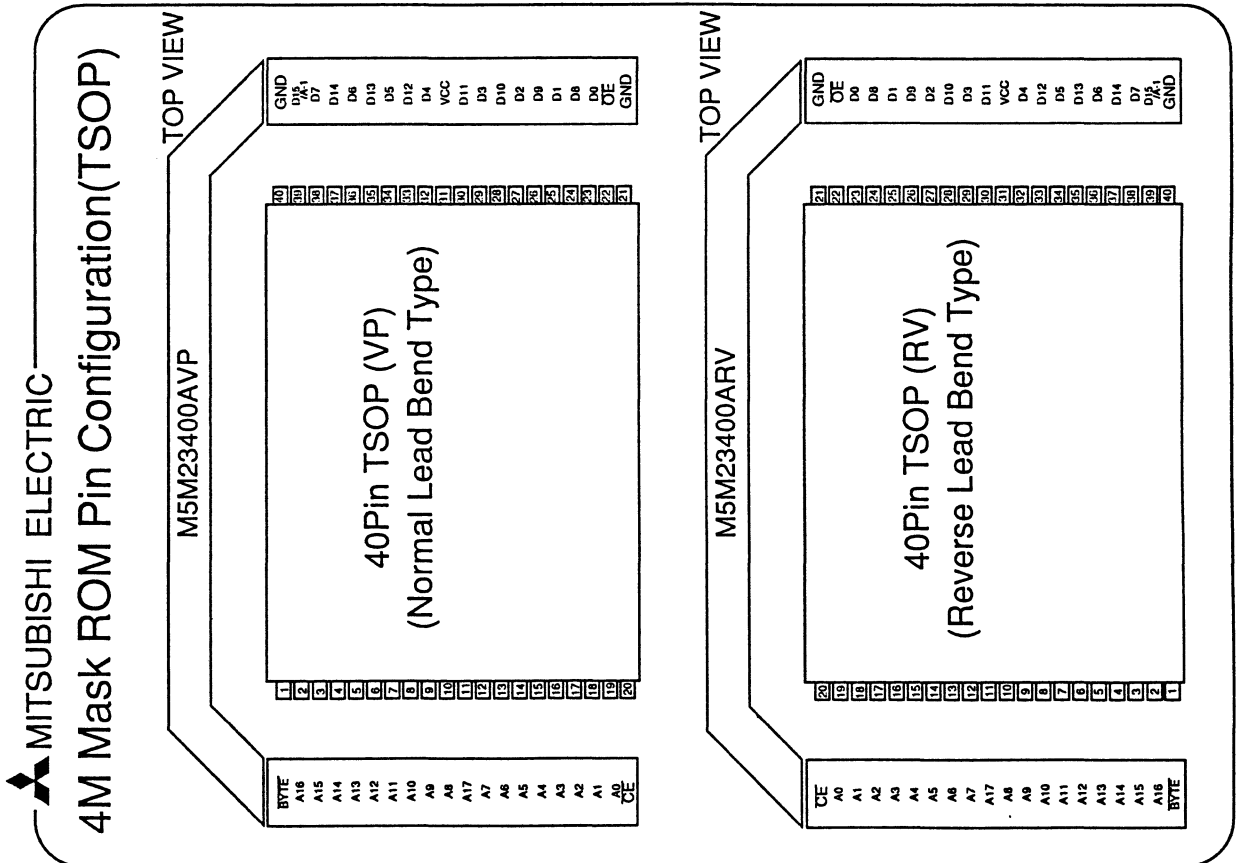
## 4M Mask ROM

### Features

1) Organization	M5M23400A	... 512Kx8/256Kx16
	M5M23401A	... 512Kx8
2) High Speed Access Time		150ns(max.)
3) Low Power		30mA(Active)/0.1mA(Standby)
4) Package	M5M23400AP	... 40pin DIP(600mil)
	M5M23400AFP	... 40pin SOP(525mil)
	M5M23400AVP/RV	... 40pin TSOP(10x14mm)
	M5M23401AP	... 32pin DIP(600mil)
	M5M23401AFP	... 32pin SOP(525mil)
	M5M23401AVP/RV	... 40pin TSOP(10x14mm)

### Technology

- 1) High performance Si-Gate CMOS
- 2) Design rule 1.1  $\mu$ m



## Versatile Memory M6M72561J, J-I

### 1. Temperature range

M6M72561J

0 ~ 70°C

M6M72561J-I

- 40 ~ 85°C

### 2. Package

68PLCC

### 3. Function

OTPROM : Organization ..... 32Kx8 / 16Kx16 bit

Access time ..... 200ns

Programming... 27C256 Compatible(Socket Adapter)

SRAM : Organization..... 2Kx8 / 1Kx16 bit

Access time .....150ns

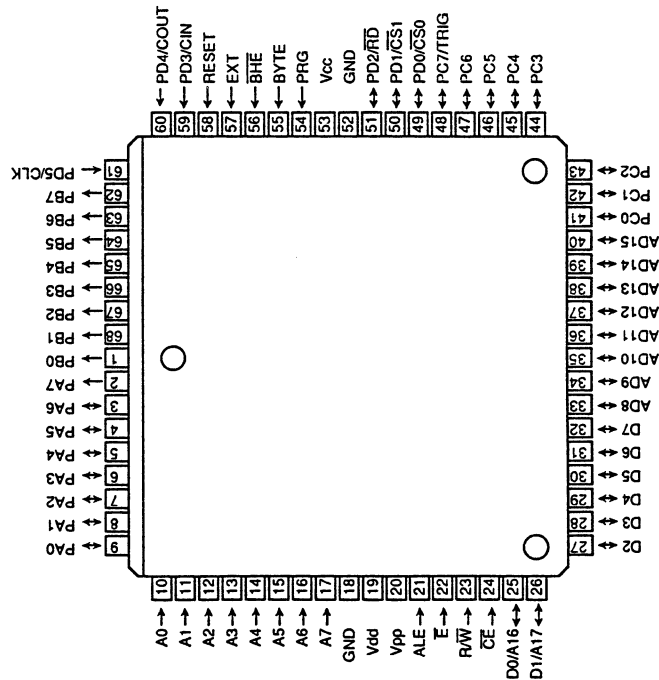
Counter : Presetable 8 bit up - counter

I / O Port : Input Port..... 8 + 6 bit

Output Port ..... 8 bit

I / O Port ..... 8 bit

## M6M72561J / J-I Pin Configuration





## Technical Strategy of Module

High Performance

DRAM Module:60ns  
Fast SRAM Module:45ns

High Density

1M×36bit DRAM  
4M×9bit DRAM  
512K×8bit SRAM.  
(Compatible  
4MSRAM DIP)

New Concept

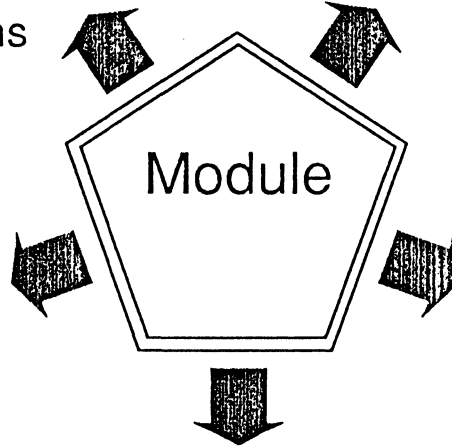
Stacked Memory  
(Fast SRAM)  
Module for SMT

Various Package

SIM,SIP,ZIMP  
DIP

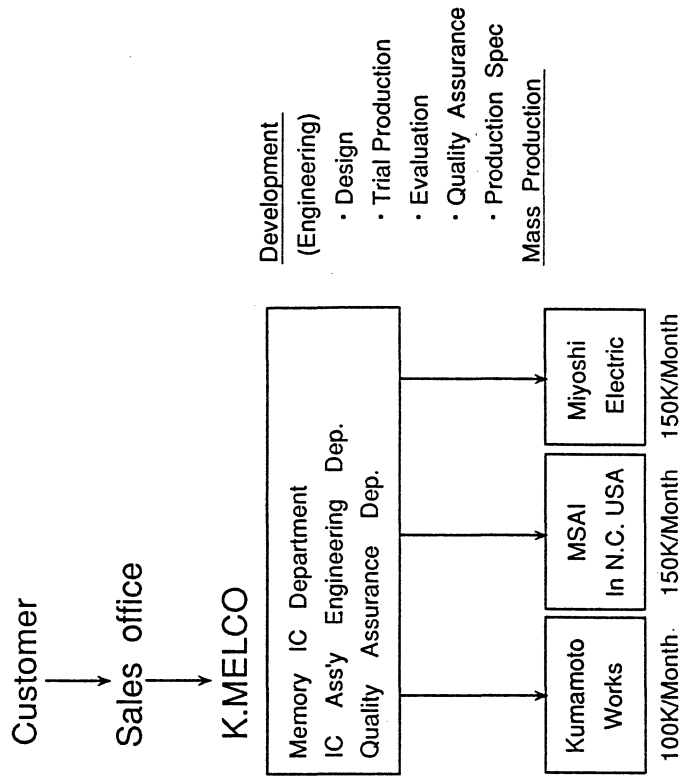
As Memory

Pseudo-Pseudo SRAM Module  
Custom Module



MELCO

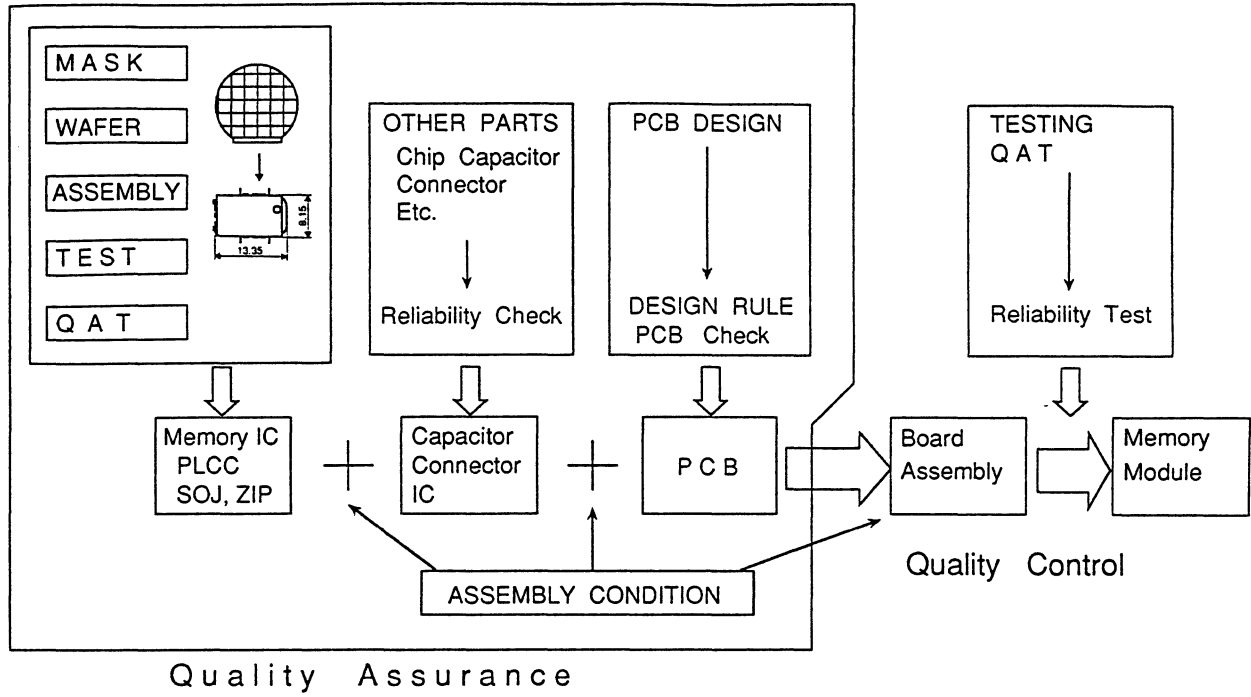
Memory Module  
Development and Production Route



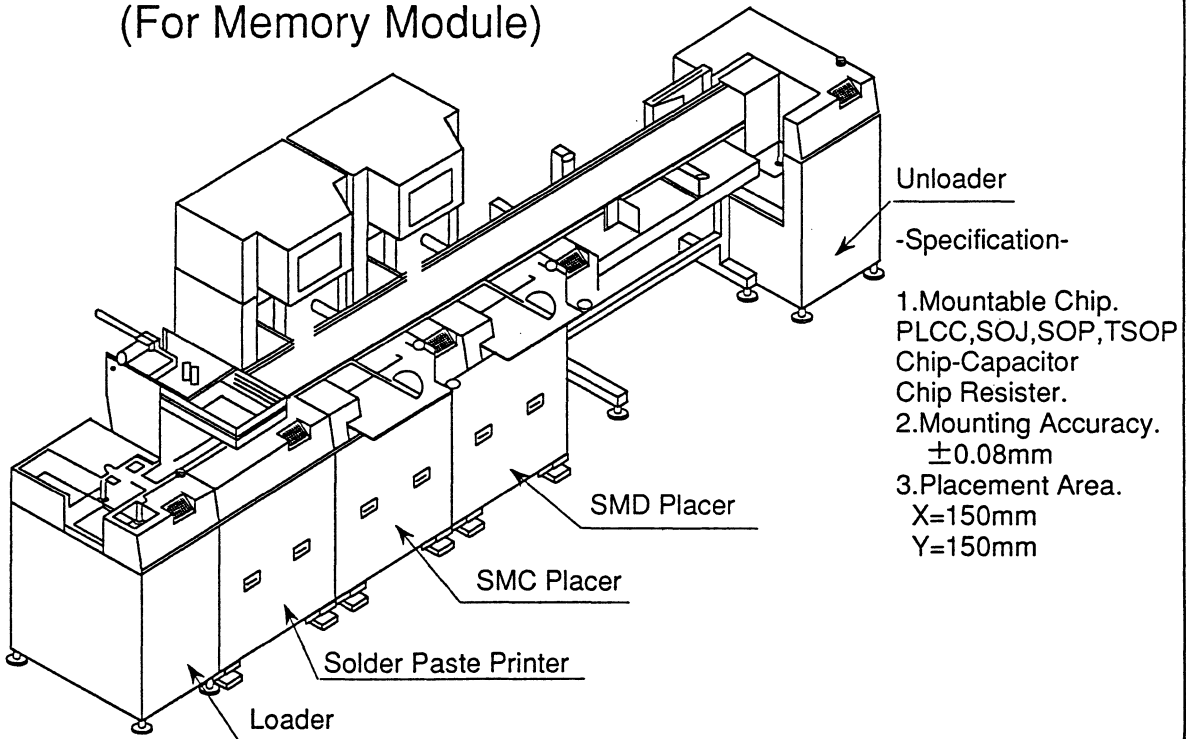
Concept of  
Mitsubishi Surface Mount Technology

- \* High reliable SMD memory IC is mounted
- \* Full automatic chip placement system
- \* Accurate SMD placement with pattern recognition system
- \* AIR Reflow soldering
- \* Ultrasonic and vapor phase cleaning
- \* Total quality control from wafer process to memory Module

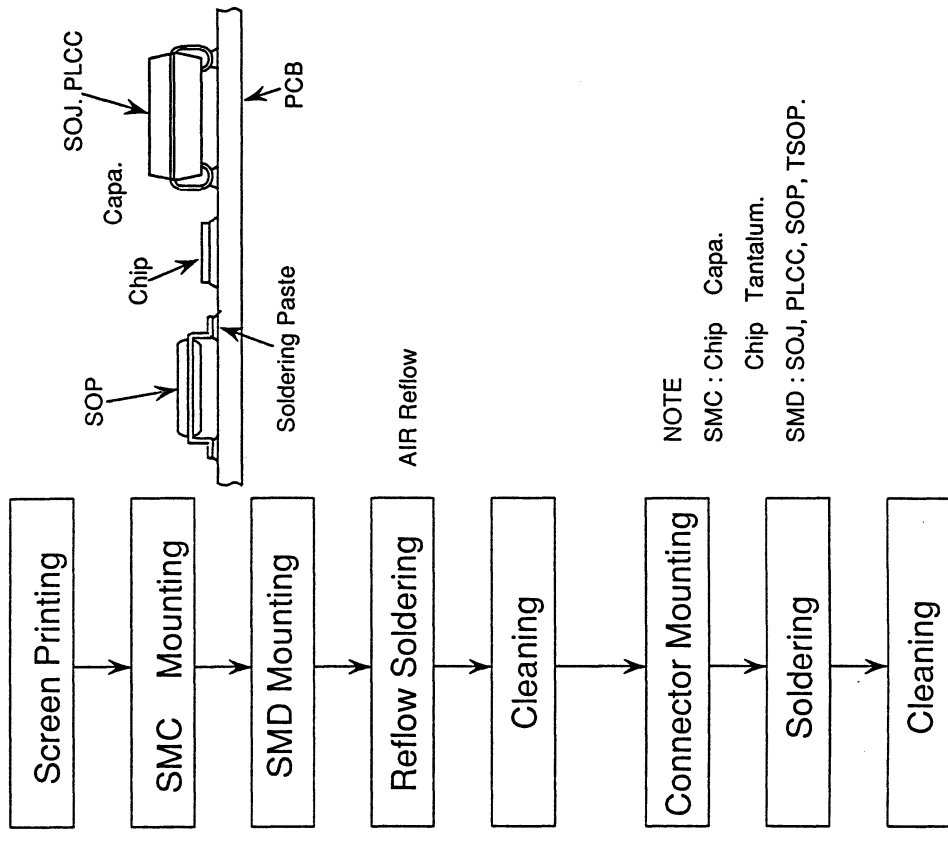
## Total Quality Assurance of Memory Module



## Automatic Chip Placement System (For Memory Module)



### Assembly Flow Chart Of Memory Module



### Mitsubishi Memory Module Series



Type		Pin	Density	DRAM	SRAM	ROM	VRAM
SIMM	2.54 mm	30	256K X 9	MH25609BAJ			
			1M X 9	MH1M09B0J MH1M09A0AJ			
			4M X 9	MH4M09A0J			
			256K X 8		MH25608S1N		
	1.27 mm	64	512K X 8		MH51208SN		
			256K X 36	MH25636BJ			
			512K X 36	MH51236BJ			
			1M X 36	MH1M36BJ			
			2M X 36	MH2M36CJ			
			2M X 40	MH2M40AJ			
SIP	2.54 mm	30	256K X 9	MH25609BAJA			
			1M X 9	MH1M09B0JA MH1M09A0AJA			
			4M X 9	MH4M09A0JA			
			DIP (600mil)	2.54 mm	32	128K X 8	
256K X 8		MH25608TNA					
512K X 8		MH51208TNA MH51208ANA MH51208UNA					
34	512K X 8					MH51208RNA *	
36	1M X 8				MH1M08TNA*		
	2M X 8				MH2M08TNA*		
40	512K X 8	MH51208PNA					
42	256K X 16					MH25616RNA	
	2M X 8	MH2M08PNA*					
44	512K X 16					MH51216RNA	
46	256K X 16	MH25616PNA					
ZIMP	1.27 mm	46	128K X 16				MH12816JZ
		64	64K X 32		MH6432NZ		

\*: under development

## X36bit Memory Module, Organization LIST

Height	Words	TYPE NAME	Thickness	Loaded Memory IC				Access time	Comment
				Main		Parity			
25.4mm (1 inch)	256K	MH25632BJ	5.08	M5M44256BJ	8pcs	-----	-----	70, 80,100	W/B Module
		MH25636BJ	5.08	M5M44256BJ	8pcs	M5M4256AJ	4pcs	85,100,120	
		MH26636BJ	5.08	M5M44256BJ	8pcs	M5M44266BJ	1pcs	80,100	
	512K	MH51232BJ	8.5	M5M44256BJ	16pcs	-----	-----	70, 80,100	W/B Module
		MH51236BJ	8.5	M5M44256BJ	16pcs	M5M4256AJ	8pcs	85,100,120	
		MH52236BJ	8.5	M5M44256BJ	16pcs	M5M44266BJ	2pcs	80,100	
	1M	MH1M36DJ	8.5	M5M44400J	8pcs	M5M41000BJ	4pcs	80,100	TSOP Module W/B Module
		MH1M36EJ	5.08	M5M44400AJ	8pcs	M5M41000BVP	4pcs	80,100	
		MH1M36FJ	5.08	M5M44400AJ	8pcs	M5M44410AJ	1pcs	80,100	
	2M	MH2M36EJ	8.5	M5M44400AJ	16pcs	M5M41000BVP	8pcs	80,100	TSOP Module W/B Module
		MH2M36FJ	8.5	M5M44400AJ	16pcs	M5M44410AJ	2pcs	80,100	
	31.75 (1.25)	1M	MH1M36BBJ	4.3	M5M41000BVP	32pcs	M5M41000BVP	4pcs	70, 80,100
MH1M36CJ			5.08	M5M44400J	8pcs	M5M41000BJ	4pcs	80,100	
32.77 (1.29)	4M	MH2M36CJ	8.5	M5M44400J	16pcs	M5M41000BJ	8pcs	80,100	
		MH4M36AJ	8.5	M5M44400AJ	32pcs	M5M44400AJ	4pcs	80,100	
40.64 (1.6)	1M	MH1M36BJ(SC)	8.5	M5M41000BJ	32pcs	M5M41000BJ	4pcs	70, 80,100	Solder Coat gold plated
		MH1M36BJ(g)	8.5	M5M41000BJ	32pcs	M5M41000BJ	4pcs	70, 80,100	

M5M4256AJ :18PIN PLCC ,256KD (X1) page  
 M5M44256BJ :26PIN 300mil SOJ,1MD (X4) Fast page  
 M5M44266BJ :26PIN 300mil SOJ,1MD (X4) Fast page, W/B  
 M5M41000BJ :26PIN 300mil SOJ,1MD (X1) Fast page  
 M5M41000BVP:24PIN TSOP ,1MD (X1) Fast page  
 M5M44400J :26PIN 350mil SOJ,4MD (X4) Fast page  
 M5M44400AJ :26PIN 300mil SOJ,4MD(X4) Fast page  
 M5M44410AJ :26PIN 300mil SOJ,4MD(X4) Fast page, W/B

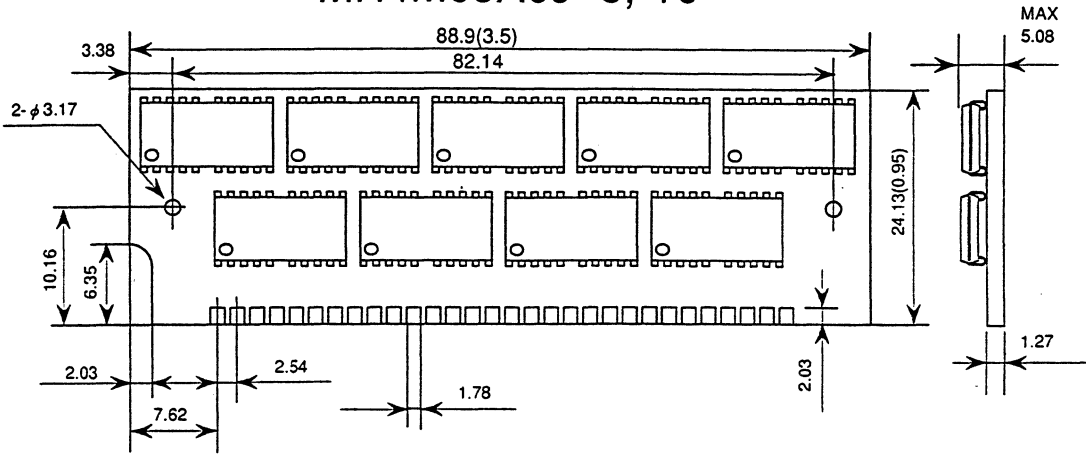
## SRAM Module Organization LIST

	Words	Bits	DEVICE NAME	Pin Number	Access time (ns)	Stand-by *2 current (μA)	Loaded IC	
							Memory IC	Other
SIMM	256K	8	MH25608SIN	35	70,85,100	200	M5M5256BFP 8pcs	
	512K	8	MH51208SN	64 **	70,85,100	400	M5M5256BFP 16pcs	
DIP (600mil)	128K	8	MH12808TNA	32	85,100,120	100	M5M5256BFP 4pcs	M74HCT138-1FP 1pcs
	256K	8	MH25608TNA	32	85,100,120	200	M5M5256BRV/VP 8pcs	M74HC138VP 1pcs
			MH51208TNA	32	85,100,120	400	M5M5256BRV/VP 16pcs	M74HC138VP 2pcs
	512K	8	MH51208ANA	32	85,100,120	undecided	M5M51008VP/RV 4pcs	M74HC138VP 1pcs
			MH51208UNA	32	85,100,120	undecided	M5M51008FP 4pcs	M74HC138VP 1pcs
			MH51208PNA	40	8MHZ,10MHZ	3.5mA **	M5M44256BJ 4pcs	M66200FP 1pcs M66213FP 2pcs
	1M	8	MH1M08TNA **	36	85,100,120	undecided	M5M51008VP/RV 8pcs	M74HC138VP 1pcs
			MH2M08TNA **	36	85,100,120	undecided	M5M51008VP/RV 16pcs	M74HC138VP 2pcs
	2M	8	MH2M08PNA **	42	8MHZ,10MHZ	undecided	M5M44400J 4pcs	M66200FP 1pcs M66213FP 2pcs
								256K
ZIMP	64K	32	MH6432NZ	64	15,20	undecided	M5M5258BJ 4pcs	

\*1:1.27mm lead pitch, \*2:Vcc=3V, \*3:Vcc=5.5V, \*4:under development

M5M5256BFP :256KSRAMfSOP  
 M5M5256BRV/VP :256KSRAM TSOP  
 M5M51008VP/RV :1M SRAM TSOP  
 M5M44256BJ :1M DRAM (X4) SOJ  
 M5M44400J :4M DRAM (X4) SOJ  
 M74HCT138-1FP :Decoder SOP  
 M74HC138VP :Decoder VSOP  
 M66200FP :D RAM Controller SOP  
 M66213FP :ADDRESS Buffer SOP

### 4MX9 DRAM Memory Module PIN configuration MH4M09A0J -8,-10

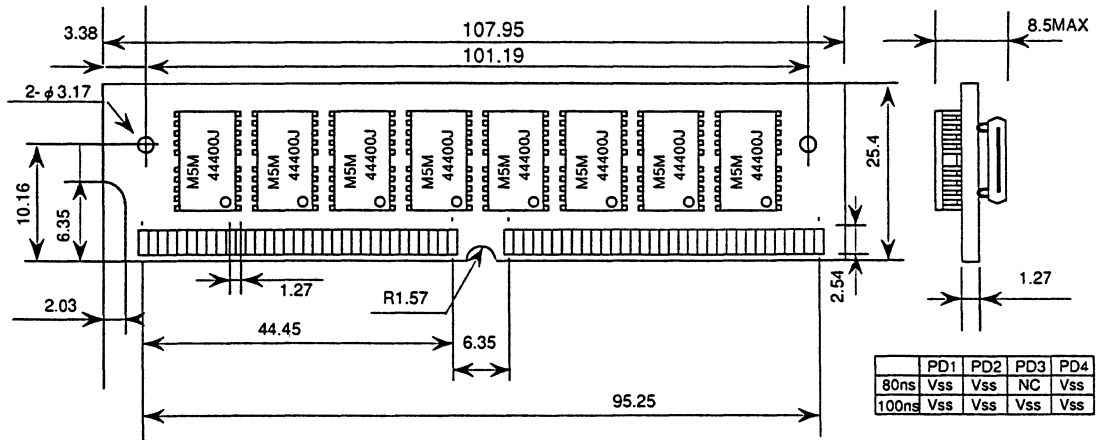


1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30

Vcc CAS DO0 A0 A1 DO1 A2 A3 A3 Vss DQ2 A4 A5 DO3 A6 A7 DO4 A8 A9 A9 A10 A10 DO5 W Vss DO6 NC DO7 DO7 QP, RAS CASP DP Vcc

- chip carrier M5M44100J -8,-10
- socket Molex Type 78810  
AMP Type 643930

### 1MX36 DRAM Memory Module PIN configuration MH1M36DJ -8,-10



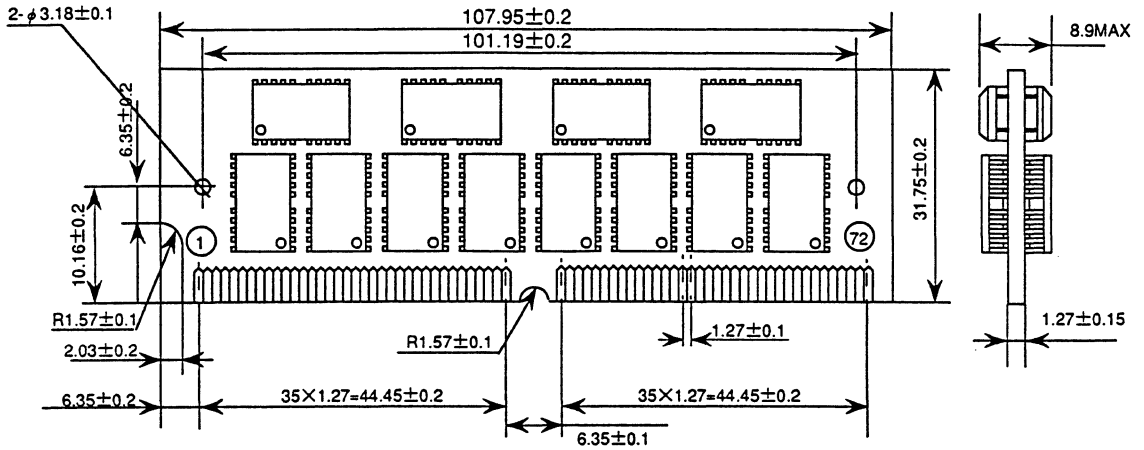
	PD1	PD2	PD3	PD4
80ns	Vss	Vss	NC	Vss
100ns	Vss	Vss	Vss	Vss

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72

Vss DO0 DO16 DO17 DO18 DO19 VDD NC A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A9 A10 A10 A11 A11 A12 A12 A13 A13 A14 A14 A15 A15 A16 A16 A17 A17 A18 A18 A19 A19 A20 A20 A21 A21 A22 A22 A23 A23 A24 A24 A25 A25 A26 A26 A27 A27 A28 A28 A29 A29 A30 A30 A31 A31 A32 A32 A33 A33 A34 A34 A35 A35 A36 A36 A37 A37 A38 A38 A39 A39 A40 A40 A41 A41 A42 A42 A43 A43 A44 A44 A45 A45 A46 A46 A47 A47 A48 A48 A49 A49 A50 A50 A51 A51 A52 A52 A53 A53 A54 A54 A55 A55 A56 A56 A57 A57 A58 A58 A59 A59 A60 A60 A61 A61 A62 A62 A63 A63 A64 A64 A65 A65 A66 A66 A67 A67 A68 A68 A69 A69 A70 A70 A71 A71 A72 A72

- chip carrier M5M44400J -8,-10
- socket Molex Typ 78841-7202  
M5M41000BJ -8,-10 TI TS820102B-72-00

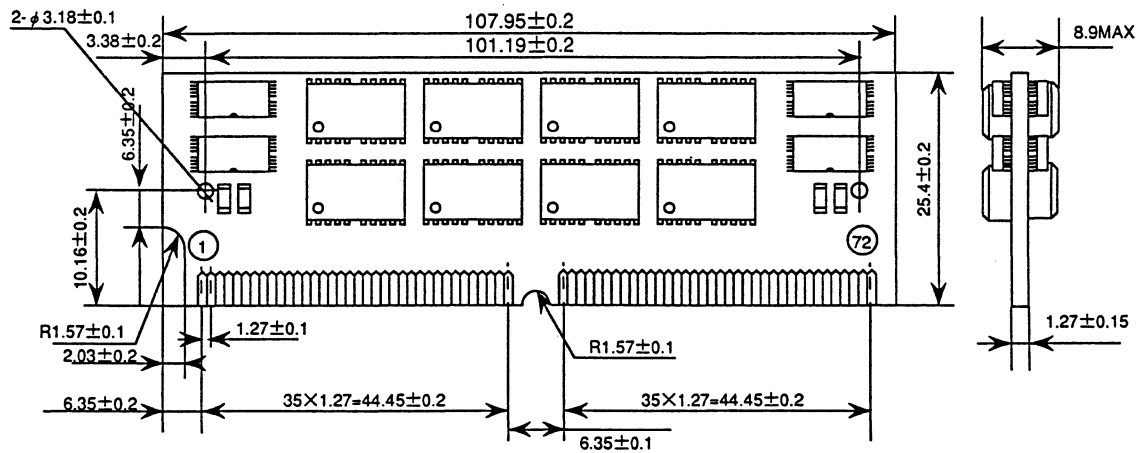
## 2M×36 DRAM Memory Module PIN configuration MH2M36CJ -8,-10



1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72																																											
V <sub>16</sub>	DO0	DO16	DO1	DO17	DO2	DO18	DO3	DO19	DO4	DO20	DO5	DO21	DO6	DO22	DO7	DO23	DO8	DO24	DO9	DO25	DO10	DO26	DO11	DO27	DO12	DO28	DO13	DO29	DO14	DO30	DO15	DO31	DO16	DO32	DO17	DO33	DO18	DO34	DO19	DO35	DO20	DO36	DO21	DO37	DO22	DO38	DO23	DO39	DO24	DO40	DO25	DO41	DO26	DO42	DO27	DO43	DO28	DO44	DO29	DO45	DO30	DO46	DO31	DO47	DO32	DO48	DO33	DO49	DO34	DO50	DO35	DO51	DO36	DO52	DO37	DO53	DO38	DO54	DO39	DO55	DO40	DO56	DO41	DO57	DO42	DO58	DO43	DO59	DO44	DO60	DO45	DO61	DO46	DO62	DO47	DO63	DO48	DO64	DO49	DO65	DO50	DO66	DO51	DO67	DO52	DO68	DO53	DO69	DO54	DO70	DO55	DO71	DO56	DO72

- chip carrier M5M44400J -8,-10  
M5M41000BJ -8,-10
- socket Molex Type 78841-7202  
TI TS820102B-72-00

## 2M×36 DRAM Memory Module PIN configuration MH2M36EJ -6,-7,-8,-10

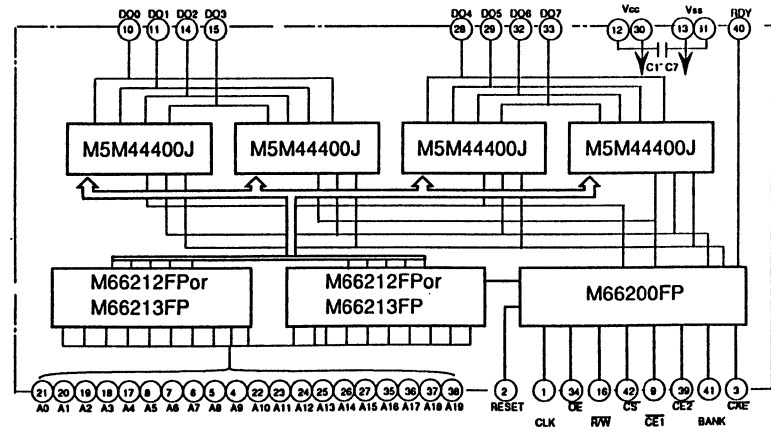
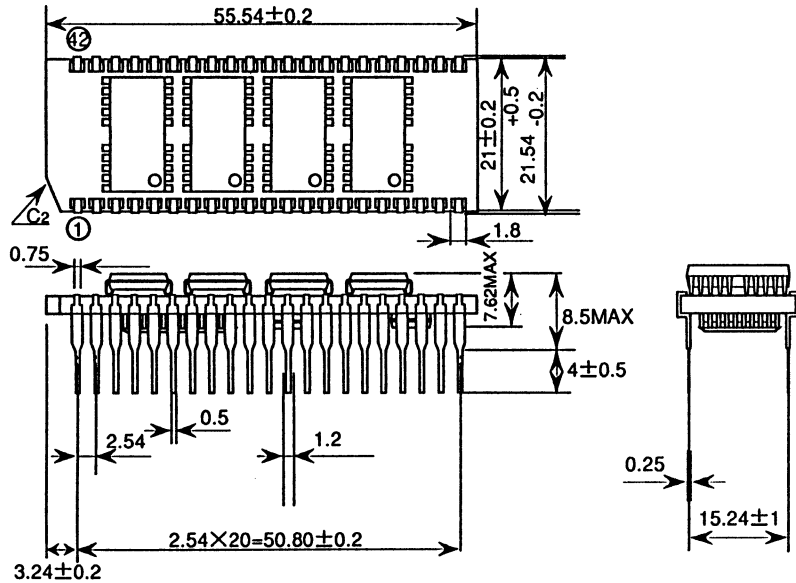


1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72																																											
V <sub>16</sub>	DO0	DO16	DO1	DO17	DO2	DO18	DO3	DO19	DO4	DO20	DO5	DO21	DO6	DO22	DO7	DO23	DO8	DO24	DO9	DO25	DO10	DO26	DO11	DO27	DO12	DO28	DO13	DO29	DO14	DO30	DO15	DO31	DO16	DO32	DO17	DO33	DO18	DO34	DO19	DO35	DO20	DO36	DO21	DO37	DO22	DO38	DO23	DO39	DO24	DO40	DO25	DO41	DO26	DO42	DO27	DO43	DO28	DO44	DO29	DO45	DO30	DO46	DO31	DO47	DO32	DO48	DO33	DO49	DO34	DO50	DO35	DO51	DO36	DO52	DO37	DO53	DO38	DO54	DO39	DO55	DO40	DO56	DO41	DO57	DO42	DO58	DO43	DO59	DO44	DO60	DO45	DO61	DO46	DO62	DO47	DO63	DO48	DO64	DO49	DO65	DO50	DO66	DO51	DO67	DO52	DO68	DO53	DO69	DO54	DO70	DO55	DO71	DO56	DO72

- chip carrier M5M44400AJ -6,-7,-8,-10  
M5M41000BJ -6,-7,-8,-10
- socket Molex Type 78841-7202  
TI TS820102B-72-00

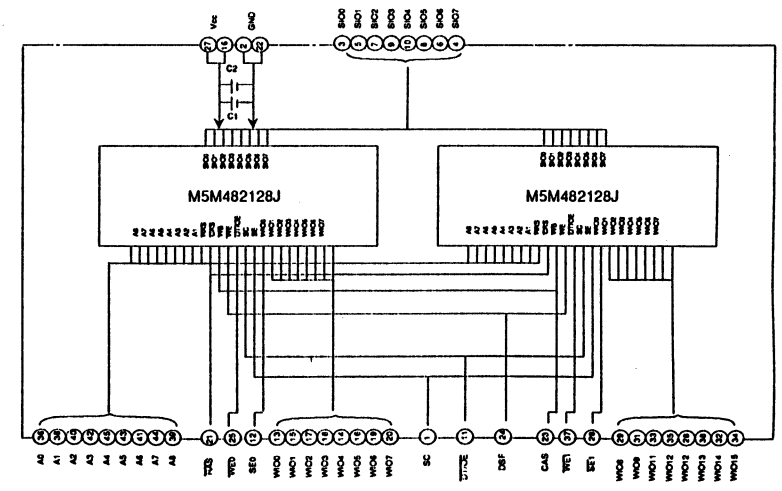
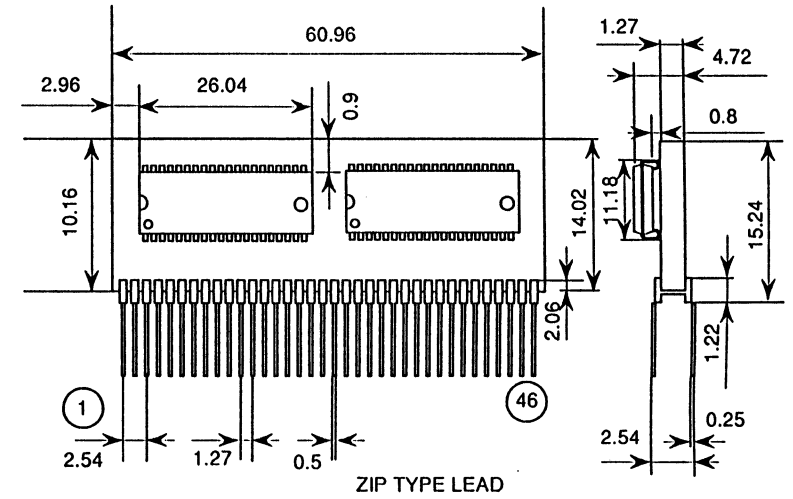


### 2M×8 Pseudo-Pseudo SRAM Module MH2M08PNA PIN configuration



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### 128K×16 Video RAM Module MH12816JZ PIN configuration, Dimension







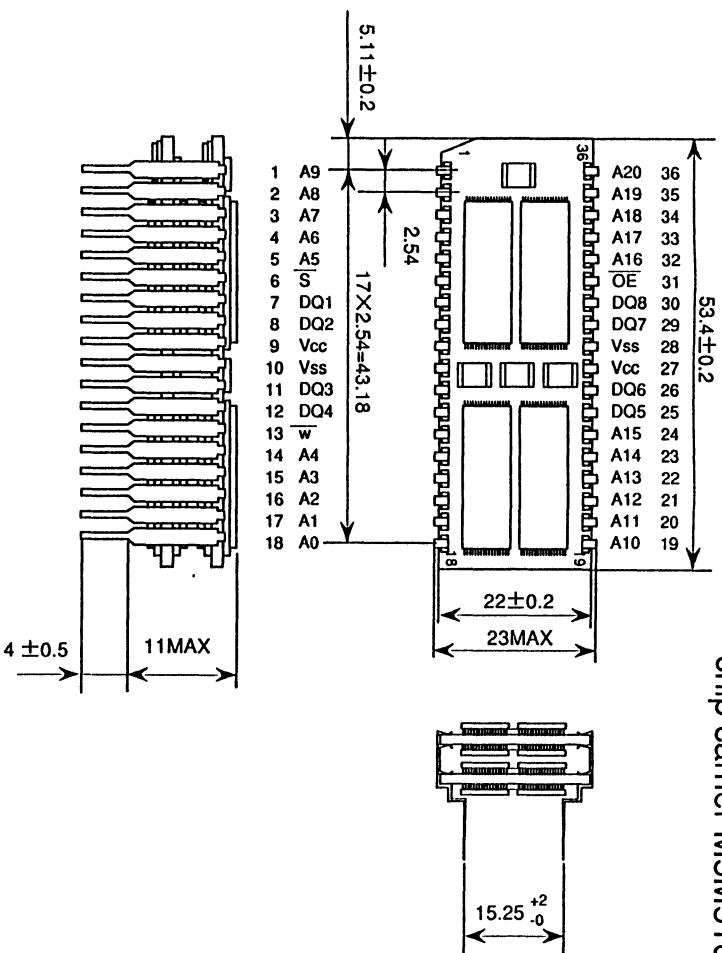
MITSUBISHI ELECTRIC



# 2MX8 SRAM Memory Module PIN configuration

## MH2M08TNA -85, 10, 12

chip carrier M5M51008VP, RV

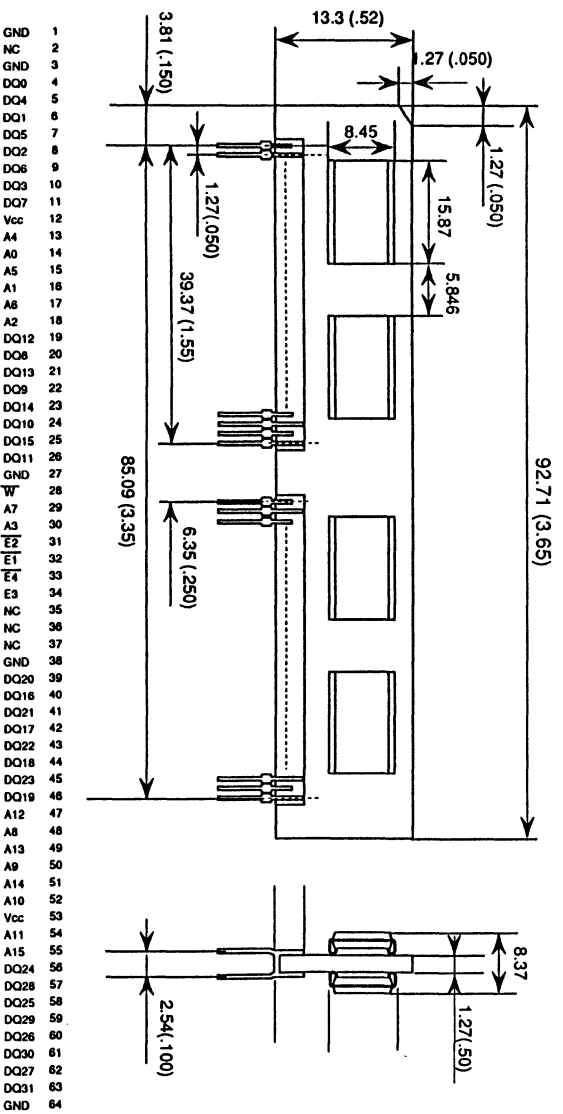


MITSUBISHI ELECTRIC

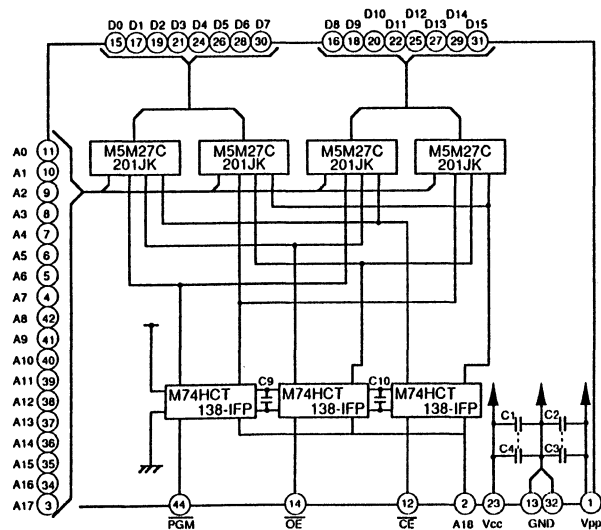
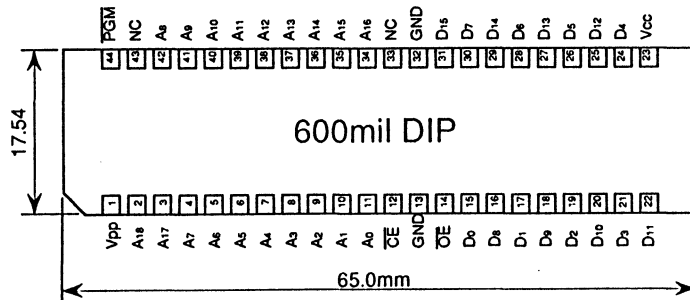


# MH6432NZ Fast SRAM Module PIN configuration, Dimension

chip carrier M5M5258BJ 8pcs

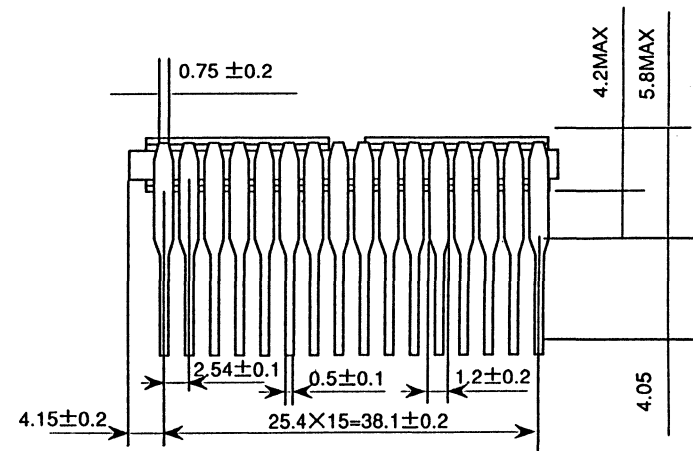
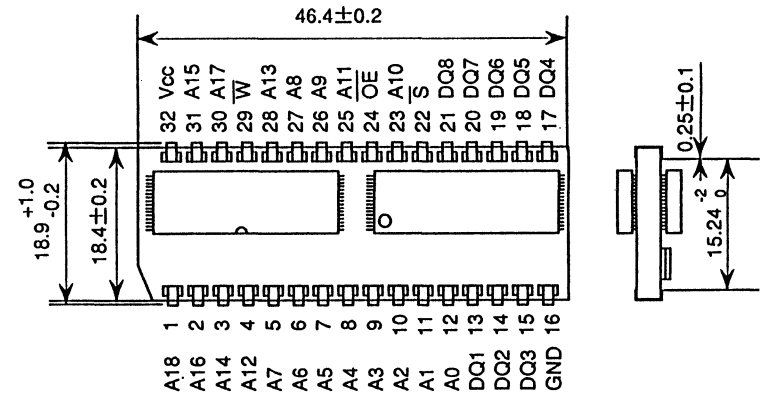


512K×16 EPROM Module  
MH51216RNA PIN Configuration, Dimension



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512K×8 SRAM Memory Module  
PIN configuration, Dimension  
MH51208ANA -85L,-10L,-12L,-15L  
-85H,-10H,-12H,-15H



chip carrier M5M51008VP, RV

## SOCKET FOR TSOP

Type of Device	Package Dimension	Test/Burn-In Socket	Burn-In Socket
M5M5178VP,RV(64K SRAM) M5M5256BVP,RV(256K SRAM) M5M27C256AVP,RV(256K OTPROM) M5M28C64AVP,RV(64K E <sup>2</sup> PROM)	28pin(Mitsubishi Original)	IC51-0282-673-1 *1	
M5M41000BVP,RV M5M44256BVP,RV (1M DRAM)	24pin(Type I, 6×16,0.5mmpitch)	IC51-0242-1006-1(20) *1	CTP2024001A *2
M5M51008VP,RV(1M SRAM)	32pin(Type I, 8×20,0.5mmpitch)	IC51-0322-1207-1 *1	CTP032-002A *2
M5M27C101VP,RV(1M OTPROM) M5M27C102VP,RV( / ) M5M27C201VP,RV(2M OTPROM) M5M27C202VP,RV( / ) M5M23400AVP,RV(4M MaskROM) M5M23401AVP,RV( / )	40pin(Type I, 10×14,0.5mmpitch)	IC51-0402-965-1 *1	IC162-0402-041 *1
M5M44100ATP,RT M5M44400ATP,RT (4M DRAM)	26pin(Type II, 300mil,1.27mmpitch)	—	CTP2026003B *2

\*1 YAMAICHI ELECTRIC MFG.CO.,LTD. TEL OSAKA (06) 396 - 6191, CA U.S.A 408 - 452 - 0797

\*2 TEXAS INSTRUMENTS JAPAN LTD. TEL OSAKA (06) 204 - 1882, MASS U.S.A 508 - 699 - 5247

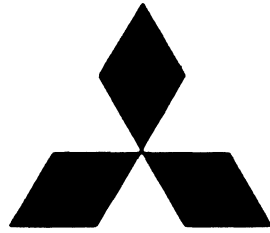
Burn-In Socket means a open top type (No Force Insertion)  
Test/Burn-In socket means a socket with lid.



Notes:

Notes:

Notes:



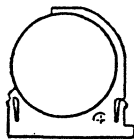
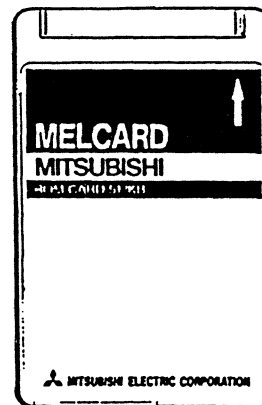
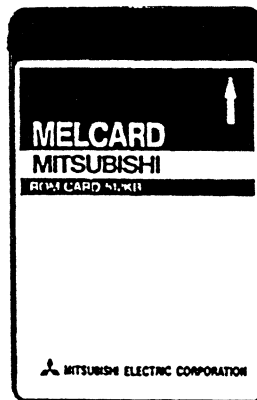
# MITSUBISHI

## MEMORY CARD

SRAM

OTPROM

MASK ROM



January 1991

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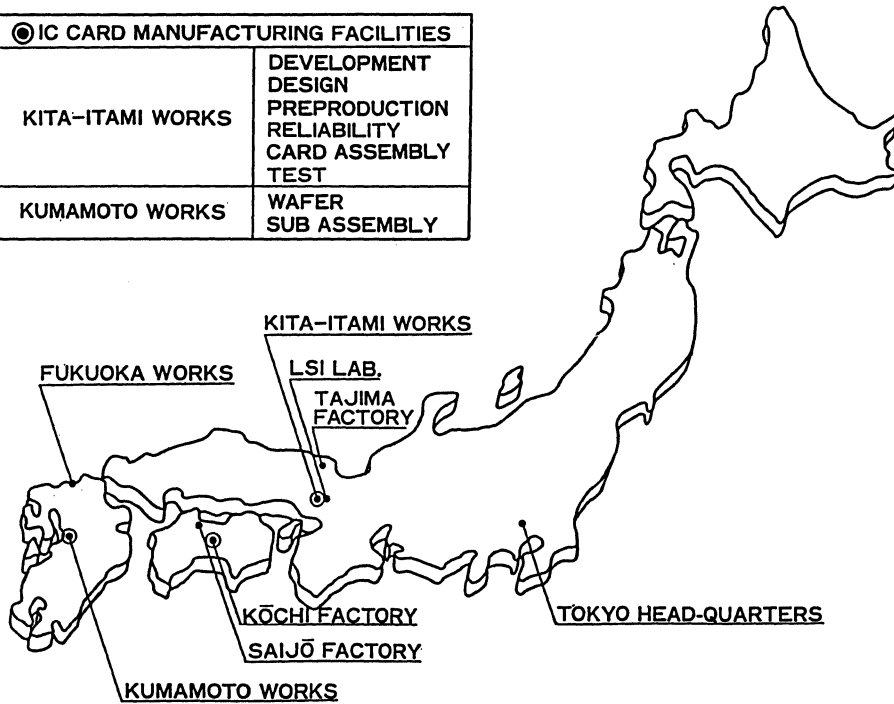
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· EEPROM CARD .....	40
· DRAM CARD .....	42
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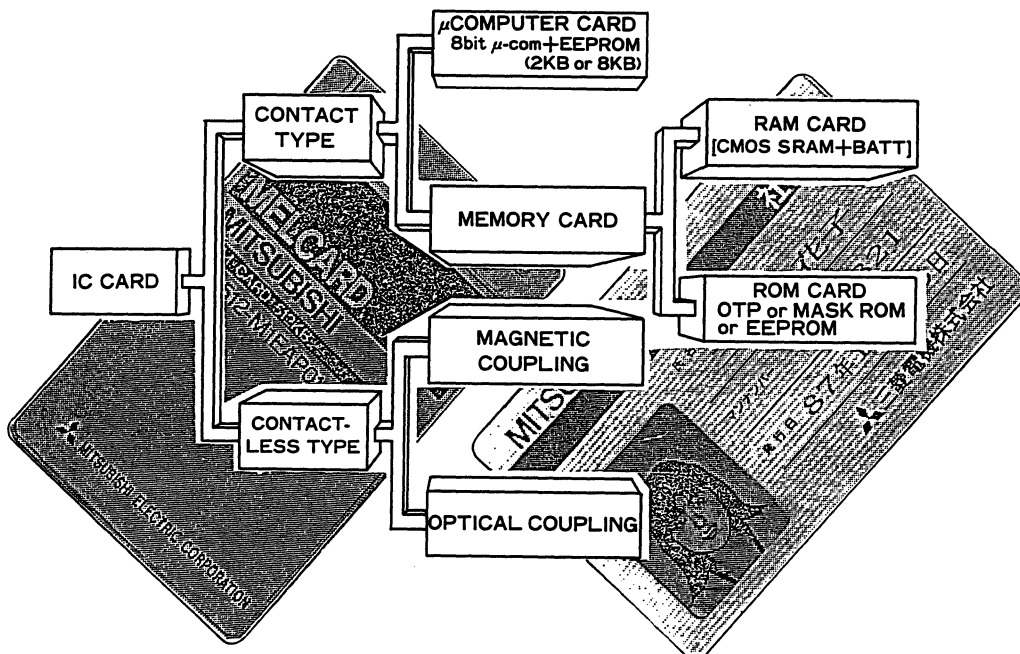


# LOCATION OF MANUFACTURING FACILITIES

◎ IC CARD MANUFACTURING FACILITIES	
KITA-ITAMI WORKS	DEVELOPMENT DESIGN PREPRODUCTION RELIABILITY CARD ASSEMBLY TEST
KUMAMOTO WORKS	WAFER SUB ASSEMBLY



# CLASSIFICATION



2

Rev

## MITSUBISHI MEMORY CARD ( I )

Products				Type name	Access (ns)	Other	Sample	Production	Note		
S t a t i c  R A M	2 P  60 pin	8 bit	W/O  W P  B M	32KB	MF332A-M4DAPXX	200	W/O buffer	-	Yes		
				32KB	MF332A-MDDAPXX	200		-	Yes		
				64KB	MF364A-M2DAPXX	200	W/O buffer	-	Yes		
				64KB	MF364A-M9DAPXX	200		-	Yes		
				128KB	MF3128-M1DAPXX	200		-	Yes		
				128KB	MF3128-M1EAPXX	250		-	Yes		
				256KB	MF3256-M1DAPXX	200		-	Yes		
				256KB	MF3256-M1EAPXX	250		-	Yes		
				512KB	MF3512-M1DAPXX	200		-	Yes		
				512KB	MF3512-M1EAPXX	250		-	Yes		
	256KB	MF3256-M3EARXX	250	] 4.2t, Built in rechargeable battery	-	Yes					
	512KB	MF3512-M3EARXX	250		-	Yes					
				W/  W P  B M	32KB	MF332A-MADAPXX	200		-	Yes	
					64KB	MF364A-M6DAPXX	200		-	Yes	
					128KB	MF3128-M6DAPXX	200		-	Yes	
					128KB	MF3128-M6EAPXX	250		-	Yes	
					256KB	MF3256-M6DAPXX	200		-	Yes	
					256KB	MF3256-M6EAPXX	250		-	Yes	
					256KB	MF3256-MGDAPXX	200	Low Stand-by	Yes	'91/1Q	Low Stand-by
					256KB	MF3256-MHDAPXX	200	Low Voltage	Yes	'91/1Q	
			512KB		MF3512-M6DAPXX	200		-	Yes		
			512KB		MF3512-M6EAPXX	250		-	Yes		
			512KB	MF3512-MGDAPXX	200	Low Stand-by	Yes	'91/1Q	Low Stand-by		
			512KB	MF3512-MHDAPXX	200	Low Voltage	Yes	'91/1Q			
			1MB	MF31M0-M6DAPXX	200	1Mbit SRAM×8	Yes	'91/1Q			
			2MB	MF32M0-M6DAPXX	200	1Mbit SRAM×16	Yes	'91/1Q			

Note : [Card thickness : 3.4mm unless otherwise noted, Panel material : Metal]

2 P : two-piece connector type,

C/E : Card edge type

8 bit: data width = 8bit type,

16 bit: data width = 16bit type

W/ : with ,

W/O : without

B M : battery monitor option,

W P : write protect option





MITSUBISHI MEMORY CARD (IV)



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Products			Type name	Access (ns)	Other	Sample	Production	Note
2 P 60 pin	16 bit	64KB	MF465A-F1EAPXX	250	256K x 2pcs	-	Yes	CE/OE W/O buffer
		128KB	MF4129-F1EAPXX	250	256K x 4pcs	-	Yes	
		128KB	MF4129-F3EAPXX	250	1M x 1pc	-	Yes	
		256KB	MF4257-F1EAPXX	250	256K x 8pcs	-	Yes	
		256KB	MF4257-F3EAPXX	250	1M x 2pcs	-	Yes	
		512KB	MF4513-F1EAPXX	250	256K x 16pcs	-	Yes	
		512KB	MF4513-F3EAPXX	250	1M x 4pcs	-	Yes	
		1MB	MF41M1-F1EAPXX	250	1M x 8pcs	-	Yes	
		2MB	MF42M1-F1EAPXX	250	1M x 16pcs	-	Yes	
		4MB	MF44M1-F1DAPXX	200	2M x 16pcs	Yes	'91/1Q	
O T P	8 bit	32KB	MF432A-F3EACXX	250	256K x 1pc	Yes	'91/1Q	
		64KB	MF464A-F2EACXX	250	256K x 2pcs	Yes	'91/1Q	
		128KB	MF4128-F2EACXX	250	256K x 4pcs	Yes	'91/1Q	
		128KB	MF4128-F4EACXX	250	1M x 1pc	Yes	'91/1Q	
		256KB	MF4256-F2EACXX	250	256K x 8pcs	Yes	'91/1Q	
		256KB	MF4256-F4EACXX	250	1M x 2pcs	Yes	'91/1Q	
		512KB	MF4512-F2EACXX	250	256K x 16pcs	Yes	'91/1Q	
		512KB	MF4512-F4EACXX	250	1M x 4pcs	Yes	'91/1Q	
		1MB	MF41M0-F2EACXX	250	1M x 8pcs	Yes	'91/1Q	
		2MB	MF42M0-F2EACXX	250	1M x 16pcs	Yes	'91/1Q	
C/E	16 bit	64KB	MF465A-F2EACXX	250	256K x 2pcs	Yes	'91/1Q	CE/OE W/O buffer
		128KB	MF4129-F2EACXX	250	256K x 4pcs	Yes	'91/1Q	
		128KB	MF4129-F4EACXX	250	1M x 1pc	TBD	TBD	
		256KB	MF4257-F2EACXX	250	256K x 8pcs	Yes	'91/1Q	
		256KB	MF4257-F4EACXX	250	1M x 2pcs	Yes	'91/1Q	
		512KB	MF4513-F2EACXX	250	256K x 16pcs	Yes	'91/1Q	
		512KB	MF4513-F4EACXX	250	1M x 4pcs	Yes	'91/1Q	
		1MB	MF41M1-F2EACXX	250	1M x 8pcs	Yes	'91/1Q	
		2MB	MF42M1-F2EACXX	250	1M x 16pcs	Yes	'91/1Q	

MITSUBISHI MEMORY CARD (V)



	Products		Type name	Access(ns)	Other	Sample	Production	Note	
M A S K	2 P 60 pin	16 bit	512KB	MF7513-F3EAPXX	250	4M × 1pc	—	'91/1Q	
			1MB	MF71M1-F3EAPXX	250	4M × 2pcs	—	Y e s	
			2MB	MF72M1-F3EAPXX	250	4M × 4pcs	—	'91/1Q	
D R A M	2 P 60 pin	8 bit	512KB	MF1512-M1CAPXX	150		—	Y e s	
		16 bit	512KB	MF1513-M1CAPXX	150		—	Y e s	
			1MB	MF11M1-M1CAPXX	150		—	Y e s	
			2MB	MF12M1-M1CAPXX	150		—	Y e s	
			3MB	MF13M1-M1CAPXX	150		—	Y e s	
E E P R O M	2 P 60 pin	8 bit	W/ WP	8KB	MF808A-F1EAPXX	250		Yes	'91/1Q
				16KB	MF816A-F1EAPXX	250		Yes	'91/1Q
				32KB	MF832A-F1EAPXX	250		Yes	'91/1Q
				64KB	MF864A-F1EAPXX	250		Yes	'91/1Q
				128KB	MF8128-F1EAPXX	250		Yes	'91/1Q
				192KB	MF8192-F1EAPXX	250		Yes	'91/1Q

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MITSUBISHI MEMORY CARD (VI)



Products				Type name	Access(ns)	Other	Sample	Production	Note	
S t a t i s t i c M	2 P	8/16	W P · B M 付	64KB	MF365A-L2DAT××	200		Yes	'91/2Q	JEIDA PC9 Ver 4 PCMCIA Ver 1.0
				128KB	MF3129-L2DAT××	200		Yes	'91/2Q	
				256KB	MF3257-L2DAT××	200		Yes	'91/1Q	
				512KB	MF3513-L2DAT××	200		Yes	'91/1Q	
				1MB	MF31M1-L2DAT××	200		Yes	'91/1Q	
				2MB	MF32M1-L2DAT××	200		Yes	'91/1Q	
O T P	2 P	8/16		256KB	MF4257-G1EAT××	250		'91/3	'91/2Q	
				512KB	MF4513-G1EAT××	250		'91/3	'91/2Q	
				1MB	MF41M1-G1EAT××	250		'91/3	'91/2Q	
				2MB	MF42M1-G1EAT××	250		'91/3	'91/2Q	
				4MB	MF44M1-G1EAT××	250		'91/3	'91/2Q	
M A S K R O M	2 P	8/16		512KB	MF7513-G1DAT××	200		TBD	TBD	JEIDA PC9 Ver 4 PCMCIA Ver 1.0
				1MB	MF71M1-G1DAT××	200		TBD	TBD	
				2MB	MF72M1-G1DAT××	200		'91/1Q	'91/2Q	
				4MB	MF74M1-G1DAT××	200		'91/1Q	'91/2Q	
				8MB	MF78M1-G1DAT××	200		'91/1Q	'91/2Q	
				16MB	MF716M-G1DAT××	200		'91/3Q	'91/4Q	
F l a s h	2 P	8/16		256KB	MF8257-G1EAT××	250		TBD	TBD	JEIDA PC9 Ver 4 PCMCIA Ver 1.0
				512KB	MF8513-G1EAT××	250		TBD	TBD	
				1MB	MF81M1-G1EAT××	250		'91/2	'91/2Q	
				2MB	MF82M1-G1EAT××	250		'91/2	'91/2Q	

Note : [Card thickness : 3.3mm unless otherwise noted, Panel material : Metal]

2 P : two-piece connector type

8/16bit: data width = 8bit or 16bit (controllable)

W / : with , W/O : without

B M : battery monitor option, W P : write protect option

# MITSUBISHI MEMORY CARD (VII)

## OTP Programming Adapter

Products	Type name	Applicable OTP IC	Sample	Production	Note
2 P	MFT2A01-001	256Kbit	-	Yes	
	MFT2A02-001	1Mbit	-	Yes	
	MFT2A03-001	1Mbit (data width=16 bit)	-	Yes	
C/E	MFT2A01-002	256Kbit	-	Yes	
	MFT2A02-002	1Mbit	-	Yes	

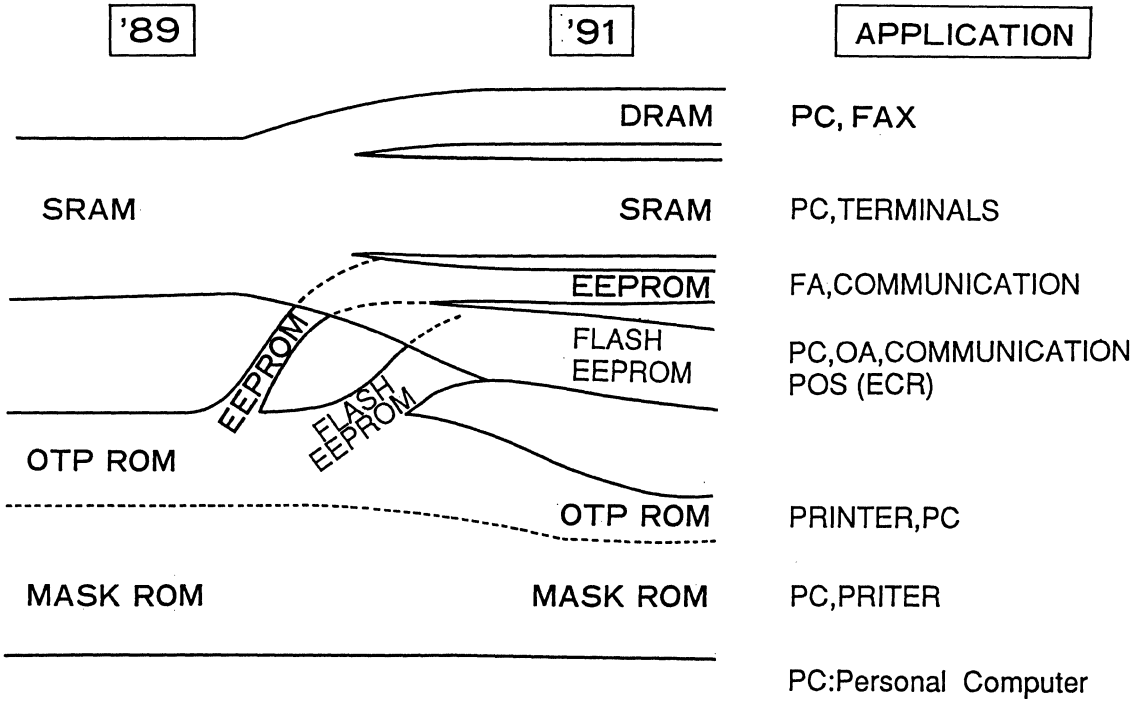
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## Connector

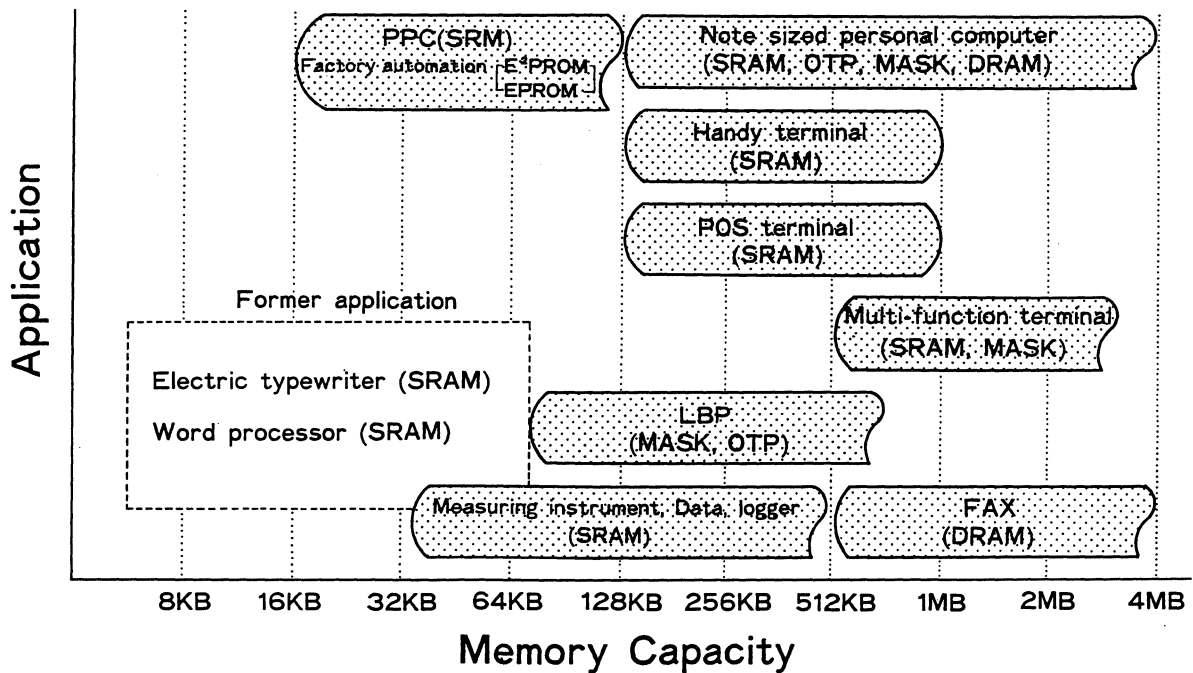
Products		MELCO Type name	Mfr. & Type name	Sample	Production	Note	
2 P	Right Angle	same length	MFC60P1-01-R2	Du pont 69740-001	-	Yes	
		longer GND pin	MFC60P1-05-R2	Du pont 86291-001	-	Yes	
	Straight	same length	MFC60P1-01-S2	Du pont 69739-001	-	Yes	
		longer GND pin	MFC60P1-05-S2	Du pont 86465-001	-	Yes	
	Ejector		—	—	Du pont 86933-001	Yes	-
			—	—	JAE JC20EA-D60PR-LT1-A1	Yes	-
C/E	Right Angle	MFC50C1-01-R1	—	—	-	Yes	
	Push-in Push-out	MFC50E1-C01	Hoshiden Electronics	HGC342-01-200	Yes	-	



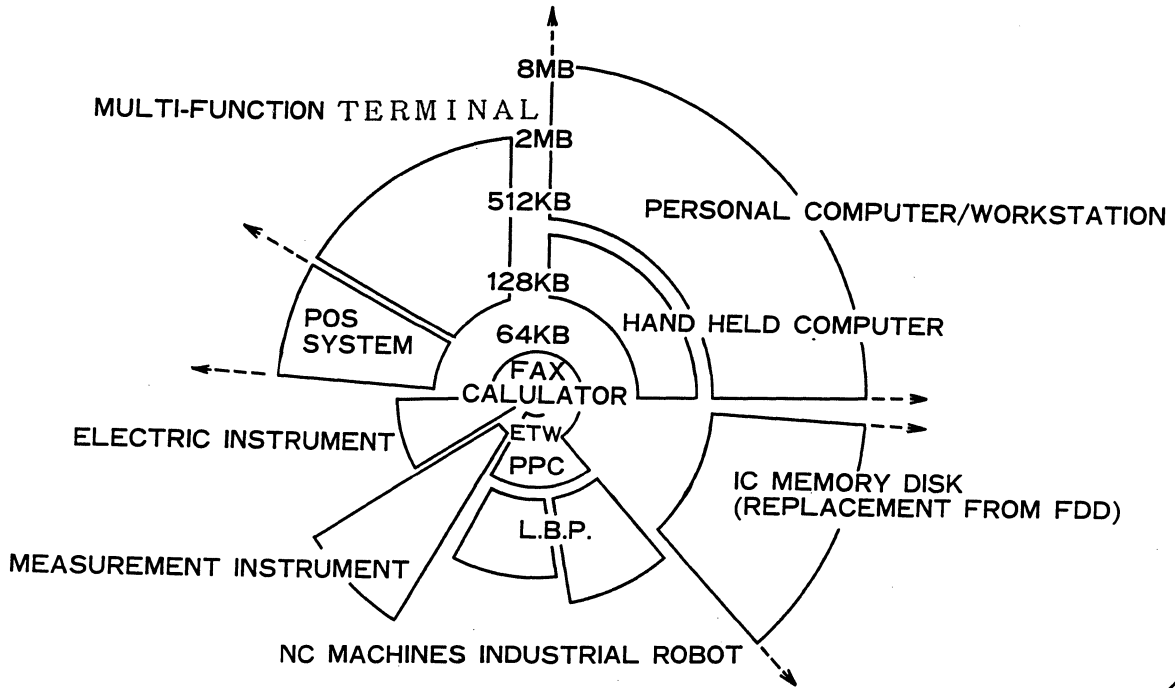
# TREND OF MEMORY ICS FOR MEMORY CARDS



# Application of High Capacity Memory Card



# Application Systems and Memory Capacity of Memory Card



# APPLICATION EXAMPLES FOR PERSONAL COMPUTER

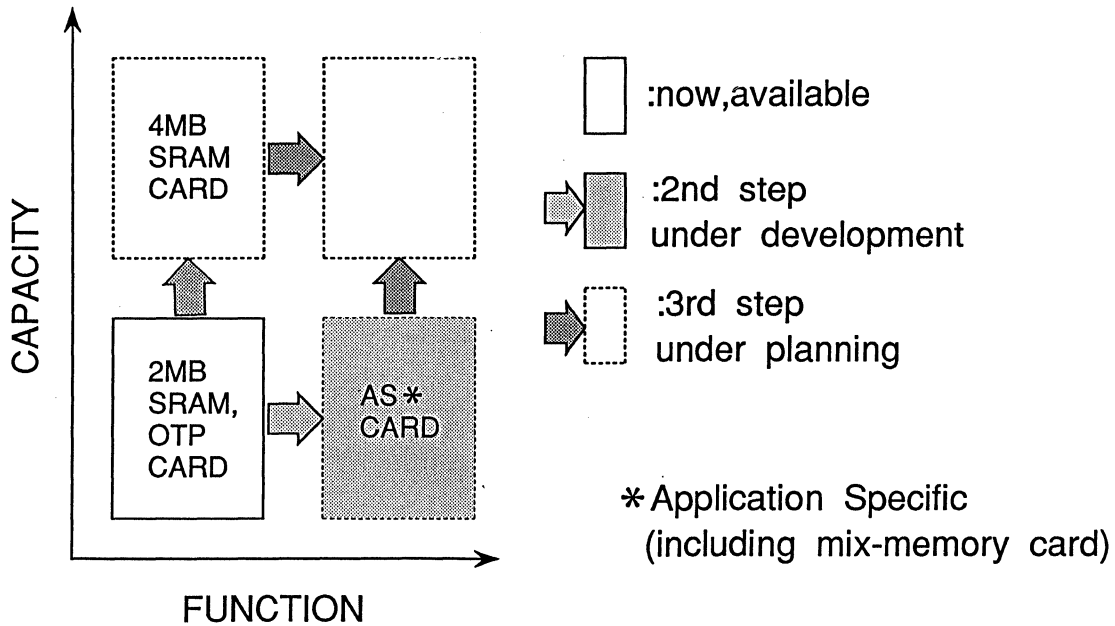
WITHOUT MEMORY CARD	WITH MEMORY CARD	
	CASE I USING FLOPPY DISK	CASE II USING MEMORY CARD
<p>SOFTWARE/DATA</p>	<p>PLUS MEMORY EXPANSION</p> <p>[DRAM CARD]</p>	<p>[SRAM CARD OTPROM CARD MROM CARD]</p> <p>PLUS MEMORY EXPANSION</p> <p>[DRAM CARD] [SRAM CARD]</p>

## MARKET TRENDS and MITSUBISHI DEVELOPMENT PLAN

	'88	'89	'90	'91	'92
Market	POS terminal, Handy terminal	FAX		Image processing equipment	Telecommunication terminal Solidstate memory disk Pam-top. P.C.
SRAM	512KB RAM CARD	1MB/2MB RAM CARD			4MB RAM CARD
FEEPROM	1MB/2MB OTP CARD	1MB/2MB MROM CARD	1MB/2MB FE <sup>2</sup> CARD	4MB/8MB FE <sup>2</sup> CARD	
Development plans		1MB/2MB/3MB DRAM CARD	4MB~12MB DRAM CARD		32MB DRAM CARD
DRAM					
AS		* ASIC CARD (I)	ASIC CARD (II)	ASIC CARD (III)	ASIC CARD (IV)

\* ASIC CARD (I): Mix memory card  
 ASIC CARD (II): Multi-function card having custom ICs.

## DEVELOPMENT STRATEGY for MEMORY CARD



## DEVELOPMENT STRATEGY of NEW(HR) MEMORY CARD

### 1. APPLICATION of MOST ADVANCED IC to CARD

- A) SRAM 256kb → 1Mb
- B) DRAM 1Mb → 4Mb
- C) OTP 2Mb → (4Mb)
- D) MASKROM 4Mb → (8~16Mb)
- E) FEEPROM (1Mb)
- F) HCMOS LOGIC and ASIC for INTERFACE

## 2. IMPROVEMENT of CARD RELIABILITY with TSOP IC

- A) SEVERE BURN-IN TEST to TSOP IC
- B) COMPLETE TESTING to TSOP IC
- C) ZERO FAILURE in PROCESS of CARD ASSEMBLY

## 3 · HIGH RELIABLE PCB ASSEMBLY PROCESS

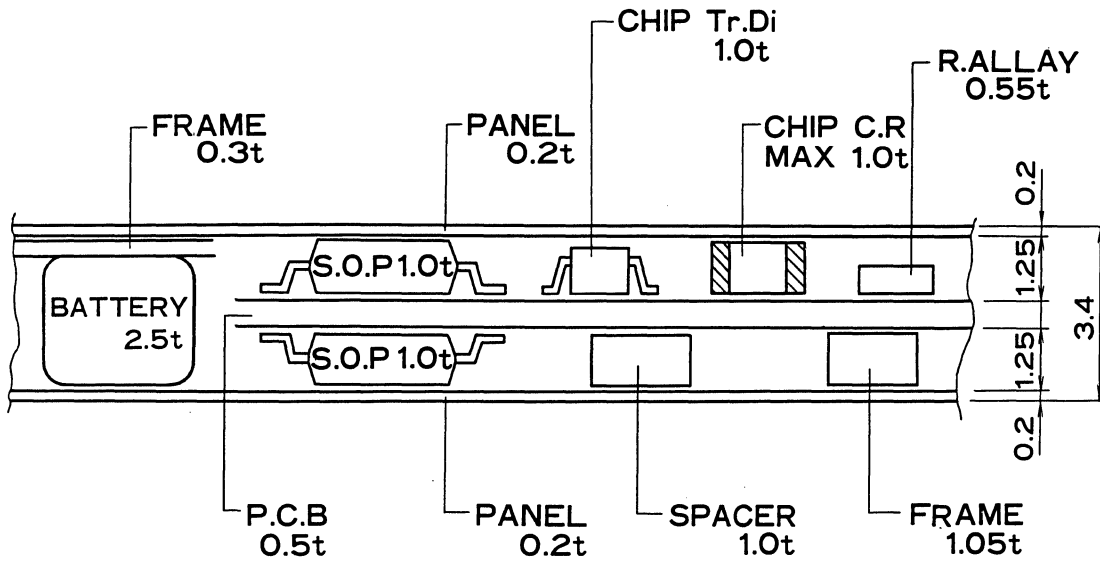
- A) WIRE BONDING
  - NO-OXIDIZATION SOLDERING  
(with non-active gas)
- B) REFLOW SOLDERING
  - VAPOR PHASE SOLDERING  
AIR FLOW SOLDERING  
(in low temperature and uniform heating)

## Memory Cards New Product Plan

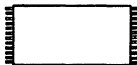

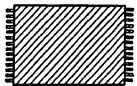
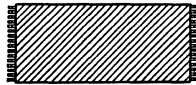

	Sample	Production
• 1MB/2MB SARM Cards	:Yes	91/1Q
• 512KB to 3MB DRAM Cards	:Yes	Yes
• 4MB to 12MB DRAM Cards	:91/1Q	91/ 2Q
• 128KB to 2MB Flash E <sup>2</sup> PROM Cards	:91/1Q	91/ 2Q
• JEIDA Ver.4(PCMCIA) Cards	:Yes	91/ 1Q

## FEATURES of MELCARDS

- Uses TSOP(1.0mm) for most advanced memory and high reliability.
- One to 16(~24) memory ICs can be mounted in a card
- AS ICs can be mounted in a card.
- Apply special screening tests to memory ICs.
- Buffered interface.
- Ability to change memory type(SRAM, OTP, MROM...), capacity(32KB to 8MB), or data bit width(8bit, 16bit) without changing connector type.



MELCO TSOP SERIES PLAN

Pin Count	Pkg Width	Package Length			
		13.4mm	14mm	16mm	20mm
24 Pin	6mm	—	 256K V-RAM	 1M D-RAM	—
28 Pin	8mm	 256K S-RAM	—	—	—
32 Pin	8mm	—	—	—	 1M S-RAM
40 Pin	10mm	—	 1M OTP	—	—

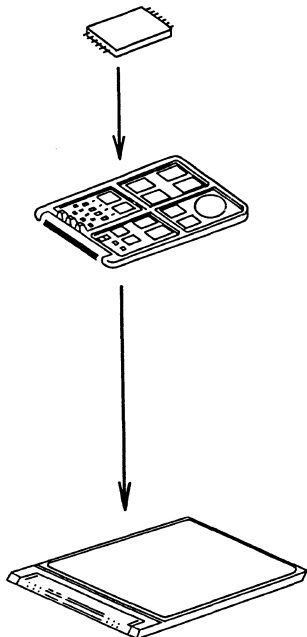
## Reliability Evaluation Flow for New Products

Reliability evaluation of the new component parts

Reliability evaluation of the module fabricated with the new component parts

Electrical characteristic evaluation: temperature dependence and parameter distribution

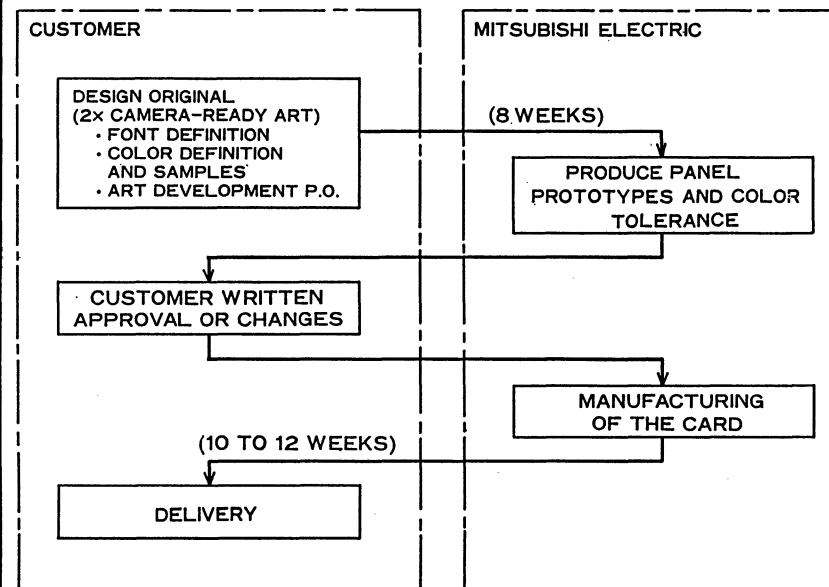
Reliability evaluation of memory cards



16

## CUSTOMER-DEFINED ARTWORK DEVELOPMENT FLOW

The following exhibits the typical development flow for customer-defined artwork development.



Note that artwork is NOT released for volume Memory-Card production unless Mitsubishi Electric Corp. has received the customer's written approval of artwork prototypes. Typical turn-around time from customer

inputs to delivery of artwork prototypes is 8 weeks. Non-standard artwork turn-around times will vary. Pricing for customer-defined artwork development is quoted upon customer request.



## Reliability Test Results of TSOP

Test Items	Test Conditions	Sample	Sample Size	Failures
Solderability	230°C, 5sec Measuring items : visual	M5M5256VP	22	0
		M5M27256VP	22	0
		M74HC138VP	22	0
		4066VP,245VP		
		M51959VP	22	0
Temperature Cycling	-65°C ~150°C 100 $\phi$	M5M5256VP	160	0
		M5M27256VP	50	0
		M74HC138VP	50	0
		4066VP,245VP		
		M51959VP	50	0
High Temperature Storage	150°C, 1000h	M5M5256VP	160	0
		M5M27256VP	196	0
		M74HC138VP	110	0
		4066VP,245VP		
		M51959VP	88	0
Humidity Bias	85°C/85% RH 5.0V, 1000h	M5M5256VP	176	0
		M5M27256VP	110	0
		M74HC138VP	110	0
		4066VP,245VP		
		M51959VP	88	0
Pressure Cooker Test	121°C, 2atm 240h	M5M5256VP	242	0
		M74HC138VP 4066VP,245VP	110	0
Operation Life Test	125°C, 6.0V 1000h	M5M5256VP	352	0
	150°C, 8.5V 1000h	M74HC138VP 4066VP,245VP	110	0

Note 1. Pre-conditionings for PCT and moisture resistance:  
Bake(125°C, 24h)→VPS(215°C, 10sec)

Note 2. Measuring items: electrical characteristics

## Memory Cards Reliability Test Results of Module (HR Series)

Test Items	Test Conditions	Sample Size	Failures
High Temperature Bias	125°C, 7V, 1000h	56	0
High Temperature Storage	125°C, 1000h	56	0
Temperature Cycling	-40°C ~125°C, 100 $\phi$	98	0
Moisture Resistance	85°C/85% RH, 1000h	56	0
Low Temperature Storage	-40°C, 1000h	27	0

Note 1. Measuring item: electrical characteristics

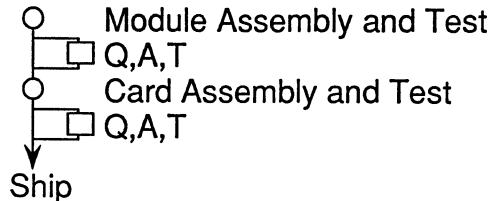
## Memory Cards

### Reliability Test Results of Memory Card (HR Series)

Test Items	Test Conditions	Sample Size	Failures
High Temperature Bias	85°C, 5V, 1000h	67	0
Low Temperature Storage	-40°C, 1000h	27	0
Moisture Resistance	85°C / 85% RH, 1000h	56	0
Temperature Cycling	-40°C ~ 85°C, 10 $\infty$	67	0
Vibration	1.5mm(P·P), 10~55Hz, 2h/X,Y,Z	16	0
Bending	5kg stress, 100times	37	0
Torsion	5kg stress, 100times	37	0
Fall	0.75m, plastic tile, 3times	27	0

Note 1. Measuring items: electrical characteristics.

## 2-Stage Quality Assurance Test



Q,A,T		Module	Card
Grupe A	Electrical	○	○
	Visual Mechanical	○	○
Grupe B	Temperature Cycling	○	
Grupe C	Temperature Cycling	○	○
	Storage	○	○
	Operating Life	○	○
	Moisture Resistance	○	○
	Vibration		○
	Bending		○
	Torsion		○
	Fall,etc.		○



# PIN ASSIGNMENT OF CARD

## 50-pin of Card-Edge Type

Pin No.	Symbol	Input or Output	SRAM 8bit 8MB	SRAM 16bit 8MB	OTP 8bit 8MB	OTP 16bit 8MB	MASK 8bit 8MB	MASK 16bit 8MB
1	GND	Input	GND	GND	GND	GND	GND	GND
2	C D	Output	C D	C D	C D	C D	C D	C D
3	Vpp1/BM	I/O	B M	B M	Vpp1	Vpp1	N. C	N. C
4	A22/Vpp2	Input	A22	N. C	A22	Vpp2	A22	N. C
5	A21	"	A21	A21	A21	A21	A21	A21
6	A20	"	A20	A20	A20	A20	A20	A20
7	A19	"	A19	A19	A19	A19	A19	A19
8	A18	"	A18	A18	A18	A18	A18	A18
9	A17	"	A17	A17	A17	A17	A17	A17
10	A16	"	A16	A16	A16	A16	A16	A16
11	A15	"	A15	A15	A15	A15	A15	A15
12	A12	"	A12	A12	A12	A12	A12	A12
13	A 7	"	A 7	A 7	A 7	A 7	A 7	A 7
14	A 6	"	A 6	A 6	A 6	A 6	A 6	A 6
15	A 5	"	A 5	A 5	A 5	A 5	A 5	A 5
16	A 4	"	A 4	A 4	A 4	A 4	A 4	A 4
17	A 3	"	A 3	A 3	A 3	A 3	A 3	A 3
18	A 2	"	A 2	A 2	A 2	A 2	A 2	A 2
19	A 1	"	A 1	A 1	A 1	A 1	A 1	A 1
20	A 0	"	A 0	A 0	A 0	A 0	A 0	A 0
21	D 0	I/O	D 0	D 0	D 0	D 0	D 0	D 0
22	D 1	"	D 1	D 1	D 1	D 1	D 1	D 1
23	D 2	"	D 2	D 2	D 2	D 2	D 2	D 2
24	D 3	"	D 3	D 3	D 3	D 3	D 3	D 3
25	D 4	"	D 4	D 4	D 4	D 4	D 4	D 4
26	D 5	"	D 5	D 5	D 5	D 5	D 5	D 5
27	D 6	"	D 6	D 6	D 6	D 6	D 6	D 6
28	D 7	"	D 7	D 7	D 7	D 7	D 7	D 7
29	D 8	"	N. C	D 8	N. C	D 8	N. C	D 8
30	D 9	"	N. C	D 9	N. C	D 9	N. C	D 9
31	D10	"	N. C	D10	N. C	D10	N. C	D10
32	D11	"	N. C	D11	N. C	D11	N. C	D11
33	D12	"	N. C	D12	N. C	D12	N. C	D12
34	D13	"	N. C	D13	N. C	D13	N. C	D13
35	D14	"	N. C	D14	N. C	D14	N. C	D14
36	D15	"	N. C	D15	N. C	D15	N. C	D15
37	C E	Input	C E	C E	C E	C E	C E	C E
38	A10	"	A10	A10	A10	A10	A10	A10
39	O E	"	O E	O E	O E	O E	O E	O E
40	A11	"	A11	A11	A11	A11	A11	A11
41	A 9	"	A 9	A 9	A 9	A 9	A 9	A 9
42	A 8	"	A 8	A 8	A 8	A 8	A 8	A 8
43	A13	"	A13	A13	A13	A13	A13	A13
44	A14	"	A14	A14	A14	A14	A14	A14
45	LOWE/WE/PGM1	"	W E	LOWE	PGM1	PGM1	N. C	N. C
46	HIWE/PGM2	"	N. C	HIWE	N. C	PGM2	N. C	N. C
47	WP/N. C	Output	W P	W P	N. C	N. C	N. C	N. C
48	C 1	—	N. C	N. C	N. C	N. C	N. C	N. C
49	Vcc	Input	Vcc	Vcc	Vcc	Vcc	Vcc	Vcc
50	GND	"	GND	GND	GND	GND	GND	GND

# List of Symbols



Symbol	Name	Function
NC	No Connection	No signal should be applied to NC.
BM/NC	Battery Monitor / No Connection	Monitor pin of built-in battery voltage. / No signal should be applied to NC.
C D, CD 1, CD 2	Card Detector	Detector for card insertion or removal. CD is connected to GND for CE type, CD1 and CD2 are shorted together and not being connected to GND for 2P (60-pin) type.
A 0~A 2 2	Address Bus	Address bus line. Max.No is depend on memory capacity and unnecessary pins are NC.
D 0~D 7	Data Bus	Data bus line. Lower 8bits Data for 16bits bus type .
D 8~D 1 5	Upper 8bits Data Bus	Data bus line for 16bits bus type use only. Upper 8bits Data for 16bits bus type .
$\overline{C E}$	Card Enable	When $\overline{C E}$ is "L", the card is active for read/write.
$\overline{W E}$	Write Enable	For 8bits bus card use only. When $\overline{W E}$ is "L", the card allows to write data.
$\overline{O E}$	Output Enable	When $\overline{O E}$ is "L", the card allows to read data.
$\overline{S 1}$ , $\overline{L O W E}$	Write Enable of Lower 8bits Data	For 16bits bus card use only. When "L", the card allows to write lower 8bits data.
$\overline{S 2}$ , $\overline{H I W E}$	Write Enable of Upper 8bits Data	For 16bits bus card use only. When "L", the card allows to write upper 8bits data.
V p p 1, V p p 2	Power supply for Programming use of OTP card	Apply a rated voltage in programming mode. ( programming, verify, and program-inhibit ) Connected to Vcc in condition of read, output disable and standby modes. Vpp1 : Lower 8bits use for 16bits bus type. Vpp2 : Upper 8bits use for 16bits bus type.
$\overline{P G M 1}$ , $\overline{P G M 2}$	Program	OTP card use only. When PGM is specified in pin assignment. PGM1or2 : "L" for program, "H" for verify.
WP/NC	Write Protect Monitor / No Connection	Monitor pin of write protect switch condition. "H" level (Vcc level) at write protect condition, "L" level (GND level) at normal condition. / No signal should be applied to NC.
C 1, C 2		C1 and C2 are reserved for future use, normally NC.
B 0, B 1, B 2		2P type (60pin) use only. These pins are used to distinguish a kind of card.
V c c G N D	Power Supply	Power supply for card.

## Pin Configuration of JEIDA/PCMCIA Card

Pin No.	Symbol	I/O	Function	Pin No.	Symbol	I/O	Function
1	GND		0V	35	GND		0V
2	D3	I/O	Data I/O	36	CD1	I/O	Card Detect 1
3	D4	I/O	"	37	D11	I/O	Data I/O
4	D5	I/O	"	38	D12	I/O	"
5	D6	I/O	"	39	D13	I/O	"
6	D7	I/O	"	40	D14	I/O	"
7	CE1	I	Card Enable 1	41	D15	I/O	"
8	A10	I	Address input	42	CE2	I	Card Enable 2
9	OE	I	Output Enable	43	RFSH	I	Refresh for PSRAM
10	A11	I	Address input	44	RFU		Reserved for Future Use
11	A9	I	"	45	RFU		"
12	A8	I	"	46	A17	I	Address input
13	A13	I	"	47	A18	I	"
14	A14	I	"	48	A19	I	"
15	WE (PGM)	I	Write Enable (Program input)	49	A20	I	"
16	RDY/BSY	O	Ready/Busy for EEPROM	50	A21	I	"
17	VCC		Power Supply	51	VCC		Power Supply
18	VPP1		Power Supply for Program (Even Byte)	52	VPP2		Power Supply for Program (Odd Byte)
19	A16	I	Address input	53	A22	I	Address input
20	A15	I	"	54	A23	I	"
21	A12	I	"	55	A24	I	"
22	A7	I	"	56	A25	I	"
23	A6	I	"	57	RFU		Reserved for Future Use
24	A5	I	"	58	RFU		"
25	A4	I	"	59	RFU		"
26	A3	I	"	60	RFU		"
27	A2	I	"	61	REG	I	Attribute Memory select
28	A1	I	"	62	BVD2	O	Battery Voltage Detect 2
29	A0	I	"	63	BVD1	O	Battery Voltage Detect 1
30	D0	I/O	Data I/O	64	D8	I/O	Data I/O
31	D1	I/O	"	65	D9	I/O	"
32	D2	I/O	"	66	D10	I/O	"
33	WP	O	Write Protect	67	CD2	O	Card Detect 2
34	GND		0V	68	GND		0V

Note 1 : Pins 36 and 67 are grounded.

2 : No signal should be applied to any "RFU" pin.

SRAM CARD

[32KB / 64KB / 128KB / 256KB / 512KB / 1MB / 2MB]

Mitsubishi SRAM card is consisted of 256kb or 1Mb SRAM ICs with VSOP (TSOP), many kinds of buffer ICs, decoder ICs and voltage detectors.

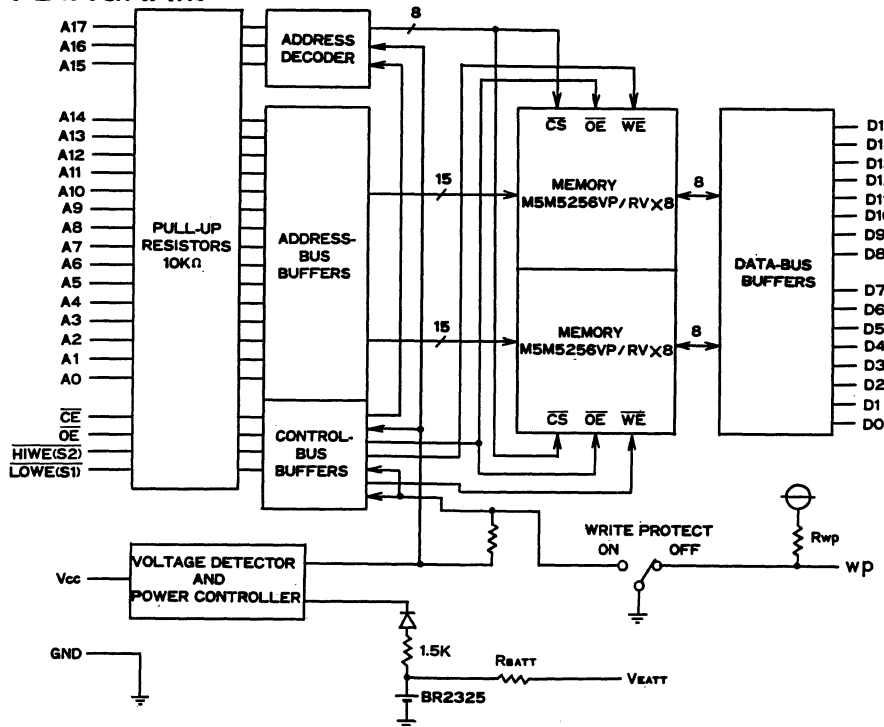
- Write protect switch : with or without
- Battery monitor terminal : with or without
- Access time : 200ns (150ns type is also available by screening)
- Card dimension : 54.0×85.6×3.4t (mm)
- Buffer on address bus, data bus and control lines

Application

Book type personal computer, Handy-terminal, Multifunction terminal, POS-terminal etc.

MF3513-M6DAPXX  
[512KB SRAM CARD]

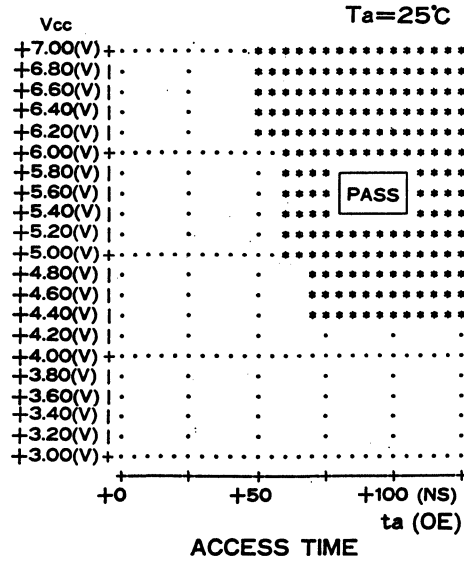
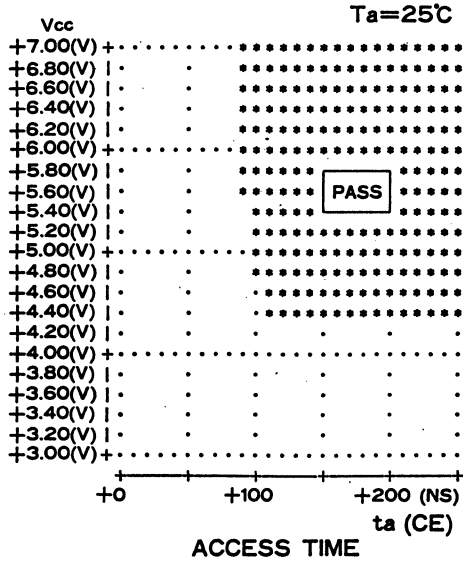
BLOCK DIAGRAM



# MF3513-M6DAPXX

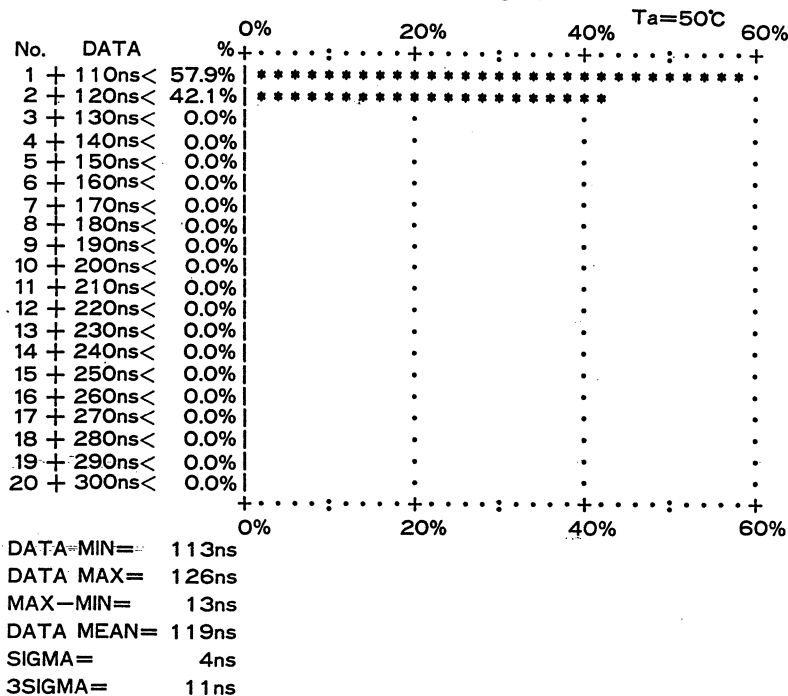
Card enable access time

Output enable access time



# MF3513-M6DAPXX

## Distribution of ta (CE) 512K BYTES RAM CARD

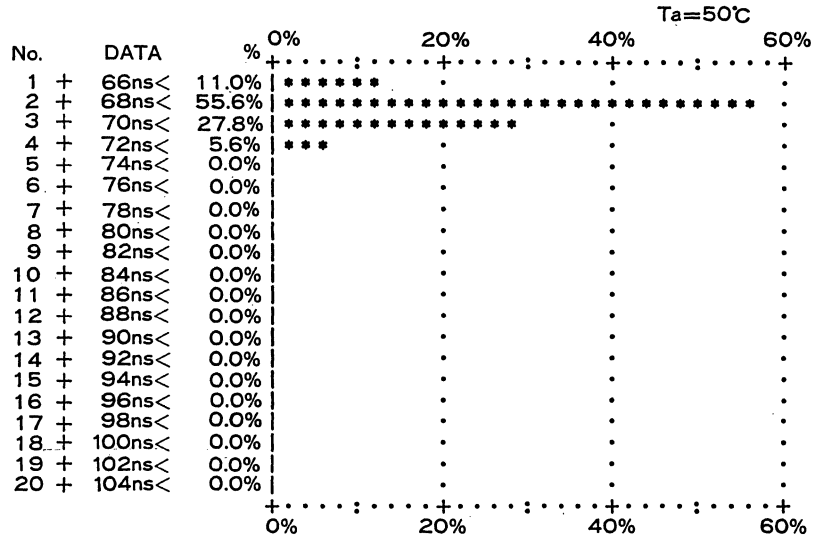




# MF3513-M6DAPXX

MELCARD

## Distribution of $t_a$ (OE) 512K BYTES RAM CARD

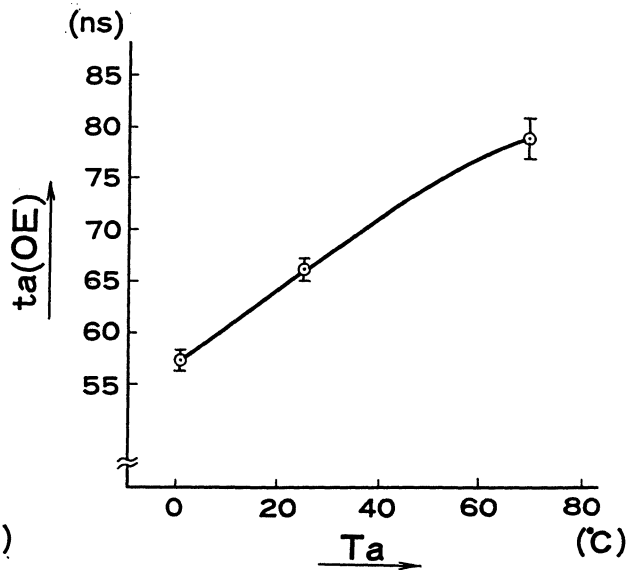
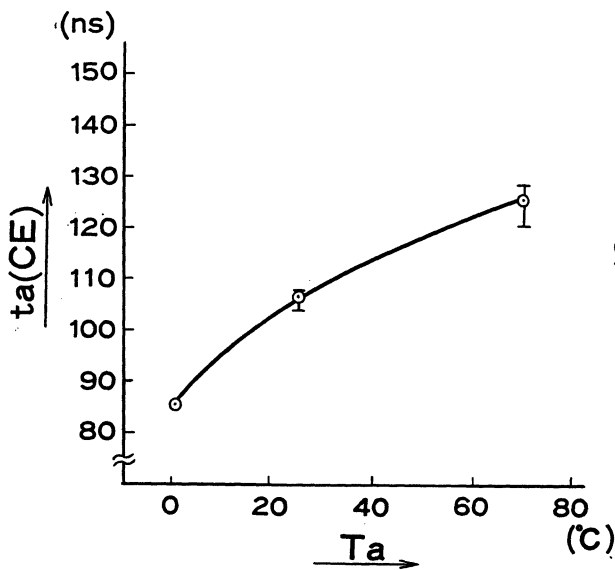


DATA MIN= 66ns  
 DATA MAX= 72ns  
 MAX-MIN= 6ns  
 DATA MEAN=69ns  
 SIGMA= 1ns  
 3SIGMA= 4ns

# MF3513-M6DAPXX

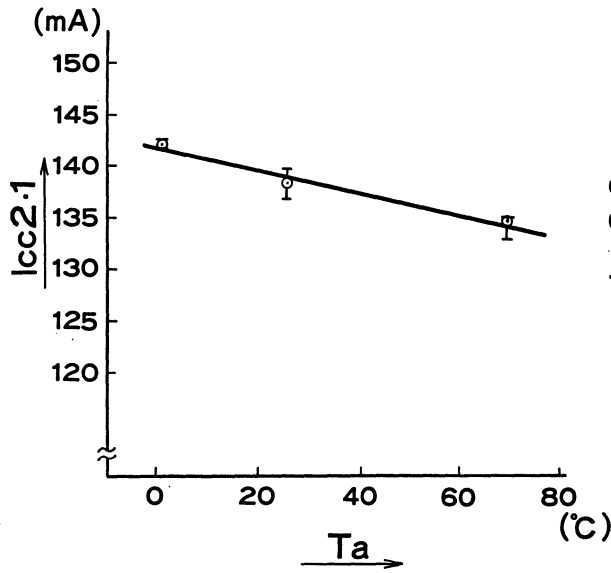
MELCARD

## Access Time vs Ambient Temperature

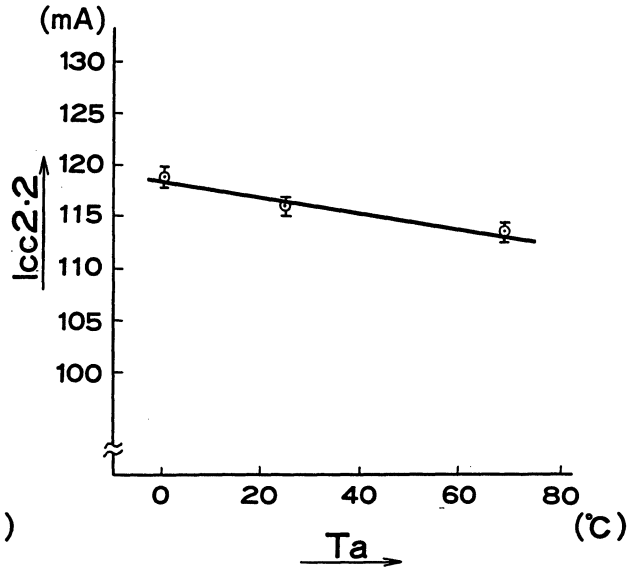


# MF3513-M6DAPXX

## Active Supply Current(Icc2) vs Ambient Temperature



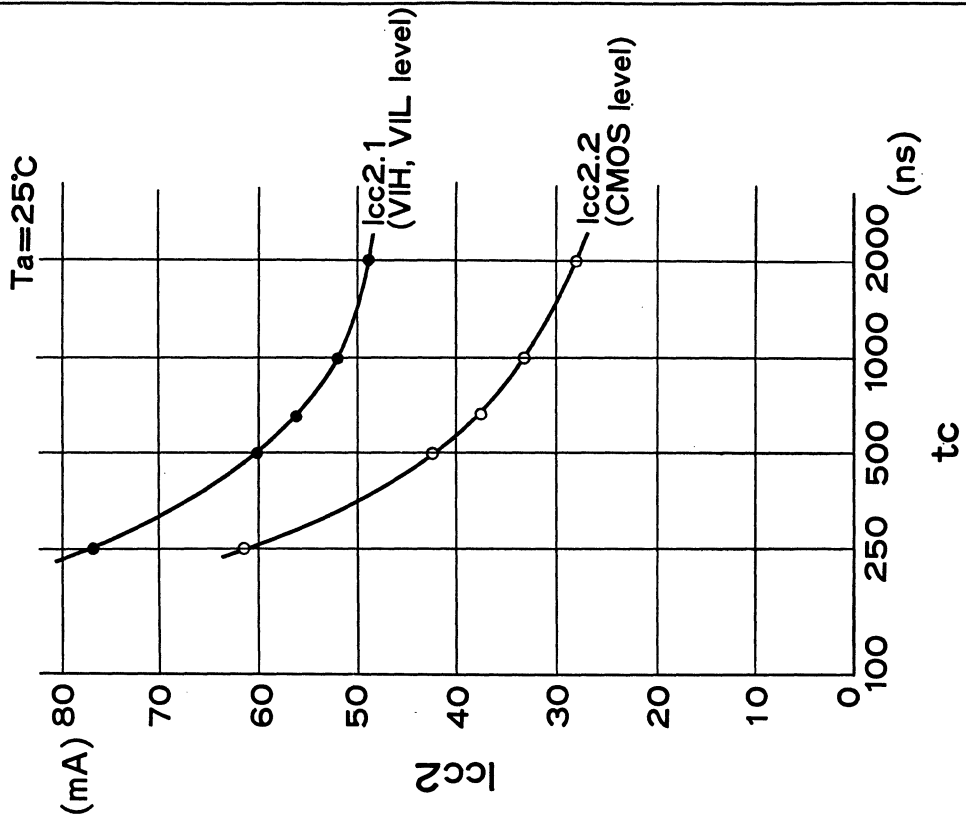
(VIH, VIL level)



(CMOS Level)

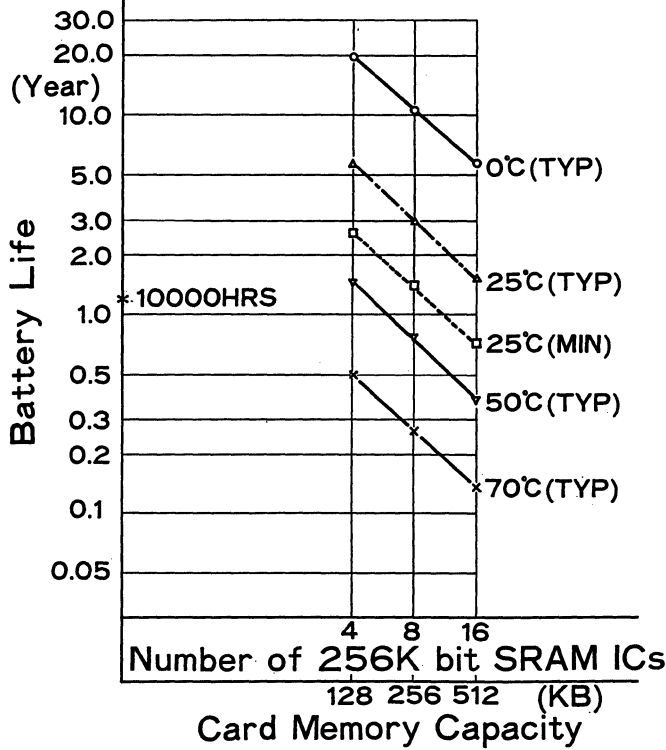
### Cycle time(tc)

### -Active supply current(Icc2) MF3512-M6DAPXX



SRAM Card Battery Life vs Memory Capacity

(calculation)



BATTERY TYPE BR2325

CARD TYPE

128K : MF3128-M6DAPXX

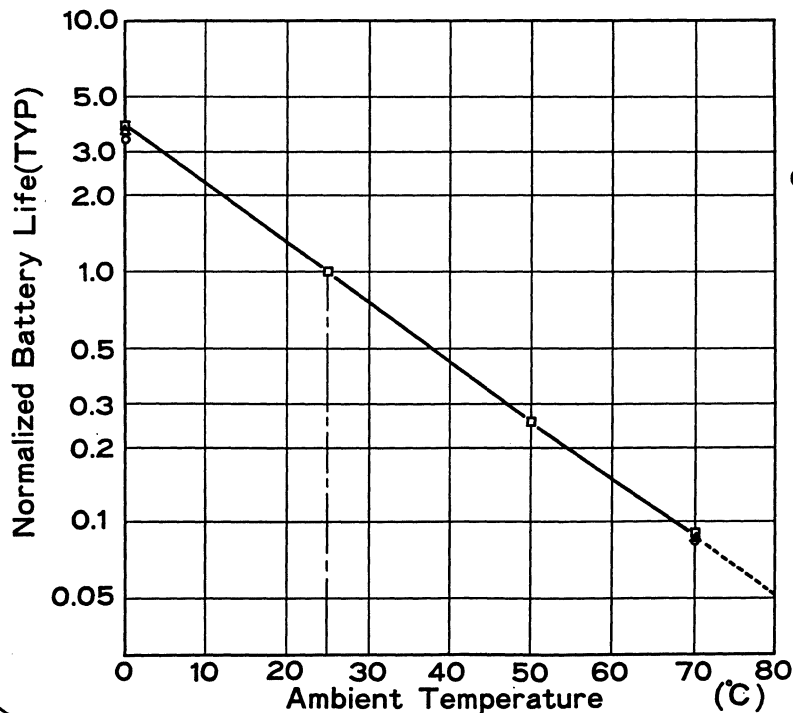
256K : MF3256-M6DAPXX

512K : MF3512-M6DAPXX

STANDBY CURRENT of a RAM

0.8uA(typ) Ta=25°C

Battery Life vs Ambient Temperature (calculation)



BATTERY TYPE : BR2325

CARD TYPE

128K : MF3128-M6DAPXX ○

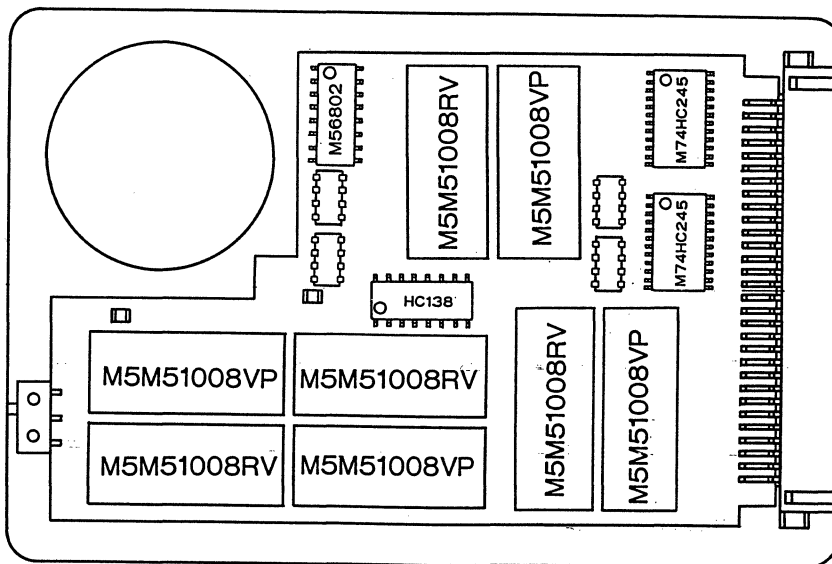
256K : MF3256-M6DAPXX △

512K : MF3512-M6DAPXX □

## Features of Low Standby SRAM card

Item	Low Standby SRAM card	Standard SRAM card
Standby current	0.1mA typ.	13mA typ.
Access time	200ns	200ns
Battery monitor	Yes	Yes
Write Protect	Yes	Yes
Write Protect monitor pin	CMOS output	51K $\Omega$ pull-up resistor or GND
Resistors on address bus	A15~A18:100K $\Omega$ pull-down resistors Other address pin: No resistor	10K $\Omega$ pull-up resistors

## 2MB SRAM CARD



Unit : mm

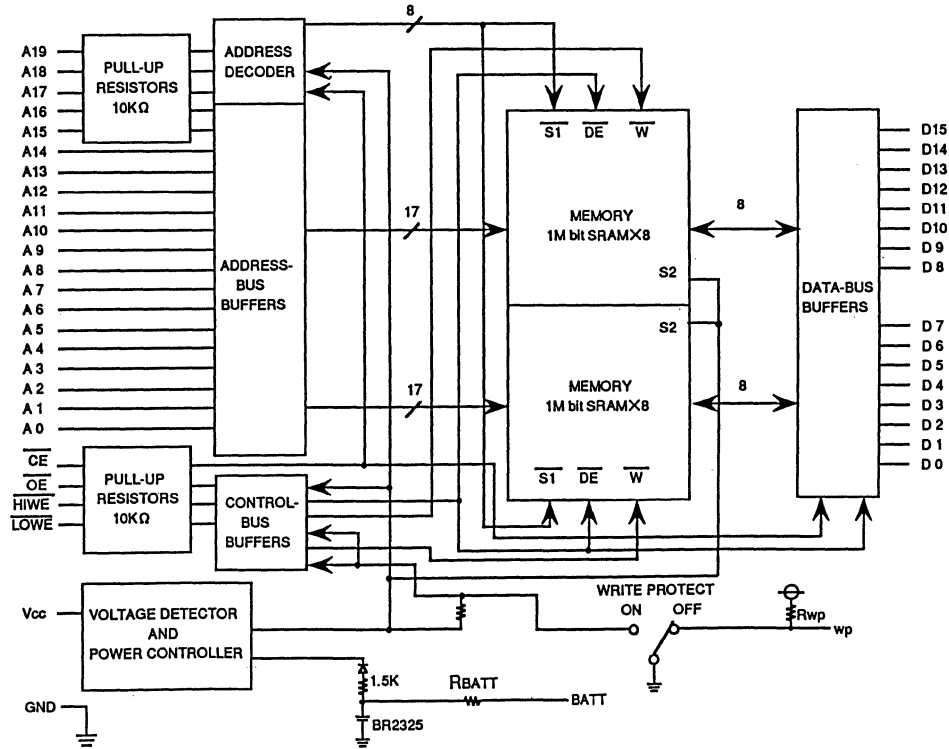
MF32M1-M6DAPXX

MELCARD

Rev

BLOCK DIAGRAM

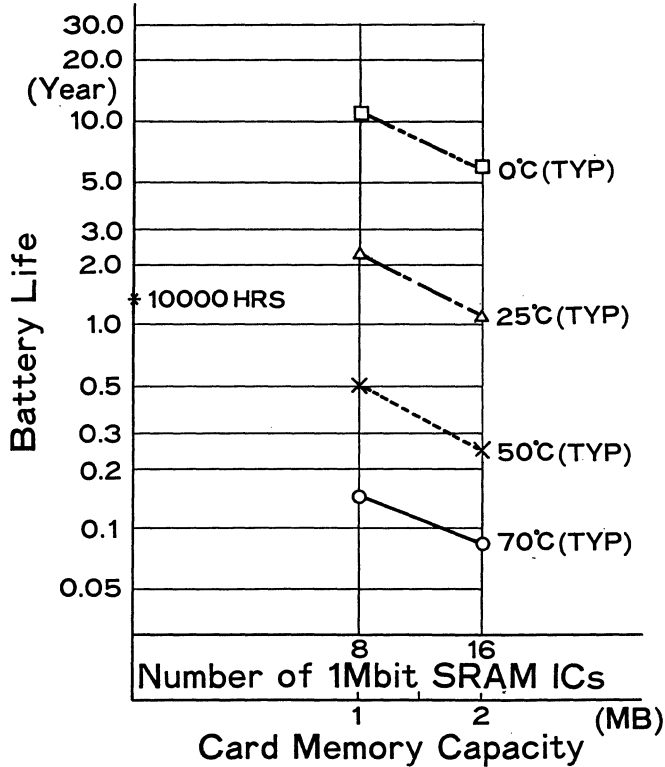
[2MB SRAM CARD]



SRAM Card Battery Life vs Memory Capacity

MELCARD

(Preliminary)



BATTERY TYPE CR2325

CARD TYPE

1MB : MF31M0-M6DAPXX

2MB : MF32M0-M6DAPXX

STANDBY CURRENT of a RAM

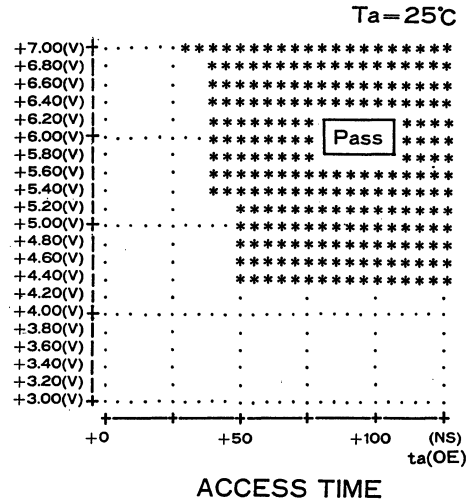
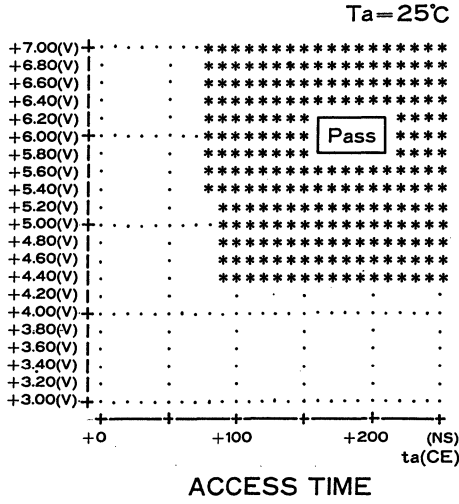
1.0uA(typ) Ta=25°C

Vcc=3V

# 2MB SRAM CARD (MF32M1-M6DAPXX)

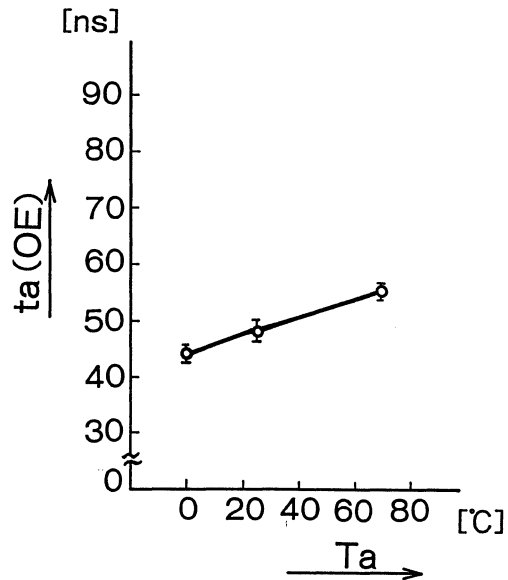
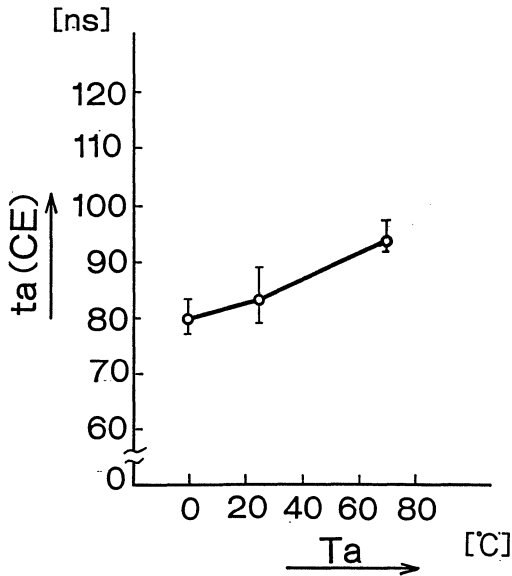
Card Enable access time

Output Enable access time



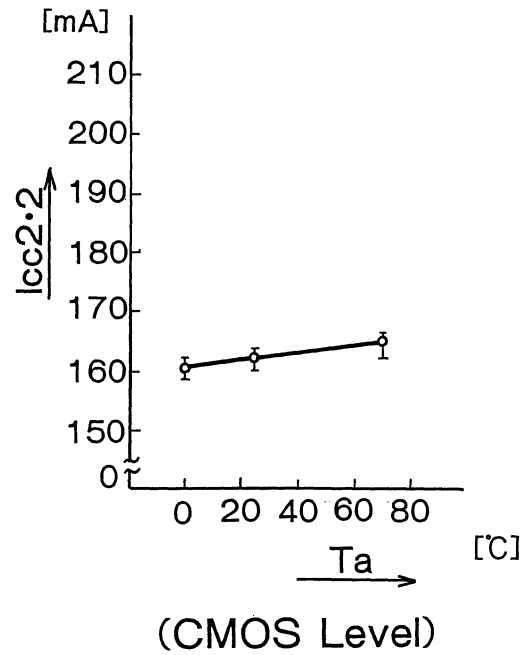
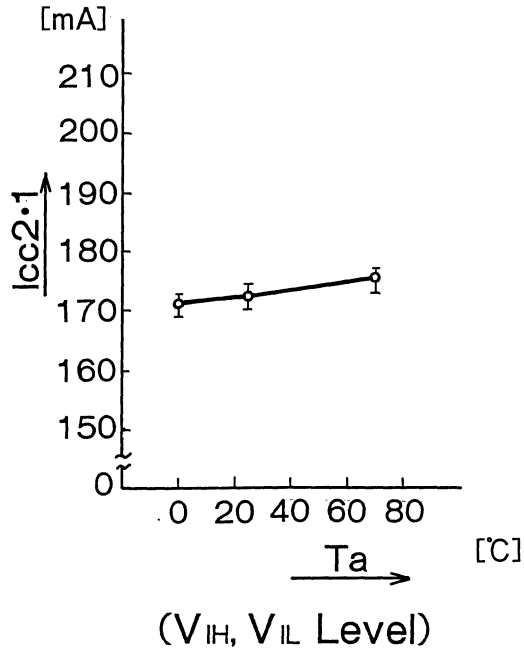
## MF32M1-M6DAPXX

Access Time vs Ambient Temperature

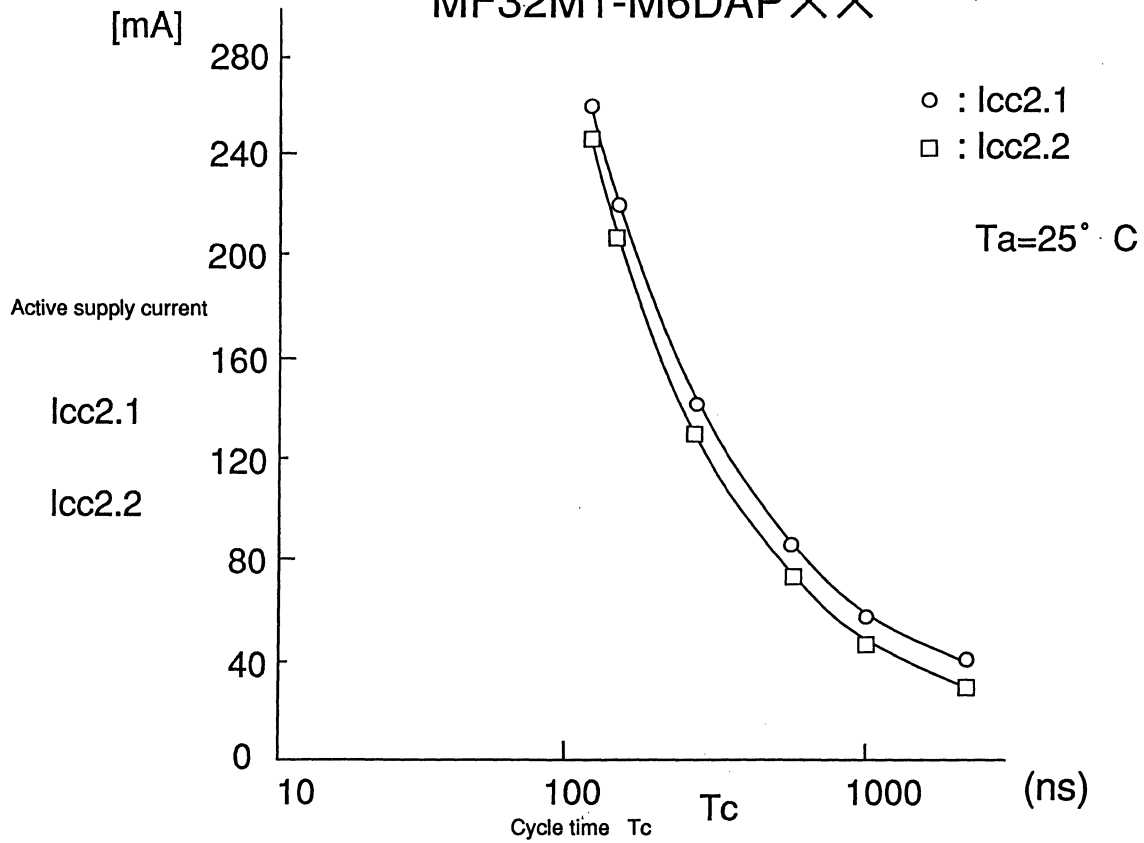


MF32M1-M6DAPXX

Active Supply Current (I<sub>CC2</sub>) vs Ambient Temperature



MF32M1-M6DAPXX





## JEIDA SRAM CARD [128KB/256KB/512KB/1MB/2MB]

### DESCRIPTION

Mitsubisi JEIDA SRAM cards are developed based on JEIDA IC Memory card guideline Ver.4 which is the same specification issued by PCMCIA in U.S.A.

### FEATURES

- Access time 200ns max.
- Buffered interface
- Thickness  $3.3 \pm 0.1$ mm
- Interface level TTL level
- Battery life 2 years typ.(2MB)
- 2 level battery voltage detection

### APPLICATION

Book type personal computer ,Handy-terminal



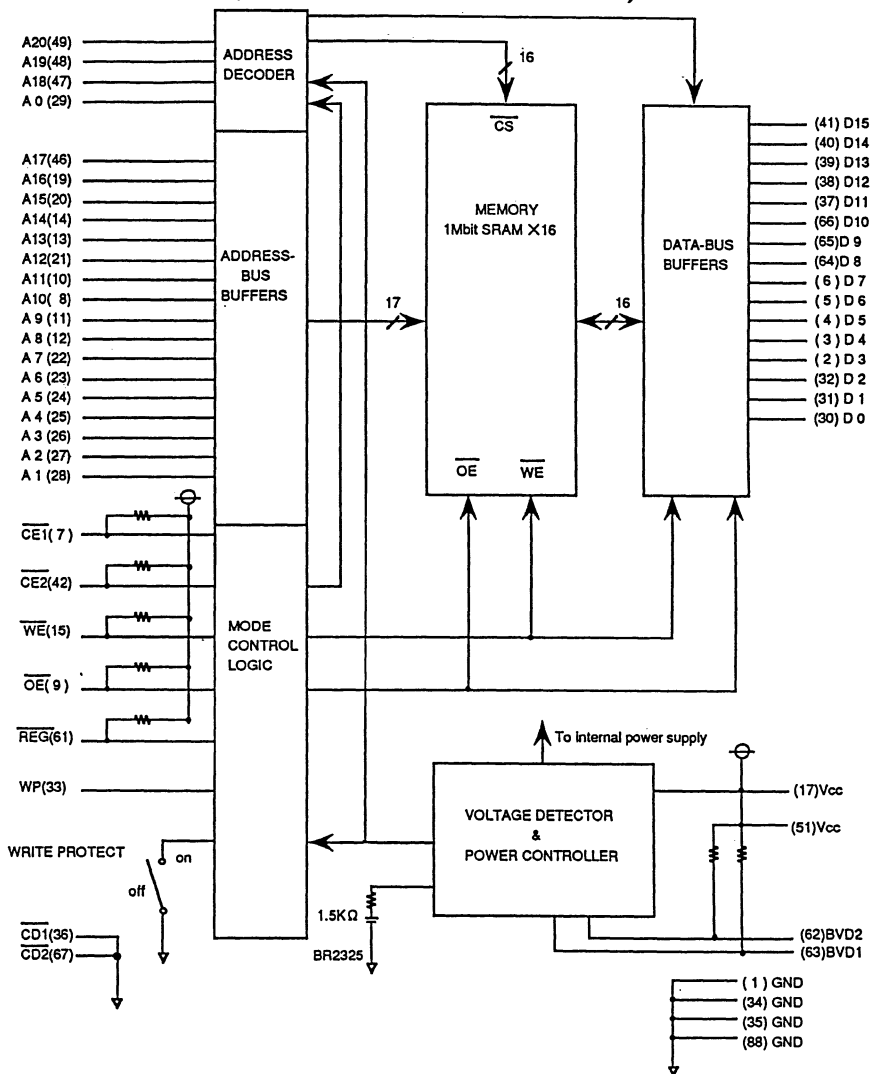
## Comparison between MELCARD and JEIDA Guideline

Item \ Type		MITSUBISHI		JEIDA Guideline Ver.4
		2P-60 Type	JEIDA Type	
Dimensions (mm)	Length	$85.6 \pm 0.2$	$85.6 \pm 0.2$	$85.6 \pm 0.2$
	Width	$54.0 \pm 0.1$	$54.0 \pm 0.1$	$54.0 \pm 0.1$
	Thickness	$3.4 \pm 0.1$	$3.3 \pm 0.1$	3.3~5.0
Pin Counts		60	68	68
Data-bus Width		8 or 16	8/16	8/16
Maximum Capacity		8MB(16MB)	64MB	64MB
Battery Voltage Detection		Analog	Digital (2 levels)	Digital (1or2 levels)
Card Information		Yes: [Memory Type]	No:[FFh]	No:[FFh]
			Yes:[Under planning]	Yes:[Defined]



MF32M1-L2DATXX  
(2MB SRAM CARD)

REV



MITSUBISHI ELECTRIC

MF32M1-L2DATXX

MELCARD  
MITSUBISHI IC CARD

Vcc(V)	T <sub>a</sub> = 25 °C		Vcc(V)	T <sub>a</sub> = 25 °C	
	ACCESS TIME	t <sub>a</sub> (CE)		ACCESS TIME	t <sub>a</sub> (OE)
6.2.0	1.0	1.0	6.2.0	1.0	1.0
6.0.0	1.0	1.0	6.0.0	1.0	1.0
5.8.0	1.0	1.0	5.8.0	1.0	1.0
5.6.0	1.0	1.0	5.6.0	1.0	1.0
5.4.0	1.0	1.0	5.4.0	1.0	1.0
5.2.0	1.0	1.0	5.2.0	1.0	1.0
5.0.0	1.0	1.0	5.0.0	1.0	1.0
4.8.0	1.0	1.0	4.8.0	1.0	1.0
4.6.0	1.0	1.0	4.6.0	1.0	1.0
4.4.0	1.0	1.0	4.4.0	1.0	1.0
4.2.0	1.0	1.0	4.2.0	1.0	1.0
4.0.0	1.0	1.0	4.0.0	1.0	1.0
3.8.0	1.0	1.0	3.8.0	1.0	1.0
3.6.0	1.0	1.0	3.6.0	1.0	1.0
3.4.0	1.0	1.0	3.4.0	1.0	1.0
3.2.0	1.0	1.0	3.2.0	1.0	1.0
3.0.0	1.0	1.0	3.0.0	1.0	1.0

Note: 16bit access

# OTP ROM CARD

[32KB / 64KB / 128KB / 256KB / 512KB / 1MB / 2MB / 4MB]

## DESCRIPTION

Mitsubishi OTP ROM card is consisted of 256Kbit, 1Mbit or 2Mbit OTP ICs with VSOP (TSOP), address bus buffer ICs, decoder ICs and control bus buffer IC.

## Features

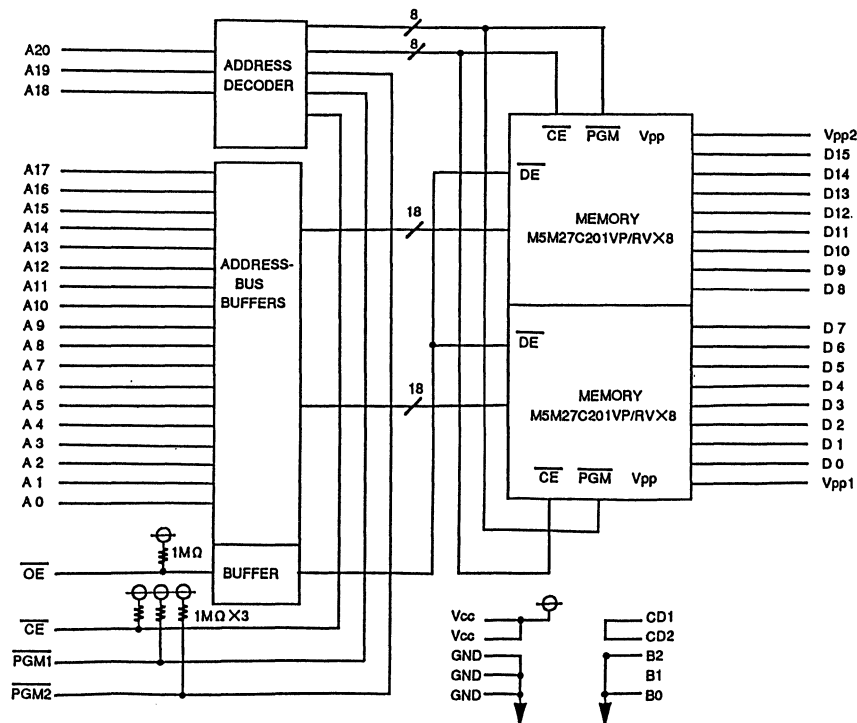
- Data bit length:8bit type or 16bit type
- access time:250ns (200ns type is also available by screening)
- Card dimension:54.0×85.6 ×3.4t (mm)
- Buffer on address bus and control line

## Application

Book type personal computer,Printer, Multifunction terminal,PBX,etc.

# MF44M1-F1DAP××

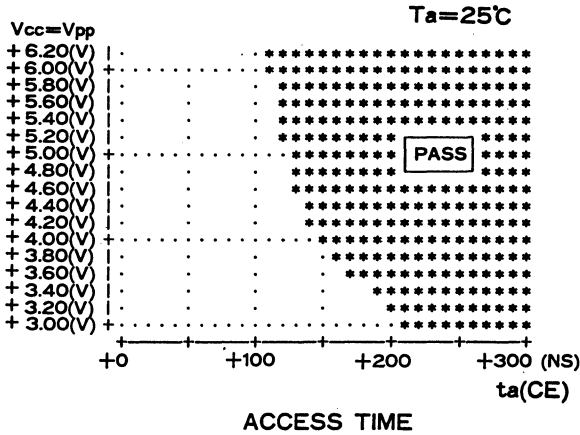
## BLOCK DIAGRAM



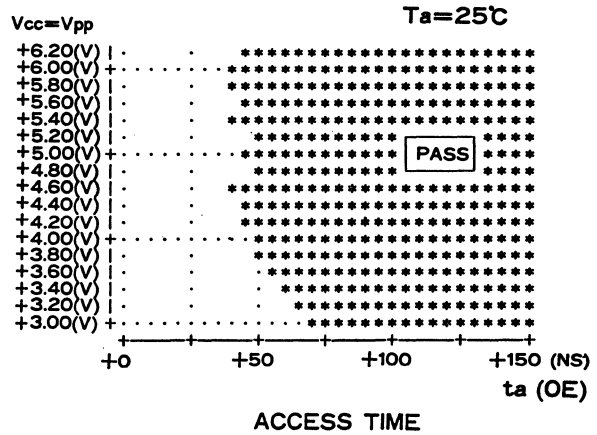


MF42M1-F1EAPXX

Card enable access time

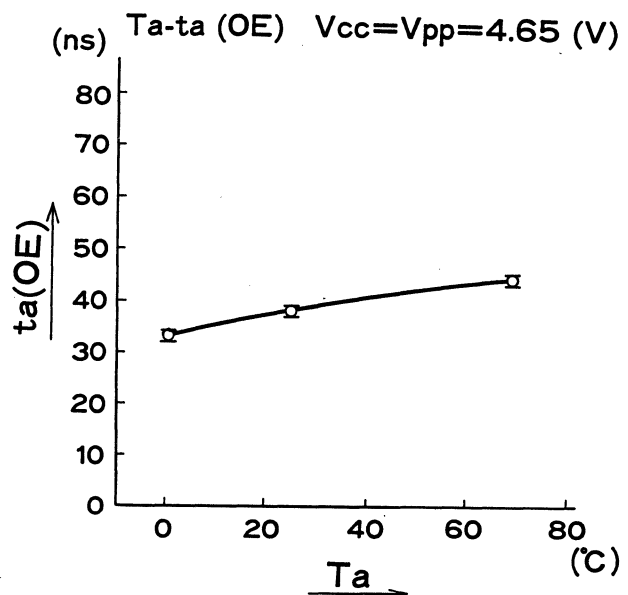
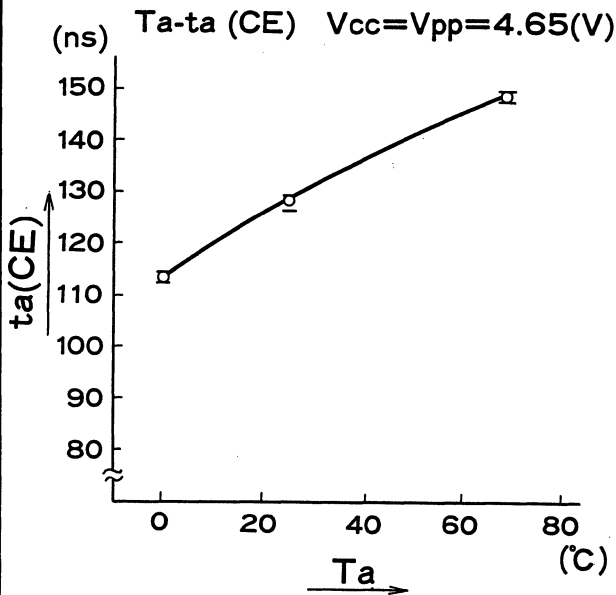


Output enable access time



MF42M1-F1EAPXX

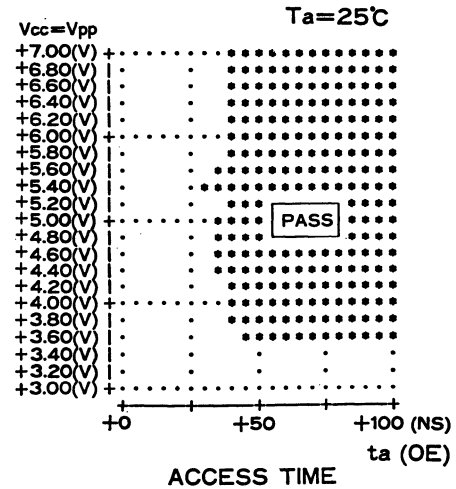
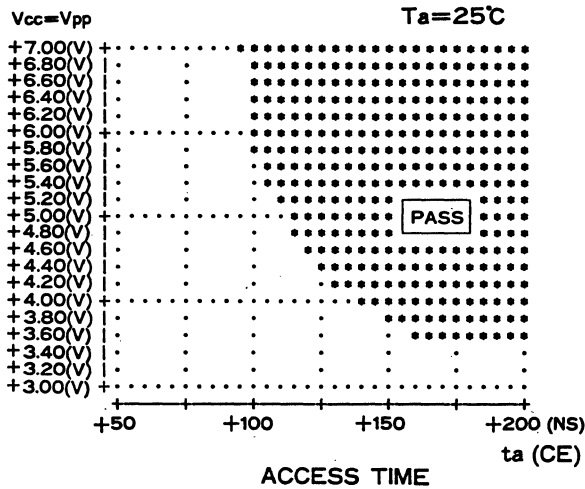
Access Time vs Ambient Temperature



# MF4512-F3EAPXX

Card enable access time

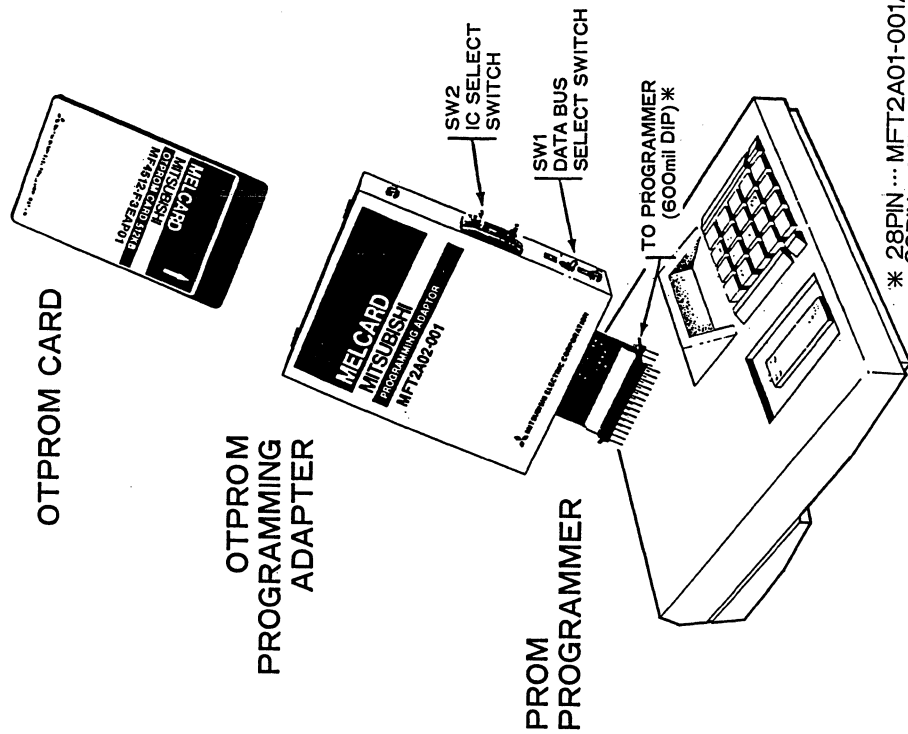
Output enable access time



## PROGRAMMING FLOW CHART [Card-Level Programming]

FLOW CHART	FAILURE RATE	NOTE
<div style="border: 1px solid black; padding: 5px; text-align: center;">PROGRAMMING &amp; DATA CHECK</div>	[Programming error] 0.1~1%/IC (average 0.3%)	Programming error
<div style="border: 1px solid black; padding: 5px; text-align: center;">BAKING (125°C) 40hr</div>		Baking method is the other method of burning in. But please understand that the panel color may change slightly. In that case please paste labels on the card panel.
<div style="border: 1px solid black; padding: 5px; text-align: center;">DATA CHECK</div>	[Baking error] 0.1~1%/IC (average 0.3%)	

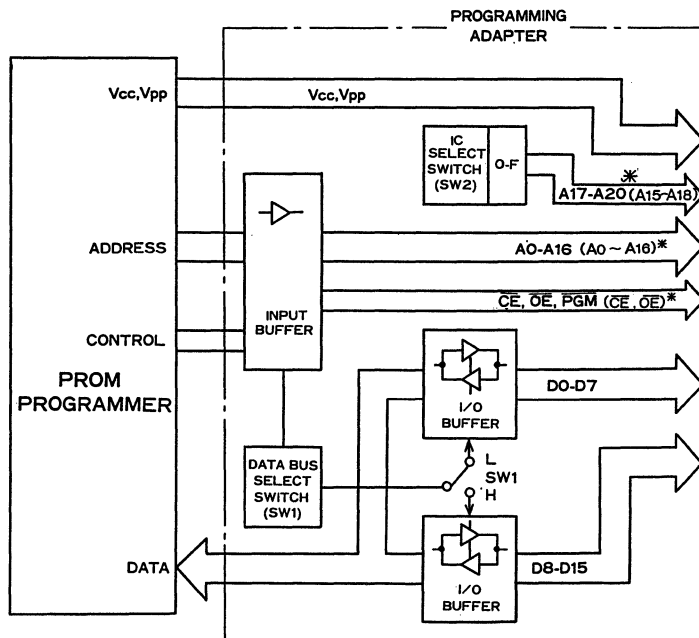
OTPROM MEMORY CARD PROGRAMMING ADAPTER



\* 28PIN ... MFT2A01-001/002  
 32PIN ... MFT2A02-001/002  
 40PIN ... MFT2A03-001

MFT2A02-001/002

BLOCK DIAGRAM



OTPROM CARD

\* ( ) Signal · MFT2A01-001/002



**MELCARD**

## Programming Adapter Selection Table of Card and Programmer

[256Kbit PROM Type]

Adapter Part Number	Card Type	Recommended PROM Programmers			
MFT2A01-001	(8bit) MF432A-F2XXPXX MF464A-F1XXPXX MF4128-F1XXPXX MF4256-F1XXPXX MF4512-F1XXPXX	MAKER	TYPE	SOCKET	ROM TYPE
	(16bit) MF465A-F1XXPXX MF4129-F1XXPXX MF4257-F1XXPXX MF4513-F1XXPXX	DATA I/O	280		F/P CODE =93/32
MFT2A01-002	(8bit) MF4128-F2XXCXX MF4256-F2XXCXX MF4512-F2XXCXX	Minato Electronics	Model 1890		E510
	(16bit) MF4129-F2XXCXX MF4257-F2XXCXX MF4513-F2XXCXX	Advantest Corp.	R4949	R49492B	256I
		Ando Electric Co., Ltd.	AF9720		256
		Promac Data Systems Corp.	Model 2A		256
		Ando Electric Co., Ltd.	AF9704		256



**MELCARD**

## Programming Adapter Selection Table of Card and Programmer

[1M bit PROM Type]

Adapter Part Number	Card Type	Recommended PROM Programmers			
MFT2A02-001	(8bit) MF4128-F3XXPXX MF4256-F3XXPXX MF4512-F3XXPXX MF41M0-F1XXPXX MF42M0-F1XXPXX	MAKER	TYPE	SOCKET	ROM TYPE
	(16bit) MF4257-F3XXPXX MF4513-F3XXPXX MF41M1-F1XXPXX MF42M1-F1XXPXX	Minato Electronics	Model 1890		E72A
MFT2A02-002	(8bit) MF4128-F4XXCXX MF4256-F4XXCXX MF4512-F4XXCXX MF41M0-F2XXCXX MF42M0-F2XXCXX	Advantest Corp.	R4949	R49492B	1MH2
	(16bit) MF4257-F4XXCXX MF4513-F4XXCXX MF41M1-F2XXCXX MF42M1-F2XXCXX	Ando Electric Co., Ltd.	AF9704		2201
		Promac Data Systems Corp.	Model 2A		2201
		Minato Electronics	Model 1890		E716
MFT2A03-001	(16bit) MF4129-F3XXPXX	Advantest Corp.	R4949	R49493B	1MH1
		Ando Electric Co., Ltd.	AF9704		2202
		Promac Data Systems Corp.	Model 2A		2202

**EEPROM CARD**

[8KB/16KB/32KB/64KB/128KB/192KB]

**DESCRIPTION:**

EEPROM card which is placed twenty-four 64Kbit EEPROM devices maximumly.

**FEATURES:**

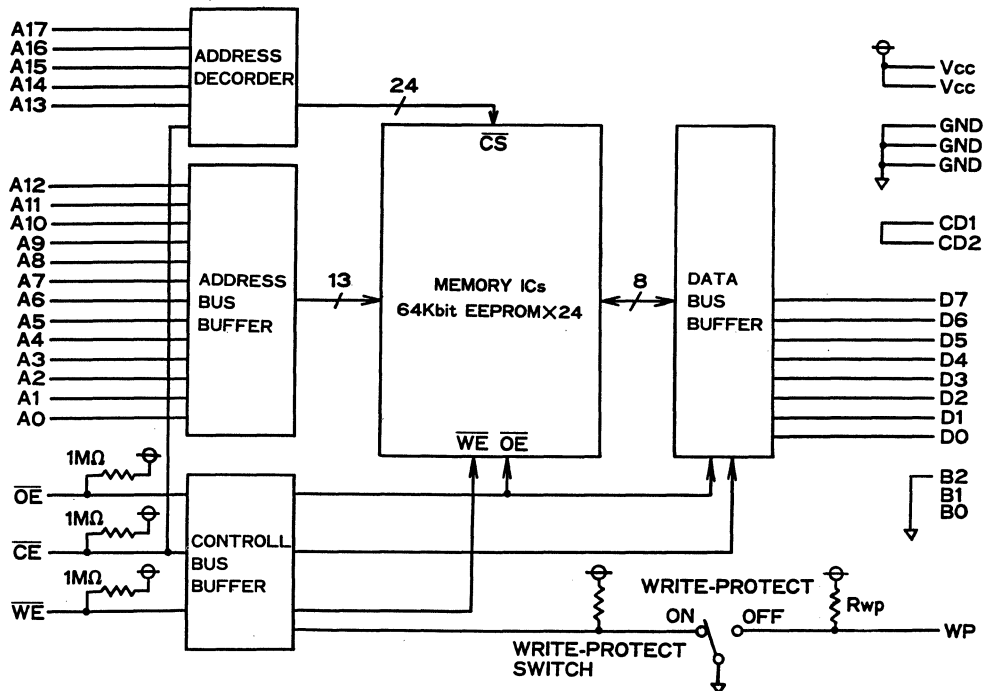
- Fast read access time : 250ns
- Data polling
- Page mode write : 32bytes
- Automatic erase before write : 10ms max.
- Erase/write cycle : 10,000 cycles min.
- data retention : 10 years min.
- Buffers on address and data bus

**APPLICATION:**

Factory automation, NC machine, Telephone

**MF8192-F1EAPXX (192KB EEPROM CARD)**

**BLOCK DIAGRAM**

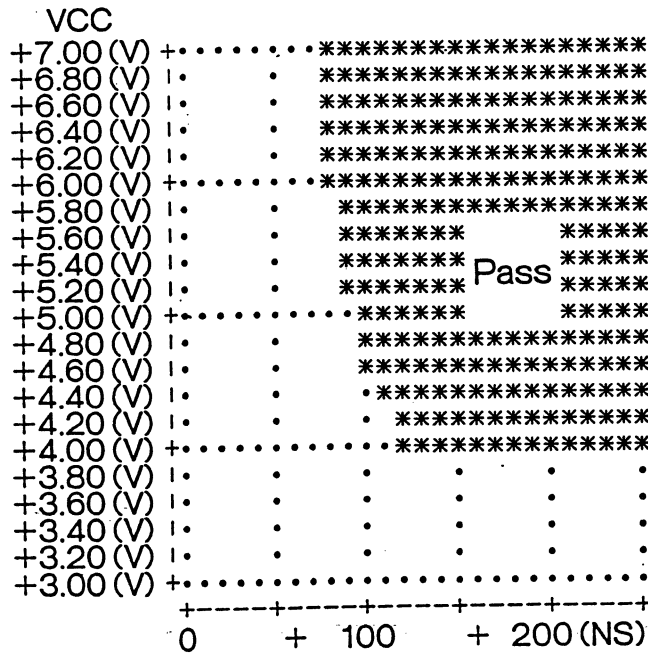




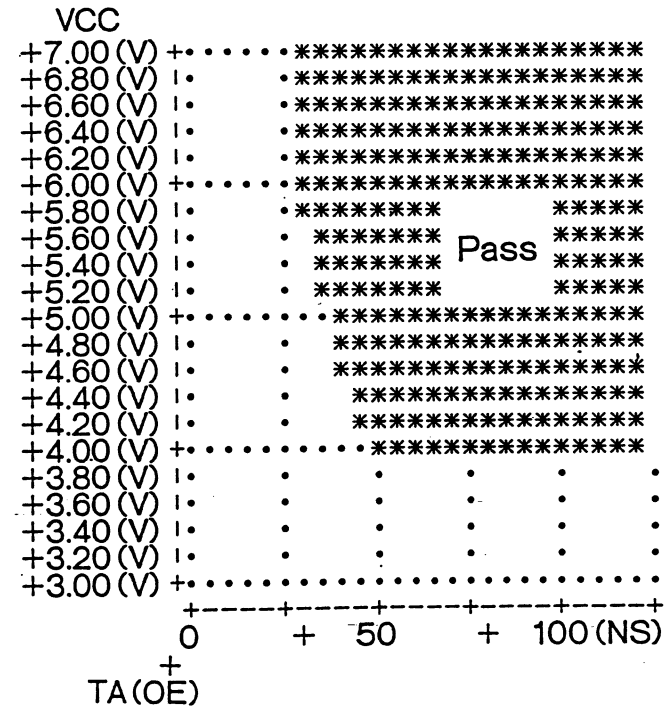
# MF816A-FIEAPXX

Card Enable access time  
Ta = 25°C

Output Enable access time  
Ta = 25°C



ACCESS TIME ta(CE)



ACCESS TIME ta(OE)

**DRAM CARD**

[512KB/1MB/2MB/3MB]

**DESCRIPTION**

These are consisted of industry standard 256KX4 dynamic RAMs in Very Small Outline Package (TSOP).

The mounting of TSOP make possible the thin outline and large memory capacity card.

**FEATURES**

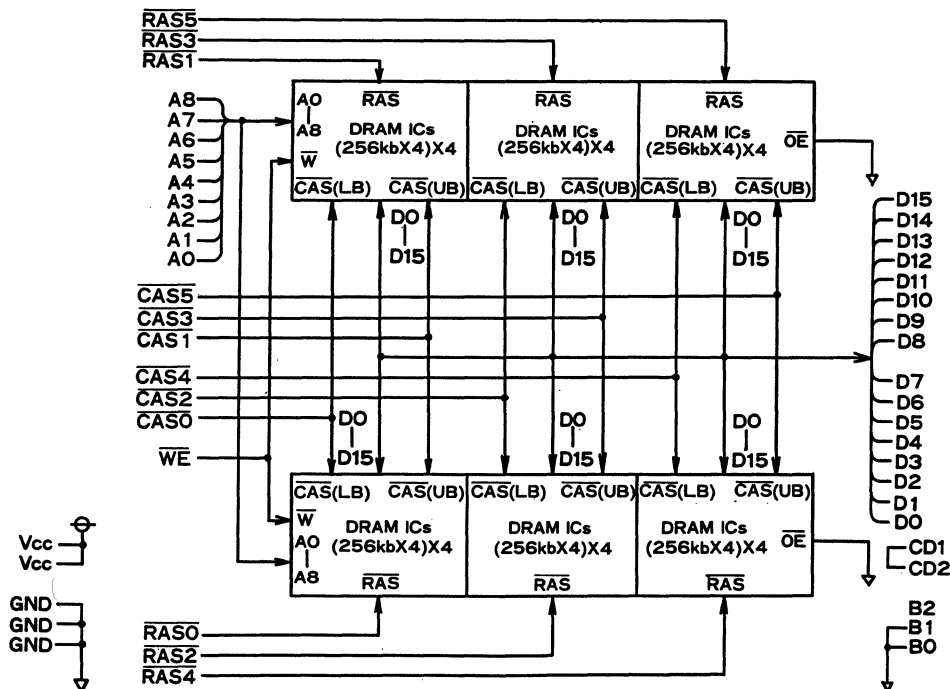
- High Speed : Access Time 150ns.
- Standard Card Size : 54mm(W)X85.6mm(L)X3.4mm(T).
- 60pins 2piece connector type.
- Low stand-by current.
- 512 refresh cycles Per 64mS
- RAS only refresh, CAS before RAS refresh, and Hidden refresh, modes are available and Page-mode Capabilities.

**APPLICATION**

Main/Extension memory unit for FAX, Personal computer.

**MF13MI-M1CAPXX (3MB DRAM CARD)**

**BLOCK DIAGRAM**



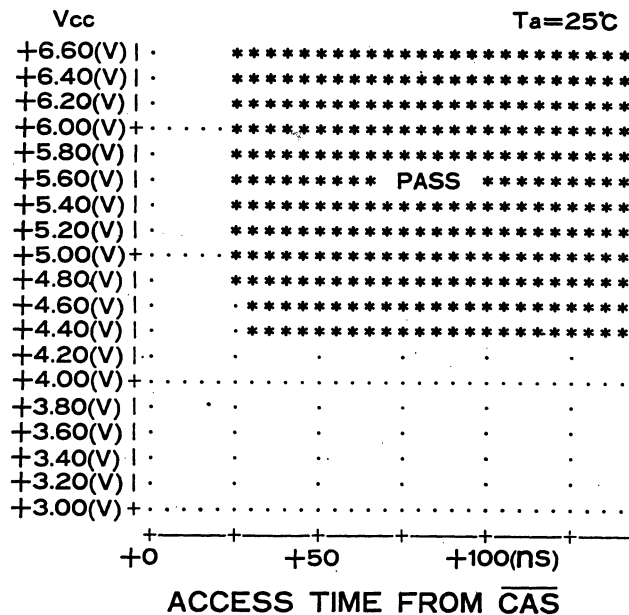
## Features of DRAM CARD

(512KB/1MB/2MB/3MB, 16bit DATA width)

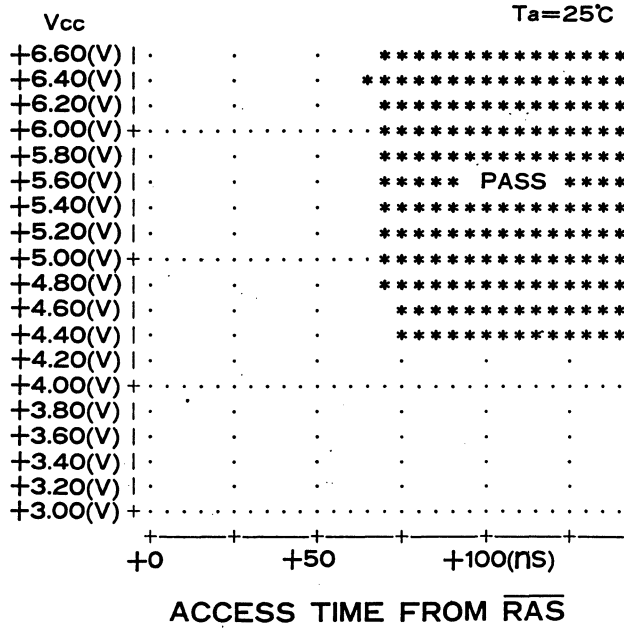
Memory Capacity	Access Time (Max, ns)	Operation Current (Max, mA)	Stand-by Current (Max, mA)		Control Pin	
			$\overline{RAS}=\overline{CAS}$ =V <sub>IH</sub>	$\overline{RAS}=\overline{CAS}$ =V <sub>CC</sub> -0.5V	$\overline{RAS}$	$\overline{CAS}$
512KB	150	200	8	2	$\overline{RAS0}$	$\overline{CAS0}, \overline{CAS1}$
1MB	150	208	16	4	$\overline{RAS0}, \overline{RAS1}$	$\overline{CAS0}, \overline{CAS1}$
2MB	150	224	32	8	$\overline{RAS0}, \overline{RAS1}$ $\overline{RAS2}, \overline{RAS3}$	$\overline{CAS0}, \overline{CAS1}$ $\overline{CAS2}, \overline{CAS3}$
3MB	150	240	48	12	$\overline{RAS0}, \overline{RAS1}$ $\overline{RAS2}, \overline{RAS3}$ $\overline{RAS4}, \overline{RAS5}$	$\overline{CAS0}, \overline{CAS1}$ $\overline{CAS2}, \overline{CAS3}$ $\overline{CAS4}, \overline{CAS5}$

## MF12M1-M1CAPXX

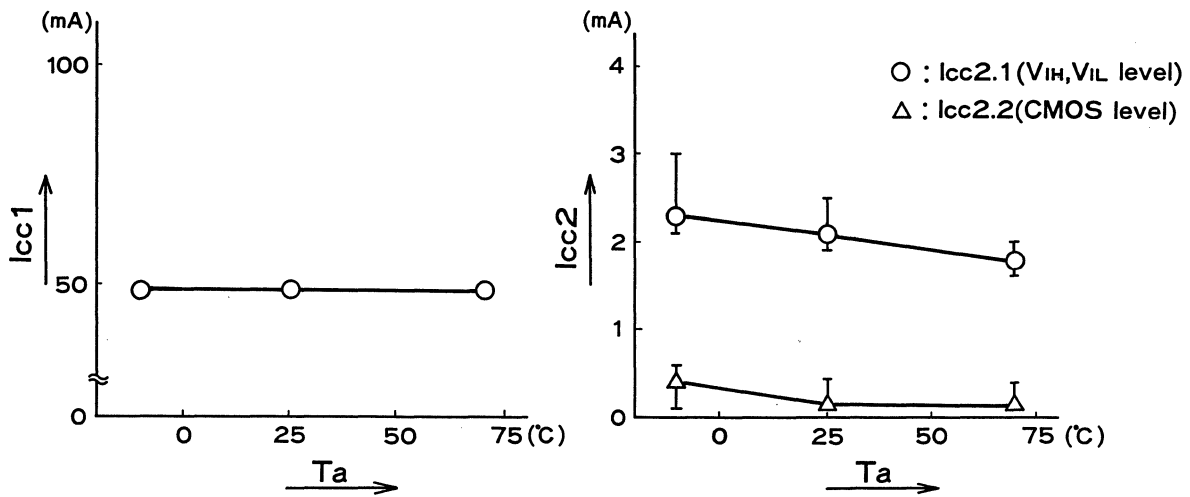
### ACCESS TIME FROM $\overline{CAS}$



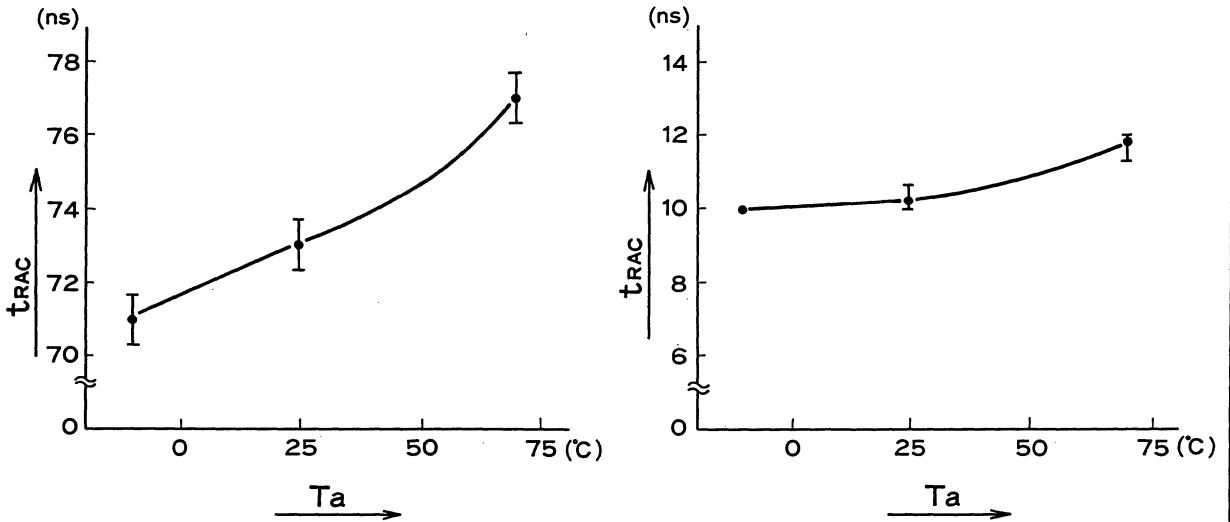
### MF12M1-M1CAPXX ACCESS TIME FROM RAS



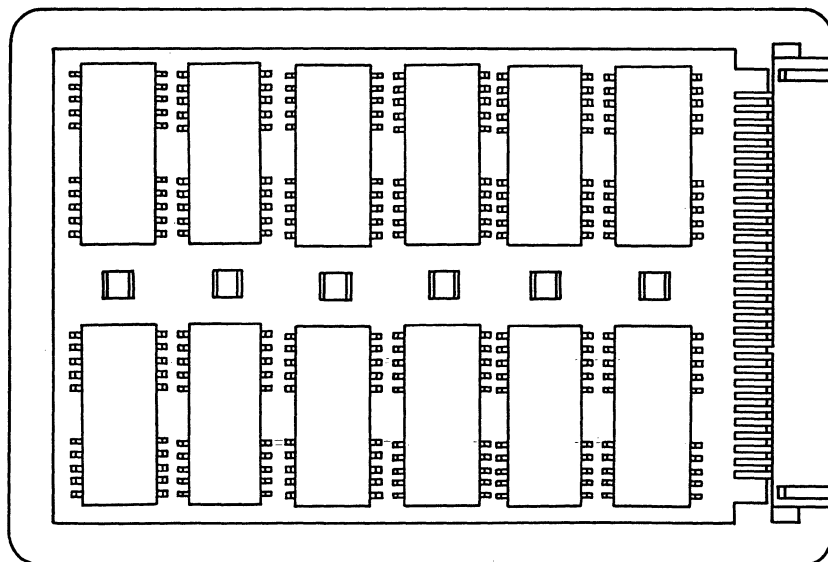
### 512KB DRAM CARD (MF1512-MICAPXX) Supply Current (Icc1, Icc2) vs Ambient Temperature



### 512KB DRAM CARD (MF1512-MICAPXX) Access Time vs Ambient Temperature



### 12MB\* DRAM CARD LAYOUT (Preliminary)



\* 12 pieces 4Mbit DRAM IC each side of PCB=Total 24 x 4Mb DRAM IC's

## DRAM CARD [2MB/4MB/8MB/12MB]

### DESCRIPTION

These memory cards contain 4,8,16 or 24 industry standard 1Mb×4 Dynamic RAMs in Thin and Small Outline Package(TSOP). The use of TSOP makes possible 3.4mm card thickness and highest density memory capacity credit card size.

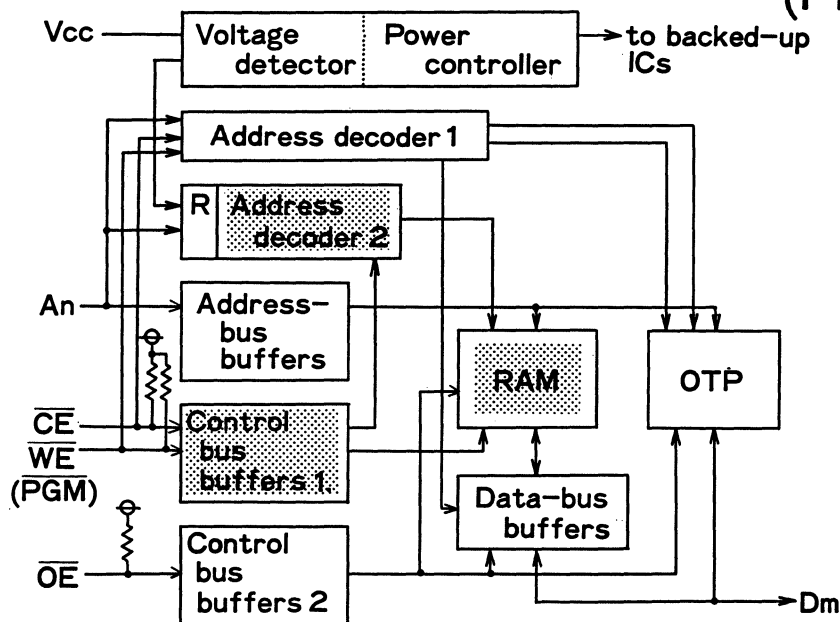
### FEATURES

- High Speed : Access Time from  $\overline{\text{RAS}}$  150ns.
- Standard Card Size : 54mm(W)×85.6mm(L)×3.4mm(T).
- 60pins pin-and-socket (2p)connector type.
- Low stand-by current
- $\overline{\text{RAS}}$  only refresh,  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh Hidden refresh, and Page-mode functions are available.

### APPLICATION

Main/Extension memory unit for Personal Computer, Laser-Printer, FAX etc.

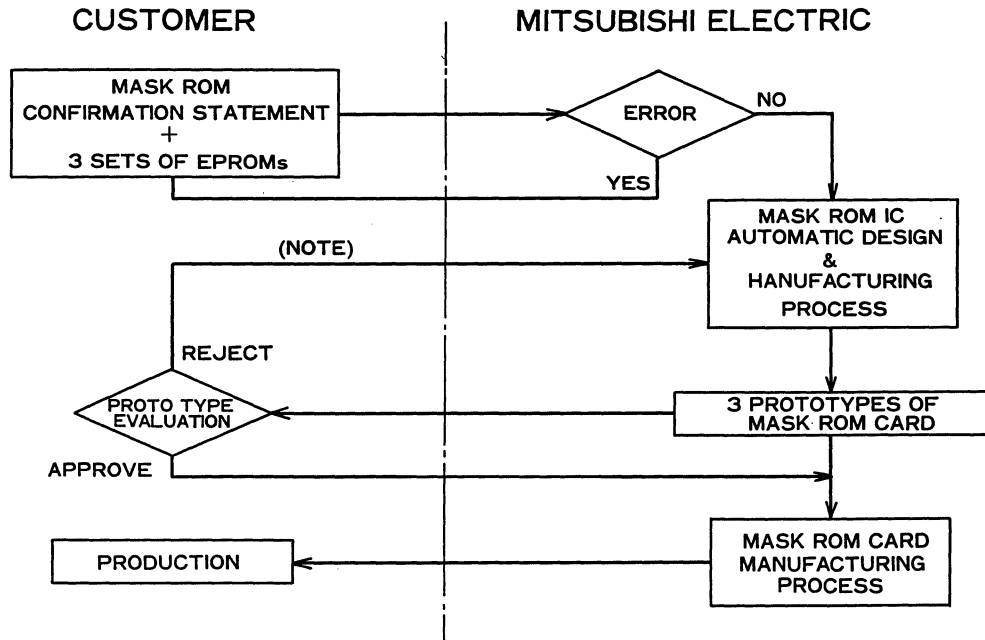
## Block diagram of Mixed card (RAM/OTP) (Preliminary)



..... Backed-up ICs

R: pull-up or pull-down resistors

# MASK ROM CARD DEVELOPMENT SYSTEM



(NOTE) If the customer change the MASK ROM code, another MASK ROM charge is required.

# EJECTION TYPE CONNECTORS

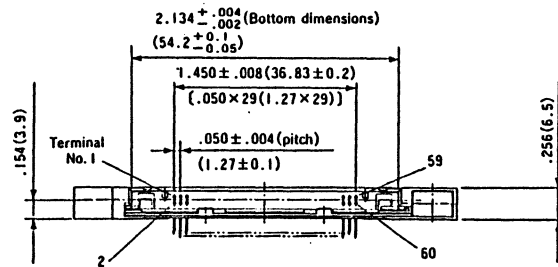
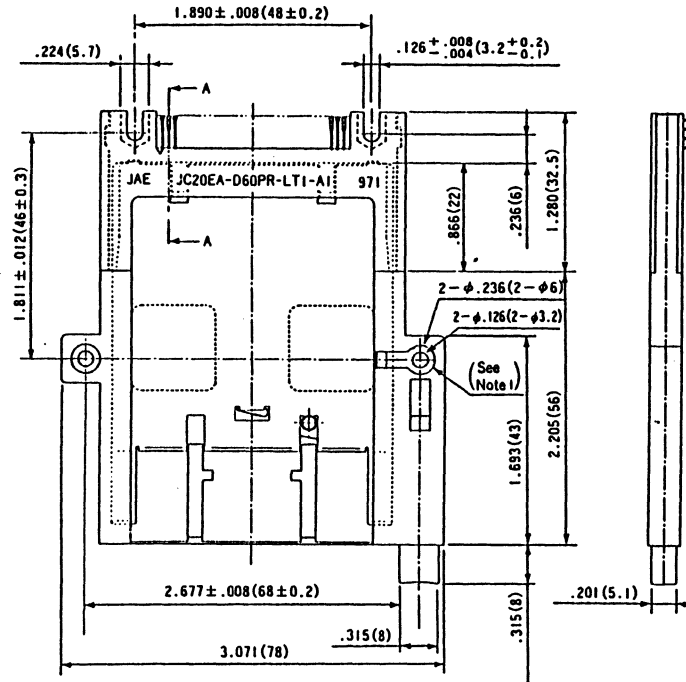
Applicable Card Type	Mfr, Part Number and Mfr	Mechanism for ejection	Dimensions
2P (60pin)	86933-001 Mfr : Du pont	Push-Button Ejection	70mm(W) × 86.5mm(L) × 10mm*(H)  (4mm stand-off)
	JC20EA-D60PR-LT1-A1 Mfr : JAE	Push-Button Ejection	78mm(W) × 88.5mm(L) × 6.5mm*(H)
CE (50pin)	HGC032-01-010 Mfr : HOSHIDEN ELECTRONICS	Spring-Activated Push In-Push Out	70.5mm(W) × 90mm(L) × 14mm*(H)

※Hight is from PCB





49

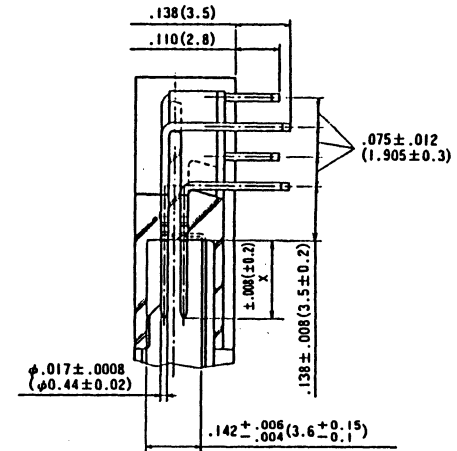


**JAE**

**CONNECTOR WITH ONE-PUSH EJECTOR BUTTON**

●PART NUMBER : JC20EA-D60PR-LT1-A1

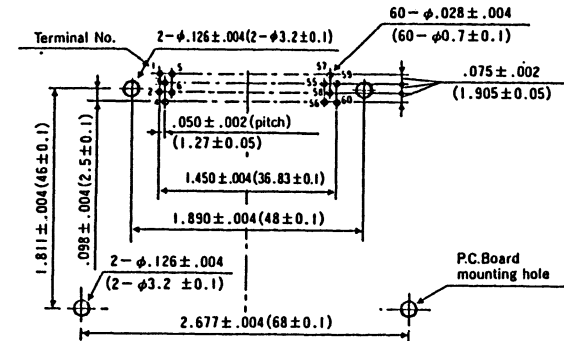
Section A-A



**DIMENSION X**

Terminal Nos. 29, 30, 32, 59, 60	.197"(5mm)
Other terminals	.157"(4mm)

●P.C.B. MOUNTING HOLE DIMENSIONS (Ref.)



(Note 1) Shown here is the lug mounting position for using an optional version with a grounding lug. The P.C. Board mounting hole requires a ground area to connect this lug.

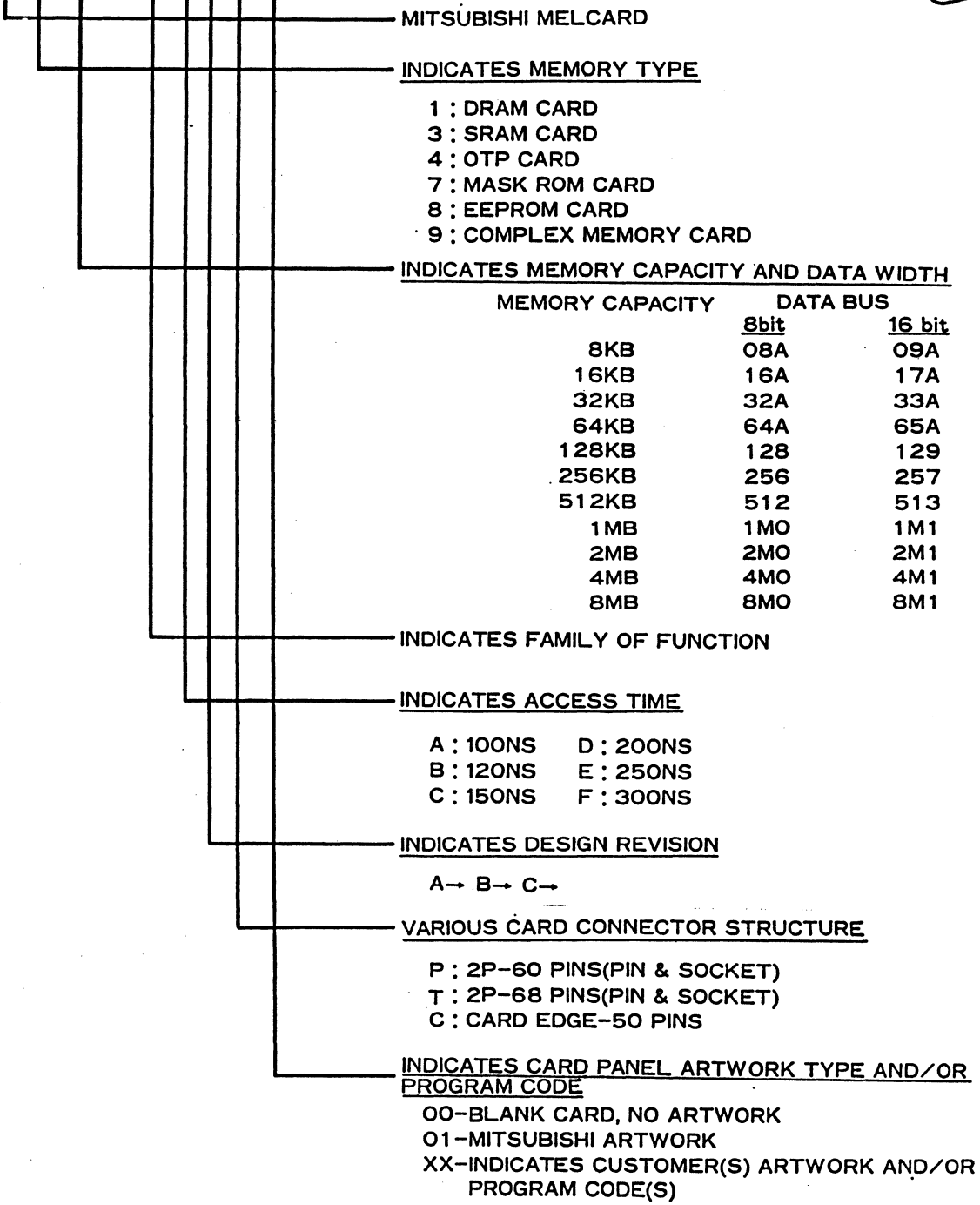


MELCARD

MITSUBISHI ELECTRIC  
MEMORY CARD PRODUCT DESIGNATION



MF 3 128 - M1 E A P XX



Notes:

Notes:



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# MITSUBISHI ELECTRONICS AMERICA, INC.

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FAX: 408-720-0104

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FAX: 213-217-5781

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San Diego, CA 92127  
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FAX: 914-896-8639

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