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SUBJECT: OPERATION OF THE IN-OUT ELEMENT

To: **Distribution List**

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Date: February 26, 1954

Abstract: In the system of terminal equipment installed in the WWI computer, control of a complete input or output operation involves three factors, the in-out element, computer subprograms, and the individual external unit control. A detailed description of the complete system logically is made up of descriptions of the operation of each of the terminal units. This report describes the functions of the in-out element (IO switch, IO control, and IO register) which is time shared among all the units. Since the in-out instructions, by which the computer controls the actions of external units, are intimately associated with the in-out element, a detailed description of these instructions is also contained in the report. Frequent references are made to separate reports to be written describing operations of the individual terminal units. It is planned that the present report on the in-out element in conjunction with one of these separate reports will constitute a complete explanation of the operation of a given piece of terminal equipment.

This note is a revision of and therefore replaces Engineering Note E-466, Operation of the In-Out Element, by E.S. Rich and Engineering Note E-499, Operation of the Block Transfer Orders, by B.E. Morriss.

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1.0 WWI TERMINAL EQUIPMENT SYSTEM

1.1 General Arrangement

Applications of the WWI computer which are being studied or which have been contemplated require a flexible system of terminal devices to permit communication between the computer and both human controllers and remote equipment external to the computer. Since this system includes many separate input units and output units, some of which have more than one mode of operation, a means of programmed selection among units and modes of operation is required, and complete control of the unit function by the computer must be provided. Few of the devices to be incorporated into the WWI terminal equipment system were designed specifically for such an application. The controls required for the various units, therefore, although similar in some respects, differ considerably in many of their details. To reduce the total amount of equipment in the system, a centralized selection and control element (In-Out Element) was designed to accomplish the control functions which are common to many or all of the terminal units. A further reduction in the amount of circuitry required was obtained by utilizing computer subprograms to accomplish certain control functions. Thus, in the WWI terminal equipment system the control of a complete in-out operation involves three factors: The in-out element, computer subprograms, and the individual external unit control.

1.2 Organization of Reports Describing System

A detailed description of the complete terminal equipment system logically breaks down into descriptions of each of the terminal devices since these are essentially independent units. For expediency, it is planned that this complete description will take the form of a series of E-notes and M-notes each dealing with one unit or class of units. A list of the existing notes on individual units is presented in Appendix A. This list will be changed as additional notes are completed. However, to avoid excessive repetition in successive reports, a discussion of the in-out element and of the computer control orders which are common to all terminal devices is presented separately in this report. It is the writer's opinion that one should not strive necessarily for a complete understanding of the in-out element per se since some features apply to a limited number of terminal units. It is intended that this report be read in conjunction with one describing a particular type of terminal device. In combination, then, the two reports will contain a complete explanation of the operation of that type of unit.

2.0 GENERAL DESCRIPTION OF TERMINAL EQUIPMENT SYSTEM

2.1 Terminal Devices

A general background on the scope of the WWI terminal equipment system may be obtained by referring to Engineering Note E-450. This note briefly summarizes the purpose of the system and the types of units contained in it, and it presents a few of the problems which have

arisen during its design. For completeness in the following discussions, a list of the devices whose incorporation into the WWI terminal equipment system has been actively undertaken is given below.

(a) Paper tape and printing units, including

1) Photoelectric readers
2) Mechanical readers
3) Punches
4) Printers

(b) Display oscilloscopes with automatic vector and character generators

(c) Scope cameras

(d) Magnetic tape units (each can be a reader and recorder)

(e) Magnetic drum for auxiliary computer storage

(f) Magnetic drum for buffer storage for multiple asynchronous inputs and outputs

(g) Indicator lights

(h) Insertion switches

(i) Miscellaneous special-purpose devices as required for special computer applications.

2.2 Basic In-Out Transfer Processes

For each unit of terminal equipment one can define a basic process or cycle which accomplishes the reading or recording of a single word. For the units listed, the digits of a word are handled in parallel although the length of the word varies from two digits in the case of magnetic tape to 16 digits in the case of magnetic drums. For some units (e.g. magnetic drum) each cycle of operation requires an initiation pulse from the computer while for other units (e.g. magnetic tape) the basic cycle will continue as long as the unit is selected by the computer. In general there is a precise time during the basic cycle of a unit when the actual information transfer to or from the unit takes place. This timing is governed entirely by the unit so facilities must be provided for handling the transfer when it occurs. It is usually undesirable to hold up the computer program for terminal units with a relatively long period in the basic cycle. Therefore, a buffer register (the in-out register, IOR) is contained in the in-out element to receive such transfers. The computer program can continue in parallel with these transfers for single reading or recording operations. However, for units such as magnetic drums the period of the basic cycle can be reduced by controlling the time of requesting transfers to and from these units. Therefore, special instructions called the block transfer

instructions are available. As the name implies these instructions will transfer blocks of information to and from the external units. These orders depend on equipment within the computer and thus do not allow parallel operation. The data flow during an in-out operation, then, may be outlined as follows. For recording, the computer program transfers a word to IOR and starts a recorder which later takes the word from IOR at the proper time in its recording cycle. For reading, the computer program first clears IOR, then starts a reader. At some point during this cycle a word is transferred to IOR. Following this the computer program must transfer the contents of IOR to the desired destination within the computer.

The sequences just described illustrate in part how the control of a complete in-out operation involves a computer subprogram, action by the in-out element, and action by an individual unit control. In general, the subprogram is needed to specify the terminal device and mode of operation desired and to handle the necessary data transfers between the computer and the IOR. The in-out element provides coordination between the operations of the computer and those of the external units, while the unit controls are essentially matching circuits to permit physical interconnection between the terminal devices and the IOE.

2.3 Functions of the In-Out Element

The coordination provided by the IOE includes the following specific functions:

(a) Selecting external units and their modes of operation.

(b) Providing buffer storage for data being transferred between the computer and external units.

(c) Stopping the computer if it attempts to get ahead of an external unit.

(d) Giving an alarm if an external unit gets ahead of the computer program.

(e) Synchronizing computer and external pulse signals.

(f) Allowing certain external units to operate through several in-out processes or cycles in response to a single computer order.

(g) Allow automatic assembly or breakdown of 16-digit computer words for units whose words contain less than 16 digits.

(h) Provide a means of terminating an in-out operation and indicating unsuccessful transfers to the computer for units capable of giving such indications.

(i) Counting any delays needed between steps in the in-out operation.

All of these actions may not be required with every piece of terminal equipment. In fact function (a) is the only one which is involved in all cases. The differences stem from whether the unit is a reader or a recorder, whether it handles words one at a time or in blocks, from its relative operating speed, and from the actual form which the data transfer signals must take. These differences will be dealt with in detail in the reports for the individual units.

2.4 General Operation of the In-Out Element.

Essential to a complete understanding both of the operation of the various terminal devices and of the operation of the IOE is a discussion of the computer instructions which initiate and control in-out transfers. However, a detailed description of these instructions cannot be given without specific reference to elements of the IOE and to the characteristics of certain terminal units. In the following section a general outline of the in-out instructions including typical instruction sequences is given, and in Section 2.42 the elements that make up the IOE are briefly discussed. Folllowing that (Section 3.0) a complete explanation, combining the functions of IOE and the in-out orders is given. In the latter section, features that are peculiar to certain units are indicated so that, if desired, one may ignore those portions of the discussion which are not pertinent to the terminal unit being studied.

2.41 In-Out Instructions.

The transfer of information between the computer and terminal units is accomplished by sequences containing two or more instructions from the following list of special in-out instructions. Devices, such as the scope camera, for which a control action alone is required, use only a single instruction (si).

1. si - Select In-Out Operation. The si instruction stops any unit which had previously been selected and selects and starts a unit and mode of operation determined by the address section of the instruction. Other special actions are started on this instruction depending on the unit and mode of operation selected. Some of these actions are:

(a) Initiate reading for single-cycle readers such as magnetic drums.

(b) Transfer the content of AC to the vertical decoder for display purposes.

(c) Transfer the content of AC to the magnetic drum for selecting a starting drum address.

(d) Transfer the content of AC to one-half of the register of the output coder.

(e) Set IOC to form interblock space and record block marker for magnetic tape record.

2. rc - Record. Except for display scopes the rc instruction will transfer the content of AC to IOR and initiate recording in the unit selected. In this case the address section of the instruction has no significance. If display is selected the content of AC sets the horizontal decoder and the content of the register specified by the address section of the instruction is transferred to IOR. This information is used for vector and numerical displays.

3. bo - Block Output. The bo instruction transfers the contents of AC to the IO delay counter to specify the number of words to be read. It also initiates an automatic transfer of words from computer storage to the recorder selected with the first word coming from the storage register corresponding to the address of the bo instruction. Successive words are taken from consecutive storage registers. The number of words recorded is counted in the IO delay counter so that process is stopped by an end-carry from this counter or for some units, such as the buffer drum, by an unsuccessful recording indication.

4. bi - Block Input. The bi instruction transfers the contents of AC to the IO delay counter to specify the number of words to be read. It also performs an automatic transfer of a block of words from the reader into the storage registers starting with the register corresponding to the address of the bi instruction. Successive words are placed in consecutive storage registers. The number of words read is counted in the IO delay counter so the process is stopped by an end carry from this counter or for some units, such as the buffer drums, by an unsuccessful reading indication. A bi instruction of zero-block length may lead to trouble in a program and should be considered illegal (see Section 3.55).

It is necessary that the in-out instructions occur in the proper sequence although other computer instructions may be interspersed among them. The number of computer instructions that may be performed between in-out instructions varies among the different terminal units and depends on the inherent timing in each unit. The sequences of instructions which may be used are also dependent on the unit being selected. Therefore reference should be made to the individual report on a unit to determine which sequences are applicable. Some units may use the block transfer instructions while others may not. Some readers require an si instruction with each rd or bi instruction while others may use as many rd or bi instructions (up to the capacity of the reader) as desired. In general, the number of rc or bo instructions which may be given after an si instruction selecting a recorder is limited by the capacity of the recorder. This may be as low as one recording as is the case with the output coder.

The in-out sequences are given below. It will be obvious that, in certain cases, proper execution of the in-out instructions requires specific contents in AC at the time of the instruction. Since the required AC content may be derived in different ways, instructions for inserting the necessary information into AC are not included in the sequences.

(a) Single Read for each Selection

Sequence		Effect
si (reader)	- - si (reader)	Select and start single-cycle reader which then reads one word to IOR and stops. Other special functions are also performed.
rd (x)		
-	- - rd (x)	Transfer content of IOR to AC.

Only one rd instruction is permissible. For some units the rd instruction may be replaced by a bi instruction.

(b) Multiple Read for each Selection

Sequence		Effect
si (reader)	- - si (reader)	Selects and starts desired reader and performs other special functions.
rd x		
rd x	- - rd x	Initiate reading if necessary. After word has been read, transfer word from IOR to AC and prepare IOR for next read.
-		
-		
rd x	- - si (stop)	This order necessary only for continuous cycle readers. Any si instruction will stop any unit which may be operating at the time.
si (stop)		

For some units any or all rd instructions may be replaced by bi instructions.

(c) Recording

Sequence	Effect
si (recorder)	si (recorder) - select recorder and perform other special functions (e.g. set vertical decoder.)
rc x	rc x-transfer word from AC (recorders other than scopes) or storage (for scopes) to IOR. Initiate recording. Address x applies only to display scopes.
rc x	
-	
-	
si (stop)	si (stop) - required only for continuous cycle recorders. Magnetic tape has a special stop-after-record mode.

For some units any or all rc instructions may be replaced by bo instructions.

2.42 Units of the In-Out Element

The IOE may be broken up into three major parts, (1) In-out switch (IOS,420), which accomplishes function (a) of the nine listed in Section 2.3, (2) the in-out register (IOR,403), which provides function (b) and to which reference has already been made, and (3) the in-out control (IOC, 410), which serves functions (c) through (i). Descriptions of these parts are given below.

2.421 In-Out Switch (IOS,420). The in-out switch is an 11-digit register with connections to and from the computer bus. This register operates a crystal matrix which decodes the words read into the register into a large number of outputs. Selection of an external unit in a particular mode of operation is accomplished by the transfer to IOS of an 11-digit character (or address), which is the code of the desired selection.

Physically, the crystal matrix just referred to consists of an assembly of several matrices, as shown in drawing C-37326. An 8-position matrix connected to three digits of the IOS register is used to select one of eight other matrices corresponding to eight different classes of terminal equipment (i.e., paper tape and printing equipment, scopes, magnetic tape units, magnetic drums, etc.). Each of the latter matrices is designed to provide the selection and control actions which are peculiar to its respective class of terminal units. These matrices are controlled by some of the remaining digits of the IOS register. Drawing B-37314 of the magnetic tape matrix is attached as an example.

A given setting of IOS may energize several output lines, and certain output lines are energized by more than just one particular IOS content. For example, if one wants to record in the forward direction on magnetic tape unit #2, the corresponding setting of IOS would raise the potential of the following, and only the following, output lines (see drawing B-37314):

C01 & MT02	Record
C05 & MT16	All magnetic tape units
MT10	Unit #2
MT11	Unit #2 forward

The flip-flops of IOS have output gate tubes to permit the checking of the transfer from storage to IOS. Note, however, that the checking loop includes only the flip-flops of IOS, not the switching matrix also. Complete checking of the selection would incur considerable complication of equipment, and since matrix operation has proved very reliable in WWI experience, such checking is ommitted in the interest of simplicity.

2.422 In-Out Register (IOR,403). The purpose of the in-out register (see drawing C-50820) is to store the word the program has supplied for recording until the selected recorder calls for it, and to store the word read from the selected reader until the program removes it. IOR also has facilities for shifting. In the case of magnetic tape IOR is shifted to form 16-digit characters when recording. Similarly, in one mode of reading punched paper tapes, the IOR is shifted to form 16-digit words from groups read off the tape. All shifting is from right to left. Additional gate tubes are provided on the IOR for reading to the check bus to check transfers between IOR and the computer.

2.423 In-Out Control (IOC,410). The seven functions of IOE which are performed by the IOC (functions (c) through (i), Section 2.3) are accomplished by the following components that make up IOC (see drawing D-37320):

Synchronizer	(415)
Interlock	(413)
Alarm Control	(414)
IO Delay Counter	(404)
IO Control Counter	(411)
Reset Control	(412)
Shift Pulse Generator	(416)
Block Control	(417)

A brief description of these components follows and a detailed explanation of their operation is given in Section 3.0.

(a) Synchronizer (415). Pulses which originate in external units bear no fixed time relationship to computer clock pulses. Since certain of the pulses generated by external units must cause actions within sections of the IOE which sections also must independently respond to computer pulses, it is necessary to properly phase the external pulses with the computer pulses so that no ambiguous results can occur. This phasing is made possible by the IO synchronizer. Basically it exchanges an asynchronous input pulse (ASYNCHRONOUS INITIATION pulse) for the next occurring computer supply pulse.

For some external units, pulse synchronization is done as a convenience to assist in trouble shooting rather than as a necessity. For example, the photoelectric reader generates a 0.1 μs timing pulse to sense gate tubes controlled by the phototube amplifiers. Pulses out of these gate tubes constitute the parallel read-in to the IOR of one word. To

facilitate viewing these pulses and the consequent flip-flop transitions on the same synchroscope used for computer testing, the photoelectric-reader timing pulse is passed through the IO synchronizer, and the gate tubes are sensed by the resulting synchronized pulse. The read-in to the IOR, therefore, is accurately timed with respect to computer pulses.

(b) Interlock (413). The IO interlock prevents the computer program from getting ahead of the terminal unit which is operating. This interlock is a flip-flop which is set by the computer control whenever an in-out process is started and is cleared when the process is completed. In a computer program each instruction that calls for action by the IOE or by terminal equipment first sense the IO interlock. If it is cleared, the instruction will be carried out but if the interlock is set, the computer will be stopped. In the latter case, the computer is restarted when the particular in-out process is completed.

The interlock permits a computer program not involving in-out instructions to be carried out during the recording of reading processes. So for the most efficient use of the time between the recording or reading of two consecutive characters, the length of the computer program between in-out instructions should equal that required for the respective in-out process. If this program is shorter, the computer will be idle during the rest of the time interval, but if this program is longer, the in-out unit will wait if it can, or sound an in-out alarm if it cannot wait, as discussed in the next section.

(c) Alarm Control (414). The alarm control is provided to produce an alarm which stops the computer when either of two conditions occurs: (1) when the terminal unit gets ahead of the computer program (this would result from a programming error), or (2) when certain malfunctions occur in the terminal equipment in use (those for which warning signals are available). For some external units theoretically, the first condition could never occur so no programming alarm could be produced. These are single-cycle units which begin an in-out process only upon or after a specific command from the computer. Such units include:

(1) mechanical paper tape readers,

(2) paper tape punches,

(3) printers,

(4) display scopes,

(5) magnetic drums.

In contrast, devices that can get ahead of the computer program are continuous reading units such as magnetic tape and the photoelectric paper tape reader. These must carry out their reading processes, regardless of computer action when the moving tapes reach a particular position. If such units start a reading process before the computer program has prepared for this process, an alarm will be given by the IO alarm control.

Alarm control consists of a flip-flop which is set to its "Alarm" position by an external unit at the completion of each in-out process and is cleared to its "no-alarm" position by a computer pulse on each in-out instruction. The pulses from external units which set this flip-flop first sense a gate tube that is open when the flip-flop is in the "alarm" position, so if the flip-flop has not been cleared since the previous in-out process, an alarm results.

(d) IO Control Counter (411). The IO control counter allows certain external units to operate through several cycles or in-out processes in response to a single rc or rd instruction. It performs its task by counting and properly distributing the end-carries from the IO delay counter or synchronous Initiation pulses from the synchronizer which signify that one step or in-out process has been completed. These pulses must be distributed in two ways: (1) until the proper number of processes has been performed, they must give a cycle pulse to indicate that the step is over and the next step or process may begin; (2) after the proper number of processes has been performed, they must produce a completion pulse so that the next in-out order may proceed. The completion pulse (end-carry from IOC counter) clears the interlock, starts the computer if the computer stopped for the in-out process, sets the alarm control, and goes to those external units requiring a completion pulse.

With certain units only one cycle is desired per in-out order, so in such cases the control counter is preset to all ones and no cycle pulses are produced. The settings of the control counter required by units such as magnetic tape units, photoelectric readers, and scopes and the functions performed by the cycle pulses are described in the separate reports on these units.

(e) IO Delay Counter (404). The delay counter was incorporated in IOC to provide a facility for accurately and reliably timing the various steps in the operation of external units and of IOC. The use of a single flexible counter eliminates the need for several special-purpose counters or for relatively unreliable multivibrator delay elements. Delays up to 32 milliseconds may be measured. The delay pulse is always coincident with a low-frequency supply pulse from the computer and for this reason the delay is accurate only to about 5 microseconds. Examples of timing performed by this counter are the following:

(1) Time for IOS to set-up (about 15 microseconds)

(2) Length of magnetic tape recording pulse (about 150 microseconds)

(3) Time requiredto form an inter-block space on magnetic tape (about 12 milliseconds)

(4) Time for scope deflection amplifiers to stabilize following a change in deflection (about 30 microseconds)

(5) Length of scope intensification pulses.

The delay desired for a given operation is obtained by resetting the flip-flops of the counter prior to starting the count. This is accomplished through reset control (412) described in paragraph (f) below. The actual count may be started by an in-out order, by an external unit as required, or by cycle pulses from IO control counter.

The IO delay counter is also used for counting the cycles on block transfer orders. This is discussed in more detail in Section 3.5 which describes the block transfer orders.

(f) IO Reset Control (412). The IO reset control governs the settings of the IO delay counter and of the IO control counter at the start of an in-out operation or at the start of a cycle in an in-out operation. Reset control consists of gate tubes that are turned on and off by IOS. Its inputs are (1) pulses from the computer control matrix, (2) end-carries from the IO delay counter, (3) end-carries and cycle pulses from the IO control counter, and (4) special control pulses from external units. Appropriate mixing of input and output pulses is provided so that, for a given piece of terminal equipment (as determined by the setting of IOS), the two counters can be reset to any required value on one or more of the above listed input pulses. IO reset control also controls the distribution of pulses to other parts of IOE (e.g. set interlock and clear alarm control) and to in-out units.

(g) Shift-Pulse Generator (416). The shift-pulse generator is required for those units which operate through more than one read or record cycle in response to a single rd or rc instruction. Such units handle a 16-digit word by treating only a fraction of the total word at a time and repeating their operations until all 16 digits have been processed. In order to break the full-length word into parts, the shift-pulse generator is used to shift the IOR following each in-out cycle so that the next group of digits to be treated occupies the same position in the register that the preceding group held. Shifts of either two digits or five digits are provided by this generator.

(h) Block Control (417). The block control was originally installed to provide a means of exiting from the block transfer orders. However, certain units such as the buffer drum and output coder are capable of indicating whether a reading or recording operation has been successful. The block control is also used to transfer these indications to the computer for rd and rc instructions.

Block control is normally cleared and may be set only be an unsuccessful indication from an external unit or by an end-carry from IO delay counter when the counter is used to count the cycles in a block transfer instruction. The operations initiated because of the status of block control will depend on the pulse used to sense it. Block control will always be cleared after it has been sensed. The means and results of sensing block control are discussed in more detail in Section 3.0.

3.0 DETAILED OPERATION OF THE IN-OUT ELEMENT

The following sections describe the operation of the IOE in detail. Since the steps of its operation necessarily follow in the sequence of the control pulses in the in-out instructions, the details of these instructions are discussed concurrently. As was pointed out earlier, some features both of IOE and of the in-out instructions are peculiar to certain terminal devices. Discussions of these features are left for the individual unit reports where practical, but if contained here, their uniqueness is indicated by reference to specific terminal units.

3.1 Actions on the si Instruction

All in-out sequences start with an si instruction, the address section of which specifies the particular unit to be selected as well as the mode of operation desired of that unit. This instruction has standard program timing so only the operation timing will be discussed. For reference, the operation timing is listed in Table I attached. As with all in-out instructions, the instruction cannot be allowed to proceed if a previously started in-out operation has not been completed. The first pulse of operation timing (TP-6), therefore, is reserved for sensing the the IOC interlock to determine whether the computer should be halted. This question need be answered only if the previously selected terminal unit was a recorder (output unit). Since the program must always execute an rd or bi instruction following any action of a reader (input unit), any necessary computer stoppage on account of that reader will have occurred on the rd or bi instruction. A specific requirement of the rd instruction which will be clarified in Section 3.4 and in individual unit reports is that the IO interlock always be set on the rd instruction. Therefore, it not only is unnecessary to sense the IO interlock if the previously selected unit was a reader, but it is important that it not be sensed in such a case since otherwise the computer would be hung up.

Referring to the block diagram of IOC (drawing D-37320) the selective sensing is accomplished by GT01 in the interlock (413). This gate tube is controlled by the line C01 from IOS which is energized for all settings of IOS which select output units. If a reader has been selected and a new si instructions is programmed, the sense pulse finds GT01 off so the sense is deleted. On the other hand, if a recorder had been selected, GT01 would be on and the pulse would pass to GT02 and go out of the STOP CLOCK line to CPC to stop the computer. Simultaneously, it will clear the interlock flip-flop so that when a COMPLETION pulse is received from the IO control counter (411), signifying the end of the recording process, it will find GT03 on and so will pass through to the START CLOCK input of CPC and restart the computer. If the recording process had been completed before an si instruction was attempted, the COMPLETION pulse from IO control counter would have found the interlock flip-flop holding a ONE, GT03 would have been off preventing an unwanted START CLOCK pulse, and the pulse would have cleared the interlock after a short delay.

Following the SENSE (si)pulse, or the START CLOCK pulse if the computer had been stopped for completion of a recording operation, the remaining steps of the si instruction will occur in a normal fashion. On TP7 the flip-flops of $\overline{IOS}$ are cleared, and a STOP pulse is sent to those terminal units whose design is such that a pulse is required to stop their operation. The individual unit controls are arranged so that all units are stopped either by changing the IOS setting or by the STOP pulse. One-half microsecond after IOS is cleared, the new IOS setting is read into the IOS flip-flops from PAR which is holding the address section of the si instruction. The same information is also read on TP7 from PAR to $\overline{CR}$ via the check bus preparatory to a transfer check. On TP7.5 IOR is cleared, preparing it to receive information.

Also on TP7, an IOS DELAY START pulse is sent to IOC. This basically stops the computer clock for a length of time sufficient to allow the circuits of the IOS matrices to respond to the new setting of the IOS flip-flops. The response time of these circuits is about 15 microseconds. The clock delay, therefore, is necessary to insure that all gate tubes on the IOS outputs are fully on or off as required by the new IOS setting before the next time pulse since pulses at that time must be gated by IOS. Specifically the IOS DELAY START pulse causes the following action in IOC. It first is routed directly to the STOP CLOCK input to CPC. Simultaneously it ensures that the IO interlock (413) is cleared. It presets all digits of the IO control counter (411) and the 15 FF01's of the IO delay counter (404) to ONE's and it ensures that the end-carry control flip-flop, FF03, of the IO delay counter is on ZERO. This pulse is also mixed onto the IO Delay Counter START line out of reset control (412) to cause the start control flip-flop FF02, of the IO delay counter, to be set to ONE. Gate tube GT04 on FF02 is now on so pulses occurring at a one-megacycle rate are fed into the delay counter. The first of these ADD pulses cannot occur until one microsecond after the IOS DELAY START pulse. The latter pulse, delayed 0.25 microsecond, is therefore used to reset the delay counter (by clearing appropriate digits to ZERO), so that the time required to once more reach full count (all ONE's) is approximately equal to the desired delay.

The "approximation" involved in measuring delays is pointed out in the following description of how the computer clock is restarted. Since the end-carry from the 15-stage counter is delayed more than 0.5 microsecond in passing through the series of carry gate tubes, it is desirable to exchange this for a pulse that is undelayed with respect to computer clock pulses to minimize timing problems in other sections of IOC. In addition to being undelayed, the pulses that go to CPC must coincide with a low-frequency supply-pulse (LFSP) since they cannot occur during the restoration periods of the CPC flip-flops. For the above reasons the counter end-carry is used to set FF03 to a ONE and to clear FF02 to prevent further counting. The next occurring LFSP then passes GT04 on FF03 and effectively becomes the end-carry pulse from the counter. The LFSP's consist of groups of 11 one-megacycle clock pulses with a 5-microsecond spacing between groups so the effective counter end-carry will randomly occur from one to six microseconds after the last ADD pulse

to the computer. This end-carry clears FF03 so only one LFSP will pass GT04, and it again presets the counter flip-flops (FF01's). This presetting feature is required for other functions of the IO delay counter as will become evident later.

Inasmuch as all flip-flops of the IO control counter (411) were preset to ONE's by the IOS DELAY START pulse, the end-carry from the IO delay counter (404) passes through the four gate tubes GT01 and emerges as a COMPLETION pulse. This COMPLETION pulse presets the IO control counter to ONE's in preparation for subsequent steps of the order; it passes through on gate tube GT03 in the IO interlock to restart the computer clock, and it sets the alarm control (414) to a ONE. The COMPLETION pulse, which is a synchronized one, is also made available to the individual unit controls. On the IOC block diagram this is labelled SYNC COMPLETION and it is utilized only in special cases which will be pointed out where pertinent in the separate reports on individual units.

On TP8 the contents of the IOS flip-flops are read to the CR so a standard transfer check can be made on TP1. Note that checking the transfer from storage to IOS involves only the flip-flops of IOS, not the switching matrix also. To include the latter in the checking loop would require considerable additional equipment, and since the matrix circuits of WWI have proved very reliable, such checking was omitted in the interest of simplicity.

Also on TP8 the vertical deflection decoder for the display scopes is cleared. This is a preparatory action which in some cases is superfluous (but harmless) at this time. This pulse is also routed through gate tubes on the IOS to clear the storage address registers (SAR) and group selection registers (GSR) in the magnetic drum systems. The drum SAR's and GSR's are therefore cleared only for those settings of IOS which turn these gate tubes on. This will be discussed further in the reports on magnetic drums.

On TP1 the contents of AC are transferred via the main bus to the vertical deflection decoder (left 11 digits) and, if ordered by the IOS setting (certain modes of the auxiliary drum or the buffer drum selected), these contents are also read to one of the magnetic-drum SAR's and/or GSR's. The transfer from AC to the vertical decoder takes place on every $\overline{si}$ instruction and therefore is meaningless unless a scope is selected. For certain units (e.g. the output coder) the content of AC is also transferred to IOR.

The final step of operation timing on the $\overline{si}$ instruction is accomplished by the EU start and the IOC RESET ($\overline{si}$) pulses which also occurs on TP1. The IOC RESET ($\overline{si}$) pulse is applied to gate tubes in reset control (412) and all actions resulting from it depend on the setting of IOS. Detailed discussions of the various actions, therefore, will not be given here. In general they consist of resetting the IO delay counter and the IO control counter as required for the succeeding in-out process. It will be recalled that both these counters were left with all digits holding ONE's a necessary condition for proper reset action.

In addition the IOC RESET (si) may affect the IO interlock and the alarm control flip-flops and start the IO delay counter. The EU start pulse is used to start those readers whose control circuits required a pulse for this purpose.

3.2 Action on the rc Instruction

If an si instruction which selects an output unit has been programmed, another si instruction should not in general be programmed without an intervening rc or bo instruction. Although in certain cases this can be done, it must always be done with care and with a complete understanding of the effect on the unit being selected. The operation timing on the rc instruction will be essentially the same for all units except display. If a display is selected, the address of the rc instruction will specify the register in internal storage whose content is to be transferred to the IOR. The content of IOR is then used in vector and character displays. This will be discussed in more detail in the memorandum describing the operation of the display system. The address of the rc instruction has no significance for other output units and the information to be recorded is obtained from AC.

On the first pulse of operation timing, TP6, the IO interlock (413) is sensed to determine whether the clock should be stopped for the completion of a previous in-out instruction (see Table II). This pulse is not gated by IOS and therefore occurs on every rc instruction. It is fed to gate tube GT02 on the IO interlock so if the interlock is set, it will pass through to the STOP CLOCK input of CPC and will clear the interlock to signify that the clock must be restarted by the next completion pulse from IO control counter. The latter action has been described in the preceding section. In-out instructions which may precede an rc instruction are an si instruction, a bo instruction, or another rc instruction. The rc instruction is not always held up by an si instruction but it must always wait for the completion of a previous recording operation. Proper operating in this respect is ensured by appropriately setting the IO interlock on the IOC reset pulses.

Also on TP6 of the rc instruction, the content of the selected register in core memory (CM) is read to PAR in preparation for the storage transfer required if the display system has been selected.

IOR is cleared on TP7.5 of the rc instruction in preparation of transferring the content of storage (if scopes are selected) or AC (if scopes are not selected) to IOR.

On TP8 of the rc instruction, the horizontal deflection decoder for scopes is cleared. This is in preparation for transferring the contents of AC to the decoder.

If the display system is selected, the content of storage is read to IOR to be used by the vector and character generators on TP8 of the rc instruction. After a half-microsecond delay PAR is cleared in preparation for a parity count on the content of IOR.

On TP1 of the rc instruction the content of AC is transferred to the horizontal decoder and, if the display system is not selected, the content of AC is transferred to IOR. Only the left 11 digits are transferred to the horizontal decoders. The content of AC is also read to PAR and a parity count made. After the completion of the parity count, the content of PAR parity digit (PARA) is transferred to the IOR parity digit (IORA) to be recorded if the output unit uses a parity check (e.g. the auxiliary storage drums). Block control is sensed with a sense BC #3 pulse on TP2 of the rc instruction to determine whether the previous recording operation had been successful. If block control is clear, the operation is successful and TP3 of the rc instruction may be performed. However, if block control is set, the preceding recording operation was not successful. In this case the BC sense #3 pulse will pass through gate tube GT02, clear TPD, reset CS to the ck instruction, and add one to PC. This will terminate the rc instruction without performing the record operation and skip the next instruction in the computer program. This operation is only significant for units capable of giving an unsuccessful recording indication.

The remaining action produced on the rc instruction by operation timing are the IOC Reset and Initiate Record pulses which occur on TP3. The IOC Reset pulse serves a similar but not identical function to that of the IOC Reset on the si order (see Section 3.1). It may reset the IO delay counter and the IO control counter for various counts depending on which gate tubes in reset control (412) have been turned on by IOS, but in all cases it will clear the IO alarm control and set the IO interlock. The Initiate Record pulse will transfer the content of IOR to output units which do not require any intervening action in IOC.

3.3 Cycling Feature of the IO Control Counter

A discussion of one general feature of the IO control counter is pertinent at this point. It was stated in Section 2.423 (d) that the purpose of this counter is to permit certain terminal devices to go through more than one cycle of operation in response to a single rc or rd instruction. These cycles may be necessary to count delays or may be used simply to perform more than one transfer per rc or rd instruction. An example of the latter is the automatic assembly of a 16-digit computer word from eight 2-digit magnetic-tape words when reading from that unit. If such cycles involve delays measured by the IO delay counter, the latter must be reset at the beginning of the cycle. In order to provide this cycling feature two other pulses in addition to the IO control counter end-carry are available; Even Cycle pulses and Odd Cycle pulses. An Even Cycle pulse is generated by a pulse adding to the counter if the least significant digit of the counter is set to zero. An Odd Cycle pulse is generated if the least significant digit is set to one and any other digit of the counter is set to zero. A mixing of these two pulses is called a Cycle pulse. These pulses may be used to initiate action in the terminal equipment and set and start delays in the IO delay counter. They may also be sent to the shift-pulse generator to shift the content of IOR to the left by either two or five shift pulses. This shifting is necessary for automatic assembly modes of operation in magnetic and paper tape units. A shift

of two digits is required for magnetic tape units while a shift of five digits is used in one mode of operation for paper tape readers and the paper tape punch. At present no other units require IOR shifting although other use is made of the cycle pulses.

3.4 Actions on the rd Instruction

An si instruction which selects an input unit must be followed by an rd instruction (exception in block transfer from magnetic drums or other units which may operate in the block transfer mode). Besides the standard program timing, it utilizes TP6 through TP2 for its operation timing (see Table III). On TP6 the IO interlock is sensed to see if any previously programmed in-out operation is still going on. If so, the computer clock is stopped and the interlock flip-flop is cleared as described in Section 3.1. The SENSE pulse on rd is identical with that on the rc instruction; it is never gated by the IOS. Also on TP6, the A-register is cleared in preparation for a later transfer to this register. PAR is cleared a half-microsecond later in preparation for use in a parity count.

On TP7, which can occur only after completion of the reading operation from the reader to IOR, the content of IOR is transferred to AR via the main bus and also to the check register via the check bus. Since the content of IOR is no longer needed, IOR is cleared after a short delay in preparation for a possible succeeding rd instruction. The content of IOR (including IORA, the parity digit) is also transferred to PAR and a parity count performed. A parity alarm can be generated only for input units which carry a parity digit (e.g. the auxiliary storage drum).

On TP8 the contents of the AR are read to CR via the main bus so a transfer check can be performed on TP1. Note that the transfer from IOR to AC through AR is checked only as far as AR. TP1 clears AC in preparation for receiving the contents of AR on the ADD pulse on TP2.

An IOC Reset (rd) pulse is sent to IO reset control on TP2 of the rd instruction. This pulse always sets the IO interlock and clears the IO alarm control. It can also be used to set IO control counter in preparation for other rd orders if more than one cycle is used in reading, or be used to set and start IO delay counter if delays are required.

Also on TP2 of the rd instruction, a BC Sense #3 pulse is sent to block control to determine whether reading had been successful. If not, the next order is skipped in the program in the manner discussed in Section 3.2 for the rc instruction. Again this operation is significant only for units capable of giving an unsuccessful read operation.

3.5 Block Transfer Operation

3.51 Requirements in Design of Block Transfer Instructions

The block transfer instructions, bi and bo, are special instructions which are required for high-speed block transfers between

computer storage and magnetic drums. They should not necessarily be associated with so-called block-by-block (continuous cycle) units such as the magnetic tape devices. In fact, a block instruction cannot be used for magnetic tape recording while one can be used with the Flexowriter paper tape reader (a single cycle unit). Basically these instructions permit more than one 16-digit word to be transferred in response to a single programmed instruction. They are cyclic in nature so they permit the fastest possible rate of transfer; the upper limit on this rate is set by the time required for one time-pulse cycle including the necessary references to storage (approximately 30 microseconds). In the case of magnetic drums, which can handle information even faster than this, the block instructions permit efficient utilization of computer time. For slower units, on the other hand, where other computer instructions could be performed during the intervals between successive reading or recording operations, the advantage of the block transfer instructions is only a reduction in the number of instructions needed in the program. The distinction as to which units can use either the single-word-transfer instructions, rc or rd, or the block instructions is mentioned briefly in Section 3.52 and will be clarified further in the separate reports on the individual units, but it may be generally stated that any unit which does not use the IO Delay Counter to count delays during its actual reading or recording cycle can use the block instructions.

Essential ingredients of a cyclic block transfer instruction are (1) provision for indexing from one computer storage register to the next, (2) provision for transferring between IOR and storage, (3) provision for counting the desired number of words in the block, and (4) provision for initiating an input or output operation and for interlocking to ensure that a new operation is not started until a previous one has been completed. In addition to these requirements, the first cycle of the instruction must select the proper starting storage address and must cause the proper setting of the block-length counter, while the last cycle of the instruction must return the computer to its normal mode of operation starting with the next instruction in the program and on the proper time pulse of that instruction.

A further requirement on the block transfer instructions has been imposed by the buffer drum. This unit differs from other terminal devices in that it is impossible for a programmer to know in advance how much data can be transferred. It cannot be guaranteed that a block transfer of a given number of words will be completed, (i.e., there may be an insufficient number of filled drum registers when reading or an insufficient number of empty registers when recording). Provision must therefore be made for terminating the instruction when it is established that the requested number of words cannot be handled and for registering this fact to the program.

The manner in which the above requirements are met is described in detail in the following step-by-step examinations of the bi or bo instructions.

3.52 Actions Common to the bi and bo Instructions

The bi and bo instructions do not utilize standard program timing pulses so that a description of all actions that take place within the computer during these instructions will be presented. Tables IV and V list the pulses for these instructions. Certain operations are common to both instructions and are described in this section. The common operations include setting IO delay counter to count the number of cycles in the block transfer, setting the starting point in storage for transfers, and indexing storage selection on successive cycles. It should be pointed out early that timing pulses 6,7, and 8 are performed only once since on TP5 of the block transfer instructions, the time pulse distributor is cleared and after the first cycle the instruction will proceed through timing pulses 1-5 only.

On TP6 of the bo and bi instructions IO interlock is sensed to determine whether the clock should be stopped for the completion of a previous in-out operation. This action is discussed in Section 3.1 for the si instruction. As with the rc and rd instructions, this pulse is not gated by IOS. The bi instruction must wait for the first word to be read into IOR while the bo must wait for completion of a previous recording operation.

At the same time the interlock is sensed on TP6, the bi and bo instructions complete the check on the transfer of data to the control switch and storage switch, which was started on the previous TP5, by performing a Storage Switch Read Out, Control Matrix to bus 2 (for bo) or to bus 3 (for bi) and a check Register Read In. The transfer check is completed on TP7.

Also, on TP6, two preparatory actions are accomplished: AR is cleared so data may be transferred to it on TP8 and an AC sign check command given. The AC Sign Check allows the number place in AC, which defines the block length, to be negative since this pulse leaves AC holding the positive magnitude of the number.

On TP7, the contents of AC are read via the bus to the IO delay counter which is used during block instructions to count the number of words in the block. Obviously this counter cannot be used for measuring delays during the execution of a block instruction. It is for this reason that some terminal devices (those which require delays to be counted) cannot utilize the block instructions. Prior to the transfer from AC, the IO delay counter will have been holding all ONE's. The read-in is to the zero sides of the flip-flops, so following the read-in it will contain the complement of the words to be counted, the necessary condition for producing an end-carry after the desired number of counts. Only digits 4-15 of AC are transferred to IO delay counter making a maximum transfer of 4095 words possible. Also on TP7 a Check Magnitude command is given to restore the sign control to its proper state following the sign check, and an add to PC command is given so that the next instruction performed will come from the next storage register.

On TP8 of the bi and bo instructions the contents of the storage switch are read to AR, and AC is cleared. At this time the storage switch is holding a number corresponding to the address section of the bi or bo instruction which specifies the computer storage register into which the first word of the block will be transferred. After a short delay the content of AR is transferred to AC. AC is used for indexing the selection in storage during the block transfers. An add pulse is also sent to the IO delay counter on TP8. Since n+1 pulses are required to produce a carry if IO delay counter is set to the complement of n, this first pulse is needed to correct the count.

On TP's 1,2,3, and 4 the transfers to and from the external unit are performed. These operations are discussed separately in Section 3.53 for the bi instruction and in Section 3.54 for the bo instruction. Whether the block transfer has been completed is also determined during this interval.

To index the storage address in AC an End-Around Carry is performed on TP4 of the bi and bo instructions. This adds one to the contents of AC. The storage switch is cleared on TP4 and the address of the next storage register used in the block transfer is read from AC to the storage switch on TP5. No attempt is made to check this transfer. The time pulse distributor is also cleared on TP5 so that TP's 6,7, and 8 will only be included on the first cycle of the bi and bo instructions.

3.53 Actions on the bi Instruction

The procedure for setting the IO delay counter to count the words in the transfer and the procedure for setting AC for indexing storage on TP's 6,7, and 8 of the bi instruction have been discussed in Section 3.52. The procedure for transferring information to storage from IOR and initiating successive reads or exiting from the instruction are discussed in this section.

On TP1 of the bi instruction storage is cleared preparing it to receive information from IOR.

On TP2 the content of IOR is read into TS and PAR. The parity digit of IOR (IORA) is also transferred to the parity digit of PAR (PARA) and a parity count performed. A parity alarm can be generated only for input units which carry a parity digit (e.g. the auxiliary storage drum). The content of IOR is also read to CR via the check bus on TP2 in preparation for a transfer check.

Also on TP2 block control will be sensed by a Sense BC #4 pulse. If block control is clear, no action will result. However, if block control is set, the instruction will be terminated as discussed in Section 3.55. Block control will not be set at this time unless an unsuccessful read was attempted or if the ADD to IODC pulse on TP8 of the first cycle produced an end carry. This carry will only occur if a zero length block transfer is requested. One will also be added to the IO delay counter on TP2 of the bi instruction, indicating that a word has been read.

The information in PAR is transferred to CR via the bus on TP3 and a transfer check is made on TP4.

On TP4 of the bi instruction the content of PAR is read into core memory if a core memory register is selected by the storage switch. IOR is also cleared at this time in preparation for reading in another word.

Block control is also sensed on TP4 of the bi instruction with a Sense BC #1 pulse. If block control is set, indicating the end of the transfer, the order is terminated as discussed in Section 3.55. If block control is clear, a read initiation pulse is sent to the reader selected (if such a pulse is required) and an IOC reset (rd) pulse is sent to IO reset control to initiate any further action required in the reading process. Block control will only be set at this time if an end-carry is received from the IO delay counter after adding one to it on TP2. This end-carry indicates that all of the words requested have been read into the computer.

The IO interlock is sensed on TP5 so that no further action will take place until an Async. Initiation pulse is received indicating that the next word has been read into IOR. As discussed in Section 3.52, the next storage address is read from AC into the storage switch on TP5 and and TPD is cleared so the next timing pulse will be TP1.

3.54 Action on the bo Instruction

The procedure for setting the IO delay counter to count the words in the transfer and the procedure for setting AC for indexing storage on TP's 6,7, and 8 of the bo instruction are discussed in Section 3.52. The procedure for transferring information from storage to IOR and initiating successive records or exiting from the instruction are discussed in this section.

On TP1 of the bo instruction the content of core memory is read into PAR if a core memory register is selected by the storage switch. IOR is also cleared in preparation for reading information into it on TP2 of the bo instruction.

On TP2 of the bo instruction the content of storage is read into PAR and IOR. After a slight delay it is also read into CR via the check bus. A parity count is also made at this time and the count is read into IOR parity digit (IORA).

Also on TP2 of the bo instruction, block control is sensed with a Sense BC #2 pulse. If block control is set, the instruction is terminated as discussed in Section 3.55. If block control is clear, a record initiation pulse is sent to the recorder selected and IOC reset (rc) pulse is sent to IO reset control to initiate any further action required in the recording process. Block control will only be set at this time if an end-carry is received from the IO delay counter after adding one to it on TP8 or on TP3. If an end-carry is received on TP8, a zero block transfer

had been requested. IO interlock is also sensed so that TP3 of the bo instruction will not occur until an Async. Initiation pulse is received by IOC. This pulse will indicate that the recording has been completed or that recording has been attempted but was not successful. In the latter case block control will also be set.

On TP3 block control is sensed with a Sense BC#4 pulse. If block control is set, the instruction is terminated as discussed in Section 3.55. If block control is clear, no action occurs. Block control can only be set at this time by an unsuccessful pulse from an external unit.

Also on TP3 of the bo instruction, one is added to the IO delay counter and the content of IOR is transferred to CR via the main bus so that a transfer check may be completed on TP4.

The next storage address for recording is selected on TP's 4 and 5 and has been discussed in Section 3.52. The time pulse distributor is also cleared on TP5 so that the next time pulse in the cycle will be TP1.

3.55 Exist from Block Transfer Instructions

To terminate the block transfer instructions, the computer control must be changed so that it will automatically proceed with the remaining instructions of the program. To carry out this function, the computer is made to go through its standard program-timing sequence starting with TP1. All of the sense pulses which find Block Control set, therefore, do the following:

(a) Reset the Control Switch to the ck order which does nothing but CR clear and program timing from TP1-5.

(b) Clear the Time Pulse Distributor so that the program timing will start at its beginning (TP1).

Block control is normally cleared and is set only when the block transfer is completed. It may be set by an end-carry from IO delay counter or from an external unit if a reading or recording process is reported unsuccessful. The end-carry from the IO delay counter is gated by gate tube GT06. This gate tube is on only if FF02 of the IO delay counter is cleared. Therefore, block control will not be set by an IO delay counter end-carry when the counter is used to count a delay (i.e. if the carry is initiated by a delay start pulse).

After every block instruction, AR will contain the address of the computer storage register at which the block began (the address section of the block instruction), and AC will contain the address of the computer storage register which would have been used next. That is: If a zero length transfer was requested, AC contains the address of the block instruction; if the transfer of "n" words was requested and all "n" were handled, AC contains the address of the block instruction plus "n", and if only "m" words were transferred because only "m" words were available

from the buffer drum or only "m" spaces were available for recording, AC contains the block transfer address plus "m".

The use of the zero length transfer with the bo instruction causes no confusion because no action is initiated by the si instruction which precedes it and a check is performed to see that the recording is desired before it is initiated. The use of the zero length transfer with the bi instruction always results in some change in the state of the reader because the reading of the first word was initiated by the preceding si instruction. This is a consequence of the decision to keep the number of si instructions as low as possible by allowing the use of the same si for both single and block reading or single and block recording.

Thus, the reader will always be indexed one word although the word is discarded by the zero length transfer unless a flip-flop register in test storage is selected. In the latter case the word will be read into the flip-flop register. If no information were available (as might be the case with the buffer drum), all zeros would have been read in. Since IOR is not cleared on zero-block-length reading, another reading operation cannot be given without an intervening si-instruction. It should be clear that use of zero-block-length reading must be done with extreme care and should be considered an illegal operation.

Signed G.A. Young
G.A. Young

Approved E.S. Rich
E.S. Rich

ESR/GAY/mrs
Attached Tables I-V
Attached Drawings: C-37314 D-37326
E-37320 D-50820

cc: N.L. Daggett, S.H. Dodd, R.R. Everett, E.P. Farnsworth, S.B. Ginsburg, R.H. Gould, F.E. Heart, F.E. Irish, D.R. Israel, H.J. Kirshner, R.P. Mayer, K.E. McVicar, B.E. Morriss, J.H. Newitt, L.H. Norcott, J.A. O'Brien, A.V. Shortell, N.H. Taylor, R.L. Walquist, C.W. Watt, A.M. Werlin, C.R. Wieser, C.W. Adams, J.W. Forgie, C.A. Zraket, L.L. Holmes, A. Curtiss, S. Desjardins, D.A. Morrisson, N.N. Alperin, D.J. Neville, R.B. Paddock, T. Sandy

TABLE I

OPERATION TIMING FOR si - SELECT IN-OUT OPERATION

TP6	Sense interlock (if requested by IOS)
TP7	Clear IOS PAR to CB (rt 11) Stop all external units IOS Delay Start
TP7.5	PAR Read Out IOS Read In IOR clear
TP8	IOS Read Out CR Read In Vertical Decoder Clear (Magnetic drum SAR and/or GSR clear if requested by IOS)
TP1	Transfer Check AC Read Out Vertical Decoder Read In SAR and/or GSR Read In (if ordered by IOS) IOR Read In (if ordered by IOS) IOC Reset (si) EU Start

This order also has standard program timing.

TABLE II

OPERATION TIMING FOR rc - RECORD

TP6	Sense interlock CM Read (& PAR Clear)
TP7.5	IOR Clear
TP8	Horizontal Decoder Clear Storage Read Out } (if scopes selected) IOR Read In }
TP8.5	PAR Clear
PT1	AC Read Out Horizontal Decoder Read In PAR Read In IOR Read In (if scopes are not selected) Parity count, De 1.7μs PARA to IORA
TP2	Sense BC#3
TP3	IOC Reset (rc) Initiate Record

This order also has standard program timing.

TABLE III

OPERATION TIMING FOR rd - READ

TP6	Sense Interlock Clear AR
TP6.5	Clear PAR IOR Read to CB IOR Read Out AR Read In PAR Read In IORA to PARA Parity Count Parity Check (if requested by IOS)
TP7.5	Clear IOR
TP8	AR Read Out CR Read In
TP1	Transfer Check AC Clear
TP2	Add (AR to AC) IOC Reset (rd) Sense BC#3

This order also has standard program timing.

TABLE IV

COMPLETE TIMING FOR bi - BLOCK IN

(This order does not have standard program timing.)

TP6
- Sense Interlock
- AC Sign Check
- Clear AR
- Storage Switch Read Out
- Control Matrix Read to Bus 3
- Check Register Read In

TP7
- Transfer Check
- Add to Program Counter
- Check Magnitude
- AC Read Out
- IODC Read IN (to zero side)

TP8
- Storage Switch Read Out
- AR Read In
- AC Clear
- Add to IODC

TP8.5
- Add (AR to AC)

TP1
- Storage Clear

TP2
- IOR Read Out
- Storage Read In
- IOR Read to CB
- IORA to PARA
- Parity Count
- Parity Check (if requested by IOS)
- Add to IODC
- Sense BC#4 will be set only if done by Block mem. or with length block...

TP3
- PAR Read Out
- CR Read In

TP4
- Transfer Check
- Clear IOR
- Sense BC#1 end of block or inactivity set.
- End Around Carry
- CM Write (TSS Clear 1/2 μs later MAR when ready)

TP5
- AC Read Out
- Storage Switch Read In (Selects TS or CM & Leaves other switch clear)
- Sense interlock
- Clear Time Pulse Distributor

TABLE V

COMPLETE TIMING FOR bo - BLOCK OUT

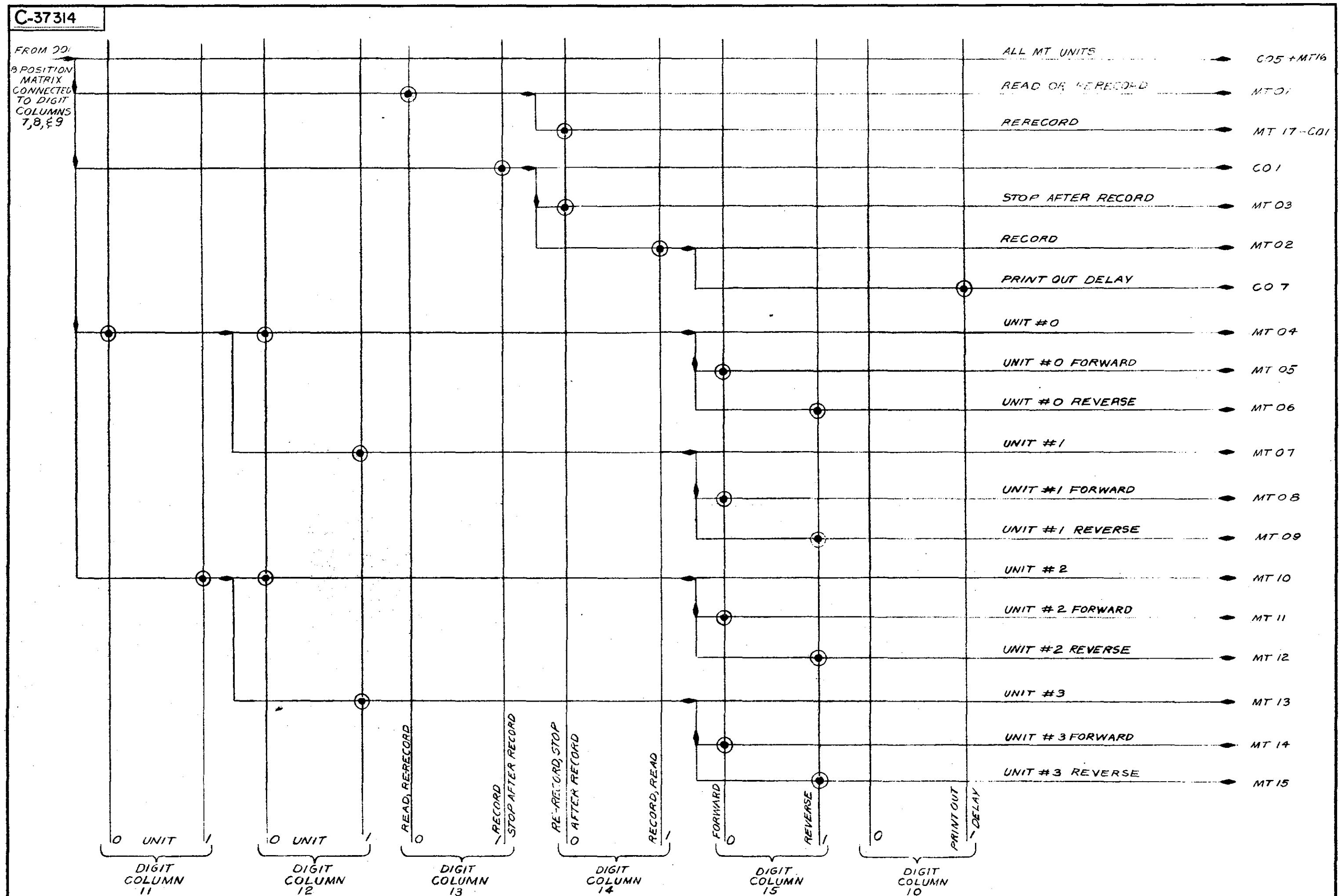
(This order does not have standard program timing.)

TP6	Sense interlock AC Sign Check Clear AR Storage Switch Read Out Control Matrix Read to Bus 2 Check Register Read In
TP7	Transfer Check Add to Program Counter Check Magnitude AC Read Out IODC Read In (to zero side)
TP8	Storage Switch Read Out AR Read In AC Clear Add to IODC
TP8.5	Add (AR to AC)
TP1	CM Read (& PAR Clear)
TP1.5	IOR Clear
TP2	Storage Read to CB Storage Read Out PAR Read In IOR Read In Parity Count, De 1.7μs PARA to IORA Sense Interlock Sense BC #2
TP3	IOR Read Out CR Read In Sense BC#4 Add to IODC
TP4	MAR Clear (TSS 1/2 μs later) Transfer Check End Around Carry
TP5	AC Read Out Storage Switch Read In (Selects TS or CM & Leaves other switch cleared) Clear Time Pulse Distributor

APPENDIX A

List of Note on In-Out Units

Unit	Note
1. WWI Auxiliary Drum	The WWI Auxiliary Magnetic Drum System, E-520, by J.W. Forgie.
2. Indicator Lights and Intervention Registers	Operation of Indicator Lights and Intervention Registers, M-1985, by B.E. Morriss, G. Young.
3. Magnetic Tape	Use of Magnetic Tape and Delayed Output Equipment, M-2269-1, by H. Denman.
4. Display System	Increased Facilities for Visual Display in the WWI Input-Output System, M-2728, by G. Young.
5. Paper Tape Units	Paper Tape Units and Printers in the WWI Input-Output System, M-2729, by G. Young.
6. Special Purpose Units	
a. MITE Buffer Storage	M-1963
b. Output Coder	M-2273



NOTE: MATRIX CONNECTIONS ⊕ ALLOW ANY "OFF" INPUT LINE TO TURN OFF ALL CONNECTED OUTPUT LINES. "OFF" SIGNALS PASS ALONG HORIZONTAL LINES FROM LEFT TO RIGHT ONLY.

GRADED BY: DATE: THIS IS A GRADED DRAWING HIGHEST GRADE APPROVED
GRADE I FOR REFERENCE
GRADE II PRELIMINARY DESIGN
SHD 9/8/53 GRADE III FINAL DESIGN

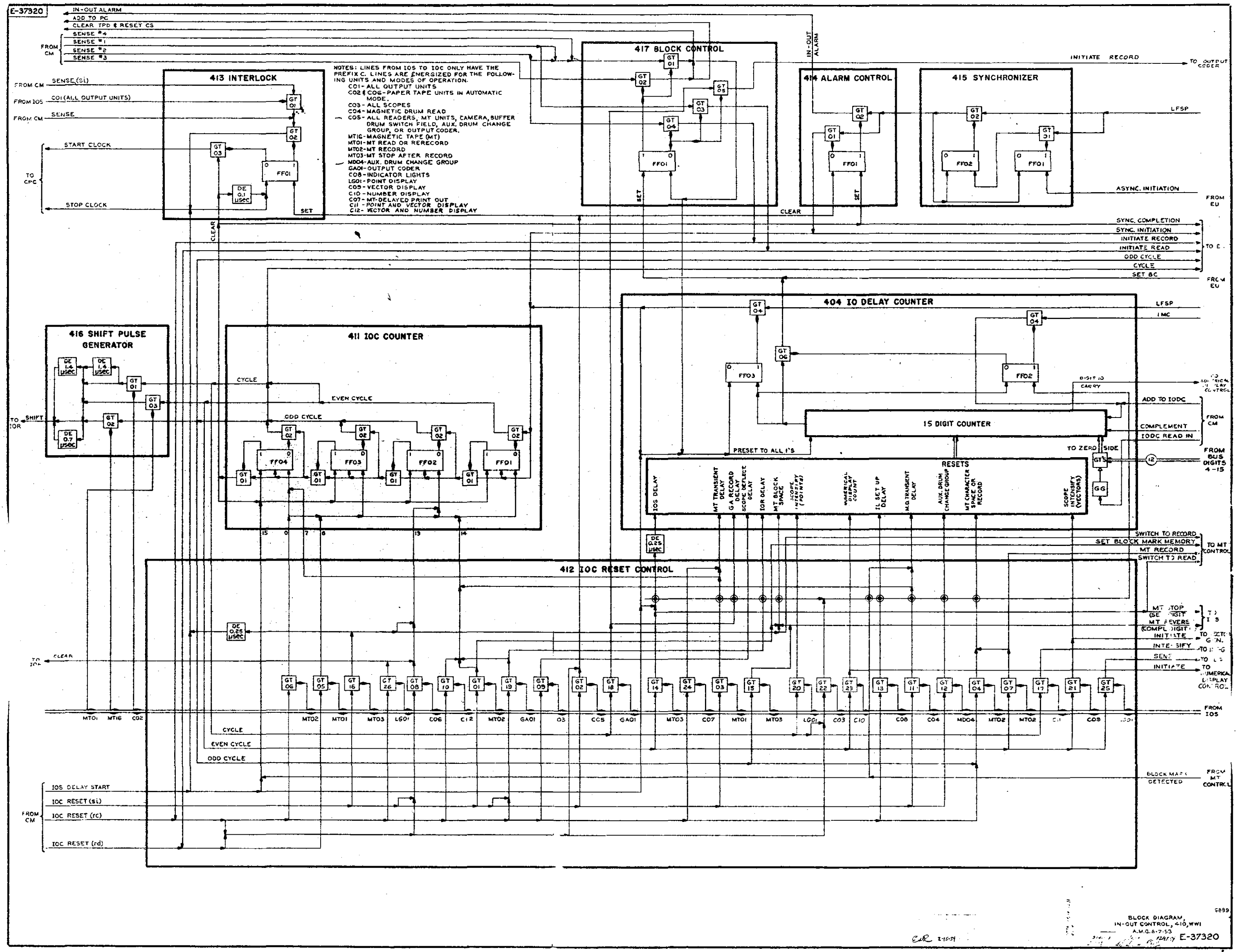
CHG.	CH#	DATE	APPD.
1	5529	7/30/53	

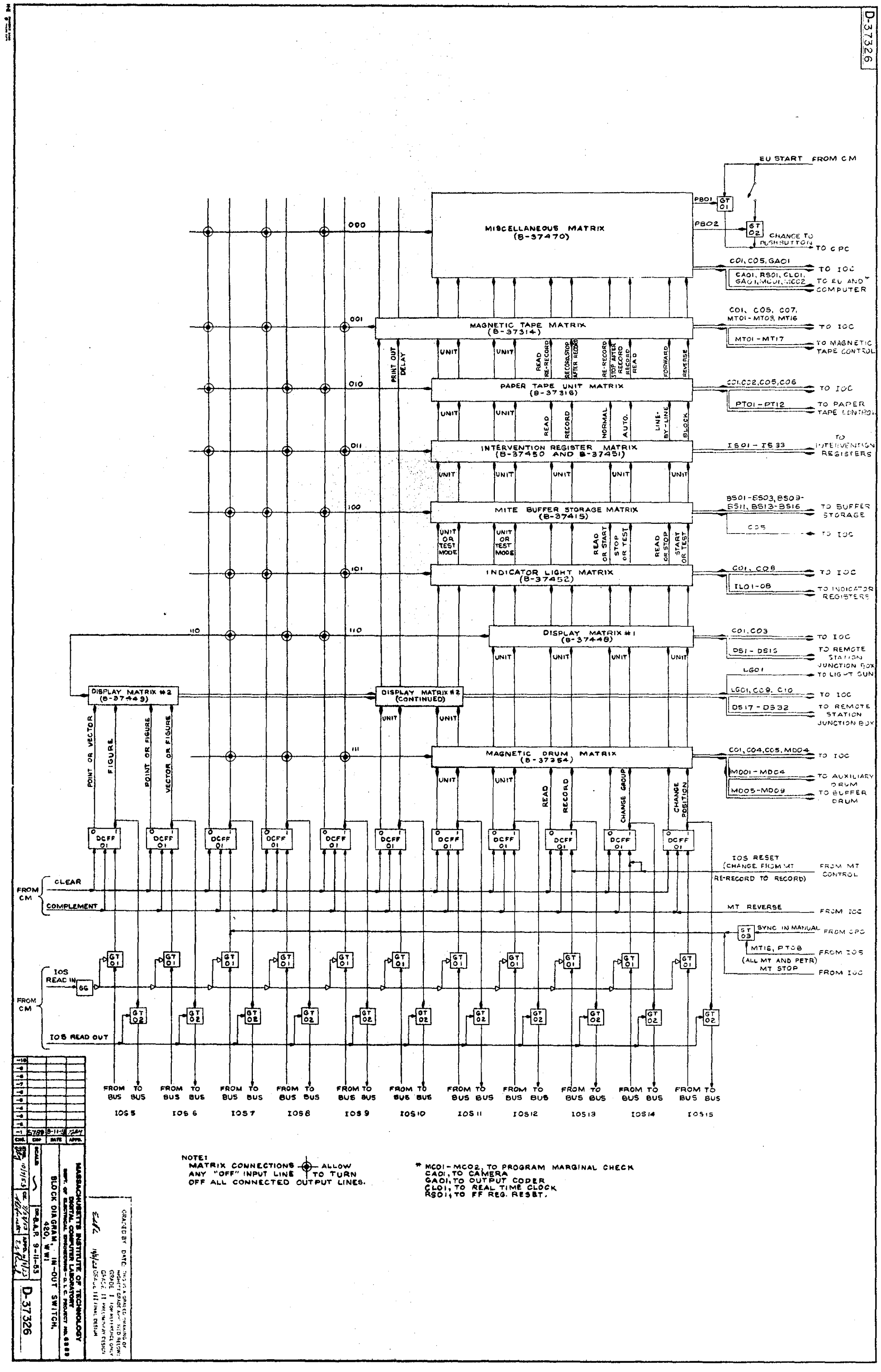
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIGITAL COMPUTER LABORATORY
DEPT. OF ELECTRICAL ENGINEERING — D. I. C. PROJECT NO. 6889

BLOCK DIAGRAM, IOS
MAGNETIC TAPE MATRIX 420, WWI

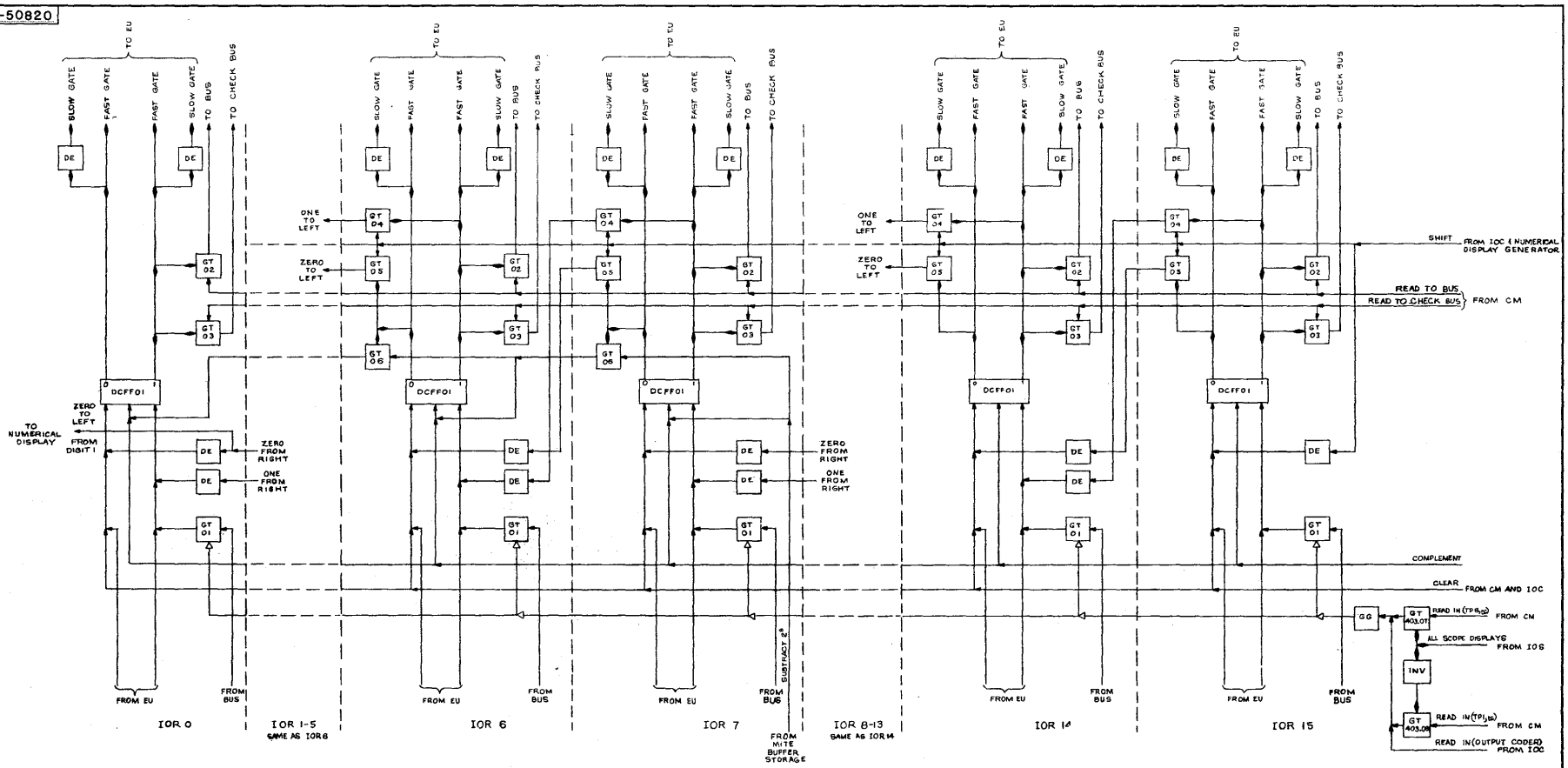
SCALE: ——— DR. E.G.V. 7-31-53
ENG. 8/14/53 CK. 8/ /53 APPD. 8/25/53

C-37314


E-37320
IN-OUT ALARM
ADD TO PC
CLEAR TPD & RESET CS
SENSE #4
SENSE #1
SENSE #2
SENSE #3
FROM CM
413 INTERLOCK
START CLOCK
STOP CLOCK
TO CPC
SET
CLEAR
NOTES: LINES FROM IOS TO IOC ONLY HAVE THE PREFIX C. LINES ARE ENERGIZED FOR THE FOLLOWING UNITS AND MODES OF OPERATION.
C01 - ALL OUTPUT UNITS
C02 & C06 - PAPER TAPE UNITS IN AUTOMATIC MODE.
C03 - ALL SCOPES
C04 - MAGNETIC DRUM READ
C05 - ALL READERS, MT UNITS, CAMERA, BUFFER DRUM SWITCH FIELD, AUX. DRUM CHANGE GROUP, OR OUTPUT CODER.
MT16 - MAGNETIC TAPE (MT)
MT01 - MT READ OR RERECORD
MT02 - MT RECORD
MT03 - MT STOP AFTER RECORD
MD04 - AUX. DRUM CHANGE GROUP
GA01 - OUTPUT CODER
C08 - INDICATOR LIGHTS
LG01 - POINT DISPLAY
C09 - VECTOR DISPLAY
C10 - NUMBER DISPLAY
C07 - MT-DELAYED PRINT OUT
C11 - POINT AND VECTOR DISPLAY
C12 - VECTOR AND NUMBER DISPLAY
417 BLOCK CONTROL
414 ALARM CONTROL
415 SYNCHRONIZER
INITIATE RECORD
TO OUTPUT CODER
LFSP
ASYNC. INITIATION
FROM EU
SYNC. COMPLETION
SYNC. INITIATION
INITIATE RECORD
INITIATE READ
ODD CYCLE
CYCLE
SET BC
416 SHIFT PULSE GENERATOR
SHIFT
411 IOC COUNTER
CYCLE
EVEN CYCLE
ODD CYCLE
404 IO DELAY COUNTER
LFSP
IMC
15 DIGIT COUNTER
ADD TO IODC
COMPLEMENT
IODC READ IN
FROM CM
PRESET TO ALL 1'S
TO ZERO SIDE
RESETS
FROM BUS DIGITS 4-15
IOS DELAY
MT TRANSIENT DELAY
G.A. RECORD DELAY
SCOPE DEFLECT DELAY
IOR DELAY
MT BLOCK SPACE
SCOPE INTENSIFY (POINTS)
NUMERICAL DISPLAY COUNT
IL SET UP DELAY
MD TRANSIENT DELAY
AUX. DRUM CHANGE GROUP
MT CHARACTER SPACE OR RECORD
SCOPE INTENSIFY (VECTORS)
SWITCH TO RECORD
SET BLOCK MARK MEMORY
MT RECORD
SWITCH TO READ
TO MT CONTROL
412 IOC RESET CONTROL
CLEAR
MT STOP
MT REVERS
INITIATE
INTENSIFY
SENSE
INITIATE
FROM IOS
CYCLE
EVEN CYCLE
ODD CYCLE
BLOCK MARK DETECTED
FROM MT CONTROL
IOS DELAY START
IOC RESET (si)
IOC RESET (rc)
IOC RESET (rd)
BLOCK DIAGRAM,
IN-OUT CONTROL, 410, WWI
A.M.G. 6-7-53
E-37320


D-37326
EU START FROM CM
PBO1
PBO2
GT 01
GT 02
CHANGE TO PUSHBUTTON
TO CPC
MISCELLANEOUS MATRIX (B-37470)
CO1, CO5, GAO1
TO IOC
CAO1, RSO1, CLO1, GAO1, MCO1, MCO2
TO EU AND* COMPUTER
000
001
MAGNETIC TAPE MATRIX (B-37314)
CO1, CO5, CO7, MTO1 - MTO3, MT16
MTO1 - MT17
TO MAGNETIC TAPE CONTROL
PRINT OUT DELAY
UNIT
READ
RE-RECORD
RECORD STOP AFTER RECORD
RE-RECORD
STOP AFTER RECORD
RECORD
READ
FORWARD
REVERSE
010
PAPER TAPE UNIT MATRIX (B-37316)
CO1, CO2, CO5, CO6
PTO1 - PT12
TO PAPER TAPE CONTROL
RECORD
NORMAL
AUTO.
LINE-BY-LINE
BLOCK
011
INTERVENTION REGISTER MATRIX (B-37450 AND B-37451)
IS01 - IS33
TO INTERVENTION REGISTERS
100
MITE BUFFER STORAGE MATRIX (B-37415)
BS01 - BS03, BS09 - BS11, BS13 - BS16
TO BUFFER STORAGE
CO5
UNIT OR TEST MODE
READ OR START
STOP OR TEST
READ OR STOP
START OR TEST
101
INDICATOR LIGHT MATRIX (B-37452)
CO1, CO8
ILO1 - 08
TO INDICATOR REGISTERS
110
DISPLAY MATRIX #1 (B-37448)
CO1, CO3
DS1 - DS16
TO REMOTE STATION JUNCTION BOX
LGO1
TO LIGHT GUN
LGO1, CO9, C10
DS17 - DS32
DISPLAY MATRIX #2 (B-37449)
DISPLAY MATRIX #2 (CONTINUED)
POINT OR VECTOR
FIGURE
POINT OR FIGURE
VECTOR OR FIGURE
111
MAGNETIC DRUM MATRIX (B-37354)
CO1, CO4, CO5, MDO4
MDO1 - MDO4
TO AUXILIARY DRUM
MDO5 - MDO9
TO BUFFER DRUM
CHANGE GROUP
CHANGE POSITION
DCFF 01
IOS RESET (CHANGE FROM MT RE-RECORD TO RECORD)
FROM MT CONTROL
FROM CM
CLEAR
COMPLEMENT
MT REVERSE
FROM IOC
GT 03
SYNC IN MANUAL
FROM CPC
MT16, PT08
FROM IOS
(ALL MT AND PETR) MT STOP
IOS READ IN
GG
IOS READ OUT
FROM BUS
TO BUS
IOS 5
IOS 6
IOS 7
IOS 8
IOS 9
IOS 10
IOS 11
IOS 12
IOS 13
IOS 14
IOS 15
NOTE: MATRIX CONNECTIONS ALLOW ANY "OFF" INPUT LINE TO TURN OFF ALL CONNECTED OUTPUT LINES.
* MCO1 - MCO2, TO PROGRAM MARGINAL CHECK
CAO1, TO CAMERA
GAO1, TO OUTPUT CODER
CLO1, TO REAL TIME CLOCK
RSO1, TO FF REG. RESET.
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIGITAL COMPUTER LABORATORY
BLOCK DIAGRAM, IN-OUT SWITCH, 480, WWI
DR. B.A.R. 9-11-53
D-37326

D-50820



GRADED BY: DATE: THIS IS A GRADED DRAWING OF HIGHEST GRADE APPLICABLE BELOW
GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
GRADE III FINAL DESIGN

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BLOCK DIAGRAM
403 DC IN-OUT REGISTER, WWI

SCALE: — DR. B.R 8-8-53 CK. 12-22-53 APPD. 12-22-53

D-50820