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SUBJECT: RESULTS OF THE XI-1 CENTRAL COMPUTER EVALUATION - 18 MARCH 1955

TO: N. H. Taylor

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ABSTRACT: This is the second in a series of evaluations to be performed on the XD-1 Central Computer. Results of the first evaluation are discussed in Memorandum 6M-3443, "Results of the XD-1 Central Computer Evaluation -- 1 March 1955.

For this evaluation, log book data and daily operation reports which covered the period including 7-18 March 1955 were studied to determine the reliability of the central computer and circuit margins. Log book data and operation reports were furnished by IBM. On 18 March 1955, a computer test was performed; details of this test are given in table IV.

Results of the evaluation showed that the percentage of usable assigned time was greater than 91 percent, but the mean good-time between failures was only 3.8 hours for the 7-18 March period and 1.06 hours for the computer test. Twelve core memory parities, eleven resistor failures, and five card read-in failures were responsible for 52 percent of the failures during the two-week period; five card machine failures and two core memory parities constituted the seven failures which occurred during the computer test.

Tube tapping revealed that about 1.5-2 percent of the tubes and 2.5-3 percent of the plug-in units in the central computer are sensitive to vibration.

Most margins are similar to those noted in the first evaluation except for the low margin on the Master Clock Crystal Oscillator which is only -14 volts. Sense amplifier margins for core memories #1 and #2 have been improved, and the margins which differed from other margins on similar circuits have been corrected.

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No important changes or additions have been made in the computer except the addition of the automatic marginal checking equipment.

I. Logical and Physical State of the Computer:

There have been few changes in the logical and physical state of the computer since it was evaluated on March 1 (See 6M-3443).

An attempt was made to remove the dust from the computer, but some of the dust was blown from the outside of the plug-in units to the inside of the units.

Due to the design of the card reader circuits, it is impossible to get the card reader out of an in-out pause except by turning off the power to the card reader.

The automatic marginal checking system has been connected. Also, PER 75--lock address counter -- clear IO interlock -- are now wired in. Chilled water has been added to the air cooling system.

Two new reliability programs, the special punch program and the complement checkerboard program, were run during this reliability test. RCC 03, the manual operations reliability program, could notbe run, so the sections of the computer that were not tested on March 1 were not tested during this test.

II. Reliability:

In order to determine the reliability of the XD-1 Central Computer, a study of log book entries has been made and an evaluation test lasting eight hours was performed.

1. Log Book Data

A summary of data taken from the XD-1 log for the period of 7-18 March 1955 is given in Table I. Reliability calculated from this data for the above period of time is as follows:

Percentage of usable assigned time = 91.5%
Mean good-time between failures = 3.8 hours

2. Evaluation Test -- 18-19 March 1955

Results of an eight-hour evaluation test performed 18-19 March 1955 are shown in Table II. The following reliability figures were obtained for this period:

Percentage of usable assigned time = 98.5%
Mean good-time between failures = 1.06 hours

3. Reliability Analysis

Percentage of usable assigned time for the periods covered by log book data and evaluation tests was found to be greater than 91 percent; a minimum of 75 percent was expected for this test.

The mean good-time between failures was only 3.8 hours according to information taken from the log book. This figure is lower than the 4.72 hour figure obtained for the evaluation test on 1 March 1955.

A list of the failures incurred (see table III) shows that parity errors, resistor failures, and card read-in failures contributed greatly to the low figure of mean good-time between failures. The percentage of failures for each type of failure is as follows: parity errors, 22.2%; resistor failures, 20.4%; card read-in failures, 9.3%. Eight of the eleven resistor failures were due to one-percent resistors in the sense amplifiers which failed during a thirteen-hour period on 16 March 1955.

There has been trouble with these Stemag 1% resistors before. Usually a group of these resistors will suddenly open or increase greatly in resistance. The resistors with the largest amount of resistance are most likely to fail. Extensive voltage, power, humidity, and temperature tests have been made without detecting the cause of these failures. This latest group of resistor failures occurred just after the chilled water was added to the cooling system, so a new series of tests that will feature temperature and humidity cycling is planned.

Results of the evaluation test show that the mean good-time between failures was 1.06 hours for the eight-hour period. This figure showed no improvement over the 1.08 hours found during the previous test on 1 March 1955, and it is still very small. Failures which occurred during the test were:

Memory parities	2
Card punch failure	2
Card reader failures	3

Both memory parities occurred while program RMM 2 04 was running in memory #1. Parity errors were much less frequent during this test than during the 1 March 1955 test when six parity errors occurred during the ten-hour period. The cause of the memory parity errors is not known.

Card punch failures were noted when the "special punch" program was run. When the word which determines the information to be punched on the card (control word in test register B) was 1.77777 - 1.77776, 1.28 percent of the words (15.4 percent of the cards) were punched incorrectly. With 0.70707 - 0.70707 in test register B, less than six tenths of one percent of the words were punched incorrectly. No errors occurred when the control word was changed to 1.25252 - 1.25252. It is believed that these failures are caused by drawing too much corrent through a cam-operated circuit breaker in the punch.

Improper feed during read-in caused two card reader failures; the third failure was a jam in the card reader. The jam resulted when cards were punched with many holes in each card -- this made the cards weak and resulted in the cards being jammed in the reader. When the card feed mechanism is adjusted properly, this trouble should not occur; the special tools needed to adjust the mechanism were not available at that time.

Failures which occurred during the power-off, power-on sequence were not included in the computation of mean good-time between failures or the percentage of usable assigned time.

III. Margins and Margin History

For the period of 7-18 March 1955, margins have been taken on the circuits in the central computer using most of the programs and the same procedures as described in the 1 March 1955, evaluation (See Memorandum 6M-3443).

A review of margin lines which did not meet the arbitrarily chosen ± 20 percent variation of supply voltage on 1 March 1955 is as follows:

Program: RAE 01
Equipment Group: MC-2, Arithmetic

Voltage	Margin	Logic	Circuit	Remarks
-150	A	1-4	AFF	These margins have changed from + 28 and -19 volts to + 27 and -16 volts. They are still below the ± 20 percent criteria and require more improvement.
-300	A	1	C^{FF}	These margins have changed from + 22 and -50 volts to + 25 and -57 volts. These margins are improved but the positive margin is low.
+ 90	B	4-6	B^{GT}	These margins changed from + 21 and -17 volts to + 25 and -20 volts. Margins on even bits for the chain of B^{GT}'s in the L and R adder are also + 25 and -20 volts.
	B	1-3	B^{GT}	

Program: RMM 2 04
(Checking Core Memory #1)
Equipment Group: MC-1 Memory

-150	A	1-3	AFF	These margins are now + 78 and -42 volts for RMM 2 04 which compares favorably with a similar circuit in Memory #2.

-150	C	1	SA	These margins have been increased from + 20 and -20 volts to + 36 and -23 volts.

Program: RMM 2 04
(Checking Core Memory #2)
Equipment Group MC-1 Memory

Voltage	Margin	Logic	Circuit	Remarks
-150	F	1	SA	These margins have been increased from + 28 and -26 volts to + 45 and -30 volts.
-300	D	1	DPD	This margin has been increased to -50 volts, which is comparable to memory #1 margins for a similar circuit.

The following circuits failed to meet the ± 20 percent criteria during the evaluation period:

Program: RCC 02
Equipment Group: MC-3, Program and Control

+ 90	C	1-3	$_{A}$GT	The $_{A}$GT's in the parity circuits had margins of + 25 and -18 volts. These margins are similar to those found on the chain of gates in the L and R adder, so this may be a reasonable figure for this configuration of gates.
+90	F	1	$_{A}$OSC	This line affects the two-megacycle oscillator whose margins are + 25 and -14 volts. The negative margin is low. Installation of a new oscillator is scheduled; this should remedy the low margin.

Margins taken on the In-Out equipment group showed that most circuits had reasonable margins. Low margins were attributed to the weak two-megacycle oscillator.

4. Shock Tests

The shock tests consisted of a power on-off sequence and the tapping of tubes and plug-in units.

As on March 1, the AC and DC voltages would not come up at the computer frames when the power was turned on at the power control frame. No other troubles were noticed during the power on-off sequence.

194 tubes, 115 plug-in units and eight memory driver panels were vibrated. Two tubes, both of them in the memory, and six plug-in units caused failures when they were tapped. One of the six plug-in unit failures were traced to a tube in the unit, and the other units only failed the first time that they were tapped.

The percentage of tapped tubes that failed during this test, 1.03%, is only two-thirds of the percentage, 1.65%, that failed during the test on March 1. Also, 5.21% of the tapped plug-in units failed this time, compared with 2.73% of the tapped units that failed during the March 1 test. These differences are caused by a slight difference in the testing procedures used during the two tests. During the first test, the tubes in the plug-in unit were tapped, then the plug-in unit itself was vibrated. During the second test, the plug-in unit was vibrated first. This was done to see if vibrating the plug-in units would also vibrate the tubes in the unit (this method can't be depended on). Therefore, some of the plug-in unit failures that occurred during the second test are really failures of the tubes in the plug-in unit. However, if it is assumed that 2.73% (the result of the first test) of the plug-in unit failures were caused by something (poor pin connections, loose solder joints, etc.) besides tubes, the results of this test appear close to the results of the first test, and it may be assumed that about 1.5-2% of the tubes and 2.5-3% of the plug-in units in the central computer are sensitive to vibration.

V. Conclusions:

In spite of the decrease in the mean-good-time between computer failures, it is believed that the reliability of the computer has increased since the last reliability test was performed. The apparent decrease is due to improved record keeping. However, the time between failures is still too low. The usable percentage of assigned time is very good.

Since the last test, there have been no important changes in the physical or logical state of the machine except the addition of the automatic marginal checking equipment.

The shock tests indicate that 2.5-3% of the plug-in units and 1.5-2% of the tubes are sensitive to vibration. Also, there is still some trouble in the power control circuits.

A review of the eight margins which failed to meet the arbitrary $\pm$ 20 percent criteria for the first evaluation revealed that the $_{A}$FF's on line -150 volts A 1-4 in MC-2 and the $_{C}$FF's on line -300 volts A 1 in MC-2 do not have sufficient margins. Margins on the sense amplifiers in core memories #1 and #2 have been improved. The negative margin on the master clock crystal oscillator was only -14 volts -- this situation should be remedied when the new oscillator is installed.

TABLE I

XD-1 Log Book Analysis -- 7-18 March 1955

The following data was obtained from XD-1 log entries for the period of 7-18 March 1955. About thirty hours of computer operation are not included because the data was either incomplete or did not fit any of the categories listed below; twelve errors occurred during these thirty hours.

Assigned Time	Type of Program	No. of Failures	Time Lost
36 hrs. 8 min.	Reliability	19	4 hrs. 11 min.
97 hrs. 35 min.	Simulation and Test	17	4 hrs. 44 min.
44 hrs. 37 min.	Marginal Checking	7	2 hrs. 42 min.
178 hrs. 20 min.		43	11 hrs. 37 min.

Percentage of Usable Assigned Time

$$100 \times \frac{178.33 \text{ hrs.} - 15.22 \text{ hrs.}}{178.33 \text{ hrs.}} = 91.5\%$$

Mean Good-Time Between Failures

$$\frac{163.11 \text{ hrs.}}{42 \text{ failures}} = 3.8 \text{ hours}$$

TABLE II
Evaluation Test Results -- 17-18 March 1955

The following data was obtained during the XD-1 Evaluation on 18-March 1955.

Assigned Time	Type of Program	No. of Failures	Time Lost
6 hrs. 23 min.	Reliability	6	6.5 min.
1 hr. 9 min.	Shock Tests	1	.5 min.
7 hrs. 32 min.		7	7 min.

Percentage of Usable Assigned Time

$$100 \times \frac{7.53 \text{ hrs.} - .12 \text{ hrs.}}{7.54 \text{ hrs.}} = 98.5\%$$

Mean Good-Time Between Failures

$$\frac{7.41 \text{ hrs.}}{7 \text{ failures}} = 1.06 \text{ hrs.}$$

TABLE III
XD-1 Failures for 7-18 March 1955

The following failures were noted in the XD-1 log for the period 7-18 March 1955:

No. of Failures	Description of Failures
	Alarms
12	Unexplained parity errors
2	Unexplained error stops
1	Unexplained intermittent errors in cyclic programming facility
5	Unexplained check sum errors and failures during read-in from card reader.
	Plug-In Units
11	Resistors
2	Tubes
2	Checked and no trouble found
2	Information not yet available
	Card Machines
1	Printer and punch not operable
4	Cards jammed in card reader
3	Punch failed to punch correctly
	Miscellaneous
2	Shorted wires
1	Wiring error
2	Circuit breakers tripped (one was accidental)
1	Breaker lead
1	Unsoldered wire
2	Accidental -15 volt short

TABLE IV
Time Schedule for Central Computer Test Run, 18-19 March 1955

FROM TO The following programs were run for the indicated lengths of time.

5:15 pm 7:27 pm

Program	Time
RCC 01	5 min.
RCM 01	Run Once
RMM 2 04	15 min.
Switch memories and repeat RMM 2 04	15 min.
RCM 01	Run Once
RCC 02	15 min.
RCM 01	Run Once
RAE 01	20 min.
Special Punch	5 min.
RMM 1 08	15 min.
RMM 2 07	15 min.
RAE 03	5 min.

7:27 pm 7:50 pm The computer power was removed from the power shutdown test.

7:50 pm 7:03 pm Computer power was restored and the following programs were run:

RCC 01
RMM 2 04
RAE 03
RCC 02
RAE 01
RMM 1 08
RMM 2 07
RCM 01

8:03 pm 10:05 pm The reliability programs which were run from 5:15 to 7:27 pm were repeated.

10:05pm 11:14 pm Approximately ten percent of the plug-in units and two percent of the tubes were tapped.

11:14pm 1:16 am The reliability programs which were run from 5:15 to 7:27 pm were repeated.

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