F. Williams Sarles, Jr.
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ELECTRICAL ENGINEERING DEPARTMENT
MASTER'S THESIS PROPOSAL

TITLE: A Transistorized Amplifier-Discriminator for Core Memory Output Sensing

STATEMENT OF THE PROBLEM

The information output of a coincident-current magnetic-core memory of the type used in Whirlwind I (WWI) and the Memory Test Computer (MTC) is essentially the presence or absence of ±0.1-volt, 1-microsecond pulses at specified times. The problem, in brief, is to develop and construct experimentally a transistor system to convert the memory output into the presence and absence of standard computer pulses. In WWI and MTC, standard pulses are 0.1-microsecond long, varying from +20 volts to +40 volts in amplitude; those in a proposed transistor computer will be about 0.1-microsecond long and between -0.5 volt and -3 volts in amplitude. The techniques to be used in a transistor sensing amplifier will involve difference-signal amplification, conversion of the positive and negative pulses from the memory into unipolarity pulses, conversion of these unipolarity pulses into standard computer pulses, and pulse-mixing techniques to allow the use of multiple sense windings in a memory plane. Preliminary investigations have indicated that presently available transistors are capable of handling the greater part of the necessary circuitry.

HISTORY OF THE PROBLEM

Recent developments in Division 6 of Lincoln Laboratory have led to proposals for the development of a new general-purpose computer. One of the primary objectives in the design of this system is a reduction in size and power requirements through the use of transistors wherever possible. In addition, the potentially higher reliability of transistors over vacuum tubes should ultimately result in an increase in over-all reliability of such a system.

A 256 x 256 coincident-current magnetic-core memory will be incorporated in the computer. As stated previously, the memory information output consists of the presence or absence of ±0.1-volt, 1-microsecond pulses at specified times; these must be converted into the standard pulses used in the computer. Four vacuum-tube sensing amplifiers have been designed in conjunction with 32 x 32 and 64 x 64 memories, but no efforts have been made thus far to use transistor circuitry.

The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19(122)-458.

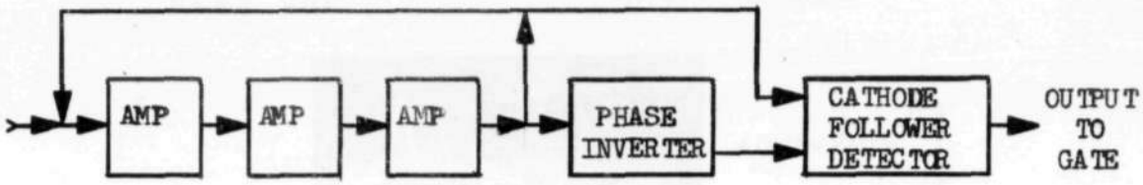
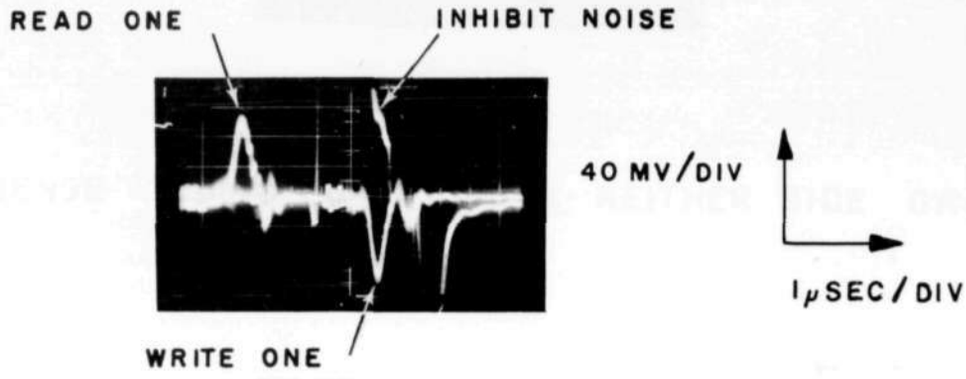


Fig. 1 - Mod. I Sense Amplifier Block Diagram

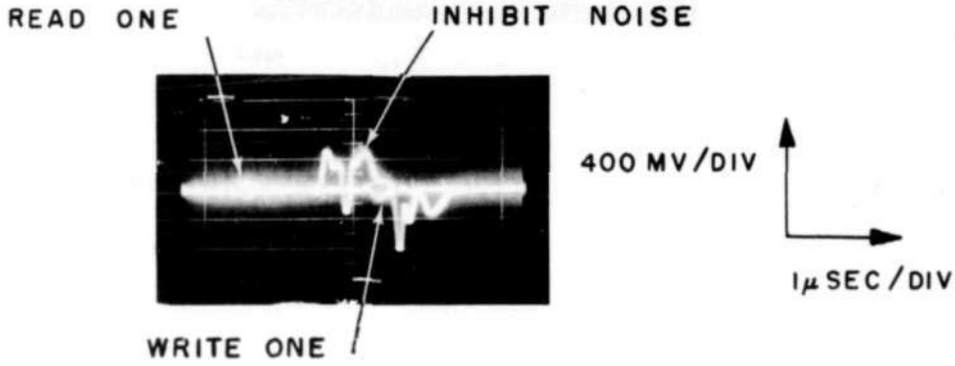
The Mod. I vacuum-tube sensing amplifier (Fig. 1) has a single-ended input into three cascaded pentode amplifiers operating in a feedback loop. The third stage drives one side of a cathode-follower detector and a phase inverter which in turn drives the other side of the detector. The detector output can then set a gating circuit which is strobed, or sampled, at the proper time by a standard 0.1-microsecond pulse.

In experimental setups, this amplifier may have been adequate, and it was used for a while in the WWI memory system. However, it finally proved unsatisfactory because of capacitive noise pickup by the sensing winding. Figure 2a shows the difference voltage across the sense winding with neither side connected to ground. The first pulses are ONEs being read out of a 128 x 128 memory plane; the pulses occurring about 4 microseconds later are ONEs written back into the memory plane. Figures 2b and 2c show the results of grounding either side of the sense winding. The noise has increased considerably, and half of the ONEs have disappeared or at least seem to be greatly reduced in amplitude.

Such a situation obviously requires an amplifier with a balanced input and common-mode rejection; these conditions may be achieved with a transformer or a difference amplifier. Accordingly, the Mod. II sensing amplifier was designed using triode difference amplifiers throughout as indicated in Fig. 3. The output of four cascaded difference amplifiers drives a cathode-follower detector which in turn operates a standard gating circuit.



(a)



(b)

FIG. 4
SENSE-WINDING OUTPUT SHOWING INHIBIT NOISE

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FIG. 2a

SENSE-WINDING OUTPUT WITH NEITHER SIDE GROUNDED

FIG. 2b

SENSE-WINDING OUTPUT WITH ONE SIDE GROUNDED

FIG. 2c

SENSE-WINDING OUTPUT WITH THE OTHER SIDE GROUNDED

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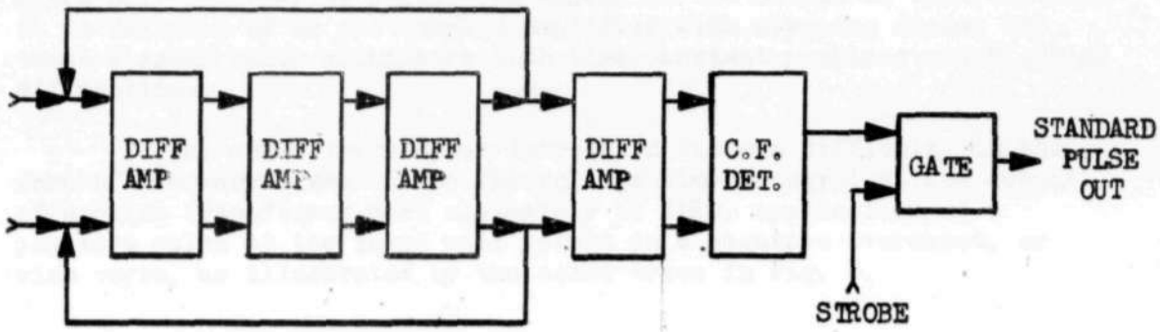

Fig. 3 - Mod. II Sensing-Amplifier Block Diagram

With the Mod. II amplifier, a new problem arose. The use of an inhibit winding for writing information into the memory greatly reduces the number of cathodes required for driving the memory, but operation of this winding disturbs nearly every core in the inhibited memory plane during the rise and the fall of the inhibit pulse. The summations of these disturbances result in pulses which may be as high as 1 volt, as shown in Figures 4a and 4b. By the time these pulses reached the fourth stage of the Mod. II sensing amplifier, they were of sufficient amplitude to cause blocking in this stage.

A second problem was involved in the RC time constants of the interstage coupling circuits. These were originally 70,000 microseconds but were later reduced to 1000 microseconds because of difficulties encountered with extraneous low-frequency transients. In the case of a 64 x 64 memory, C. Laspina indicates that an RC time constant of 200,000 microseconds would be preferable in view of certain pulse sequences which might occur[1].

Efforts to overcome these difficulties resulted in the Mod. III and Mod. IV sense amplifiers. The Mod. III unit was designed by the WWI group for use in the WWI memory. About the same time, the Mod. IV amplifier was designed for use in the MTC. Both units incorporate a transformer input as shown in Fig. 5.

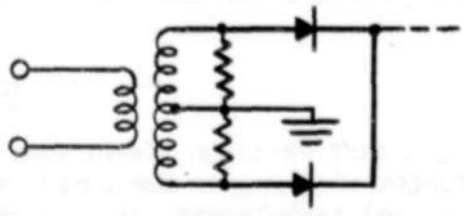

Fig. 5 - Input Circuit of Mod. III and Mod. IV Sensing Amplifiers

1. Laspina, C. A., "Basic Circuits - Sensing Amplifier, Preliminary Specifications, PB#20" M-2274, Digital Computer Laboratory, M.I.T., 3 July 1953.

Since only unipolarity pulses can appear at the output of this curcuit, it is followed by an a-c coupled amplifier with clamping diodes between stages, which eliminates both time-constant problems and blocking difficulties.

The pulse transformer introduced its own difficulty in the form of recovery time. Since the voltage-time integral at the output of a pulse transformer must ultimately be ZERO, application of a positive pulse at the input will result in a negative overshoot, or vice versa, as illustrated by the solid trace in Fig. 6.

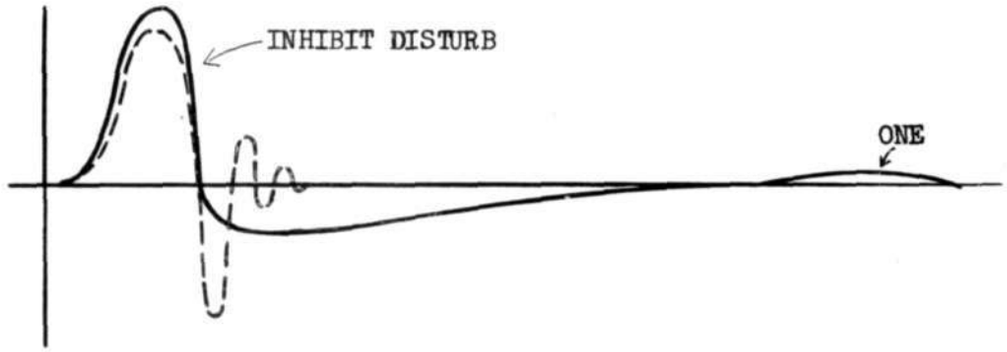

Fig. 6 - Pulse Transformer Overshoot and Recovery

In the memory cycle, information pulses follow the inhibit pulses, but if information occurs while the overshoot from the inhibit pulse is still present, erroneous data may result. Consequently, it is desirable to reduce the recovery time in order to attain a minimum cycle time in the memory. Recent experiments by R. Zopatti at Lincoln Laboratory indicate that the recovery time can be reduced to about 1.5 microseconds by connecting a few turns on the transformer across 1 or 2 ohms of resistance. This results in the dotted trace in Fig. 6 and does not seem to impair the quality of the information pulses.

Vacuum-tube circuitry has not yet yielded a completely satisfactory solution to the sensing problem. It is expected that transistor techniques, although possibly introducing problems of their own, will circumvent some of the inherent difficulties of previous vacuum-tube designs.

PROPOSED PLAN OF ATTACK

Since it is immediately apparent that any system of sensing will require a balanced input and common-mode rejection, the approaches can be divided into two classes, transformer inputs and difference-amplifier inputs.

An important factor to be considered in the design of the sensing amplifier is the total delay time throughout the unit. This delay is usually defined as the time elapsed between the peak amplitude of a ONE at the input and the peak amplitude of the corresponding standard pulse at the output of the unit. WWI and MTC have been designed in such a manner that if a ONE has not arrived at the output of the sensing amplifier by a given time, the computer assumes that the information is a ZERO.

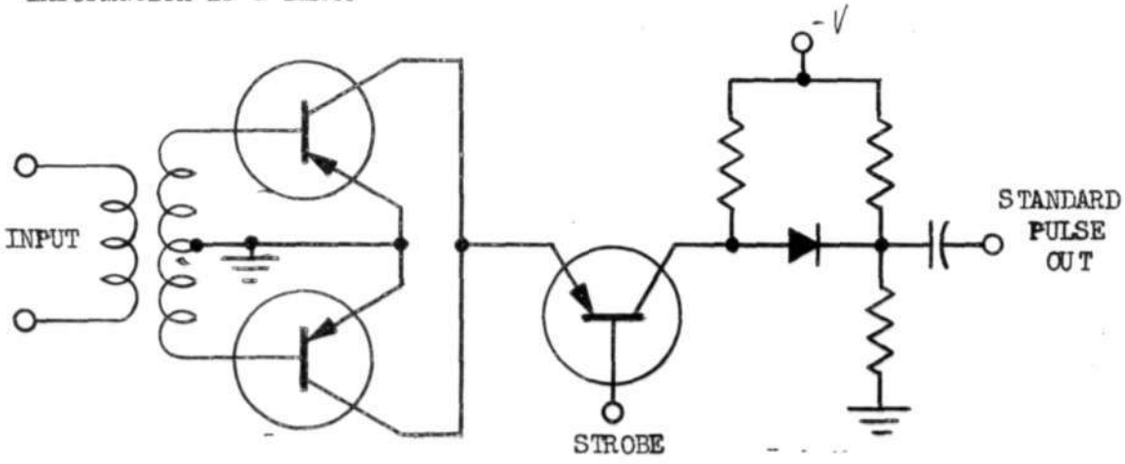

Fig. 7 - Transformer Input Circuit

Figure 7 shows a circuit which could be used with a transformer input. This circuit has the advantage of extreme simplicity but involves the disadvantages of transformer recovery time and delay time through the transformer. Experimental verification of the operational feasibility of the circuit should be a simple matter. If it proves feasible, the major problem will be an investigation of the methods of reducing transformer recovery and delay time.

The alternative to a transformer input is the use of a difference amplifier. A preliminary investigation has been started toward the development of suitable circuitry for this purpose. This has revealed that the primary difficulties in such circuitry would be d-c unbalance because of parameter variations in the transistors and d-c drift. In this case, the major problem would be an investigation of the techniques for minimizing these difficulties.

If a satisfactory difference amplifier can be developed, ONE pulses can easily be changed to unipolarity pulses by the use of diode rectifiers at the output of the circuit. Conversion of the 1-microsecond memory pulses to 0.1-microsecond pulses will be attempted either through the use of a two-transistor chain gate following the diodes or by gating the difference amplifier itself so that it is inoperative except during strobe time. Figures 8 and 9 show possible circuits incorporating these methods.

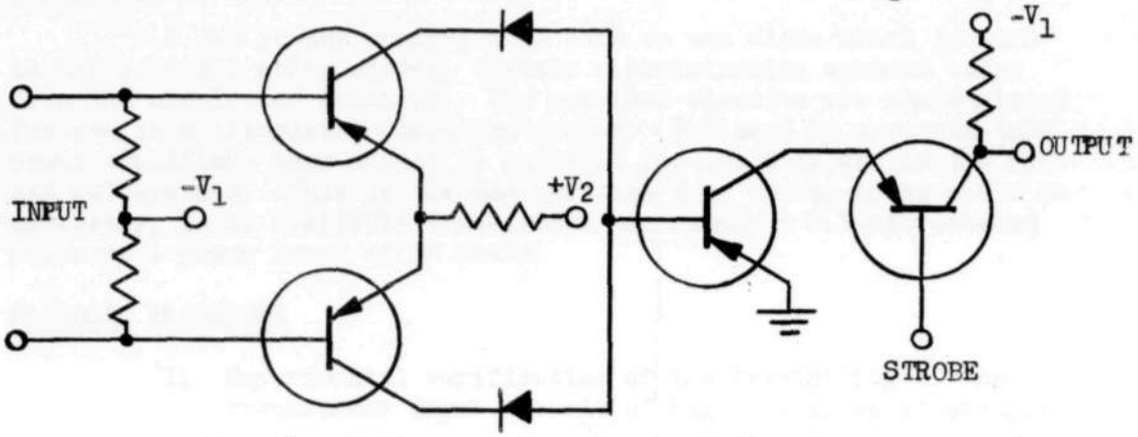

Fig. 8 - Difference Amplifier with Gated Output

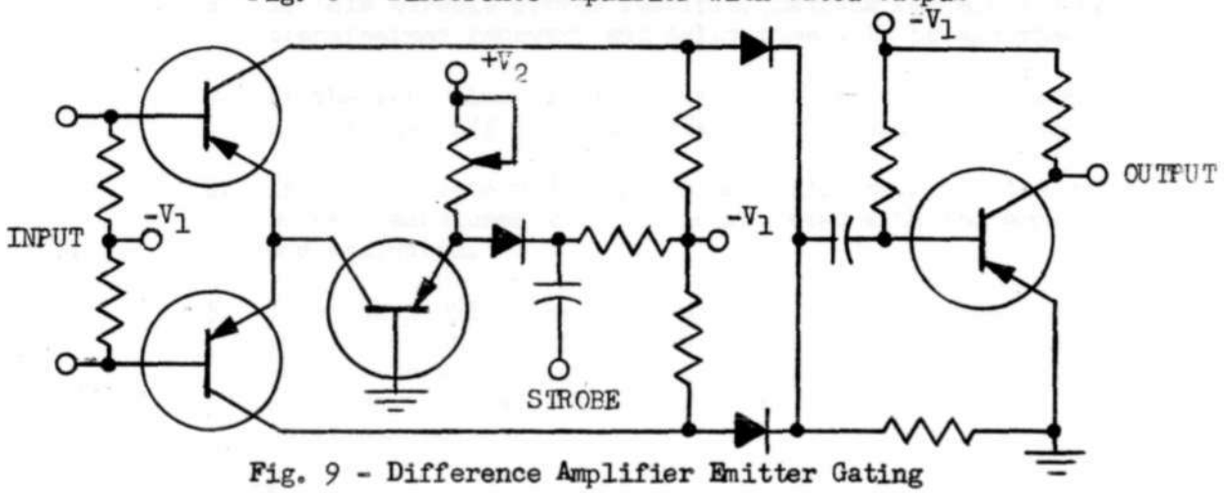

Fig. 9 - Difference Amplifier Emitter Gating

A 256 x 256 memory plane will probably contain at least four sensing windings. All of the circuits contemplated have been designed with diode outputs to allow these outputs to be mixed. In the case of the circuit of Fig. 9, for example, this could be accomplished as shown in Fig. 10.

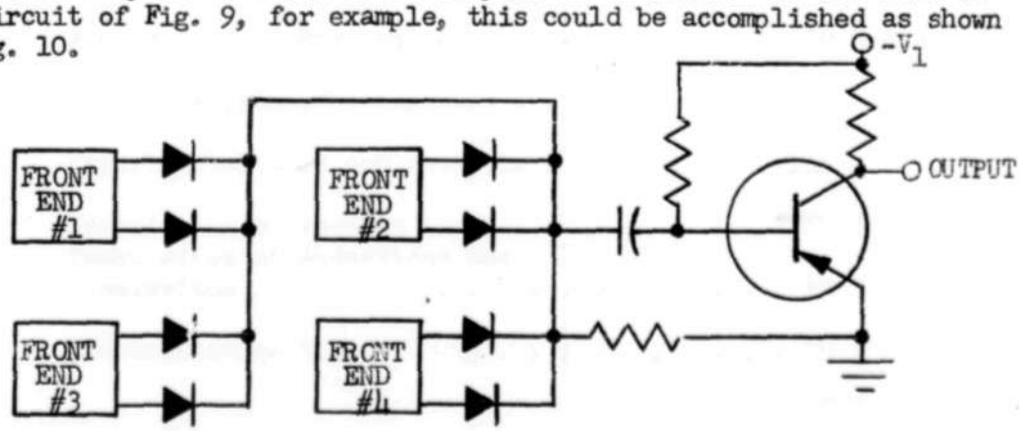

Fig. 10 - A Possible Mixing Scheme Using the Circuit of Fig. 9

A ONE in any winding will turn on one diode which in turn back-biases all other diodes, thereby discriminating against noise from the unselected windings. The previous circuits are contemplated for use in a transistor computing system. Followed by a vacuum-tube power amplifier, they should be suitable for possible use in the MTC and WWI systems. This is the one instance when vacuum-tubes would be necessary, as no available transistors can supply a 0.1-microsecond pulse at a power level of 10 watts.

PROPOSED PROCEDURE

1. Experimental verification of the feasibility of the transformer input circuit of Fig. 7 will be attempted.

2. If this circuit proves feasible, methods for minimizing transfoermer recovery and delay time will be analyzed.

3. At the same time, investigation will continue to develop a suitable difference amplifier for a sensing system.

4. If a satisfactory difference amplifier results, the gating schemes mentioned will be incorporated with the amplifier and evaluated.

5. If a 256 x 256 plane with multiple sense windings is available, an experimental model incorporating the more satisfactory techniques will be built and tested. In any case, a model suitable for use with MTC will be built and tested.

EQUIPMENT NEEDED

All necessary equipment is available from Lincoln Laboratory.

ESTIMATED TIME

Preparation of Proposal	50 hours
Further search of literature	20
Experimental work and analysis	165
Correlation of results and formulation of deductions and conclusions	40
Preparation of thesis	75
	350

SIGNED: F. Williams Sarles, Jr.
F. Williams Sarles, Jr.

DATE: March 7, 1955

FWS,jr./dg

SUPERVISION AGREEMENT

I consider this material adequate for a Master's Thesis and agree to supervise and evaluate the Thesis.

APPROVED: Richard D. Thornton
Richard D. Thornton
Instructor of Electrical Engineering

Distribution: J. W. Forrester
R. R. Everett
S. H. Dodd, Jr.
R. H. Baker
D. R. Brown
Staff, New-Components-and Circuits Section, Group 63
Staff, Memory Section, Group 63
Staff, Logical-Design Section, Group 63
Staff, System-Design Section, Group 63
R. D. Thornton, M.I.T., 10-441

Drawings: A-62054, Page 3
A-62053, Page 4

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