Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

Subject: MTC MEETING OF SEPTEMBER 9, 1952

To: MTC Planning Group

From: R. R. Everett and W. A. Hosier

Date: September 10, 1952

Abstract: Decisions and progress relevant to the proposed Memory Test Computer (MTC) are summarized for distribution to those interested, and to trace development of the computer.

Present:

| | | |
|---|---|---|
| H. Anderson | W. A. Hosier | R. Pfaff |
| J. Crane | R. Hughes | N. H. Taylor |
| R. R. Everett | K. H. Olsen | R. von Buelow |

Upon being asked to summarize MTC developments of the past two weeks, K. Olsen listed the following:

1. The few ceramic cores of smallest size (.06" O.D.) recently received and tested have been so much better than expected that a ceramic array for MTC does not seem so remote; does this mean that we need to speed up the other circuits (e. g., carry, parity check) to correspond to the shorter access time of the ferrite memory? Taylor doubted that we really do; about all we stand to gain in testing the array from increased speed is to ascertain effects of heating, and this might be more readily accomplished by other means, such as a repeated read-rewrite cycle of the sort proposed for memory display.

2. R. Hughes is perfecting the proposed peaker and buffer circuits.

3. H. Platt of Best's group is presumably still carrying on the studies of the plug-in flip-flop proposed at the meeting of August 22. It is important from the procurement standpoint to have conclusions from this work quite soon.

4. Matching difficulties have been encountered in the series arrangement of peakers and delays proposed for the carry circuit: different frequencies of the pulse spectrum are reflected unequally in the delay lines, causing distortion. Olsen proposed substitution of a carry flip-flop for the delay lines to circumvent this. However, before conceding that the delay line carry would require more development than we can afford to devote to it, Taylor suggested that we review the work done on delay lines going into WWI register drivers. There a reactive network was successfully used to clean up pulses which had been smeared by delay lines. It was agreed to try this, and report at the next meeting; if it does not solve the problem, we will revert to the carry flip-flop. If a carry flip-flop is included, high-speed carry will doubtless come along "free"; if not, it will have to be decided whether or not a high-speed carry justifies its cost.

5. Similar considerations, though less stringent, apply to the low-speed parity check. Olsen proposed a direct-coupled arrangement using 4 gate tubes per digit, a dim view of which was taken by Taylor as requiring too much development of untried techniques. It was agreed to present at the next meeting a specific quantitative comparison, in speed and equipment, of alternative parity check systems.

The importance of the time schedule was again mentioned - particularly lest dates on the procurement schedule pass without having the necessary decisions made. Smead agreed to act as "watch-dog" about this.

The metallic ribbon cores recently acquired from Magnetic Metals are quite promising; they do require more driving current than the previously tested cores from Magnetics, Inc., but the same drivers will probably be able to handle them.

At Taylor's suggestion, Papian and Ogden agreed to proceed with construction of trial circuits for a ceramic array, carrying this effort and that for metallic cores along in parallel until one or the other shows a distinct superiority.

Signed R. R. Everett
R. R. Everett

Signed W. A. Hosier
W. A. Hosier

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