Engineering Note E-475

Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

Subject: A MAGNETIC-CORE GATE AND ITS APPLICATION IN A STEPPING REGISTER

To: 6889 Engineers

From: G. R. Briggs

Date: October 30, 1952

Abstract: A magnetic-core gate to replace diodes is a necessity if an all-core computer is to be made feasible. A device is described composed of two magnetic cores and a resistance which will operate as a gate between the cores of a stepping register, replacing the diodes conventionally used. The theory of operation is presented, indicating an upper limit to the operating frequency of about 50 kc at present. A possible method of increasing the operating frequency is discussed.

1.0 Introduction

A magnetic-core device to prevent undesirable core interaction is needed in an all-core computer to insure that information pass only in a forward direction through the machine. Diodes have been used so far, but they have two serious disadvantages:

1) Preventing current flow in one direction is not sufficient in itself to eliminate unwanted core interaction.

2) Diodes in core circuits operate with large back-voltage forward-current products at the frequencies desired. Diodes commercially available, operating with the back-voltage forward-current products required with even the smallest cores now obtainable, are not too reliable. This situation is expected to improve considerably with the availability of smaller cores, such as the F-291 ferramic series. Diode heating is also a serious problem at high speeds.

A better device than a diode for preventing undesirable core interaction would be a switch in series with core-coupling windings. This switch could be closed only when useful information transfer is desired and left open at all other times. Applied to a stepping register,[1] (see Figure 1), the switch would be closed when transferring a "one" from the first to the second core, but open during transfer of the "one" from the second core to the third and while setting up the first core to a "one". This switch would operate properly if it were closed by the advance time pulse applied to the first core. The switch could be thought of as a time pulse operated gate circuit. Such a device, approximating a time pulse operated switch, using magnetic cores, without diodes, is the subject of this note.

2.0 A Magnetic-Core Gate Applied to a Stepping Register

A saturable reactor could be used to couple stepping-register cores, as shown in Figure 2. If it is desired that small coupling exist between core 1 and core 2, then the saturable reactor should be capable of absorbing the voltage output on core 1, producing no voltage drop across winding N_2 of core 2. This means that

$$e_1 = \frac{N_1 d\phi_1}{dt} = e_3 = N_3 \frac{d\phi_3}{dt}, \qquad (1)$$

or, if $\Delta\phi_1$ and $\Delta\phi_3$ are the flux changes that occur in a given time, by integrating equation (1);

$$N_1\Delta\phi_1 = N_3\Delta\phi_3. \qquad (2)$$

For the flux change $\Delta\phi_1$, the smallest possible current flow in the coupling circuit is desired to keep the loading of core 1 as small as possible. This means that $\frac{\Delta\phi_3}{N_3 I}$ unsaturated should be as large as possible, where $N_3 I$ is the mmf required by core 3 to produce the flux change $\Delta\phi_3$. On the other hand, if it is desirable to be able to pass information from core 1 to core 2 with as little loss as possible, core 3 should be capable of being saturated by an externally applied current pulse. The flux change in core 3 should then be as small as possible,

---

1. For a complete discussion of diode-coupled stepping registers, see Sims, Robert C., An Investigation of Magnetic-Core Stepping Registers for Digital Computers, Thesis, Digital Computer Laboratory, Massachusetts Institute of Technology, 1952.

whereas the information current should be as large as possible;

$\frac{\Delta\Phi_3}{N_3 I}$ saturated should be as small as possible. This is best accomplished by a core exhibiting a rectangular hysteresis loop, as shown in Figure 4. If the core is d-c biased by a current source to point b, and if c is the saturation operating point, it is obvious that the ratio

$$\frac{\frac{\Delta\Phi_3}{N_3 I}\text{ unsaturated}}{\frac{\Delta\Phi_3}{N_3 I}\text{ saturated}}$$

will have its greatest value. If the core were not biased to point b, but left unbiased at a, the mmf pulse required would have to be larger by an amount equal to the magnetizing mmf. This reduces $\frac{\Delta\Phi_3}{N_3 I}$ considerably for the materials available and is undesirable. This effect is illustrated in Figure 3, a plot of switching time of a stepping-register information core versus applied mmf. The data were taken for an arrangement which operated satisfactorily as a gate core. The switching time of the stepping core was measured as a function of the mmf drive applied to the stepping core for:

(1) an unloaded stepping core,

(2) a stepping core loaded with an unbiased gate core, and

(3) a stepping core loaded with a gate core biased almost to point b in Figure 4.

Major loop operation of the gate core was insured by a resetting saturation-current pulse applied to the gate core simultaneously with the resetting pulse applied to the stepping core. From Figure 3 it is plain that the biased gate core loads the stepping core much less than the unbiased gate core at the moderate switching times used in practice(half a microsecond and up).

Let us now follow the action of this gate during a stepping-register cycle of operation. Starting initially with "zero's" in both core 1 and core 2 and with the gate core biased to point b, as shown in Figure 5, repeated application of advance pulses 1 and 2 and

of the gate-core saturation pulse will have no effect because none of the cores are switched. Suppose core 1 is switched to a "one" by an information pulse from the previous stepping core; then in order to reduce the loading of core 1 as much as possible as it is switching, the gate core should keep the coupling-circuit current flow as small as possible. The gate core flux changes to some point, say c, under the influence of the small current I_1. This current loads core 1 negligibly and has no effect on core 2 since it is not in the proper direction to switch this core. At the end of this information pulse core 1 is in a "one" state, the gate core is at point d, and core 2 is still in a "zero" state. On the next advance pulse (1) it is necessary for the core to exhibit small $\frac{\Delta\phi_3}{N_3 1}$ in order that the "one" in core 1 may be passed on to core 2. Application of the gate-core saturation pulse will switch the gate core to point f, where $\frac{\Delta\phi_3}{N_3 1}$ will now be small.

This means that the gate-core flux change that occurred in setting up core 1 to a "one" state must be removed before the gate core works like a closed switch. During this process current flows in the coupling circuit in a direction opposed to the gate-core saturation pulse (Lenz' law) or in the I_1 direction in Figure 5. This current tends to switch core 1 back to a "zero" state before core 1 has time to pass the "one" on to core 2. For a coupling circuit containing no resistance, from equation (2) for setting up core 1 to a "one" state,

$$\Delta\phi_3 = \frac{N_1}{N_3}\Delta\phi_1, \qquad (3)$$

and if the flux change $\Delta\phi_3$ is removed, the corresponding flux change in core 1

$$\Delta\phi'_1 = \frac{N_3}{N_1}\Delta\phi'_3 = \frac{N_3}{N_1}\Delta\phi_3 = \frac{N_1}{N_3}\,\frac{N_3}{N_1}\Delta\phi_1 = \Delta\phi_1. \qquad (4)$$

This means that core 1 is switched completely back to a "zero" state before use can be made of its stored information. If some series resistance is introduced into the coupling circuit, however, (R in Figure 2), then it becomes possible to switch the gate core from point d to point e so slowly that the output emf of the gate core can never become large enough to drive sufficient current through the resistance to produce a large enough $N_1 I$ to reach the "knee" of the hysteresis loop of core 1 and switch this core. The best procedure is to apply a gate-core current pulse corresponding to approximately twice the magnetizing mmf of the core, slowly switching the core to a point in the neighborhood of e in Figure 5, then applying

a relatively fast, large, saturation-current pulse, moving on the loop rapidly to point f. Since the total flux change from e to f is small, much more rapid variation of mmf is possible without generating too large an output emf. After the switch-back of the gate core is complete, advance pulse 1 can occur, driving core 2 to a "one" state and resetting core 1 to a "zero" state. This is shown in Figure 6. I_2 is the coupling-circuit current flowing in this case. At the end of this process, the gate-core saturation-current pulse is removed, allowing the gate core to return to point h, which is the same as point b in Figure 5.

Next, one must consider the effect of advance pulse 2, which will reset core 2 to "zero", driving the "one" into the next stepping register core through a similar gate circuit. Information will tend to pass backward into core 1 now, as shown in Figure 7. The current I_3 tends to flow in the coupling circuit, and since the gate core still looks like a short circuit to this current, core 1 could be switched again. This situation can be remedied by adding a second gate core, as shown in Figure 8.

The windings on the two gate cores are poled as shown. Operation can be followed by reference to Figure 9. With "zero's" in both core 1 and core 2, application of advance pulses 1 and 2 and of the saturation-current pulse to the gate cores produces no switching of any core. On setting up core 1 to a "one" state, current I_1 flows in the coupling circuit, switching gate core A to point b, but not switching gate core B because of the reversed winding polarity. Gate core A is then slowly switched to d and then more rapidly to e by the gate-core saturation pulse, as discussed above. Gate core B is also saturated by the same gate-core current pulse, with negligibly small change in flux. On advance pulse 1, the "one" is driven from core 1 to core 2, as shown in Figure 10. I_2 in Figure 10 is the coupling-circuit current flow in this case, and if the gate-core saturation mmf is equal to or greater than the mmf applied to gate core B by the current I_2, then the switching of gate core B can be inhibited; the combination of gate cores looks like a closed switch, and core 2 will be switched to a "one" state. At the end of advance pulse 1, the gate-core saturation pulse can be removed, leaving the cores in the state represented by point g in Figure 10. So far in this discussion, core B has served no purpose. On advance pulse 2 (Figure 11), the "one" is switched out of core 2 into the following gate core, setting up a current I_3 (Lenz' law) in the coupling circuit. I_3 tends to switch core B (not affecting gate core A), and this switching absorbs the voltage output of core 2, keeping the current I_3 small. I_3 can be kept small enough to produce no switching of core 1 and also small enough to load core 2 negligibly.

Before the next advance pulse 1 can occur, gate core B must be switched back again to point j at least, or spurious information would be introduced into the coupling circuit by the action of the gate-core saturation pulse on core B. This is again done by applying a long current pulse of approximately twice the magnetizing mmf of core B, (the same pulse used to reset core A when driving core 1 to a "one"), slowly switching gate core B to point j in Figure 11. The output voltage of the gate core can be so small during this process that the current it can force through R is insufficient to switch core 2 to a significant extent. Thus core A acts as an isolation element upon setting up core 1 to a "one" state, whereas core B acts as an isolation element upon reading out the transferred "one" from core 2.

3.0 Analysis of the Performance of the Magnetic-Gate Stepping Register

For purposes of analysis, it is sufficient to consider only one gate core at a time; see Figure 12. Divide the problem into two cases:

(a) Setting up core 1 to a "one" state and switching back the gate core prior to applying advance pulse 1.

(b) Transferring of the "one" from core 1 to core 2 and then driving the "one" out of core 2 into the following stepping core and finally switching back the gate core prior to applying advance pulse 1 again.

Let N_1, N_2, N_3 be the number of turns on the cores, as shown in Figure 12. Also let:

$\Delta\phi_1$ = flux change produced by switching core 1.

$\Delta\phi_2$ = flux change produced by switching core 2. Major loop operation is assumed.

$\Delta\phi_3$ = flux change produced by partially or completely switching the gate core.

I_{m1} = maximum current flow in the coupling circuit produced by switching back core 3 for case (a).

F_{m1} = corresponding mmf in core 1.

I_{m2} = maximum current flow in the coupling circuit produced by switching back core 3 for case (b).

F_{m2} = corresponding mmf in core 2.

t_1 = switching time of core 1.

t_2 = switching time of core 2.

t_3 = switching time of core 3 while blocking current flow.

T = switching time of core 3 during resetting of the core.

F_1 = mmf required to switch unloaded core 1 in time t_1.

F_2 = mmf required to switch unloaded core 2 in time t_2.

F_{L2} = mmf reflected into core 2 by the output load on core 2.

F_{L1} = mmf reflected into core 1 by the input load on core 1.

In analyzing the operation, the approximation made by Sims[1] will be used. He assumed that the output voltage of any core is a rectangular pulse of constant voltage amplitude and of fixed duration, t. This implies $\frac{d\phi}{dt}$ is a constant during switching of a core. This approximation is very crude and can be expected to yield only qualitatively correct results. The true output voltage shapes, in practice, are more nearly triangular. But use of any more accurate approximation complicates the theory to a tremendous extent.

Case a: On switching core 1 to a "one" state, a relatively small current flows in the coupling circuit, causing a flux change in the gate core to occur. The drop across R will be so small during this process that it can be neglected and since the current flow is not in the proper direction to switch core 2, we have approximately,

$$N_1\Delta\phi_1 = N_3\Delta\phi_3, \qquad (5)$$

Where $\Delta\phi_3$ is the flux change that has occurred in the gate core. In order to reduce the loading effect on core 1 as much as possible, the current flow in the coupling circuit should be as small as possible. This is best done by decreasing $\Delta\phi_3$ as much as possible, reducing the mmf required by the gate core to produce the flux change to a minimum. By equation (5), N_3 must be increased ($N_1\Delta\phi_1$ assumed constant, of course).

---

1. Sims, R. C., loc. cit.

This means that the minimum mmf requirement is brought about by the maximum number of turns N_3 and that, accordingly, the coupling-circuit current is a minimum. This is the same as requiring the energy loss in the gate core to be as small as possible. $\Delta\phi_3$ can be generated by completely switching a small gate core or only partially switching a larger gate core. The former method is advantageous, because the largest possible ratio of unsaturated to saturated $\frac{\Delta\phi}{NI}$ is obtained by allowing the gate core to switch as far as possible in the unsaturated state. This is true because in practice the gate core cannot be biased quite to the "knee" of the hysteresis loop for reasons of stability, so that $\frac{\Delta\phi}{NI}$ will first be small until the "knee" is reached, then will increase greatly during the rest of the total flux change excursion. The average $\frac{\Delta\phi}{NI}$ that occurs during the process is thus reduced as the $\Delta\phi$ excursion is reduced. Another advantage gained with a small core of the same magnetic material is that usually a reduction in switching mmf can be obtained for a given switching time, t , as the core size is reduced. One serious disadvantage in practice is that N_3 must increase (or $\frac{N_3}{N_1}$, at least) as the gate core size is reduced. More turns must be wound on a core with a smaller central hole. The wire size must thus be very rapidly reduced as the core size is reduced. An optimum gate core size must therefore exist in the practical case.

As explained in section 2.0, the flux change $\Delta\phi_3$ must be gotten rid of before the occurrence of the next time pulse. The maximum $\frac{d\phi_3}{dt}$ that can be tolerated is one that will force a current of magnitude less than that which will tend to switch core 1 appreciably in a time T, the length of time it takes to get rid of the flux change in the gate core. This current corresponds to an mmf slightly larger than the magnetizing mmf of the stepping core. If this current is called I_{m1},

$$N_3\left(\frac{d\phi_3}{dt}\right)_{max.} = I_{m1}R; \qquad (6)$$

or, since $F_{m1} = N_1 I_{m1}$,

$$\frac{d\phi_3}{dt}_{max.} = \frac{F_{m1}R}{N_1 N_3} . \qquad (7)$$

If T_A is the switch-back time of the gate core A,

$$\left(\frac{d\phi_3}{dt}\right)_{max.} = \frac{\Delta\phi_3}{T_A} \quad \text{by Sims' approximation.} \tag{8}$$

This leads finally to:

$$T_{A\ min.} = \frac{N_1 N_3}{F_{m1} R}\Delta\phi_3 = \frac{N_1^2 \Delta\phi_1}{F_{m1} R}\ , \tag{9}$$

by substitution of $\Delta\phi_3$ by $\Delta\phi_1$ by equation (5). $T_{A\ min.}$ is the minimum switch-back time that can be tolerated; longer times are, of course, allowed. $T_{A\ min.}$ depends upon the value of R and varies inversely with R. R has an upper limit, as explained below. Use of the Sims approximation here gives too low a value of T_a, because in reality the maximum $\frac{d\phi_3}{dt}$ will exceed the average $\frac{d\phi_3}{dt}$.

$$\text{Or,} \left(\frac{d\phi_3}{dt}\right)_{max.} > \left(\frac{d\phi_3}{dt}\right)_{ave.} = \frac{\Delta\phi_3}{T}, \text{ or } T > \frac{\Delta\phi_3}{\left(\frac{d\phi_3}{dt}\right)_{max.}} = T_{min.} \tag{10}$$

Case B will next be considered. Here gate core B blocks coupling current flow on reading out of core 2. On resetting gate core B, a current I_{m2} flows as shown in Figure 12, tending to switch core 2 again. Carrying out the same analysis for this case, an expression for $T_{B\ min.}$ can be found which is the same as equation (9) with N_2^2, replacing N_1^2, if core 1 and core 2 are identical, as they are in all practical stepping registers. N_1 greater than N_2 is always required (see p. 15). This means that $T_{B\ min.}$ is less than $T_{A\ min.}$, but the value of T which must be used is the larger of the two values or $T_{A\ min.}$, because resetting of core A and core B must be done on every advance pulse for one or more coupling circuits in a register composed of many stepping cores. The net stepping period T must then be greater than the larger of T_A or T_B.

Upon driving the "one" from core 1 into core 2, the coupling-circuit current flow must supply the mmf F_2 to switch core 2 in time t_2, plus any additional mmf (F_{L2}) reflected back into core 2 by current flow in the load circuit (the next gate core). The voltage loop equation of the coupling circuit becomes, again using Sims' approximation:

$$\frac{R(F_2+F_{L2})}{N_2} + \frac{N_2\Delta\phi_2}{t_2} = \frac{N_1\Delta\phi_{1p}}{t_2}\ . \tag{11}$$

$\Delta\phi_{1p}$ is the flux change that occurs in core 1 during the switching of core 2, and $\frac{\Delta\phi_{1p}}{t_2} = \frac{d\phi_1}{dt}$ during this process, $\frac{d\phi_1}{dt}$ being considered constant. $\Delta\phi_{1p}$, rather than $\Delta\phi_1$, is used because core 1 is in general not switched completely by the time core 2 is switched completely. This is necessary to prevent possible attenuation of the information as it passes down a line of cores.[2] After the core has completely switched, all the output voltage of core 1 must appear across R; core 1 is therefore loaded much more heavily and requires a fairly long time to finish switching. In fact, it may not have time to switch completely by the end of advance pulse 1. If the core is practically completely switched, say greater than nine-tenths of a complete switch, by the time core 2 is completely switched, whether or not it is able to complete the switching process by the end of advance pulse 1 is not very important in practice; the introduction of spurious information is negligible on the next advance pulse 1. The ratio $\frac{\Delta\phi_{1p}}{\Delta\phi_1}$ depends upon the turns ratio $\frac{N_1}{N_2}$ as well as upon R, from equation (11).

Solve equation (11) for $\Delta\phi_{1p}$:[2]

$$\Delta\phi_{1p} = \frac{R}{N_1 N_2} t_2 (F_2 + F_{L2}) + \frac{N_2}{N_1} \Delta\phi_2,$$

and dividing by $\Delta\phi_1$,

$$\frac{\Delta\phi_{1p}}{\Delta\phi_1} = \frac{R\, t_2}{N_1 N_2 \Delta\phi_1} (F_2 + F_{L2}) + \frac{N_2}{N_1} \frac{\Delta\phi_2}{\Delta\phi_1}. \qquad (12)$$

Since usually core 1 and core 2 are the same size, $\Delta\phi_1 = \Delta\phi_2$, and

$$\frac{\Delta\phi_{1p}}{\Delta\phi} = \frac{R\, t_2}{N_1 N_2 \Delta\phi} (F_2 + F_{L2}) + \frac{N_2}{N_1} \qquad (13)$$

where $\Delta\phi \equiv \Delta\phi_1 = \Delta\phi_2$.

This shows if $\frac{\Delta\phi_{1p}}{\Delta\phi_1}$ is less than 1, as it must be for proper operation, $\frac{N_2}{N_1}$ less than 1 is always required. If $\frac{\Delta\phi_{1p}}{\Delta\phi}$ is equal to a maximum of 0.9, say, then $\frac{N_2}{N_1}$ is 0.9 maximum, and then only if R = 0. As R is increased to allow the recovery of the gate core in a reasonable

2. Buck, D. A., Binary Counting with Magnetic Cores, E-438, Digital Computer Laboratory, Massachusetts Institute of Technology, December 2, 1952.

time, $\frac{N_2}{N_1}$ must be correspondingly decreased. Substituting for R its value from equation (9) and solving for $\frac{T_{min.}}{t_2}$,

$$\frac{T_{min.}}{t_2} = \frac{N_1 (F_2 + F_{L2})}{N_2 F_{m1}} \cdot \frac{1}{\frac{\Delta\phi_{1p}}{\Delta\phi} - \frac{N_2}{N_1}} .$$

Since $\frac{\Delta\phi_{1p}}{\Delta\phi} = 0.9$, we get finally,

$$\frac{T_{min.}}{t_2} = \frac{F_2 + F_{L2}}{F_{m1}} \cdot \frac{1}{\frac{N_2}{N_1}\left(0.9 - \frac{N_2}{N_1}\right)} . \qquad (14)$$

It is, of course, desirable for maximum operating speed to keep $\frac{T_{min.}}{t_2}$ as small as possible. $T_{min.}$ has its minimum value for $\frac{N_1}{N_2} = \frac{2}{0.9} = 2.2$. Although this turns ratio gives the fastest operation, it also requires a rather large core-driving mmf.

To calculate the core 1 driving mmf required, the mmf reflected into core 1 from the coupling circuit to core 2 is:

$$F_{\text{reflected into core 1}} = \frac{N_1}{N_2} (F_2 + F_{L2}). \qquad (15)$$

Also, the mmf required to switch core 1 is very nearly F_2, since t_1 for $\frac{\Delta\phi_{1p}}{\Delta\phi} = 0.9$ is equal to t_2. This means that the mmf required to switch core 1 only 90% in the same time as a 100% switch of core 2 is less than F_2. No data are available to give an idea of how much less F_1 is, but for the purposes of this report, F_1 can be assumed equal to $F_2 \equiv F$. Also, another mmf is reflected into the core 1 from the previous gate core, which looks almost like an open circuit to core 1 on advance pulse 1, F_{L1}. F_{L2} is the load of the gate core following core 2. This gate core also looks almost like an open circuit to core 2, but F_{L2} is not equal to F_{L1} because the turns ratios are different in the two cases. Finally, the mmf drive which must be supplied to core 1

by advance pulse 1 is:

$$F_{drive} \cong F_{L1} + F + \frac{N_1}{N_2}(F + F_{L2}). \qquad (16)$$

If the gate core material is rectangular enough that voltage drop across the gate cores can be neglected when they are saturated, then only the loading effect of the unsaturated gate cores need be considered in finding the driving mmf. This gate core loading effect is best determined experimentally; Figure 3 gives data on the best ferrite gate cores tried. These cores were identical to the stepping cores and were considerably larger than is desirable; smaller cores are now becoming available and will soon be tested as gate cores. Molybdenum-permalloy cores also show great promise as gate cores, but the data for them are incomplete as yet.

T for the case of MF-1118 stepping cores of the F-259 size will now be calculated for a typical circuit, using the data of Figure 3 and also the data of Figure 13. Figure 13 contains curves of applied mmf versus switching time for the case of 5%, 10%, and 20% of complete core switching. This information is of importance in determining F_{m1}, for F_{m1} is the maximum mmf that can be applied to core 1 by the slow switching of the gate core without causing more than a negligible percentage of switching of this core.

The first step is to pick a reasonable value for $t_1 \cong t_2$, the switching time of the core. Let us pick $t_1 = 0.7$ of a microsecond (say), then $F + F_{L2} = 8.3$ ampere turns, from Figure 3. From Figure 13, assuming a 10% allowable core switching by the gate core, F_{m1} is about 2 ampere turns. For a turns ratio $\frac{N_1}{N_2} = 1.5$, for which the data of Figure 3 were taken, $T_{min.} = 19$ microseconds. This means an upper frequency limit of about 50 kc for the circuit tested. This experimental value of T can be used to find a better value of F_{m1} from Figure 13. A better value would be $F_{m1} = 1.9$ ampere turns. $T_{min.}$ can now be corrected slightly with this better value. Unfortunately this result cannot as yet be verified because the minimum prf of the test equipment is 150 kc at present. The mmf necessary to drive the register can also be calculated from equation (16) for this case. $F_{L1} + F = 7.4$ ampere turns from Figure 3, and the driving mmf = $7.4 + 1.5\ (8.3) = 19.9$ ampere turns. Switching an unloaded core in 0.7 microsecond takes $F = 6.2$ ampere turns. For 100% efficiency, it should take 12.4 ampere turns to switch both core 1 and core 2, or 7.5 ampere turns are necessary to handle gate core and resistive losses in this circuit. This efficiency is better than that of the diode-coupled stepping register[1] for this low turns ratio of $\frac{N_1}{N_2} = 1.5$.

---

1. Sims, R. C., loc. cit.

To indicate future possibilities, consider the driving mmf for the case $F_{L1} = F_{L2} = 0$, or the gate cores acting as perfect open circuits. Then for $\frac{N_1}{N_2} = 2.2$ (optimum) the driving mmf = 3.2F. This indicates a maximum efficiency of 62% for the fastest possible circuit. Also, $\frac{T_{min.}}{t_2} = \frac{4.9\ F_2}{F_{m1}}$ from equation (14) for the ideal case. $\frac{F_2}{F_{m1}}$ depends mostly upon the rectangularity of the core; it is 1 for a perfectly rectangular loop. It is about 3 for the ferrite cores presently in use. Thus $T_{min.}$ lies ideally between 5 and 15 times the switching time of the stepping cores.

4.0 Summary

The feasible speed of the magnetic-core plus resistance gate with ferrite cores of the F-259 size appears to be about 50 kc, which is 20 times slower than the corresponding diode-coupled circuits. Gate core driving requirements are very moderate, as the back emf's generated by the gate core during the saturation and slow switch-back pulses are small. The emf's generated across the gate-core external-pulse windings during the gate-core blocking operations are, however, quite large. These emf's always tend to increase the pulser plate voltage and require a pulser tube with sharp cut-off characteristics, biased considerably below cut-off. This can be quite serious if a long stepping register contains a fairly large number of "one's". Another disadvantage is that the individual cores must be switched in a time much less than the period of operation, producing larger back emf's upon driving than would be necessary with a diode-coupled register of the same transfer speed.

The logical place to use this circuit and other low-speed circuits based upon this gate would be for in-out problems in a computer of WWI speed. Even here the improvement in reliability over comparable diode-coupled circuits would be decreased because of the greater reliability of the diode circuits at low speeds, where the diode forward currents and back emf's can be kept small. Reducing the speed of diode circuits is limited by the forward resistance of the diodes, however, and this requires use of rather bulky selenium diodes at low speeds.

A possible method of increasing the frequency of operation is under investigation, and results will probably be incorporated into a future E-note. A capacitor is used instead of the resistor in the coupling circuit. The "ringing" current flow in this capacitor can be used to switch the gate core back after a blocking operation, requiring no external

gate-core current pulse. The reversed polarity of current flow in the coupling circuit does not tend to switch core 1 back, and the partial switching of core 2 that occurs instead is not serious. The stepping rate of the circuit is quite critical; it can only be varied a few percent from optimum for given circuit parameters. A "one" has been successfully cycled around a closed loop of four stepping cores at 300 kc by this circuit. In common with other capacitor-coupled core circuits tested it will require a great deal of engineering to make the circuit less critical to variations in parameters and driving currents.

Signed George R. Briggs
George R. Briggs

Approved
Norman H. Taylor

Approved William K. Linvill
William K. Linvill

GRB/bs

Drawings Attached:

A-52750 Fig. 1 and 2
A-52792 Fig. 3
A-52757 Fig. 4 and 5
A-52751 Fig. 6 and 7
A-52752 Fig. 8 and 9
A-52758 Fig. 10 and 11
A-52753 Fig. 12 and 13

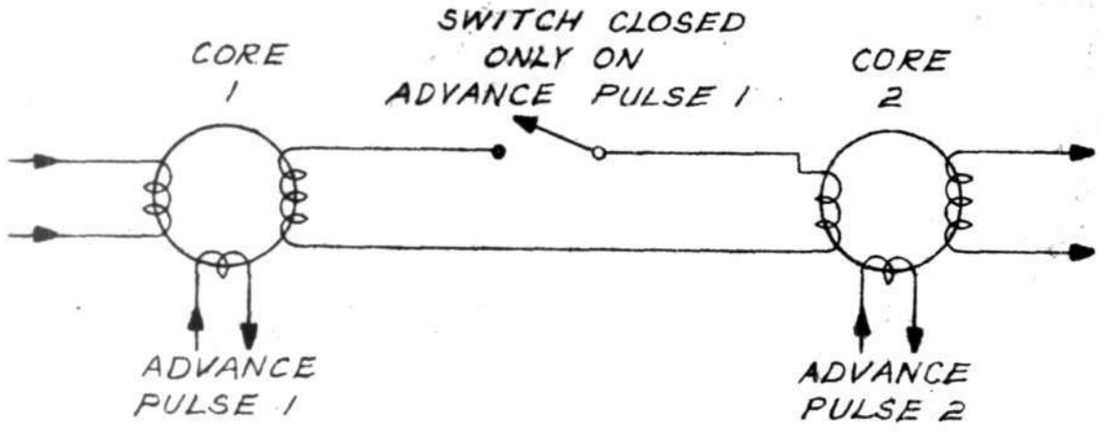

FIG. 1

STEPPING REGISTER WITH SWITCH ISOLATION

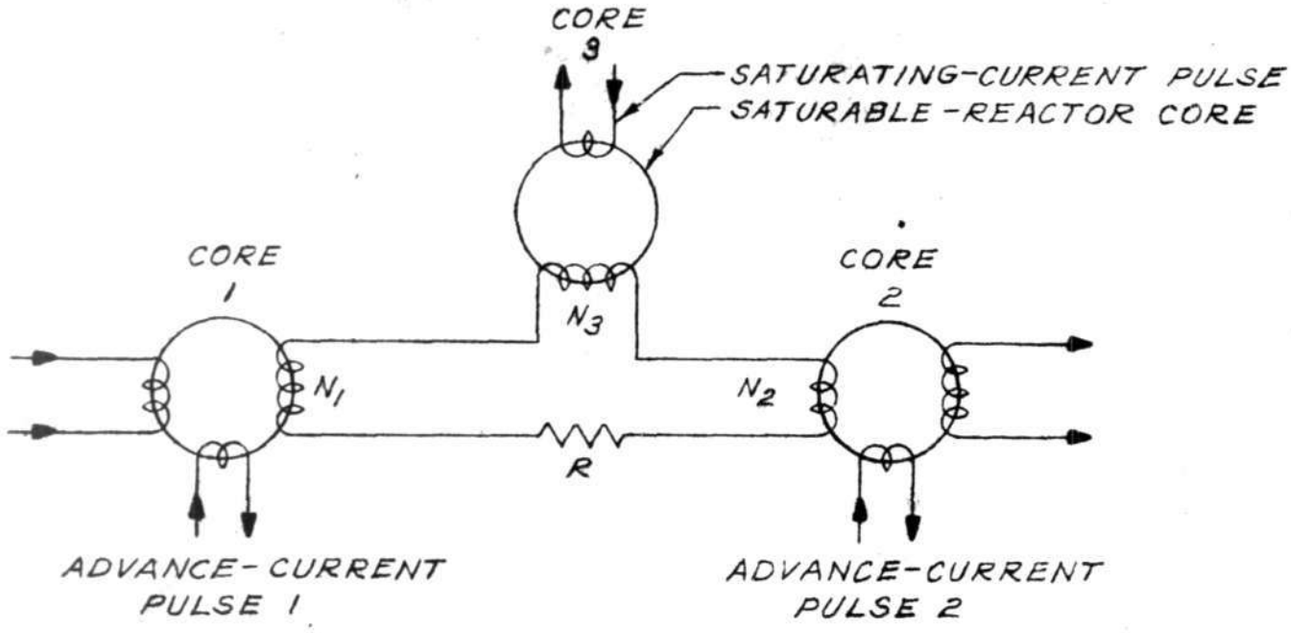

FIG. 2

A MAGNETIC-CORE GATE STEPPING REGISTER

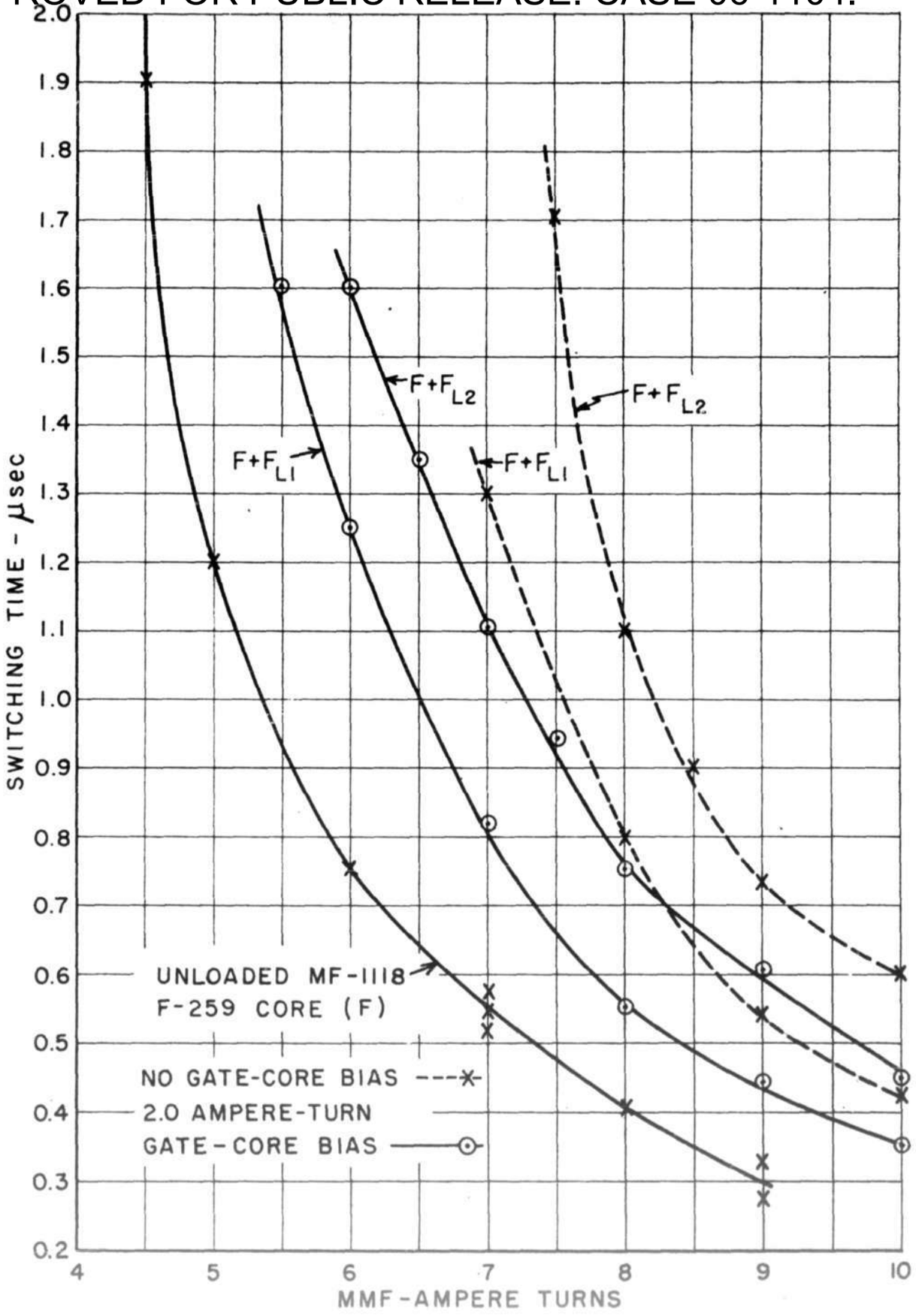

FIG. 3
SWITCHING TIME OF STEPPING CORE
WITH AND WITHOUT GATE-CORE LOAD

A-52792

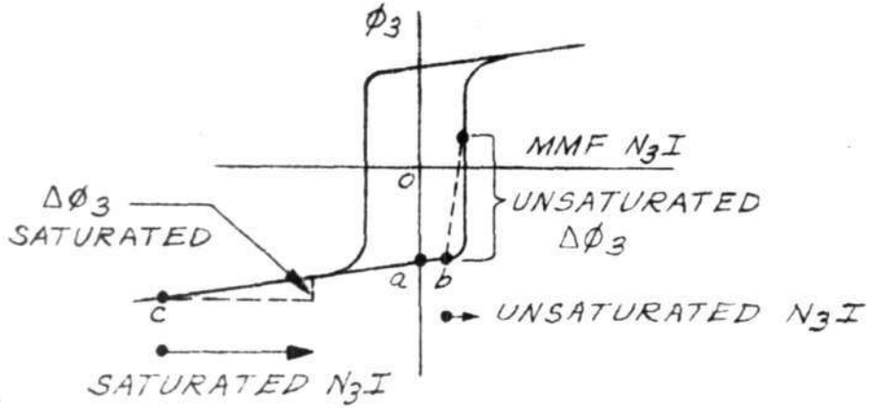

FIG. 4

GATE-CORE OPERATION

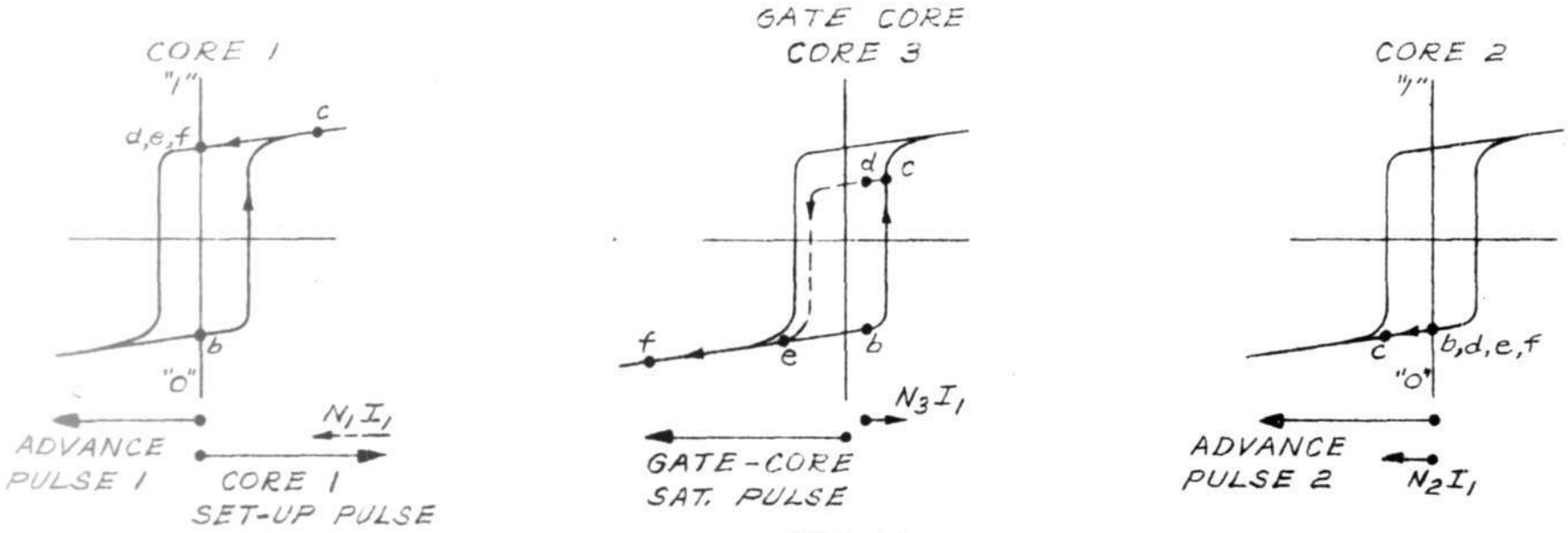

FIG. 5

SET-UP OF CORE 1 AND RESET CORE 3

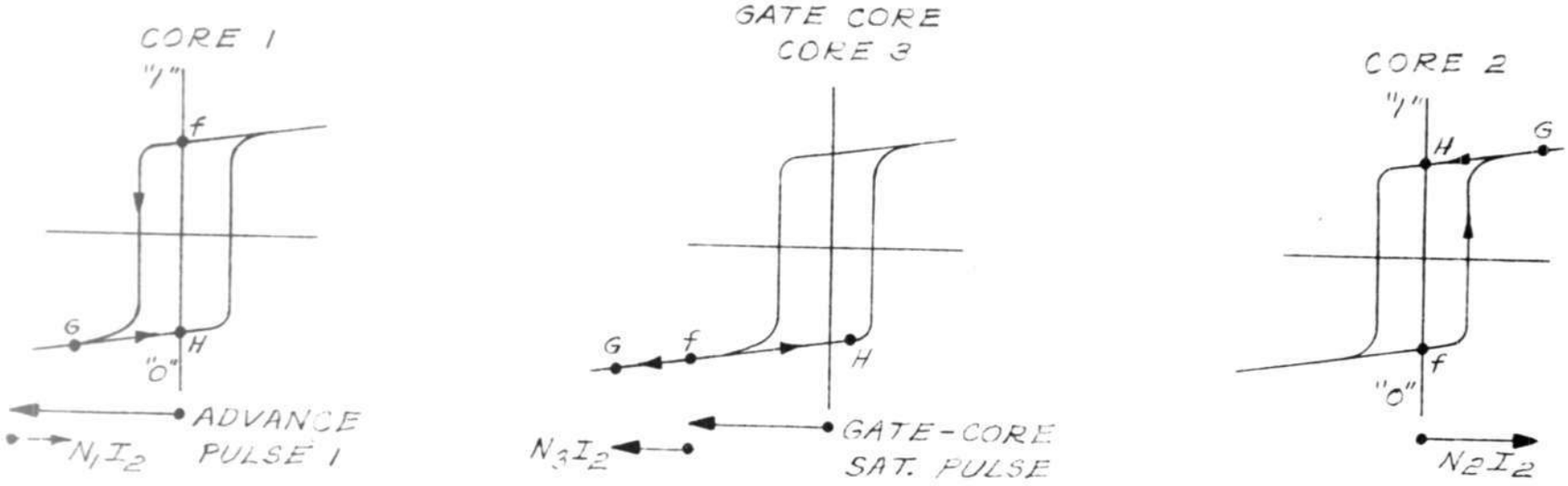

FIG. 6

TRANSFER OF "1" FROM CORE 1 TO CORE 2

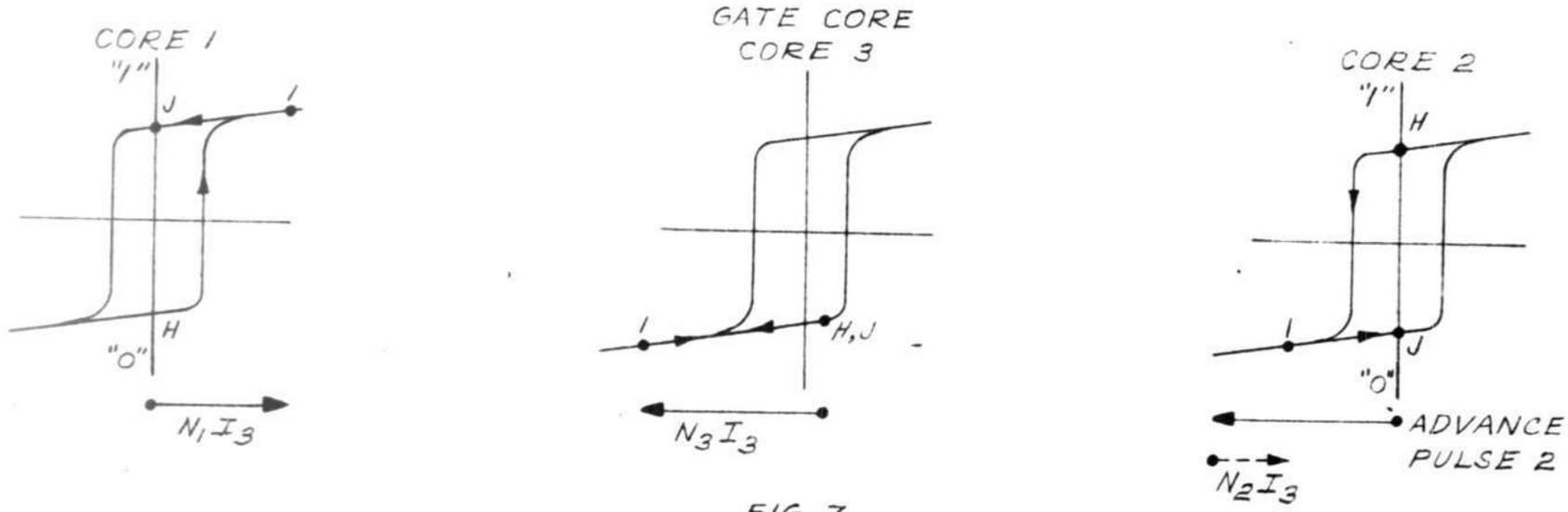

FIG. 7

READING OUT "1" FROM CORE 2

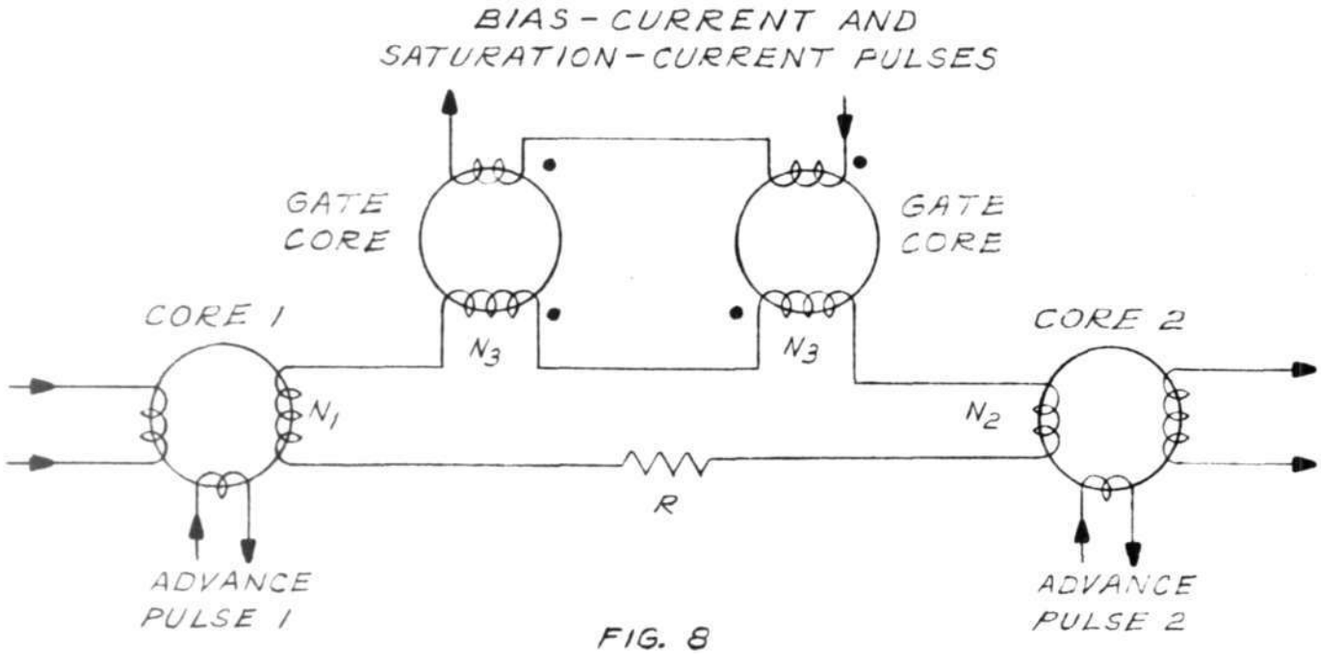

FIG. 8

FINAL CIRCUIT OF MAGNETIC-CORE GATE IN A STEPPING REGISTER

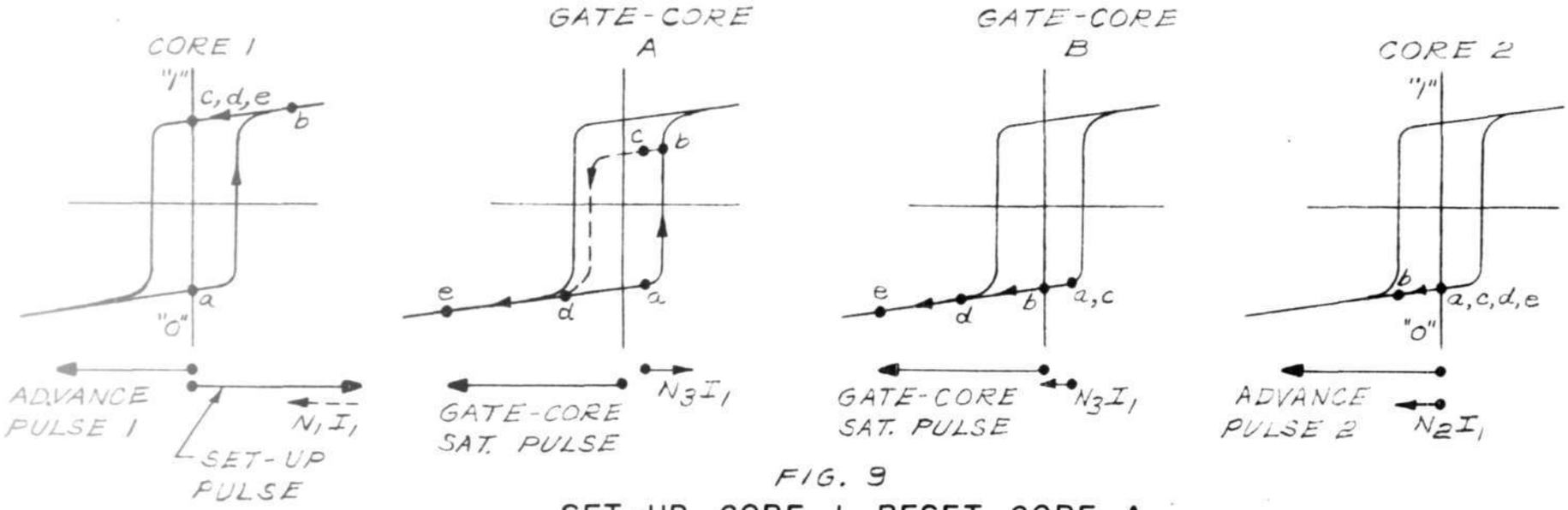

FIG. 9

SET-UP CORE 1, RESET CORE A

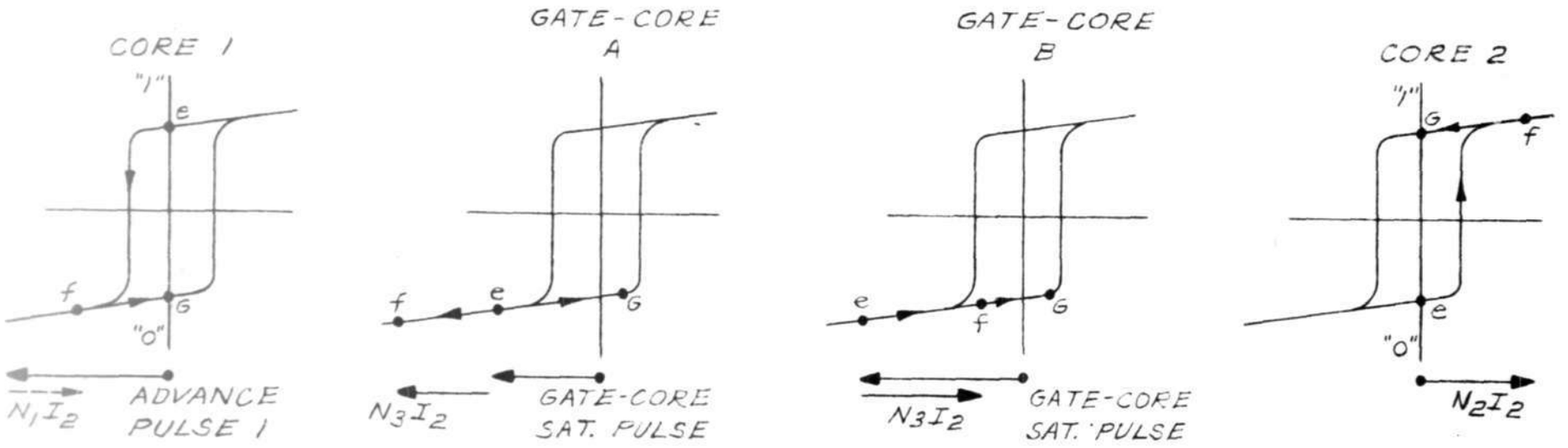

FIG. 10

TRANSFER OF "1" FROM CORE 1 TO CORE 2

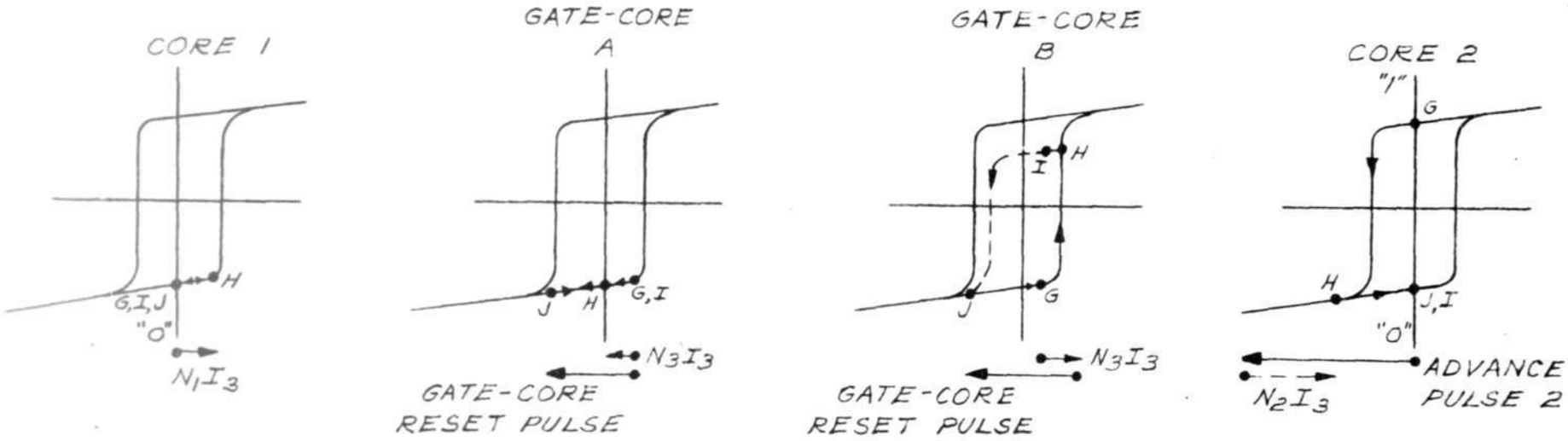

FIG. 11

READ-OUT "1" FROM CORE 2 AND RESET CORE B

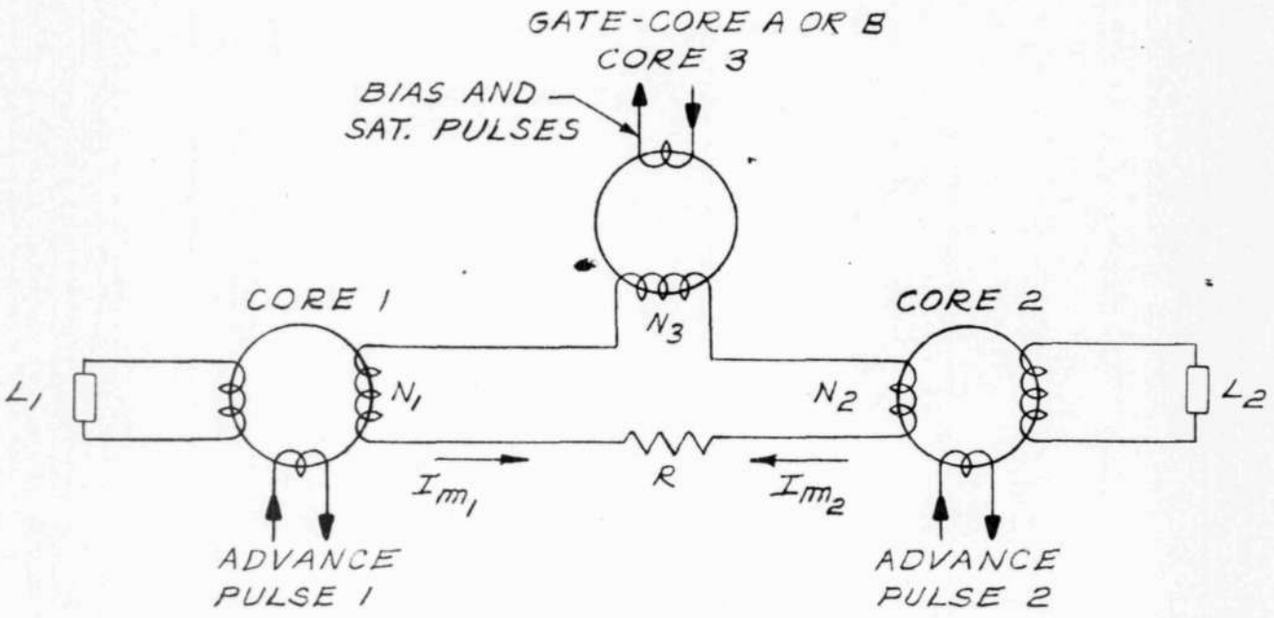

FIG. 12

GENERALIZED DIAGRAM OF CIRCUIT

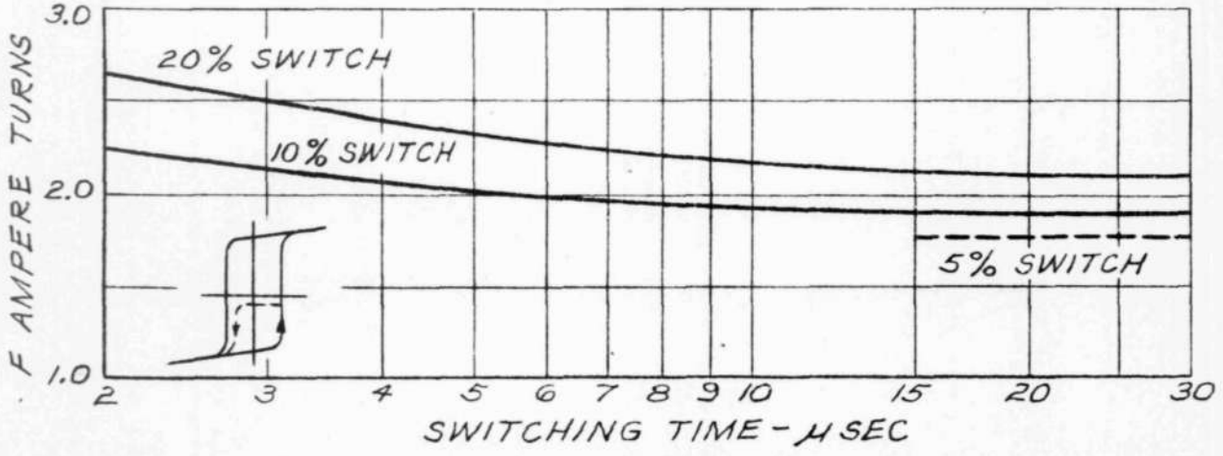

FIG. 13

F VS. SWITCHING TIME FOR PARTIAL SWITCHING OF A FERRITE CORE MF-1118 (F-259)

Engineering Note E-475

Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

Subject: A MAGNETIC-CORE GATE AND ITS APPLICATION IN A STEPPING REGISTER

To: 6889 Engineers

From: G. R. Briggs

Date: October 30, 1952

Abstract: A magnetic-core gate to replace diodes is a necessity if an all-core computer is to be made feasible. A device is described composed of two magnetic cores and a resistance which will operate as a gate between the cores of a stepping register, replacing the diodes conventionally used. The theory of operation is presented, indicating an upper limit to the operating frequency of about 50 kc at present. A possible method of increasing the operating frequency is discussed.

1.0 Introduction

A magnetic-core device to prevent undesirable core interaction is needed in an all-core computer to insure that information pass only in a forward direction through the machine. Diodes have been used so far, but they have two serious disadvantages:

1) Preventing current flow in one direction is not sufficient in itself to eliminate unwanted core interaction.

2) Diodes in core circuits operate with large back-voltage forward-current products at the frequencies desired. Diodes commercially available, operating with the back-voltage forward-current products required with even the smallest cores now obtainable, are not too reliable. This situation is expected to improve considerably with the availability of smaller cores, such as the F-291 ferramic series. Diode heating is also a serious problem at high speeds.

A better device than a diode for preventing undesirable core interaction would be a switch in series with core-coupling windings. This switch could be closed only when useful information transfer is desired and left open at all other times. Applied to a stepping register,[1] (see Figure 1), the switch would be closed when transferring a "one" from the first to the second core, but open during transfer of the "one" from the second core to the third and while setting up the first core to a "one". This switch would operate properly if it were closed by the advance time pulse applied to the first core. The switch could be thought of as a time pulse operated gate circuit. Such a device, approximating a time pulse operated switch, using magnetic cores, without diodes, is the subject of this note.

2.0 A Magnetic-Core Gate Applied to a Stepping Register

A saturable reactor could be used to couple stepping-register cores, as shown in Figure 2. If it is desired that small coupling exist between core 1 and core 2, then the saturable reactor should be capable of absorbing the voltage output on core 1, producing no voltage drop across winding N_2 of core 2. This means that

$$e_1 = \frac{N_1 d\phi_1}{dt} = e_3 = N_3 \frac{d\phi_3}{dt}, \qquad (1)$$

or, if $\Delta\phi_1$ and $\Delta\phi_3$ are the flux changes that occur in a given time, by integrating equation (1);

$$N_1\Delta\phi_1 = N_3\Delta\phi_3. \qquad (2)$$

For the flux change $\Delta\phi_1$, the smallest possible current flow in the coupling circuit is desired to keep the loading of core 1 as small as possible. This means that $\frac{\Delta\phi_3}{N_3 I}$ unsaturated should be as large as possible, where $N_3 I$ is the mmf required by core 3 to produce the flux change $\Delta\phi_3$. On the other hand, if it is desirable to be able to pass information from core 1 to core 2 with as little loss as possible, core 3 should be capable of being saturated by an externally applied current pulse. The flux change in core 3 should then be as small as possible,

---

1. For a complete discussion of diode-coupled stepping registers, see Sims, Robert C., An Investigation of Magnetic-Core Stepping Registers for Digital Computers, Thesis, Digital Computer Laboratory, Massachusetts Institute of Technology, 1952.

whereas the information current should be as large as possible;

$\frac{\Delta\Phi_3}{N_3 I}$ saturated should be as small as possible. This is best accomplished by a core exhibiting a rectangular hysteresis loop, as shown in Figure 4. If the core is d-c biased by a current source to point b, and if c is the saturation operating point, it is obvious that the ratio

$$\frac{\frac{\Delta\Phi_3}{N_3 I}\text{ unsaturated}}{\frac{\Delta\Phi_3}{N_3 I}\text{ saturated}}$$

will have its greatest value. If the core were not biased to point b, but left unbiased at a, the mmf pulse required would have to be larger by an amount equal to the magnetizing mmf. This reduces $\frac{\Delta\Phi_3}{N_3 I}$ considerably for the materials available and is undesirable. This effect is illustrated in Figure 3, a plot of switching time of a stepping-register information core versus applied mmf. The data were taken for an arrangement which operated satisfactorily as a gate core. The switching time of the stepping core was measured as a function of the mmf drive applied to the stepping core for:

(1) an unloaded stepping core,

(2) a stepping core loaded with an unbiased gate core, and

(3) a stepping core loaded with a gate core biased almost to point b in Figure 4.

Major loop operation of the gate core was insured by a resetting saturation-current pulse applied to the gate core simultaneously with the resetting pulse applied to the stepping core. From Figure 3 it is plain that the biased gate core loads the stepping core much less than the unbiased gate core at the moderate switching times used in practice(half a microsecond and up).

Let us now follow the action of this gate during a stepping-register cycle of operation. Starting initially with "zero's" in both core 1 and core 2 and with the gate core biased to point b, as shown in Figure 5, repeated application of advance pulses 1 and 2 and

of the gate-core saturation pulse will have no effect because none of the cores are switched. Suppose core 1 is switched to a "one" by an information pulse from the previous stepping core; then in order to reduce the loading of core 1 as much as possible as it is switching, the gate core should keep the coupling-circuit current flow as small as possible. The gate core flux changes to some point, say c, under the influence of the small current I_1. This current loads core 1 negligibly and has no effect on core 2 since it is not in the proper direction to switch this core. At the end of this information pulse core 1 is in a "one" state, the gate core is at point d, and core 2 is still in a "zero" state. On the next advance pulse (1) it is necessary for the core to exhibit small $\frac{\Delta\phi_3}{N_3 1}$ in order that the "one" in core 1 may be passed on to core 2. Application of the gate-core saturation pulse will switch the gate core to point f, where $\frac{\Delta\phi_3}{N_3 1}$ will now be small. This means that the gate-core flux change that occurred in setting up core 1 to a "one" state must be removed before the gate core works like a closed switch. During this process current flows in the coupling circuit in a direction opposed to the gate-core saturation pulse (Lenz' law) or in the I_1 direction in Figure 5. This current tends to switch core 1 back to a "zero" state before core 1 has time to pass the "one" on to core 2. For a coupling circuit containing no resistance, from equation (2) for setting up core 1 to a "one" state,

$$\Delta\phi_3 = \frac{N_1}{N_3}\Delta\phi_1, \qquad (3)$$

and if the flux change $\Delta\phi_3$ is removed, the corresponding flux change in core 1

$$\Delta\phi'_1 = \frac{N_3}{N_1}\Delta\phi'_3 = \frac{N_3}{N_1}\Delta\phi_3 = \frac{N_1}{N_3}\,\frac{N_3}{N_1}\Delta\phi_1 = \Delta\phi_1. \qquad (4)$$

This means that core 1 is switched completely back to a "zero" state before use can be made of its stored information. If some series resistance is introduced into the coupling circuit, however, (R in Figure 2), then it becomes possible to switch the gate core from point d to point e so slowly that the output emf of the gate core can never become large enough to drive sufficient current through the resistance to produce a large enough $N_1 I$ to reach the "knee" of the hysteresis loop of core 1 and switch this core. The best procedure is to apply a gate-core current pulse corresponding to approximately twice the magnetizing mmf of the core, slowly switching the core to a point in the neighborhood of e in Figure 5, then applying

a relatively fast, large, saturation-current pulse, moving on the loop rapidly to point f. Since the total flux change from e to f is small, much more rapid variation of mmf is possible without generating too large an output emf. After the switch-back of the gate core is complete, advance pulse 1 can occur, driving core 2 to a "one" state and resetting core 1 to a "zero" state. This is shown in Figure 6. I_2 is the coupling-circuit current flowing in this case. At the end of this process, the gate-core saturation-current pulse is removed, allowing the gate core to return to point h, which is the same as point b in Figure 5.

Next, one must consider the effect of advance pulse 2, which will reset core 2 to "zero", driving the "one" into the next stepping register core through a similar gate circuit. Information will tend to pass backward into core 1 now, as shown in Figure 7. The current I_3 tends to flow in the coupling circuit, and since the gate core still looks like a short circuit to this current, core 1 could be switched again. This situation can be remedied by adding a second gate core, as shown in Figure 8.

The windings on the two gate cores are poled as shown. Operation can be followed by reference to Figure 9. With "zero's" in both core 1 and core 2, application of advance pulses 1 and 2 and of the saturation-current pulse to the gate cores produces no switching of any core. On setting up core 1 to a "one" state, current I_1 flows in the coupling circuit, switching gate core A to point b, but not switching gate core B because of the reversed winding polarity. Gate core A is then slowly switched to d and then more rapidly to e by the gate-core saturation pulse, as discussed above. Gate core B is also saturated by the same gate-core current pulse, with negligibly small change in flux. On advance pulse 1, the "one" is driven from core 1 to core 2, as shown in Figure 10. I_2 in Figure 10 is the coupling-circuit current flow in this case, and if the gate-core saturation mmf is equal to or greater than the mmf applied to gate core B by the current I_2, then the switching of gate core B can be inhibited; the combination of gate cores looks like a closed switch, and core 2 will be switched to a "one" state. At the end of advance pulse 1, the gate-core saturation pulse can be removed, leaving the cores in the state represented by point g in Figure 10. So far in this discussion, core B has served no purpose. On advance pulse 2 (Figure 11), the "one" is switched out of core 2 into the following gate core, setting up a current I_3 (Lenz' law) in the coupling circuit. I_3 tends to switch core B (not affecting gate core A), and this switching absorbs the voltage output of core 2, keeping the current I_3 small. I_3 can be kept small enough to produce no switching of core 1 and also small enough to load core 2 negligibly.

Before the next advance pulse 1 can occur, gate core B must be switched back again to point j at least, or spurious information would be introduced into the coupling circuit by the action of the gate-core saturation pulse on core B. This is again done by applying a long current pulse of approximately twice the magnetizing mmf of core B, (the same pulse used to reset core A when driving core 1 to a "one"), slowly switching gate core B to point j in Figure 11. The output voltage of the gate core can be so small during this process that the current it can force through R is insufficient to switch core 2 to a significant extent. Thus core A acts as an isolation element upon setting up core 1 to a "one" state, whereas core B acts as an isolation element upon reading out the transferred "one" from core 2.

3.0 Analysis of the Performance of the Magnetic-Gate Stepping Register

For purposes of analysis, it is sufficient to consider only one gate core at a time; see Figure 12. Divide the problem into two cases:

(a) Setting up core 1 to a "one" state and switching back the gate core prior to applying advance pulse 1.

(b) Transferring of the "one" from core 1 to core 2 and then driving the "one" out of core 2 into the following stepping core and finally switching back the gate core prior to applying advance pulse 1 again.

Let N_1, N_2, N_3 be the number of turns on the cores, as shown in Figure 12. Also let:

$\Delta\phi_1$ = flux change produced by switching core 1.

$\Delta\phi_2$ = flux change produced by switching core 2. Major loop operation is assumed.

$\Delta\phi_3$ = flux change produced by partially or completely switching the gate core.

I_{m1} = maximum current flow in the coupling circuit produced by switching back core 3 for case (a).

F_{m1} = corresponding mmf in core 1.

I_{m2} = maximum current flow in the coupling circuit produced by switching back core 3 for case (b).

F_{m2} = corresponding mmf in core 2.

t_1 = switching time of core 1.

t_2 = switching time of core 2.

t_3 = switching time of core 3 while blocking current flow.

T = switching time of core 3 during resetting of the core.

F_1 = mmf required to switch unloaded core 1 in time t_1.

F_2 = mmf required to switch unloaded core 2 in time t_2.

F_{L2} = mmf reflected into core 2 by the output load on core 2.

F_{L1} = mmf reflected into core 1 by the input load on core 1.

In analyzing the operation, the approximation made by Sims[1] will be used. He assumed that the output voltage of any core is a rectangular pulse of constant voltage amplitude and of fixed duration, t. This implies $\frac{d\phi}{dt}$ is a constant during switching of a core. This approximation is very crude and can be expected to yield only qualitatively correct results. The true output voltage shapes, in practice, are more nearly triangular. But use of any more accurate approximation complicates the theory to a tremendous extent.

Case a: On switching core 1 to a "one" state, a relatively small current flows in the coupling circuit, causing a flux change in the gate core to occur. The drop across R will be so small during this process that it can be neglected and since the current flow is not in the proper direction to switch core 2, we have approximately,

$$N_1\Delta\phi_1 = N_3\Delta\phi_3, \qquad (5)$$

Where $\Delta\phi_3$ is the flux change that has occurred in the gate core. In order to reduce the loading effect on core 1 as much as possible, the current flow in the coupling circuit should be as small as possible. This is best done by decreasing $\Delta\phi_3$ as much as possible, reducing the mmf required by the gate core to produce the flux change to a minimum. By equation (5), N_3 must be increased ($N_1\Delta\phi_1$ assumed constant, of course).

---

1. Sims, R. C., loc. cit.

This means that the minimum mmf requirement is brought about by the maximum number of turns N_3 and that, accordingly, the coupling-circuit current is a minimum. This is the same as requiring the energy loss in the gate core to be as small as possible. $\Delta\phi_3$ can be generated by completely switching a small gate core or only partially switching a larger gate core. The former method is advantageous, because the largest possible ratio of unsaturated to saturated $\frac{\Delta\phi}{NI}$ is obtained by allowing the gate core to switch as far as possible in the unsaturated state. This is true because in practice the gate core cannot be biased quite to the "knee" of the hysteresis loop for reasons of stability, so that $\frac{\Delta\phi}{NI}$ will first be small until the "knee" is reached, then will increase greatly during the rest of the total flux change excursion. The average $\frac{\Delta\phi}{NI}$ that occurs during the process is thus reduced as the $\Delta\phi$ excursion is reduced. Another advantage gained with a small core of the same magnetic material is that usually a reduction in switching mmf can be obtained for a given switching time, t , as the core size is reduced. One serious disadvantage in practice is that N_3 must increase (or $\frac{N_3}{N_1}$, at least) as the gate core size is reduced. More turns must be wound on a core with a smaller central hole. The wire size must thus be very rapidly reduced as the core size is reduced. An optimum gate core size must therefore exist in the practical case.

As explained in section 2.0, the flux change $\Delta\phi_3$ must be gotten rid of before the occurrence of the next time pulse. The maximum $\frac{d\phi_3}{dt}$ that can be tolerated is one that will force a current of magnitude less than that which will tend to switch core 1 appreciably in a time T, the length of time it takes to get rid of the flux change in the gate core. This current corresponds to an mmf slightly larger than the magnetizing mmf of the stepping core. If this current is called I_{m1},

$$N_3\left(\frac{d\phi_3}{dt}\right)_{max.} = I_{m1}R; \qquad (6)$$

or, since $F_{m1} = N_1 I_{m1}$,

$$\frac{d\phi_3}{dt}_{max.} = \frac{F_{m1}R}{N_1 N_3} . \qquad (7)$$

If T_A is the switch-back time of the gate core A,

$$\left(\frac{d\phi_3}{dt}\right)_{max.} = \frac{\Delta\phi_3}{T_A} \quad \text{by Sims' approximation.} \tag{8}$$

This leads finally to:

$$T_{A\ min.} = \frac{N_1 N_3}{F_{m1} R}\Delta\phi_3 = \frac{N_1^2 \Delta\phi_1}{F_{m1} R}\ , \tag{9}$$

by substitution of $\Delta\phi_3$ by $\Delta\phi_1$ by equation (5). $T_{A\ min.}$ is the minimum switch-back time that can be tolerated; longer times are, of course, allowed. $T_{A\ min.}$ depends upon the value of R and varies inversely with R. R has an upper limit, as explained below. Use of the Sims approximation here gives too low a value of T_a, because in reality the maximum $\frac{d\phi_3}{dt}$ will exceed the average $\frac{d\phi_3}{dt}$.

$$\text{Or,} \left(\frac{d\phi_3}{dt}\right)_{max.} > \left(\frac{d\phi_3}{dt}\right)_{ave.} = \frac{\Delta\phi_3}{T}, \text{ or } T > \frac{\Delta\phi_3}{\left(\frac{d\phi_3}{dt}\right)_{max.}} = T_{min.} \tag{10}$$

Case B will next be considered. Here gate core B blocks coupling current flow on reading out of core 2. On resetting gate core B, a current I_{m2} flows as shown in Figure 12, tending to switch core 2 again. Carrying out the same analysis for this case, an expression for $T_{B\ min.}$ can be found which is the same as equation (9) with N_2^2, replacing N_1^2, if core 1 and core 2 are identical, as they are in all practical stepping registers. N_1 greater than N_2 is always required (see p. 15). This means that $T_{B\ min.}$ is less than $T_{A\ min.}$, but the value of T which must be used is the larger of the two values or $T_{A\ min.}$, because resetting of core A and core B must be done on every advance pulse for one or more coupling circuits in a register composed of many stepping cores. The net stepping period T must then be greater than the larger of T_A or T_B.

Upon driving the "one" from core 1 into core 2, the coupling-circuit current flow must supply the mmf F_2 to switch core 2 in time t_2, plus any additional mmf (F_{L2}) reflected back into core 2 by current flow in the load circuit (the next gate core). The voltage loop equation of the coupling circuit becomes, again using Sims' approximation:

$$\frac{R(F_2+F_{L2})}{N_2} + \frac{N_2\Delta\phi_2}{t_2} = \frac{N_1\Delta\phi_{1p}}{t_2}\ . \tag{11}$$

$\Delta\phi_{1p}$ is the flux change that occurs in core 1 during the switching of core 2, and $\frac{\Delta\phi_{1p}}{t_2} = \frac{d\phi_1}{dt}$ during this process, $\frac{d\phi_1}{dt}$ being considered constant. $\Delta\phi_{1p}$, rather than $\Delta\phi_1$, is used because core 1 is in general not switched completely by the time core 2 is switched completely. This is necessary to prevent possible attenuation of the information as it passes down a line of cores.[2] After the core has completely switched, all the output voltage of core 1 must appear across R; core 1 is therefore loaded much more heavily and requires a fairly long time to finish switching. In fact, it may not have time to switch completely by the end of advance pulse 1. If the core is practically completely switched, say greater than nine-tenths of a complete switch, by the time core 2 is completely switched, whether or not it is able to complete the switching process by the end of advance pulse 1 is not very important in practice; the introduction of spurious information is negligible on the next advance pulse 1. The ratio $\frac{\Delta\phi_{1p}}{\Delta\phi_1}$ depends upon the turns ratio $\frac{N_1}{N_2}$ as well as upon R, from equation (11).

Solve equation (11) for $\Delta\phi_{1p}$:[2]

$$\Delta\phi_{1p} = \frac{R}{N_1 N_2} t_2 (F_2 + F_{L2}) + \frac{N_2}{N_1} \Delta\phi_2,$$

and dividing by $\Delta\phi_1$,

$$\frac{\Delta\phi_{1p}}{\Delta\phi_1} = \frac{R\, t_2}{N_1 N_2 \Delta\phi_1} (F_2 + F_{L2}) + \frac{N_2}{N_1} \frac{\Delta\phi_2}{\Delta\phi_1}. \qquad (12)$$

Since usually core 1 and core 2 are the same size, $\Delta\phi_1 = \Delta\phi_2$, and

$$\frac{\Delta\phi_{1p}}{\Delta\phi} = \frac{R\, t_2}{N_1 N_2 \Delta\phi} (F_2 + F_{L2}) + \frac{N_2}{N_1} \qquad (13)$$

where $\Delta\phi \equiv \Delta\phi_1 = \Delta\phi_2$.

This shows if $\frac{\Delta\phi_{1p}}{\Delta\phi_1}$ is less than 1, as it must be for proper operation, $\frac{N_2}{N_1}$ less than 1 is always required. If $\frac{\Delta\phi_{1p}}{\Delta\phi}$ is equal to a maximum of 0.9, say, then $\frac{N_2}{N_1}$ is 0.9 maximum, and then only if R = 0. As R is increased to allow the recovery of the gate core in a reasonable

2. Buck, D. A., Binary Counting with Magnetic Cores, E-438, Digital Computer Laboratory, Massachusetts Institute of Technology, December 2, 1952.

time, $\frac{N_2}{N_1}$ must be correspondingly decreased. Substituting for R its value from equation (9) and solving for $\frac{T_{min.}}{t_2}$,

$$\frac{T_{min.}}{t_2} = \frac{N_1 (F_2 + F_{L2})}{N_2 F_{m1}} \quad \frac{1}{\frac{\Delta\Phi_{1p}}{\Delta\Phi} - \frac{N_2}{N_1}} .$$

Since $\frac{\Delta\Phi_{1p}}{\Delta\Phi} = 0.9$, we get finally,

$$\frac{T_{min.}}{t_2} = \frac{F_2 + F_{L2}}{F_{m1}} \quad \frac{1}{\frac{N_2}{N_1}\left(0.9 - \frac{N_2}{N_1}\right)} . \qquad (14)$$

It is, of course, desirable for maximum operating speed to keep $\frac{T_{min.}}{t_2}$ as small as possible. $T_{min.}$ has its minimum value for $\frac{N_1}{N_2} = \frac{2}{0.9} = 2.2$. Although this turns ratio gives the fastest operation, it also requires a rather large core-driving mmf.

To calculate the core 1 driving mmf required, the mmf reflected into core 1 from the coupling circuit to core 2 is:

$$F_{\text{reflected into core 1}} = \frac{N_1}{N_2} (F_2 + F_{L2}). \qquad (15)$$

Also, the mmf required to switch core 1 is very nearly F_2, since t_1 for $\frac{\Delta\Phi_{1p}}{\Delta\Phi} = 0.9$ is equal to t_2. This means that the mmf required to switch core 1 only 90% in the same time as a 100% switch of core 2 is less than F_2. No data are available to give an idea of how much less F_1 is, but for the purposes of this report, F_1 can be assumed equal to $F_2 \equiv F$. Also, another mmf is reflected into the core 1 from the previous gate core, which looks almost like an open circuit to core 1 on advance pulse 1, F_{L1}. F_{L2} is the load of the gate core following core 2. This gate core also looks almost like an open circuit to core 2, but F_{L2} is not equal to F_{L1} because the turns ratios are different in the two cases. Finally, the mmf drive which must be supplied to core 1

by advance pulse 1 is:

$$F_{drive} \cong F_{L1} + F + \frac{N_1}{N_2}(F + F_{L2}). \qquad (16)$$

If the gate core material is rectangular enough that voltage drop across the gate cores can be neglected when they are saturated, then only the loading effect of the unsaturated gate cores need be considered in finding the driving mmf. This gate core loading effect is best determined experimentally; Figure 3 gives data on the best ferrite gate cores tried. These cores were identical to the stepping cores and were considerably larger than is desirable; smaller cores are now becoming available and will soon be tested as gate cores. Molybdenum-permalloy cores also show great promise as gate cores, but the data for them are incomplete as yet.

T for the case of MF-1118 stepping cores of the F-259 size will now be calculated for a typical circuit, using the data of Figure 3 and also the data of Figure 13. Figure 13 contains curves of applied mmf versus switching time for the case of 5%, 10%, and 20% of complete core switching. This information is of importance in determining F_{m1}, for F_{m1} is the maximum mmf that can be applied to core 1 by the slow switching of the gate core without causing more than a negligible percentage of switching of this core.

The first step is to pick a reasonable value for $t_1 \cong t_2$, the switching time of the core. Let us pick $t_1 = 0.7$ of a microsecond (say), then $F + F_{L2} = 8.3$ ampere turns, from Figure 3. From Figure 13, assuming a 10% allowable core switching by the gate core, F_{m1} is about 2 ampere turns. For a turns ratio $\frac{N_1}{N_2} = 1.5$, for which the data of Figure 3 were taken, $T_{min.} = 19$ microseconds. This means an upper frequency limit of about 50 kc for the circuit tested. This experimental value of T can be used to find a better value of F_{m1} from Figure 13. A better value would be $F_{m1} = 1.9$ ampere turns. $T_{min.}$ can now be corrected slightly with this better value. Unfortunately this result cannot as yet be verified because the minimum prf of the test equipment is 150 kc at present. The mmf necessary to drive the register can also be calculated from equation (16) for this case. $F_{L1} + F = 7.4$ ampere turns from Figure 3, and the driving mmf $= 7.4 + 1.5\,(8.3) = 19.9$ ampere turns. Switching an unloaded core in 0.7 microsecond takes $F = 6.2$ ampere turns. For 100% efficiency, it should take 12.4 ampere turns to switch both core 1 and core 2, or 7.5 ampere turns are necessary to handle gate core and resistive losses in this circuit. This efficiency is better than that of the diode-coupled stepping register[1] for this low turns ratio of $\frac{N_1}{N_2} = 1.5$.

---

1. Sims, R. C., loc. cit.

To indicate future possibilities, consider the driving mmf for the case $F_{L1} = F_{L2} = 0$, or the gate cores acting as perfect open circuits. Then for $\frac{N_1}{N_2} = 2.2$ (optimum) the driving mmf = 3.2F. This indicates a maximum efficiency of 62% for the fastest possible circuit. Also, $\frac{T_{min.}}{t_2} = \frac{4.9\ F_2}{F_{m1}}$ from equation (14) for the ideal case. $\frac{F_2}{F_{m1}}$ depends mostly upon the rectangularity of the core; it is 1 for a perfectly rectangular loop. It is about 3 for the ferrite cores presently in use. Thus $T_{min.}$ lies ideally between 5 and 15 times the switching time of the stepping cores.

4.0 Summary

The feasible speed of the magnetic-core plus resistance gate with ferrite cores of the F-259 size appears to be about 50 kc, which is 20 times slower than the corresponding diode-coupled circuits. Gate core driving requirements are very moderate, as the back emf's generated by the gate core during the saturation and slow switch-back pulses are small. The emf's generated across the gate-core external-pulse windings during the gate-core blocking operations are, however, quite large. These emf's always tend to increase the pulser plate voltage and require a pulser tube with sharp cut-off characteristics, biased considerably below cut-off. This can be quite serious if a long stepping register contains a fairly large number of "one's". Another disadvantage is that the individual cores must be switched in a time much less than the period of operation, producing larger back emf's upon driving than would be necessary with a diode-coupled register of the same transfer speed.

The logical place to use this circuit and other low-speed circuits based upon this gate would be for in-out problems in a computer of WWI speed. Even here the improvement in reliability over comparable diode-coupled circuits would be decreased because of the greater reliability of the diode circuits at low speeds, where the diode forward currents and back emf's can be kept small. Reducing the speed of diode circuits is limited by the forward resistance of the diodes, however, and this requires use of rather bulky selenium diodes at low speeds.

A possible method of increasing the frequency of operation is under investigation, and results will probably be incorporated into a future E-note. A capacitor is used instead of the resistor in the coupling circuit. The "ringing" current flow in this capacitor can be used to switch the gate core back after a blocking operation, requiring no external

gate-core current pulse. The reversed polarity of current flow in the coupling circuit does not tend to switch core 1 back, and the partial switching of core 2 that occurs instead is not serious. The stepping rate of the circuit is quite critical; it can only be varied a few percent from optimum for given circuit parameters. A "one" has been successfully cycled around a closed loop of four stepping cores at 300 kc by this circuit. In common with other capacitor-coupled core circuits tested it will require a great deal of engineering to make the circuit less critical to variations in parameters and driving currents.

Signed George R. Briggs
George R. Briggs

Approved
Norman H. Taylor

Approved William K. Linvill
William K. Linvill

GRB/bs

Drawings Attached:

A-52750 Fig. 1 and 2
A-52792 Fig. 3
A-52757 Fig. 4 and 5
A-52751 Fig. 6 and 7
A-52752 Fig. 8 and 9
A-52758 Fig. 10 and 11
A-52753 Fig. 12 and 13

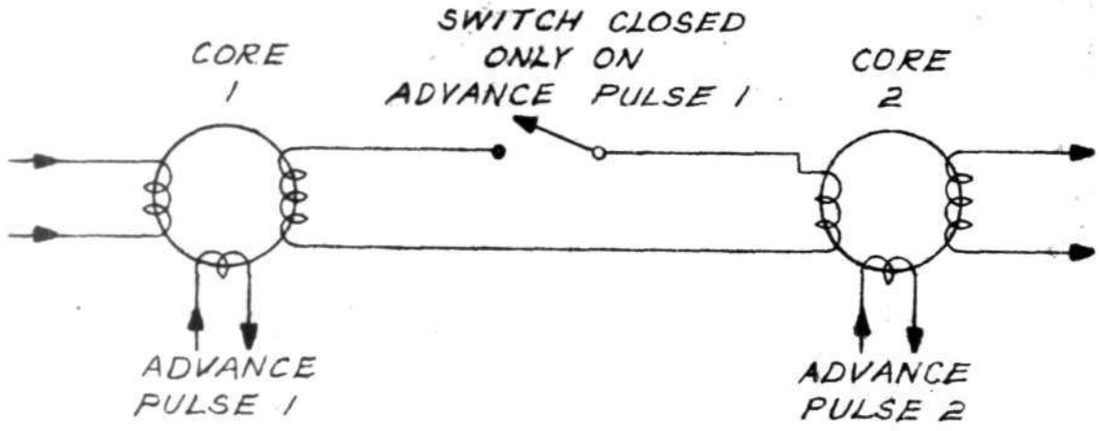

FIG. 1

STEPPING REGISTER WITH SWITCH ISOLATION

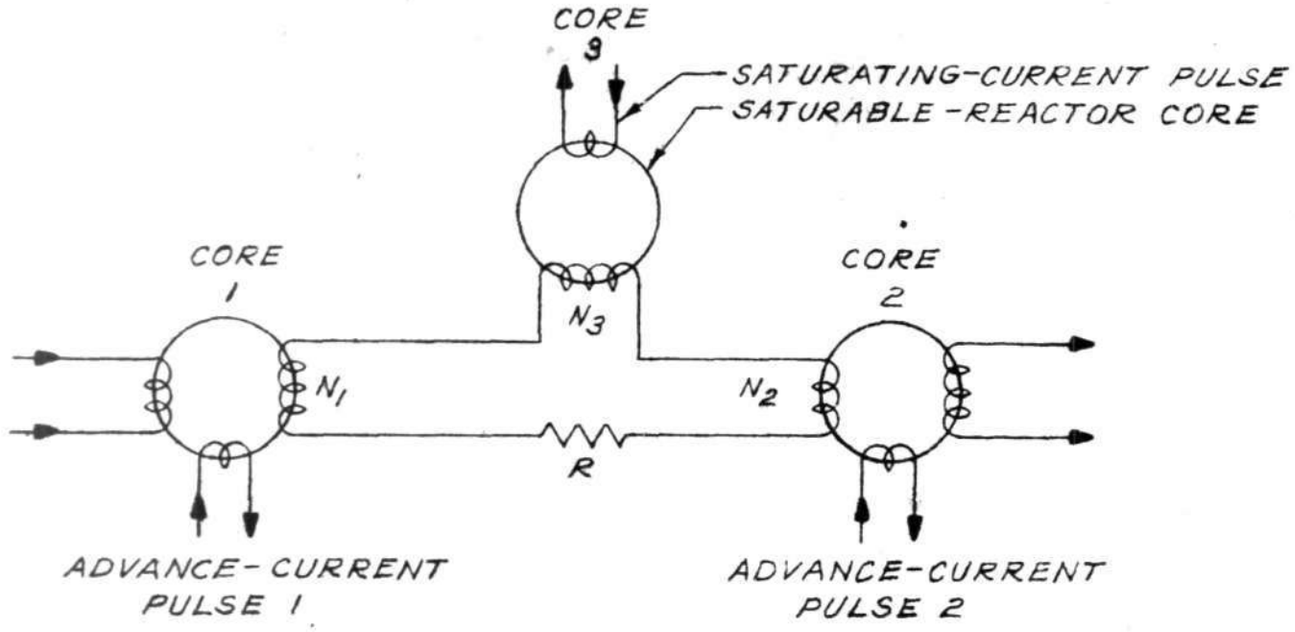

FIG. 2

A MAGNETIC-CORE GATE STEPPING REGISTER

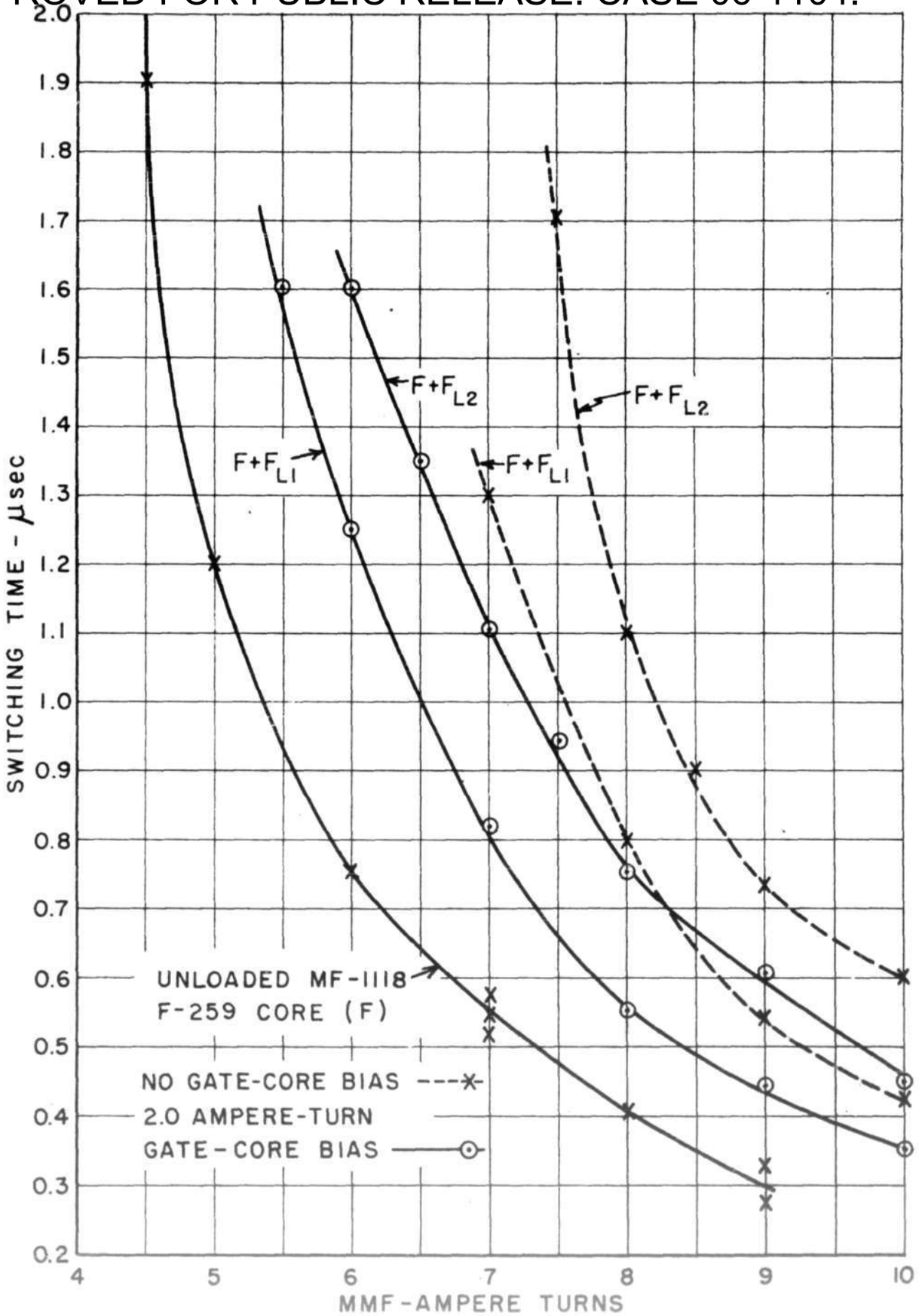

FIG. 3
SWITCHING TIME OF STEPPING CORE
WITH AND WITHOUT GATE-CORE LOAD

A-52792

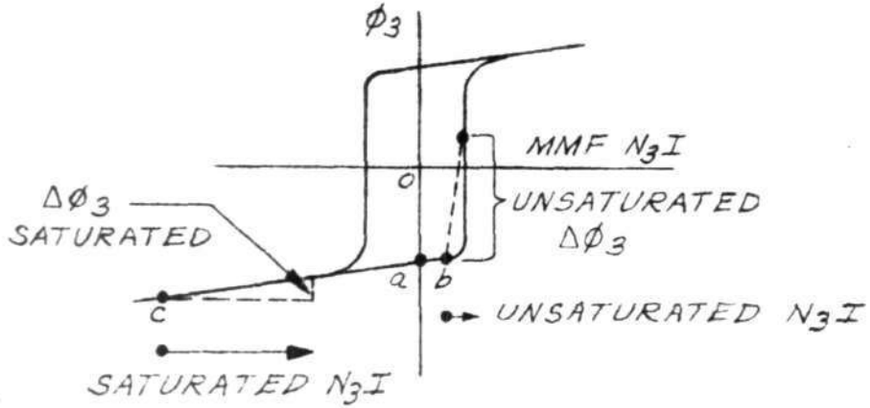

FIG. 4

GATE-CORE OPERATION

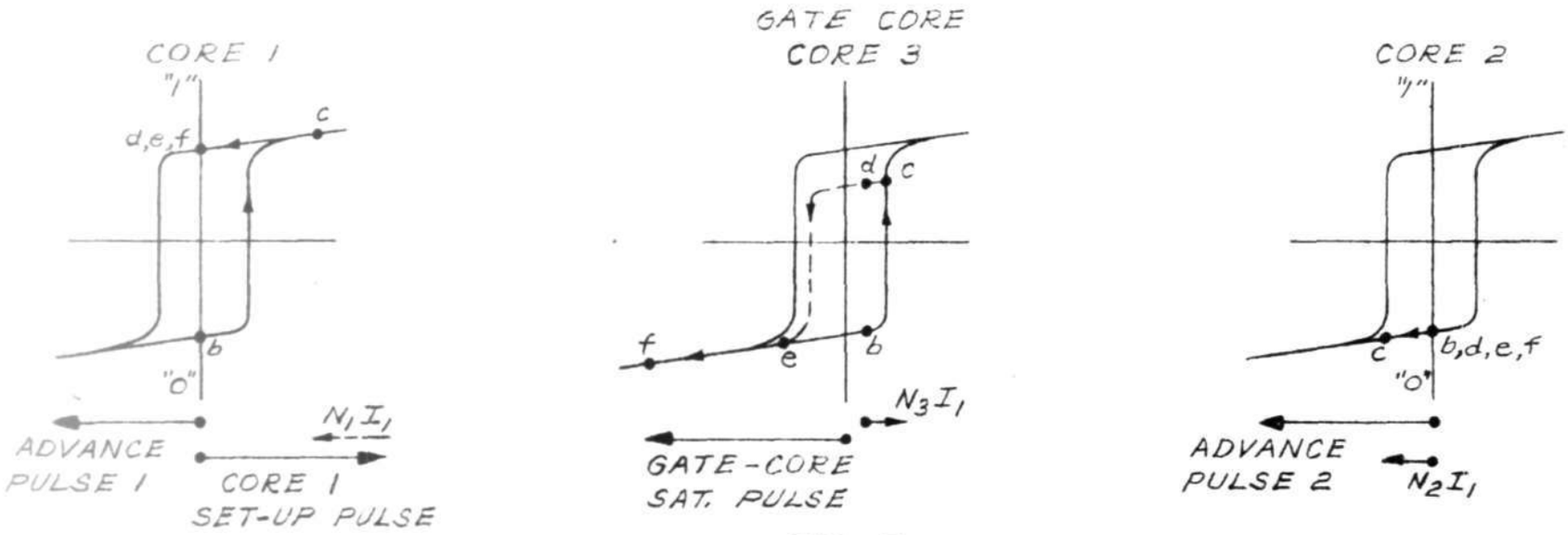

FIG. 5

SET-UP OF CORE 1 AND RESET CORE 3

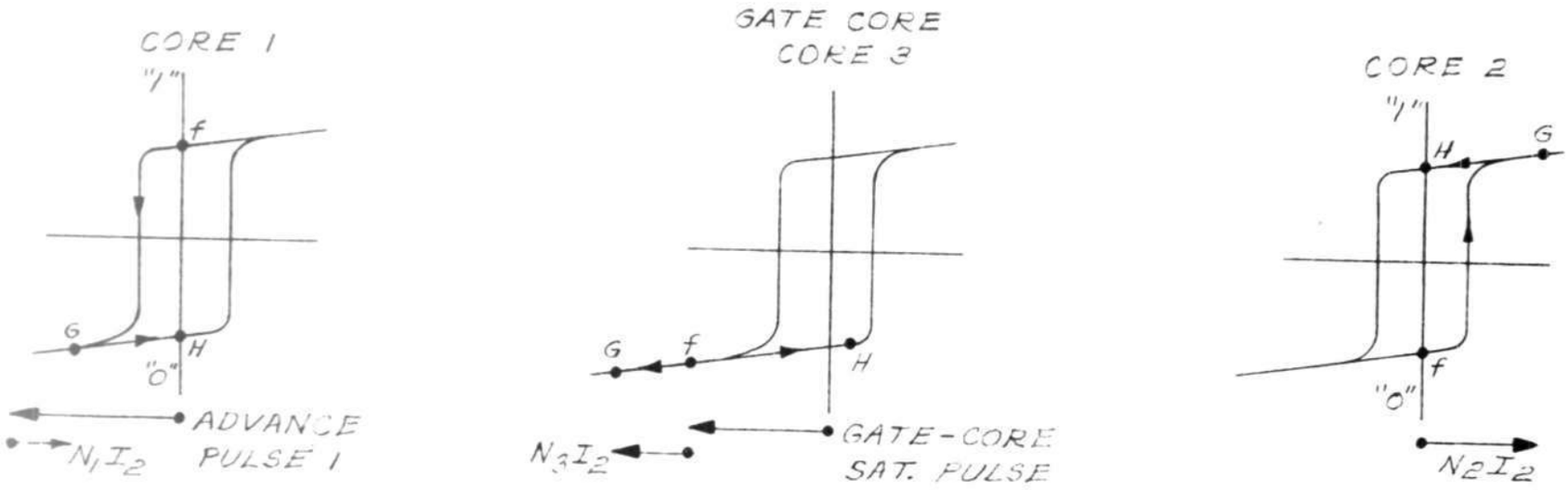

FIG. 6

TRANSFER OF "1" FROM CORE 1 TO CORE 2

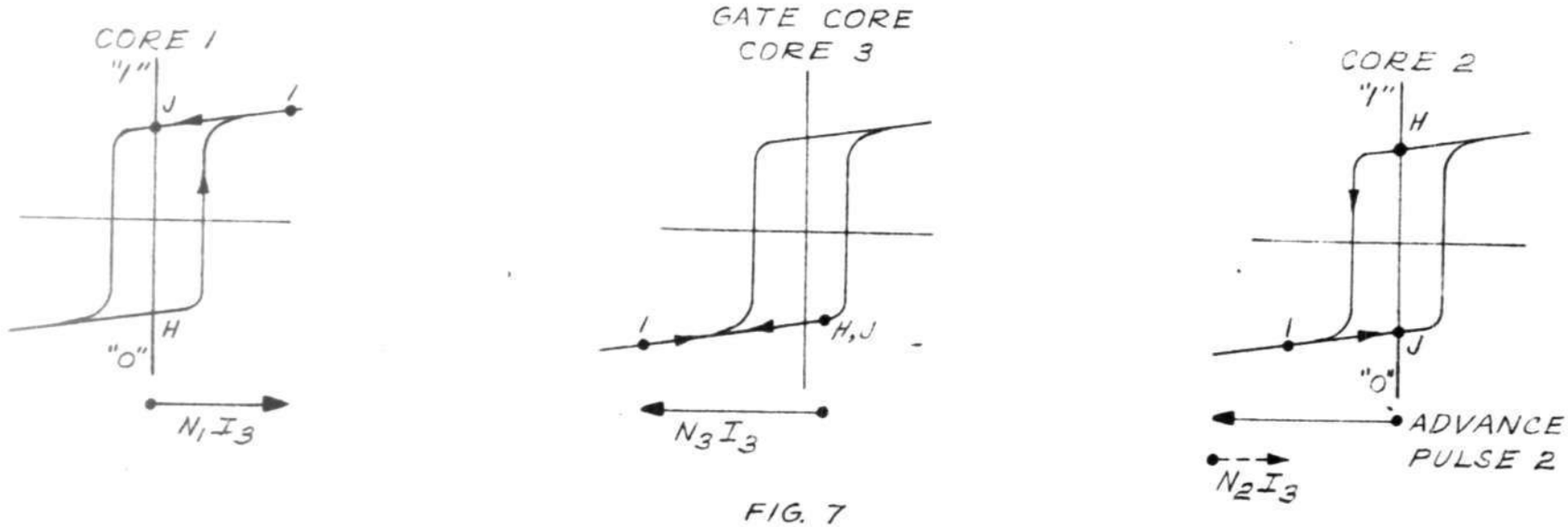

FIG. 7

READING OUT "1" FROM CORE 2

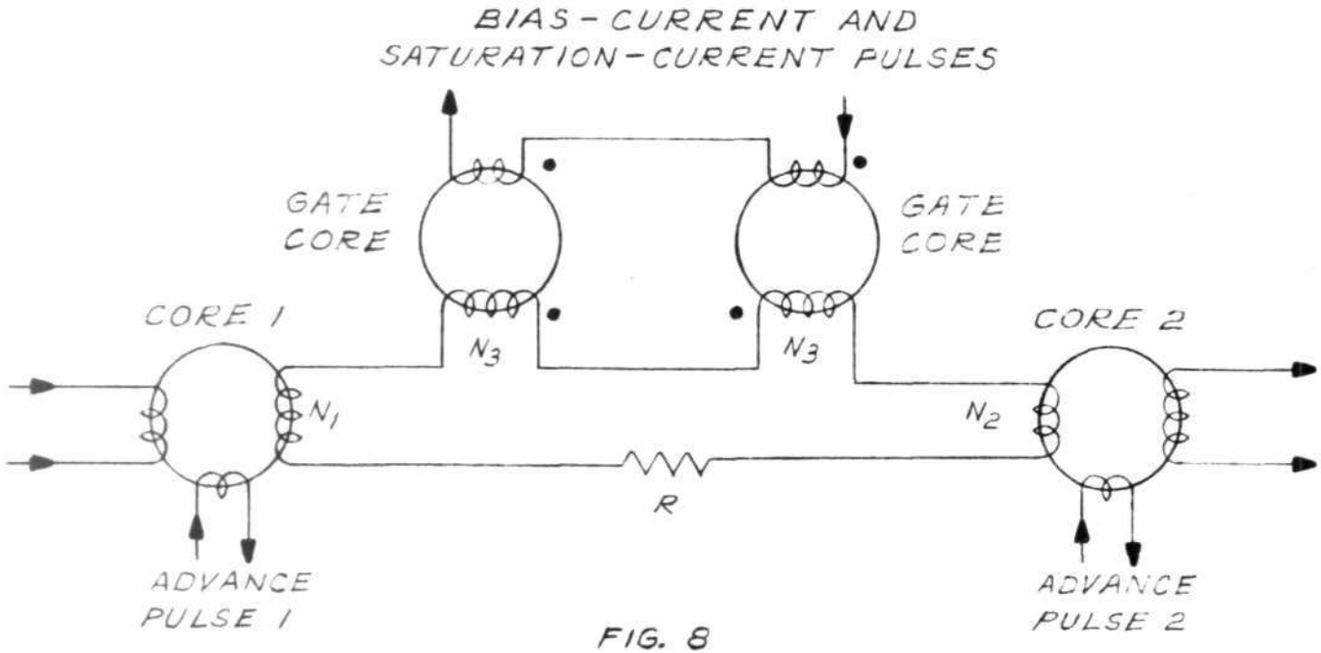

FIG. 8

FINAL CIRCUIT OF MAGNETIC-CORE GATE IN A STEPPING REGISTER

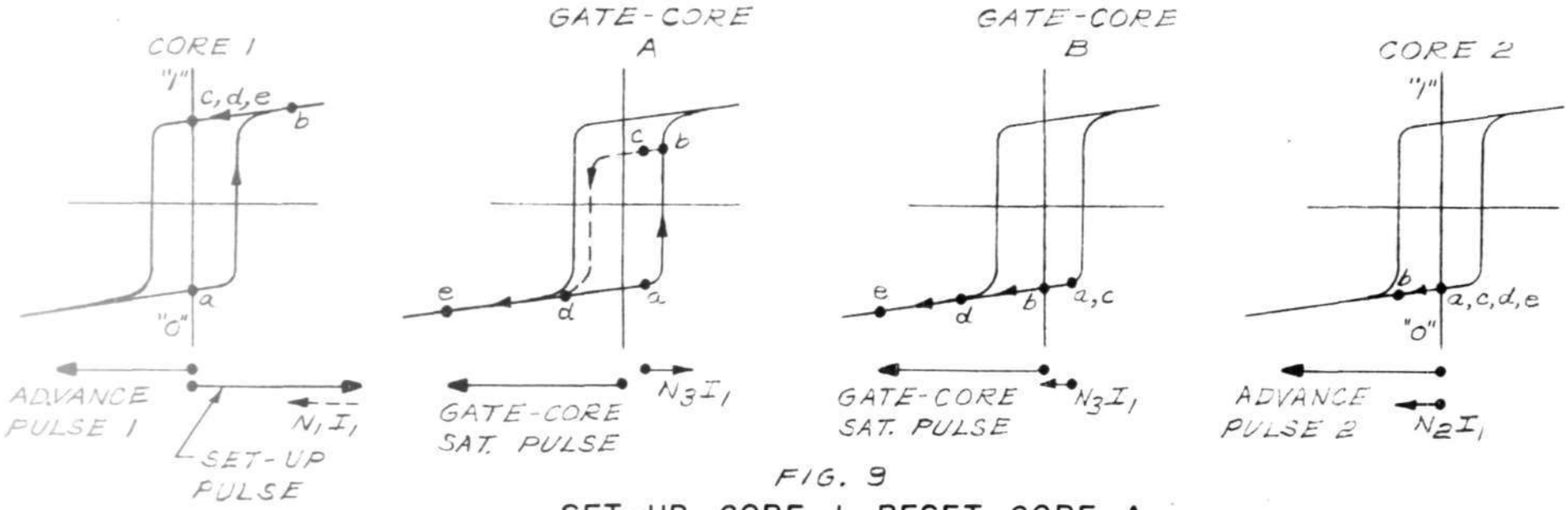

FIG. 9

SET-UP CORE 1, RESET CORE A

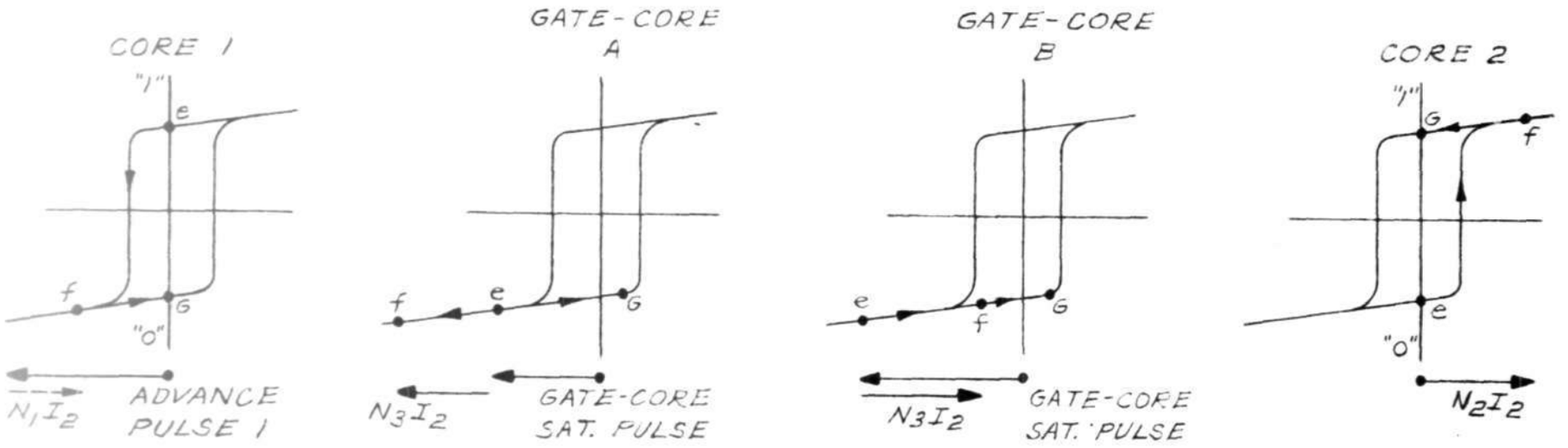

FIG. 10

TRANSFER OF "1" FROM CORE 1 TO CORE 2

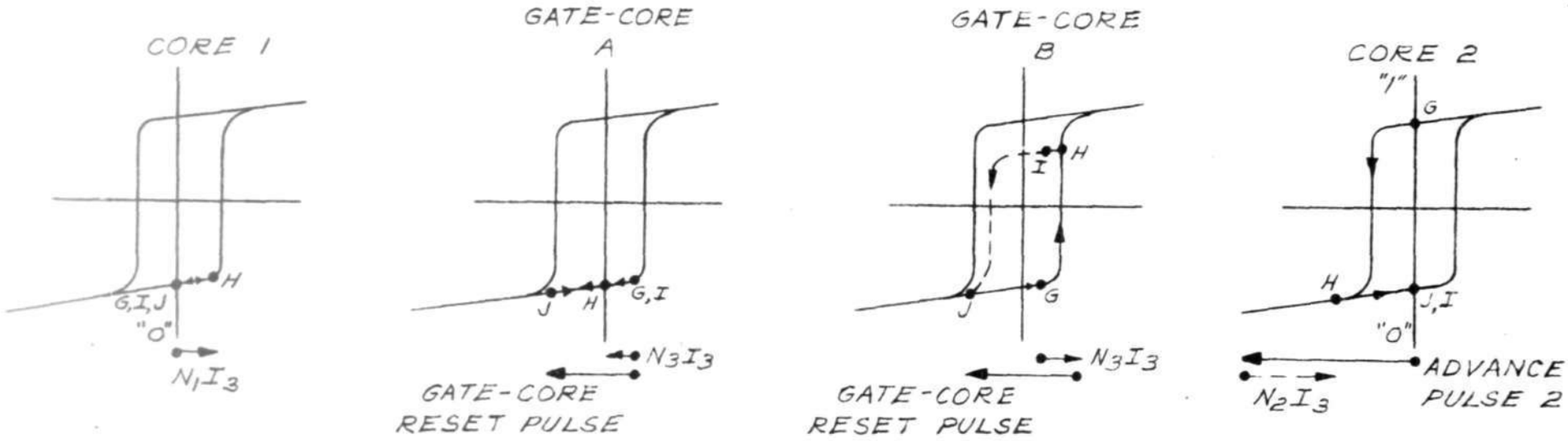

FIG. 11

READ-OUT "1" FROM CORE 2 AND RESET CORE B

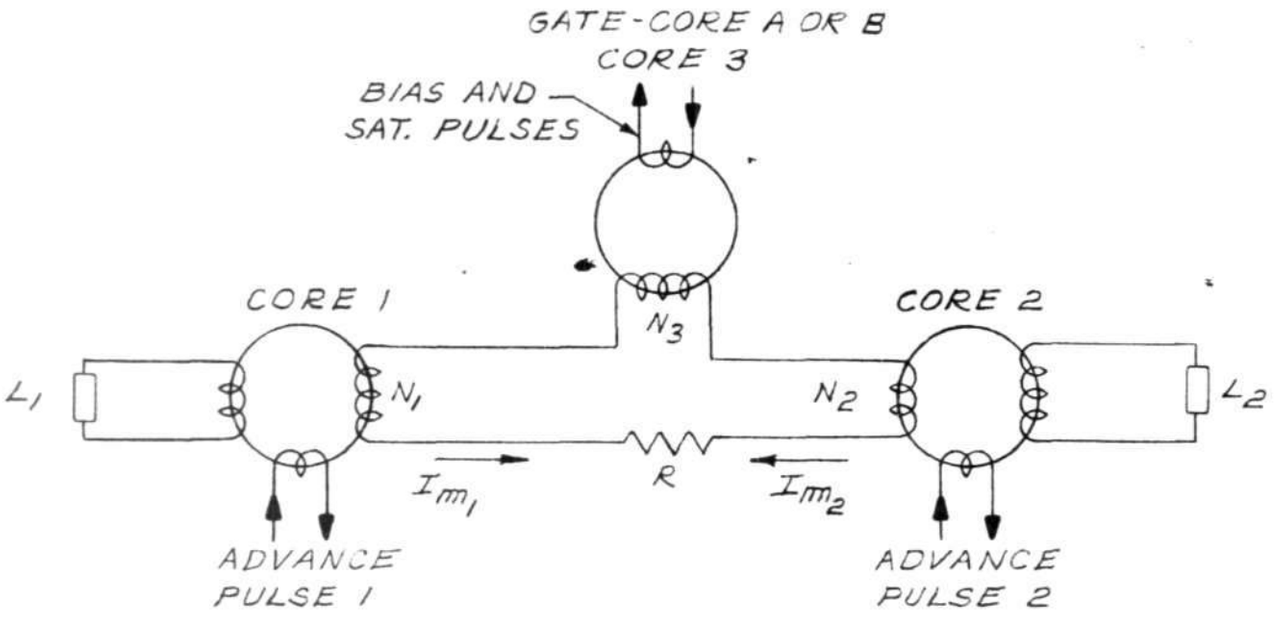

FIG. 12

GENERALIZED DIAGRAM OF CIRCUIT

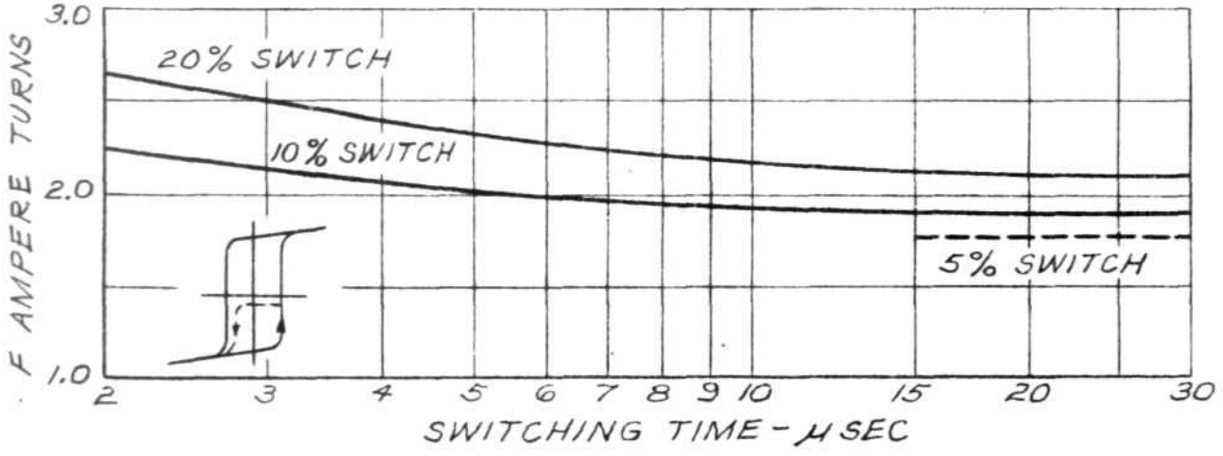

FIG. 13

F VS. SWITCHING TIME FOR PARTIAL SWITCHING OF A FERRITE CORE MF-1118 (F-259)