Microdata
1600/30 Computer

GENERAL DESCRIPTION

The Microdata 1600/30 computer is a member of Microdata's newest, advanced family of minicomputers, offering economy, high speed, microprogrammed architecture and flexibility through which the user can tailor the machine to his specific requirements.

The 1600/30 has all of the standard features of Microdata's 1600/20 and 1600/21 computers. In addition to being upwards compatible, it operates 40 percent faster than either of those models.

Efficient utilization of core memory and high throughput are achieved by the use of a large repertoire of macro instructions. High-speed read-only control memories reduce the number of CPU circuits which otherwise would be needed for 1600/30 instructions. The system uses TTL monolithic integrated circuits, including a large number of medium and large-scale integration types.

Modular design of core memory, read-only memory, processor options and input/output elements permits inexpensive system expansion within the compact basic enclosure.

STANDARD FEATURES

- Variable precision operations
- Character/string manipulation
- Stack processing
- Memory addressing to 32,768 bytes
  - 4096 and 8192 byte plug-in memory modules
  - 32,768 bytes of memory in basic enclosure
  - 1.0 microsecond memory cycle time
- Six operational registers
  - Accumulator (1) — 16 bits
  - Auxiliary accumulator (B) — 16 bits
  - Index register (X) — 16 bits
  - Program counter (P) — 15 bits
  - Overflow (O) — 1 bit
  - Word length control (W) — 2 bits

- Extensive, powerful instruction set including 110 different operations:
  - Control (16)
  - Multi-bit arithmetic and logical shifts (12)
  - Conditional jumps (17)
  - Input/Output (6)
  - Inter-register (19)
  - Stack control (8)
  - Character string manipulation (5)
  - Multiply/divide (2)
  - Decimal arithmetic (add and subtract instructions) (2)
  - Memory reference including jump, compare and variable word length operations (21)
  - Dual CPU communication (2)
- Eight operand addressing modes, including:
  - Direct to page 0 (first 256 bytes)
  - Direct relative to P (±128 bytes)
  - Indirect to page 0 (first 256 bytes)
  - Indirect relative to P (±128 bytes)
  - Indexed (to 32,768 bytes)
  - Indexed with bias (to 32,768 bytes)
  - Extended (to 32,768 bytes)
  - Literal (1 to 4 bytes in-line)
- Multi-precision 1, 2, 3 or 4-byte load, store and arithmetic operations
- Flexible I/O facilities including:
  - Programmed transfers to/from A register, B register and memory
  - Concurrent buffered I/O
  - Direct memory access
- Expandable priority interrupt system
- Standard power fail detect and automatic restart
- Standard Real-time clock
- Built-in bootstrap loader in nonvolatile read-only memory
- Standard software, including:
  - Loaders
  - Teletype debug and operating system
  - Two-pass assembler
  - Text editor
  - Single user BASIC
  - Diagnostics
- Power: 115/230 vac ±10%, 47 to 63 Hz, Average Configuration less than 400 watts
- Environment: 0 to 50°C
- Dimensions: Deck-top configuration, 10.5 inches high, 19 inches wide, 20 inches deep

ORGANIZATION

Basic elements of the 1600/30 are operational registers, core memory, control section, input/output system and interrupt system.

REGISTERS

The computer contains six operational registers which are accessible to the programmer, occupying nine of the 15 registers in the primary file of the basic 1600 hardware. The remaining seven file

registers are used for internal operations and buffering and are not directly accessible. The secondary file, containing 15 additional general-purpose registers, are unused in the 1600/30. Special input/output systems and instruction augmentation may be specified employing the unused file registers.

CORE MEMORY

The magnetic core memory is organized into pluggable modules of 4096 or 8192 bytes each. It is byte addressable, each byte containing eight information bits. The standard version of the 1600/30 may be expanded to 32,768 bytes within the basic enclosure. Special implementations can be employed to accommodate up to 65,536 bytes. A direct memory access (DMA) port is standard. Selector and multiplexer channels are available as options which allow interfacing of peripheral devices directly with memory and providing transfer rates of up to 1 million bytes per second.

CONTROL SECTION

The control section and associated read-only memory (ROM) provide the operational architecture and basic instruction repertoire through a series of microprogrammed sequences which operate at 200 nanoseconds per command. The 1600/30 system architecture employs 1536 words (16-bit) of high-speed read-only memory. The read-only memory can be expanded to a total of 16,384 words.

INPUT/OUTPUT SYSTEM

Three types of Input/Output are available: Program-controlled transfer of data bytes via the Byte Input/Output Bus. Buffered concurrent transfer of data bytes via the Byte Input/Output Bus. Direct transfer to memory via the direct memory access (DMA) channel.

The Standard Byte I/O Bus provides a path for transfer of data, control, and status between the processor and external peripheral devices. The direct memory access (DMA) channel option communicates directly with memory for data transfers.

Concurrent Input/Output

The concurrent I/O allows for block transfers between the external device on the Byte I/O bus and memory, at an asynchronous rate up to 50,000 bytes per second. The transfers are fully automatic, and once started, proceed without program intervention. Concurrent I/O requests take priority over instruction execution.

INTERRUPT SYSTEM

The priority interrupt system provides for internal processor interrupts, I/O peripheral device interrupts, and groups of individual external interrupts, each with its own unique interrupt memory address and priority assignment.

External Interrupts

External interrupts originate with device controllers or interrupt modules on the Byte I/O bus. An interrupt module provides control of eight external interrupt signals. Device controllers may also generate interrupts to signify individual data transfers, end of operation, or error conditions.

The external interrupt system contains a single interrupt line, a priority line, and a select line. A device may initiate an interrupt request only if priority has been received from higher level interrupts on the priority chain. Devices not requiring interrupt service will propagate priority to the next device in line.

Internal Interrupts

Internal interrupts are supplied as part of the basic 1600/30 system, and have priority over external interrupts. Internal interrupts are established for system features such as console interrupt, power fail/restart and real-time clock.

Console

The standard console interrupt is triggered by a switch on the console, allowing an operator to exert control.

Real-Time Clock

The real-time clock interrupt occurs when a preset clock count in a unique memory location is incremented to zero. The clock count location is automatically advanced at each one-millisecond clock time. The real-time clock interrupt is enabled and disabled under program control.

Power Fail and Automatic Restart

The power-fail interrupt provides an interrupt when a loss of primary power is detected. A minimum of one millisecond of computer operation is assured after the interrupt. The power restart interrupt occurs when the power is applied and is up to normal operating levels and the processor is placed in the run mode.

INSTRUCTION REPERTOIRE

Control

The control-group instructions are single byte instructions which provide specific control functions.

Code	Mnemonic	Description
00	HLT	HALT
01	TRP	TRAP
02	ESW	ENTER SENSE SWITCHES
04	DIN	DISABLE INTERRUPT SYSTEM
05	EIN	ENABLE INTERRUPT SYSTEM
06	DRT	DISABLE REAL TIME CLOCK
07	ERT	ENABLE REAL TIME CLOCK
08	RO1	RESET OVERFLOW AND SET WORD LENGTH TO 1
09	RO2	RESET OVERFLOW AND SET WORD LENGTH TO 2
0A	RO3	RESET OVERFLOW AND SET WORD LENGTH TO 3
0B	RO4	RESET OVERFLOW AND SET WORD LENGTH TO 4
0C	SO1	SET OVERFLOW AND SET WORD LENGTH TO 1
0D	SO2	SET OVERFLOW AND SET WORD LENGTH TO 2
0E	SO3	SET OVERFLOW AND SET WORD LENGTH TO 3
0F	SO4	SET OVERFLOW AND SET WORD LENGTH TO 4
34	NOP	NO OPERATION

Conditional Jumps

The conditional jump instructions are a two-byte format. The first byte provides the operation code which includes the condition being tested and whether the jump will be made on the condition being true or false. The second byte contains an 8-bit signed value which specifies a jump location relative to the program counter which holds the address of the next instruction to be executed.

Code	Mnemonic	Description
10	JOV	JUMP IF OVERFLOW SET
11	JAZ	JUMP IF A EQUAL TO ZERO
12	JBZ	JUMP IF B EQUAL TO ZERO
13	JXZ	JUMP IF X EQUAL TO ZERO

14	JAN	JUMP IF A NEGATIVE
15	JXN	JUMP IF X NEGATIVE
16	JAB	JUMP IF A EQUALS B
17	JAX	JUMP IF A EQUALS X
18	NOV	JUMP IF OVERFLOW NOT SET
19	NAZ	JUMP IF A NOT EQUAL TO ZERO
1A	NBZ	JUMP IF B NOT EQUAL TO ZERO
1B	NXZ	JUMP IF X NOT EQUAL TO ZERO
1C	NAN	JUMP IF A NOT NEGATIVE
1D	NXN	JUMP IF X NOT NEGATIVE
1E	NAB	JUMP IF A NOT EQUAL TO B
1F	NAX	JUMP IF A NOT EQUAL TO X
5A	JEP	JUMP IF EVEN PARITY

Shifts

The shift group of instructions provides both arithmetic and logic shifts of A Register, B Register, and A and B Registers together. A signed shift count is specified in the second byte of the instructions.

Code	Mnemonic	Description
20	LLA	LOGICAL LEFT A
21	LLB	LOGICAL LEFT B
22	LLL	LOGICAL LEFT LONG
24	LRA	LOGICAL RIGHT A
25	LRB	LOGICAL RIGHT B
26	LRL	LOGICAL RIGHT LONG
28	ALA	ARITHMETIC LEFT A
29	ALB	ARITHMETIC LEFT B
2A	ALL	ARITHMETIC LEFT LONG
2C	ARA	ARITHMETIC RIGHT A
2D	ARB	ARITHMETIC RIGHT B
2E	ARL	ARITHMETIC RIGHT LONG

Extended Arithmetic

The extended arithmetic instructions provide for signed variable-length decimal addition and subtraction with up to 16 digits of accuracy. The decimal add and subtract instructions are single-byte format employing the use of B Register and X Register as pointers to variable-length data to be processed. Multiply and divide are three-byte format instructions operating on 16-bit binary values.

Code	Mnemonic	Description
3C	DAD	DECIMAL ADD
3D	DSB	DECIMAL SUBTRACT
3E	MUL	MULTIPLY
3F	DIV	DIVIDE

Register Operate

The register operate group of single byte instructions provides for special arithmetic and logical operations on individual registers and between registers.

Code	Mnemonic	Description
40	ORA	OR B WITH A
41	XRA	EXCLUSIVE-OR B WITH A
42	ORB	OR A WITH B
43	XRB	EXCLUSIVE-OR A WITH B
44	INX	INCREMENT X
45	DCX	DECREMENT X
46	AWX	ADD WORD LENGTH TO X
47	SWX	SUBTRACT WORD LENGTH FROM X
48	INA	INCREMENT A
49	INB	INCREMENT B
4A	OCA	ONE'S COMPLEMENT A
4B	OCB	ONE'S COMPLEMENT B
4C	TAX	TRANSFER A TO X
4D	TBX	TRANSFER B TO X
4E	TXA	TRANSFER X TO A
4F	TXB	TRANSFER X TO B
58	MST	MULTIPLY STEP
59	ADC (ADX)	ADD TO X
5B	EBX	EXCHANGE B AND X

Stack Control

The stack control group of instructions provides for CPU context switching of all active registers to and from a designated stack. The stacking capability of the 1600/30 is efficient in processing multiple external interrupts and in employing reentrant coding techniques.

Code	Mnemonic	Description
50	RTN	RETURN
51	CAL	CALL
52	PLX	PULL X
53	PSX	PUSH X
54	PLA	PULL A
55	PSA	PUSH A
56	PLB	PULL B
57	PSB	PUSH B

Character/String Manipulation

The character/string manipulation group of instructions provides the capability to process both individual characters and strings of characters in a manner compatible to common Input-Output operations and communications processing.

Code	Mnemonic	Description
35	CLC	COMPARE LOGICAL
5C	MOV	MOVE
5D	GCC	GENERATE CYCLIC CODE
5E	SCH	SEARCH
5E	SCH	SEARCH NOT
5F	GAP	GENERATE ASCII PARITY

Memory Reference

The 21 instructions of the memory reference group obtain their operands from memory. The operand memory location is addressed by one of eight modes. The number of bytes required for the instruction depends on the addressing mode and the length of the operand. The return jump through X instruction always uses the extended mode of addressing.

Code	Mnemonic	Description
30	RTX	RETURN JUMP THROUGH X
60	JMP	JUMP
68	RTJ	RETURN JUMP
70	IWM	INCREMENT WORD IN MEMORY
78	DWM	DECREMENT WORD IN MEMORY
80	LDX	LOAD X
88	STX	STORE X
90	LDB	LOAD B
98	STB	STORE B
A0	ADA	ADD TO A
A8	ADV	ADD VARIABLE
B0	SBA	SUBTRACT FROM A
B8	SBV	SUBTRACT VARIABLE
C0	CPA	COMPARE A (LESS THAN, EQUAL TO, GREATER THAN
C8	CPV	COMPARE VARIABLE (LESS THAN, EQUAL TO, GREATER THAN
D0	ANA	AND
D8	ANV	AND VARIABLE
E0	LDA	LOAD A
E8	LDV	LOAD VARIABLE
F0	STA	STORE A
F8	STV	STORE VARIABLE

Dual CPU

These two instructions should only be used in a dual CPU configuration. They provide for communication between two CPUs either in core memory or by internal interrupts.

Code	Mnemonic	Description
23	TNS	TEST AND SET
27	GAI	GENERATE ALTERNATE INTERRUPT

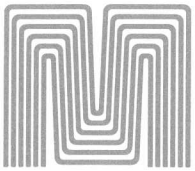
Byte Input/Output Instructions

Byte programmed Input/Output operations provide transfer of data, control and status over the Byte I/O channel. This channel permits intermixed program and concurrent I/O transfers. Up to 32 devices on the bus may be operating in the Byte I/O or concurrent block transfer mode at the same time.

Code	Mnemonic	Description
31	IBA	INPUT BYTE TO A
32	IBB	INPUT BYTE TO B
33	IBM	INPUT BYTE TO MEMORY
39	OBA	OUTPUT BYTE FROM A
3A	OBB	OUTPUT BYTE FROM B
3B	OBM	OUTPUT BYTE FROM MEMORY

SYSTEM ELEMENTS AND OPTIONS

Item	Description
Packaging	
2001	Rack mountable enclosure including fan
2002	Desk-top enclosure
2004	63-inch equipment cabinet and enclosures
Magnetic Core Memory	
2204	4096-byte (8-bit) core memory module
2208	8192-byte (8-bit) core memory module
General Purpose and Utility Interfaces	
2501	General purpose I/O wire-wrap board including 72 sockets (16 pin) and six 24-pin sockets occupying one I/O slot.
2510	Byte I/O controller provides independent input controller and output controller each with 8-bit data transfers operating in the programmed concurrent I/O or interrupt modes.
2511	Full word I/O interface provides 32 input lines and 32 output lines; data transfers are under program control.
2514	Selector channel; operates via direct memory access (DMA), will accommodate up to four I/O devices.
2515	Multiplexer channel; operates via direct memory access (DMA), provides for simultaneous operation of up to four I/O devices.
Communications Interfaces	
2600	Synchronous modem interface; provides independent control for transmission and receiving elements of synchronous modems operating up to 9600 baud. Each control element includes programmed, concurrent I/O and interrupt data transfer modes. The unit will accommodate programmed sync pattern, 5-, 6-, 7- or 8 bit character size. Interface signals are EIA standard RS-232-C.
2610	Asynchronous communications controller for 103 and 202 Data Sets or 20 ma current loop teletype. Single channel, full duplex, programmable baud rates (75 to 9600 baud), character lengths, stop bits, and parity error checking.
2613	Asynchronous modem interface provides simultaneous operation of eight full duplex channels for type 103 and 202 data sets. Each channel is programmable for baud rates (75 to 9600 baud), character length, stop bits, and parity error checking.
2614	Asynchronous communications controller provides simultaneous operation of eight full duplex asynchronous channels. Each channel can select, by switch or jumpers, one of ten standard baud rates (75 to 9600 baud), one of four character lengths, 1 or 2 stop bits and parity error checking. EIA Standard RS-232-C or teletype 20 ma current loop.
2630	Automatic call unit controller provides control functions for four Bell Model 801 Automatic Call Units, EIA Standard RS-232-C interface levels.
Peripheral Systems	
2710	Paper tape system — 300 cps paper tape reader, 75 cps paper tape punch, I/O controller, and interconnecting cables. Unit is rack mountable requiring 10.5 inches of rack space. Reader and punch use standard 8-channel fanfold paper or mylar tape.
2720	Card reader system — card reader, controller and interconnecting cable. 300 cpm, 80-column cards, 1000-card input hopper, 1000-card output stacker.
2732	Line printer system — line printer, controller, and interconnecting cable. 245 eight channel VFU optional lpm, 132 columns, 64-character set.
2811	Magnetic tape system — one tape transport, I/O controller which will accommodate up to four transports and interconnecting cables; 9-track, 25 ips, 800 bpi, 7 inch reel, read/write dual-gap head, 20,000 bytes/second transfers via concurrent I/O channel.
2821	Magnetic tape transport (add-on unit for 2811 system), 9-track, 25 ips, 800 bpi, 7 inch reel, read/write dual-gap head.
2821-7	Magnetic tape transport (add-on unit for 2811 system), 7-track, 25 ips, 800 bpi, 7 inch reel, read/write dual-gap head.
2852	Disc memory system — moving-head disc drive unit (one fixed and one removable disc), I/O controller, interconnecting cables, and 63 inch cabinet for mounting. Random access time 95 ms (average), 4.9 million byte capacity, 200,000 bytes per second transfer rate. Requires DMA selector channel.
Standard Software Packages	
MAP1630	Machine language symbolic assemblers for use on 1600/30 computer.
TOS	Teletype operating system.
TED	Tape editor.
Diagnostics	CPU, memory and peripheral interface diagnostics for 1600/30 computer.
I/O Drivers	Callable subroutines are provided for all system I/O devices.
BASIC	Single user BASIC interpreter.



™ **Microdata**

Microdata Corporation
17481 Red Hill Avenue
Irvine, California 92705
(714) 540-6730 TWX: 910-595-1764