1	GND	2	GND
3	+12V	4	+12V
5	+12V	6	+12V
7	-12V	8	-12V
9	DPIN	10	DPOT
11		12	
13	+5V	14	+5V
15	MST	16	
17	MACK	18	RD
19	TYP1	20	SLB
21	PFD	22	MDIS
23	AB08	24	AB09
25	AB10	26	AB11
27	GND	28	GND
29	AB12	30	AB13
31	AB14	32	AB15
33		34	
35	STOP	36	SACK
37	MBIN	38	MBOT
39	DB00	40	DB01
41	DB02	42	DB03
43	+5V	44	+5V
45	DB04	46	DB05
47	DB06	48	DB07
49	DB08	50	DB09
51	DB10	52	DB11
53	DB12	54	DB13
55	DB14	56	DB15
57	EXEC	58	IN
59	GND	60	GND
61	IOCL	62	OUT
63	CLK	64	SER
65	IUR	66	IL1
67	IAR	68	IL2
69	RST	70	IUA
71	PLSE	72	ECHO
73	+5V	74	+5V
75	AB03	76	AB04
77	AB05	78	AB06
79	AB07	80	AB00
81	AB01	82	AB02
83	PRIN	84	PROT
85	GND	86	GND

AB##	Address Bus
DB##	Data Bus
	I/O Operation Signals
	Utility Signals
	Interrupt Signals
	DMA Signals

Signal	Description	Direction
MBIN	Memory bank control in	
MBOT	Memory bank control out	
EXEC	Instruction is "Select" or "Select and Present"	P --> I
IN	Instruction is "Input"	P --> I
OUT	Instruction is "Output"	P --> I
PLSE	Interface strobe	P --> I
RST	Reset all interfaces	P/C --> I
CLK	1Mhz timing reference	P --> I
TYP1	Type-1 processor installed	P --> I
SER	Interface controller status	P <-- I
IUR	Interrupt request	P <-- I
IOCL	Synchronize IUR into the processor	P --> I
PRIN	Interrupt priority in	I <-> I
PROT	Interrupt priority out	I <-> I
IUA	Interrupt acknowledge	P --> I
IAR	Interrupt address request	P --> I
ECHO	Transfer Complete	P --> I
IL1	Non-maskable interrupt (Vector 0002)	P <-- I
IL2	Non-maskable interrupt (Vector 0006)	P <-- I
DPIN	DMA priority in	I <-> I
DPOT	DMA priority out	I <-> I
STOP	Stop processor	P <-- I
SACK	Stop acknowledge	P --> I
PFD	Power failure detected	PSU --> System
SLB	Select least-significant byte	P/I --> I/M
MST	Memory start	P/I --> M
RD	Read mode	P/I --> M
MACK	Memory acknowledge	P/I <-- M

All signals are active-low!