MEMOREX

660-1
Disc Storage Drive
Maintenance Manual

660-1.20-00

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INTRODUCTION

1.1 GENERAL

The Memorex 660-1 Disc Storage Drive is a direct access disc storage unit. It reads and writes information on Memorex Mark VI, IBM 2316, or equivalent disc packs.

The disc pack serves as permanent or temporary information storage media which can be written on by one drive, removed and stored, and then installed on another drive with no loss of compatibility.

To record (write) and recover (read) information, a disc pack is installed on a 660-1 disc drive. The drive is responsible for performing the three basic operations: seek, read, and write. To do this, it rotates the disc pack at the required speed (2400 rpm ±2%), selects one of 20 read/write heads for an operation, and positions it to the prescribed track on the disc surface (all 20 heads position to the same cylinder simultaneously, but only one head is selected to read or write at a time). The drive allows the controller to synchronize read/write operations by referencing to an index on the disc pack.

The 660-1 drive receives commands and data from the central processing unit through a controller. Up to eight drives can communicate with the same controller. Figure 1-1 is a simple block diagram showing the system configuration when more than one drive is connected to a single controller.

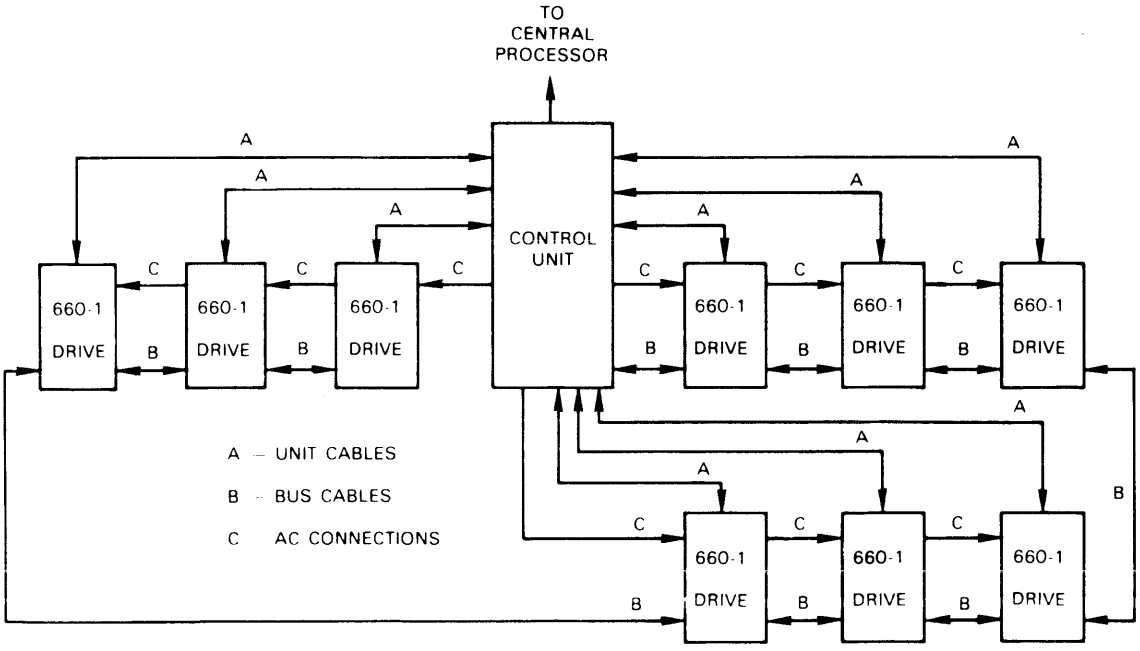


FIGURE 1-1. SYSTEM CONFIGURATION

AC power is supplied externally and, in the typical installation, also comes from the controller (as shown in Figure 1-1). There are two configurations of the 660-1 drive (A and B) to accommodate either 60- or 50-Hz power supplies. Details of AC power requirements are given in Section 2.3.2.1.

The 660-1 drive includes a self-contained DC power supply and does not depend on the controller for DC power (except for special termination power which is supplied by the DC line from the controller).

Standard voltage levels on 660-1 interface connectors are +5 volts for logical zero and 0 volts for logical one. Exceptions to this are identified in the appropriate pin connection lists in Section 2.3.2.

1.2 STORAGE MEDIA

Memorex Mark VI, IBM 2316, or equivalent disc packs serve as the storage media for the drive. Figure 1-2 shows the recording discs, slotted index disc on the bottom of the pack, and top and bottom protective pack covers.

Each pack consists of eleven aluminum discs which are coated with a magnetic oxide and mounted 0.4 inches apart on a common hub. Information is recorded on the 20 inner disc surfaces in the form of polarized magnetic particles called bits. The bits are recorded on 203 concentric circles (track 000 to track 202) on each disc surface. Since corresponding tracks on all 20 surfaces are vertically aligned, they are considered information cylinders: there are 203 cylinders per pack. Cylinders 200, 201, and 202 are ordinarily reserved as spares under the control of initialization routines.

A Memorex Mark VI or IBM 2316 disc pack is installed on a drive by raising the cabinet cover and lowering the disc pack onto the spiindle. The disc pack is secured to the spindle by twisting the pack's handle clockwise. When the disc pack is secured, its cover can be removed, the cabinet cover closed, and the machine started by pressing the START switch on the operator control panel. Interlocks prevent the drive motor from starting until the pack cover has been removed and the cabinet cover closed.

1.3 BASIC DRIVE OPERATIONS

1.3.1 Seek

1.3.1.1 First Seek (To Cylinder 000)

When the START switch on the operator control panel is pressed (assuming that the drive is connected to a controller and that its main power switch is closed), power is supplied to the spindle drive motor and the disc pack begins rotating. Once the discs reach 70% of the rated speed, the 20 read/write heads are positioned to cylinder 000 (home position) in a first seek sequence. This begins with a forced forward seek which is not completed as in a normal seek. Instead, the carriage moves all the way out to the forward stop and when it comes to rest against the forward stop, it makes a normal reverse seek to home position (cylinder 000).

After the detent engages, the drive signals the controller that it is ready for further instructions. Normally, this would mean a seek command to some cylinder where one head would be selected to read or write information.

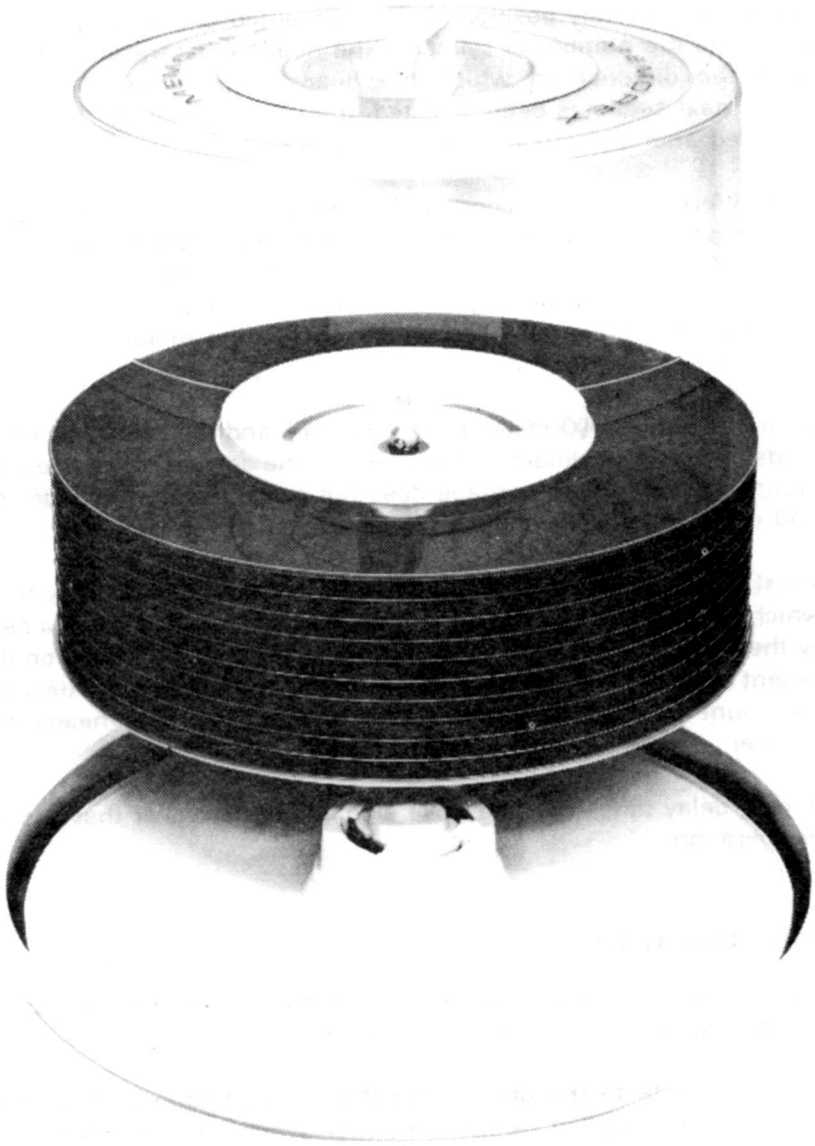


FIGURE 1-2. MEMOREX MARK VI DISC PACK

1.3.1.2 Seeks Other Than First Seek

The controller initiates a seek by sending the address of the cylinder scheduled for the next seek to the drive where that address is compared with the address of the cylinder at which the heads are presently positioned. The computed difference between the two addresses represents the number of cylinders the heads must travel. Comparison logic also determines the direction in which the heads must move. Once the cylinder scheduled for the next seek has been selected, the controller sends the address of the head to be selected after the proper cylinder is reached.

Meanwhile, the difference count is converted by the drive into an analog voltage which powers the linear positioning motor. Before the difference count voltage reaches the linear positioning motor, it is compared with a speed sense voltage supplied by a tachometer located in the positioning motor. This comparison is made by a servo amplifier to control the voltage supplied to the positioning motor so that the access speed of the heads is controlled.

The detent is then picked, a 100-msec delay is started, and the linear positioning motor moves the heads to the new cylinder. The purpose of the delay is to provide a time check on the positioning system. If the carriage does not reach the new cylinder and detent within the 100 msec, a seek incomplete signal is sent to the controller.

During a normal seek, the position of the heads is monitored constantly by a cylinder transducer which sends a pulse to the present address register each time a new cylinder is reached by the heads. Each pulse increases or decreases (depending on direction of travel) the present address by one, which causes the difference count to decrease. When the difference count reaches zero, the detent engages and the heads stop at the prescribed cylinder.

After the damping delay times out, the drive signals the controller that it is ready for a read or write operation.

1.3.2 Write Operation

Writing is performed by a magnetic recording head which flies close to the surface of the disc while the disc rotates rapidly under or over it.

The controller sends data to the drive using the double-frequency nonreturn-to-zero technique. Clock pulses supplied by the controller synchronize recording of the data pulses. Every 400 nsec (called a bit cell time) a clock pulse is recorded. If no other pulse is recorded between two clock pulses, that bit cell time represents a logical zero. Two pulses recorded during a bit cell time (one pulse each 200 nsec) represents a logical one.

The pulses are recorded as magnetic-flux reversals in a track 0.007-inches wide. Two erase poles, which follow the read/write gap by 0.005 inches, trim previously written data from the sides of a written track. This process is called side trimming and allows for deviation in head positioning by reducing fringe pickup from tracks adjacent to the one being used. The final width of a newly recorded track is 0.006 inches.

The data track remains on the disc surface where it can be read at any time until it is erased by new data.

1.3.3 Read Operation

The same head poles used to write the data track are used to read it. The magnetic-flux changes, recorded on the disc surface, cause current reversals in the two center-tapped read coils. The current reversals are converted to an output signal which is transmitted to the controller. The recorded clock pulses serve as a built-in clock for the transmitted data.

SECTION 2
MACHINE DESCRIPTION

This section contains descriptions of the disc storage drive from three viewpoints: machine parameters, machine assemblies and parts, and functional areas.

2.1 MACHINE PARAMETERS

For machine parameters, see Table 2-1 on the following page. Data transfer timing is shown in Figure 2-1.

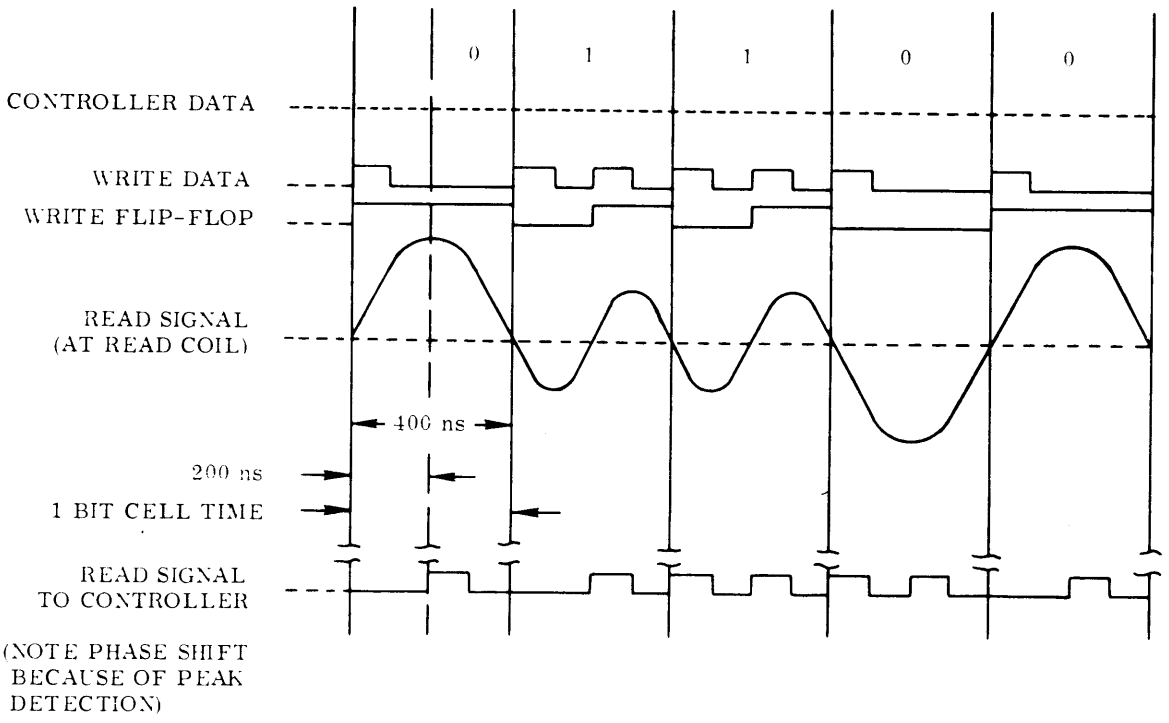


FIGURE 2-1. TIMING DIAGRAM

TABLE 2-1. BASIC MACHINE PARAMETERS

Capacity	
Maximum disc pack capacity, 8-bit bytes	29 million
Bits available to a single access	Over 576,000
Data Retrieval Times	
Rotational time	25 msec (2400 rpm ±2%)
Track-to-track position time	12 msec nominal*
Maximum access time	60 msec
Average access time**	35 msec
Readback data cell time	400 nsec, nominal
Read data pulse width	70 nsec, nominal; 85 nsec, maximum; 55 nsec, minimum
Bit shift (clock/data)	±90/±70 nsec
Recommended data separation method in control unit	VFO with 240 nsec clock window/160 nsec data window
Write Operation	
Technique	Double-frequency, nonreturn-to-zero
Density, track 000	1530 bits/inch (zero's rate), nominal
Density, track 202	2228 bits/inch (zero's rate), nominal
Data transfer rate	2.5 megabits/sec, nominal
Read Operation	
Double-frequency recording technique provides self-clocking read data	
Data is sent to controller as stream of binary bits	
Disc Pack Characteristics	
Recording discs	11
Recording surfaces	20
Tracks per surface	200 plus 3 spares
Recording disc's outside diameter	14.030 + 0.000 - 0.010 inches
Diameter of track 000	13.012 inches, nominal
Diameter of track 202	8.928 inches, nominal
Disc pack cover outside diameter	14.55 inches, maximum
Radial dimension of track 202 to reference	4.464 inches, nominal
Radial dimension of track 000 to reference	6.506 inches, nominal
Disc pack weight	14 lbs (approximate)
Coating material	Magnetic oxide
Heads	
Number of heads	20
Width of track as written	0.007 inches
Width of track when erased	0.006 inches
Track spacing center-to-center	0.010 inches
Operator Controls	ENABLE-DISABLE, READ/WRITE-READ ONLY, START-STOP
Overall Dimensions	
Width	30 inches
Depth	24 inches
Height	39 inches
Weight	395 lbs
Environment	
Temperature range	60°F to 90°F***, 70°F optimum
Relative humidity range	20% to 80%, 50% optimum
Maximum wet bulb temperature	78°F
Heat dissipation	4000 BTU/hr
Electrical Requirements	
Model A AC power	187-253 vac, 60 Hz
Model B AC power	187-253 vac, 50 Hz
Phase	Receive 3-phase, use single-phase
DC power supply	Self-contained, except for special termination requirements
Maximum start current	25 amps
Maximum run current	7.8 amps
Nominal current(208v)	5.0

*This figure does not include average latency time of 12.5 msec due to rotation.

**Average access time = $\frac{\text{time to do all possible seeks}}{\text{number of seeks possible}}$

***Temperature changes less than 15° per hour are acceptable.

2.2 MACHINE ASSEMBLIES AND PARTS (See Figure 2-2)

A. Linear positioning motor
B. Read/Write amplifier cards
C. Tachometer
D. Operator control panel
E. Running time meter
F. Air filter
G. Interior control panel (connector side)
H. Blower motor
I. DC power supply
J. Spindle drive motor
K. Interior control panel (access for maintenance)
L. Logic card file
M. Detent mechanism and cylinder transducer
N. Read/Write heads
O. Cam tower
P. Spindle
Q. Index transducer

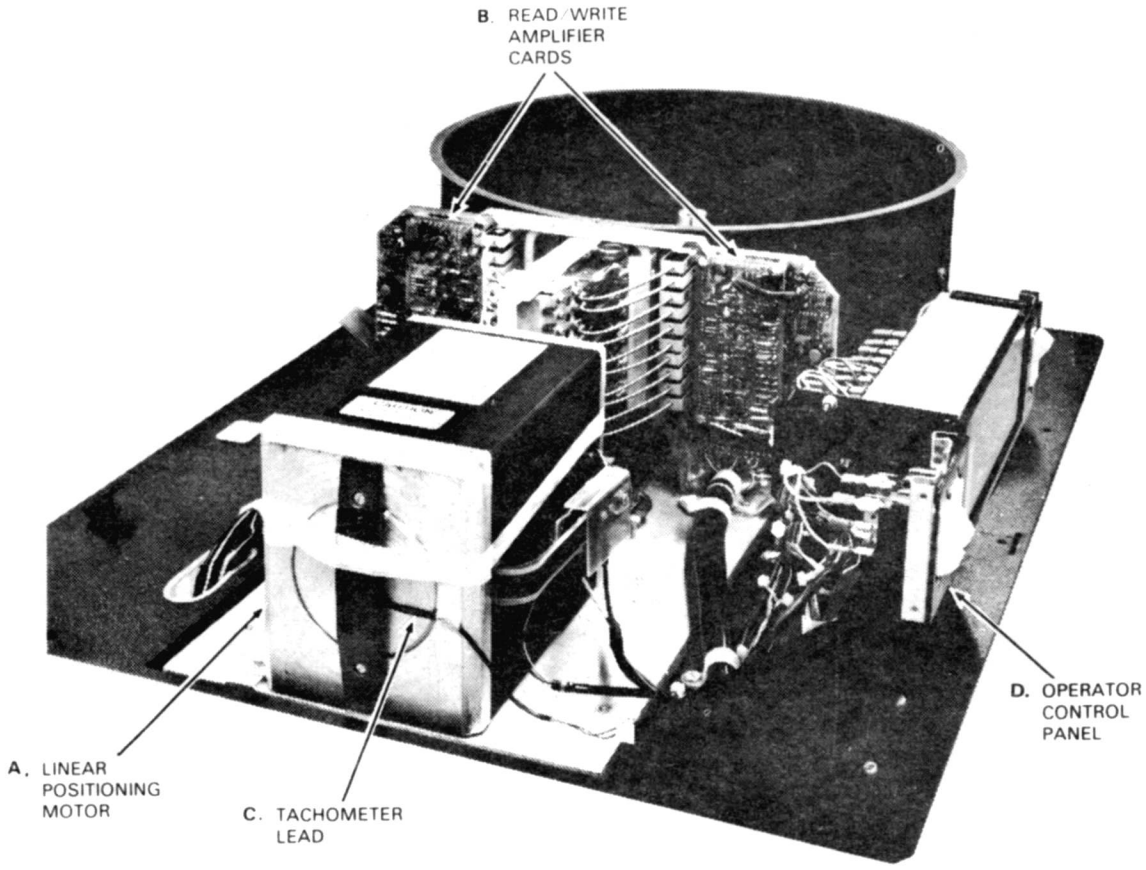


FIGURE 2-2. MACHINE ASSEMBLIES AND PARTS (Sheet 1 of 4)

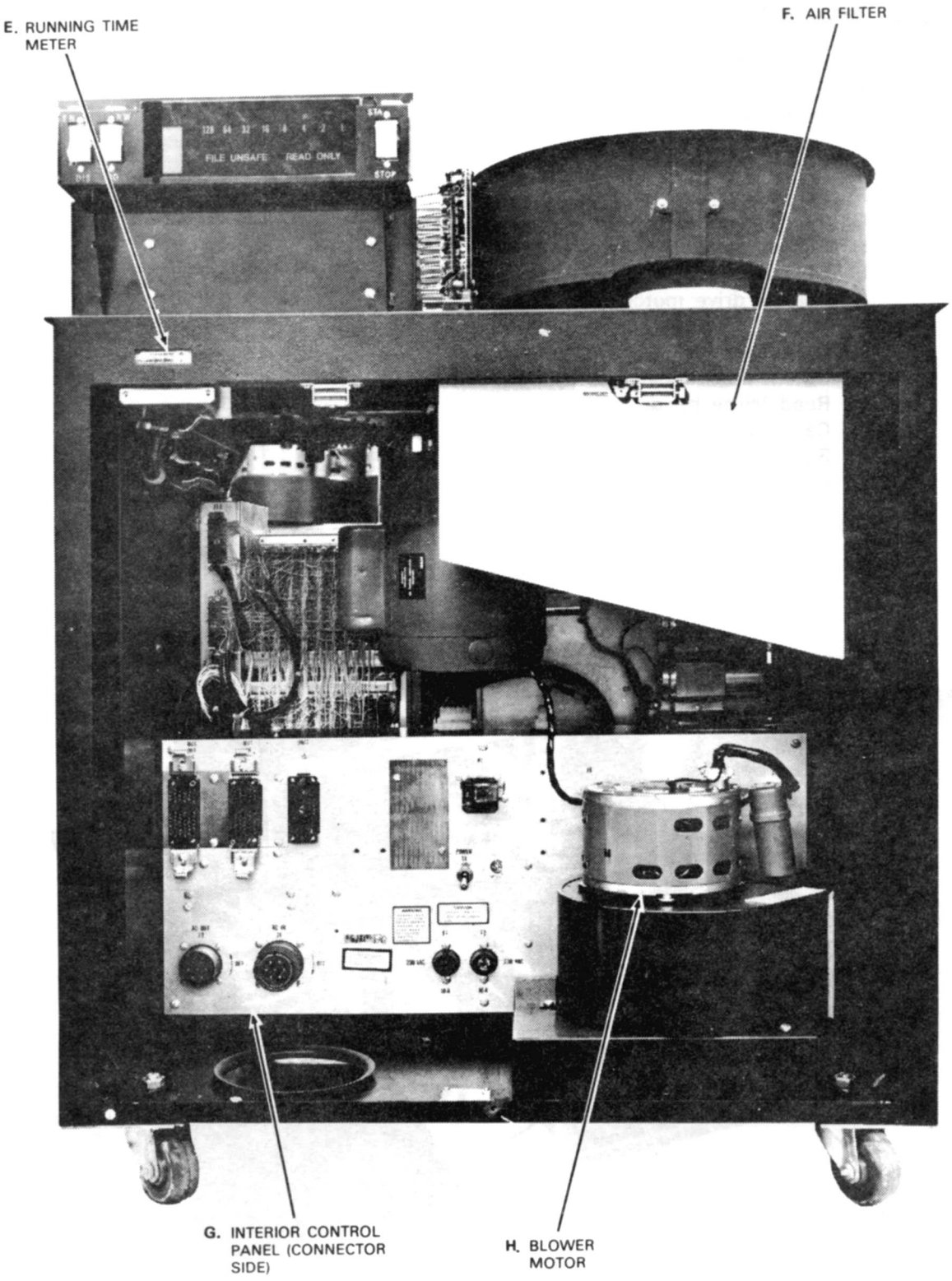


FIGURE 2-2. MACHINE ASSEMBLIES AND PARTS (Sheet 2 of 4)

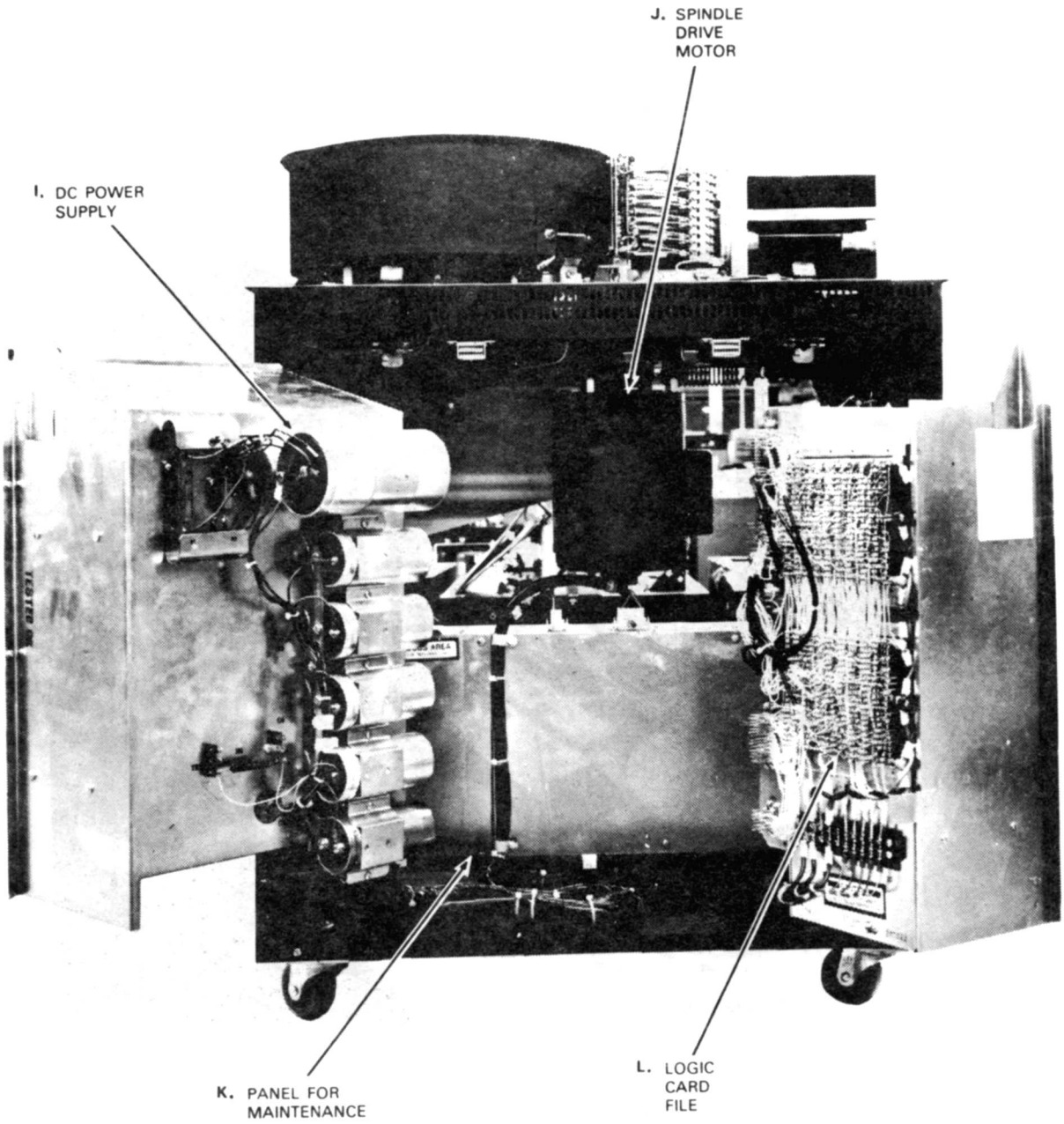


FIGURE 2-2. MACHINE ASSEMBLIES AND PARTS (Sheet 3 of 4)

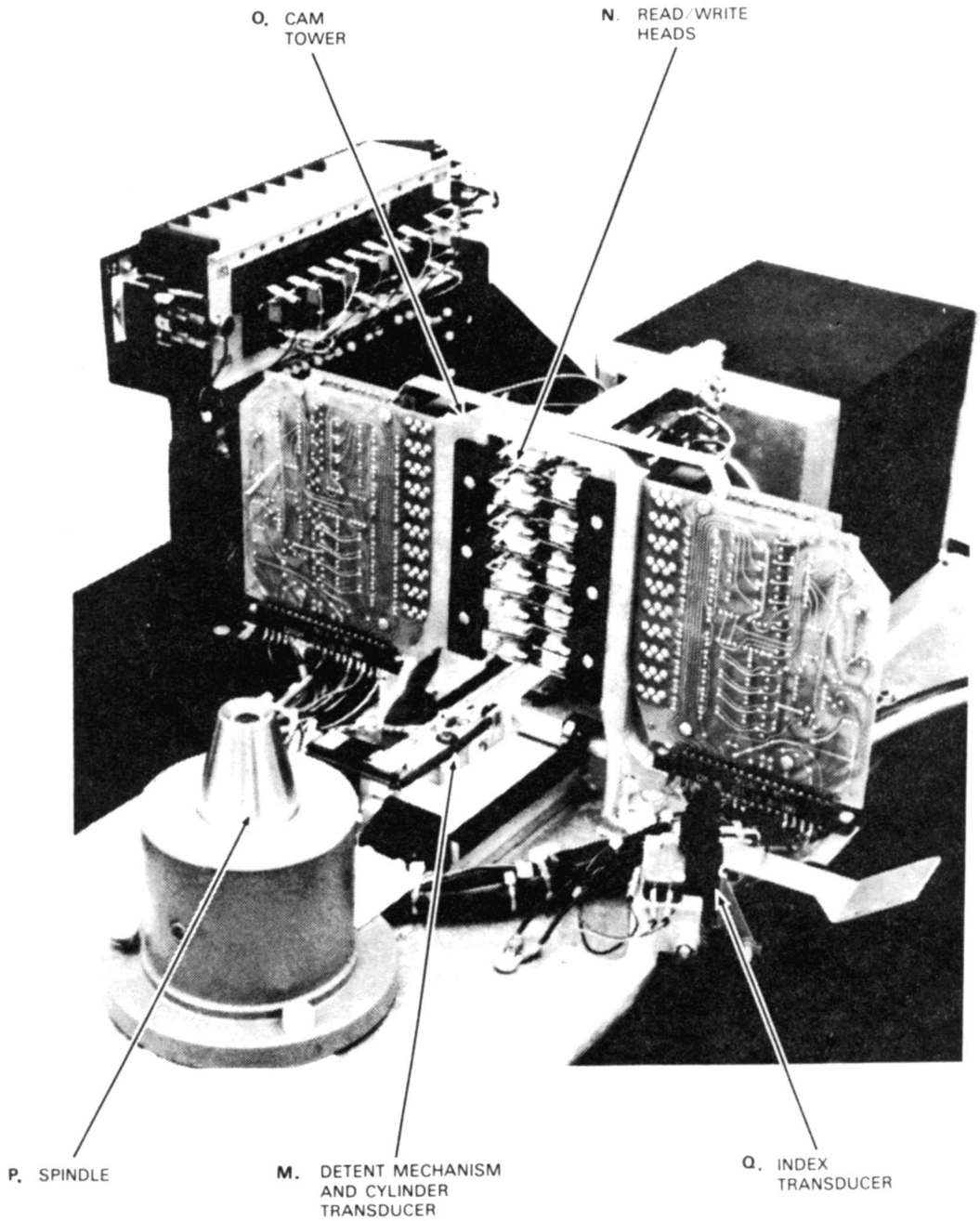


FIGURE 2-2. MACHINE ASSEMBLIES AND PARTS (Sheet 4 of 4)

2.3 FUNCTIONAL AREAS

The various assemblies and parts identified in Section 2.2 can be classified into five major functional areas.

A. Cabinet and cooling system
B. I/O interface
C. Operator control panel
D. Positioning and spindle drive mechanisms
E. Control circuitry

The disc pack, which is not an integral part of the drive, is described in Section 1.2.

2.3.1 Cabinet and Cooling System

2.3.1.1 Cabinet

The cabinet housing the unit is 30 inches wide, 24 inches deep, and 39 inches high. Figure 2-3 is a diagram showing cabinet dimensions and floor space needed for maintenance. A drive weighs approximately 395 pounds.

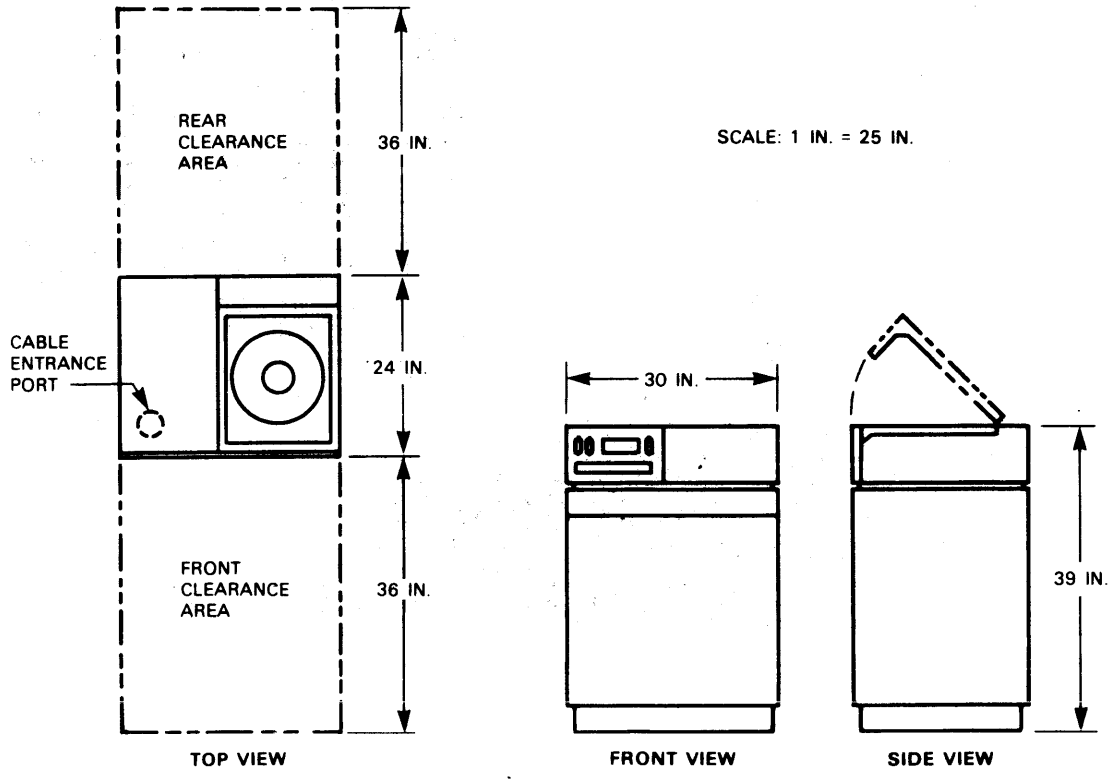


FIGURE 2-3. CABINET DIMENSIONS

Front and back covers are attached to the mainframe by magnetic strips which pull off for easy access to the cabinet's interior. The side panels and two top covers are also attached by magnetic strips. The kick panel on the front of the cabinet and the one on the back are each attached by two sheetmetal screws. The logic card file and DC power supply/servo assembly are housed in doors which swing out of the back of the cabinet on hinges (see Figure 2-4).

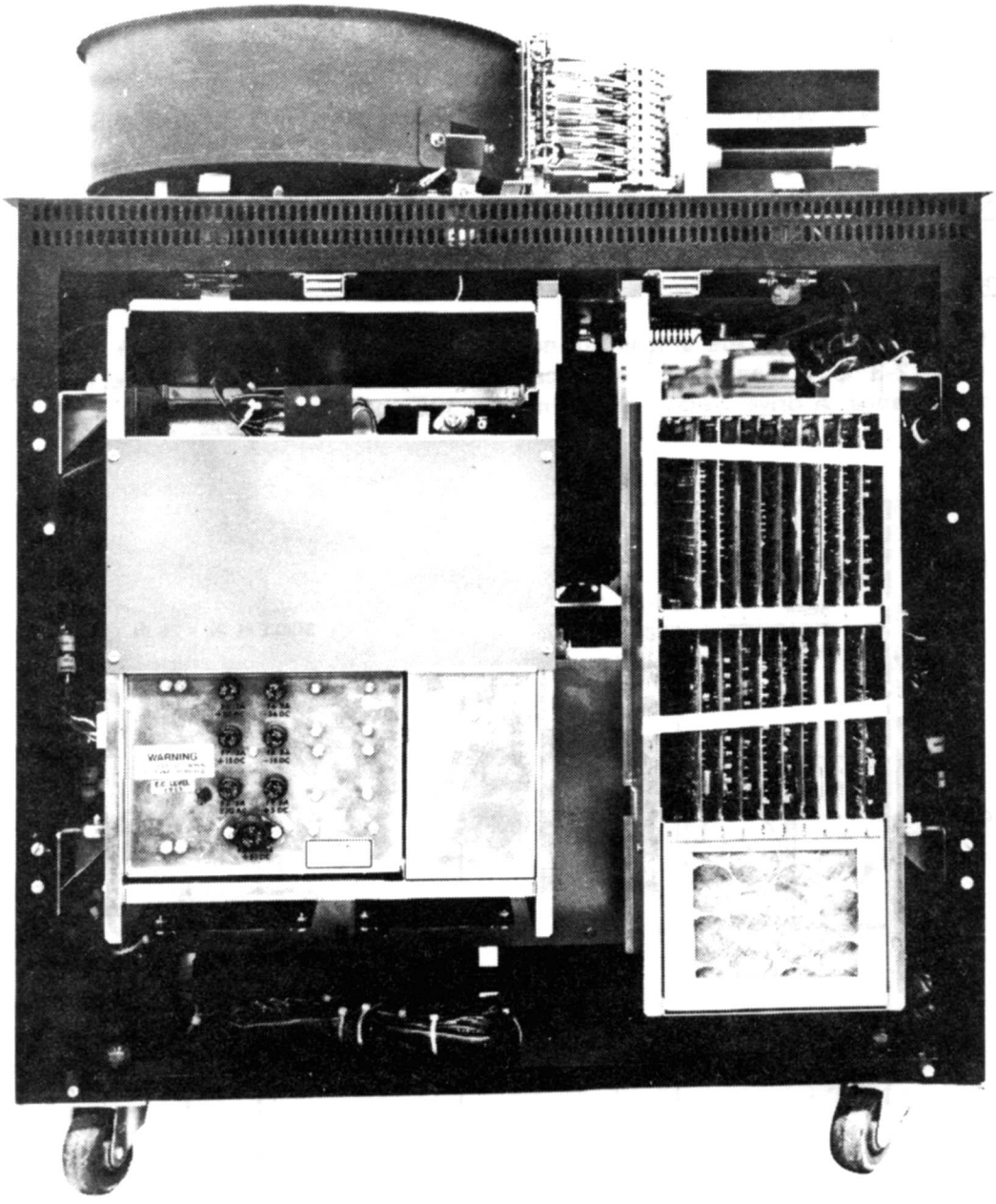


FIGURE 2-4. DC POWER SUPPLY AND LOGIC FILE DOORS

2.3.1.2 Cooling System

A squirrel-cage blower motor and three muffin fans are used for cooling the drive. The main blower is located on the floor of the cabinet just inside the front panel. Driven by a 1/8-horsepower motor, it pulls cool air into the cabinet through a filter. The air is then routed through a duct up the side of the cabinet and into the deckplate area. No air is forced into the disc pack itself. Disc rotation draws air from the duct in the cabinet side, through an absolute filter assembly, and into the shroud. From there, the air flows into the positioning motor area, and back down into the interior of the cabinet. A portion of this air is used to cool both the spindle drive motor and the blower motor.

The components within the power supply door are cooled by two muffin fans mounted near the bottom of the door. Air for cooling this assembly is a mixture of internal cabinet air and air drawn in through holes in the back cover plate of the main cabinet. This air is forced up over the power supply components and then exhausted out ports near the top of the cabinet.

The logic card file is similarly cooled except that only one muffin fan is used and its input air comes exclusively from vents in the back cover plate of the drive.

2.3.2 Input/Output (I/O) Interface

One or more 660-1 disc drives interface to the controller with two classes of cables, the bus cable and the unit cable.

The bus cable contains all signal lines which are common to all drives in the string. The bus cable supplied by Memorex consists of coaxial cables whose characteristic impedances are approximately 51 ohms each.

The unit cable contains all signals unique to the particular drive. The unit cable supplied by Memorex consists of six 95-ohm coaxial cables. A frame ground is also provided through the shield of this cable.

2.3.2.1 Power Requirements (AC and DC)

The following list defines the power requirements for the two basic Model 660-1 configurations (Model 660-1A and Model 660-1B).

Model	Voltage (vac)	Current (amp)	Frequency (Hz)
1A	187-253	25 (start); 5.0 (run)	60 ± 1/2
1B	187-253*	25 (start); 5.0 (run)	50 ± 1/2

*A wire change in the 660-1 is required when 380 vac is used.

Both configurations receive power via six-wire cables. The sixth wire serves as a chassis ground, and as a grounded neutral in areas where only 380-vac, 50 Hz Wye-connected power is available. When neutral is used, a terminal board change is required so that power is received from line-to-neutral (in a four-wire, 380 vac system, line-to-neutral is 220 vac). Neutral is normally not used in 60-Hz configurations.

AC power is supplied as three-phase, but the individual units draw current from only one phase. The phases are rotated (between in and out connectors) in a multiunit system to provide a balanced load. No more than three drives are jumpered together as a string so that each phase supplies power to only one drive.

DC power for the logic and control functions is provided by the unit itself. A self-contained DC power supply is located in the power supply/servo door at the back of the cabinet. The logic circuitry is discussed in the logic description section of Volume B.

Cable lengths should conform to the following specifications (refer to Figure 1-1).

Cable A - Separate run for each drive	50 ft (maximum)
Cable B - Jumper connection from drive to drive	100 ft (maximum accumulated)
Cable C - Jumper connection from drive to drive (maximum of three drives per group: eight per controller)	100 ft (maximum accumulated)

To satisfy electrical requirements in most areas of the United States, a maximum AC power cable length of 14 ft is recommended. (UL and local codes must be checked for each installation.)

2.3.2.2 Communication Lines

The communication lines illustrated in Figure 1-1 are identified in more detail in Figure 2-5. These lines can be listed in two basic categories, input and output.

Input (to 660-1 from controller)

A. Select Unit Line
B. Unit Bus Lines (eight)
C. Tag Lines (three)
D. Write Data Coaxial Line
E. Sequence In Line
F. Controlled Ground Line

Output (from 660-1 to controller)

A. Cylinder Address Register Lines (eight)
B. Attention Line
C. Unit Is Selected Line
D. Selected Unit Ready Line
E. Selected Unit On Line Line
F. Selected Unit Index Pulse Line
G. Selected File Unsafe Line
H. Selected Unit Seek Incomplete Line
I. Selected Unit End of Cylinder Line
J. Read Data Coaxial Line
K. Composite Index/Sector Pulse Line
L. Selected Unit Read Only Line
M. Selected Unit Write Current Sense Line
N. Heads Extended Line (common to all drives)
O. Sequence Out Line
P. Selected Unit Sector Pulse Line

Detailed descriptions of the above lines are included in Section 4.

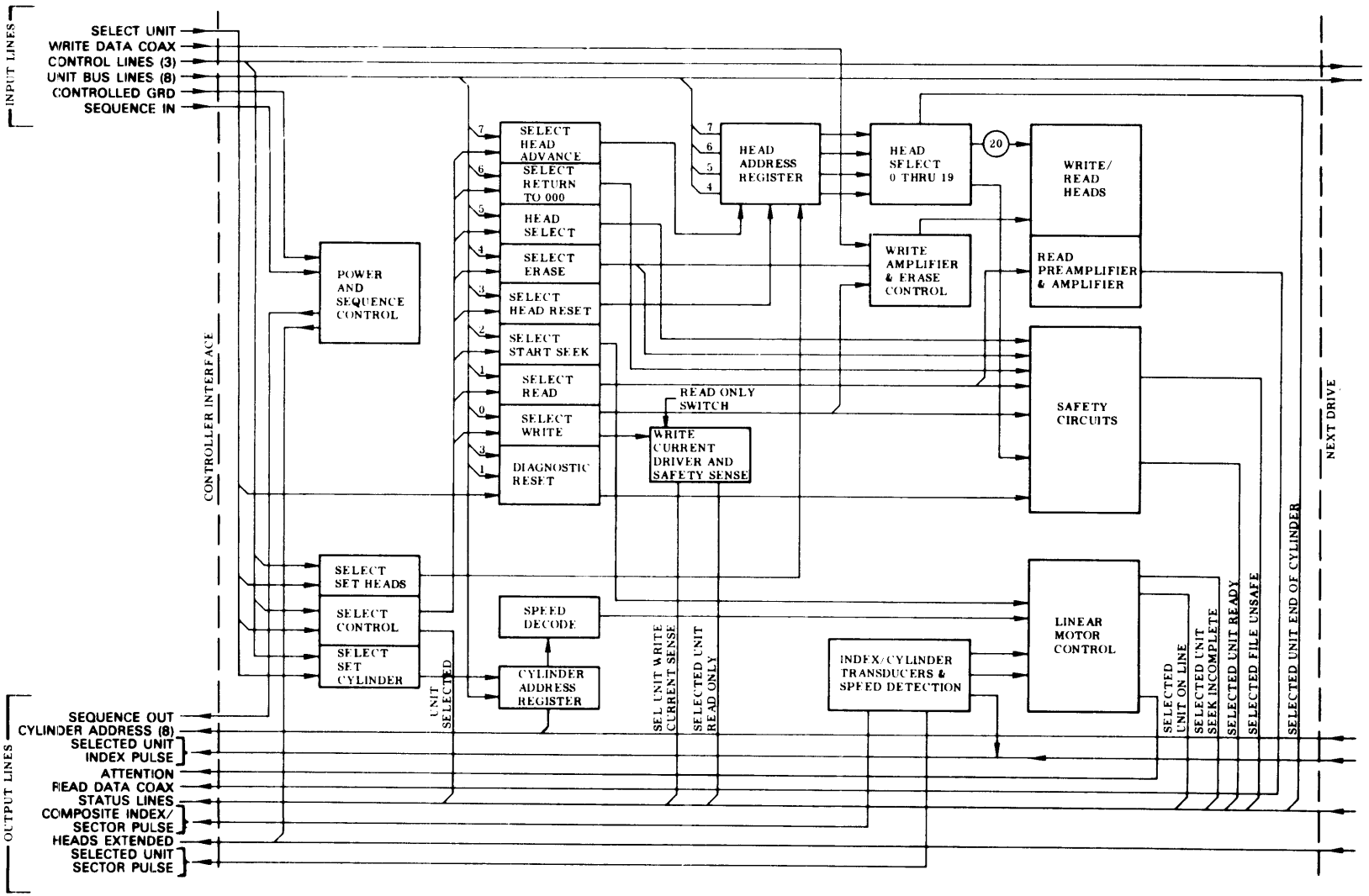


FIGURE 2-5. COMMUNICATION LINES

2.3.2.3 Interface Connections

The 660-1 drive is designed so that multiple units can be connected in chain fashion (as in Figure 1-1). Power control circuitry is provided to allow the controller to start the units—one at a time. As soon as the first unit reaches 70% of its full speed, sequencing logic enables the second unit to start. This sequence continues until all units in the chain are running. Provision is made to bypass a unit's sequencing logic when that 660-1 drive is out of service or being maintained. The following tables list the pin connections for the input and output cables.

TABLE 2-2. POWER CONNECTIONS

AC and Sequence Control Connector		
In Pin Connection	**Description**	**Out Pin Connection**
A	187/253 vac, phase A	B
B	187/253 vac, phase B	C
C	187/253 vac, phase C	A
D	Safety ground	D
E	110 vac convenience outlet	E
F	110 vac convenience outlet	F
G	Frame ground	G

TABLE 2-3. BUS CABLE CONNECTIONS

In Pin Connection	Line Description	Out Pin Connection
1	Unit Bus 0	1
2	Return ground	2
3	Unit Bus 1	3
4	Unit Bus 2	4
5	Return ground	5
7	Unit Bus 3	7
8	Unit Bus 4	8
10	Return ground	10
11	Unit Bus 5	11
12	Unit Bus 6	12
13	Return ground	13
14	Unit Bus 7	14
15	Unused*	15
16	Return ground	16
17	Set Cylinder (tag line)	17
18	Set Head (tag line)	18
20	Return ground	20
21	Control (tag line)	21
22	Unused*	
23	Return ground	23
24	Unused*	
25	Unused*	

TABLE 2-3. BUS CABLE CONNECTIONS (Continued)

In Pin Connection	Line Description	Out Pin Connection
26	Return ground	26
27	Unused*	
28 through 39	Spares**	
40	Cylinder Address Register 1	40
41	Return ground	41
42	Cylinder Address Register 2	42
43	Cylinder Address Register 4	43
44	Return ground	44
45	Cylinder Address Register 8	45
46	Cylinder Address Register 16	46
47	Return ground	47
48	Cylinder Address Register 32	48
49	Cylinder Address Register 64	49
50	Return ground	50
51	Cylinder Address Register 128	51
52	Selected Unit Ready	52
53	Return ground	53
54	Selected Unit On line	54
55	Selected Index	55
56	Return ground	56
57	Selected File Unsafe	57
58	Selected Unit Seek Incomplete	58
59	Return ground	59
60	Selected Unit End of Cylinder	60
62	Selected Unit Read Only	62
63	Return ground	63
64	Selected Unit Write Current Sense	64
65	Heads Extended	65 Switch contact
66	Return ground	66
67	Selected Unit Read Only	67
70	Not used (reserved)	70
71	Ground for pins 70 and 76	71
72	Reserved	72
73 through 75	Spares**	73 through 75
76	Controlled Ground	76
77	Sequence In	
	Sequence Out	77
78	Twisted pair ground for pin 77	78
79	+5 vdc to termination plug	79
80	Spare	80
82	Spare	82

NOTE: Pins 6, 9, 19, 61, 68, 69, and 81 do not exist on the Bus Cable connector

*The term "unused" indicates that the connector pin has a wire connected to it but it is not used

**The term "spare" indicates that the connector pin is available, but no wire is connected to it.

TABLE 2-4. UNIT CABLE CONNECTIONS

In Pin Connection	Description
1 through 4	Spares
5	Write data coax
6 through 11	Spares
12	Read data coax
13	+5 vdc (used as termination power source on 660-1)
14 and 15	Spares
16	Composite Sector and Index
17	Common for 16
18 through 20	Spares
21	Attention
22	Unit Is Selected
23	Select Unit
24	Spare
25	Shield ground
26	Common for 21
27	Common for 22
28	Common for 23

2.3.3 Operator Control Panel

Figure 2-6 shows how the keys and lights are displayed on the operator control panel. The functions of operator control switches and indicators are as follows:

ENABLE-DISABLE Switch

ENABLE Position—The switch enables the logical connection between the controller and the drive.

DISABLE Position—The switch disables the logical connection between the controller and the drive.

If the drive is performing an operation under the command of the controller, changing the state of the switch will not change off-line logic until the controller deselects. Upon next select, off-line status is returned to the controller.

READ/WRITE-READ ONLY Switch

READ/WRITE Position—The switch enables read and write circuitry.

READ ONLY Position—The switch disables the write and erase circuitry to allow a READ ONLY operation. A line is available in the I/O interface to indicate that the READ ONLY mode has been selected. The controller designer must incorporate this signal in system status if the central processor is to recognize the condition.

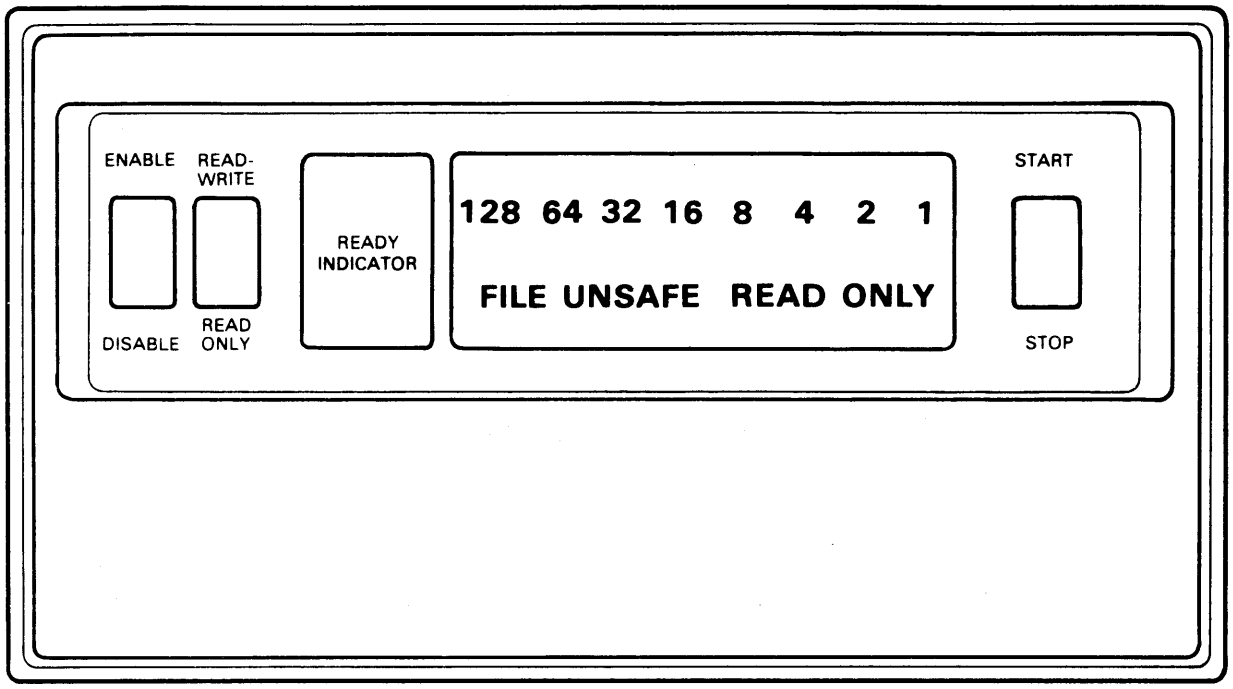


FIGURE 2-6. OPERATOR CONTROL PANEL

Ready Indicator

This indicator illuminates when the drive has reached operational speed and the heads are positioned to track 000 on the initial load operation. This light signifies that the drive is ready for instructions. The indicator goes off when the STOP switch is pressed or when the system power is dropped. The indicator also goes off if a Seek Incomplete state occurs.

File Monitor Indicators

This indicator cluster calls out the cylinder position (weighted, binary number readout) and indicates a FILE UNSAFE condition (red light) and READ ONLY mode (white light).

The access position indicator continuously identifies the cylinder at which the heads are positioned.

The FILE UNSAFE indicator lights when the safety circuits determine that the file is not usable.

The READ ONLY indicator lights when the write and erase circuits are disabled by the READ ONLY switch.

START-STOP Switch

START Position—This switch is operable when the main power switch to the unit is on, a pack has been loaded, and the cover is closed. Pressing this switch powers the spindle drive motor and, when the disc pack speed is greater than 1700 rpm and the pack's stabilization delay of 60 seconds has expired, loads the heads and positions them to cylinder 000.

STOP Position—With the switch in this position, power to the motor cuts off and the carriage is retracted, which unloads the heads. Dynamic braking stops the spindle within 12 seconds.

2.3.4 Positioning and Spindle Drive Mechanisms

2.3.4.1 Positioning Motor

The linear positioning motor consists of a stationary permanent magnet surrounding a movable, bobbin-wound armature. The armature is free to slide in and out of the permanent magnet through a hole in one of the magnet's faceplates. See Figure 2-7.

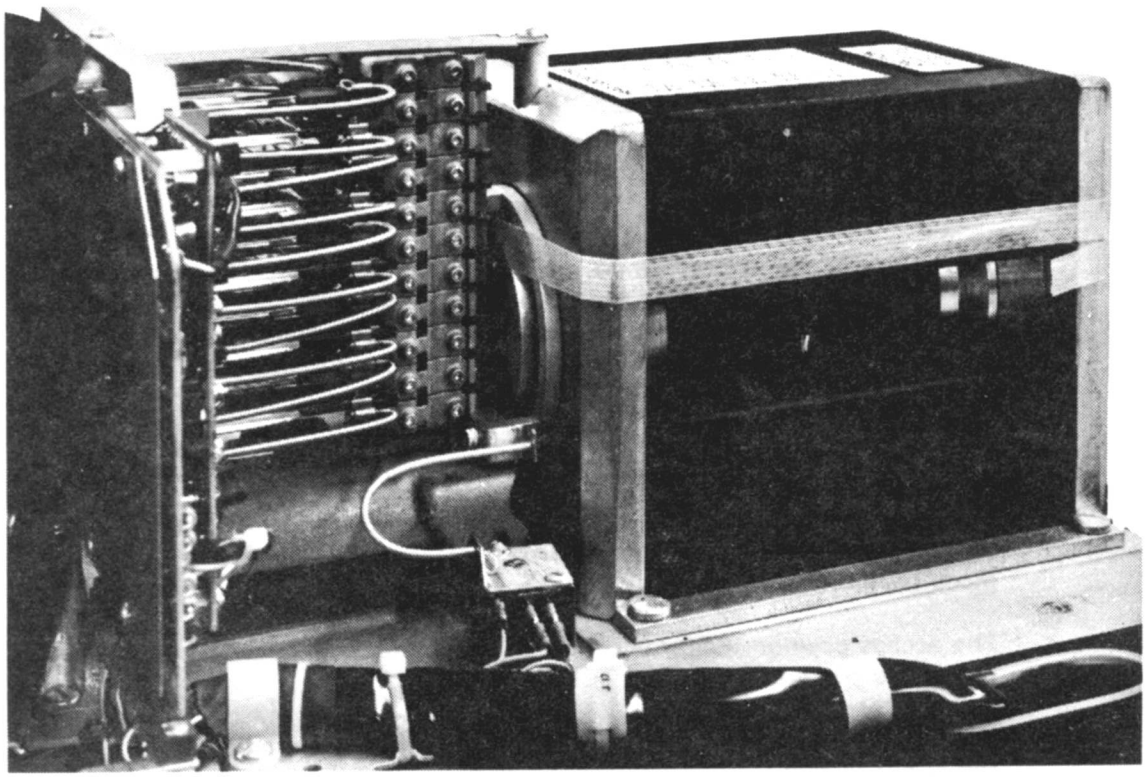


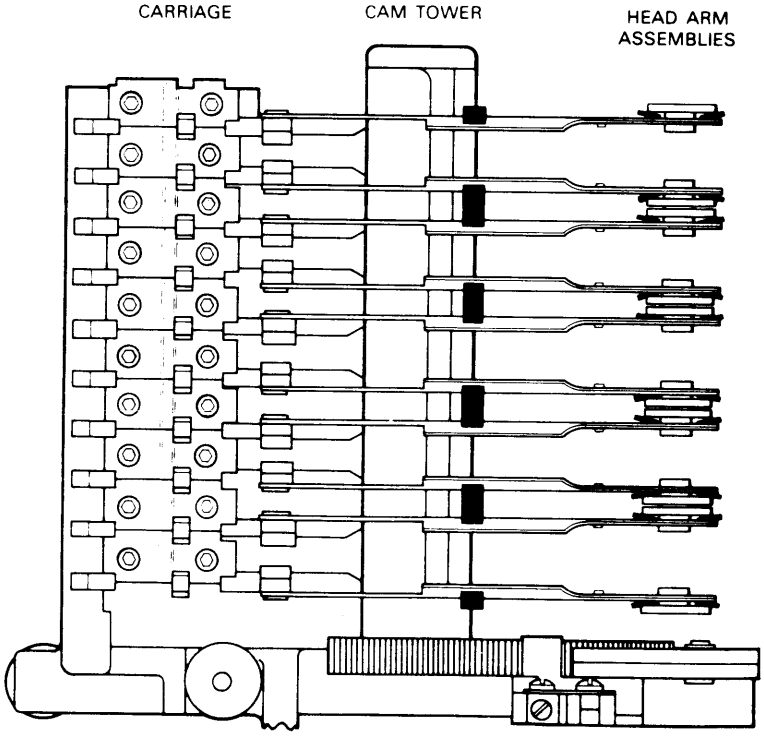
FIGURE 2-7. LINEAR POSITIONING MOTOR

Fastened to the armature by three screws is the Tee-block which holds the head-arm assemblies. The Tee-block is mounted on a carriage that moves freely along hardened aluminum tracks on three pairs of opposed ball bearing rollers. Movement of the armature in and out of the permanent magnet moves the carriage forward and back. This linear travel positions the heads over or under their respective disc surfaces or pulls them out and away from the disc pack.

Power for this movement is provided by a direct current which is fed to the armature. The magnetic field built up around the armature by this current reacts with the permanent magnetic field and the reaction either forces the armature out away from the permanent magnet or pulls it into the field. Direction depends on the polarity of current; speed depends on the current level. Two beryllium copper strips serve as flexible connectors between the armature coil and the DC power supply leads.

2.3.4.2 Head-Arm Assemblies

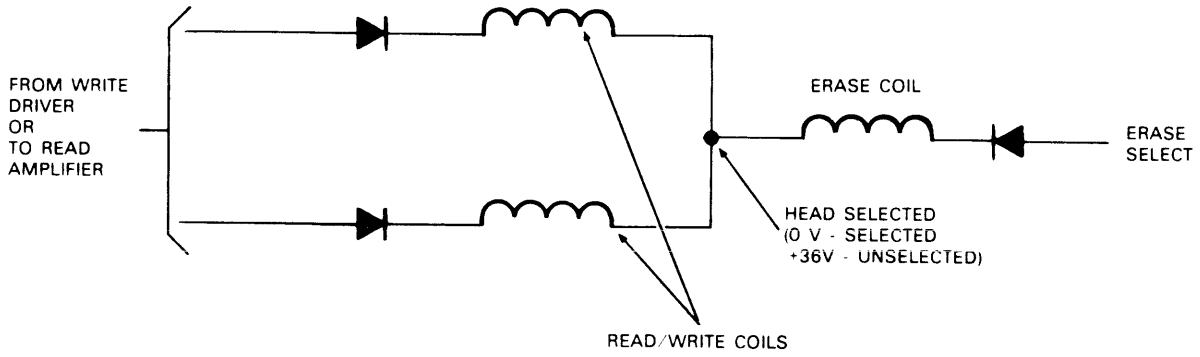
Attached to the Tee-block are 20 read/write head arm assemblies. These assemblies are mounted in two banks of ten each; half of them facing up, the other half facing down. Each head arm assembly consists of a read/write head attached to a support arm (see Figure 2-8).



NOTE: CAMS ARE REPRESENTED BY SOLID RECTANGLES. HEADS ARE SHOWN LOADED AND RIDING FREE OF CAMS

FIGURE 2-8. HEAD MOUNTING CONCEPT

The read/write heads contain the read/write gap and erase poles. As can be seen in Figure 2-9, the read/write gap precedes the erase pole (by 0.005 inches). The coils which carry the read/write and erase currents are also illustrated in Figure 2-9. Two coils are connected in series (center tapped) on the read/write pole and another pair of series-wound coils is used on the erase poles. Head selection (using transistor switching) places ground on the center tap of the selected head as shown in the sketch below.



Each head shoe is gimbal-mounted to allow pivoting on any horizontal axis. Vertical mobility is provided by a leaf spring built into the arm. This freedom of movement allows the head to maintain the correct altitude above the disc surface.

The leads connected to the read/write and erase coils are encased in a flexible coil spring. This spring supports the leads between the head arm and read/write circuitry.

The leaf spring is designed to maintain a constant loading force on the heads (350 grams, nominal). When the heads are in the retracted position, plastic unload cams bear against a ramp surface (also on an integral part of the head arm). They counter the loading force and hold the heads in the unload position. The purpose of the cams is to keep the heads sufficiently separated to clear the discs during load and unload operations. The cams are attached to an aluminum tower which arches over the arms.

The load/unload ramp rides off its cam as the head moves into the pack. When the ramp is clear of the cam, spring tension from the leaf spring forces the head toward the disc surface. Between the head and disc surface, an air cushion or bearing created by the rotating disc counters the spring loading force and keeps the head at the required flying height (80 microinches, nominal).

As the arm is retracted, the ramp rides back onto its cam and the head is lifted clear of the disc surface. Just as loading the heads is an inseparable part of initial seek, unloading is integrated with the retract operation.

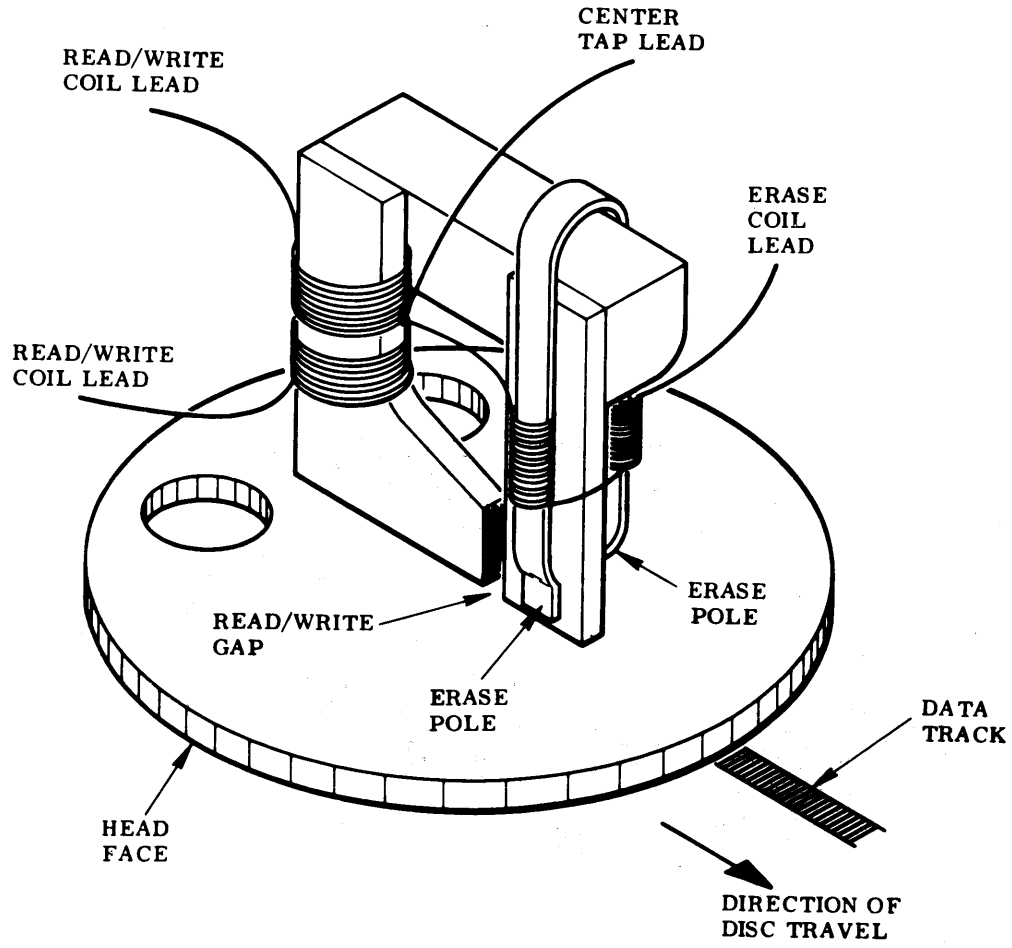


FIGURE 2-9. READ/WRITE AND ERASE POLES

2.3.4.3 Detent Mechanism

A rack of teeth, called the detent rack, is mounted on the carriage directly under the array of arms. As the carriage moves along the track during positioning, the rack moves with it. Spacing of the rack teeth is 0.020 inches.

A double detent pawl is mounted on the carriage way opposite the rack. Each pawl has a set of four teeth with the same pitch as the rack teeth. The two pawls (Figure 2-10) are offset from one another by half their pitch (0.010 inches). This offset spacing allows the pawl to engage the rack in twice as many positions as there are teeth. When one pawl is engaged, the other rests on top of the adjacent rack tooth. This is commonly referred to as odd/even detenting. One detent pawl engages at all odd cylinder positions while the other engages at all even cylinder positions.

The two pawls are spring loaded and held in the detent-out position by a detent actuator. See Figure 2-11a.

The cylinder transducer is located opposite the detent rack teeth as shown in Figure 2-11b.

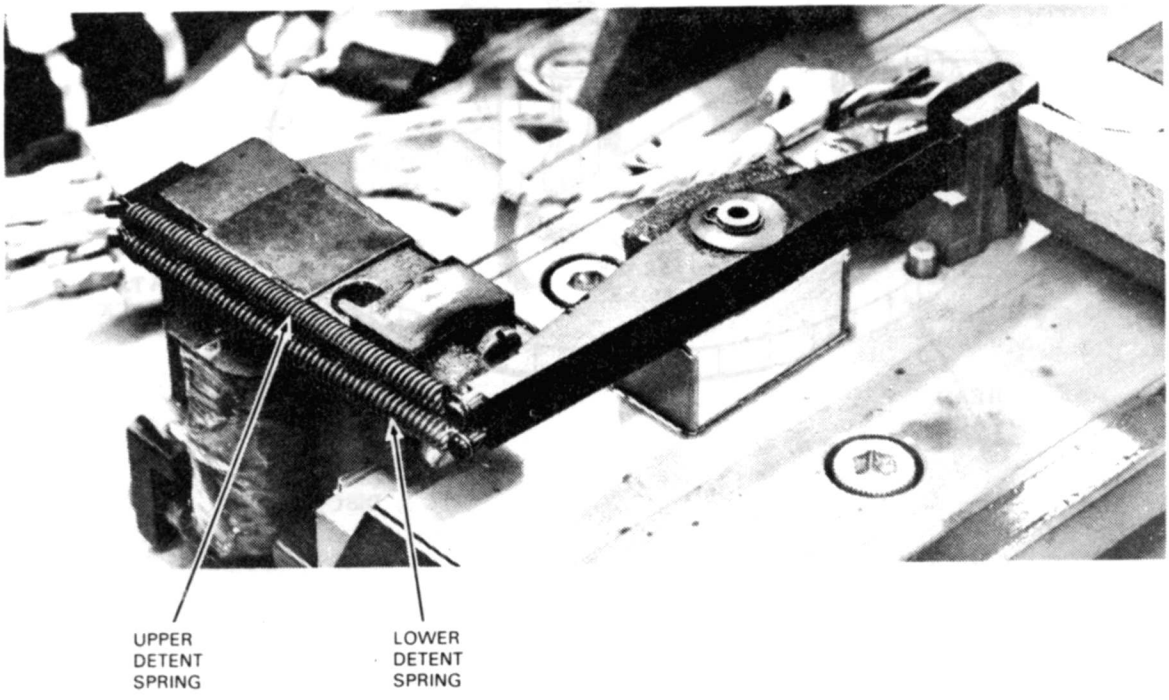


FIGURE 2-10. DOUBLE DETENT PAWL AND CYLINDER TRANSDUCER

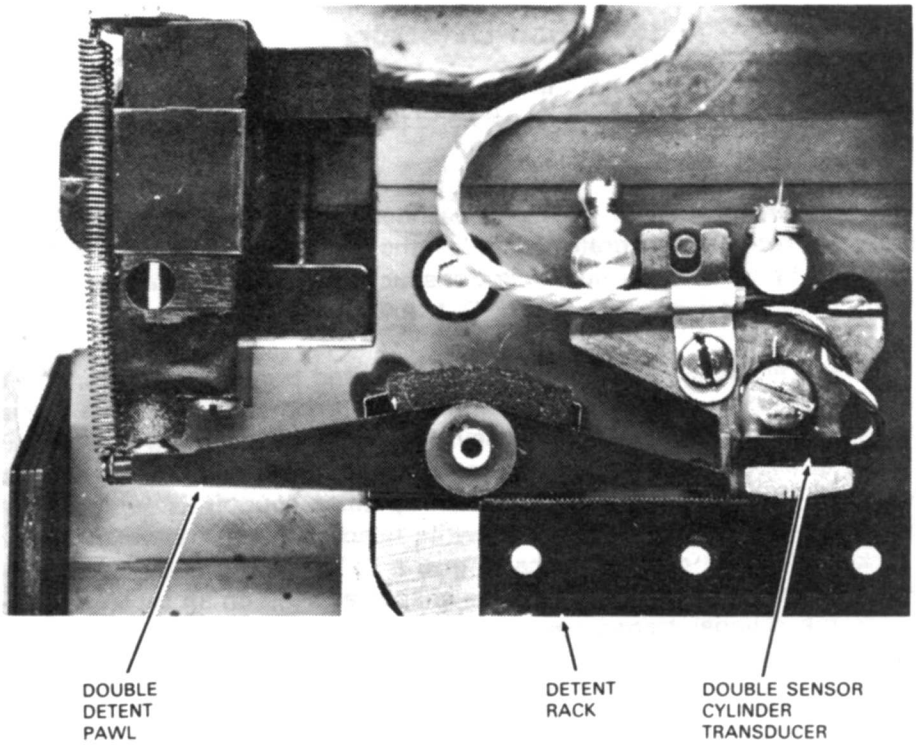


FIGURE 2-11a. SPRING-LOADED DETENT PAWLS AND DETENT ACTUATOR

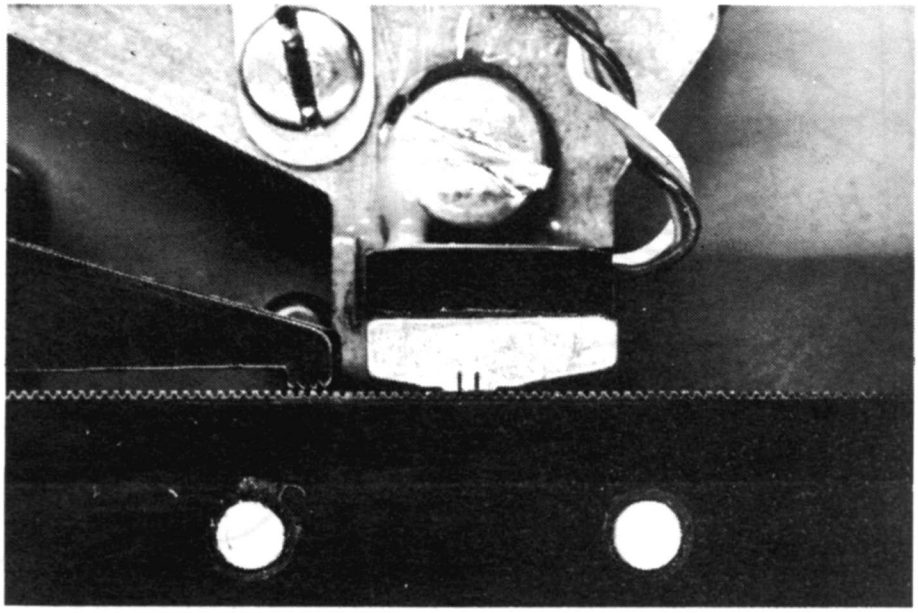


FIGURE 2-11b. CLOSE-UP OF CYLINDER TRANSDUCER, DETENT PAWL, AND RACK TEETH

2.3.4.4 Motion and Position Detectors

There are two basic movements in the 660-1 drive which must be monitored: (1) the linear travel of the carriage along its way and (2) the rotary motion of the disc pack on its spindle.

As the heads are positioned from one cylinder to another within the disc pack, it is necessary to keep an accurate count of the number of cylinders passed. This is accomplished by a variable reluctance transducer mounted on the carriage way facing the detent rack. See Figures 2-10 and 2-11a/b.

This cylinder transducer contains two sets of paired primary and secondary coils (see Figure 2-12). The two sets are separated from one another so that while one is opposite a rack tooth, the other is opposite a valley. The primaries are wired in series and excited at 145 kHz at about 3 volts. Each time a rack tooth passes a primary-secondary pair, it couples them. The coupling indicates to an up-down counter in the logic that another cylinder has been reached by the read/write heads. The peak-to-valley spacing allows each rack tooth to be counted twice to give a 0.010-inch cylinder-spacing indication. Figure 2-13 shows the sequence of pulse shapes as seen on an oscilloscope when rack teeth pass the cylinder transducer.

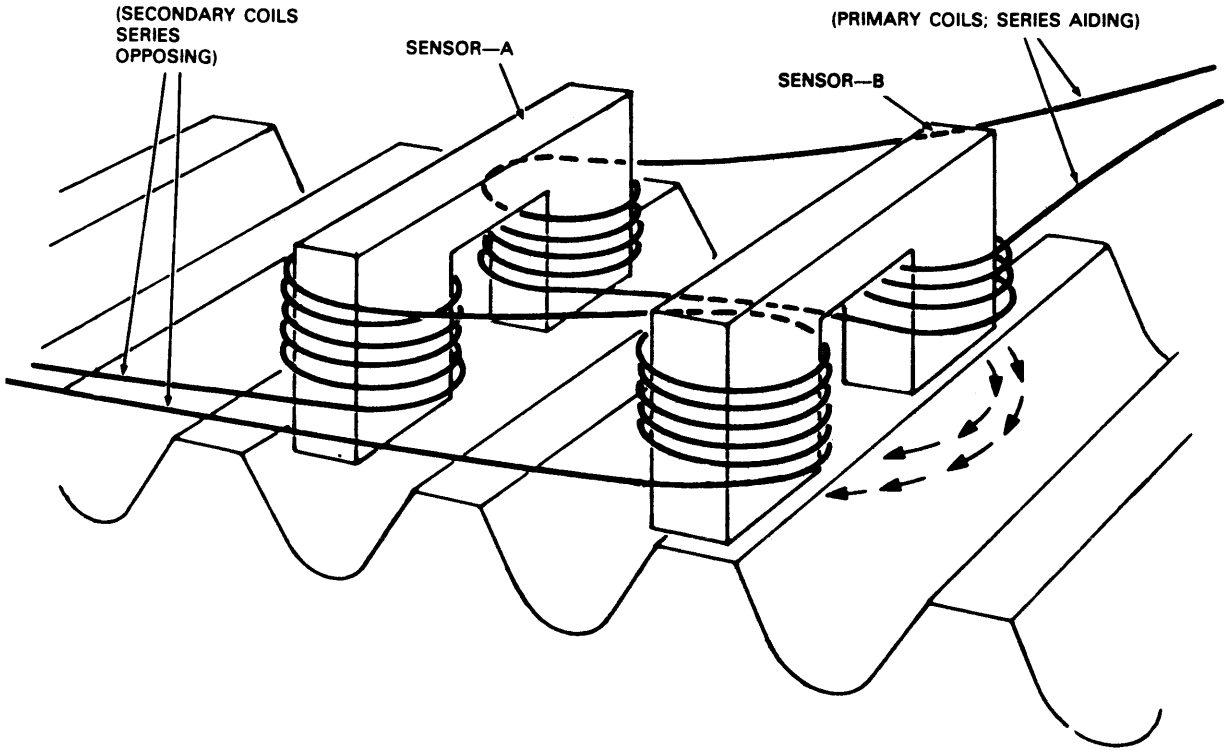
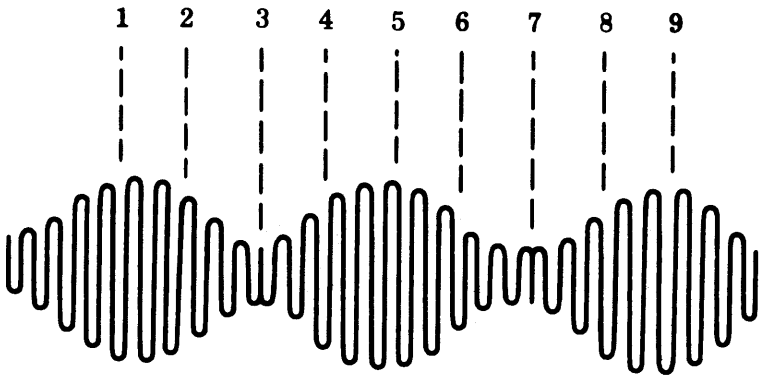


FIGURE 2-12. CYLINDER TRANSDUCER, PRIMARY AND SECONDARY PAIRS

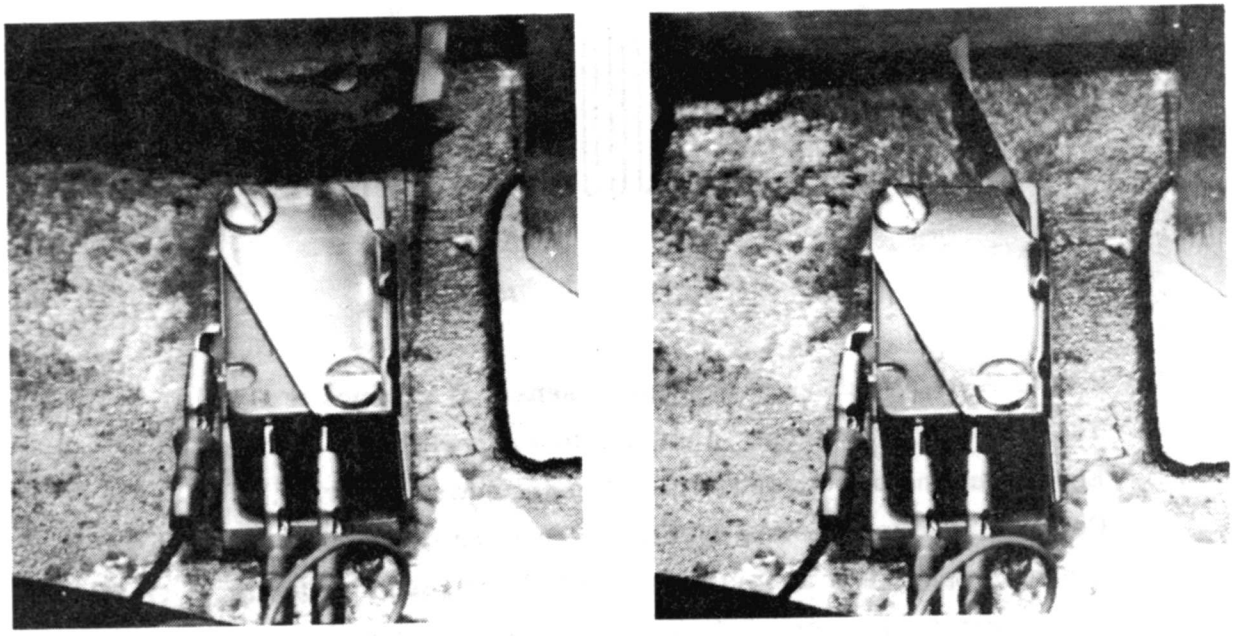


1. Sensor A is fully coupled by a tooth; sensor B is opposite a valley.
2. Tooth moving away from A; another tooth approaching B.
3. Equal coupling of both sensors; null point; phase reversal.
4. Coupling of A approaching minimum; coupling of B approaching maximum.
5. Sensor A opposite a valley; sensor B fully coupled by a tooth.
6. Tooth approaching sensor A; tooth moving away from B.
7. Equal coupling of both sensors; null point; phase reversal.
8. Tooth approaching sensor A; tooth moving away from B.
9. Sensor A fully coupled by a tooth; sensor B is opposite a valley.

FIGURE 2-13. CYLINDER TRANSDUCER OUTPUT WHEN COUNTING

Home position (cylinder 000) is the reference cylinder to which the heads are sent when their present address is not known. The heads are sent to cylinder 000 after they have been in the retracted position (this is called a restore). Whenever the heads must be positioned to home from a location without a known address, they are first sent to the forward stop, which is assigned an address of 202. A reverse seek of 203 cylinders is initiated and when a zero difference count (compare) condition is reached, the carriage is detented. This is home position (cylinder 000).

Certain safety circuits need to know whether the heads are extended or retracted. A microswitch mounted on the carriage way near the positioning motor is operated when the heads are retracted. See Figure 2-14.



HEADS RETRACTED

HEADS EXTENDED

FIGURE 2-14. HEADS RETRACTED/EXTENDED SWITCH

Rotational speed of the disc pack and location of index are monitored by the index transducer (Figure 2-15), which is mounted on the spindle end of the baseplate. When a disc pack is installed, the edge of the slotted disc on the bottom of the pack separates a permanent magnet from a single coil (see Figure 2-16). As the pack rotates, the slot or slots pass between the magnet and coil. Since the disc is aluminum, there is minimum coupling when the air gap between the magnet and coil is blocked by the disc and maximum coupling when the slots appear (see Figure 2-17 for an illustration of an index/sector disc).

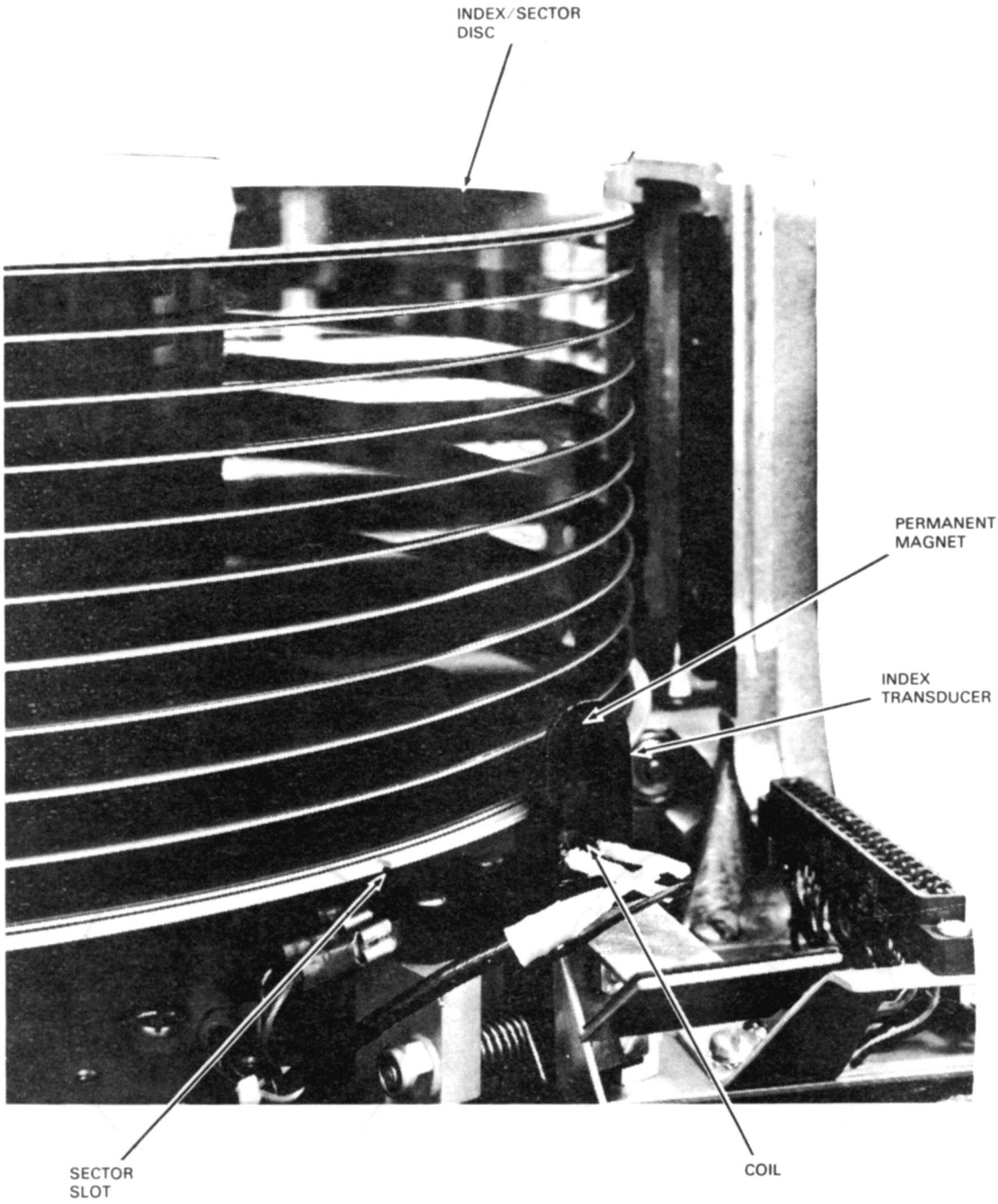


FIGURE 2-15. INDEX TRANSDUCER

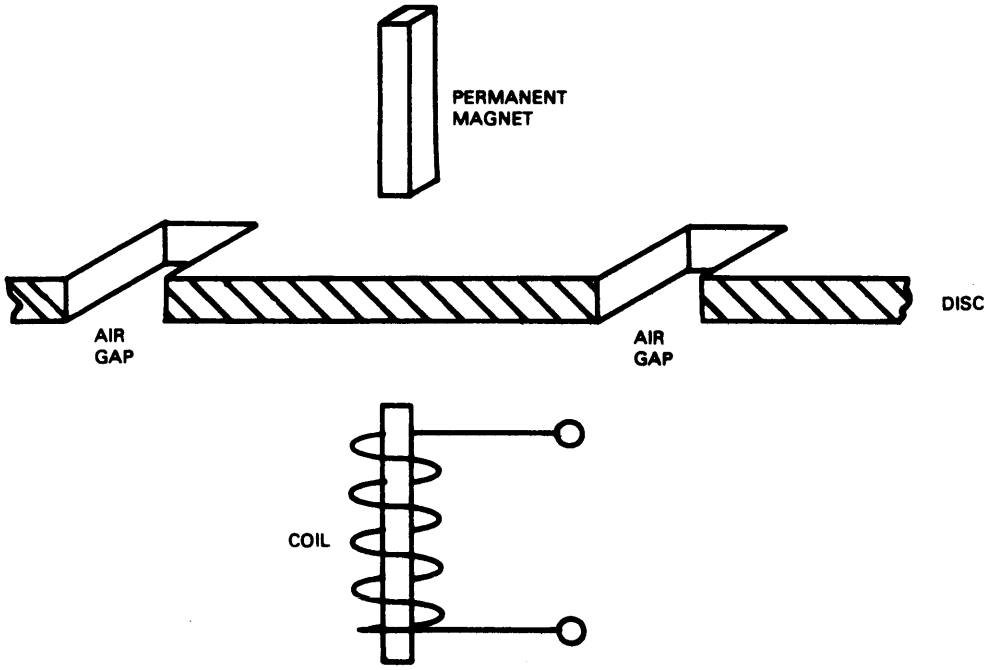


FIGURE 2-16. COIL AND SLOT RELATIONSHIP

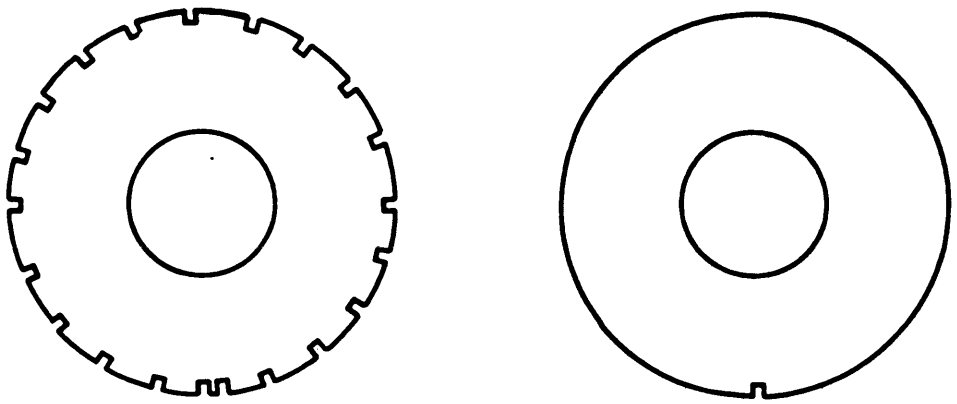
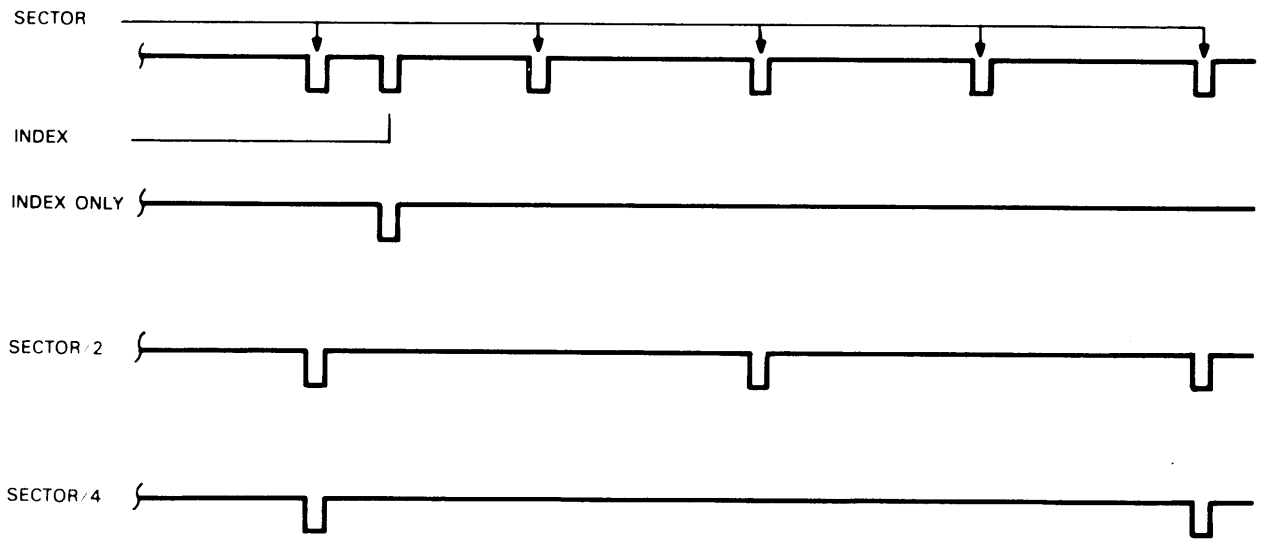


FIGURE 2-17. DISC CONFIGURATIONS

The drive is capable of operating with either of two types of disc packs. For packs with a single index slot, the drive provides an index pulse to the controller each time the index slot passes a reference location on the drive top plate. For packs which have sector slots, a manual change on one of the circuit cards enables logic which discriminates between index slots and sector slots and provides outputs on the appropriate interface lines. In addition, a manual selection may be made to select every second or every fourth sector slot on one of the interface lines (see Figure 2-18).

The composite index/sector signal in the unit cable gives an electrical representation of the disc slots and is continuously available to the controller. This signal is a logical **ONE** during the time the sector or index slot is passing through the transducer.

Disc pack rotational speed is detected by testing the rate of index pulses. Each index pulse clocks a flip flop. This flip-flop triggers a delay circuit. If the disc pack is rotating at least at 70% of its maximum speed, the following index pulse will occur before the delay circuit times out and an upspeed signal will be generated.



THE SELECTED INDEX IS ALSO AVAILABLE IN THE BUS CABLE.

FIGURE 2-18. INDEX SECTOR RELATIONSHIPS

2.3.4.5 Spindle Drive System

Rotation of the disc packs is provided by the spindle drive system which includes the spindle drive motor, spindle, and drive belt (see Figure 2-19).

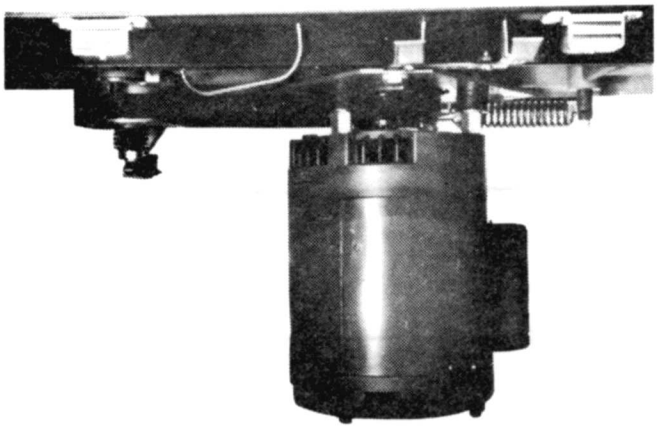
The disc pack drive system is powered by a one-half horsepower, 60- or 50-Hz, single-phase AC motor. As shown in Figure 2-19, the motor transfers torque to the spindle drive pulley by a simple belt loop. Tension on the belt is maintained by a special motor shock mounting; no idler pulley is used.

The drive motor also serves as a dynamic brake for the disc pack drive. When the STOP switch is pressed or when the disc pack cover is opened, AC power to the motor is cut off and DC power (55 volts) is applied to the motor coil for about 12 seconds, stopping it.

The disc pack spindle is bolted into a hole in the baseplate with the spindle pulley below the baseplate and its disc pack mounting surface above. A speed ratio between the motor pulley and the spindle pulley reduces spindle rotation to 2400 ±48 rpm.

A disc pack is secured to the spindle cone with 206 ±32 pounds of force by a locking shaft within the spindle and Belleville washers below the spindle pulley.

DISC PACK MOUNTING SURFACE



MOTOR, PULLEYS, AND BELT

FIGURE 2-19. SPINDLE DRIVE SYSTEM

A spindle assembly includes a mechanical lock which engages when the top cover is raised to load or unload a disc pack (see Figure 2-20). When the cabinet cover is lifted, an arm on the cover tilts the index transducer back. This movement causes a pawl under the baseplate to engage one of several notches in the spindle pulley. As long as the cover is raised, the pawl will prevent the spindle from turning. This lock can be bypassed by removing the cover from the machine.

The assembly also includes a pack-on switch which automatically closes when a disc pack is installed (see Figure 2-21). The pack-on switch is a safety feature and must be closed for the spindle drive motor to operate.

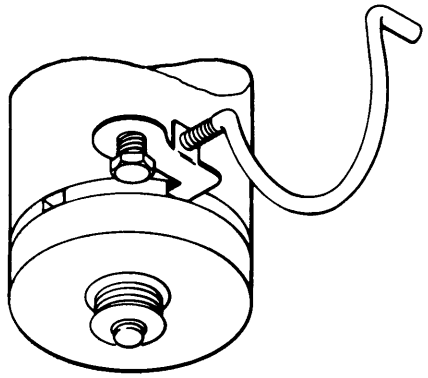


FIGURE 2-20. MECHANICAL SPINDLE LOCK

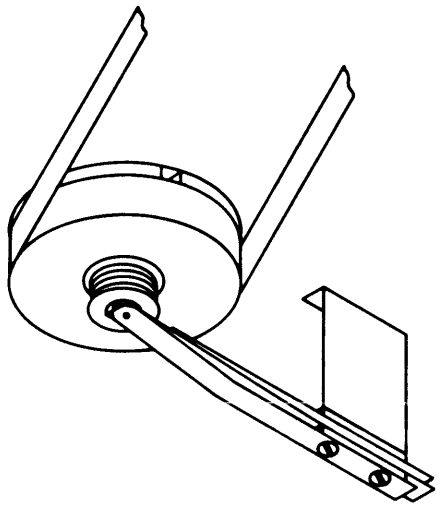


FIGURE 2-21. PACK-ON SWITCH AND SPINDLE GROUND

SECTION 3
INSTALLATION

3.1 GENERAL

The following information is provided as a guide to personnel responsible for installing a 660-1 drive. It outlines basic procedures which should bring the drive on line in as short a time as is practical. These procedures are not intended as a substitute for whatever standard practice the customer may have for equipment installation.

3.2 UNPACKING AND INSPECTION

The following tools are required for unpacking the drive:

Knife or large diagonal cutters	Socket wrench, 3/4-inch
Allen wrench, 5/32-inch	Open end wrench, 31/2-inch
Large screwdriver	Fork lift (not mandatory)

Unpack and inspect the drive as follows:

1. Examine the shipping package and visible portions of the drive. Check for panel dents, mars, or scratches before opening the shrink bag. If signs of damage are found, contact the delivering carrier to make a physical examination of damage. The carrier is required to complete and sign a damage report form. If no damage is noted, the unit may be unpacked.
2. If the drive was **not** shipped by an air carrier, proceed to step 3. For drives shipped by air, begin the unpacking procedure as follows.
   a. Cut the four (4) straps and remove from container. (Refer to Figure 3-1.)

   WARNING

   Use care when cutting these straps; they can spring back and cause injury to anyone standing near the crate.

   b. Remove the top corrugated pad.
   c. Push the bottom corrugated pad down to the floor and away from the bottom tray.
   d. From the rear of the drive, lift the drive with a fork lift. Run the forks between the base of the corrugated tray and the bottom corrugated pad. Lift the drive up until its casters are free of the four (4) plastic feet. Remove the bottom corrugated pad and four plastic feet and then lower the drive to the floor.
   e. If the drive must be raised manually, use at least four persons.

   WARNING

   Use extreme care when lifting the drive manually. The weight of the drive is in excess of 390 pounds.

3. Slit the shrink bag from top to bottom along the center side of the package marked OPEN THIS SIDE, and along the center top side of the equipment box. (Refer to Figure 3-1.) To avoid scratching the paint while cutting the bag, grip the seam running from top to bottom and pull the bag away from the drive.

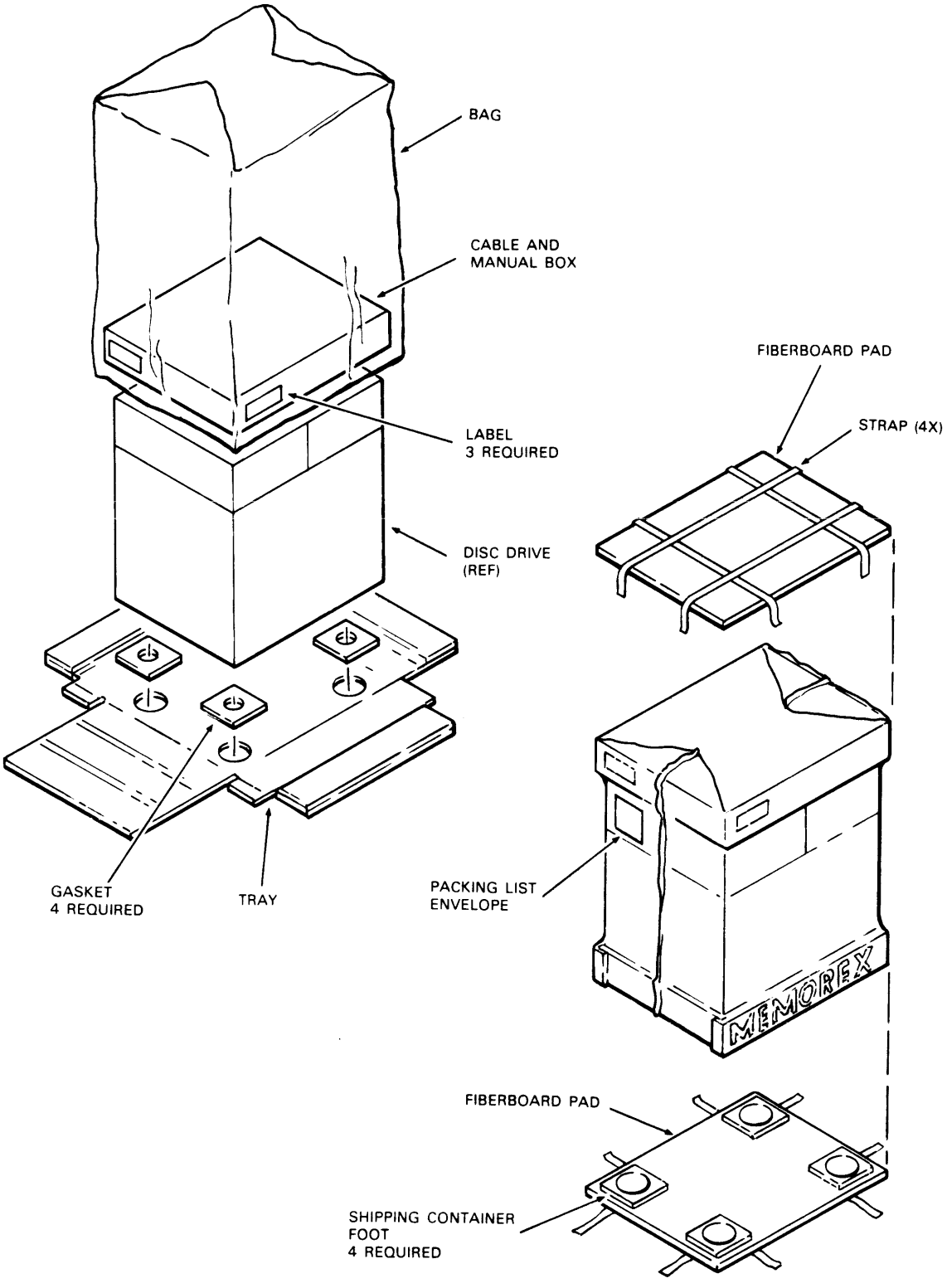


FIGURE 3-1. DRIVE PACKING CRATE

4. Remove the staples from the end flaps of the bottom tray marked OPEN THIS SIDE.

5. Unroll the center section of the bottom tray between the flaps to allow the drive to be rolled free of the tray.

6. Roll the drive free of the tray and out of the shrink bag. Discard the bag. Remove the equipment box from the top of the drive and lay aside for later use.

7. Remove all strips of tape joining the two top covers of the drive, and joining the top covers with the front and rear panels of the drive.

8. Open the operator cover and remove two 16-unit desiccant bags from the disc shroud. Close the operator cover.

9. Remove the control cover assembly.

10. Remove the strip of tape joining the linear motor and head carriage and the two 16-unit dessicant bags (see Figure 3-2).

11. Loosen and remove the two deck plate clamps. (Refer to Figure 3-2.)

12. Remove the two masonite spacers between the drive frame and deck plate at the magnet end. (Refer to Figure 3-2.)

13. Replace the control cover assembly.

14. Remove the rear panel from the drive.

15. Remove the strips of tape from the back of the printed circuit boards, and the strips of tape joining the printed circuit boards with the side of the logic gate frame.

16. Raise slightly and fully open the power supply gate. Remove the gate brace block from under the logic gate by lifting the gate and sliding the block out. Corrugated fiberboard may be contained in a space between the block and gate; if so, remove the fiberboard with the block. Close the power supply gate.

17. Remove the three 16-unit desiccant bags below the power supply gate. Replace the rear panel on the drive.

18. Open the equipment box and remove the kick plates and mounting screws. Install the kick plates on the drive using the holes provided at the bottom of the main frame.

19. Place the drive in its assigned location. Remove the caster blocks from the equipment box and install on the drive casters.

The desiccant bags, bottom tray, power supply gate brace block, deck plate clamps and spacers should be placed in storage for reuse in the event of reshipment or long-term storage.

3.3 REPACKING FOR RESHIPMENT OR STORAGE

3.3.1 Preparation

The disc storage drive is prepared for removal from the site or long-term storage by setting all circuit breakers to OFF and disconnecting all external cables.

The drive is repacked at the site without the use of a shrink bag and the bottom tray. As described below in Section 3.3.2, only internal repacking of the drive and external taping of the drive covers and panels is required.

3.3.2 Packaging

Use the following packaging instructions to provide protection against vibration and rubbing during shipment. The following procedure assumes that the original packing materials were saved for reuse and that glass-reinforced tape, polyethylene stock, or equivalent materials are available.

1. Open the operator cover and place two 16-unit desiccant bags inside the disc shroud. Close the operator cover.

2. Remove the control cover assembly.

3. Tape the linear motor and retracted head carriage together as a unit. (Heads must be in the retracted position for shipment.) The tape is to run horizontally all around the linear motor and bobbin assembly.

CAUTION

Tape must not contact the heads or the head/arm assemblies, or in any way affect alignment.

4. Insert two masonite spacers between the frame and deck plate at the magnet end. (Refer to Figure 3-2.)

5. Install two deck plate clamps over the frame end and attach to the predrilled holes in the deck plate. Tighten the clamps until the deck plate is drawn up to the masonite spacers. (Refer to Figure 3-2.)

6. Replace the control cover assembly.

7. Remove the rear panel from the drive.

8. Fully open the power supply gate and insert the gate brace block under and to the rear of the logic gate by lifting the logic gate slightly and sliding the block under it. If there is more than $1/16$-inch space between the block and gate, use corrugated fiberboard as a shim to fill the gap. Close the power supply gate while lifting it slightly so that it rests on part of the block.

9. Tape across the back of the printed circuit boards and part way down the side of the logic gate frame to insure that the boards stay in place during shipment. Close the logic gate while lifting it slightly so that it rests on part of the block.

10. Place three 16-unit desiccant bags below the power supply gate. Replace the rear panel on the drive.

11. Use strips of tape to join the two top covers of the drive and to join the top covers with the front and rear panels of the drive. This will provide protection against vibration and rubbing.

12. Remove the caster blocks from the casters to allow the drive to be rolled freely.

13. Package the external cables, manuals, and caster blocks in the equipment box.

14. For shipping, the drive must be tied down to the vehicle according to recommendations of the carrier. A hand-lift truck may be used for removing the drive from the site and placing it into the vehicle.

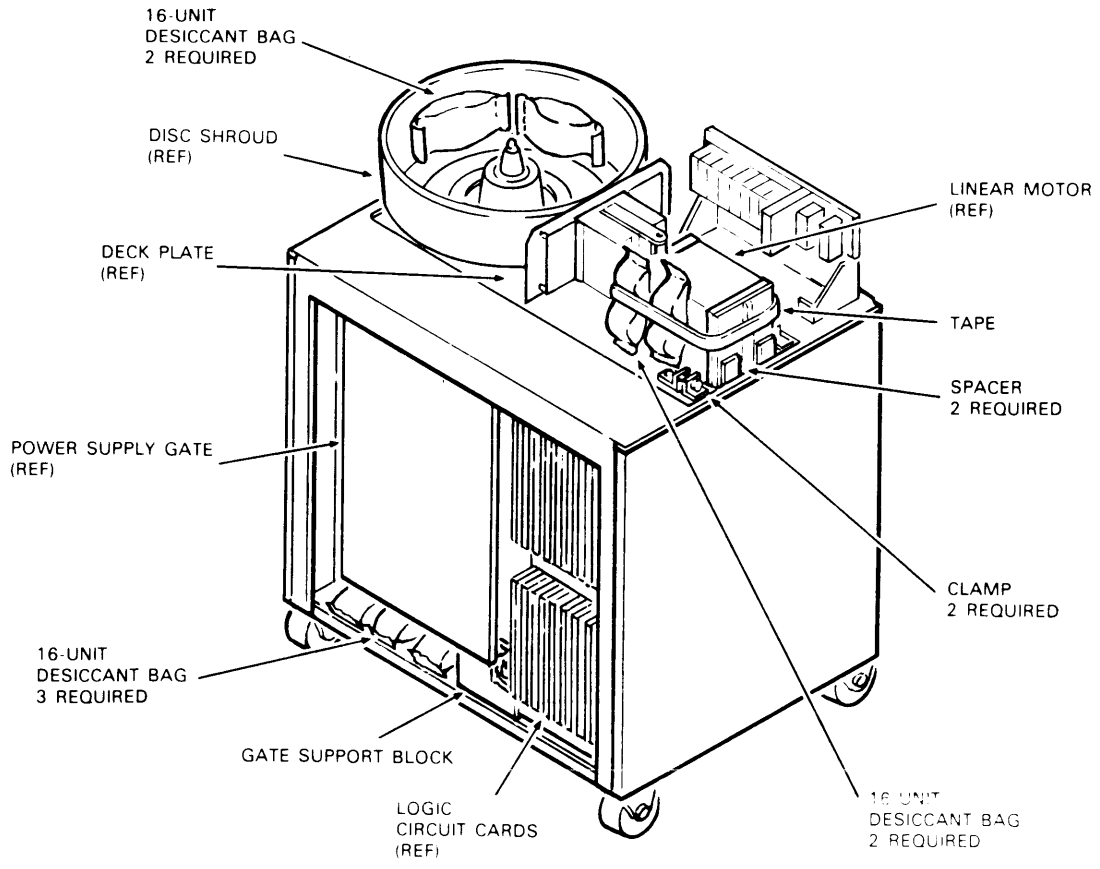


FIGURE 3-2. DRIVE UNPACKING MATERIALS

3.4 ENVIRONMENT

The disc drive should be placed so that a clearance of three feet exists at both the front and rear of the machine. This allows room to remove the front and rear panels for maintenance. Refer to Figure 2-3. The room temperature range should be between 60°F and 90°F with temperature changes less than 15°F per hour. The relative humidity should be between 20% and 80%.

The optimum room temperature is 70°F with a relative humidity of 50%.

3.5 PRIMARY POWER SOURCE DETERMINATION

WARNING

In certain cases, a hazardous condition will exist if the power source does not match the J1 configuration.

The Memorex 660-1 disc drive requires as a minimum, three phases of power and a non-current neutral (earth ground). The drive normally operates from 208/230 vac. In addition to the primary power, provisions are made in the 60-Hz (A Model) machine for the connection of auxiliary 110 vac convenience-outlet power. The 50-Hz (B Model) machine contains provision for a neutral wire which allows operation from 380 vac, wye-connected power.

The exact drive configurations are discussed below.

3.5.1 660-1A (60-Hz Model Drive)

The power source must provide power to the first drive of a string as follows:

J1 Pin	Requirement
Pin A	Phase A, 208/230 vac
Pin B	Phase B, 208/230 vac
Pin C	Phase C, 208/230 vac
Pin D	Earth (frame) ground or non-current carrying neutral
Pins E and F	115 vac isolated from primary power, single. At the user's option, pins E and F may be connected to earth ground at the power source. However, the convenience outlets are not usable in this case.
Pin G	Power cable shield which is connected (at the source) to the same non-current carrying neutral or earth (frame) ground which is applied to pin D.

3.5.2 660-1B (50-Hz Model Drive) 220 Vac Operation

The power source must provide power to the first drive of a string as follows. (Refer to Schematic Diagram 201945, AC Power Distribution 50 Hz, at EC Level 24018.)

NOTE

The convenience outlets are deleted from 50-Hz machines (Model B) at the factory.

J1 Pin	Requirement
Pin A	Phase A, 220 vac
Pin B	Phase B, 220 vac
Pin C	Phase C, 220 vac
Pin D	Connected to neutral at the source. As an option, pin D may be left disconnected provided there are no floating wires in the AC power cable.
Pins E and F	Connected to earth (frame) ground at the source.
Pin G	Power cable shield which is connected (at the source) to earth (frame) ground.

The Model 660-1B drives which have interior control panels at EC levels less than 1181 must be modified as follows:

1. Disconnect all AC power cables from the drive (both J1 and J2).
2. Remove the cover from the rear of the interior control panel.
3. Locate and remove (from the terminal board) the green #12 AWG wire connected to the upper terminal of TB1-4. With an ohmmeter, confirm that the wire is connected to frame ground with a resistance of 0.05 ohm or less. With the ohmmeter, confirm that TB1-4, lower terminal, has a resistance to ground of 5 megohms or more.
4. Connect the green wire, removed from TB1-4, to TB1-5 and, at the same time, jumper TB1-5 to TB1-6 with the U-shaped terminal jumper P/N 150368. Confirm with the ohmmeter that J1-E, J1-F, J1-G, and J2-E, and J2-G all have a resistance to ground of 0.05 ohm or less.

3.5.3 660-1B (50-Hz Model Drive) 380 Vac Operation

For the drive to operate with this source of power it must be modified as follows (refer to Schematic Diagram 201945, AC Power Distribution 50 Hz, at EC Level 24018):

1. Disconnect **all** AC power cables from the drive (both J1 and J2).
2. Remove the cover from the rear of the interior control panel and move the red wire, connected to one half of the main power switch S1, from TB1-3 to TB1-4.
3. Unsolder the blue wire from the lug of the F2 fuse holder and solder it to the tip of the F2 fuse holder. When this operation has been performed, both the blue wire and the violet wire will be soldered together at the tip of the fuse holder.

The power source must provide power to the first drive of a string as follows:

NOTE

The convenience outlets are deleted from 50-Hz machines (Model 1B) at the factory.

J1 Pin	Requirement
Pin A	Phase A, 380 vac
Pin B	Phase B, 380 vac
Pin C	Phase C, 380 vac
Pin D	Connected to neutral at the source.
Pin E and F	Connected to earth (frame) ground at the source.
Pin G	Power cable shield which is connected (at the source) to earth (frame) ground.

The Model 660-1B drives which have interior control panels at EC levels less than 1181 require additional modification as follows:

1. Remove the cover from the rear of the interior control panel and move the red wire, connected to one half of the main power switch S1, from TB1-3 to TB1-4
2. Locate and remove (from the terminal board) the green #12 AWG wire connected to the upper terminal of TB1-4. With an ohmmeter, confirm that the wire is connected to frame ground with a resistance of 0.05 ohm or less. With the ohmmeter, confirm that TB1-4, lower terminal, has a resistance to ground of 5 megohms or more.
3. Connect the green wire, removed from TB1-4, to TB1-5 and, at the same time, jumper TB1-5 to TB1-6 with the U-shaped terminal jumper P/N 150368. Confirm with the ohmmeter that J1-E, J1-F, J1-G, and J2-E, J2-F, and J2-G all have a resistance to ground of 0.05 ohm or less.
4. Unsolder the blue wire from the lug of the F2 fuse holder and solder it to the tip of the F2 fuse holder. When this operation has been performed, both the blue wire and the violet wire will be soldered together at the tip of the fuse holder.

3.6 INSTALLATION

An appropriate Memorex Off-Line Tester and a CE alignment pack (yellow shield, P/N 203142) are needed to perform the necessary operational checks on the drive. To prepare the drive for operation, proceed as follows:

1. Check to be certain the power switch, S1, on the interior control panel, is in the OFF (down) position. Then, connect the primary AC power cable (all cables are shipped in a separate carton) between the AC IN connector, J1, on the interior control panel and the controller.

NOTE

Because the disc drive has ground currents in excess of 5.0 milliamperes, the controller, or control unit to which these drives are connected, must have electrical grounding that contains the following:

a. An insulated grounding conductor that is identical to the grounded and ungrounded branch-circuit supply conductors (except that it is finished to show a green color or green with a yellow stripe) is to be installed as part of the branch circuit that supplies the unit or system.

b. The grounding conductor mentioned above is to be grounded at the service equipment.

c. The attachment-plug receptacles, in the vicinity of the unit or system, are all to be of a grounding type, and the grounding conductors serving these receptacles are to be connected to the grounding conductor that serves the unit or system.

If the drive is one of a string of drives, the second and third drives in each group of three receive their power via the AC OUT connector, J2, on the previous drive. All cables which are connected to the drive must enter the machine through the cable hole in the bottom of the machine. (Reference Figure 1-1).

NOTE

The maximum three-phase current which can be fed through the AC connections on any drive, to power it and succeeding drives in the string, is 26.0 amps per phase.

2. Check to be certain that all the switches on the operator control panel are down.

3. Install the CE pack on the drive. Move the carriage out by hand a short distance to check that the heads will not hit the edges of the discs.

NOTE

This procedure is included as a precaution against attempting to perform a first seek with heads which might be out of line as a result of damage during shipment.

4. Connect the Model 120 Off-Line Tester to the drive as instructed in the Model 120 instruction manual.

5. Turn the main power switch, S1, ON. The logic and power supply cooling fans will come on. Examine the machine for any signs of component overheating.

6. Select START with the START-STOP switch on the operator control panel. The disc pack will begin rotating and the main blower will come on. Following a pack temperature stabilization delay of 60 seconds, the heads will move out to the forward stop and then perform a reverse seek to cylinder 000. If any head chattering (the sound the heads make when they come in contact with the disc) occurs, power down immediately by selecting STOP. Head chattering means that either a head(s) or disc pack is damaged. If no head chattering occurs, proceed with the installation checkout.

7. Check head alignment as described in Section 5.7.

8. Check the index transducer circumferential alignment. The procedure for this check can be found in Section 5.4.

9. Use the off-line tester to perform random seeks in the AUTOCYCLE mode for 10 minutes. Then seek to cylinder 000. Verify that the carriage is at cylinder 000 by checking the cylinder scale on top of the Tee-block.

10. Select STOP with the START-STOP switch. Make certain that the disc pack comes to a complete stop within 10 to 15 seconds after STOP has been selected. This verifies that dynamic braking is working properly.

11. Attach the kick panels to the bottom of the machine with the clips which are already mounted. Replace the two top covers. Be sure the disc pack cover (right-hand) is closed while installing it. Otherwise, the door-open interlock arm may not properly engage the paddle on the index transducer.

12. Select START with the START-STOP switch. When the disc pack motor comes up to speed, open the disc pack cover door. When it is open about 1 inch, the heads should retract and the motor should shut off. Close the disc pack cover door.

13. Use the off-line tester to make a quick write/read check.

    a. Select READ/WRITE with the READ/WRITE-READ ONLY switch.

    b. Write all ONEs with any head on cylinders 000 and 128.

c. Select the READ mode. Monitor the output of the Read Amplifier, A10, by connecting an oscilloscope to pin 4 of A10.

d. The double-frequency (2F) pulses observed on the oscilloscope should be at a 5-MHz rate with less than ±10-nsec jitter between adjacent pulses.

e. Write all ZEROs with the same head on cylinders 000 and 128. The single-frequency pulses (1F) should be at a 2.5-MHz rate.

f. Disconnect the oscilloscope.

14. Select STOP with START-STOP switch, turn the main power switch, S1, OFF and disconnect the Model 120 off-line tester.

15. Connect the controller's bus cable to the BUS IN connector J3 on the interior control panel of the drive. If the drive is not the first drive in a string of drives, connect the cable that comes from the Bus Out connector, J4, of the previous drive to the Bus In connector, J3.

16. If the drive is the only drive or the last drive in a string of drives, plug a line terminator assembly into the Bus Out connector, J4.

17. Connect the proper unit cable from the controller to the Unit connector, J5, on the interior control panel. The controller has a separate unit cable for each drive.

18. When all cables are connected, replace the sheet metal cable cover.

19. All machines, as they are shipped from the factory, have their Index/Sector boards (located in slot B05 on the logic door at the back of the machine and labeled IXSR) wired for the index-only mode. If the sector mode is required, the jumper wire must be removed from between terminals E7 and E8 and installed between either E1 and E2, E3 and E4, or E5 and E6, depending on whether the sector slot count is to be divided by 1, 2, or 4, respectively.

20. Turn the main power switch, S1, ON and then replace the front and rear panels.

21. If the 660-1 drive is one of a string of drives (but not the last drive), it should be checked for proper power-up sequencing. To do this, first make certain that a disc pack is on the drive and that the disc pack cover is closed. Leave the drive's START-STOP switch in the STOP position. Place the next drive's START-STOP switch in the START position. In a power-up sequence from the controller, the drive under test will not come on; it will be bypassed and the next drive in the string will turn on.

22. To make certain that the next drive turns on when the drive being installed comes up to speed, place the START-STOP switch on both drives in the START position. Power up from the controller and observe the first drive come up to speed (70% of spindle drive motor speed). At this time, the spindle drive motor on the second drive should begin rotating.

23. As the last step in the installation check, select STOP with the START-STOP switch. The drive is now ready to perform.

SECTION 4
THEORY OF OPERATION

This section is intended to explain in general terms the basic operations of the disc drive, including: power up, first seek, seeks other than first seeks, read, write, restore, and power down. A discussion of the drive/controller interface is also included.

4.1 INTERFACE

Each drive communicates with the central processing unit through a controller. The drive receives commands and data to be recorded from the controller on its input lines and provides the controller with status information and read data on its output lines.

4.1.1 Timing

The controller must satisfy certain timing requirements in order to instruct a drive to perform operations. The timing requirements associated with several basic drive operations are defined by the timing diagrams of Figure 4-1.

1. Seek to Specified Cylinder and Head (Timing Diagram A)

   In a seek operation, the controller causes the drive's carriage to move to a new cylinder address and the head-setting circuits to enable one of the 20 heads partially. To do this it must:

   a. Set the new cylinder address into the CAR.

   b. Reset the head register.

   c. Set the new head address into the head register.

   d. Start the seek with a Seek Start signal.

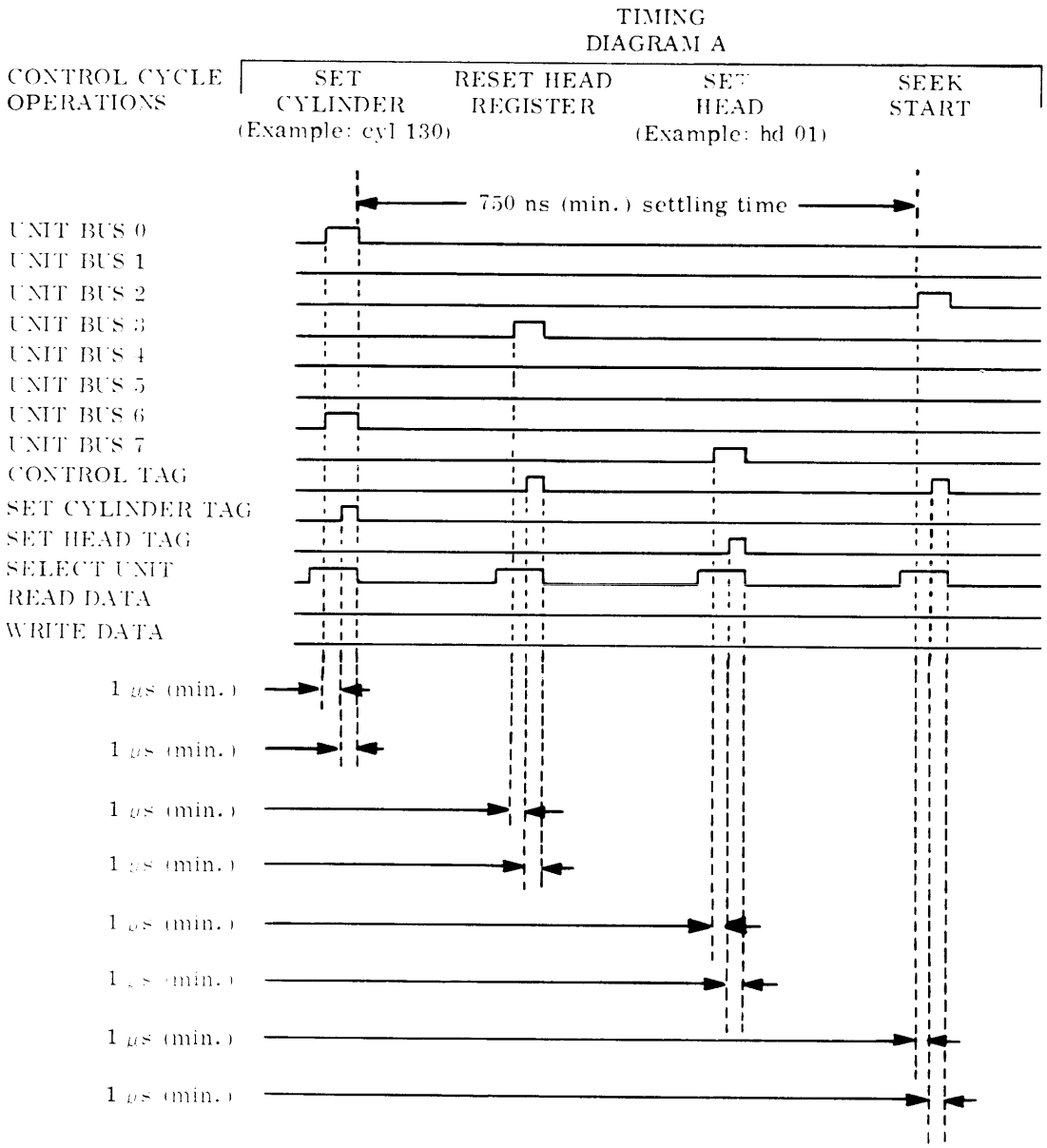
2. Read (Timing Diagram B)

   When the heads are positioned at the correct cylinder with the appropriate address in the head register, the controller may cause the drive to begin reading. To do this it must:

   a. Raise the Control tag line and Unit Bus 5 to select the head.

   b. Raise the Select Unit line and Unit Bus 1 to enable the read gate.

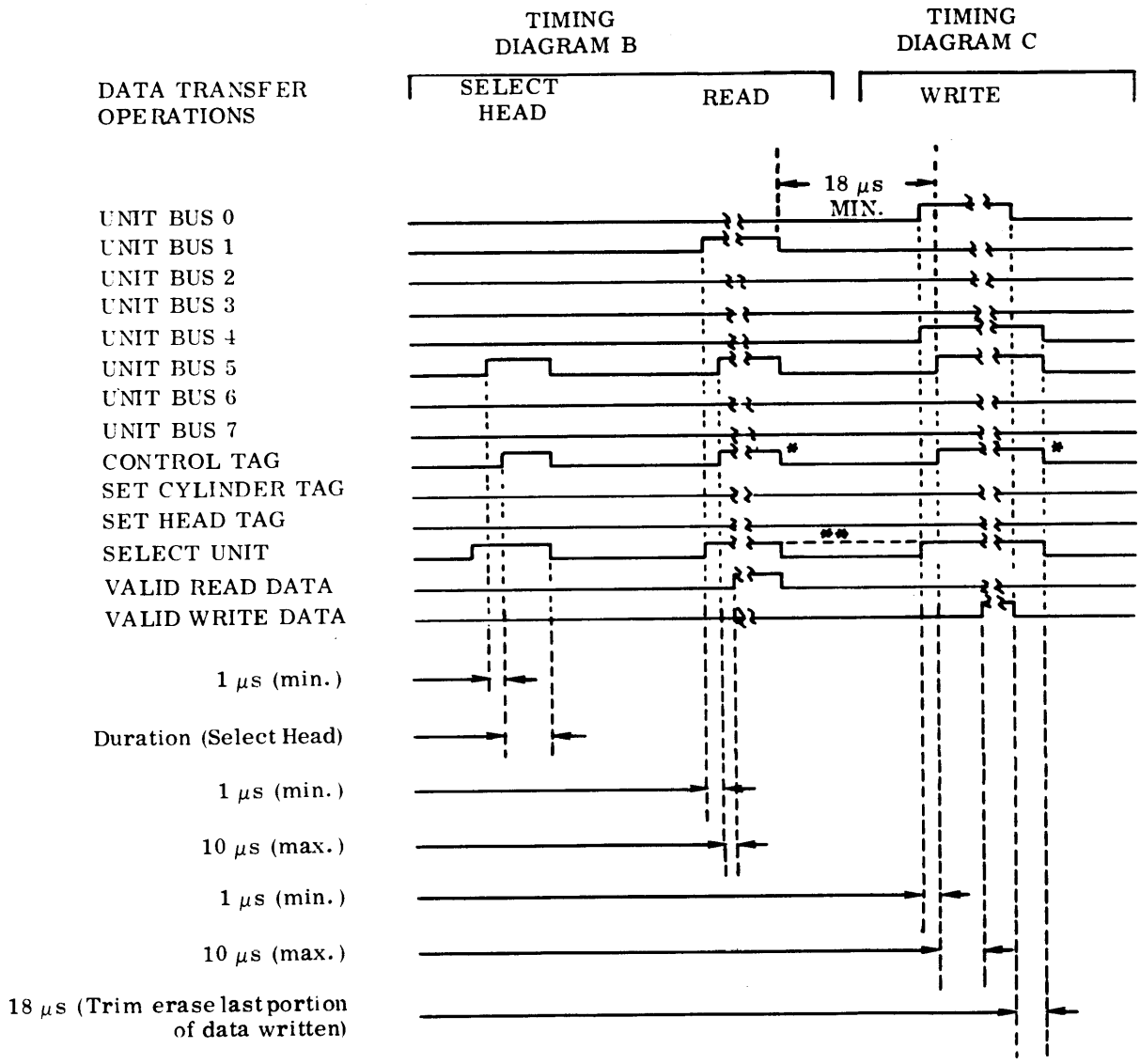
   A read operation may be initiated whenever the drive's Ready line to the controller is active, Unit Bus 0 (Write) is inactive, and the Write Data line is held disabled. Valid read data appears on the Read Data output line 10 μsec after the Control tag line enables the Select Head and Read lines.



GENERAL TIMING DIAGRAM NOTES:

1. These diagrams apply to signals at disc pack drive connectors. No allowance is made for propagation delays.
2. Select Unit must always be raised before command is given so controller can check to be sure only one unit is being selected.
3. All 1 μs times have the tolerance ±200 ns.

FIGURE 4-1. GENERAL TIMING DIAGRAM (Sheet 1 of 3)



* On a read or write operation, control tag's trailing edge must occur before bus lines are changed.

**Select unit may be left enabled between read and write operations.

FIGURE 4-1. GENERAL TIMING DIAGRAM (Sheet 2 of 3)

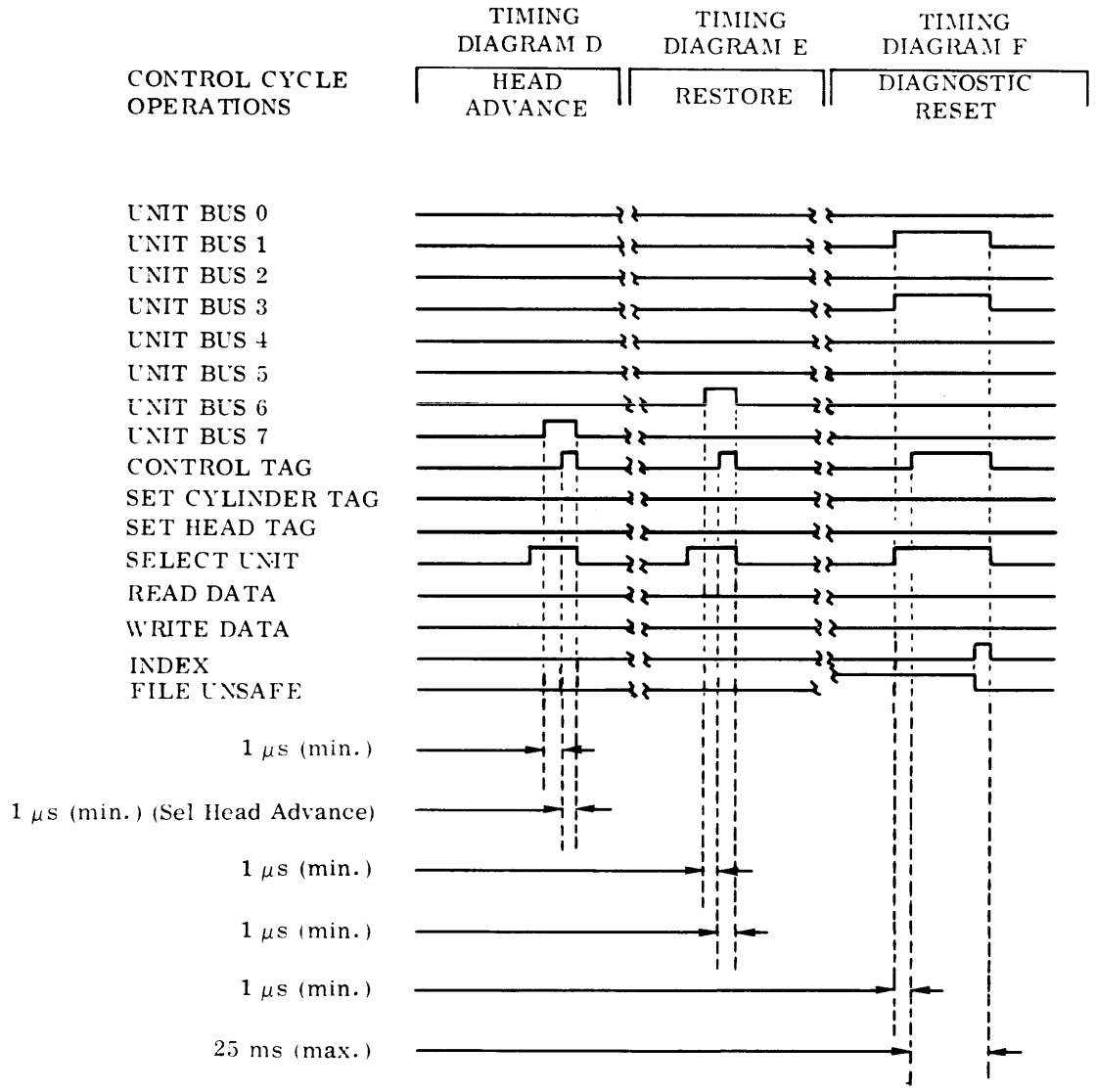


FIGURE 4-1. GENERAL TIMING DIAGRAM (Sheet 3 of 3)

3. Write (Timing Diagram C)

When the heads are positioned at the correct cylinder with the appropriate address in the head register, the controller may cause the head to begin writing. To do this it must:

a. Raise Unit Bus 0 (Write) and Unit Bus 4 (Erase) simultaneously.

b. Raise the Select Unit line (if it is not already active), Control tag line, and Unit Bus 5 to select the head; this must not occur sooner than 18 μsec after a read operation ends or else the erase current transient might alter data on the disc surface.

NOTE

A write operation is usually preceded by a read operation. This is because the controller verifies that the heads are correctly positioned and that the correct head is selected by reading some characteristic track address information before beginning a write operation.

c. When concluding a write operation, Unit Bus 4 must be held active for 18 μsec after Unit Bus 0 is dropped. This is needed to allow the erase current to erase all the way to the end of the track. Since the erase poles trail the write gap by 0.005 inches, removing erase current at the same time the write gate is disabled would leave 0.005 inches of untrimmed data.

Write and erase may be selected any time the Ready line to the controller is active, the drive is not reading, and the READ/WRITE-READ ONLY switch is in the READ/WRITE position. Valid write data appears on the disc surface no later than 10 μsec after the Control tag line enables the Select Head and Write lines.

4. Head Advance (Timing Diagram D)

When a read or write operation uses the tracks of a cylinder in a consecutive sequence, head selection advances one head at a time from the first head selected to the end of the cylinder. To do this, the controller must:

a. Raise the Select Unit line.

b. Raise Unit Bus 7 (Head Advance line during control cycle).

c. Raise the Control tag line to enable the Select Unit and Head Advance lines.

When the head address increments to 20 (one more than the highest head address), the drive sends an End of Cylinder signal to the controller. Refer to Section 4.1.2.2. The head address may be advanced if no other head is already selected.

5. Restore (Timing Diagram E)

Whenever the exact position of the heads is in doubt, the controller can cause them to move to a known position (cylinder 000) by initiating a restore (recalibrate) operation. To do this it must:

a. Raise the Select Unit line.

b. Raise Unit Bus 6 (Restore line during control cycle).

c. Raise the Control tag line.

A restore command may be issued at any time except during a read or write operation.

6. Reset Attention

The drive logic which generates the Attention signal to the controller may be reset by a Reset Attention command from the controller. To do this it must:

a. Raise the Select Unit line.

b. Raise Unit Bus 1 (Read line during control cycle).

c. Raise the Control tag line.

The controller uses the same lines to initiate Reset Attention as it does for Read because Reset Attention is most frequently used just before a read operation. However, Reset Attention may be issued at any time except during a write operation.

7. Diagnostic Reset (Timing Diagram F)

The Diagnostic Reset command is used to reset the file unsafe logic in the drive when that logic has been set as part of a diagnostic routine. To issue a Diagnostic Reset command, the controller must:

a. Raise the Select Unit line.

b. Raise Unit Bus 1 and Unit Bus 3.

c. Raise the Control tag line.

The Diagnostic Reset command may be issued at any time except during a write operation.

4.1.2 Interface Lines

4.1.2.1 Input (Controller to Drive)

1. Select Unit Line

   A separate Select Unit line exists for each drive. This line selects the drive to be used. The Select Unit line goes low and remains low during read, write, and control operations; it goes high when the drive is not selected.

2. Unit Bus Lines (eight)

   These time-shared lines are used to perform control functions and to gate addresses to the drive. Individual Bus Line functions are listed below.

UNIT BUS LINE FUNCTIONS

LINE FROM CONTROLLER	FUNCTIONS DURING		
	CONTROL CYCLE	SET CYLINDER CYCLE	SET HEAD CYCLE
Bus 0	Write	Cylinder 128	
Bus 1	Read	Cylinder 64	
Bus 2	Seek Start	Cylinder 32	
Bus 3	Reset Head Register	Cylinder 16	Head 16
Bus 4	Erase	Cylinder 8	Head 8
Bus 5	Select Head	Cylinder 4	Head 4
Bus 6	Restore	Cylinder 2	Head 2
Bus 7	Head Advance	Cylinder 1	Head 1

NOTE

Control, with Bus 1 and Bus 3 both low, causes a diagnostic reset of FILE UNSAFE.

3. Tag Lines (three)

   These three lines are used to perform setup and control functions by acting as strobe pulses (minimum 1 μsec) and gate enablers (duration variable) for the time-shared bus lines. The following descriptions assume that the Select Unit line is low and that no file unsafe condition exists.

   a. Set Cylinder

      When this tag line is activated (goes low), the drive decodes the existing data on all eight Unit Bus lines as the new cylinder address. This data is transferred into the CAR.

   b. Set Head

      When this tag line is low, the drive decodes the existing data on Unit Bus lines 3, 4, 5, 6, and 7 as the new head address. The bits representing ONEs are transferred into the Reset Head Register as the new address.

c. Control

Commands may be issued to the drive by combining this tag line with one or more Unit Bus lines. The control tag may be either a pulse or a gate-enabling signal depending on the command issued. The five commands which require a control pulse are Reset Attention (Unit Bus 1), Seek Start (Unit Bus 2), Reset Head Register (Unit Bus 3), Restore (Unit Bus 6), and Head Advance (Unit Bus 7). The five commands which require a control gate-enabling signal are Write (Unit Bus 0), Read (Unit Bus 1), Erase (Unit Bus 4), Select Head (Unit Bus 5), and Diagnostic Reset (Unit Bus 1 and Unit Bus 3).

4. Write Data Coaxial Line

Information to be stored on the disc pack is received serially from the controller on this line. A bit is sent at the beginning of each 400-nsec bit cell time for a binary 0, and a bit is sent at the beginning of each 400-nsec bit cell time plus a data bit in the center of the cell time (200-nsec interval) for a binary 1. Pulse width is 70 ±15 nsec, with a fall time of less than 30 nsec.

NOTE

Binary 0 and Binary 1 refer to binary values of the data and not to signal levels.

5. Sequence In Line (Seq In)

This line receives a signal from the previous drive or controller to start the power-up sequencing of the drive. The signal must be delayed approximately one second by the controller after application of primary AC power to the drive.

6. Controlled Ground Line (Cont Grd)

This line receives a signal from the controller to enable the Sequence In signal to set the sequence latch. The controller uses this line to stop the drive before removing the primary AC power from it.

4.1.2.2 Output (Drive to Controller)

1. CAR Lines (eight)

When the Select Unit line is active, the various combinations of low and high levels present on these 8 lines indicate to the controller the cylinder address in the drive.

2. Attention Line

This line goes low when either one of two conditions exists:

a. A normal seek has been completed, or

b. 100 msec have expired since a seek command was given and detenting did not occur.

Typically, the controller initiates a seek or restore operation in a drive and then drops communication with that drive so that it can attend to other peripheral equipment. Attention interrupts (has priority over) the other communication when the drive finishes the seek or restore (either successfully or unsuccessfully). This line does not depend on the signal Select Unit and is reset when the drive is commanded to read. A separate Attention line is provided for each drive via unit cables.

3. Unit Is Selected Line

   This line goes low as a signal to the controller that the drive is selected. A separate line exists for each drive via unit cables.

4. Selected Unit Ready Line

   This line goes low when the drive has satisfactorily completed a seek. The Select Unit line must be active for this line to be active.

5. Selected Unit On Line

   This line goes low when heads have been loaded and the drive is ready to read or write.

6. Selected Unit Index Pulse Line

   This line goes low for 2.7 μsec when an index slot is detected. The Select Unit line must be active for this line to be active.

7. Selected File Unsafe Line

   This line goes low when a selected drive is unsafe for operation.

8. Selected Unit Seek Incomplete Line

   This line goes low as a signal to the controller that the access mechanism failed to reach a normal detent position within 100 msec or less. The Select Unit line must be active for this line to be active.

9. Selected Unit End of Cylinder Line

   This line goes low when the selected drive's head advance logic has reached the end of the present cylinder (head address of 20). The signal informs the controller that there are no more tracks in that cylinder. The Select Unit line must be active for this line to be active.

10. Read Data Coax Line

    The information read off the disc pack is sent to the controller on this line in the form of negative-going pulses 70 ±15 μsec wide. A binary 0 is represented by a pulse at the beginning of each 400-nsec bit cell time. A binary 1 generates two pulses during the bit cell time (one every 200 nsec).

11. Composite Index/Sector Pulse Line

    This line goes low each time an index or a sector slot is detected.

12. Selected Unit Read Only Line

    This line goes low when the READ/WRITE-READ ONLY switch on the operator control panel is in the READ ONLY position. The Select Unit line must be active for this line to be active.

13. Selected Unit Write Current Sense Line

    This line goes low when Write current is flowing in any head on the selected drive.

14. Heads Extended Line (common to all drives)

    This line is used in the controller as an indication that a drive or drives have heads extended. This is not a logic level signal but a switch closure to ground. Its maximum sink current from a positive external voltage source is 100 ma. This switch is intended to prevent the controller from powering down on a drive or string of drives until all heads have been retracted.

15. S quence Out Line (Seq Out)

    When the drive motor reaches 70% of its operating speed (or the START-STOP switch is in the STOP position), the drive provides 0 vdc to the Sequence In line of the next drive in the string. If the main power switch is off, Seq In bypasses the drive's power-up circuitry to become Seq Out. This permits the remaining drives to be started.

16. Selected Unit Sector Pulse Line

    This line goes low when a sector slot is detected on the disc pack. The Select Unit line must be active for this line to be active.

4.2 POWER UP

Because the starting current of a 660-1 disc drive is much higher than its operating current, simultaneous starting of multiple drives could result in a power line overload. To avoid this, the drives in a multiple drive system are automatically started up in sequence. The first drive to power up provides a sequence signal to the second drive so that it can power up. When it powers up, it provides a sequence signal to the third drive. This sequencing continues until the last drive in the string is supplied with the sequence signal.

When the initial power is turned on, the sequence circuitry in all system drives is reset in preparation for power-up instructions from the controller. The up-speed circuitry is also reset at this time.

In order for the controller to power up a drive, the following conditions must be met by the drive: disc pack installed, disc pack cover closed, main power switch on, and the START-STOP switch in the START position.

When the controller commands the first drive in a string to power up (by enabling its Sequence In line), primary AC voltage is first applied to the disc pack motor. The motor starts and causes the spindle and disc pack to begin rotating.

The slotted disc on the bottom of the pack induces pulses in the index transducer. The rate of these pulses increases with disc pack rotation speed and when the disc pack reaches 70% of its operating speed, the up-speed circuitry is enabled by the index pulses. The up-speed logic generates a signal which causes a sequence signal to be sent to the next disc drive in the string. The signal from the up-speed circuitry also starts a 60-second delay in the first drive to allow the disc pack's temperature to stabilize before the first seek is performed. When the delay times out, the drive's logic is ready to perform a first seek.

If primary AC power is not available to a particular drive (the main power switch is open), that drive is bypassed in the power-up sequence so that the next drive is able to power up. A drive's power-up logic is also bypassed if its START-STOP switch is in the STOP position. Although that drive does not power up, it generates a sequence signal for the next drive in the string.

4.3 FIRST SEEK

During a 60-second warmup delay, the Servo Sequencer logic, CAR, PAR and delay timers (Seek Incomplete, Forward Seek and Ready), are held reset. When the warmup delay times out, the Servo Sequencer logic is enabled. The Servo Sequencer logic consists of four flip-flops and associated gates which initiate each step (logic state) in any seek or restore sequence. This logic controls the progress of the servo and other access logic from state to state. The sequencing logic is synchronized by free-running clock pulses generated by the transducer oscillator.

The first strobe pulse following the warmup delay steps the Servo Sequencer into the first state in a first seek sequence (this sequence is identical to a restore sequence). At this point, a brief Forward Seek delay is initiated. This delay has no function at this time since the detents are not engaged. It is intended for forward seeks and restore operations to allow the detents to disengage (pick) before applying current to the servo. Following this delay, a prescribed amount of current is fed to the linear motor to start it moving forward slowly.

NOTE

There is one insignificant difference between a first seek sequence and a restore sequence. A first seek always begins with the carriage fully retracted; the carriage could be at any position along the carriage way at the beginning of a restore operation.

The Servo Sequencer monitors the forward velocity line and senses when the line goes true and subsequently false. The CAR and PAR reset signals are remoed when the line goes true. When the line goes false, it indicates that the carriage has come to rest against the forward carriage stop. With the carriage at the forward carriage stop, the forward current to the linear motor is removed and a holding current is applied. This holding current keeps the carriage stable while the logic prepares to begin a reverse seek.

A count of 202 is forced into the direct set inputs of the PAR. A present address of 202 is used even though the carriage is actually positioned at cylinder 203. This is because the logic on the transducer amplifier board causes the logic to miss the first count during the reverse portion of a first seek or restore operation. Another Forward Seek delay is begun, and a Seek Incomplete delay begins. As soon as the Forward Seek delay times out, the Servo Sequencer logic initiates a normal reverse seek to cylinder 000 (since the CAR flip-flops are still reset, the carriage destination is cylinder 000). The Seek Incomplete delay determines the amount of time the positioning mechanism is allotted to complete the seek before a Seek Incomplete signal is sent to the controller.

An adder circuit derives the algebraic difference between the contents of CAR and PAR. This difference is the number of cylinders the carriage must travel to arrive at cylinder 000. The output of the adder is converted to a voltage that corresponds to a velocity desired for a seek of this length. This voltage is converted to a current which is applied to the linear motor. The motor accelerates the carriage toward cylinder 000.

As the carriage (and linear motor bobbin) move, a voltage is induced in the tachometer. This voltage is fed back and compared with the desired velocity voltage. Current to the motor is controlled by the algebraic difference of the desired voltage and the actual voltage. Consequently, the current is increased, decreased, or reversed, depending on the relative values of the desired and actual velocity voltages.

As the carriage approaches its destination, the voltage programming the desired velocity is decreased by steps. Each time it decreases, it drops below the actual velocity voltage fed back by the tachometer. The excess of actual voltage causes the carriage to decelerate at each step.

When the carriage reaches cylinder 000, contents of the CAR and PAR agree (difference is 0). This generates a Compare signal which causes the reverse current to the motor to be replaced by a small amount of forward current. Momentum carries the carriage almost one cylinder past cylinder 000. By then, the forward current overcomes momentum and causes the carriage to reverse direction of travel. The Compare signal also activates the detent actuator logic so that the detent pawls are in the process of engaging the rack during the turnaround period. Since the carriage reverses direction before one of the pawls can completely set, the carriage is detented while it is traveling in the forward direction. As soon as the tachometer senses the lack of forward velocity a Ready delay is initiated. This delay provides time to allow the small mechanical vibrations caused by detenting to fade before a Ready signal is sent to the controller. Following this delay, the drive signals the controller that it is ready for a seek command to some cylinder.

If, for some reason, the carriage is not detented within the time allowed by the Seek Incomplete delay, a Seek Incomplete signal is sent to the controller, which will normally respond by initiating a restore operation. A restore operation is identical to a first seek. Its purpose is to bring the carriage to a known position (cylinder 000) from an unknown position.

4.4 SEEKS OTHER THAN FIRST SEEKS

The controller initiates a seek while a drive is in the ready state. To do this it must first select the drive. It then transfers the address of the destination cylinder to the drive on the eight Unit Bus lines. This address is gated into the CAR in the drive during the Set Cylinder cycle. Next, the head register is cleared when Unit Bus line 3 goes low during the Control cycle. Then, the head address is transferred to the drive on Unit Bus lines 3 through 7 and gated into the head register during the Set Head cycle. Finally, the drive is enabled to begin the seek when Unit Bus 2 goes low during the Control cycle. This generates a Seek Start signal in the drive logic.

The Seek Start signal causes the Servo Sequencer logic (refer to the First Seek discussion for a description of the Servo Sequencer logic) to advance to the first state in a normal seek sequence. In this state, a comparison (algebraic addition) is made between the complement of destination address (which is stored in the CAR) and the present address of the carriage (which is stored in the PAR). If these two addresses are the same, no seek is performed. If they are different, the difference represents the number of cylinders the carriage must travel to reach its destination. The sense of the carry out of the Adder determines the direction of travel (false = forward seek and true = reverse seek).

Forward Seek

If the comparison by the Adder logic results in a forward seek, a brief Forward Seek delay is begun and holding current to the linear motor is dropped. The delay gives the carriage time to relax its forward pressure against the detent pawls after holding current drops so that the detent actuator logic can pick the detent pawls clear of the detent rack. At the same time the Forward Seek delay begins, a Seek Incomplete delay is initiated. As soon as the Forward Seek delay times out, the detent actuator logic disengages the detent pawl, and Seek Forward signals are generated. One of these signals enables the output of the Adder logic and the other enables the up-down counter in the PAR.

Output of the Adder goes to speed decode logic which encodes the difference into a series of seven forward- or reverse-velocity signals. These velocity signals are converted by the Servo Sytem to a voltage that corresponds to a programmed velocity. This voltage is converted to current which is applied to the linear motor. The amount of current applied determines the peak velocity the carriage will reach and the polarity of the current determines the direction of travel. For longer seeks, the peak velocity will be greater.

As the carriage reaches each new cylinder, the cylinder transducer amplifier generates a count pulse that alters the PAR contents by one (increases during forward seeks, decreases during reverse seeks). When the contents of the PAR equal the contents of the CAR, the carriage has reached the destination cylinder. At this point, a Compare signal is generated and the last step of the positioning voltage is dropped. In its place, a low-level Forward Detent Velocity signal is generated. This signal provides a small amount of current to the linear motor in the forward direction. The Compare signal activates detent actuator logic so that the detent pawls begin to engage (set).

When one of the detent pawls fully sets against a detent rack tooth, the carriage stops moving. The zero velocity detector senses this and causes the Forward Detent Velocity voltage to be replaced by a small amount of holding current, also in the forward direction. The Ready delay is initiated. This delay provides time to allow the small mechanical vibrations of the carriage to fade before a Ready signal is sent to the controller. Following this delay, the drive signals the controller that it is ready for the next operation. In addition to the Ready signal, the drive sends an Attention signal to the controller. This signal serves as an interrupt to the controller and as soon as it completes whatever operation it is engaged in at the time it receives the Attention signal, it reselects the drive and instructs it to perform some operation (probably a read or write operation).

Reverse Seek

A reverse seek differs little from a forward seek. If the Adder logic generates a reverse seek command instead of a forward seek command, the detent pawl is picked immediately and reverse current is applied to the linear motor as soon as holding current is dropped. This is possible because of the relative slopes of the detent pawl teeth and detent rack teeth. When the carriage is traveling backwards, the detent pawls will not lock up against a tooth face. When the destination cylinder is reached during a reverse seek (Compare signal is generated) the reverse current to the motor is replaced by Forward Detent Velocity current and the detent pawls begin to engage just as during a forward seek. However, momentum carries the carriage almost one full cylinder past the destination cylinder before the Forward Detent Velocity current can overcome it and reverse the direction of travel. The carriage begins moving forward and then the detent pawl sets. This turnaround portion of a reverse seek is necessary to allow the detent pawls to engage while the carriage is moving forward. As soon as the zero velocity detector senses that the carriage has stopped moving, the Ready delay begins. Following the delay, Ready and Attention signals are sent to the controller.

4.5 READ/WRITE OPERATION

After the heads are positioned to the prescribed cylinder, the controller selects one head to read. It does this by activating the Select Unit line and Unit Bus 1 to enable the read gate and then Unit Bus 5 and the Control tag line to select the head whose address is contained in the Head Address Register. To initiate a write operation, the controller activates Unit Bus 0 and Unit Bus 4 simultaneously. Then it activates the Select Unit line, Control tag line, and Unit Bus 5 to select the head.

Although the ultimate purpose of the seek may be to write data on the track, the selected head will usually be instructed to read first. This is because it is necessary for the system to verify the accuracy of the seek by reading bytes of information which identify the track (e.g., home address). However, since it is easier to understand the read operation after learning how data is recorded, the write process is described first.

4.5.1 Write Operation

Information is recorded on a disc surface using the double-frequency nonreturn-to-zero technique. The stream of data is received from the controller as a series of clock and data pulses. Every 400 nsec (2.5 MHz) a clock pulse arrives, establishing a time base; the interval from clock pulse to clock pulse is called a bit cell time. If there is no data pulse between two clock pulses, that bit cell time represents a binary 0. A bit cell time containing a data pulse midway between two clock pulses (200 nsec after a clock pulse and 200 nsec before the next clock pulse) represents a binary 1.

These pulses enter the Write logic where they are amplified by a line receiver. The pulse output of the line receiver toggles a complementary flip-flop. The outputs of the flip-flop are used alternately to cause the polarity of a flux field in the read/write head to reverse each time a pulse is received. The flux field is used to polarize ferric-oxide particles on the disc surface as the disc rotates under the head. Each flux reversal causes a polarity reversal in the recorded track. Consequently, each polarity change in the recorded track corresponds to either a clock or data pulse and is called a bit.

The read/write head used by the drive consists of a ferrite core whose ends are separated by a very small gap. A center-tapped coil is wound around a portion of the core. When current passes through the coil in one direction, a flux field builds up across the gap in the core. This is shown in Figure 4-2. The polarity of the flux field depends on the polarity of the current.

When the head is loaded (flying just above the disc surface), the gap in the core is close enough to the disc surface for the flux field to flow into the disc coating and magnetize its ferric-oxide particles. This is the flux field that reverses with each clock or data pulse, recording a series of binary ones and zeros that correspond to the series received from the controller. See Figure 4-3.

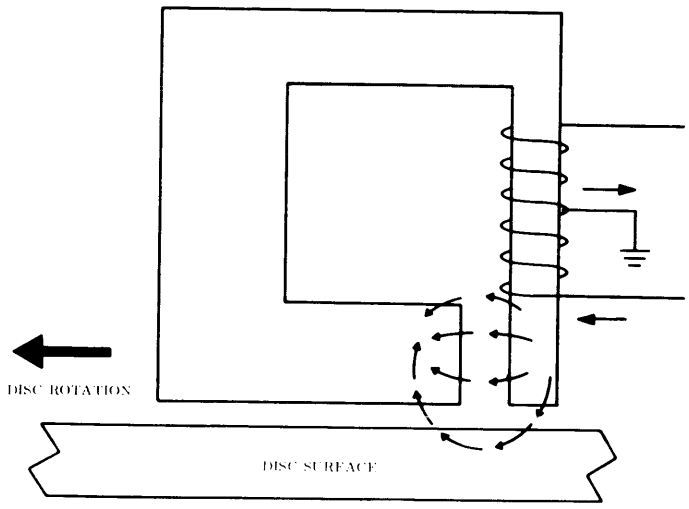


FIGURE 4-2. READ/WRITE COILS AND GAP

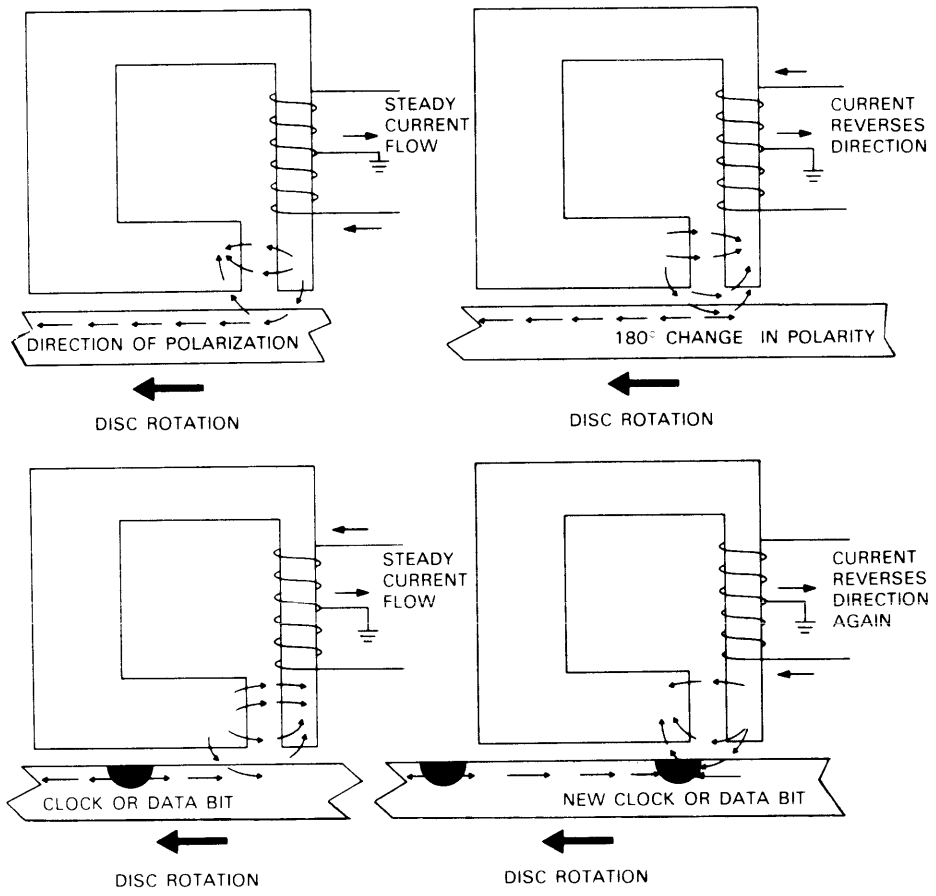


FIGURE 4-3. BIT GENERATION BY FLUX REVERSAL

As a track of data is being written, narrow bands on each side of the track are erased. This is done to allow for slight variations in head positioning. It assures that there is no residual data from the previous recording along the edges of the new track. The side trimming is accomplished by a horseshoe-shaped electromagnet which is fixed to the core of the read/write gap and then under the side trim erase poles (see Figure 4-4).

The coil on the erase poles is actually a pair of series-wound coils which are connected to the read/write coils in a Y configuration. The common point of these coils is tied to the head selection logic (see Figure 4-4). When the head is selected to write and erase (the common point goes low), direct current is applied to the erase coils. The steady flux induced by the direct current eliminates any unwanted polarity reversals (bits) along the sides of the new data track.

In addition to clearing a band of disc surface on each side of the track, the side trim erase narrows the data track slightly as a result of fringing from the erase poles. A new data track is narrowed from its original width of approximately 0.007 inches to approximately 0.005 inches.

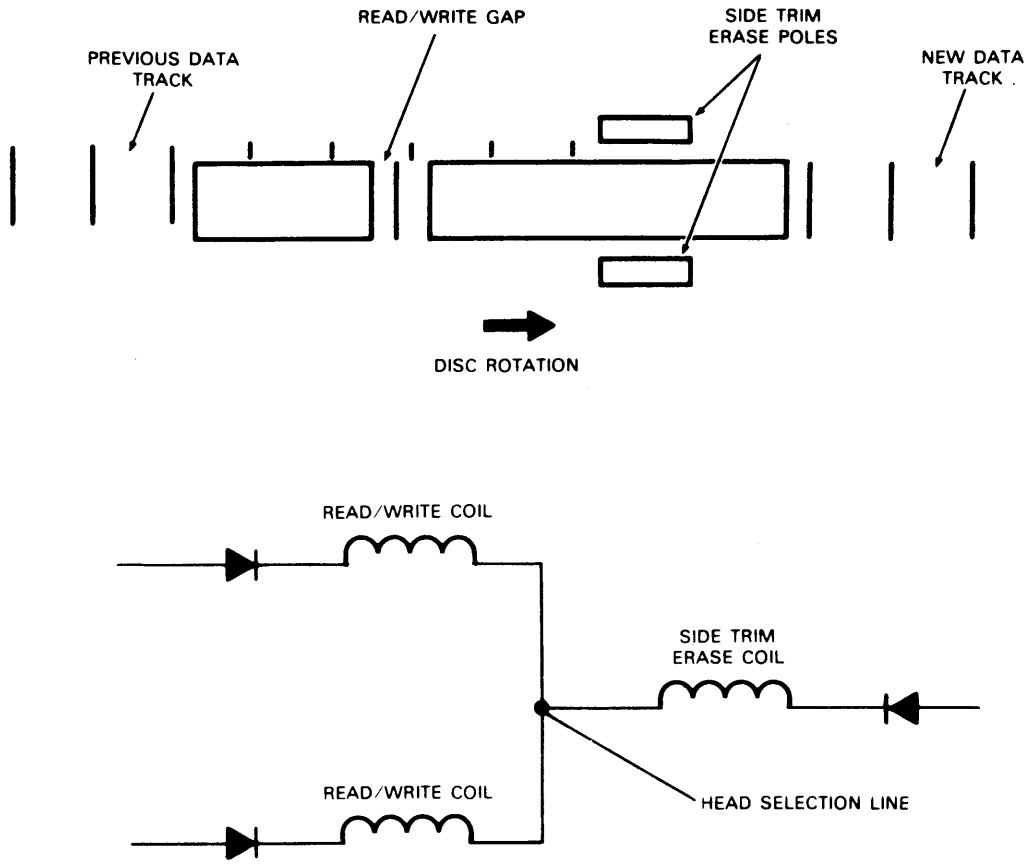


FIGURE 4-4. SIDE TRIM ERASE CONCEPT

4.5.2 Read Operation

During a read operation, the selected head flies over a previously written data track. As a length of track that is magnetized in one direction passes under the read/write gap, the steady magnetic field of the track induces no voltage in the read/write coil. Therefore, no voltage output appears on the read/write coil leads. Whenever a bit passes under the gap, the direction of magnetic flux reverses under the read/write coil and a signal is induced into the read/write coil, providing a signal to the Read Preamplifier.

The Read Preamplifier differentiates this head output signal so that each voltage peak becomes a zero crossing. That is, in the output of the Read Preamplifier, the zero crossings represent data bits. This output goes to the Read Amplifier via line drivers.

The Read Amplifier filters and amplifies the Read Preamplifier output. The amplified read signal is then limited to produce a square wave which is then shaped into a series of pulses with a duration of 70 nsec. These pulses are replicas of the original clock and data pulses received from the controller.

4.6 POWER DOWN

4.6.1 By Operator

When the START-STOP switch is placed in the STOP position, the heads begin to retract and the Servo Sequencer logic resets to state 0000. This assures that the servo system will be prepared to perform a first seek following the next power up. When the heads are fully retracted, the Heads Extended-Heads Retracted switch transfers to the Heads Retracted position. A safety interlock prevents turnoff of the drive motor unless the heads return to the fully retracted position. The disc pack motor leads are switched from primary AC voltage to the dynamic braking circuit. Dynamic braking current (DC) is applied to the motor for 12 seconds, bringing the motor, spindle, and disc pack to a smooth halt.

4.6.2 By Controller

When the controller powers down a drive it removes the Controlled Ground line, resetting the sequence latch. The output of the sequence latch causes the heads to retract and AC voltage to be removed from the disc pack motor. Dynamic braking is not applied in this case so the disc pack motor slowly coasts to a stop.

SECTION 5
ADJUSTMENT AND REPLACEMENT PROCEDURES

The procedures in this section are provided as an aid for servicing a drive. Alignment and adjustment procedures described herein should not be employed unless a problem has been specifically identified by careful troubleshooting analysis.

5.1 SAFETY PRECAUTIONS

Although the drive utilizes solid-state circuitry, the presence of primary AC voltage and the existence of moving parts require caution when servicing the machine. The use of standard safety practices and observing the precautions listed below and elsewhere in this manual will prevent personal injury or damage to the drive.

1. Whenever working on primary power circuits, make certain the drive is unplugged at the AC IN and AC OUT connectors.

2. Unplug or plug in printed circuit boards only if the main power switch (S1) on the interior control panel is off.

3. Operating a drive with the shroud area cover removed should be done only when necessary for making field adjustments. Operating without the cover greatly increases the head exposure to disc interference due to airborne foreign particles.

4. Keep fingers away from spinning discs when operating a drive without the shroud assembly.

5. Keep hands away from fast seeking read/write head arms.

6. Keep watches and tools away from the linear positioning motor, as it is surrounded by a strong magnetic field.

7. Keep hands away from the drive belt.

8. Never force an electrical seek without a spinning disc pack unless all head assemblies have been removed. Read/write heads or disc surface could be damaged.

9. Do not operate the drive with the Read Amplifier board present, but with either Read/Write Amplifier (left or right) unplugged. Damage may result to the Read Amplifier board.

10. Grounding any back panel pin for test purposes may be necessary; however, do not connect any pin to a supply voltage unless directed by a test procedure or damage can result.

11. Do not operate drive with power supply gate open.

5.2 TOOLS AND TEST EQUIPMENT

A list of tools and test equipment useful in maintaining and repairing the drive is given in Table 5-1. Items asterisked are necessary to perform procedures in this section. Other items are for making repairs, for performing service operations that cannot be performed easily with standard tools, or for installation of future field changes.

There are two versions of the 120-2 Off-line Tester. The difference between the two is the connection to the drive. One version connects in the front of the drive at J3 and J5. Disconnect the control unit Bus In, Bus Out, and Unit cables from drive connectors J3, J4, and J5 and connect the Bus In and Bus Out cables together. Replace the Bus In and Unit cables with the corresponding off-line tester cables. If there is a terminator in location J4, remove it.

The other version (latest) connects at the back of the drive's logic gate at J13 and J14. Disconnect the two cables already located at these points on the drive and connect the tester cables in their place. This connection allows the drive to remain connected to the control unit. The only visible difference between the two testers is the size of the cable plugs—big plugs connect in the front of the drive and the small plugs connect at the back of the logic gate.

TABLE 5-1. TOOLS AND TEST EQUIPMENT

ITEM	DESCRIPTION
Volt Meter	VTVM, 10, 50, and 100 vdc scale, 1% accuracy
Oscilloscope	Dual trace, to 50 MHz, with two 1:1 probes
20 Surface Disc Drive Special Tools	Memorex Kit P/N 202148 CONSISTING OF: *Logic Extender PCB (P/N 1981) *Power Supply Extender PCB (P/N 1986) *20 Surface CE Disc Pack (P/N 203142) Amp Coax Pin Extractor (P/N 150690) Amp Pin Extractor 16-20G (P/N 150691) Amp Pin Extractor 10GA (P/N 150692) Elco Pin Extractor (P/N 150792) Marking Ink Solvent (P/N 153503) Fastener Field Kit (P/N 200505) *Carriage Moving Tool (P/N 200515) *Detent Replacement Tool (P/N 200540) *Head Clamp Torque Wrench (P/N 200552) Wirewrap Tool (P/N 200553) Wire Unwrap Tool (P/N 200554) *Head Adjustment Tool (P/N 200555) Lubrication Kit (P/N 200824) *Head Weldment Preloader (P/N 200945) *Carriage Torque Wrench (P/N 200965) *120-2 Off-Line Disc Drive Tester (P/N 201291) Head Cleaning Kit (P/N 202159) *Carriage Alignment Tool Gauge (P/N 201452) *Carriage Alignment Tool Arm (P/N 201453) *Linear Motor Alignment Tool (P/N 202419)

5.3 POWER SUPPLY ADJUSTMENTS

Before proceeding with any other maintenance adjustment, always check the power supply voltages using the procedures given below. If the output of an individual power supply is within the limits specified do not change the adjustment. If a power supply output is outside the specified limits, adjust the output potentiometer so that the power supply delivers the exact voltage required.

5.3.1 ±15V +5V Power Supply

Adjustment of the ±15V +5V Power Supply (P/N 001911) requires separate adjustment procedures for each power supply output. These procedures are given in the following paragraphs, and require the use of a voltmeter with an accuracy of at least 1%.

NOTE

Always have a drive running and warmed up (on for at least 15 minutes) before checking or adjusting a power supply.

5.3.1.1 ±15-Volt Supply

Check for +15 vdc at TP3 on board C02. If the output at TP3 is not within the range +14.25 to +15.75 volts, adjust potentiometer R8 to provide +15.0 volts at TP3. To increase the voltage output, turn the potentiometer clockwise.

Check for -15 vdc at TP2 on board C02. If the output at TP2 is not within the range -14.25 to -15.75 volts, adjust potentiometer R18 to provide -15.0 volts at TP2. To increase the voltage output, turn the potentiometer clockwise.

5.3.1.2 +5-Volt Supply

The +5-volt power supply is factory set and normally does not require field adjustment. The output voltage from this supply is monitored by a 5-Volt High-Low Detector circuit located on the Transducer Amplifier PC board (B06).

If the output of the +5-volt power supply should exceed the threshold of the high detector, or fall below the level of the low detector, the circuits will trigger silicon-controlled rectifier SCR 1 (located on the side of the logic gate), thus clamping the +5-volt power supply to ground. This initiates an Emergency Heads Retract signal and causes the drive to shut off.

There are two designs of High-Low Detector circuits in existence, and procedures for adjusting the +5-volt power supply are dependent upon which design is used. The design configuration may be determined by noting the EC level of the Transducer Amplifier PC board (TAMP).

1. Adjustment procedure for drives with **TAMP at EC level 480 or lower**

NOTE

This procedure requires a voltmeter capable of resolving +5.0 volts with an accuracy of ±5.0 millivolts.

a. Measure the high threshold at TP8 of board B06. It must be +5.20 ±0.01 volts. If the threshold is out of this range, adjust potentiometer R44 (bottom potentiometer on board B04) until the voltage at TP8 is +5.20 ±0.01 volts.

b. Measure the low threshold at TP4 of board B06. It must be 4.80 ±0.05 volts. If the threshold is out of this range, board B06 must be replaced.

c. Measure the +5-volt power supply level at TP6 of board B06. It must be +5.00 ±0.05 volts. If the threshold is out of this range, adjust potentiometer R31 (middle potentiometer on board C02) until the voltage at TP6 is +5.00 ±0.01 volts.

d. Test the operation of the 5-Volt High-Low Detector circuit in accordance with item 3 below.

2. Adjustment procedure for drives with **TAMP at EC level 487 or higher**

NOTE

This procedure requires a voltmeter that has a ±2% to ±5% accuracy and can be used as a null detector (i.e., differentially).

a. The voltage at TP8 of board B06 is factory set by means of a precision zener diode to +5.60 ±0.05 volts and is not field adjustable. Verify that this voltage is correct within the accuracy of the instrument.

NOTE

The zener voltage above is used to generate the high and low thresholds, and a reference voltage. This reference voltage is brought out to TP26 of board B06.

b. The reference voltage at TP26 of board B06 is factory set to +5.10 ±0.06 volts and is not field adjustable. Verify that this voltage is correct, within the accuracy of the instrument.

NOTE

The 5-volt power supply in a drive with a TAMP at EC 487 or higher is nominally set to +5.1 volts. The high threshold is 5.4 volts and the low threshold is 4.8 volts, thus giving a DC noise immunity of ±0.3 volts nominal.

c. Measure the voltage difference between the reference voltage at TP26 of board B06 and the 5-volt supply level at TP6 of board B06. The voltage must be 0.0 ±0.05 volts. If not, adjust potentiometer R31 on board C02 (middle potentiometer) until the voltage difference between TP6 and TP26 of B06 is 0 volts ±10 millivolts.

d. Test the operation of the 5-Volt High-Low Detector circuit in accordance with item 3 below.

3. Test procedure for 5-Volt High-Low Detector Circuit, all EC levels

a. Allow the drive to complete a First Seek.

b. Jumper pin 22 to pin 18 of the TAMP PC board (B06). This raises the voltage on the high detector above the high threshold, causing the following actions which must be verified.

(1) The +5-volt power supply output is clamped to ground (between 0.0 and +1.2 volts).

(2) The carriage is fully retracted.

(3) The servo is disabled (i.e., no motor current is measured at current sense resistor R5).

c. Turn off the main power switch (S1) and START-STOP switch (S2).

d. Turn on the main power switch. The level of the +5-volt power supply must go to its nominal value; +5.0 volts for drives with TAMP PC boards of EC 480 or lower, and +5.1 volts for drives with TAMP PC boards of EC 487 or higher.

e. Jumper pin 22 of the TAMP PC board to ground (any pin A or Z). This lowers the voltage on the low detector below the low threshold, which must clamp the level of the +5-volt power supply to ground. Verify that the 5-volt level is between 0.0 and +1.2 volts.

f. Return the drive to service.

5.3.2 ±36-Volt Supply

With the machine running and warmed up (on for at least fifteen minutes), check for +36 vdc at TP4 on board C03. If the output at TP4 is not within the range +35.0 to +37.0 volts, adjust potentiometer R8 to provide +36.0 volts at TP4. To increase the voltage output, turn the potentiometer clockwise.

Check for -36 vdc at TP1 on board C03. If the output at TP1 is not within the range -35.0 to -37.0 volts, adjust potentiometer R18 to provide -36.0 volts at TP1. To increase the voltage output, turn the potentiometer clockwise.

5.3.3 ±15-Volts Servo Power Supply

This ±15 volts is used by boards C01 and B04 and is independent of the ±15-volt supply described previously in this section.

The Servo Driver board (C01) has two potentiometers that are adjusted at the factory to provide the ±15V used by boards C01 and B04 (this ±15V is independent of the ±15V supplied to other logic). These voltages should be verified before making any adjustments to the servo.

1. Connect a digital voltmeter between pins N and R of B04 (R is ground).
2. Adjust R35 (bottom potentiometer) on C01 to +15 ±0.150V.
3. Connect the digital voltmeter between pins P and R of B04 (R is ground).
4. Adjust R41 (top potentiometer) on C01 to -15 ±0.150V.

This power supply adjustment procedure is also included as part of the servo adjustment procedure, given elsewhere in this section.

5.3.4 +5-Volts Servo Power Supply

The +5-volt servo power supply is contained on Servo Protect PC board B02 (when present), and is not field adjustable. Verify that the voltage at TP11 on board B02 is between +5.0 volts to 5.2 volts. If not, board B02 must be replaced.

5.4 INDEX TRANSDUCER BLOCK ALIGNMENT

Accuracy of carriage tracking and alignment of the index transducer block are checked using the burst track located at cylinder 118 of the CE disc pack (yellow shield; P/N 203142). The following alignment check and adjustment procedures assume that the preparations described in paragraph 5.7.1 have been completed.

5.4.1 Transducer to Index Disc Gap (Radial Adjustment)

The gap between the index disc and the back of the index transducer is set at the factory to assure correct amplitude at the transducer output. Normally, no field adjustment is necessary unless an index transducer is defective. This adjustment is important to keep the contact between the disc and the index transducer to a minimum. Failure to do so may produce contamination, which could lead to HDI. If a check of the transducer outputs indicates that adjustment of the gap is necessary, perform the following steps.

1. Install a disc pack on the drive and leave the drive turned off.

2. Loosen the locking nut on the radial adjustment setscrew. This screw is located on the back of the index transducer.

3. Turn the setscrew counterclockwise while rotating the disc pack by hand.

4. Stop turning the setscrew when the disc begins to rub slightly against the index transducer.

5. Turn the setscrew in one-fourth turn (90° clockwise) so that the disc no longer rubs against the index transucer.

6. Hold the setscrew steady and tighten the locking nut.

7. Start the drive and with both top covers on and closed, measure the amplitude of the negative lobe at TP20 on board B06. If it is less than 275 mv (Figure 5-1), the adjustment has been performed incorrectly or the transducer is defective.

NOTE

This adjustment affects the transducer circumferential alignment. Transducer circumferential alignment must be checked after the radial adjustment is completed.

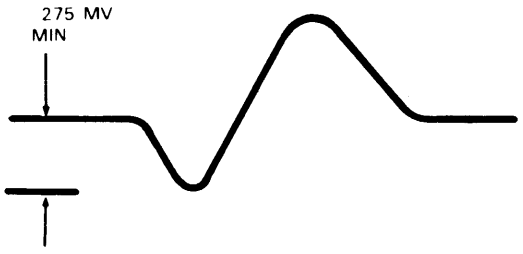


FIGURE 5-1. INDEX TRANSDUCER WAVESHAPE

5.4.2 Index Transducer Circumferential Alignment Check

1. Install a CE disc pack and connect an off-line tester to the drive. Refer to the operating manual that accompanies the tester for instructions on how to install and operate the tester.

2. Use an oscilloscope with direct probes (1:1 attenuation). Set the display to A-B. Set the vertical scale at 50 mv/cm and the sweep speed to 1 μsec/cm.

   Connect the two scope probes to TP4 and TP5 on A10. Sync on +Index (TP2 on board B05).

3. Turn the drive on, position the carriage to cylinder 118, and select either head 09 or 10.

4. Check the pulse-burst timing of the selected head. The scope trace should resemble the one illustrated in Figure 5-2. The pulse burst should occur 3 μsec ±2 μsec after the leading edge of +Index.

5. Repeat the check on the other head (09 or 10). The pulse-burst timing should be between 0 and 10 μsec. If the pulse-burst timing is off for both of these heads, the index transducer block requires alignment.

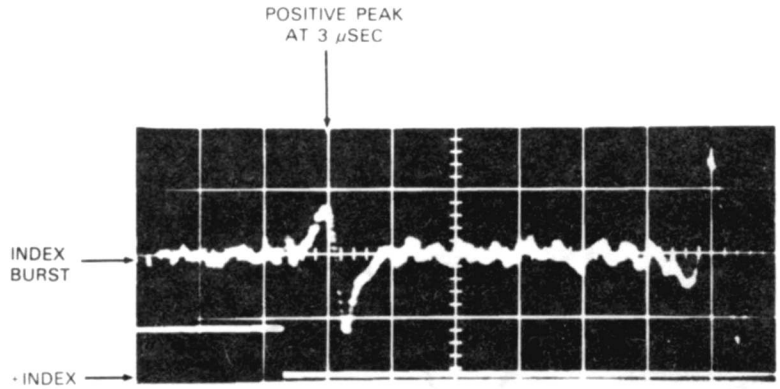


FIGURE 5-2. PULSE BURST

5.4.3 Index Transducer Circumferential Alignment

While observing the burst-track display (Figure 5-2) on the scope, tighten the adjustment nut slightly (Figure 5-3). If tightening the nut causes the pulse burst to appear closer to the 3 ±2 μsec range after Index, continue tightening until the pulse burst falls within that range. If not, loosen the nut until the pulse burst occurs after the optimum interval.

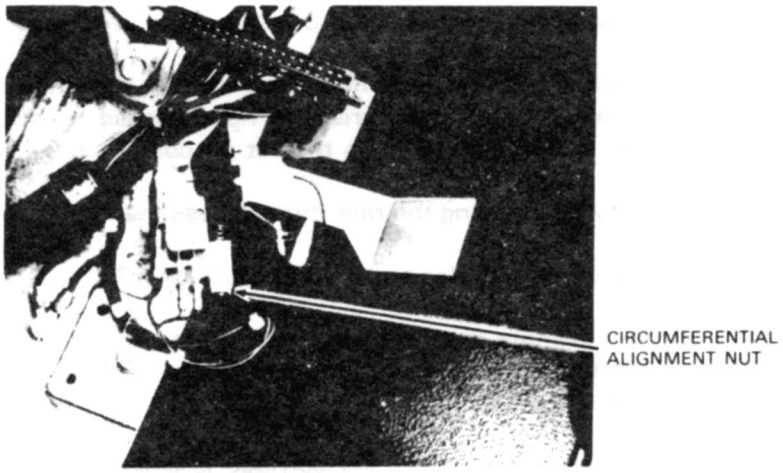


FIGURE 5-3. INDEX TRANSDUCER

5.5 CYLINDER TRANSDUCER REQUIREMENTS AND ADJUSTMENTS

Two sources of seek errors related to the cylinder transducer are: (1) incorrect amplitude at the transducer secondary output, and (2) incorrect horizontal mechanical displacement between the moving rack teeth and the pawl teeth at the time count pulses are generated. Both sources can be diagnosed by an oscilloscope check.

5.5.1 Alignment Specifications

The following list and Figure 5-4 define specifications for acceptable cylinder transducer alignment.

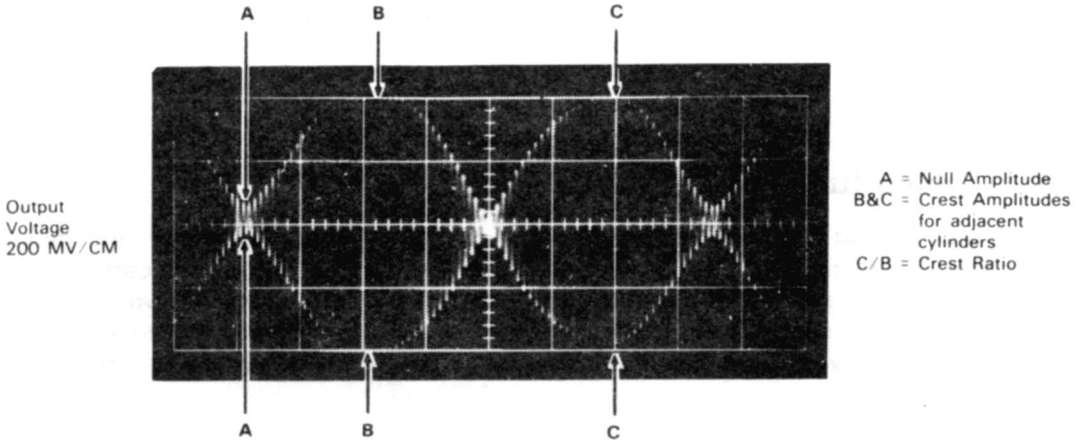


FIGURE 5-4. TRANSDUCER OUTPUT

1. Transducer oscillator output must be 3.0 volts ±0.15 volts peak-to-peak.

2. Peak-to-peak crest amplitude (the maximum output achieved between two adjacent null regions), when the carriage is not detented, must be within the range of 450 mv to 1400 mv. This is true at all points along the rack.

3. Null amplitude anywhere along the rack must be less than 80 mv peak-to-peak.

4. The carriage bearing (spring-loaded) torque must be 17 ±1 inches-lb.

5. The ratio of the maximum peak-to-peak crest amplitude to the minimum peak-to-peak crest amplitude for adjacent crests must be 1.2 to 1.0. This is defined as the crest ratio.

6. The peak-to-peak amplitude when the carriage is detented must be between 70% and 90% of the peak-to-peak crest amplitude associated with the detented position. This requirement applies for all detented cylinder positions.

Where these values specify maximum and minimum levels, levels above the minimum or below the maximum specified are acceptable.

5.5.2 Transducer Oscillator Check

The oscillator signal is applied to the primary winding of the transducer. Before examining the cylinder transducer output characteristics, it is important to be sure the oscillator output is within tolerance.

1. Set the oscilloscope vertical scale to 1 volt/cm.

2. Connect the scope probe to pin 16 of the TAMP board (B06). The output should be 3.0 volts ±0.15 volts peak-to-peak.

3. If the oscillator output is outside the required range, adjust R4 on B06 until the output meets the specifications.

5.5.3 Transducer Alignment Check

Remove the shroud assembly to gain access to the cylinder transducer and detent mechanism. For steps that require manually positioning and detenting the carriage, the servo and detent actuator should be disabled by removing fuse F4, the +55-vdc fuse, and the heads should be carefully loaded by hand with no pack installed on the drive. Contact of a head's surface with the opposing head will not cause damage if the loading is done slowly and carefully.

For steps in the procedure that require small carriage movements; e.g., moving to an adjacent cylinder to determine crest ratio, the use of a Carriage Moving Tool (P/N 200515) is recommended. This tool is installed as follows:

1. Move the carriage to the fully retracted position.

2. Screw the handwheel all the way onto the threaded shaft of the tool.

3. Insert the shaft through the hole in the plastic cable cap on the back of the linear motor and screw it all the way into the threaded hole in the end of the tachometer rod attached to the Tee-block.

4. Carefully load the heads by lightly pressing your right hand against all the heads and moving the carriage forward with your left hand.

5. Spin the handwheel clockwise until it comes to rest against the plastic cable cap. The wheel can now be turned clockwise to move the carriage slowly in the reverse direction until a desired position is reached.

CAUTION

Be sure to remove the Carriage Moving Tool before re-enabling the servo and performing seeks, or damage may result to the tool or linear motor.

5.5.3.1 Check Position Indicator Scale

Move the carriage by hand to the home position (cylinder 000) and manually detent the carriage. Although the scale on top of the Tee-block identifies home position, its accuracy should be checked by examining the position of the detent pawls with respect to the rack (refer to Figure 5-5a). When the carriage is in the home position, the bottom pawl is engaged and there are either two or no rack teeth (depending on the rack configuration installed) in back of the top pawl. A small dental mirror is useful for observing the tooth-pawl relationship without removing head assemblies from the drive.

5.5.3.2 Transducer Amplitude Check. (Refer to Figure 5-5b.)

1. Set the oscilloscope's vertical scale to 100 mv/cm and the sweep speed to 5 msec/cm.

2. Connect Channel A of the scope to pin 8 of board B06.

3. Observe the scope trace while moving the carriage by hand (at a moderate speed) over the range of cylinders 000 to 202. Note the changing crest and null values along the rack. In particular, note the following characteristics:

   a. The maximum peak-to-peak crest value along the rack

   b. The minimum peak-to-peak crest value along the rack

   c. The peak-to-peak null value along the rack

4. The values of the crests and nulls must conform to the specifications outlined in 5.5.1, steps 2 and 3.

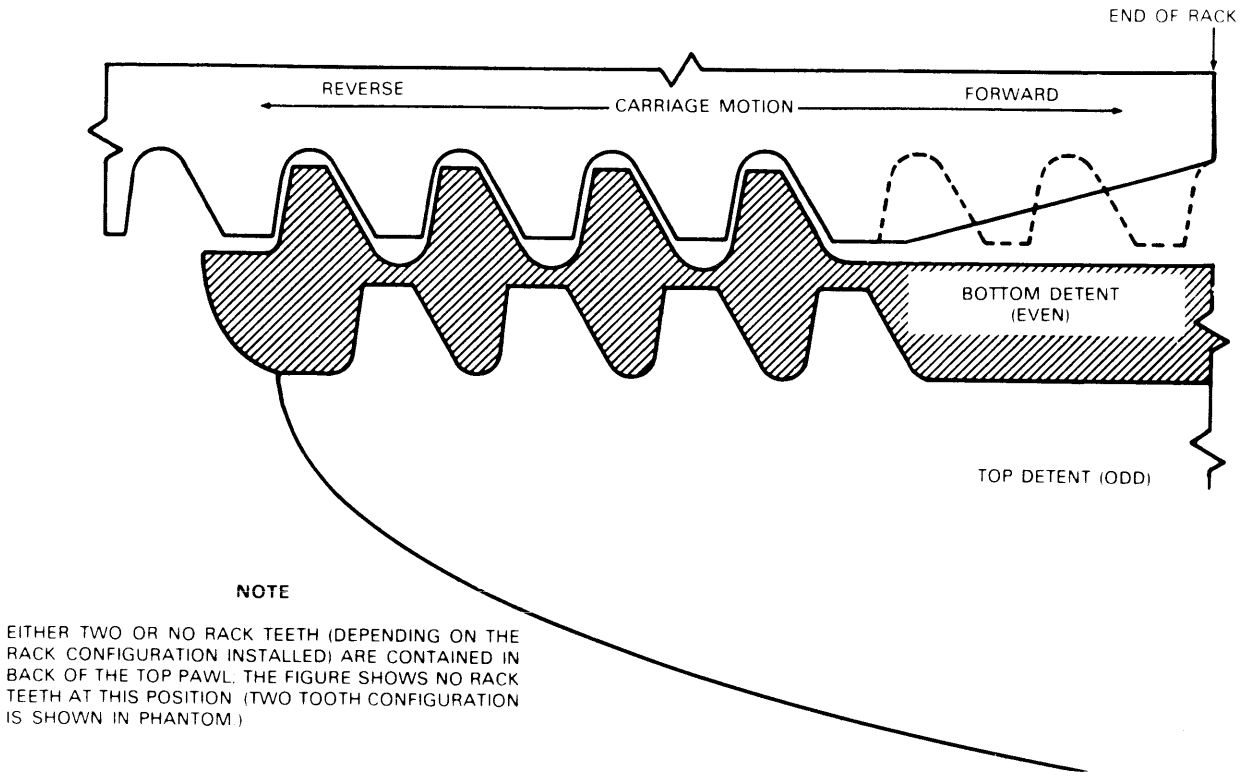


FIGURE 5-5a. RACK PAWLS AT CYLINDER 000

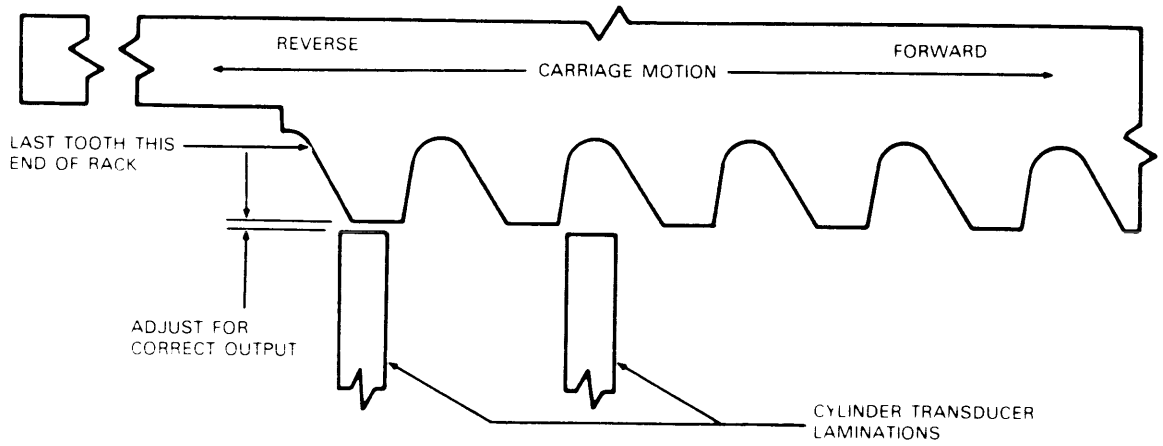


FIGURE 5-5b. RACK AND CYLINDER TRANSDUCER AT CYLINDER 202

5.5.3.3 Transducer-to-Pawl-Setting Time Relationship Check

Seek errors can be caused by the detent pawls setting too soon or too late and missing the required detent position. Correct this problem by shifting the transducer slightly until the pair of laminations of the transducer are aligned correctly.

1. Place a "scratch" pack on the drive and run for five minutes to verify proper operation of the servo. The cylinder count location must be between 1.9 and 3.0 mil of the total distance of the functional tooth. This can be checked by observing Compare and Tach Amp signals as follows.

2. Set the oscilloscope as follows:

   Time: 1 msec/cm
   Channel A: 1 V/cm
   Channel B: 100 mv/cm

3. Connect oscilloscope as follows:

   Ground connector: Pin A of any logic card
   Channel A probe: A05-TP8 (+Compare)
   Channel B probe: B04-TP3 (Tach Amp)
   Trigger In: A06-TP4 (+Seek Forward)

4. Perform sequential one-track forward seeks and observe the waveform as shown in Figure 5-6a. Change the horizontal time sweep to 0.5 msec/cm and decalibrate the oscilloscope time base to extend the Tach Amp profile over the 10-cm scale as shown in Figure 5-6b (arrow points to reference knee). The signal, Compare, must go high within 2.5 to 3.1 cm on all one-track forward seeks.

5. If the waveform does not meet the above specification, adjustment of the cylinder transducer is **necessary** (see 5.5.5).

5.5.3.4 Transducer-to-Pawl Positional Relationship Check (Cylinder 202 Check)

Make this check to verify that field adjustments or replacements to a cylinder transducer have not caused setup on an incorrect rack tooth. Improper positional alignment will result in consistent seek errors and will cause the drive to restore to an incorrect cylinder position.

1. Move the carriage to rest against the forward carriage stop.

2. Detent at this position.

3. Mount the Carriage Moving Tool on the linear motor and provide a constant forward force on the carriage assembly by stretching a heavy rubber band between the top back of the Tee-block and the spindle nose.

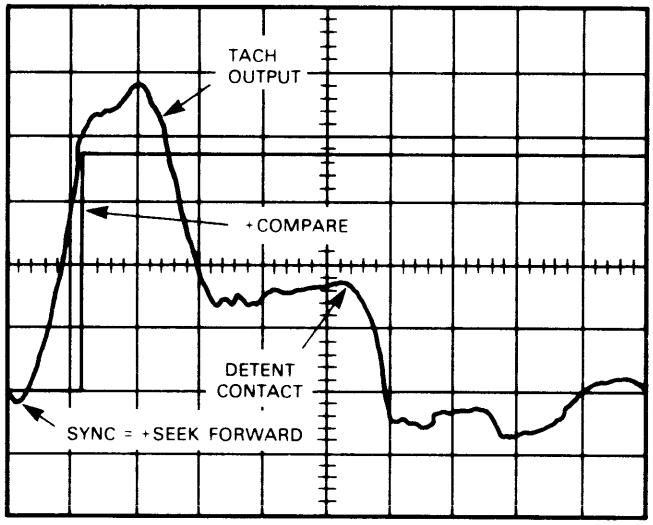


FIGURE 5-6a. CYLINDER COUNT LOCATION WAVEFORM (1 msec/cm)

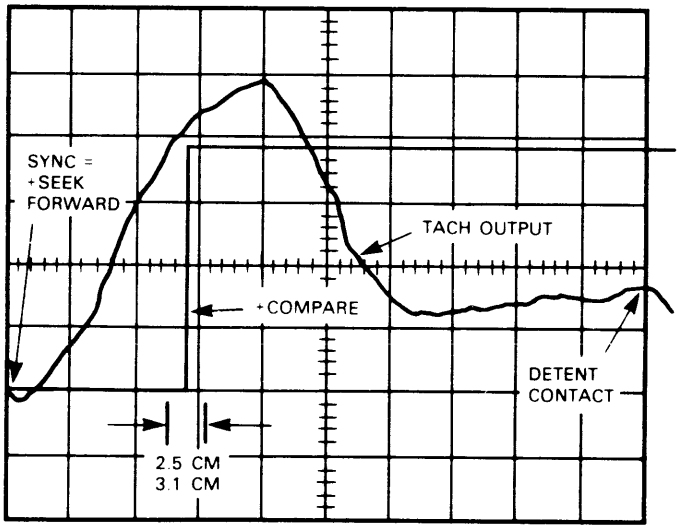


FIGURE 5-6b. WAVEFORM OF CYLINDER COUNT LOCATION EXPANDED (0.5 msec/cm decalibrated)

4. Slowly move the carriage in the reverse direction by turning the handwheel clockwise and observe the secondary output of the cylinder transducer at pin 8, B06. Allow the carriage to detent at each position as the carriage is moved back.

5. Stop at the first detented position after observing the first true null. Ignore the false, high-amplitude (greater than 200 mv) null that occurs first as the carriage is backed away from the stop.

The cylinder position arrived at must be 202, as read on the drive position indicator scale.

Failure to detent at cylinder position 202 after the above procedure indicates either a cylinder transducer adjusted to the wrong tooth on the rack or an improperly adjusted cylinder position indicator scale. Repeat the appropriate checks in this procedure to determine which error is present and correct it.

5.5.4 Cylinder Transducer Partial Realignment Procedures

If seek errors occur and if the cylinder transducer characteristics are found deficient (as a result of performing the analysis described in paragraph 5.5.3), the problem may be corrected by alignment. The procedures in paragraph 5.5.4.1 are designed to increase or decrease the transducer output amplitude as needed.

The procedures in paragraph 5.5.4.2 are designed to assure that the generation of count pulses occurs when the detent rack teeth are in the correct position with respect to the detent pawl teeth. This relationship is important because it determines whether or not the detent pawl sets at the right instant following Compare.

5.5.4.1 Amplitude Adjustment

If the crest amplitude is too low at one or more points along the rack, make the adjustment described in steps 1 through 3 below. If a null is too high, make the adjustment described in step 4 below.

1. Move the carriage to the cylinder which showed the lowest crest amplitude.

2. With the blade of a beryllium screwdriver set against the back of the leaf spring (A in Figure 5-7), tap the handle of the screwdriver lightly until the amplitude increases the necessary amount. This technique is capable of increasing the amplitude by about 50 mv. If the deficiency is greater than that, turn the drawback screw (B in Figure 5-7) counterclockwise a quarter turn. If necessary, tap the leaf spring again.

3. Check for clearance between the transducer and rack by pushing against the back of the transducer (where the coils are—not at the base). If there is clearance, output of the secondary coils will increase. If the output does not increase, the transducer is too close to the rack and step 4 should be performed.

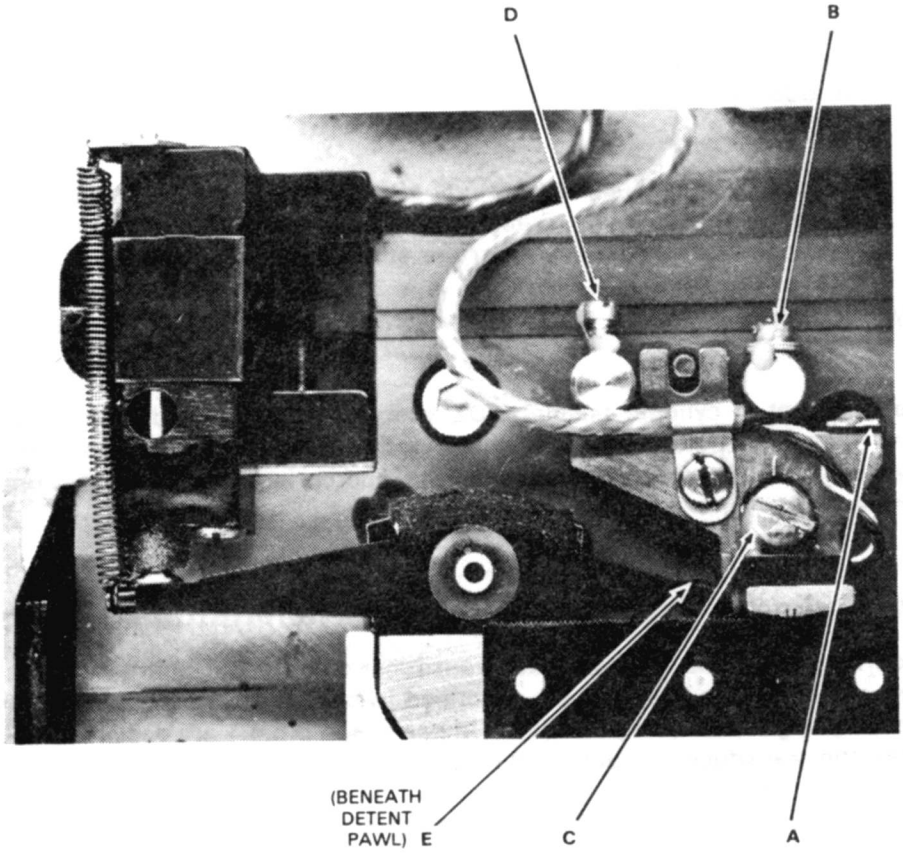


FIGURE 5-7. CYLINDER TRANSDUCER ADJUSTMENT DETAILS

4. To draw the transducer back away from the rack (to provide clearance or to decrease a high null), turn the drawback screw clockwise slightly until there is either enough clearance or the null amplitude is low enough. If correcting a high null, perform this operation with the carriage at the position where the highest null was observed.

5. Move the carriage to any other cylinder positions which showed low peaks or high nulls. The new output at these positions should be satisfactory since the adjustment was made at the worst-case cylinder position.

5.5.4.2 Detented Output and Crest Ratio Adjustment

If the detented-output to crest-output relationship or crest ratio is out of tolerance, it may be possible to readjust by the following procedure. If it is convenient, it is recommended that the transducer be completely readjusted following the procedure in paragraph 5.5.5.

1. Detent the carriage at the cylinder position of highest percentage (as determined in section 5.5.3.3) detent-to-crest relationship. If the highest percentage is 70% or less, completely readjust per paragraph 5.5.5. If greater than 70%, perform step 2.

2. Turn screw D (Figure 5-7) clockwise to reduce the detented amplitude by 10%. If the amplitude starts to increase, keep turning clockwise to raise the amplitude to the crest, then down to within 70% to 90% of the crest. It is advisable to stop at 90% on the first try to allow readjustment later, if additional specifications of amplitude and crest ratio are not met.

3. Recheck all specifications per paragraph 5.5.3.

5.5.5 Transducer Adjustment Procedure

Follow this procedure when it is necessary to adjust or replace the cylinder transducer.

1. Connect Channel A of the oscilloscope to pin 8 of B06. Loosen the transducer hold-down screw (C in Figure 5-7). Turn the drawback screw (B) until the face of the transducer is approximately even with the teeth of the detent pawl. Turn pivot screw (D) counterclockwise until it is away from the transducer base. With the blade of a beryllium screwdriver, push on the leaf spring (A) until the base of the transducer is against the dowel pin (E) on the carriage way.

2. Manually load the heads, taking care that the rack does not contact the face of the transducer. While moving the carriage back and forth, turn screw B counterclockwise and press on the leaf spring until an output amplitude of approximately 300 mv is obtained on the scope.

3. Retract the heads. Snug down the transducer hold-down screw (C) to ensure that the transducer is flush with the surface of the carriage way. The transducer should still be against the dowel pin (E).

4. Manually detent the pawls and, while holding the pawls picked, load the heads and detent the rack at cylinder 000. Using a dental mirror, check the number of teeth showing to the right of the top pawl teeth. On older racks, two teeth should be showing; on newer racks, no teeth should be showing (see Figure 5-5).

5. When the above is true, the bottom pawl should be detented and the cylinder scale should indicate 000. If necessary, adjust the scale to cylinder 000.

6. Manually pick both pawls, move the carriage out to cylinder 200, and detent. The bottom pawl should be detented. While applying slight forward pressure on the carriage, pick the bottom pawl and then pick the top pawl. The scale should now indicate 202.

7. When the carriage is detented at cylinder 202, observe the scope and turn pivot screw (D) clockwise until the first crest (peak) is obtained. Using the dental mirror, check the transducer coil-to-tooth relationship (see Figure 5-5b). The left coil should be approximately at the top dead center (slightly left) over the last tooth. If it is, proceed to step 9.

8. If the left coil is between the last two teeth, slowly turn the pivot screw (D) clockwise until the next crest is reached. Check the coil-to-tooth relationship. It should now be as specified in step 7.

9. At this time, record the peak amplitude. Slowly turn the pivot screw (D) clockwise until 80% of the recorded peak is obtained.

10. Check the overall amplitude. If necessary, turn the drawback screw (B) slightly counterclockwise and push on the transducer base to the right of the drawback screw until the amplitude is approximately 1000 mv. Now, with the heads retracted, slowly tighten the transducer hold-down screw (C).

11. Load the heads again and check the overall amplitude. It should now be between 600 and 800 mv. If over this range, turn the pivot screw (D) slightly counterclockwise and then turn the drawback screw (B) **slowly clockwise** until the amplitude is between 600 and 800 mv.

12. If the amplitude in step 11 is below 600 mv, the transducer must be moved slightly towards the rack.

13. Retract the heads and install the Carriage Moving Tool at the rear of the linear motor. Manually detent the pawls and move the carriage out to the crash stop position. Release the pawls and, with slight forward pressure on the carriage, turn the Carriage Moving Tool handwheel clockwise. Observe the scope and listen for the audible detenting.

14. The scope presentation should increase to a high peak and then decrease to a high null (false null). It should then increase to another peak and start decreasing to the first true null. While approaching this null or going through it to the next peak, **stop** when a detent is heard. The cylinder scale should indicate 202 and the detented amplitude should be 70% to 90% of the peak amplitude. The peak can be checked by turning the handwheel of the Carriage Moving Tool slowly clockwise.

15. At the detent, the amplitude should increase slightly when turning the handwheel clockwise and then it should decrease. If these requirements are met, proceed to the next step.

16. Connect the scope as indicated in paragraph 5.5.3.3. Perform one-cylinder alternate seeks between cylinders 000 and 001. Sync the scope to obtain the pattern shown in the waveform in Figure 5-6.

17. Change the scope speed to 0.5 ms/cm and, with the decalibrated control, adjust until the detent contact knee is at the 10-cm graticule on the scope. Check the positive-going edge of the Compare signal. It should be between 2.5 and 3.1 cm from the leftmost graticule.

18. If Compare is to the right of the 3.1-cm graticule, the transducer must be pivoted counterclockwise. Turn pivot screw (D) in Figure 5-7 slowly clockwise until Compare goes high at 2.8 cm.

NOTE

Observe the detent knee; it may move while adjusting. Keep it on the 10-cm graticule.

19. If Compare is to the left of the 2.5-cm graticule, the transducer must be pivoted clockwise. To accomplish this, tap on the leaf spring with the blade of a beryllium screwdriver until Compare is at 2.8 cm. It may be necessary to back off on the pivot screw slightly. Again, watch the detent knee and keep it on 10-cm graticule. Recheck at cylinders 100-101 and 201-202.

20. Verify that the amplitude output of the transducer meets all the requirements as given in paragraph 5.5.3.2, Transducer Amplitude Check.

21. Run the drive for five minutes and verify proper cylinder counting.

5.5.6 Detent Plunger Clearance

Remove the disc pack and check clearance between the detent actuator plunger and the detent pawls. There must be 0.005 to 0.008 inches clearance when the detent is engaged in the rack. Both top and bottom detents must meet this requirement. If specifications are not met, proceed as follows:

1. Add or remove shims (P/N 200438) as required to maintain clearance as close to but not less than 0.005 inches as practical.

2. Install shroud, scratch pack, and top cover.

3. Run for five minutes to verify proper detenting.

5.6 SERVO ADJUSTMENTS

5.6.1 Servo Power Supply

The Servo Driver board (C01) has two potentiometers that are adjusted at the factory to provide the ±15 volts used by boards C01 and B04 (this ±15 volts is independent from the ±15 volts supplied to other logic). These voltages should be verified before making any adjustments to the servo.

1. Connect a digital voltmeter between pins N and R of B04 (R is ground).

2. Adjust R35 (bottom potentiometer) on C01 to +15±0.150 V.

3. Connect the digital voltmeter between pins P and R of B04 (R is ground).

4. Adjust R41 (top potentiometer) on C01 to -15±0.150 V.

5.6.2 Servo Adjustment Procedure

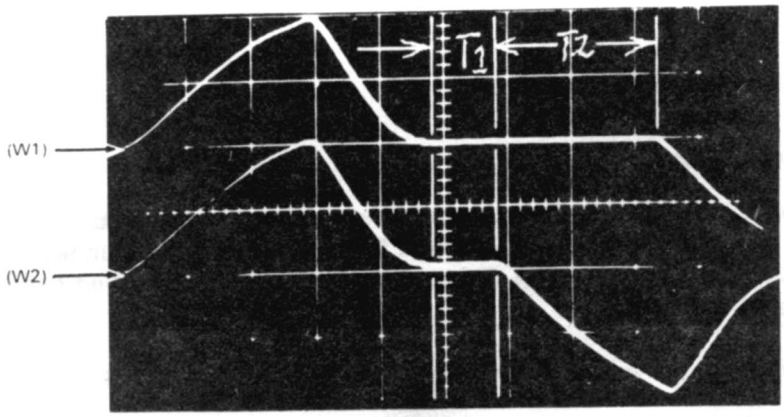
The drive's top covers must be installed and the drive must be in a ready state before making the servo adjustments.

1. Set servo gain R18 (bottom potentiometer) on B04 fully CCW and then perform a first seek.

2. Adjust the holding current by connecting a digital voltmeter between TP-1 and TP-7 (ground) on B04 and then adjusting the offset control R34 (top potentiometer) until a voltage of +200 ±10 mv is indicated on the digital voltmeter.

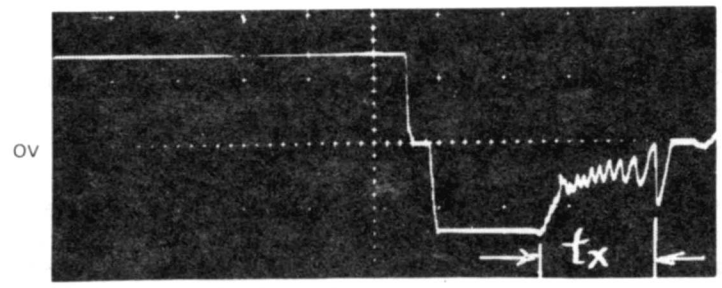
3. Check the power rate circuit by observing B04-TP3 (Tach Amp) with an oscilloscope. Sync on Seek Forward, A06-TP4. Set the oscilloscope's vertical gain to 5 V/cm and time base to 10 msec/cm. Perform alternate 202 track seeks with minimum delay between seeks (i.e., do not time-share control unit with computer). After five minutes of running in this mode, the extra power rate delay (T2) which switches ON and OFF verifies that the power rate circuit is operational as shown in Figure 5-8.

4. The servo gain can be adjusted by observing B04-TP1 (Programmed Current) with an oscilloscope. Sync on + Seek Forward, A06-TP4. Set the oscilloscope's vertical gain to 10 V/CM and time base to 5 msec/cm. Perform alternate 202 track seeks, with minimum delay between seeks, for 8 to 10 minutes from a cold start to allow the servo temperature to stabilize. The servo gain should be adjusted only when the high power rate is on (A05-11 is high), and the servo is running in its slower state. Connect the other oscilloscope channel to A05 pin 11 (+ High Power Rate) and adjust the servo gain potentiometer R18 on B04 (bottom potentiometer) when + High Power Rate is observed at +5 Vdc (high logic level). The servo gain should be adjusted to achieve the proper gain margin as illustrated in Figure 5-9b. Note that the time Tx between the Break (95% of the saturated voltage) and Compare (last negative peak) in each of the photos is of different length.

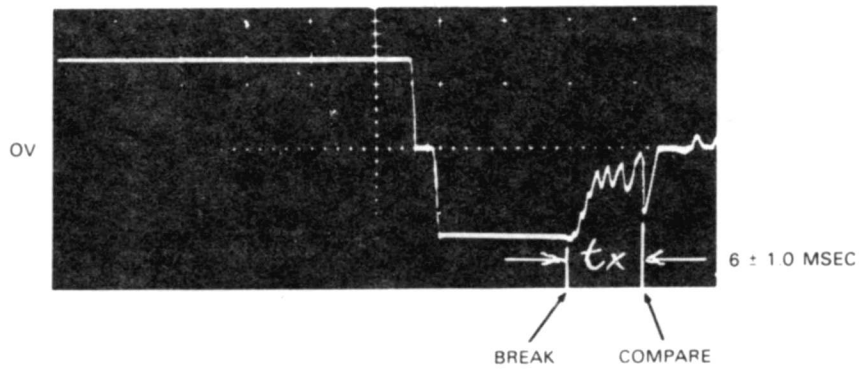


(W1) WAVEFORM WITH POWER RATE IN (with T1 and T2 between seeks)
(W2) WAVEFORM WITH POWER RATE OUT (with only T1 between seeks)
(T1) NORMAL DELAY BETWEEN SEEKS
(T2) POWER RATE DELAY (28 ±6 msec)

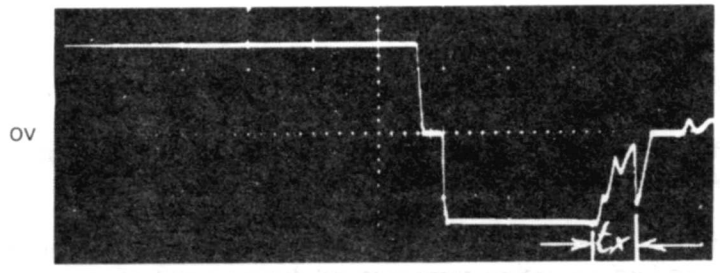
FIGURE 5-8. POWER RATE WAVEFORMS



a. Servo Gain Too Low



b. Servo Gain Set Properly



c. Servo Gain Too High

FIGURE 5-9. ERROR AMPLIFIER OUTPUT

If Seek Incomplete or File Unsafe ever occurs during adjustment of the servo gain, set servo gain R18 (bottom potentiometer on B04) to minimum (fully CCW), restore the drive to the ready state, and perform the servo gain adjustment again.

As a final check for servo performance, observe A04 pin S (-Seek Ready) on the oscilloscope while running alternate 58 track seeks. Set the oscilloscope vertical gain to 1 V/cm, time base to 5 msec/cm, and sync on negative internal. The sum of the time interval measured from Seek Start to Ready on the forward seek and the time interval measured from Seek Start to Ready on the reverse seek must be less than 72 msec. If this time interval is 72 msec or greater, the servo gain (step 4) is usually misadjusted.

5.7 OFF-LINE HEAD ALIGNMENT

5.7.1 Head Alignment Check

The following preparations must be made before head alignment can be analyzed.

1. See that the shroud is in place.

CAUTION

Be certain the carriage and heads are fully retracted before installing or removing a disc pack.

2. Install a CE disc pack.

CAUTION

Do not operate a drive with the RWAL or RWAR boards removed or damage to the hex inverters (D3 & D4) on certain earlier versions of the RAMP boards may result.

3. Preparation of the off-line tester. To substitute an off-line tester for the control unit, perform the following steps (ignore steps a and b below and perform step 4 if an off-line tester is not available).

   a. Check to be certain all switches on the off-line tester are in the off position.

   b. Connect the tester to either J3 and J5 or J13 and J14, depending on the type of tester being used (see 5.2). If a terminator is in location J4, remove it.

4. Head and Pack Thermal Equilibrium. The temperature stabilization cycle, which assures standard operating temperature during head alignment, is performed as follows:

   a. Run the drive for 1 hour with a disc pack installed and all covers on.

   b. Run the drive for 20 minutes with a CE pack installed and the control cover off.

5. Scope Connection. Use a scope with direct probes (1:1 attenuation), setting the display to A-B so that the two test points are read differentially. Set the vertical scale at 5 mv/cm and the sweep speed to approximately 3 ms/cm (or enough to observe one complete revolution).

   Sync externally on +Index (TP2 on board B05) and set up the scope inputs to measure differentially the outputs of either the left Read Preamplifier board or the right Read Preamplifier board, depending on which head is to be checked. For heads 1, 2, 5, 6, 9, 10, 13, 14, 17, and 18, use the left Read Preamplifier and attach scope probes to pins 18 and 19 of A10. For heads 0, 3, 4, 7, 8, 11, 12, 15, 16, and 19, use the right Read Preamplifier and attach scope probes to pins 20 and 21 of A10.

Once the above preparations have been completed, the off-line head alignment check is performed as follows: perform steps 1 through 3 below and bypass step 4 if an off-line tester is being used. If an off-line tester is not available, ignore steps 1 through 3 and perform step 4.

1. Position the heads to cylinder 73 with the off-line tester. Refer to the manual that accompanies the tester for operating instructions.

2. Select one of the heads with the off-line tester.

3. Select the READ mode with the tester. When the head starts reading, the scope trace should resemble the curve in Figure 5-10.

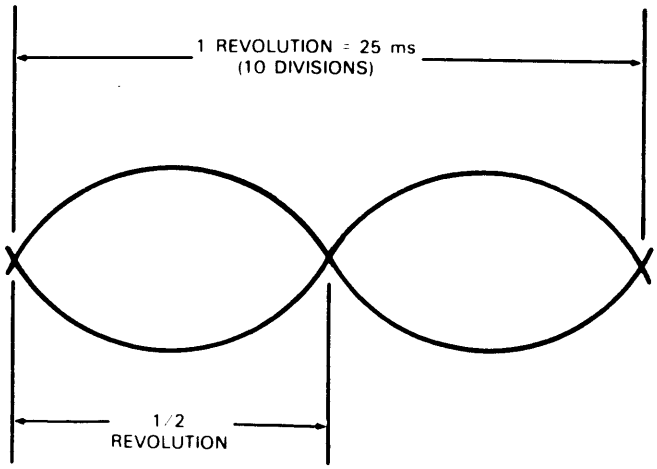


FIGURE 5-10. HEAD ALIGNMENT READ SIGNAL AT ONE REVOLUTION

4. The following steps must be performed if an off-line tester is not used.

   a. Position the heads to cylinder 73 via the controller.

   b. Select one of the heads by jumpering the appropriate Head Select line to ground. This can be accomplished at the Line Select input lines on the Read Amplifier board (A10). For best results, all the heads should be checked to arrive at an average alignment.

   c. A read signal should appear on the scope; the trace will resemble the curve in Figure 5-10.

5. The first zero crossing is at +Index. The third zero crossing should occur 10 divisions later (this is determined by the sweep speed setting on the oscilloscope). If the head is properly aligned, the second zero crossing will fall on, or very near, the centerline of the display; i.e., the two lobes of the trace will be equal.

   Record the amount of deviation (if any) of the second zero crossing from the centerline on the scope.

6. Repeat check 5 above for all heads.

7. All the heads should be checked so that they are aligned with respect to each other, as well as with respect to the reference cylinder. To do this, calculate the average deviation of all the heads that do not deviate more than ±0.8 division from the centerline. All the heads must be within ±0.4 division from the average deviation for all heads and ±0.8 division from the centerline on the scope.

8. Adjust any head that does not meet the requirements outlined in step 7 to within ±0.2 division of the average deviation.

NOTE

Do not adjust any head that is within the tolerances.

5.7.2 Head Alignment

The following alignment procedure assumes that the conditions necessary for performing a head alignment check (described in Section 5.7.1) are satisfied. In addition, check to be certain that all switches on the off-line tester are off and the off-line tester cables are properly connected.

1. Position the heads to cylinder 73 of the CE disc pack.

2. Select the head that is to be aligned.

NOTE

If all the heads on the front side of the Tee-block (B- and D-type heads) are to be aligned, start with the bottom assembly and work up.

If all the heads on the back side of the Tee-block (A- and C-type heads) are to be aligned, start with the top assembly and work down.

3. Select the READ mode with the off-line tester.

4. Loosen the four screws holding the two clamps, which hold the head-arm assembly in place, just enough to allow the assembly to move when moderate pressure is applied.

5. Pull lightly against the tab on the head-arm assembly so that the assembly moves all the way back in its slot against the Tee-block.

6. Tighten one of the clips (bottom clip for a B- or D-type head; top clip for an A- or C-type head) to restrict its movement without restricting the movement of the head-arm assembly (Figure 5-11).

NOTE

The alignment tool should always push back against the clip that is tightened down. Since the tool twists clockwise, the bottom clip must be tightened on the front side of the Tee-block and the top clip on the back side.

7. While observing the trace on the scope, carefully twist the alignment tool clockwise so the assembly moves forward (toward the spindle). Stop twisting as soon as the second zero crossing falls within the tolerances listed in Section 5.7.1, step 7.

8. If the head goes too far forward, reperform steps 5 through 7.

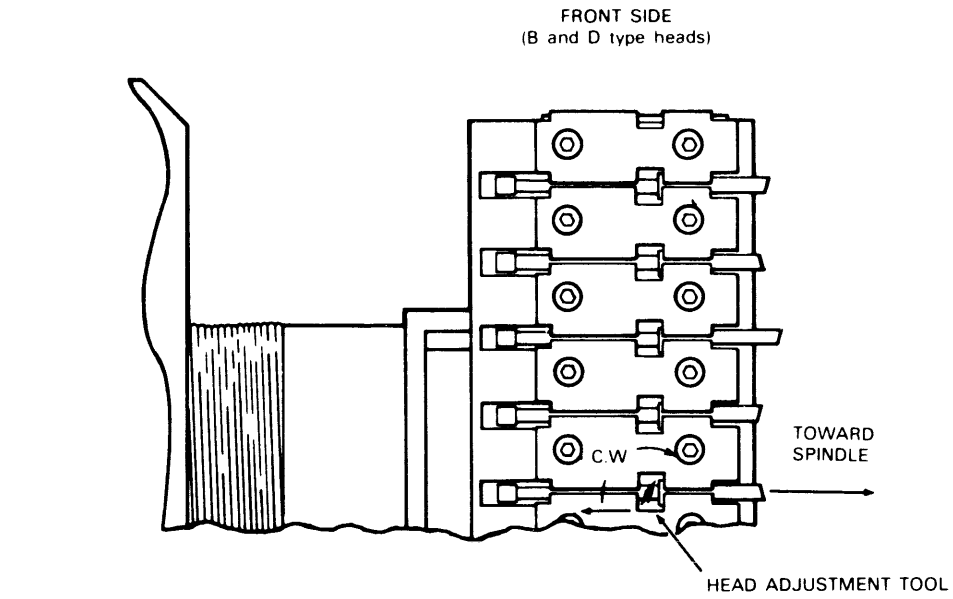
NOTE

Do not try to align the head while pushing the assembly back. Always align the head while adjusting it in the forward direction.

9. Before tightening the second clip, check the alignment of the adjacent head(s). To do this, it is necessary to deselect the head just aligned and select an adjacent head.

10. When the adjacent heads are aligned, tighten all clips with the Memorex Head Clamp Torque Wrench (P/N 200552).

NOTE: THIS ILLUSTRATION SHOWS ONLY THE TOP 10 SETS OF CLIPS.



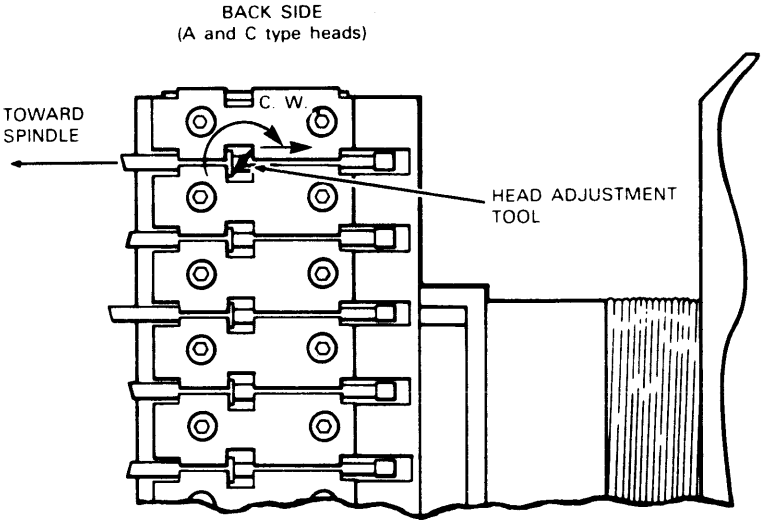


FIGURE 5-11. HEAD-ARM MOUNTING CLIPS AND ALIGNMENT SLOTS

5.8 HEAD UNLOAD CAM REPLACEMENT

1. Turn off the main power switch (S1) on the interior control panel.

2. Remove the control cover, pack enclosure, and shroud assemblies.

3. Carefully push the carriage all the way out to the forward stop while holding the palm of hand flush against the head arm edges so the heads will not slap together.

4. Unscrew the cam screws and remove the old cams by pulling them along the head arms away from the cam support and then away from the arms.

5. Leaving the carriage in the forward position, install the new cams in the reverse order of step 3. Make sure the cams are pushed against the sides of the recesses in the cam support before the screws are tightened. If the cams were installed properly there will be clearance between the outer edges of the head arm assemblies and the vertical surfaces of the cams.

6. Push the carriage back (away from the spindle) until the heads are fully unloaded.

7. Reinstall the shroud, pack enclosure, and control cover assemblies.

5.9 HEAD-ARM ASSEMBLY REPLACEMENT

1. Remove the disc pack and control covers from the drive.

2. Disconnect the head plug from its board.

3. Remove the two side clamps (one above and one below the head arm) which hold the assembly in the Tee-block slot (Figure 5-11).

4. Grip the head-arm assembly at points A, B, and C (Figure 5-12) with the Memorex Head-Arm Assembly Replacement (Preloader) Tool (P/N 200945).

5. Close the jaws of the tool so that the head-arm assembly leaf spring is bent back enough to clear the cam supporting it.

CAUTION

Do not touch the head shoe face or press against the flexure. Refer to Figure 5-12, points D and E. Even slight pressure against the flexure could bend it and impair the head's flying attitude.

6. While holding the jaws of the tool closed, extract the assembly from the Tee-block slot.

7. To install a head-arm assembly, reverse steps 1 through 5.

NOTE

When the head is properly mounted, the bleed holes are located in the leading half of the head shoe (relative to disc pack rotation).

Whenever a read/write head is replaced, an alignment check must be made on it and the two adjacent heads (one adjacent head if the replaced head is at the top or bottom of the Tee-block). This is advisable because the adjacent head-arm assemblies may move slightly when the clips they share with the replaced head are removed.

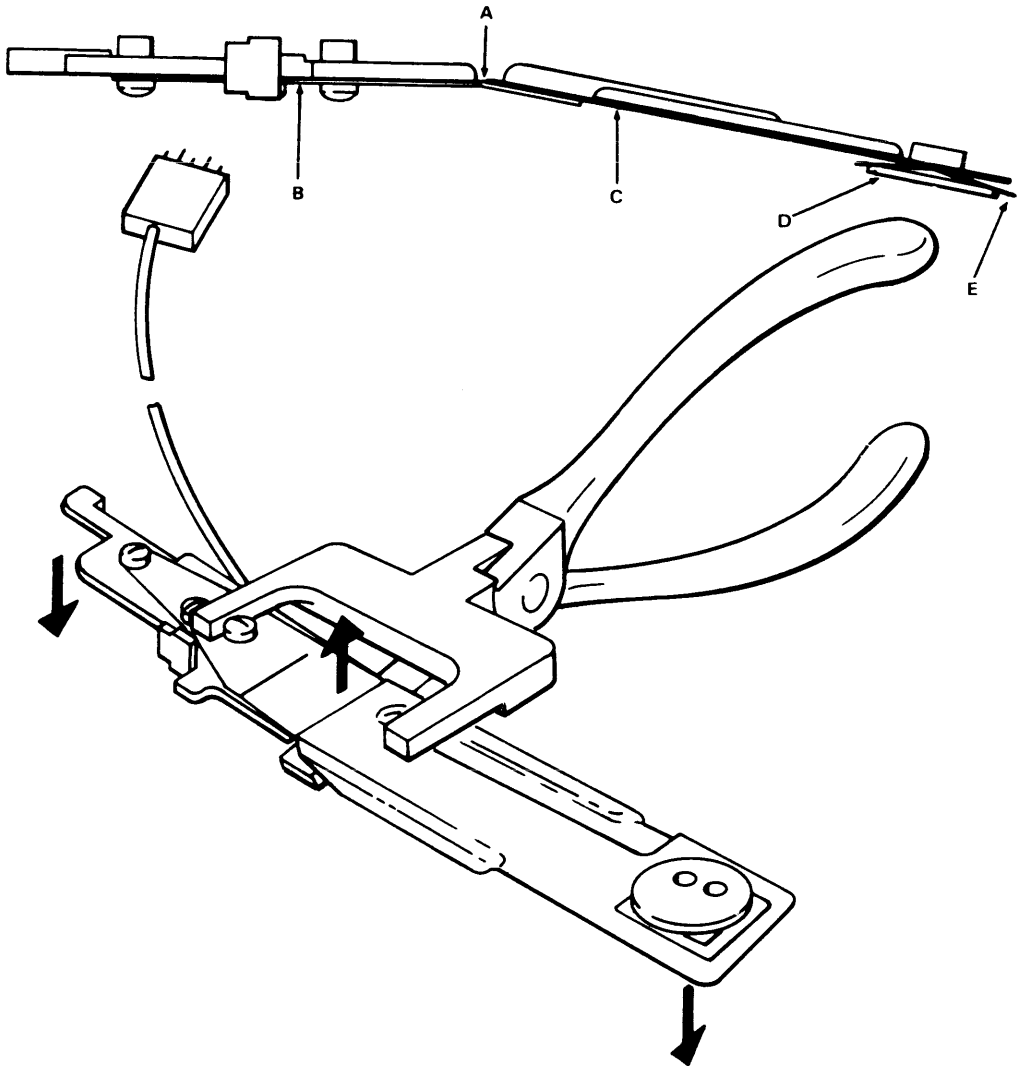


FIGURE 5-12. PRELOADING THE HEAD-ARM ASSEMBLY FOR INSTALLATION

5.10 SPINDLE DRIVE MOTOR REPLACEMENT

5.10.1 Motor Plate Assembly Removal

1. On the interior control panel, turn the main power switch (S1) off and disconnect the drive motor power plug.

2. Remove the spindle drive belt (see Section 5.11 for removal procedure).

3. Place a support block on the cross member of the interior control panel under the drive motor.

4. Break the adhesive bond holding the three shoulder screws (Figure 5-13) and loosen the screws.

5. Pivot the motor plate assembly slightly to extend the belt tension spring. Remove the two shoulder screws and plastic washers in the slotted area.

6. Allow the motor plate assembly to pivot back, releasing tension on the spring, and remove the remaining shoulder screw and washer.

7. Lift the motor plate assembly from the drive.

8. Remove the four sets of nuts and lock washers, offset the bracket, and vibration-mount, hex-standoff assembly and pulley.

5.10.2 Motor Plate Assembly Installation

1. Install the vibration-mount, hex-standoff assembly, offset bracket, and four sets of nuts and lockwashers.

NOTE

Be certain the spring bracket orientation corresponds to Figure 5-13.

2. Install the motor plate to the vibration-mount studs and secure with the four nuts and lock washers.

3. Install the motor pulley and position it on the motor shaft so that the distance from the top face of the pulley to the top surface of the motor plate is 0.240 ±0.015 inches.

4. Apply adhesive (P/N 110877) to the shoulder screw threads.

5. With the motor supported by a wood block, insert the shoulder screw and washer in the pivot hole located in the deck plate. Snug down the screw (finger tight).

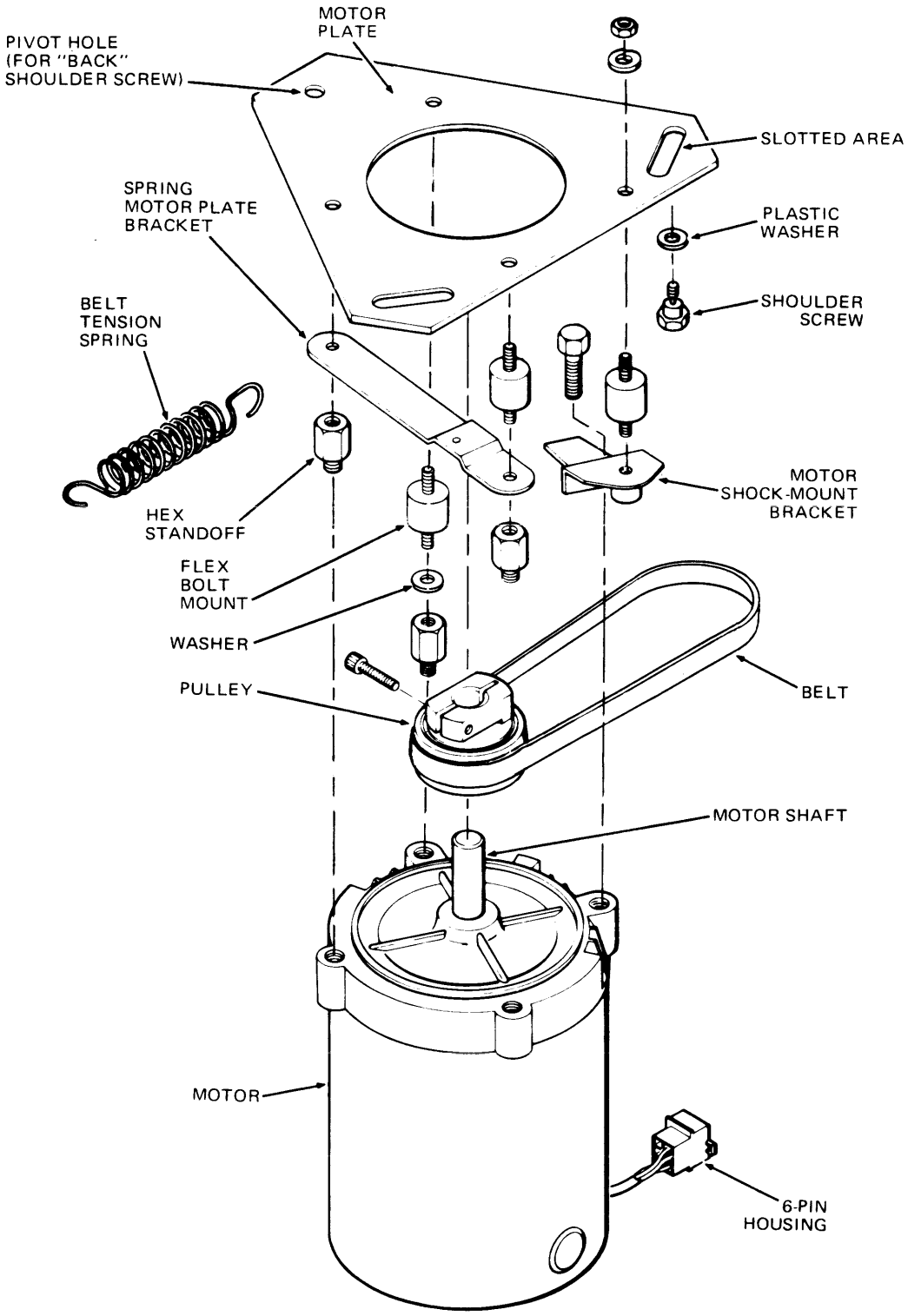


FIGURE 5-13. DRIVE MOTOR AND MOUNT ASSEMBLY

6. Fit the free end of the belt tension spring into the groove on the post and pivot the motor plate assembly slightly to extend the spring.

7. Install the two shoulder screws and washers in the slotted holes.

8. Allow the motor plate assembly to pivot back, releasing tension on the spring.

9. Tighten all three shoulder screws to approximately 10 inch-lb of torque. Excessive tightening will indent the aluminum baseplate or break off the screw head.

10. Install the drive belt (refer to Section 5.11 for installation procedure).

11. Insert the drive motor power plug in its socket.

5.11 SPINDLE DRIVE BELT REPLACEMENT

1. On the interior control panel, turn the main power switch (S1) off and unplug the spindle drive motor.

2. Pivot the drive motor on its back shoulder bolt (Figure 5-13); this will allow enough slack in the belt for it to drop off the pulleys.

3. Slip the belt between the pack-on switch and the bottom of the spindle, and remove the belt from the drive.

4. If the pulleys are not clean, clean them with isopropyl alcohol.

5. Install a new belt.

NOTE

Be sure the replacement belt is the right length for the drive: 60-Hz drives use P/N 200230; 50-Hz drives use P/N 200253.

The smooth side of the belt should be inside against the pulley faces.

The belt should be centered on the flat of the motor pulley.

6. Check the pack-on switch clearance; refer to Section 5.12 for details.

5.12 SPINDLE ASSEMBLY REPLACEMENT

1. With the main power switch (S1) off, remove the disc pack cover, shroud, and spindle drive belt (refer to Section 5.11 for belt removal procedure).

2. Remove all four spindle flange bolts.

3. Lift the spindle out of the baseplate.

4. Install new spindle assembly (P/N 200003) and tighten the flange bolts securely.

NOTE

Be sure the new spindle pulley is clean; if it isn't, clean it with isopropyl alcohol.

5. Replace the spindle drive belt.

6. Check brake pawl-to-pulley clearance. If necessary, deform the linkage rod to provide the necessary clearance (0.100 ±0.050 inches). See Figure 5-14.

7. Install a disc pack on the spindle and check clearance between the bottom of the shoulder of the carbon plug and the plastic bushing on the middle leaf of the pack-on switch (Figure 5-15). If necessary, deform (bend) the upper contact arm of the switch so that the clearance is 0.025 ± 0.010 inches.

8. Remove disc pack and replace the shroud.

9. Check head alignment. (Refer to Section 5.7 for head alignment procedure.)

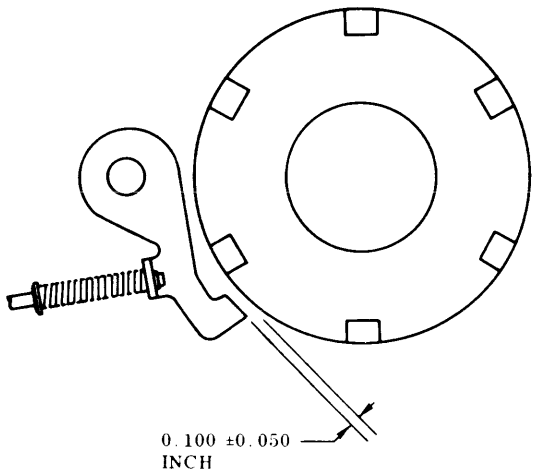


FIGURE 5-14. BRAKE PAWL-TO-SPINDLE PULLEY CLEARANCE

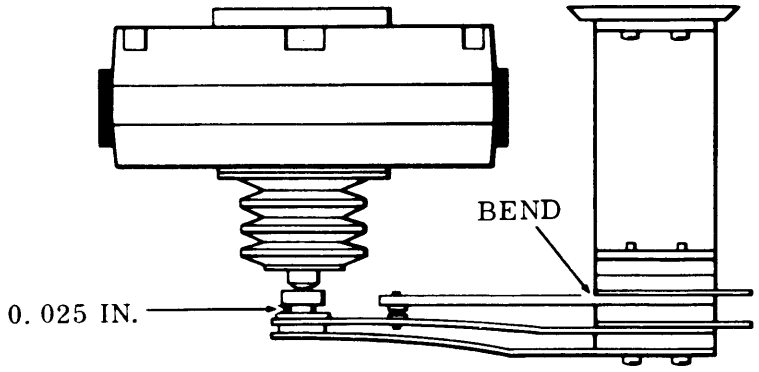


FIGURE 5-15. PACK-ON SWITCH-TO-SPINDLE CLEARANCE

5.13 TORSION ROD REPLACEMENT

1. Turn off the main power switch (S1) located on the interior control panel.
2. Remove the disc pack, if one is installed.
3. Remove the shroud-area cover:
   a. Release the two latches located at the back of the drive where the top cover meets the main frame.
   b. Tilt the rear of the cover assembly up approximately 5°.
   c. Pull the assembly toward the front of the drive approximately three-fourths of an inch.
   d. Lift the cover straight up and off the machine.

CAUTION

Do not hit the index transducer or the PC board mounted on the cam tower. Hold the cover with both hands in a way that will keep the door closed no matter how the cover assembly is tilted. This is important for the next step.

4. Stand the top cover assembly on a clean, flat surface in a vertical position (90° from normal on its rear surface).
5. Allow the door to lie back gently into a fully open position. This releases tension on the torsion bars.

6. Remove the two metal clamps which bundle the four torsion bars.

7. Lift the torsion bars out of their respective slots in the two plastic bearing blocks.

NOTE

Rods which miss contact with the hinge (when the door is fully open) by more than 0.03 inches should be replaced.

8. Install torsion rods by reversing steps 1 through 7.

NOTE

The first two rods installed should always be on the same side (i.e., install the upper rod and the lower rod on one side; then install the upper and lower rods on the other side).

9. At points of friction, lubricate the rods sparingly with a silicone grease (P/N 110875).

5.14 INDICATOR LAMP REPLACEMENT

CAUTION

Do not replace lamps by removing the front glass. Removing the glass may scratch the film insert behind the glass.

1. Remove the drive's rear panel by pulling it out from the top; it is held on by magnetic clips.

2. Release the two latches located at the back of the drive where the control cover assembly meets the main frame.

3. Lift the control cover assembly from the rear.

4. Remove the lamp socket plate on the rear of the operator control panel assembly.

5. Tilt the lamp socket plate to expose the front of the bulbs.

6. Pull the bulb straight out; these are slide-base sockets, not threaded sockets.

7. Replace the lamp socket plate.

5.15 BOBBIN CHANGE PROCEDURE

The recommended technique for field replacement of the bobbin on the linear motor assembly is as follows.

5.15.1 Disassembly

1. Place the START-STOP switch in the STOP position.

2. Remove the front and rear cover assemblies, control cover assembly, and disc pack. Turn off the main power switch (S1).

NOTE

Figure 5-16 is an exploded view of the deck plate assembly. Components to be removed during this procedure are referenced by their numeric callouts.

3. Remove the three screws (1, 2, and one not shown) that attach the carriage (3) to the bobbin coil (4). This will disconnect the carriage ground assembly. Heads 8 and 9 must be removed to gain access to the top screw.

4. Unplug the harness connection (J18) to the tachometer coil and remove the socket (P18) from its supporting bracket.

5. Disconnect the linear motor quick-disconnect terminals at connector (18).

6. Remove screw (21) from the terminal bracket mounting assembly (14). Plastic guard (20) can now be removed.

7. Remove the temperature sensor assembly (12) from the flex conductor clamp (18) by unscrewing the two nuts (11).

8. Push the carriage toward the spindle while holding the bobbin in the linear motor. Be careful not to launch the heads.

9. Unscrew the tachometer rod at the rear of the carriage assembly (3). Leave the rod in the tachometer.

10. Verify that the guide bar (22) mounted to the deck plate (25) on the left side of the linear motor (6) is flush with the motor's left side. This guide bar will be used to locate the linear motor when it is remounted.

11. Remove the three bolts (24) holding the linear motor to the deck plate. The left side cover must be removed to gain access to the rear motor bolt.

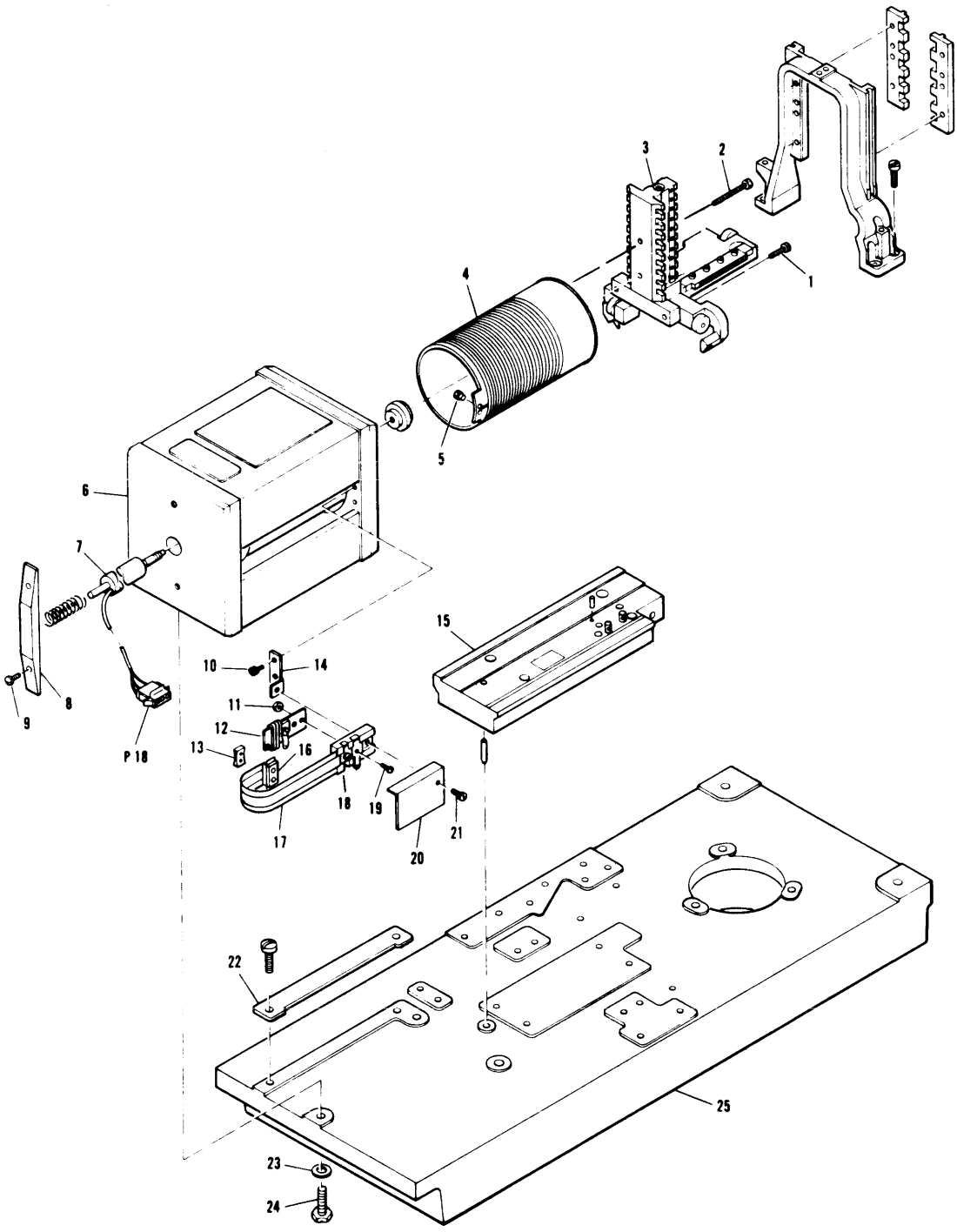


FIGURE 5-16. DECK PLATE ASSEMBLY

12. Slide the linear motor assembly (including tachometer and rod) to the rear and place it on a nonmagnetic surface.

WARNING

The linear motor is very heavy and has a strong magnetic attraction. Any attempt to place it near a magnetic surface may unbalance you and result in damage to the motor or injury to you.

13. Remove the linear motor cable cap (8) and slide the tachometer (7) and rod out of the linear motor (6). Place the tachometer and rod at least 2 feet away from the linear motor.

14. Place the linear motor on its side and position the flex conductor assembly so that the bobbin connection is exposed.

15. Pre-tin the soldering iron with 60/40 tin/lead solder and unsolder the two aluminum wires that connect the bobbin (4) to the flex conductor assembly (17).

16. Remove the two screws (16) that hold the flex conductor assembly (17) to the bobbin (4). The flex conductor assembly can now be removed from the linear motor assembly.

17. Remove the bobbin terminal pad (13).

18. Push the bobbin terminal nuts (5), one at a time, into the nut insertion hole in the linear motor armature and then remove them.

NOTE

There is a hole drilled in the linear motor pole piece to allow inserting and removing these nuts.

19. Remove the bobbin coil (4).

5.15.2 Preassembly (See Figure 5-16.)

1. Inspect new bobbin assembly to assure that the aluminum leads have not been damaged in transit. Do not flex the leads excessively.

2. Insert the bobbin assembly (4) into the linear motor assembly(6).

3. Using a soldering iron, clean all old solder from the mounting pads of the flex conductor assembly (17). Be sure to open the hole in the center of each pad. Tin the entire surface with a fresh coat of tin/lead solder.

4. Mount the bobbin terminal nuts (5) one at a time by placing them into the linear motor nut insertion hole and pulling them up into the correct position in the bobbin assembly (4) with mounting screws (16) (not shown).

5. Once the bobbin terminal nuts are in place, partially remove the bobbin assembly from the linear motor. This will inhibit the bobbin terminal nuts from dropping back into the motor pole piece holes when the mounting screws (16) are removed.

6. Mount the bobbin terminal pad (13) and flex conductor assembly (17) using the two mounting screws (16).

5.15.3 Soldering (See Figure 5-16.)

1. Insert the tinned end of the red lead from bobbin assembly down through the hole in the lower pad of the flex conductor assembly (bobbin assembly enters the linear motor assembly from the right) and insert the tinned end of the black lead down through the hole in the upper pad. The black and red leads will not cross if the assembly is correct.

2. Bend the tinned portions of the leads so that they lie flat on top of the flexible conductor mounting surfaces. Make sure the leads are not touching the linear motor.

NOTE

The bobbin leads have had a double tinning process applied that allows the aluminum wire to be compatible with tin/lead solder. Excessive heat from the soldering iron may cause this treatment to "de-wet," in which case the bobbin assembly will have to be replaced.

3. Tin the soldering iron with 60/40 tin/lead solder.

4. Solder the two wires to their respective pads as follows: place the soldering iron tip on the bobbin lead and apply tin/lead resin core solder to the tip. Assist the flow of solder by moving the iron tip back and forth along the bobbin lead wire. Continue applying the solder and moving the iron until the bobbin lead is fully imbedded in the newly applied solder. Allow the joint to cool, and inspect it for any excess solder which may have flowed off the terminal pad. Remove any excess solder.

5.15.4 Assembly (See Figure 5-16.)

1. Place the linear motor assembly on the deck plate and align it against the guide bar (22) and the way (15). Secure the motor using the three bolts (24). Verify that tightening these bolts has not caused the motor to move.

2. Remove the tachometer rod from the tachometer. Keep the rod at least 2 feet from the linear motor. Insert the tachometer (7) into the linear motor (6).

3. Insert the tachometer rod into the tachometer and screw it into the back of the carriage assembly (3).

4. Push the carriage assembly (3) to the rear and attach it to the bobbin assembly (4) using the three screws (1, 2, and the one not shown). Be sure to reconnect the carriage ground assembly to the carriage, reversing the procedure in 5.15.1, step 3. This must be done while the bobbin is fully retracted into the motor to provide for correct alignment and clearance as checked below.

5. Slide the bobbin coil forward ½ inch and verify that there is clearance between the bobbin coil (4) and the linear motor pole piece inside the linear motor assembly (6) by pushing on the back of the bobbin. The bobbin must be free to move left, right, up, and down. Push the carriage forward to approximately cylinder 200 (restrain the carriage during launch so the heads do not slap). Again verify that the bobbin is free of the linear motor.

6. Install the linear motor cable cap (8) and reconnect the tachometer at P/J18.

7. Mount the temperature sensor assembly (12) on the flex conductor assembly (17) with nuts (11) and install the combined assemblies and plastic guard on the linear motor using the screw (21).

8. Reconnect the linear motor power leads. The white lead connects to the terminal on the temperature sensor while the black lead connects to the right-hand terminal on the flex conductor assembly.

9. Manually retract the heads.

10. Install head assemblies 8 and 9.

5.15.5 Testing

1. Remove the +55 V fuse, F4.

2. Connect the drive to a Memorex 120-2 Off-Line Tester. Turn on the main power switch (S1) and leave the START-STOP switch in the STOP position.

3. Place a "scratch" disc pack on the drive.

4. Ground A08, pin 10. The disc pack should start spinning.

5. After the disc pack is up to speed, push the carriage forward and launch the heads. Manually position the carriage back and forth; there must not be any binding or drag.

6. Manually retract the heads, turn off the main power switch (S1), and then replace the +55 V fuse, F4.

7. Turn on the main power switch (S1) and allow the disc pack to come up to speed (about 10 seconds).

8. Hold the heads retracted switch in the retracted position and manually push the heads into the pack as far as cylinder 000.

9. Be sure your fingers are free of the carriage and then release the heads retracted switch; the carriage must go to the fully retracted position. Carriage motion in the forward direction indicates the motor leads are reversed. If this occurs, immediately turn off the main power switch (S1), manually retract the heads, and reverse the leads connected in 5.15.4, step 8.

10. Place the START-STOP switch in the START position and allow the drive to complete a first seek. Run random seeks for at least 5 minutes to assure proper assembly.

11. Remove the jumper from A08, pin 10.

12. Align heads 8 and 9 as instructed in Section 5.7.

13. Place the START-STOP switch in the STOP position and turn off the main power switch (S1).

5.15.6 Final Assembly

1. Install the left cover assembly and the back cover assembly.

2. Install the control cover assembly.

3. Turn on the main power switch (S1) and install the front cover assembly.

4. Return the drive to the system.

5.16 CARRIAGE WAY AND LINEAR MOTOR ALIGNMENT PROCEDURE

This procedure is to be followed when aligning the carriage way to the spindle following the replacement of the carriage way or whenever alignment is in question. The procedure requires the Carriage Alignment Tool Gauge (P/N 201452), the Carriage Alignment Tool Arm (P/N 201453), and the Linear Motor Alignment Tool (P/N 202419).

1. Turn off the main power switch (S1).

2. Remove the control cover assembly and pack enclosure assembly.

3. Remove the disc pack shroud.

4. Remove the following head/arm assemblies: 7-D, 8-B, 9-A, and 10-C.

5. Remove the three bobbin mounting screws and disconnect the tach rod from the Tee-block. (Refer to Figure 5-16.)

6. Loosen the linear motor mounting bolts and slide the motor away from the carriage way.

7. Loosen the four carriage way mounting bolts.

8. Place the alignment gauge on the spindle and install the stepped end of the alignment tool arm on the Tee-block in place of head/arm 9-A. (See Figure 5-17.)

9. Holding the arm in place with one hand, slowly and carefully load the heads and then slide the carriage through its full travel. Adjust the way by rotating it about its locating dowel pin to obtain 0.005 inches clearance between the arm and the gauge. This clearance must be maintained along the entire length of travel of the carriage (Figure 5-17).

10. Tighten the carriage way mounting bolts.

11. Recheck the adjustment by repeating steps 8 and 9. Remove the gauge and arm.

12. Remove the plastic tach coil retainer from the rear of the linear motor by removing the two mounting screws. Remove the tach coil and tach rod as one assembly.

CAUTION

Avoid tach-rod demagnetization which can be caused by contact with steel or magnetic objects such as the linear motor magnets, tools, or retaining spring. Do not drop the tach rod.

13. Loosen the retaining screws on the linear motor guide bar.

NOTE

This guide bar is used to locate the linear motor when it must be removed and reinstalled in the same location, such as during bobbin replacement.

14. Reposition the linear motor against the way. Insert the Linear Motor Alignment Tool through the tach coil hole in the linear motor and into the tach rod hole in the Tee-block.

CAUTION

The flat portion at the rear of the alignment tool must be up and parallel to the top surface of the deck plate during this adjustment to locate the diamond pin properly.

Position the linear motor so that the alignment tool slides freely in the linear motor while held to the Tee-block throughout the entire length of travel of the carriage.

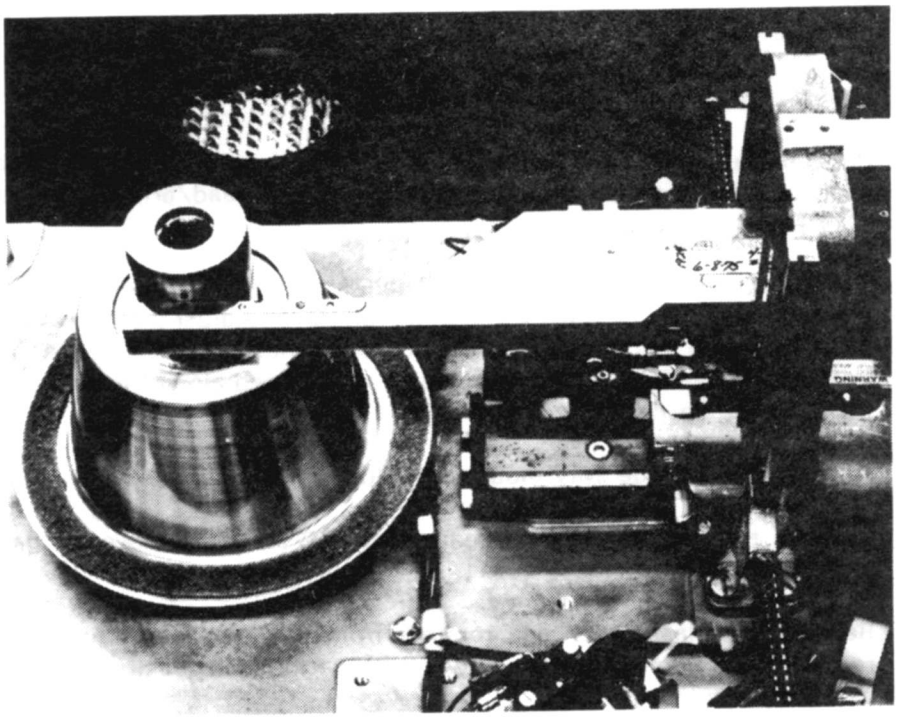


FIGURE 5-17. CARRIAGE WAY ALIGNMENT

15. Tighten the linear motor mounting bolts.

16. Recheck the linear motor alignment by repeating step 14.

17. Position the linear motor guide bar against the linear motor and tighten the retaining screws.

18. Replace the tach coil and tach rod. Check for tach rod interference (see 6.1.17).

19. Replace the tach coil spring and plastic retainer.

20. Position the bobbin on the carriage and Tee-block so that, throughout its travel, it does not rub against the linear motor pole piece. Tighten the mounting screws.

21. Replace the head/arm assemblies.

22. Replace the disc pack shroud and enclosure assembly.

23. Replace the control cover assembly.

24. Install a scratch disc pack.

25. Turn on the main power switch (S1), and start the drive using the Memorex 120-2 Off-line Tester.

26. Run in the random seek mode to ensure the absence of HDI.

27. Remove the scratch disc pack and install the CE disc pack.

28. Adjust the alignment on the heads which were just removed and check the alignment on the remaining heads (see 5.7).

29. Check the alignment of the index transducer and adjust as required (see 5.4).

30. Stop the drive and remove the tester and the CE disc pack.

5.17 CARRIAGE LOAD FORCE (PRELOAD) ADJUSTMENT

To adjust for a positive force on the carriage load bearing and ensure that the load bearing maintains full contact with the carriage way, proceed as follows. This procedure requires the Carriage Torque Wrench (P/N 200965).

1. Turn off the main power switch (S1).

2. Remove the control cover assembly and the pack enclosure assembly.

3. Remove the disc pack shroud.

4. Insert the Carriage Torque Wrench under the carriage load bearing axle (see Figure 5-18) and check the torque required just to separate the bearing from the surface of the way. This torque must be 17 ±1 inches-lb. If this torque is not obtained, tighten the locking nut (Figure 5-18) while ensuring that the bearing is against the way. Continue tightening the locking nut until the load of the bearing on the way is from 16 to 18 inches-lb.

CAUTION

Forces less than 16 inches-lb may cause data and seek errors while forces greater than 18 inches-lb cause excessive wear to the bearing system.

5. Turn on the main power switch (S1), and start the drive using the 120-2 Off-line Tester.

6. Perform 10 to 20 restore seek operations and, after stopping the drive, recheck the load force and verify that the bearing is in full contact with the carriage way.

7. Replace the disc pack shroud, pack enclosure assembly, and control cover assembly.

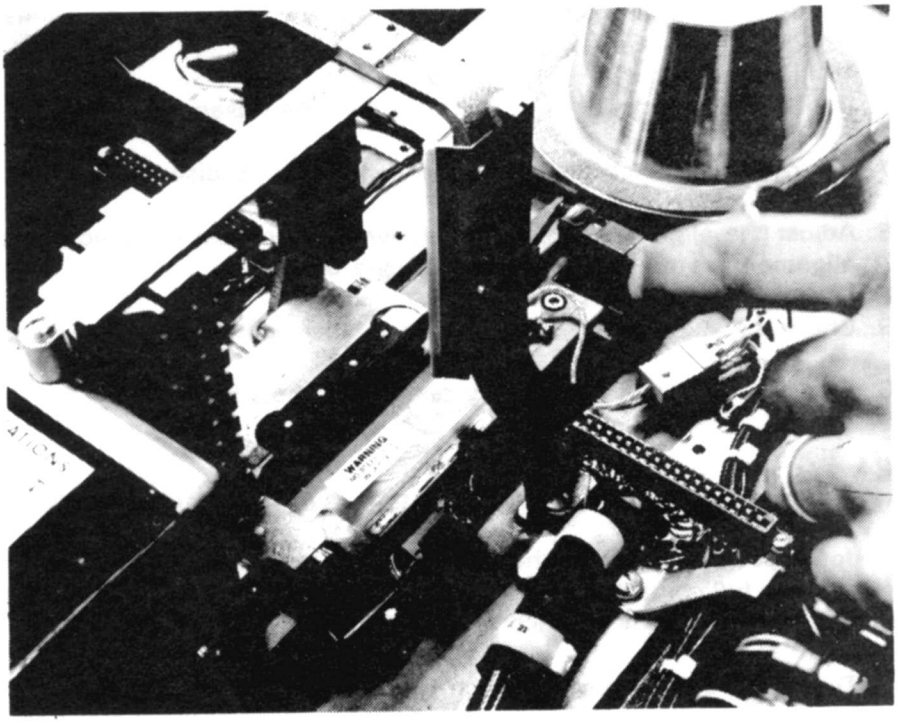


FIGURE 5-18. CARRIAGE LOAD FORCE ADJUSTMENT

SECTION 6
SCHEDULED AND UNSCHEDULED MAINTENANCE

6.1 PREVENTIVE MAINTENANCE

Preventive maintenance for the drive consists of both scheduled and unscheduled maintenance routines. A tabulation of preventive maintenance routines is given in Table 6-1. The table lists the frequency, where applicable, and provides references to the maintenance manual section where the procedure to be performed is given. Maintenance will require the use of a Lubrication Kit and a Head Cleaning Kit.

Maintenance operations should be performed at the indicated intervals to assure reliable operation of the drive. Preventive maintenance should be limited to these routines as long as the drive is functioning normally.

TABLE 6-1. PREVENTIVE MAINTENANCE CHART

PROCEDURE	REFERENCE	FREQUENCY
Fan Rotation Check (visual check)	—	1 month
Air Filter Inspections	6.1.1	1 month
Pack Shroud Cleaning	6.1.2	1 month
Head Inspection and Cleaning	6.1.3	1 month
Detent Rack Cleaning and Pawl Lubrication	6.1.4	2 months
Spindle Oiling	6.1.5	2 months
Detent Pawl Oiling	6.1.6	2 months
Spindle Brake Oiling	6.1.7	2 months
Carriage Way Oiling	6.1.8	2 months
Air Filter Replacement	6.1.9	6 months
Plunger/Pawl Clearance Check	6.1.10	6 months
Detent Reed Cleaning	6.1.11	6 months
Detent Actuator/Wiper Oiling	6.1.12	6 months
Plunger/Washer Oiling	6.1.13	6 months
Detent Pivot-Block/Wick Oiling	6.1.14	6 months
Absolute Filter Replacement	6.1.15	1 year
Head Unload Cam Replacement	See 5.8	1 year
HDI Prevention and Recovery	6.1.16	As required
Linear Tachometer Maintenance	6.1.17	As required

6.1.1 Air Filter Inspections

Inspect the intake air filter below the main blower at the bottom of the cabinet. Replace if there is evidence of an accumulation of dirt which would restrict air flow.

Also inspect the air filter at the rear of the logic assembly. Replace if there is evidence of an accumulation of dirt which would restrict air flow.

6.1.2 Pack Shroud Cleaning

Using a vacuum cleaner, clean any accumulated loose dirt from all interior surfaces of the pack shroud. Remove any remaining particles with adhesive tape.

6.1.3 Head Inspection and Cleaning

Check the bearing surfaces and bleed holes of the heads for contamination. Contamination is the presence of slight oxide streaks on the bearing surfaces, oxide buildup around the periphery, or an excessive accumulation of oxide or other foreign material in the bleed holes. Clean only those heads that show signs of contamination. If dark brown or black streaks (burned oxide or aluminum) exist on a bearing surface, the head has experienced Head-to-Disc Interference (see Section 6.1.16) and must be replaced.

If the head shoes need cleaning, clean the heads per the following procedure using a cleaning kit (P/N 202159).

1. Remove the shroud-area top cover, the disc pack, and the shroud. Turn off the main power switch (S1) located on the interior control panel.

2. Move the carriage out by hand until the load/unload ramp is just at the point of riding off the cam. Do not load the heads.

3. Wrap a Kimwipe* tissue around a head paddle (a wooden tongue depressor will do) and dampen (do not soak) one end of it with 91% isopropyl alcohol (9% distilled water). Wipe the bearing surface of each head thoroughly with the dampened portion of the Kimwipe. After wiping the bearing surface with the dampened end of the paddle, push the paddle further into the assembly and use the dry portion of the Kimwipe to dry the surface of the head. Remove the paddle by pushing it toward the center of the carriage until it is clear of the cleaned head and then pull it out. This technique will prevent the dampened portion of the Kimwipe from contacting the cleaned surface of the head.

CAUTION

It is extremely important that the surface of the head be dried immediately after cleaning with alcohol to prevent evaporation which will result in a residue on the bearing surface.

*Kimwipe is a trade mark of Kimberly Clark.

4. After all contaminated heads have been cleaned, check the flexures and arm assemblies for loose pieces of Kimwipe tissue and remove them.

5. Return the carriage to the retracted position and inspect the gimbal flexures and arms for broken welds. Replace any defective assemblies.

6. Replace the shroud and disc pack and turn the main power switch back on.

7. Start the drive.

8. Replace the remaining covers.

NOTE

There is no scheduled preventive maintenance for disc packs. If the packs are handled properly and the drive is maintained regularly, there is no need for pack cleaning.

6.1.4 Detent Rack Cleaning and Pawl Lubrication

Clean the surface of the detent rack with a soft bristle brush dampened with 90% isopropyl alcohol (from the Head Cleaning Kit). Use a Kimwipe tissue to lightly coat the rack and pawls with hydraulic oil (from the Lubrication Kit) to retard corrosion.

6.1.5 Spindle Oiling

Apply a drop of hydraulic oil to the threads at the top of the spindle to ensure easy removal of the disc packs.

6.1.6 Detent Pawl Oiling

Apply two drops of hydraulic oil between the detent pawls. (Shroud must be removed.)

6.1.7 Spindle Brake Oiling

Place a drop of hydraulic oil between the washer and pawl of the mechanical spindle brake. Compress the spring on the brake spindle to separate the washer and pawl.

6.1.8 Carriage Way Oiling

Clean the carriage way with a Kimwipe dampened with isopropyl alcohol and wipe dry Apply a light coat of hydraulic oil on the carriage way (under the rollers) where the carriage bearings come into contact.

6.1.9 Air Filter Replacements

Replace both the intake air filter located under the blower motor and the air filter located at the rear of the logic assembly.

6.1.10 Plunger/Pawls Clearance Check

Check for 0.005 to 0.008 inches of clearance between the plunger and detent pawls. Remove shims if necessary to meet specification. Replace plunger with a new one if clearance is greater than 0.008 inches with no shims.

6.1.11 Detent Reed Cleaning

Clean any accumulated wear particles from the detent reed located under the detent actuator cap.

6.1.12 Detent Actuator/Wiper Oiling

Add one drop of hydraulic oil to the hole on the top of the detent actuator to provide proper lubricant to the internal wiper. If wiper is not present, install one.

6.1.13 Plunger/Washer Oiling

Add one drop of hydraulic oil to the felt washer on the front of the plunger. If washer is not present, install one.

6.1.14 Detent Pivot-Block/Wick Oiling

Add six drops of hydraulic oil to the wick at the detent pivot block to keep the pawl's contact surfaces and pivot shaft lubricated.

6.1.15 Absolute Filter Replacement

Replace the Absolute Filter, which filters air to the shroud area. This filter cannot be inspected for accumulation of particles and should be replaced yearly to maintain adequate air flow and filtration.

6.1.16 Prevention, Recognition, and Recovery from HDI

As stated previously, the shoe does not contact the disc, but rides above it on a lubricating film of air.

Head-to-Disc Interference (HDI) results when the lubricating air film fails. The main causes of HDI are foreign particles in the lubricating film, contamination buildup on the surface of the shoe or disc, or a defective disc surface.

Because of the catastrophic propagation tendency of HDI, preventive techniques should be employed to minimize susceptibility, recognition symptoms should be clearly understood, and proper recovery procedures should be followed. Discussions of these areas are given in the following subparagraphs.

6.1.16.1 Prevention of HDI

1. Preventive Maintenance

   Proper preventive maintenance of the drive at the scheduled periods, especially the head/arm assemblies, filtration system, moving parts, and head cams.

2. Handling and Storage

   Packs should always be stored with the covers on, and only in cabinets that are clean and free of dust and foreign particles. The pack covers (top and bottom) should also be together when the pack is removed, and the pack stored in a clean location. Any cracked or broken covers should be replaced immediately. Disc packs should be handled with care to avoid dropping or bumping. Never place a dropped pack on a drive.

3. Access Door

   Never leave the access door on a drive open unnecessarily. The longer it is open, the greater the susceptibility to contamination.

4. Pack Labels

   Use only manufacturer-recommended pack labels installed in the specified locations. Labels that work loose are a source of contamination.

CAUTION

Tobacco smoke and ashes can create serious contamination problems for disc drives and disc packs.

6.1.16.2 Recognition of HDI

HDI may be recognized by one or more of the following symptoms.

1. Repetitive Hard Read Errors— Because of adverse propagation effect, do not move any pack with repetitive hard read errors to more than one additional drive. If errors persist, then the possibility of HDI exists and must be investigated.

2. Audible Tinkling Sound—An audible tinkling sound from the disc which may progress to a screech.

3. Visible Damage—Visible damage on any surface characterized by one of the following:

   a. Any scratch (radial, tangential, or diagonal) where the aluminum substrate is exposed.

   b. Concentric adjacent scratches of any length.

   c. A single scratch over three inches (approximately) in length.

   d. Imbedded particles.

NOTE

The edge of a disc may have aluminum visible and not indicate HDI.

4. Oxide on Bearing Surface in Shoe—Dark brown (oxide) or black streaks (burned oxide and/or aluminum) anywhere on the bearing surface indicates HDI. Slight oxide streaks on the bearing surface, oxide buildup around the periphery, or contamination in the bleed holes may not indicate HDI. Refer to the Preventive Maintenance Procedures for Head Inspection and Cleaning.

   A discoloration of the epoxy around the read/write core also indicates HDI.

6.1.16.3 Recovery from HDI

1. Inspect all heads and determine which ones are involved in the HDI.

2. Replace heads involved in the HDI and clean the remaining heads as described in Section 6.1.3.

3. Inspect all disc packs which were recently on the drive in question for possible damage. If any surface in a pack is badly damaged (cannot be restored to operation by cleaning), then the pack must be replaced. Clean only those disc surfaces that are contaminated or have been involved in the HDI. The cleaning procedure is as follows:

CAUTION

If the shroud is removed while cleaning a pack, surface 19 will be erased.

   a. Remove access plate from side of shroud on the drive.

   b. Install disc pack.

   c. Wrap a Kimwipe around a cleaning paddle (wooden tongue depressor will do) and dampen (do not soak) one side with 91% isopropyl alcohol (9% distilled water).

   d. Insert paddle between discs and exert light pressure on surface to be cleaned while manually rotating the pack.

   e. Slowly withdraw the paddle while the pack is rotating.

f. Immediately turn paddle over and dry the cleaned surface while slowly rotating the pack. Make sure the alcohol is not allowed to evaporate, or harmful residues will form.

g. Slowly withdraw the paddle while the pack is rotating.

h. Check for and remove any remnant pieces of Kimwipe.

i. Replace access plate on the side of the shroud.

4. Mount a good disc pack on the recovered drive and power up. After the drive comes to ready, power down and check for possible HDI. If there are no indications of HDI, power up and run in a random seek mode for 15 minutes. Power down and check for possible HDI. If no indication of HDI exists, align the replaced heads, clean the inner surfaces of the shroud, and restore the drive to operation. If HDI occurs during any of the above operations, repeat the entire recovery procedure.

5. If the damaged pack was salvageable, then certify the pack by placing it on a drive and following the procedures outlined in step 4.

6. Check for possible HDI on all the heads in all the drives on which the damaged pack was used. If any indication of HDI exists, repeat the entire recovery procedure for each drive affected.

6.1.17 Linear Tachometer Maintenance

A faulty linear tachometer can result in seek errors. Two likely areas of trouble with the tachometer are tach rod interference and tach rod demagnetization.

6.1.17.1 Tach Rod Interference (Rubbing)

To check for tach rod interference, proceed as follows:

1. With a CE disc pack in place and spinning, remove F4, the +55 vdc power supply fuse. This disables the servo.

2. Manually position the carriage to the forward stop.

3. Remove the plastic tach retainer from the rear of the linear motor by removing the two mounting screws.

4. Note the relationship of the tach rod to the tach coil as the carriage is manually repositioned to the fully retracted position. The tach rod must not rub against the tach coil sufficiently enough to move the coil. Although full clearance should exist between the tach rod and the tach coil, a slight rubbing (insufficient to move coil) is acceptable.

5. If rubbing is excessive, replace the complete tach assembly.

6.1.17.2 Tach Rod Demagnetization

Tach rod demagnetization can be caused in several ways:

1. Contact with steel or magnetic objects such as linear motor magnets, tools, or tach coil retaining springs.

2. Dropping the tach rod.

3. High temperature—over-temperature condition on the linear motor which damages the bobbin.

4. Tach rod to tach coil interference.

A demagnetized tach rod can be detected by performing the checks in Section 5.6.2, Servo Adjustment Procedure.

6.2 TROUBLESHOOTING

Figure 6-1 (Sheets 1 through 11) presents a flowchart for use in troubleshooting the drive in the field. The flowchart begins with an assumed drive malfunction or failure. Possible origins of the failure are traced by sequences of decision and processing functions. The decision functions constitute yes-no questions on the observable symptoms of failure. The processing functions constitute instructions which process both the yes and no responses to the questions. Using the flowchart should aid service personnel in isolating the failure to a general functional area or mechanical section of the drive. Eliminating the cause of failure can then be accomplished by adjustment or replacement of malfunctioning components.

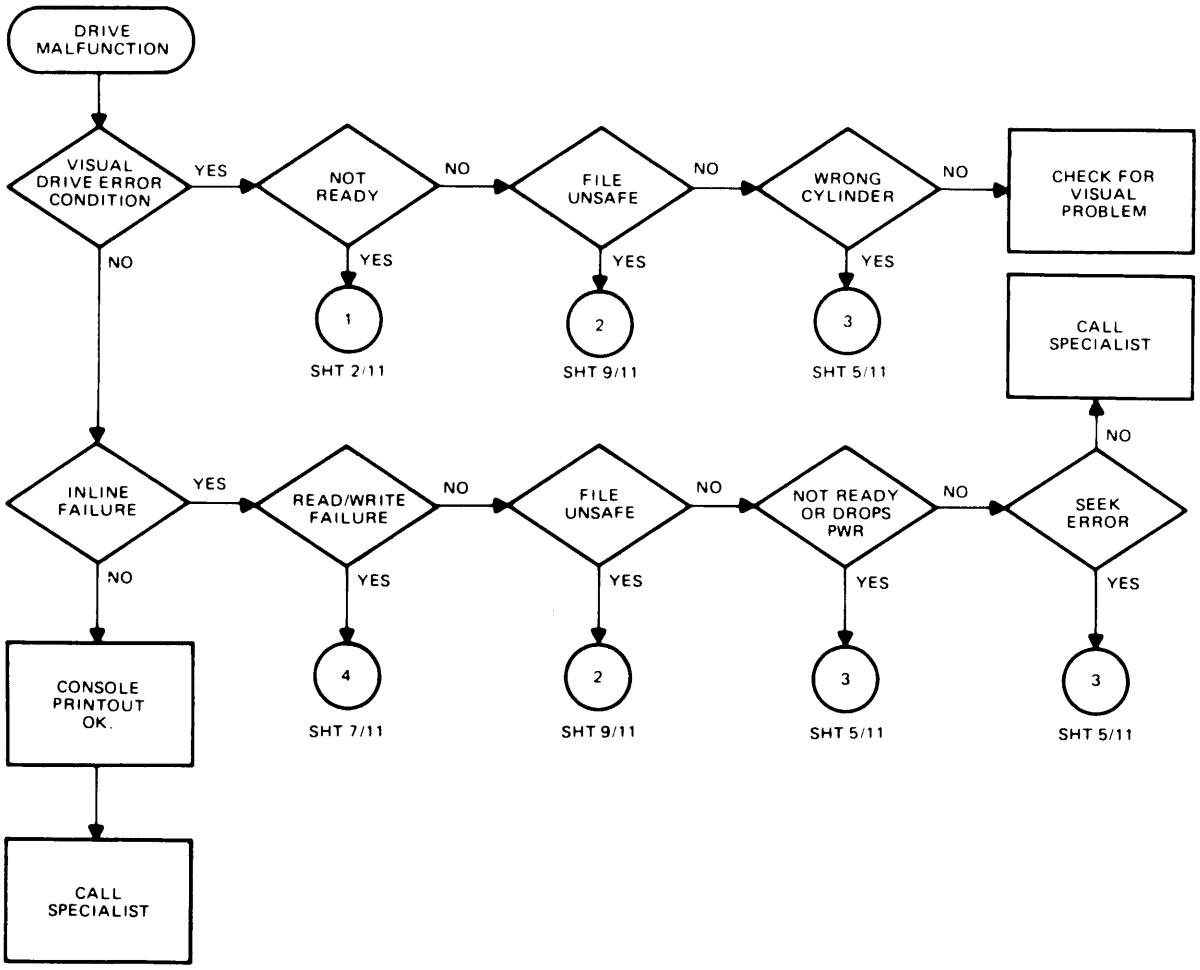


FIGURE 6-1. TROUBLESHOOTING FLOWCHART (Sheet 1 of 11)

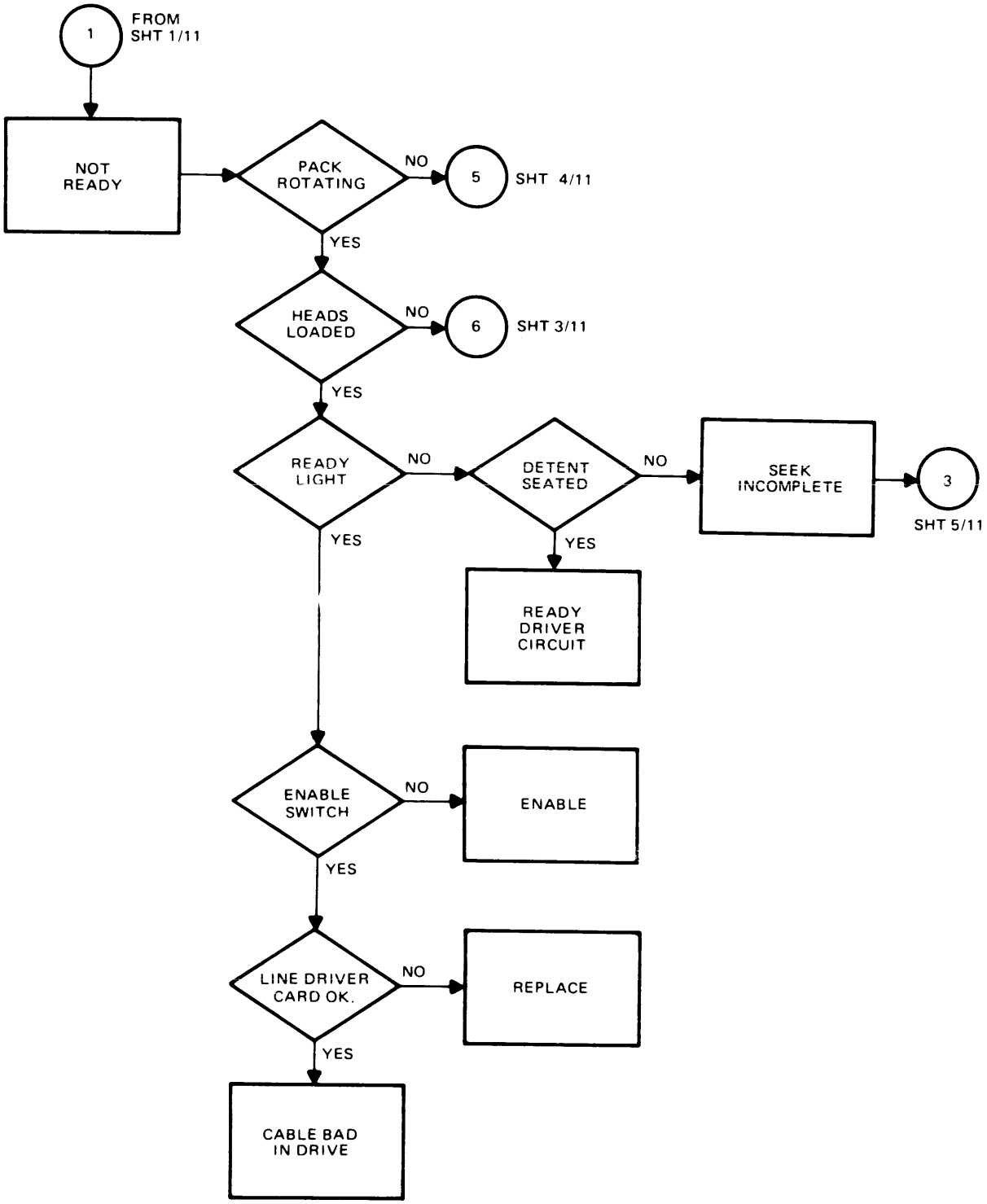


FIGURE 6-1. TROUBLESHOOTING FLOWCHART (Sheet 2 of 11)

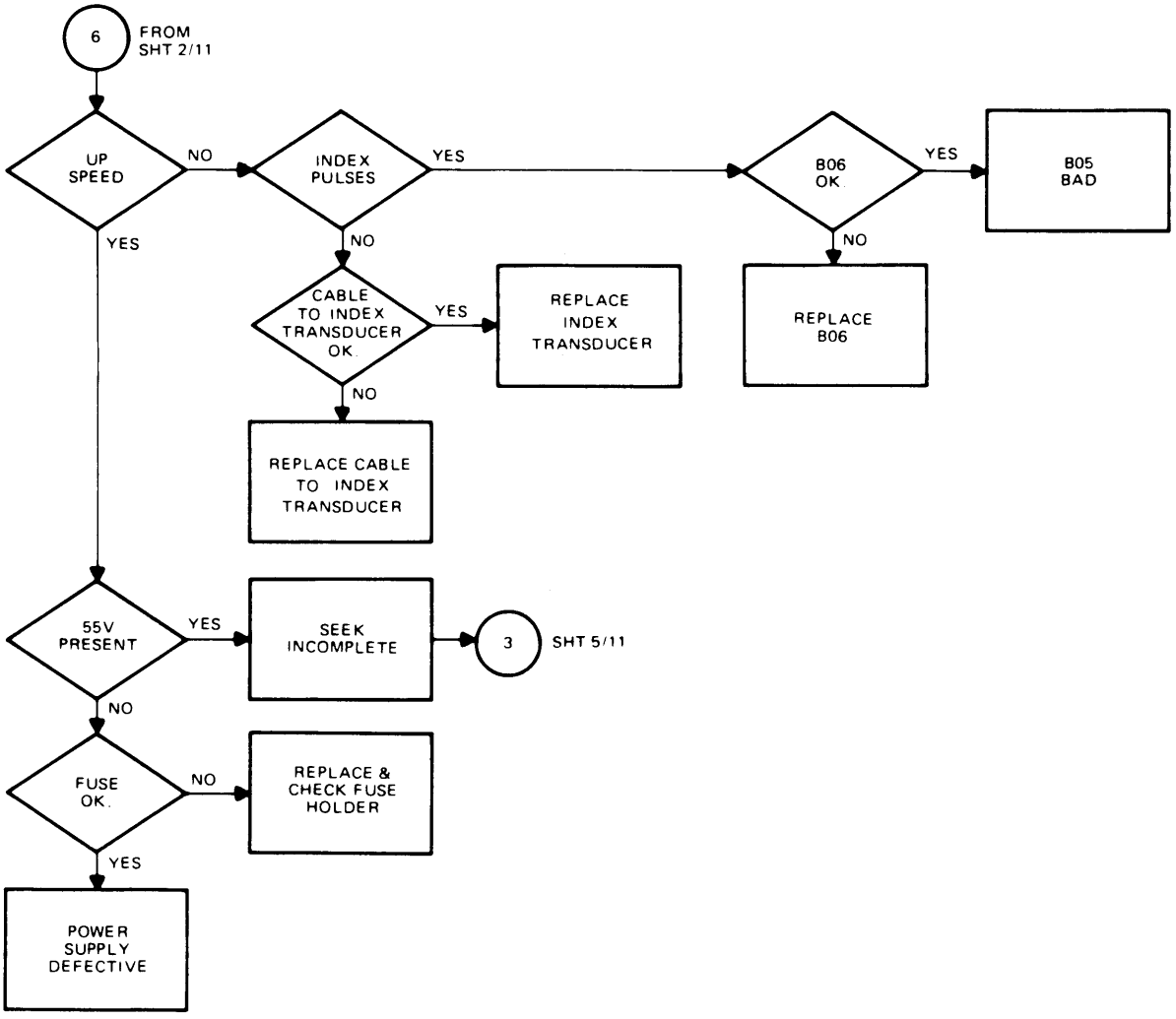


FIGURE 6-1. TROUBLESHOOTING FLOWCHART (Sheet 3 of 11)

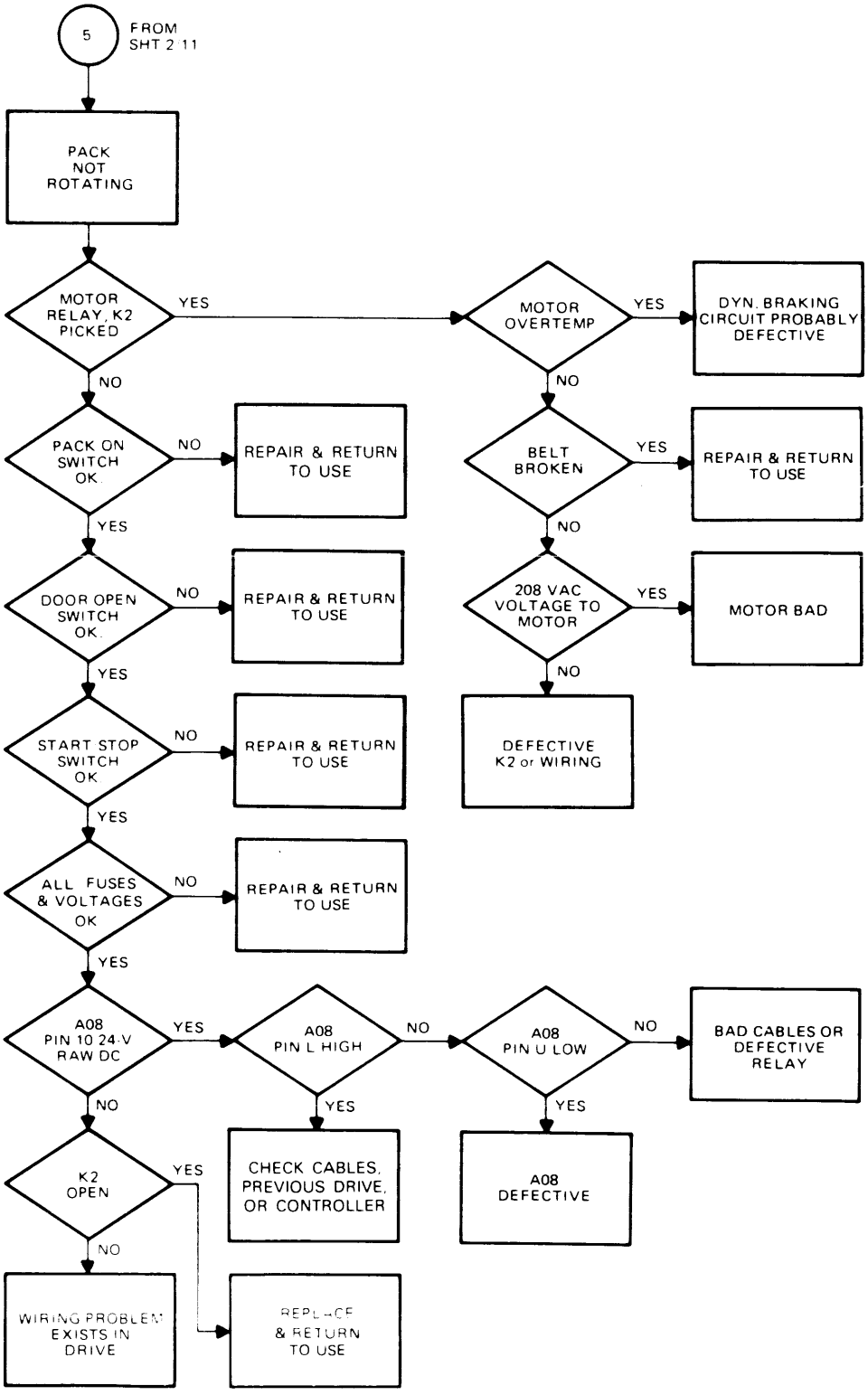


FIGURE 6-1. TROUBLESHOOTING FLOWCHART (Sheet 4 of 11)

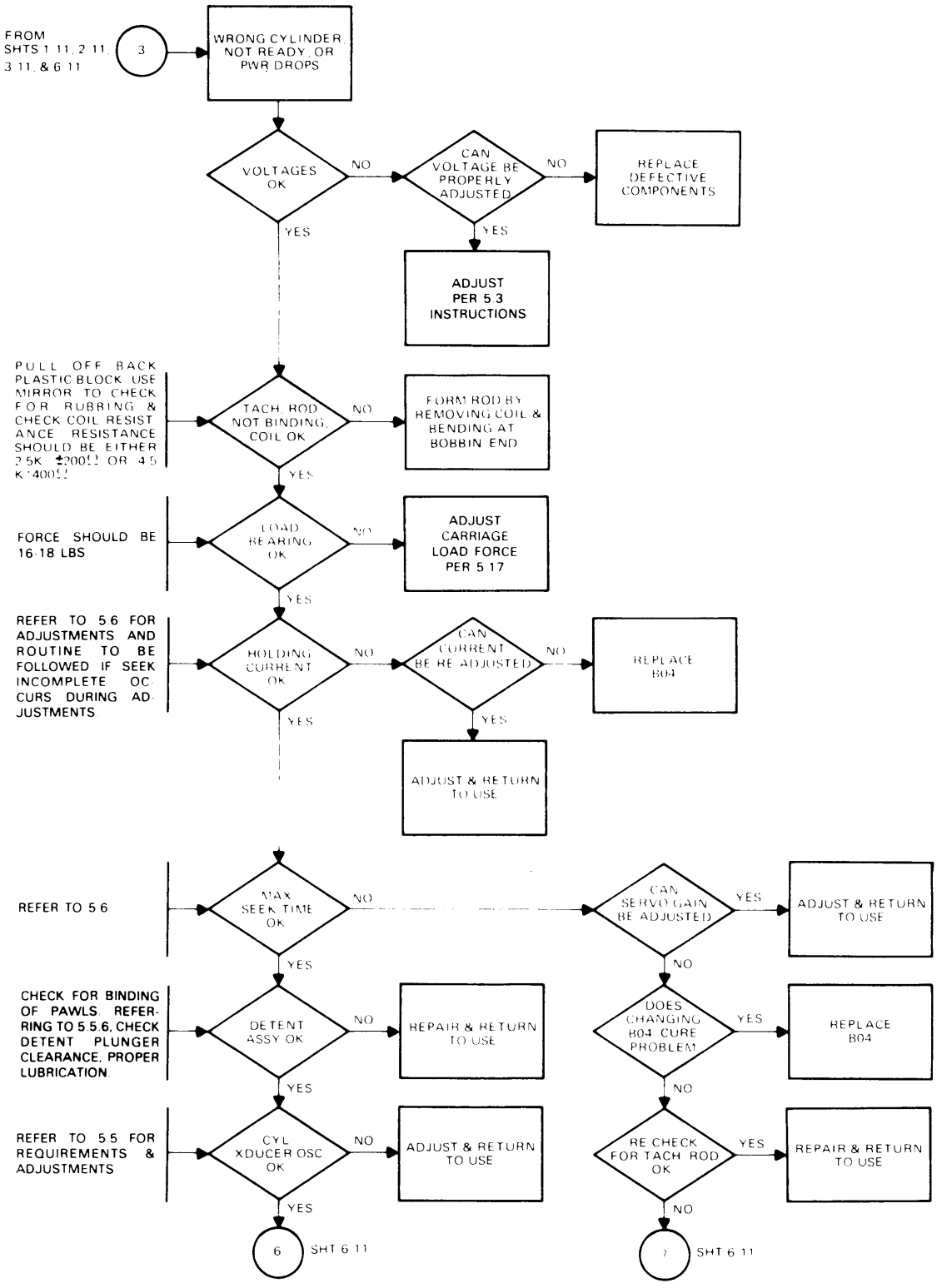


FIGURE 6-1. TROUBLESHOOTING FLOWCHART (Sheet 5 of 11)

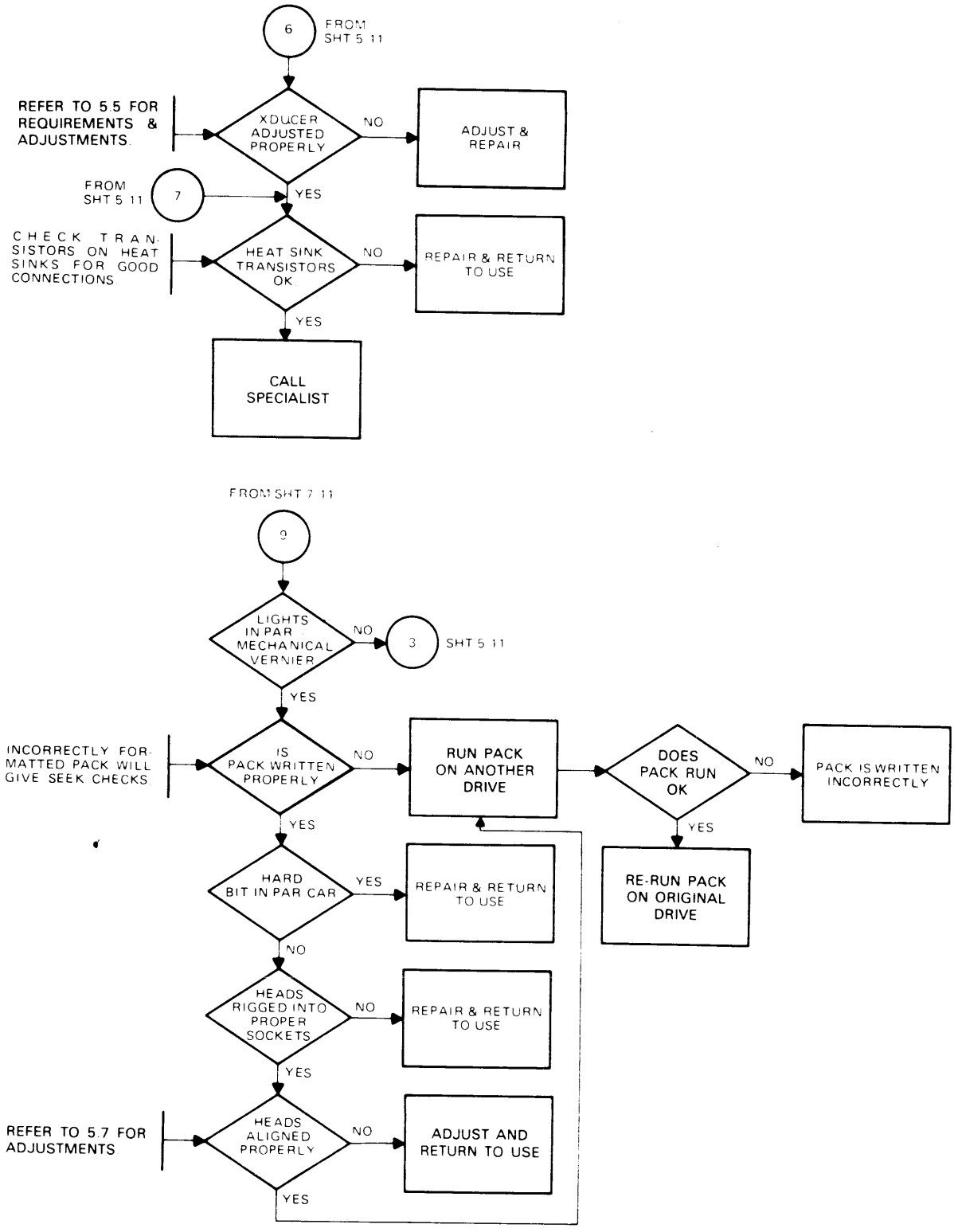


FIGURE 6-1. TROUBLESHOOTING FLOWCHART (Sheet 6 of 11)

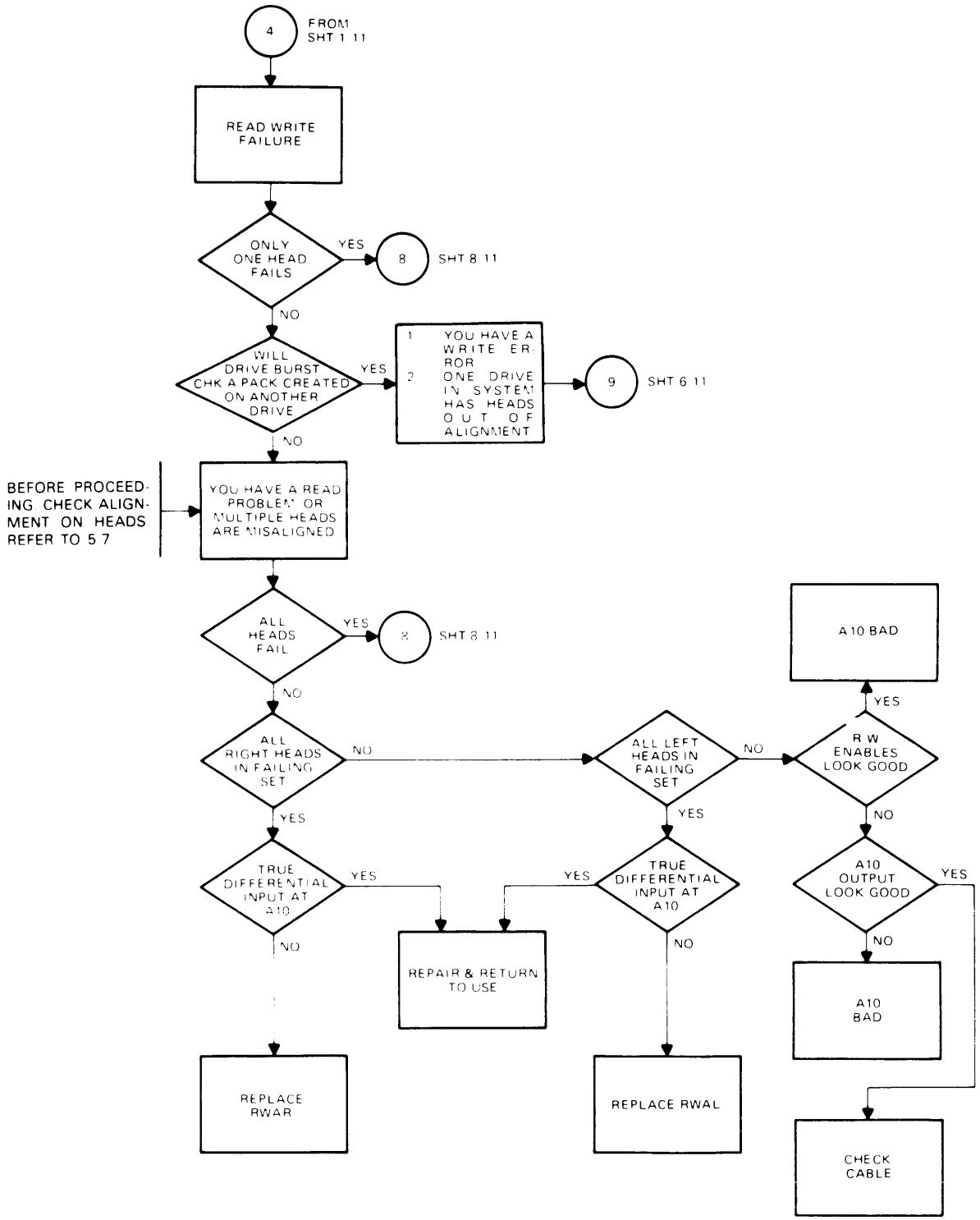


FIGURE 6-1. TROUBLESHOOTING FLOWCHART (Sheet 7 of 11)

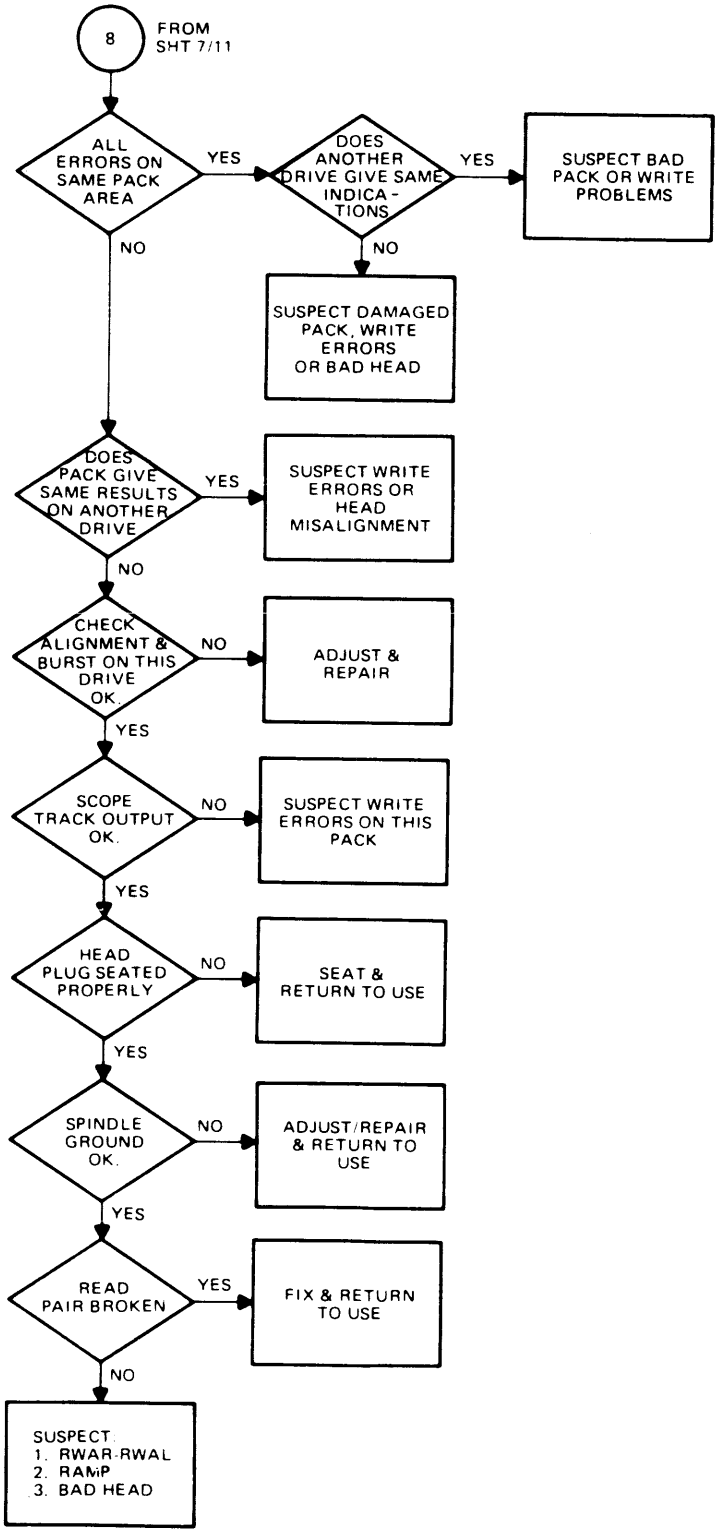


FIGURE 6-1. TROUBLESHOOTING FLOWCHART (Sheet 8 of 11)

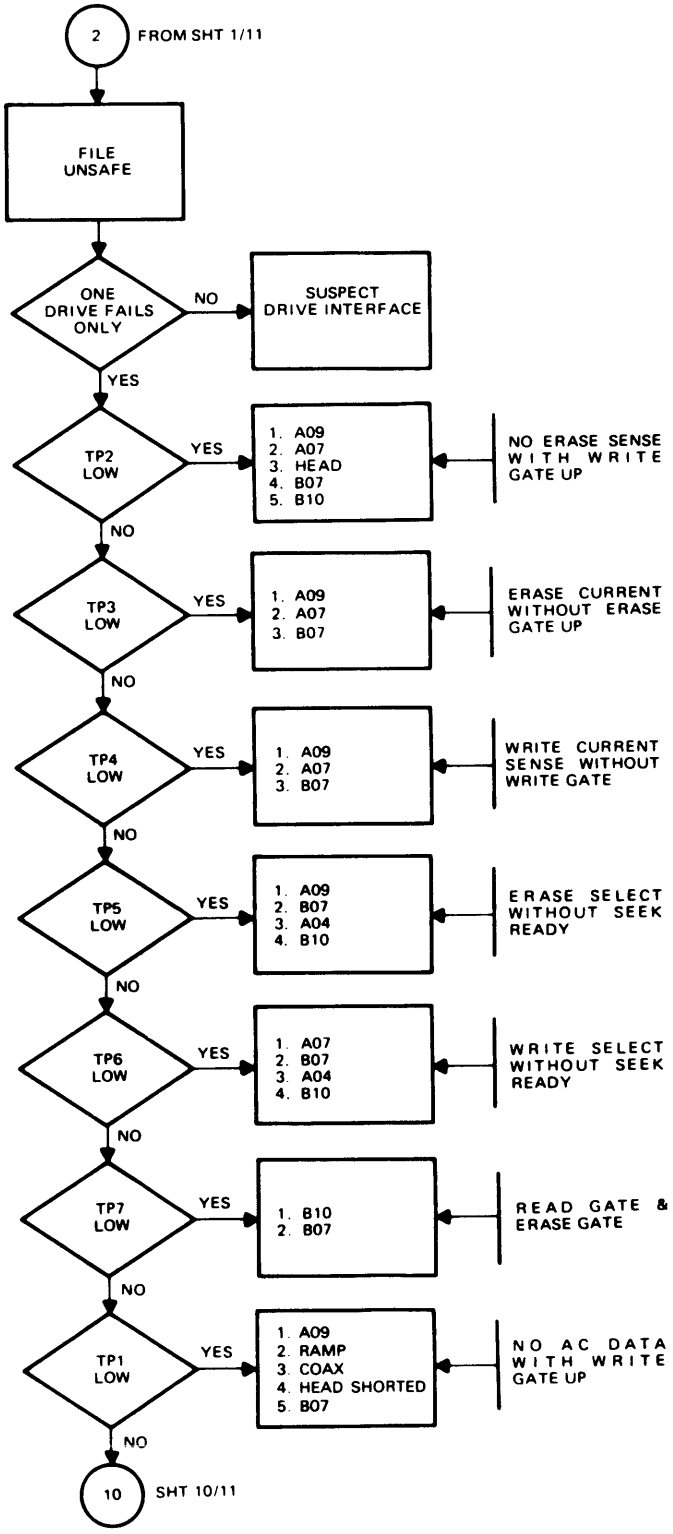


FIGURE 6-1. TROUBLESHOOTING FLOWCHART (Sheet 9 of 11)

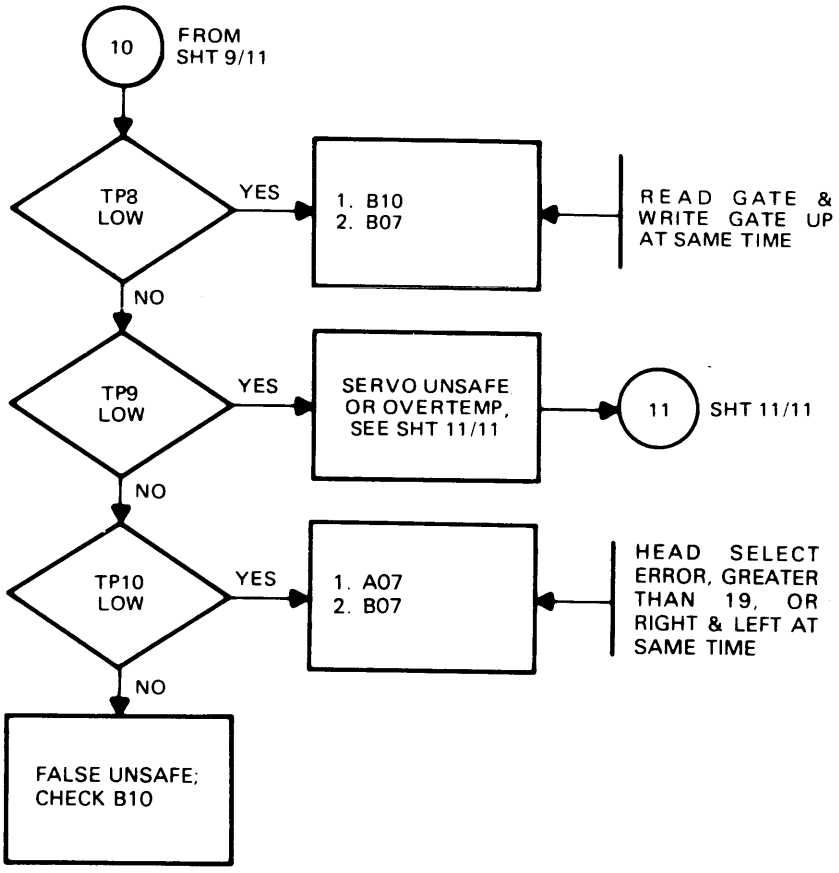


FIGURE 6-1. TROUBLESHOOTING FLOWCHART (Sheet 10 of 11)

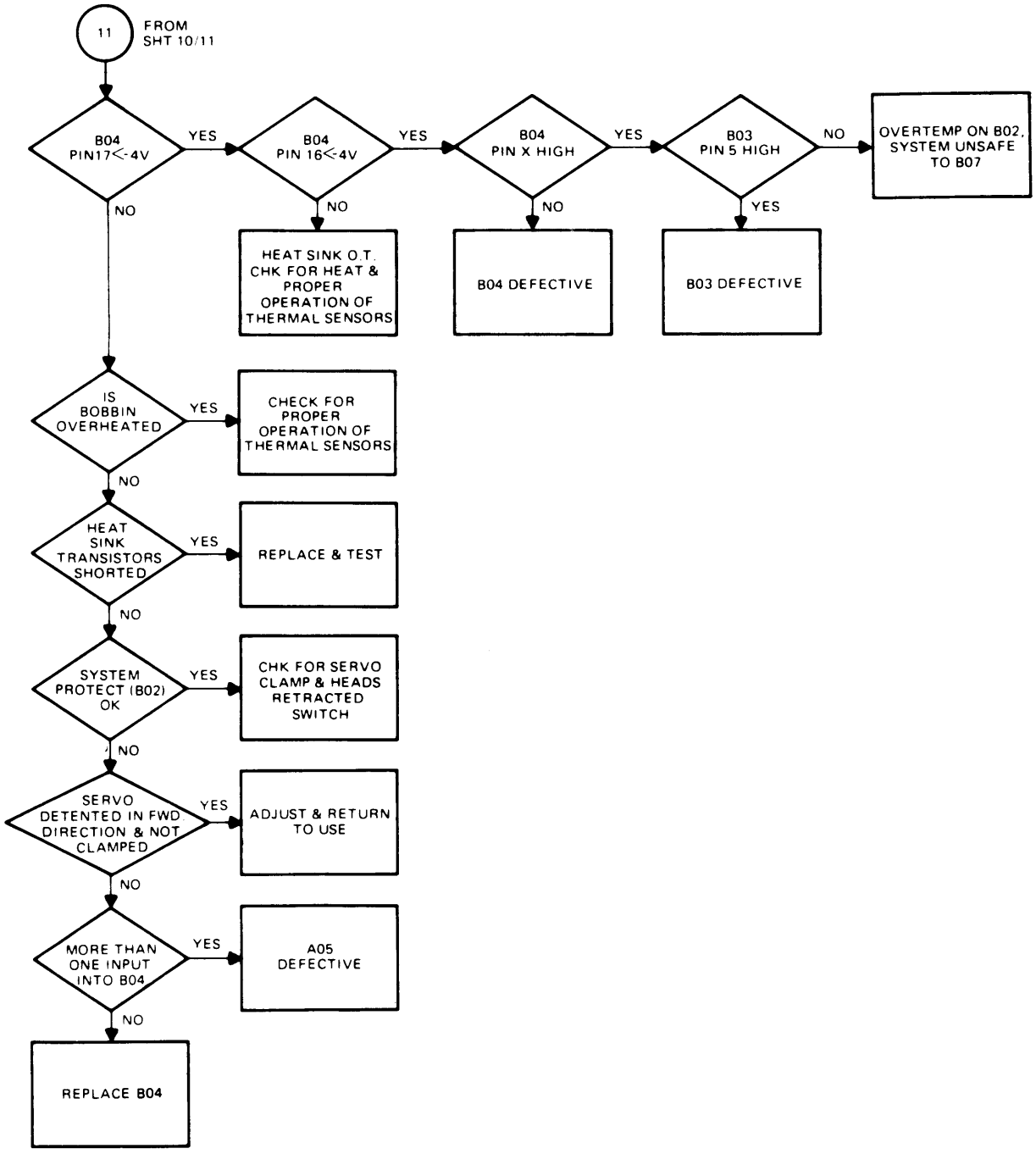


FIGURE 6-1. TROUBLESHOOTING FLOWCHART (Sheet 11 of 11)

APPENDIX A
LOGIC STANDARDS AND INTEGRATED CIRCUIT INFORMATION

This section of the manual defines standard Memorex Disc Storage Drive Logic levels and logic symbols, and presents schematic and connection diagrams for the integrated circuits used in the drive. The section is primarily developed to aid in the interpretation of the logic diagrams presented in Volume B of this manual.

VOLTAGE LEVELS FOR THE TWO LOGIC STATES

The following voltage levels and state terms are defined for the two logic levels:

Logical 1	High	Nominally +5 volts.
Logical 0	Low	Nominally 0 volts.

INVERSION SYMBOL

A small circle at the input(s) of a logic symbol indicates that a relative low input signal activates the function. The absence of a small circle indicates that a high relative input activates the function. A small circle at the output of a function indicates that the output of the activated function is a relative low. Conversely, the absence of a small circle at the output indicates that the output of the active function is a relative high.

LOGIC SYMBOLS AND DEFINITIONS

The following logic symbols and definitions outline the rules governing symbology for the drive logic diagrams.

AND, NAND, OR, NOR Functions

Output of the AND function, as it is used in drive logic, is active when all its inputs are active. Any nonactive AND inputs will cause a nonactive output. Output of the OR function is active when any one or more input(s) is active. The output of an OR function is nonactive when all inputs are nonactive.

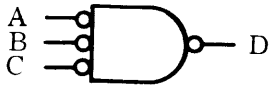
The NAND function is defined as the same as the AND function, except inversion is accomplished. The NOR function is defined as the same as the OR function, except inversion is accomplished.

NOTE

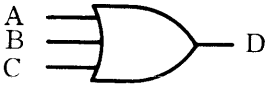
The above activity definitions do not refer to logical one or logical zero, or to electrical levels or states.

A bar at the input of any gate indicates power gate.

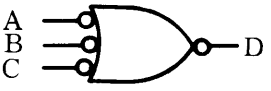
Positive AND Function—Output is high when all inputs are high.



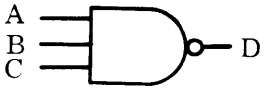
Negative AND Function—Output is low when all inputs are low.



Positive OR Function—Output is high when one or more input is high.



Negative OR Function—Output is low when one or more input is low.



Positive NAND Function—Output is low when all inputs are high.

Negative NAND Function—Output is high when all inputs are low.

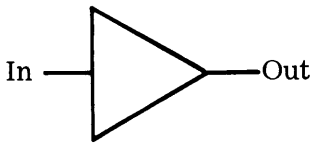
Negative NOR Function—Output is high when one or more input is low.

Positive NOR Function—Output is low when one or more input is high.

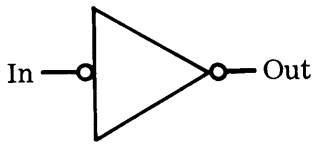
Exclusive OR Function—Output is high when A or B is high, but not when both A and B are high or low.

Amplifiers/Inverters

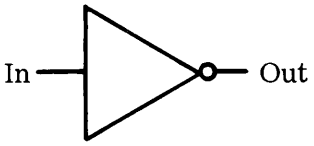
An amplifier may consist of one or more stages, does not necessarily have a gain of greater than unity, and may or may not accomplish inversion.



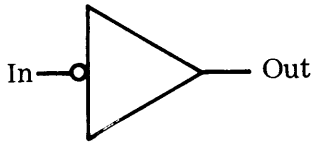
Amplifier Function—A high input gives a high output.



Amplifier Function—A low input gives a low output.

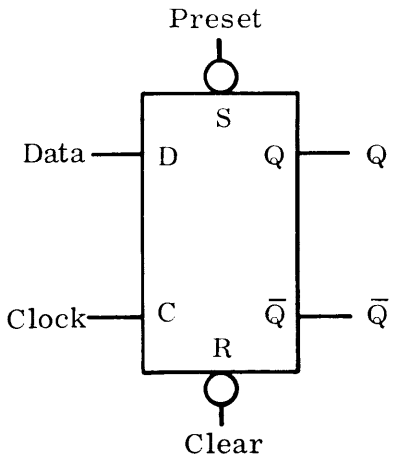


Inverter Function—A high input gives a low output.



Inverter Function—A low input gives a high output.

Flip-Flops

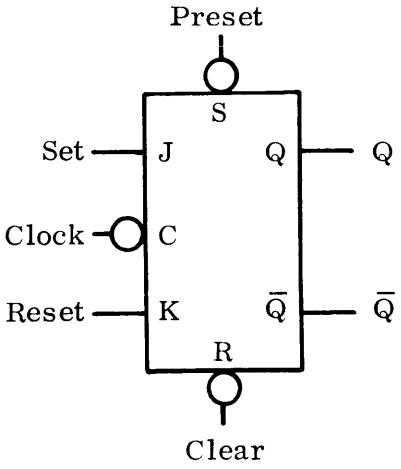


D-Type Edge-Triggered Flip-Flop

If D, S, and R are high, Q will go high on the leading edge of a clock pulse.

If D is low, S and R are high, $\overline{Q}$ will go high on the leading edge of a clock pulse.

Preset and Clear are independent of D and C inputs.



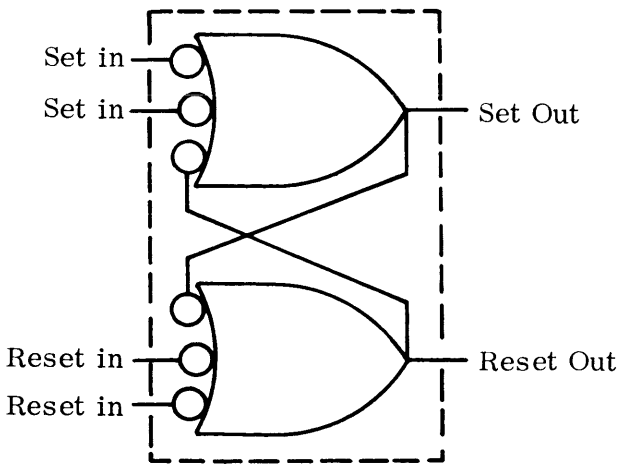
J-K Flip-Flop

If J, S, and R are high, and K is low, Q will go high on the trailing edge of a clock pulse.

If K, S, and R are high, and J is low, $\overline{Q}$ will go high on the trailing edge of a clock pulse.

If J, K, S, and R are high, Q and $\overline{Q}$ will alternate high on the trailing edge of every clock pulse.

Preset and Clear are independent of clock.



Flip-Flop (Latch)

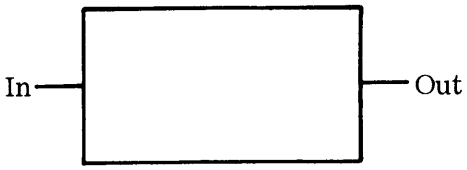
This device stores a single bit. It has two sets of Set and Reset inputs. It has two possible outputs: Set and Reset.

If any Set input is low and all Reset inputs are high, Set out will be high.

If any Reset input is low and all Set inputs are high, Reset out will be high.

If all inputs are high (Set and Reset), the latch will maintain its last state.

General Logic Symbol



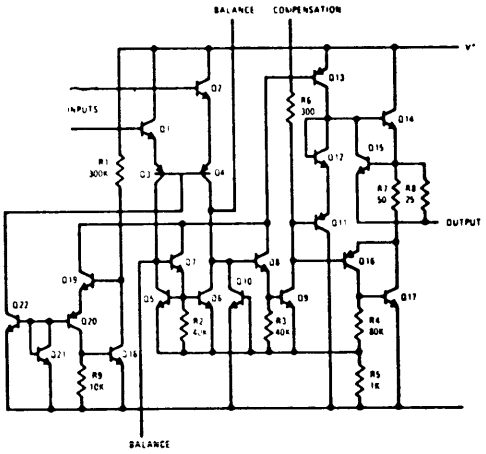
General logic symbols for other functions are represented by a rectangle. The symbol is labeled to define the function performed.

IC COMPONENTS

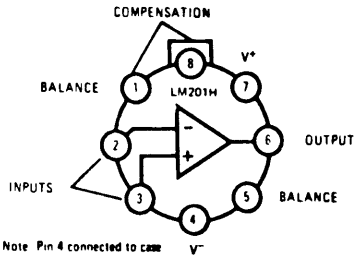
Integrated circuit (IC) components used in the drive are defined on the following pages.

LM Logic

LM201, LM201A and LM301A

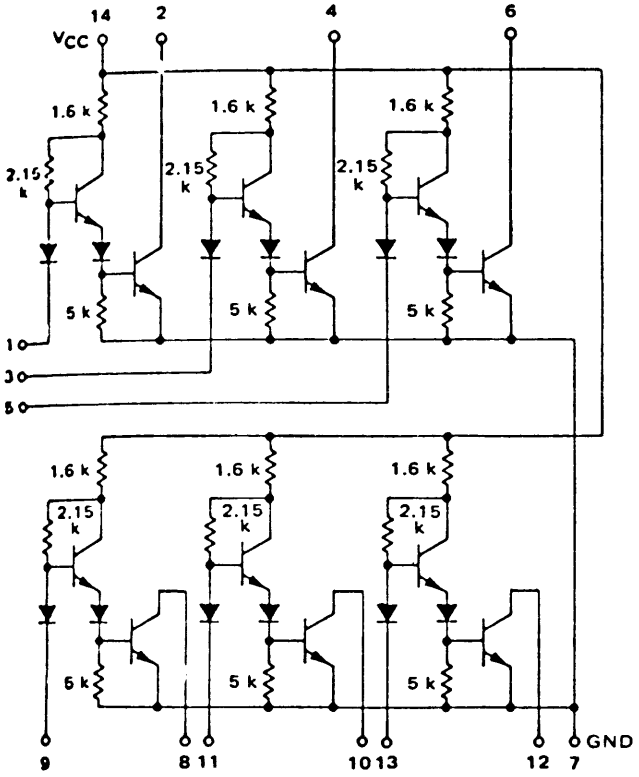


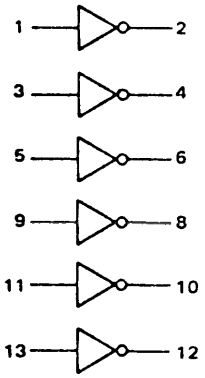
Metal Can



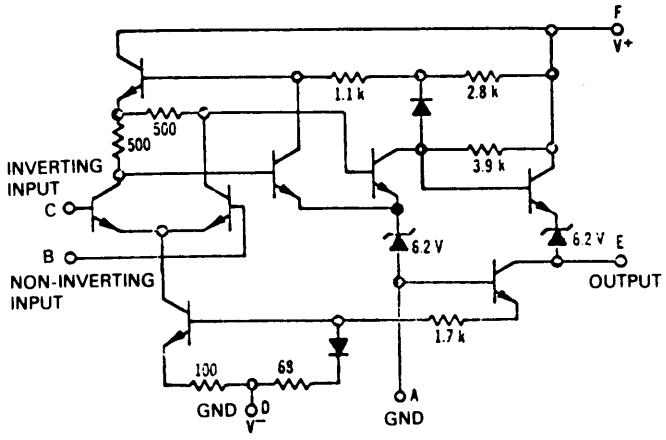
MC Logic

MC 835P

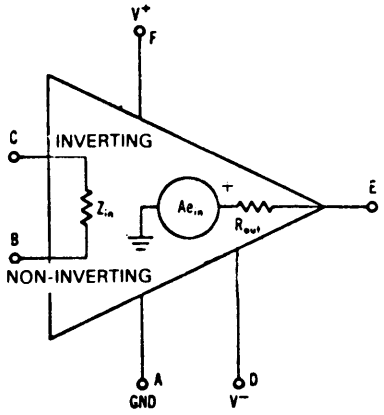




MC 1710CP



CIRCUIT SCHEMATIC



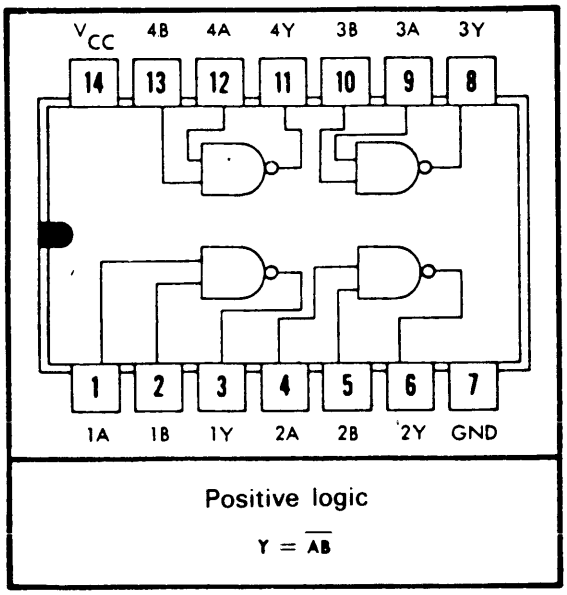
EQUIVALENT CIRCUIT

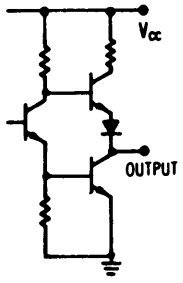
PIN CONNECTIONS

Schematic	A	B	C	D	E	F
P package	2	3	4	6	9	11

7400 Series Logic

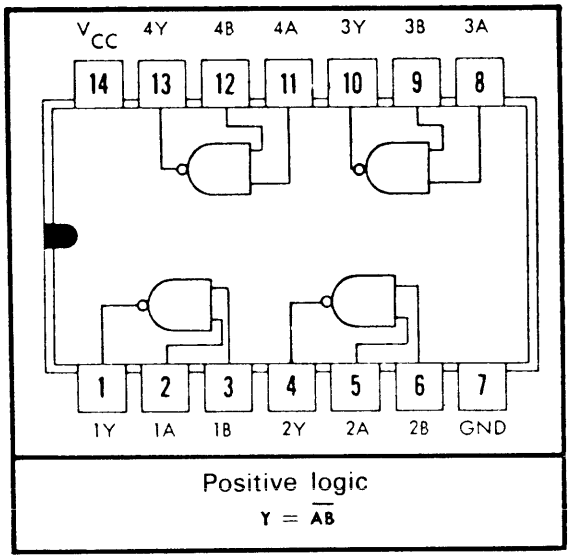
SN7400N and SN47L00
QUADRUPLE 2-INPUT POSITIVE NAND GATE





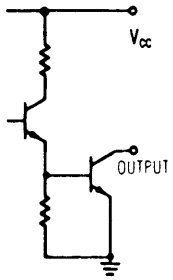
output circuit

SN7401N
QUADRUPLE 2-INPUT POSITIVE NAND GATE
(WITH OPEN-COLLECTOR OUTPUT)



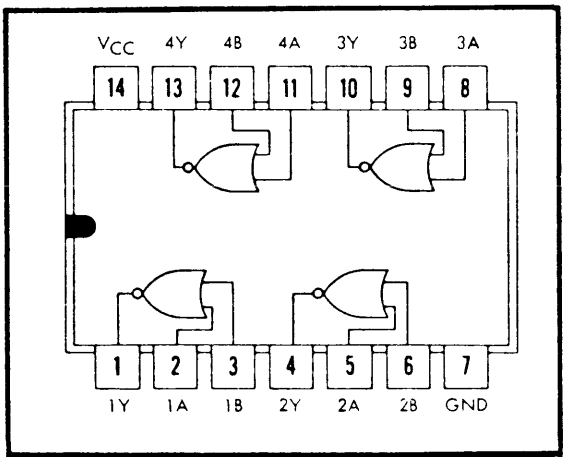
Positive logic

$Y = \overline{AB}$



output circuit

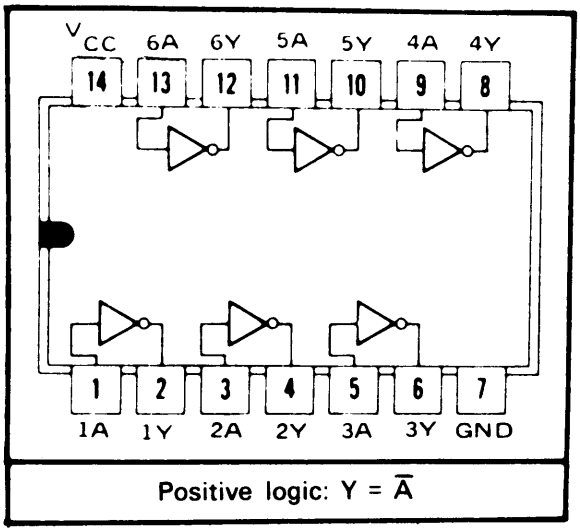
SN7402N
QUADRUPLE 2-INPUT POSITIVE NOR GATE



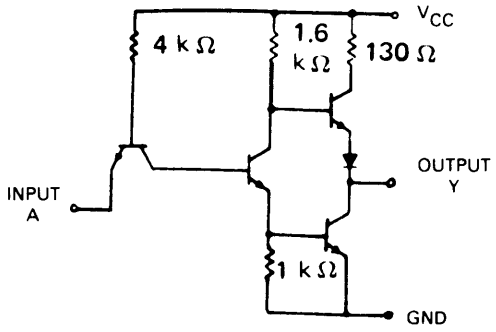
Positive Logic

$Y = \overline{A + B}$

SN7404
HEX INVERTER

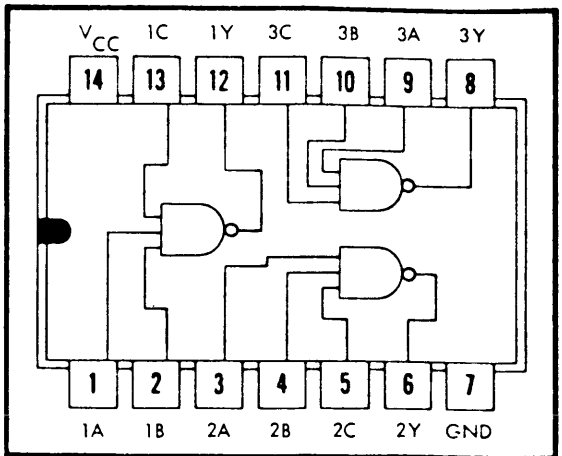


Positive logic: $Y = \overline{A}$



Schematic (each inverter)

SN7410N
TRIPLE 3-INPUT POSITIVE NAND GATE

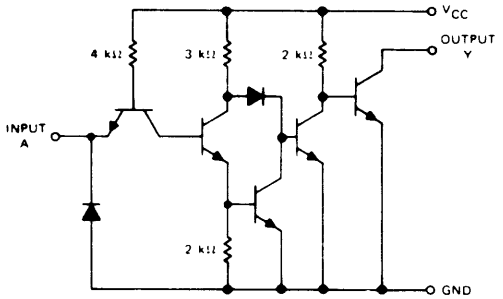


Positive logic

$Y = \overline{ABC}$

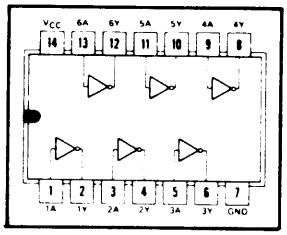
SN7416
HEX INVERTER

Schematic (each inverter)



NOTE: Component values shown are nominal.

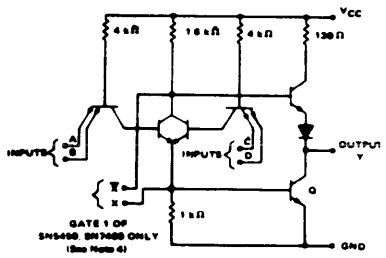
J OR N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



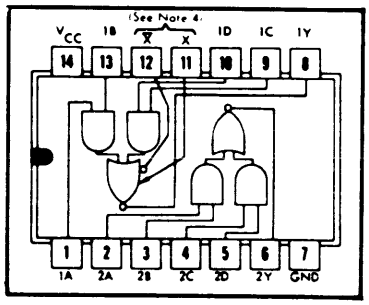
Positive logic $Y = \overline{A}$

SN7451
DUAL 2-INPUT, 2-WIDE AND-OR-INERT GATES

Schematic (each gate)

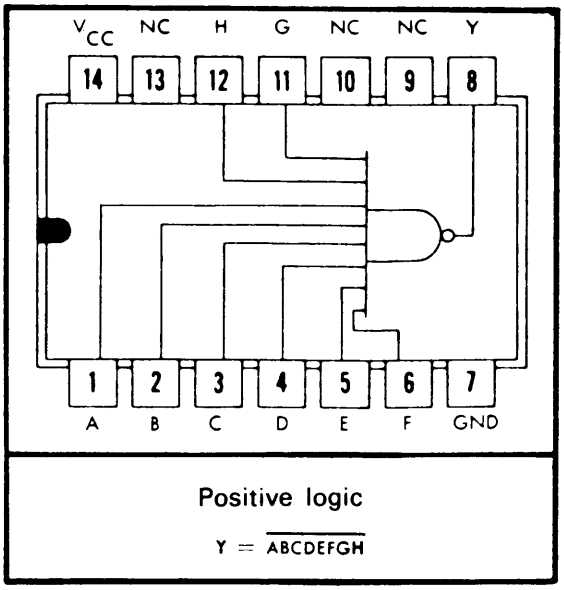


J OR N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



Positive logic: $Y = \overline{(AB) + (CD) + (X)}$
X = Output of SN5460/SN7460

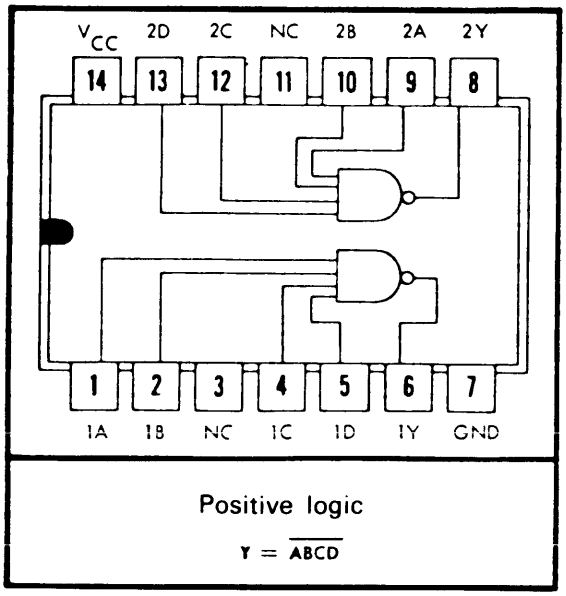
SN7430N
8-INPUT POSITIVE NAND GATE



Positive logic

$Y = \overline{ABCDEFGH}$

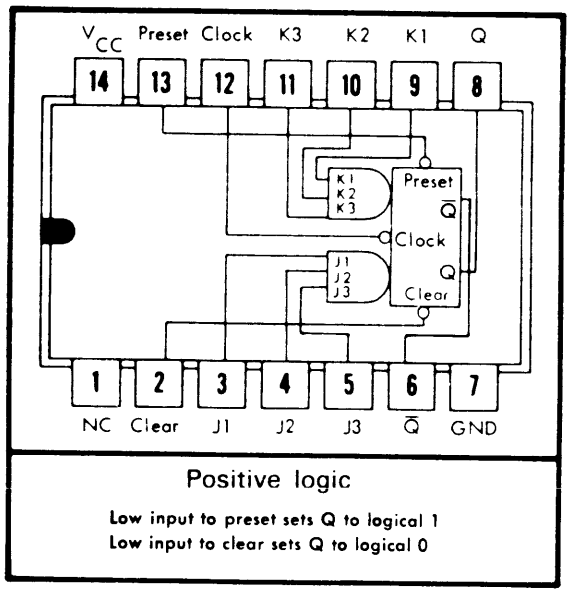
SN7440N
DUAL 4-INPUT POSITIVE NAND BUFFER



Positive logic

$Y = \overline{ABCD}$

SN7472N
J-K MASTER-SLAVE FLIP-FLOP



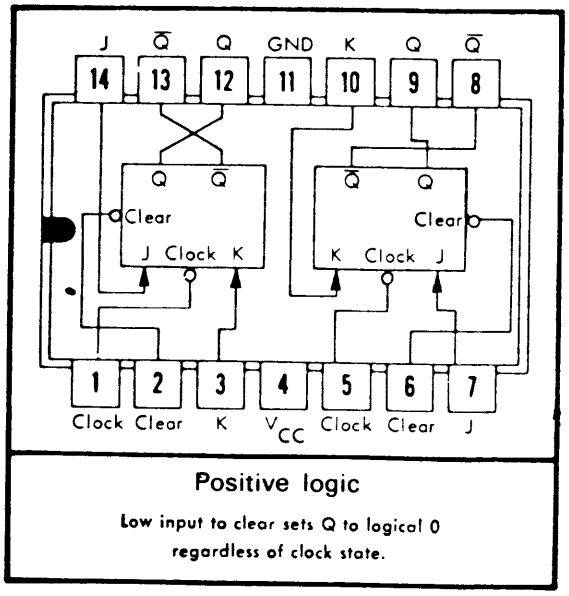
Positive logic

Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0

TRUTH TABLE		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES: 1. J = J1 • J2 • J3
2. K = K1 • K2 • K3
3. t_n = bit time before clock pulse.
4. t_{n+1} = bit time after clock pulse.

SN7473N
DUAL J-K MASTER-SLAVE FLIP-FLOP



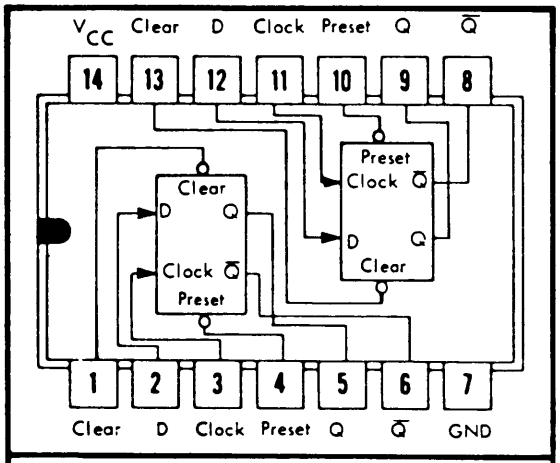
Positive logic

Low input to clear sets Q to logical 0
regardless of clock state.

TRUTH TABLE (Each Flip-Flop)		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES: 1. t_n = bit time before clock pulse.
2. t_{n+1} = bit time after clock pulse.

SN7474N
DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOP



Positive logic

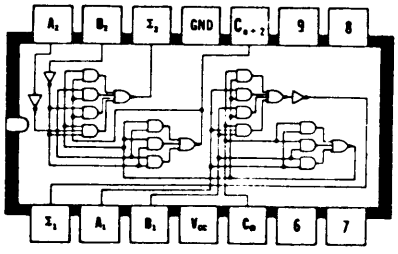
a. Low input to clear sets Q to logical 0.
b. Low input to preset sets Q to logical 1.
c. Clear or preset inputs dominate regardless of clock and D inputs

TRUTH TABLE (Each Flip-Flop)

t_n	t_{n+1}	
INPUT D	OUTPUT Q	OUTPUT $\overline{Q}$
0	0	1
1	1	0

NOTES: 1. t_n = bit time before clock pulse.
2. t_{n+1} = bit time after clock pulse.

SN5482N/SN7482N
2-bit Binary Full-adder



Add delay — 40 nsec per bit
Carry delay — 8 nsec per bit
Power dissipation — 195 mW

APPENDIX B
LOGIC DESCRIPTIONS

This appendix contains logic descriptions for the logic diagrams contained in Volume B of this publication.

EC LEVEL VARIANCES

The logic diagrams manual contains diagrams that reflect the equipment at various EC levels. Where differences in EC levels are minor, certain paragraphs within a description may be marked as applicable to a particular EC level only. Where differences in EC levels are significant, more than one logic description is provided to assure clarity. In other cases, a single logic description applies to all configurations.

To be certain to select the proper description for a particular version of an assembly:

1. Check the EC level of the PC board.
2. Locate the diagram(s) in the manual applicable to the board design level.
3. Locate and read the proper description while referring to the logic diagram.

PAGINATION

Pagination within this appendix is such that all logic descriptions are paginated after the logic board described, in sequence. For example, the Transducer Amplifier board (B06) description is paginated B06-1, B06-2, etc. The only exception to this pagination system is the last description in the appendix, which covers all power supplies, including boards C02 and C03.

LAMP DRIVERS (A02)

Since all lamp drivers on board A02 are basically the same, only one circuit is described; the lamp driver for the FILE UNSAFE lamps on the operator control panel.

When the signal +File Unsafe (entering the board on pin Y) is low, the ground return path for lamps DS13 and DS14 is open. When a file unsafe condition occurs in a drive (see Control Safety board B07 logic description), the signal +File Unsafe goes high. This signal is inverted and enables a NOR gate. The output of the NOR gate goes high, causing the output of the lamp driver to go low, completing the ground return path for the two lamps. Since the lamps are connected to +24 volts, completing the ground path lights the lamps.

A lamp test feature is also incorporated into the board. When the signal -Lamp Test (entering the board on pin 9) goes low, it is applied directly as the second input to all NOR gates in each of the lamp driver circuits, and thus enables all NOR gates. The high outputs of all NOR gates cause the outputs of their associated lamp drivers to go low, completing the ground return paths for all lamps, which light if they are operable.

SERVO SEQUENCER (A03)

The purpose of the Servo Sequencer logic board (A03) is to provide a set of signals to the Servo Sequencer Decode logic to initiate required operations, such as a forward seek, reverse seek, restore, or to reset the CAR, PAR, or the timers. Refer to the Servo Sequencer Decode board (A04) description for a complete list of the conditions and operations initiated by Servo Sequencer Decode logic.

The control state signals are generated by four J-K flip-flops which comprise the state counter. In addition, a -Clear Signal, which also serves as the direct reset input to the four flip-flops, goes to the On-Line and Attention latches on board A04. The two conditions (set or reset) possible for each of the four J-K flip-flops provide 16 possible states that the system may assume. These 16 states are shown in the Servo Sequencer State diagram 201162 and 201839.

Each circle in the state diagram represents one unique state and the four digits within each circle define the conditions of the four J-K flip-flops. From left to right, the digits A, B, C, and D refer to flip-flops C3A, C3B, B3A, and B3B, respectively. These flip-flops will be called A, B, C, and D throughout this description. A logical 1 in the circle indicates that the corresponding flip-flop is set and a logical 0 means that it is reset. The list of callouts next to each circle represents the operation to be performed while the Servo Sequencer logic is in the given state. These output conditions are decoded by the Servo Sequencer Decode logic board (A04).

Transitions, or changes from state to state are represented by arrows on the state diagram. Callouts on each arrow indicate conditions that must be met to allow that specific transition. A closed loop (i.e., an arrow which begins and ends at the same state) indicates conditions which, when they are met, will cause the system to remain in that state. A set of Boolean equations which summarize the prerequisites for each flip-flop's set and reset state is given at the end of this description.

All transitions, except those involving Seek Incomplete (T1 on state diagram) require that only one flip-flop change state. This means that for each change-of-state arrow in the state diagram, there is a single gate on the Servo Sequencer logic board that will cause the particular flip-flop to change its state. For example, the transition from state 0001 to state 0101 occurs after the Forward Seek delay (T2) times out. This transition requires that flip-flop B be set by a one on its J input. This logical function is fulfilled by NAND gate B1B and NOR gate C1C.

Transfer of the flip-flops from one state to another is synchronized by the trailing edge of the -Strobe B (clock) pulse, which is inverted by D3B. The pulse is generated by the cylinder transducer oscillator and enters the board on pin 14. In the following description, it is assumed that the transfer in states does not occur until the next strobe pulse.

First Seek and Restore

During the 60-second warm-up delay (T5 signal), -Seek Enable, which enters the board on pin 21 as a high level, is inverted by D5D, NORed by D2D, and inverted again by D3A to reset all four J-K flip-flops through their direct reset inputs. This low level leaves the card on pin 13 as the -Clear signal, which resets the Attention and On-Line latches on the Servo Sequencer Decode logic board. In this state (0000), the CAR, PAR, and timers are reset. When T5 times out, -Seek Enable goes low, which enables the Servo Sequencer logic. This initiates a restore sequence. This means First Seek and Restore are identical once the Servo Sequencer logic is enabled.

On the next strobe, flip-flop D is set by the output of NAND gate B2A and NOR gate B2C, which are enabled because flip-flops A, B, and C are reset. The logic is now at state 0001, where the CAR and PAR are still reset but the timers are now enabled. The Seek Start and Restore flip-flops on board A04 are reset to prevent a new Seek Start or Restore signal from entering the logic. The logic remains at state 0001 until +T2 (the Forward Seek delay) times out. When +T2 (which enters the board on pin 11) goes high, NAND gate B1B is enabled and its output is NORed by C1B. This sets flip-flop B, bringing the logic to state 0101. This state results in the generation of the signal -Force Forward Slow, which goes to the Adder and Speed Decode board. The logic will remain in this state until Forward Velocity is detected, at which time flip-flop D will be reset on the trailing edge of the next strobe pulse, via NAND gate B5B and NOR gate A5B, resulting in state 0100.

When motion in the carriage is detected, the signal +FWD VELOCITY at pin 18 goes high, setting forward flip-flop D4B. Since +FWD VELOCITY may go true momentarily (due to noise induced into the tachometer by the initial current surge into the linear motor), diode CR1 prevents the setting of flip-flop D4B while the heads are retracted.

When D4B is set, NAND gate C5B and NOR gate D5B set flip-flop C. The logic is now at state 0110 and forward motion is being monitored. The CAR and PAR are no longer held reset. The logic will continue in this state until the carriage comes to rest against the forward stop. When forward motion is no longer detected, NAND gate A1B and NOR gate B2C set flip-flop B so that the logic is at state 0111. Holding current is applied to the linear motor to hold the carriage firmly against the forward stop while a force count of 202 is entered into the PAR through the direct set inputs. The Forward Seek delay (T2) begins, and when it times out, NAND gate B2B and NOR gate D2B set flip-flop C3A. This causes the logic to move to state 1111.

This is the normal reverse seek state. Since CAR was cleared until state 0110 and PAR was preset to 202 in state 0111, a normal reverse seek to cylinder 000 is initiated. The Seek Start and the Restore flip-flops on board A04 remain reset.

Reverse Seek

If T1 times out before the counter logic counts 202 cylinders, causing the adder to declare a compare condition, NAND gates A4A and D5C and NOR gates A3B and A5B will reset flip-flops B, C, and D (this is one of the two transitions which involves a change in state to more than one flip-flop). Resetting flip-flops B, C, and D would put the logic into the seek incomplete (1000) state. If, however, a Compare condition is reached before T1, the logic transfers to state 1101 because NAND gate A4B and NOR gate A3B reset flip-flop C. The Seek Start and the Restore flip-flops on board A04 are still reset.

Detent

In addition, the Servo Sequencer Decode logic sends a +Detent signal to the detent actuator, allowing the detent pawls to begin dropping, and a -FWD Detent Velocity signal to the servo drivers on board B04. It is still possile for T1 to time out and, if it does so while the logic is in state 1101, the logic will transfer to state 1000 (this is the second transition involving more than one flip-flop). During normal operation, the -FWD Detent Velocity signal will cause the servo to reverse the polarity of the motor current and the carriage to reverse its direction of travel. Forward motion sensing logic will then detect the forward movement of the carriage, causing the logic to transfer to state 1100. This occurs when NAND gate B5C and NOR gate A5B reset flip-flop D. No change in external conditions takes place at this time. The logic is waiting for one of two events to occur, which will determine which state the logic moves to next. If T1 times out before zero velocity (lack of forward motion) is detected, the logic will go to state 1000, the Seek Incomplete state. If the detent pawl engages the rack and stops the carriage before T1 times out, zero velocity is detected and the logic transfers to state 1110. NAND gate C5A and NOR gate D5B set flip-flop C. In this state, the detent is in, the timers are reset, holding current is applied to the linear motor, and the Seek Start and Restore flip-flops on board A04 are held reset. On the trailing edge of the next strobe, the logic moves to state 1010. NAND gate C4C and NOR gate C4B reset flip-flop B. The detent is in and holding current keeps the carriage steady. The Ready delay, (T4) starts. When it times out, NAND gate D1A and NOR gate D2B reset flip-flop A, resulting in state 0010.

Ready

This is the ready state. The logic returns to this state after successful completion of any servo positioning operation. The Servo Sequencer Decode logic sends a +Seek Ready signal to the controller and the timers are reset. Since the Seek Start and the Restore flip-flops on board A04 are not held reset in this state, either one can be set by the controller, taking the logic out of the ready state. A +Restore signal will reset flip-flop C through NAND gate A4C and NOR gate A3B. This transfers the system to state 0000, the first state of the Restore sequence described above.

Seek Start

A +Seek Start signal will enable NAND gate A1B and NOR gate B2C, setting flip-flop D. This will transfer the logic to state 0011. In this state, the logic is ready for a seek operation. When the cylinder address is set into the CAR (prior to starting a seek), the -Compare line indicates whether the address set into CAR is different from the present location of the carriage as stored in PAR. If -Compare is low, the system is seeking the cylinder at which it is presently located. This causes the sequencer to return to the ready state (0010) through NAND gate B5A and NOR gate A5B resetting flip-flop D. If, on the other hand, -Compare is high, a seek is required and NAND gate A3A and NOR gate D2C set flip-flop A, bringing the logic to state 1011. The delay timers (T1 through T4) are now running. If the +Carry line is high at this time, it will enable NAND gate C1A and NOR gate C1B, which will set flip-flop B. This will cause the logic to transfer to the reverse state 1111, initiating a reverse seek. The sequence of states following state 1111 is described above.

Forward Seek

The carriage is still positioned at cylinder 000; however, the +Carry line is probably low, indicating a forward seek. In this case, the logic will wait until T2 times out. At this point, NAND gate A5A resets flip-flop C, resulting in state 1001. A forward seek to the address in the CAR is initiated. From this state, the logic can either continue on through the normal seek sequence by transferring to the detent state (1101) when a compare condition is reached or it can transfer to the seek incomplete state (1000) if T1 times out first. The sequence of states following state 1101 is described above.

Seek Incomplete

If the Seek Incomplete delay (T1) times out in states 1001, 1100, 1101, 1111, or 0101 it would cause a transfer to the seek incomplete state (1000) as described above. In this state the timers are reset and a +Seek Incomplete signal is sent to the controller. The Servo Sequencer Decode logic removes all its outputs to the servo and disables the servo driver. The Servo Sequencer logic awaits initiation of a Selected Unit Restore signal by the controller. A -Restore signal, inverted by D2A, enables NAND gate D1B and NOR gate D2B and allows the system to transfer to state 0000, which is the first state of the restore sequence described above.

SUMMARY OF PREREQUISITES FOR
FLIP-FLOPS' SET AND RESET STATES

$J_A = (\overline{B} \cdot C \cdot D \cdot \overline{\text{COMPARE}}) + (C \cdot D \cdot T2)$

$K_A = (\overline{B} \cdot C \cdot \overline{D} \cdot T4) + (\overline{B} \cdot \overline{C} \cdot \overline{D} \cdot \text{RESTORE})$

$J_B = (A \cdot D \cdot \text{CARRY}) + (A \cdot D \cdot \text{COMPARE} \cdot \overline{\text{T1FF}}) + (\overline{A} \cdot \overline{C} \cdot D \cdot T2)$

$K_B = (A \cdot D \cdot \text{T1FF}) + (A \cdot \text{T1FF} \cdot \text{FWD FF}) + (A \cdot C \cdot \overline{D})$

$J_C = (A \cdot B \cdot \overline{D} \cdot \overline{\text{FWD FF}}) + (\overline{A} \cdot B \cdot \overline{D} \cdot \text{FWD FF})$

$K_C = (A \cdot D \cdot \text{T1FF}) + (A \cdot D \cdot \text{COMPARE}) + (A \cdot \overline{B} \cdot D \cdot T2) + (\overline{A} \cdot \overline{B} \cdot \text{RESTORE})$

$J_D = (\overline{A} \cdot \overline{B} \cdot \text{SEEK START} \cdot \overline{\text{RESTORE}}) + (\overline{A} \cdot \overline{B} \cdot \overline{C}) + (\overline{A} \cdot B \cdot C \cdot \overline{\text{FWD FF}})$

$K_D = (\overline{B} \cdot C \cdot \text{COMPARE}) + (A \cdot \text{T1FF}) + (\overline{A} \cdot B \cdot \overline{C}) + (B \cdot \overline{C} \cdot \text{FWD FF})$

SERVO SEQUENCER DECODE (A04)

The Servo Sequencer Decode board (A04) decodes the four output signals of the Servo Sequencer logic into signals to be used by various logic systems in the drive. Some decoded signals are also sent to the controller as status lines.

The four Servo Sequencer signals (-A, -B, -C, and -D), which originate at the $\overline{Q}$ outputs of the four J-K flip-flops of A03, enter board A04 at pins 4, 5, 8, and 9, respectively. These signals are inverted by D1A, D1D, D2A, and D2D. The outputs of the inverters are sent to the decode logic both directly and through inverters D1B, D1C, D2B, and D2C. This means both inverted and non-inverted versions of the input signals are used for decoding. The eight outputs of the eight inverters are labeled +A, +B, +C, +D, -A, -B, -C, and -D, respectively. These outputs go in various combinations to a set of positive NAND gates and to one positive NOR gate, which comprise the decode logic. Some gates use only two of the signals as inputs, while others use three or four. Two multiple input gates also use the $\overline{Q}$ outputs of the Seek Start flip-flop (D3B) and the Restore flip-flop (D3A). These flip-flops store the controller commands Seek or Restore during execution. When the signal -Selected Unit Control goes low, both of these flip-flops are reset. When the necessary combination of inverter outputs are high, a particular gate(s) will be enabled. The outputs of the enabled gates go to other logic in the drive and or the controller. For example, if the input lines to inverters D1A and D2A are both high, while the inputs to inverters D1D and D2D are low, the eight inverter outputs will be in these states: -A, +B, -C, and +D are high and +A, -B, +C, and -D are low. This combination of levels will enable NOR gate D4A and NAND gate A2B. The output of D4A resets the Seek Start and Restore flip-flops and prevents setting of the Attention latch. A2B generates the signal -Force Forward Slow. Other outputs from the Servo Sequencer Decode board include:

-Holding Current
When this line is low, holding current is applied to the positioning motor, keeping a light force on the carriage in the forward direction against the engaged detent pawl.

-FWD Detent Velocity
This line goes to the operational amplifiers in the servo to select the proper current value for the positioning motor to move the carriage forward at the proper detent velocity.

-Seek Forward
This line goes to the Adder and Speed Decode logic to enable the forward direction adder gates.

+Seek Forward
This line goes to the PAR to enable the counter to count up during a forward seek.

-Seek Reverse
This line goes to the PAR to enable the counter to count down during a reverse seek.

+Seek Reverse
This line goes to the Adder and Speed Decode logic to enable the reverse direction adder gates.

-Force Forward Slow
This line goes to the Adder and Speed Decode logic to simulate an address difference of 4 and select the corresponding forward velocity.

-Force Count
This line goes to the direct set inputs of the PAR flip-flops to force a present address of 202 into the Control Safety logic, which generates a signal that resets the head register and is applied to the Cylinder Transducer Amplifier board to prevent the cylinder transducer from generating count pulses.

+Seek Ready
This line goes to the Control Safety logic and is used to partially enable the gate that generates -Selected Set Cylinder signal. It also goes to the controller as a status line.

+Seek incomplete
This line goes to the Index/Sector logic to turn off the READY lamp driver and to disable the servo. It also goes to the controller as a status line.

+Seek Start
This line goes to the Servo Sequencer logic as one of the condition lines that change the states of the four state flip-flops.

-Restore
This line goes to the Servo Sequencer logic as one of the condition lines that change the states of the four state flip-flops.

+On Line
This line goes to the controller as a status line.

+Attention
This line goes to the controller as a status line.

Not all the outputs of the Servo Sequencer Decode board are conditioned by the eight inverter outputs. The two D-type flip-flops discussed earlier are responsible for the signals +Seek Start and -Restore. The signal +Seek Start is generated at the Q output of flip-flop D3B when it is set by +Unit Bus 2 going high during the control cycle (Unit Bus 2 is +Seek Start during the control cycle). The signal -Restore is generated at the $\overline{Q}$ output of flip-flop D3A when it is set by +Unit Bus 6 going high during the control cycle. Flip-flops D3B and D3A are clocked by an inverted -Selected Unit Control signal.

The On-Line latch (C5B/C5A) is held reset by the signal -Clear until the 60-second warm-up delay times out. During this period, the signal +On Line is low, indicating to the controller that the disc drive is not on line. The On-Line latch is also held reset if the signal +Enable latch is low (ENABLE-DISABLE switch in the DISABLE position). The signal +On Line goes high when the On-Line latch is set. This occurs when the output of NAND gate C3A goes low (in the READY state with Seek Start false). A high +On Line informs the controller that the drive is on line.

The Attention latch (D5B/D5A) is also held reset by the signal -Clear until the 60-second warm-up delay times out. The signal -Reset Attention, initiated by the controller, can also reset the Attention latch. When signals +D or +B satisfy NOR gate D4A, flip-flops D3B and D3A are reset and the Attention latch is set. However, the signal +Attention is not gated to the controller because NAND gate B5A is disabled. NAND gate B5A is enabled when NAND gate C3A is satisfied upon entering the READY state (0010).

ADDER AND SPEED DECODE (A05)

The principal function of the Adder and Speed Decode card is to compute the difference between the contents of the Command Address Register (CAR) and the Present Address Register (PAR). If the contents are equal, a Compare signal is generated to be used by the Servo Sequencer (card A03). If the contents are different, speed decodes and access directions are generated and sent to the Servo Control (card B04).

The Difference Generator, together with the True/Complement Block, determine the CAR/PAR (track) difference and access direction of the servo (forward or reverse). The Difference Generator consists of two 4-bit binary full adders: 1D and 2D. The carry output of 1D is connected to the carry-in of 2D. Together these two adders can add numbers up to 8 bits. The True/Complement Block is made up of two 4-bit true/complement elements: 1C and 2C. The function of 1C and 2C is to convert the 4 binary inputs (A_n) to corresponding outputs (Y_n) in either true of complement form by the use of two control lines, B and C. Further, the control lines will also set all outputs to either a logical 0 or a logical 1, independent of the state of the data inputs. These four possible output states are tabulated below.

Truth Table of True/Complement Device

	Control Inputs		Outputs			
State	**B**	**C**	Y_1	Y_2	Y_3	Y_4
Complement	0	0	$\overline{A_1}$	$\overline{A_2}$	$\overline{A_3}$	$\overline{A_4}$
True	0	1	A_1	A_2	A_3	A_4
Logical 1	1	0	1	1	1	1
Logical 0	1	1	0	0	0	0

The access direction of the servo depends on the magnitude of the +PAR and -CAR signals. For example, for any seek length of less than 96 in the forward direction (-CAR greater than PAR), the complement of the difference count (-Difference) is generated by the Difference Generator. Because of the unipolar speed decoding logic in this card, the -Difference signals are decoded at the True/Complement Block output. These outputs must be in their true states (control lines B and C equal 01). The True/Complement Gating must therefore provide (-Carry) • (+Force Forward Slow) • (+ $\geq$ 96) to force the true state.

For seek lengths less than 96 tracks in the reverse direction, (PAR greater than -CAR), the true difference and +Carry are generated by the Difference Generator. The resulting True/Complement Block outputs are complemented to conform with the unipolar speed decode usage. This is accomplished by the logic equation (+Carry) • (+Force Forward Slow) • (+ $\geq$ 96).

For seeks greater than 96 tracks, forward or reverse, the Difference Bit Gating gates only the difference of 96 until this number is reached, and then gates actual track difference. Block 2C (CAR 128, 64, 32, and 1 lines) is in the true state for forward direction and in the complement state for reverse direction. Block 1C outputs are set to a logical 1 (control lines B and C equal 10). Block 2C is decoded as follows: -Difference Of 32 and -Difference Of 64 signals are extracted from -CAR 128, 64, and 32 lines, and the -Difference Of 1 line (2A, pins 8 and 11) is inhibited.

The Compare signal is generated whenever gate 2B inputs are all high (-CAR = PAR). The delay provided by R5 and C13 is to prevent transients from giving a false compare. Forward Compare gate 5D is enabled whenever 5C, pin 2 is high (not reverse). The Reverse Compare signal is delayed again for the duration of one-shot 5A (.08 msec). This is done by the trailing edge of the one-shot pulse, which sets flip-flop 4B. Due to the cylinder counting scheme, a -Difference Of 1 must also be forced for the duration of the one-shot to compensate for reverse turnaround to detent at the correct cylinder. As soon as +Reverse goes away, 4B is reset and ready.

There are two safety inhibit lines in this card: PAR ≥ 224 (Reverse Inhibit) and -CAR ≥ 203 (Forward Inhibit). Forward Inhibit becomes active (3C pin 6 low) whenever the CAR contents are greater than 202, by the following equation:

$$\text{Forward Inhibit} = \overline{128} \cdot \overline{64} \left[\overline{32} + \overline{16} + \overline{8} \cdot (\overline{4} + \overline{2} \cdot \overline{1})\right]$$

Instead of allowing the carriage to crash into the Crash Stop, the carriage remains in the previous position and waits for the Seek Incomplete status.

The Reverse Inhibit signal (3B, pin 6) becomes active whenever the PAR contents are less than zero, resulting in a huge number in PAR. This is caused by excessive servo gain, with the result that the carriage detents behind zero. To prevent the next seek from going up and onto the head unload cams at high speed, the Reverse Drive signal is inhibited and waits for a Seek Incomplete status.

Because the density of one-track seeks increases the average access time, velocity is forced 1 difference count beyond "compare" to achieve a faster one-track forward seek. This is accomplished by triggering One-Shot Timer 4A (1.8 msec) by -Forward Seek to force -Difference of 1 (3B, pin 12) and -Forward Drive (5B, pin 11) for the duration of the one-shot timer. For seeks greater than 1 track, the 1.8-msec interval is insignificant.

The Anticipate logic (on forward seeks only) controls the gain of the servo by switching an FET switch on and off in the shaper feedback path. In order to not overshoot the decelerating portion of the programmed velocity curve and to maintain its optimal time response capability, the servo anticipates (follows a lower gain path) to insure its ability to arrive at the detent velocity at the proper distance from the desired detent tooth. The logic is enabled after One-Shot Time 4A times out. Then, the +Drive Into Pack signal sets the +Anticipate signal to turn off Gain Switch Q26 on the B04 card when the servo has met the deceleration curve for the first time. This action decreases the servo gain on the concluding decelerating portion of the velocity curve. The Anticipate logic is never active in the reverse direction because flip-flop 4B is preset on reverse (-Seek Forward goes high).

The High Power Rate delay circuit is used to delay the time between seeks whenever the temperature of the bobbin has reached its upper limit. Bobbin temperatures above this limit will cause bobbin material fatigue and result in a machine failure. If the bobbin is below the critical temperature, +High Power Rate is low and +T4 goes through gates 5B, pin 3 and 5B, pin 8 to bypass the delay logic. If the bobbin has reached its critical temperature (too hot), +High Power Rate is high. It enables 5B, pin 4 and blocks the previous bypass path. Signal +T4 activates one-shot 4A to set latch 4C at the end of its timing pulse to extend +T4 to 28 msec. This allows the bobbin to cool for this length of time until the next seek.

CYLINDER/PRESENT ADDRESS REGISTER (A06)

The CAR receives the cylinder address from the controller and stores it for comparison by the Adder and Speed Decode board.

The PAR counts the pulses from the cylinder transducer amplifier and gives an electrical indication of the present head position to the Adder and Speed Decode board and to the present address indicator lamps on the operator control panel. If these register outputs are not identical, the servo in the drive moves the heads until the pulses received from the cylinder transducer amplifier change the present address to equal the cylinder address.

Cylinder Address Register

The CAR consists of eight D-type flip-flops: A5B, B5B, C5B, C5A, B5A, A5A, C4B, and C4A. It receives its input instructions at the set inputs of the flip-flops directly from the controller via Unit Bus lines 0, 1, 2, 3, 4, 5, 6, and 7 when the signal -Selected Set Cylinder goes low. The set outputs go back to the controller through line drivers for confirmation that the proper address was received. The reset outputs are routed to the Adder and Speed Decode board. Bit 128 is also inverted and set to the Write logic board.

Present Address Register/Counter

The PAR consists of an eight-bit register using eight D-type flip-flops: A3B, A3A, A2A, A2B, B2A, B2B, C2A, and C2B. The inputs of the flip-flops are from adder circuits A1A, A1B, B1A, B1B, C1A, C1B, D1A, and D1B, respectively. The register/adder can either add to or subtract from the register's present contents when the input -Cyl Count goes low. The counter counts up or down depending on whether the signal +Seek Forward or -Seek Reverse is active.

In preparation for the reverse portion of a Restore operation, the PAR is direct set to a count of 202. To do this, the PAR is first reset. Since the direct set inputs of the 1-, 4-, 16-, and 32-bit register flip-flops (A3B, A2A, B2A, and B2B) are tied to +5 volts via R1, the signals +PAR 1, +PAR 4, +PAR 16, and +PAR 32 are low. The low signal -Force Count causes the remaining PAR signals to be high, resulting in a weighted value of 202.

Up-Count Operation (Present Address Register)

Assuming all the D flip-flops in the PAR are reset (cylinder 000) and the signal +Seek Forward is active, the only flip-flop with a high input is A3B. This comes from the output of the bit-1 adder (A1A). On the first -Cyl Count pulse from the cylinder transducer amplifier, flip-flop 1 sets and the signal +PAR 1 is generated.

Once flip-flop 1 is set, its D input goes low because the two high inputs to A1A reset it, causing its Σ output to go low. At the same time the carry out of adder 1 goes high. Adder 2 now has one high input which in turn causes the D input of flip-flop 2 to go high. At this point, the D input of flip-flop 1 is low and the D input of flip-flop 2 is high. The next -Cyl Count pulse clears flip-flop 1 and sets flip-flop 2, generating the signal +PAR 2.

When flip-flop 1 is reset, its D input went high and the D input of flip-flop 2 remained high. The next -Cyl Count pulse sets flip-flop 1. Flip-flop 2 remains set because of its high D input. The signals +PAR 1 and +PAR 2 are thus generated, giving a weighted value of three. The next -Cyl Count pulse resets both flip-flops 1 and 2 and sets flip-flop 4. This generates the signal +PAR 4. The sequence continues until the cylinder transducer amplifier ceases generating cylinder count pulses.

Down-Count Operation (Present Address Register)

In the following description, it is assumed that flip-flop 4 is set so that the register is generating the signal +PAR 4. To count down, the -Seek Reverse signal must be active. This signal is inverted and applied to the B inputs of all the adders. At this point, flip-flop 4 is set, the D inputs of flip-flops 1 and 2 are high, and the D input of flip-flop 4 is low. The first -Cyl Count pulse sets flip-flops 1 and 2 and resets flip-flop 4, resulting in a +PAR 2 and a +PAR 1, giving a weighted value of three. When this happens, the D input of flip-flop 1 goes low, the D input of flip-flop 2 remains high, and the D input of flip-flop 4 remains low. The next -Cyl Count pulse resets flip-flop 1 and flip-flop 2 remains set, generating the signal +PAR 2.

This causes the D input of flip-flop 1 to go high and the D input of flip-flop 2 to go low. The D input of flip-flop 4 remains low. Another -Cyl Count pulse sets flip-flop 1. Flip-flops 2 and 4 remain reset. The resulting output is the signal +PAR 1.

At this point, the D input of flip-flop 1 goes low and the D inputs of flip-flops 2 and 4 remain low. Another -Cyl Count pulse resets flip-flop 1 while the other flip-flops remain reset for a count output of zero.

HEAD SELECTION AND REGISTER (A07)

The Head Selection and Register logic receives the head address information from the controller and stores it in the head register. The output of the head register is decoded into a Line Select signal which activates the desired read/write head to either read or write. This logic is also used to generate the safety signals -Head Select Error and +End of Cyl.

The clock inputs for all the flip-flops in the head register, except the bit-1 flip-flop, come from the reset output of the next lower bit flip-flop. That is, the reset output of the bit-1 flip-flop clocks the bit 2 flip-flop and so on up to the bit-16 flip-flop. Bit-1 flip-flop is clocked by the signal, +Selected Head Advance. When this line goes high, the head register contents are increased by one. The reset output of each flip-flop is also tied back to its own D input. The reason for this is discussed in the HEAD ADVANCE section.

The set and reset outputs of each flip-flop (except bit 1) go to a pair of negative NAND gates. These gates are also conditioned by the output of the positive NAND gate B2A. B2A will enable those gates only if the +Select Head line is high. If this condition is met, the set and reset outputs of the four flip-flops are gated to the -Line Select gates.

There are ten -Line Select lines, each one gated by a four-input positive NAND gate. The inputs to the ten gates consist of various combinations of the inverted set and reset outputs of the head register flip-flops (excluding bit 1). Depending on which flip-flops are set by the +Unit Bus and +Selected Set Head lines, one of the 10 -Line Select lines will be selected.

Each -Line Select line is capable of partially enabling two read/write heads. One of each pair of heads is gated by a set of read, write, and erase gates called -Read LF (A1C), -Write LF (A1B), and -Erase LF (A1A). The other head in each pair is gated by a similar set of gates called -Read RT (B1D), -Write RT (B1A), and -Erase RT (B1B). This means that if -Line Select 5 is low while the outputs of A1B and A1A are low, the LF head on -Line Select 5 will write and erase.

The 20 heads are each selected by a combination of: one of the 10 Select lines and one or two of the LF (LEFT) or RT (RIGHT) lines (one line if the head must read and two lines if it must write and erase). This technique uses what is known as 2-by-10 matrix selection. The 20 heads are classified in two groups of 10: one group of 10 LF heads and one group of 10 RT heads.

The RT heads are selected with the three gates B1D, B1A, and B1B. The LF heads are selected with the three gates A1C, A1B, and A1A. These sets of gates determine whether the RT or LF heads read or write and erase. For instance, to accomplish reading on the RT heads, the signal -Read RT must be low (i.e., gate B1D must be enabled). For the RT heads to write and erase, the signals -Write RT and -Erase RT must be low (i.e., gates B1A and B1B must be enabled). Similar requirements apply to the LF heads.

Selection of the three RT gates instead of the three LF gates, or selection of the LF gates instead of the RT gates, depends on the relative states of the bit-1 and bit-2 flip-flops. If both flip-flops are in the same state (both set or both reset), either D2C or D2D will be enabled. In either case, a low output from one of the two gates enables OR gate D2A. The high out of D2A partially enables the set of RT gates. The inverted output of D2A

goes to the three LF gates and, in this case, disables them. If the states of the two flip-flops are different (bit 1 set and bit 2 reset or bit 1 reset and bit 2 set), both D2C and D2D are disabled. Since the outputs of both are high, D2A is also disabled. The low out of D2A disables the set of RT gates. The low is also inverted and partially enables the set of LF gates. In brief, the set of RT gates is partially enabled when the states of the bit-1 and bit-2 flip-flops are the same and the set of the LF gates is partially enabled when the states are different. The output of D2B also leaves the board on pin Y as +Left Select.

Selection of read or write and erase functions is the responsibility of the three input lines +Selected Read Gate, +Selected Write Gate, and +Selected Erase Gate. Each signal partially enables two gates, one in the set of RT gates and one in the set of LF gates. One of these two gates is enabled by either the output of D2A or D2B. Consequently if +Selected Read Gate is high while the output of D2A is high, B1D is enabled. Its low output leaves the board on pin E as -Read RT. It goes to the Read Amplifier board where it enables appropriate circuitry for RT operation.

It should be remembered that a write operation must always be accompanied by an erase operation. For example, when +Selected Read Gate is high, +Selected Write Gate and +Selected Erase Gate are both low. When +Selected Write Gate is high, +Selected Erase Gate must also be high and +Selected Read Gate is low.

HEAD ADVANCE

Because of controller operation, the head register operates as a 5-stage binary ripple counter when head advance is commanded. If none of the head register flip-flops is directly set by the +Unit Bus signals, the register will count each time a +Selected Head Advance pulse is applied to flip-flop A2A until the maximum head address is reached (10011 in binary or 19 in base 10).

During a head advance sequence, the Unit Bus lines entering A07 are all low. The direct set and direct reset inputs to all the flip-flops are high. This means each flip-flop is conditioned by its clock and D inputs. Assuming that, as the sequence begins, all five flip-flops are reset, the $\overline{Q}$ output of A2A is high. Since this output serves as the D input to its own flip-flop, A2A will set on the leading edge of the next clock pulse, +Selected Head Advance. When this happens, the $\overline{Q}$ out of A2A goes low, causing the D input to be low. This has no immediate effect on A2A; it prepares the flip-flop to be reset by the next clock pulse. Outputs of the bit-2 through bit-16 flip-flops are selecting -Line Select 0 at this point.

On the leading edge of the next clock pulse into A2A, that flip-flop will reset, causing its $\overline{Q}$ output to go high. This output again prepares A2A to go high on the next clock pulse, but it also serves as the clock pulse to the bit-2 flip-flop, B3A. Since the bit-2 flip-flop was in the reset state when the clock pulse arrived from A2A, it set on the leading edge of the pulse. Now the bit-2 flip-flop is set and the other bit flip-flops are decoded by the -Line Select 1 gate.

The next clock pulse into A2A will set that flip-flop. Again, this change has no immediate effect on the logic other than to prepare A2A to reset again, supplying another clock to the bit-2 flip-flop. When this happens (A2A resets), the clock pulse into B3A resets that flip-flop. The Q output of B3A goes high and serves as a clock pulse to the bit-4 flip-flop, B3B. B3B sets, creating a new set of inputs to the line select gates. With the bit-4 flip-flop set and the others reset, -Line Select 2 is selected. This sequence continues until -Line Select 9 is selected.

END OF CYL/HEAD SELECT ERROR

In addition to the Line Select signals, two safety signals are generated on this board. They are +End of Cyl and -Head Select Error. The signal +End of Cyl informs the controller when the drive has advanced to head address 20 or beyond and the signal -Head Select Error goes to the Control Safety logic if an unsafe (to the disc) condition exists within the logic or its programming.

When the head register has advanced to a numerical value which enables -Line Select 9, the high Q output of the bit-16 flip-flop partially enables AND gate A5C in addition to generating the signal -Sixteen. Other inputs to AND gate A5C are +Unit Selected and the output of NOR gate A4C which is active whenever the bit-4 or bit-8 register flip-flop is set.

The next clock pulse after -Line Select 9 has been activated sets flip-flop A2A. The following clock pulse resets flip-flop A2A causing flip-flop B3A to reset. This in turn causes flip-flop B3B to set, and its low $\overline{Q}$ output enables OR gate A4C. The high output of A4C enables gate A5C which enables gate A4A, generating the signal +End of Cyl.

Exceeding the legal head address and attempting to select a head is considered a head selection error. For that reason, the low out of A5C enables another OR gate A4D. If the +Selected Head line is high at this time, the high out of A4D enables AND gate A5B, generating the signal -Head Select Error.

The -Head Select Error signal is also generated when both -Erase LF and -Erase RT lines or both -Write LF and -Write RT lines are selected simultaneously. Either of these conditions will satisfy OR gate A4D which causes AND gate A5B to generate the signal -Head Select Error. Again, this assumes that the signal +Select Head is active. This signal -Head Select Error goes to the Control Safety logic to help generate a -File Unsafe signal.

POWER-UP SEQUENCING AND CONTROL (A08)

The Power-Up Sequencing and Control board (A08) prevents simultaneous starting of two or more drives in a multiple-drive configuration. Since the starting current of the spindle drive motor is much higher than the running current, simultaneous starting of more than one drive could result in a power overload. If a unit in a string of drives is disabled by switching, circuitry on A08 causes that drive to be bypassed. The Power-Up Sequencing and Control board provides a 60-second delay ater the spindle drive motor reaches operating speed to allow the disc pack temperature to stabilize before generating signals needed by the Control Safety, Servo Sequencer, and Index/Sector boards. Other signals generated by the Power-Up Sequencing and Control board are used by the Servo Sequence Decode and Adder/Speed Decode board. Signals are also generated for use by the Cylinder Transducer Amplifier and the controller. Finally, the Retract Heads signals and the 12-second dynamic braking signals originate on the Power-Up Sequencing and Control board.

Throughout the following description, these conditions are assumed to exist (unless noted otherwise).

1. The Door Closed-Door Open switch (S2) is in the Door Closed position, causing NAND gate C5A-1 to be high.

2. A disc pack is installed on the unit, closing the Pack-On switch (S4).

3. The main power switch (S1) on the interior control panel is on, providing the necessary DC voltages for logic and relay operation.

4. The Heads Extended-Heads Retracted switch (S3) is in the Heads Retracted position, causing NAND gate C5C-9 to go low and NAND gates A4C-9 and B4A-1 to go high. The Heads Retracted position of S3 also causes NOR gate A4B-6 to go high, enabling it, which partially enables NAND gate A4A-3.

5. The START-STOP switch (S7) on the operator control panel is in the START position, causing NAND gate C5A-13 and NOR gate C4A-1 to go high and NAND gate B4A-2 to go low.

6. The ENABLE-DISABLE switch is in the ENABLE position, setting the Enable latch.

Power Up

If a multiple-drive system is used, the individual drives must be automatically powered up one at a time to prevent power line overloading. The first drive to power up provides a sequence signal to the second drive so that it can power up. When it powers up, it provides a sequence signal to the third drive so that it can power up. This sequencing continues until the last drive in the string is supplied with the sequence signal.

In the following description it is assumed that the drive is the first one in a string and provides a sequencing signal to the next drive in the string.

When initial power is turned on, and while current is building up in the coil of the sequence bypass relay (K1), the Sequence latch (C4D/C5B) is reset by the ground potential through CR6 and K1, pin 1. This signal (-Power Up Reset) is also used by the Index/Sector board and the Cylinder Transducer Amplifier. As soon as K1 opens, the reset condition on the Sequence latch is removed.

When the controller generates the signals Controller Sequence In and Controller Controlled Ground, the signals +Sequence In and +Controlled Ground both go high enabling NAND gate B4D. The low output NAND gate B4D sets the Sequence latch, causing its set output to go high. This high signal is applied to NAND gate C4B-5, partially enabling it, and to NAND gate C5A-2. Since the other two inputs to gate C5A are filled by the closure of switches S7 and S2, gate C5A is enabled. The low output of C5A and the low output of NOR gate A4B are applied to NAND gate A4A, enabling it, causing the command signals -Retract Heads and +Retract Heads to be inactive. The output of NAND gate A4A also enables NOR gate A5B-5, whose low output is inverted by B5B. The high output of B5B turns transistor Q1 on, which provides a ground path for relays K1 and K2, the running time meter and spindle drive motor relays, respectively. K2 energizes and applies primary AC power to the spindle drive motor. The drive motor starts and causes the spindle and disc pack to begin rotating.

When the spindle drive motor reaches 70% of its operating speed, the signal +Up Speed goes high. This signal is inverted by B5C and routed to the input of NOR gate C4A-2. With C4A enabled, its output enables NAND gate C4B, which is inverted by C4C, generating the signal -Sequence Out. This signal is the Sequence In signal to the next drive in the string, and causes the next drive to begin its power-up sequence.

The low output of NAND gate B5C is also applied to NAND gate A5A-2. The input to NAND gate A5A-3 went low at the same time Q1 turned on. Thus, gate A5A is enabled and its output goes high, enabling NOR gate A5C, whose output is inverted by A5D and applied as a high input to a 60-second delay circuit, and to NAND gate B5D-13.

NOTE

See the Delay Timer logic description for a detailed description of the time delay circuits.

After the delay times out, NAND gate B5D-12 goes high, enabling it. The low output of gate B5D is applied to NOR gate B5A-2, enabling the gate and generating the signals +Seek Enable and -Seek Enable. These signals go to the Control Safety, Servo Sequencer, and Index/Sector boards to enable the logic on those boards to perform their respective functions in a first-seek sequence. When the heads start to move into the disc pack, the Heads Extended-Heads Retracted switch moves to the Heads Extended position. This causes NOR gate A4B-6 to go low; but since A4B-5 remains high (+Up Speed signal is still present), the signals +Retract Heads and -Retract Heads remain inactive. The Heads Extended position of the switch also causes a low signal to be applied to NAND gate A4C-9. This enables gate A4C since the other input is the -Seek Enable signal, which is low. The high output of gate A4C enables NOR gate A5B, whose output keeps the disc pack motor running, and enables NOR gate A5C (via NAND gate A5A) to assure that the two Seek Enable signals remain active.

If the drive just discussed has no AC power applied (e.g., S1 is open), the sequence bypass relay (K1) will not become energized and the -Sequence In signal at pin L will pass through the closed relay contacts to become the signal -Sequence Out to the next drive in the string. In other words, a unit without AC power is bypassed in the power-up sequencing. Another set of contacts on K1 disconnects the line receiver from the Controller Sequence In signal while the unit is being bypassed.

When a drive in a string of units has its START-STOP switch in the STOP position, NOR gate C4A-1 is low, enabling that gate. The high output of gate C4A partially enables NAND gate C4B. When the Sequence latch is set, either by the controller or by a preceding drive, NAND gate C4B is enabled and its output goes low. This signal is inverted by C4C and the line driver, generating the signal -Sequence Out, which is routed to the next drive in the string.

With S7 in the STOP position, a disc pack motor never starts running because NAND gate C5A-13 is low, generating the command signals +Retract Heads and -Retract Heads via NAND gate A4A and inverter A4D. Since the heads are retracted, NAND gate A4C-9 is high, causing the gates output to be low, disabling NOR gate A5B, causing transistor Q1 to turn off. This means relay K2 is open, preventing primary AC power from being applied to the spindle drive motor.

The last unit in a string of units, or a solitary unit, powers up as described in the beginning of this paragraph. However, in either of these cases, the signal at pin K of A08 (Sequence Out) is terminated instead of going to another unit. A drive can also be powered up by connecting an off-line tester to J14.

Power Down

To power down a drive, the START-STOP switch is placed in the STOP position. NAND gate C5A-13 then goes low, disabling it and causing its output to go high. This causes NAND gate B4A-2 to go high, partially enabling it. This high signal is NANDed by gate A4A and the command signals +Retract Heads and -Retract Heads become active. The heads begin to retract and the Servo Sequencer logic board (A03) is reset to state 0000. When the heads are fully retracted, the Heads Extended-Heads Retracted switch changes to the Heads Retracted position, disabling NAND gate A4C. The output of A4C goes low and disables NOR gate A5B. The output of gate A5B goes high turning transistor Q1 off. K2, the motor relay, switches the spindle drive motor leads from the primary AC voltage to the dynamic braking circuit. The Heads Retracted position of the switch also causes NAND gate B4A-1 to go high, enabling it. This low output is inverted by NOR gate B4B and a 12-second delay circuit begins timing out. For 12 seconds, NAND gate B4C is enabled, and dynamic braking current is applied to the spindle drive motor, stopping it.

The controller powers down a string of units by removing the Controller Controlled Ground signal to reset the Sequence latch. The low output of the Sequence latch disables NAND gate C5A, which causes the Retract Heads signals to become active. The heads retract and Q1 turns off. Dynamic braking is not applied in this case so the spindle drive motor coasts slowly to a stop.

If the disc drive door is opened while the machine is running, NAND gate C5A-1 will go low, disabling it. The heads will be retracted and the motor and meter relay will be disabled. Dynamic braking will be applied in this case.

The READ/WRITE-READ ONLY, the ENABLE-DISABLE, the START-STOP, and the Door Open-Door Closed and the Heads Extended-Heads Retracted switches are each connected to interface latches. Each RC/latch combination acts as an antibounce circuit by holding its output until the switch arm contacts the opposite side. The Heads Extended-Heads Retracted switch antibounce circuit differs slightly from the other four circuits by using diodes CR1, CR2, and CR10. CR10 prevents resistors in the antibounce circuit from activating Q1 on the Servo Control board when the Heads Extended-Heads Retracted switch is closed. CR1 blocks feedback from other Heads Extended-Heads Retracted switches in a string of drives. CR2 allows the use of a relay on the Heads Extended-Heads Retracted line by preventing the relay from being energized by reverse current (through the resistors in the antibounce circuit) when the heads are retracted.

If the READ/WRITE-READ ONLY switch is placed in the READ ONLY position, R1 is grounded and the interface latch is set; NAND gate D3D-13 goes high and NAND gate D3A-1 goes low. If the signal -Unit Selected is inactive (high) NAND gate D3D is enabled and its output goes low. The Read Only latch (D3C/D3B) is set and the signal +Read Only goes high. This signal is sent back to the controller and to the READ ONLY indicator on the operator control panel. The READ ONLY indicator lights. The ENABLE-DISABLE switch controls the Enable latch in a similar fashion.

If the unit is selected (-Unit Selected is low), the READ/WRITE-READ ONLY and the ENABLE-DISABLE switches have no effect while the unit is performing an operation.

WRITE LOGIC (A09)

The data to be written onto the disc pack (Write Data Input) is routed from the controller to pin 2 of the Write Logic board A09 (see Write Logic System Logic Diagram). This data is in the form of pulses and enters the line receiver which consists of Q18, Q19, and Q20. The output of Q20 is connected to complementary flip-flop C1A whose state will change each time a pulse is received from Q20. The output of the flip-flop is amplified by differential amplifier Q21/Q22 whose push-pull output (Write Data) is sent out of pins 3 and 4 of the Write Logic board to both the Read Write Amplifier (Left) and the Read Write Amplifier (Right). Thus, each data or clock pulse will cause a change in the direction of write current through the selected head.

Because the Write Data is sent to both left and right Read/Write Amplifiers simultaneously, provision must be made for selecting either the left or right Write Amplifier.

The left column of heads and its associated circuitry is a mirror image of the right column of heads and its associated circuitry. Therefore, only the operation of the right column of heads will be discussed in detail.

For the right column of heads to write, the signal -Write (RT) which enters pin D of the Write Logic from the Head Selection and Register logic must be active. Applying a low level to inverter D2B turns on transistor Q9 which turns on Q10 by applying a zener reference level of 6.2 volts to its base. Q10, in conjunction with the inductor and precision resistor in the emitter circuit, operates as a constant current source to supply 40 ma to pin 11. This is the signal +Write I (RT). This current goes to the Read/Write Amplifier (Right) board.

When the drive is writing, write current is sensed by shunting a small amount of current through R22 and R23 turning transistor Q13 off. This turns off Q14 and the signal -Write I (Sense) is generated and sent to the Control Safety Logic. An inverted version of this signal is sent to the controller, via Line Driver (B09).

If the CAR has been programmed to cylinder 128 or greater, the signal -CAR 128 at pin C is active. This results in Q8 turning on, shunting some of the current supplied to Q10. Thus the signal +Write I (RT) is only 35 ma for the higher numbered (inner) cylinders of the disc pack. This is done because the heads fly closer to the disc surface and the density of data is greater at the inner cylinders, requiring reduced head current.

While the head is writing it must also be erasing on both sides of the newly recorded track in order to remove any trace of previous information, which, because of head positioning tolerances, would otherwise remain and affect disc pack interchangeability. The signal -Erase (RT) at pin F of the Write Logic accomplishes this through inverter D2E, turning Q5 on. Q6 is then turned on and the signal +Erase I (RT) is activated. This signal supplies 48 ma of current (as determined by resistor R18) to pin 10 which connects to the Read/Write Amplifier (RT) to activate the proper erase head in the right column of erase heads.

The fact that the drive is erasing is sensed by the erase sense circuit. If the erase circuit is turned on, a small amount of the erase current is shunted through R16 to Q3 burning it off. When Q3 is turned off, transistor Q4 is turned off and the gate D5C is turned on. The signal -Erase I (Sense) is active at pin 21 and is routed to the Control Safety logic.

Under certain conditions it is necessary to prevent any writing on the disc. In these cases the Control Safety logic generates the signal -Write Inhibit, which enters the Write Logic at pin H and is inverted by D2D. Transistor Q7 turns on and shunts all write current to ground, preventing it from entering the write coils on the selected head.

The Write Logic board also contains the circuit for generating the signal -AC Write. The head inductance causes voltage spikes at the Write Amplifier when write current is switched. A sample of these pulses is routed to the Write Logic, pin 8, where it is amplified by Q15. The AC signal is coupled through C6 to the base of Q16 turning it on and off as data pulses are received. C7 charges through Q16 during a data pulse and the charged capacitor holds Q17 off while the string of data pulses is present. The time constant is such that a steady stream of pulses at the 1F rate (2.5 MHz) will keep Q17 turned off. Under these conditions, gate D5B is turned on and the logic signal -AC Write at pin 22 is enabled.

READ AMPLIFIER (A10)

Because the left column of heads and its associated read circuitry is a mirror image of the right column of heads and its associated circuitry, only the right column of heads is discussed.

The signal read off the disc is amplified by the Read Preamplifier (Right) and enters the Read Amplifier on pins 20 and 21. The signal from the Read Preamplifier (Left) enters on pins 18 and 19. A diode selection gate controlled by Q1, Q2, Q3, and Q4 chooses either the left or the right signal for amplification by the Read Amplifier. The signal +Left Select, which enters the Read Amplifier on pin 17, determines which diode gate will be turned on. If the signal +Left Select is low, the signal Read Preamplifier Output (Right) will pass through diodes CR13/CR17 and CR14/CR18 and be routed to the bases of a filter driver, transistors Q5 and Q6. Transistors Q7 and Q8 provide a constant current source for the filter driver.

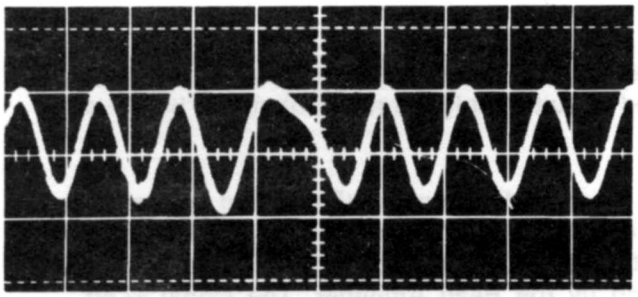
The collectors of Q5 and Q6 are connected to a low pass filter, which eliminates frequency components of the signal above 3.5 MHz. The filter output is amplified and limited by five differential amplifier stages consisting of Q9/Q10, Q11/Q12, Q13/Q14, Q15/Q16, and Q17/Q18. Transistors Q19/Q20 and Q21/Q22 comprise a pulse-forming network which forms the pulses into 70-nsec widths. The pulses are shaped and amplified to the desired level and then coupled through driver transistor Q27 to the controller as the Read-Output-to-Cont signal. A Read pulse turns Q27 on. Transistor Q25 is turned on when the signal -Selected Read Gate on pin 3 goes high. This grounds the emitters of transistors Q23 and Q24, preventing pulses from reaching driver Q27 and keeping noise off the Read Coax when no Read is in progress.

The Read Amplifier also contains the line select drivers which receive their signals from the Head Selection and Register logic. These line-select drivers supply the required voltage levels to the head-select transistors on the Read/Write Amplifier boards. Each line-select driver connects to two head-select transistors, one on the left and one on the right Read/Write Amplifier. The head selected for erase current is determined by the Line Select signals also.

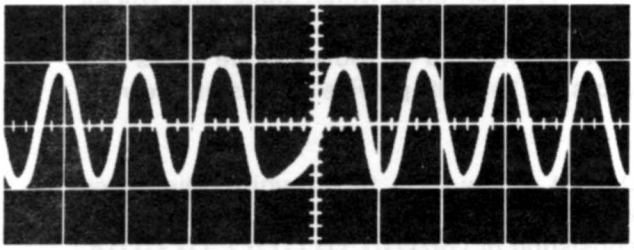
Read Amplifier PC Board (A10) Waveform Notations

Five oscilloscope photographs of waveforms taken at progressive points in the signal flow path of the Read Amplifier are shown below. A hexadecimal EF data pattern is used to show the effects of a single logical zero in the midst of a pattern of logical ones. The oscilloscope sweep rate is adjusted to show the full 16-bit data pattern (3.2 μsec). Photographs A, B, and C were taken differentially and photographs D and E were taken single-ended.

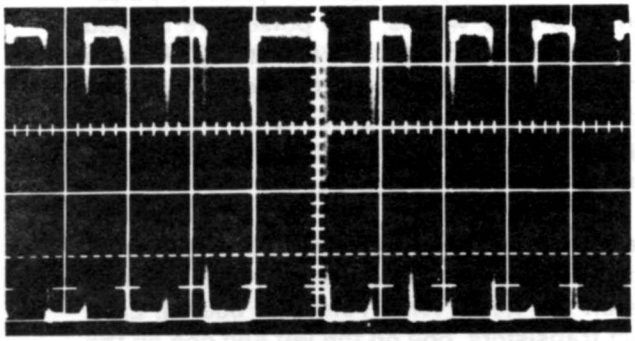
Note that with the input level used, the amplifier and first limiter operate in the linear mode so that the waveforms shown in A and B show no clipping. Waveform C shows that the signal is fully limited following the fourth limiter. Photograph D shows that the pulse shaper has created 70-nsec pulses for each zero crossing of the input signal. Photograph E shows that these pulses are rectified so that only negative pulses are produced on the read output line.



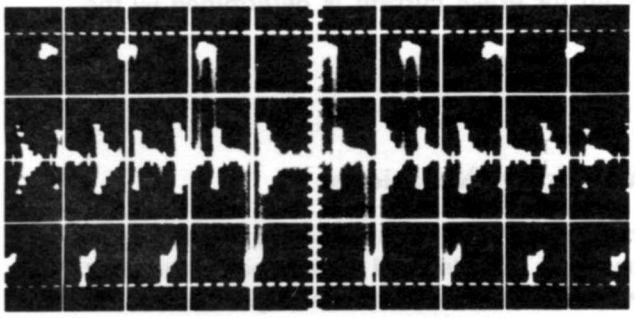
A 3.5 MC FILTER OUTPUT
200 mv/division



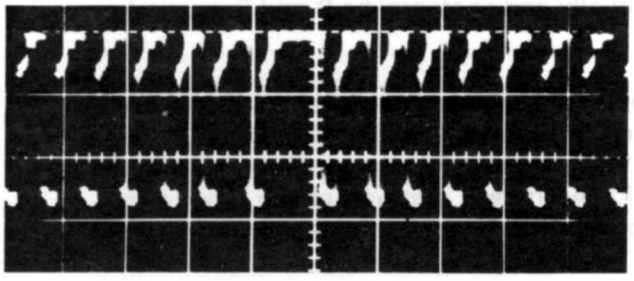
B FIRST LIMITER OUTPUT (TP5)
1 volt/division



C FOURTH LIMITER OUTPUT
1 volt/division



D PULSE SHAPER OUTPUT
1 volt/division



E LINE DRIVER OUTPUT (TP1)
2 volts/division

SYSTEM PROTECTION (B02)

System Protection board (B02) protects the linear-motor bobbin winding from overheating should the carriage fail to retract within 400 msec after Retract Heads has been commanded. Following this period, the protection circuit limits the amount of current applied to the bobbin winding by clamping the signal Programmed Current for 110 msec out of each 140-msec duration.

The System Protection circuit also detects any seek attempts during a clamp operation and causes a File Unsafe to be generated under this invalid condition.

Linear Motion Protection Circuit Operation

When the signal +Retract Heads goes high, a forced reverse velocity is applied to the linear motor by the servo system and the heads begin retracting out of the disc pack. After the signal +Retract Heads is inverted by 1C-6, it triggers the single-shot delay circuit (3A), whose output is delayed from going high for 400 msec. Normally, during this 400 msec, complete head retraction takes place. After 400 msec, the linear motor protection circuit, although turned on, is not utilized because, upon retraction, the effect of the rectangular clamping waveform is overridden by 100% clamping. When the 400 msec times out, NAND gate 1C-8 is enabled, which in turn enables NOR gate 1C-11. The high output of 1C-11 turns on the free-running rectangular waveform generator, which consists of a 140-msec astable generator (2A-6) and 30-msec one shot (2A-9). The high output of 1C-11 also enables NAND gate 2C-12. The rectangular waveform becomes the signal -Servo Clamp, which is applied directly to the signal Programmed Current. The signal -Servo Clamp goes active 110 msec out of each 140 msec, clamping the Programmed Current and drastically limiting power to the bobbin winding for approximately 80% of each 140-msec period. This limits average bobbin current to a safe value if the heads fail to retract. The current that is applied for 30 msec of each 140-msec period provides enough energy to bring the carriage and heads to a fully retracted position.

Loss of +5 volts from the logic supply will also cause the linear motor protection circuit to operate. Upon loss of the +5-volt logic supply, the output from the +5-volt Servo Supply (+5Vs) applied through R12 ensures that the output of gate 1C-6 goes low, initiating a chain of events identical to that described for Retract Heads.

A +Seek Incomplete signal, after a 1-μsec delay, also causes the linear motor protection circuit to operate.

System Unsafe Circuit Operation

The Servo Unsafe latch and the Overtemp latch are initially set by -Pwr Up Reset or by manually pressing the CE Reset button (S1). The Servo Unsafe latch sets if the servo clamp is enabled while a seek is in process; normally an illegal combination of conditions. If the heads have not been commanded to retract, +Retract Heads is low (normal operating condition) and the output of gate 1C-6 is high, partially enabling NAND gate 2C-8. If a clamp operation (caused by a circuit failure) is in progress, the output of gate 2C-12 is pulsing low, partially enabling NAND gate 2B-1.

At this time, any seek attempt will cause the output of NOR gate 2B-13 to go low. This enables NAND gate 2B-1, which enables NAND gate 2C-8, setting the Servo Unsafe latch. NOR gate 1C-3 is thus enabled, and the signal -System Unsafe is generated. The signal -System Unsafe causes a File Unsafe to be generated.

NOR gate 1C-3 can also be enabled by setting the Overtemp latch causing a -System Unsafe.

+5V Servo Supply

This +5V Servo supply is derived from the +36-volt Servo supply. It is used to supply the 5 volts for the operation of the logic on B02 board and has an output on pin 11. The 5 volts is controlled by a 5.1V, 1% zener diode (CR1) at that input of the operational amp (A1). This amplifier provides a high gain element in the feedback loop of the regulator. It feeds the series pass element Q1 whose output becomes the +5V(s).

DELAY TIMERS (B03)

The six delay timer circuits contained on the Delay Timer board (B03) generate signals of the required duration for use by the Servo Sequencer board and the Power-Up Sequencing and Control board. In general, these durations are times required for certain mechanical functions.

The delay timer circuits generating the signals +T1, +T2, +T3, and +T4 all have basically the same design except that each time delay network has a different RC value which determines the duration of the delay. Because of this similarity, only the delay timer circuit associated with +T1 is described in detail. All timers used by the Servo Sequencer board are reset and started with the same signal, +Reset Timers.

When the signal +Reset Timers is decoded by the Servo Sequencer Decode board it is applied to pin 7 of the Delay Timers board. The signal is inverted by D2C and applied as a low to the reset input of the Seek Incomplete Delay latch (D6A/D6B), resetting it. The signal is also inverted by D7A and applied as a high to the 100-msec time delay circuit consisting of Q1-Q5. This high signal, which must be 10 μsec or longer, resets the time delay circuit if it has not timed out. Since the 100-msec time delay circuit requires a low-going signal to initiate it, nothing happens until the +Reset Timers signal goes low. When it does, the output of D7A goes low, initiating the time delay. This delays the signal for 100 msec before it sets the Seek Incomplete Delay latch. This means the signal +T1 is delayed 100 msec after the signal +Reset Timers goes low. The signals +T2, +T3, and +T4 are generated in similar fashion.

The signal +T6 (labeled 12-Second Dynamic Braking) is used by the Power-Up Sequencing and Control board (A08) to limit the application of dynamic braking current to the spindle drive motor to 12 seconds. This current is applied to the spindle drive motor when the START-STOP switch on the operator control panel is placed in the STOP position.

When the signal +Start T6 is low, the Dynamic Braking latch (D3A/D3B) is reset. NAND gate D3C is disabled and its high output resets the time delay circuit. The high reset output of the latch is routed back to one input of the NAND gate (D3C), partially enabling it. When the signal +Start T6 goes high, it is applied to the other input of NAND gate D3C, enabling it, causing its output to go low. This low signal is delayed 12 seconds by the 12-second time delay circuit (Q21-Q25). When the time delay circuit times out, the Dynamic Braking latch D3A/D3B is set. Thus, the signal +T6 goes low 12 seconds after the application of the signal +Start T6.

The circuit used to generate the signal +T5 (labeled 60-Second Warm Up), uses two 10-second time delays, a latch, and a two-bit ripple counter for its operation. The signal +T5 is used in the seek enable circuit on the Power-Up Sequence and Control board (A08).

When the signal +Start T5 is low, the latch consisting of D3D/D4A and the 2-bit warm-up timer counter (D1A/D1B) are reset. When the signal +Start T5 goes high it is applied to the input of NAND gate D4C. Since the other inputs to NAND gate, D4C, are high as a result of a previous resetting of the latch and the arm-up time counter, the gate is enabled. Ten seconds later, because of the 10-second time delay (Q26-Q30), the latch consisting of D3D/D4A sets. Once the latch is set, the low reset output of the latch disables NAND gate D4C and the high set output of the latch enables NAND gate D4B.

The output of NAND gate D4B goes low and, 10 seconds later, because of the 10-second time delay (Q31-Q35), the latch resets. The latch and the two 10-second timers toggle once every 20 seconds. The set output of the latch is fed to the clock input of the first J-K flip-flop of the warm-up time counter. This counter counts the number of times the latch is reset. NAND gate D2A decodes a count of three. Three consecutive 20-second delays produce one 60-second delay. The 60-second delay signal is inverted by NOR gate D2B and becomes the signal +T5 (60-Second Warm Up). The low out of NAND gate D2A is also fed back to the input of NAND gates D4B and D4C, stopping additional toggling of the latch.

SERVO SYSTEM (B04)

This PC board has the responsibility of controlling the servo. It accepts the binary velocity decodes through a Digital-to-Analog (D/A) Converter and converts them to an analog current. Since this binary coded current cannot be used efficiently due to its huge dynamic range, a Shaper Circuit is used to optimally shape this current to a non-linear velocity scheduling voltage. The algebraic sum of the velocity scheduling voltage and tach feedback velocity voltage drives the Error Amplifier. The Error Amplifier output voltage serves as an input to the current driver which controls motor current and direction via a power bridge circuit.

The D/A Converter receives the 7 -Difference signals from the Adder and Speed Decode card (A05). Each of these difference count inputs controls a transistor-saturating switch that connects +15 V to a precision current programming resistor. These resistors connect to the summing junction of operational amplifier A4 (Shaper Amplifier). Thus each digital input results in analog current into the op-amp summing junction.

The function of the shaper circuit is to optimally shape the digitally selected input current to a desired analog voltage to drive the Error Amplifier. A non-linear function was found to be most appropriate as a velocity scheduling for the servo system to achieve the fastest seeks possible. The shaper feedback circuit has seven feedback paths. The FET switch (Q26) is turned on only on forward accelerating portion of the seek when the gain requirement is lower. The other five paths, through the use of diodes CR6 through CR10 (see schematic of B04 card), are prebiased to turn on precisely at different points of the curve, thus changing the gain of the amplifier at these points.

Due to a high output impedance of the tachometer (2.5K), the device is buffered with a unity gain, non-inverting amplifier A1 and drive transistors Q1 and Q2. The tachometer is lightly loaded by R3 to provide a convenient scale of factor of 100 mV per 1 inch per second of carriage velocity. The Tachometer Amplifier analog output is converted to an analog current by R45 and R18. R18 is a resistance potentiometer to compensate for tachometer scale factor variations and to adjust servo gain.

The Error Amplifier, A6, with feedback resistor R83, compares the algebraic sum of the shaped analog velocity current with the analog tachometer current and provides an output error voltage, Programmed Current, proportional to the difference. It is this error voltage that drives the linear motor to achieve the programmed velocity during the entire seek. The access direction is determined on chopper switches Q16 and Q17 depending whether the Forward or Reverse is activated. For forward seeks, -Forward Drives signal is low which turns Q17 off, thus providing shaper output a path to drive the inverting input of the Error Amplifier. Q16 at this time is turned on by -Reverse Drive being high, thereby shunting drive signal to ground. Because of the symmetrical switching network, Reverse works in the same manner except that Q16 is turned off and Q17 is turned on.

There are two velocity detecting circuits: the Forward Velocity Detector (A3), which detects ¾ IPS and the 2 IPS Detector (A2). The +Forward Velocity signal from the Forward Velocity Detector is used by the Servo Sequencer as a status signal for seek

incompletes and other interlocking purposes. Whenever the carriage exceeds 3/4 inch per second in the forward direction, the Tach Buffer Amplifier output will exceed 75 mV. The Voltage Comparator Circuit (A3), comparing this voltage with its 75-mV reference, will provide a logic 1 output. The 2 IPS Detecting Circuit (A2) also compares the Tach Output Voltage against its reference which is set at 200 mV. A logic 1 output is provided from Q11 until velocity is greater than 2 ips.

Four safety circuits are mounted on the card to protect the servo system. The first is the Servo Coast Clamp circuit, which restricts the maximum error output to 2. 85 and -. 9V whenever +Holding Current is active. The normal Holding Current output is 200 mV, so the clamp has no effect. If the carriage were manually forced back and forth, the clamp would prevent the transistor bridge from providing excessive motor currents. Transistor Q20 (see schematic) turns on the limit Error Amplifier positive voltage to +0.1 V, thus limiting motor current to less than 200 ma (servo coast mode). There are two conditions for activating the clamp circuit; one is to prevent servo from acceleration whenever forward deceleration current has been activated (IC2 pin 12 low via $\overline{\text{(Anticipate)}}$ • (Forward Drive) • (Force Forward Slow). The other is to allow the carriage to coast into detent via a 2-ips detector, A2 (similar to Forward Velocity Detector), with the following condition: ($\leq$2 IPS) (Forward Velocity) • (Forward Detent Velocity).

The second safety circuit provides an overtemperature protection to the Power Bridge transistors and the motor bobbin. When the bobbin temperature exceeds 230°F or the power transistors overheat, the +Over Temp signal goes high, thus disabling the servo and causing a File Unsafe condition. There are two inputs to the Overtemperature Sensor Voltage Comparator (A7). These inputs are connected to the negative-temperature-coefficient resistors (thermistors) which are tied to -15 V. The voltage dividers, consisting of the external thermistors and R110 and R111, normally hold the input to the comparator more positive than -5 V. If the thermistors decrease in resistance sufficiently to cause the input to fall below -5 V, the comparator will provide a true logic output called +Over Temp to initiate File Unsafe Condition. There is a -15 V clamp connected to the output of the comparator. Its function is to clamp the +Over Temp to ground when loss of -15 V caused a File Unsafe Condition (i.e., Q25 turns on), thus preventing a race condition between loss of -15 V Retract Heads and Servo Disable (caused by File Unsafe).

Another safety circuit is activated by loss of either +5 V or -15 V. Either condition will cause CR4 to impress its zener voltage across R43 and the base-emitter of Q13 and thus provide a programmed current to drive the Error Amplifier to retract heads.

Another positive clamp circuit clamps the output of the Error Amplifier so as to prevent forward accelerating currents to the linear motor and thus prevent the servo from on-off chattering and acceleration during detenting. +Holding Current is used to turn the Holding Clamp on to limit forward drive to 3.5 amp and reverse drive to 1.2 amp in case the carriage is manually pushed.

INDEX/SECTOR (B05)

As the disc pack rotates, the Index Transducer generates a dipulse each time an index or a sector slot passes it. The index transducer amplifier circuit on board B06 provides a logic level when the dipulse exceeds a preset threshold. The Index/Sector logic board (B05) converts this signal into a 2-μsec pulse, which is utilized by the controller and by other circuits on the board. The Index/Sector logic also has the ability to separate the index pulses from the sector slot pulses when used in installations operating with sector mode packs. It can divide the sector slot count by 1, 2, or 4 to provide for several different sector modes of operation. In addition to utilizing index pulses for determining whether or not the spindle drive motor is up to speed, the Index/Sector logic also decodes the following signals: +Selected Seek Ready, +Drive Ready, +Servo Disable, and +Pick. It inverts the signal +Selected Read Gate for use in the Read Amplifier board (A10).

Selection of mode (index only or sector mode) and sector slot count division is made at the time the machine is installed.

Index Only Mode

In the index only operating mode, the disc pack must have only one slot; the index slot. In this mode, the $\overline{Q}$ output of flip-flop B4A is physically grounded with a jumper wire, forcing it low and partially enabling NAND gate C5B-5.

When an index slot is detected, a low logic signal is applied to pin 19 of B05. This low input is inverted by C4A, applying a high input to NAND gate C4D-12. The RC network R1-C11 provides immunity from short bursts of negative-going noise on the input. The low input to the index width time delay circuit causes its output to switch high 2.0 μsec later, enabling NAND gate C4D. This 2-μsec pulse that is generated represents the index slot. The low output of NAND gate C4D is inverted by D4C, generating the signal +Composite Index Sector. Since there are no sector slots when operating in the index only mode, only index slot pulses are present on this line. The low output of NAND gate C4D also enables NAND gate C5B, whose output goes high, generating the signal +Index.

The signal +Index is inverted by D4A to generate the signal -Index, which is used to directly reset the sector division flip-flops in addition to being sent to the upspeed circuitry.

Sector Mode

In the sector mode, the disc pack index position is derived from two closely spaced slots; a sector slot and an index slot. Other slots, evenly spaced around the disc are the remaining sector slots. In this mode, the $\overline{Q}$ output of flip-flop B4A is left ungrounded.

As the disc pack rotates, the index slot and sector slot signals are all shaped into 2-μsec pulses as described above.

The output of NAND gate C4D is a string of pulses composed of both index and sector slot pulses; each index slot pulse follows one of the sector slot pulses by less than 300 μsec. This signal is the inverted version of +Composite Index Sector, which leaves the board on pin 17. The signal at the output of NAND gate C4D is also routed to NAND gates C5D-12 and C5B-6 in addition to serving as the clock input to flip-flop B4A.

In the sector mode of operation the logic separates the sector slot pulses from the index slot pulses. All of the sector slot pulses may be used by the controller (+Sector ÷ 1), half the sector slot pulses may be used (+Sector ÷ 2), or one-quarter of the sector slot pulses may be used (+Sector ÷ 4), depending on which sector mode selection terminals have been jumpered.

In the following discussion it is assumed that an index slot pulse has just occurred, resetting flip-flops C2B and C2A, and a sector slot pulse is just starting to be generated at the output of NAND gate C4D.

During the duration of the negative 2-μsec sector slot pulse at the output of C4D (i.e., before the positive-going trailing edge of that pulse sets flip-flop B4A), flip-flop B4A is in the reset state and its Q output is low, partially enabling NAND gate C5D-11. The presence of the sector slot pulse satisfies the input requirements of NAND gate C5D, whose output goes high and is inverted by C3B. If a jumper is placed between terminals E1 and E2, the signal is inverted again by D2C to become +Sector ÷ 1. With these terminals jumpered, every sector slot pulse will be transferred through the logic.

When the 2-μsec sector slot pulse returns high, NAND gate C5D is disabled and its low-going output clocks flip-flop C2A. The Q output of C2A goes high and partially enables NAND gate C3A-2. The second 2-μsec sector slot pulse causes the output of NAND gate C5D to go high. This satisfies NAND gate C3A and its output goes low. If a jumper is placed between terminals E3 and E4, the output of NAND gate C3A is inverted by D2C to become +Sector ÷ 2. With these terminals jumpered, every other sector pulse will be transferred through the logic.

If only every fourth sector slot pulse is desired, terminals E5 and E6 must be jumpered. In this mode, both flip-flops C2B and C2A are used as a two-bit counter, while NAND gate D2A decodes a count of three plus the following sector slot pulse (four total). The output of NAND gate D2A is jumpered across terminals E5 and E6, and inverted by D2C to generate the signal +Sector ÷ 4.

In any sector mode, upon detection of an index pulse, the low output of inverter D4A causes flip-flops C2B and C2A to reset.

When the adjacent index/sector slot pulses are detected, the first pulse clocks flip-flop B4A, setting it, causing its $\overline{Q}$ output to go low. The low $\overline{Q}$ output triggers a 380-μsec index time delay circuit. While the delay circuit is timing out, the $\overline{Q}$ output of flip-flop B4A is low, partially enabling NAND gate C5B-5. Since the index slot pulse follows the sector slot pulse by less than 300 μsec, the second pulse detected at the output of NAND gate C4D causes NAND gate C5B-6 to go low, enabling it, generating the signal +Index. When the time delay circuit times out, it directly resets flip-flop B4A, causing its Q output to go high. This disables NAND gate C5B until the adjacent index/sector slot pulses are detected during the next disc revolution.

Upspeed Detection

The rate at which index pulses leave NAND gate C5B and inverter D4A determines whether or not the disc pack is up to the required speed. The upspeed detection circuit consists of NAND gates C3C, C3D, and C5C; flip-flops B4B, D5A, and D5B; and two 37-μsec upspeed time delay circuits (A and B).

When a drive is turned on, the signal -Power Up Reset directly rests flip-flop D3B. The spindle drive motor starts turning and accelerates.

To generate the signal +Upspeed, flip-flops D5A and D5B must be set at the same time. This will cause $\overline{Q}$ outputs of both flip-flops to be low, enabling NAND gate C5C, generating the signal +Upspeed.

During the time the spindle drive motor is accelerating, the slow rate of the -Index pulses is clocking flip-flop B4B alternately so that the state of the Q and $\overline{Q}$ outputs are reversing each time an index pulse occurs. At the same time, NAND gates C3C and C3D are strobed by the signal +Index so that one or the other gates is enabled, depending on the output state of flip-flop B4B. At slower spindle drive motor speeds, the 37-μsec upspeed time delay circuits alternately time out and alternately reset flip-flops D5A and D5B. Therefore, while the index pulse rate is low (low motor speed), the two flip-flops (D5A and D5B) are never in the same state.

As the motor speed increases, the alternation of flip-flop B3B becomes faster and at 70% of motor operating speed, the upspeed time delay circuits no longer have sufficient time to time out. Flip-flops D5A and D5B are then both set at the same time. Because the upspeed time delay circuits never time out, both flip-flops D5A and D5B are being clocked and set continuously without ever being reset. The $\overline{Q}$ outputs of D5A and D5B are both low, enabling NAND gate C5C, generating the signal +Upspeed. The signal +Upspeed is routed to the Power-Up Sequencing and Control board to indicate that the disc pack is up to speed.

If the disc pack speed drops, such as with a belt breakage, the reverse of the upspeed sequence described above will take place and the signal +Upspeed will go low.

The complete loss of index pulses (such as with a circuit or transducer failure) will also cause the signal +Upspeed to go low. When this happens, flip-flop B4B is no longer toggled and the 37-μsec upspeed time delay circuits time out and reset flip-flops D5A and D5B.

Other Functions

The other functions of the Index/Sector board are:

1. The signal +Selected Read Gate is inverted by C5A to become -Selected Read Gate. It is used by the Read Amplifier board.

2. The signal +Selected Seek Ready is decoded from the signals -Unit Is Selected and -Seek Ready by NAND gate D3A. This signal goes to the Control Safety board.

3. The individual disc drive is ready (+Drive Ready) if NOR gate D2B has all high inputs. This will cause the large unit number indicator on the operator control panel to light. This indicator will not light if the signals -File Unsafe or +Seek Incomplete are active or if -Seek Enable is inactive.

4. Inverter C1A will generate a +Servo Disable signal if NAND gate D1C is enabled. This condition occurs if the signals +Drive Ready and either -Seek Enable or +Retract Heads are inactive.

5. The signal +Pick is generated by decoding an inverted -D, -A, and -C and then generating a fixed-duration pulse with the circuit consisting of inverter C4C, NAND gate D3B, resistor R3, and capacitor C14. This signal is used by the Actuator Driver board.

TRANSDUCER AMPLIFIER (B06)

The controller initiates a seek by sending a new address to the CAR. The output of the CAR is compared to the PAR address. The computed difference between the two addresses represents the number of cylinders the heads must travel to the new address. As the heads move, the position of the heads is monitored constantly by a cylinder count scheme, which sends a count pulse to the PAR each time the heads reach a new cylinder. Each pulse increases or decreases (depending on the direction of head travel) the PAR count by one, which decreases the difference between the PAR and CAR by one. When the difference is zero, the heads are at the addressed cylinder and a detent engages to inhibit head movement.

Electro-Mechanical Sensing

Information within a disc pack is recorded on 20 surfaces, with each surface having 203 concentric circles (track 000 to track 202). Since corresponding tracks on all 10 discs are vertically aligned, the corresponding 20 tracks are considered information cylinders—there are 203 cylinders; i.e., 20 track 000s, 20 track 111s, and so on up to 20 track 202s.

As the heads are positioned from one cylinder to another, the linear travel of the carriage is monitored by accurately counting the number of cylinders reached. This is accomplished by a cylinder count scheme (Figure B06-1), which consists of a rack of teeth (called the detent rack), a double detent pawl, a double sensor cylinder transducer, a 145-KHz oscillator, and associated amplification and logic circuits.

As shown in Figure B06-1, the detent rack is mounted on the carriage and as the carriage moves the detent rack moves with it. Spacing of the rack teeth is 0.020 inches. The double detent pawl and cylinder transducer are mounted opposite the detent rack, on the carriage way, and are stationary.

The number and spacing of the rack teeth, and the alignment of the rack teeth with respect to the transducer sensors and the sensor spacing, is such that each rack tooth represents a cylinder count as a rack tooth passes a sensor (see Figure B06-1, COUNT detail).

The purpose of the detent pawl is two-fold: as a seek is completed, it engages the rack teeth, inhibiting head movement until a new seek is initiated, and it ensures the final finite track positioning for the heads as it engages.

Each pawl has a set of teeth with the same pitch as the rack teeth. The two pawls are offset from each other by one-half their pitch (0.010 inches). This offset spacing allows the pawl assembly to engage the rack in twice as many positions as there are rack teeth; i.e., when one pawl is engaged the other rests on the adjacent rack tooth. One detent pawl engages at all odd cylinder positions while the other engages at all even cylinder positions.

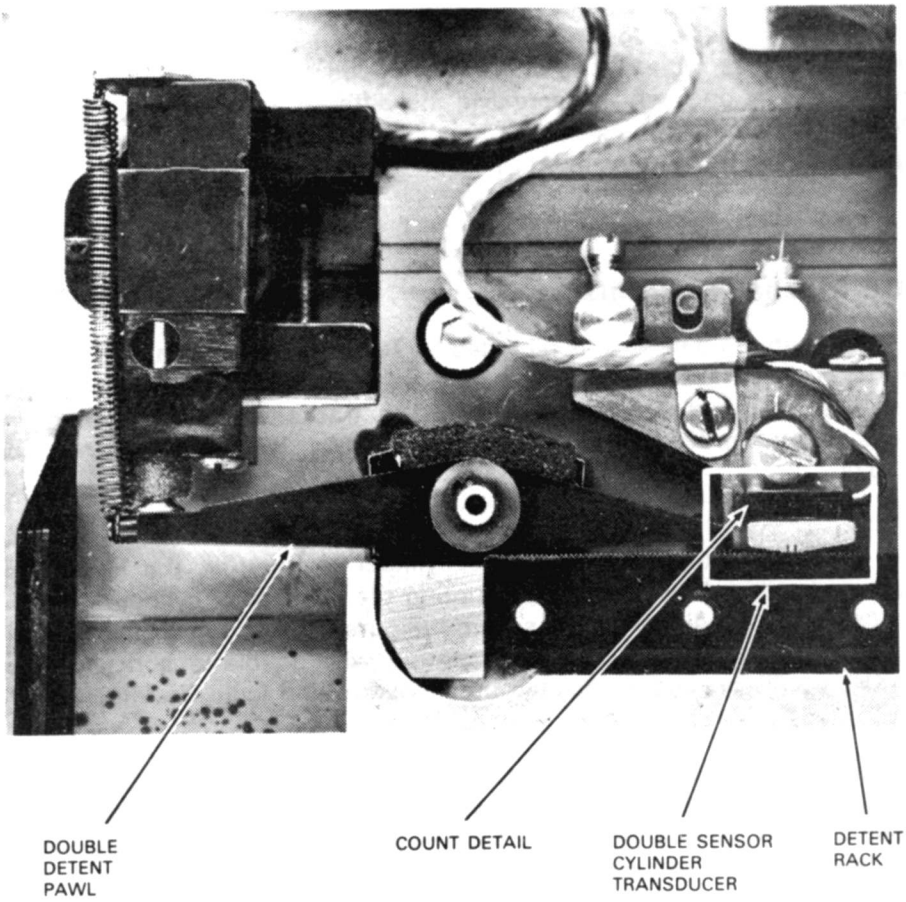


FIGURE B06-1. DETENT PAWL, DETENT PACK, AND CYLINDER TRANSDUCER LOCATIONS

The purpose of the cylinder transducer is to generate an output each time a new cylinder is reached (i.e, each time a rack tooth reaches a sensor). Thus, the teeth in the detent rack (which move as the carriage moves) are counted as they reach a sensor. As shown in Figure B06-2, the sensors are spaced apart so that when a rack tooth is opposite one sensor, a valley is opposite the other sensor. The two sensors are primary-secondary pairs. The primaries are in series and are driven by a 145-KHz Colpitts-type oscillator at a level of about 3 volts peak-to-peak. The secondaries are connected series opposing so that the outputs are 180° out of phase.

Each time that a rack tooth reaches a sensor (see Figure B06-2, sensor B), it couples the primary-secondary pair such that a maximum transducer secondary output exists because of the sensor couple. At this time, sensor A is opposite a valley (between two teeth) and its output is minimum, as well as being 180° out of phase. As the carriage moves to an adjacent cylinder, the rack-tooth-to-sensor relationship changes such that the output of sensor A is maximum and sensor B is opposite a valley; its output is minimum. At this time, the transducer secondary ouput is maximum because of sensor A coupling. During the period that the rack-to-sensor relationship was changing from coupling sensor B to coupling sensor A, a point was reached such that both sensors were equally coupled for an instant, and since the two sensor secondaries are connected series opposing, the two equal outputs partially cancel so that the resultant transducer secondary output is a minimum (null). Thus, there is always maximum output from the transducer secondary when a sensor is coupled, and minimum output when both sensors are equally coupled and their outputs are equal (see Figure B06-3).

The Cylinder Transducer Amplifier board (B06) uses the combination of the envelope amplitude and the phase change to generate the cylinder count pulses as the carriage moves from cylinder to cylinder.

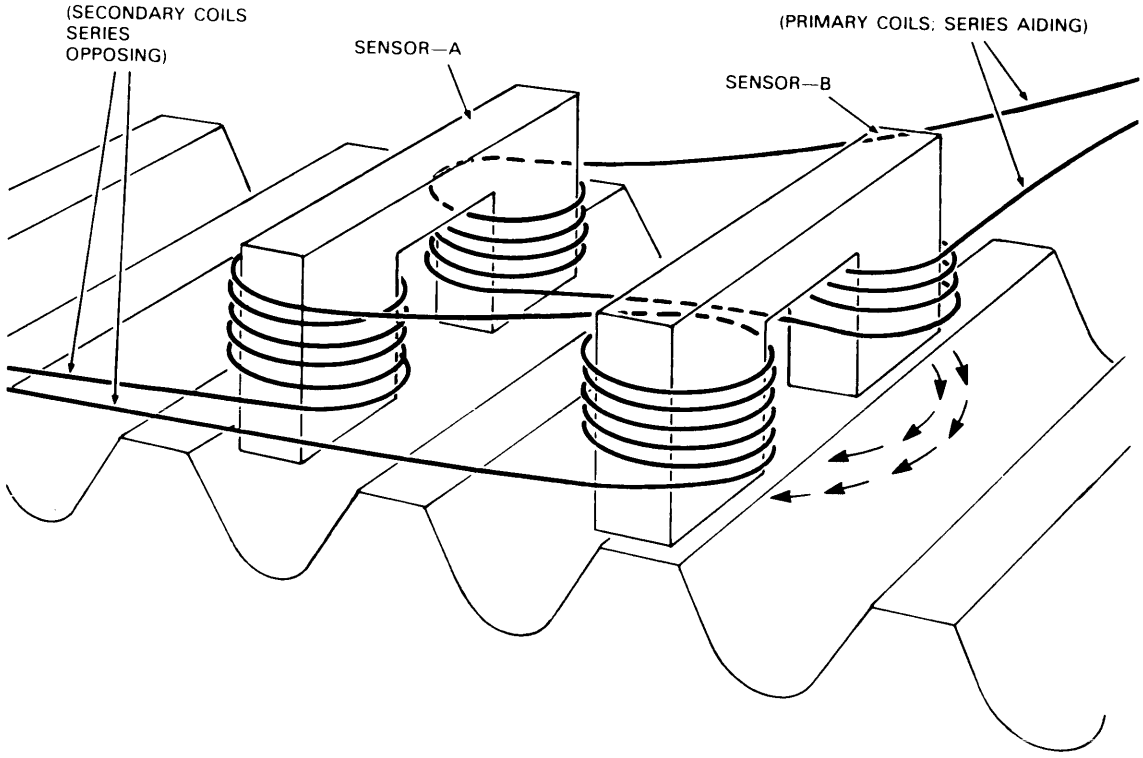


FIGURE B06-2. CYLINDER TRANSDUCER COUPLING

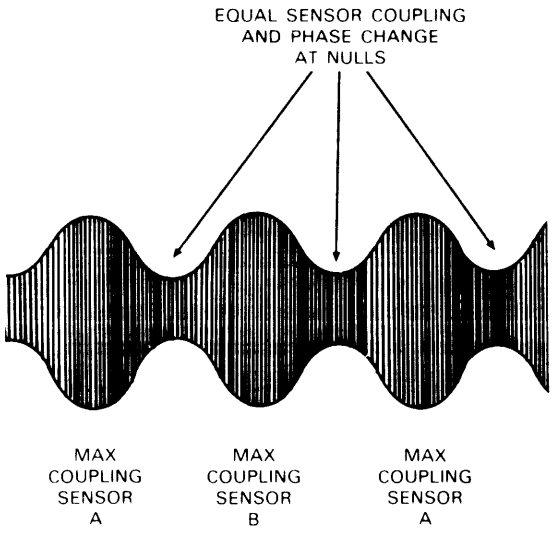


FIGURE B06-3. ADDED TRANSDUCER SECONDARY OUTPUTS

Strobe Pulse Generation

In addition to exciting the cylinder transducer primary winding, the sine wave output of the 145-KHz Colpitts-type oscillator is applied through two complementary emitter followers to the clock comparator (D2). This comparator has thresholds of 25 mv above and below zero volts and converts the oscillator signal to a nearly symmetrical square wave with a period of approximately 7 μsec. A filter network at the input of D2 eliminates any high frequency components which may be present on the oscillator signal due to noise or crossover distortion.

The output of the clock comparator goes directly to a 200-nsec one-shot (Q6), which triggers on the negative-going edge of the square wave, and generates a positive pulse, +Strobe B (see Figure B06-4). The clock comparator output is also inverted by B2F for use as the +Clock. The +Clock signal goes to another 200-nsec one-shot (Q5), which triggers on the negative-going edge of the square wave, generating the signal +Strobe A. The pulse +Strobe A follows the pulse +Strobe B by 3.5 μsec, and both pulses are used as clocking signals for various flip-flops on the board. These strobe and clock signals are generated continuously regardless of whether or not the carriage is moving.

Note that clock comparator feedback resistor R23 is connected to the output of inverter B2F instead of from the output of the clock comparator itself, to take advantage of a full 5-volt swing. This provides a more consistent hysteresis, thus preventing multiple transitions as the clock comparator input signal passes through 0. Also, at the output of B2F, R30 pulls the inverter output from its normal 3.5 volts up to the 5 volts needed by the feedback circuit. The other two comparators on the board use this same feedback scheme in their operation.

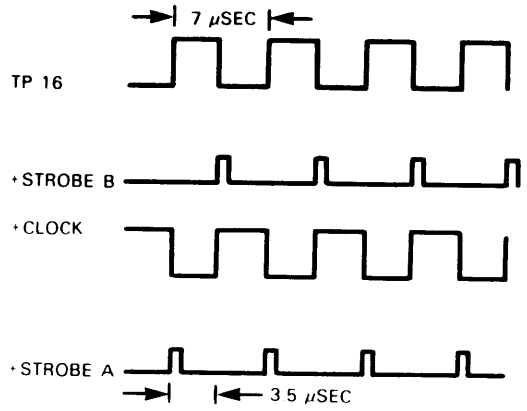


FIGURE B06-4. STROBE PULSE RELATIONSHIPS

Cylinder Count Generation

The output of the cylinder transducer secondary winding is connected to the arm level comparator (D3) and the count comparator (D4). Because of transformer action and the effect of shunt capacitor C10, the output signal from the secondary winding of the cylinder transducer is shifted 90° with respect to the output of the 145-KHz oscillator. This difference in phase allows the strobe pulses to perform their sampling while the output is near peak amplitude (see Figure B06-5).

The cylinder count flip-flop (B1B) must be reset by the signal +Arm before a cylinder count can be generated. Arm level comparator D3 accomplishes this as follows: as the carriage moves, the rack teeth pass by the cylinder transducer and the amplitude of the coupled envelope (as illustrated in Figure B06-3) increases. When the amplitude reaches about 65% of its peak value, the arm level comparator turns on and applies a high level signal to the set input of arm flip-flop B1A. The arm flip-flop is clocked by either the next +Strobe A or +Strobe B, depending on whether the cylinder transducer is coupling a phase A or phase B output. The signal +Arm goes high and is applied to the reset input of the cylinder count flip-flop. It also goes to the set input of the delay count flip-flop (C2B).

Since the count enable flip-flop (C2A) has been set during a previous count, NAND gate B5B-4 is high. The next +Strobe A pulse enables NAND gate B5B, which resets the cylinder count flip-flop via inverter B2C. At the same time, the delay count flip-flop (C2B) sets.

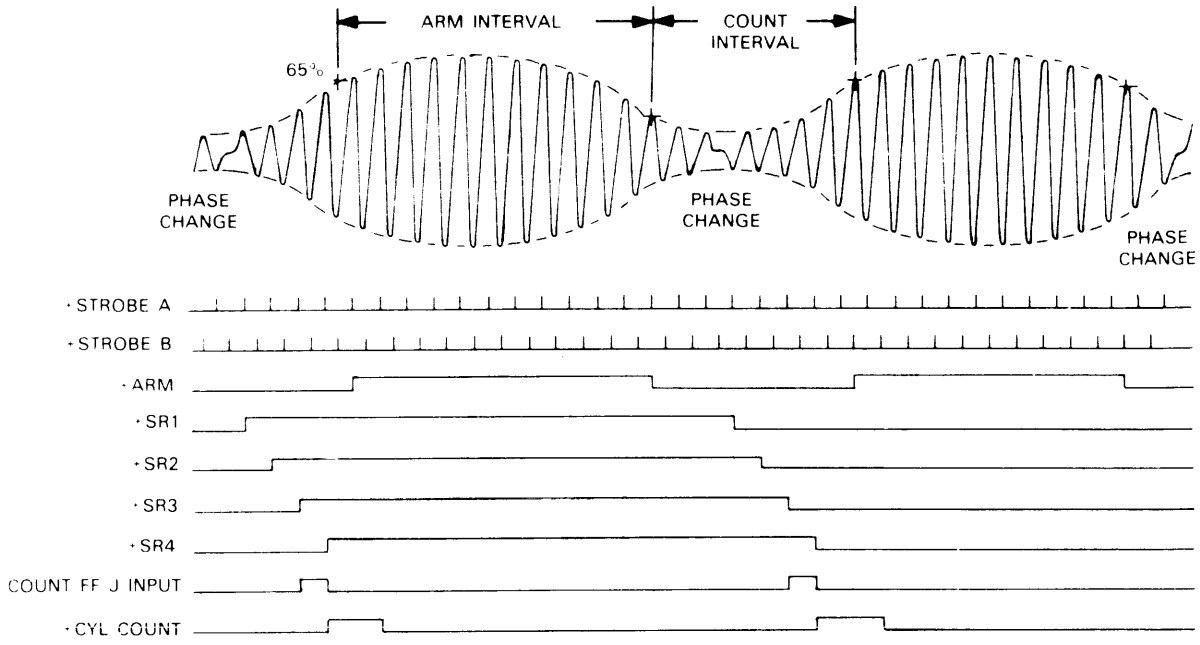


FIGURE B06-5. TRANSDUCER AMPLIFIER TIMING RELATIONSHIPS

The amplitude of the coupled envelope increases to its maximum value and then starts to decrease. When it drops to about 25 mv, the arm level comparator turns off and applies a high level to the reset input of the arm flip-flop. The next strobe pulse resets the arm flip-flop and the signal +Arm goes low. However, cylinder count flip-flop B1B remains reset at this time because its set input is low. The delay flip-flop (C2B) remains set, applying a high level to NAND gate B3B-3.

As the carriage continues moving, the amplitude of the coupled envelope decreases until it reaches a null. At this point, fringe coupling begins taking place across another rack tooth and the phase of the coupled envelope changes 180°.

Since the threshold of the count comparator is near zero volts, its output follows the output of the secondary of the cylinder transducer. Assuming that the circuit has just armed during a phase B tooth and the cylinder transducer is just starting to couple across a phase B tooth, the output of the count comparator during +Strobe A time is low. This low signal is inverted by B2E and applied as a high level to the set input of flip-flop C4A. The +Strobe A signal clocks the flip-flop, setting it. This makes the signal +SR1 high and -SR1 low. The next count comparator output and +Strobe A cause +SR2 to go high and -SR2 to go low, with +SR1 and -SR1 remaining the same. The next count comparator ouput and +Strobe A cause +SR3 to go high and -SR3 to go low, with the previous SR signals remaining the same. NAND gage B4A is now satisfied and its output goes low, enabling NOR gate B4B, which causes NAND gate B3B-5 to go high. At the same time, NAND gate B3C is satisfied, which causes NAND gate B3B-4 to go high, enabling it. The low output of B3B is inverted by B2B and applied as a high level to the set input of the cylinder count flip-flop (B1B). The next +Strobe A clocks the cylinder count flip-flop and the signal +Cyl Count is generated. At this time, flip-flop C3B is set,

causing +S44 to go high and -SR4 to go low. The output of this last flip-flop in the count shift register is used as a memory for the previous phase detected out of the cylinder transducer.

The count shift register will operate in a complementary manner when changing from phase A to phase B outputs. The count shift register, which consists of flip-flops C4A, C4B, C3A, and C3B, serves as a filter to assure that a count signal will only be generated when there is actually a valid change in phase at the transducer output. Any short duration transients will be ignored by this circuit.

As the amplitude of the modulation envelope increases to 65% of its peak amplitude, the arm level comparator turns on and prepares the circuit to generate another Cyl Count signal when the phase changes again.

The exclusive OR circuit formed by NAND gates B3C, B3A, and NOR gate B4C detects a difference in the state of SR4 and SR3 as a phase change regardless of whether the cylinder transducer is moving from a phase A tooth to a phase B tooth or from a phase B tooth to a phase A tooth.

To assure that short-term transients will not cause unwanted inputs to the cylinder count flip-flop, NAND gates B4A, B4D, and NOR gates B4B are included as an exclusive OR circuit at the input of NAND gate B3B. This circuit requires that at the time of a detection of change of phase, the first stage (SR1) of the count shift register be in the same state as that of the third stage (SR3). Thus, any noise present at the count comparator input that is of two clock period's duration or less (14 μsec or less), and which has been shifted down the register as an apparent change of phase, will be ignored because the output of NOR gate B4B will not be high at the required time. However, note that there will be several hundred clock times available for detecting the phase change even at the highest carriage speeds so that any phase change missed because of unwanted noise will still be detected before the cylinder transducer output changes phase again.

If the carriage should continue for a short distance after a compare, and move into the area where the cylinder count flip-flop becomes armed by the increasing envelope amplitude of the next tooth, the count circuitry would generate a cylinder count output when the carriage reversed and moved through a null on its way to the proper detent position. To prevent this invalid count, the signal -Compare is connected to the inputs of NAND gates B3C and B3A to disable NAND gate B3B during a compare condition. Therefore, a Cyl Count signal will not be generated during this condition.

The Restore and Initialization logic, made up of the delay count flip-flop (C2B) and the count enable flip-flop (C2A), is effective only at the beginning of the reverse seek portion of a restore or first seek operation. These two flip-flops are directly reset by the signal -Force Count when the count of 202 is forced into the PAR as the carriage is stationary at its forward stop. The output of the delay count flip-flop (C2B) is connected to NAND gate B3B-3, disabling it until the first Strobe A time after the arm flip-flop is set.

To allow the 203 counts that are detected between the forward carriage stop and cylinder zero to be compatible with the count of 202 which is loaded into the PAR, the clock input to count flip-flop B1B is delayed one full cylinder count by the action of count enable flip-flop (C2A).

Once the first rack tooth is passed on the reverse portion of a restore or first seek operation, both the delay count flip-flop and the count enable flip-flop will be set and stay set until another restore or first seek operation is initiated.

Figure B06-6 shows the restore initialization timing relationships (counting from the carriage stop on a restore operation).

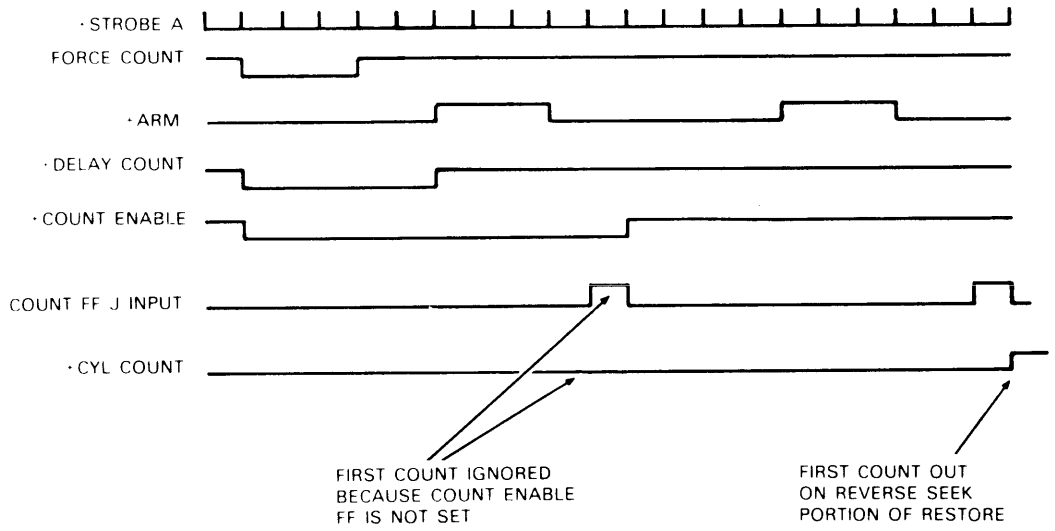


FIGURE B06-6. RESTORE INITIALIZATION

Other Transducer Amplifier Circuitry

The Cylinder Transducer Amplifier board also generates the two timing signals +Clock and -Strobe B, which synchronize the Servo Sequencer logic. The Index Transducer Amplifier is a part of board B06, but is described in the Index/Sector description. Although the AC Fail Detection circuit and the Hi-Low Detection circuit are functionally a part of B06, they are discussed in greater detail in the Power Supply description.

CONTROL SAFETY LOGIC (B07)

The Control Safety logic (PC board B07) receives signals from the controller and from within the drive and decodes them into signals which initiate operations, inhibit operations, and serve as status signals to the controller. The Control Safety logic also decodes any unsafe conditions which might harm recorded data. For instance, trying to read and erase at the same time is considered an unsafe (to the data) condition.

If an unsafe condition is decoded, the Control Safety logic generates a File Unsafe signal to disable the servo and to cause the FILE UNSAFE lamp on the operator control panel to light. The File Unsafe also goes to the controller as a status line. As a result of an unsafe condition, the Control Safety logic generates a Write Inhibit signal which clamps the Write current drivers. This prevents the heads from writing during the unsafe condition.

The Control Safety logic is responsible for decoding the following control signals on the Unit Bus lines from the controller, tag lines from the controller, and various conditioning signals from within the drive.

+Unit Is Selected and -Unit Is Selected

The signal +Unit Is Selected leaves the board on pin 4 and is sent to the controller as a status line to signal the controller that the drive has been selected. The signal -Unit Is Selected leaves the board on pin K and enables the line drivers associated with the CAR and status lines on boards B08 and B09, respectively. For the Unit Is Selected signals to be active, +Select Unit from the controller must be high. Thus, the output of inverter D2C becomes low, generating the signal -Unit Is Selected. Gate C5A inverts this signal, generating the signal +Unit Is Selected. Diode CR1 permits clamping of the +Select Unit line by the -Power Up Reset signal, so that power on and off transients will not activate the line.

-Selected Set Cylinder

This signal leaves the board on pin T and enters the Cylinder/Present Address Register board (A06) on pin 18. It is used to clock the eight D-type flip-flops in the CAR. The signal is derived from the signals +Unit Is Selected (from inverter C5A), +Seek Ready (from the Sevo Sequencer Decode logic), and +Set Cylinder (tag line from the controller). When these inputs are high, NAND gate C5B is enabled and its output goes low, generating the signal -Selected Set Cylinder.

+Selected Set Head

This signal leaves the board on pin S and enters the Head Selection and Register board (A07) on pin K. It is used to enable the direct set inputs of the five head register flip-flops. One or more of the five flip-flops are set by selecting one or more of the five Unit Bus lines which also enable the five gates. The signal is derived from a high +Unit Is Selected (from inverter C5A) and +Set Head (tag line from the controller). When these signals are high, NAND gate C4D is enabled and its output goes low. This output is inverted by C5C to become +Selected Set Head.

-Selected Unit Control

This signal leaves the board on pin 9 and enters the Servo Sequencer Decode board (A04) on pin T. After it is inverted, it serves as the clock input to the Seek Start and Restore flip-flop. The signal is derived from a high +Control (tag line from the controller), +Select Unit (from the controller), +Enable Latch (output of the Enable latch), and -File Unsafe (no unsafe condition exists). When these signals are high, the NAND gate C1A is enabled and it goes low, generating the signal -Selected Unit Control.

-Reset Attention

This signal leaves the board on pin F and enters the Servo Sequencer Decode board (A04) on pin X. It is used to reset the Attention latch. The signal is derived from a high +Unit Bus 1 (bus line from the controller), +Select Unit (tag line from the controller), and +Control (tag line from the controller). When these signals are high, NAND gate D2B is enabled, and its output goes low, generating the signal -Reset Attention. This signal does not require either the Enable latch or File Unsafe to be true.

+Selected Write Gate

This signal leaves the board on pin 15 and enters the Head Selection and Register board (A07) on pin 5. It is used to partially enable the Write (Left) and Write (Right) gates. The signal is derived from a high +Selected Unit Control (output of inverter C4A), +Unit Bus 0 (Select Write Gate), +Select Head (from pin P), and -Read Only (READ/WRITE mode is selected on the READ/WRITE-READ ONLY switch). When these signals are high, NAND gate D3B is enabled and its output goes low. This output is inverted by C4C to become +Selected Write Gate.

+Selected Read Gate

This signal leaves the board on pin W and enters the Head Selection and Register board (A07) on pin 6. It is used partially to enable the Read (Left) and Read (Right) gates. It is derived from a high +Unit Bus 1 (Select Read Gate) and +Selected Unit Control (from inverter C4A). When these signals are high, NAND gate D4D is enabled and its output goes low. This output is inverted by D4C to become +Selected Read Gate.

+Selected Erase Gate

This signal leaves the board on pin 8 and enters the Head Selection and Register board (A07) on pin 4. It is used partially to enable the Erase (Left) and Erase (Right) gates. It is derived from a high -Read Only (READ/WRITE mode is selected on the READ/WRITE-READ ONLY switch), +Select Head (from pin P), +Unit Bus 4 (Select Erase Gate), and +Selected Unit Control (from inverter C4A). When these signals are high, NAND gate D3A is enabled. This output is inverted by D2A to become +Selected Erase Gate.

+Reset Head Reg

This signal leaves the board on pin 17 and enters the Head Selection and Register board (A07) on pin L. After it is inverted, it is used to reset the five head register flip-flops. It can be generated by either of two conditions: (1) when -Force Count (input pin V) is generated by the Servo Sequencer Decode while an address of 202 is forced into the PAR as part of a first seek or restore operation (this means the Head Register is cleared each time a Restore operation occurs), or (2) when NAND gate D4A is enabled by +Selected Unit Control (from inverter C4A) and +Unit Bus 3 (Reset Head Register). This low output is inverted by D4B to become +Reset Head Reg.

+Select Head

This signal leaves the board on pin X and enters the Head Selection and Register board (A07) on pin F. It is used partially enable the outputs of the 2-, 4-, 8-, and 16-bit flip-flops in the head register, causing the head decoding logic to select the head whose address is contained in the register. It is derived from a high +Unit Bus 5 (Select Head) and +Selected Unit Control (from inverter C4A). When these signals are high, NAND gate D5A is enabled and its output goes low. This output is inverted by D5B to become +Select Head.

+Selected Head Advance

This signal leaves the board on pin Y and enters the Head Selection and Register board (A07) on pin 7. It is used to increment the head register, increasing the head register contents by one with each clock pulse. This signal is derived from a high +Unit Bus 7 (Select Head Advance) and +Selected Unit Control (from C4A). When these two signals are high, NAND gate D5D is enabled and its output goes low. This output is inverted by D5G to become +Selected Head Advance.

In addition to generating the above control signals, the Control Safety logic generates File Unsafe signals if any of ten separate file unsafe conditions occur. Each unsafe condition or combination of conditions has a latch for storing occurrences of the condition. The outputs of these latches are applied to a 10-input NOR gate structure, which generates the signal +File Unsafe.

The conditions capable of setting each of the ten unsafe condition latches are explained in the paragraphs below. The latches corresponding to the first four conditions are designed with an RC network on the set output so that the latches are insensitive to short-term occurrences of the specified condition. These short-term conditions may occur in normal operation due to unavoidable time delays in the write and erase circuits.

No AC Write (Test Point 1)

If the write gates in the Head Selection and Register logic have been selected, but no voltage changes at the write current driver output are detected, a File Unsafe condition exists. When this occurs, the signal +Selected Write Gate at the output of inverter C4C is high and -AC Write (Sense) entering the board on pin N is also high. These two high signals enable NAND gate B5C and its output goes low. This low signal sets the No AC Write latch C3B/B3A and the signal No AC Write goes low. This low signal enables NOR gate A3A whose output goes high. This high output is inverted by A2D and enables NOR gate B2B, generating the signal +File Unsafe. Each time a +File Unsafe is generated, it is inverted by B1C and B1B to become -File Unsafe and -Write Inhibit, respectively.

No Erase I (Test Point 2)

If the write gates in the Head Selection and Register logic have been selected, but no erase current is being applied to the erase coils, a File Unsafe condition exits. When this occurs, the signal +Selected Write Gate at the output of C4C is high and the signal -Erase I (Sense) entering the board on pin 11 is high. These high signals enable NAND gate B5A, and its output goes low setting the No Erase I latch C3A/B3B. This low signal enables NOR gate A3A, which causes the output of NOR gate B2B to go high, generating the signal +File Unsafe.

Erase Select Error (Test Point 3)

If erase current is being applied to the erase coils, but the erase gates in the Head Selection and Register logic have not been selected, a File Unsafe condition exists. When this occurs, the output of NAND gate D3A is high, partially enabling NAND gate B5B. (Note that the output of NAND gate D3A, when inverted by D2A, becomes +Selected Erase Gate.) At the same time, the output of inverter B5D is high because the signal -Erase I (Sense) entering the board on pin 11 is low. Thus, NAND gate B5B is enabled and its low output sets the Erase Select Error latch C3D/B3C. The signal Erase Select Error enables NOR gate A3A, which causes the output of NOR gate B2B to go high, generating the signal +File Unsafe.

Write Select Error (Test Point 4)

If write current is being applied to the write coils, but the write gates in the Head Selection and Register logic have not been selected, a File Unsafe condition exists. When this occurs, the output of NAND gate D3B is high, partially enabling NAND gate A2B. (Note that the output of NAND gate D3B, when inverted by C4C, becomes +Selected Write Gate.) At the same time, the output of NAND gate A2A is high because the signal -Write I (Sense) entering the board on pin L is low. Thus, NAND gate A2B is enabled and its low output sets the Write Select Error latch C3C/B3D. The signal Write Select Error enables NOR gate A3A, which causes the output of NOR gate B2B to go high, generating the signal +File Unsafe.

Erase and Not Ready (Test Point 5)

If the erase gates in the Head Selection and Register logic have been selected, but the drive is not ready to seek, a File Unsafe condition exists. When this occurs, the signal +Selected Erase Gate at the output of gate D2A is high, partially enabling NAND gate A5C. If the drive is not ready to seek, the signal +Seek Ready, which enters the board on pin 16, is low. This signal is inverted by C4B and enables NAND gate A5C. The output of A5C goes low and sets the Erase and Not Ready latch B4C/B4B. The signal Erase and Not Ready goes low and enables NOR gate A3B, which causes the output of NOR gate B2B to go high, generating the signal +File Unsafe.

Write and Not Ready (Test Point 6)

If the write gates in the Head Selection and Register logic have been selected, but the drive is not ready to seek, a File Unsafe condition exists. When this occurs, the signal +Selected Write Gate at the output of inverter C4C is high, partially enabling NAND gate A5D. If the drive is not ready to seek, the signal +Seek Ready, which enters the board on pin 16, is low. This signal is inverted by gate C4B and enables NAND gate A5D. The output of A5D goes low and sets the Write and Not Ready latch B4D/B4A. The signal Write and Not Ready goes low and enables NOR gate A3B, which causes the output of NOR gate B2B to go high, generating the signal +File Unsafe.

Erase and Read (Test Point 7)

If the erase gates and the read gates in the Head Selection and Register logic have been selected simultaneously, a File Unsafe condition exists. When this occurs, the signal +Selected Read Gate at the output of inverter D4C is high, partially enabling NAND gate A5B. At the same time, the signal +Selected Erase Gate at the output of inverter D2A is also high. Thus, NAND gate A5B is enabled and its low outputs sets the Erase and Read latch A4C/A4B. The signal Erase and Read goes low and enables NOR gate A3B, which causes the output of NOR gate B2B to go high, generating the signal +File Unsafe.

Write and Read (Test Point 8)

If the write gates and the read gates in the Head Selection and Register logic have been selected simultaneously, a File Unsafe condition exists. When this occurs, the signal +Selected Write Gate at the output of inverter C4C is high, partially enabling NAND gate A5A. At the same time, the signal +Selected Read Gate at the output of inverter D4C is also high. Thus, NAND gate A5A is enabled, and its low output sets the Write and Read latch A4D/A4A. The signal Write and Read goes low and enables NOR gate A3B, which causes the output of NOR gate B2B to go high, generating the signal +File Unsafe.

System Unsafe (Test Point 9)

If the servo driver or the linear motor bobbin overheats, or if a circuit failure is detected on the System Protection board, a File Unsafe condition exists. When this occurs, the signal System Unsafe, which enters the board on pin 10, goes low and sets the System Unsafe latch C2D/C2A. The output of the latch goes low and enables NOR gate B2B, generating the Signal +File Unsafe.

Head Select Error (Test Point 10)

If any of the conditions that constitute a head select error occur (see Head Selection and Register description), a File Unsafe condition exists. When this occurs, the signal -Head Select Error, which enters the board on pin E, goes low and sets the Head Select Error latch C2C/C2B. The output of the latch goes low and enables NOR gate B2B, generating the signal +File Unsafe.

The ten unsafe condition latches are reset simultaneously by the signal Reset Unsafe, which comes from inverter B2A. This signal can be generated by any of three conditions. When the signal +Seek Enable (entering the board on pin 22) is low, it enables NOR gate B1A, which causes the output of inverter B2A (Reset Unsafe) to go low. The second condition for generating a Reset Unsafe signal is the grounding of the -CE Reset line. This is accomplished by either grounding pin 18 or by pressing the CE Reset button (S1). This action will also enable NOR gate B1A, which causes the output of inverter B2A (Reset Unsafe) to go low. The third method of generating a Reset Unsafe signal is by enabling NAND gate D1B (Diagnostic Reset). To enable this NAND gate, the signals +Unit Bus 1 (Select Read Gate), +Select Unit (tag line from the controller), and +Control (tag line from the controller) must all be high, enabling NAND gate D1C. The low output of NAND gate D1C is inverted by D1A, which partially enables NAND gate D1B. The signals +Index and +Unit Bus 3 must also be high to enable NAND gate D1B completely. When D1B is enabled, its low output enables NOR gate B1A, which causes the output of inverter B2A (Reset Unsafe) to go low, resetting the ten unsafe condition latches.

It may be desirable to disable the File Unsafe logic while diagnosing a field problem. There are two ways to accomplish this. Jumpering pin 18 to ground will hold all latches reset and cause the file to ignore any unsafe condition which may occur. The second method consists of jumpering pin B to ground. This is probably the more useful technique since it allows any unsafe condition which may occur to set the appropriate latch, but prevents the +File Unsafe signal from affecting other drive circuits. Be certain to remove this jumper when service is completed so that the safety circuits are again active.

LINE DRIVERS (B08 & B09)

Line drivers are used to transmit signals between the drive and the controller.

Since all line drivers on B08 and B09 are basically the same, only one circuit is described in detail—the line driver on board B08 which transmits the signal, CAR 128.

When a drive has been selected, the signal -Unit Selected, entering the board on pin 14, goes low. This low input is inverted by B3C and partially enables NAND gate B4C. When the signal +CAR 128 becomes active, it goes high and enables NAND gate B4C. Transistor circuit Q1/Q2 activates its output going low, thus enabling the signal Cylinder Address Register 128.

The cathode side of diode CR1 is connected to the signal -Power Up Reset. If -Power Up Reset goes active (low), the top eight-line NAND gates are disabled to prevent intermittent status line conditions during AC power up or power down, while other in-line drives are in use.

LINE RECEIVERS (B10)

The line receivers on B10 consist of fourteen line receiver amplifier circuits. The ten receivers at the top of the print are similar and provide active outputs. The eleventh receiver down from the top of the print has NORed inputs and is not used at the present time. The remaining three circuits (at the bottom of the page) have their outputs applied to logic gates and a delay circuit to inhibit noise.

The top ten line receivers are basically the same and all operate the same as the one whose input is connected to pin 16. For example, if the signal Unit Bus 4 goes active (low), the output of the line receiver goes high, enabling the signal +Unit Bus 4.

Since the three line receivers at the bottom of the page are similar, only one circuit will be described in detail—the line receiver and its associated circuitry that receives the signal Control from the controller. When the signal Control goes active (low), the output of the line receiver connected to pin E also goes low. This low signal partially enables NAND gate D1D. The low output of the line receiver also goes to NOR gate A1C enabling it. The output of A1C is inverted and enables NOR gate A1D which starts the 300-nsec-delay noise-inhibit circuit. After 300 nsec the output of the noise-inhibit circuit goes low and enables NAND gate D1D whose output is the signal +Control.

If a noise spike is picked up by the Control signal line (noise spikes are typically less than 300 nsec in duration), the inputs of gate D1D are not satisfied and the signal +Control does not go active.

SERVO DRIVER (C01)

The Servo Driver is a current driver of a power bridge design. The forward half of the bridge is activated by the positive-going Programmed Current signal from the Error Amplifier on the B04 card, while the reverse half is activated by the negative-going voltage. The function of these current amplifiers is to convert the output voltage of the Error Amplifier into properly proportioned forward or reverse currents which drive the linear motor.

Operational amplifier 1A amplifies the positive portion of the Error Amplifier output to turn Q4 on. The collector of Q4 output drives the base of Q3 in order for its collector to have enough current to drive the upper part of the Power Bridge (Q6 and Q7). The emitter of Q4 drives the lower part of the Power Bridge (Q3 and Q4). The path of current flow is thus completed—Linear Motor current flows through Q7, the linear motor itself, Q4, and feedback resistor R5. Feedback current is provided from R5 to 1A. Operational amplifier 2A is in a low-gain mode at this time, due to diode CR1 clamping its output at a diode voltage below the input which is virtually zero.

When Q9 is turned on by Q4, its collector current turns Q12 on to clamp the output of amplifier 2A near 0 volt to make sure the other side of the bridge is off. When the error voltage crosses zero to a negative voltage, Q9 turns off and C14 discharges to keep Q12 from turning off or amplifier 2A from turning on until Q4 and Q7 are off. This creates a small dead zone near 0 volt to assure that both sides of the driver are not on simultaneously.

The other half of the bridge works exactly like the previous case, except amplifier 2A amplifies a negative input and amplifier 1A clamps on a negative signal by diode CR6.

The Servo Driver can be disabled in the event of certain unsafe conditions such as after the heads have retracted or a seek incomplete status. These conditions activate a transistor switch which clamps both sides of the Servo Driver to ground (approximately +0.8 volt) to cut off motor current. The Servo Driver is disabled by logic signals, +Servo Disable or +Emergency Retract • -Heads Retracted Sw. This is done by applying a +Servo Disable signal to CR13 or +Emergency Retract to R23 and -Head Retracted Sw to the cathode of CR12, thus turning Q5 on and shunting the outputs of op amps 1A and 2A (see schematic). Q14 disables the servo when loss of -15 V has retracted the heads and -Heads Retracted Sw is low. Q14 draws current from R21 to turn Q6 and Q7 on, thus disabling the servo.

Another function of this card is to provide a logic signal (+High Power Rate) to the Servo Sequencing logic indicating that the maximum permissible bobbin temperature has been reached. Exceeding this temperature could cause irreparable damage to the bobbin. The +High Power Rate circuit consists of integrator 3A and voltage comparator 4A. 3A integrates the current through the bobbin (thus power) and provides a voltage output proportional to the rise in bobbin temperature (13°F per volt). 4A is referenced to generate a +High Power Rate signal at 11. 5 volts. When this signal is true, the delay between seeks is increased by an additional 28 msec.

ACTUATOR DRIVER (C04)

The detent actuator consists of a permanent horseshoe magnet with a ferromagnetic reed in the gap between poles. The base of the reed is stationary, but the reed is flexible enough for its top to bend from one permanent magnet pole to the other. Two coils are wrapped in opposite directions around the reed. When current is sent through one coil, the reed is polarized in one direction and the top of the reed is attracted to one permanent magnet pole. Current applied to the other coil reverses polarity in the reed so that it transfers to the other permanent magnet pole.

When the reed moves toward one pole (because of current in the coil), it pushes a plunger rod. In turn, this rod pushes against one end of the detent pawls, causing them to pick (disengage from the detent rack). When the reed transfers to the other pole (because of current in the other coil), it releases the plunger rod. With no pressure against the plunger rod, the spring-loaded detent pawls set (engage with the detent rack).

The Actuator Driver logic is responsible for providing the required amount of current to one of the two actuator reed coils in order to either pick or set the detent pawls.

Normal Seek

In the following discussion, it is assumed that the drive is about to perform a normal seek; the detent pawl is set, the signal +Detent at pin M is high, and there is no current flowing in either actuator coil. As a result of the last set operation, the reed is against the set pole of the permanent magnet, applying no force to the plunger rod.

Pick

When +Detent goes low in preparation for a seek operation, it applies a low to the base of Q8, turning it off. With Q8 off, the base of Q9 goes high, turning that transistor on. With Q9 on, the base of Q17 goes high and that transistor turns on. This supplies current to the pick coil.

NOTE

Q17, the pick transistor; Q18, the holding current driver; and Q19, the set transistor are located on the heat sink No. 4 and not on the Actuator Driver board.

This current reverses the polarity of the actuator reed so that it transfers to the pick pole of the permanent magnet. As the reed transfers, it pushes the plunger rod against the detent pawls, causing them to disengage from the rack. As the current increases through Q17 and the pick coil, a positive voltage develops across R18. This slight positive bias is coupled to driver amplifier Q8/Q9, restricting the current flow through it which, in turn, limits the current through Q17 and the pick coil to a desired value.

The low +Detent signal also turns off driver amplifier Q10 Q11, driving the base of Q18 high, turning it on. This provides holding current to the pick coil for as long as +Detent remains low. Holding current keeps the actuator reed in the pick position to assure that the detents stay picked throughout the seek operation.

Since holding current is sufficient to keep the actuator reed in the pick position once it has completed the transfer, pick current is maintained only long enough to assure that the detent pawls are picked. The 2.0-msec one-shot (Q3, Q5, Q6, and Q7) holds the pick for 2.0 msec and then the current is dropped. During the 2.0 msec, there is both pick current and holding current in the pick coil. For the remainder of the seek, there is only holding current in the pick coil.

Set

Until the carriage reaches the target cylinder and the Adder and Speed Decode board recognizes a compare condition, +Detent remains low.

When the target cylinder is reached and the signal +Detent goes high, the 2.0-msec one-shot (Q12, Q13, and Q14) begins timing out. At the same time, CR4 is back biased and turns off. This causes driver amplifier Q15/Q16 to turn on, which causes the base of the set coil drive transistor (Q19) to go high, turning it on. Current begins flowing in the set coil and the reed swings to the set pole piece. This releases the plunger rod, allowing the spring-loaded detent pawl to engage. As the current increases through Q19 and the set coil, a positive voltage is developed across R36, which limits the current through Q19 and the set coil to a desired value.

During the 2.0-msec charge time, current flowing through Q19 flows in the set coil. When the 2.0-msec one-shot times out, the set coil current is removed. The attraction of the set pole piece to the permanent magnet holds the reed in the set position until current is generated in the pick coil.

Special Conditions

Additional current is supplied in the pick coil to pick the detent pawls before a first seek.

This is done because, before a first seek, the carriage is retracted. This means the detent pawl teeth are not resting against the detent rack and the pawls are pivoted further in the set direction than they are when the carriage is not retracted. Consequently, the backs of the pawls are pushing the plunger rod back against the actuator reed. At other times, when the carriage is not retracted, there is no force against the actuator reed other than the attraction of the set pole to the permanent magnet. The reed is able to develop momentum before it has to overcome the spring load on the detent pawls. However, before a first seek, this load resists the actuator reed from the start, requiring more current in the pick coil to complete the reed transfer in the time required.

This extra current is generated whenever the signal +CAR/PAR Reset (entering the board on pin 12) is high. This high turns inverter Q17 on, shunting some of the base current from the driver amplifier (Q8/Q9) during the 2.0-msec pick-drive pulse. This decreases the current limiting influence of Q8 on Q9, allowing more current to flow through pick transistor Q17 and the pick coil.

When a Restore operation is initiated, the signal +Pick at pin 17 goes high to assure that a new 2.0-msec pick-drive pulse is generated.

The high on pin 17 turns on Q4, which causes the 2.0-msec one-shot (Q3, Q5, Q6, and Q7) to begin timing out. This, in turn, allows the driver amplifier (Q8/Q9) and transistor Q17 to conduct. As a result, current is supplied to the pick coil and the detent pawls disengage. After 2.0 msec, current is removed from the pick coil.

READ/WRITE AMPLIFIERS

Because the Read/Write Amplifier (Left) is a mirror image of the Read/Write Amplifier (Right), only Read/Write Amplifier (Right) will be discussed.

The write data which was sent out from pins 4 and 3 of the Write logic enters the Read/Write Amp (Right) at pins B and C, respectively. This data is routed to the appropriate gating diodes to the selected head. Which head is selected depends on which Line Select signal is active. The data is written onto the disc surface facing the selected head.

The same head selection technique is used for reading as is used for writing. On the Read/Write Amplifier (right) board, the signal from the head is coupled through diode gates CR36 through CR39. The state of these diodes is determined by the read select transistors Q13 and Q14. When Q13 and Q14 are turned on, the diode gates (CR 36 through CR39) are energized allowing the signal from the selected head to pass into the Preamplifier. The signal +Read Driver (Right), which enters the RWAR board on pin 13, controls the state of Q13 and Q14.

READ PREAMPLIFIERS

Since both Read Preamp (Left) and Read Preamp (Right) are identical, only Read Preamp (Right) will be discussed in detail. Both preamps are mounted (with standoffs) on their respective Read/Write Amplifier boards.

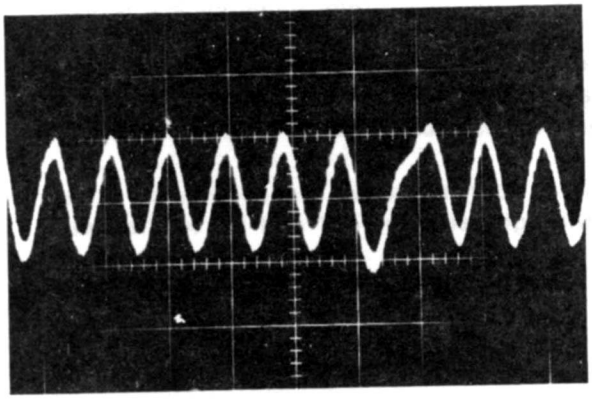
The signal read off of the selected head enters terminals E1 and E2 on the Read Preamp board. The signal is then routed to emitter followers Q1/Q3. Transistors Q1/Q3 provide a high input impedance for the circuit. The output of the first differential amplifier is amplified by differential amplifier Q2/Q4. Current feedback, provided by C3 and R7, reduces stage gain but increases bandwidth. Transistors Q5/Q6 are constant current sources for Q2/Q3, respectively. The outputs of the differential amplifier are further amplified by two more differential amplifiers consisting of Q7/Q8 and Q9/Q10. Capacitor C6, between the collectors of Q7 and Q8, limits the upper frequency response of the stage. Note that the values of R19 and C7 in the next amplification stage are selected to differentiate the signal and convert the peaks of the signal to zero crossings.

The output of Q9 and Q10 is applied via a four-transistor low-impedance driver (consisting of Q11, Q12, Q13, and Q14) through terminals E3 and E7 to the Read Amplifier as the signal Read Preamp Output (Right).

Read Preamplifier PC Board Waveform Notations

Eight scope photographs of waveforms taken at various points in the signal flow path of the read preamplifier are shown on this and the next page. A hexadecimal EF data pattern is used to show the effects of a single logical zero in the midst of a pattern of logical ones. The oscilloscope sweep rate is adjusted to approximately 2.2 μsec/division, and all measurements are taken differentially as shown on the applicable logic diagram.

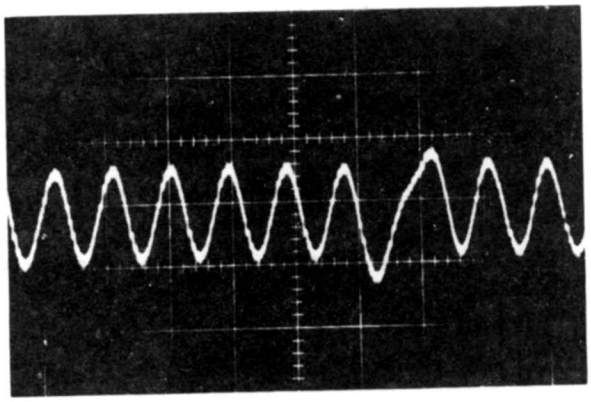
Note that photographs E and F show the read signal after differentiation by C7 and associated components.



A

TEST POINTS E1 AND E2

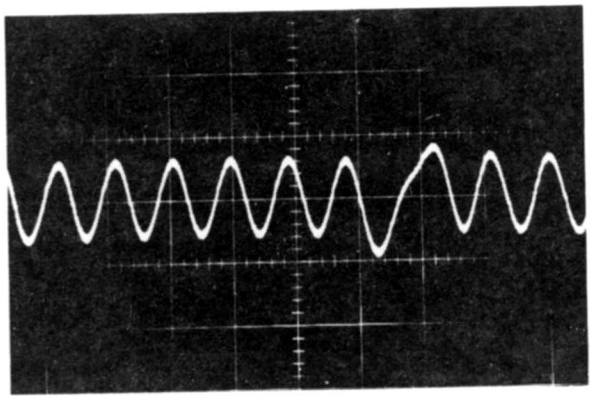
5 millivolts/division



B

Q1 AND Q3 EMITTERS

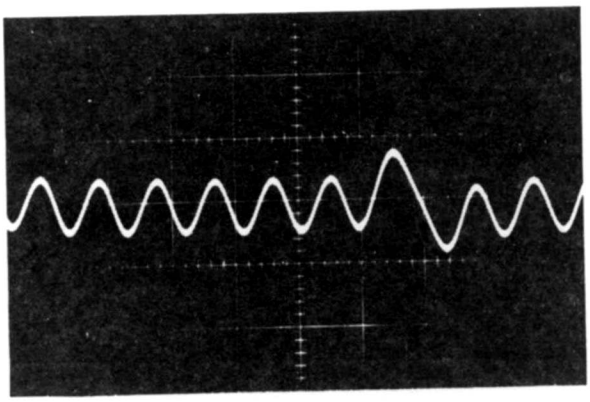
5 millivolts/division



C

Q2 AND Q4 COLLECTORS

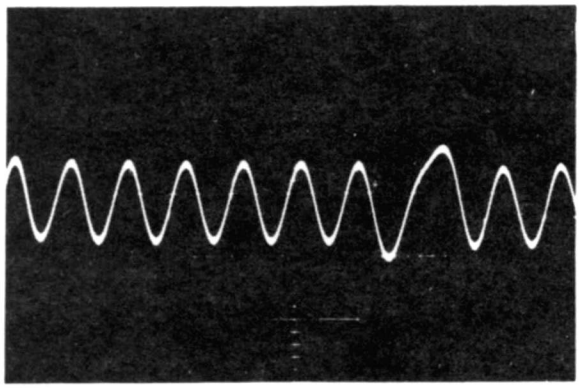
20 millivolts/division



D

Q7 AND Q8 COLLECTORS

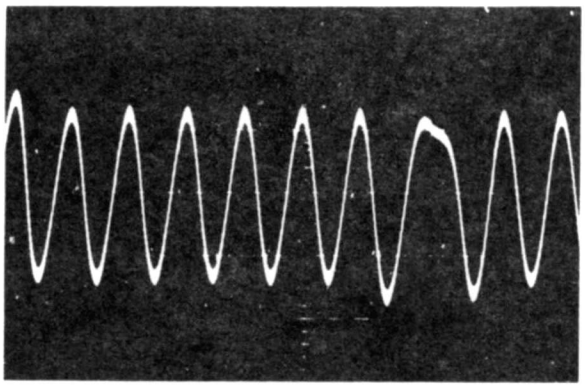
20 millivolts/division



E

Q9 AND Q10 COLLECTORS

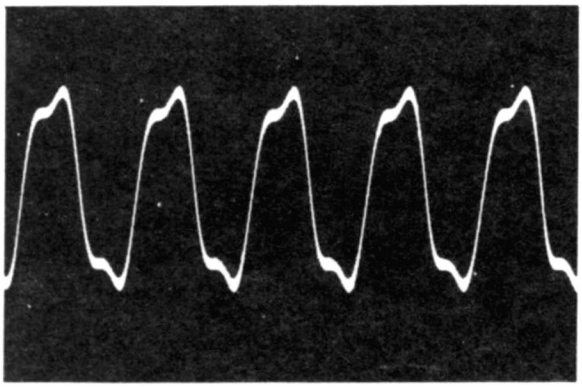
20 millivolts/division



F

TEST POINTS E3 AND E7

100 millivolts/division

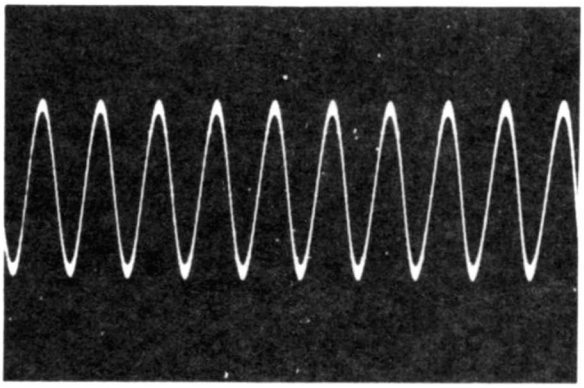


G

1F DATA PATTERN

100 millivolts/division

Input to preamplifier is
17 millivolts peak to peak



H

2F DATA PATTERN

100 millivolts/division

Input to preamplifier is
12 millivolts peak to peak

For comparison, photographs G and H show the preamplifier output for constant 1F and 2F patterns (all zeros and ones).

POWER SUPPLIES

The disc storage drive receives its primary AC power from the controller or, if in a string of drives, it receives its AC power from the previous drive in the string.

The three-phase primary AC voltage enters the drive at J1 (the AC IN connector) on the interior control panel. In addition to supplying primary AC power for the machine, these three voltage lines are directly connected to J2 (AC OUT connector) where they supply primary power to the next drive in a string of drives.

Within the drive, two of the three primary power lines are connected to the arms of S1, the DPST Power ON-OFF switch, which is also located on the interior control panel. Phases are rotated between drives to minimize the load on each of the available phases.

In addition to the primary power lines, 115-vac lines enter J1 to provide voltage at two convenience outlets. This power is also routed to J2 to supply convenience outlet voltage to the next drive in the string. Chassis ground also enters the drive at J1 and leaves it at J2 for the next drive in the string of drives.

The drive provides its own DC power. This is regulated in two stages. The first regulation occurs at the main power transformer, T1. This is ferroresonant and is capable of 3% to 5% line-load regulation. The +5-, ±15-, and ±36-DC voltages are further regulated by solid state series regulators as needed by both the logic and analog circuits.

The relays and lamps are powered by +24 RAC, which is rectified and filtered off T1, but not regulated. It does have the benefits of the transformer regulation, however.

Another voltage that is not regulated is +55 vdc. It is used by the linear motor servo, drive motor braking circuit, and the detent actuator. This voltage is taken from across a large capacitor (C3) to provide the large, short-term surges of current required to accelerate the linear motor and to provide adequate energy storage to retract the heads from the pack in case of an AC power failure.

Basic Operation

For the following description use the Primary AC Power schematic diagram 201055, the DC Power Distribution schematic diagram 201113, and the Actuator Driver schematic diagram 001972.

When S1, the Power Switch on the Primary AC Power schematic is turned ON, the primary power is routed through fuses F1 and F2 and line filters FL1 and FL2 to pins 1 and 3 of J9. It is then applied to the input of the power transformer T1. The secondary outputs (approximate clipped sine waves because of the ferroresonant action) are rectified to supply voltages for the generation of various regulated DC voltages used throughout the drive. This AC input voltage to T1 is also applied to the power supply fans B4 and B5 and the logic fan B3. These fans begin rotating as soon as the power switch is turned on.

The output of the secondary windings (pin 6 and pin 8) is bridge rectified by CR4 to become +24 RAC at the right side of fuse F7. This rectified AC voltage is connected to S4, the Pack On switch, via pin 11 of J23. It is further filtered by capacitors C6 and C7 (after passing through isolating diode CR5) and supplies voltage to the ±15-volt regulator on C02. Assuming the Pack On switch is closed (a disc pack is on the spindle), +24 RAC is routed from S4 via J23 pin 10 and J24 pin 13 to pin 13 of J10 on the Primary AC Power schematic. This voltage is then applied to one side of both relay coils of K1 and K2. The other sides of K1 and K2 are connected to pin 12 of J10 which is routed to the Relay Driver (-K1/K2 Pick) on the Power-Up Sequencing and Control board. If -K1/K2 Pick is active (see Power-Up Sequencing and Control logic description), K1 and K2 coils are energized. At this time the contacts of K2 apply the primary power to the disc motor (spindle drive motor) and the disc pack spindle begins rotating. At the same time, two sets of contacts on K1 apply the primary power to the blower motor and it begins cooling the interior of the drive. Another set of K1 contacts connect to 24 volts AC (24 VAC) which comes from pin 6 of T1, on the DC Power Distribution schematic. The other side of these contacts go to Elapsed Time Meter M1, whose contacts are shown on the DC Power Distribution schematic (pin 8 of J23). The other side of M1 is connected to pin 7 of T1 to complete the circuit. M1 begins counting elapsed time.

All during this time the regulators on C02 and C03, shown as large boxes on the DC Power Distribution schematic, supply various regulated DC voltaged used throughout the drive.

When the START/STOP switch on the Operator Control Panel is placed in the STOP position, a DC dynamic-braking voltage is applied to the disc motor (spindle drive motor) as follows. When the STOP position is selected, -K1/K2 Pick goes inactive and the arms of K2 switch to the upper contacts as shown on the Primary AC Power schematic. The heads retract, the elapsed time meter stops, and the DC signal -12-Sec Dynamic Braking is applied to pin B on the Actuator Driver schematic diagram. Transistors Q1 and Q2 turn on, causing Q13 and Q14 to turn on. Transistors Q13 and Q14 (also shown on the DC Power Distribution schematic diagram in addition to being shown on the Actuator Driver schematic diagram), supply a ground path for the +55-volt supply, which is used to bring the disc motor to a stop within 12 seconds.

±15-Volt Supply (Main)

The ±15-volt power supply is located on board C02. For the following description use the ±15V and 5V Power Supply schematic diagram 001912.

A closed-loop regulator design is used in both the +15- and -15-volt supplies. The +15-volt regulator is shown above the ground line on the schematic; the -15-volt regulator is shown below the ground line. Because the -15-volt regulator is basically a mirror image of the +15-volt regulator, only the +15-volt regulator willl be described.

The reference voltage for the +15-volt regulator is developed across the zener diode CR1, whose operating voltage is derived through R6, which is connected to the +15-volt regulated output line. The slightly positive temperature coefficient of CR1 is cancelled by the negative temperature coefficient of the base-to-emitter voltage of the error amplifier Q3. The current through Q3 determines the voltage drop across R2 and R1 which allows just enough current to reach the base of the pass element (Q15 of the Q1/Q15 Darlington pair) to support the total load current requirement while delivering the desired voltage output. This total load current flows through the emitter of Q15 and the resistor R4.

Completing the loop, a sample of the output voltage is taken at potentiometer R8 and applied to the base of Q3. This sample of voltage (approximately 7.5 volts) determines the exact voltage delivered by the supply.

If the load current increases significantly (such as during a short circuit on the +15-volt line), the voltage drop across R4 increases, causing Q2 to conduct more heavily. The increased collector current of Q2 causes R2 and R1 to drop a larger voltage which reduces the conduction of Q1 and Q15, thus limiting the load current to a safe value without damaging the pass transistor Q15.

+5-Volt Supply

The +5-volt supply is located on board C02. For the following description use the ±15V and 5V Power Supply schematic diagram 001912. The +5-volt supply is on the lower portion of the schematic.

The regulator used in the +5-volt supply is of the closed-loop variety. The zener diode CR3, which derives its operating voltage from the +15-volt supply via R21, feeds a voltage divider R22, R23 which holds the base of Q9 at a constant voltage level. The voltage at the collector of Q10 (base of Q8) allows the proper current to reach the base of the pass elements Q11 and Q12 in order to conduct the load current while delivering the desired voltage at the output. The load current flows through the resistive network consisting of R26, R27, and R28, which is in series with the pass elements.

A sample of the output voltage is taken at R31 (approximately 2.5 volts) and applied to the base of Q10. This sample of voltage determines the exact voltage delivered by the supply and can be adjusted with R31.

As the load increases (such as during a short circuit on the +5-volt line), the voltage drop across the resistive network R26, R27, and R28 increases, causing Q7 to conduct more heavily. With Q7 conducting heavily, a lower voltage is placed on the base of Q8 reducing its conduction which, in turn, reduces the conduction of Q11 and Q12, thus limiting the load current to a safe value without damaging the pass elements Q11 and Q12.

±36-Volt Supply

The ±36-volt power supply is located on board C03. For the following description use the 36V Power Supply/AC Power Fail schematic diagram.

A closed loop regulator design is used in both the +36- and the -36-volt supplies. The +36-volt regulator is shown above the ground line on the schematic; the -36-volt regulator is shown below the ground line. Because the -36-volt regulator is basically a mirror image of the +36-volt regulator, only the +36-volt regulator is described.

The reference voltage for the +36-volt regulator is developed across the zener diode CR1, whose operating voltage is derived from the +36-volt output line via R6. The slightly positive temperature coefficient of CR1 is cancelled by the negative temperature coefficient of the base to emitter voltage of error amplifier Q3. The current through Q3 determines the voltage drop across R2 and R1 which allows just enough current to reach the base of the pass element (Q20 of the Q1/Q20 Darlington pair) to support the total load current requirement while delivering the desired voltage output. This total load current flows through the emitter of Q20 and resistor R4.

Completing the loop, a sample of the output voltage is applied to the base of Q3 via R7 and R8. This sample voltage (approximately 7.5 volts) determines the exact voltage delivered by the supply.

If the load current increases significantly, the voltage drop across R4 increases, causing Q2 to conduct more heavily. The increased collector current of Q2 causes a larger voltage drop across R1 and R2, which reduces the conduction of Q1 and Q20, thus limiting the load current to a safe value without damaging pass transistor Q20.

AC Fail Detection

The AC Fail Detection circuit is located on board C03. For the following description, use the 36V Power Supply/AC Power Fail schematic diagram. The AC Fail Detection circuit is shown in the lower portion of the schematic.

The AC Fail Detection circuit uses a differential amplifier to compare a known DC voltage with a rectified AC voltage derived from the main power transformer (T1). If the AC voltage fails, an Emergency Retract signal is generated to retract the heads so that the disc will not be damaged while the spindle drive motor coasts to a stop.

The reference voltage for the reference side of the differential amplifier (Q7/Q8) is developed across zener diode CR7, whose operating voltage is derived from the +55V Power Supply via R23. Although the input to the 55-volt supply is derived from transformer T1, failure of the primary AC input circuit will not immediately cut off this supply. This is because of the discharge action of a large filter capacitor (C3 on DC Power Distribution schematic diagram) which is connected across the input. The resistive divider network of R24-R25 holds the base of Q7 at a constant 3.4 volts.

The AC voltage for the AC detection side of the differential amplifier (Q7/Q8) comes from pins 5 and 9 of primary power transformer T1 (refer to the DC Power Distribution schematic diagram). These pins are routed to C03, pins 6 and 8, where the AC voltage is applied to a full-wave rectifier (diodes CR3 and CR8). Capacitor C12 provides a time constant of several cycles of AC. Zener diode CR5 and resistor R22 cause the voltage at the top of R28 to be high enough to turn Q8 on. With Q8 on, Q7 turns off when AC is present on T1. The high voltage at the collector of Q7 causes Q9 to turn off, which keeps the output line at pin P (+Emergency Retract) low while AC is present on transformer T1.

If the primary AC voltage is removed (by a power failure or if the main power switch (S1) on the interior control panel is turned off), the voltage is removed from the base of Q8, turning it off. The +55 volts at pin 7 remains for several seconds after the AC power is removed and Q7 turns on. The low voltage at the collector of Q7 turns on Q9, which passes DC current to generate the signal +Emergency Retract. The signal +Emergency Retract causes the heads to retract. Figure PS-1 shows the decaying voltage on capacitor C12 after AC power is removed from the drive. The effect of the 5V undervoltage detector is not shown in this figure, but it will also operate (at some undetermined time after AC power is removed) to generate an Emergency Retract signal.

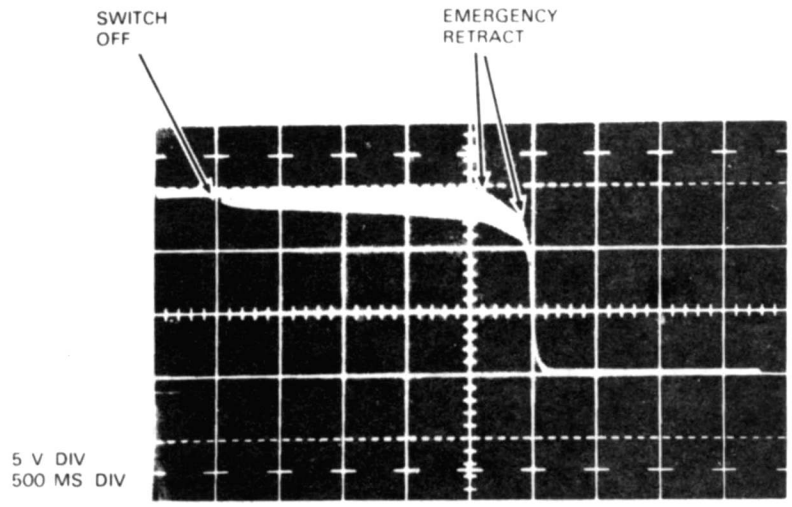


FIGURE PS-1. C12 DECAY VOLTAGE

±15-Volt Supply (Servo)

The ±15-volt servo power supply is located on the Servo Driver board C01. For the following description use the Servo Driver schematic diagram 001752. The ±15-volt servo power supply is shown on the lower portion of the schematic. Because the -15-volt regulator is basically a mirror image of the +15-volt regulator, only the +15-volt regulator is described.

The reference voltage for this regulator is developed across zener diode CR9, whose operating voltage is derived through R37, which is connected to the +15-volt servo voltage output line. The cathode of CR9 is connected to the emitter of Q8, whose collector current determines the voltage drop across R34 and R31. This voltage drop allows just enough bias on the pass transistor's (Q5) base to support the total load current requirement while delivering the desired voltage output. This total load current flows through the emitter of Q5 and resistor R33.

The output voltage is sampled by the base of Q8 via the potentiometer R40. This sample of voltage (approximately 7.5 volts) determines the exact voltage delivered by the supply.

If the load current increases, tending to decrease the output voltage, the voltage drop across R33 increases, thus placing the base of Q5 at a more positive voltage with respect to its emitter, causing Q5 to conduct more heavily. This extra load current, during this condition reestablishes the output to +15 volts.

Hi-Lo Voltage Detection

The purpose of the hi-lo voltage detection circuit is to disable the +5-volt supply if that supply goes above or below predetermined voltage levels. It does this by shorting out the +5-volt supply with a silicon-controlled rectifier (SCR). The loss of the +5 volts causes the heads to retract in addition to protecting all logic in the machine by removing the logic operating voltage.

The hi-lo voltage detection circuit is located on board B06. For the following description, use the Transducer Amplifier schematic diagram 001977. The hi-low voltage detection circuit is shown on the lower right-hand portion of the schematic.

The +5-volt supply is connected, through R43, to the inverting input of comparator A3. The non-inverting input of A4 is connected to the reference voltage developed from the 5.6-volt zener diode CR5. Therefore, during normal conditions, input (pin 3) of A4 is positive with respect to input (pin 2). Hence, the output of A4 is a positive voltage. This positive voltage is routed through R48 and turns on Q10. Q7 and Q8 are turned off and the output at pin 1 is low. Pin 1 is connected to the gate of an SCR which is connected between the +5-volt power supply line and ground. Thus, under normal conditions, the +5-volt power supply remains unaffected.

If the +5-volt power supply increases in voltage to greater than +5.4 volts, the inverting input of A4 becomes positive with respect to its noninverting input and A4's output goes negative. This negative output turns off Q10. Q7 and Q8 turn on, generating the signal +Fire Crowbar SCR at pin 1. The SCR fires and shorts out the +5-volt supply. The A4 output also forces the signal +Emergency Retract high (pin 21) causing the heads to retract.

Also, during normal conditions, the noninverting input (pin 3) of A3 is negative with respect to the inverting input (pin 2) because of voltage division across R64, R46, and R47. Hence, the output of A3 is a negative voltage during normal conditions. This output is also held low during conditions of power up (when the 5V has not yet reached its regulated value) by the signal -Pwr Up Reset entering the board on pin 20.

If the +5-volt supply decreases to a voltage of less than 4.8 volts, the inverting input of A3 becomes negative with respect to its noninverting input and A3's output goes positive, generating the signals +Emergency Retract and +Fire Crowbar.

GLOSSARY A
LOGIC SIGNAL GLOSSARY
(Source of Signal is Shown in Parenthesis)

A

A (Servo Sequencer Logic)
Output of the A state flip-flop.

AC WRITE (Write Logic)
This signal is active if an actual AC write signal is being applied to the heads. It is used to sense an unsafe read/write condition.

ATTENTION (Servo Sequencer Decode Logic)
This line signals the controller upon completion of a seek or the detection of a seek incomplete condition.

B

B (Servo Sequencer Logic)
This is the output of the B state flip-flop.

BOBBIN OVER TEMPERATURE (B04)
This signal becomes active if the linear motor bobbin gets too hot. This is not a logic signal but the voltage drop across a negative temperature coefficient resistor which is connected to a negative voltage.

C

C (Servo Sequencer Logic)
Output of the C state flip-flop.

CAR 1 through CAR 128 (Cylinder/Present Address Register Logic)
These are the eight states of the CAR. They indicate to the Adder and Speed Decode logic the desired position of the carriage. On some drive models, they are also sent to the controller on separate status lines.

CAR/PAR RESET (Servo Sequencer Decode Logic)
This decoded Servo Sequencer logic signal resets both the CAR and the PAR prior to a First Seek or Restore. It is also used by the Actuator Driver logic.

CARRY (Adder and Speed Decode Logic)
This is the carry-out line of the bit 128 element. This signal is stored by the state counter as an indication of direction for the next seek.

CE RESET (Control Safety Logic and Servo Protect Logic)
This signal (activated by a pushbutton on the respective board) resets the latches which form the File Unsafe logic.

CLEAR (Servo Sequencer Logic)
This signal directly resets the four state flip-flops in the Servo Sequencer logic and resets the On-Line and Attention latches in the Servo Sequencer Decode logic.

CLOCK (Transducer Amplifier Logic)
This signal is a square wave version of the 145-kHz oscillator output.

COMPARE (Adder and Speed Decode Logic)
This signal is generated if the CAR and PAR contents are equal. It implies that the carriage is positioned at the desired cylinder.

COMPOSITE INDEX-SECTOR (Index/Sector Logic)
This signal becomes active each time an index or a sector slot is detected. It is sent to the controller.

CONT GRD (From controller via line receiver to the Power-Up Sequencing and Control Logic.)
This line, Controlled Ground, receives a signal from the controller to enable the Sequence In signal to set the Sequence latch.

CONTROL (From controller via line receiver to the Control Safety Logic.)
Commands from the controller are issued to the drive by combining this signal with one or more Unit Bus line signals.

CYL COUNT (Transducer Amplifier Logic)
This signal represents a cylinder count and is generated each time a detent rack tooth causes a phase shift in the cylinder transducer output.

CYLINDER 1 THROUGH CYLINDER 128 (Lamp Drivers)
These signals light the cylinder position lights on the operator control panel.

CYLINDER TRANSDUCER SEC OUTPUT (Transducer Amplifier Logic)
This is the 145-KHz sine wave signal that is induced by coupling through the detent rack teeth.

D

D (Servo Sequencer)
This is the output of the D state flip-flop.

DETENT (Servo Sequencer Decode Logic)
This signal causes the detent pawl to engage (set) the detent rack by pulsing the detent actuator set coil.

DISABLE (Power-Up Sequencing and Control Logic)
This signal resets the Enable latch. It is a function of the ENABLE-DISABLE switch on the operator control panel.

DOOR CLOSED (Power-Up Sequencing and Control Logic)
This signal is active when the Door Open-Door Closed switch is in the Door Closed position.

DOOR OPEN (Power-Up Sequencing and Control Logic)
This signal is active when the Door Open-Door Closed switch is in the Door Open position.

DRIVE READY (Index/Sector Logic)
This signal lights the Ready lamp on the operator control panel.

DRIVER OVER TEMPERATURE (Servo Control Logic)
This signal becomes active if the servo driver transistor heat sinks exceed normal operating temperature. This is not a logic signal but two negative temperature coefficient resistors parallel connected to a negative voltage.

E

EMERGENCY RETRACT (5V High-Low Detector on Transducer Amplifier Board)
This signal is generated when the 5-volt supply goes out of its specified range. It guarantees that the heads are retracted during certain failure conditions.

ENABLE (Power-Up Sequencing and Control Logic)
This signal sets the Enable latch. It is a function of the ENABLE-DISABLE switch on the operator control panel.

ENABLE LATCH (Power-Up Sequencing and Control Logic)
This signal enables the drive to be selected by the controller.

END OF CYL (Head Selection and Register Logic)
This signal becomes active when the selected drive head counter has reached the end of present cylinder (head address of 20).

ERASE AND NOT READY (Control Safety Logic)
This signal is used to generate a File Unsafe signal. It is active if the erase gates in the Head Selection and Register logic have been selected but the drive is not ready to seek.

ERASE AND READ (Control Safety Logic)
This signal is used to generate a File Unsafe signal. It is active if the erase gates and the read gates in the Head Selection and Register logic have been selected simultaneously.

ERASE I (LF) (Write Logic)
This signal supplies current to the erase heads on the left-hand column of read/write heads.

ERASE I (RT) (Write Logic)
This signal supplies current to the erase heads on the right-hand column of read/write heads.

ERASE I (SENSE) (Write Logic)
This signal indicates that erase current is being applied to the heads.

ERASE LF (Head Selection and Register Logic)
This signal enables the left erase current driver.

ERASE RT (Head Selection and Register Logic)
This signal enables the right erase current driver.

ERASE SELECT ERROR (Control Safety Logic)
This signal is used on the board to generate a File Unsafe signal. It is active if erase current is being applied to the erase coils but the erase gates in the Head Selection and Register logic have not been selected.

F

FILE UNSAFE (Control Safety Logic)
This line goes to the controller and is active when the drive has detected a condition within its circuitry which could cause damage to recorded data.

FORCE COUNT (Servo Sequencer Decode Logic)
This signal occurs just prior to the reverse seek portion of a Restore operation. Its prime function is to force a constant address into the PAR such that the PAR will have counted down to zero when the carriage reaches cylinder zero.

FORCE FORWARD SLOW (Servo Sequencer Decode Logic)
This line goes to the Adder and Speed Decode logic to simulate an address difference of 4 and select the corresponding velocity during the forward portion of a Restore.

FWD DETENT VELOCITY (Servo Sequencer Decode Logic)
This signal goes to the error operational amplifier in the Servo Control logic. It selects the proper current value for the linear positioning motor to move the carriage forward at the proper velocity for engaging with the detent.

FWD VELOCITY (Servo Control Logic)
This signal becomes active when the carriage is moving forward at a speed greater than 1 ips. This signal going false is an indication to the Servo Sequencer logic that the carriage has come to rest either against the detent or against the forward carriage stop.

FWD VELOCITY 1 through FWD VELOCITY 7 (Adder and Speed Decode Logic)
These signals represent CAR/PAR differences and are used by the servo system to achieve various forward velocities with the linear positioning motor.

H

HEAD SELECT ERROR (Head Selection and Register Logic)
This signal is generated if a head number greater than 19 is selected or if both left and right heads are selected to write or erase simultaneously.

HEADS EXT (Power-Up Sequencing and Control Logic)
When the Heads Extended-Heads Retracted switch is in the Heads Extended position this signal is active. This signal is the complement of Heads Retracted.

HEADS EXT TO CONT (Power-Up Sequencing and Control Logic)
This signal is used in the controller as an indication that a unit or units have heads extended.

HEADS RET (Power-Up Sequencing and Control Logic)
This signal starts the 12-second dynamic braking current if the START-STOP switch is in the STOP position. This signal also removes current from the motor relay (K2). It is also used by the Servo Control logic to disable current to the linear motor when the heads are retracted.

HOLDING CURRENT (Servo Sequencer Decode Logic)
When this line is active, holding current is applied to the linear positioning motor, keeping a light force on the carriage in the forward direction against the engaged detent pawl.

HOLDING CURRENT (Actuator Driver Logic)
When this line is active, current is maintained in the detent actuator pick coil to hold the detent picked while a seek is in progress.

I

INDEX (Index/Sector Logic)
This line is pulsed each time an index slot is detected by the index transducer.

K

K1/K2 PICK (Power-Up Sequencing and Control Logic)
This signal provides a ground return to pull in the motor relay (K2) and the meter relay (K1).

L

LEFT SELECT (Head Selection and Register Logic)
This signal is active if the left-hand column of read/write heads has been selected.

LINE SELECT 0 through LINE SELECT 9 (Head Selection and Register Logic)
These signals activate the line select drivers on the Read Amplifier board.

LINE SELECT DRIVER 0 through LINE SELECT DRIVER 9 (Read Amplifier)
These signals drive the head switch transistors on the Read/Write Amp logic.

N

NO AC WRITE (Control Safety Logic)
This signal is used to generate a File Unsafe signal. It is active if the write gates in the Head Selection and Register logic have been selected but no voltage changes at the write current driver output are detected.

NO ERASE I (Control Safety Logic)
This signal is used on the board to generate a File Unsafe signal. It is active if the write gates in the Head Selection and Register logic have been selected but no erase current is being applied to the erase coils.

O

ON LINE (Servo Sequencer Decode Logic)
This line indicates to the controller that the cables are connected, heads have been loaded, the ENABLE-DISABLE switch is in the ENABLE position and the unit is ready to seek and then to read or write.

OSC OUTPUT (Transducer Amplifier Logic)
This is the sine wave output of the 145-kHz oscillator.

OVER TEMP (Servo Control Logic)
This signal becomes active if either the servo transistors or the linear motor overheat.

P

PAR 1 through PAR 128 (Cylinder/Present Address Register Logic)
These are the eight stages of the Present Address Register. They indicate to the Adder the present cylinder position of the carriage.

PICK (Index/Sector Logic)
This signal is pulsed during a restore operation to assure the detent pawl is picked properly.

PICK DRIVE (Actuator Driver Logic)
This signal drives the actuator pick coil current driver.

POWER UP RESET (Power-Up Sequence and Control Logic)
This signal is pulsed when the primary AC power is turned on. It is used to initialize various logic to a known state.

R

READ DRIVER (LF) (Read Amplifier Logic)
The transistor switch which allows the left-hand row of read/write heads to read is turned on by this signal.

READ DRIVER (RT) (Read Amplifier Logic)
The transistor switch which allows the right-hand row of read/write heads to read is turned on by this signal.

READ LF (Head Selection and Register Logic)
This signal enables the left read driver.

READ ONLY (Power-Up Sequencing and Control Logic)
This signal becomes active when the READ/WRITE-READ ONLY switch on the operator control panel is in the READ ONLY position. It is sent to the controller as a status line and is used within the file to inhibit any write operations.

READ OUTPUT TO CONT (Read Amplifier Logic)
The information read off of the disc pack is sent to the controller on this line.

READ PREAMP OUTPUT (LEFT) (Read/Write Amplifier Logic)
This is the output of the left preamplifier, which is the first stage in amplifying and shaping the data read off of the discs by any of the left bank of heads.

READ PREAMP OUTPUT (RIGHT) (Read/Write Amplifier Logic)
This is the output of the right preamplifier, which is the first stage in amplifying and shaping the data read off the discs by any of the right column of heads.

READ RT (Head Selection and Register Logic)
This signal enables the right read driver.

READ/WRITE (Power-Up Sequencing and Control Logic)
This signal is enabled when the READ/WRITE-READ ONLY switch is in the READ/WRITE position.

RESET ATTENTION (Control Safety Logic)
This signal resets the Attention latch (on the Servo Sequencer Decode logic) when the controller commands a Read operation.

RESET HEAD REG (Control Safety Logic)
This signal resets the Attention latch (on the Servo Sequencer Decode logic) when the controller commands a Read operation.

RESET HEAD REG (Control Safety Logic)
This signal resets the head register to address zero during a Restore operation or when commanded by the controller.

RESET TIMERS (Servo Sequencer Decode Logic)
This signal is used to reset the following delay timers: Seek Incomplete, Forward Seek, First Seek, and Ready. All timers start simultaneously when this reset signal goes false.

RESTORE (Servo Sequencer Decode Logic)
This is the output of a flip-flop which is set when a restore operation is commanded by the controller. It is reset after the detent pawl is picked at the start of a Restore operation.

RETRACT HEADS (Power-Up Sequencing and Control Logic)
This signal commands the heads to retract if the START/STOP switch is in the STOP position, the disc pack door is opened, Upspeed goes false, or if the Sequence latch is reset.

REV VELOCITY 1 through REV VELOCITY 7 (Adder and Speed Decode Logic)
These signals represent CAR/PAR differences and are used by the servo system to achieve various reverse velocities with the linear motor.

RIGHT SELECT (Head Selection and Register Logic)
This signal is active if the right-hand column of read/write heads has been selected.

S

SECTOR ÷ 1, SECTOR ÷ 2, SECTOR ÷ 4 (Index/Sector Logic)
These are the three possible jumper selections of sector pulses to the controller. One jumper selects every sector pulse, another every second sector pulse, and the other every fourth sector pulse.

SECTOR/INDEX (Transducer Amplifier Logic)
This is the output of the Index Transducer Amplifier board.

SEEK ENABLE (Power-Up Sequencing and Control Logic)
This signal enables the drive to perform seeks if it has met all safety conditions. Loss of this signal turns off the Ready indicator light on the operator control panel, disables the servo, and holds the Servo Sequencer logic reset.

SEEK FORWARD (Servo Sequencer Decode Logic)
This signal enables the forward direction adder gates and PAR counter to count up during a forward seek.

SEEK INCOMPLETE (Servo Sequencer Decode Logic)
This signal indicates that the carriage failed to reach a normal detent position within 100 msec or less. It goes to the controller as a status line.

SEEK READY (Servo Sequencer Decode Logic)
This line indicates that the drive has satisfactorily completed a seek. It goes to the controller as a status line.

SEEK REVERSE (Servo Sequencer Decode Logic)
This signal goes to the Adder and Speed Decode logic to enable the reverse direction adder gates and the PAR counter to count down during a reverse seek.

SEEK START (Servo Sequencer Decode Logic)
This is the output of a flip-flop which is set when a seek operation is commanded by the controller. It is reset after the detent pawl is picked at the start of the seek operation.

SELECT UNIT (From controller via line receiver to the Control Safety Logic)
This signal from the controller selects the one drive out of the string (attached to the controller) which is to receive commands.

SELECTED WRITE GATE (Control Safety Logic)
This signal partially enables the Write LF and Write RT gates in the Head Selection and Register logic.

SELECTED ERASE GATE (Control Safety Logic)
This signal, decoded from the command input lines, partially enables the Erase LF and Erase RT gates in the Head Selection and Register logic.

SELECT HEAD (Control Safety Logic)
This signal, decoded from the command input lines, enables the outputs of head register flip-flops (2 through 16).

SELECTED HEAD ADVANCE (Control Safety Logic)
This signal, decoded from the command input lines, increases the head register by one count each time it is activated.

SELECTED READ GATE (Control Safety Logic)
This signal, decoded from the command input lines, partially enables the Read RT and the Read LF gates in the Head Selection and Register logic.

SELECTED SEEK READY (Index/Sector Logic)
The unit selected has satisfactorily completed a seek or Restore if this signal is active.

SELECTED SET CYLINDER (Control Safety Logic)
This signal, decoded from the command input lines, loads the CAR with the address on the bus input lines.

SELECTED SET HEAD (Control Safety Logic)
This signal, decoded from the command input lines, loads the Head Register with the address on the bus input lines. Only bus lines which are true will cause the register flip-flops to change state.

SELECTED UNIT CONTROL (Control Safety Logic)
This pulse, decoded from the control input lines, is used to initiate the control function specified on the bus input lines.

SEQ IN (From controller via line receiver to the Power-Up Sequencing and Control Logic)
This line is activated from the controller or from a previous drive in a string of drives. It starts the power-up sequencing of the drive.

SEQ OUT (Power-Up Sequencing and Control Logic)
This signal provides the Sequence In signal for the next drive in a string of drives.

SERVO DISABLE (Index/Sector Logic)
This signal inhibits drive current to the servo under conditions of Seek Incomplete or File Unsafe.

SERVO DRIVER INPUT (Servo Control Logic)
This is the output of the error amplifier (A4) which feeds the servo driver. The servo driver supplies current to the linear motor.

SET CYLINDER (From controller via line receiver. Enters at Control Safety Logic.)
When this line from the controller is activated, the drive interprets the pre-established data on all eight Unit Bus lines as the new cylinder address. It is a tag line from the controller.

SET DRIVE (Actuator Driver Logic)
This signal drives the actuator set coil current driver to set the detent pawls.

SET HEAD (From controller via line receiver. Enters at Control Safety Logic.)
When this line from the controller is activated, the drive interprets the pre-established data on Unit Bus lines 3, 4, 5, 6, and 7 as the new head address.

START (Power-Up Sequencing and Control Logic)
This signal results from the START-STOP switch being in the START position. It initiates a sequence of operations which bring the drive up to operating speed, restores the carriage to cylinder zero and places the drive in a ready state.

START T5 (Power-Up Sequencing and Control Logic)
This signal starts the 60-second warm-up delay timer.

START T6 (Power-Up Sequencing and Control Logic)
This signal starts the 12-second dynamic-braking delay timer.

STOP (Power-Up Sequencing and Control Logic)
This signal results from the START-STOP switch being in the STOP position. It stops the machine by retracting the heads, removing current to the motor relay and then applying 12-second dynamic braking to the motor.

STROBE B (Transducer Amplifier Logic)
This signal is used for cylinder transducer output phase detection and as a clock for the Servo Sequencer state flip-flops. It is a 200-nsec pulse which is triggered by the rising edge of the clock signal.

STROBE A (Transducer Amplifier Logic)
This signal clocks the various J-K flip-flops on the Transducer Amplifier board.

SYSTEM UNSAFE (System Protection Logic)
This signal is derived from the Servo Unsafe and Over Temperature latches on System Protection board B02, and when active, results in a File Unsafe signal from the Control Safety board (B07).

T

T1 (Delay Timers Logic)
This is the Seek Incomplete delay signal.

T2 (Delay Timers Logic)
This is the Forward Seek delay signal.

T3 (Delay Timers Logic)
This is the First Seek delay signal.

T4 (Delay Timers Logic)
This is the Ready delay signal.

T5 (Delay Timers Logic)
This is the warm-up delay signal (60 seconds).

T6 (Delay Timers Logic)
This is the dynamic-braking delay signal.

12-SECOND DYNAMIC BRAKING (Power-Up Sequencing and Control Logic)
This signal causes a direct current to be applied to the spindle drive motor for dynamic braking.

U

UNIT BUS 0 through UNIT BUS 7 (From controller via line receivers)
These lines from the controller are used to perform control functions and to carry cylinder and head addresses to the drive.

UNIT IS SELECTED (Control Safety Logic)
When the drive is selected, this signal enables the line drivers associated with the CAR and status lines on logic boards B08 and B09. It tells the controller that the drive is selected.

UPSPEED (Index/Sector Logic)
This signal indicates that disc rotation speed is 70% or more of its maximum operating speed.

W

WRITE AND NOT READY (Control Safety Logic)
This signal is used on the board to generate a File Unsafe signal. It is active if the write gates in the Head Selection and Register logic have been selected but the drive is not ready to seek.

WRITE AND READ (Control Safety Logic)
This signal is used on the board to generate a File Unsafe signal. It is active if the write gates and the read gates in the Head Selection and Register logic have been selected simultaneously.

WRITE DATA (Write Logic)
These data pulses are routed to the write current driver before they are applied to the heads.

WRITE DATA INPUT (From controller. Enters at Write Logic)
This is binary information from the controller to be recorded on the disc.

WRITE I (LF) (Write Logic)
This signal activates the left write current driver on the left Read/Write Amplifier.

WRITE I (RT) (Write Logic)
This signal activates the right write current driver on the right Read/Write Amplifier.

WRITE I (SENSE) (Write Logic)
This line to the controller becomes active when a head on the selected unit is drawing current (writing).

WRITE INHIBIT (Control Safety Logic)
This signal clamps the write current drivers to prevent writing during a File Unsafe condition.

WRITE LF (Head Selection and Register Logic)
This signal enables the left write current driver.

WRITE RF (Head Selection and Register Logic)
This signal enables the right write current driver.

WRITE SELECT ERROR (Control Safety Logic)
This signal is used on the board to generate a File Unsafe signal. It is active if write current is being applied to the write coils but the write gates in the Head Selection and Register logic have not been selected.

GLOSSARY B
GENERAL GLOSSARY

A

ACCESS SPEED
This is the velocity of the carriage (and heads) during a seek operation. Its peak will vary with the length of the seek.

ACCESS TIME
This is the time required for the carriage to perform a seek. Average access time is 35 msec; maximum is 60 msec.

AC FAIL CONDITION
This is a condition of loss of AC voltage into the disc drive. This condition will cause an emergency retract of the heads from the disc pack, thus preventing possible damage to the disc pack.

ATTENTION
This condition occurs if a normal seek is completed or if 100 msec have expired since a seek command was given and detenting did not occur.

B

BALANCED LOAD
The three phases of the primary AC power lines are rotated (between in and out connectors) in a multiunit system to provide a balanced load to the power source.

BIT CELL TIME
The bits of data are transferred in equal periods called bit cell times. Each bit cell time begins with a clock pulse. If there is a bit in the middle of the bit cell time, that bit cell time represents a logical ONE. If there is no bit between clock pulses, the bit cell time represents a logical ZERO.

BOBBIN-WOUND ARMATURE
This is the movable cylinder upon which the linear motor coil is wound.

BUS CABLE
The bus cable contains signal lines which are common to all 660-1 drives in a string of drives.

BUS LINES
These eight time-shared lines from the controller are used to perform control functions and to gate addresses to the drive.

C

CAM TOWER
This is a metal framework which arches over the carriage and head arm assembly. It provides a mounting surface for the unload cams.

CAR
This is the abbreviation for the cylinder address register. This register holds the cylinder address which is sent by the controller prior to a seek operation.

CARRIAGE
This is the movable assembly on which the Tee-block is mounted. It carries the Tee-block and head/arm assemblies forward and back as the linear motor positions them.

CENTRAL PROCESSING UNIT
This is the computer, the machine that processes the data.

CHASSIS GROUND
This is the metal frame and chassis of the hinged assemblies of the drive.

CLOCK PULSES
See double-frequency technique.

COMMAND
This is an instruction from the controller to perform some operation (e.g., set the cylinder address into the CAR).

COMPARE CONDITION
This occurs when the outputs of the CAR and the PAR are identical. It means the heads are positioned at the desired cylinder.

COMPARISON LOGIC
Comparison logic in the Adder and Speed Decode logic compares the outputs of the CAR and the PAR. This is done to determine required access speed and polarity of the signal to the servo system in order to position the heads to the desired cylinder.

CONTROL CYCLE
During this operation cycle, which is enabled by the Control Tag line, control functions are entered into the drive from the controller on one or more bus lines.

CONTROLLER
This is the machine that coordinates communication between the peripheral equipment (e.g., disc storage drives) and the central processing unit (computer).

COUNT PULSES
Refer to Cylinder Count Pulses.

CROWBAR
This is a silicon-controlled rectifier which can be fired to ground the logic power supply when abnormal overvoltage or undervoltage conditions are detected by a safety circuit.

CYLINDER
Cylinders are corresponding tracks on all 20 surfaces of a disc pack. There are 203 cylinders per disc pack.

CYLINDER COUNT PULSE
A cylinder count pulse is generated by the Transducer Amplifier logic each time the heads reach a new cylinder during a seek.

CYLINDER TRANSDUCER
This is a device which senses the change of cylinder position of the read/write heads as the carriage moves by during a seek. It operates by electrically sensing the passage of teeth on the detent rack mounted on the carriage.

D

DATA
This is information which is written on or read from disc surfaces. It is transferred between the disc drive and the central processing unit in serial binary form.

DATA TRANSFER RATE
This is the rate at which data can be written onto or read from the disc. Its value is given in megabits/second.

DELAY TIMERS
These are circuits which generate signals of fixed durations. These signals provide a time reference for other operations in the drive.

DENSITY
See track density.

DETENTED
This term describes the condition of the access mechanism and logic when the teeth of the detent pawl are engaged with the teeth of the detent rack. The carriage is stopped during this condition.

DETENT ACTUATOR
This is the electromagnet-read assembly which causes the detent pawl to engage or disengage (set or pick) with the rack teeth.

DETENT PAWL
This is the pawl portion of a ratchet device which stops the carriage at the desired cylinder by engaging its teeth into the teeth on the detent rack.

DETENT RACK
This is a metal bar mounted on the side of the carriage with a row of teeth facing the detent pawl. The detent pawl engages these teeth to stop the carriage at the end of a seek. The rack teeth are also used by the cylinder transducer to help detect changing cylinder position during a seek.

DIFFERENCE COUNT

This is the numerical difference between the outputs of the CAR and PAR as decoded by the Adder logic. It represents the number of cylinders the carriage must move to complete a seek.

DISC PACK

The disc pack is the storage medium used by disc storage drives. It consists of 11 flat metal discs, coated with a magnetic oxide material and stacked about 0.4 inches apart.

DOUBLE-FREQUENCY TECHNIQUE

This is a system of recording data in which a logical ZERO is represented by only a clock bit at the beginning of a bit cell time. For a logical ONE, there is a clock bit at the beginning of the bit cell time and a data bit in the middle of the bit cell time. Logical ONEs are distinguishable from logical ZEROs because their bit frequency is double the logical ZERO bit frequency.

DYNAMIC BRAKING

When the STOP switch is pressed, AC power to the spindle drive motor is removed and a DC voltage is applied to the motor coil to bring it to a smooth, quick stop.

E

ERASE CURRENT

This is the DC current which is applied to the erase coil. (See definition of erase poles.)

ERASE POLES

These are the tips of an electromagnet (part of the Read/Write Head assembly) that straddle the track of written data. Whenever data is being written, the erase coil is energized and trims the area along the sides of the freshly recorded data to provide a constant width data track with unrecorded disc area between tracks.

F

FILE

This term means the same as disc storage drive.

FILE MONITOR INDICATOR

This set of lights, which is located on the operator control panel, indicates the present cylinder position in weighted binary numbers.

FILE UNSAFE CONDITION

This could be any of a number of conditions in the drive which the safety circuits consider would endanger the data on the disc pack if continued disc operation were attempted.

FIRST SEEK
This term describes the sequence of operations which positions the carriage to cylinder 000 when the drive is first turned on.

FLYING HEIGHT
This is the clearance between the head face and the rotating disc face. Flying height is nominally 80 microinches.

FORCED FOWARD SEEK
At the beginning of a first seek or restore operation, the carriage is slowly moved to the forward carriage stop. This operation is called a forced forward seek.

FORWARD CARRIAGE STOP
This piece of stiff spring steel, which is fixed to the end of the carriage way, stops the carriage so that the heads cannot be positioned too far into the disc pack.

FORWARD SEEK
This term describes the operation of the carriage as it positions the heads toward the forward carriage stop (from a lower cylinder address to a higher cylinder address).

FORWARD STOP
Refer to Forward Carriage Stop.

H

HEAD
See Read/Write Head.

HEAD ALIGNMENT
This is a process by which each head arm assembly is adjusted radially so that it is centered over a reference track on a calibration disc pack.

HEAD ARM ASSEMBLY
A head arm assembly consists of a stainless steel spring fixture upon which a head shoe mounts. It is attached to the Tee-block tower and is used to insert the read/write head into the disc pack. There are 20 head arm assemblies in a 660 disc pack drive.

HEAD SHOE
This is the ceramic disc-like portion of a read/write head in which the read/write and erase poles are encased.

HEADS EXTENDED
The heads are extended when they are positioned into the disc pack. A switch near the linear motor is actuated by the carriage when the heads are extended.

HEADS RETRACTED
The heads are retracted when they are positioned out of the disc pack.

HOLDING CURRENT

After the heads are positioned to the desired cylinder, a small amount of forward current is applied to the linear positioning motor to hold the detent rack teeth firmly against the detent pawl teeth. Holding current is also a term used to refer to the current maintained in the detent actuator pick coil to hold the detent picked while a seek is in progress.

HOME POSITION

This is cylinder 000, the cylinder closest to the outer rim of the disc pack. This is the destination cylinder of all first seek and restore operations.

I

INDEX

This is a slot on the edge of the bottom plate of a disc pack; it is used as a reference point by the controller for synchronizing read/write operations. This index slot is also used by the drive logic for determining rotational speed of the disc pack.

INDEX ONLY MODE (As opposed to Sector Mode)

This is the mode of operation for a disc pack drive which uses a disc pack with an index slot on the bottom plate. There are no sector slots.

INDEX/SECTOR DISC PACK

A disc pack which contains both an index slot and a number of evenly spaced sector slots on the rim of its bottom plate is called an index/sector disc pack.

INDEX TRANSDUCER

This is a device which detects the presence of index or sector slots by means of magnetic coupling.

INDEX TRANSDUCER ALIGNMENT

This is a process by which the index transducer is adjusted circumferentially until the Index signal appears within the proper time relationship to a reference signal recorded on a calibration disc pack.

INTERIOR CONTROL PANEL

This panel, inside the drive, contains the power-on switch, the fuses, and the cable connectors.

L

LINEAR POSITIONING MOTOR

This motor positions the carriage (with attached read/write heads) to the desired cylinder. It operates on the principle of a programmed current applied to a moving coil in a permanent magnet field to produce a desired carriage velocity.

LINEAR TACHOMETER

This device, located in the linear positioning motor, generates a voltage proportional to the speed of the linear positioning motor. It is part of the feedback loop in the positioning motor servo.

LOADING FORCE

This is the force applied to a read/write head by the leaf spring. It attempts to push the head toward the disc. The air cushion between the head and disc surface created by the rotating disc counters the spring loading force and keeps the head at the required flying height.

LOAD/UNLOAD RAMP

This is the portion of a head arm which bears against an unload cam as the heads are extended or retracted.

LOGICAL CONNECTION

This term refers to any electrical connection within the disc drive other than a supply voltage or data.

LOGICAL ONE (Drive Interface Signals)

This is a relative term that identifies the more negative level of a digital logic signal.

LOGICAL ZERO (Drive Interface Signals)

This is a relative term that identifies the more positive level of a digital logic signal.

M

MULTIUNIT SYSTEM

This is a system which consists of more than one disc storage drive. A multiunit system can contain up to eight drives.

N

NONRETURN-TO-ZERO TECHNIQUE

This is a technique of recording information onto a magnetic disc by changing the direction of magnetization of a segment of the disc track each time a bit is received.

O

ODD/EVEN DETENTING

Because the two detent pawls are offset from one another by half their pitch, they are able to engage the detent rack in twice as many positions as there are teeth. The scheme is called odd/even detenting because one detent pawl stops the carriage at all odd numbered cylinders while the other stops it at all even numbered cylinders.

ONE LEVEL

Refer to Logical One.

ONE SHOT

This is a monostable multivibrator circuit. When triggered, a one shot remains in a given state for a predetermined time before returning to its original state unless reset by the input signal before the predetermined interval elapses.

OPERATOR CONTROL PANEL

This control panel contains all the switches and indicators which are accessible to the operator.

P

PACK-ON SWITCH
This switch, mounted on the bottom of the spindle assembly, prevents voltage from being applied to the spindle drive motor unless a disc pack is on the spindle.

PAR
This is the abbreviation for the present address register. This register holds the cylinder address to which the heads are presently positioned.

PICK
This means to disengage the detent pawl from the detent rack by applying current to the pick coil of the detent actuator.

PROGRAMMED CYLINDER
This is the cylinder selected by the controller as the destination of the next seek.

PROGRAMMED VELOCITY
This is the desired carriage velocity for a seek of a given length. The current fed to the linear motor coil is controlled by the speed decode and linear velocity tachometer output so that when it reaches the amount required to produce the desired velocity, it is stabilized. The carriage maintains its programmed velocity until the speed decode requirements change.

R

RAMP SURFACE
Refer to Load/Unload Ramp description.

READ DATA COAX
The information which is read from the disc is routed to the controller on this line.

READ ONLY MODE
This is a mode of operation which can be selected by the READ/WRITE-READ ONLY switch on the operator control panel. When the drive is in this mode, the write and erase circuitry are disabled.

READ/WRITE GAP
This is the narrow air space between the pole pieces in a read/write head. When write current is applied to the head, a flux field builds up across the gap.

READ/WRITE HEADS
These are flat ceramic discs which contain the read, write, and erase coils. The read/write heads are mounted on flexible metal arms so that they can be inserted into the disc pack for reading or writing on their respective disc surfaces.

READY CONDITION
The disc drive is in the ready condition when it has satisfactorily completed a seek.

RECORDING DISC
This is a flat disc coated with magnetic oxide upon which the desired information is stored. A disc pack used on a disc storage drive contains 11 discs with 20 usable recording surfaces.

RESTORE

This term describes the sequence of operations which position the carriage to cylinder 000. This operation can be commanded by a single input from the controller and is used to return the carriage to the known reference cylinder before seeking to a desired cylinder on the pack.

RETRACTED POSITION

Refer to Heads Retracted.

REVERSE SEEK

This term describes the operation of the carriage as it positions the heads toward the outer rim of the disc pack (from a higher cylinder address to a lower cylinder address).

ROTATIONAL TIME

This is the time it takes the disc pack to make one complete revolution. At nominal line voltage and frequency, rotational time is 25 msec.

RUN CURRENT

This is the AC current required by a single drive after it has been started.

S

SECTOR MODE

This is the mode of operation for a disc storage drive which uses a disc pack with sector slots as well as an index slot on its bottom plate.

SEEK

This is the operation which positions the heads to a new cylinder.

SEEK INCOMPLETE

This is a condition sensed within the disc drive when a seek was started and apparently not completed within a nominal 100 msec. Completion of the seek is sensed by the lack of forward velocity detected out of the linear tachometer.

SPINDLE

This is the tapered axle the disc pack is mounted on.

SPINDLE DRIVE MOTOR

This is the electric motor which rotates the disc pack via a drive belt and a spindle.

SPINDLE DRIVE SYSTEM

The spindle drive system consists of the spindle drive motor, the drive belt, and the spindle.

SPINDLE LOCK

This is a mechanical lock which prevents the spindle from turning while the door covering the disc pack is open. It does this by engaging a pawl in one of several notches in the spindle pulley.

START CURRENT
This is the AC current required to start a drive.

STATE
This term refers to the combinations of conditions (set or reset) of the four flip-flops in the Servo Sequencer logic. These different states initiate different operations within the drive.

STATUS LINE
These lines contain signals which go back to the controller to inform it of various operating conditions within the drive.

STRING
This term refers to a group of more than one disc storage drive in a multiunit system.

T

TACHOMETER
Refer to Linear Tachometer.

TAG LINES
These three lines from the controller are used to perform setup and control functions. The lines initiate the set cylinder cycle, the set head cycle, and the control cycle.

TEE-BLOCK
This is an aluminum fixture which is mounted on the carriage. The head arm assemblies are attached to the Tee-block.

TRACK
Information is recorded on a disc surface in a narrow circular path called a track. There are 203 concentric tracks on each disc surface, each nominally 0.007 inches wide.

TRACK DENSITY
This term refers to the number of bits per inch that are stored on a given track. Track density is greater on inner (high numbered) tracks.

TRACK-TO-TRACK POSITION TIME
This is the time it takes the carriage to move from one track to an adjacent one.

TURNAROUND
When the carriage reaches the prescribed cylinder at the end of a reverse seek, the servo system causes the carriage to reverse direction and then go forward for a short distance. The period from the time the carriage first reaches the prescribed cylinder until it detents is called the turnaround. This step is required because the detent teeth can properly engage only while the carriage is moving forward.

U

UNIT
This term means the same as disc storage drive.

UNIT CABLE
The Unit cable contains all signal lines from the controller which are unique to the particular drive. A separate Unit cable is sent to each unit in a string.

UNIT NUMBER PLUG
This is the removable plastic assembly which assigns the desired logical unit number to a particular disc drive. It contains the required arrangement of magnets to operate read switches and cause the drive to look at the appropriate Select Unit line on the bus.

UNLOAD CAMS
When the heads are being retracted from the disc pack, the unload cams on the cam tower counter the loading force of the leaf springs and cause the heads to lift away from the surfaces of the discs.

UNSAFE CONDITION
Refer to File Unsafe Condition.

UP-DOWN COUNTER
This is a register, whose contents are increased or decreased by one with each pulse applied to it. The Present Address Register in the drive can be operated as an up-down counter.

UPSPEED
When the disc pack is rotating at a speed which is at least 70% of its normal operating speed it is considered to be upspeed. Dropping to less than 70% of normal operating speed is sensed as a safety condition which will force the logic to retract the heads from the disc to prevent possible damage.

W

WARM-UP DELAY
This 60-second delay allows the temperatuare of the rotating disc pack to stabilize before a seek is initiated.

WRITE CURRENT
This is the current which is applied to the selected read/write coil to cause it to record information on the disc surface.

WRITE DATA COAX
The information sent from the controller which is to be written on the disc enters the drive on this line.

Z

ZERO LEVEL
Refer to Logical Zero.

COMMENTS FORM

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