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MEMOREX

A Burroughs Company

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8" OEM Disc Drives
Technical Manual

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Preface

This manual is for customer engineers who handle 112/114 disk drives. It describes how to operate, handle and maintain the equipment.

This manual consists of the following ten sections.

Section 1:	General Description
Section 2:	Operation
Section 3:	Installation and Checkout
Section 4:	Theory of Operation
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Section 1

General Description

1. GENERAL DESCRIPTION

1.1 GENERAL

1.1.1 General

The 112/114 micro-disk drives are high performance disk drives with unformatted storage capacities of 23.7MB and 47.4MB respectively.

The unit consists of contact start-stop type heads and media, a unique head positioning band actuator, air filter, and a DC motor and other parts to drive the disks. All these are contained within a sealed cover. And outside the cover there is a printed circuit board with the following functions; read-write, driver receiver and sequence logic.

The unit is remarkably compact, highly reliable and inexpensive. It was designed to be the same size as an 8-inch floppy disk drive. The unit can also be connected in daisy chain configuration of up to 4 units. Its data format is of a fixed length and together with its easy-to-handle interface, has simplified system design.

1.1.2 Features

(1) Compact
Since the disks are 200mm in outer diameter and are driven by a DC motor directly connected to the spindle, the device is extremely compact in size. The unit measures 217mm (8.5 in) in width, 111mm (4.4 in) in height and 356mm (14.0 in) in length.

(2) Economical
The positioning mechanism of the drive is a stepping motor which uses a steel band and a viscous damper. This has made the unit less expensive.

(3) High Reliability
The heads, disks, and the positioner are within the disk enclosure and are protected by a plastic cover. In the disk enclosure, there is a breathing filter and a recirculation filter to keep the air clean, thus ensuring reliability.

(4) Preventive maintenance is unnecessary.

(5) DC Power
Because a built-in DC motor is used, the unit does not have to be modified to suit line frequencies (50Hz/60Hz) or input power voltages (110, 115, 220, 240V).

(6) Physical Size
The unit is the same size as an 8 inch floppy disk. Therefore, when replacing a floppy disk, the locker need not be changed.

(7) Mounting Plane
The unit can be installed in its locker either vertically or horizontally.
This allows easier installation and flexible system design.

(8) Low Power Consumption
Very low power demand (seeking 70W, non seek 60W) permits it to be used in a wide range of environmental temperature (5°C to 45°C) without a cooling fan.

(9) Audible Noise
The unit's low noise output, approx. 60dB (A-scale weighting) even during seeking makes it ideal for office use.

(10) Vibration
Vibration is not transmitted to external parts because the unit is fitted to the locker with vibration isolating rubber mounts.

1.2 SPECIFICATIONS

1.2.1 Environmental Condition of Installation Site

(1) Temperature

Operating	5 to 45°C (41° to 113°F)
Non-operating	-40 to 60°C (-40° to 140°F)
Gradient	Less than 15°C/H

(2) Humidity

Operating	20% to 80% RH (Moisture must not condense.)
Non-operating	5% to 95% RH

(3) Vibration

Operating	Less than 0.2G (3 to 60Hz) (except resonance)
	Both ways 2 minutes x 30 cycle (sine wave)
Non-operating (power OFF after installation)	
	Less than 0.4G (3 to 60Hz)
	Both ways 2 minutes x 30 cycle (sine wave)
During storage or transportation	
	Less than 3G

(4) Shock

Operating	Less than 2G (maximum 10ms)
Non-operating	Less than 3G (maximum 10ms)
During storage or transportation	
	Less than 5G (maximum 30ms)

(5) Altitude

Operating	Less than 3,000m (10,000 ft)
Non-operating	Less than 12,000m (40,000 ft)

1.2.2 Power Source Specifications

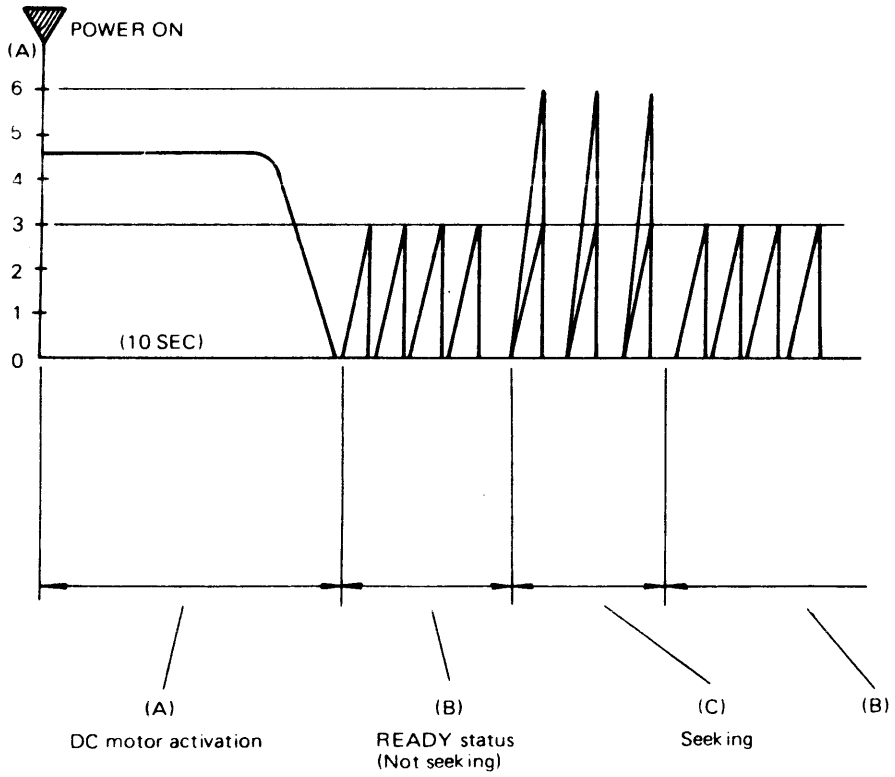
(1) Consumption Current

Voltage	Peak Current	Steady Current
+5V ±5%	6.0A max	3.4A
−12V ±5%	0.7A max	0.7A
+24V ±10%	6.0A max. (Pulse) 4.5A (10 sec.*)	1.6A

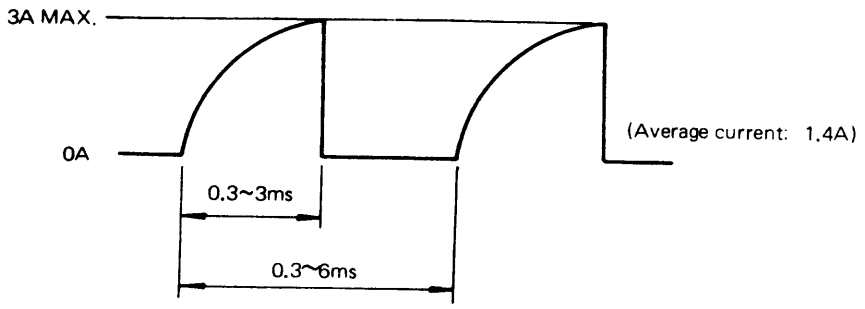
The voltage value above is the voltage at the power input terminal of the unit. Steady current is the current at AVERAGE SEEK + LATENCY TIME + 1 revolution READ or WRITE.
* Start-up time

(2) Current Wave Form

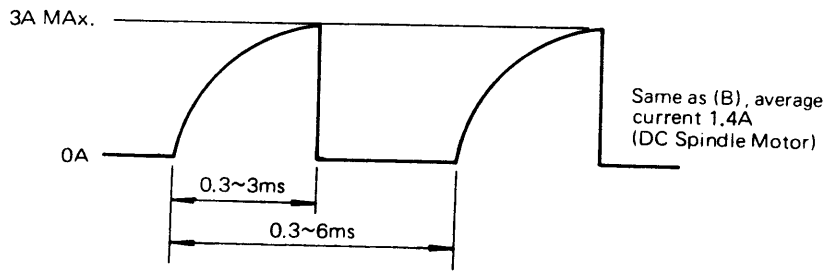
(a) +24V current wave form



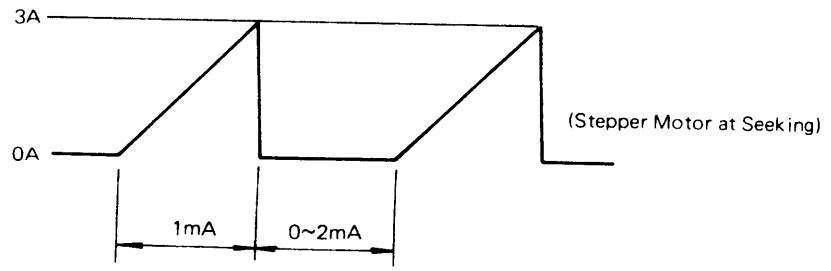
Magnified wave of (B) part



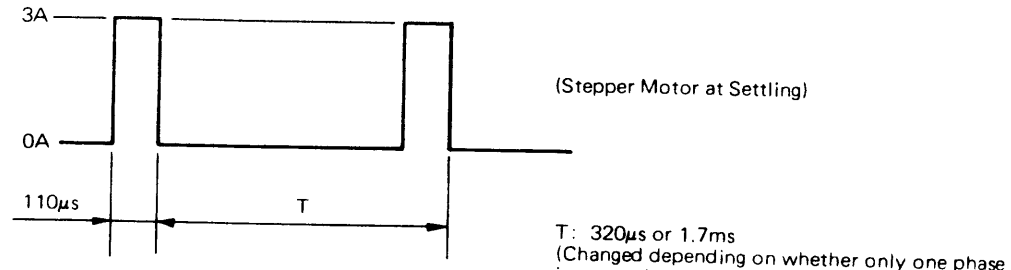
Magnified wave of (C) part



+



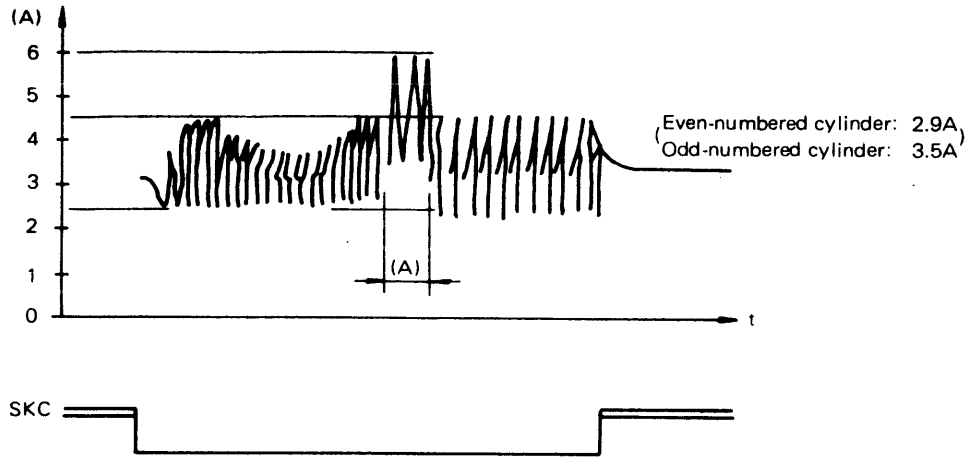
OR



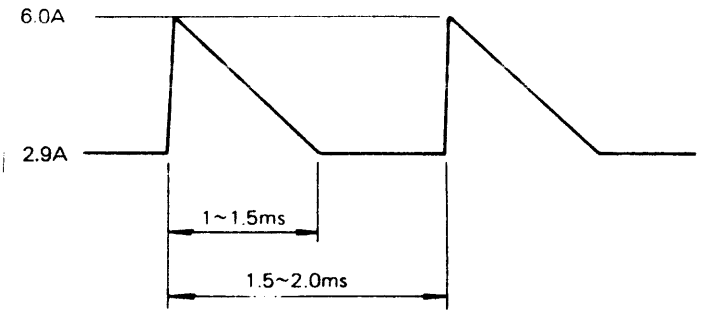
Note: The current wave shape of the (C) part is the shape formed by the lapping of the above two types of waves asynchronously.

(b) +5V current wave shape

The +5V current, at the time of seeking, forms the following switching current wave form.



Magnified wave of (A) part



Note: The 6A peak current of the (A) part is present 3 or 4 times in one seek.

1.2.3 Performance

Table 1.1 Performance

Specification \ Model		Micro disk drive 112	114
Total storage capacity			
Unformatted	[MB]	23.74	47.47
Formatted	[MB]	19.97	39.98
Storage capacity/track			
Unformat	[B]	24320^{+32}_{-0}	
Format	[B]	20480	
Number of disks		2	4
Number of heads (R/W)		4	8
Number of heads (Clock)		1	
Number of cylinders		244	
Number of tracks/cylinder		4	8
Number of sectors		Variable hard	
Recording density	[BPI]	12,360	
Track density	[TPI]	195	
Transfer rate	[MB/S]	1.2	
Rotational speed	[rpm]	2,964	
Average latency time	[ms]	10.1	
Recording method		MFM	
Positioning time	Min [ms]	30	
	Ave [ms]	70	
	Max [ms]	140	
Input voltage		+24V ±10%, 1.8A (max. 6.0A) +5V ±5%, 3.5A (max. 6.0A) −12V ±5%, 0.7A (max. 0.7A)	
External size			
Width x height x depth	[mm]	217 x 111 x 356 (8.5" x 4.4" x 14.0")	
Disk size	[mm]	Outer diameter 200 (7.9"), Inner diameter 100 (3.9")	
Weight	[kg]	6.3 (13.9 lb.)	

* Formatted capacity of 80 sectors/track

1.2.4 Reliability

(1) MTBF
MTBF is defined as follows.
MTBF = operating time/the number of equipment failures.
Operating time is the entire time at which the power is ON except during maintenance work. Failure of the unit means trouble that requires either repairs, adjustments, or a replacement. Mishandling by the operator, power failure, control unit problems, cable problems and failure due to unsuitable environment are not included.
The MTBF of the 112/114 is expected to exceed 10,000 hours (engineering specification).

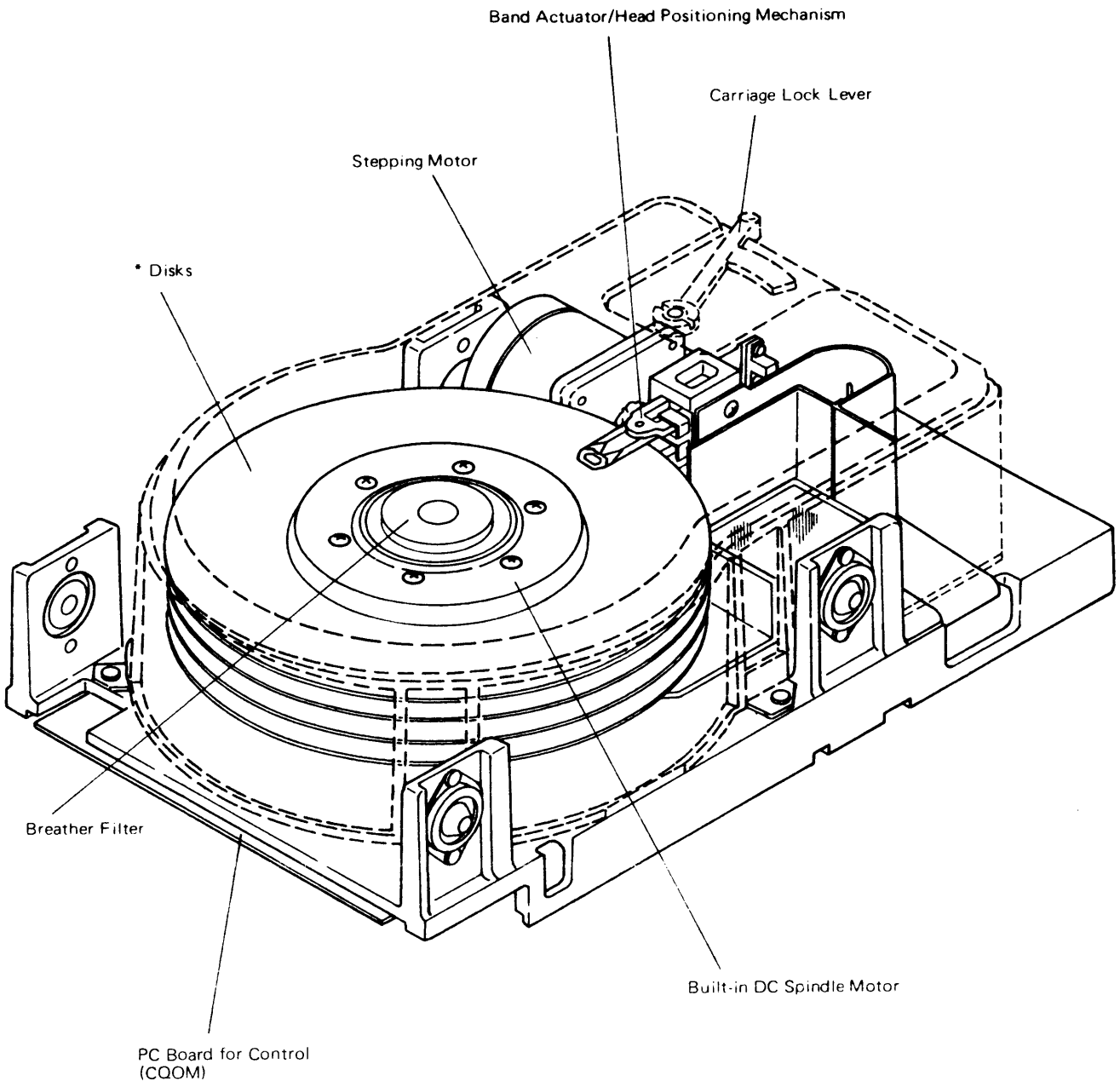
(2) MTTR
MTTR is the average time a well-trained service technician should take to diagnose and correct a failure to the sub-assembly level. The 112/114 is designed for an MTTR of 30 minutes or less.

(3) Component Life
The 112/114 need not be overhauled for the first five years.

(4) Power Loss
Integrity of the data on the disk is guaranteed against all forms of abnormal DC power loss. However, if the power failure occurs during a WRITE operation, the data is not guaranteed.

(5) Error Rate
An error detected during initialization, and processed to be replaced by a spare record is not included in the error rate.
(a) Recoverable Error Rate
An error which is recoverable with one try of the RETRY command should not exceed once per 10^{10} bits read.
(b) Non Recoverable Error Rate
Errors that cannot be recovered within 16 retries are included in the MTBF.
(c) Positioning Error Rate
The rate of positioning errors recoverable by one retry is one error or less per 10^6 seeks.
(d) Media Error
i) No error will be found at H0 and H1 in cylinder 000.
ii) The following shows the number of defective spots in the 112/114.
112 . . . . Less than 20
114 . . . . Less than 40

1.3 EXTERNAL APPEARENCE



*NOTE: 112 contains two disks.
114 contains four disks.

Fig. 1.1 External Appearance

Section 9

Operation

2. OPERATION

2.1 GENERAL

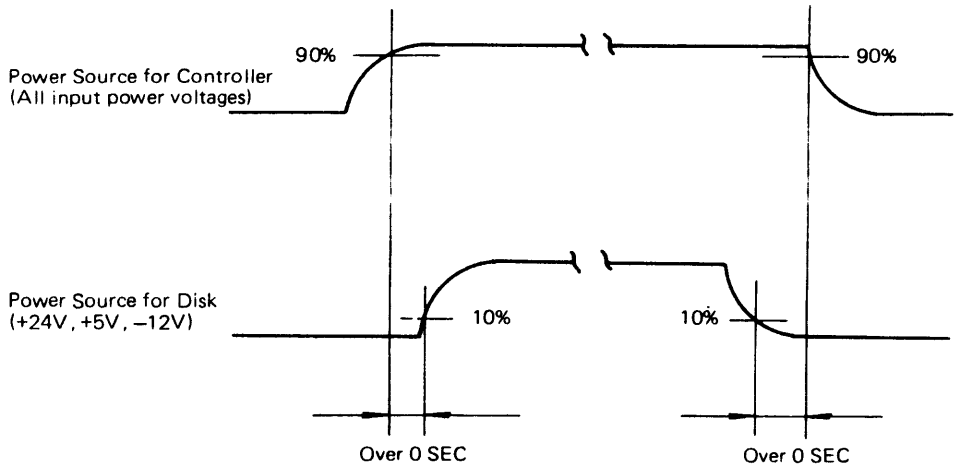
Power-on/off for the unit is described in this section.

2.2 POWER ON/OFF SEQUENCE

The 112/114 micro disk drive has no power ON/OFF switch of its own. Therefore, power ON/OFF for the micro disk drive is performed by the power ON/OFF function of the system.

If the write gate signal coming from the controller is kept OFF in advance to a power-on or power-off, a sequence of the power source (+24V, +5V, −12V) of the device is unnecessary. That is, the stored data is not destroyed and mechanical and electric errors do not occur. In order to keep the write gate signal OFF during a power-ON/OFF transition, the power source of the controller and the device must adhere to the following sequence.

(1) Basic Sequence



Power-On/Off Sequence

(2) By detecting the +5V voltage level in the drives the write gate signal is inhibited and power sequencing is unnecessary if the +5V power source for the drive is supplied from the +5V power source for the controller, and the interface signal from the controller is determined only by the +5V power source for the controller.

Section 5
Installation and Checkout

3. INSTALLATION AND CHECKOUT

3.1 GENERAL

Unpacking, installation, cable connections, configuration settings, how to install the unit into the system, etc., are described in this section.

This unit is packed so as to withstand the shocks of long distance transportation. When the difference in the storage (or shipping) environment and the unpacking environment exceeds 20°C (36°F), the carton should be allowed to stand at the unpacking site for approximately 3 hours prior to unpacking in order to avoid condensation.

3.2 UNPACKING

The device is wrapped in a polyethylene bag, and enclosed in a inner case and outer box. An exterior view of the carton is shown in Fig. 3.1.

(1) Place the unit (Note: Do not turn disk drive upside-down) near the installation area.

(2) Remove the adhesive tape on the box and open it.

(3) Remove the upper inner case and pull the unit out by grasping the base of the unit.

(4) Store packing material for possible future use.

3.3 VISUAL INSPECTION

After unpacking, check the following.

(1) There should be no crack, rust etc. that mar its appearance and integrity.

(2) All parts should be firmly fixed and there should be no loose screws, etc.

(3) The carriage lock (shipping restraint) should be in tact with no abnormalities.

(4) The duplicate media defect label should be correct.

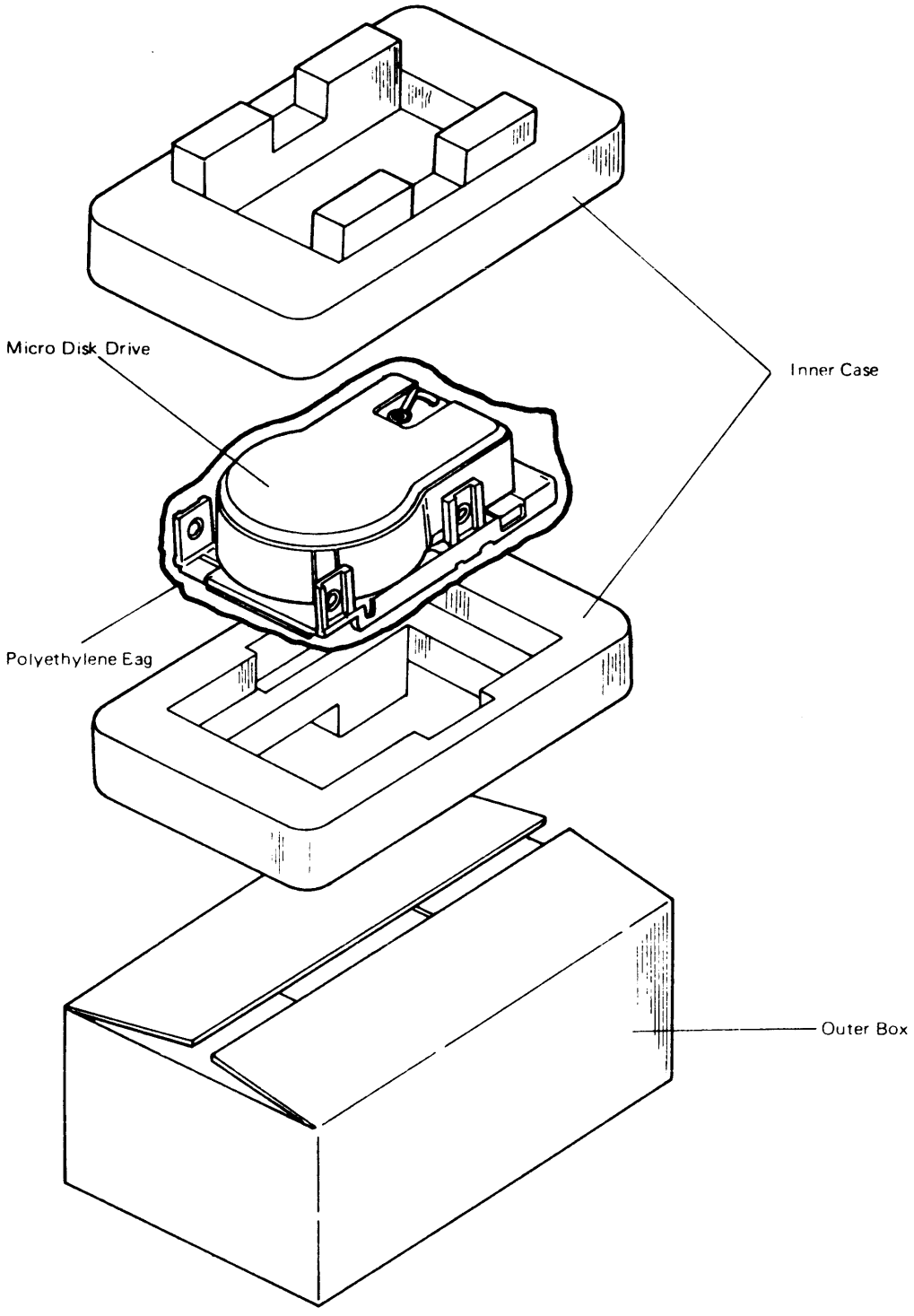


Fig. 3.1 Exterior View and Construction of Carton

3.4 MOUNTING

3.4.1 Installation in Locker

The accompanying diagram shows how to install the drive according to the dimensions and the structure of the frame. (Dimensions are in millimeters)

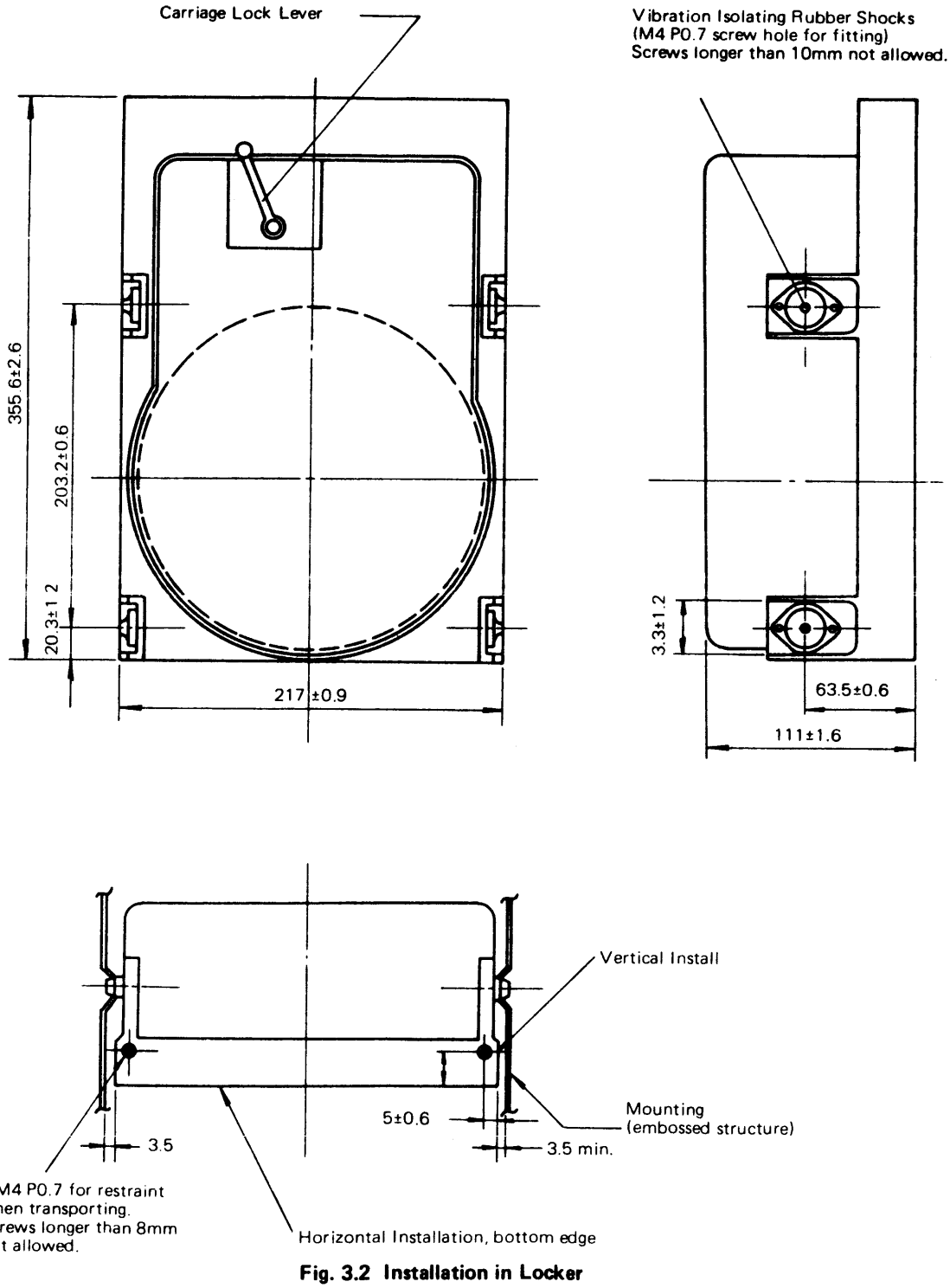


Fig. 3.2 Installation in Locker

3.4.2 Securing for Transportation

If the unit is installed in the locker during transportation, in order to prevent damage, set the carriage lock lever to LOCK.

CAUTION: Before placing the carriage restraint in the LOCK position, insure that the heads are at Track 0. Do NOT use the carriage restraint to position the heads.

(1) Fixing Carriage

Pull up the lock lever, rotate it in the direction of the arrow and fix the carriage (LOCK) or reslease it (FREE).

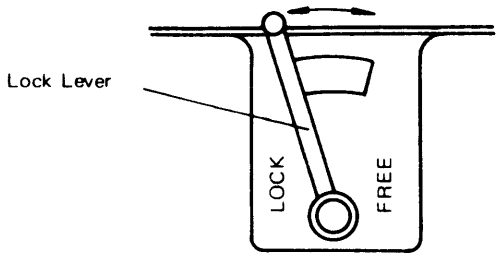


Fig. 3.3 Shows LOCK State

(2) Securing the Unit

Secure the unit to the mounting frame using the screw hole that is provided to transport the unit.

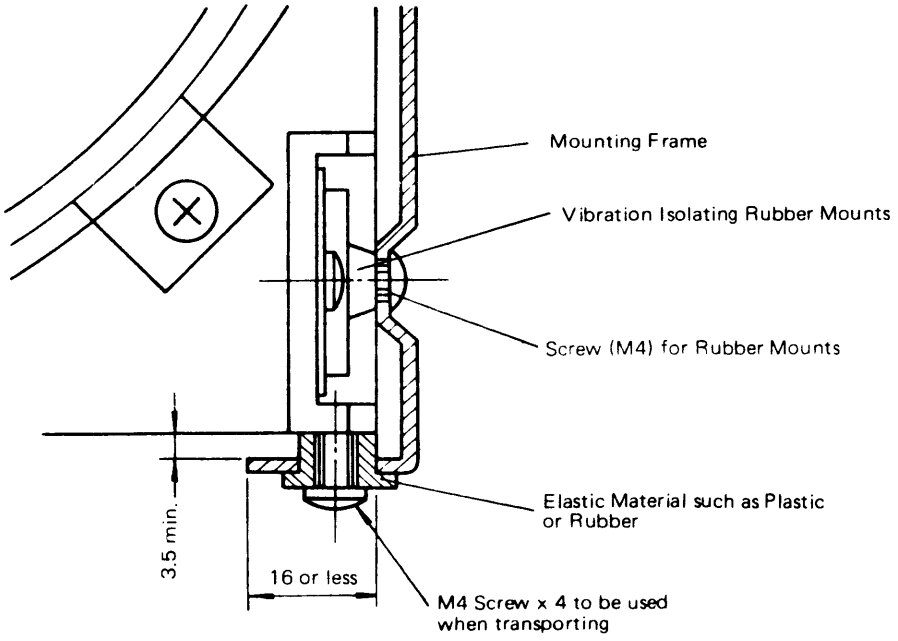
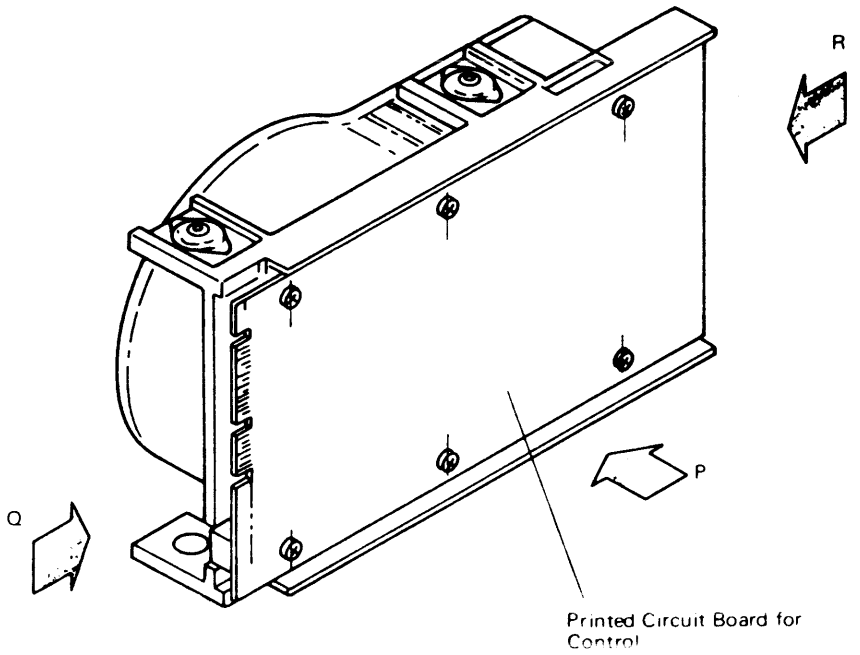


Fig. 3.4 Securing the Unit

3.4.3 Service Area

Maintenance, securing for transportation, cable connection, are accessed as shown below. When determining the service area and where to install the locker, make sure that there is enough room for maintenance work.



P side: Maintenance operations on PCB.

Q side: Cable connections.
Installation and removal of the securing screw when transporting.

R side: Accessing the carriage lock lever to secure the carriage.
Installation and removal of the securing screw when transporting.
Bad track label and a name-plate.

Fig. 3.5 Maintenance Access on the Unit

3.5 CABLE

3.5.1 Cable and Connector Specifications

Table 3.1 shows specifications recommended for cables and connectors.

Table 3.1 Cable and Connector Specification

Connector	Name	Type	Maker
A cable (50P)	Cable side connector	FCN-767J050-AU/1 or 88373-1 or 3415-0001	Fujitsu AMP 3M
	Device side card edge	–	–
	Cable	455-248-50 or 171-50	Spectrastrip Ansley
B cable (20P)	Cable side connector	FCN-767J020-AU/1 or 88373-6 or 3461-0001	Fujitsu AMP 3M
	Device side card edge	–	–
	Cable	455-248-20 or 171-20	Spectrastrip Ansley
Power cable	Cable side connector	1-480270-0	AMP
	Device side connector	1-380909-0	AMP
	Contact	60619-1	AMP
	Cable	AWG14 (+5V, RTN) AWG16(+24V, RTN) AWG20 (-5V/-7V to -16V, RTN)	–

3.5.2 Cable Connections

(1) Connection of One Unit

Fig. 3.6 is an example of only one unit connected to the controller. The unit is also operable when both Cable A and Cable B are connected at the same time.

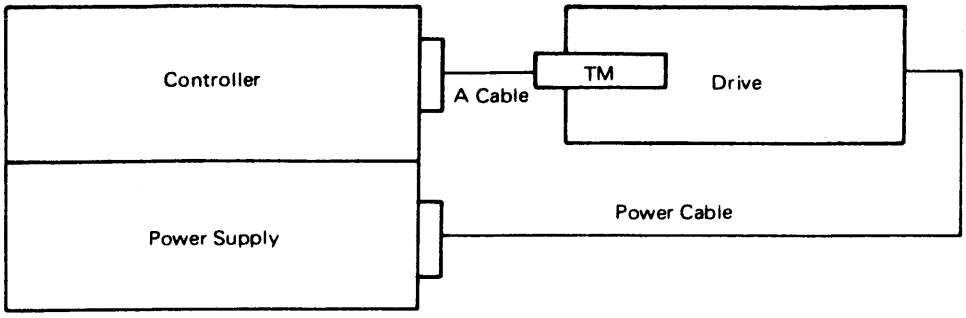


Fig. 3.6 Connection of One Unit

(2) Connection of 2 to 4 Units

When 2 to 4 units are connected, cable A (control signal) is daisy chained, and cables B (R/W signal) are connected in radial.

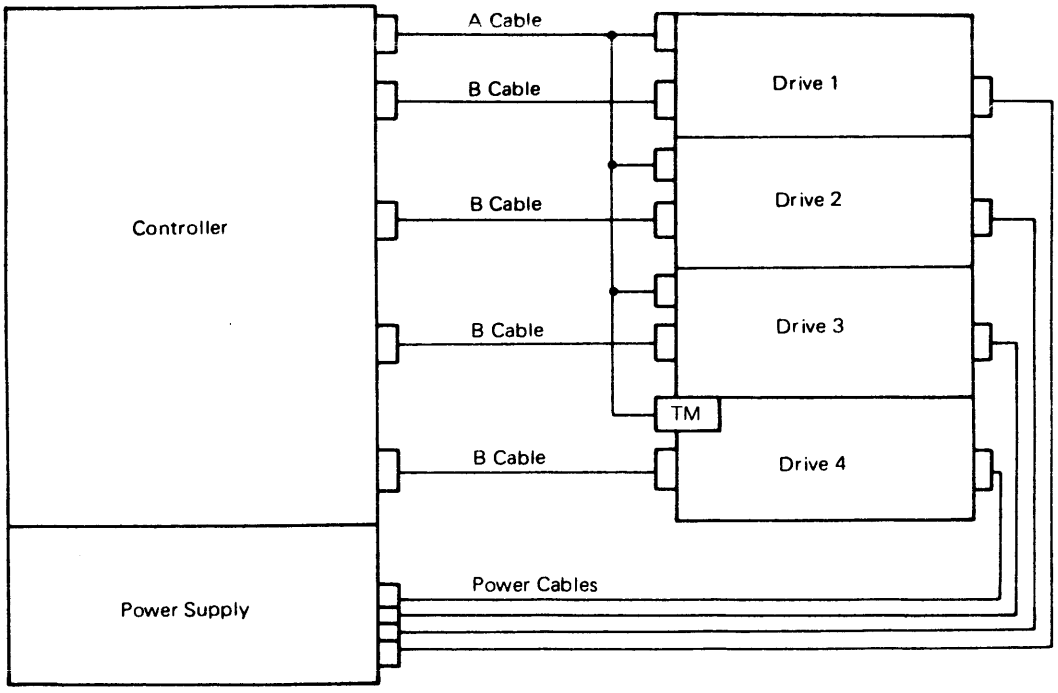


Fig. 3.7 Connection of 2 to 4 Units

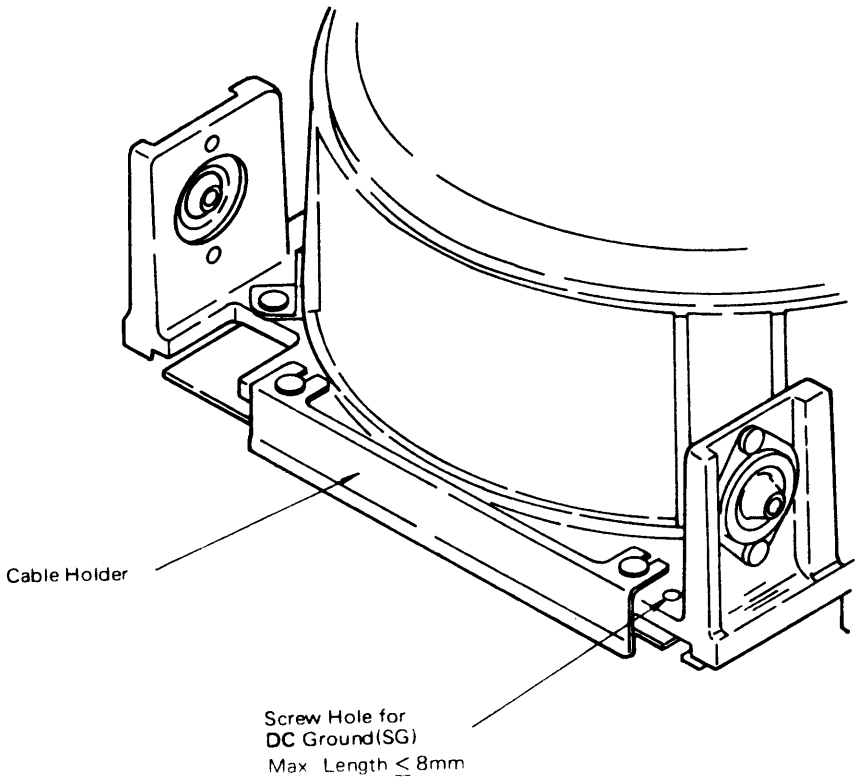
(3) Caution in Connecting the Cable

In order to reduce the influence of external electrical noise and the like, the following should be noted.

(a) The power cable and the interface cable should not be in the same plane.

(b) If the power is supplied from the system, a voltage drop would occur in the DC cable, so that each voltage must be set while measuring at the input terminal entry of the unit.

(c) If the unit is installed in a system, and or if it is installed in the 19 inch rack, firmly connect an SG ground to the hole which is provided in the casting so as to reduce the influence of external noise.
A screw hole (M4 P0.7) is provided in the casting for DC ground as shown below. Use an M4 screw less than 8mm in length.



3.6 SWITCH ARRANGEMENT

The functions and assignment procedures of the different switches on the circuit board of the 112/114 are described below.

3.6.1 Drive Select (Device Number Selection)

The drive select switch is used to select one logical unit number up to a maximum of 4 devices. Of the 4 switches, you are to turn ON one relevant switch while turning OFF the other 3. The device number selection procedures are shown in Table 3.2 and Fig. 3.8

Table 3.2 Device Number Selection

Device Number	SW3 Switch			
	Key 8	Key 7	Key 6	Key 5
1	O	X	X	X
2	X	O	X	X
3	X	X	O	X
4	X	X	X	O

O: ON
X: OFF

SW3 (Mounting Location B5)

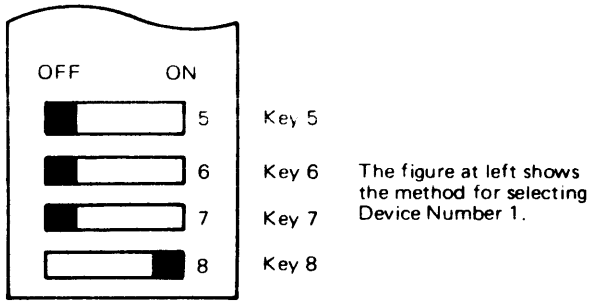


Fig. 3.8 Device Selecting Switch

3.6.2 Seek Complete

When sending the SEEK COMPLETE onto the A cable of the interface, turn ON Key 4 of SW3.
However, at this point, be sure not to leave DRIVE SELECT Key 4 in the ON status (See Fig. 3.9).

SW3 (Mounting Location B5)

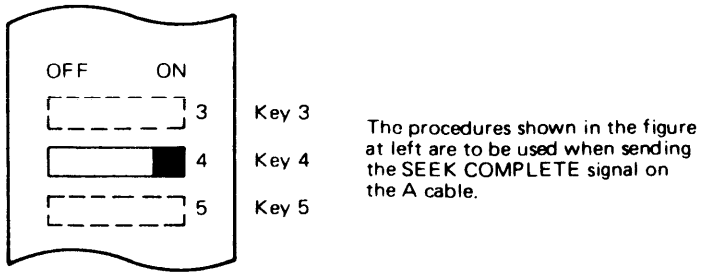


Fig. 3.9 SEEK COMPLETE Switch

3.6.3 Sector/Byte Clock

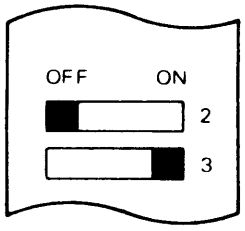
This switch is used to select either SECTOR pulses or BYTE CLOCK onto the interface cable. The switch assignment procedures are shown in Table 3.3 and Fig. 3.10 below.

Table 3.3 SECTOR/BYTE CLOCK

Signal Name	SW2 Switch	
	Key 3	Key 2
SECTOR	O	X
BYTE CLOCK	X	O

O: ON
X: OFF

SW2 (Mounting Location $\overline{A2}$)



The figure at left shows the method for sending sector pulses.

Fig. 3.10 SECTOR/BYTE CLOCK

3.6.4 Sector During the Generation of Index

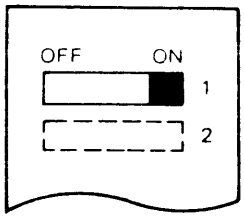
This is used to select whether or not to send the sector mark generated during the same times as Index onto the interface. The switch selection procedures are shown in Table 3.4 and Fig. 3.11.

Table 3.4 SECTOR during the Generation of INDEX

Selection Content	SW2
	Key 1
Send the SECTOR.	X
Do not send the SECTOR.	O

O: ON
X: OFF

SW2 (Mounting Location $\overline{A2}$)



The figure at left shows the switch selection procedures when INDEX and SECTOR are not sent simultaneously

Fig. 3.11 SECTOR during the Generation of INDEX

3.6.5 Write/Read Data, Write/PLO Clock

The method for sending WRITE/READ DATA and WRITE/PLO CLOCK signals onto the A cable of the interface is shown in Table 3.5 and Fig. 3.12

Table 3.5 W/R DATA and W/PLO CLOCK

Signal Name	Assigned Switch SW4
±WRITE DATA	Key 7, Key 8 ON
±READ DATA	Key 1, Key 2 ON
±WRITE CLOCK	Key 5, Key 6 ON
±PLO CLOCK	Key 3, Key 4 ON

SW4 (Mounting Location B4)

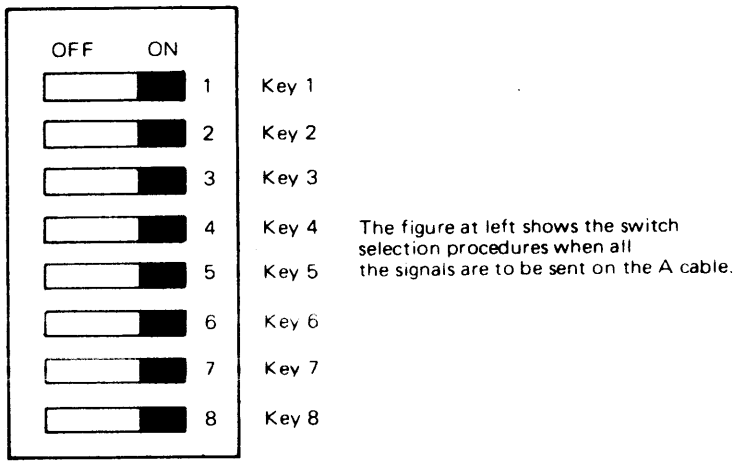


Fig. 3.12 W/R DATA and W/PLO CLOCK

3.6.6 Assigning the Number of Sectors

The number of sectors can be assigned by using a combination of the SW1 and SW2 switch keys. Each key of the respective switch corresponds to binary powers of the byte count (2^0 to 2^{11} bytes). See Table 3.6.

Table 3.6 Sector Counter Byte Table

SW1	No. of Bytes	SW2	No. of Bytes
Key 8	1	Key 8	256
Key 7	2	Key 7	512
Key 6	4	Key 6	1024
Key 5	8	Key 5	2048
Key 4	16		
Key 3	32		
Key 2	64		
Key 1	128		

The method of assigning the number of sectors is shown in Table 3.7 and Fig. 3.13, where the LAST SECTOR indicates the number of excess bytes. This also indicates that only the last sector becomes longer because of excess bytes.

Table 3.7 Method of Assigning the Number of Sectors

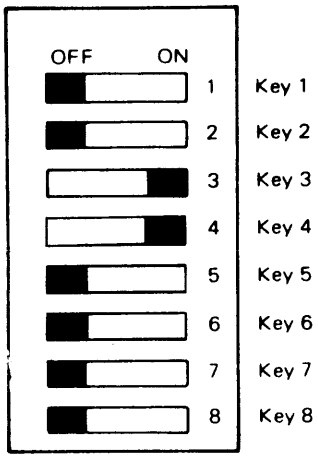
SECTORS	SW1								SW2				BYTES/SECTOR	LAST SECTOR
	8	7	6	5	4	3	2	1	8	7	6	5		
5	1	1	1	1	1	1	1	1	1	1	1	1	4095	$+3845^{+32}_{0}$
6	1	0	1	0	1	0	1	1	1	1	1	1	4053	$+2^{+32}_{0}$
7	0	1	0	0	1	0	0	1	1	0	1	1	3474	$+2^{+32}_{0}$
8	0	0	0	0	0	1	1	1	1	1	0	1	3040	0^{+32}_{0}
9	0	1	1	1	0	0	0	1	0	1	0	1	2702	$+2^{+32}_{0}$
10	0	0	0	0	0	0	0	1	1	0	0	1	2432	0^{+32}_{0}
11	0	1	0	0	0	1	0	1	0	0	0	1	2210	$+10^{+32}_{0}$
12	0	1	0	1	0	1	1	1	1	1	1	0	2026	$+8^{+32}_{0}$
13	0	1	1	1	0	0	1	0	1	1	1	0	1870	$+10^{+32}_{0}$
14	1	0	0	1	0	0	1	1	0	1	1	0	1737	$+2^{+32}_{0}$
15	1	0	1	0	1	0	1	0	0	1	1	0	1621	$+5^{+32}_{0}$
16	0	0	0	0	1	1	1	1	1	0	1	0	1520	0^{+32}_{0}
17	0	1	1	0	1	0	0	1	1	0	1	0	1430	$+10^{+32}_{0}$
18	1	1	1	0	0	0	1	0	1	0	1	0	1351	$+2^{+32}_{0}$
19	0	0	0	0	0	0	0	0	1	0	1	0	1280	0^{+32}_{0}
20	0	0	0	0	0	0	1	1	0	0	1	0	1216	0^{+32}_{0}
21	0	1	1	0	0	0	0	1	0	0	1	0	1158	$+2^{+32}_{0}$
22	1	0	0	0	1	0	1	0	0	0	1	0	1105	$+10^{+32}_{0}$
23	1	0	0	0	0	1	0	0	0	0	1	0	1057	$+9^{+32}_{0}$
24	1	0	1	0	1	1	1	1	1	1	0	0	1013	$+8^{+32}_{0}$
25	0	0	1	1	0	0	1	1	1	1	0	0	972	$+20^{+32}_{0}$
26	1	1	1	0	0	1	0	1	1	1	0	0	935	$+10^{+32}_{0}$
27	0	0	1	0	0	0	0	1	1	1	0	0	900	$+20^{+32}_{0}$
28	0	0	1	0	0	1	1	0	1	1	0	0	868	$+16^{+32}_{0}$
29	0	1	1	0	0	0	1	0	1	1	0	0	838	$+18^{+32}_{0}$
30	0	1	0	1	0	1	0	0	1	1	0	0	810	$+20^{+32}_{0}$
31	0	0	0	0	1	0	0	0	1	1	0	0	784	$+16^{+32}_{0}$
32	0	0	0	1	1	1	1	1	0	1	0	0	760	0^{+32}_{0}
33	0	0	0	0	0	1	1	1	0	1	0	0	736	$+32^{+32}_{0}$
34	1	1	0	1	0	0	1	1	0	1	0	0	715	$+10^{+32}_{0}$
35	0	1	1	0	1	1	0	1	0	1	0	0	694	$+30^{+32}_{0}$
36	1	1	0	0	0	1	0	1	0	1	0	0	675	$+20^{+32}_{0}$
37	1	0	0	0	1	0	0	1	0	1	0	0	657	$+11^{+32}_{0}$
38	0	0	0	0	0	0	0	1	0	1	0	0	640	0^{+32}_{0}
39	1	1	1	1	0	1	1	0	0	1	0	0	623	$+23^{+32}_{0}$
40	0	0	0	0	0	1	1	0	0	1	0	0	608	0^{+32}_{0}
41	1	0	0	0	1	0	1	0	0	1	0	0	593	$+7^{+32}_{0}$
42	1	1	0	0	0	0	1	0	0	1	0	0	579	$+2^{+32}_{0}$
43	1	0	1	0	1	1	0	0	0	1	0	0	565	$+25^{+32}_{0}$
44	0	0	0	1	0	1	0	0	0	1	0	0	552	$+32^{+32}_{0}$
45	0	0	1	1	1	0	0	0	0	1	0	0	540	$+20^{+32}_{0}$
46	0	0	0	0	1	0	0	0	0	1	0	0	528	$+32^{+32}_{0}$

Table 3.7 Continued

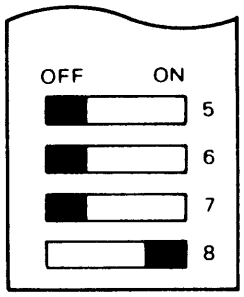
SECTORS	SW1								SW2				BYTES/SECTOR	LAST SECTOR
	8	7	6	5	4	3	2	1	8	7	6	5		
47	1	0	1	0	0	0	0	0	0	1	0	0	517	$+21^{+32}_{-0}$
48	0	1	0	1	1	1	1	1	1	0	0	0	506	$+32^{+32}_{-0}$
49	0	0	0	0	1	1	1	1	1	0	0	0	496	$+16^{+32}_{-0}$
50	0	1	1	0	0	1	1	1	1	0	0	0	486	$+20^{+32}_{-0}$
51	0	0	1	1	1	0	1	1	1	0	0	0	476	$+44^{+32}_{-0}$
52	1	1	0	0	1	0	1	1	1	0	0	0	467	$+36^{+32}_{-0}$
53	0	1	0	1	0	0	1	1	1	0	0	0	458	$+46^{+32}_{-0}$
54	0	1	0	0	0	0	1	1	1	0	0	0	450	$+20^{+32}_{-0}$
55	0	1	0	1	1	1	0	1	1	0	0	0	442	$+10^{+32}_{-0}$
56	0	1	0	0	1	1	0	1	1	0	0	0	434	$+16^{+32}_{-0}$
57	0	1	0	1	0	1	0	1	1	0	0	0	426	$+38^{+32}_{-0}$
58	1	1	0	0	0	1	0	1	1	0	0	0	419	$+18^{+32}_{-0}$
59	0	0	1	1	1	0	0	1	1	0	0	0	412	$+12^{+32}_{-0}$
60	1	0	1	0	1	0	0	1	1	0	0	0	405	$+20^{+32}_{-0}$
61	0	1	1	1	0	0	0	1	1	0	0	0	398	$+42^{+32}_{-0}$
62	0	0	0	1	0	0	0	1	1	0	0	0	392	$+16^{+32}_{-0}$
63	0	1	0	0	0	0	0	1	1	0	0	0	386	$+2^{+32}_{-0}$
64	0	0	1	1	1	1	1	0	1	0	0	0	380	0^{+32}_{-0}
65	0	1	1	0	1	1	1	0	1	0	0	0	374	$+10^{+32}_{-0}$
66	0	0	0	0	1	1	1	0	1	0	0	0	368	$+32^{+32}_{-0}$
67	0	1	0	1	0	1	1	0	1	0	0	0	362	$+66^{+32}_{-0}$
68	1	0	1	0	0	1	1	0	1	0	0	0	357	$+44^{+32}_{-0}$
69	0	0	0	0	0	1	1	0	1	0	0	0	352	$+32^{+32}_{-0}$
70	1	1	0	1	1	0	1	0	1	0	0	0	347	$+30^{+32}_{-0}$
71	0	1	1	0	1	0	1	0	1	0	0	0	342	$+38^{+32}_{-0}$
72	1	0	0	0	1	0	1	0	1	0	0	0	337	$+56^{+32}_{-0}$
73	1	0	1	1	0	0	1	0	1	0	0	0	333	$+11^{+32}_{-0}$
74	0	0	0	1	0	0	1	0	1	0	0	0	328	$+48^{+32}_{-0}$
75	0	0	1	0	0	0	1	0	1	0	0	0	324	$+20^{+32}_{-0}$
76	0	0	0	0	0	0	1	0	1	0	0	0	320	0^{+32}_{-0}
77	1	1	0	1	1	1	0	0	1	0	0	0	315	$+65^{+32}_{-0}$
78	1	1	1	0	1	1	0	0	1	0	0	0	311	$+62^{+32}_{-0}$
79	1	1	0	0	1	1	0	0	1	0	0	0	307	$+67^{+32}_{-0}$
80	0	0	0	0	1	1	0	0	1	0	0	0	304	0^{+32}_{-0}
90	0	1	1	1	0	0	0	0	1	0	0	0	270	$+20^{+32}_{-0}$
100	1	1	0	0	1	1	1	1	0	0	0	0	243	$+20^{+32}_{-0}$
110	1	0	1	1	1	0	1	1	0	0	0	0	221	$+10^{+32}_{-0}$
120	0	1	0	1	0	0	1	1	0	0	0	0	202	$+80^{+32}_{-0}$
130	1	1	0	1	1	1	0	1	0	0	0	0	187	$+10^{+32}_{-0}$
140	1	0	1	1	0	1	0	1	0	0	0	0	173	$+100^{+32}_{-0}$
150	0	1	0	0	0	1	0	1	0	0	0	0	162	$+20^{+32}_{-0}$
160	0	0	0	1	1	0	0	1	0	0	0	0	152	0^{+32}_{-0}

"0" indicates the OFF and "1" the ON status.

SW1 (Mounting Location $\overline{A}3$)



SW2 (Mounting Location $\overline{A}2$)



The figure indicates the switch selection procedures for 40 sectors.

Fig. 3.13 Method of Assigning the Number of Sectors

3.6.7 Delay SKC

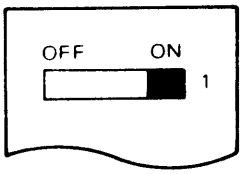
This is used to select whether or not to include settling time when SEEK COMPLETE is sent to the interface. The switch assignment procedure are shown in Table 3.8 and Fig. 3.14.

Table 3.8 DELAY SKC

Signal Name	SW3
	Key 1
Include settling time	O
Does not settling time	X

O: ON
X: OFF

SW3 (Mounting Location B5)



The figure at left shows the switch assignment procedures when sending the SKC signal which includes setting time delay provided by the drive.

Fig. 3.14 DELAY SKC

3.6.8 Controlling the Basic Drive Select Signals

Even when the relevant drives are not selected, the four basic signals (such as, INDEX, DRIVE READY, SECTOR/BYTE CLOCK and SEEK COMPLETE) can be sent to the interface cables (both A and B). The method of sending these signals is shown in Table 3.9 and Fig. 3.15.

Table 3.9 Drive Selection Control

Cable A	SW3 Key 2	Cable B	SW3 Key 3
Gate	O	Gate	O
Does not gate	X	Does not gate	X

O: ON
X: OFF

SW3 (Mounting Location B5)

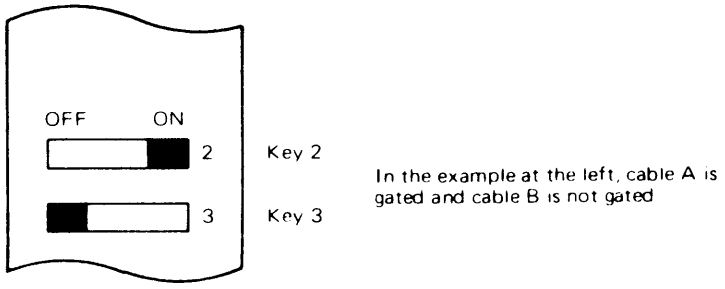


Fig. 3.15 Drive Selection Control

3.6.9 Time Margin Measurement Switch

This is a switch for measuring time margins. Set this switch to OFF only when measuring margins.

SW2 (Mounting Location $\overline{A}2$)

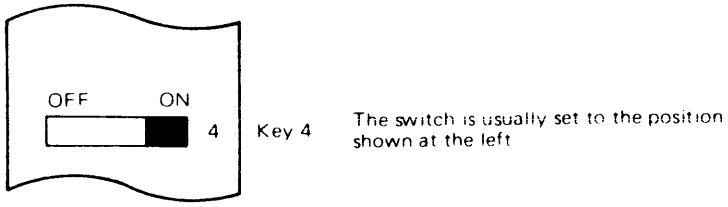
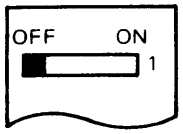


Fig. 3.16 Time Margin Measurement Switch

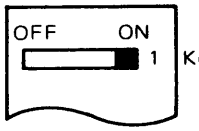
3.6.10 Timing Specification Selection

The drive utilizes SW5 (Mounting Location M3) to provide SA4000 interface compatibility.

(1) PLO Clock and Read Data



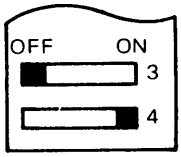
Read Data is clocked by the positive transition of PLO Clock.



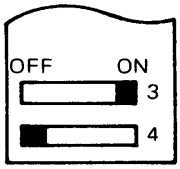
Read Data is clocked by the negative transition of PLO Clock.

(for SA4000 Controller)

(2) Direction and Step Pulse



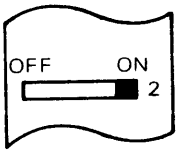
The direction signal is sampled at the drive on the leading edge of the step pulse.



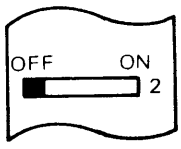
The direction signal is sampled at the drive on the trailing edge of the step pulse.

(for SA4000 Controller)

(3) Track Format Selection



Gaps in the track format are all "0".

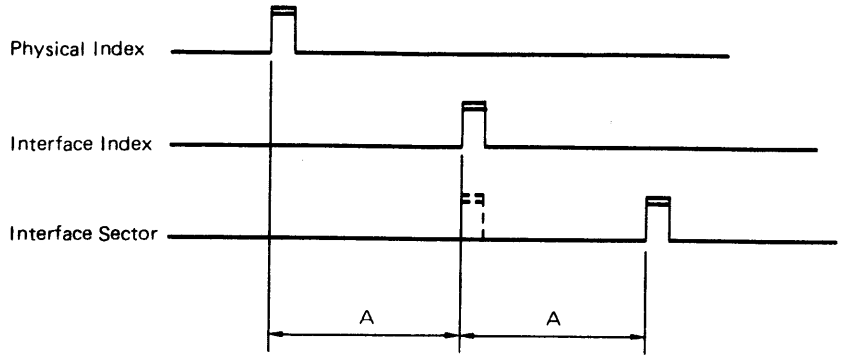


Gaps in the track format are all "1".

3.6.12 Media Error

(1) Media Error Display Method

A media defect is displayed by Cylinder Address, Head Address, Position (bytes from Physical Index) and Defect Length (bits). The maximum media defect length is 64 bytes (512 bits). The Physical Index represents the Index Pattern Division recorded on the clock track. The relationships of the Physical Index and Interface Index/Sector are shown below.



A: This represents the number of bytes of one sector.

(2) Relation of the Defective Area Display Value and the defective Sector.

(i) Calculation of the defect Area

Defect Position: B bytes

Defect Length: C bits

$C \div 8 = C' \ldots\ldots$ remainder C''

Defect Area: $B \sim B + C' \quad (C'' \leq 1)$

$B \sim B + C' + 1 \quad (2 \leq C' \leq 7)$

(ii) Calculation of a Defect Sector Number

A Defective Sector Number can be calculated by using the following formula.

$$\text{Defective sector number} = \left[\frac{X}{A}\right] - 1$$

Note 1: X: Defective position display value

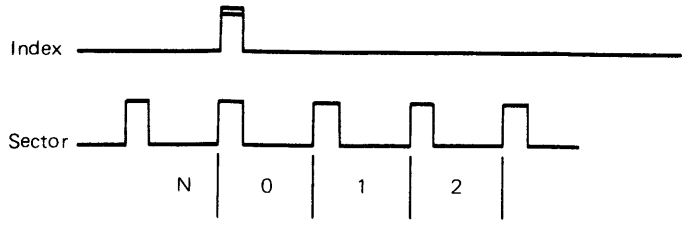
A: Number of bytes of one sector

[ ]: This indicates that all the numbers after the decimal point are to be omitted.

For example, [2.3] = 2

1: Compensates for the difference between Physical and Interface Index.

Note 2: The sector next to the index is assumed to be the 0 sector.



(3) Examples of Defect Sector Number Calculation

(i) A = 304 Bytes
B = 800 Bytes
C = 10 Bits
10 ÷ 8 = 1 . . . 2
X = 800 ~ 802

○ X = 800

$$\text{Defect Sector} = [\frac{800}{304}] - 1$$
$$= 2 - 1 = 1$$

○ X = 800

$$\text{Defect Sector} = [\frac{800}{304}] - 1$$
$$= 2 - 1 = 1$$

1 Sector is detective.

(ii) A = 304 Bytes
B = 286 Bytes
C = 480 Bits
480 ÷ 8 = 60 . . . 0
X = 286 ~ 346

○ X = 286

$$\text{Defect Sector} = [\frac{286}{304}] - 1$$
$$= 0 - 1 = -1$$

○ X = 346

$$\text{Defect Sector} = [\frac{346}{304}] - 1$$
$$= 1 - 1 = 0$$

0 Sector and N (last) Sector are defective.

Section 4
Theory of Operation

4. THEORY OF OPERATION

4.1 GENERAL

This section consists of three parts. The first concerns major assembles of the device. The second takes up the magnetic head and magnetic disk. These are part of the disk enclosure, however, they are explained below because they are closely related to the electric control portion. The last describes electric control such as interface, R/W, etc.

4.2 OPERATION OF MECHANICAL PORTION

4.2.1 Disk Enclosure

In the disk enclosure (DE), disks, spindle, actuator, heads, etc., are protected by a sealed plastic cover. Each of these parts can be seen through the plastic cover. The disk enclosure is sealed at the factory after assembly, and must not be opened in the field.

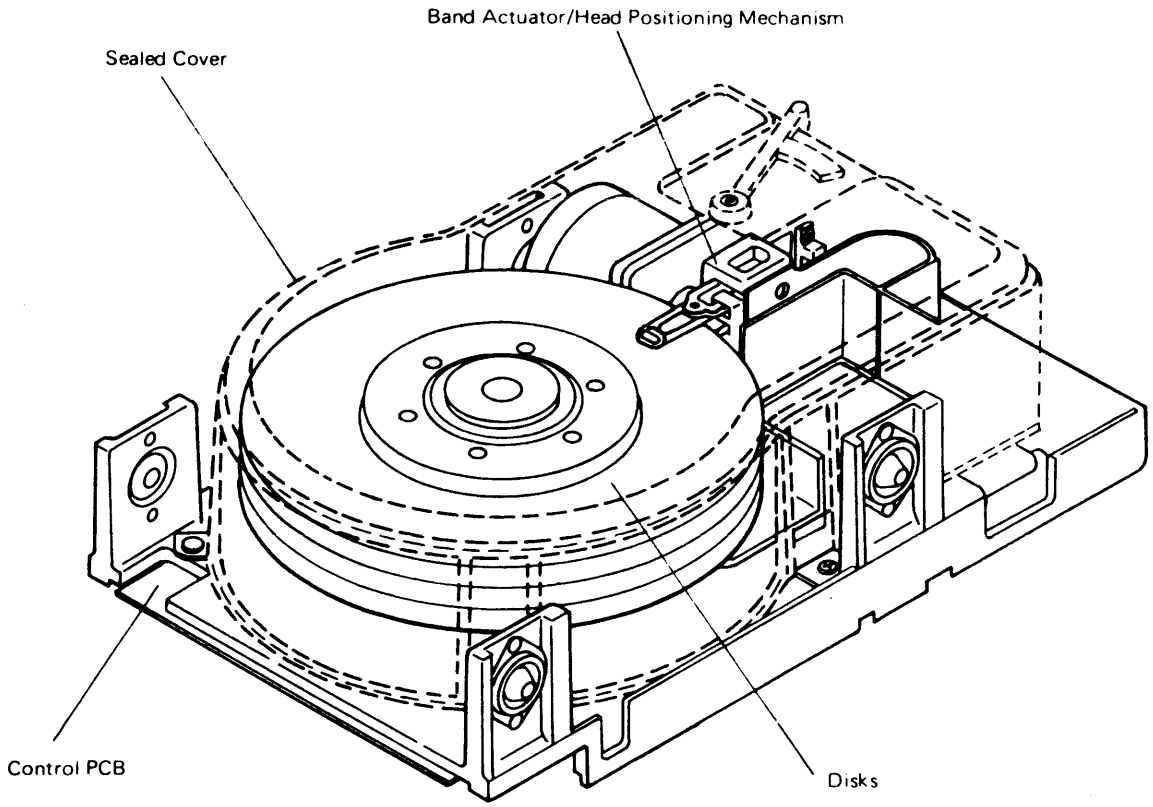


Fig. 4.1 Appearance of the Unit

4.2.2 Spindle

The disk spindle is fixed to the base of the DE from the top side.
The base is sealed to prevent the intrusion of air through the bearings. At the top of the spindle is a hub, to which recording media are fitted. A DC motor is set concentrically with the spindle to drive the disks. The spindle is grounded to the DE through an anti-static brush.

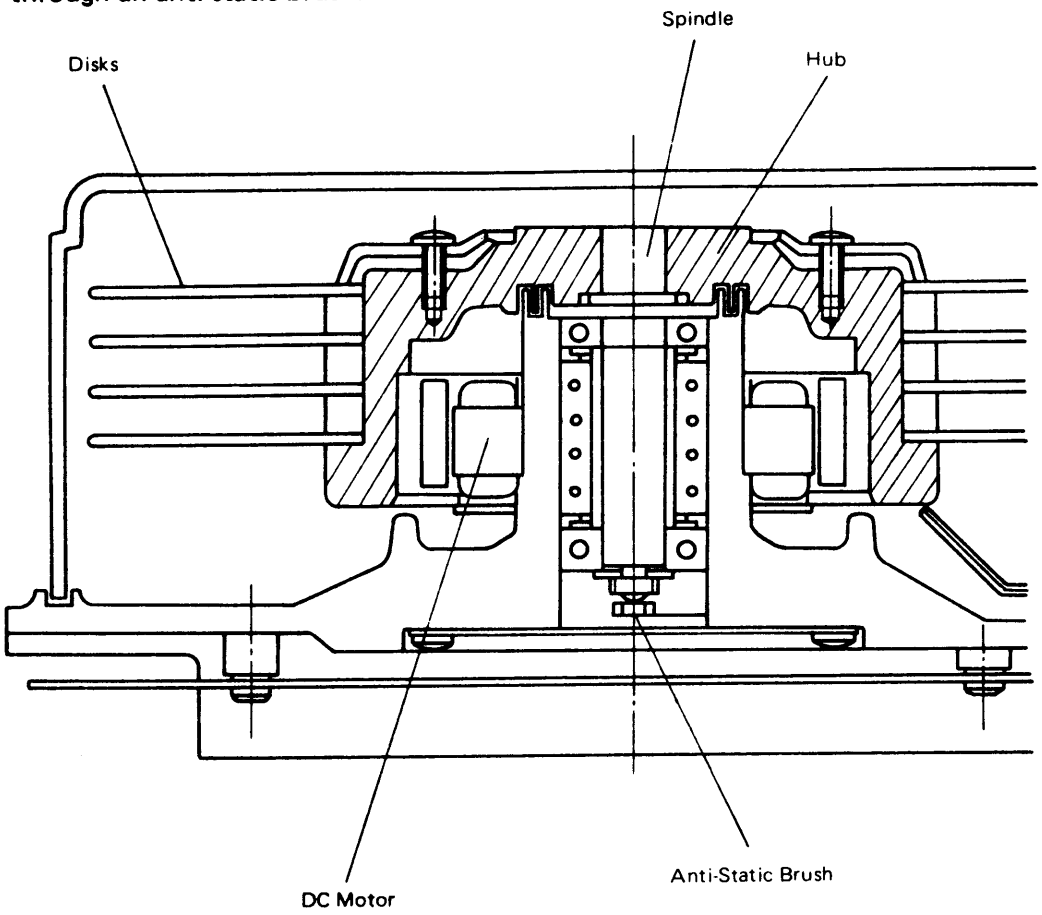


Fig. 4.2 Spindle

4.2.3 Carriage Assembly

Carriage assembly consists of a four-phase stepping motor, band actuator, viscous damper, and carriage with linear bearings. The assembly is controlled by a special driving circuit which achieves an average positioning time of 70ms. In addition to high speed, the structure of the assembly gives increased reliability.

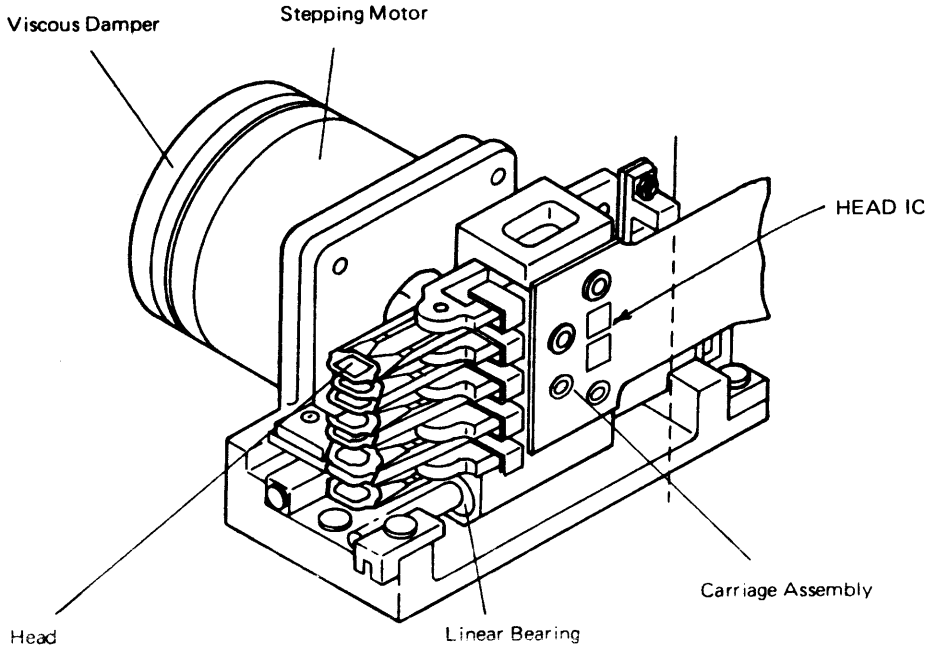


Fig. 4.3 Carriage Assembly

If the disks do not rotate, the heads rest on the disk surface. Therefore, during maintenance or when transporting the drive, the carriage must be locked to protect the heads.

4.2.4 Air Circulation in DE

The unit is provided with CSS heads which have a flying height of about 0.45 microns. Therefore, a small dust-particle could cause a head crash. For this reason the DE is perfectly sealed. There are two filters. One for breathing, the other one is for recirculation to keep the air inside the DE clean.

The filter for breathing serves:

(1) To prevent suction near the spindle when it starts rotating.

(2) To prevent the intrusion of dust into the DE, when the air pressure inside of the DE decreases due to the difference in temperature between the inside of the DE and the atmosphere.
The recirculation filter is fitted inside of the pipe which forms a closed loop in the DE. When suction occurs by virtue of the rotation of the spindle, the air in the DE circulates through the closed loop. Thus the air circulates continuously whenever the spindle is rotating to keep it clean.
These two filters can eliminate 99.97% of contaminates with a particle size larger than 0.3 micron.

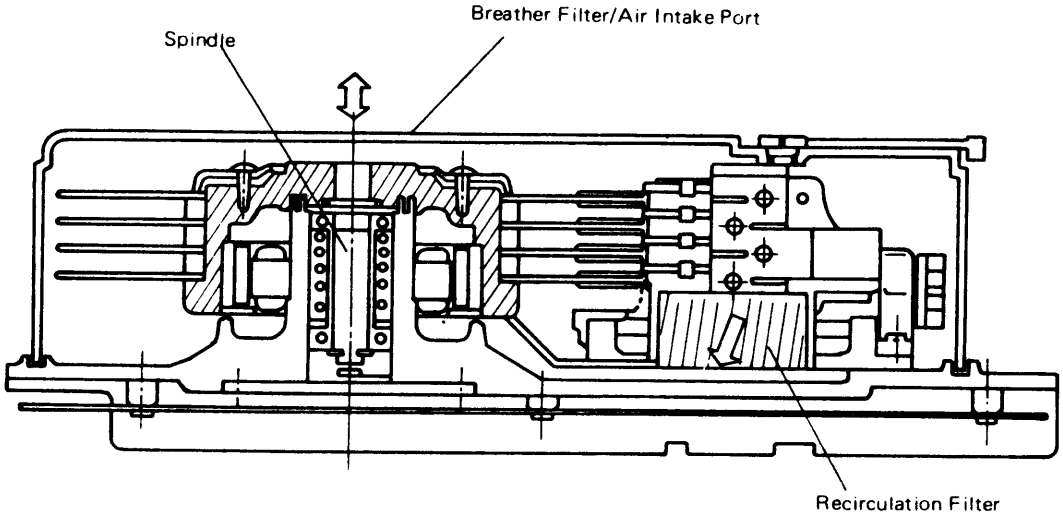


Fig. 4.4 Air Circulation Inside the DE

4.3 MAGNETIC HEADS AND RECORDING MEDIA

4.3.1 Magnetic Heads

To accomplish high density recording, CONTACT START/STOP (CSS) flying heads are employed. The heads fly on the surface air flow generated by the rotating disk. The CSS system differs from the conventional ramp load system in that the heads are always over the recording media and rest on the disk surface when the disk is not rotating.

Therefore, the head and disk make contact, and the wear caused by this contact must be minimized. For this reason, the CSS type head is lightly loaded and the surface pressure is reduced by using a tapered flat slider such as that shown in Fig. 4.6. The slider has 3 rails. The air intake end of the slider is tapered to obtain flying force by means of the air flow over the disk surface. Reads and writes are performed by a ferrite core at the rear of the head, the minimum flying height position.

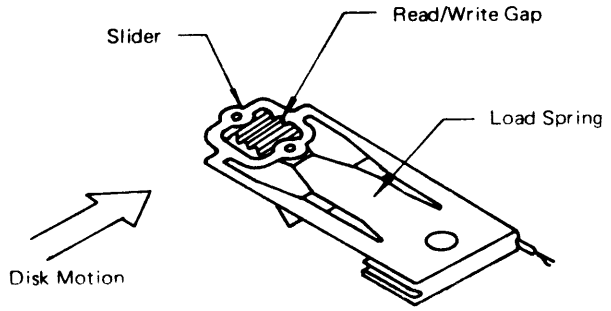


Fig. 4.5 Read/Write Head

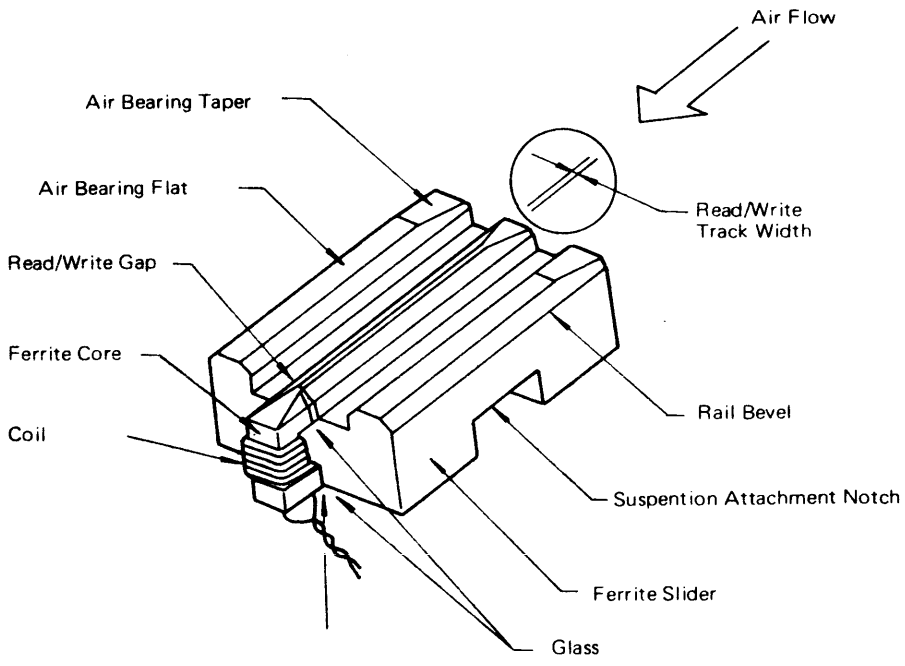
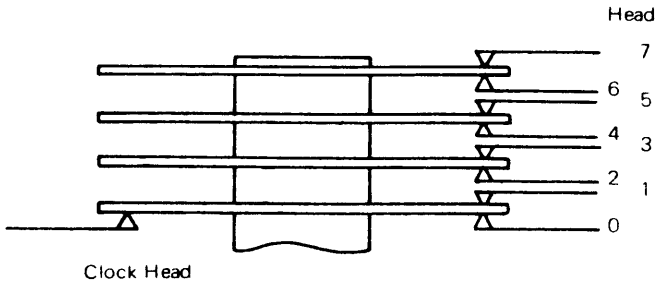


Fig. 4.6 Structure of Head Slider

4.3.2 Recording Media (Magnetic Disk)

A magnetic disk is made of an aluminum substrate on which magnetic material is coated, measures 200mm (8 inches) in diameter, and 2mm in thickness. It is used to store data. Because of the CSS characteristic of the drive, the media surface is lubricated with a special lubrication in order to prevent wear. Up to four disks are installed for a maximum storage capacity of 23.4M bytes.
The index information is stored in the outer circumference (beyond the data field) on the under side of the lowest disk.

4.3.3 Head and Surface Configuration

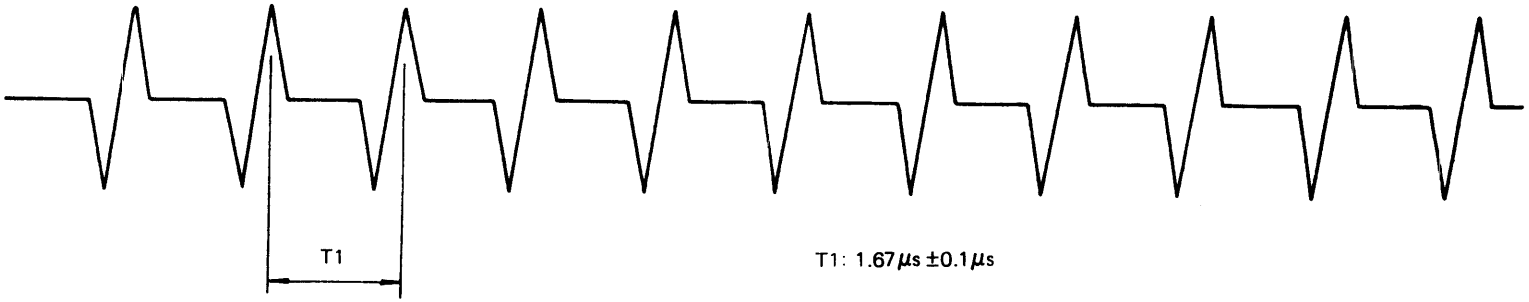


4.3.4 Clock Track Format

As was described in 4.3.2, the clock track is the outermost track on the bottom surface. It contains $12{,}000^{+32}_{-0}$ data intervals for generating clock signals as well as one index pattern.

Fig. 4.7 shows the clock signal waveform and index pattern waveform.

(1) Clock Signal Waveform



(2) Index Pattern Waveform

Fig. 4.7 Clock Signal Waveform/Index Pattern Waveform

4.4 FORMAT

4.4.1 General

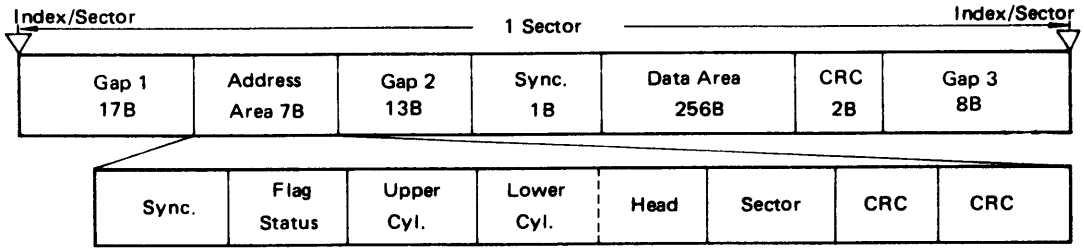
A sector (or record) is used to allocate addresses. Each sector has an address areas (AA) which ensure that the correct sector is located, and a data area (DA) in which data is stored.

The index and sector signals are used to inform the controller of the beginning of a track and sector. The sector format is determined by the control unit. On the other hand, the device must be set to generate the desired fixed length sector format by means of switches.

A fixed length format of 80 sectors is described as an example in this section.

4.4.2 Track Format

Example of a format of 80 sectors.



Note: (1) The format shown here is only an example and the construction of an optimum format compatible to the system is possible.

(2) A different SYNC BYTE pattern between the address area and the data area is permissible. A recommended pattern is "0E" and "09" (Hex.) respectively.

4.4.3 Detail of The Format

(1) GAP 1
The gap allows for displacement of the head, circuit tolerances, and write to read transient after write operation under worst case conditions. The gap must be a minimum of 16 bytes, in which all "0"s are written.

(2) SYNC BYTE
This shows the starting point of the address area.
A recommended pattern is "0E" (Hex.).

(3) FLAG STATUS/LOGICAL UNIT
This shows the status of each sector (record).
Normal record, spare record, or replacement record may be indicated here. However, its meaning is defined by the control unit.

(4) UPPER CYLINDER ADDRESS/LOWER CYLINDER ADDRESS
This indicates the cylinder address on the track.

(5) HEAD ADDRESS
This indicates the head address on the track.

(6) SECTOR ADDRESS
This indicates the sector (record) address on the track.

(7) CRC (CYCLIC REDUNDANCY CHECK)
This is the area which checks whether the data was correctly read.

(8) GAP 2
This is an area where a write splice would occur when the data area of the sector was updated. Since the read circuit may be reactivated after the write Splice area, all "0" must be written in this 12 or more Byte area. The read circuit requires an "0"s area to synchronize read circuits.

(9) SYNC BYTE
Indicates the beginning of the data area.

(10) DATA AREA
This is the area where data is written and read.

(11) CRC
See (7)

(12) GAP 3
This is pad time required by the control unit. All "0"s are written in this 6 Byte area.

4.5 INTERFACE

4.5.1 General

Logical and physical conditions for the reception/transmission of signals in the interface of a 112/114 micro disk drive are described in this chapter.

(1) Connection
There are two connectors for external connection on this unit. These are called "A" and "B" connectors. The cables connected to these are called cable "A" and cable "B". "A" cables may be connected in daisy chain. When this configuration is utilized, the terminator must be removed from all but the last drive. See Fig. 3.7. The "B" cable is connected in a radial fashion. Therefore, the control unit, requires "B" cables and connectors in proportion to the number of drives connected.

(2) Timing Specification
The timing specifications for signals are referenced at the connector position of the unit. Consequently, with regard to the signal timing from the unit, time lag of the cable, and time lag due to the number of circuit stages in the control unit must be considered.

(3) Interface Transmission Level
There are two types of interface drivers and receivers used. For the high frequency signal lines, balanced line differential devices are used. These lines are indicated by "(1 pair)" in the diagrams below. The control and select lines are TTL level and 0 volt is active or true.

4.5.2 Type and Name of Signal Line

(1) A Cable Signal Line

Controller Side		Drive Side	
(3)	HEAD SELECT 0 ~ 2	INDEX	(1)
		READY	(1)
(4)	DRIVE SELECT 1 ~ 4		
(1)	DIRECTION	SECTOR/BYTE CLOCK	(1)
(1)	STEP	WRITE FAULT	(1)
(1)	FAULT CLEAR	TRACK 0	(1)
(1)	WRITE GATE		
		(SEEK COMPLETE)	(1)*
(1)	READ GATE		
*(1 pair)	WRITE DATA	READ DATA	(1 pair)*
*(1 pair)	WRITE CLOCK	PLO CLOCK	(1 pair)*
12 line + 2 pairs		6 line + 2 pairs	

* This signal line is connected by a switch setting on the PCB.

(2) B Cable Signal Line

		INDEX	(1)
		READY	(1)
		SECTOR/BYTE CLOCK	(1)
		SEEK COMPLETE	(1)
(1 pair)	WRITE DATA	READ DATA	(1 pair)
(1 pair)	WRITE CLOCK	PLO CLOCK	(1 pair)
2 pairs		4 line + 2 pairs	

4.5.3 Signal Lines

(1) Input Signals

(a) HEAD SELECT 0 ~ 2
These binary coded signal lines select one of eight data heads positioned in the disk drive.

(b) DRIVE SELECT 1 ~ 4
These signal lines enable the input/output signals of the disk drive having a matching logical unit number. Each line selects one drive. The signal line of DRIVE SELECT 4 can be changed to the SEEK COMPLETE signal by a switch setting on the PCB.

(c) DIRECTION
This indicates the seek direction of the data heads when STEP PULSES are sent to the disk drive. When this signal is TRUE, it causes a seek in the inner direction. And if this signal is FALSE, this causes a seek in the outer direction (Toward track 0).

(d) STEP
This signal triggers the carriage to move the data heads one track in the direction indicated by the DIRECTION signal. The following three step modes are provided.

i) Controlled Step Mode
If the step pulse rate is 1kHz or less, the drive performs a seek one track in response to one STEP pulse from the controller.

ii) Slave Step Mode
If the step pulse rate is more than 3kHz but less than 3MHz the drive does not perform SEEK individually in response to each STEP signal from the controller, but rather starts the seek operation after receiving all STEP pulses from the controller. The drive will then move the heads at high speed to the desired track according to an ideal velocity curve stored in ROM.
When the SEEK operation is finished, the drive responds by sending the SEEK COMPLETE signal.

Note: STEP RATE of 1kHz to 3kHz is prohibited.

iii) Return to Zero Mode
When the drive has received more than 255 step pulses in the slave step mode, it performs a SEEK at normal speed to TRACK 0.

(e) FAULT CLEAR
This signal line resets the write fault latch. The width of the pulse must be greater than 100ns.

(f) WRITE GATE
This signal line gates write current to the selected data head.

(g) READ GATE
This signal line gates read data from the selected data head to the data separator. Separated READ DATA and READ CLOCK are then provided to the interface. READ GATE is valid when 5.0μs (6-byte) have elapsed after READ GATE is active.

(h) WRITE DATA (Balanced Transmission)
This is the write data signal in NRZ format.
The signal is sent out by the controller using balanced line transmission levels.
The WRITE DATA signal is synchronized by the trailing edge of WRITE CLOCK IN THE DRIVE. WRITE DATA may be input to either the A or B cable depending on the switch setting on the PCB.

(i) WRITE CLOCK (Balanced Transmission)
This is the WRITE CLOCK signal from the controller synchronized with WRITE DATA. WRITE CLOCK may be input to either the A or B cable dependings on the switch setting on the PCB. This signal is derived from the PLO Clock generated in the drive and sent to the controller.

(2) Output Signals

(a) Index
This pulse is sent out at the rate of once per revolution of the disks. The width of a pulse is 0.8μs. This signal is available to both the A and B cables.

(b) Ready
This signal indicates that the drive is selected and the disks are rotating at the correct speed. (The PLO circuit synchronizes with the speed of the disk). This signal is available to both the A and B cables.

(c) SECTOR (BYTE CLOCK)
Either SECTOR Pulses or BYTE CLOCK is available through the selection of a switch on the PCB on the drive. This signal is available to both the A and B cables.

i) BYTE CLOCK
This is a pulse which occurs $24{,}320^{+32}_{-0}$ times on the track. The width of pulse is 0.42μs.

ii) SECTOR PULSE
The number of SECTOR pulses which occur per revolution of the disks is switch selectable. The pulse is generated by counting the number of bytes within one sector. One sector may contain a maximum of 4,095 bytes. The width of this pulse is 0.8μs.

(d) TRACK 0
This indicates that the data heads are at Track 0.

(e) WRITE FAULT
This indicates that one of the following fault conditions occurred during WRITE. The WRITE FAULT is retained until it is reset by a FAULT CLEAR pulse.
i) WRITE GATE is sent out when the drive is not READY.
ii) WRITE GATE and READ GATE are sent at the same time.
iii) WRITE GATE is sent when two Head ICs are selected at the same time.
iv) WRITE GATE is sent when SKC (seek complete) is false.
v) During WRITE, a normal write current does not flow to the data head.

(f) READ DATA (Balanced Transmission)
These lines transmit the recovered data in the form of NRZ data synchronized with PLO clock. The READ DATA becomes valid 5.0μs after the leading edge of READ GATE. READ DATA is available to both the A and B cables when enabled by a switch on the PCB.

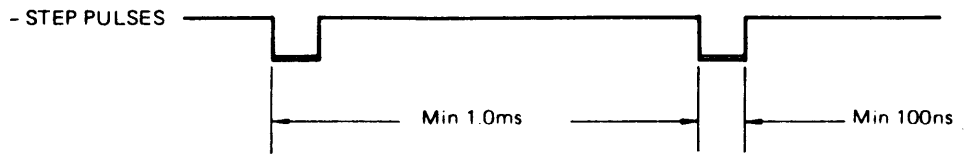
(g) PLO CLOCK (Balanced Transmission)
This pulse is sent out every other bit. When READ GATE is false, the PLO CLOCK is synchronized with the pulse read from the clock track. When READ GATE is true, the PLO is synchronized with the READ DATA from the data head. The controller uses the PLO CLOCK during a write operation as WRITE CLOCK. PLO CLOCK is available to both the A and B cables when enabled by a switch on the PCB. This pulse is selectable by a switch key to provide a normal or inverted triggering.

(h) SEEK COMPLETE
The SEEK COMPLETE signal indicates that the selected data head in the drive is positioned over the required track. This signal may contain the settling time for the seek operation. A READ/WRITE operation is legal the instant this signal turns TRUE. This signal is available to both the A and B cables, however, in case of CNA it is enabled by a switch key on the PCB.

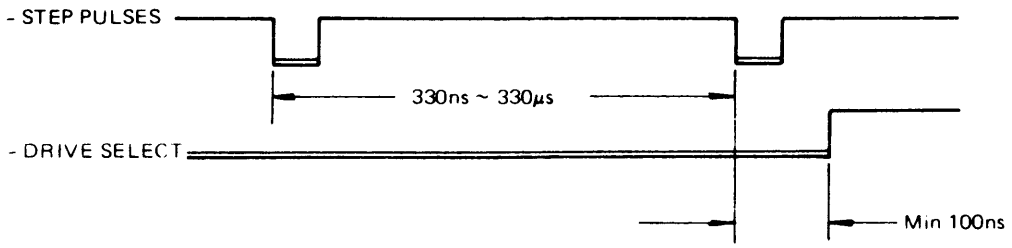
4.5.4 Timing Specifications

(1) SEEK Timing

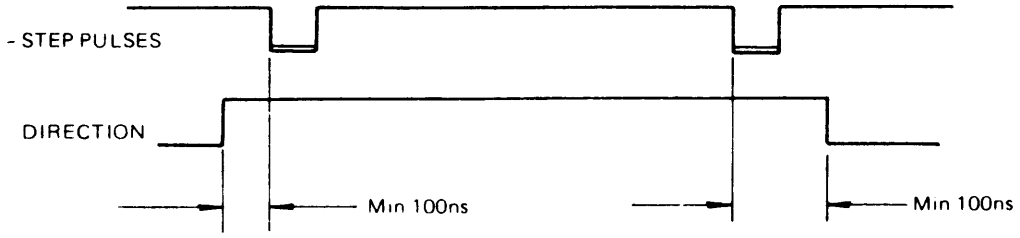
CONTROLLED STEP MODE



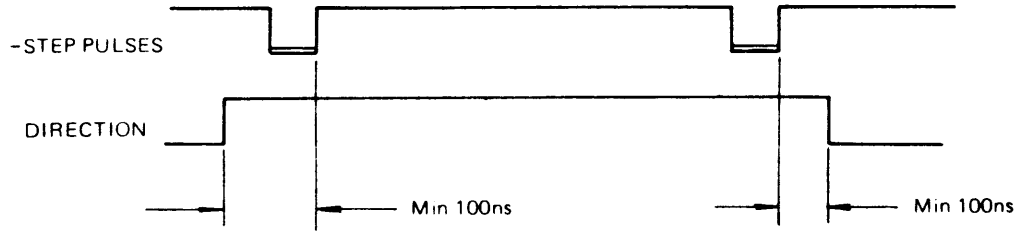
SLAVE STEP MODE



(i) Key 3 - OFF and key 4 - ON on SW5

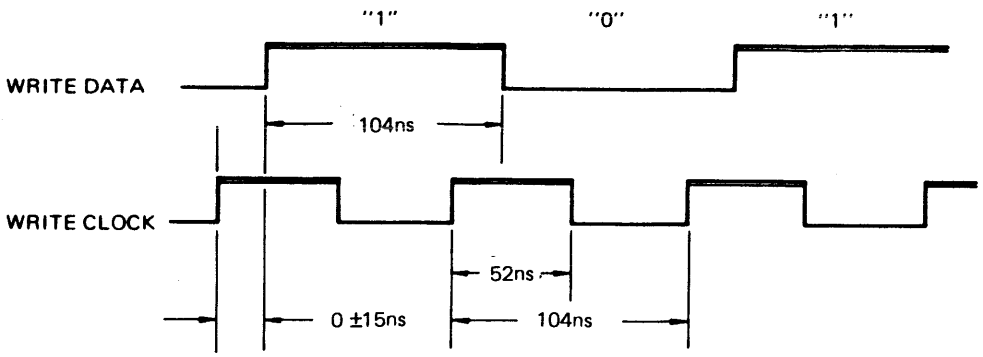


(ii) Key 3 - ON and key 4 - OFF on SW5



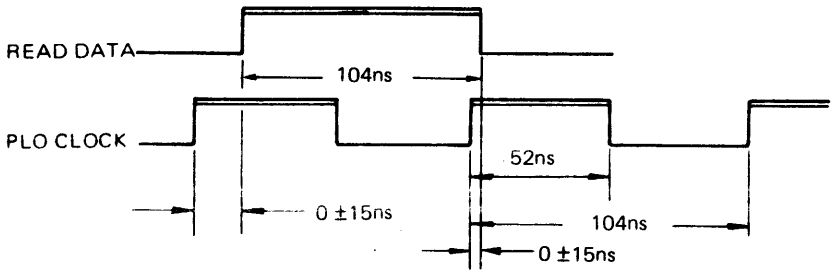
(2) WRITE/READ DATA Timing

WRITE DATA, WRITE CLOCK

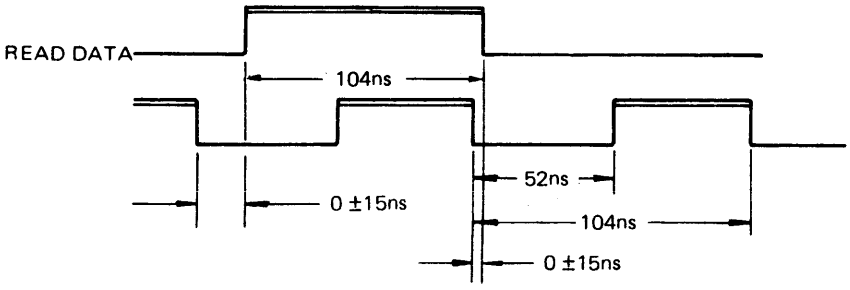


READ DATA, PLO CLOCK

(i) Key 1 - OFF on SW5

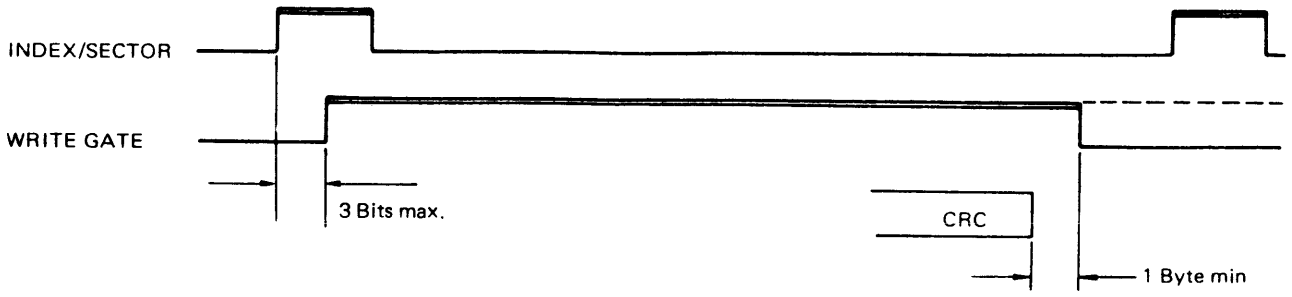


(ii) Key 1 - ON on SW5

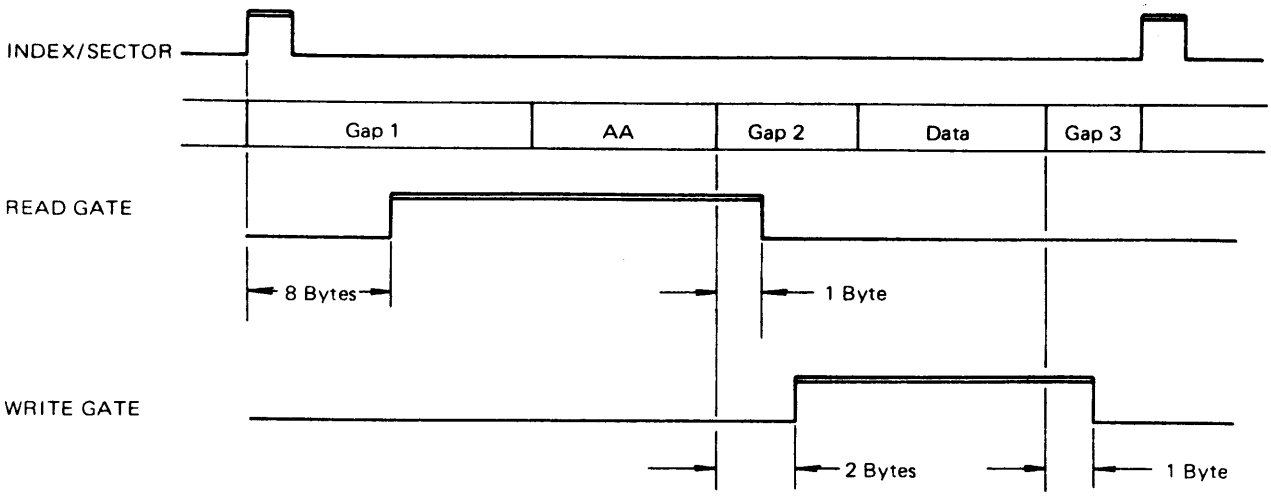


4.5.5 Format Timing Specification

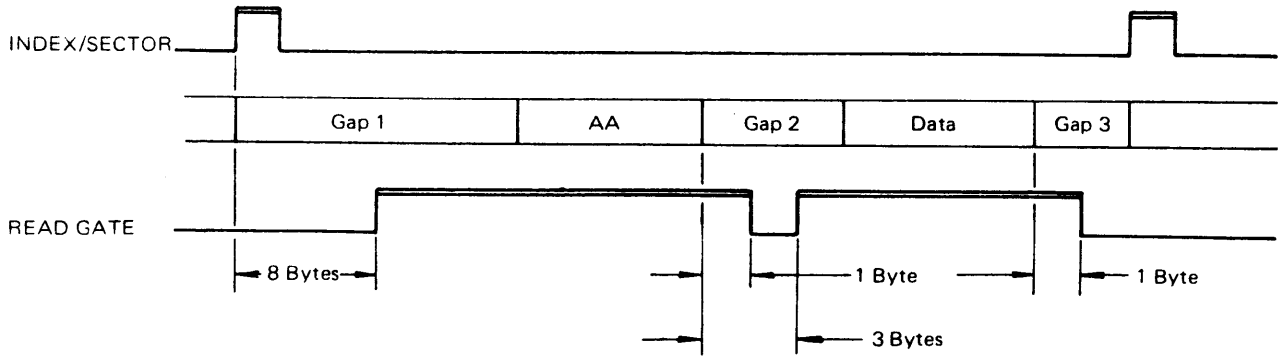
(1) Format Write



(2) Data Write



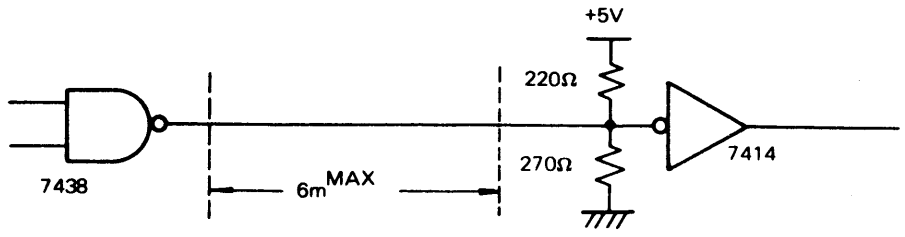
(3) Data Read



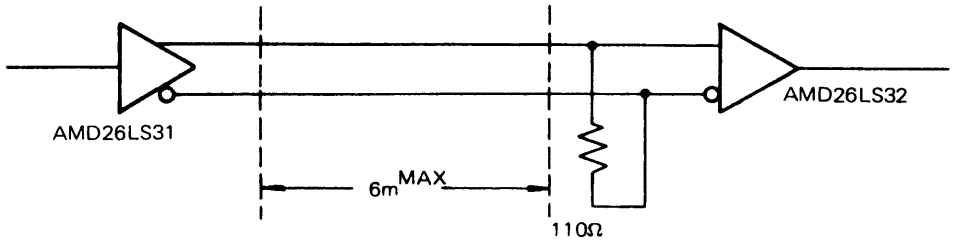
4.5.6 Driver/Receiver

Both types of Driver/Receivers used on the drive are shown in the following diagram. The maximum cable length specification includes all cables from the controller to the last drive when the A cable is daisy chained.

Control signal (TTL)



R/W signal (Balanced Transmission)



R/W signal (Balanced Transmission)

4.5.7 Pin Assignment in Connectors

CNA

1	GND	2	-HEAD SELECT 0
3	"	4	" 1
5	"	6	" 2
7	"	8	SPARE
9	"	10	-INDEX
11	"	12	-READY
13	"	14	-SECTOR/BYTE CLOCK
15	"	16	-DRIVE SELECT 1
17	"	18	" 2
19	"	20	" 3
21	"	22	" 4
23	"	24	-DIRECTION
25	"	26	-STEP
27	"	28	-FAULT CLEAR
29	"	30	-WRITE GATE
31	"	32	-TRACK 0
33	"	34	-WRITE FAULT
35	"	36	-READ GATE
37	"	38	GND
39	+WRITE DATA	40	-WRITE DATA

CNA (continued)

41	GND	42	-WRITE CLOCK
43	+WRITE CLOCK	44	GND
45	+PLO CLOCK	46	-PLO CLOCK
47	GND	48	+READ DATA
49	-READ DATA	50	GND

Key slot: Between 8P and 10P.

CNB

1	-INDEX	2	GND
3	-READY	4	"
5	-SECTOR/BYTE CLOCK	6	"
7	-SEEK COMPLETE	8	"
9	+WRITE DATA	10	-WRITE DATA
11	GND	12	+WRITE CLOCK
13	-WRITE CLOCK	14	GND
15	+PLO CLOCK	16	-PLO CLOCK
17	GND	18	+READ DATA
19	-READ DATA	20	GND

Key slot: Between 8P and 10P.

CNC

1	+24V	2	+24V RTN
3	−12V RTN	4	−12V
5	+5V	6	+5V RTN

4.6 ELECTRIC CIRCUIT OPERATION

4.6.1 Block Diagram

The block diagram for the electric circuit is shown in Fig. 4.8.

4.6.2 Start/Stop Circuit

When all DC voltages are applied to the unit, the brake relay is opened and the driving circuit of the DC spindle motor is enabled, thus turning the disks. The speed of the spindle motor is monitored by an internal timer. When the disks are rotating at the correct speed, the stepping motor is energized, and the SEEK COMPLETE and the READY signals are sent to the interface. When the power is turned off, the brake relay is closed, and the DC motor is connected to the brake resistor from the driving circuit. This brakes the DC motor and the disk comes to a complete stop in about 25 seconds.

When power is applied to the circuit, a recalibrate to track zero sequence is initiated automatically, and heads are located at cylinder 0 before the Ready Signal goes true.

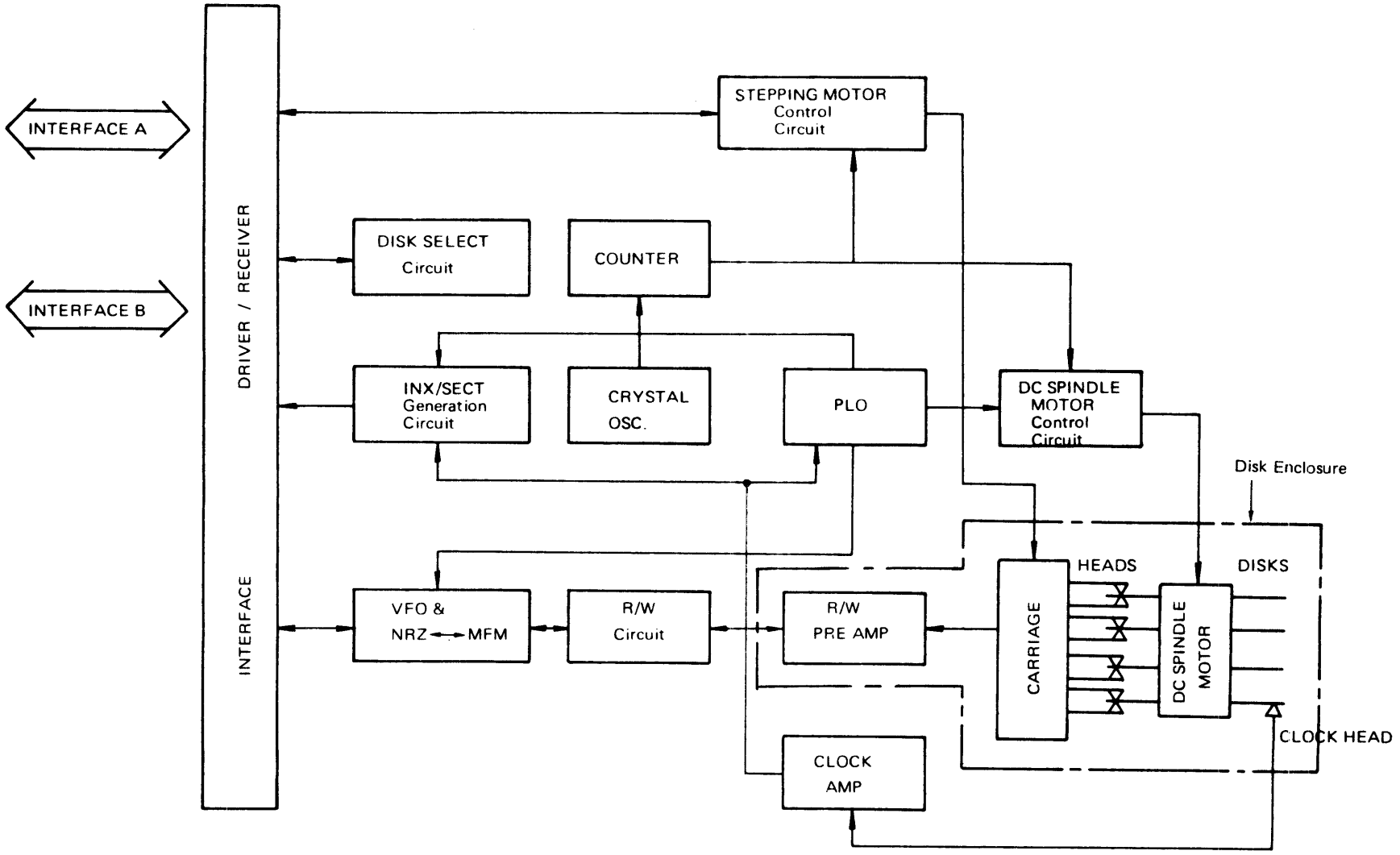


Fig. 4.8 Block Diagram

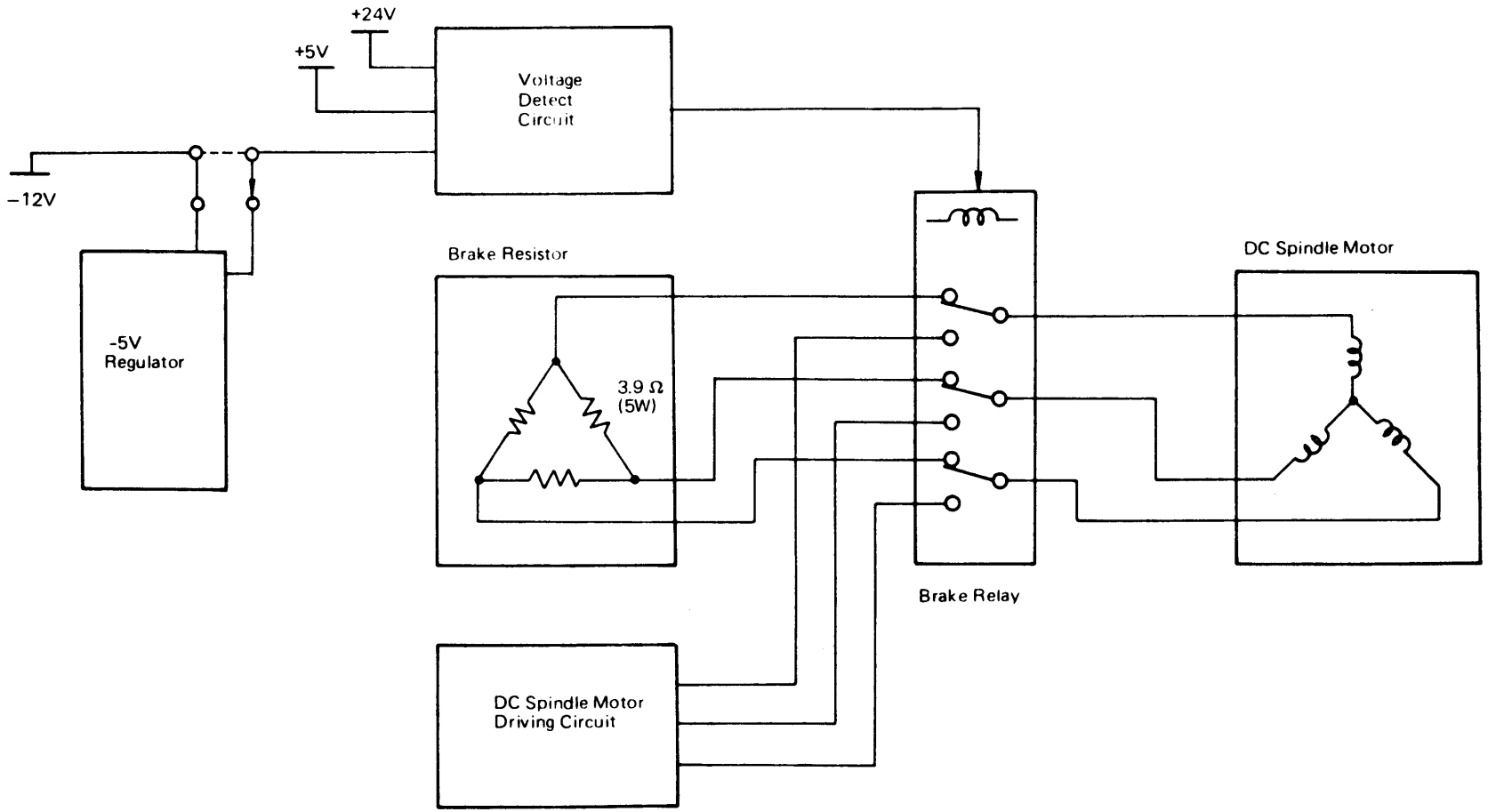


Fig. 4.9 Start/Stop Circuit Block Diagram

4.6.3 DC Spindle Motor Driving Circuit

The integral DC spindle motor consists of 4-poles with a 3-phase outer rotor. The detection of the rotation angle is conducted by three hall-effect elements fitted into the motor.

The motor driving circuit controls the coil current of the motor by sensing the three pairs of output signals from the hall-effect elements. The driving circuit also serves to detect the coil current of the motor in order to regulate the current required during start-up, and if the value exceeds specification, the circuit turns off the coil current. Fig. 4.10 shows the block diagram of the DC spindle motor driving circuit. Fig. 4.11 shows the timing chart.

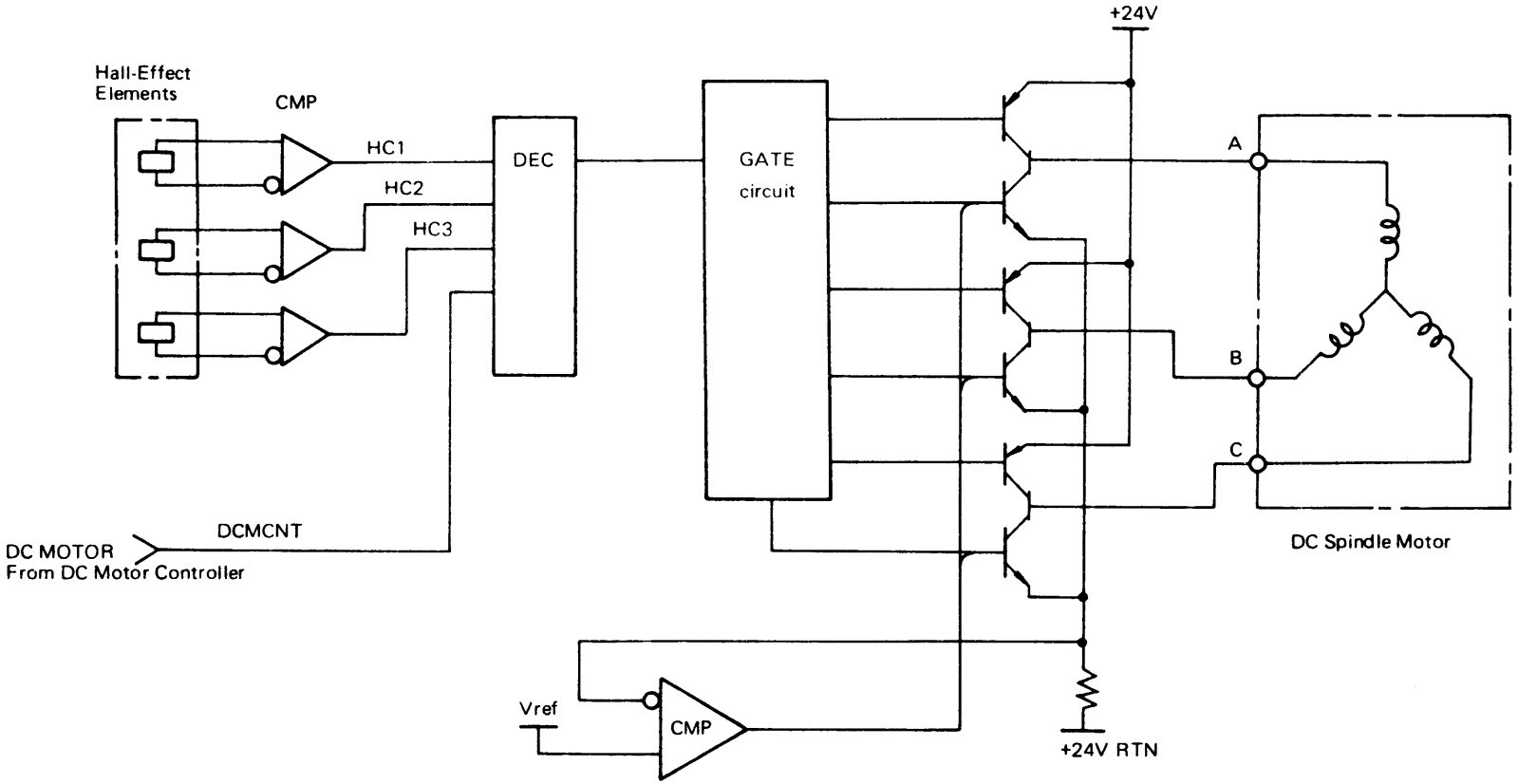
4.6.4 DC Spindle Motor Controller

The DC spindle motor controller controls the rotational speed so that it falls within the range 2964 rpm ±2% by comparing the reference frequency of signals generated by the internal oscillator with the frequency of clock signals from the clock head on the lower disk.

Fig. 4.12 shows the block diagram of the DC spindle motor controller, and Fig. 4.13 shows the timing chart.

4.6.5 Unit Select Operation

The unit may be configured as logical unit number 1, 2, 3 or 4 by setting the proper switch keys on the PCB. The select operation enables the interface of the drive with the logical unit designated by the controller. The drive is selected when the logical unit number compares with the drive select 1 to 4 signals from the controller. Refer to Section 3.6.1 for the setting procedure.



Note: DCMCNT is the signal which controls the speed of the DC spindle motor.
When DCMCNT is logical "1", it blocks current to the motor.
When DCMCNT is logical "0", it permits the current to flow.

Fig. 4.10 DC Spindle Motor Driving Circuit Block Diagram

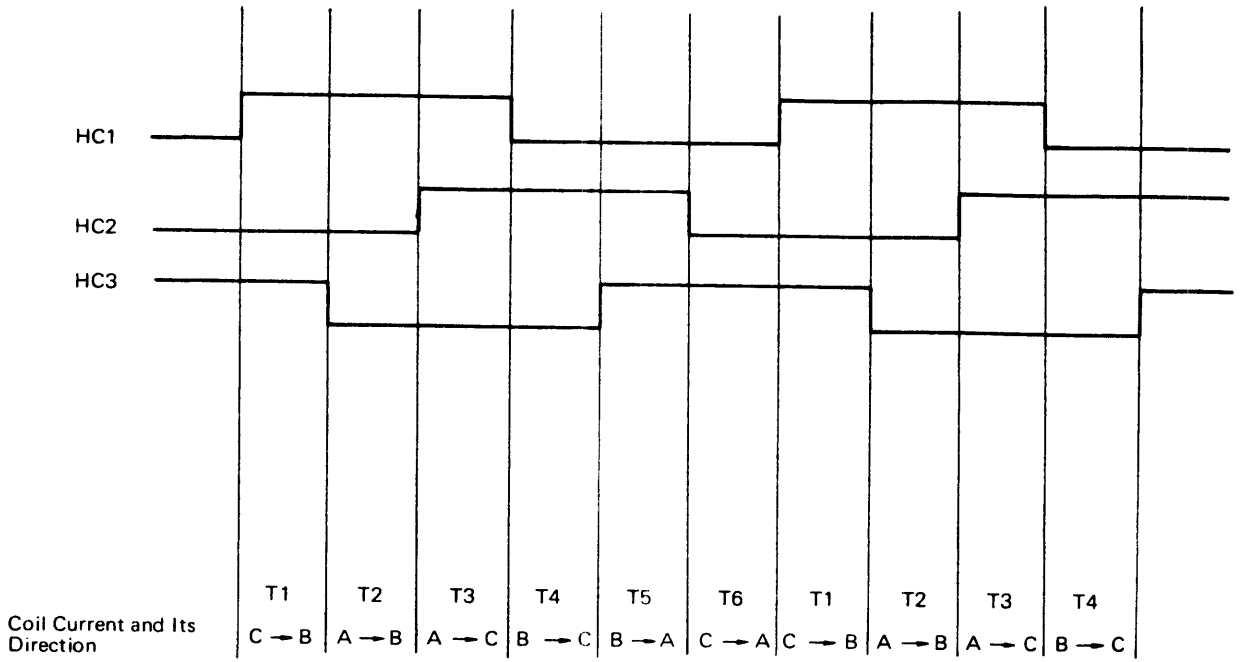


Fig. 4.11 DC Spindle Motor Driving Circuit Timing Chart

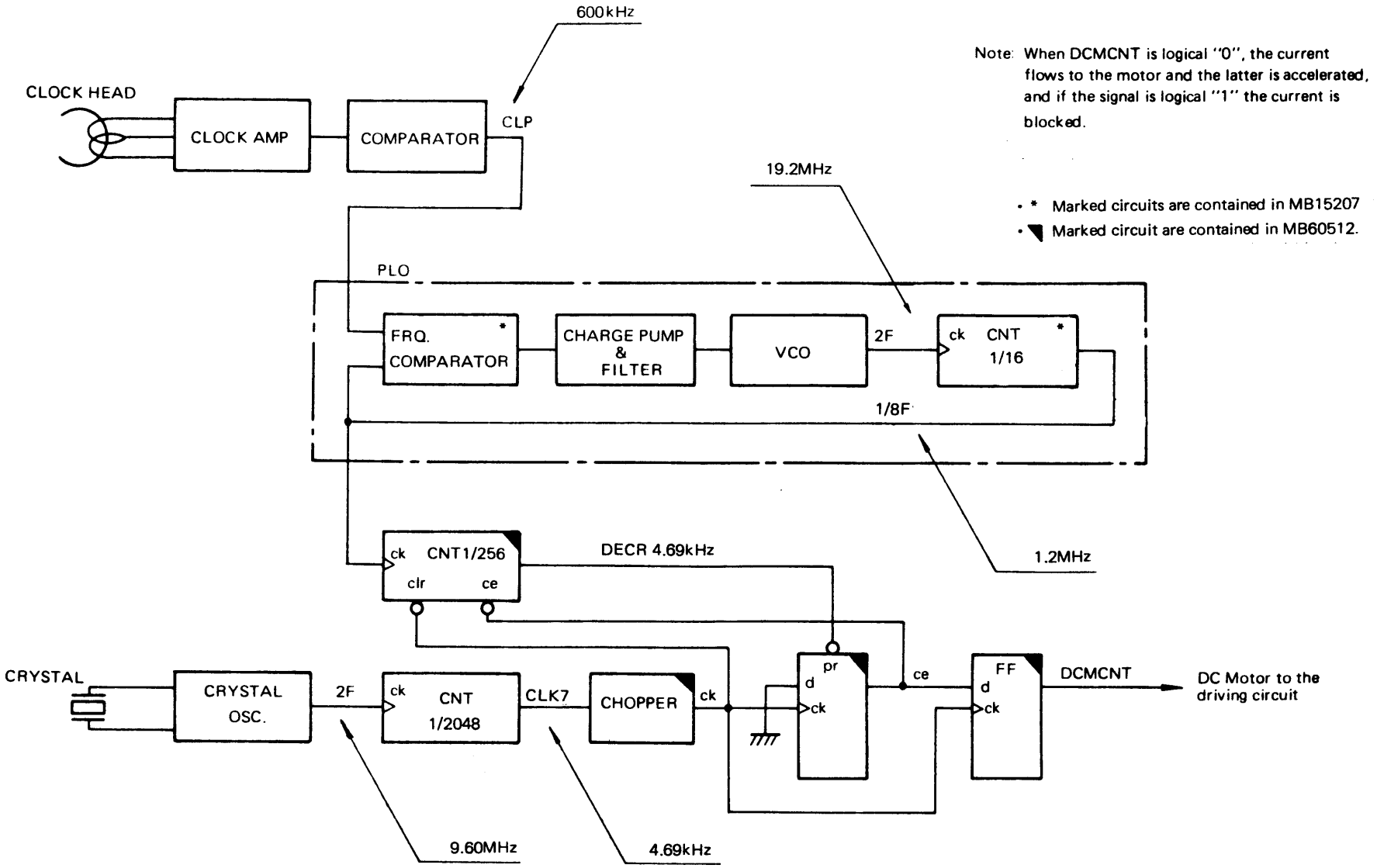
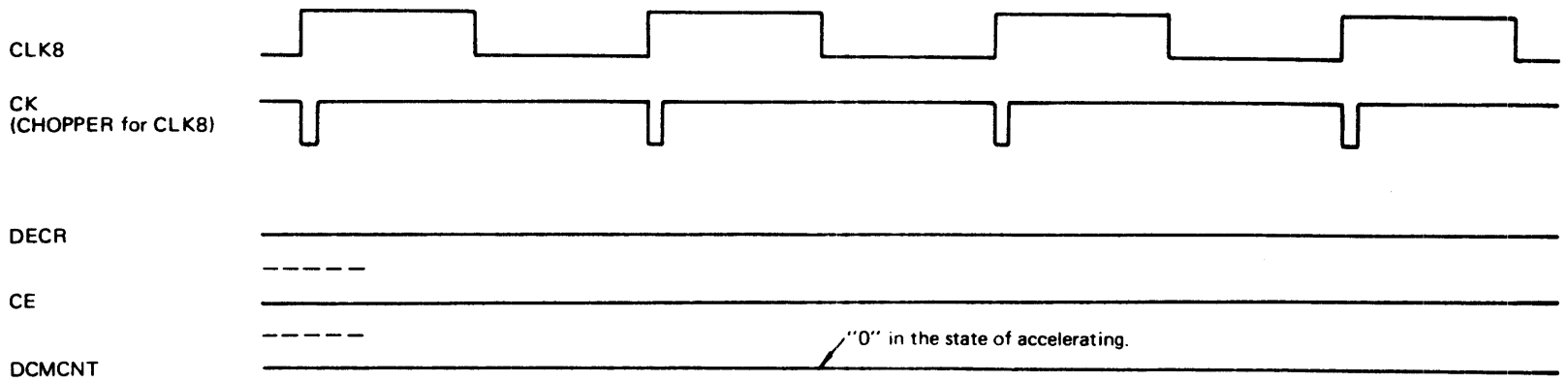


Fig. 4.12 DC Spindle Motor Control Block Diagram

(1) During Acceleration (when motor is rotating slowly) DCMCNT is "0".



(2) During Deceleration (when the motor is rotating fast) DCMCNT is "1".

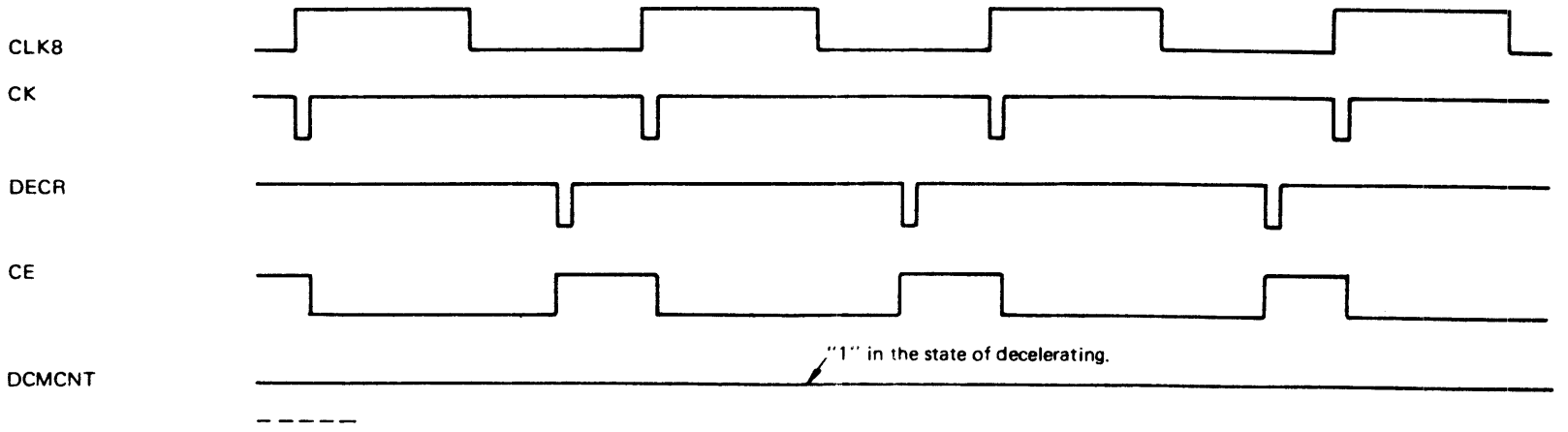


Fig. 4.13 DC Spindle Motor Control Timing Chart (1)

(3) Under Control (the speed of rotation is controlled to the 2964 rpm ±2%).

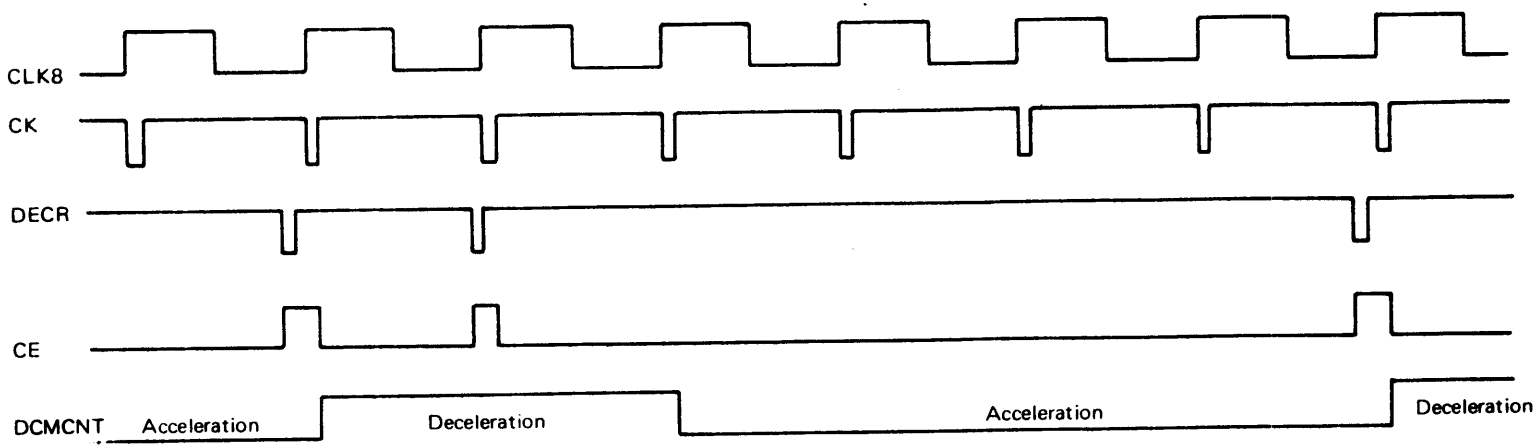


Fig. 4.13 DC Spindle Motor Control Timing Chart (2)

4.6.6 SEEK Control

(1) General

There are two modes of operation for the head positioning stepper motor: controlled step mode and slave step mode. The seek control circuit monitors the frequency of the step pulse transmitted from the controller to the drive, and if the input frequency is less than 1kHz, the controlled step mode is automatically selected. If the input frequency is over 3kHz, the slave step mode is automatically selected. However both the step rates of 1kHz to 3kHz and over 3MHz are prohibited.

When 255 or more step pulses are received in slave mode, the drive will automatically return the heads to track 0. This operation is called RETURN TO ZERO (RTZ). Fig. 4.14 shows the block diagram of seek control. Fig. 4.15 shows the flowchart.

(2) Controlled Step Mode

In this mode, the stepper motor performs a SEEK directly controlled and synchronized with the step pulse sent from the controller. The direction of the seek is controlled by the DIRECTION line from the controller. Fig. 4.16 shows the timing chart of controlled step mode.

(3) Slave Step Mode

In this mode, the seek is performed by step pulses generated by the speed up/slow down circuit within the drive. After receiving and storing all step pulses in the 3kHz to 3MHz range, coming from the controller, the seek is controlled automatically by the drive in order to complete the operation in the least amount of time.

The step rate of the speed up/slow down circuit is stored in ROM which is accessed in the Slave Step mode according to the value of the seek counter and the difference counter. The pulse train is formed depending on the data read out from ROM. Fig. 4.17 shows the timing chart. Fig. 4.18 shows the step rate of speed up/slow down.

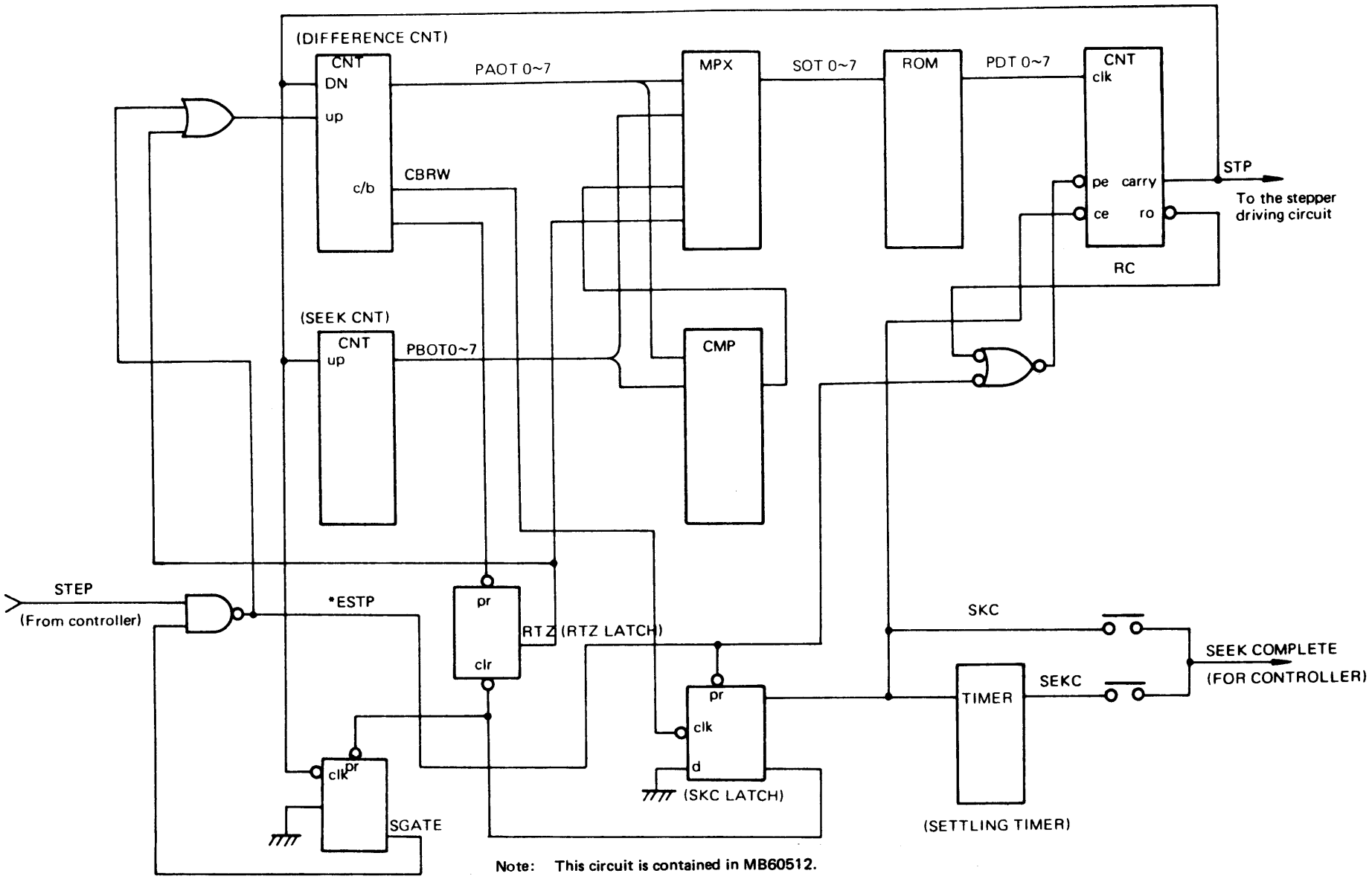
(4) RTZ Mode

When more than 255 step pulses in slave step mode are received from the controller, the internal difference counter is kept at 255 and at the same time, RTZ LATCH is set. After all the step pulses from the controller are received, the SEEK is performed in the outer direction until the TRACK 0 indication is received by the speed up/slow down circuit. The step rate of the speed up/slow down circuit, in this case, is determined by the data from ROM accessed by the RTZ LATCH bit. In the RTZ mode, the regular step rate is 500 pps. Fig. 4.19 shows the timing chart.

(5) SEEK COMPLETE

The SEEK COMPLETE signal indicates to the controller that a seek operation has been completed. The unit can be set by a switch on the PCA to use the SKC signal which includes the settling time.

Refer to item 3.6.7 for the setting method of switch. Fig. 4.20 shows the timing chart of the SEEK COMPLETE response.



Note: This circuit is contained in MB60512.

Fig. 4.14 SEEK Control Block Diagram

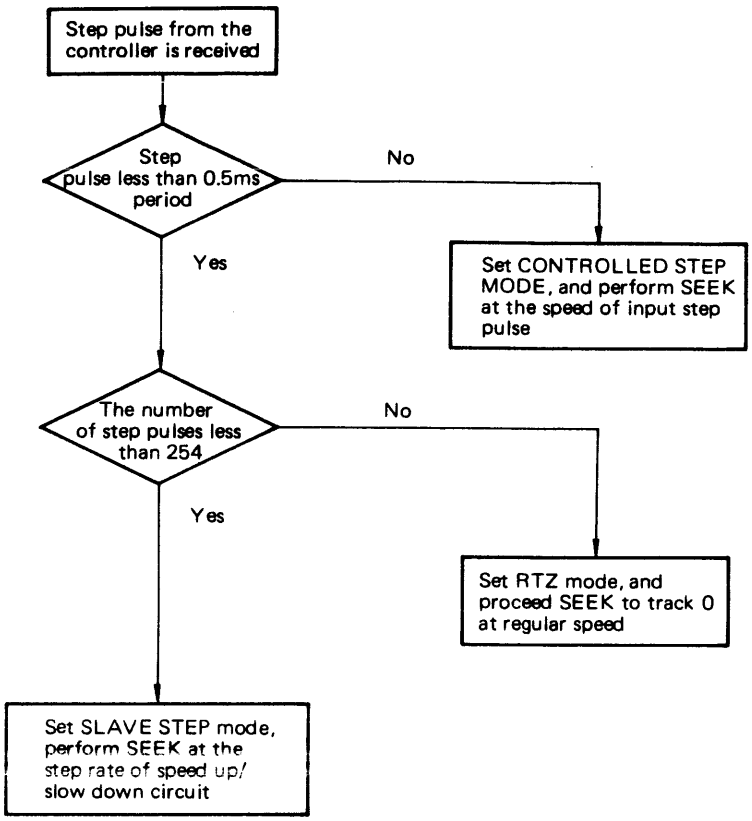


Fig. 4.15 SEEK Control Flow Chart

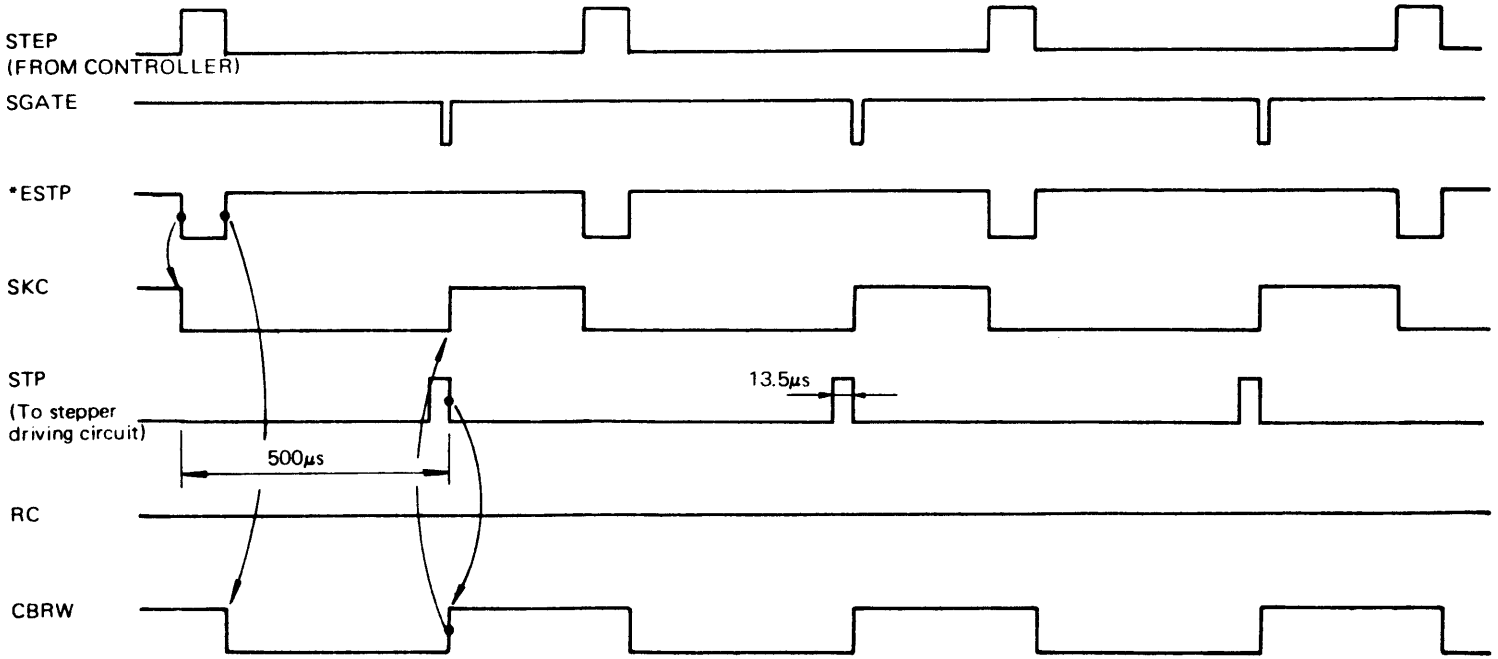


Fig. 4.16 CONTROLLED STEP Mode Timing Chart

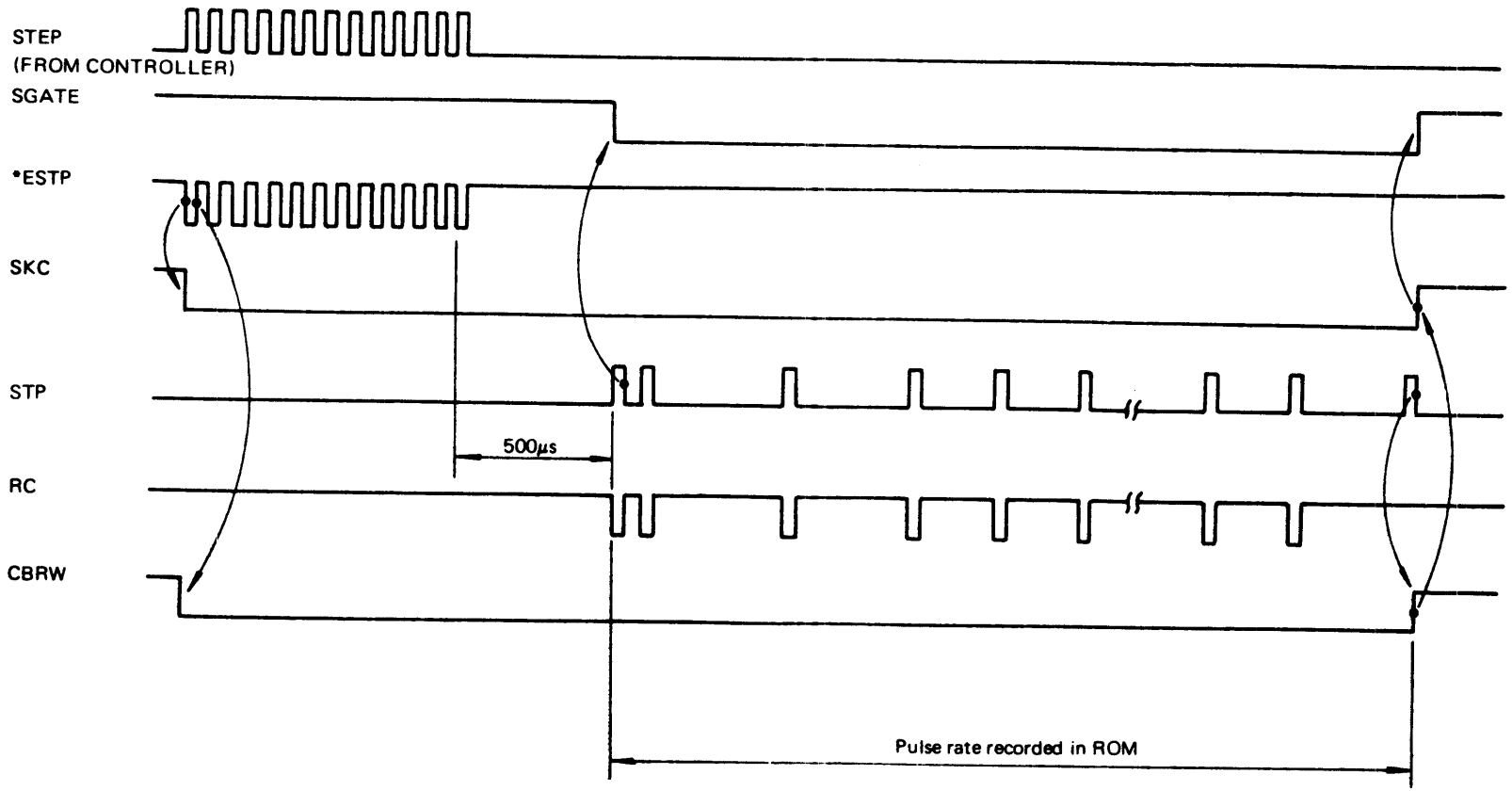
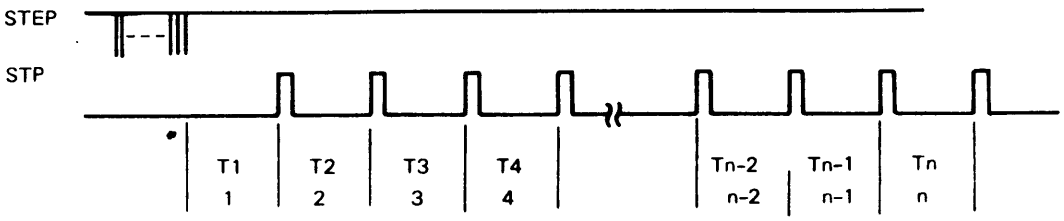


Fig. 4.17 SLAVE STEP Mode Timing Chart



Step No.	Pulse Interval
1	0.50ms
2	0.20
3	3.00
4	1.10
5	0.90
6	0.82
7	0.72
8	0.69
9	0.66
10	0.64
11	0.61
12	0.58
13	0.56
14	0.53
15	0.50
16	0.48
17	0.45
18	0.44
19	0.42
20	0.40
21	0.39
22	0.37
23	0.35
24	0.33

Step No.	Pulse Interval
n	2.00ms
n-1	1.20
n-2	1.00
n-3	0.90
n-4	0.82
n-5	0.72
n-6	0.69
n-7	0.64
n-8	0.61
n-9	0.58
n-10	0.56
n-11	0.53
n-12	0.50
n-13	0.48
n-14	0.45
n-15	0.44
n-16	0.42
n-17	0.40
n-18	0.39
n-19	0.37
n-20	0.36
n-21	0.35
n-22	0.33
n-23	0.33

Example:

(1) Pulse rate at 7 track seek mode;
0.50 + 0.20 + 3.00 + 1.10 + 1.00 + 1.20 + 2.00 = 9.00 [ms]

(2) Pulse rate at 8 track seek mode;
0.50 + 0.20 + 3.00 + 1.10 + 0.90 + 1.00 + 1.20 + 2.00 = 9.90 [ms]

Fig. 4.18 Speed Up/Slow Down Step Rate

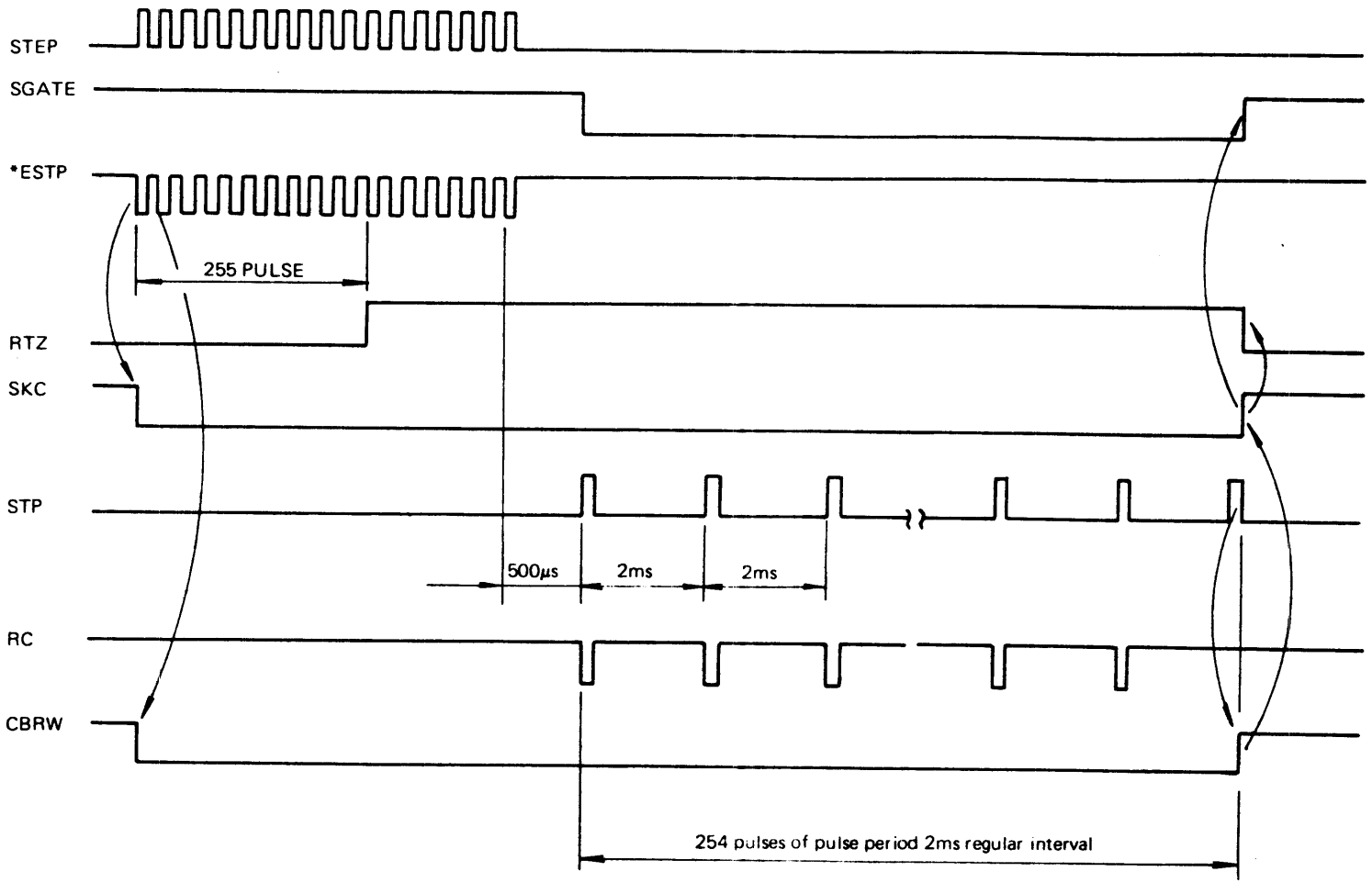
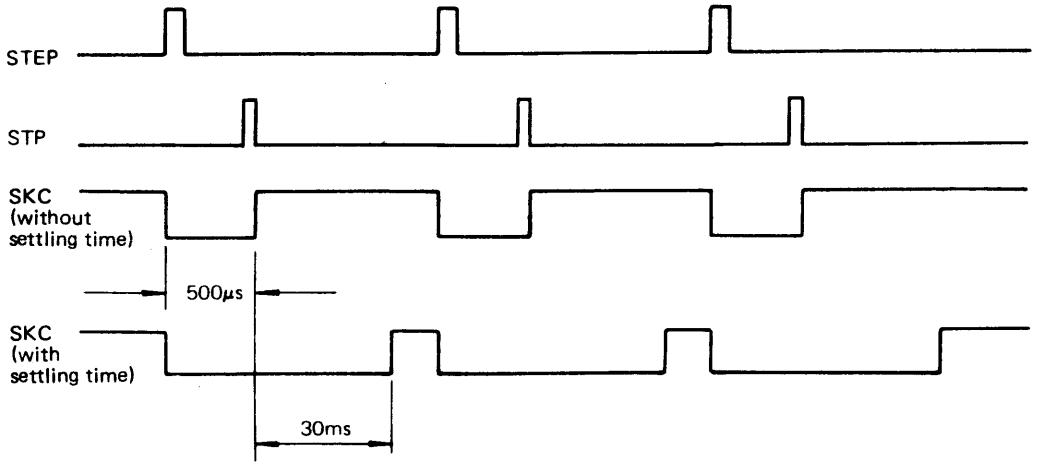


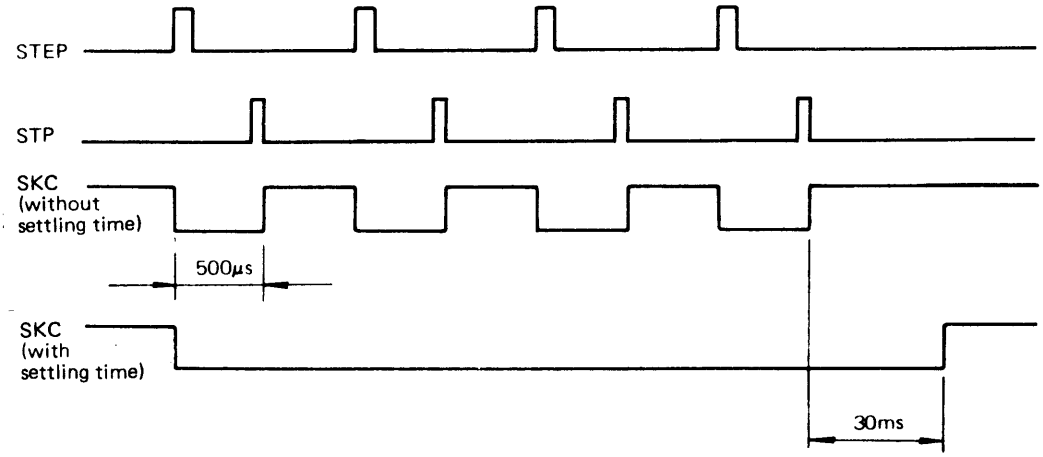
Fig. 4.19 RTZ Mode Timing Chart

(1) Response at the Time of CONTROLLED STEP Mode

(a) When the input step pulse period is more than 30ms.



(b) When the input step pulse period is less than 30ms.



(2) Response at the Time of SLAVE STEP Mode

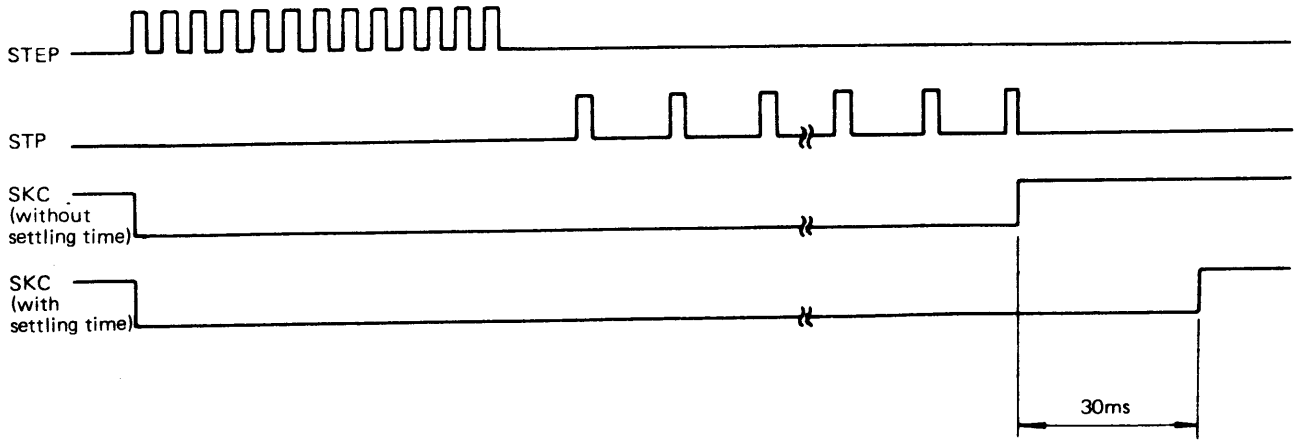


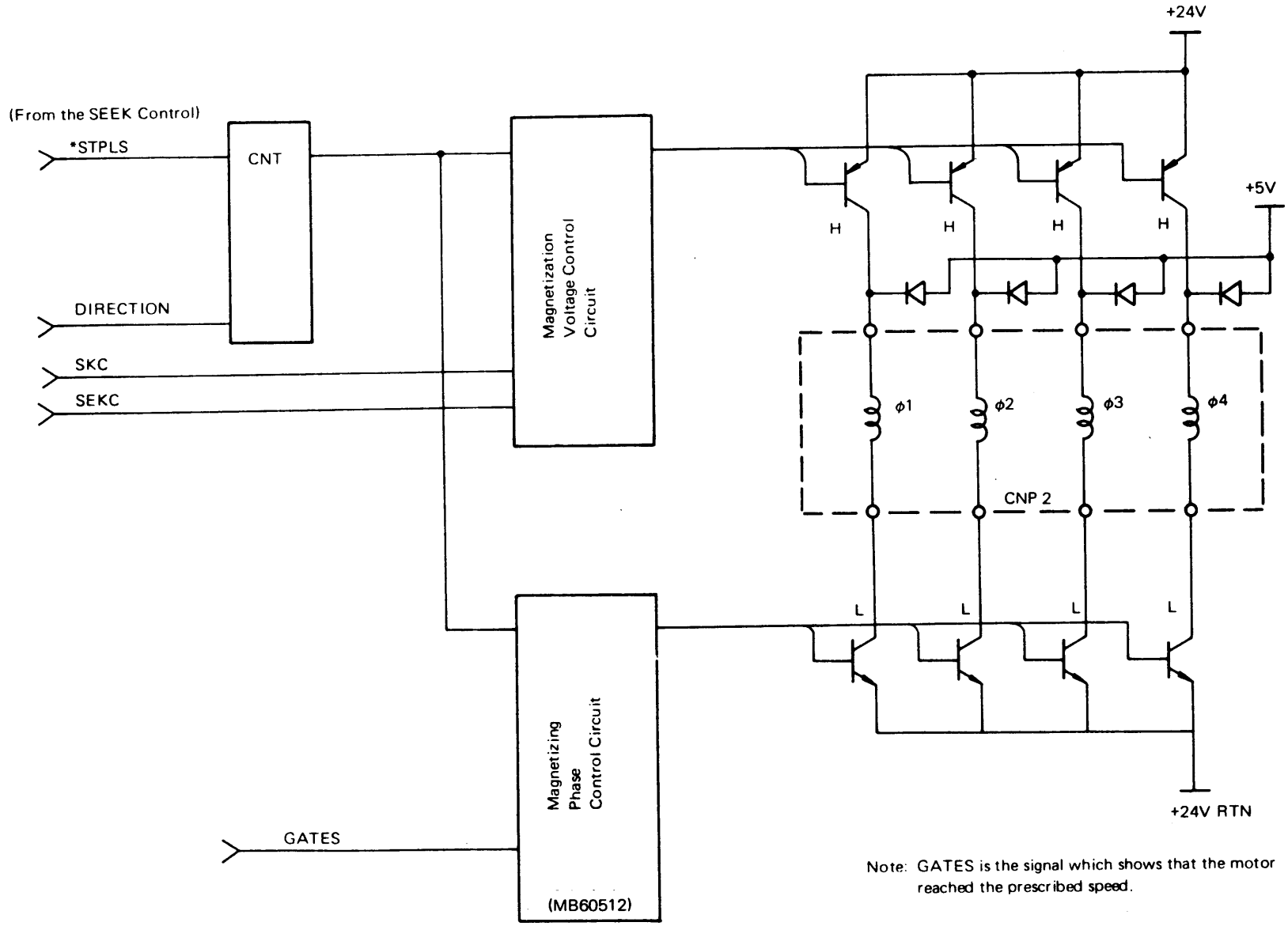
Fig. 4.20 SEEK COMPLETE Response Timing Chart

4.6.7 Stepper Driving Circuit

The four phase stepping motor is used to position the data heads, and the stepper driving circuit is the circuit for driving the stepping motor. For stepper motor rotation, the 1 - 2 phase magnetization system is employed. The magnetizing phase control circuit controls the winding of the stepping motor to be magnetized and the timing of its magnetization by means of step pulse STP and DIRECTION coming from the seek control circuit. The stepper driving system requires two types of magnetization voltage, +24V and +5V. Switching occurs between these two voltages in order to maximize performance during the power-on, seeking, and settling operations.

(1) During SEEK
During the SEEK operation, when magnetization starts, a voltage of +24V is fed for about 1ms to the phase of the stepping motor to be magnetized, and after that a voltage of +5V is fed to the phase until the magnetization of that phase is switched to the other phase.

(2) During Settling
During settling time, which starts after the SEEK operation has completed, and lasts for about 30ms, the stepping motor is magnetized by a switching voltage of +24V/+5V. The switching rate is changed depending on whether only one phase is magnetized or two phases are magnetized at the time of SEEK completion.
And after the settling is completed, the hold torque of the stepping motor is created by using +5V. Fig. 4.21 shows block diagram of the driving circuit. Fig. 4.22 shows the timing chart.



Note: GATES is the signal which shows that the motor reached the prescribed speed.

Fig. 4.21 Stepper Driving Circuit Block Diagram

(1) Magnetizing Phase Control Circuit

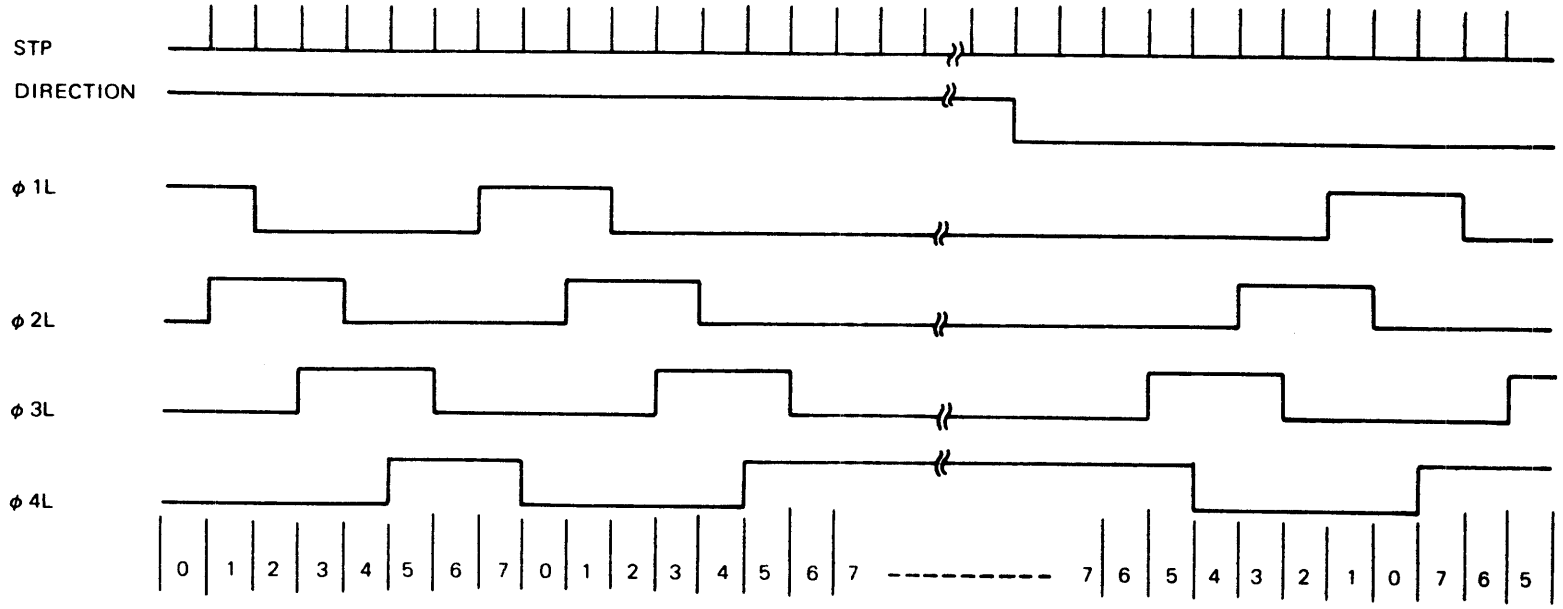


Fig. 4.22 Stepper Driving Circuit Timing Chart (Page 1 of 2)

(2) Magnetization Voltage Control Circuit

T3 1 phase magnetized stopping time 324μs
2 phase magnetized stopping time 1,728μs

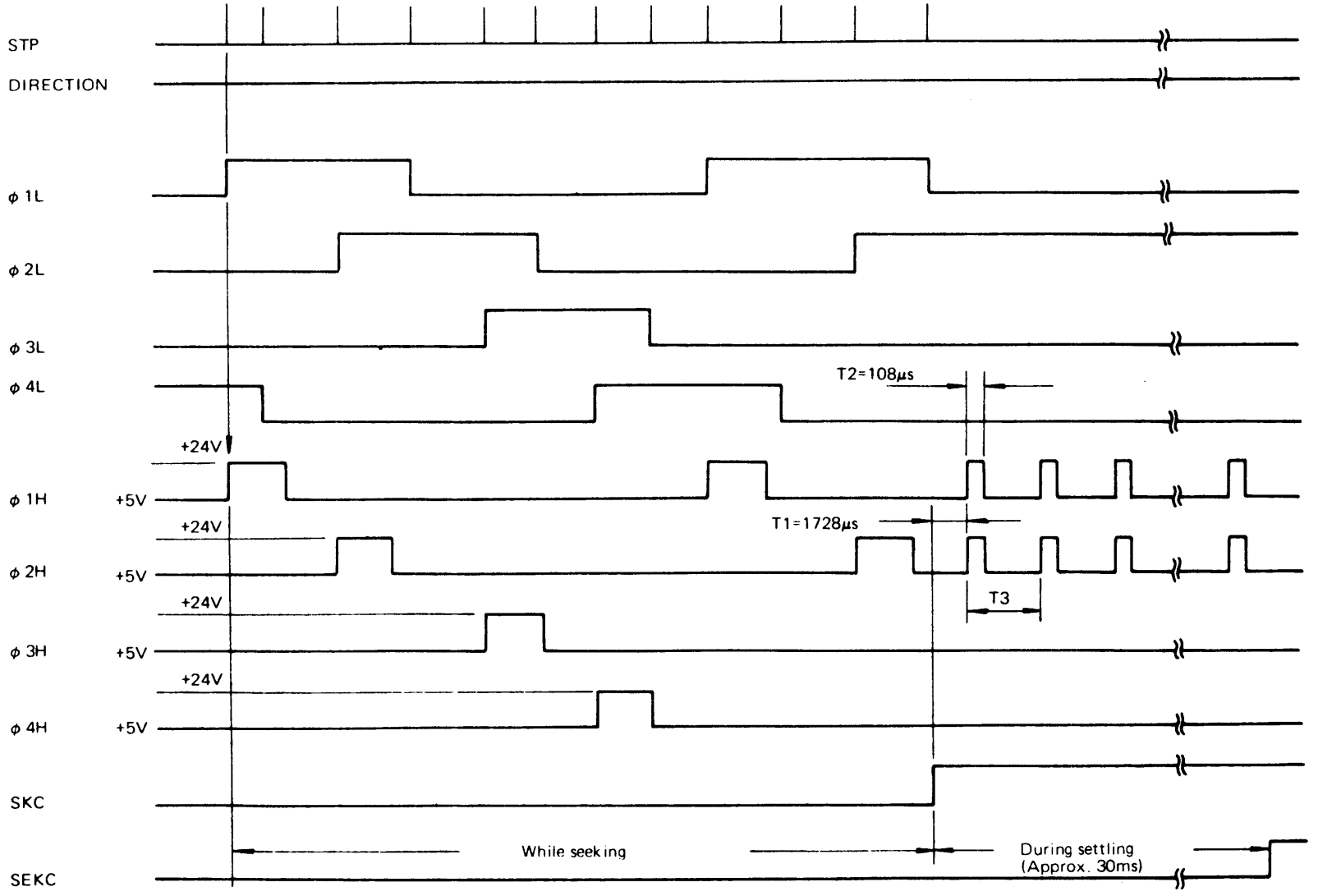


Fig. 4.22 Stepper Driving Circuit Timing Chart (Page 2 of 2)

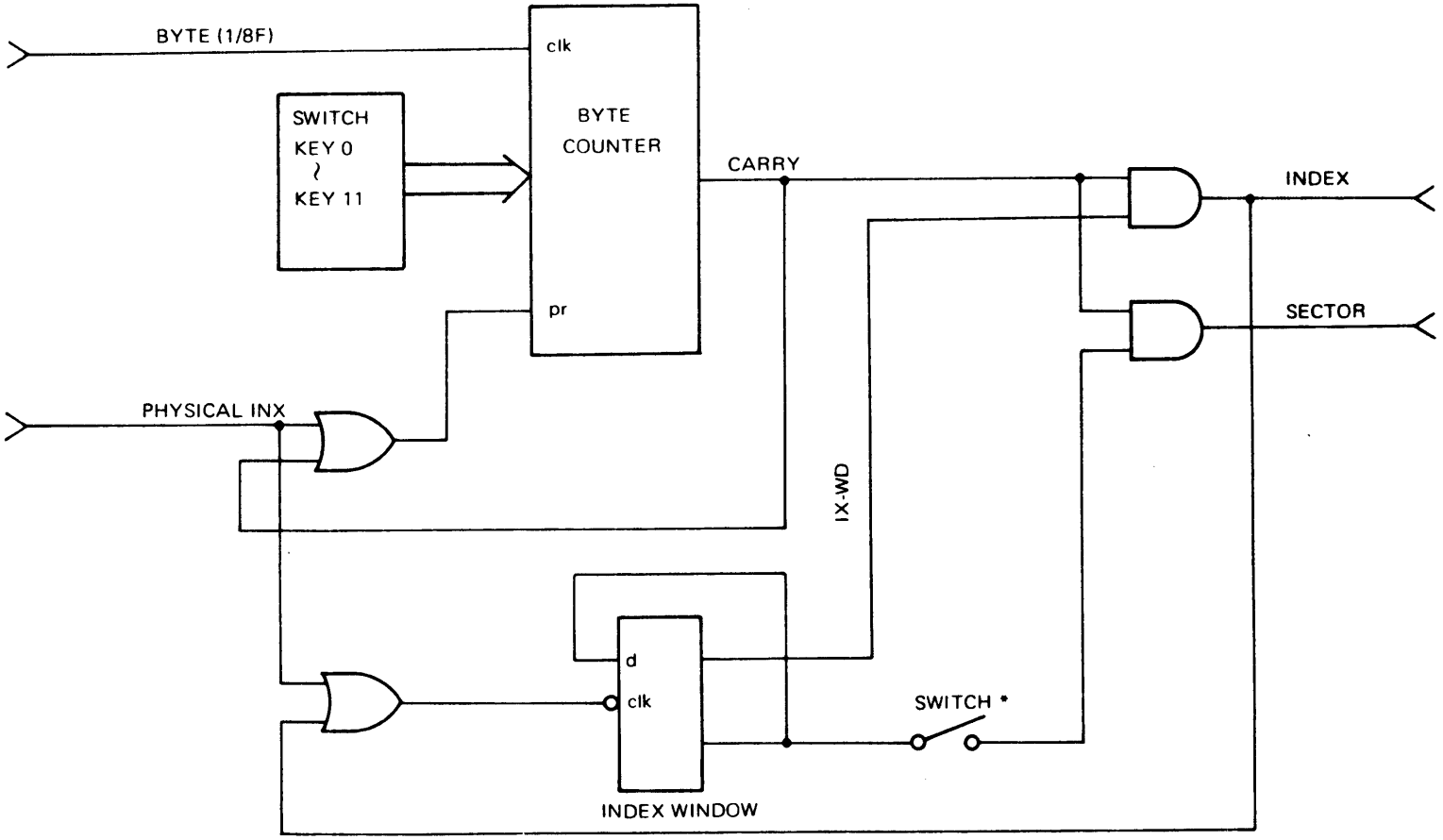
4.6.8 Index and Sector Generation Circuit

On the clock track, there is one index pattern and $24{,}320^{+32}_{-0}$ byte clocks stored. Sector pulses are generated by the byte counter. This counter is preset by each index or the sector pulse to the value set by switches and counts the byte clock (1/8F) from the PLO clock which is synchronized to the clock signal coming from the clock track. The length of a sector is determined by the setting of the switches on the PCB.

For example, for a sector length of 304 bytes, the data preset input of the byte counter is set to (4,095 – 304) = 3,791 by switch setting, and loaded to 3,791 by the physical index which comes from the index pattern on the clock track. Then the byte counter is incremented by the byte clock (1/8F). When the number of bytes reaches 4,095, a CARRY of one byte width is sent out, which becomes sector pulse, and at the same time, the byte counter is preset to 3,791. Eighty sector pulses per one revolution are generated (24,320 divided by 304 equals 80).

Since the number of bytes stored on one track is $24{,}320^{+32}_{-0}$ bytes, if the sector length is set to 304 bytes, the last sector is lengthened by $^{+32}_{-0}$ bytes.

Refer to item 3.6.6 for switch setting method to set sector length. Fig. 4.23 shows a block diagram of the INDEX and SECTOR generation circuit. Fig. 4.24 shows the timing chart.



* Note:
- This switch determines if the sector pulse is sent during index pulse time. When closed, the sector pulse is masked at INDEX.
- This circuit except the switches is contained in MB60512.

Fig. 4.23 INDEX and SECTOR Generation Circuit Block Diagram

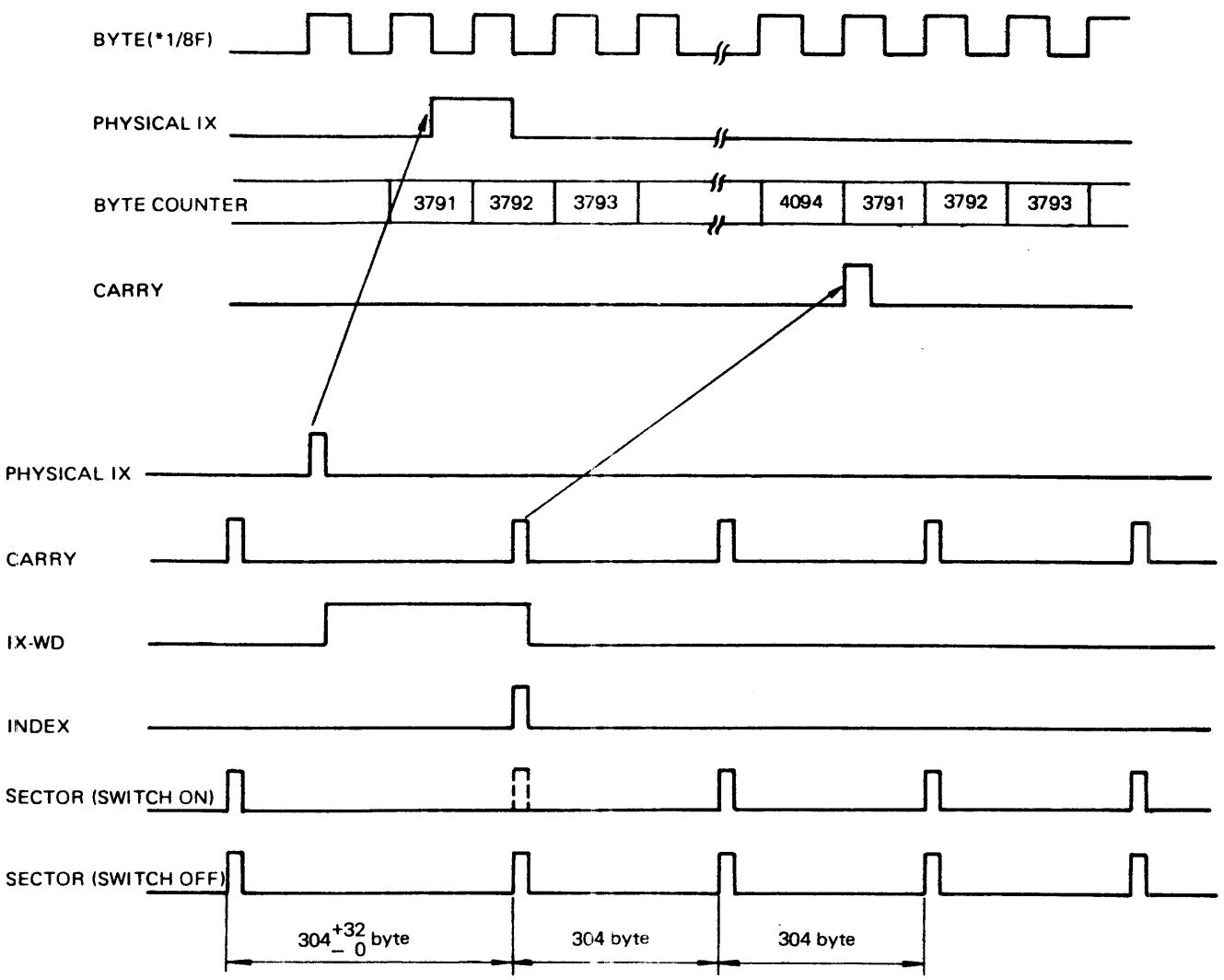


Fig. 4.24 INDEX and SECTOR Generation Circuit Timing Chart (when a Sector Length is 304 bytes)

4.6.9 Read/Write Circuit

(1) General
This circuit consists of the head select circuit, write circuit, read circuit and VFO circuit.

(2) Head Select Circuit
This is the circuit which select the designated data head in response to the head select signals (HEAD SELECT 0~ 2). HEAD SELECT 0 and 1 are converted into ECL leveled HS1 and HS2, which are decoded in a HEAD IC. HEAD SELECT 2 is decoded into chip select 0 and chip select 1 (CS0 and CS1).
The DC regulator supplies + 6VDC (VCC) and −4VDC (VEE) to the HEAD ICs within the disk enclosure. The Block Diagram of Head Select Circuit is shown in Fig. 4.25.

(3) Write Circuit
The block diagram of the write circuit is shown in Fig. 4.26.

(a) NRZ to MFM Encoder/Write Compensator
The NRZ WRITE DATA from the host is encoded into MFM WRITE DATA written on disks. At that time, MFM WRITE DATA is pre-shifted to the opposite from the expected shift direction due to the so-called peak shift phenomenon, which is more apparent on high bit density tracks. It is called write compensation. Compensated write data signal (WDP) becomes differential signals (DX/DY) through the Flip-Flop and Read/Write Bus Switch, and are sent to Head ICs. Fig. 4.26 shows the correlation between NRZ and MFM. The truth table of write compensation is shown below.

NRZ WRITE DATA				Write Compensation
1	2	3	4	
X	X	1	0	Early Data
X	1	1	1	On-time Data
X	0	1	1	Late Data
X	0	0	1	Early Clock
0	0	0	0	On-time Clock
1	0	0	0	Late Clock

Compensated data bit
Compensated clock bit

(b) Write Select Driver
WS signal line is connected to the common terminal of each head. In write mode, the voltage of WS is 3.5V and enables write current through the selected head. In non-write mode, the voltage of WS is 0V.

(c) Write Fault Detection Circuit and Fault Latch
This is the circuit which detects the occurrence of an error during the write operation. If any of the following conditions occur the circuit sets up the FAULT LATCH and transmits the WRITE FAULT to the host. The circuit also sets up the detail of an error and holds it until the FAULT CLEAR is received from the host. The detail of an error can be observed on test points on the PCB.

Error Status	The Check Terminal Set by Fault Latch
Both WRITE GATE and READ GATE come at the same time.	RGF
WRITE GATE comes when two HEAD ICs are selected at the same time.	MLT
During the WRITE operation, abnormal current flows through the data head.	UNS
The WRITE GATE signal comes when SEEK COMPLETE is false.	SEK
The WRITE GATE signal comes when the unit is not READY.	FRY

(d) Power Loss Detection Circuit
At the time of power-on/off, and when an instantaneous power-failure occurs, an abnormal current could flow through the data head due to turbulence in the logic circuit, and could cause the data on the disk to be destroyed. For this reason, the power loss detection circuit monitors the DC power level so as to clamp the power source of R/W Bus Switch and VEE to 0V very quickly in the event of a power drop, thus preventing an influx of abnormal current to the data head.

(4) Read Circuit
Figure 4.28 shows the block diagram of the read circuit.

(a) HEAD IC
During a read operation, the input to the Head IC is the head output created by induced voltage generated by the difference in magnetic flux on the disk. The head output signal is amplified about 35 times and transmitted through DX and DY to the main PCB.

(b) Low Pass Filter
The DX, DY HEAD IC outputs are amplified about 1.6 times by the R/W Bus Switch and send to LPF circuit. The filter eliminates high frequency noise from the amplified read signal. High cutoff frequency is about 9 MHz.

(c) AGC Circuit
The AGC circuit composes a feed-back loop so that the outputs of MB4311 hold 3.0 V constantly.

(d) Differentiator
The read signal after passing the filter shows flux change at its peak. The differentiator is the circuit which modulates the read signal so that its flux change point comes to a zero crossing point. The differentiator formed by CR is employed.

(e) Pulse Shaper
This is the circuit which detects the zero crossing point of the differential wavefrom in analog differentiated by the differentiator and modulates it to logical level. The output of the pulse shaper is the logical CML level.

(f) Shoulder Noise Rejection Circuit

The read waveform from the head has a so called shoulder as shown in Fig. 4.29. When this waveform is differentiated, the part of this shoulder approximates to the zero cross line, and after the output of pulse shaper, a noise pulse would overlap on it due to external noise.

The shoulder noise rejection circuit identifies a signal pulse and a noise pulse by the width of the pulse and eliminates the noise pulse which has less width than the regular pulse. The output level of this circuit is also CML level.

(g) Level Converter and Differentiating Circuit

In this part, RAW DATA is formed which becomes a regular pulse width from the leading edge and trailing edge of the output of shoulder noise rejection circuit. And it also converts the CML level to the TTL level. Fig. 4.29 shows each part of the waveform created by the read circuit.

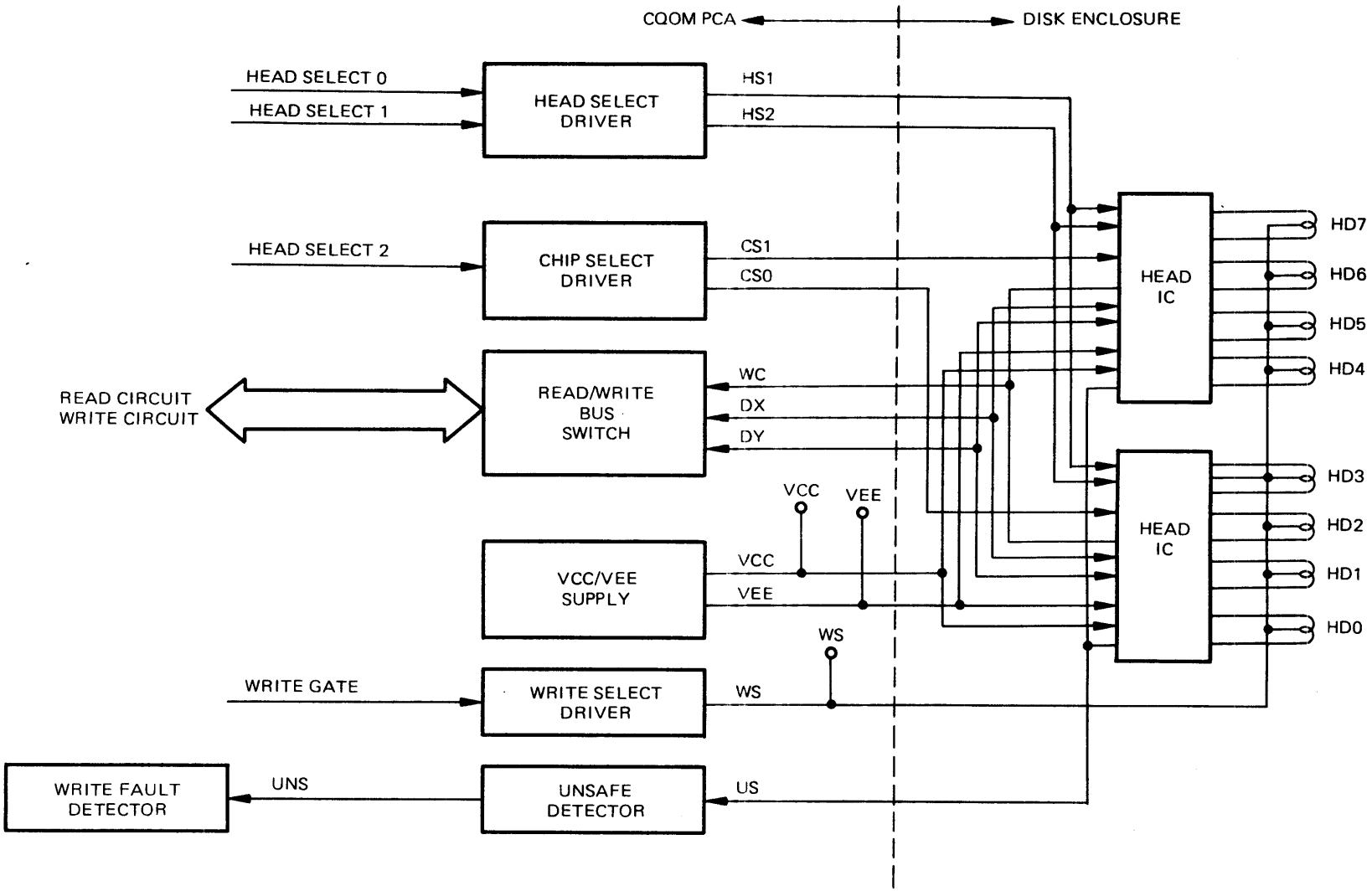


Fig. 4.25 Head Select Circuit Block Diagram

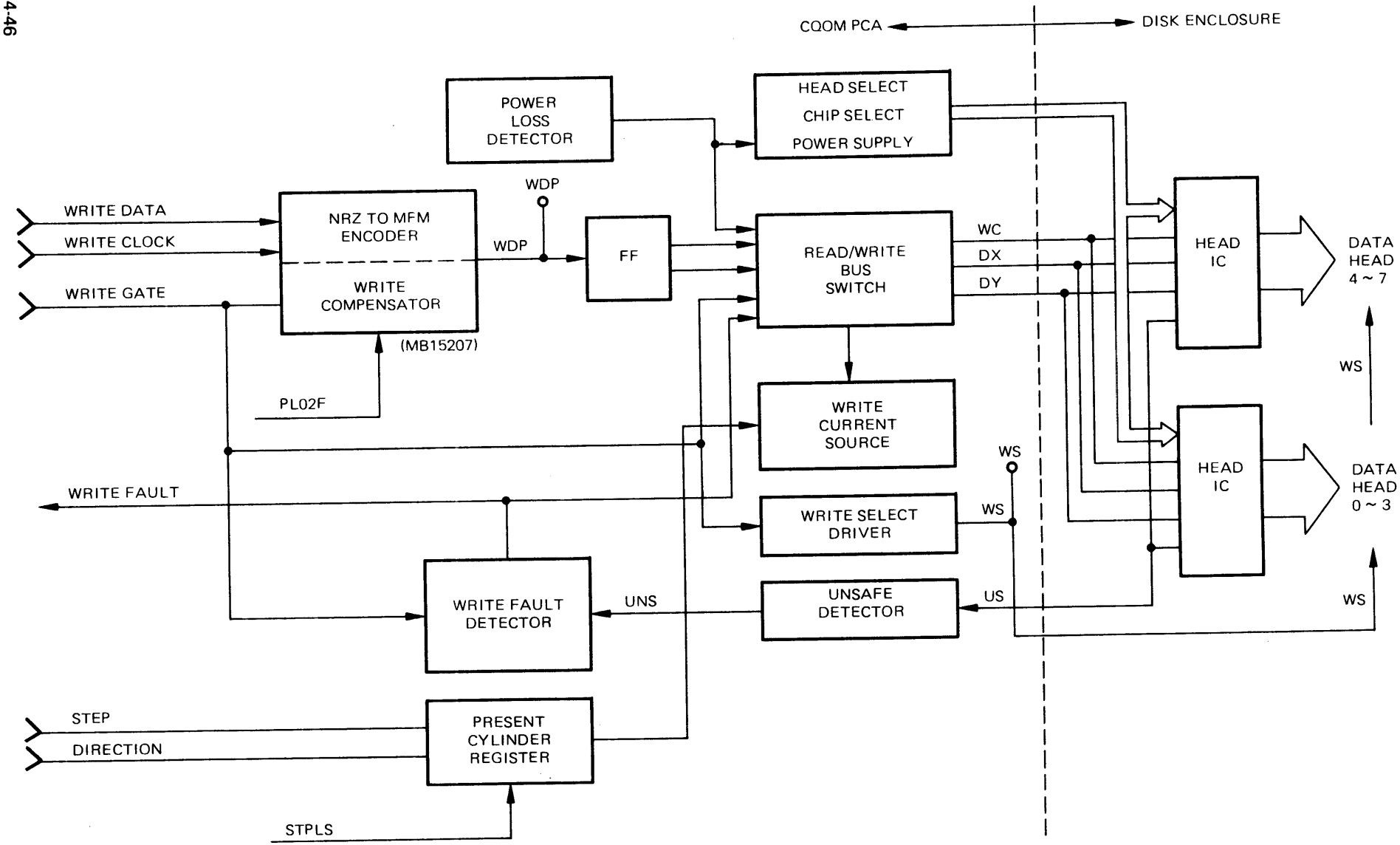
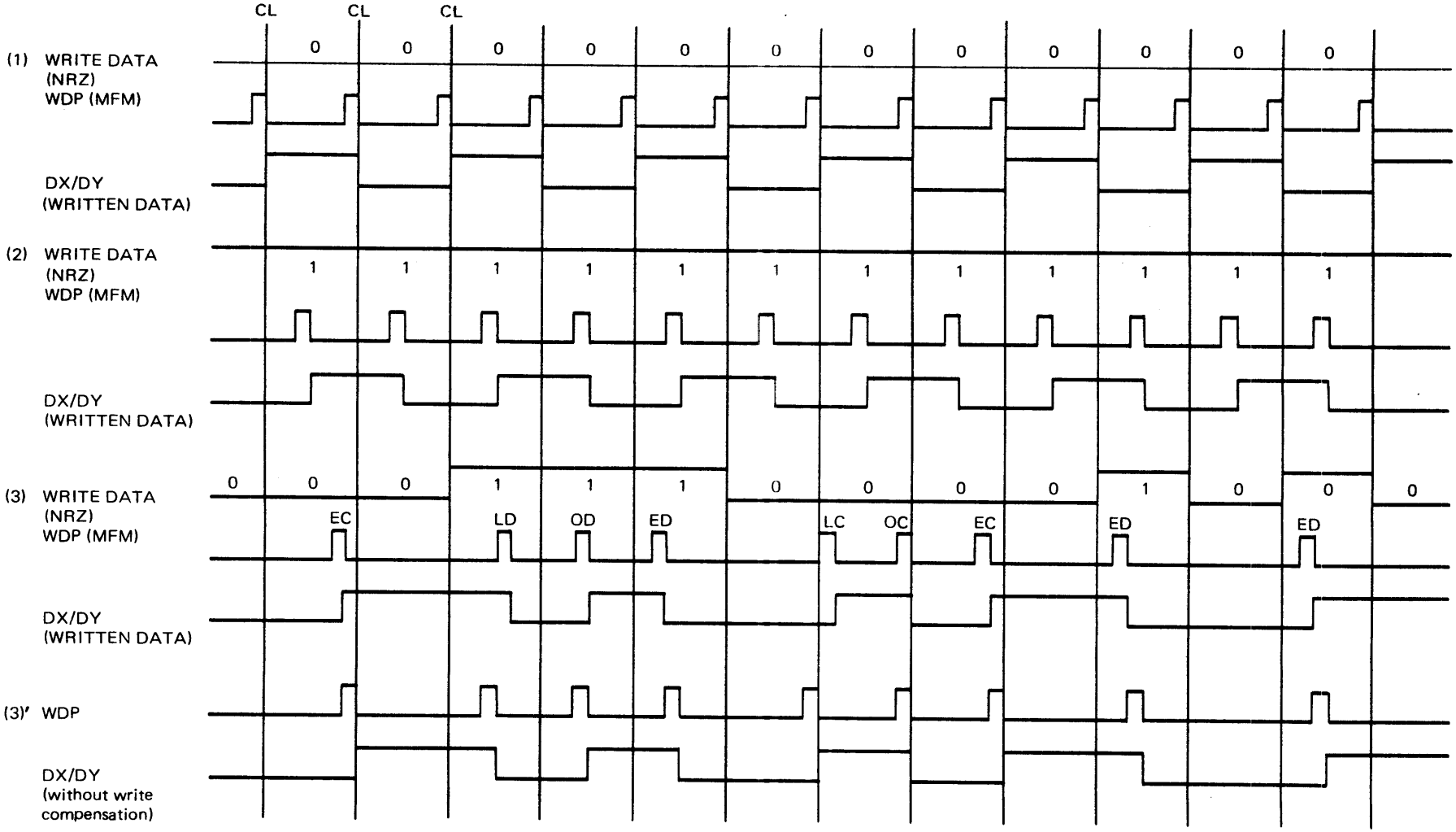


Fig. 4.26 Write Circuit Block Diagram



MFM Recording Rules:

1. There is a flux transition for each "1" data bit.
2. There is a flux transition between each pair of "0" data bits.
3. There is no transition between "01" or "10" data bit patterns.

Fig. 4.27 Correlation between NRZ and MFM with Write Compensation

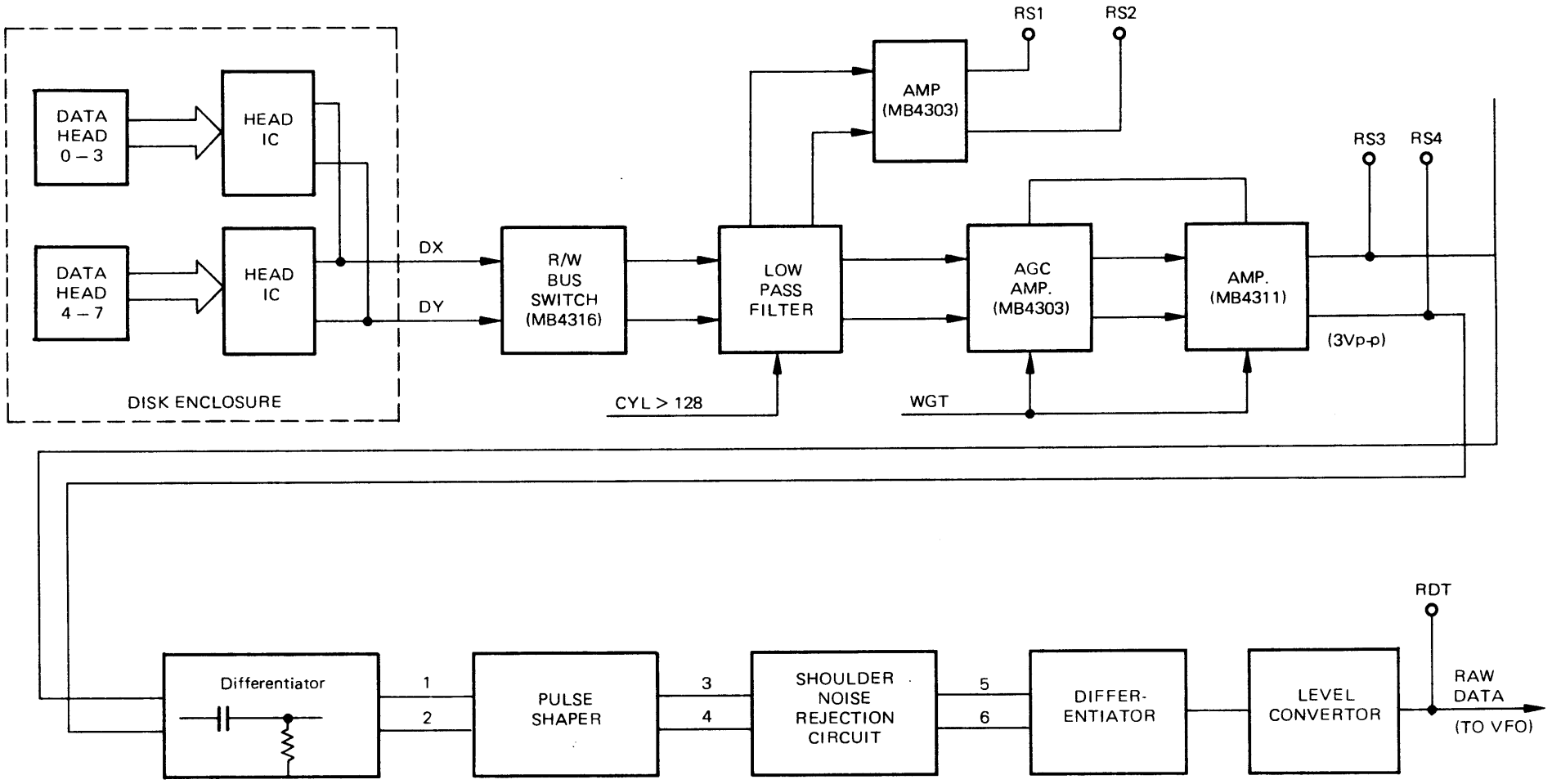


Fig. 4.28 Read Circuit Block Diagram

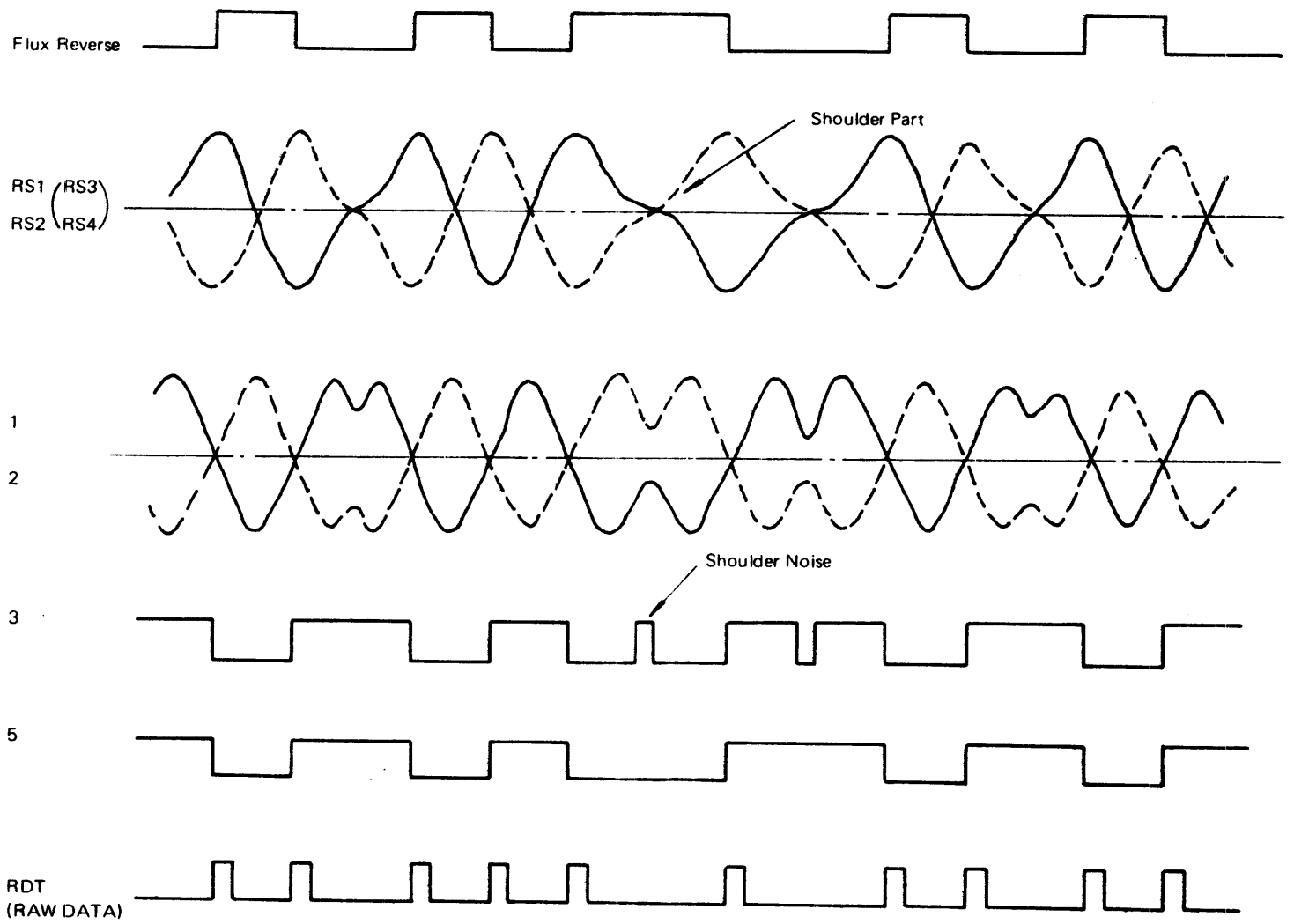


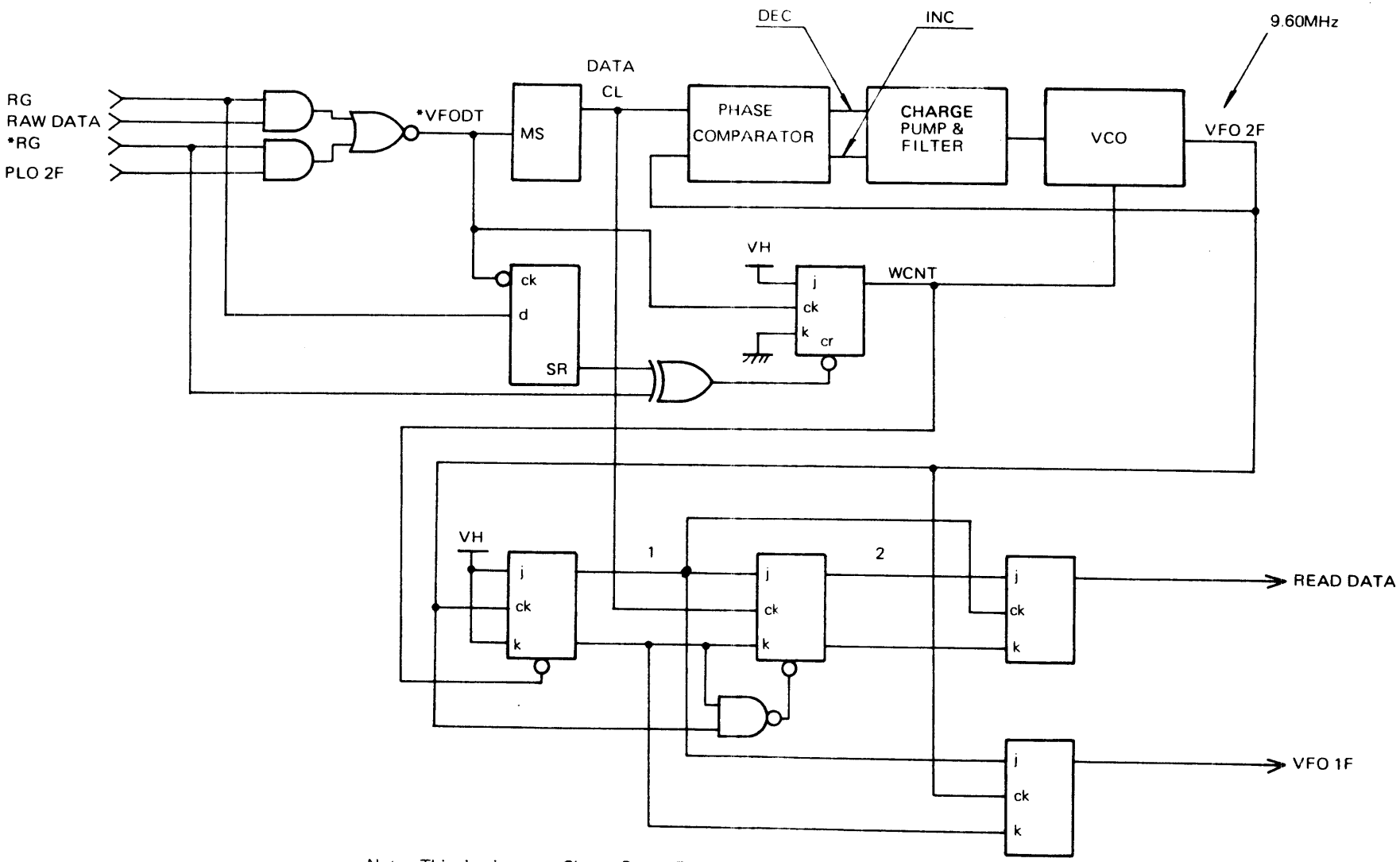
Fig. 4.29 Read Circuit Waveform

(5) VFO Circuit

The VFO circuit is a PLL (PHASE LOCKED LOOP) circuit which synchronizes to PLO2F clock during READ GATE OFF, and to read data pulse RAW DATA (RDT) in during READ GATE ON. The VFO circuit demodulates the read data to NRZ using the VFO2F clock synchronized to MFM's RAW DATA during the READ operation.

A voltage control oscillator (VCO) in the VFO circuit temporarily stops oscillation at the time of READ GATE ON/OFF, so as to shorten VFO's synchronization time when the VFO locks to RDT (Read Gate on) or PLO2F (Read Gate off). The VCO is oscillated so that the demodulated data is all "0" when READ GATE is on, because the READ GATE signal rises in the gap area where only "0's" were written.

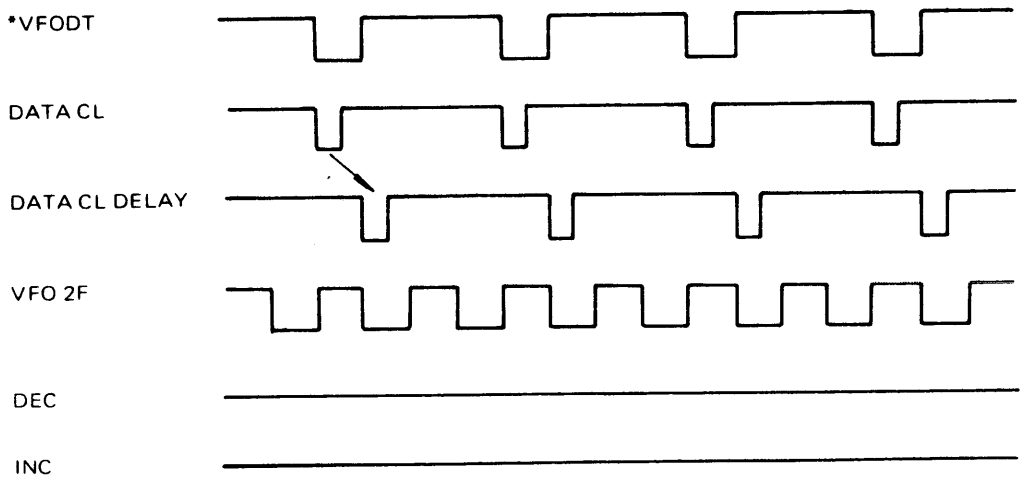
The block diagram of the VFO circuit is shown in Fig. 4.30, the timing chart of the phase comparator in the VFO circuit in Fig. 4.31, and the timing chart of the data demodulation circuit in Fig. 4.32.



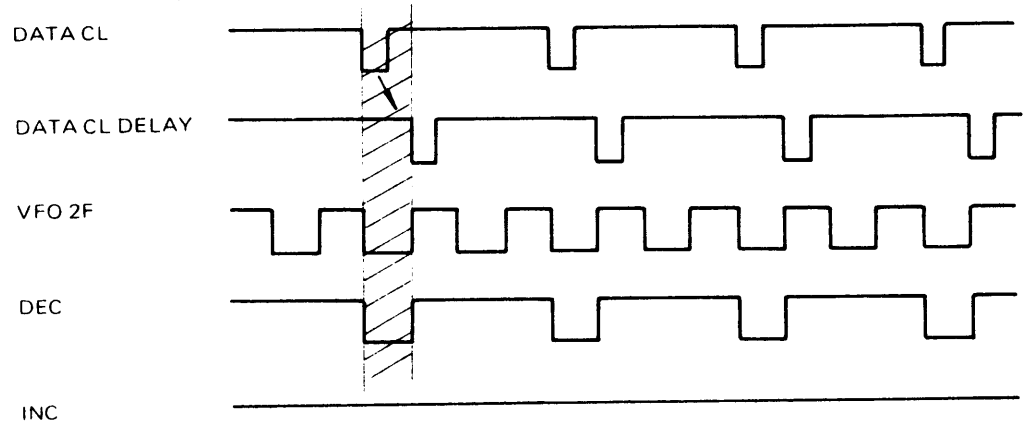
Note: This circuit except Change Pump, Filter and VCO is contain in MB15207

Fig. 4.30 VFO Circuit Block Diagram

(1) In the Same Phase



(2) VFO Phase Advances



(3) VFO Phase Delays

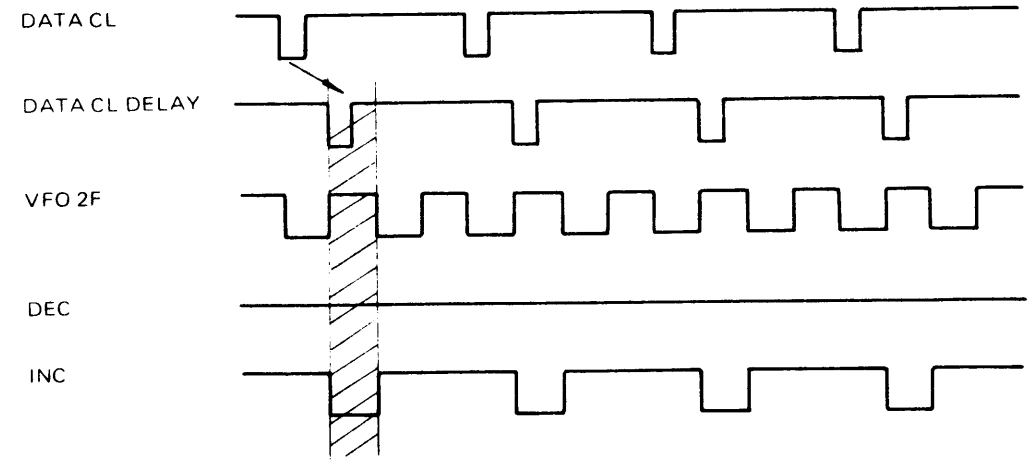


Fig. 4.31 VFO Circuit Phase Comparator Timing Chart

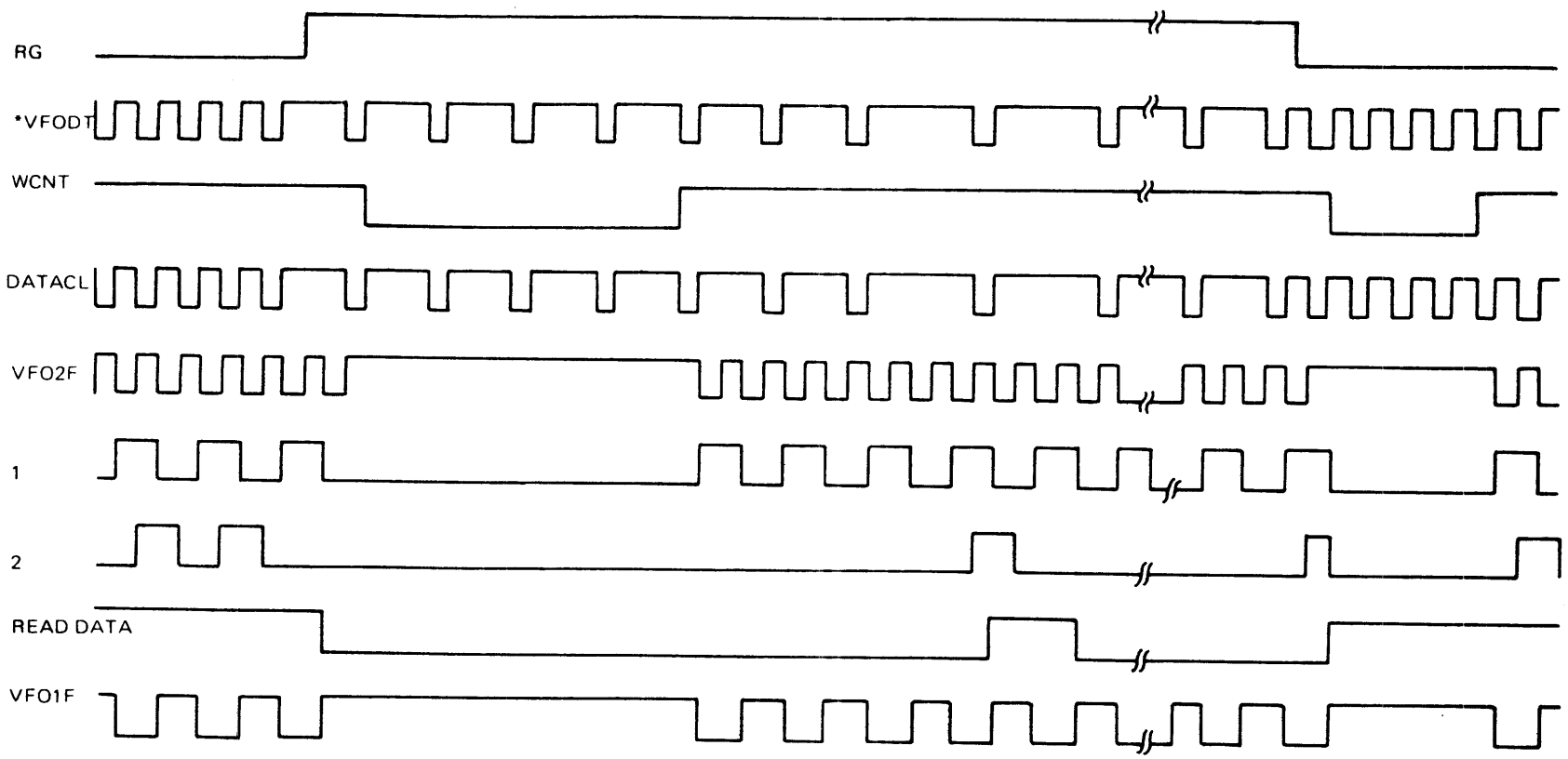
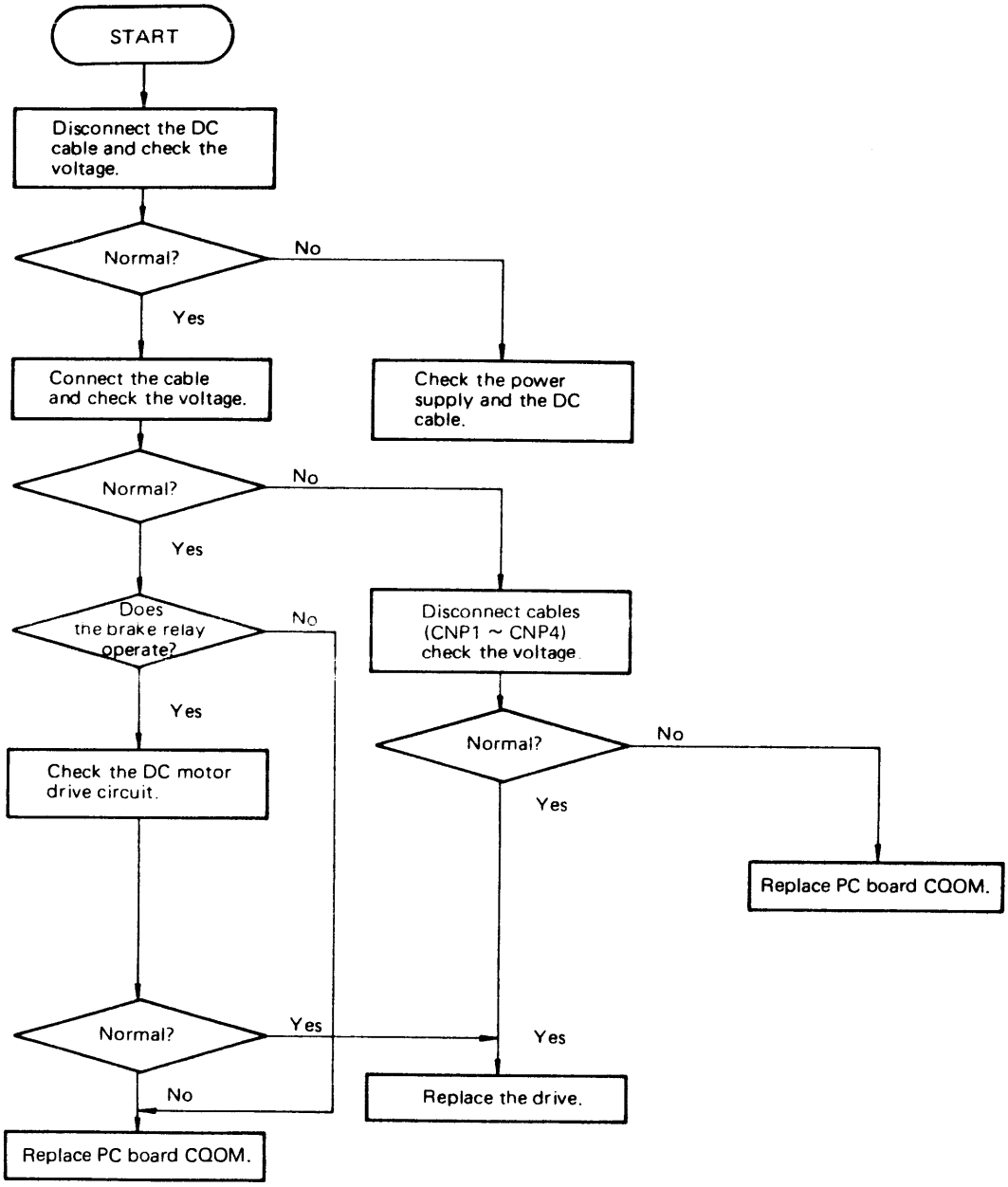


Fig. 4.32 Data Demodulation Circuit Timing Chart

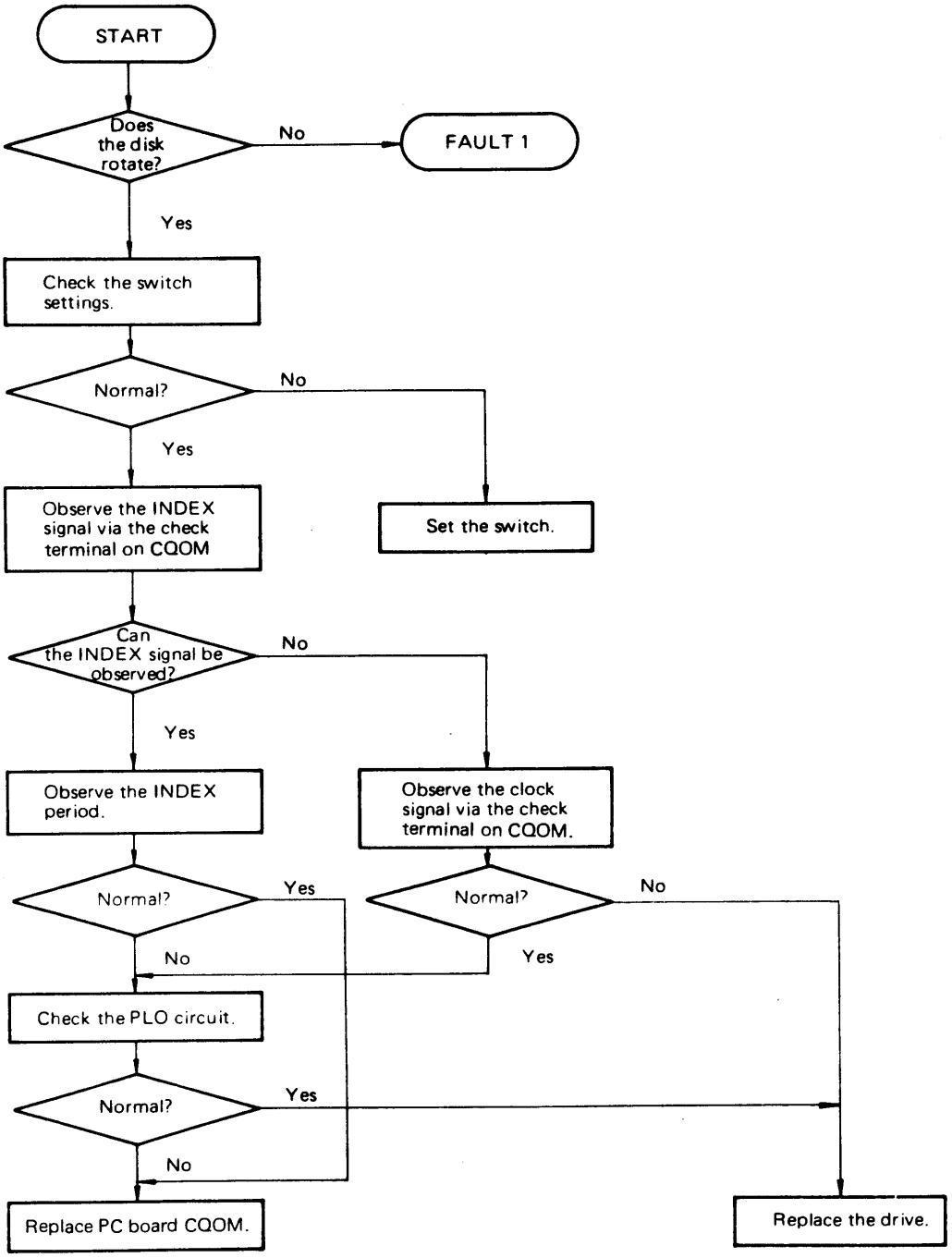
Section 5
Troubleshooting

5. TROUBLESHOOTING

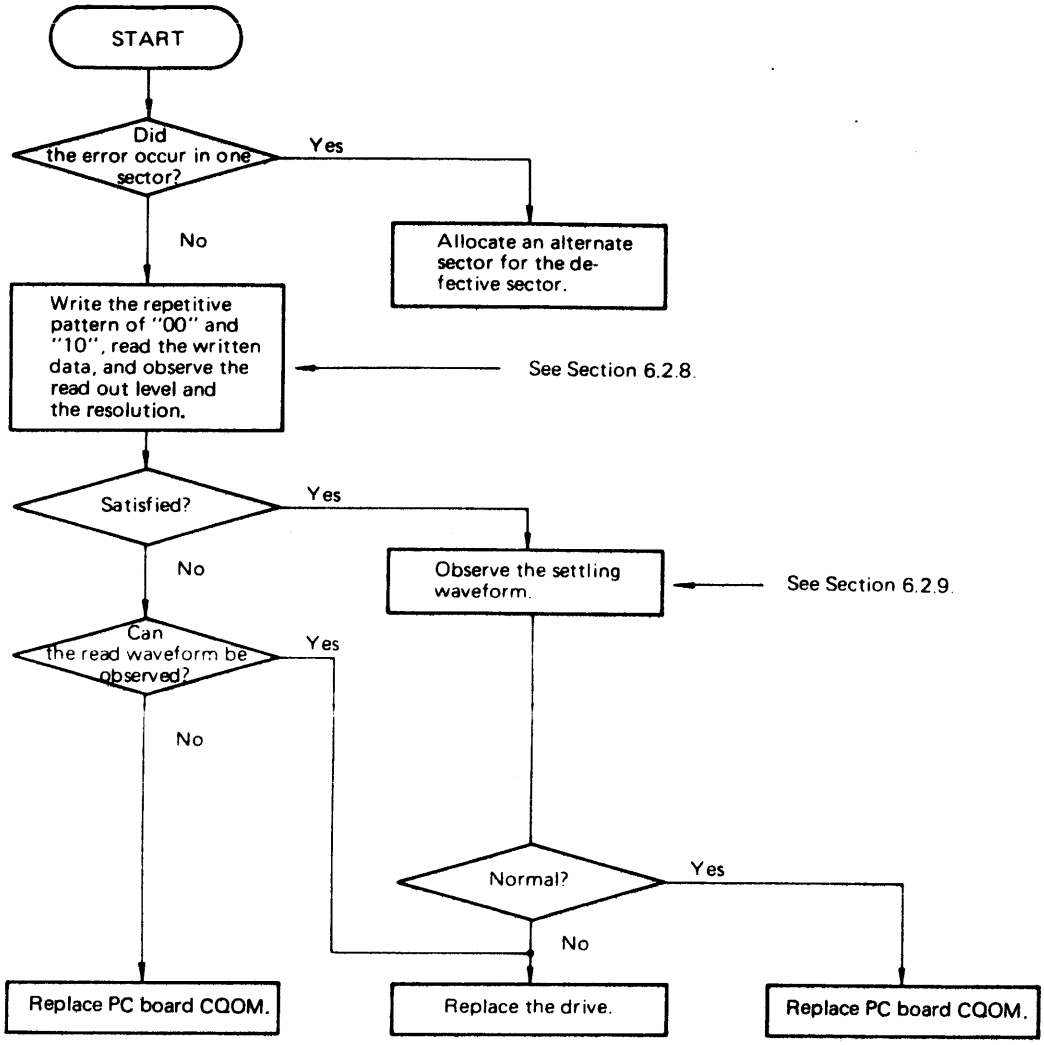
FAULT 1 The disk does not rotate.



FAULT 2 Not Ready



FAULT 3 Read Error



Section 6
Maintenance

6. MAINTENANCE

6.1 GENERAL

The unit needs no preventive maintenance. The parts required for maintenance are only the one printed circuit assembly. This section describes verification of the control circuits on the printed circuit assembly.

CAUTION: (i) Under no circumstances should the disk enclosure be opened unless in a clean room. Likewise, the retaining clamps for the DE plastic cover must not be loosened.

(ii) This printed circuit assembly contains LSIs, which are damaged easily by electrostatic discharge, therefore pins of ICs must not be touched directly by hand.

6.2 CHECKS OF THE CONTROL CIRCUIT

6.2.1 General

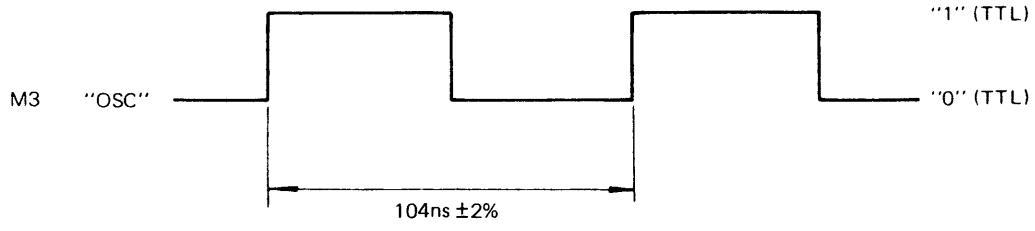
In this device there are no parts which need adjustment such as variable resistors. Only setting of the switches on the printed circuit assembly for a variety of functions is required. Accordingly, this section deals with how to removed the defective PCB when a failure occurs, and how to check the control circuits if a failure is suspected.

6.2.2 Confirming the Switch Settings

There are switches (SW1 to SW5) on the Control B (CQOM) PCB assembly which can be set to perform a variety of functions. Careful attention should be given in setting the switches in accordance with item 3.6, Switch Setting Procedure.

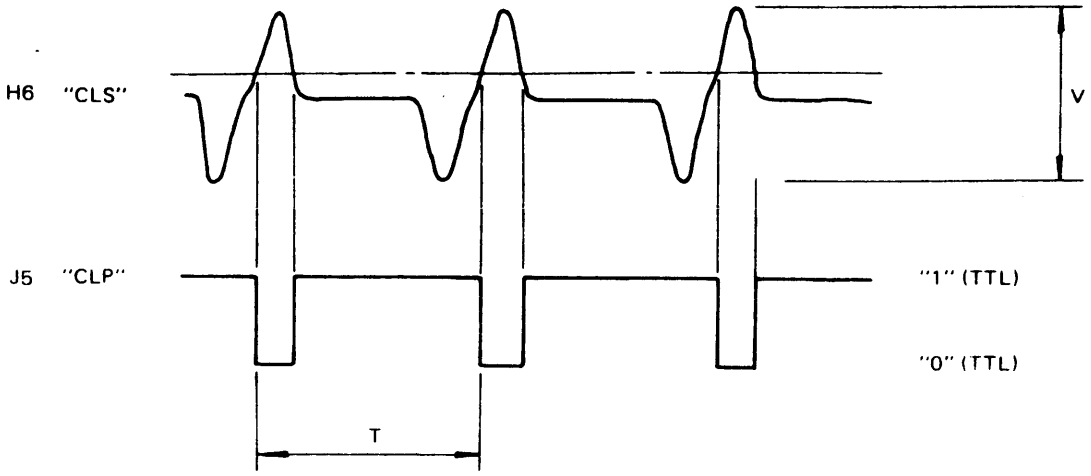
6.2.3 Check of Standard Frequency Oscillator

Observe the check terminal "OSC" on the Control O (CQOM) PCB, and confirm that the waveform is as follows.



6.2.4 Check of Clock Signal

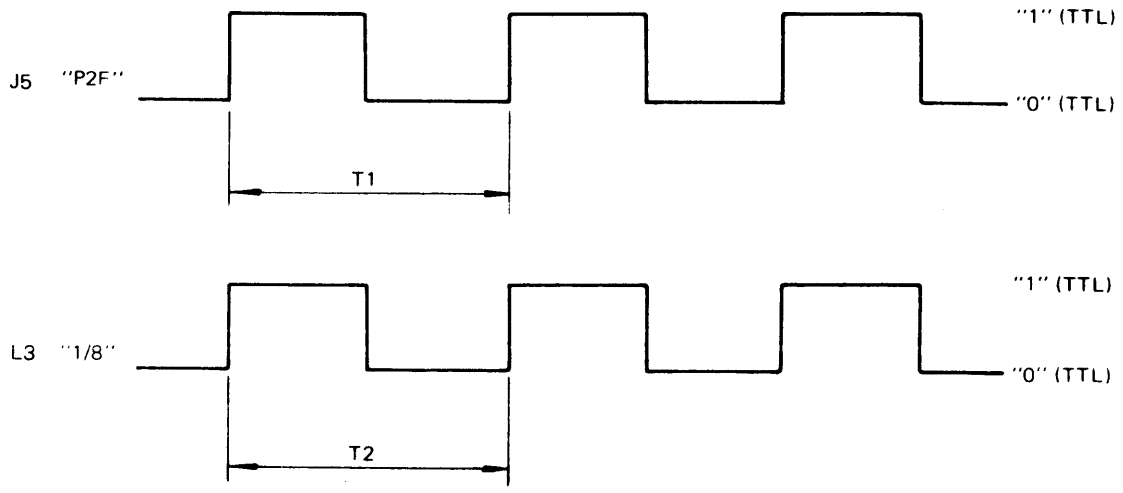
In the ready status, that is, when the disk rotation is up to speed, observe the check terminals "CLS" and "CLP" and confirm that the waveforms are as follows.



V: Over 0.8V
T: 1.69μs ±0.1μs

6.2.5 Inspection of PLO Circuit

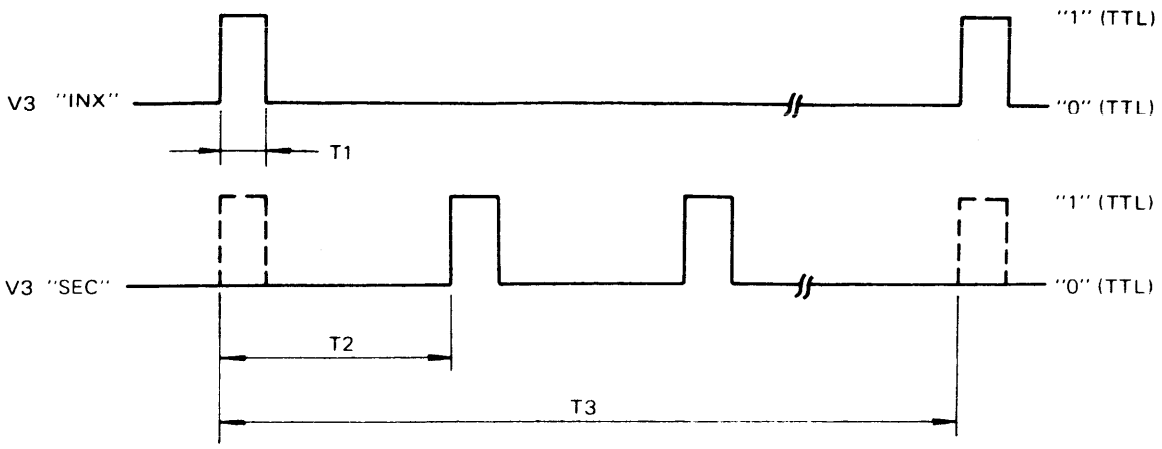
In the ready status, observe check terminals "P2F" and "1/8" or the Control O (CQOM) PCB and confirm that their waveforms are as follows.



T1: 52ns ±3%
T2: 833ns ±3%

6.2.6 Check of Index and Sector

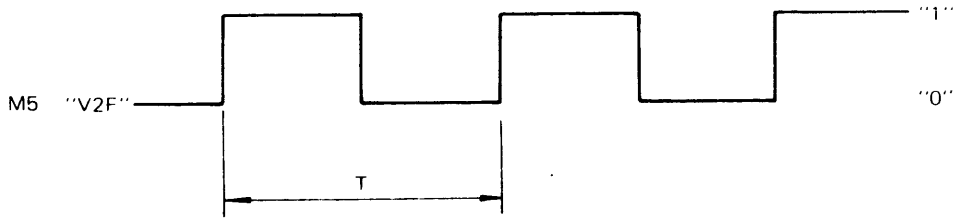
In the ready status, observe check terminals "INX" and "SEC" on the Control O (CQOM) PCB, and confirm that their waveforms are follows.



T1: 0.7μs ±5%
T2: 833μs x (bytes/sector) ±5%
T3: 20.24ms ±3%

6.2.7 Inspection of VFO Circuit

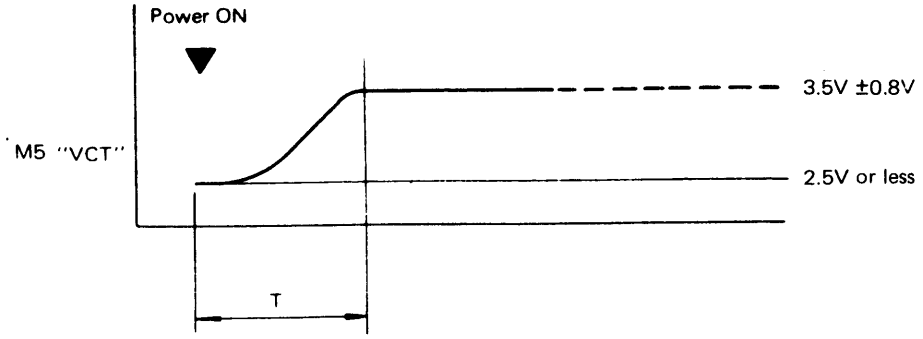
(1) Confirmation of Frequency
In the ready status, and yet not read status, observe the check terminal "V2F" in the Control O (CQOM) PCB, and confirm that the waveform is as follows.



T5: 52ns ±3%

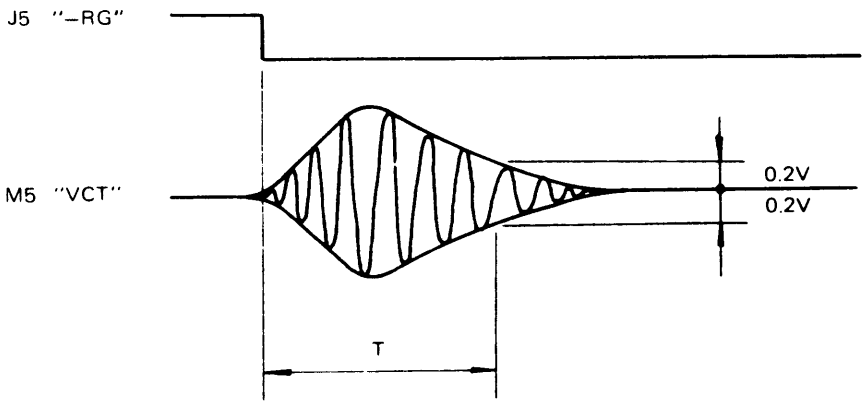
(2) Confirmation of Control Voltage
During power-on and during the read operation, observe the check terminal "VCT" and confirm that the waveform is as follows.

During Power-On



T: Less than 15 sec.

During the beginning of the read operation

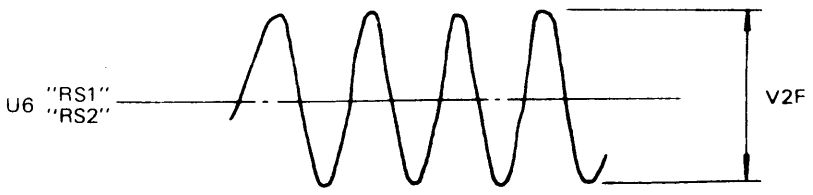


T: Less than 5μsec.

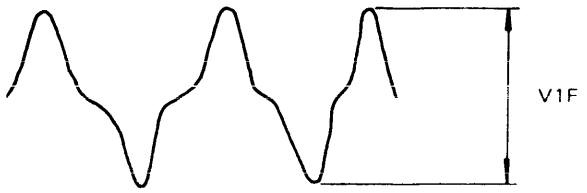
6.2.8 Observation of the Read Waveform

Write the repetitive data pattern "00" then "10", and using the differential mode, observe the output level on the check terminals "RS1" and "RS2" on the Control O (CQOM) PCB. Confirm that they satisfy the following standards in every cylinder and data head. In general, the read output level and resolution ratio at cylinder 243 are the most critical.

"00" Read Waveform



"10" Read Waveform



Read output level V2F > 0.4V
Resolution ratio (V2F/V1F) x 100 > 55%

Note: Differential observation mode:
Use both channels of the oscilloscope. Connect one channel to "RS1" and the other to "RS2". Set one of the two channels to invert and observe by the add mode. Make sure to connect ground lines to the two probes, and then connect the grounds to the 0V terminal on the PCB assembly, near "RS1" and "RS2".

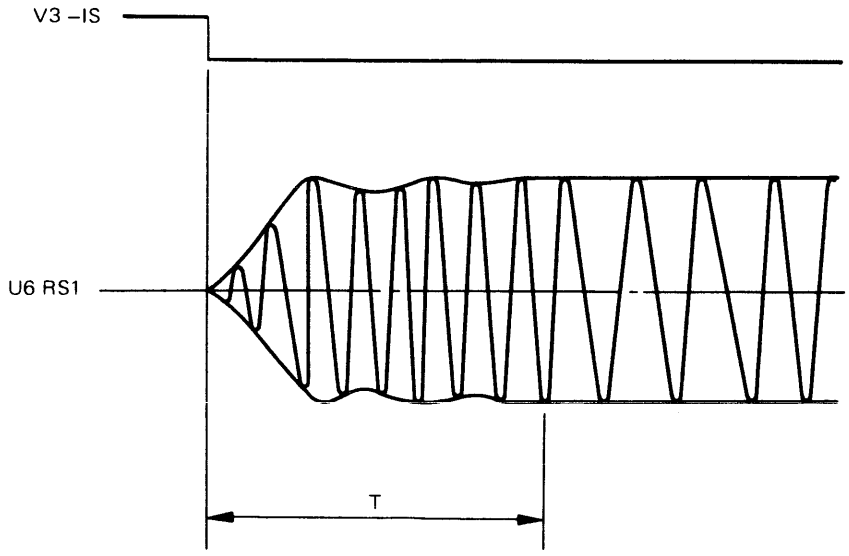
6.2.9 Observation of the AGC Amplifier Output Waveform

Observe the AGC output level on the check terminals "RS3" and "RS4" by differential mode, and confirm the following specification is satisfied regardless of cylinder address and data pattern.

R5 $^{\text{"RS3"}}_{\text{"RS4"}}$ 3.0V ±0.3V

6.2.10 Check of the Settling Waveform after Seeking

Begin a continuous alternate seek operation between two cylinders. Observe the read waveform after SEEK completion at the check terminal "RS1" on the Control O (CQOM).PCB. Confirm that it satisfies the following standards.



T: Less than 30ms

Section 7
Spare Parts

7. SPARE PARTS

To Be Supplied.

Section 8
IC Detail

8. IC DETAIL

8.1 OUTLINE

This section describes functions of TTL, ECL, CMOS, Linear IC's and original IC's.

8.2 LOGIC CONVENTION AND SYMBOLOGY

8.2.1 TTL Logic

MRX 112/114 micro disk drives use +5V transistor—transistor—Logic. TTL logic is defined in terms of standard POSITIVE LOGIC using the following definitions:

High Voltage = Logical "1"
Low Voltage = Logical "0"

The input/output logic levels of TTL are defined as follows:

(1) TTL Medium/High Speed IC

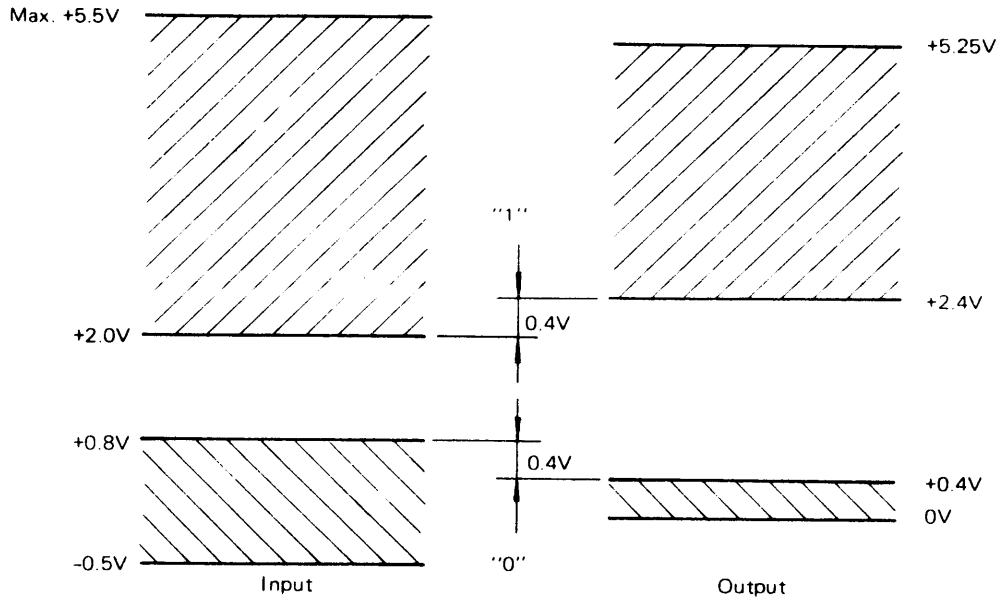


Fig. 8.1 TTL Medium/High Speed IC Level

(2) TTL Super High Speed IC

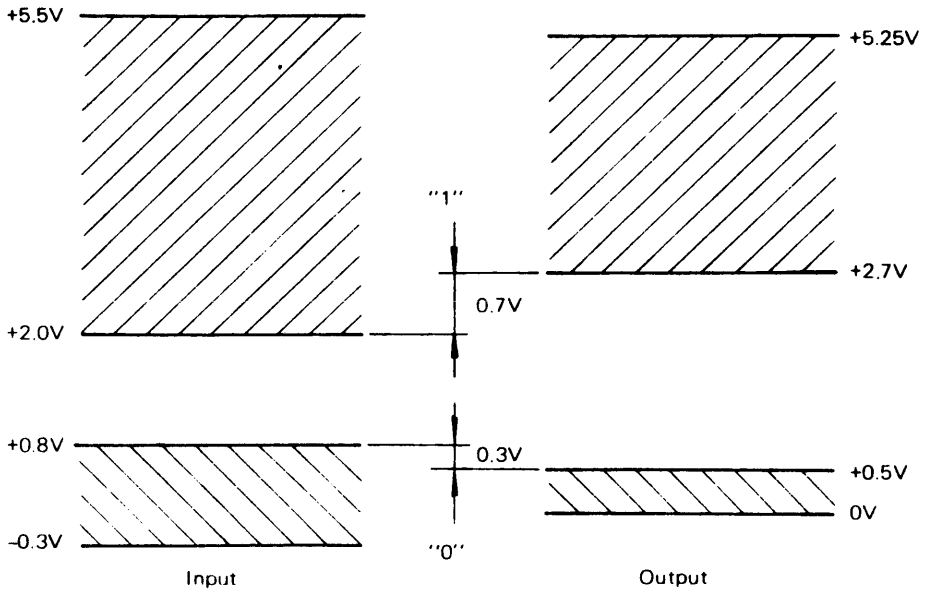


Fig. 8.2 TTL Super High Speed IC Level

(3) Low Power Schottky

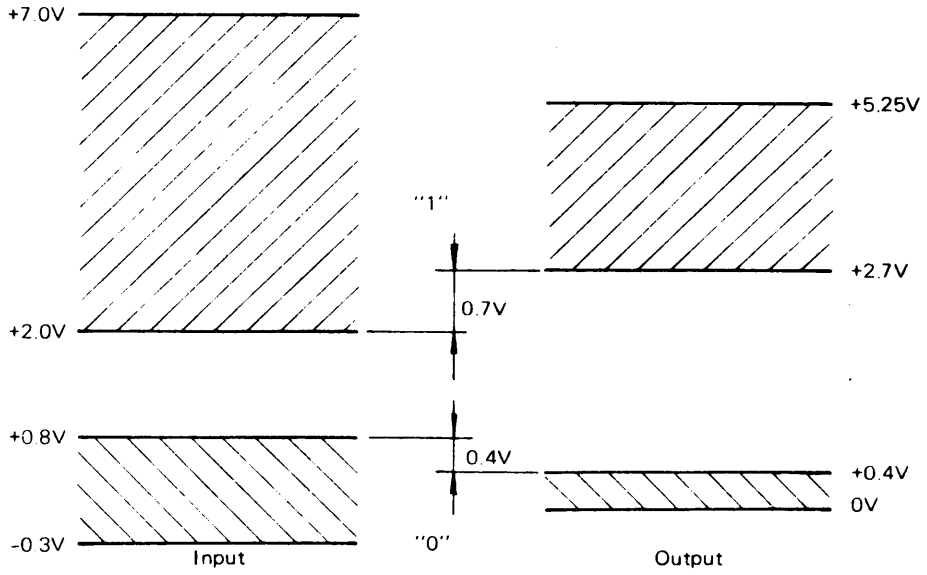


Fig. 8.3 Low Power Schottky Level

8.2.2 ECL Logic

The unit uses ECL (Emitter-Coupled-Logic). The ECL logic is defined as POSITIVE LOGIC used for the diffinition as follows.

High Voltage = Logical "1"
Low Voltage = Logical "0"

The input/output logic levels of ECL are defined as follows.

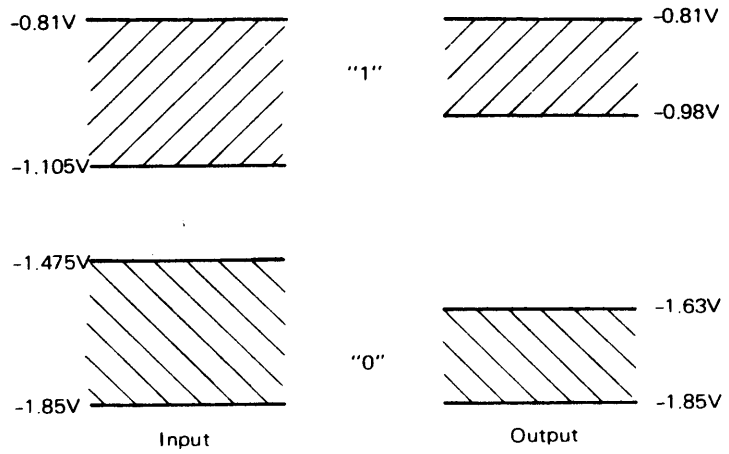


Fig. 8.4 ECL Logic Level

8.2.3 CMOS Logic

The unit uses CMOS (Complementary Metal Oxide Semiconductor). The CMOS logic is defined as POSITIVE LOGIC used for the definition as follows.

High Voltage = Logic "1"
Low Voltage = Logic "0"

The input/output logic levels of CMOS are defined as follows.

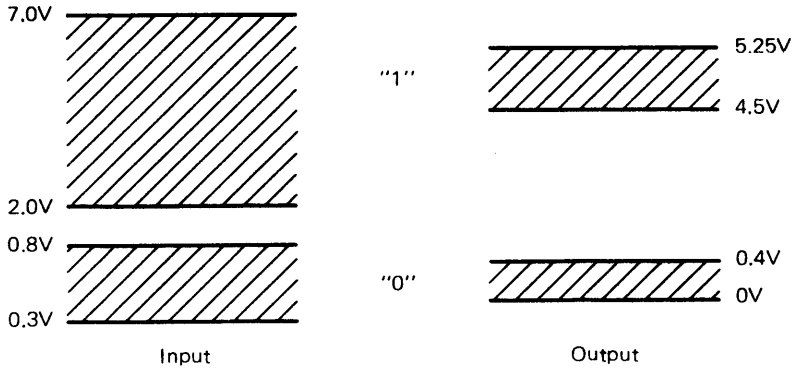
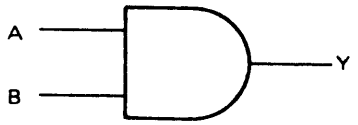


Fig. 8.5 CMOS Logic Level

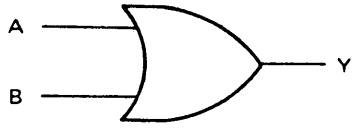
8.2.4 Logic Symbology

The following conventions are provided to aid in understanding the symbology used in this manual.

(1) TTL



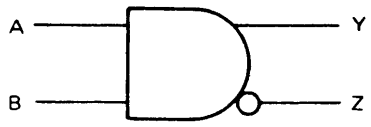
The diagram shows AND gate.
$Y = A \cdot B$



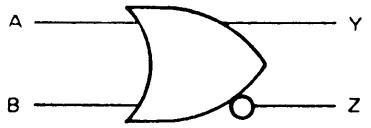
The diagram shows OR gate.
$Y = A + B$

A circle placed on any input line or on the output line indicates that logical "0" is the significant state.
The absence of a circle indicates logical "1" is the significant state.

(2) ECL



This indicates AND/NAND gate.
$Y = A \cdot B = \overline{Z}$

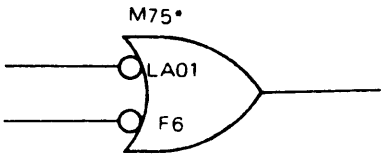


This indicates OR/NOR gate.
$Y = A + B = \overline{Z}$

This symbol has the same meansing in TTL.

(3) All logic symbols on each logic diagram are identified by a sequential numbering and element type code.

For example:



M75*: Sequential part number of each parts list.
LA01: Abbreviation of the element code name.
F6: Physical installation position of an element on the printed circuit assembly.

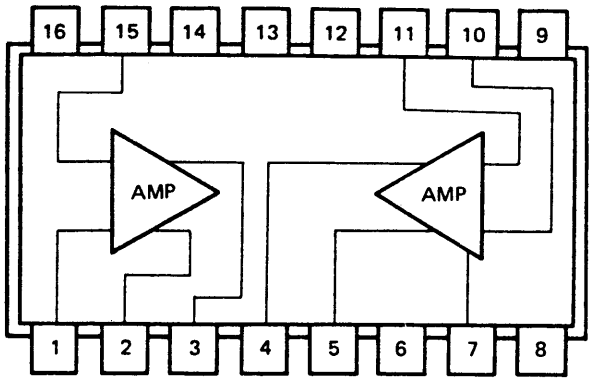
8.3 SPECIAL IC's

(1) MB4303C

AGC Amplifier

The MB4303C is a Automatic-Gain-Control Amplifier with Differential Inputs and Outputs. It contains another Differential Amplifier.

TOP VIEW

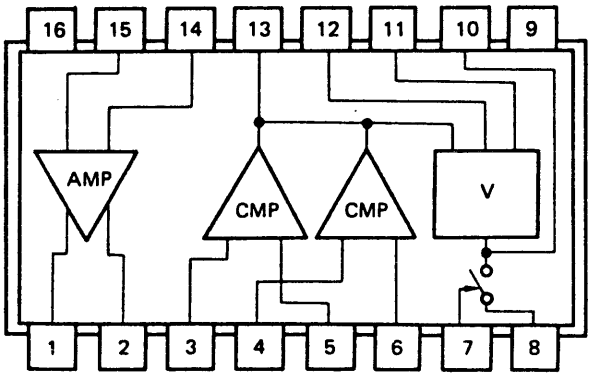


1: INPUT2
2: OUTPUT2
3: OUTPUT2
4: OUTPUT1
5: OUTPUT1
6: VR
7: VAGC
8: VG (GND)
9: Vee
10: INPUT1
11: INPUT1
12: GA
13: GB
14: VBB
15: INPUT2
16: Vcc

(2) MB4311C

Peak Detector

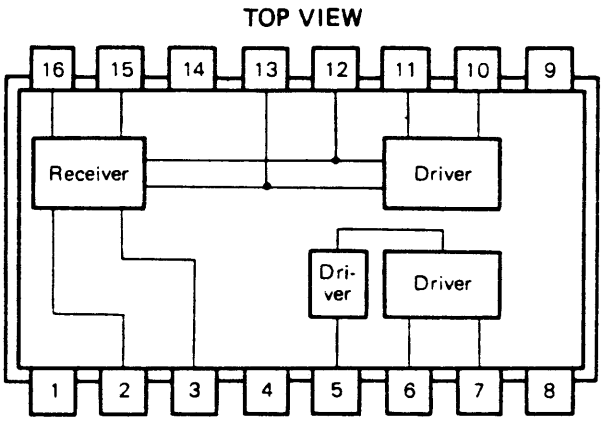
TOP VIEW



1: OUT1
2: OUT1
3: IN2
4: IN2
5: VH
6: VL
7: SQ
8: GND
9: Vee
10: AGCG
11: CLA
12: CAP
13: VAGC
14: IN1
15: IN1
16: Vcc

(3) MB4316C

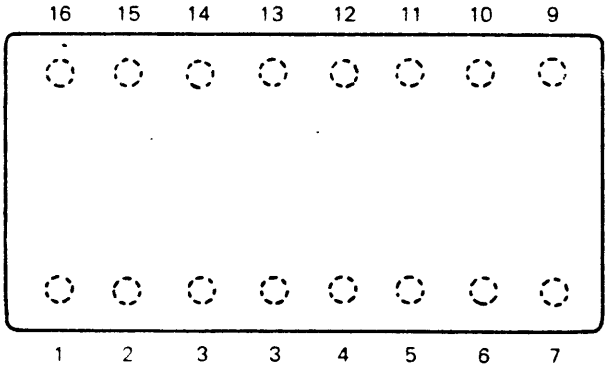
Read/Write Bus Switch



1: Vee2
2: GAN2
3: GAN1
4: IN5
5: IN4
6: OUT5
7: OUT6
8: GND
9: Vee1
10: IN2
11: IN3
12: OUT4
13: OUT3
14: IN1
15: OUT2
16: OUT1

(4) DV18

Clock Driver



1: N.C.
2: ENB
3: X_{E1}
4: N.C.
5: N.C.
6: N.C.
7: X_{EZ}
8: GND
9: N.C.
10: N.C.
11: N.C.
12: N.C.
13: OUT
14: N.C.
15: Vcc
16: N.C.

(5) MB15207C Bipolar 500 Gates Array

This IC has the following functions.

- O NRZ to MFM encoder with write compensation
- O PLO/VFO phase detector
- O Data Separator
- O Physical Index detector
- O Write Fault detector

Fig. 8.6 illustrates the pin assignment and Table 8.1 shows the pin numbers and names.

(6) MB60512C CMOS 2000 Gates Array

This IC has the following functions.

- O Stepping Motor Control
- O Sector/Index Generation
- O DC Spindle Motor Control

Fig. 8.6 illustrates the pin assignment and Table 8.2 shows the pin numbers and names.

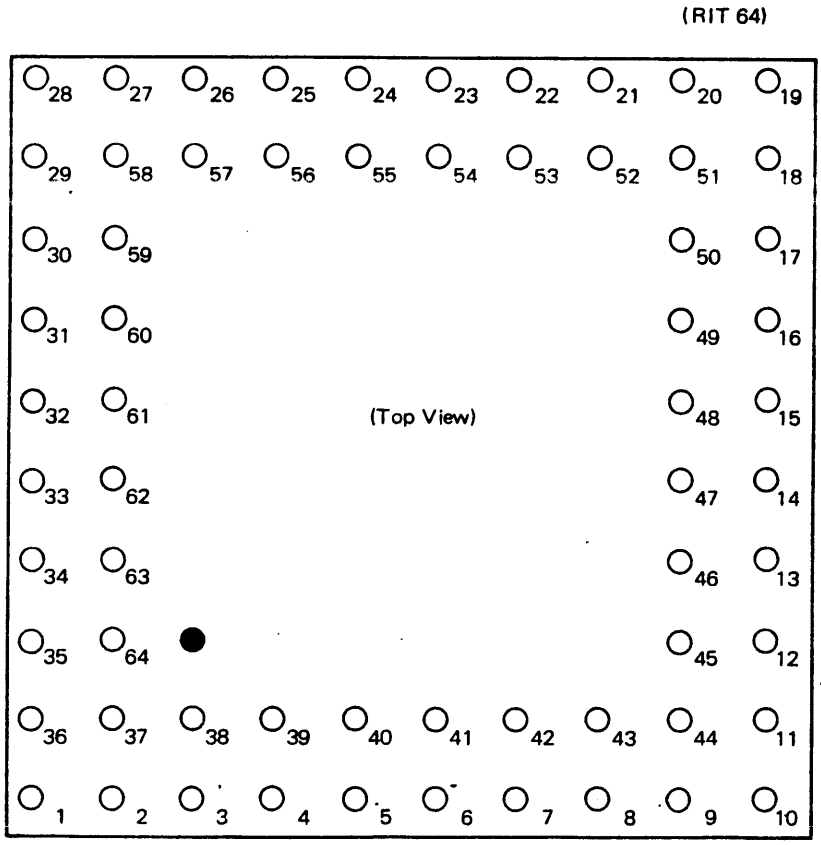


Fig. 8.6 MB15207/MB60512 Pin Assignment

Table 8.1 MB15207 Pin Numbers and Names

Pin No.	I/O	Name of Terminal	Pin No.	I/O	Name of Terminal	Pin No.	I/O	Name of Terminal	Pin No.	I/O	Name of Terminal
1	NC		17	I	RYCLR	33	I	ONT	49	O	GATES
2	O	*PDEC	18	I	CLK11	34	I	WDT	50	O	*RYCLR
3	O	P1/8	19	I	DLYCL	35	I	PSWCL	51	I	CLK10
4	NC		20	I	FMD	36	O	PSWDT	52	I	INDEX
5	I	PLOSW	21	O	PCL	37	I	DIAG	53	O	RDDT
6	I	PCL	22	O	WIN	38	O	PINC	54	VDD	GND
7	I	P1/16	23	I	*GAP00	39	O	P1/16	55	I	VF2F
8	I	*CLPLS	24	I	DTCL	40	VDD	GND	56	I	VFO2F
9	O	PINC	25	I	*RDMSK	41	I	*CPL	57	I	*VFODT
10	I	SKC	26	I	*VFODT	42	I	*CLR	58	I	RGT
11	O	ERROR	27	I	RAWDT	43	I	P1/16	59	O	LOCK
12	I	MLTSL	28	I	PLOSW	44	NC		60	O	*VFODT
13	I	UNS	29	O	VINC	45	O	*FAULT	61	VSS	+5V
14	I	*RDYRL	30	O	*VDEC	46	I	P2F	62	I	LTT
15	I	WGT	31	I	DLYSW	47	VSS	+5V	63	I	WCL
16	O	READY	32	I	ELT	48	I	*FCLR	64	O	WDTP

Table 8.2 MB60512 Pin Numbers and Names

Pin No.	I/O	Name of Terminal	Pin No.	I/O	Name of Terminal	Pin No.	I/O	Name of Terminal	Pin No.	I/O	Name of Terminal
1	O	CT5CA	17	I	PLO	33	I	BITI	49	I	CLK6
2	I	*CLR	18	I	ROMO3	34	O	*CT4CA	50	I	CLK8
3	I	DRSL1	19	I	ROMO2	35	O	*STPLD	51	I	ROMO1
4	I	SW3	20	I	ROMO0	36	I	*LDF0	52	I	ROMO7
5	I	GATES	21	I	ROMO6	37	O	DSKC	53	I	ROMO5
6	I	TRK0	22	I	ROMO4	38	O	SKCPT	54	VSS	GND
7	I	DIRON	23	O	*SOT2	39	O	DRTZ	55	O	*SOT0
8	I	STEP	24	O	*SOT1	40	VSS	GND	56	O	*SOT4
9	I	INX	25	O	*SOT3	41	O	DMCNT	57	I	BIT5
10	I	*F1/8	26	O	*DPAB	42	O	INDEX	58	I	BIT11
11	O	*DAC13	27	I	BIT12	43	O	SECT	59	I	BIT6
12	O	*DAC24	28	I	BIT10	44	I	SLSEC	60	I	BIT7
13	O	*PHAS1	29	I	BIT9	45	O	PHAS0	61	NC	
14	O	*PHAS3	30	I	BIT4	46	O	*PHAS2	62	I	BIT8
15	I	CLK7	31	I	BIT3	47	VDD	+5V	63	I	CT4CA
16	I	CLK3	32	I	BIT2	48	O	*PHAS4	64	I	*STPLR

8.4 IC INTERCHANGEABILITY

8.4.1 TTL IC Interchangeability

TYPE NO.	MARKING	DIRECT REPLACEMENT	FUNCTION
MB74LS00M	LS00	SN74LS00N	QUAD 2 NAND
MB74LS02M	LS02	SN74LS02N	QUAD 2 NOR
MB74LS04M	LS04	SN74LS04N	HEX INVERTER
MB74LS08M	LS08	SN74LS08N	QUAD 2 AND
MB74LS14M	LS14	SN74LS14N	HEX SCHMITT INVERTER
MB74LS42M	LS42	SN74LS42N	BCD TO DECIMAL DECORDER
MB74LS74M	LS74	SN74LS74N	DUAL D-TYPE FF
MB74LS86M	LS86	SN74LS86N	QUAD 2 EX-OR
MB74LS161M	LS161	SN74LS161N	4 BIT BINARY COUNTER
MB74LS164M	LS164	SN74LS164N	8 BIT SHIFT REGISTER
MB74LS174M	LS174	SN74LS174N	HEX D-TYPE FF
MB74LS191M	LS191	SN74LS191N	4 BIT UP/DOWN COUNTER
C74L-0980-0221	LS221	SN74LS221N	DUAL MONOSTABLE
MB74S04M	S04	SN74S04N	HEX INVERTER
MB74S08M	S08	SN74S08N	QUAD 2 AND
C74L-0650-0112	S112	SN74S112N	DUAL J-K, FF
C76L-0650-0124	S124	SN74S124N	DUAL VCO
C76L-0080-0026	LX32	SN7406N	HEX INVERTER with OPEN COLLECTOR OUTPUT
C76L-0080-0452	LX16	SN75452BP	DUAL 2 NAND PERIPHERAL DV
MB412C	412	AMD26LS31	DUAL LINE DV
MB413C	413	AMD26LS32	QUAD LINE RV
MB463M	463	SN7438N	QUAD 2 NAND BUFFER
MB434M	434	SN75451BP	DUAL 2 AND PERIPHERAL DV
MB7052C	7052	IM5603A	256X4 BIP-PROM

8.4.2 ECL

TYPE NO.	MARKING	DIRECT REPLACEMENT	FUNCTION
MB10115C	115	MC10115L	QUAD RECEIVER
MB10116C	116	MC10116L	TRIPLE RECEIVER
MB10131C	131	MC10131L	DUAL D M-S FF
MB10124C	124	MC10124L	QUAD TTL TO ECL CONVERTER
MB10125C	125	MC10125L	QUAD ECL TO TTL CONVERTER

8.4.3 Linear IC

C76L-0420-0033	A339	μPC117C	COMPARATOR
C76L-0130-0002	A331	μPC271C	COMPARATOR
C76L-0422-0017	A358	μPC1251C	DUAL OP-AMP
MB3501M	A733	μA733MN	AMP

8.4.4 CMOS

MB84040BM	4040	MC14040BCP	12 BIT BINARY COUNTER
MB84020BM	4020	MC14020BCP	14 BIT BINARY COUNTER

8.4.5 Special IC's

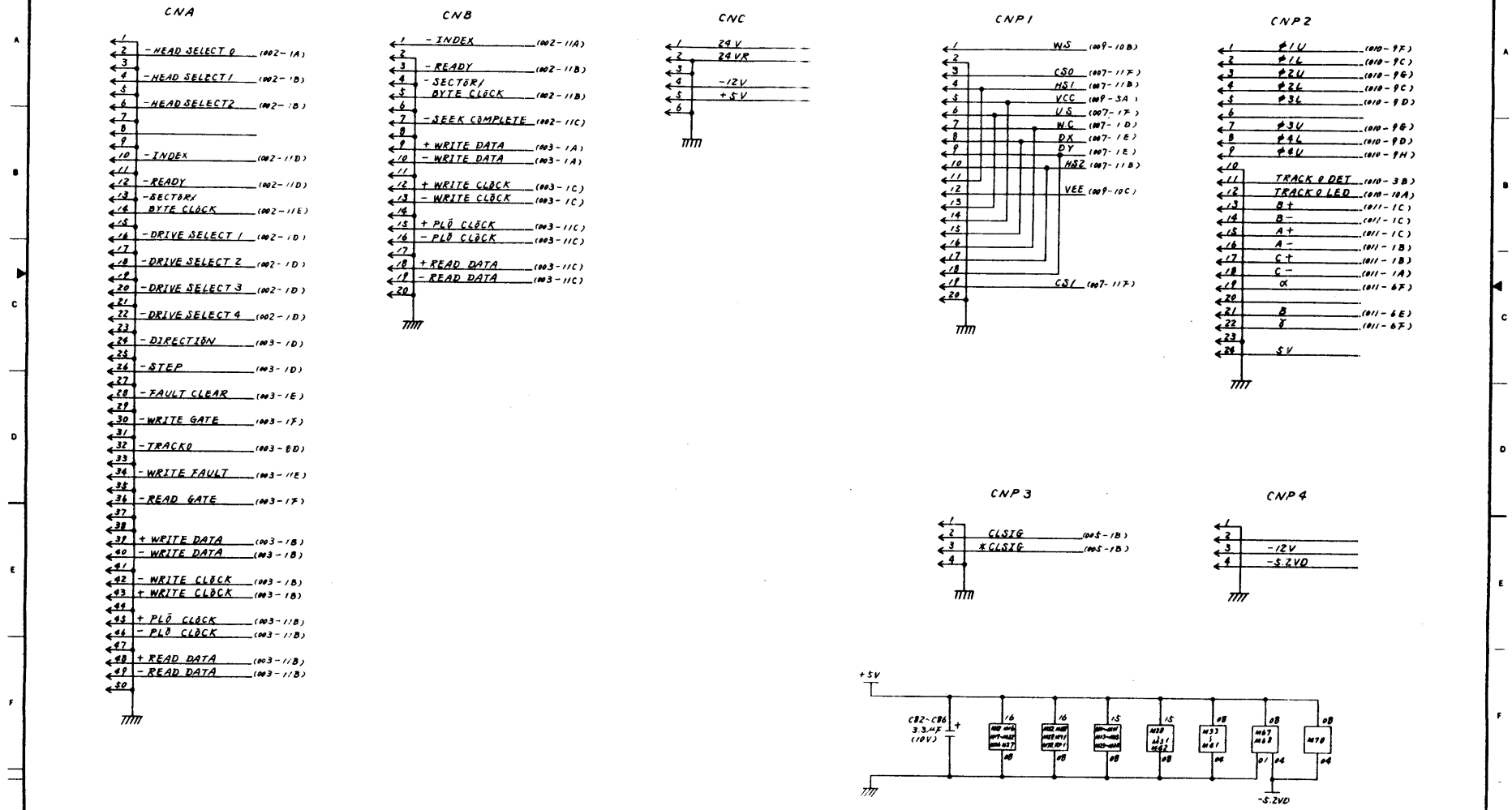
MB4303C	A4303	–	AGC AMP
MB4311C	A4311	–	PEAK DETECTOR
MB4316C	A4316	–	READ/WRITE BUS SWITCH
MB15207C	MB15207	–	DATA ENCODE/DECODE CIRCUIT
MB60512C	MB60512	–	STEPPER CONTROL
C.G24103A	DV18	–	CLOCK DRIVER

Section 9
Parts List

9. PARTS LIST

To Be Supplied.

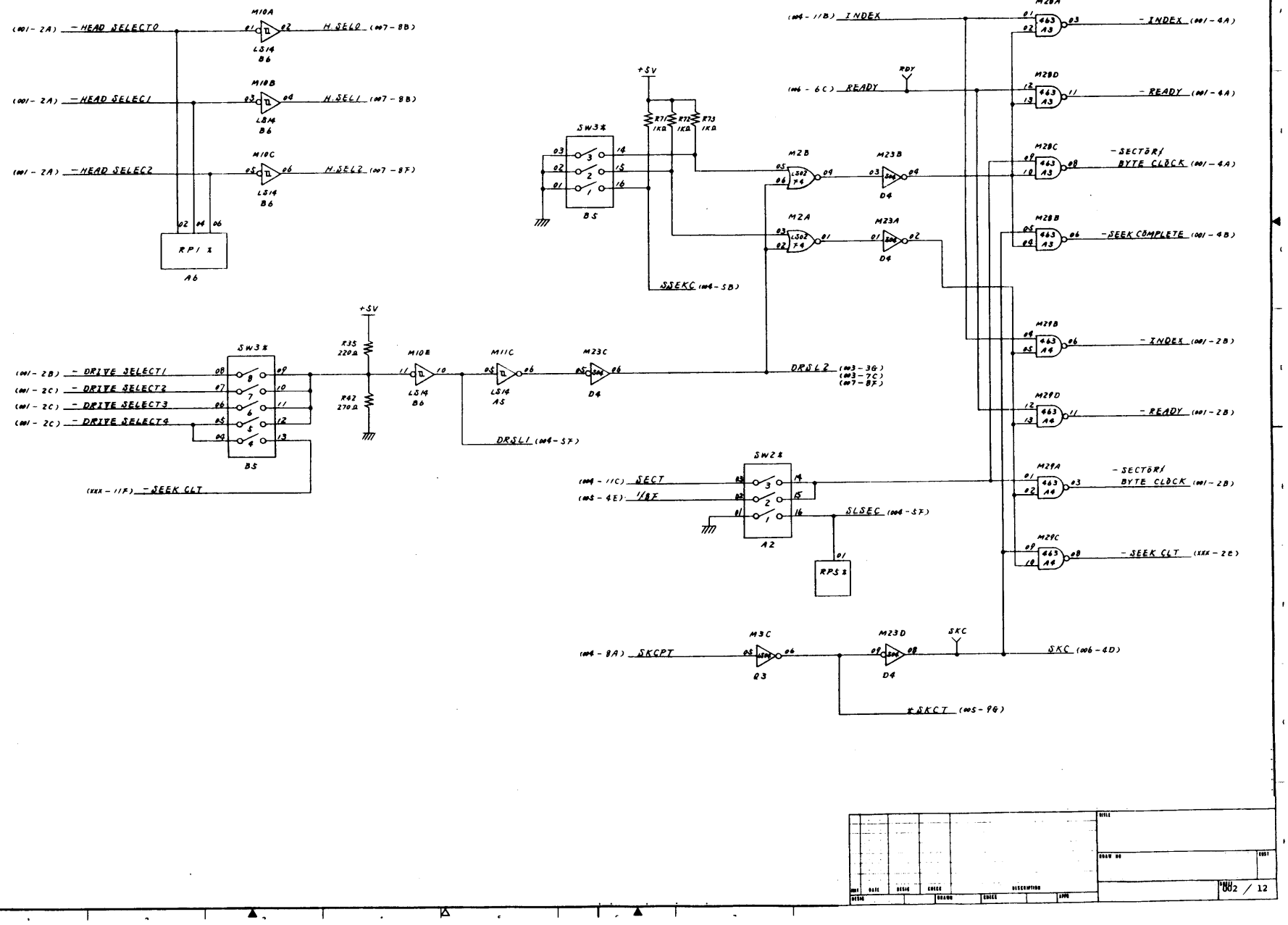
Section 10
Schematics

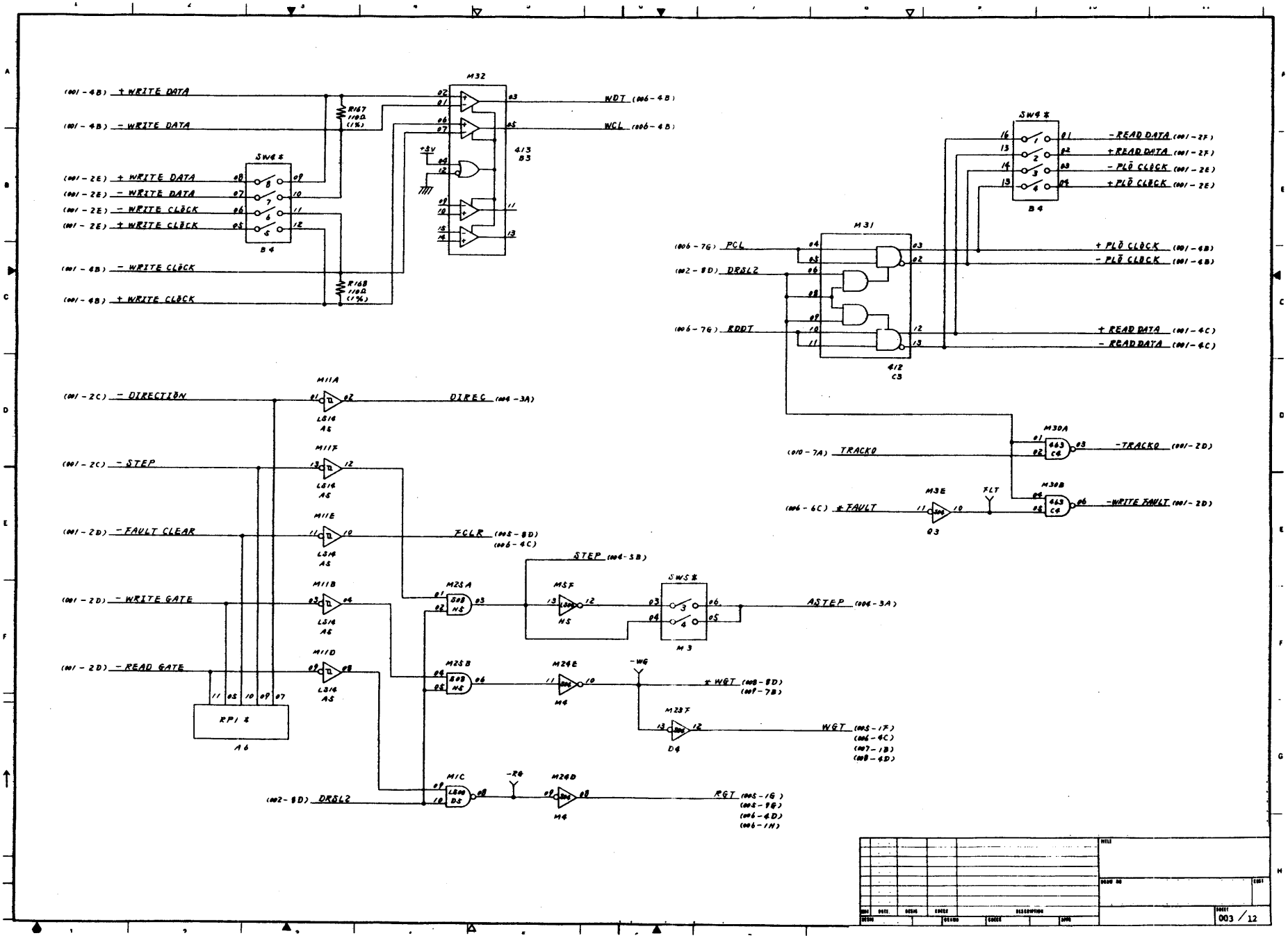


CONTROLLER 0 (CQOM)
CIRCUIT DIAGRAM

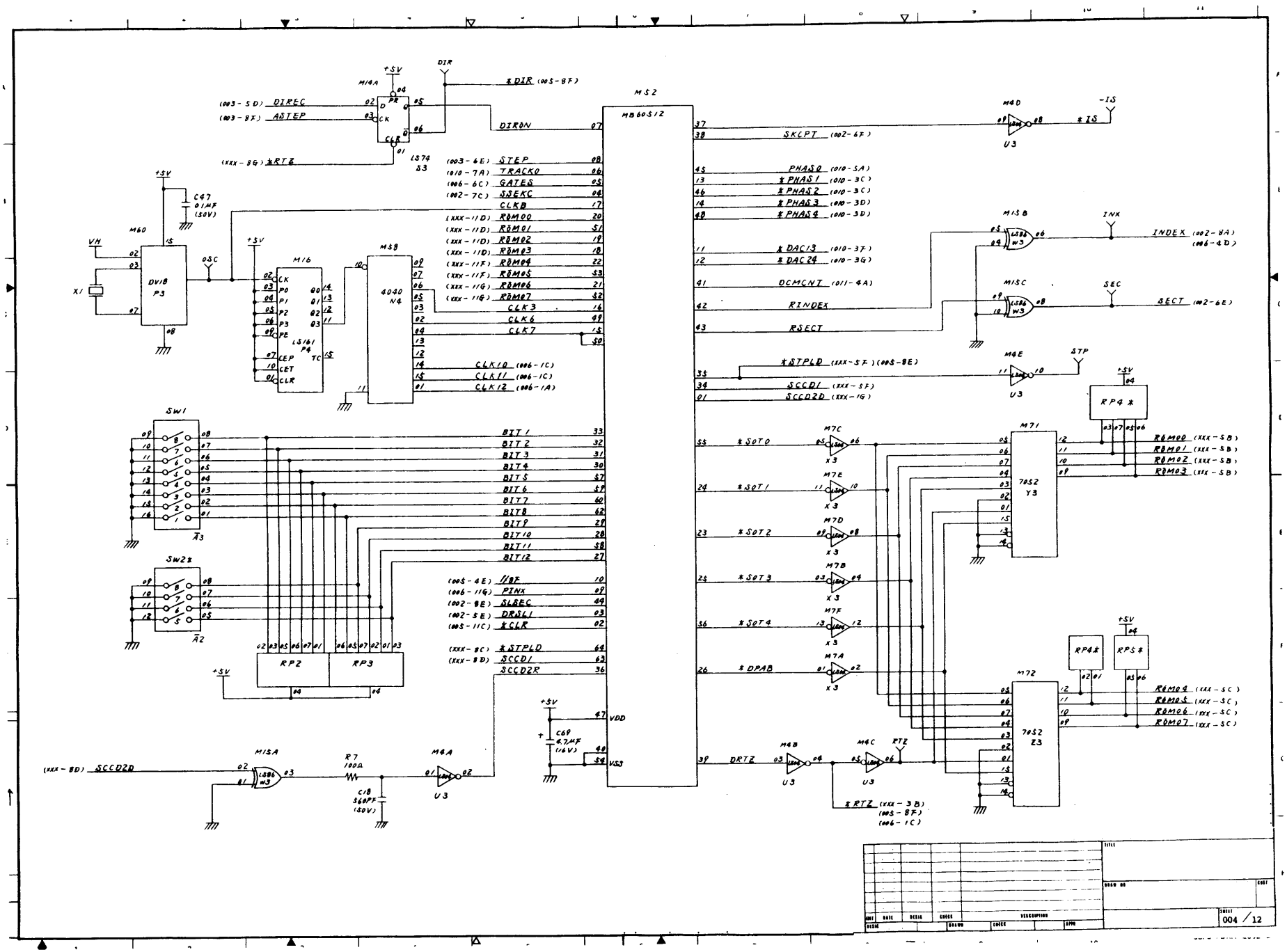
001 / 12

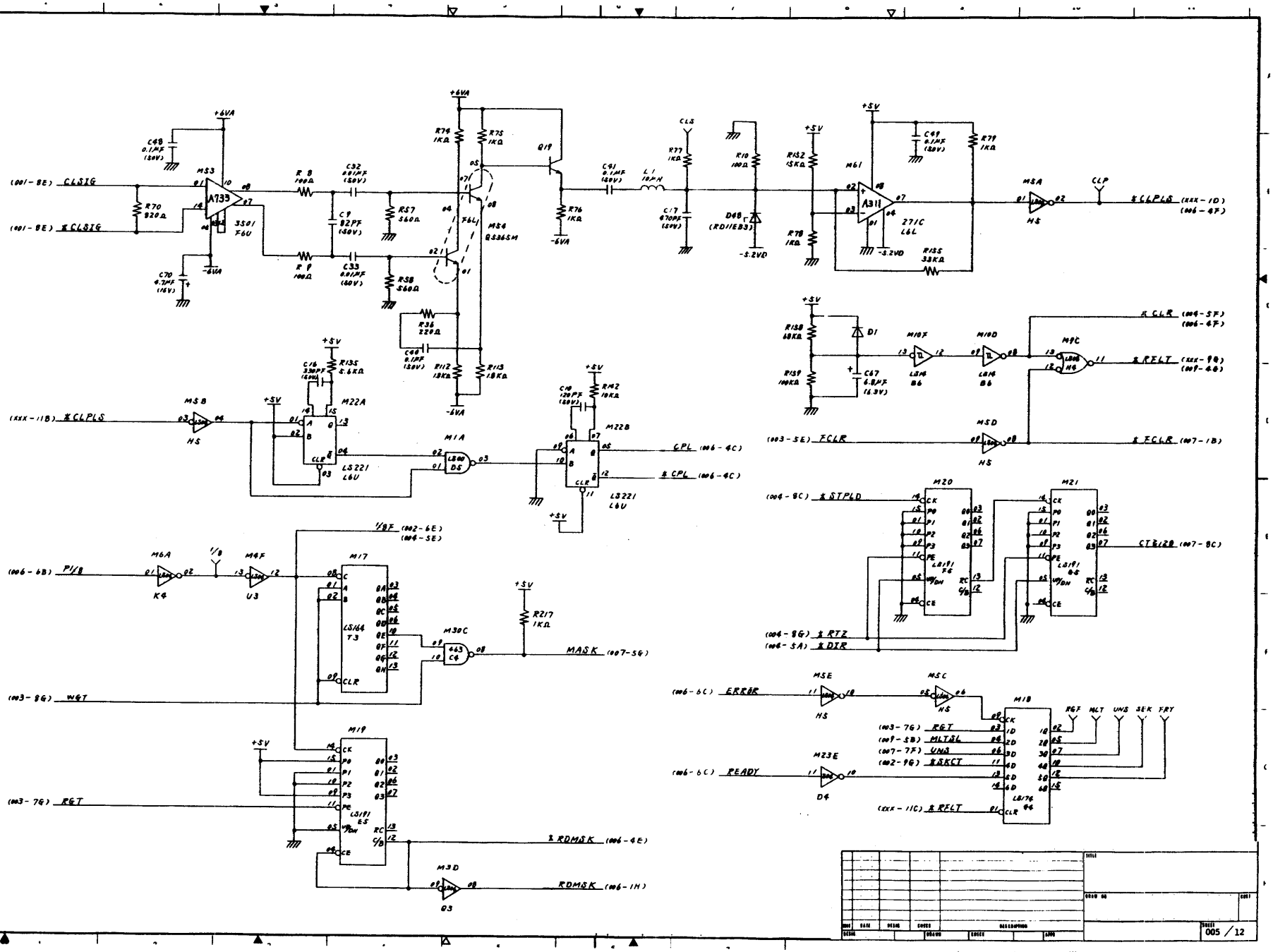
10-1

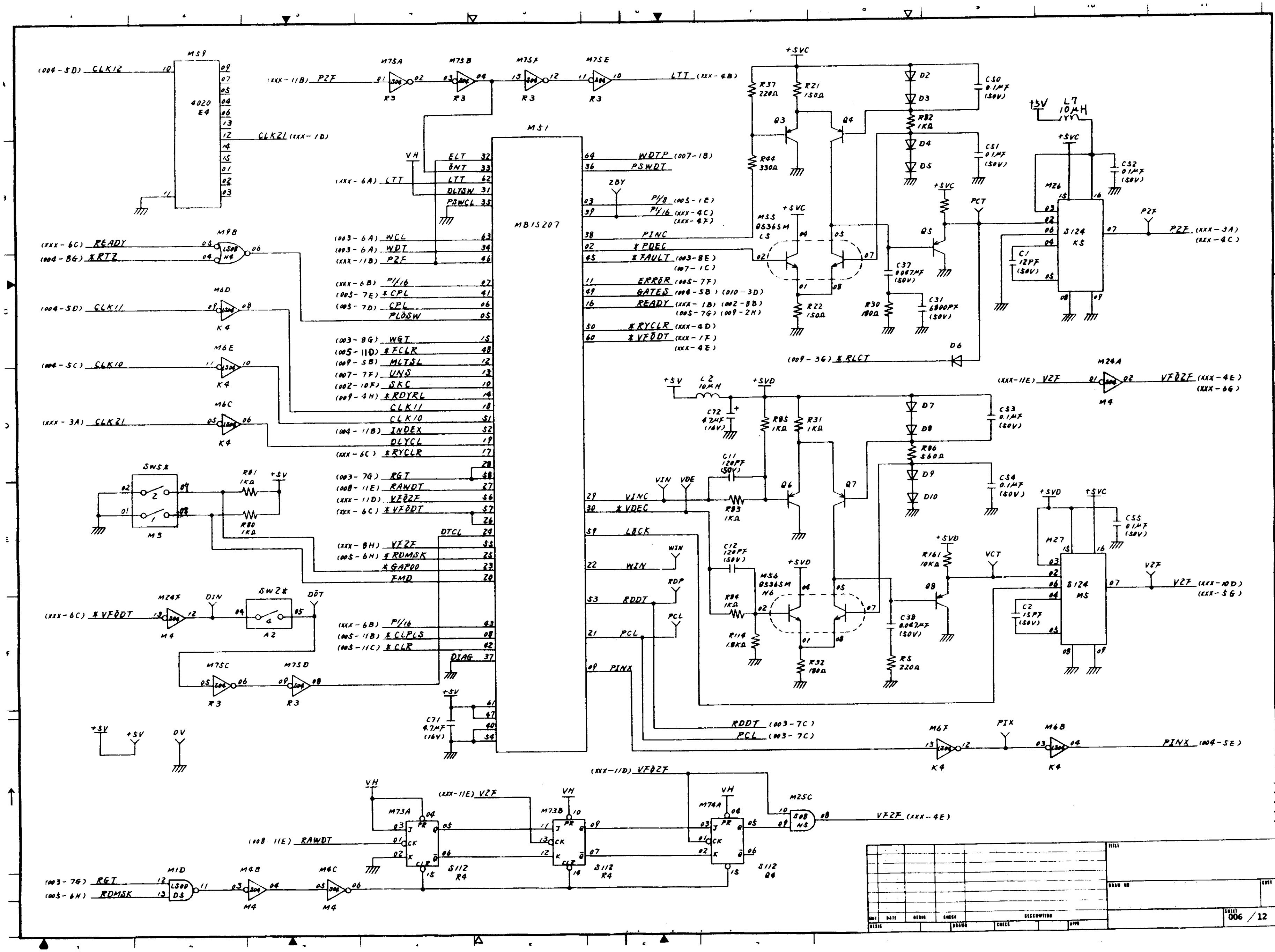

(001-2A) -HEAD SELECT0
(001-2A) -HEAD SELECT1
(001-2A) -HEAD SELECT2
M10A
M10B
M10C
LS14
B6
H.SEL0 (007-8B)
H.SEL1 (007-8B)
H.SEL2 (007-8F)
RP1 K
A6
+5V
R71 1KΩ
R72 1KΩ
R73 1KΩ
SW3 K
B5
SSEKC (006-5B)
(006-11B) INDEX
(006-6C) READY
RDY
M28A
M28D
M28C
M28B
M29B
M29D
M29A
M29C
463 A3
463 A6
-INDEX (001-4A)
-READY (001-4A)
-SECTOR/ BYTE CLOCK (001-4A)
-SEEK COMPLETE (001-4B)
-INDEX (001-2B)
-READY (001-2B)
-SECTOR/ BYTE CLOCK (001-2B)
-SEEK CLT (XXX-2E)
M2B
M2A
M23B
M23A
LS02 74
D4
(001-2B) -DRIVE SELECT1
(001-2C) -DRIVE SELECT2
(001-2C) -DRIVE SELECT3
(001-2C) -DRIVE SELECT4
R35 220Ω
R42 270Ω
M10E
M11C
M23C
LS14 A5
DRSL2 (003-3G) (003-7C) (007-8F)
DRSL1 (006-5F)
(XXX-11F) -SEEK CLT
SW2 K
A2
(006-11C) SECT
(005-4E) 1/8K
SLSEC (006-5F)
RPS K
M3C
M23D
Q3
SKC
(006-8A) SKCPT
SKC (006-4D)
*SKCT (005-9G)

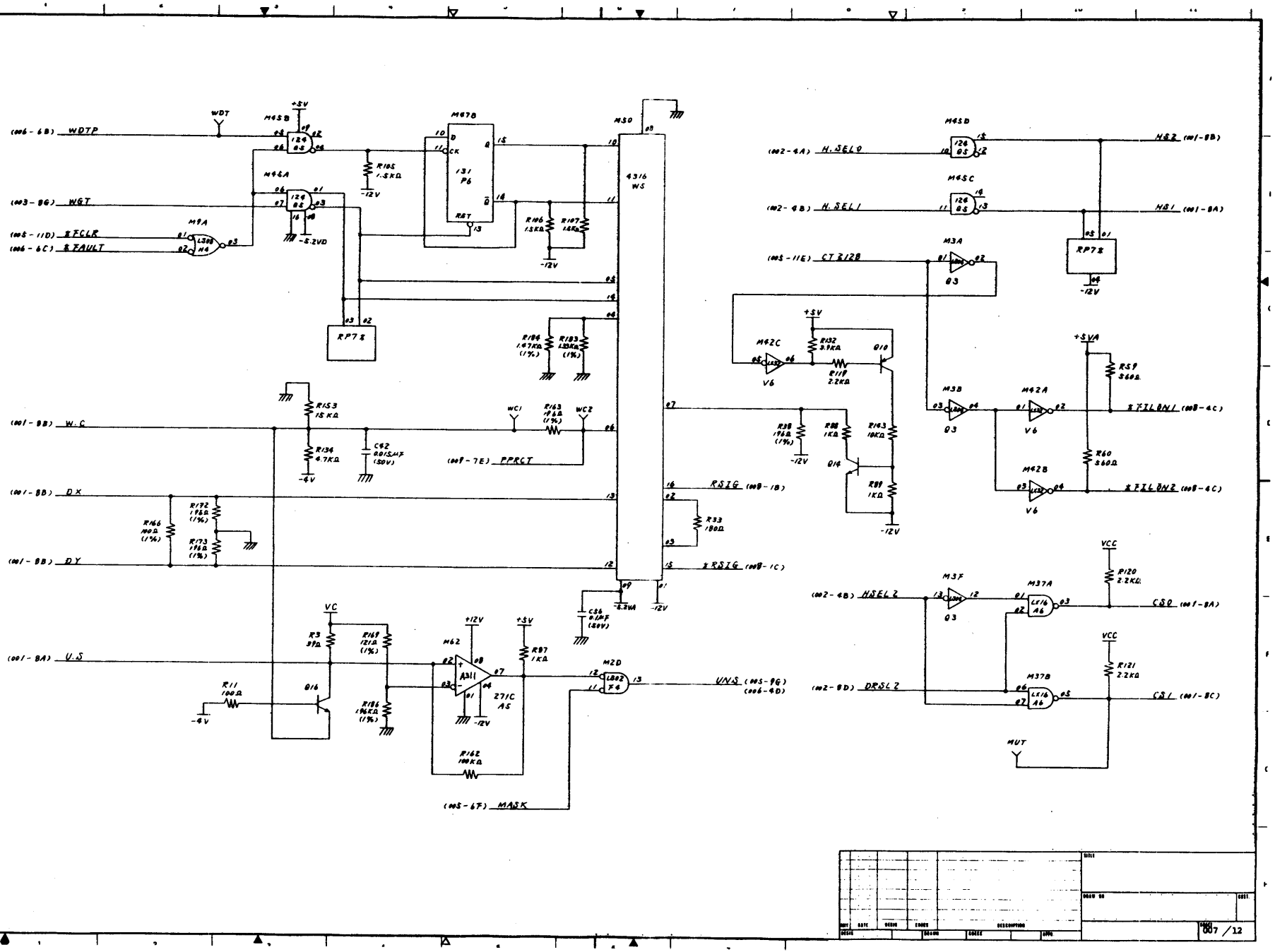

(001-4B) + WRITE DATA
(001-4B) - WRITE DATA
(001-2E) + WRITE DATA
(001-2E) - WRITE DATA
(001-2E) - WRITE CLOCK
(001-2E) + WRITE CLOCK
(001-4B) - WRITE CLOCK
(001-4B) + WRITE CLOCK
R167 110Ω (1%)
R168 110Ω (1%)
SW4 *
B4
M32
4/3 B3
WDT (006-4B)
WCL (006-4B)
+5V
(001-2C) - DIRECTION
(001-2C) - STEP
(001-2D) - FAULT CLEAR
(001-2D) - WRITE GATE
(001-2D) - READ GATE
M11A
M11F
M11E
M11B
M11D
LS14 A5
DIREC (004-3A)
FCLR (005-8D) (006-4C)
RP1 *
A6
STEP (004-3B)
M25A
M25B
M5F
M24E
M24D
M1C
SW5 *
M3
ASTEP (004-3A)
* WGT (008-8D) (007-7B)
WGT (005-1F) (006-4C) (007-1B) (008-4D)
-WG
-RG
M4
M23F
D4
(002-8D) DRSL2
RGT (005-1G) (005-9G) (006-4D) (006-1H)
(006-7G) PCL
(002-8D) DRSL2
(006-7G) RDDT
M31
4/2 C3
SW4 *
- READ DATA (001-2F)
+ READ DATA (001-2F)
- PLO CLOCK (001-2E)
+ PLO CLOCK (001-2E)
+ PLO CLOCK (001-4B)
- PLO CLOCK (001-4B)
+ READ DATA (001-4C)
- READ DATA (001-4C)
(010-7A) TRACK0
M30A
-TRACK0 (001-2D)
(006-6C) * FAULT
M3E
Q3
FLT
M30B
-WRITE FAULT (001-2D)

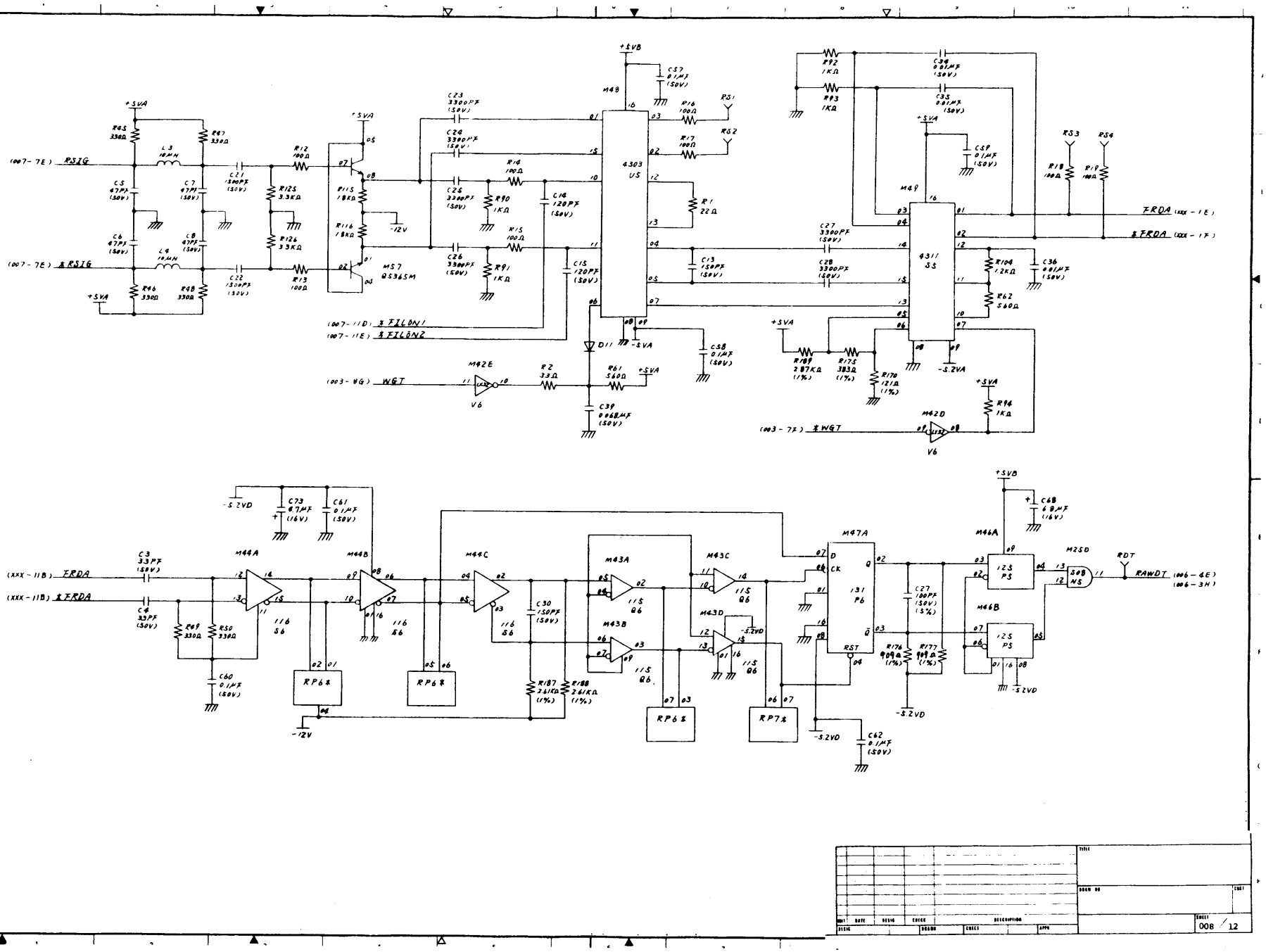
10-3


M14A
+5V
DIR
*DIR (005-8F)
(003-5D) DIREC
(003-8F) ASTEP
DIRON
(XXX-8G) *RTZ
LS74 S3
M52
MB605/12
(003-6E) STEP
(010-7A) TRACK0
(006-6C) GATE5
(002-7C) SSEKC
CLKB
(XXX-11D) RBM00
(XXX-11D) RBM01
(XXX-11D) RBM02
(XXX-11D) RBM03
(XXX-11F) RBM04
(XXX-11F) RBM05
(XXX-11G) RBM06
(XXX-11G) RBM07
CLK3
CLK6
CLK7
CLK10 (006-1C)
CLK11 (006-1C)
CLK12 (006-1A)
M60
VH
X1
DVI8 P3
OSC
C47 0.1MF (50V)
M16
LS161 P4
M58
4040 N4
SW1
A3
SW2*
A2
BIT1
BIT2
BIT3
BIT4
BIT5
BIT6
BIT7
BIT8
BIT9
BIT10
BIT11
BIT12
RP2
RP3
(005-4E) //BF
(006-11G) PINX
(002-8E) SLBEC
(002-5E) DRSLI
(005-11C) *CLR
(XXX-8C) *STPLD
(XXX-8D) SCCD1
SCCD2R
M15A
(XXX-8D) SCCD2D
R7 100Ω
C18 560PF (50V)
M14A
U3
C69 4.7MF (16V)
VDD
VSS
SKCPT (002-6F)
PHAS0 (010-5A)
*PHAS1 (010-3C)
*PHAS2 (010-3C)
*PHAS3 (010-3D)
*PHAS4 (010-3D)
*DAC13 (010-3F)
*DAC24 (010-3G)
DCMCNT (011-4A)
RINDEX
RSECT
M40
*IS
-IS
M15B
INX
INDEX (002-8A) (006-4D)
M15C
SEC
SECT (002-6E)
M4E
STP
*STPLD (XXX-5F) (005-8E)
SCCD1 (XXX-5F)
SCCD2D (XXX-1G)
M7C
M7E
M7D
M7B
M7F
M7A
*SOT0
*SOT1
*SOT2
*SOT3
*SOT4
*DPAB
X3
M71
7052 Y3
RP4*
RBM00 (XXX-5B)
RBM01 (XXX-5B)
RBM02 (XXX-5B)
RBM03 (XXX-5B)
M72
7052 Z3
RP5*
RBM04 (XXX-5C)
RBM05 (XXX-5C)
RBM06 (XXX-5C)
RBM07 (XXX-5C)
DRTZ
M4B
M4C
RTZ
*RTZ (XXX-3B) (005-8F) (006-1C)


(001-8E) CLSIG
(001-8E) *CLSIG
M33
A733
C48 0.1MF (50V)
R70 820Ω
C70 4.7MF (16V)
350/ F6U
R8 100Ω
C32 0.01MF (50V)
C9 82PF (50V)
C33 0.01MF (50V)
R57 560Ω
R58 560Ω
R36 220Ω
C60 0.1MF (50V)
R112 18KΩ
R113 18KΩ
M34 8.336SM
F6L
Q19
R74 1KΩ
R75 1KΩ
R76 1KΩ
C91 0.1MF (50V)
L1 10μH
CLS
R77 1KΩ
C17 470PF (5KV)
R10 100Ω
D48 (RD11EB3)
-5.2VD
R152 15KΩ
M61
A311
27/C L6L
R78 1KΩ
C49 0.1MF (50V)
R79 1KΩ
R135 38KΩ
M5A
CLP
*CLPLS (XXX-1D) (006-4F)
R138 68KΩ
R139 100KΩ
D1
C67 6.8MF (6.3V)
M10F
M10D
M9C
*CLR (006-5F) (006-6F)
*RELT (XXX-9B) (007-4B)
M5B
(XXX-11B) *CLPLS
C16 330PF (50V)
R135 5.6KΩ
M22A
LS221 L6U
M1A
M22B
CPL (006-4C)
*CPL (006-4C)
C19 120PF (50V)
RM2 10KΩ
M5D
(003-5E) FCLR
*FCLR (007-1B)
(006-8C) *STPLD
M20
M21
CTR/2B (007-8C)
(006-8G) *RTZ
(006-5A) *DIR
1/8F (002-6E) (006-5E)
(006-6B) P/8
M6A
K4
1/8
M6F
U3
M17
LS164 Y3
M30C
R217 1KΩ
MASK (007-5G)
(003-8G) WGT
M19
(003-7G) RGT
*RDMSK (006-4E)
M3D
Q3
RDMSK (006-1H)
(006-6C) ERROR
M5E
M5C
M18
(003-7G) RGT
(007-5B) MLTSL
(007-7F) UNS
(002-9G) *SSKCT
(XXX-11C) *RFLT
M23E
(006-6C) READY
D4
RGF
MLT
UNS
SEK
FRY
005 / 12


M59
4020
E4
CLK12
CLK21
M51
MB15207
PZF
LTT
WDTP
PSWDT
PINC
*PDEC
*FAULT
ERROR
GATES
READY
*RYCLR
*VFØDT
WCL
WDT
P/16
*CPL
CPL
PLØSW
WGT
*FCLR
MLTSL
UNS
SKC
*RDYRL
CLK11
CLK10
INDEX
DLYCL
RGT
RAWDT
VFØZF
VZF
*RDMSK
*GAPØØ
FMD
DTCL
*CLPLS
*CLR
DIAG
VINC
*VDEC
LBCK
WIN
RDDT
PCL
PINX
*RLCT
VCT
PCT
PIX
S124
S112
+SVC
+SVD
+5V
0V
VH
VFZF
006 / 12


WDT
(006-6B) WDTP
M43B
+5V
M46A
(003-8G) WGT
(005-11D) *FCLR
(006-6C) *FAULT
M9A
-5.2VD
R185 1.5KΩ
-12V
M47B
/31 P6
R186 1.5KΩ
R187 1.6KΩ
M30
4316 WS
RP7*
R184 1.67KΩ (1%)
R183 1.33KΩ (1%)
(001-8B) W.C
R153 15KΩ
R134 4.7KΩ
-4V
C92 0.015μF (50V)
WC1
R163 196Ω (1%)
WC2
(009-7E) PPRCT
(001-8D) D.X
(001-8D) D.Y
R172 196Ω (1%)
R173 196Ω (1%)
R166 100Ω (1%)
RSIG (008-1B)
R33 180Ω
*RSIG (008-1C)
C86 0.1μF (50V)
-5.2VA
VC
R3 39Ω
R169 121Ω (1%)
R186 196KΩ (1%)
Q16
R11 100Ω
-4V
M62
A311
27/C A5
+12V
+5V
R97 1KΩ
R162 100KΩ
M2D
LB02 F4
VINS (005-9G) (006-6D)
(005-6F) MASK
M45D
(002-4A) H.SEL0
H82 (001-8B)
M45C
(002-4B) H.SEL1
H81 (001-8A)
(005-11E) CT2128
M3A
03
M62C
V6
R132 3.3KΩ
R119 2.2KΩ
Q10
R38 196Ω (1%)
R88 1KΩ
R163 10KΩ
Q14
R89 1KΩ
M3B
M42A
M42B
R59 560Ω
R60 560Ω
*FILBN1 (008-4C)
*FILBN2 (008-4C)
(002-4B) HSEL2
M3F
M37A
M37B
VCC
R120 2.2KΩ
R121 2.2KΩ
CS0 (001-8A)
CS1 (001-8C)
(002-8D) DRSL2
MUT



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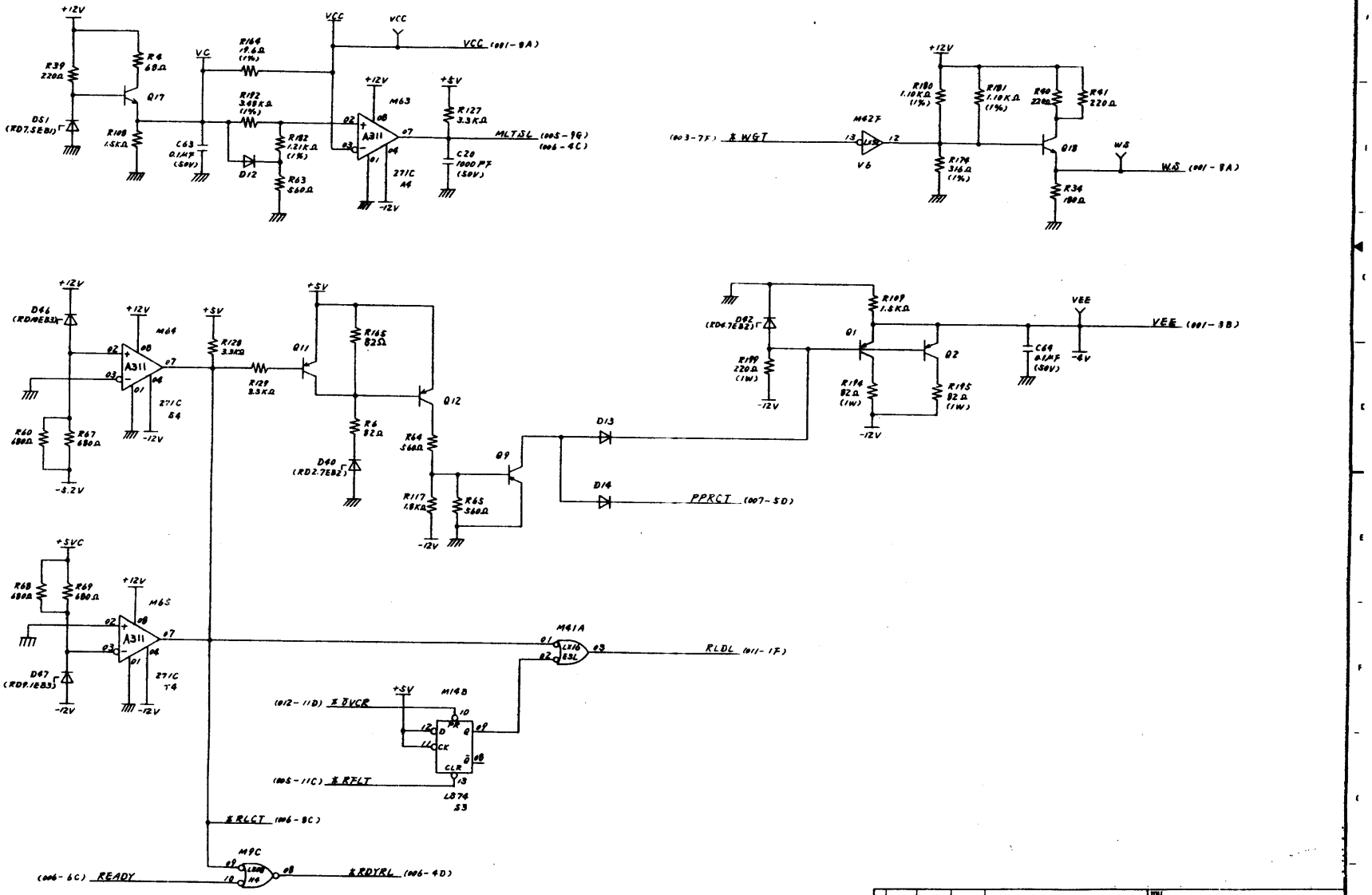
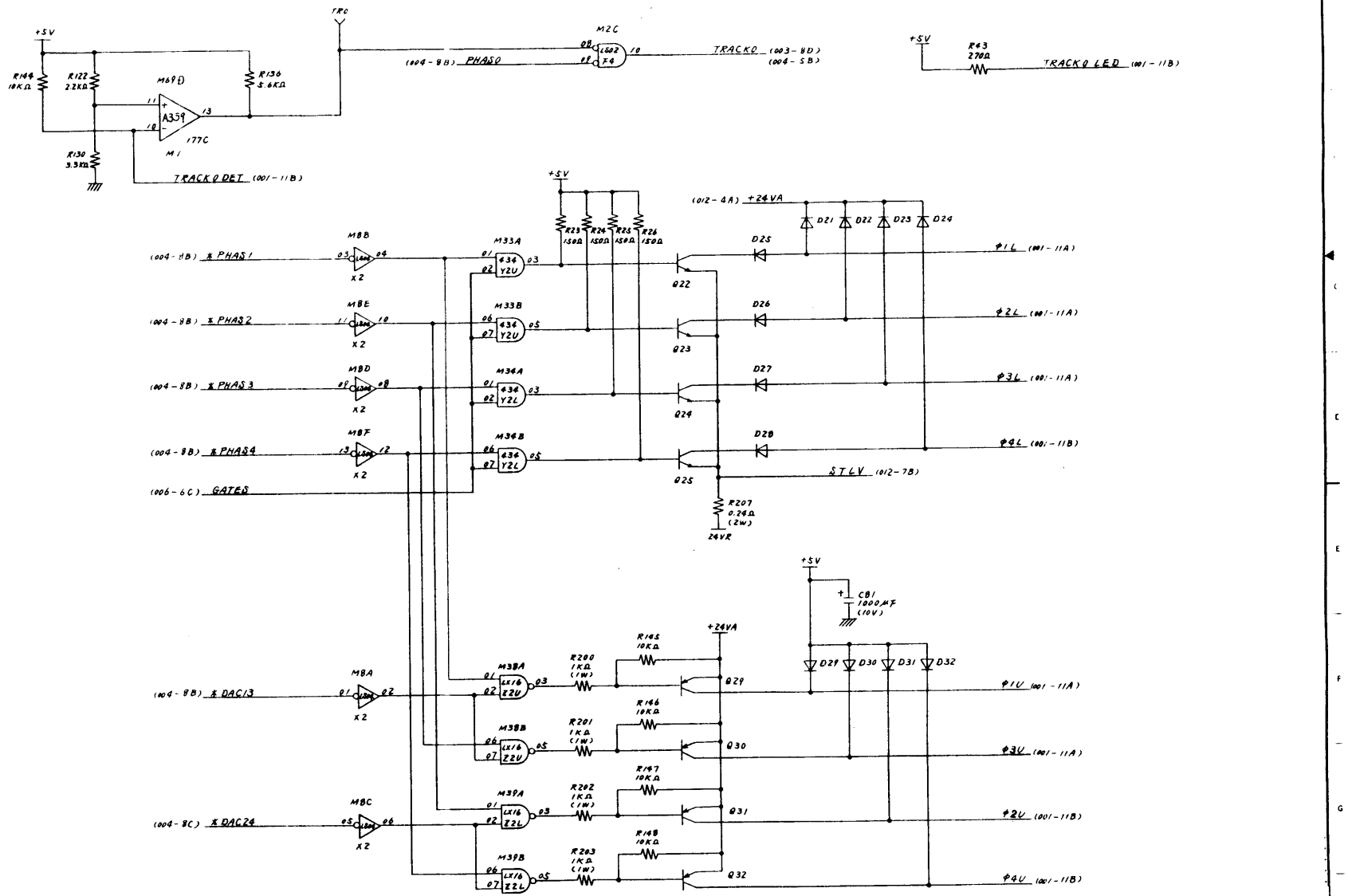
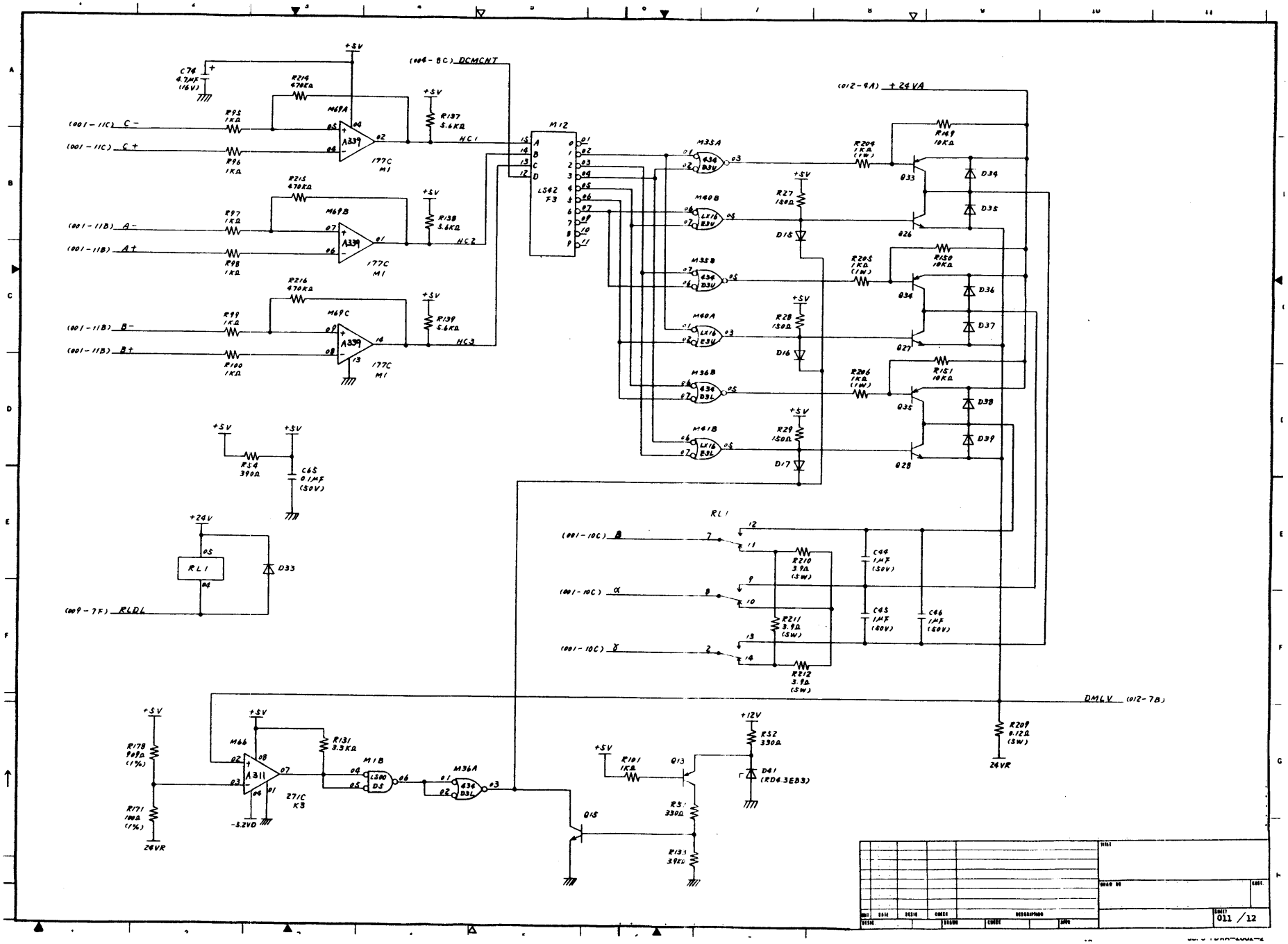
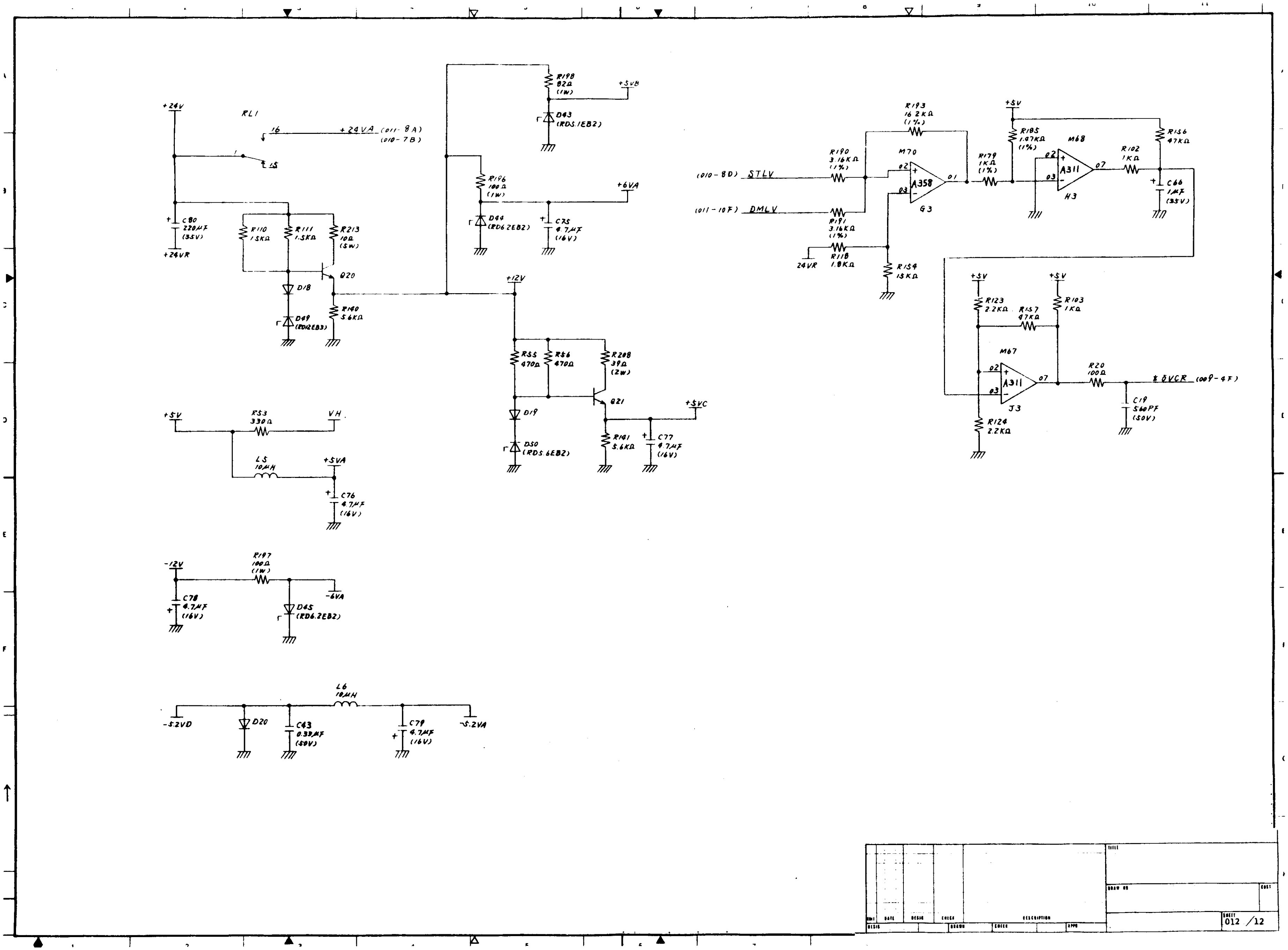
UNIT	DATE	DESIG	CHECK	DESCRIPTION	SHEET 008 / 12
DESIG		DRAWN	CHECK	APPR	


+12V
R39 220Ω
R6 68Ω
Q17
D51 (RD7.5EB3)
R108 1.5KΩ
VC
C63 0.1MF (50V)
R164 19.6Ω (1%)
R182 3.48K.Ω (1%)
R182 1.21K.Ω (1%)
D12
R63 560Ω
VCC
VCC (001-8A)
M63
A311
27/C A6
-12V
+5V
R127 3.3K.Ω
C20 1000 PF (50V)
MLTSL (005-9G) (006-4C)
(003-7F) X WGT
M62F
V6
R180 1.10K.Ω (1%)
R181 1.10K.Ω (1%)
R60 220Ω
R61 220Ω
R179 316Ω (1%)
Q18
R34 180Ω
WS
WS (001-8A)
D46 (RD8.2EB3)
M64
R28 3.3KΩ
R29 3.3K.Ω
Q11
R165 82Ω
Q12
R6 82Ω
D40 (RD2.7EB2)
R64 560Ω
R117 1.8KΩ
R65 560Ω
Q9
D13
D14
PPRCT (007-5D)
D42 (RD4.7EB2)
R109 1.6KΩ
Q1
Q2
R199 220Ω (1W)
R196 82Ω (1W)
R195 82Ω (1W)
C69 0.1MF (50V)
VEE
-6V
VEE (001-8B)
R60 680Ω
R67 680Ω
-8.2V
27/C B4
+5VC
R68 680Ω
R69 680Ω
M65
D47 (RD9.1EB3)
27/C Y4
M41A
LX10 83L
RLDL (011-1F)
(012-11D) X DVCR
M14B
LS74 S3
(005-11C) X RFLT
X RLCT (006-8C)
M9C
(006-6C) READY
X RDYRL (006-4D)

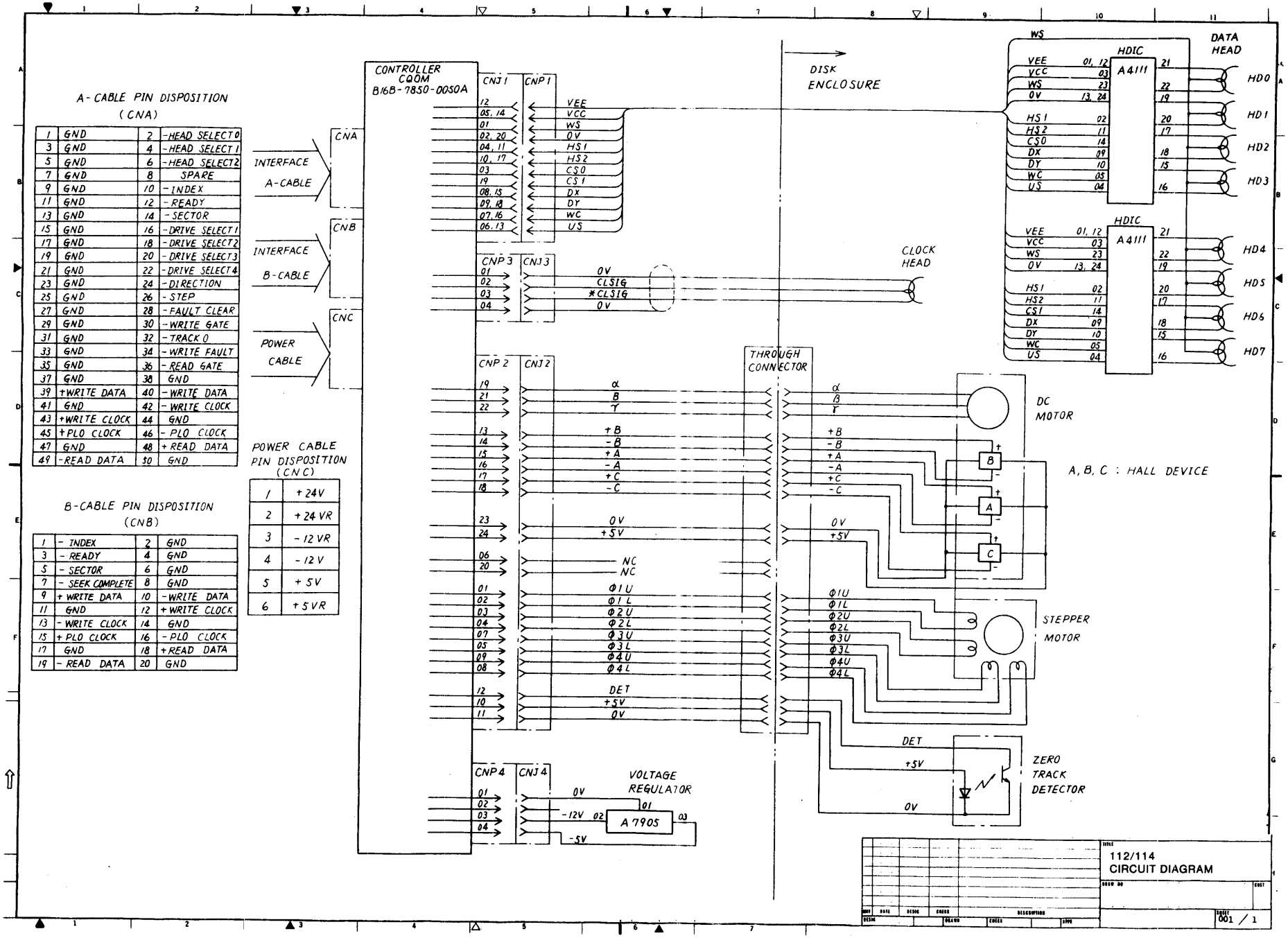
009 / 12


+5V
TRO
M2C
R144 10KΩ
R122 2.2KΩ
M69D
A359
R136 5.6KΩ
R130 3.3KΩ
M1
177C
TRACK 0 DET (001-11B)
(004-8B) PHAS0
TRACK0 (003-8D) (004-5B)
R43 270Ω
TRACK 0 LED (001-11B)
(012-4A) +24VA
D21 D22 D23 D24
R23 150Ω R24 150Ω R25 150Ω R26 150Ω
M8B (004-8B) *PHAS1
M8E (004-8B) *PHAS2
M8D (004-8B) *PHAS3
M8F (004-8B) *PHAS4
(006-6C) GATE5
X2
M33A M33B M34A M34B
Q22 Q23 Q24 Q25
D25 D26 D27 D28
Φ1L (001-11A)
Φ2L (001-11A)
Φ3L (001-11A)
Φ4L (001-11B)
STLV (012-7B)
R207 0.24Ω (2W) Z4VR
M8A (004-8B) *DAC13
M8C (004-8C) *DAC24
M38A M38B M39A M39B
R200 1KΩ (1W) R201 1KΩ (1W) R202 1KΩ (1W) R203 1KΩ (1W)
R145 10KΩ R146 10KΩ R147 10KΩ R148 10KΩ
Q29 Q30 Q31 Q32
D29 D30 D31 D32
Φ1V (001-11A)
Φ3V (001-11A)
Φ2V (001-11B)
Φ4V (001-11B)
C81 1000MF (10V)
+24VA
SHEET 010 / 12


(001-11C) C-
(001-11C) C+
(001-11B) A-
(001-11B) A+
(001-11B) B-
(001-11B) B+
(006-8C) DCMCNT
(012-9A) +24VA
(001-10C) β
(001-10C) α
(001-10C) γ
(009-7F) RLDL
DMLV (012-7B)
24VR
-5.2VD
+5V
+24V
+12V
C76 4.7MF (16V)
R214 470KΩ
R215 470KΩ
R216 470KΩ
R95 1KΩ
R96 1KΩ
R97 1KΩ
R98 1KΩ
R99 1KΩ
R100 1KΩ
R137 5.6KΩ
R138 5.6KΩ
R139 5.6KΩ
HC1
HC2
HC3
M69A
M69B
M69C
A339
177C M1
M12
LS42 F3
M35A
M40B
M35B
M40A
M36B
M41B
LX16 B3V
434 B3V
434 B3L
LX16 B3L
R204 1KΩ (1W)
R205 1KΩ (1W)
R206 1KΩ (1W)
R207 1KΩ (1W)
R27 150Ω
R28 150Ω
R29 150Ω
R149 10KΩ
R150 10KΩ
R151 10KΩ
R152 10KΩ
D15
D16
D17
D34
D35
D36
D37
D38
D39
Q33
Q34
Q35
Q36
RL1
D33
C44 1MF (50V)
C45 1MF (50V)
C46 1MF (50V)
R210 3.9Ω (5W)
R211 3.9Ω (5W)
R212 3.9Ω (5W)
R208 0.12Ω (5W)
R54 390Ω
C45 0.1MF (50V)
R178 909Ω (1%)
R171 100Ω (1%)
M66
A311
271C K3
R131 3.3KΩ
M1B
LS00 D5
M36A
R101 1KΩ
Q13
Q15
D41 (RD4.3EB3)
R52 330Ω
R53 330Ω
R133 3.9KΩ
011 / 12


+24V
RL1
16
+24VA (011-8A)
(010-7B)
C80
220μF
(35V)
+24VR
R110
1.5KΩ
R111
1.5KΩ
R213
10Ω
(5W)
Q20
D18
D49
(RD12EB3)
R140
5.6KΩ
R198
82Ω
(1W)
+5VB
D43
(RD5.1EB2)
R196
100Ω
(1W)
+6VA
D44
(RD6.2EB2)
C75
4.7μF
(16V)
+12V
R55
470Ω
R56
470Ω
R208
39Ω
(2W)
Q21
+5VC
D19
D50
(RD5.6EB2)
R141
5.6KΩ
C77
4.7μF
(16V)
+5V
RS3
330Ω
VH
L5
10μH
+5VA
C76
4.7μF
(16V)
-12V
R197
100Ω
(1W)
-6VA
C78
4.7μF
(16V)
D45
(RD6.2EB2)
L6
10μH
-5.2VD
D20
C43
0.33μF
(50V)
C79
4.7μF
(16V)
-5.2VA
R193
16.2KΩ
(1%)
R190
3.16KΩ
(1%)
M70
(010-8D) STLV
(011-10F) DMLV
R191
3.16KΩ
(1%)
A358
G3
24VR
R118
1.8KΩ
R154
15KΩ
R179
1KΩ
(1%)
+5V
R185
1.07KΩ
(1%)
M68
A311
H3
R102
1KΩ
R156
47KΩ
C66
1μF
(35V)
R123
2.2KΩ
R157
47KΩ
R103
1KΩ
M67
A311
J3
R20
100Ω
*5VCR (009-4F)
C19
560PF
(50V)
R124
2.2KΩ

012 /12


A-CABLE PIN DISPOSITION
(CNA)
B-CABLE PIN DISPOSITION
(CNB)
POWER CABLE
PIN DISPOSITION
(CNC)
CONTROLLER
CQOM
B16B-7850-0050A
INTERFACE
A-CABLE
INTERFACE
B-CABLE
POWER
CABLE
CNA
CNB
CNC
CNJ1
CNP1
CNP3
CNJ3
CNP2
CNJ2
CNP4
CNJ4
DISK
ENCLOSURE
HDIC
A4111
DATA
HEAD
HD0
HD1
HD2
HD3
HD4
HD5
HD6
HD7
CLOCK
HEAD
THROUGH
CONNECTOR
DC
MOTOR
A, B, C : HALL DEVICE
STEPPER
MOTOR
ZERO
TRACK
DETECTOR
VOLTAGE
REGULATOR
A7905
112/114
CIRCUIT DIAGRAM
001 / 1

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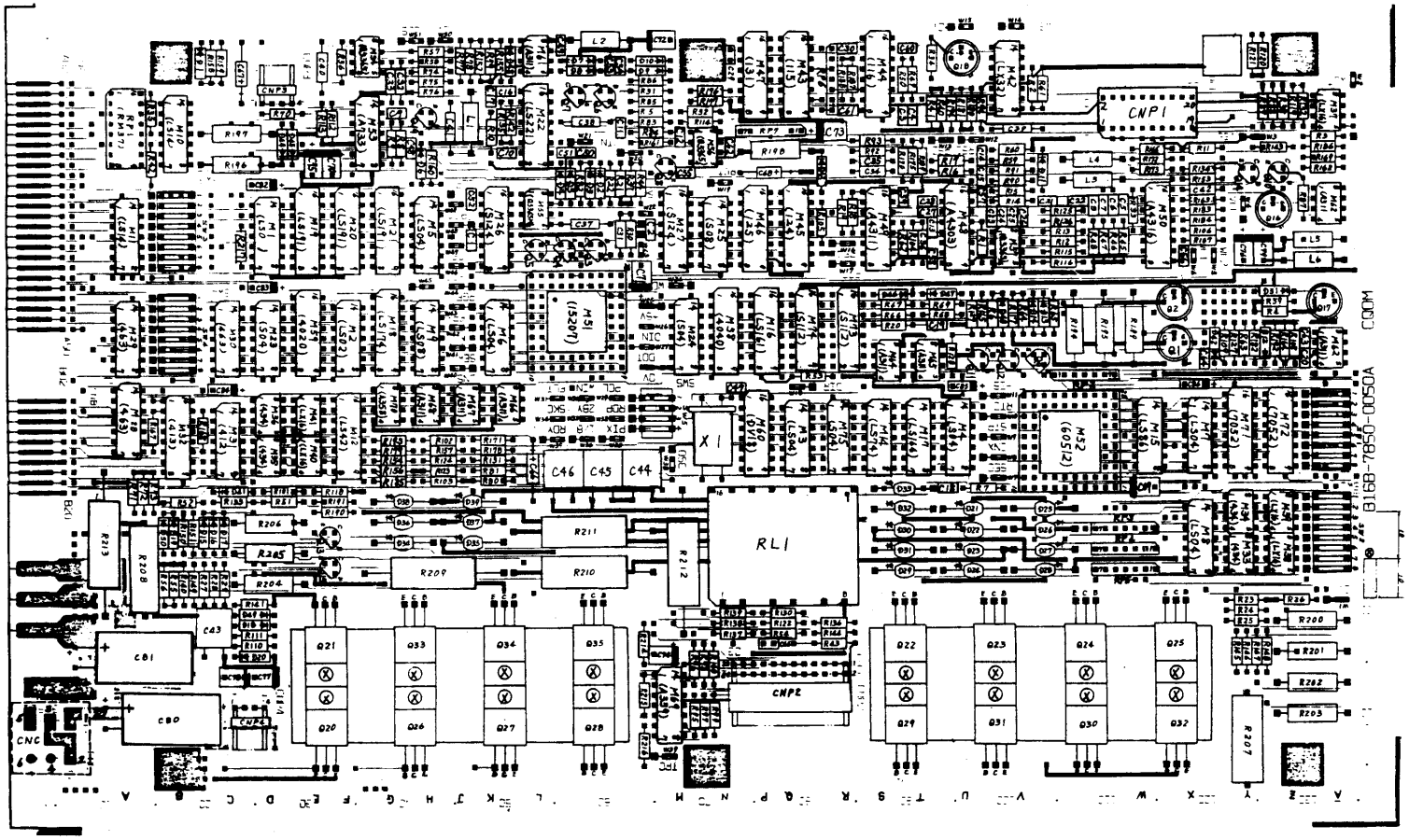

					CONTROLLER O (CQOM) MOUNTING DIAGRAM
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