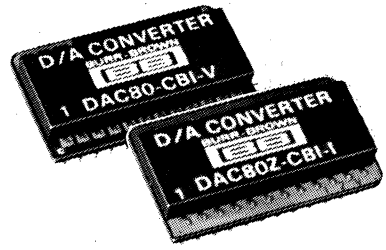
BURR-BROWN®



DAC80

IC DIGITAL-TO-ANALOG CONVERTER

FEATURES

- WIDE POWER SUPPLY RANGE MODELS AVAILABLE (Z MODELS)
- 12-BIT, 3 DIGIT RESOLUTION
- ±½LSB MAXIMUM NONLINEARITY
- COMPLETE WITH INTERNAL REFERENCE AND OUTPUT AMPLIFIER (V MODELS)
- FAST SETTLING - 300nsec to ±.01% (I MODELS)
- CERAMIC DUAL-IN-LINE PACKAGE
- LOW COST

DESCRIPTION

Use this popular 12 bit digital-to-analog converter for low cost precision performance applications.

DAC80, with internal reference and optional output amplifier, offers a maximum nonlinearity error of ±0.012%, ±30ppm/°C maximum gain drift, and monotonicity - all over a 0 to 70°C operating range. In the bipolar configuration, total accuracy drift is guaranteed to be less than ±25ppm/°C. Select TTL compatible complementary 12 bit binary (CBI) or 3 digit BCD (CCD) input codes.

Packaged within DAC80's 24 pin dual-in-line ceramic case are fast settling switches and stable, laser trimmed thin-film resistors that let you select output voltage ranges of ±2.5, ±5, ±10, 0 to +5, 0 to +10 volts (V models) or output current ranges of ±1mA or 0 to -2mA (I models). Voltage output models settle to ±0.01% of FSR in 3 microseconds for a 10 volt step change.

By specifying the new DAC80Z model with a supply range of ±11.4 to ±16.0 volts, you can use this proven D/A converter in microprocessor and semiconductor memory systems.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

© Burr-Brown Research Corporation 1978

PDS-322E

Printed in U.S.A. July, 1978

SPECIFICATIONS

ELECTRICAL

Typical at 25°C and rated power supplies unless otherwise noted.

MODEL	DAC80-CBI			DAC80-CCD			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
DIGITAL INPUT							
Resolution			12				Bits
						3	Digits
Logic Levels (TTL/Compatible)[1]							
Logic "1" (at +40μA)[2]	+2		+5.5	+2		+5.5	VDC
Logic "0" (at -1.0mA)[3]	0		+0.8	0		+0.8	VDC
ACCURACY							
Linearity Error at 25°C		±1/4	±1/2		±1/8	±1/4	LSB
Differential Linearity Error		±1/2	+1, -3/4		±1/4	±1/2	LSB
Gain Error[4]		±0.1	±0.3		±0.1	±0.3	%
Offset Error[4]		±0.05	±0.15		±0.05	±0.15	% of FSR[5]
Monotonicity Temp. Range, min	0		+70	0		+70	°C
DRIFT[6] (0°C to +70°C)							
Total bipolar drift, max (includes gain, offset, and linearity drifts)[7]			±25			±25	ppm of FSR/°C
Total error over 0°C to +70°C[8]							
Unipolar		±0.08	±0.15		±0.08	±0.15	% of FSR
Bipolar		±0.06	±0.12		±0.06	±0.12	% of FSR
Gain		±15	±30		±15	±30	ppm/°C
Exclusive of internal reference			±10			±10	ppm/°C
Unipolar Offset		±1	±3		±1	±3	ppm of FSR/°C
Bipolar Offset		±7	±15		±7	±15	ppm of FSR/°C
Differential Linearity 0°C to +70°C		±1/2	+1, -7/8		±1/2	+1, -7/8	LSB
Linearity Error 0°C to +70°C			±1/2			±1/2	LSB
CONVERSION SPEED/V models							
Settling Time to ±0.01% of FSR For FSR Change							
with 10kΩ Feedback[9]		5			5		μsec
with 5kΩ Feedback		3			3		μsec
For 1 LSB Change		1.5			1.5		μsec
Slew Rate	10	20		10	20		V/μsec
CONVERSION SPEED/I models - of FSR							
Settling Time to ±0.01% For FSR Change							
10 to 100Ω Load		300			300		nsec
1kΩ Load		1			1		μsec
ANALOG OUTPUT/V models							
Ranges[6]	±2.5, ±5, ±10, 0 to +5, 0 to +10				0 to +10		Volts
Output Current	±5			±5			mA
Output Impedance (DC)		0.05			0.05		ohms
Short Circuit Duration	Indefinite to Common						
ANALOG OUTPUT/I models							
Ranges		±1, 0 to -2			0 to -2		mA
Output Impedance - Bipolar		4.4			4.4		kΩ
Output Impedance - Unipolar		15			15		kΩ
Compliance			±2.5			±2.5	Volts
INTERNAL REFERENCE VOLTAGE		+6.3			+6.3		Volts
Maximum External Current[10]			±200			±200	μA
Tempco of Drift, max		±10	±20		±10	±20	ppm/°C
POWER SUPPLY SENSITIVITY							
+15V Supply		±0.02			±0.02		% of FSR/% V_S
-15 and +5V Supplies		±0.002			±0.002		% of FSR/% V_S
POWER SUPPLY REQUIREMENTS							
DAC80	±14, +4.75	±15, +5	±16, +16	±14, +4.75	±15, +5	±16, +16	VDC
DAC80Z[6]	±11.4, +4.75	±12, +5	±16, +16	±11.4, +4.75	±12, +5	±16, +16	VDC
Supply Drain							
±15/±12V (including 5mA load)		±25	±35		±25	±35	mA
+5V (logic supply)		+20	±30		+20	±30	mA
TEMPERATURE RANGE							
Specification	0		+70	0		+70	°C
Operating (double above specs)	-25		+85	-25		+85	°C
Storage	-55		+100	-55		+100	°C

TABLE I. Electrical Specifications

NOTES:

1. Adding external CMOS hex buffers CD 4009A will provide CMOS input compatibility.
2. Logic "1" current = 40μA max at V_{IN} = +5.0V
3. Logic "0" current = -1.6mA max at V_{IN} = +0.4V.
4. Adjustable to zero with external trim potentiometer.
5. FSR means "Full Scale Range" and is 20V for ±10V range, 10V for ±5V range, etc.
6. To maintain drift spec internal feedback resistors must be used for current output models.
7. See discussion on page 6-161.
8. With gain and offset errors adjusted to zero at 25°C. See discussion on page 6-162
9. DAC80Z supply range is ±12.0V min to ±16.0V max for 0 to +10V and ±10V.
10. Maximum with no degradation of specifications.

CONNECTION DIAGRAM

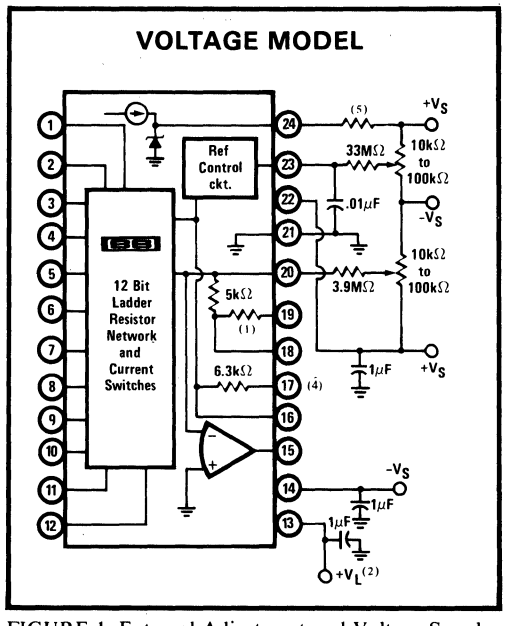


FIGURE 1. External Adjustment and Voltage Supply Connection Diagram, Voltage Model.

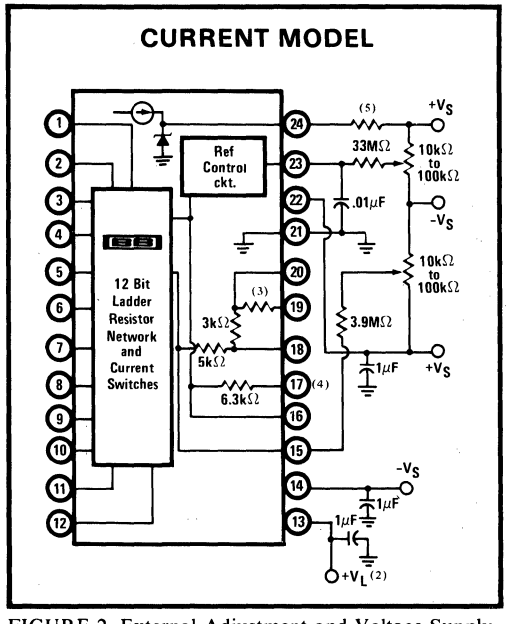


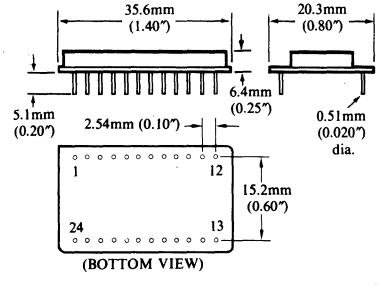
FIGURE 2. External Adjustment and Voltage Supply Connection Diagram, Current Model.

NOTES:
1. 3kΩ for CCD models, 5kΩ for CBI models.
2. If connected to $+V_S$, which is permissible, power dissipation increases 200mW.
3. CBI model, 2kΩ; CCD model,OΩ and pin 20 has no internal connection.
4. 6.3kΩ resistor internally grounded on CCD models.
5. Resistor required only for Z models, see page 6-156. Make no connection to power supply for regular models.

PIN ASSIGNMENTS

I Models	Pin #	V Models
(MSB) Bit 1	1	Bit 1 (MSB)
Bit 2	2	Bit 2
Bit 3	3	Bit 3
Bit 4	4	Bit 4
Bit 5	5	Bit 5
Bit 6	6	Bit 6
Bit 7	7	Bit 7
Bit 8	8	Bit 8
Bit 9	9	Bit 9
Bit 10	10	Bit 10
Bit 11	11	Bit 11
(LSB) Bit 12	12	Bit 12 (LSB)
Logic Supply	13	Logic Supply
$-V_S$	14	$-V_S$
I_{OUT}	15	V_{OUT}
Ref. Input	16	Ref. Input
Bipolar Offset	17	Bipolar Offset
Scaling Network	18	10V Range
Scaling Network	19	20V Range
Scaling Network	20	Summing Junction
Common	21	Common
$+V_S$	22	$+V_S$
Gain Adjust	23	Gain Adjust
6.3V Ref. Out	24	6.3V Ref. Out

MECHANICAL



CASE: Black Ceramic
MATING CONNECTOR: 245MC
PIN: Pin material and plating composition conform to method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2).
WEIGHT: 8.4 grams (0.3 oz.)
HERMETICITY: Conforms to method 1014 Condition C Step 1 (fluorocarbon) of Mil-Std-883 (gross leak).

FIGURE 3. Mechanical Specifications

DISCUSSION

DIGITAL INPUT CODES

The DAC80 accepts complementary digital input codes in either binary (CBI) or decimal (CCD) format. The CBI model may be connected by the user for any one of three complementary codes: CSB, CTC or COB.

	DIGITAL INPUT	ANALOG OUTPUT		
	MSB LSB	CSB Compl. Straight Binary	COB Compl. Offset Binary	CTC* Compl. Two's Compl.
CBI Models	000000000000	+Full Scale	+Full Scale	-LSB
	011111111111	+1/2 Full Scale	Zero	-Full Scale
	100000000000	Mid-scale -1LSB	-1 LSB	+Full Scale
	111111111111	Zero	-Full Scale	Zero
CCD Models	MSB LSB	CCD Complementary Coded Decimal - 3 Digits		
	0110 0110 0110	+Full Scale		
	1111 1111 1111	Zero		

* Invert the MSB of the COB code with an external inverter to obtain CTC code.

TABLE II. Digital Input Codes

ACCURACY

Linearity of a D/A converter is the true measure of its performance. The linearity error of the DAC80 is specified over its entire temperature range. This means that the analog output will not vary by more than ±1/2 LSB, maximum, from an ideal straight line drawn between the end points (inputs all "1"s and all "0"s) over the specified temperature range of 0 to +70°C.

Differential linearity error of a D/A converter is the deviation from an ideal 1 LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1/2 LSB means that the output voltage step sizes can range from 1/2 LSB to 3/2 LSB when the input changes from one adjacent input state to the next.

Monotonicity over a 0 to +70°C range is guaranteed in the DAC80 to insure that the analog output will increase or remain the same for increasing input digital codes.

DRIFT

Gain Drift is a measure of the change in the full scale range output over temperature expressed in parts per million per °C (ppm/°C). Gain drift is established by: 1) testing the end point differences for each DAC80 model at 0°C, +25°C and +70°C; 2) calculating the gain error with respect to the 25°C value and; 3) dividing by the temperature change. This figure is expressed in ppm/°C and is given in the specification table both with and without internal reference.

Offset Drift is a measure of the actual change in output with all "1"s on the input over the specified temperature range. The offset is measured at 0°C, +25°C and +70°C. The maximum change in OFFSET is referenced to the OFFSET at 25°C and is divided by the temperature range. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

SETTLING TIME

Settling time for each DAC80 model is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input.

Voltage Output Models: Three settling times are specified to ±0.01% of full scale range (FSR); two for maximum full scale range changes of 20V, 10V and one for a 1 LSB change. The 1 LSB change is measured at the major carry (0111 ... 11 to 1000 ... 00), the point at which the worst case settling time occurs.

Current Output Models: Two settling times are specified to ±0.01% of FSR. Each is given for current models connected with two different resistive loads: 10 to 100 ohms and 1000 to 1875 ohms. Internal resistors are provided for connecting nominal load resistances of approximately 1000 to 1800 ohms for output voltage range of ±1V and 0 to -2V. See Table V.

COMPLIANCE

Compliance voltage is the maximum voltage swing allowed on the current output node in order to maintain specified accuracy. The maximum compliance voltage of all current output models is ±2.5V. Maximum safe voltage swing permitted without damage to the DAC80 is ±5V.

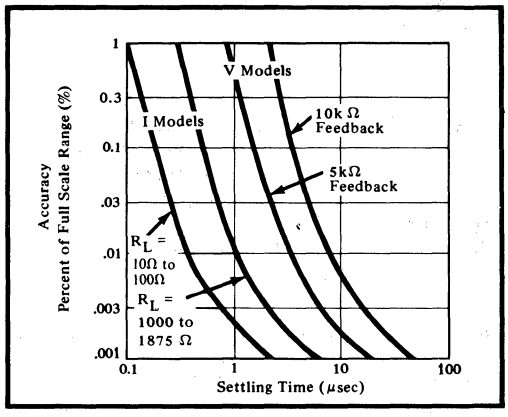


FIGURE 4. Full Scale Range Settling Time vs Accuracy

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a per cent of FSR per per cent of change in either the positive, negative, or logic supplies about the nominal power supply voltages. See Figure 5.

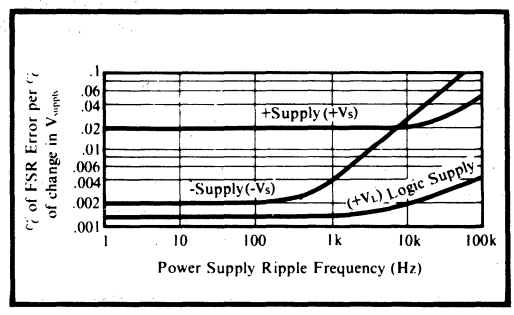


FIGURE 5. Power Supply Rejection vs Power Supply Ripple

REFERENCE SUPPLY

All DAC80 models are supplied with an internal 6.3 volt reference voltage supply. This voltage (pin 24) has a tolerance of ±5% and must be connected to the Reference Input (pin 16) for specified operation. This reference may be used externally also, but external current drain is limited to 200μA. An external buffer amplifier is recommended if this reference will be used to drive other system components.

OPERATING INSTRUCTIONS

±12 VOLT SUPPLY OPERATION

The Z models will operate with supply voltages as low as ±11.4V. For operation with supplies less than ±14V an external resistor must be connected between the positive supply and pin 24. This provides additional current required by the internal reference. The required resistor value for supply voltages of ±11.4 to ±12.6V is 2.0kΩ and for supplies of ±12.6 to ±14V is 3.9kΩ.

It is recommended that output voltage ranges -10 to +10V and 0 to +10V not be used with the Z model if the supply voltages are ever less than the recommended ±12V. The output amplifier may saturate if $|V_{supply}| - |V_{out}\ max| <$ 2.0V. This applies to units with both CBI and CCD input codes. Except for operation at lower supply voltages, the DAC80Z and DAC80 operation is identical.

POWER SUPPLY CONNECTIONS

Decoupling: For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the connection diagrams, Figures 1 and 2. These capacitors (1μF tantalum or electrolytic recommended) should be located close to the DAC80. Electrolytic capacitors, if used, should be paralleled with 0.01μF ceramic capacitors for best high frequency performance.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and gain may be trimmed by installing external OFFSET and GAIN potentiometers. If gain and offset adjust circuits are not used, pins 15, 20 and 23 should be connected as described in other sections herein. (Do not ground.) Connect the potentiometers as shown in Figure 1 and Figure 2 and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 33MΩ resistors (20% carbon or better) should be located close to the DAC80 to prevent noise pick-up. If it is not convenient to use these high-value resistors, an equivalent "T" network, as shown in Figure 6, may be substituted in each case. The gain adjust (pin 23) is a high impedance point and a .001μF to .01μF ceramic capacitor should be connected from this pin to common to prevent noise pick-up. Refer to Figure 7 and 8 for relationship of OFFSET and GAIN adjustments to unipolar and bipolar D/A converters.

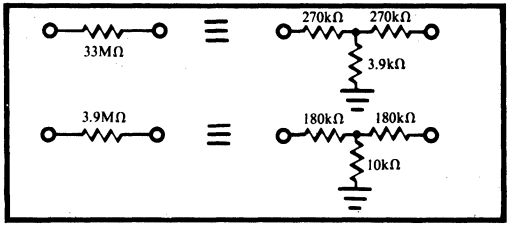


FIGURE 6. Equivalent Resistances.

Offset Adjustment: For unipolar (CSB, CCD) configurations, apply the digital input code that should produce zero potential output and adjust the OFFSET potentiometer for zero output.

For bipolar (COB, CTC) configurations, apply the digital input code that should produce the maximum negative output voltage. Example: If the FULL SCALE RANGE is connected for 20 volts, the maximum negative output voltage is -10V. See Table III for corresponding codes and the block diagram on page 6-154 for offset adjustment connections.

Gain Adjustment: for either unipolar or bipolar configurations, apply the digital input that should give the maximum positive voltage output. Adjust the GAIN potentiometer for this positive full scale voltage. See Table III for positive full scale voltages and the block diagrams for gain adjustment connections.

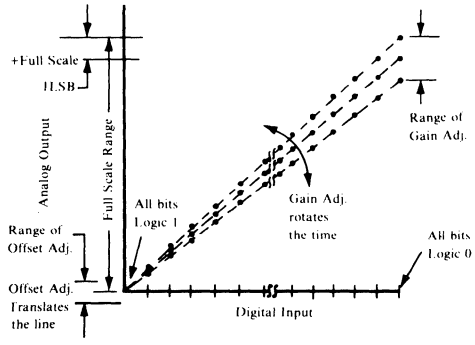


FIGURE 7. Relationship of OFFSET and GAIN Adjustments for a UNIPOLAR D/A Converter.

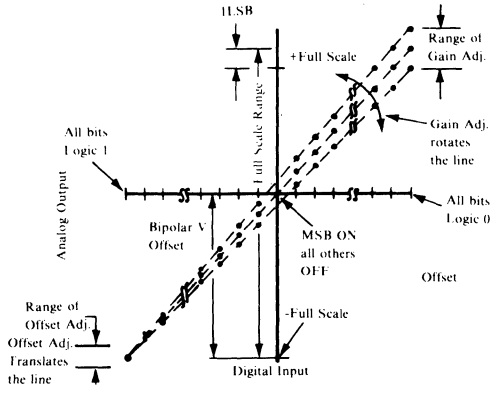


FIGURE 8. Relationship of OFFSET and GAIN Adjustments for a BIPOLAR D/A Converter

	DIGITAL INPUT	ANALOG OUTPUT			
		VOLTAGE*		CURRENT	
		0 to +10V	±10V	0 to -2mA	±1mA
CBI Models	12 Bit Resolution MSB LSB				
	000000000000	+9.9976V	+9.9951V	-1.9995mA	-0.9995mA
	011111111111	+5.0000V	0.0000V	-1.0000mA	0.0000mA
	100000000000	+4.9976V	-0.0049V	-0.9995mA	+0.0005mA
	111111111111	0.0000V	-10.0000V	0.0000mA	+1.000mA
	One LSB	2.44mV	4.88mV	0.488μA	0.488μA
CCD Models	3 Digital Resolution MSB LSB				
	0110 0110 0110	+9.990V**	N/A	-1.249mA	N/A
	0110 0110 1111	+9.900V	N/A	-1.238mA	N/A
	0110 1111 1111	+9.000V	N/A	-1.125mA	N/A
	1111 1111 1111	0.000V	N/A	0.000mA	N/A
	One LSB	10.00mV	N/A	1.25μA	N/A

** Normal full scale range with correct codes; output can go higher if illegal codes are applied.
* To obtain values for other binary (CBI) ranges: 0 to +5V range: divide 0 to +10V range values by 2.
±5V range: divide ±10V range values by 2.
±2.5V range: divide ±10V range values by 4.

TABLE III. Digital Input/Analog Output

VOLTAGE OUTPUT MODELS

OUTPUT RANGE CONNECTIONS

Internal scaling resistors provided in the DAC80 may be connected to produce bipolar output voltage ranges of ±10*, ±5 or ±2.5V or unipolar output voltage ranges of 0 to +5 or 0 to +10V.* See Figure 9.

*Refer to ±12V supply operation discussion, page 6-156.

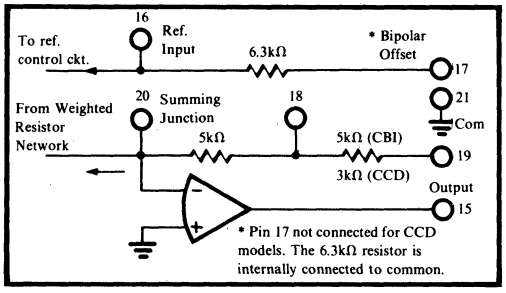


FIGURE 9. Output Amplifier Voltage Range Scaling Circuit.

Gain and offset drift are minimized in the DAC80 because of the thermal tracking of the scaling resistors with other device components. Connections for various output voltage ranges are shown in Table IV. Settling time is specified for a full scale range change: 5 microseconds for 8kΩ or 10kΩ feedback resistors; 3 microseconds for a 5kΩ feedback resistor.

Output Range	Digital Input Codes	Connect Pin 15 to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10	COB or CTC	19	20	15	24
±5	COB or CTC	18	20	N.C.	24
±2.5V	COB or CTC	18	20	20	24
0 to +10V	CSB	18	21	N.C.	24
0 to +5V	CSB	18	21	20	24
0 to +10V	CCD	19	N.C.	15	24

TABLE IV. Output Voltage Range Connections - Voltage Model DAC80.

CURRENT OUTPUT MODELS

The equivalent output circuit and resistive scaling network of the current model differ from the voltage model and are shown in Figures 10 and 11. Instructions for using the DAC80-XXX-I with a resistor or an external op amp follow. External R_{LS} or R_{LP} resistors are required to produce exactly 0 to -2V or ±1V output. TCR of these resistors should be ±100 ppm/°C or less to maintain the DAC80 output specifications. If exact output ranges are not required, the external resistors are not needed.

Internal resistors are provided to scale an external op amp or to configure a resistive load to offer two output voltage ranges of ±1V or 0 to -2V. These resistors (R_{LI}) are an integral part of the DAC80 and maintain gain and bipolar offset drift specifications. If the internal resistors are not used, external R_L (or R_F) resistors should have a TCR of ±25 ppm/°C or less to minimize drift. This will typically add ±50 ppm/°C + the TCR of R_L (or R_F) to the total drift.

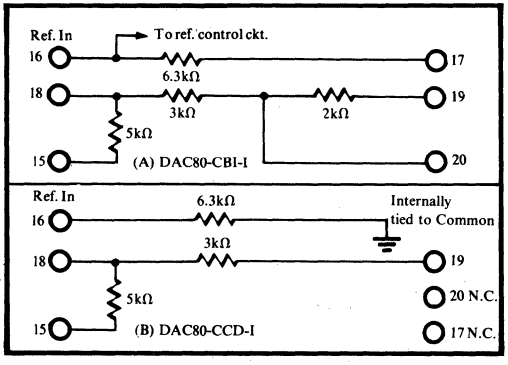


FIGURE 10. Internal Scaling Resistors

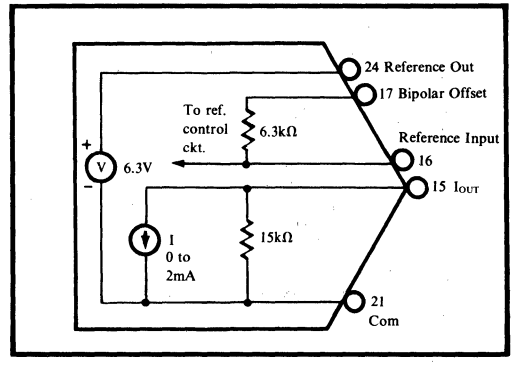


FIGURE 11. DAC80 Current Model Equivalent Output Circuit.

Digital Input Codes	Output Range	Internal Resistance R_{LI}	1% Metal Film External Resistance R_{LS}	R_{LP}	R_{LI} Connections Connect Pin 15 to	Connect Pin 18 to	Connect Pin 20 to	Reference Connect Pin 16 to	Bipolar Offset Connect Pin 17 to	R_{LS}	R_{LP}
CSB	0 to -2V	0.968kΩ	105Ω	N/A	20	19 & R_{LS}	15	24	Com (21)	Between Pin 18 & Com (21)	N/A
CCD	0 to -2V	1.875kΩ	N/A	36.5kΩ	19	Com (21)	N.C.	24	N.C.	N/A	Between Pin 15 & 21
COB or CTC	±1V	1.2kΩ	90.9Ω	N/A	18	19	R_{LS}	24	15	Between Pin 20 & Com (21)	N/A

TABLE V. DAC80-XXX-I Resistive Load Connections.

DRIVING A RESISTIVE LOAD UNIPOLAR

A load resistance, $R_L = R_{LI} + R_{LS}$, connected as shown in Figure 12 will generate a voltage range, V_{OUT}, determined by:

$$V_{OUT} = -2mA \left(\frac{15k \times R_L}{15k + R_L}\right)$$

Where R_L max = 1.36kΩ
and V_{OUT} max = -2.5V

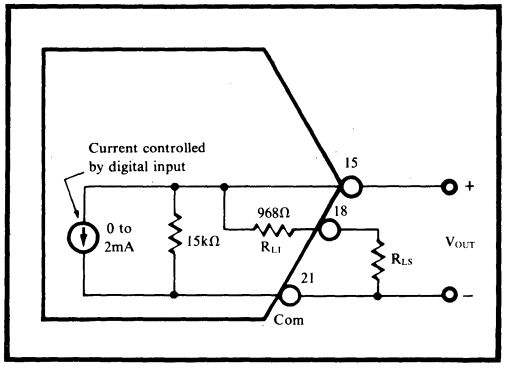


FIGURE 12. Equivalent Circuit DAC80-CBI-I connected for Unipolar Voltage Output with Resistive Load.

To achieve specified drift, connect the internal scaling resistor (R_{LI}) as shown in Table V to an external metal film trim resistor (R_{LS}) to provide full scale output voltage range of 0 to -2V. With $R_{LS} = 0$, $V_{OUT} = -1.82V$.

CCD Input Code: Connect the internal scaling resistors as shown in Table V and add an external metal film resistor (R_{LP}) in parallel as shown in Figure 13 to obtain a 0 to -2 volt full scale output voltage range for CCD input codes.

$$\text{With } R_L = \frac{R_{LI} \times R_{LP}}{R_{LI} + R_{LP}},$$

$$V_{OUT} = -1.25mA \left(\frac{15.6k \times R_L}{15.6k + R_L}\right)$$

If $R_{LP} = \infty$, $V_{OUT} = -2.08V$

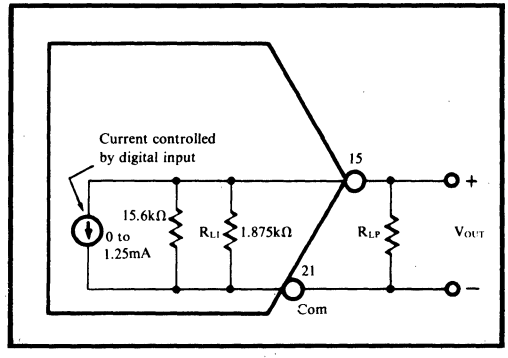


FIGURE 13. DAC80-CCD-I Connected for Voltage Output with Resistive Load

DRIVING A RESISTOR LOAD BIPOLAR

The equivalent output circuit for a bipolar output voltage range is shown in Figure 14, $R_L = R_{LI} + R_{LS}$. V_{OUT} is determined by:

$$V_{OUT} = \pm 1mA \left(\frac{R_L \times 4.44k}{R_L + 4.44k}\right)$$

Where R_L max = 5.72kΩ
V_{OUT} max = ±2.5V

To achieve specified drift, connect the internal scaling resistors (R_{LI}) as shown in Table V for the COB or CTC codes and add an external metal film resistor (R_{LS}) in series to obtain a full scale output range of ±1V.

With $R_{LS} = 0$, $V_{OUT} = \pm 0.944V$.

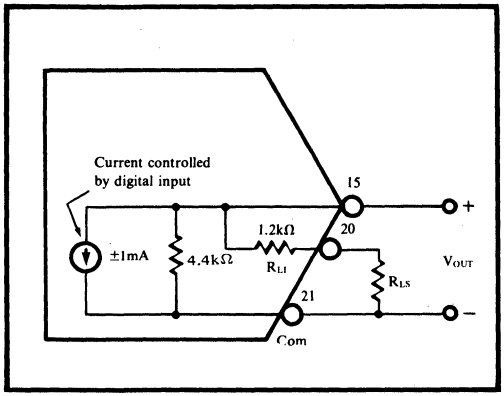


FIGURE 14. DAC80-CBI-I Connected for Bipolar Output Voltage with Resistive Load.

DRIVING AN EXTERNAL OP AMP

The current model DAC80 will drive the summing junction of an op amp used as a current to voltage converter to produce an output voltage. See Figure 15.

$$V_{OUT} = I_{OUT} \times R_F$$

where I_{OUT} is the DAC80 output current and R_F is the feedback resistor. Using the internal feedback resistors of the current model DAC80 provides output voltage ranges the same as the voltage model DAC80. To obtain the desired output voltage range when connecting an external op amp, refer to Table VI.

Output Range	Digital Input Codes	Connect Ⓐ to	Connect Pin 17 to	Connect Pin 19 to	Conect Pin 16 to
±10V	COB or CTC	19	15	Ⓐ	24
±5V	COB or CTC	18	15	N.C.	24
±2.5V	COB or CTC	18	15	15	24
0 to +10V	CSB	18	21	N.C.	24
0 to +5V	CSB	18	21	15	24
0 to +10V	CCD	19	N.C.	Ⓐ	24

TABLE VI. Voltage Range of Current Output DAC80.

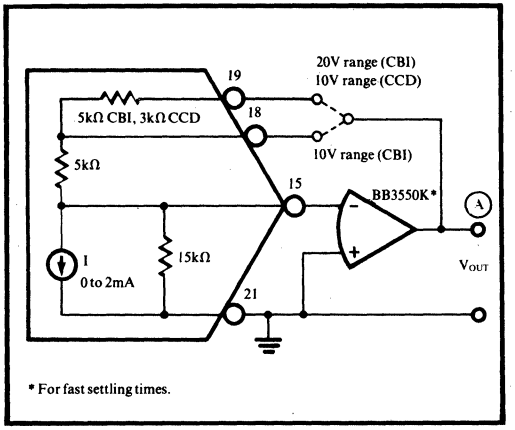


FIGURE 15. External Op Amp - Using Internal Feedback Resistors.

OUTPUT LARGER THAN 20V RANGE

For output voltage ranges larger than ±10 volts, a high voltage op amp may be employed with an external feedback resistor. Use I_{OUT} values of ±1mA for bipolar voltage ranges and -2mA for unipolar voltage ranges. See Figure 16. Use protection diodes when a high voltage op amp is used.

The feedback resistor, R_F, should have a temperature coefficient as low as possible. Using an external feedback resistor, overall drift of the circuit increases due to the lack of temperature tracking between R_F and the internal scaling resistor network. This will typically add 50 ppm/°C + R_F drift to total drift.

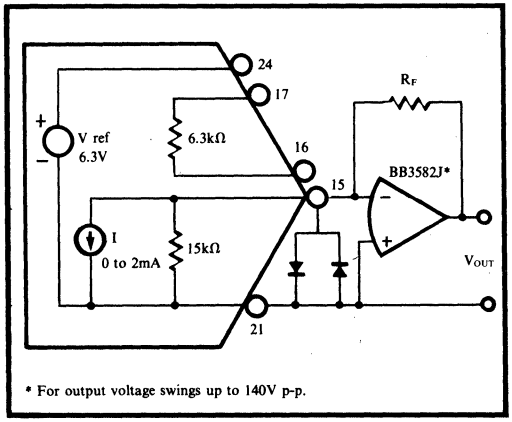


FIGURE 16. External Op Amp - Using External Feedback Resistors.

COMPUTING TOTAL ACCURACY OVER TEMPERATURE

The accuracy drift with temperature of a DAC80 consists of three primary components: Gain drift, unipolar or bipolar offset drift, and linearity drift. To obtain the worst case accuracy drift, most users would assume that all drift errors are random and would simply add them algebraically. However, the worst case accuracy drift for a DAC80 operating in the bipolar mode is about one-half of the algebraic sum of the individual drift errors.

To explain this fact, it is necessary to consider the unipolar and bipolar modes of operation separately. Note that the linearity drift of both modes is negligible. (Total linearity error is less than ±1/2 LSB over 0°C to +70°C.)

In the unipolar mode of operation, offset drift (±1 ppm/°C) is due primarily to voltage offset drift of the output op amp and, to a lesser extent, to the leakage current through the quad current switches. Gain drift consists of several components: 1) ±10 ppm/°C due to ratio drift of current weighting resistors to the reference resistor and current switch V_{BE} to the reference transistor (refer to Model 4550 data sheet); and 2) ±20 ppm/°C due to the zener reference. The sum of these two components, ±30 ppm/°C, is the maximum gain drift.

Because the parameters described could all drift in the same direction, the worst case accuracy drift in the unipolar mode is simply the sum of the components, or ±31 ppm/°C.

In the bipolar mode the major portion (67%) of gain drift is due to the zener reference. The gain and offset drifts caused by reference drift are always in opposite directions. Therefore, the accuracy drift will be the difference rather than the sum of these drifts.

First, consider the effect of reference variations on offset drift. Figure 17 shows a simplified circuit diagram of a DAC80 operating in the bipolar mode with all bits off. The current switch leakage current is negligible, so

$$V_{-FULL\ SCALE} = -\frac{RF}{R_{BPO}} \cdot V_{REF}$$

$$= -\frac{10k}{6.3k} \cdot 6.3V = -10 \text{ volts}$$

This equation shows that if V_{REF} increases, the output voltage will decrease and vice versa. If the V_{REF} drift is

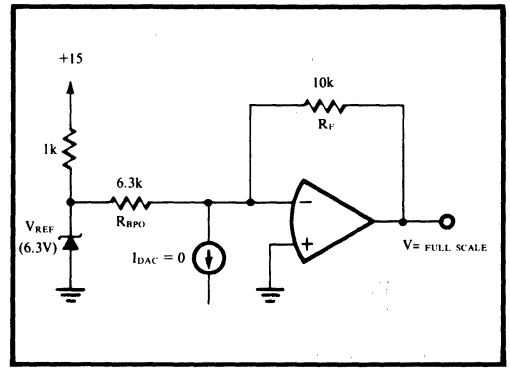


FIGURE 17. Simplified Diagram of DAC80 with "All Bits Off" Operating in Bipolar ±10V Range.

+20 ppm/°C, this is equivalent to (+20 ppm/°C) x (+6.3V) = +126μV/°C. This will result in a voltage drift at the amplifier output of

$$\frac{\Delta V_{-FS}}{\Delta T} = -\frac{R_F}{R_{BPO}} \cdot \frac{\Delta V_{REF}}{\Delta T}$$

$$= -\frac{10k}{6.3k} \cdot 126\mu V/^{o}C = -200\mu V/^{o}C.$$

Since the DAC80 is operating in the ±10V range this is equivalent to (-200μV/°C) ÷ (20V range) = -10 ppm of FSR/°C.

Now consider the effect of reference changes on gain drift. When all of the bits are turned on it can be shown that:

$$\frac{\Delta V_{+FULL\ SCALE}}{\Delta T} = +\frac{R_F}{R_{BPO}} \cdot \frac{V_{REF}}{\Delta T}$$

$$= +\frac{10k}{6.3k} \cdot 126\mu V/^{o}C = +200\mu V/^{o}C$$

$$\text{and } \frac{+200\mu V/^{o}C}{20V \text{ Range}} = +10 \text{ppm}/^{o}C \text{ of FSR.}$$

This result indicates that the drift of the minus full scale voltage will be equal in magnitude to, and in the opposite direction of, the drift of the plus full scale voltage and that

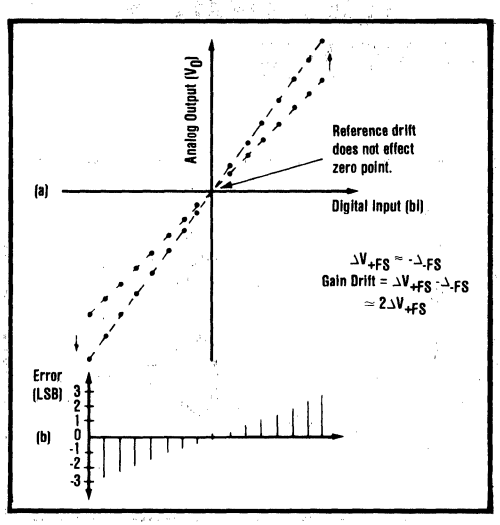


FIGURE 18. (a) Effect of a Positive Reference Drift on the Ideal D/A Transfer Function; (b) Error Distribution Due to Reference Voltage Drift in a DAC80.

zener reference variations have virtually no effect on the zero point. (See Figure 18) This equation also indicates that the gain drift is equal to the V_{REF} drift in ppm/°C, and the magnitude of the minus full scale drift and plus full scale drift is equal to one-half of the V_{REF} drift.

Using this relationship, the worst case accuracy drift for a bipolar DAC80 can be computed. The maximum TCR of the zener reference is ±20ppm/°C. The gain drift due to the reference then is also ±20ppm/°C. The full scale drift and bipolar offset drift are each half that amount or ±10ppm/°C. The maximum gain and offset drifts of the DAC80, exclusive of the reference, are ±10 and ±5ppm/°C respectively. Adding this to the full scale drift due to the reference gives a worst case total accuracy drift of ±25ppm/°C. (Random drifts, which these are, can be in the same direction, so they add directly.) This is much less that the total drift obtained by simply adding the maximum gain and bipolar offset drifts (±45ppm/°C). The maximum zero point drift is equal to one-half of the gain drift exclusive of the reference plus the offset drift exclusive of the reference, or ±10ppm of FSR/°C.

The DAC80 is specified over a 0°C to +70°C temperature range giving a maximum excursion from room temperature (+25°C) of 45°C. Assuming that gain and offset errors have been adjusted to zero at room temperature,

total worst case accuracy error
= Linearity error + Accuracy drift x ΔT
= ±0.01% + ±25ppm/°C (45°C) (100)
= ±0.12%;

total worst case bipolar zero point error
= Bipolar zero drift x ΔT
= ±10ppm of FSR% (45°C) (100)
= ±0.045%

ORDERING INFORMATION

DAC80	X	–	XXX	–	X
Low Cost 12 Bit D/A Converter Family Example: DAC80-CBI-V Binary DAC80 with voltage output	Z = Wide Supply Range Blank = Standard		INPUT CODE CBI = Complementary 12 bit binary CCD = Complementary 3 digit BCD		OUTPUT V = Voltage I = Current