Basic Four® Model 2460 Fixed Media Disc Drive Service Manual

BFISD 8052

Basic Four Information Systems®

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Basic Four Information Systems Division/Management Assistance Inc.
14101 Myford Road, Tustin, California 92680/(714) 731-5100

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CHAPTER 1

INTRODUCTION

1.1 GENERAL DESCRIPTION (FIGURE 1-1)

The Model 2460 Fixed Media Disc Drive, hereafter referred to as the Disc Drive, is a fixed media, mass memory device used for data storage with a maximum memory capacity of 66 Megabytes. The Disc Drive contains a single linear voice coil head positioner with three data read/write heads and one servo read only head. It has a spindle assembly with a single 14 inch disc and brushless dc drive motor. It contains the necessary circuitry for positioning the heads and transferring data and status information via the Controller to a host CPU. This manual contains physical and functional descriptions, installation/ operation procedures, spare parts lists, and maintenance procedures.

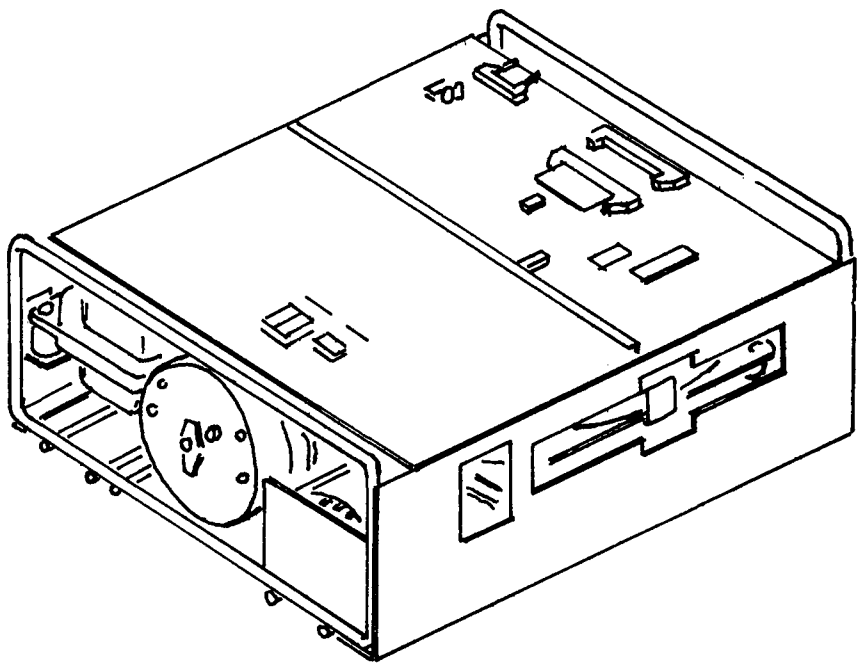


Figure 1-1. Model 2460 Fixed Media Disc Drive

1.2 PHYSICAL DESCRIPTION

The Disc Drive stores data on both sides of a single disc using two moving heads per surface. A full head area is dedicated to servo information for track following, seeking, and timing. A microprocessor controls positioning during track seeks, provides interface control and monitors disc drive operation. The major assemblies of the Disc Drive are: Head Disc Assembly (HDA), Main Logic Printed Circuit Board (PCB), Motor Control PCB, Photocell PCB, Frame Assembly, Power Supply Assembly, and Terminator.

1.2.1 HEAD DISC ASSEMBLY

The Head Disc Assembly is a contamination-resistant enclosure which contains the disc, spindle assembly, voice coil actuator, head carriage, read/write heads, and filter assemblies.

1.2.2 MAIN LOGIC PCB

The Main Logic PCB contains all the circuitry associated with read/write data transfers, interface transfers, head positioning and control.

1.2.3 MOTOR CONTROL PCB

The Motor Control PCB contains all the circuitry associated with driving the spindle motor. This circuitry receives On/Off command from the Main Logic PCB and spindle rotational feedback from the Photocell PCB.

1.2.4 PHOTOCELL PCB

The Photocell PCB contains three infrared light-emitting diodes and phototransistors used to monitor and control spindle motor rotation.

1.2.5 FRAME ASSEMBLY

The Frame Assembly is designed to contain the standard assemblies of the Disc Drive.

1.2.6 POWER SUPPLY ASSEMBLY

The Power Supply Assembly is an integrated power supply that will operate from 50 or 60 Hertz, and at a selectable input voltage of 100, 120, 220, or 240 volts ac.

1.2.7 TERMINATOR

The Terminator is a signal line terminator for the last drive connected to a Controller.

1.3 DISC DRIVE SPECIFICATIONS

Table 1-1 list the Disc Drive specifications.

WARNING

This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, may cause interference to radio communications, as temporarily permitted by regulation. It has not been tested for compliance with the limits for Class A Computing Devices pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference. Operation of this equipment in a residential area is likely to cause interference, in which case the User at his own expense will be required to take whatever measures may be required to correct the interference.

TABLE 1-1. SPECIFICATIONS

Parameters	Characteristics
PHYSICAL	
Height	6.8 inches (17.3 cm)
Width	16.6 inches (42.2 cm)
Depth	20.0 inches (50.8 cm)
Weight	47 pounds (21.3 kg)
POWER	
Ac Power	100 VAC, 120 VAC, 220 VAC or 240 VAC; 50 or 60 Hz, 425 Watts Max.
Dc Power	+24 VDC ± 5%, 7A -5 VDC ± 5%, 2A +5 VDC ± 5%, 4A +24 VDC Return -12 VDC ± 5%, 0.7A

TABLE 1-1. SPECIFICATIONS (continued)

Parameters	Characteristics
ENVIRONMENTAL	
Temperature	65°F to 75°F (18°C to 24°C)
Humidity	40% to 60% non-condensing
GENERAL	
Capacity (formatted)	66 Megabytes
Number of discs	1
Number of data heads	3
Number of data cylinders	1116 (0-1115) (excluding diagnostic)
Number of Diagnostic cylinders	5 (2-6 with Switch 10N-5 ON) (1118-1122)
Bytes per cylinders	60,480
Bytes per track	20,160
Track density	960 Tracks per inch (double density)
Recording density	6,430 Bits per inch
Data transfer rate	1.04 Megabytes per second
Recording code	MFM
Interface code	NRZ
Rotational speed	3,100 RPM
Rotational latency (average)	9.7 milliseconds
Rotational latency (maximum)	21.5 milliseconds
Positioning speed	Maximum (Milliseconds) / Typical (Milliseconds)
Single cylinder	10 / 8
Average	48 / 45
Maximum	90 / 85
Start Time	30 seconds
Stop Time	60 seconds

CHAPTER 2

INSTALLATION AND OPERATION

2.1 GENERAL

This chapter contains complete installation and operation instructions for the Disc Drive.

2.2 UNPACKING/PACKING PROCEDURE

The Disc Drive is normally shipped as part of a data processing system, and unpacking/packing instructions are included in the appropriate system manual. When the Disc Drive is shipped as a replacement unit, the following procedures should be followed.

1. Visually inspect the container for damage. Report any damage immediately.

2. Remove Disc Drive from container and place on work surface.

3. Visually inspect for loose, bent, or broken parts. Report any damage immediately.

4. The head carriage and spindle locks (refer to paragraphs 2.2.1 and 2.2.2) are in the locked position for shipment. If received in the unlocked position, DO NOT INSTALL THIS DISC DRIVE.

5. When shipping a Disc Drive back to the factory, ensure that the spindle lock and head carriage lock are properly installed (locked) and the Disc Drive is packed to prevent damage in shipment.

2.2.1 HEAD CARRIAGE LOCK

Power not being applied to the unit, place the Disc Drive in a flat position with the Main Logic PCB facing up. The head carriage lock is located at one end of the unit (indicated by arrow on the mechanism).

CAUTION

Avoid manual rotation of the spindle or movement of the carriage. Damage to the disc surface may occur.

Pull up on the head carriage lock until free from its locked position. Rotate the head carriage lock to the unlock position as shown in Figure 2-1. The head carriage lock must be placed back in its locked position when the Disc Drive is moved.

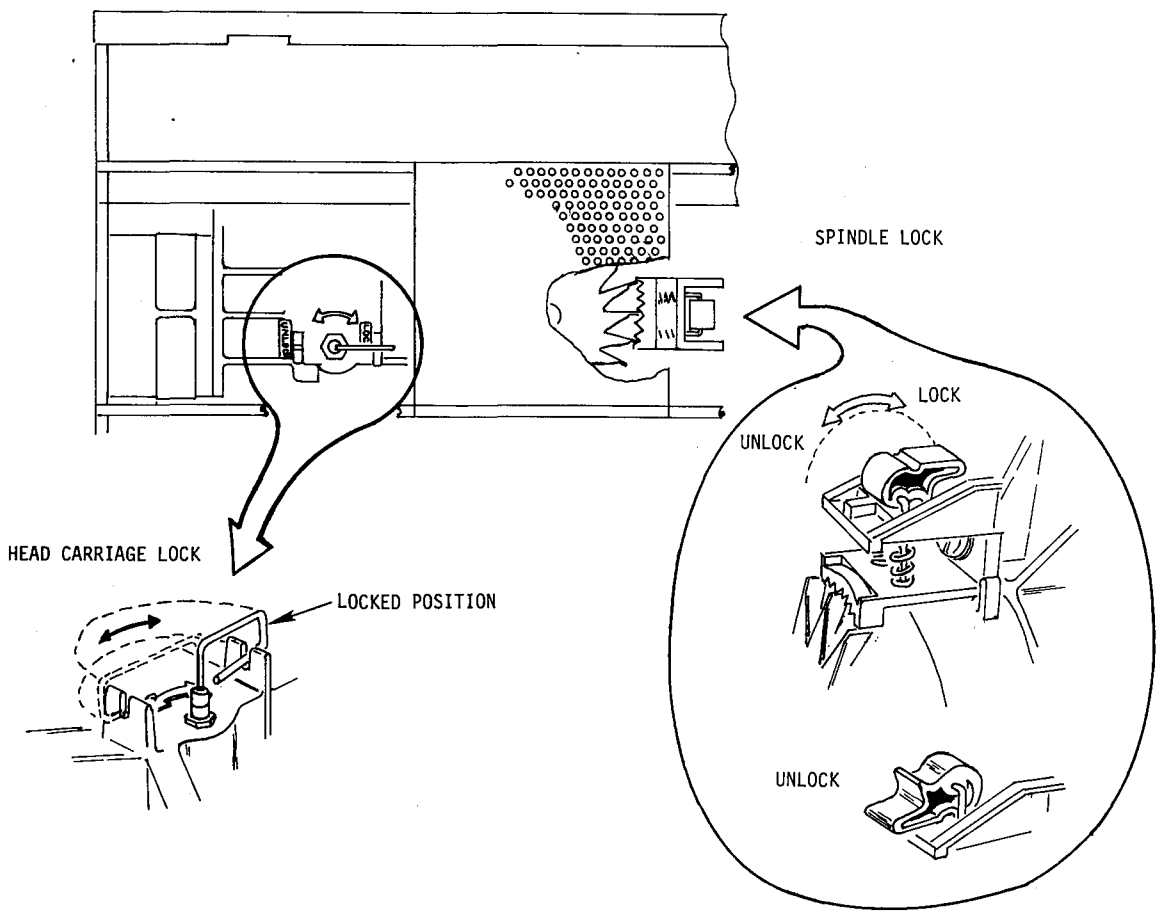


Figure 2-1. Spindle and Head Carriage Lock

2.2.2 SPINDLE LOCK

Power not being applied to the unit and the Disc Drive still in the flat position, locate the spindle lock near the center of the unit (opposite the voice coil motor) as shown in Figure 2-1.

WARNING

Ensure power has not been applied to the unit when the spindle lock is placed in its unlocked position. The Spindle motor must not be manually rotated when unlocked. At this time the fan is free to move and can present a hazard to the Service Representative.

Place the spindle lock lever in the unlocked position (refer to Figure 2-1). The spindle lock must be placed back in its locked position when the Disc Drive is moved.

2.3 INSTALLATION PROCEDURE

The following procedures detail the necessary steps to be followed when installing a replacement Disc Drive.

1. Verify the power switch is OFF, and the ac line cord is not connected.

2. Check that the ac line includes a third-wire earth ground that meets or exceeds the requirements of the National Electrical Code. This can be checked by the following procedures:

   a. Locate the circuit breaker that is to supply power to the host system. With a digital volt meter set to measure 20 volts ac, and the circuit breaker turned on, measure the drop between the green and white wires at the power source for the system (wall outlet). The measured voltage must be less than 1.8 volts ac.

   b. Switch the source circuit breaker off. Measure the resistance between the green and white wires at the wall outlet. The resistance must be less than the value shown below for the applicable circuit breaker rating.

CB Rating	Resistance
15 amperes	0.30 ohms
20 amperes	0.25 ohms
30 amperes	0.15 ohms

   If either measurement in steps a or b above is not less than the value given, request the customer to provide a power source that meets these requirements.

3. Remove cabinet covers to gain access to the Disc Drive.

4. Disconnect and tag all cables from the Main Logic PCB connectors: J2 (bus) and J9 (radial).

5. Disconnect power supply plug at rear of cabinet.

6. Lock Spindle and Head Carriage locks.

7. Remove the four screws holding drive to host CPU cabinet.

8. Remove the Disc Drive from the cabinet.

9. Make pre-power checks (refer to paragraph 2.3.1).

10. Replace Disc Drive in cabinet.

11. Unlock Spindle and Head Carriage locks.

12. Reconnect all tagged cables.

13. Reconnect power supply plug at rear of cabinet.

14. Replace covers.

15. Plug ac line into power source.

2.3.1 PRE-POWER CHECKS

Verify that the input primary power voltage and the Disc Drive power supply are configured in the same range.

1. The following ac voltage ranges are available in the Disc Drive: 100, 120, 220, and 240 volts ac.

2. To select the correct voltage range to match the ac input voltage, locate the Voltage Selection PCB at the rear of the power supply mounted on drive frame (Figure 2-2).

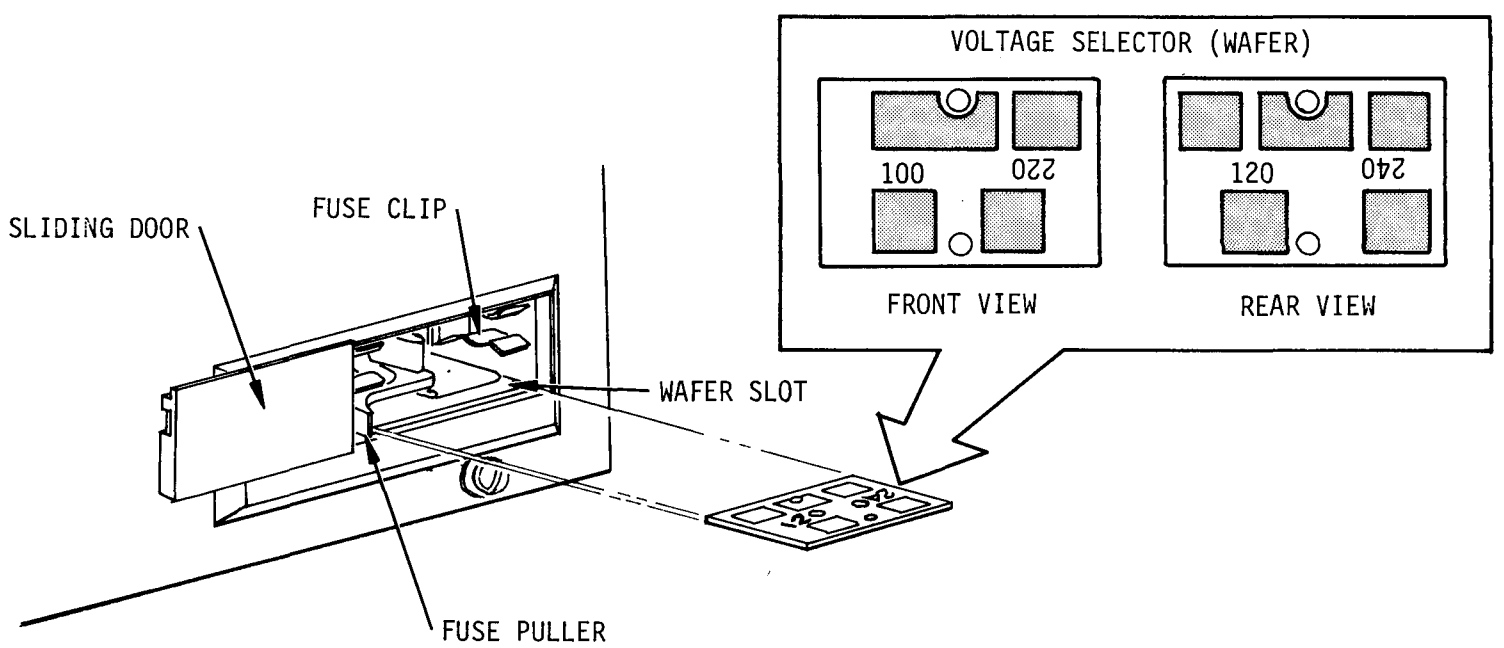


Figure 2-2. Disc Drive Voltage Selection

a. Voltage is selected by the position of this small PCB. The fuse pull lever, situated above the PCB is pushed to the left to remove the fuse.

b. With the fuse removed the selected voltage is read directly from the PCB. If a change in voltage is required, extract the PCB and reinsert it so that it is properly positioned for the required ac voltage designation (100, 120, 220, 240).

c. Check the fuse value. A four amp fuse is used with 100 and 120 volts ac, a two amp fuse is used with 220 and 240 volts ac.

d. Place the fuse pull lever in the extreme right hand position and insert the correct value fuse into the fuse holder.

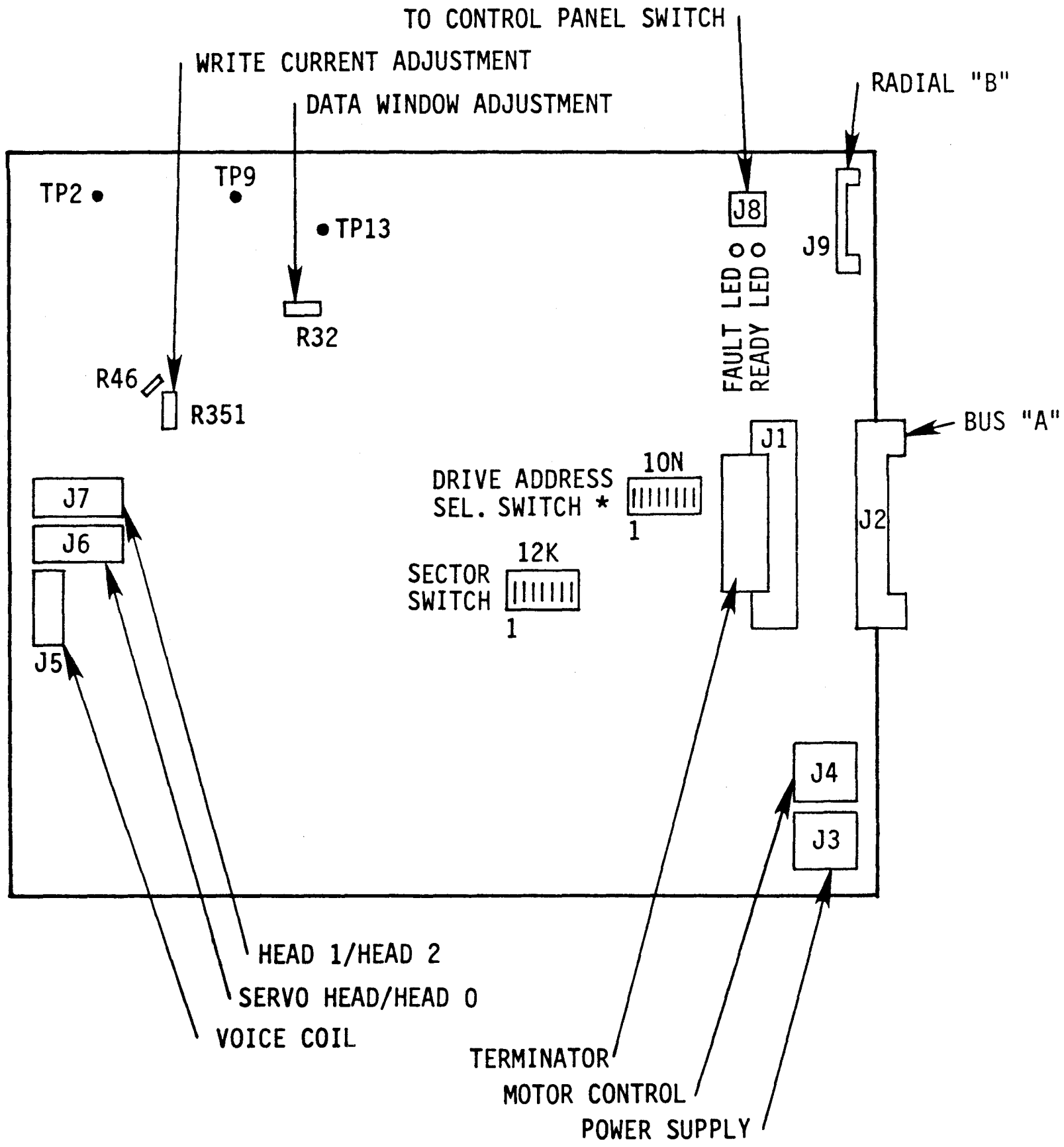
e. No power supply modification is required for changing from 60 cycle to 50 cycle sources.

3. Locate the Main Logic PCB (Figure 2-3) and verify that connectors, switch settings and jumpers are in their correct position. The connectors are listed as follows (for Switch Settings and Jumpers refer to paragraph 2.5):

Connector	Description
J1	Terminator connector, or daisy chain cable connector from/to another Disc Drive in system.
J2	Bus cable connector to the Controller.
J3	Dc power supply connector.
J4	Motor Control connector.
J5	Voice Coil connector
J6	Servo head and Data head 0 connector.
J7	Data heads 1 and 2 connector.
J8	Control Panel connector used for LEDs in identifying malfunctions in Disc Drive.
J9	Radial cable connector to the Controller.

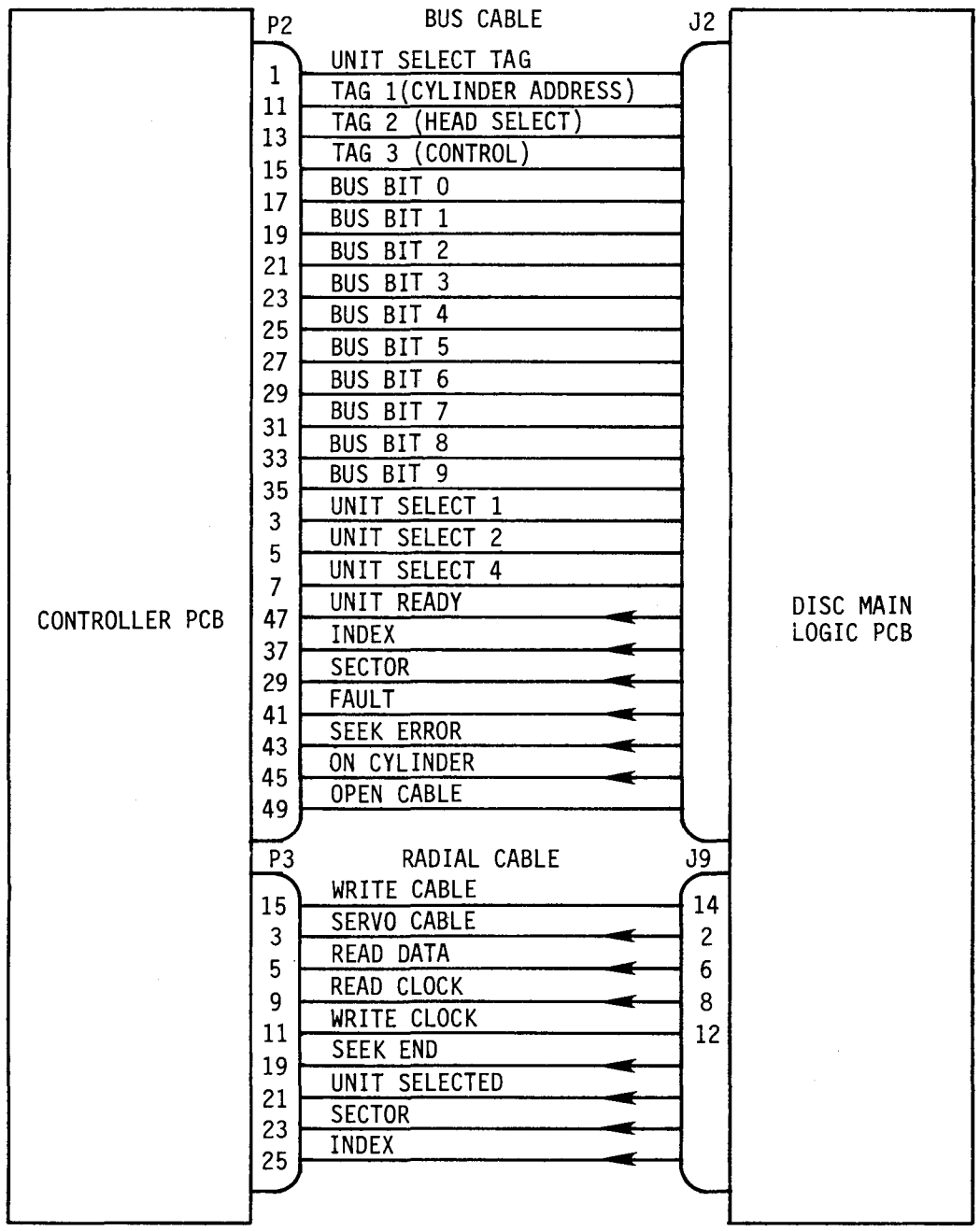
2.3.2 INTERFACE CABLING

The Bus cable (J2-P/N 902687) and Radial cable (J9-P/N 902622) are connected directly from the Disc Drive to the Controller in the host CPU. Figure 2-4 gives Interface Cabling/Pin assignments and Bus Tag Decode information.



* DRIVE ADDRESS SELECTION, 10N-1 THRU 10N-3
  WRITE PROTECT, 10N-7
  DIAGNOSTIC MODE, 10N-5

Figure 2-3. Main Logic PCB



BUS BIT	TAG 1 CYLINDER ADDRESS	TAG 2 HEAD SELECT	TAG 3 CONTROL
0	1	1	WRITE GATE
1	2	2	READ GATE
2	4	4	
3	8	8	
4	16		FAULT CLEAR
5	32		
6	64		REZERO
7	126		
8	256	1024*	
9	512	2048*	READ STATUS

*USED FOR HIGH ORDER CYLINDER ADDRESS DURING TAG 2 TIME

Figure 2-4. Interface Cable/Pin Assignments and Bus Tag Decode

2.3.3 DC VOLTAGE CHECK

Power is applied to the Disc Drive from the host CPU control panel. To apply power, complete the following steps (refer to system manual for detailed system information).

1. Place power switch in ON position.
2. When READY indicator comes on, the dc voltage checks may be done using the following procedure.
   a. Locate connector J3 on the Main Logic PCB of the Disc Drive.
   b. Test the following voltages.

Connector J3	Voltage Check
Pin 1	GND
Pin 2	+24VDC±1.2VDC
Pin 3	-5VDC±0.25VDC
Pin 4	-12VDC±0.60VDC
Pin 5	+5VDC±0.25VDC
Pin 6	GND

3. If voltages are not within tolerance, refer to paragraph 3.4.1.

2.4 CONTROLS AND INDICATORS

Controls for the Disc Drive are located on the host CPU control panel.

There are two indicator lamps (LEDs) mounted on the Main Logic PCB near J8. A green lamp will indicate a READY status. A red lamp will indicate a FAULT status. Connector J8 is provided to test the following signals.

Connector J8	Function
Pin 3	$\overline{\text{READY}}$
Pin 4	GND
Pin 5	$\overline{\text{ON CYL}}$
Pin 6	$\overline{\text{FAULT}}$
Pin 7	$\overline{\text{PWR ON}}$
Pin 8	+5V

Note: Pins 1 and 2 not used.

2.5 SWITCHES AND JUMPERS

Drive Address, Write Enable, and Diagnostic mode are selected on Switch 10N located on the Main Logic PCB (see Table 2-1 for Switch selection).

The Sector switch, 12K, is also located on the Main Logic PCB (see Table 2-1 for Switch selection).

TABLE 2-1. SWITCH SELECTION

Switch 10N		
SW No.	Position	Function
1	OFF**	Drive Select Address Bit (Binary Weight 1)
2	OFF**	Drive Select Address Bit (Binary Weight 2)
3	OFF**	Drive Select Address Bit (Binary Weight 4)
4	OFF	Reserved
5*	OFF	Diagnostic Mode
6	OFF	Reserved
7	ON	Write Enable, All Data Heads
8	OFF	Not used
Switch 12K		
SW No.	Position	Sector Number Binary Weighted
1	OFF	1
2	ON	2
3	OFF	4
4	OFF	8
5	ON	16
6	OFF	32
7	OFF	64
8	OFF	Must be in off position

*SW5 must be placed in ON position when using Diagnostic mode.
**All OFF = Drive 0

Jumpers are preset at the factory and shall not be removed. Verify all jumpers are in correct location. Jumper contacts are listed as follows:

Three Pin		Two Pin
W4	1-2	W1
W8	2-3	W2
W7	1-2	W3
W14	2-3	W5
W11	1-2	W6
W12	2-3	W9
W16	1-2	W10
		W13

CHAPTER 3

MAINTENANCE

3.1 GENERAL DESCRIPTION

This chapter provides a block diagram functional description, adjustment procedures, and troubleshooting procedures.

3.2 BLOCK DIAGRAM FUNCTIONAL DESCRIPTION (FIGURE 3-1)

The Parallel Interface communicates with all functional assemblies of the Disc Drive and the Controller. Its major function is to control and monitor head positioning, spindle speed and status information.

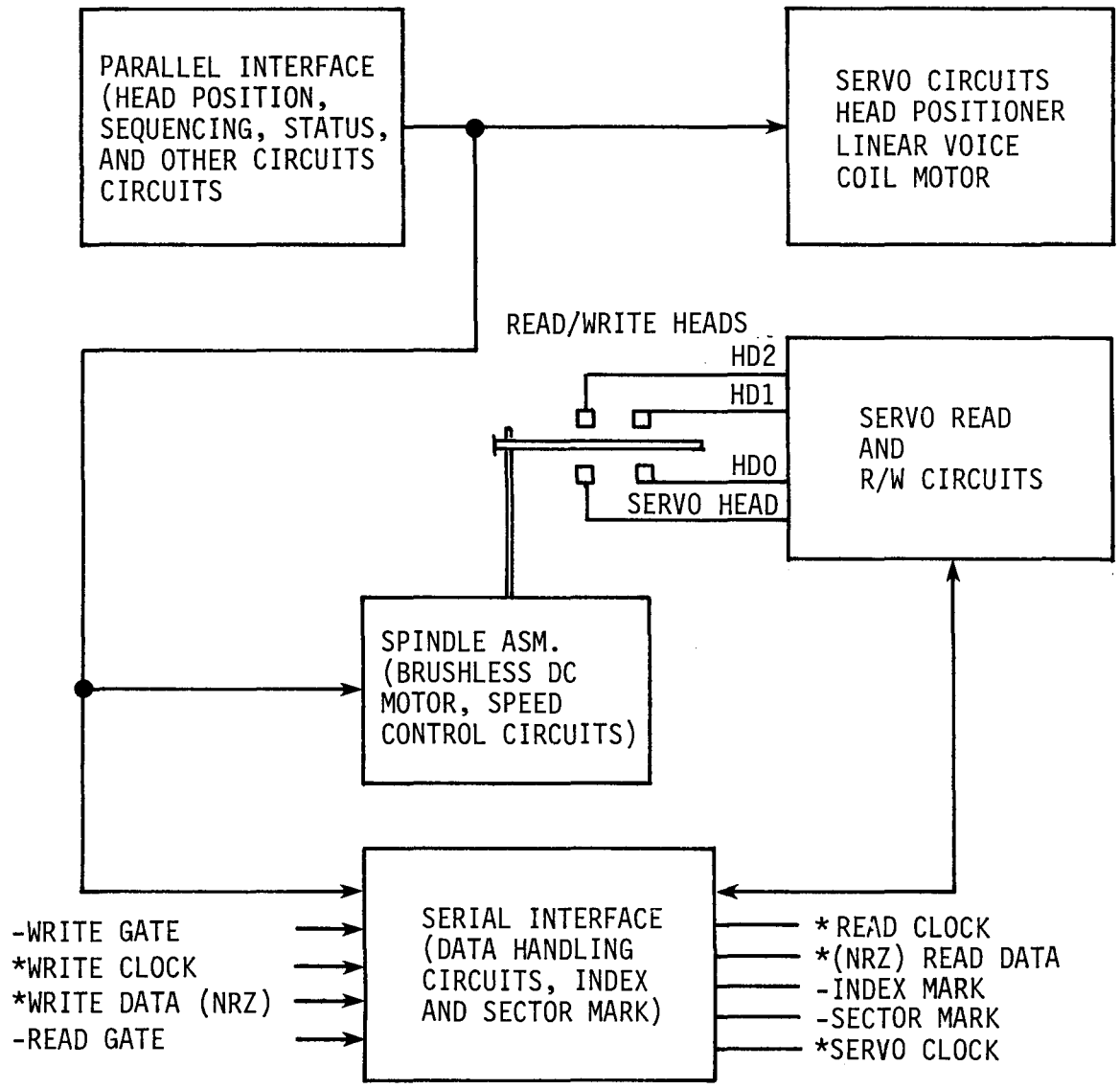
The Servo circuits, head positioner assembly, and Servo Head align the three Read/Write heads over a specified track location. The Servo circuits drive the heads to the landing zone upon detection of a low power condition or if both On Track and the Move modes are detected. These circuits also monitor voice coil speed.

The Read/Write heads and the Read/Write circuits perform the reading and writing of flux changes onto the disc.

There are three data heads and one Servo head. Head 1 and head 2 utilize the top surface, head 0 and the Servo head utilize the bottom surface of the disc (Figure 3-2).

The Spindle Motor is a brushless permanent magnet dc motor. The speed of the motor is controlled by a closed loop optical position encoder and a frequency to voltage converter.

The Serial Interface communicates with the Controller and handles the transfer of data and timing signals.



* DESIGNATES DIFFERENTIAL SIGNALS

Figure 3-1. Functional Block Diagram

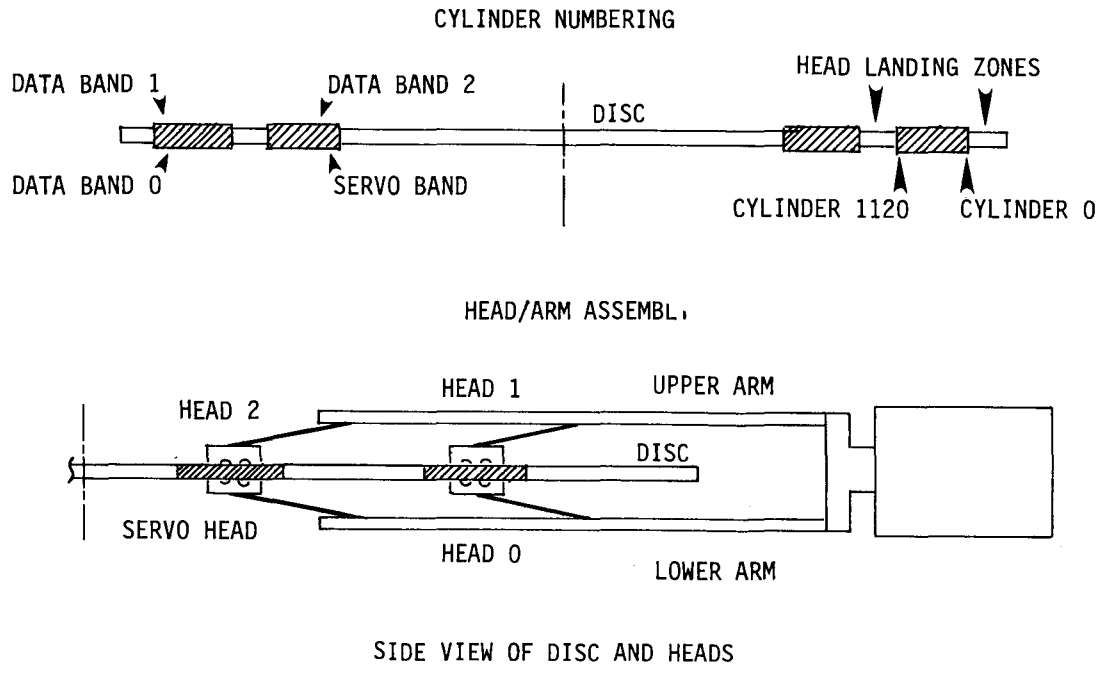


Figure 3-2. Data Head Positions

3.3 DIAGNOSTIC TESTS

There are two types of diagnostic tests available for the Disc Drive; Silver A5 and FORMAP. For a complete functional description of Silver A5 and FORMAP, refer to the appropriate User's Manual.

3.3.1 GENERAL DESCRIPTION OF SILVER A5

Silver A5 is divided into two groups:

1. Group 1 - is designed to check most controller functions and the disc drive's ability to seek and read.

2. Group 2 - uses the Diagnostic Cylinders to write and format. Checks are performed on the controller's ability to detect various errors such as ID, Alternate Cylinder and CRC. In order to run Group 2, the "Manual Intervention" option must be selected.

3.3.2 GENERAL DESCRIPTION OF FORMAP

FORMAP's basic function is to format the surface of the disc, create a map of all flaws, and to store the map on the subject disc. However, several of FORMAP's options can be used for diagnostic purposes.

The six options are:

1. Surface Read - will read the full surface of the disc and report all exceptions to normal status, which is '40' HEX.

2. Fault Map Report - will display the contents of the fault map which contains all flagged tracks and their assigned alternate tracks.

3. Selected Track Certification - will read original data of a track, store it, test the track, and if found bad or manually reassigned, copy that data to the alternate track and flag the original as bad. (REQUIRES OPTION 4 TO HAVE BEEN RUN PREVIOUSLY IN A FAULT MAP CREATED BY OPTION 4)

4. Full Surface Certification - will destroy the contents of the whole disc, test it for flaws, create a new map, and write a bootstrap in sector zero. The serial is kept in the map and once assigned, cannot be changed. (REQUIRES AUTHORIZATION)

5. Logical Sector to Sector, Head, Cylinder - will convert the logical sector number to the location of the disc surface by physical sector, head, and cylinder.

6. Sector Zero Recovery - will rewrite the bootstrap in sector zero using the serial stored in the map. (REQUIRES OPTION 4 TO HAVE BEEN RUN PREVIOUSLY IN A FAULT MAP CREATED BY OPTION 4)

3.4 ADJUSTMENT PROCEDURES

3.4.1 POWER SUPPLY ADJUSTMENTS

One of two types of power supplies are found on the Disc Drive (P/N CP353-1) and Model 2981). Regardless of which type is found, the Disc Drive must be removed from the system before the power supply can be removed for adjustment. Once removed, the power supply can be placed near to and reconnected to the Disc Drive. To remove power supply for adjustments, use the following procedure.

NOTE

There is no power switch located on the dc power supply. Power will be applied when the power cord is connected.

1. Remove ac power from the host CPU.
2. Open host CPU cabinet to gain access to Disc Drive (if required).
3. Remove ac power plug at rear of Disc Drive power supply.
4. Remove Disc Drive.
5. Disconnect dc power supply connector (J3) from Main Logic PCB.
6. Remove six retaining screws securing power supply to deckplate.
7. Remove power supply.
8. Locate adjustments (refer to Figure 3-3 or 3-4).
9. With power supply removed, reconnect power cable to J3 of the Main Logic PCB.
10. Reconnect ac power plug to power supply.
11. Apply power to host CPU.
12. Adjust voltages.
13. If power supply will not meet tolerance, it must be replaced. Turn OFF power at host CPU.

14. Disconnect power supply from Main Logic PCB.

15. Disconnect ac power plug from power supply.

16. Reinstall new power supply in Disc Drive.

17. Apply power to host CPU.

18. Test voltages.

Measurements will be done at connector J3 at the right rear of the Main Logic PCB. Ground meter at C186 on side with C186 designator. Check voltage on J3.

Pin 2 +24VDC±1.2VDC

Pin 5 +5VDC±0.25VDC

Pin 3 -5VDC±0.25VDC

Pin 4 -12VDC±0.60VDC

Pins 1 and 6 are ground

CAUTION

Use only an insulated shank screwdriver. Damage may occur to the power supply.

Adjusting of power supply will require a long (five inch) insulated shank screwdriver with 1/8 inch blade.

3.4.1.1 Power Supply (P/N CP353-1)

Three voltages +5, -5, and +24 must be adjusted by reaching through holes inside the power supply chassis as shown in Figure 3-3. The -12 is not adjustable.

Voltage	Adjustment	Wire Color Leaving Supply
+24V	R20	Red (return is Brown)
+5V	R40	Black (return is Grey)
-5V	R38	Yellow (return is Grey)
-12V	Not Adj.	Orange (return is Grey)

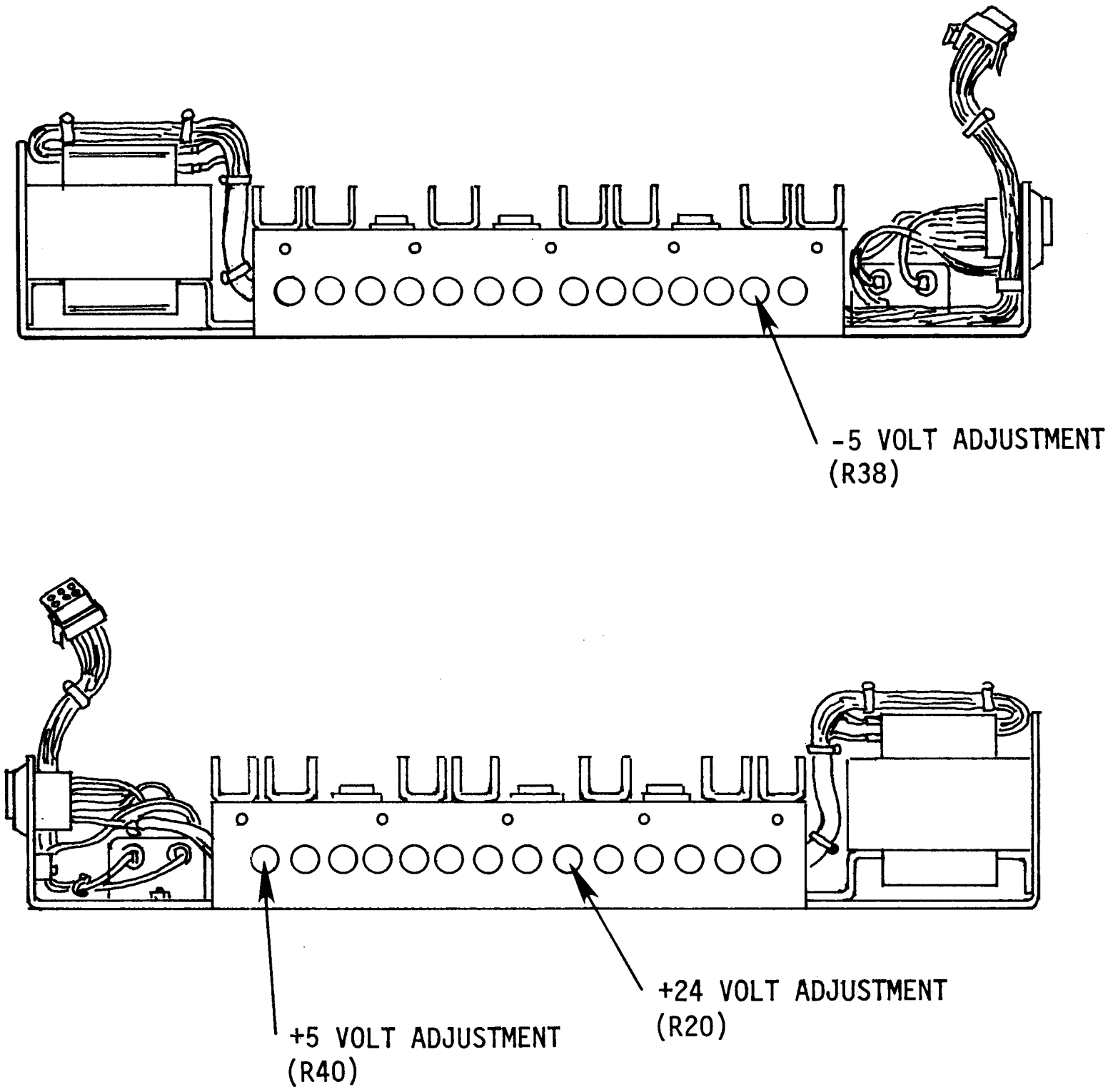


Figure 3-3. Power Supply Adjustments (P/N CP353-1)

3.4.1.2 Power Supply (Model 2981)

On this power supply, the adjustments are visible externally as shown in Figure 3-4.

Voltage	Adjustment	Wire Color Leaving Supply
+24V	R3	Black with White Lettering (return is Yellow)
+5V	R14	Red (return is Solid Black)
-5V	R20	Brown (return is Solid Black)
-12V	Not Adj.	Orange (return is Solid Black)

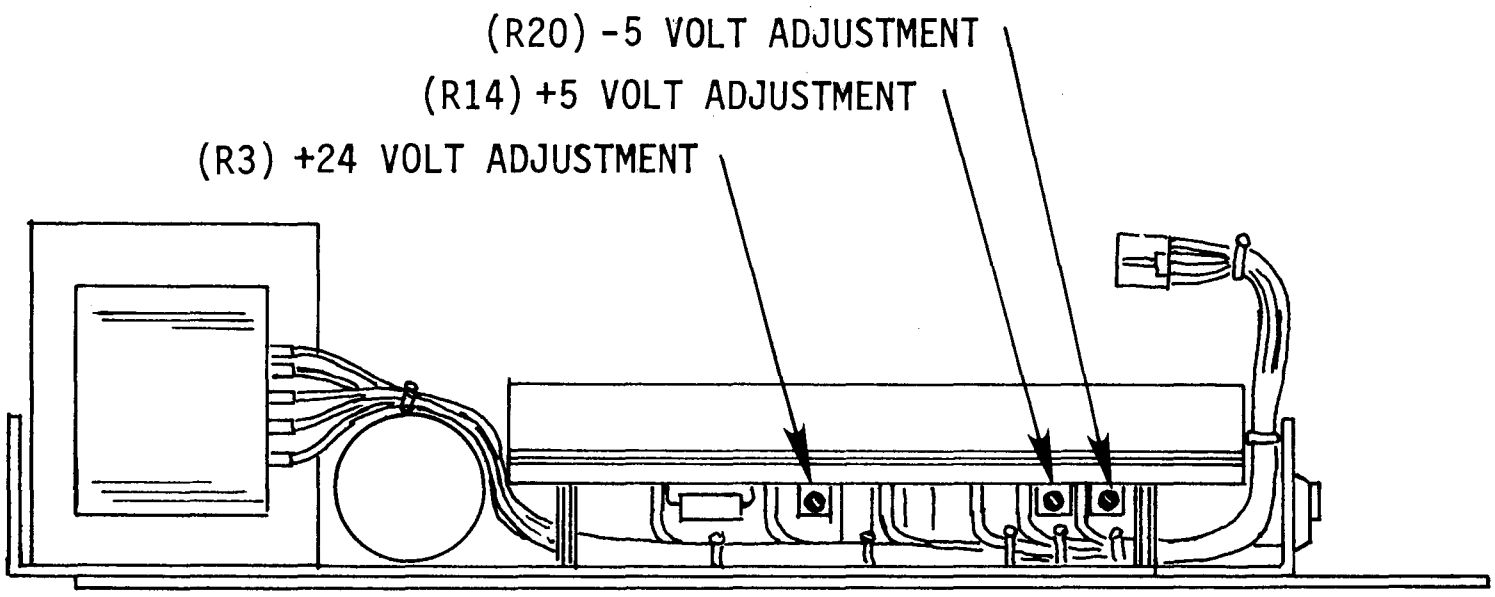


Figure 3-4. Power Supply Adjustments (Model 2981)

3.4.2 WRITE CURRENT ADJUSTMENT

For this adjustment, you must be writing all-ones. Do not use Head 2. Do not use any tracks which could contain customer data. Write as many sectors on one track as possible for best display. With an oscilloscope, use the following procedure (refer to Figure 2-3 for adjustment location).

Scope: Tektronix 465 or equivalent

Probes: Two X10 attenuation

Channel 1 to side of R46 facing transistors. Set input to 1 Volt/Division (0.1 Volt/Division with non-indicating X10 probe).

Channel 2 to other side of R46. Set input to 1 Volt/Division (0.1 Volt/Division with non-indicating probe).

Vertical display mode to ADD, Channel 2 INVERTED. Position trace near top of graticule.

Time base = 0.2 ms, TRIGGER SLOPE = "-", TRIGGER SOURCE = Channel 2, dc coupled.

NOTE: Adjust R351 (near R46) for -5V (Figure 3-5).

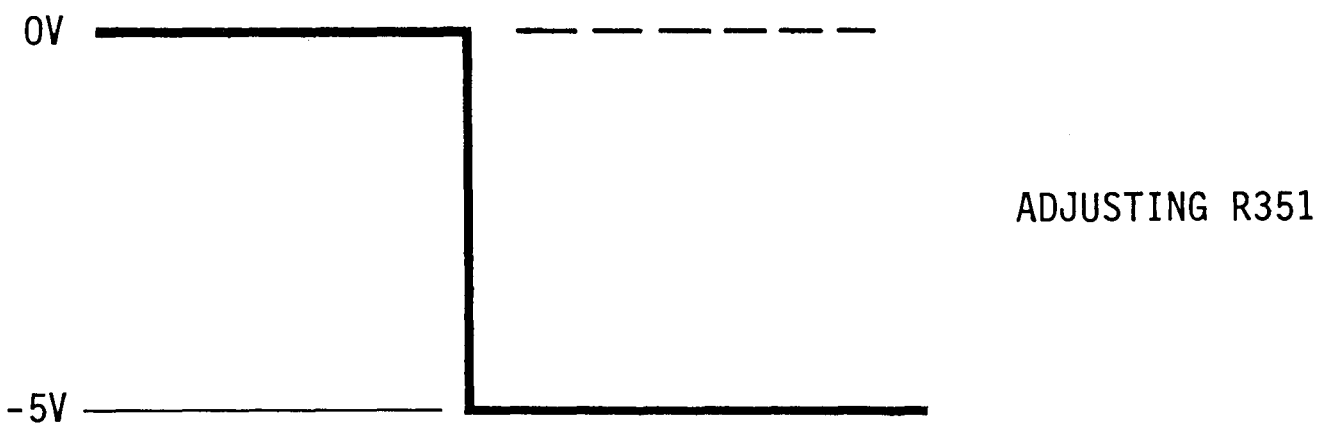


Figure 3-5. Write Current Adjustment

3.4.3 DATA WINDOW ADJUSTMENT

For this adjustment, you must first write all ones, then make the adjustments while reading all-ones. Do not use Head 2. Do not use any tracks which could contain customer data. Write as many sectors on one track as possible for best display. With an oscilloscope, use the following procedure (refer to Figure 2-3 for adjustment location).

Scope: Tektronix 465 or equivalent

Probes: Two X10 attenuation

Channel 1 to TP13 (Window), ground to TP2. Set input to display 0.5 Volt/Division (50 MV/Division with non-indicating X10 probes).

Channel 2 to TP9 (Data), ground to TP2. Set input to display 0.5 Volt/Division (50 MV/Division with non-indicating X10 probes).

Vertical display mode = CHOPPED (Channel 2 should NOT be inverted).

Time base = 0.1 us with X10 mag, TRIGGER SOURCE = Channel 1, dc coupling NORMAL mode.

Adjust R32 so Positive-Going edge of Data is in center of low-going Window pulse (Figure 3-6).

NOTE

It is normal for the display to "jitter".

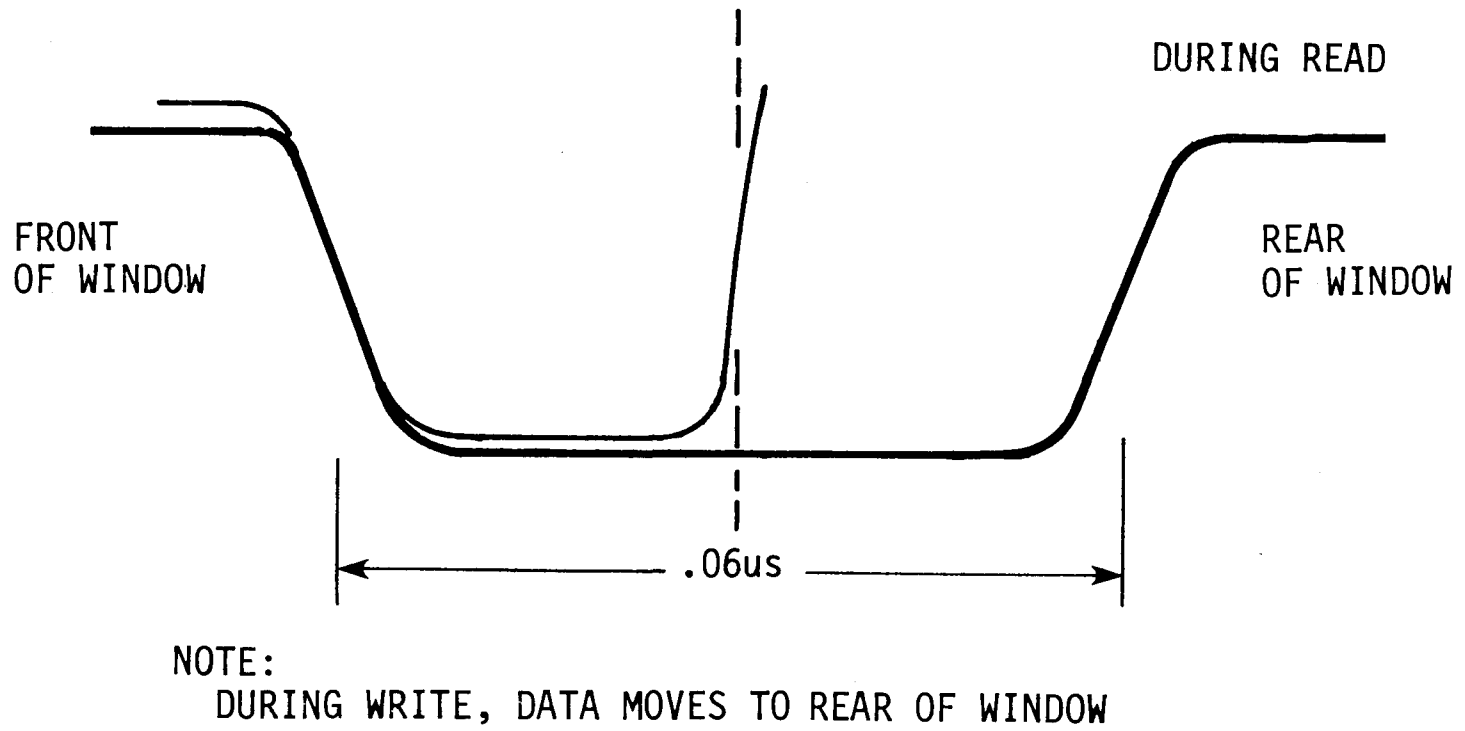


Figure 3-6. Data Window Adjustment

3.5 FAULT ISOLATION

Table 3-1 lists the Fault Isolation procedures for the Disc Drive. Table 3-2 lists the Status Bit information. Both tables are designed as an aid in troubleshooting the Disc Drive.

TABLE 3-1. FAULT ISOLATION

Spindle Rotation		
Symptom	Possible Cause	Suggested Action
Rotation does not start.	Spindle lock.	Place in Unlock position
	Incorrect or missing voltage at Main PCB connector J4.	Check power supply.
	+ OFF signal (J4-4) is +5 VDC, should be 0 volts for rotation.	Check microprocessor reset signal on Main Logic PCB: should be false. Check Power-On reset (POR): should be false. Check power reset (PRST): should be false.
	Defective Motor Control Assembly	Check J1-5 of Motor Control Assembly for +12 volts (LED voltage). Check fuse in Motor Control Assembly.

TABLE 3-1. FAULT ISOLATION (continued)

Spindle Rotation		
Symptom	Possible Cause	Suggested Action
Rotation does not start.	Defective Photocell Circuit Board	Check for open LED, defective connector or phototransistor.
	Defective Spindle Motor	Manually rotate spindle in clockwise directly only (viewed from bottom) to ensure motor is not binding. If motor is binding replaced Disc Drive. NOTE: Rotation in opposite directions may damage disc.
Spindle rotates and stops after about one minute.	Carriage Lock	Place in Unlock position.
	Defective Motor Control Assembly	Replace Motor Control Assembly.
	Defective Photocell Circuit Board	Replace Disc Drive.
	Speed Control not being sensed by Microprocessor.	Defective Main Logic PCB.
	Spindle Motor has excessive drag.	Replace Disc Drive
Spindle rotates but unit does not come Ready, or Ready condition comes and goes.	Fault Condition being sensed.	Check Fault Status.
	Intermittent power supply failure.	Replace Power Supply.
	Defective Main Logic PCB.	Replace Main Logic PCB.
	Defective Motor Control Assembly	Replace Motor Control Assembly.
	Defective Disc Drive	Replace Disc Drive.

TABLE 3-1. FAULT ISOLATION (continued)

Command Status Transfers		
Symptom	Possible Cause	Suggested Action
Incorrect state on Unit Selected (J9-21)	Device address select switch (10N).	Refer to Table 2-1 for switch definition.
	Open Cable Detect true (J1, J2 pin 28).	Check controller, cable and connectors.
	Unit Select Tag or Unit Address missing or mistimed.	Check controller, cable and connectors.
Selected unit does not issue status	Device Not Ready.	Replace Main Logic PCB.
Select unit does not accept commands.	Tag and bus data malfunction.	Check controller, cable and connectors. Replace Main Logic PCB.
Select Unit issue Seek Error.	Defective servo action.	See Head/Positioning/Servo.
Select Unit fails to issue Index.	Defective circuit.	Replace Main Logic PCB.
	Servo Head fails to READ.	See Head/Positioning/Servo.

Head/Positioning/Servo

Symptom	Possible Cause	Suggested Action
Fails to move to new Address.	Command transfer circuitry defect.	Replace Main Logic PCB.
Continuous Seek Error condition.	Defective circuitry or connection.	Defective servo circuitry on Main Logic PCB. If fault continues with operational spare installed, and spindle speed and write circuits are not the source of the fault, replacement of the disc drive is recommended. Fault connection to servo read head, check J6. Fault connection to voice coil actuator, check J5. Incorrect voltage, check J3. Carriage locked.

TABLE 3-1. FAULT ISOLATION (continued)

Head/Positioning/Servo		
Symptom	Possible Cause	Suggested Action
Seeks to incorrect cylinder address.	Defective circuitry or servo system.	Defective signal from controller or fault in the interface cable. Defective circuitry on Main Logic PCB. If symptom continues with operational spare installed, and controller and cable are not the source of the fault, replacement of the disc drive is recommended. Seek ma be correct and method of checking for correct seek locatio may be defective. This could be caused by a read/write fault.

Write Data Transfer

Symptom	Possible Cause	Suggested Action
Fault is set with each attempt to write data.	Incorrect switch setting or circuit defect.	See Table 2-2 for switch definition Multiple heads selected can be checked at TP20 which will be high if more than one head is selected. Act Unsafe condition is checked at TP1 which will be high if there are not write transitions with Write Gate true or write transitions with Write Gate false.
Data is written incorrectly and faults does not set.	Reads data difficultly.	See following section, Read Data Transfer.

Read Data Transfer

Symptom	Possible Cause	Suggested Action
Reads header fields and data fields correctly, but will not read newly written data.	Defect in write operation.	Replace Main Logic PCB.

TABLE 3-1. FAULT ISOLATION (continued)

Read Data Transfer		
Symptom	Possible Cause	Suggested Action
Fails to read, but will perform a write operation without a Fault.	Defect in Read circuitry.	Check all cable connections. Replace Main Logic PB. Replace terminator. If read error persists after replacement of Main Logic PCB and terminator and if cable connections are correct, it is possible that the format being used is erroneous. If format is correct, replacement of the disc drive is recommended.

TABLE 3-2. STATUS BIT DESCRIPTION

Status Bit	Description
0	MULTIPLE HEAD SELECT indicates that more than one head was selected.
1	NO WRITE DATA indicates that transitions in write current failed to occur with WRITE GATE active.
2	NO WRITE GATE indicates that write current was sensed when WRITE GATE was not active.
3	OFF TRACK WRITE indicates that the R/W heads were not within acceptable track following limits while WRITE GATE was active.
4	READ ONLY indicates that WRITE GATE became active while the Disc Drive was not "WRITE ENABLED".
5	PLO LOCK ERROR indicates that the PLO signal was not correctly synchronized.
6	NOT USED, always zero.
7	POWER FAULT indicates that spindle was already spinning when power was applied.
8	MULTI-TAG indicates that two or more tag lines were simultaneously active.
9	READ AND WRITE indicates that both READ GATE and WRITE GATE were simultaneously active.

TABLE 3-2. STATUS BIT DESCRIPTION (continued)

Status Bit	Description
10	OFF CYLINDER indicates that the positioner was not ON CYLINDER while WRITE GATE was active.
11	SEEK TIMEOUT indicates that the positioner failed to return to track 0 with 900 msec; or it failed to complete a seek operation within 130 msec.
12	SPEED ERROR indicates that the disc failed to reach or failed to run at operating speed.
13	GUARD BAND ERROR indicates that the positioner entered the inner or outer guard bands while performing a seek or restore operation.
14	ILLEGAL CYLINDER indicates that the disc file was commanded to seek to a cylinder address which does not exist in the drive.
15	DIAGNOSTIC CYLINDER ERROR indicates that the positioner has not moved to one of the Diagnostic Cylinders (Cylinder Address Register 2 to 7).

CHAPTER 4

SPARE PARTS LIST/REMOVAL/REPLACEMENT PROCEDURES

4.1 INTRODUCTION

This chapter contains the spare parts list (Table 4-1) and removal/replacement procedures. Figure 4-1 shows component locations.

TABLE 4-1. SPARE PARTS LIST

Item Number	MM Number	Part Number	Description
1	290000	B903028-01	Disc Controller PCB
2	290010	200098	Main Logic PCB
3	290020	200083	Motor Control PCB
4	290030	200138	Terminator
5	290100	400384-001	Power Supply Assy
6	293010	330410	Head Disc Assy

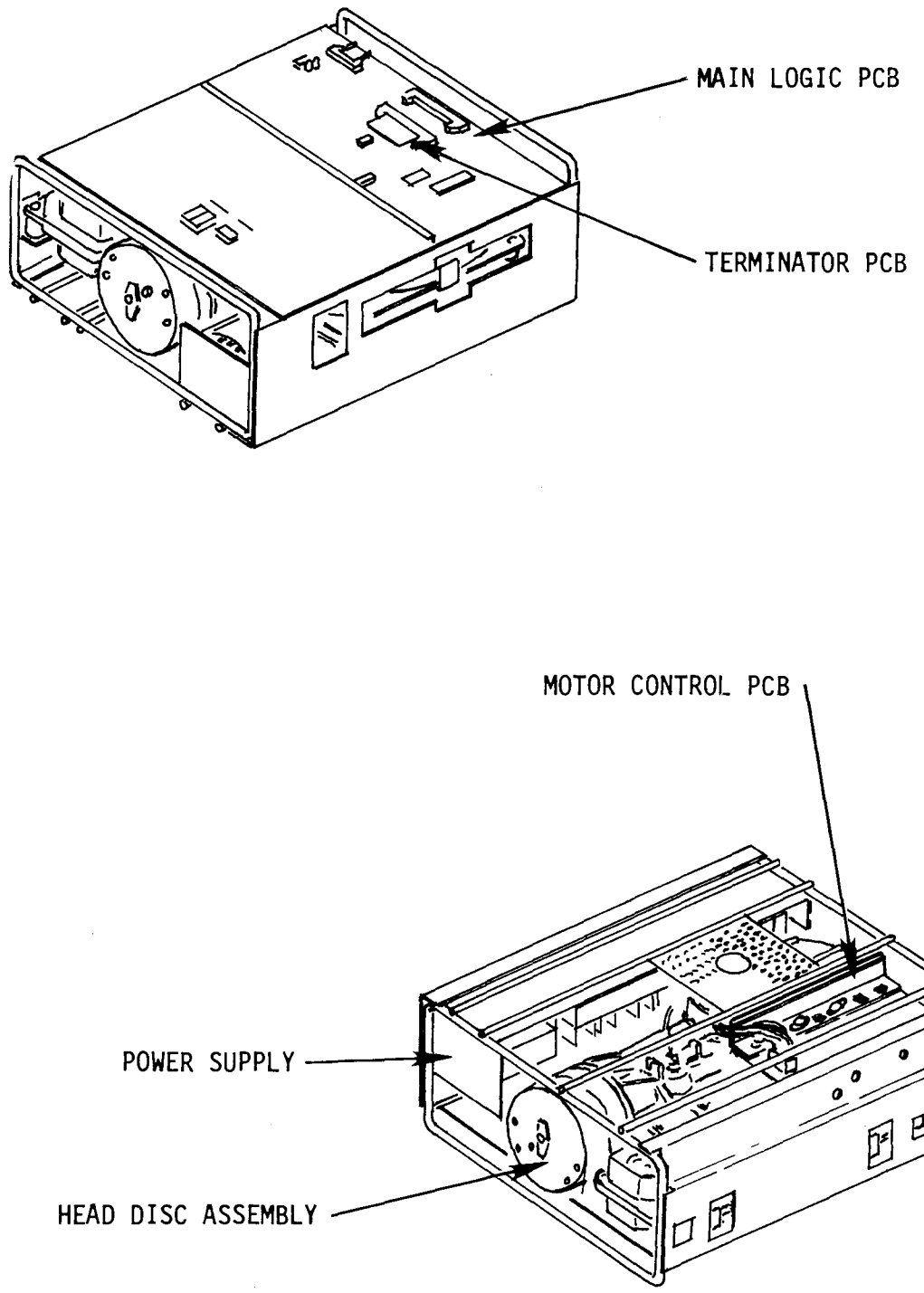


Figure 4-1. Component Locations

4.2 REMOVAL/REPLACEMENT PROCEDURES

Removal/Replacement procedures are given for spared parts.

4.2.1 HEAD DISC ASSEMBLY (HDA)

1. Remove ac power from host CPU.
2. Open host CPU cabinet to gain access to Disc Drive.
3. Remove ac power from Disc Drive power supply.
4. Remove four screws securing HDA to host CPU cabinet.

CAUTION

When removing connectors J6 and J7 (R/W Heads and Servo Head) be careful not to bend the pins. Damage may occur to the printed wiring.

5. Disconnect and tag all cables and connectors from Main Logic PCB.
6. Remove Main Logic PCB located on top of HDA.
7. Remove Motor Control PCB located on bottom of HDA.
8. Remove dc power supply located on bottom of HDA.
9. Replace Disc Drve and reverse steps 8 thru 1.
10. Ensure that all cables and connectors are secure.

4.2.2 POWER SUPPLY ASSEMBLY

1. Remove ac power from the host CPU.
2. Open host CPU cabinet to gain access to Disc Drive.
3. Remove ac power plug at rear of Disc Drive power supply.
4. Remove Disc Drive (refer to paragraph 4.2.1).
5. Disconnect dc power supply connector (J3) from Main Logic PCB.
6. Remove six screws securing power supply to the deckplate.
7. Remove power supply.
8. Replace new power supply in Disc Drive and reverse steps 7 thru 1.
9. Apply power to host CPU.

4.2.3 MAIN LOGIC PCB AND MOTOR CONTROL PCB

When removing PCBs, disconnect and tag all cables and connectors. Ensure when replacing PCBs that all cables and connectors are secure.

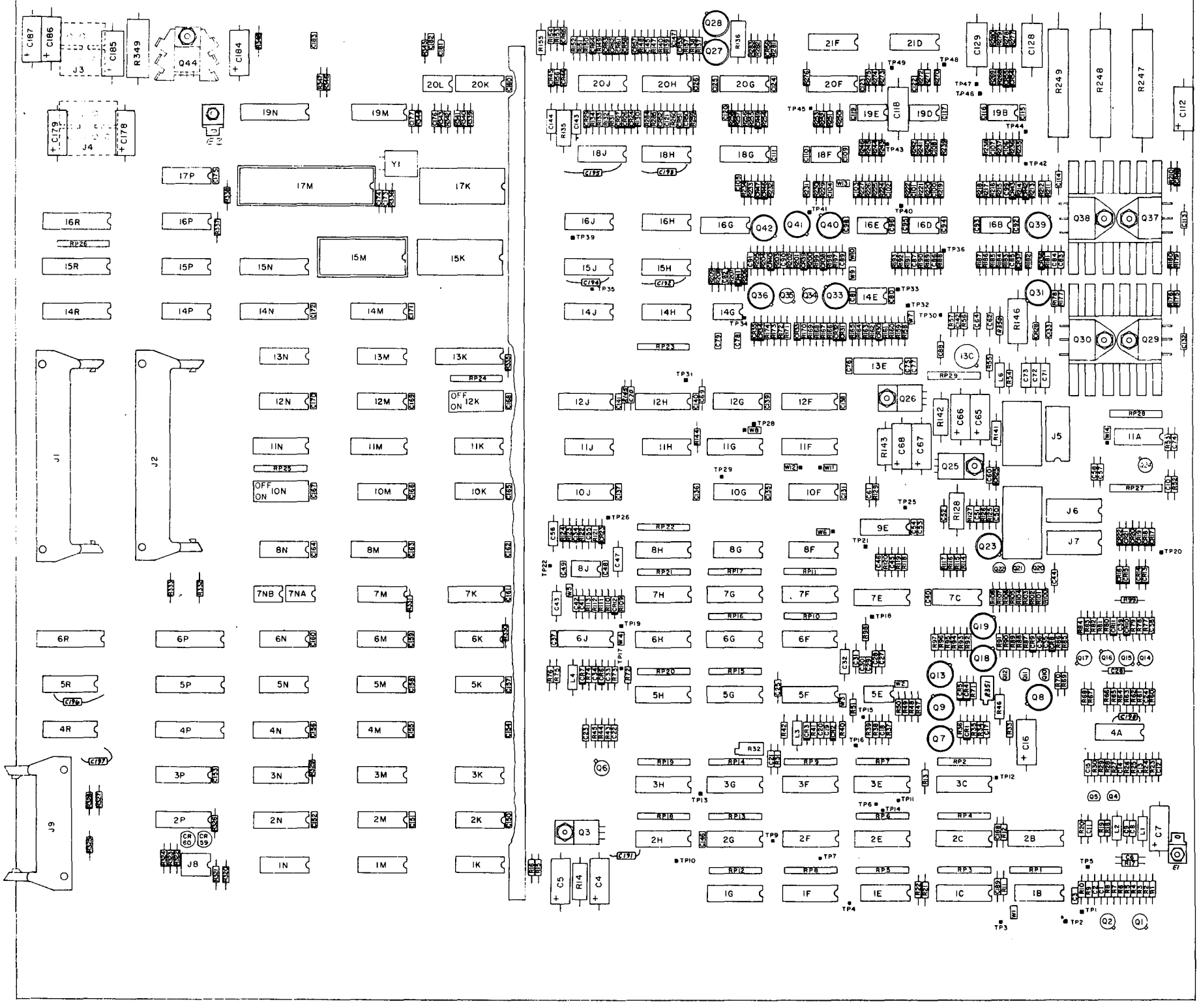
NOTE

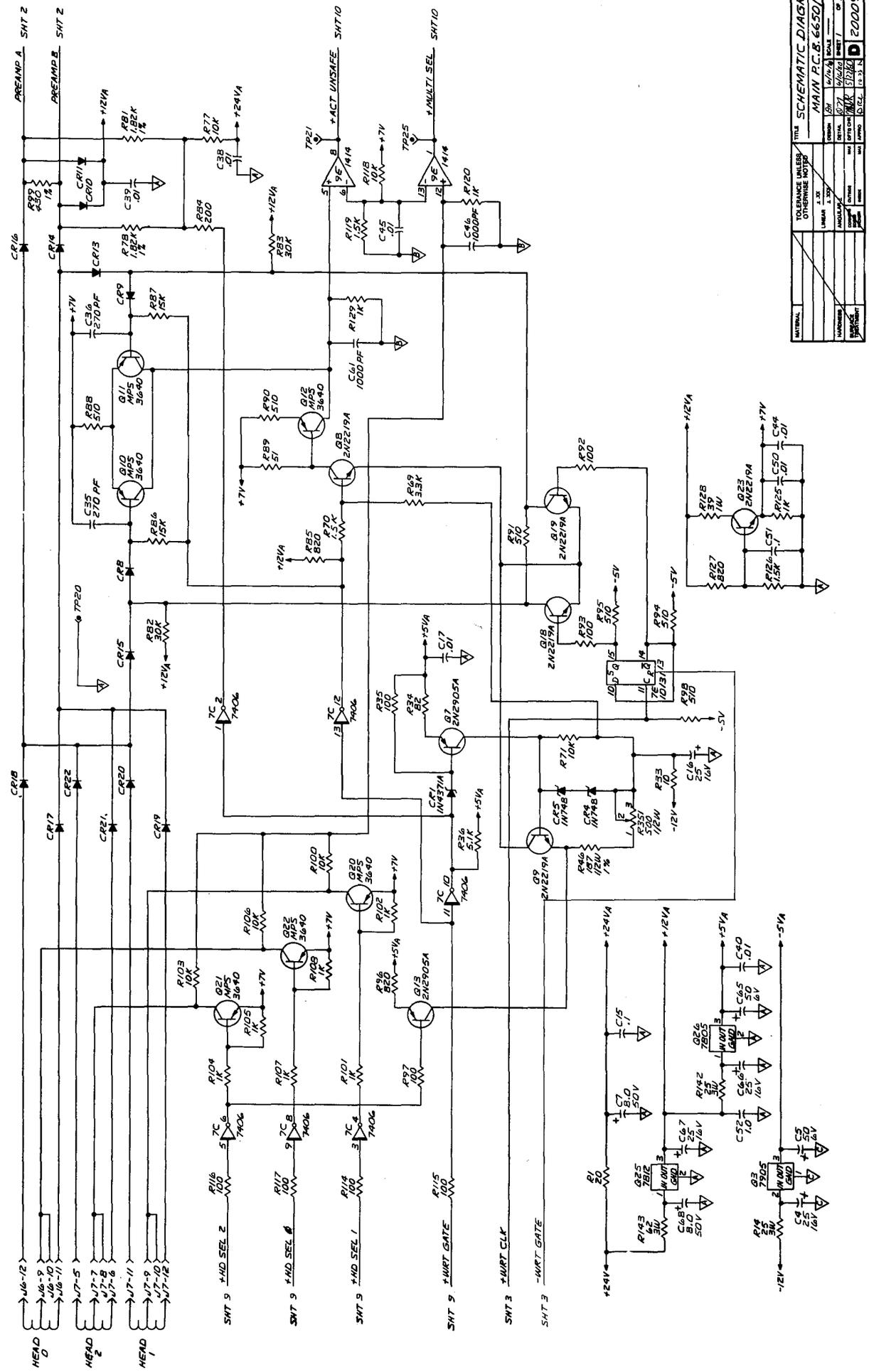
When replacing Main Logic PCB, remove and save terminator.

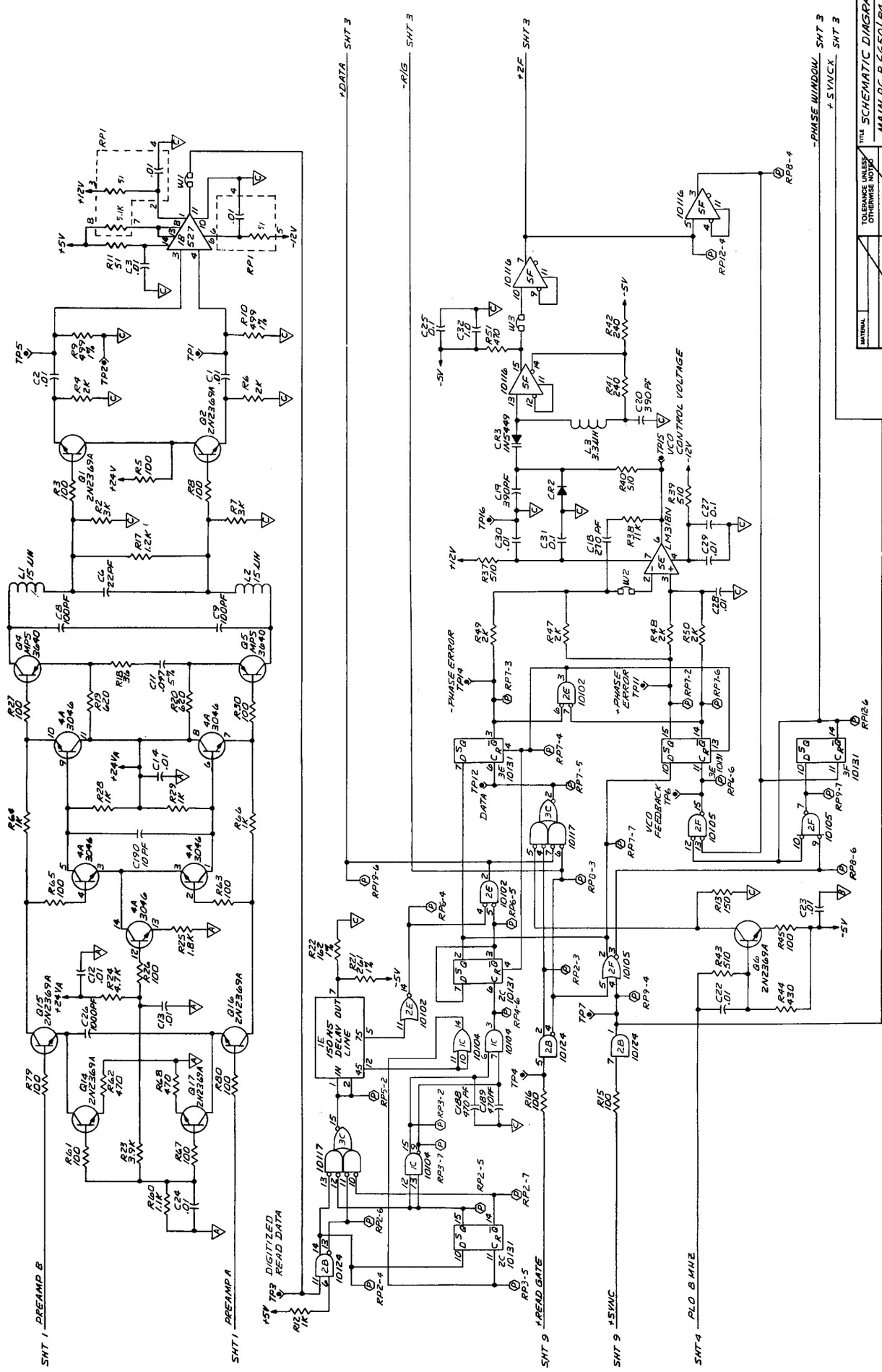
CHAPTER 5

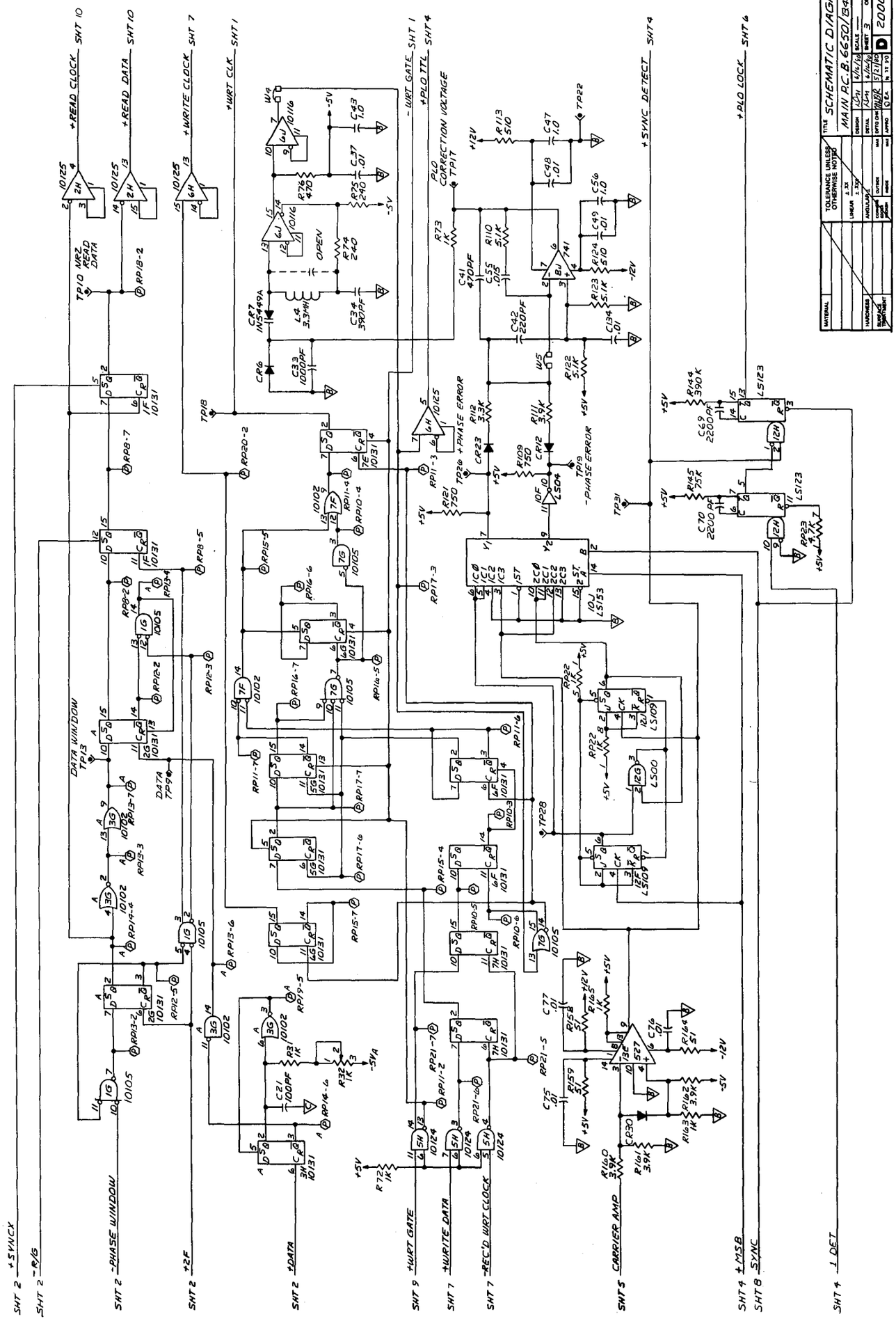
REFERENCE DATA

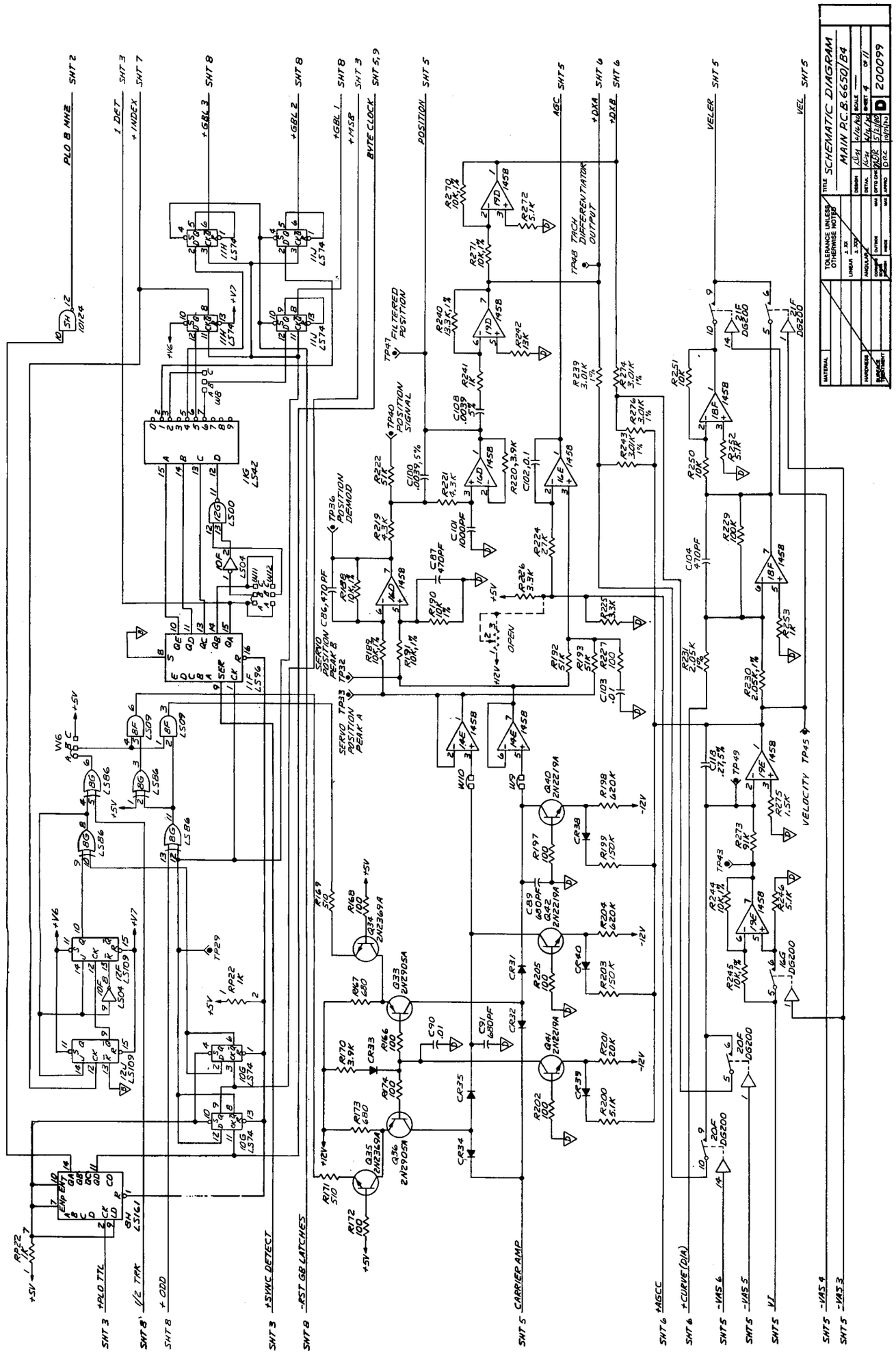
Title	Drawing Number
Main Logic PCB	200098
Schematic	200099
Motor Speed Control	200083
Schematic	200084
Power Supply (CP353-1)	17048
Power Supply (Model 2981)	2981-902
Filtered Power Supplies	330357
Terminator PCB	200138
Schematic	200139



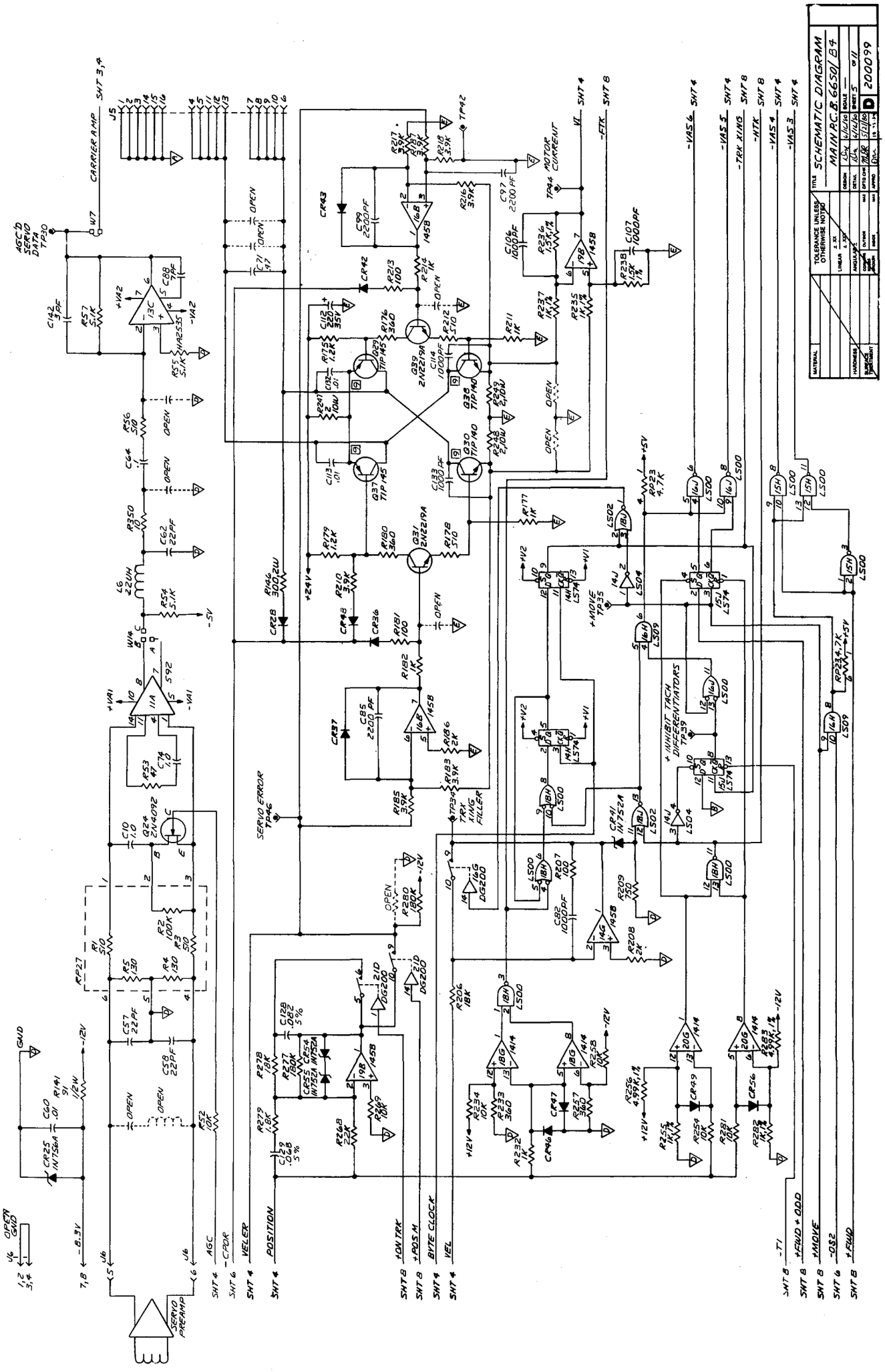

SCHEMATIC DIAGRAM
MAIN P.C.B. 6650/64
2000099
PREAMP A
PREAMP B
+ACT UNSAFE
+MULTI SEL
+HD SEL 2
+HD SEL 0
+HD SEL 1
+WRT GATE
+WRT CLK
-WRT GATE
HEAD 0
HEAD 2
HEAD 1


+DATA SHT 3
-PIS SHT 3
+2F SHT 3
-PHASE WINDOW SHT 3
+SYNCX SHT 3
SCHEMATIC DIAGRAM
MAIN P.C.B 6650/B4
200099
SHT 1 PREAMP B
SHT 1 PREAMP A
DIGITIZED READ DATA
+READ GATE
+SYNC
PLO 8 MHz
VCO CONTROL VOLTAGE
PHASE ERROR
VCO FEEDBACK


SCHEMATIC DIAGRAM
MAIN P.C.B. 6650/B4
D
200099
+READ CLOCK
+READ DATA
+WRITE CLOCK
+WRT CLK
-WRT GATE
+PLO TTL
PLO CORRECTION VOLTAGE
+SYNC DETECT
+PLO LOCK
+PHASE ERROR
-PHASE ERROR
DATA WINDOW
+SYNCX
-R/G
-PHASE WINDOW
+2F
+DATA
+WRT GATE
+WRITE DATA
-REC'D WRT CLOCK
CARRIER AMP
+MSB
SYNC
1 DET



Reference Only - Will Not Be Maintained



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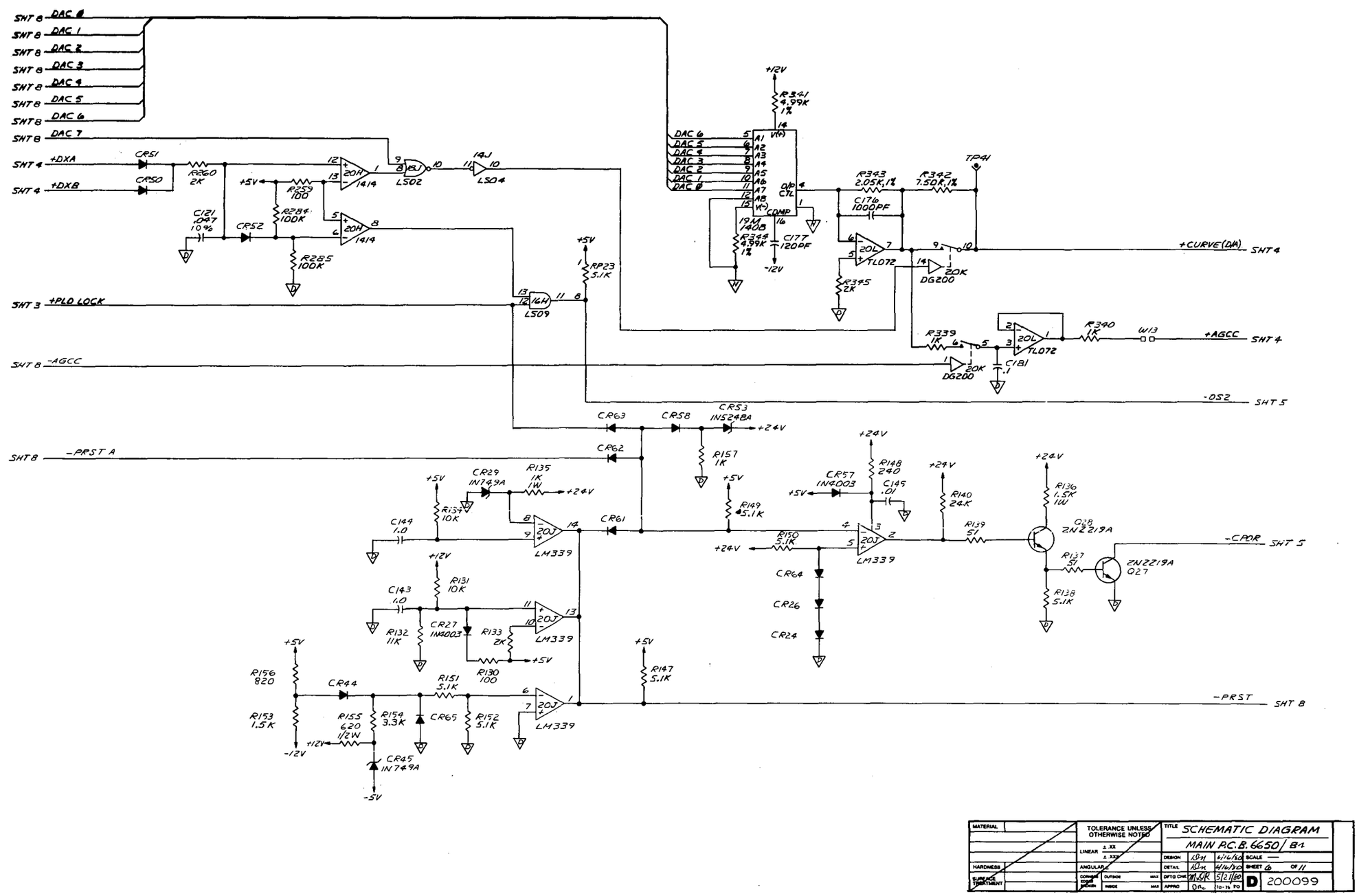

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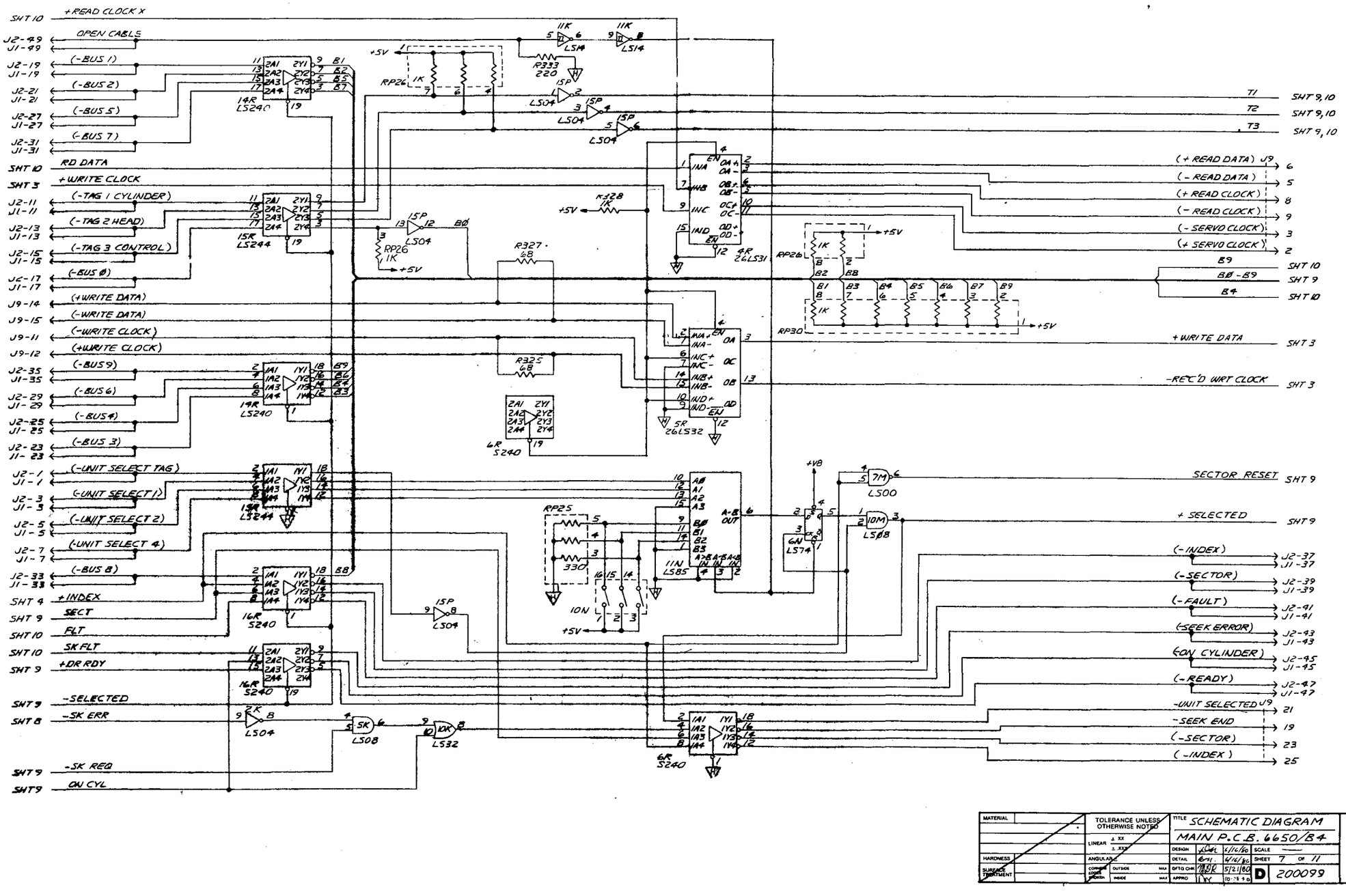
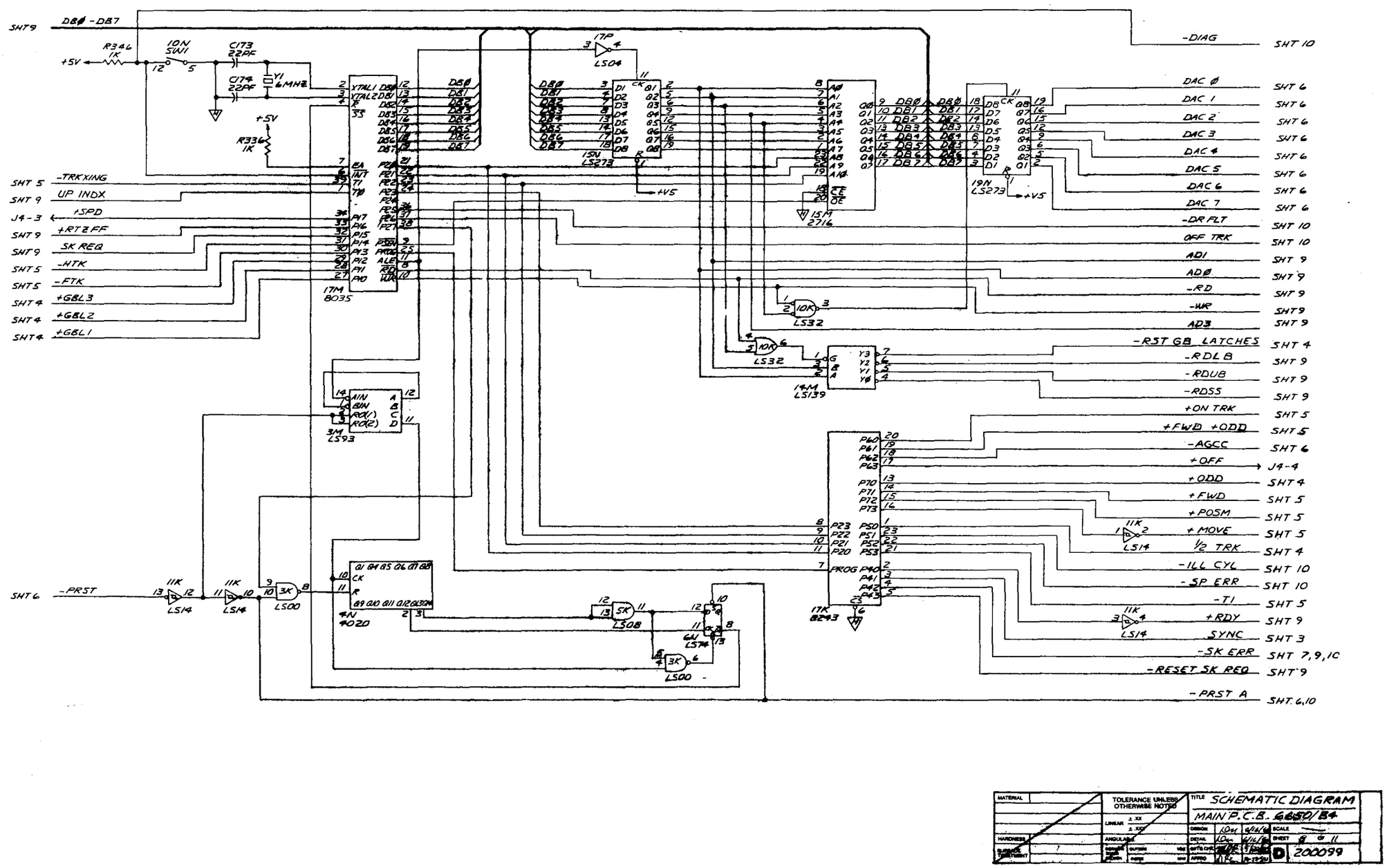


MATERIAL	TOLERANCE UNLESS OTHERWISE NOTED	TITLE	SCHEMATIC DIAGRAM
	LINEAR ± XX ± XXX		MAIN P.C.B. 6650/84
HARDNESS	ANGULAR	DESIGN	4/11/80 SCALE —
SURFACE FINISH DEPARTMENT	CONCENTRIC FORM OUTSIDE MAX INSIDE MAX	DETAIL	4/11 4/16/80 SHEET 7 OF 11
		APPRO	5/21/80 D 200099

Reference Only - Will Not Be Maintained



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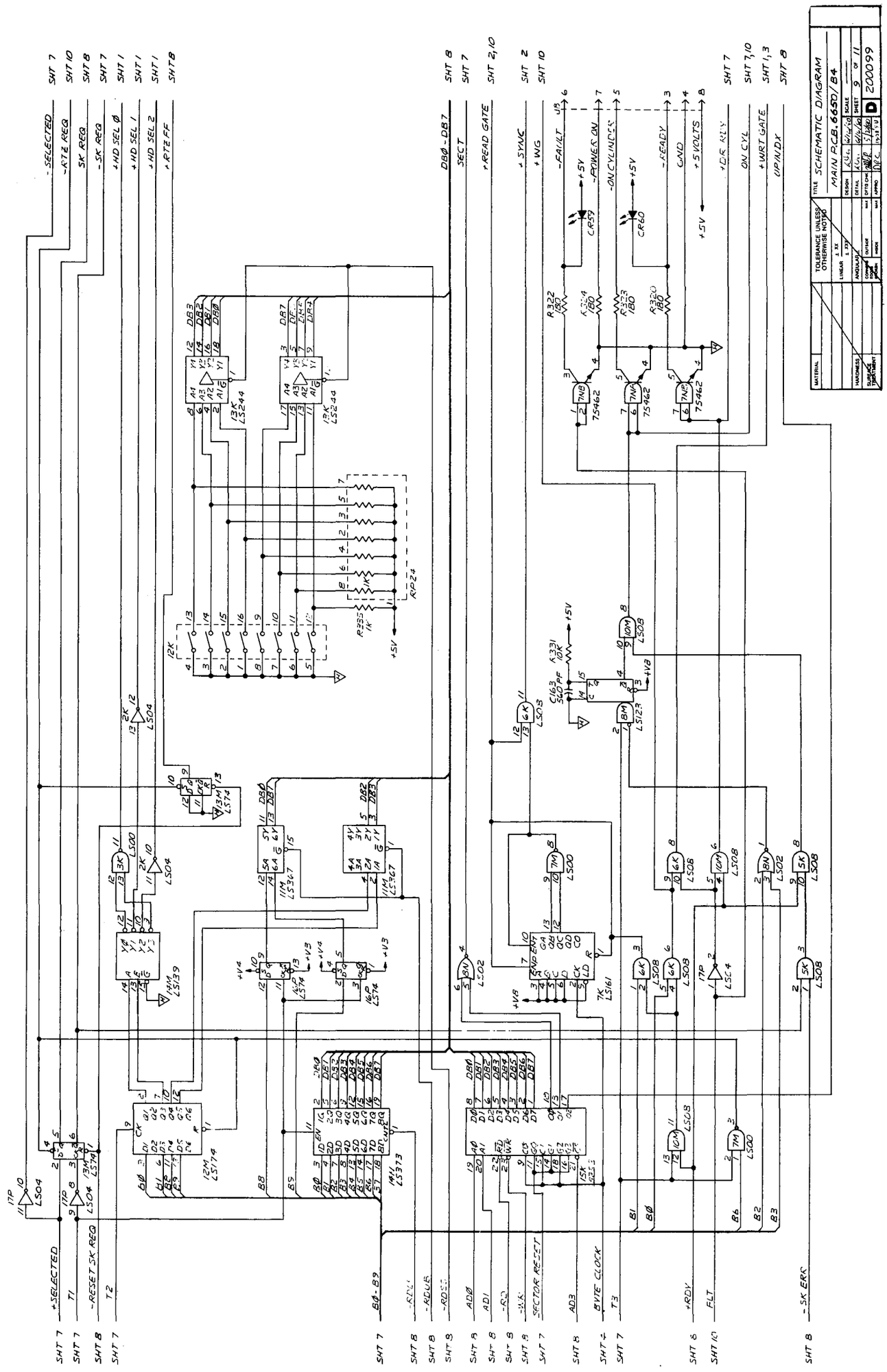
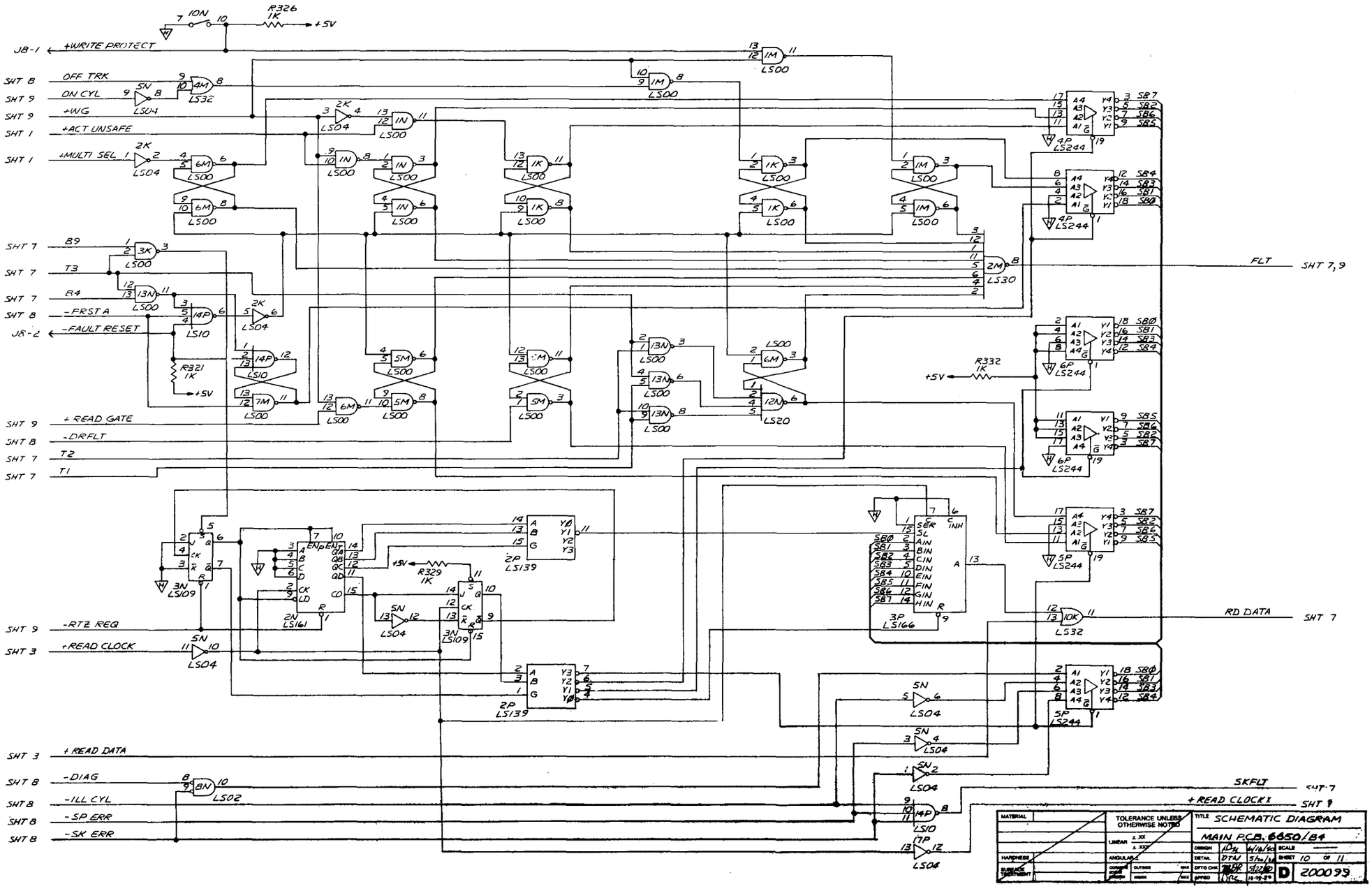

-SELECTED
-RTZ REQ
SK REQ
-SK REQ
+HD SEL Ø
+HD SEL 1
+HD SEL 2
+RTZ FF
DBØ - DB7
SECT
+READ GATE
+SYNC
+WG
-FAULT
-POWER ON
-ON CYLINDER
-READY
GND
+5 VOLTS
+DR RLY
ON CYL
+WRT GATE
UP/N.DX
+SELECTED
-RESET SK REQ
BYTE CLOCK
SECTOR RESET
+RDY
FLT
-SK ERR
SCHEMATIC DIAGRAM
MAIN PCB.6650/84
200099



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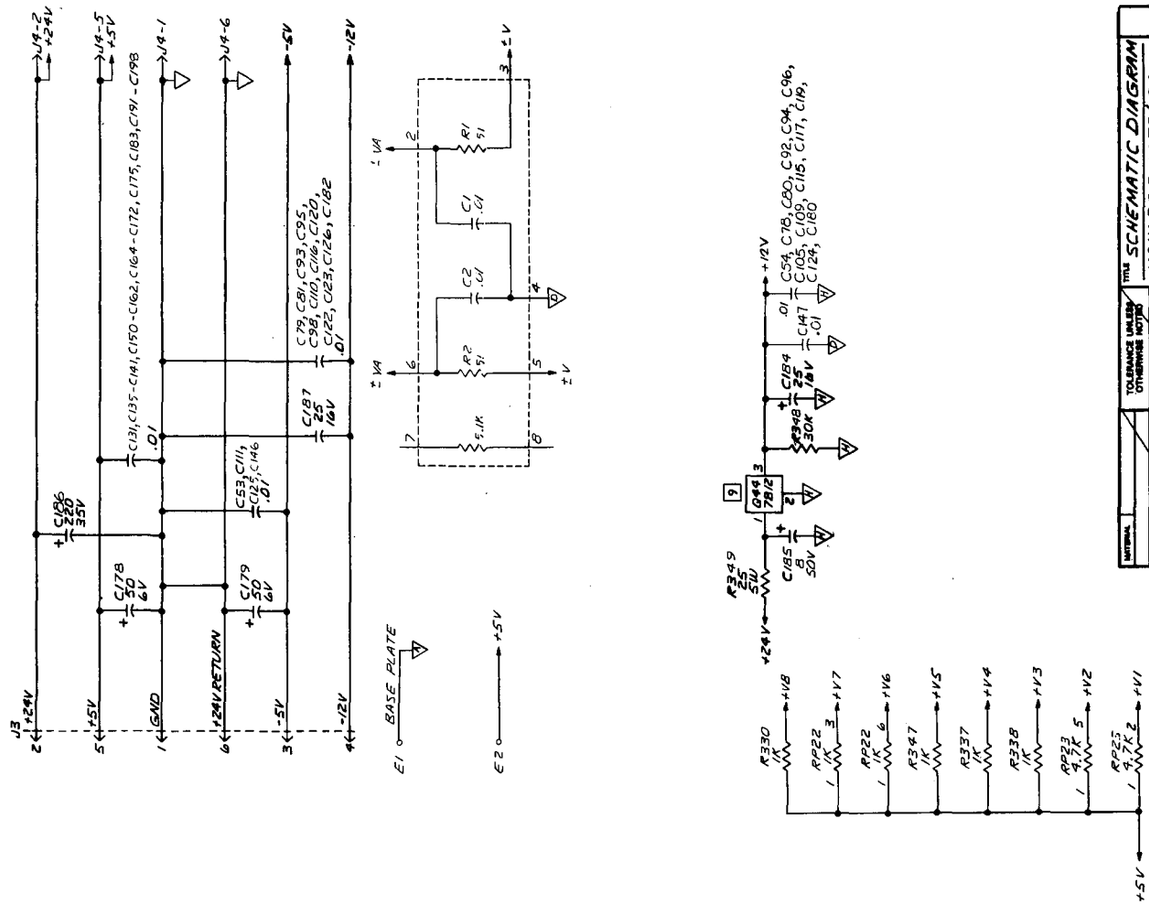
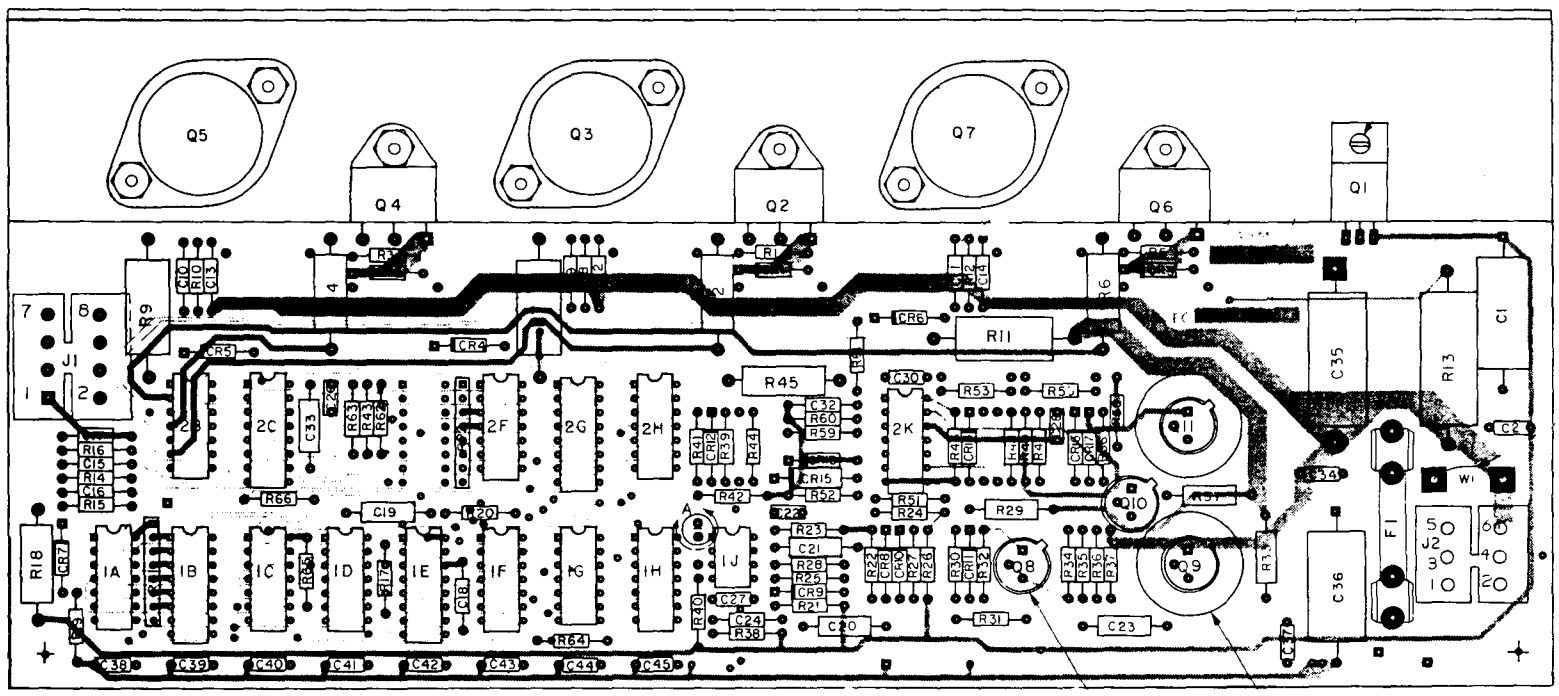

SCHEMATIC DIAGRAM
MAIN P.C.B. 6650/B4
200099
BASE PLATE
+24V RETURN
GND
+24V
+5V
-5V
-12V



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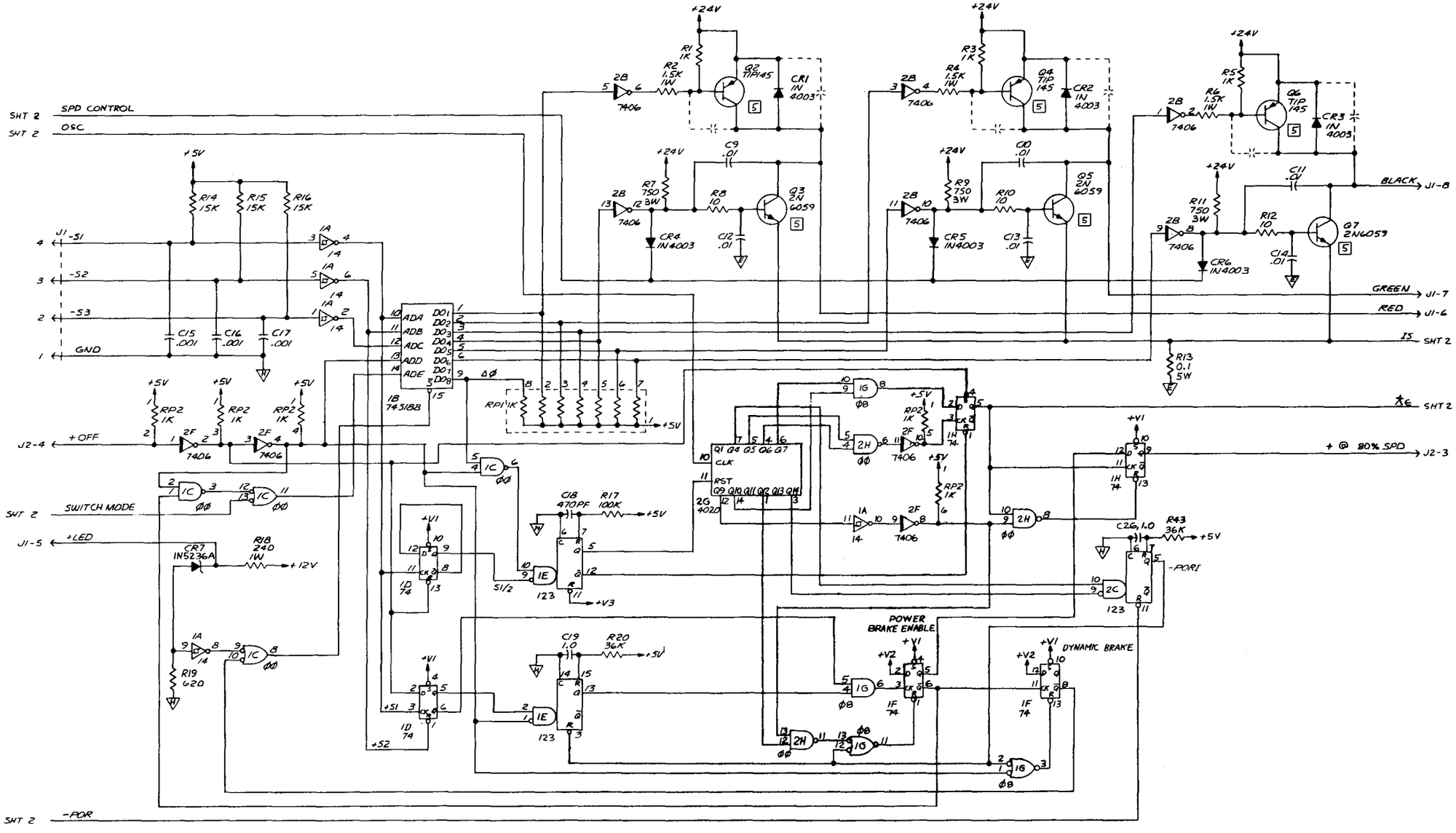
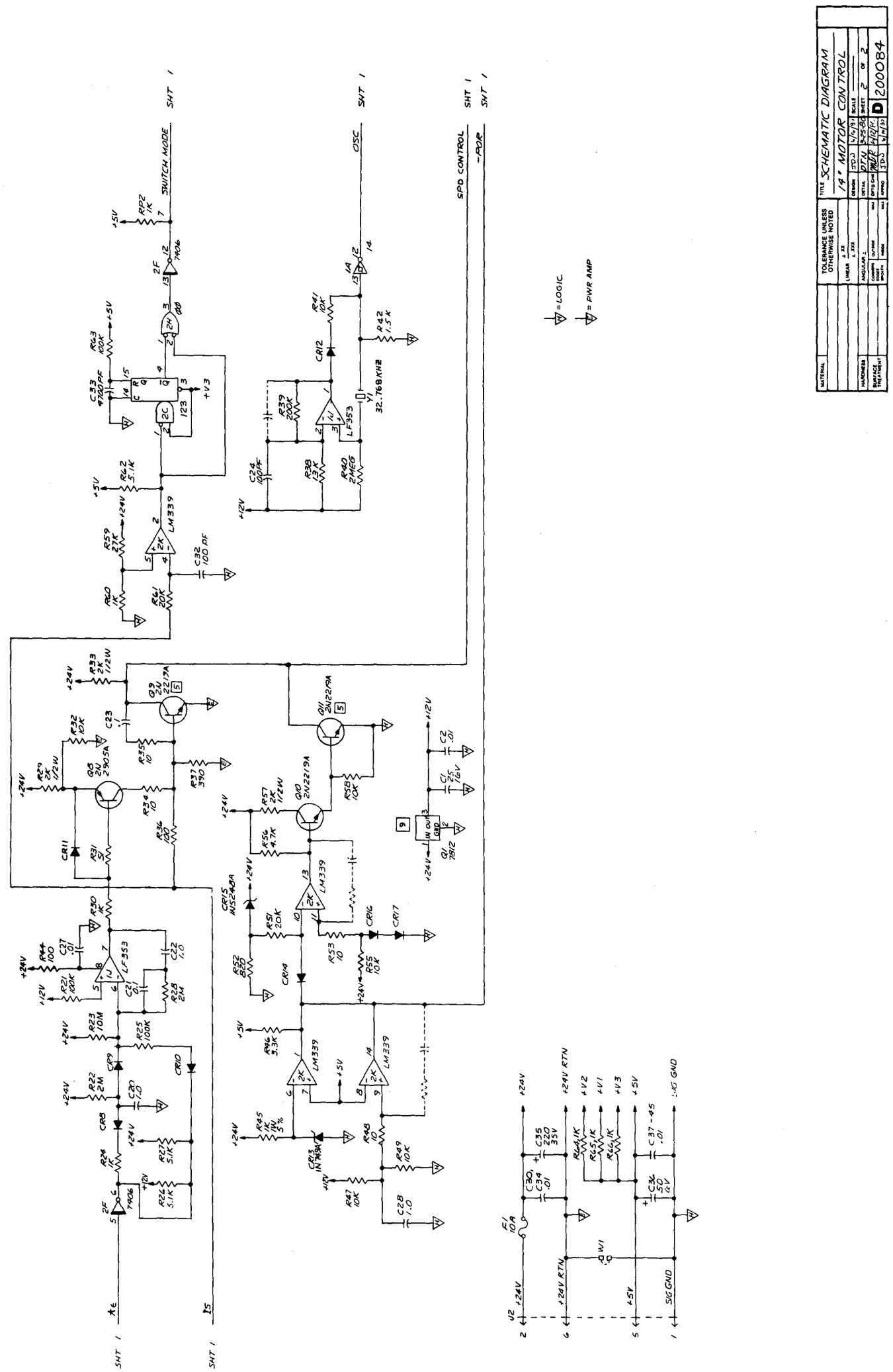


MATERIAL	TOLERANCE UNLESS OTHERWISE NOTED	TITLE SCHEMATIC DIAGRAM	
	LINEAR ± XX, ± XXX	14" MOTOR CONTROL	
HARDNESS	ANGULAR ±	DESIGN JDW 6/14/93 SCALE —	
SURFACE TREATMENT	CORNERS (EDGES BROKEN) OUTSIDE MAX, INSIDE MAX	DETAIL DTW 3-25-93 SHEET 1 OF 2	
		DFTG CHK MDR 6/14/93 D 200084	
		APPRO JDW 6/14/93	

Reference Only - Will Not Be Maintained



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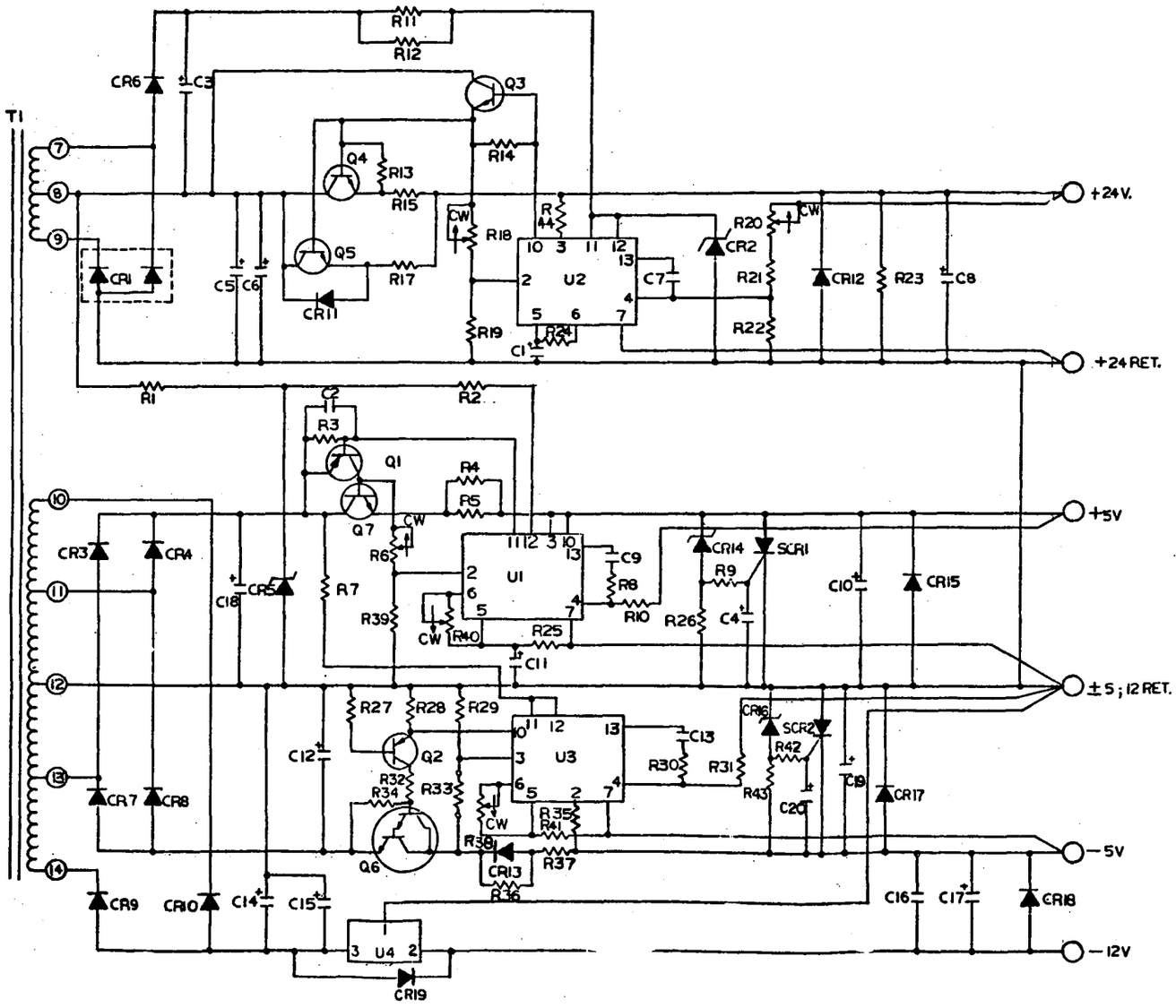


C3	47/50	CAPACITOR ALUM ELECT
C1,4,11,17,20	10/25V	CAPACITOR ALUM ELECT
C2	.1/100V	CAPACITOR MYLAR
C18	16,000/15V	CAPACITOR ALUM ELECT
C5,6	3,700/60V	〃
C8	330/35	〃
C10,19	220/16V	〃
C12	9,000/15V.	〃
C14,15	330/35V	〃 ALUM ELECT
C9,13,16	.01/100V	CAPACITOR MYLAR
CR1	R7111A	DIODE BRIDGE
CR2	IN973B	DIODE ZENER
CR5	IN965B	DIODE ZENER
CR14,6	IN753A	DIODE ZENER
CR3,4	MR750	DIODE 2.2A. 50V.
CR6,9,10,15,17,18,19	IN4003	DIODE 1A. 200V.
CR7,8,13	AE3B	DIODE 3A. 100V.
CR11,12	IN4003	DIODE 1A 200V
SCR1,2	S0508 LS3	SCR 50V. 3A.
C7	.001/100V	CAPACITOR MYLAR
Q1	2N6554	TRANSISTOR PNP
Q2	2N2907A	TRANSISTOR
Q3,4,5	2N3055	TRANSISTOR
Q7	2N3771	TRANSISTOR
Q6	2N6055	TRANSISTOR
U1,2,3	MP723	I.C VOLTAGE REGULATOR
U4	MP7912	I.C VOLTAGE REGULATOR
R33	270Ω	RESISTOR ½W 5% CF
R1,13,14,29,23	2.2K	RESISTOR ½W 5% C.F.
R2,30,34	330Ω	〃
R3,10,27,31,34,35	1K	〃
R78,26,28,32,43	82Ω	〃
R9,42,44	6.8Ω	〃
R11,12	7.5K	〃
R19	10K	〃
R36	2.7Ω	½W 5% C.F
R21	2.7K	RESISTOR ½W 2% M.F
R22	1.6K	RESISTOR ½W 2% M.F
R25,41	2.4K	RESISTOR ½W 2% M.F
R39	2.2K	RESISTOR ½W 5% C.F
R37	.1Ω	RESISTOR 2W BWH
R6,18,20,38,40	2K	POTENTIOMETER
R4,5,15,17	.12Ω	RESISTOR 2W BWH
P.C.B	17053	PRINTED CIRCUIT BOARD

QTY REQ	ITEM	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

PARTS LIST

TOLERANCE .XX = .030 .XXX = .010

CONTRACT NO.

APPROVALS	DATE
DRAWN MCCARTHY T.S.	4-26-79
CHECKED	
ENG APP.	
APPROVED	

MATERIAL

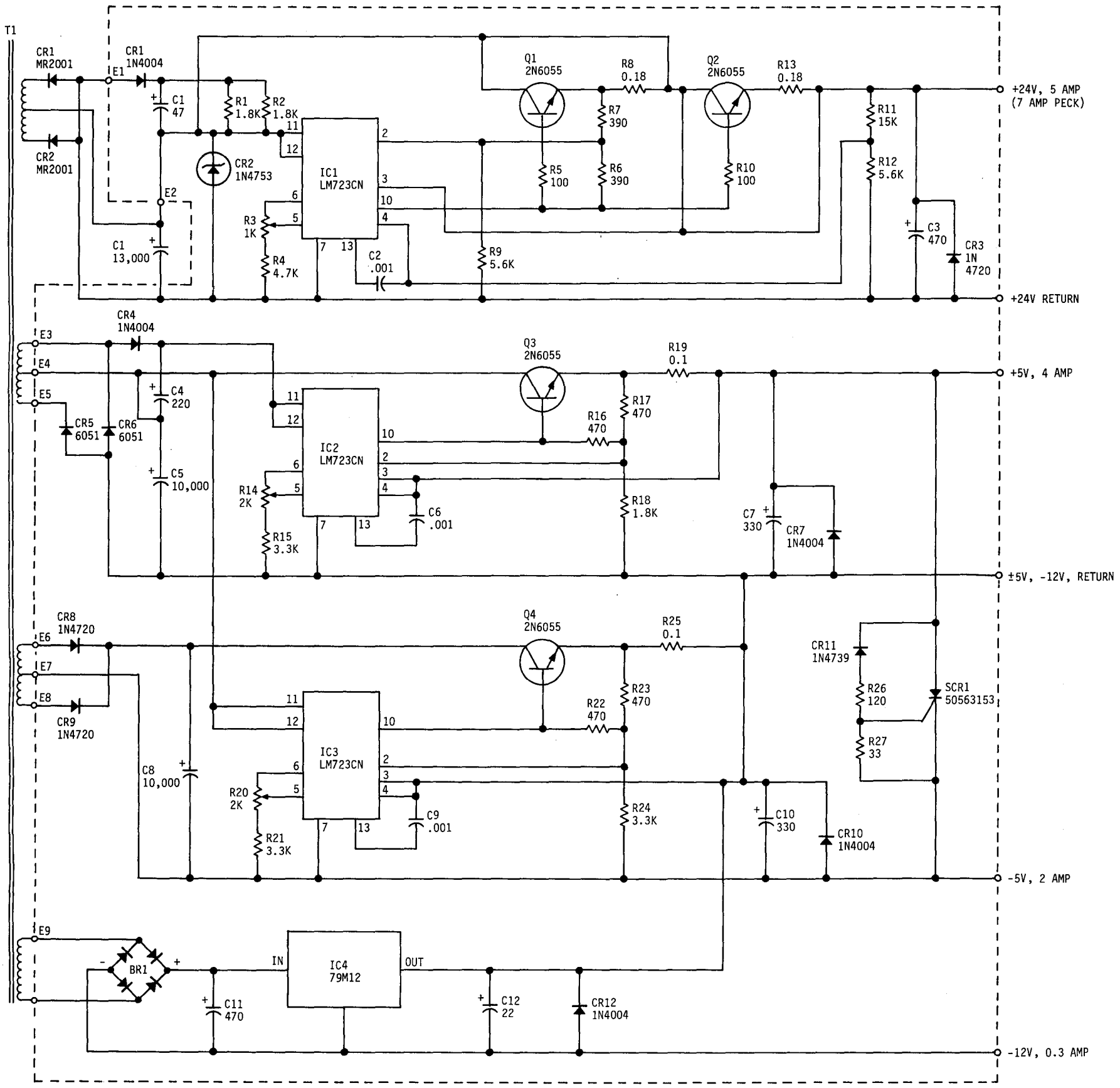
FINISH

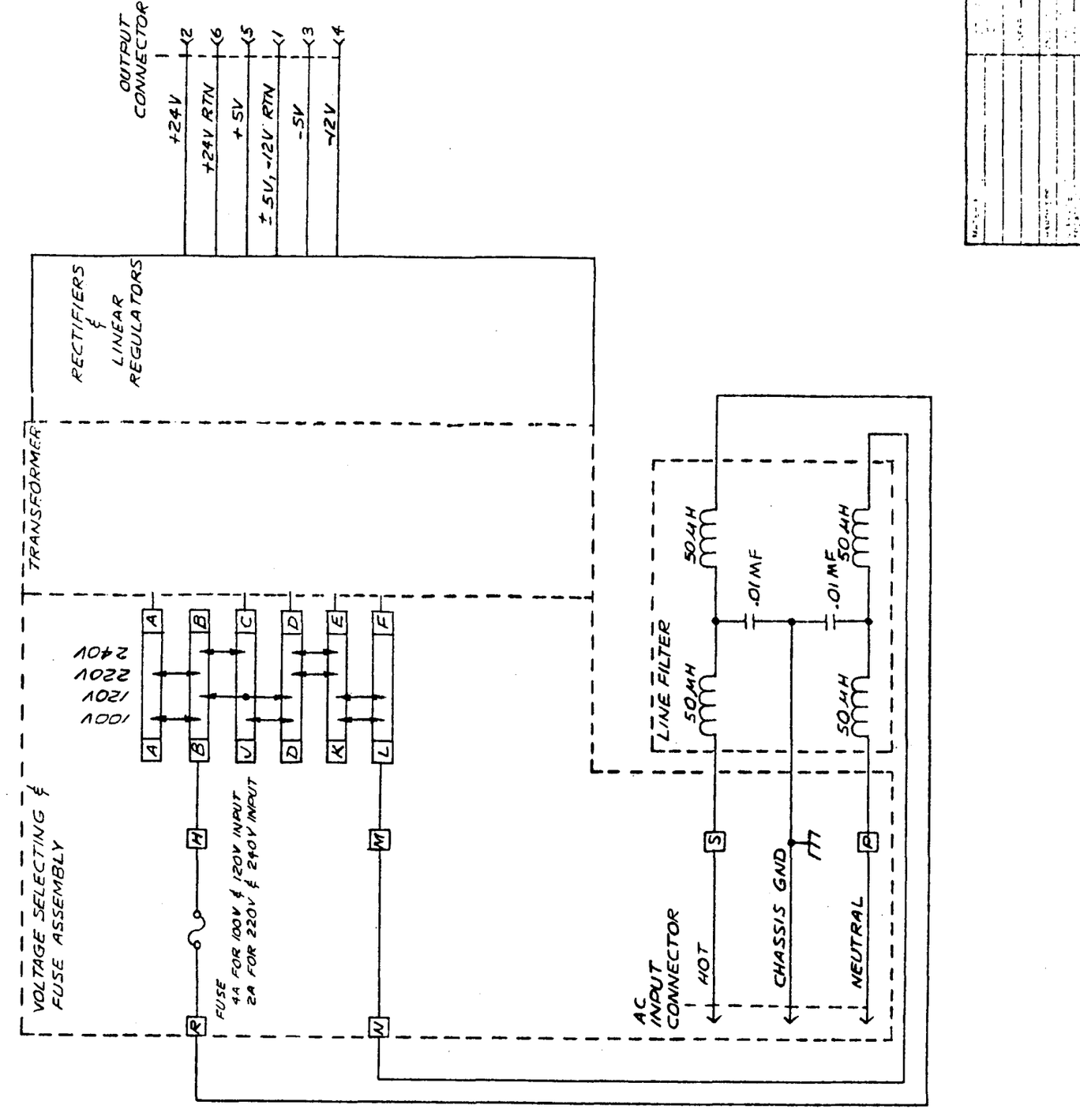
DO NOT SCALE DRAWING

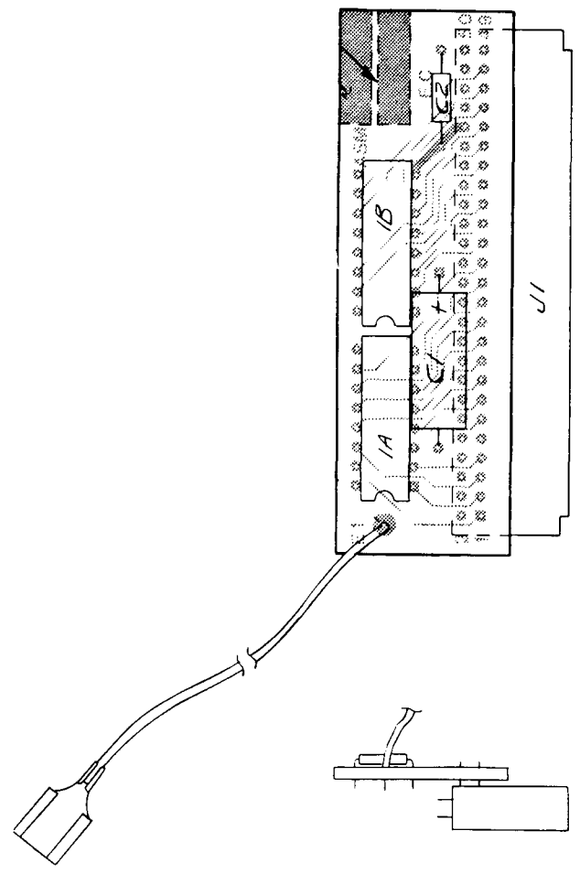
TITLE: SCHEMATIC, POWER SUPPLY

SIZE	CODE IDENT NO.	DRAWING NO.	
D	54407	17048	G

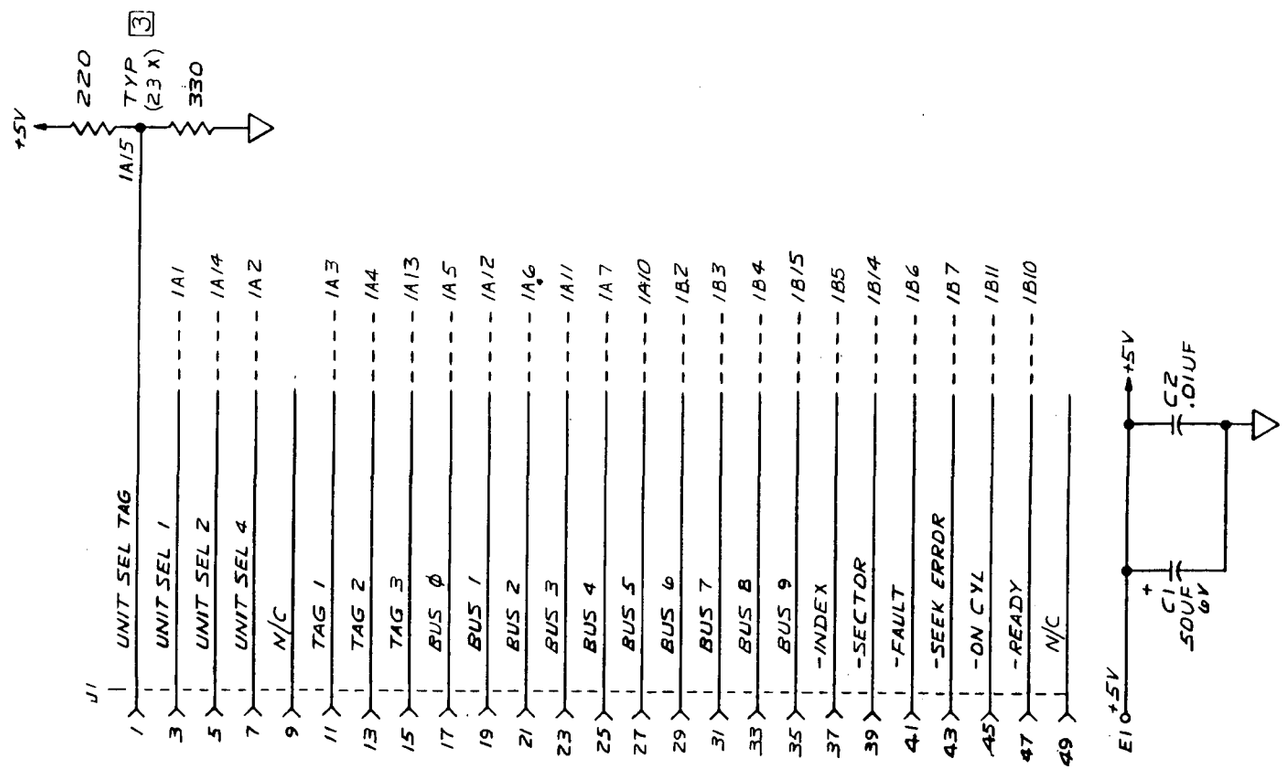
SCALE — SHEET 1 OF 1


T1
CR1
MR2001
CR1
1N4004
E1
C1
47
R1
1.8K
R2
1.8K
CR2
MR2001
CR2
1N4753
E2
C1
13,000
IC1
LM723CN
R3
1K
R4
4.7K
C2
.001
Q1
2N6055
R8
0.18
R7
390
R5
100
R6
390
Q2
2N6055
R13
0.18
R10
100
R11
15K
R12
5.6K
C3
470
CR3
1N
4720
+24V, 5 AMP
(7 AMP PECK)
+24V RETURN
R9
5.6K
CR4
1N4004
E3
E4
E5
CR5
6051
CR6
6051
C4
220
C5
10,000
IC2
LM723CN
R14
2K
R15
3.3K
C6
.001
Q3
2N6055
R19
0.1
R16
470
R17
470
R18
1.8K
+5V, 4 AMP
C7
330
CR7
1N4004
±5V, -12V, RETURN
CR8
1N4720
E6
E7
E8
CR9
1N4720
C8
10,000
IC3
LM723CN
R20
2K
R21
3.3K
C9
.001
Q4
2N6055
R25
0.1
R22
470
R23
470
R24
3.3K
CR11
1N4739
R26
120
R27
33
SCR1
50563153
C10
330
CR10
1N4004
-5V, 2 AMP
E9
BR1
IN
IC4
79M12
OUT
C11
470
C12
22
CR12
1N4004
-12V, 0.3 AMP


SCHEMATIC DIAGRAM
3350 FILTERED POWER SUPPLY
330357
AC INPUT CONNECTOR
HOT
CHASSIS GND
NEUTRAL
LINE FILTER
50μH
.01 MF
VOLTAGE SELECTING & FUSE ASSEMBLY
100V
120V
220V
240V
FUSE
4A FOR 100V & 120V INPUT
2A FOR 220V & 240V INPUT
TRANSFORMER
RECTIFIERS & LINEAR REGULATORS
OUTPUT CONNECTOR
+24V
+24V RTN
+5V
±5V, -12V RTN
-5V
-12V



MATERIAL	SEE B/M	TOLERANCE UNLESS OTHERWISE NOTED		TITLE ASSEMBLY DRAWING			
200138				84 TERMINATOR			
		LINEAR ± XX —		DESIGN KMS 9-8-80	SCALE 2/1		
		± XXX —		DETAIL BTW 9-12-80	SHEET 1 OF 1		
HARDNESS		ANGULAR ± —		DFTG CHK MJOR 8-13-80	C	200138	
SURFACE TREATMENT		CORNERS EDGES BROKEN	OUTSIDE — MAX INSIDE — MAX	APPRO KMS 9-8-80			



MATERIAL	TOLERANCE UNLESS OTHERWISE NOTED	TITLE SCHEMATIC DIAGRAM			
	LINEAR ± .XX ± .XXX	B4 TERMINATOR			
	ANGULAR ±	DESIGN [illegible] 9-8-80	SCALE ———		
HARDNESS		DETAIL WJM 7-14-80	SHEET 1 OF 1		
SURFACE TREATMENT	CORNERS EDGES BROKEN OUTSIDE MAX INSIDE MAX	DFTG CHK MDR 7-14-80	C	200139	
		APPRO [illegible] 9-8-80			

APPENDIX

DISC CONTROLLER

FOR

MODEL 2460

FIXED MEDIA DISC DRIVE

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APPENDIX A

SECTION 1

INTRODUCTION

A1.1 GENERAL DESCRIPTION

The Disc Controller provides the interface between the CPU and Disc Drive. It interfaces the 2460 Fixed Media Disc Drive to a Basic Four data processor in a system configuration. See Figure A-1 for a typical system interconnect diagram.

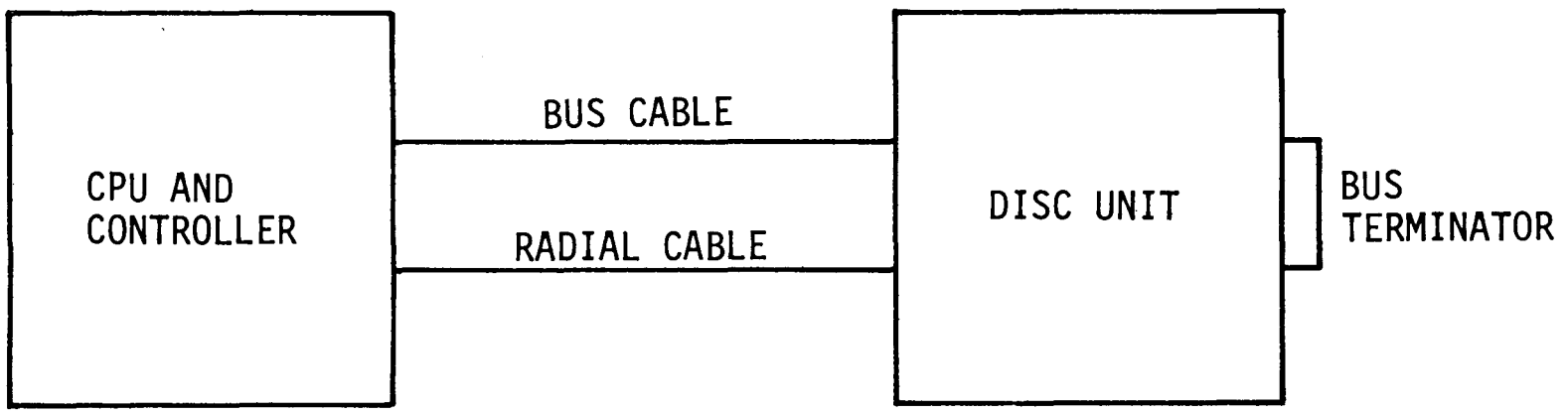
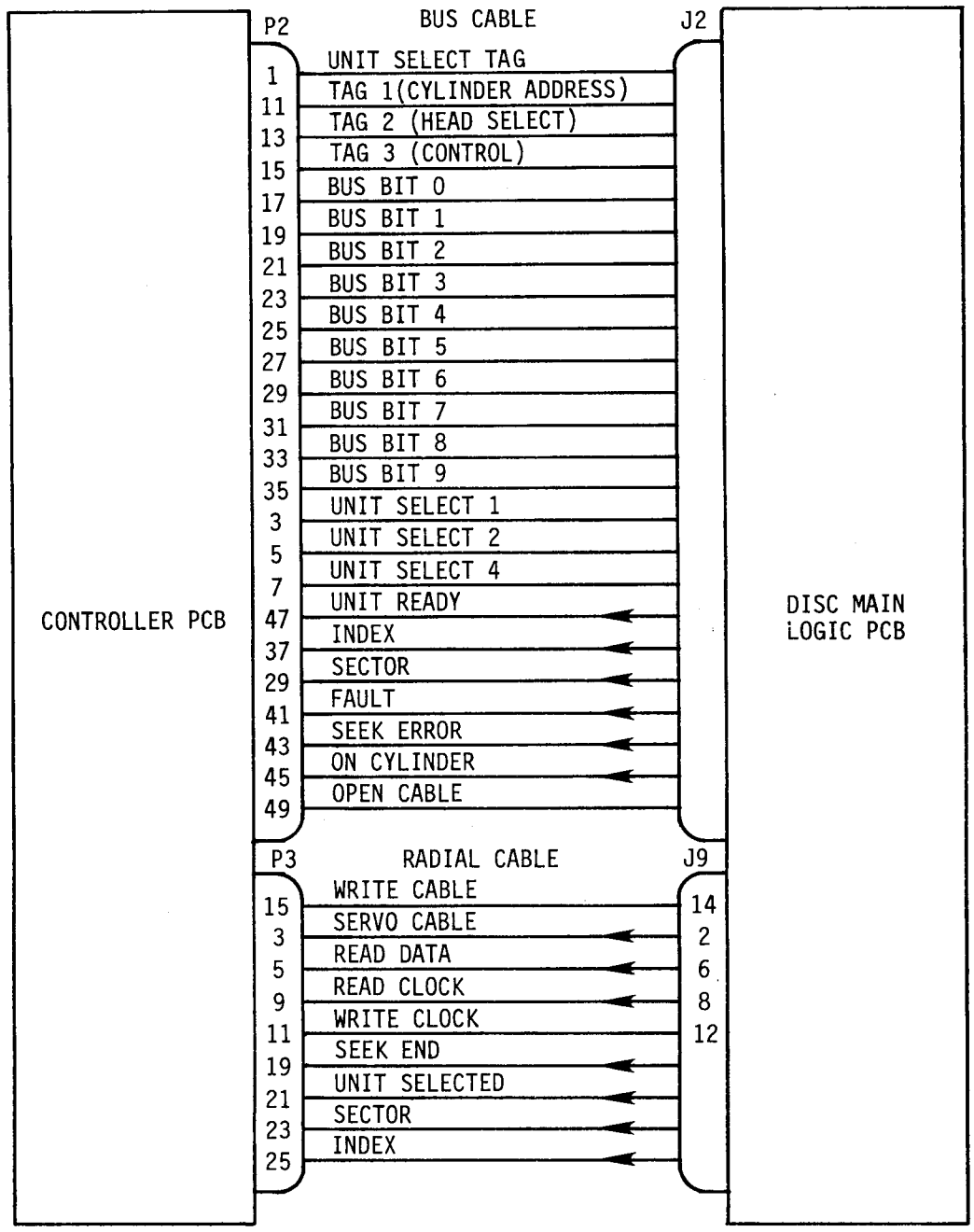


Figure A-1. System Interconnection

A1.2 PHYSICAL DESCRIPTION

The Disc Controller, hereafter referred to as the Controller, is a single PCB plugged directy into the main card cage of the processor system. Two cables (Radial Cable, P/N 902622 and Bus Cable, P/N 902687) connect the controller to the Disc Drive. A complete pin to pin listing of these cables is given in Figure A-2.



BUS BIT	TAG 1 CYLINDER ADDRESS	TAG 2 HEAD SELECT	TAG 3 CONTROL
0	1	1	WRITE GATE
1	2	2	READ GATE
2	4	4	
3	8	8	
4	16		FAULT CLEAR
5	32		
6	64		REZERO
7	126		
8	256	1024*	
9	512	2048*	READ STATUS

*USED FOR HIGH ORDER CYLINDER ADDRESS DURING TAG 2 TIME

Figure A-2. Disc Interface and Tag Bus Decode

A1.3 PHYSICAL REQUIREMENTS

A1.3.1 PHYSICAL ENVELOPE

The Controller is housed on a standard Basic Four printed circuit board (PCB) with all connectors and components mounted thereon.

A1.3.2 MOUNTING

The Controller is installed in the card cage of a standard Basic Four data processing system. All clearances and airflow provisions normal to the Basic Four system are observed.

A1.4 DATA RELIABILITY

The data reliability of the Controller is subject to the data reliability limits of the disc unit. These limits are:

1. Soft Error Rate (Recoverable Errors) - Not more than one error in 10^{10} of bits of data transferred.

2. Hard Error Rate (Non-Recoverable Errors) - Not more than one error in 10^{13} bits.

SECTION 2

MAINTENANCE

A2.1 GENERAL DESCRIPTION

Maintenance of the Controller is limited to replacement of the Controller. This section will explain the Controller function only as an aid to the Service Representatives in troubleshooting.

A Functional Block Diagram is given in Figure 3-1 and described below.

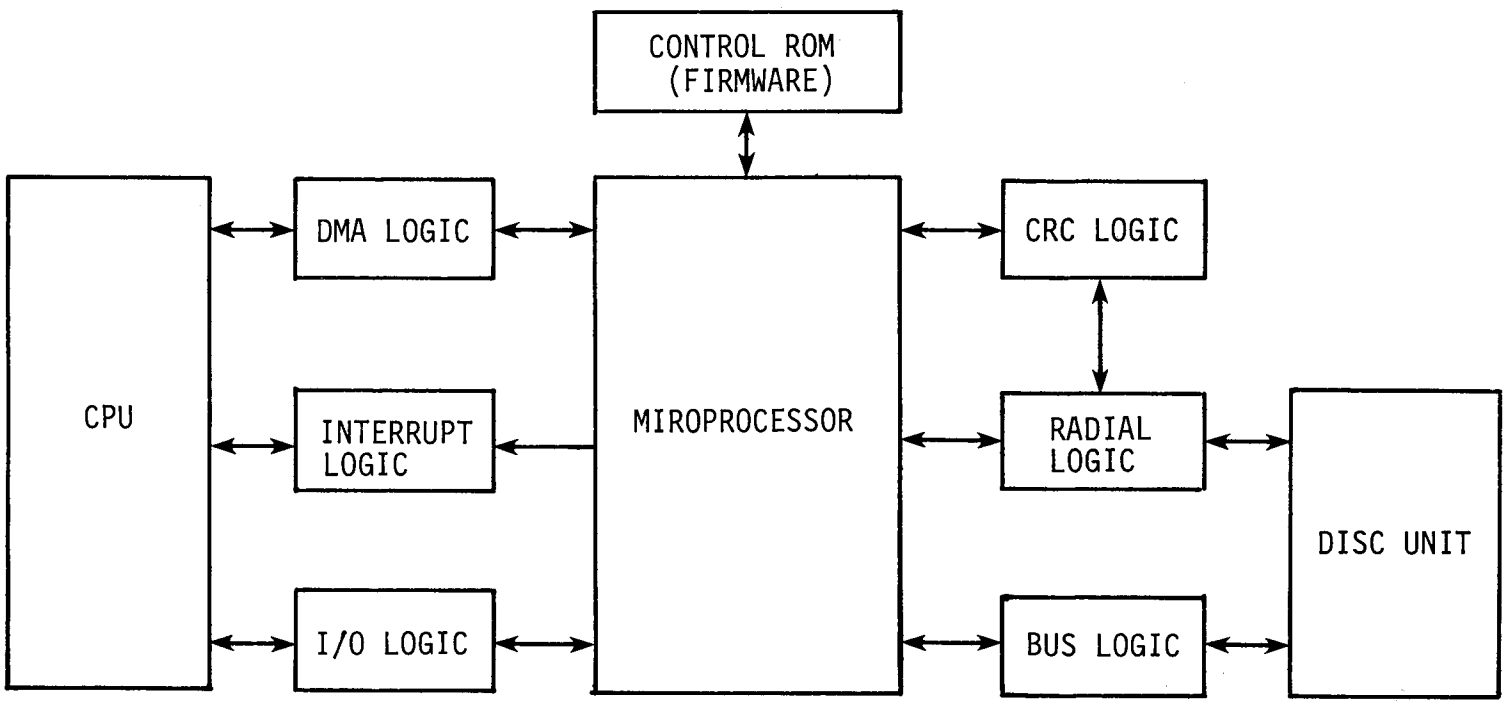


Figure A-3. Block Diagram of Controller

A2.1.1 CONTROLLER ROM

The Control ROM (FIRMWARE) automatically initiates the following:

1. The Reset Routine.
2. The Idle Loop.
3. The Transfer Preparation Routine.
4. Search ID Routine.

A2.1.2 MICROPROCESSOR

The Microprocessor initiates, tests, or controls the entire operations of the Controller as specified by firmware.

The Microprocessor does three things for each instruction cycle: it executes the present instruction (function), it fetches the next instruction, and it computes the next fetch address, next address, and stack logic.

The Microprocessor does the following:

1. Translate I/O commands issued by the CPU into commands that the Disc Drive recognizes.
2. Performs error checking of information passed between Disc Drive and CPU.
3. Detects particular conditions and then issues interrupt commands to the CPU.
4. Provides Controller and Disc Drive status information to the CPU.
5. Implements Direct Memory Access (DMA) transfer between Disc Drive and Main Memory.
6. Sychronizes timing.

A2.1.3 DMA LOGIC

The DMA Logic consists of the following:

1. DMA Interface Logic.
2. DMA Read/Write Cycle.
3. DMA Priority.

A2.1.4 INTERRUPT LOGIC

The Interrupt Logic consists of a mask F/F and an interrupt F/F. If the mask F/F is set and the interrupt F/F is set, an interrupt will be sent to the CPU (DMAINT-).

A2.1.5 I/O LOGIC

The I/O interface logic provides flags used for branch offset by the microprocessor. These flags are part of the command word which comes from the CPU or flags which indicate valid data is on the output data lines.

A2.1.6 CRC LOGIC

The CRC Logic is responsible for generating and checking the cyclic redundancy check bytes for the header and data records on the disc.

A2.1.7 RADIAL LOGIC

The Radial Interface Logic is responsible for the assembly/disassembly of the disc serial DATA1. It provides flags for branch offsets to indicate to the microprocessor when each process has been completed.

A2.1.8 BUS LOGIC

The Disc Bus Interface Logic sends commands to the disc drive and receives FAULT, SKERR, READY, ONCLY, SCTR, and INDEX from the drive.

A2.2 INTERFACE REQUIREMENTS

A2.2.1 ELECTRICAL INTERFACE

1. Signal Levels - All signals will be at standard TTL levels.

   0.1 to +04 VDC equals logical low

   +2.4 to Vcc VDC equals logical high

   The clock and data lines to the disc are differential balanced line drivers/receivers.

2. Termination - All TTL signals that pass through lines exceeding 2 feet in length are terminated with 220 Ohm pull-up and 330 Ohm pull-down resistors.

3. Drivers/Receivers - All TTL line drivers are 7438 or equivalent line drivers. All interface receiver lines are standard TTL input.

A2.2.2 CPU INTERFACE

The CPU Interface signals are as follows:

1. Master Reset

2. Clock Phase 1 and 2

3. I/O Control Registers 1 thru 3

4. Output Data Bits 0 thru 7

5. Memory Address Bits 0 thru 14 and DMA Memory Address Bit 15

6. Memory Data Bits 0 thru 7

7. DMA Acknowledge

8. DMA Request

9. DMA Interrupt

10. Read Enable

SECTION 3

GLOSSARY OF SIGNAL NAMES

A3.1 GLOSSARY

16WAY — This output of the next address control ROM is used to indicate that a 16-way branch is required.

ADDEN — This signal is generated by the DMA control logic and is used to gate the contents of the DMA address counter onto the main frame memory address bus. This signal is true throughout any DMA cycle.

BOX — X = 0 to 7. These are the outputs of the D-register. The D-register is used to buffer data until it can be written into its destination.

BINDX — This signal is the synchronized and buffered version of the index signal from the disc. This synchronization is necessary to prevent a metastable flip-flop in the address logic for the processor.

BRDY — This signal is the synchronized and buffered version of RDY. This synchronization is necessary to prevent a metastable flip-flop in the next address logic.

BSCTR — This signal is the synchronized and buffered version of the logical OR of the index and sector signals from the disc. This synchronization is necessary to prevent a metastable flip-flop in the address logic for the processor.

BYTE — This signal is generated by the bit counter on each eighth bit during a data transfer to determine the byte boundaries.

CHCLK — This signal is used by the processor to control the clock changeover logic. In addition to loading the least significant bit of the processor output bus into the clock control flip-flop, this signal initates the series of events necessary to insure a smooth changeover from one clock to another.

CLKEN — This is a test signal that is used to gate the processor clocks on and off for testing and single cycle operation with the WCS.

CLRCRC — This signal is used by the processor to reset the CRC generator/checker.

CLTAG — Set Cylinder Tag. This signal is used by the disc unit to determine that the information on the disc control bus in cylinder address information.

CPHX — X = 1 or 2. These are timing clocks from the CPU. The controller runs from these clocks during read data operations and at all other times except during a write data operation.

CRC — This signal switches the CRC data into the serial write data stream. This signal is enabled by CRCENB.

CRCDTA This is the serial CRC information that is generated by the CRC chip for a write operation.

CRCENB This signal is used during write data transfers to enable the writing of the CRC. This signal is directly controlled by the processor.

CRCERR This signal is generated by the CRC chip to indicate that the CRC that was read in was in error.

CRY This is the raw carry output of the 2901.

CRYIN This signal is controlled by the ROM and is used to gate one, zero or carry saved into the carry input of the 2901.

CRYSAV This is the saved output of the carry output from the 2901 to be used for testing, carries, or shift operations in the next processor cycle.

CTTAG Control Tag. This signal is used by the disc unit to determine that the information on the disc control bus is control information.

DATAEN This signal is used by the DMA control logic to gate the contents of the D-register onto the main frame memory data bus. This signal is true throughout a DMA cycle only when the controller is performing a disc data read operation.

DBX X = 0 thru 7. This is the processor data input bus.

D[illegible]K Disc Generated Clock. This clock is either the disc servo clock or the disc read clock as the occasion demands.

DECCNT This signal is used by the processor to decrement the general counter and test for zero result.

DFLAG This is the synchronized output of the D-flag. The synchronization is necessary to prevent a metastable flip flop in the address logic for the processor.

DFLG This is the raw output of the D-flag. This flag is set at any time that the D-register is loaded, and cleared when data is read from the D-register.

DIXX This signal in the I/O control logic is true when IOACTV is true and the controller detects the DIXX command from the CPU. This signal is used to transfer data from the controller to the CPU.

DKBSX X = 0 thru 9. These are the disc control bus signals. The information on this bit is used by the disc unit as either control information, head addresses, or as a cylinder address.

DMX X = 0 thru 7. This is the outputs of the S-register that are directed to the processor input.

DMA15 This is the most significant address bit from the DMA address logic to the memory page control in the CPU. This bit is converted to the appropriate page control bits in the CPU.

DMACK DMA Acknowledge. This signal from the CPU is used to determine that the current DMA request has been granted, and the next memory cycle belongs to the DMA logic.

DMAINT This is the DMA interrupt request line in the CPU backplane.

DMAQ This is the output of the DMA request latch. This signal is true any time that the processor wants to initiate a DMA cycle.

DMAR This is the DMA request bus signal on the CPU backplane.

DMASTB DMA Strobe. This signal is generated by the DMA interface control logic. This signal is true during the last third of the DMA cycle, and is used to strobe read data into the controller and to advance the address counter.

DOXX This signal in the I/O control logic is true any time that the signal IOACTV is true and the DOXX command is detected from the CPU. This signal is used to transfer data from the CPU to the controller.

DTAX X = 0 thru 7. This is the output from a multiplexer that can switch from either the shift register or the memory data bus into the S-register.

E/INSYC Enable INSYNC. This signal is controlled by the processor and is used by the processor to control the state of the INSYNC flip-flop.

FAULT This signal from the disc unit is used to determine that the disc unit has detected a condition that could lead to the destruction of data . The disc is therefore interlocked from further data transactions.

FX X = 0 thru 7. This is the processor output bus. The data on this bus is moved from the processor to any of several destinations.

HTAG Set Head Tag. This signal is used by the disc unit to determine that the data on the disc control bus is head address information.

IDOX X = 0 thru 7. This is the CPU input bus. This bus is used to transfer information from the controller to the CPU.

INDEX This signal from the disc unit is used to indicate that the heads are currently positioned over the beginning of the track which is also the beginning of sector zero.

INSYNC Literally "In Sync". The state of this flip-flop is used to permit data flow when the bit counter is in sync with the data flow.

INT This signal in the DMA interrupt logic is used to interrupt the CPU any time this signal is true and MASK is also true.

IONX N = 1 thru 3. These are the I/O control signals from the CPU. By decoding these bits, the appropriate I/O action can be determined.

IOACTV This signal in the I/O control logic is true any time that the c troller detects its address in conjunction with a COXX command. signal remains true for the duration of the I/O transfer.

LDADRH Load the High Address Register. This signal is used by the proc to strobe the contents of the processor output bus into the uppe byte of the DMA address counter.

LDADRL Load Lower Address Register. This strobe is used by the process to strobe the contents of the processor output bus into the lowe byte of the DMA address counter.

LDBREG Load the Buffer Register. This signal is used during data trans to load the D-register from either the memory or the disc, deper on the direction of data flow.

LDCLB This signal is used by the processor to load the contents of the processor output bus into the lower byte of the general counter.

LDCMB This signal is used by the processor to load the contents of the processor output bus into the high byte of the general counter.

LDDREG This is a strobe generated by the processor that is used to load contents of the processor into the D-register.

LDLDB Load Lower Disc Bus Control Register. This strobe which is gene by the processor is used to clock the contents of the processor put bus into the lower disc bus control register.

LDPC This signal is used by the processor to control the contents of control ROM page control flip-flop.

LDSR Load the Shift Register. This signal is used during the write c ation to parallel load the shift register with data.

LDSTAT This signal is used by the processor to strobe the contents of t processor output bus into the status register.

LDUDB Load Upper Disc Bus Control Register. This strobe is generated the processor and is used to clock the contents of the processor output bus into the upper disc control bus register.

LSHFT This signal is used by the processor to control the inputs to th shift registers in the 2901 for a left shift operation.

MAXX XX = 00 thru 14. These are the main frame memory address lines.

MASK This signal in the DMA interrupt logic is used to enable the DMA interrupt request line to the CPU.

MDOX X = 0 thru 7. This is the unbuffered memory bus from the main f memory. This is a bi-directional data bus.

MIDCY This signal generated by the DMA control logic, is used to indicate that the middle third of a DMA data transfer is now in progress.

MRST This is the master reset signal from the CPU backplane.

MUXN N = 1 or 2. These are the raw clocks that are used to generate the signals T0 and T1. During clock changeover, these signals may contain truncated clocks.

NAX X = 0 thru 3. These signals form the least significant four bits of the next processor address. Since many different signals may be gated into these bus, this forms the basis for N-way branches.

ODOX X = 0 thru 7. These are the output data lines from the CPU. This information is used to determine the controller address or to transfer data from the CPU to the controller.

OFL This is the raw overflow status bit from the 2901.

OFLSAV This is the saved overflow bit form the 2901 to be used for testing in the next processor cycle.

ONCYL This signal from the disc unit indicates that the disc unit is on a cylinder and not seeking.

OUTEN Output Enable. This signal is used to disable the disc bus output lines when the controller is first powered up. This is to prevent the random control information contained in the registers from cauing the disc unit to force a fault. Once the registers assume a known state, this signal can be enabled.

POP This signal is used to indicate that the next address for the processor instruction will come from the contents of the address stack register.

Q0 This is the I/O line for bit 0 of the Q-register in the 2901. Whether this line is an input or an output is determined by whether there is a right or left shift operation in progress.

Q0SAV This is the saved output of the Q0 bit in the 2901 to be used for right shift operations in the Q-register.

Q7 This line is the I/O for bit 7 of the Q-register in the 2901. Whether this line is an input or an output is dependent on the type of shift operation in progress.

Q7SAV This is the saved output of bit 7 of the Q-register to be used in left shift operations for the Q-register in the 2901 in the next processor cycle.

R0SAV This is the save output of RAM bit 0 in the 2901 to be used in left shift operations in the RAM.

R7SAV This is the saved output of RAM bit 7 from the 2901 to be used in left shift operations in the next processor cycle.

RADX — X = 0 thru 8. These are the ROM address bits used to fetch the next instruction from the control ROM for the processor.

RAM0 — This is the input/output line for RAM bit 0 in the 2901. Whether this line is an input or an output is determined by the type of shift operation that is in progress.

RAM7 — This is the I/O line for RAM bit 7 in the 2901. Whether this line is an input or an output is determined by the type of shift operation that is in progress.

RCLKX — X = H or L. These are the differential balanced line signals from the disc that carry the read data clock. When the read gate is asserted, this signal may be used to clock data in from the disc unit.

RDATA — This is the received read data from the disc unit. The data takes the form of serial NRZ data that is clocked in using the read clock.

RDCLK — This is the received read clock from the disc unit. This clock is used to time the flow of data from the disc unit to the controller during a read data operation.

RDDLB — Read the Lower Disc Bus Control Register. This strobe generated by the processor is used to gate the contents of the lower disc bus control register into the processor data input bus.

RDDMX — This signal is used in the data bus control logic to enable the output of the data mux onto the processor data input bus.

RDDUB — Read Disc Upper Bus Control Register. This strobe is generated by the processor and is used to gate the contents of the upper disc bus control register into the processor data input bus.

RDFLAG — Reset the D-flag. This signal is used to reset the D-flag whenever necessary.

RDTAX — X = H or L. These are the differential balanced line signals that carry read data from the disc unit to the controller.

RDY — This signal is the logical OR of the ready and on cylinder signals from the disc unit. When this signal is true, a data transfer may occur.

READ — This flag is controlled by the processor. It is used to control the flow of data from the disc unit to the memory.

READY — This signal from the disc unit is used to determine that the disc unit is rotating and up to speed, and no fault exists.

RINT — This signal is used by the processor to reset the MASK and INT flip-flops.

ROXX — XX = 00 thru 25. These are the raw ROM outputs that feed the inputs of the instruction pipeline register. These bits are not used anywhere else since it is the output of the pipeline register that is used while the next instruction fetch is in progress.

ROMXX XX = 00 thru 25. These are the outputs of the ROM pipeline buffer that contains the instruction for the 2901 part of the processor. This buffer is loaded on the rising edge of TO.

ROMYY YY = 26 thru 39. These are the raw ROM output bits that are used directly in the next address computation logic. The results of the next address computation are strobed into the address register at the rising edge of TO.

RSHFT This signal is used by the processor to control the inputs to the shift registers in the 2901 for a right shift operation.

RST This signal is the controller reset from the system. It is used to reset all of the important functions in the controller for power-on or for the bootstrap.

RTXX This signal generated by the DMA transfer logic is used to indicate that the first third of a DMA transfer cycle is underway.

SADDEN This output of the DMA control ROM is used to set the address enable flip-flop on the next clock edge.

SCLK This is the received servo clock from the disc unit. This clock is used to time the flow of data from the controller to the disc unit during a write data transfer. The clock is also re-transmitted to the disc unit.

SCLKX X = H or L. These are the differential balanced line signals for the disc servo clock. This clock is always kept in sync with the servo pattern on the disc surface.

SCTR Sector. This signal from the disc unit indicates that the heads are currently positioned over the beginning of any sector except sector zero.

SDFLAG This signal is used to set the D-flag any time that the D-register is loaded from the processor.

SDMAQ This signal is used by the processor to set the DMA request latch.

SDMST This output of the DMA control ROM is used to set the DMA strobe flip-flop on the next clock edge.

SERIN This is serial data that has been read from the disc. This signal is zero at all times when the read flag is not set.

SEROUT Serial output of the parallel to serial shift register.

SETS5 Set the S-flag On the Count of 5. This term is used to set the S-flag during read operations in anticipation of loading data into the S-register so that by the time that the processor responds to the S-flag, the data will be there.

SFLAG This is the synchronized and buffered output of the S-flag. The synchronization is necessary to prevent a metastable flip-flop in the address logic for the processor.

SFLG This is the raw output of the S-flag flip-flop. The S-flag is set when data is loaded into the S-register, and cleared when data is read from the S-register.

SGNSAV This is the saved output of the sign bit from the 2901 to be used for testing in the next processor cycle.

SIGN This is the raw sign bit from the 2901.

SINT This signal is used by the processor to control the state of the signals MASK and INT.

SKERR Seek Error. This signal from the disc unit is used to determine that the disc has not completed a seek within a specified time interval and therefore, the servo is lost and needs to be re-oriented by a rezero operation.

SMDCY This output of the DMA control ROM is used to set the mid-cycle signal flip-flop on the next clock edge.

SRX X = 0 thru 7. Shift register parallel output bit.

SRTXX This output of the DMA control ROM is used to set the RTXX flip-flop on the next clock edge.

STDC Set the Disc Control. This signal is used to load the disc transfer control flags from the processor.

SYNDET This signal is true when the sync pattern (EE_{16}) is found in the shift register.

T0 This is the processor clock that is used to define the beginning and end of the data processing cycle in the processor. On the rising edge of this clock, all data from the current cycle is strobed into destinations and the new instruction for the upcoming cycle is strobed into the instruction pipeline register.

T1 This is one of the major clock signals that controls the processor. This clock overlaps and lags T0. This clock defines the loading of the next fetch address for the processor instruction.

W+SD Write or Sync Detected. This signal is the logical OR of the signals WRITE and SYNDET.

WCLKX X = H or L. This is the differential balanced line write clock to the disc unit. This signal is the servo clock re-transmitted by the controller. This is done to absorb some of the cable and interface delays.

WDATA This is the serial data that is to be written on the disc during a write operation. All data to the disc will pass through this line.

WDTAX X = H or L. This is the differential balanced line write data signal to the disc unit. This passes all data signals to be written to the disc.

WRITE This flag is controlled by the processor. It is used to control the direction of data flow to move data from the memory to the disc.

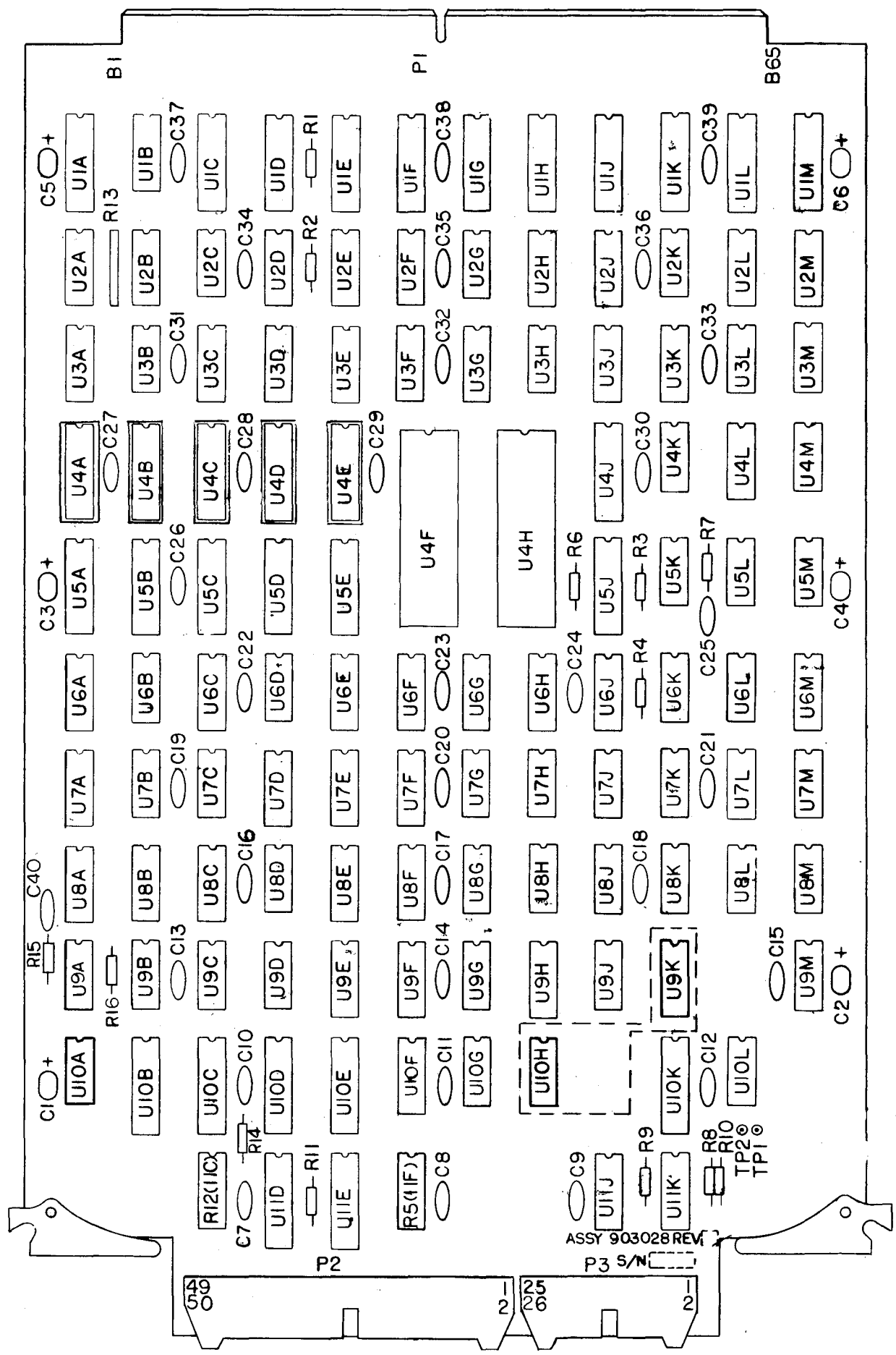
ZERO This signal indicates that the general counter has counted down to zero.

ZEROR This is the raw zero result flag from the 2901.

ZROSAV This is the saved output of the zero results bit from the 2901 to be used for testing in the next processor cycle.

SECTION 4

REFERENCE DATA


B1
P1
B65
C5
C3
C6
C4
C2
C1
C40
R13
R1
R2
R3
R4
R5(1F)
R6
R7
R8
R9
R10
R11
R12(1C)
R14
R15
R16
C7
C8
C9
C10
C11
C12
C13
C14
C15
C16
C17
C18
C19
C20
C21
C22
C23
C24
C25
C26
C27
C28
C29
C30
C31
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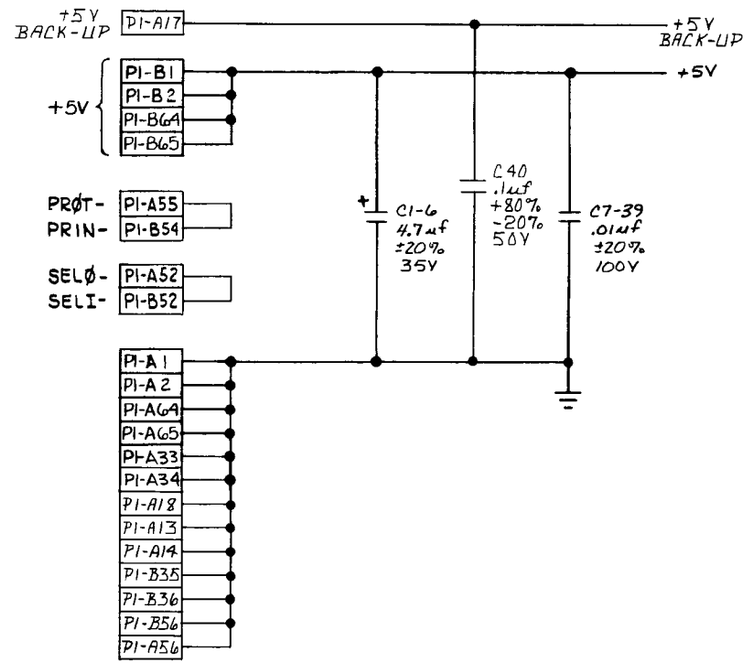

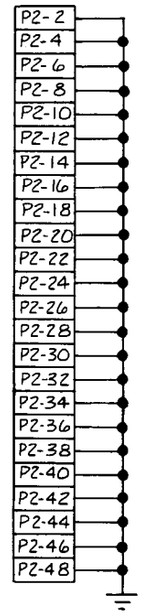

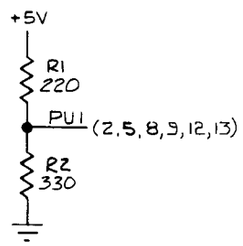

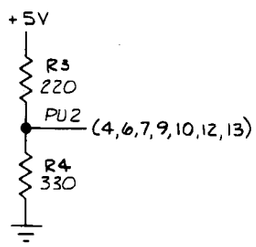

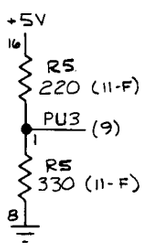

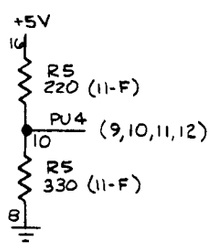

		DIMENSIONS ARE IN INCHES TOLERANCES UNLESS OTHERWISE SPECIFIED X ± .1 .XX ± .03 .XXX ± .010 ANGLES ± 1.0°	basic / four corporation 1335 South Claudina Street Anaheim, California 92805			
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			CHKD	[illegible]	7/08/77	
			ENG	[illegible]	7/27/77	SIZE C · DWG NO 903029 · REV D
			MFG			
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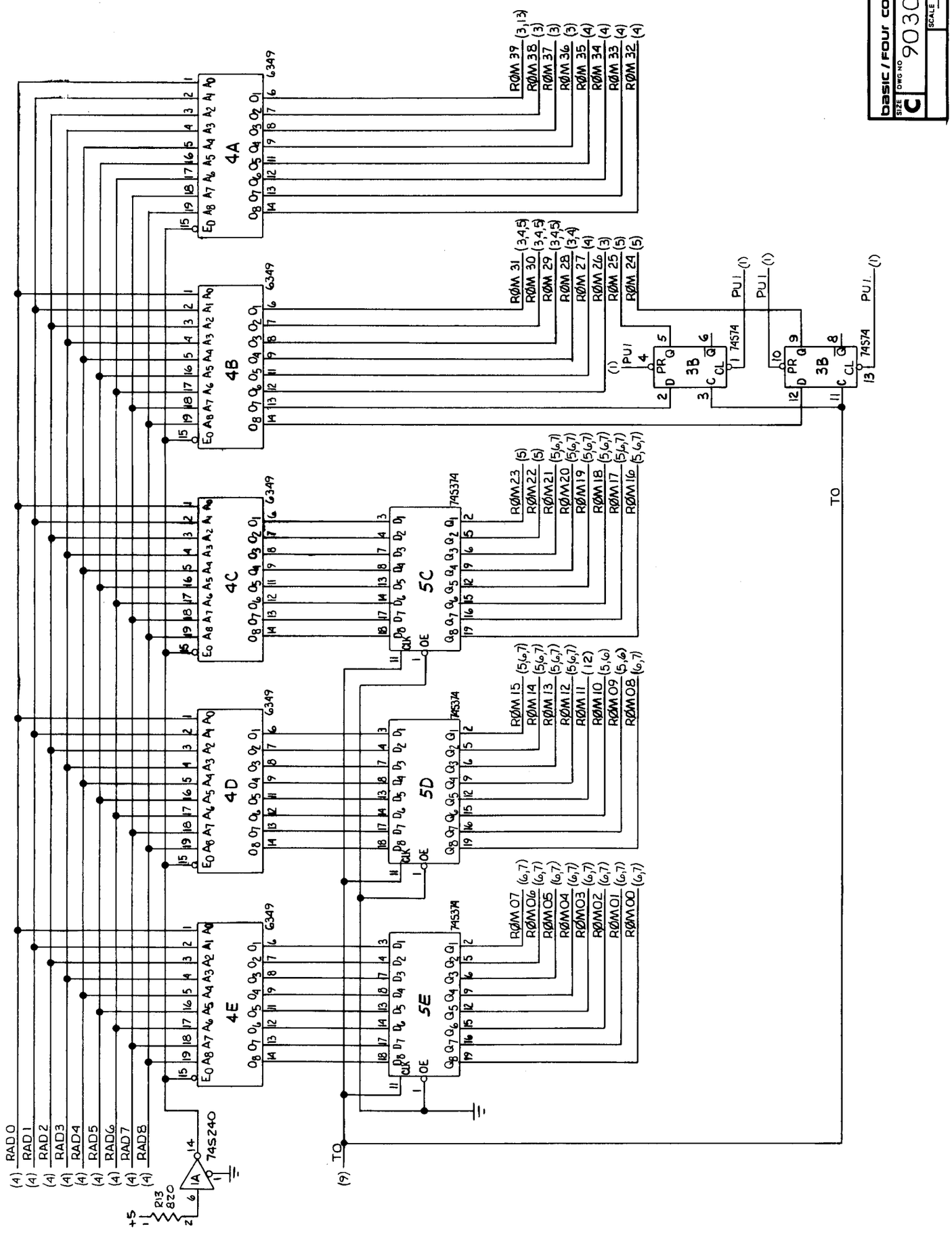
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4B
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4E
5C
5D
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ROM 31 (3,4,5)
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ROM 08 (6,7)
ROM 07 (6,7)
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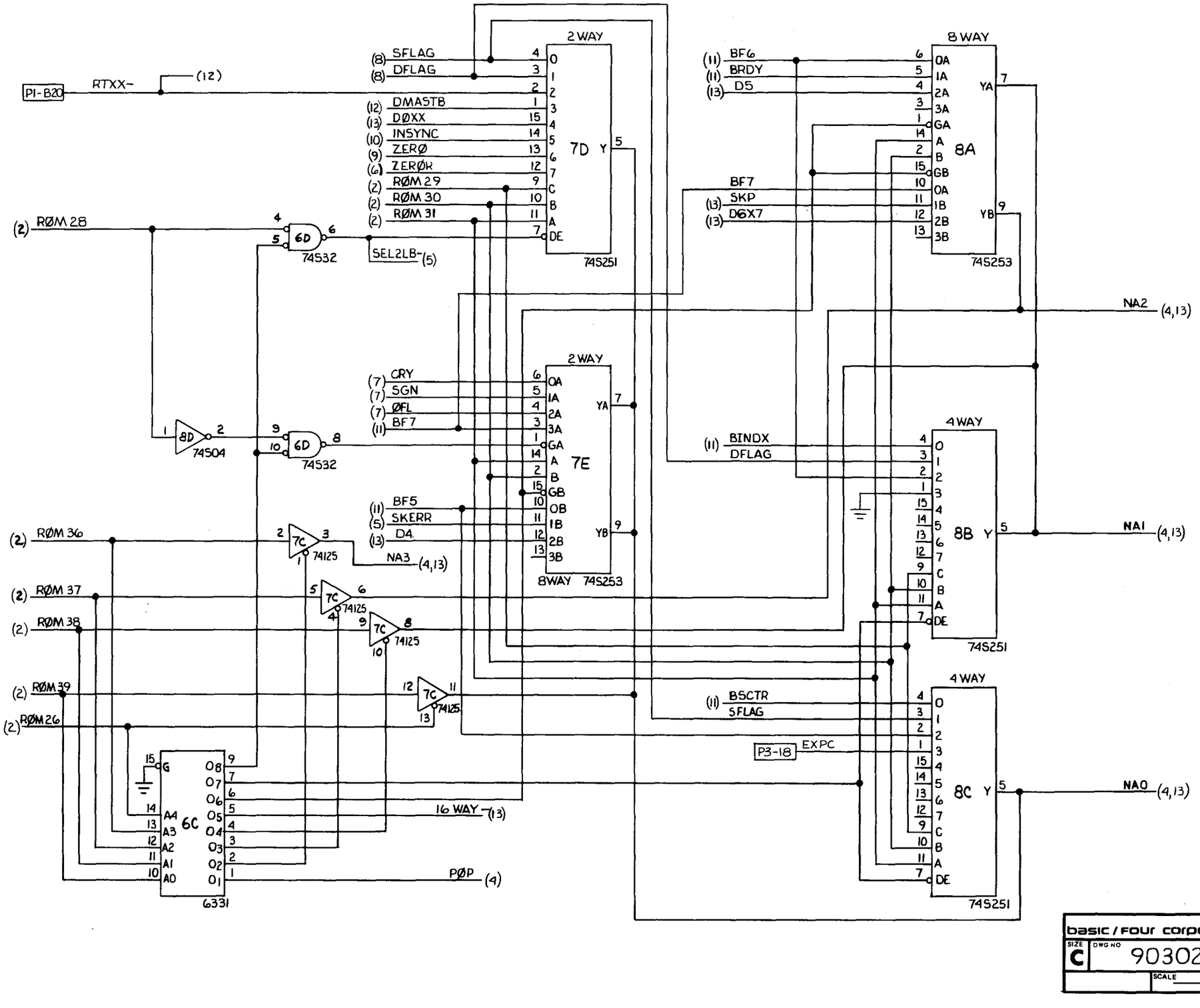

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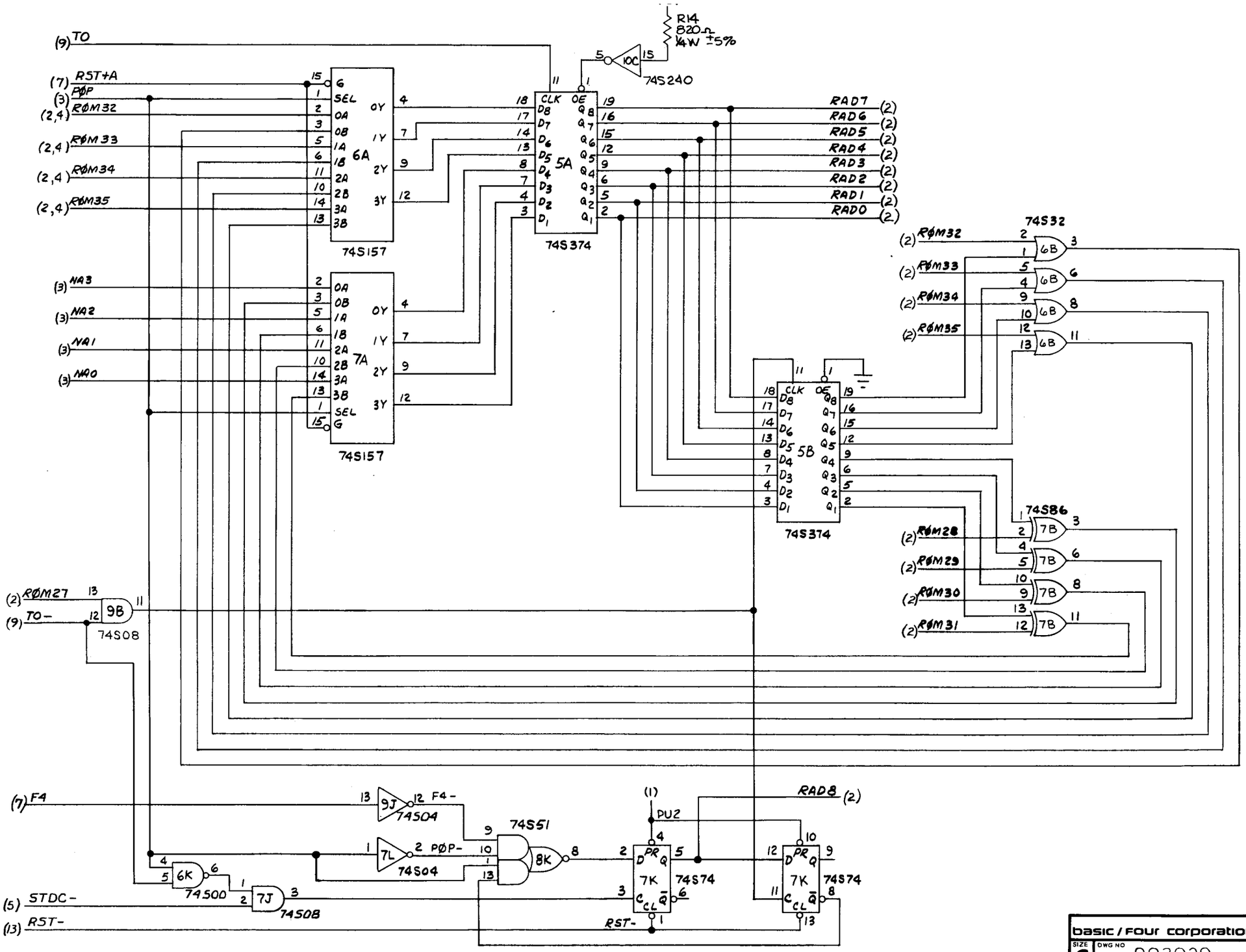

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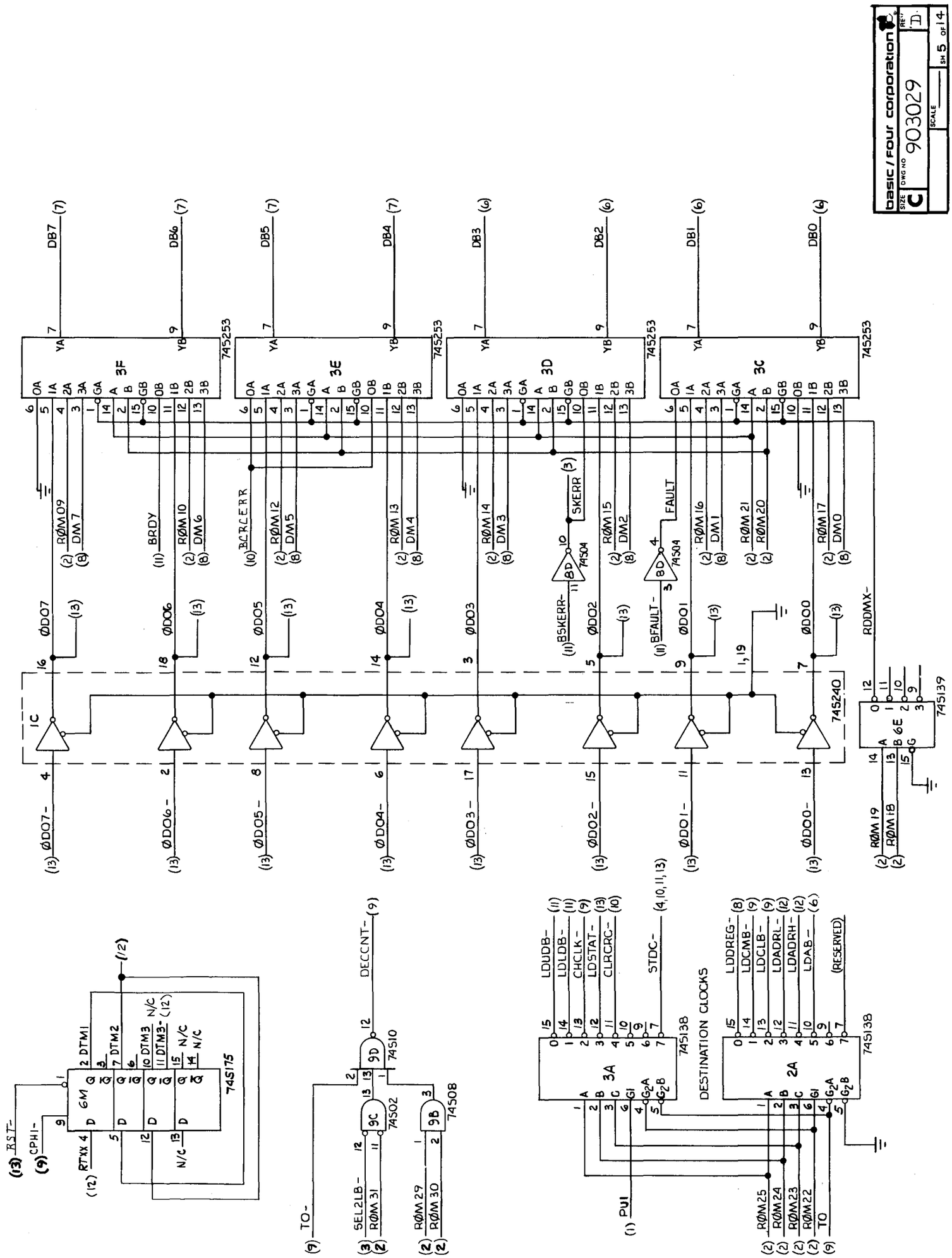
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3E
3D
3C
745253
1C
745240
6E
745139
6M
74S175
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74S10
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74S08
3A
2A
74S138
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SEL2LB-
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RØM 29
RØM 30
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CPHI-
RTXX
DTM1
DTM2
DTM3
DTM3-
N/C
LDUDB-
LDLDB-
CHCLK-
LDSTAT-
CLRCRC-
STDC-
LDDREG-
LDCMB-
LDCLB-
LDADRL-
LDADRH-
LDAB-
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ØDO3-
ØDO2-
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ØDO0-
ØDO7
ØDO6
ØDO5
ØDO4
ØDO3
ØDO2
ØDO1
ØDO0
BSKERR-
BFAULT-
SKERR
FAULT
BRDY
BCRCERR
RØM09
DM7
RØM10
DM6
RØM12
DM5
RØM13
DM4
RØM14
DM3
RØM15
DM2
RØM16
DM1
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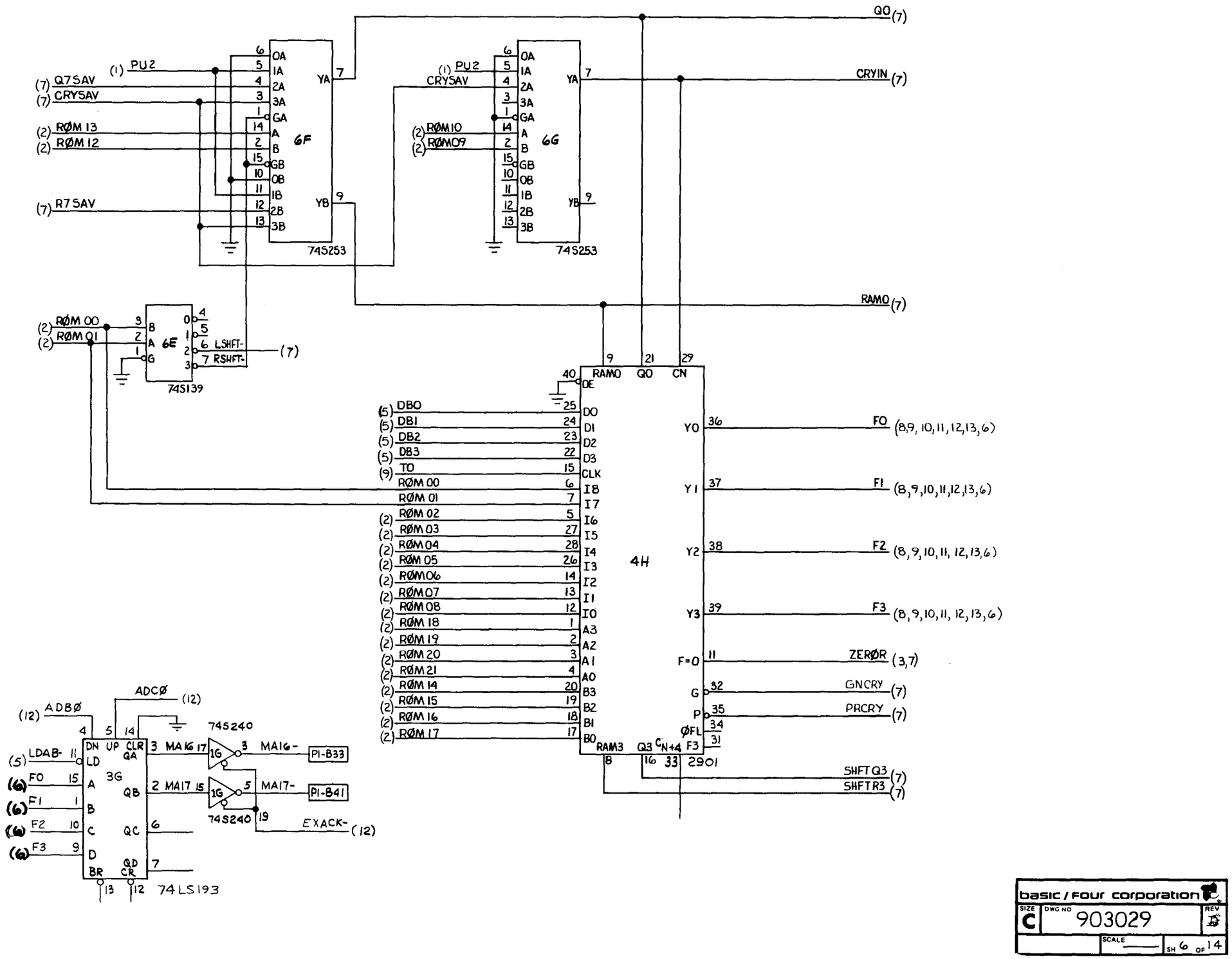
DB4
DB3
DB2
DB1
DB0



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SIZE C | DWG NO 903029 | REV B

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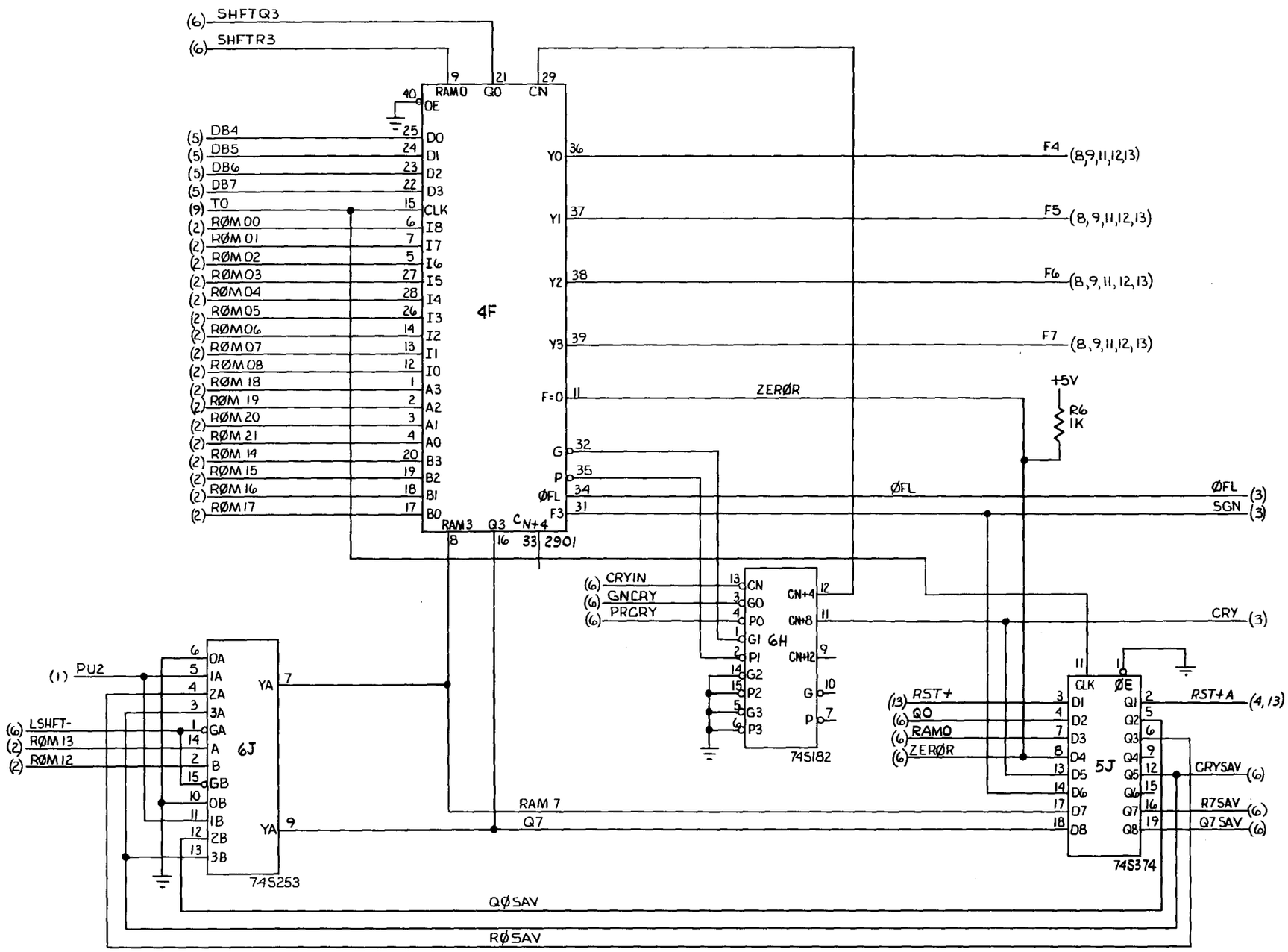

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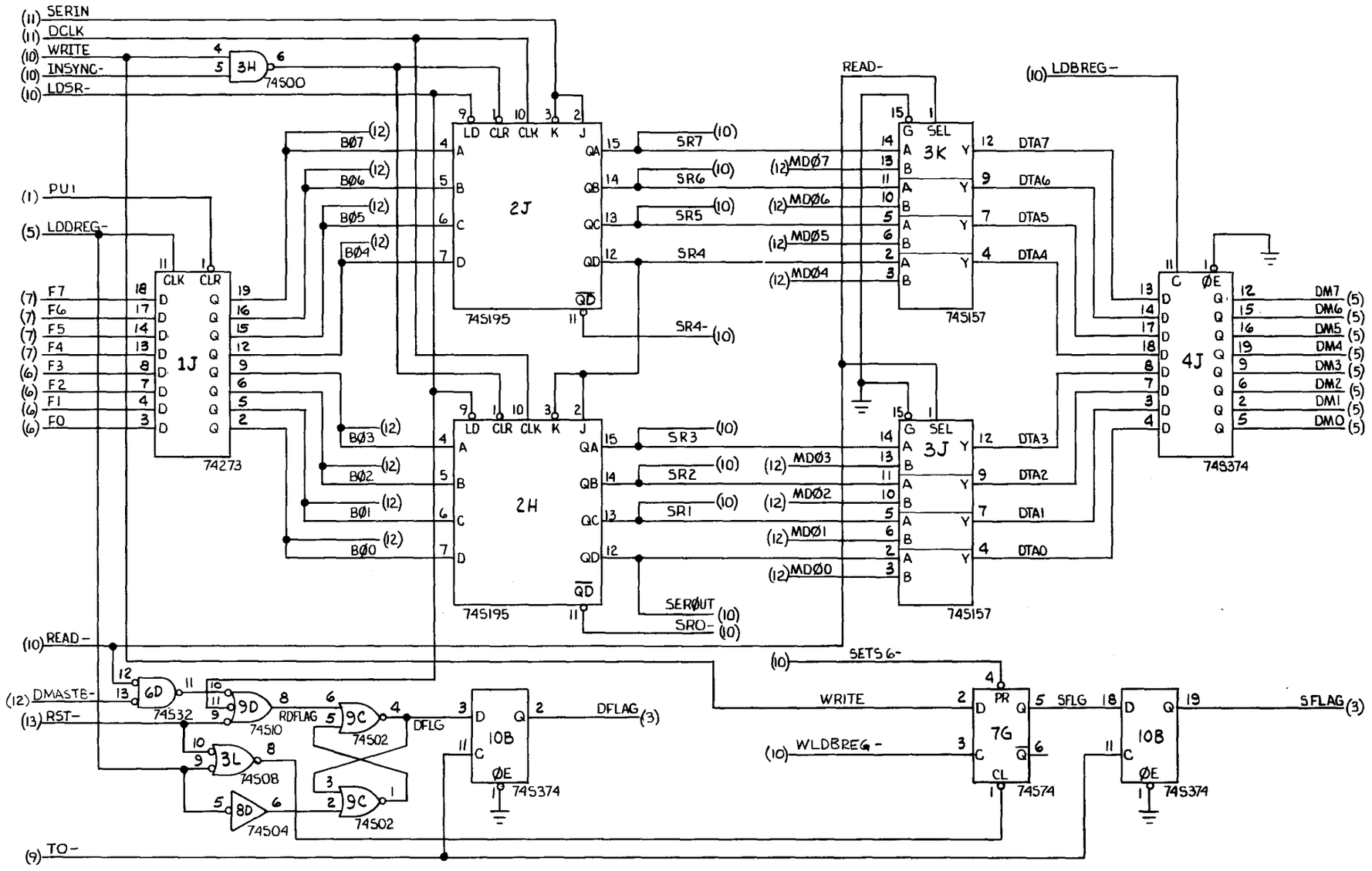

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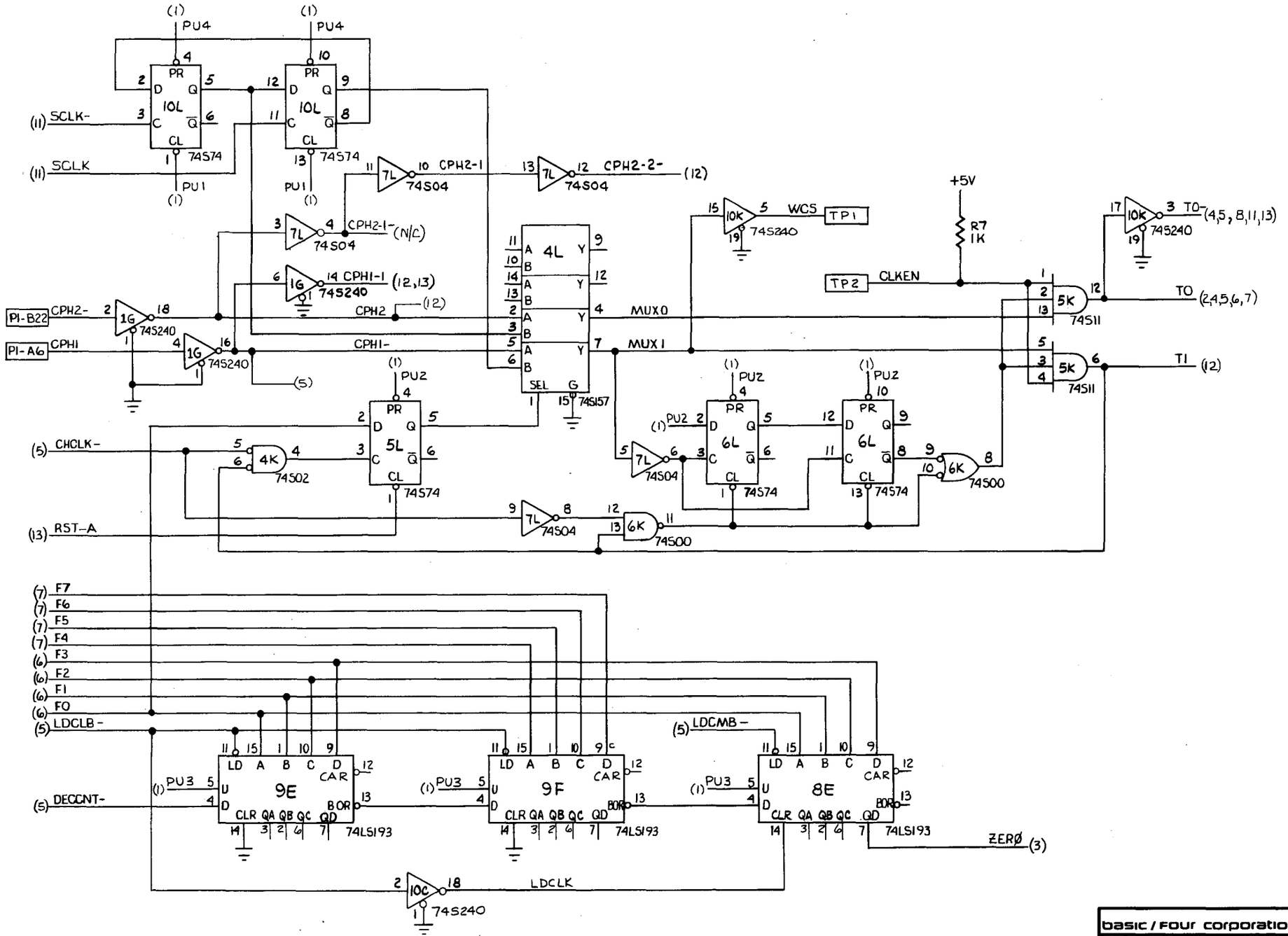

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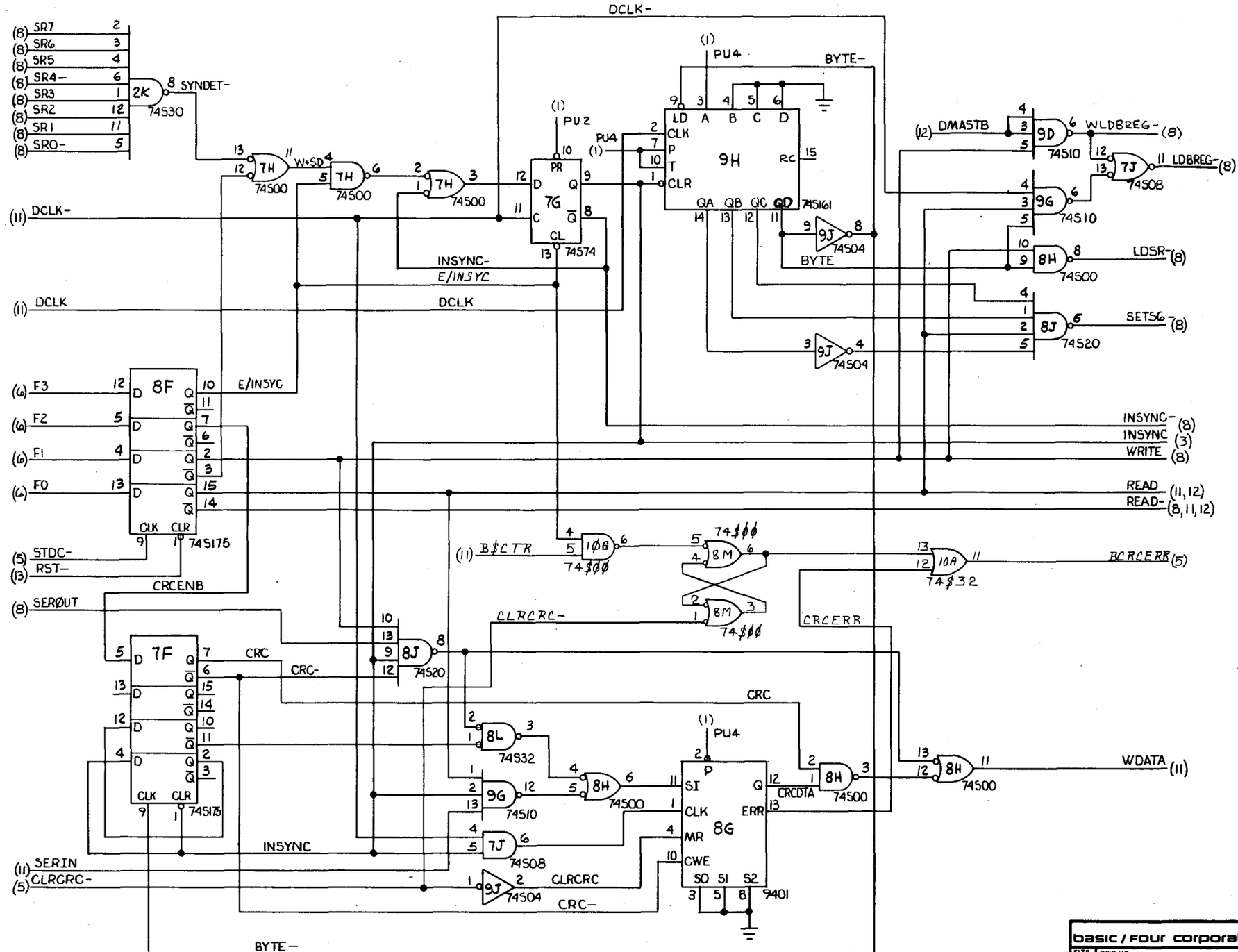

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SIZE C	DWG NO 903029		REV D
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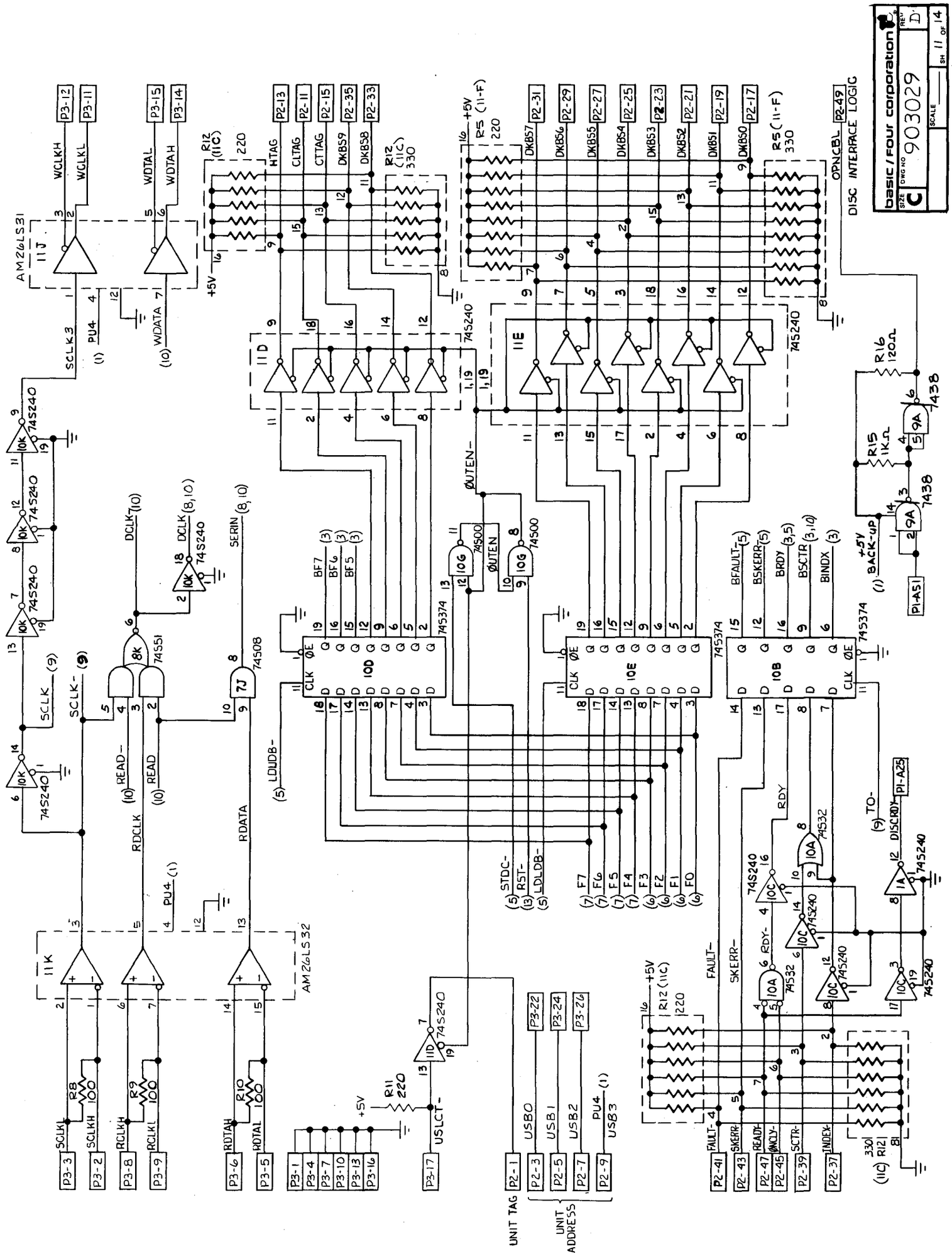
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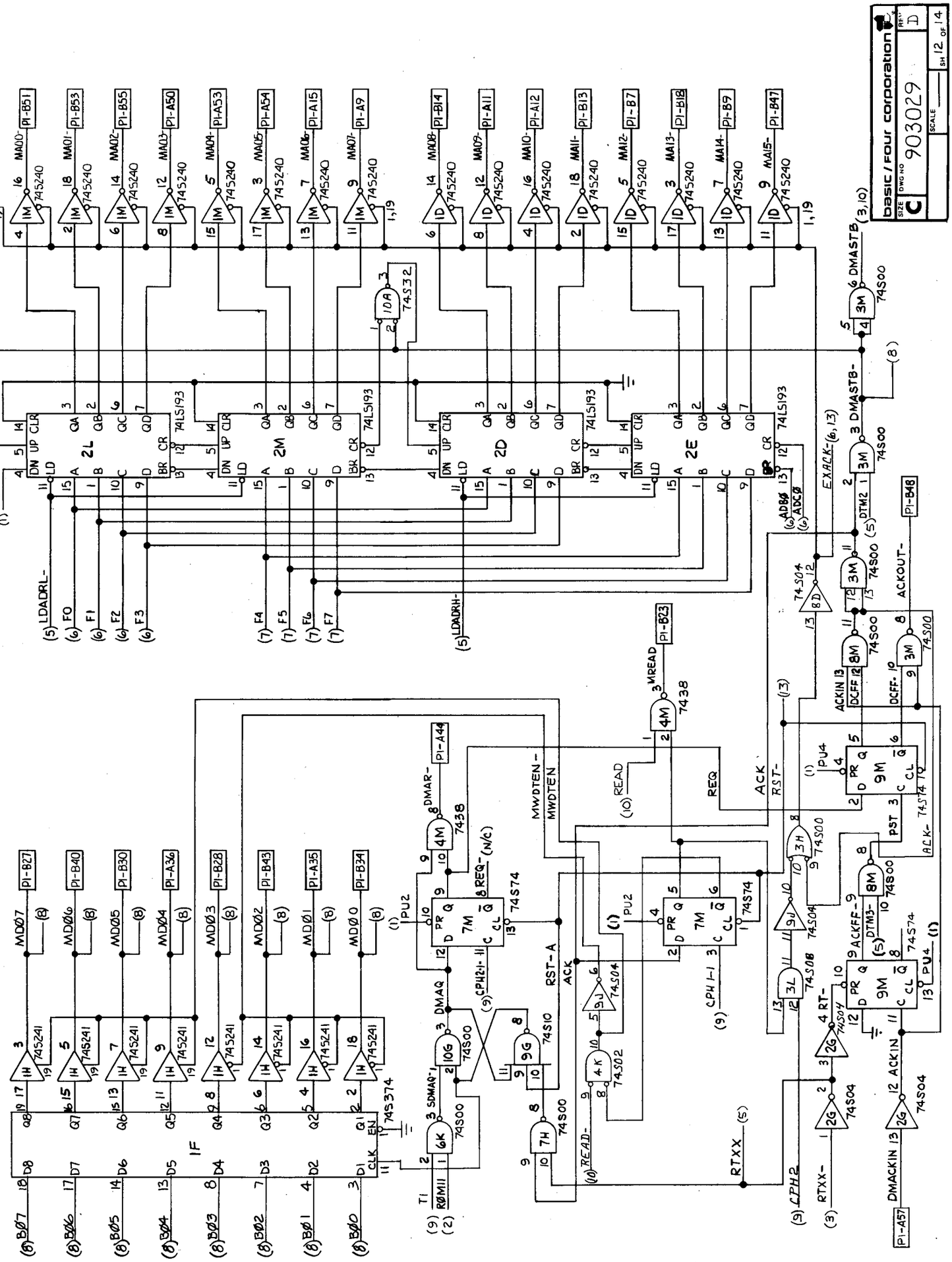
UNIT ADDRESS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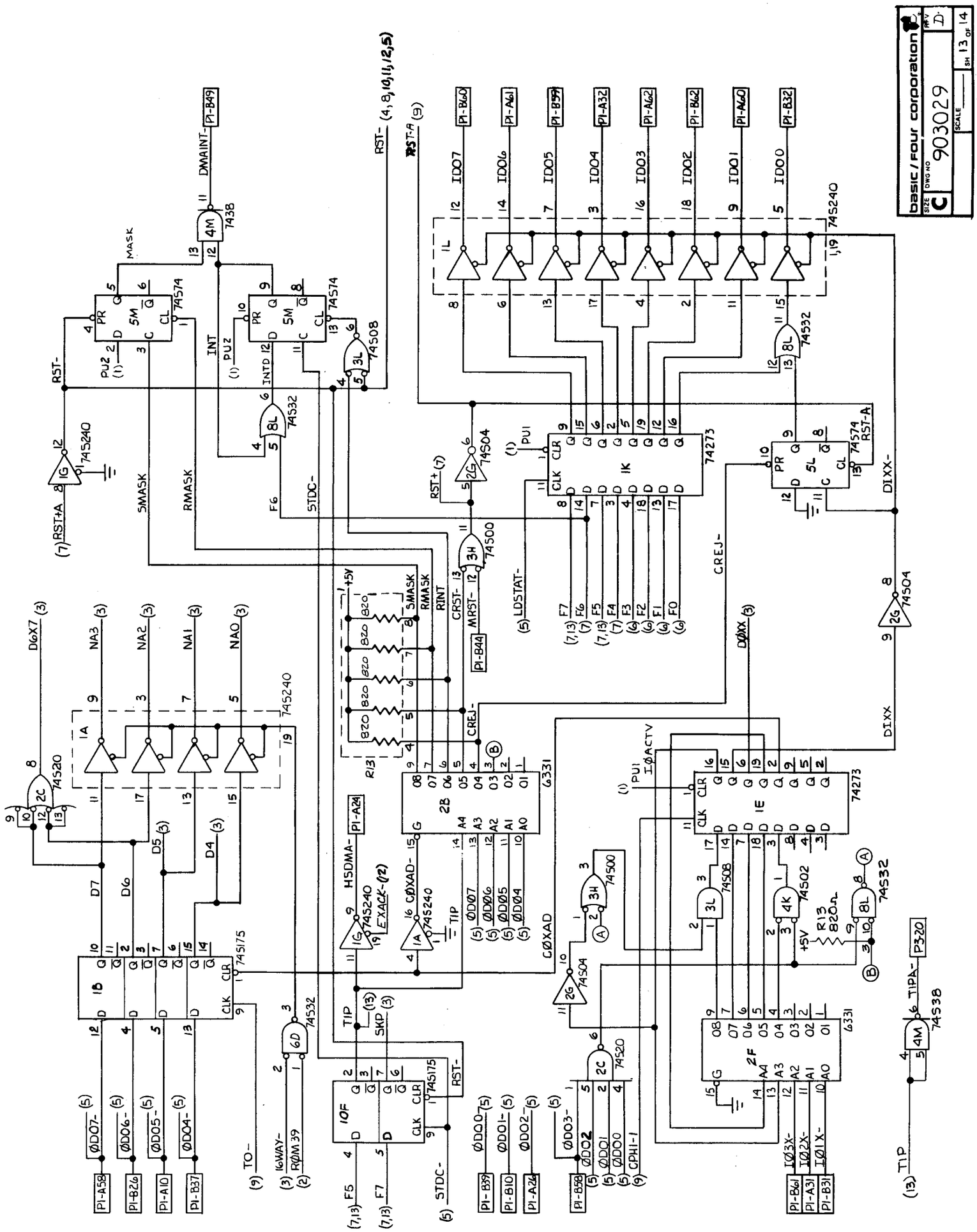
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DMAINT-
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MASK
PU2
INTD
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STDC-
SMASK
RMASK
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CRST-
MRST-
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DIXX-
DIXX
HSDMA-
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74LS273
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74LS08
74LS02
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74LS20
74LS38
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74LS63

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A		B		
(1)	GND	1	+5V	(1)
(1)	GND	2	+5V	(1)
		3		
		4		
		5		
(9)	CHP1	6		
		7	MA12-	(12)
		8		
(12)	MA07-	9	MA14-	(12)
(13)	ØD05-	10	ØD01-	(13)
(12)	MA09-	11		
(12)	MA10-	12		
(1)	GND	13	MA11-	(12)
(1)	GND	14	MA08-	(12)
(12)	MA06-	15		
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		17		
(1)	GND	18	MA13-	(12)
		19		
		20	RTXX-	(3)
		21		
		22	CHP2-	(9)
		23	MREAD	(12)
(13)	HSDMA-	24		
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		27	MDØ7	(12)
		28	MDØ3	(12)
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(13)	IØ2X-	31	IØ1X-	(13)
(13)	IDO4	32	IDOO	(13)
(1)	GND	33	MA16-	(6)
(1)	GND	34	MDØ0	(12)
(12)	MDØ1	35	GND	(1)
(12)	MDØ4	36	GND	(1)
		37	ØD04-	(13)
		38		
		39	ØD00-	(13)
		40	MDØ6	(12)
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		43	MDØ2	(12)
(12)	DMAR-	44	MRST-	(13)
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		47	MA15	(12)
		48	ACKOUT-	(12)
		49	DMAINT-	(13)
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(1)	SELØ-	52	SEL1-	(1)
(12)	MA04-	53	MA01-	(12)
(12)	MA05-	54	PRIN-	(1)
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(1)	GND	65	+5V	(1)

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4	GND	(1)
5	USB1	(11)
6	GND	(1)
7	USB2	(11)
8	GND	(1)
9	USB3	(11)
10	GND	(1)
11	CLTAG	(11)
12	GND	(1)
13	HTAG	(11)
14	GND	(1)
15	CTTAG	(11)
16	GND	(1)
17	DKBS0	(11)
18	GND	(1)
19	DKBS1	(11)
20	GND	(1)
21	DKBS2	(11)
22	GND	(1)
23	DKBS3	(11)
24	GND	(1)
25	DKBS4	(11)
26	GND	(1)
27	DKBS5	(11)
28	GND	(1)
29	DKBS6	(11)
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31	DKBS7	(11)
32	GND	(1)
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35	DKBS9	(11)
36	GND	(1)
37	INDEX-	(11)
38	GND	(1)
39	SCTR-	(11)
40	GND	(1)
41	FAULT-	(11)
42	GND	(1)
43	SKERR-	(11)
44	GND	(1)
45	ØNCLY-	(11)
46	GND	(1)
47	READY-	(11)
48	GND	(1)
49	OPNCBL	(11)
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3	SCLKL	
4	GND	
5	RDTAL	
6	RDTAH	
7	GND	
8	RCLKH	
9	RCLKL	
10	GND	
11	WCLKL	
12	WCLKH	
13	GND	
14	WDTAH	
15	WDTAL	
16	GND	
17	USLCT-	(11)
18	EXPC	(3)
19		
20	TIPA-	(13)
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22	USBO	(11)
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26	USB2	(11)

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