BCI-2004
Unibus Adapter for the PCI Local Bus
Owner's Manual

BCI-2004-OM
Revision B

The **Logical** Company
Striving to serve you better

Owner's Manual for the
BCI-2004

Unibus Adapter for the PCI Local Bus

The **Logical** Company

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1 Installation

This chapter lists the steps involved in installing the BCI-2004 hardware. References throughout this chapter tell you where to look for more detailed information. The BCI-2004 module is shown in Figure 1-1. Refer to this figure as you follow the steps outlined below.

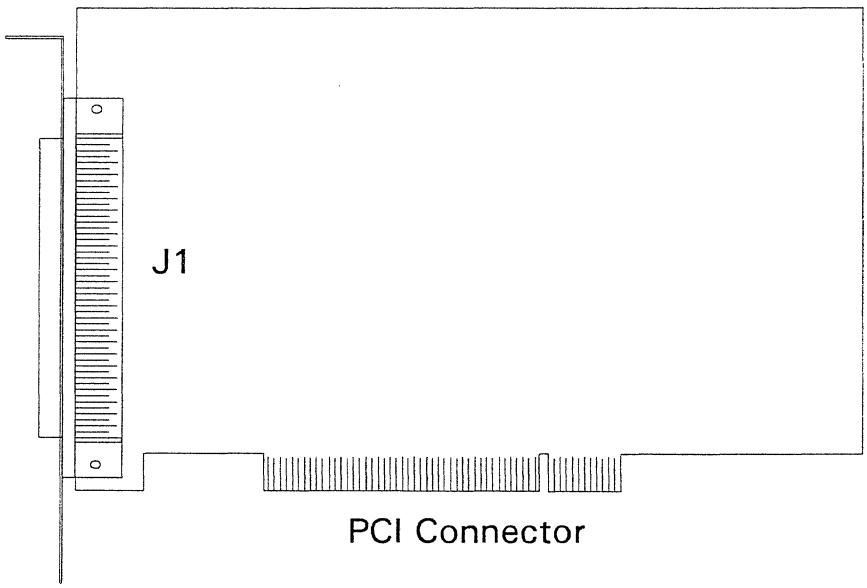


Figure 1-1: BCI-2004 Module

1. Open the workstation enclosure or expansion chassis

To remove the cover from the workstation or expansion chassis enclosure:

A. Shut down the system software as described in the instructions that came with your software.

B. Remove power to the system unit or expansion chassis.

C. Open the enclosure as described in the manuals that came with the unit.

Note

Use the anti-static wrist strap supplied with your system unit to prevent damage to the equipment. Clip the free end of the strap to the metal frame of the enclosure.

2. Install the BCI-2004 controller.

The BCI-2004 PCI controller can be installed in any available PCI Local bus slot.

A. If the back of the expansion chassis or system unit has a metal cover plate over the opening of the PCI slot you have selected, remove the anchor screw that holds the cover in place then slide the cover out of the slot.

B. Position the BCI-2004 with the gold fingers on the edge of the module next to the PCI connector of the selected slot . Gently rock the module into the PCI connector while you fit the metal bulkhead into the slot opening. Be sure that the connectors are firmly seated.

Note: If the enclosure contains RFI clips along the slot, take care when inserting the module not to push the clips out of alignment.

C. Secure the BCI-2004 using the anchor screw that you removed in Step A. Retain the cover plate for future use.

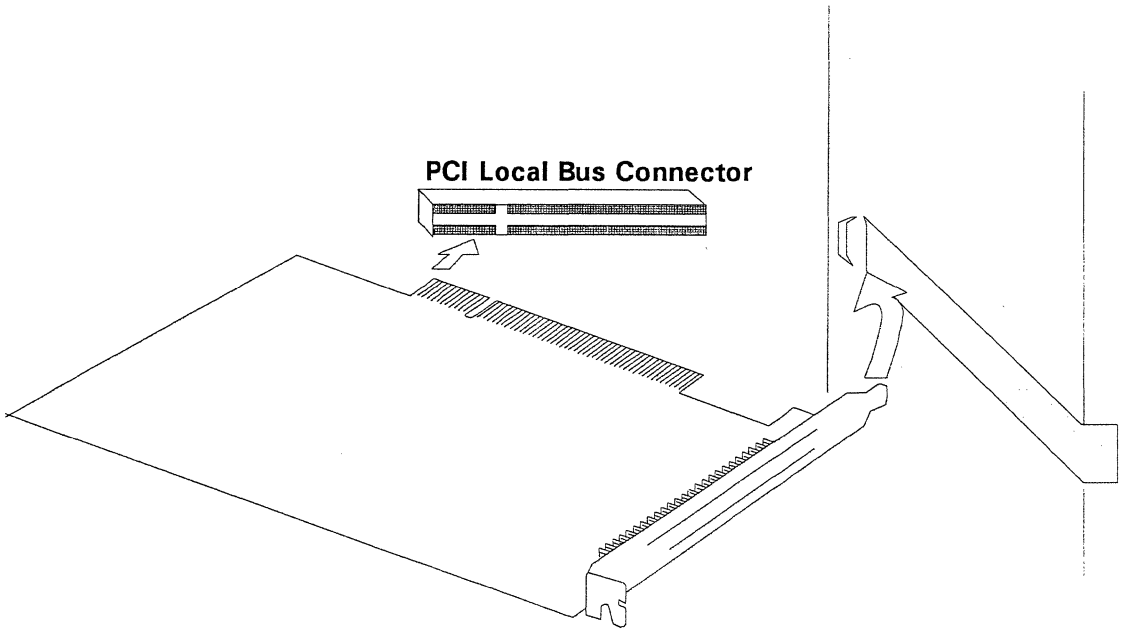


Figure 1-2: Inserting the Board into the PCI Slot

D. Remove the anti-static wrist strap, replace the cover on the enclosure and secure.

3. Check the Unibus interrupt priority settings

The BCI-2004 supports two Unibus priority levels. The CAU-2003-A and CAU-2001-A Unibus modules are factory set to allow priority levels BR4 and BR5. The priority levels supported can be selected by changing the location of zero ohm resistors on the Unibus module. The settings are shown below.

Priority Levels	Resistors Installed	
BR4, BR5	S5, S6, S8, S10, S12, S18	Factory Setting
BR4, BR6	S4, S8, S12, S15, S17, S18	
BR4, BR7	S6, S8, S12, S13, S16, S17	
BR5, BR6	S3, S4, S9, S11, S15, S18	
BR5, BR7	S3, S6, S9, S11, S13, S16	
BR6, BR7	S3, S7, S13, S14, S16, S17	
ACLO	S2	Factory Setting
DCLO	S1	Factory Setting

NOTE

ACLO and DCLO are set independently. Be sure that resistors in S1 and S2 are installed in addition to the priority interrupt resistors.

4. Install the cabinet kit.

This step describes how to install the cabinet kit with the BCI-2004-AA package. If you are installing a BCI-2004-AB kit with a CAU-2001-A Unibus module, skip to step 4.

A. Install the CAU-2003-A Unibus module.

The Unibus module installs into connectors A and B of the Unibus backplane in the first slot, replacing a Unibus cable or Unibus jumper module. Take care when installing the module to ensure that the connector on the module is clear of any adjacent modules. Allow adequate room to connect and route the ribbon cables.

Ensure that there are no vacant slots between the Unibus module and Unibus controllers. For proper system operation, any vacant slots must have a Unibus bus grant module installed.

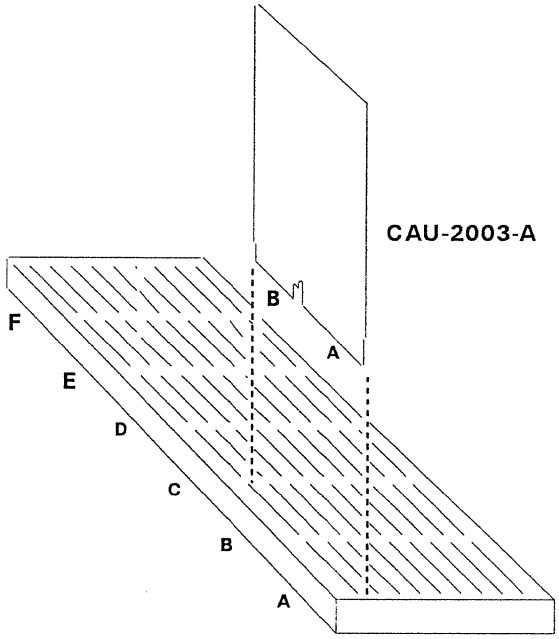


Figure 1-3: Installing the CAU-2003-A Unibus Module

B. Install the ribbon cables

Connect the supplied CAB-2101 ribbon cables to the CAU-2003-A Unibus module. Align the triangle on each cable connector to pin one of the connector on the module. The connectors are positioned so that the two cables can be dressed together.

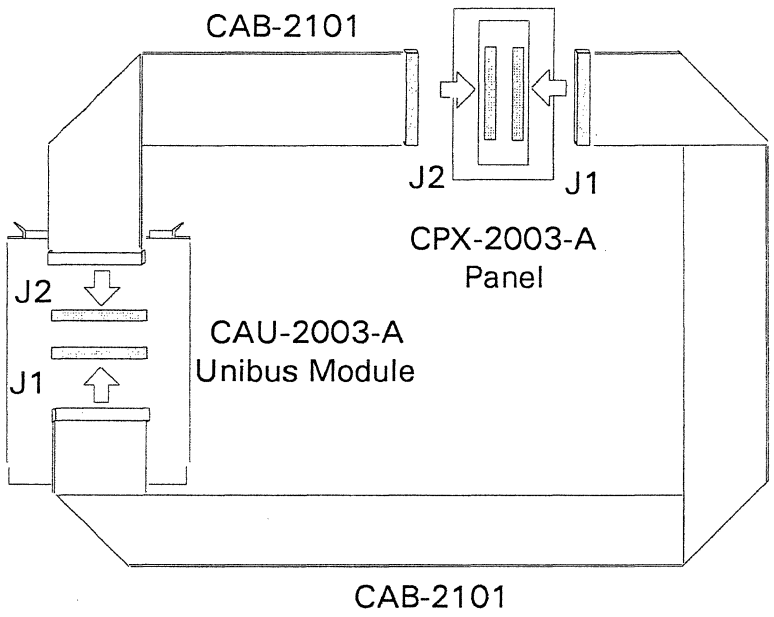


Figure 1-4: Installing Ribbon Cables

Remove a blank panel from the I/O bulkhead of your system cabinet. Feed the ribbon cables out through the opening in the bulkhead and connect them with the CPX-2003-A panel. Connect J1 on the panel to J1 on the module again aligning pin one.

C. Install the CPX-2003-A bulkhead panel

Install the CPX-2003-A panel into the I/O bulkhead and secure with the two supplied screws.

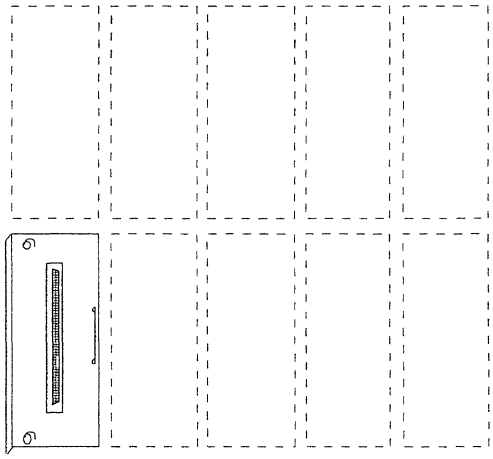


Figure 1-5: Mounting the Panel into the Bulkhead

6. Install the CAU-2001-A Unibus module.

The Unibus module installs into connectors A and B of the Unibus backplane in the first slot, replacing a Unibus cable or Unibus jumper module. Take care when installing the module to ensure that the connector on the module is clear of any adjacent modules. Allow adequate room to connect and route the interconnect cable.

Ensure that there are no vacant slots between the Unibus module and Unibus controllers. For proper system operation, any vacant slots must have a Unibus bus grant module installed.

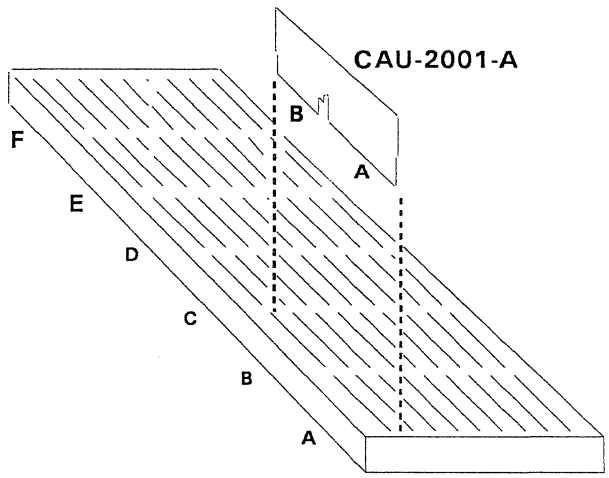


Figure 1-6: Installing the CAU-2001-A Unibus Module

6. Install the interconnecting cable

Use the supplied 8-foot cable (CAB-1104-8) to connect the controller to the cabinet kit or the CAU-2001-A Unibus module. Pin assignments for the cable are provided in Appendix C.

The interconnect cable is keyed and can be inserted in only one direction.

Be sure to allow adequate space in your backplane for the interconnect cable to exit the Unibus chassis. It is important that the cable connector does not make contact with any other modules in the Unibus backplane. Re-configuration of modules within the backplane may be required to provide sufficient space.

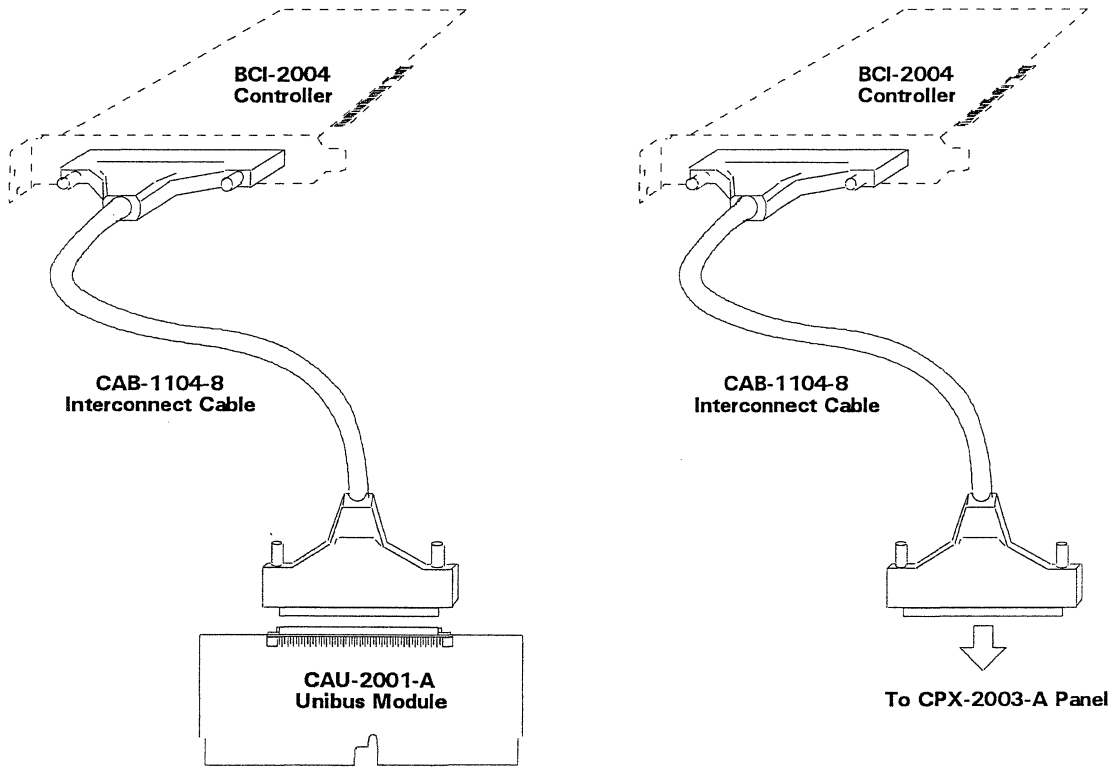


Figure 1-7: Installing the Interconnect Cable

The BCI-2004 installation is complete. Go to step 6 to verify installation.

7. Power up the system and verify installation.

The following conventions are used in this manual:

`output`	In examples, computer output is shown in this type.
`user input`	In examples, user input is shown in bold type.
`[CR]`	This is used to specify pressing the Return/Enter key.

A. Apply power to the computer system and wait for the self-test to complete.

B. To verify that the BCI-2004 is recognized by the system and to confirm the physical slot number, use the console show config command.

```
P00>>>show config
                        Digital Equipment Corporation
                            AlphaServer 2000 4/200

SRM Console V3.9-89                VMS PALcode X5.48-89, OSF PALcode X1.35-55

Component    Status              Module ID
CPU 0           P                B2020-AA DECchip (tm) 21064-3
Memory 0        P                B2023-BA  64 MB
I/O                              B2111-AA
                                 dva0.0.0.0.1              RX26

 Slot Option                     Hose 0, Bus 0, PCI
   1  NCR 53C810                 pka0.7.0.1.0              SCSI Bus ID 7
                                 dka0.0.0.1.0              RZ28
                                 dka600.6.0.1.0            RRD43
                                 mka500.5.0.1.0            TLZ06
   2  Intel 82375EB                                        Bridge to Hose 1, EISA
   6  DECchip 21040-AA           ewa0.0.0.6.0              08-00-2B-E4-23-F9
   8  00131356

 Slot Option                     Hose 1, Bus 0, EISA
   7  CPQ3011
```

The console firmware found a BCI-2004 (option 00131356) in PCI slot 8. The AlphaServer 2000 labels PCI backplane slots 6-8 as module bulkheads PCI0-PCI2 on the rear of the chassis. Please note that the internal backplane slot number is used for all hardware and software installation. For other PCI based Alpha systems, refer to the owner's guide delivered with the system for the PCI slot numbering convention.

C. OpenVMS or Windows NT diagnostics are available to verify the basic operation of the module. Call our factory for more information.

2 General Description

Product Description

The PCI Unibus Adapter provides a means to connect Unibus controllers to a workstation with a PCI Local bus.

The PCI Unibus Adapter consists of a BCI-2004 PCI controller, a CAB-1104-8 interconnect cable, and a choice of Unibus cable adapter modules. The PCI Unibus adapter enables the workstation to read and write the entire Unibus address space and to control Unibus interrupt requests and DMA transfers.

The BCI-2004 controller is a single slot PCI option that contains circuitry to interface the PCI to the Unibus and internal registers for control and status.

The CAB-1104-8 cable is eight feet long and consists of a twisted pair shielded cable terminated at each end with high density connectors. The cable is used to connect the PCI controller to the Unibus module or cabinet kit.

Connection to Unibus signals contained in an expansion chassis or user equipment containing a Unibus cable connection can be accomplished in two ways: using a cabinet kit with bulkhead panel and ribbon cables or through direct connection to a Unibus module:

- The cabinet kit consists of a CAU-2003-A Unibus module, two 6-ft flat ribbon cables, and a CPX-2003-A bulkhead panel. The cabinet kit can be used when connecting to a Unibus chassis that utilizes bulkhead panels for FCC and emissions control. The CAU-2003 is a dual-width module and installs into a Unibus backplane slot 1, connectors A and B, replacing a Unibus cable or Unibus jumper module. The two 6-ft flat ribbon cables connect the CAU-2003-A module to the CPX-2003-A bulkhead panel. Figure 2-1 depicts the components of the BCI-2004-AA cabinet kit package.

- The CAU-2001-A Unibus module provides the means to connect to the Unibus signals contained in an expansion chassis, or user equipment containing a Unibus cable

connection. The CAU-2001-A is a dual-width module approximately the size of the end of a Unibus cable. The module installs into a Unibus backplane slot 1, connectors A and B, replacing a Unibus cable or Unibus jumper module. Figure 2-2 shows the components of a BCI-2004-AB package.

Part Numbers

Packages

BCI-2004-AA	Unibus adapter package with cabinet kit. Includes BCI-2004-A controller, CAB-1104-8 interconnect cable, and CPX-2003-AA cabinet kit.
BCI-2004-AB	Unibus adapter package, no cabinet kit. Includes BCI-2004-A controller, CAB-1104-8 interconnect cable, and CAU-2001-A Unibus module.

PCI Controller

BCI-2004-A	PCI controller

Unibus Module

CAU-2001-A	Unibus adapter module for use without panel

Cabinet Kit

CPX-2003-AA	Cabinet kit includes CPX-2003-A bulkhead panel, CAU-2003-A Unibus module, and 2 each CAB-2101-72 flat ribbon cables.
CAU-2003-A	Unibus adapter for use with bulkhead panel
CPX-2003-A	Bulkhead panel
CAB-2101-72	6-ft flat ribbon cable

Interconnect Cable

CAB-1104-8	8-ft interconnect cable

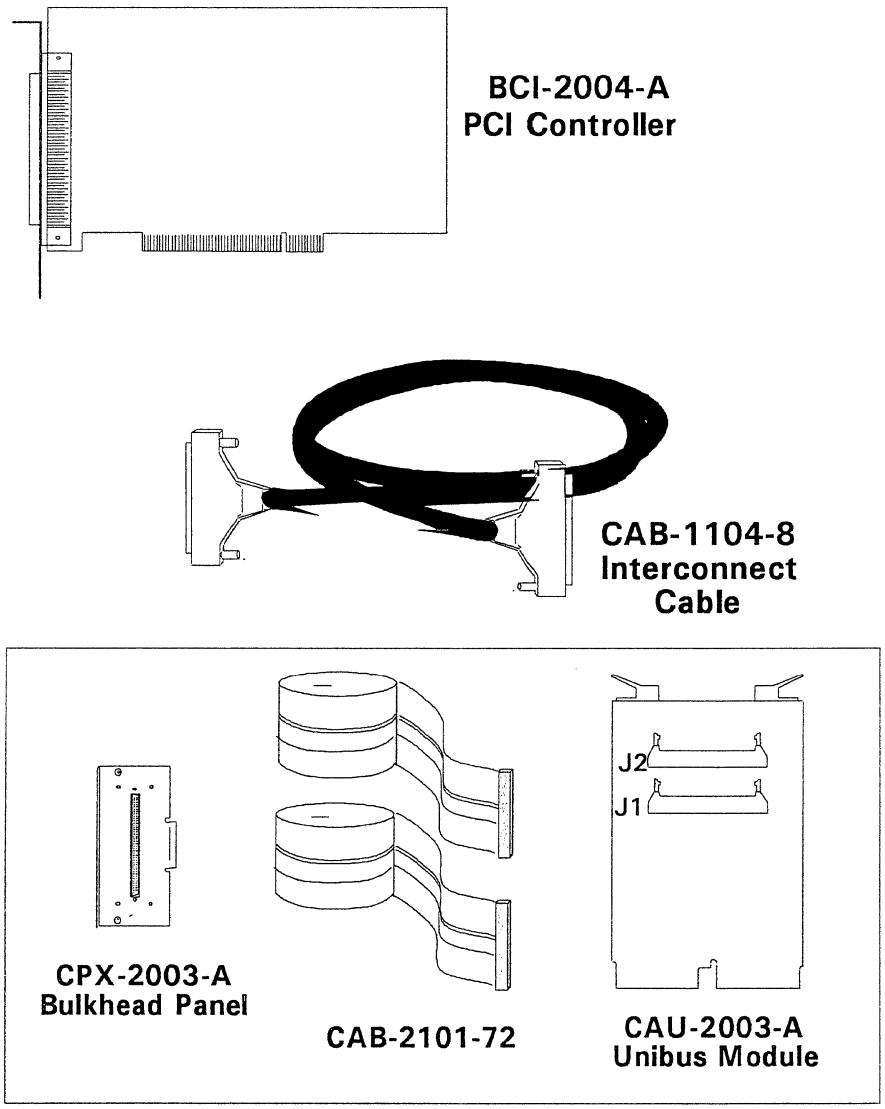


Figure 2-1: BCI-2004-AA Package

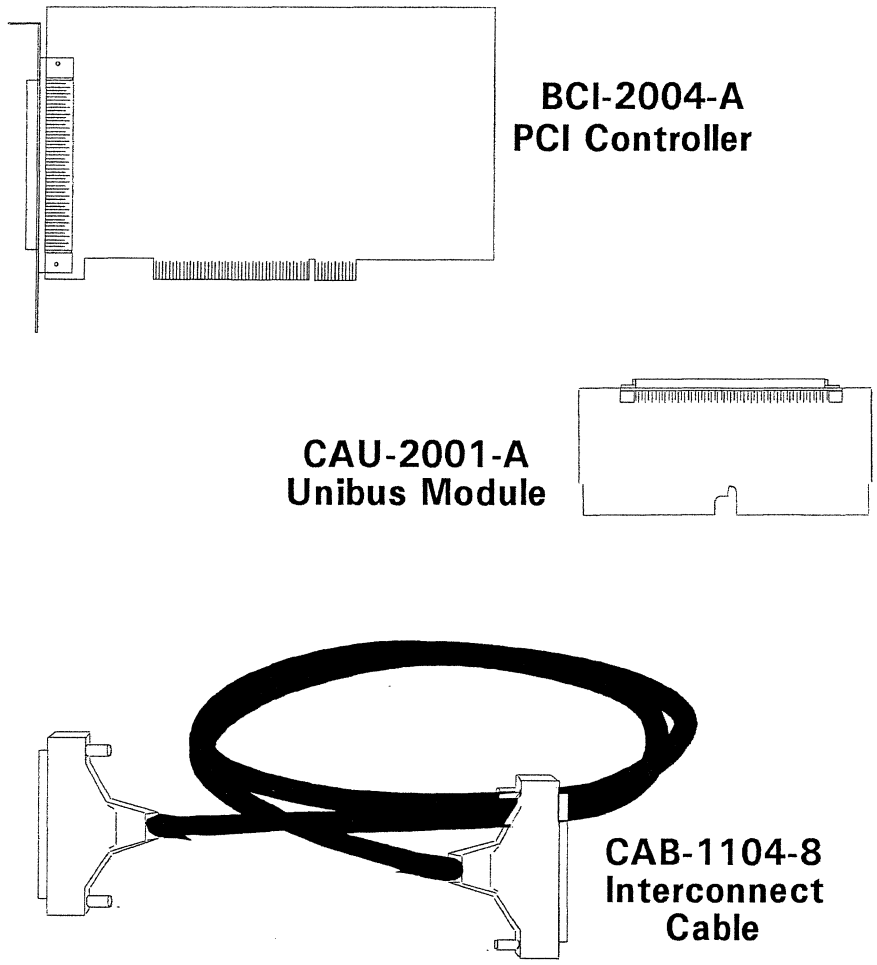


Figure 2-2: BCI-2004-AB Package

Specifications

Physical Dimensions

BCI-2004-A	Standard short card measuring 6.875 inches by 4.2 inches (17.46 cm by 10.67 cm).
CAU-2001-A	Dual-width Unibus module, 5.2 inches by 2.3 inches (13.2 cm by 5.8 cm)
CAU-2003-A	Dual-width Unibus module, 5.2 inches by 8.9 inches (13.2 cm by 22.8 cm)
CPX-2003-A	Bulkhead panel, 4.7 inches by 2.2 inches

Interface

Interconnect Cable	8-foot, terminated with a 100-pin high density connector at each end.
CPX-2003 to CAU-2003	6-foot, 50-pin flat ribbon cables, 2 each.

Electrical

Power Required:	
BCI-2004-A	2.0 amps @ 5.0 volts +3.3 volts not used +12 volts not used
CAU-2001-A	+5 and ±15 volts not used
CAU-2003-A	+5 and ±15 volts not used
Unibus Load	1 dc load
Bus Drive Capability	19 additional dc loads

Environmental

Operating Conditions:	
Temperature	5° to 50° C (41° to 122° F)
Relative Humidity	20% to 80% noncondensing

Storage Conditions:

Temperature	-40° to 66° C (-40° to 150° F)
Relative Humidity	10% to 95% noncondensing

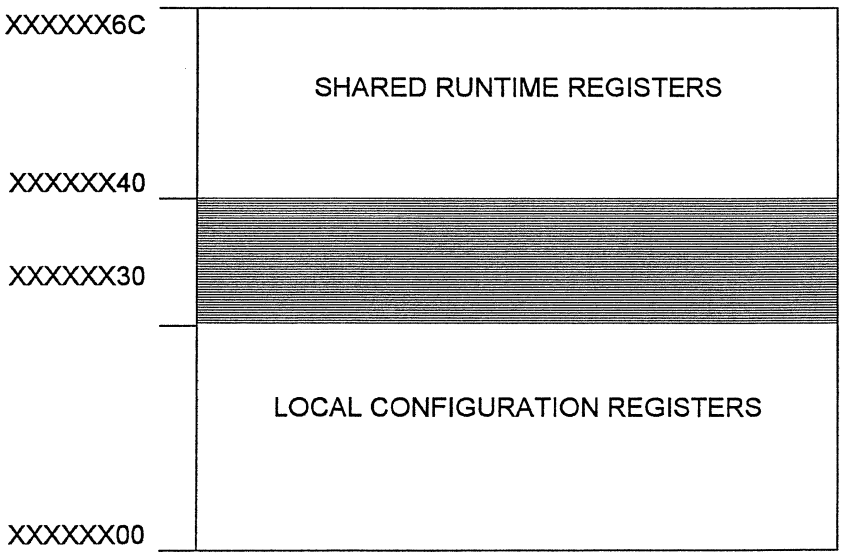
3 Operation

Address Assignment

The BCI-2004 does not use switches or jumpers to define device address assignments as found in other bus implementations. Device address assignments are defined by the PCI host during configuration, which is usually performed immediately following a power-up operation. During configuration, the host accesses each PCI slot to determine if a device is present. If a device is present, the host obtains device information such as device type, vendor ID, revision, and the amount of PCI address space required to service the device.

The BCI-2004 contains two registers, BADM and BADLA, to define the PCI local address space requirements for the BCI-2004.

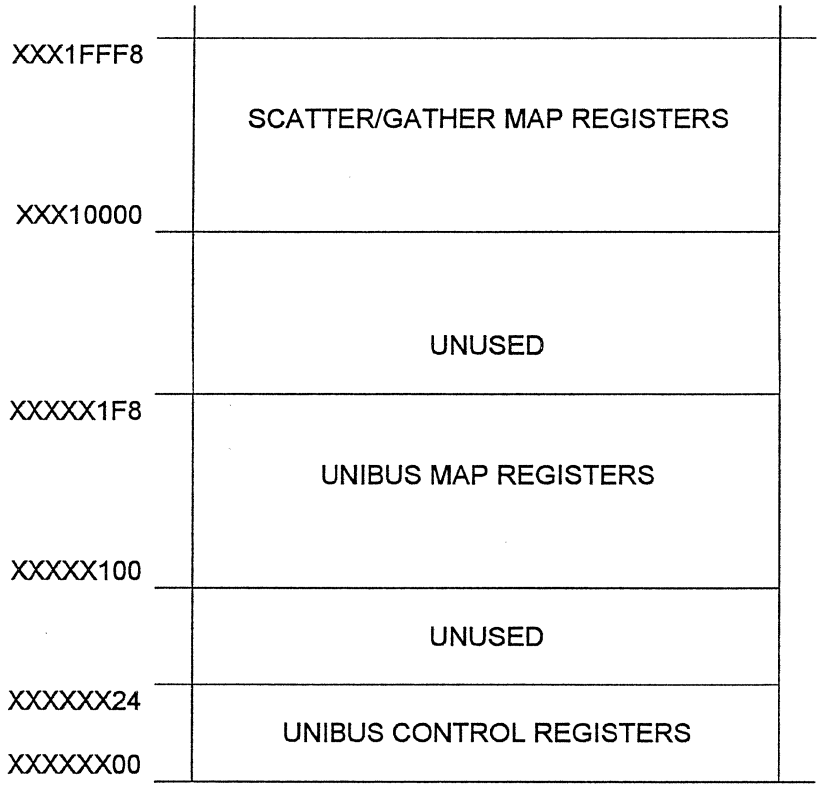
The PCI control address space is defined at configuration time by the PCI configuration register BADM. This register defines two address spaces, one for local configuration registers and the second as shared runtime registers.



X is defined by the BADM register, see Figure 4-11.

Figure 3-1: PCI Control Address Space

The Unibus control address space is defined at configuration time by the PCI configuration register BADLA. This register defines an address space of 128K bytes for adapter control registers.



X is defined by the BADLA register, see Figure 4-13.

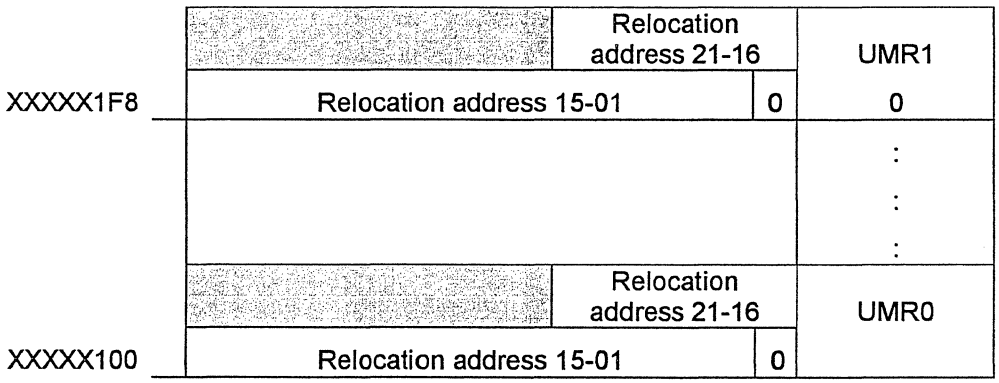
Figure 3-2: Unibus Control Address Space

The Unibus control address space is defined at configuration time by the PCI configuration register BADLA. This register defines addresses for the ten Unibus control and status registers.

XXXXXX24	TPR
XXXXXX20	MAP CONTROL
XXXXXX1C	SCATTER/GATHER CSR
XXXXXX18	UNIBUS ADDRESS
XXXXXX14	UNIBUS MAINTENANCE
XXXXXX10	UNIBUS PRIORITY
XXXXXX0C	UNIBUS VECTOR
XXXXXX08	UNIBUS DATA
XXXXXX04	PCI ADDRESS REGISTER
XXXXXX00	CONTROL AND STATUS

X is defined by the BADLA register, see Figure 4-13.

Figure 3-3: Unibus Control Register Address Space



X is defined by the BADLA register, see Figure 4-13.

Figure 3-4: Unibus MAP Registers

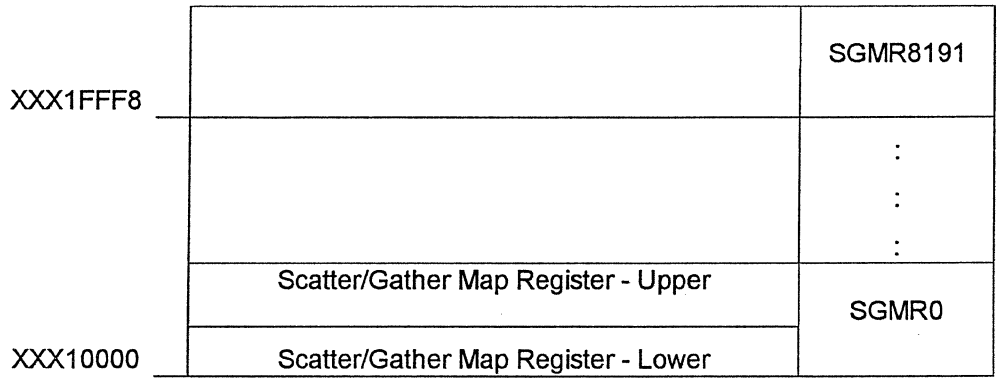


Figure 3-5: Scatter/Gather Map Registers

Unibus PIO Operation

A PCI host can access the entire 256 K bytes of Unibus space by using the Unibus Address register on the BCI-2004. The upper 8 K bytes is the Unibus I/O page. The five types of Unibus data transfers supported are read word, data-input-pause, write word, write lower byte, and write upper byte.

The Unibus Map Registers are accessed directly at 100-1FF.

The cycle type is controlled by the C0 and C1 bits in the UAR. Setting C0 and clearing C1 selects a data-input-pause access. A Data-input-pauses access is a Unibus read followed by a Unibus write byte or word access. A Data-input-pause access is used to prevent a Unibus location from being modified by a DMA or interrupt device before a write access is completed. A Data-input-pause access must be followed by a Unibus write access to complete the Data-input-pause operation.

When a Unibus access is requested, the BCI-2004 must acquire mastership of the Unibus in order to perform the Unibus access. If the BCI-2004 does not have Unibus mastership, the BCI-2004 asserts NPR on the Unibus to request mastership. Unibus access may be delayed due to a DMA or interrupt cycle in process or due to a faulty Unibus condition. If the BCI-2004 does not obtain mastership of the Unibus within 50 microseconds, internal flag XER in the Unibus DATA register is set to indicate a transfer error. When XER is set, the PCI bus access to the Unibus is completed although data may not transfer correctly. When the BCI-2004 obtains Unibus mastership, the PIO access to the Unibus can begin.

A Unibus word read is performed when the UAR is written with C1 set to zero. Only 16-bit Unibus reads are supported. During the read access of the Unibus, the BCI-2004 places the PIO address on the Unibus and asserts MSYN. Each Unibus slave device decodes the address on the Unibus to determine if it is selected. A Unibus slave device places its data on the Unibus and asserts SSYN if selected. The BCI-2004 stores the Unibus data from the slave

and de-asserts MSYN. The Unibus slave device de-asserts SSYN and removes its data from the Unibus, completing the Unibus read cycle. Reading the bus only starts an operation. The PCI bus master must check the DONE bit in the Unibus Data Register to determine when the Unibus read data is available. When the DONE bit is set, read data is valid and the Unibus read access is completed. You must loop on reading the data register, until the DONE bit is set. The time should be 500ns or more between reads of the data register to allow DMA cycles to occur between reads. When the DONE bit is set, either the XER bit will also be set (NXM error), or the low 16 bits will contain the data read from the bus. Unibus devices only perform word read operations. If a PCI byte read is specified, a Unibus word read occurs and the proper byte is delivered to the PCI master. The PCI bus access is completed when the BCI-2004 supplies the read data to the PCI bus.

A Unibus write occurs when the UAR is written with C1 set to one. When performing a 16-bit write to the Unibus, first write the data to the UDR. Then write the address to the UAR, with address bit 0 cleared, C1 set, and C0 cleared. To do a byte write, duplicate the data to be written in both bytes, and write to the UDR. Then write the address to the UAR, with C1 and C0 both set. After starting a write, loop on the data register until DONE sets, then check the XER bit. During the write access to the Unibus, the address, data and C1 signals are asserted on the Unibus by the BCI-2004. The BCI-2004 then asserts MSYN to inform slave devices that address, data and control information is valid on the Unibus. Unibus slave devices decode the address on the Unibus to determine if selected. A Unibus slave device stores the Unibus data and asserts SSYN if selected. The BCI-2004 de-asserts MSYN and removes address, data and C1 from the Unibus. The Unibus slave device then de-asserts SSYN, completing the Unibus write operation. The DONE flag in the Unibus Data Register is cleared on the start of a Unibus access and sets when the Unibus write cycle is completed. The DONE flag must be set before beginning another Unibus access.

Some Unibus devices require that the BIS(B) and BIC(B) instructions generate Data-Input-Pause(DATIP) bus cycles. To have the BCI-2004 do these DATIP cycles, set C0 and Clear C1. For byte DATIP cycles, address bit 0 should be cleared for the read, but set to the desired value for the write-back. DATIP operations are similar to read operations except that after the DATIP read is completed, the host must write back to the same Unibus address without releasing the bus. DATIP cycles block DMA or interrupt cycles from occurring between the read and write portions of the operation, which if allowed to occur, could cause data corruption. The BCI-2004 does not need to wait to gain Unibus mastership during the write since bus mastership is retained from the read portion of the operation. The BCI-2004 immediately places the address, data and C1 signal on the Unibus. The BCI-2004 then asserts MSYN. The addressed Unibus device stores the received data and asserts SSYN. Then, the BCI-2004 de-asserts MSYN. The slave device de-asserts SSYN completing the Unibus write cycle.

If a Unibus device fails to respond within 15 microseconds after the assertion of MSYN, the internal BCI-2004 flag XER is set in the Unibus Data Register. If the Unibus time-out occurs during a PCI bus read access, then the BCI-2004 completes the PCI bus cycle after setting the XER flag. The data on a Unibus time-out should be considered invalid and discarded. The data written to a Unibus during a Unibus time-out should be considered discarded.

Unibus DMA Operation

When DMA is enabled, all Unibus DMA accesses, except DMA to Unibus I/O address space, are to PCI local bus memory. The Unibus DMA addresses are mapped to the PCI bus. Three Local Configuration Registers are used to define Unibus to PCI accesses, The three registers are Local Range, Local Base Address, and PCI Base Address registers.

Five internal Unibus Control Registers are used to control DMA operation. The five registers are Control & Status Register (CSR), Scatter/Gather Control & Status Register (SGCSR), Scatter/Gather Map Registers (SGMR), Map Control & Status Register (MCSR), and Unibus Map Registers (UMR). The CSR is used to enable DMA and to check for errors. The SGCSR is used to enable interrupts and used to verify address mapping in diagnostic mode. SGMRs are made up of 8192 registers used to form the upper 23 bits of a 32-bit DMA address, bits 31-9. The upper 13 bits of the DMA Unibus address, bits 22-9, are used to select 1 of 8192 registers. Each SGMR also contains bits to specify Byte Offset, Page Not Present, and Page Valid. . MCSR is used to enable Unibus mapping. UMR consists of 31 registers emulating the functions of the Unibus Map found in PDP11 systems. The values programmed into these registers are used to convert the 18-bit Unibus address to a 22-bit address. The MCSR and UMRs are assigned Unibus addresses but can be only accessed from the host and not from the Unibus.

When enabled, DMA transfers are independent of the host and occur on demand from any Unibus master. Multiple DMA devices can be enabled simultaneously with arbitration of the Unibus performed by the BCI-2004. Only one Unibus master can have ownership of the Unibus at a time. Five types of DMA transfers are supported including read word, write word, write byte, read-modify-write word, read-modify-write byte. DMA transfers to Unibus I/O addresses are blocked and are not passed to the PCI bus but data can be transferred to any responding Unibus I/O device.

During a Unibus DMA sequence, if a Unibus SACK signal is not received by the BCI-2004 within approximately 10 microseconds of the BCI-2004 asserting signal NPG on the Unibus, an error condition occurs causing the BCI-2004 to set the GER flag and the DMA arbitration sequence is aborted.

Unibus Interrupt Operation

The BCI-2004 supports all four Unibus interrupt levels, although only two can be used at a time. The two levels used are selected with jumpers on the CAU-2001 or CAU-2003 Unibus module. The BRA and BRB fields of the CSR must be set to match the jumpers. The modules are shipped with BR4 and BR5 selected. This corresponds to zero in BRA and BRB.

The Unibus interrupts can be enabled or disabled under program control. The BCI-2004 controller contains an internal priority register which can be programmed by the PCI host to establish priority. The value stored in the priority register determines the level of Unibus

interrupts passed on to the host for processing. When an interrupt request is received by the BCI-2004, the controller compares the level of the request to the value in the register. If the Unibus interrupt is a higher priority than the value contained in the internal register and the interrupt enable bit is set, the interrupt is passed on to the PCI bus.

A Unibus interrupt is granted when the BPR is written with the Grant Enable (GNT) bit set and a request is present which is higher than the value being written into the priority field. While the grant is in progress, the Grant Busy (GBSY) bit is set in the Bus Vector Register (BVR). The host services the interrupt by reading the BCI-2004 Control and Status register to determine the type of interrupt service requested. In this case, the host determines service for a Unibus interrupt is requested. The host reads the internal vector register to obtain the vector of the interrupting device. After reading the vector, the PCI bus interrupt is cleared. The host uses the vector to determine the type of service requested by a Unibus device and performs the proper operations to satisfy the request.

There are several of ways of handling bus interrupts:

1) A PCI interrupt may be generated when a grantable request is present.

2) Status may be checked to determine when a grantable request is present.

3) A grant may be attempted at any time.

For the first two methods, update the Priority register every time the PSW is changed. Set the IEN bit at the same time. To generate a PCI interrupt, bits 8 and 11 of the PLX Interrupt Control/Status register (ICSK) must be set. For method #2, check either the INT bit (14) of the CSR, or bit 15 if the ICSR. Checking the ICSR register is preferred, as it is slightly faster.

During a Unibus interrupt sequence, if a Unibus SACK signal is not received by the BCI-2004 within approximately 10 microseconds of the BCI-2004 asserting BUS BG4, BG5, BG6, or BG7 on the Unibus, the BCI-2004 aborts the grant and clears the GBSY and Vector Valid (VAV) bits in the BVR.

4 Registers

Register Description Format

This chapter discusses each of the BCI-2004 registers.

The bit assignments are shown for each register with the most significant bit shown at the left and the least significant bit shown on the right. Bit numbers shown correspond to the PCI bits.

The BCI-2004 contains five groups of registers: PCI configuration registers, Local Configuration registers, Shared Runtime registers, Local DMA registers, and Unibus registers. The following pages describe the operation of each group of registers.

PCI configuration registers conform to the *PCI Local Bus Specification* Revision 2.1, published by the PCI Special Interest Group. The Local Configuration, Shared Runtime, and Local DMA registers are implemented by the PLX 9060—the device used by the BCI-2004 to interface to the PCI bus.

PCI Bus Configuration Registers

The BCI-2004 controller contains a unique 256-byte region called configuration header space. Portions of this configuration header space are mandatory in order for a PCI controller to be in full compliance with the PCI specification. This section describes each register contained within the configuration register set.

Local Addr*	31 24 23 16 15 08 07 00				PCI Addr
00h	Device ID (DID)		Vendor ID (VID)		00h
04h	Status (STS)		Command (CMD)		04h
08h	Class Code (CLCD)			Revision ID (RID)	08h
0Ch	Self Test (BIST)	Header Type (HDR)	Latency Timer (LAT)	Cache Line Size (CALN)	0Ch
10h	PCI Base Address for Memory Mapped Runtime Registers (BADM)				10h
14h	PCI Base Address for I/O Mapped Runtime Registers (BADIO)				14h
18h	PCI Base Address for Local Address Space 0 (BADLA)				18h
1Ch	PCI Base Address Register (PCIBAD)				1Ch
20h	PCI Base Address Register (PCIBAD)				20h
24h	PCI Base Address Register (PCIBAD)				24h
28h	PCI Base Address Register (PCIBAD)				28h
2Ch	PCI Base Address Register (PCIBAD)				2Ch
30h	PCI Expansion ROM Base Register (EXROM)				30h
34h	Reserved				34h
38h	Reserved				38h
3Ch	Max_Lat (MAXLAT)	Min_Gnt (MINGNT)	Interrupt Pin (INTPIN)	Interrupt Line (INTLN)	3Ch

* Offset from chip select address

Shaded areas are not available for customer use.

Figure 4-1: PCI Configuration Registers

PCI Configuration ID Register (IDR) Offset 00h

The read-only Identification register contains the vendor and device identification numbers. Write operations have no effect on this register.

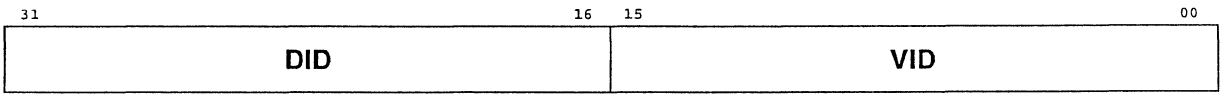


Figure 4-2: Identification Register

Bit	Name	Function	Read	Write	Value after Reset
15-00	VID	Vendor ID. This field identifies the manufacturer of the device.	Yes	Local only	1356h
31-16	DID	Device ID. This field identifies the particular device.	Yes	Local only	0013h

PCI Command Register (CMD) Offset 04h

The PCI Command register contains read/write PCI command information.

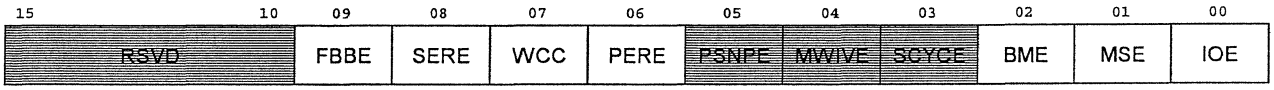


Figure 4-3: PCI Command Register Bits

Bit	Name	Function	Read	Write	Value after Reset
00	IOE	I/O Space. A value of 1 allows the device to respond to I/O space accesses. A value of 0 disables the device from responding to I/O space accesses.	Yes	Yes	0
01	MSE	Memory Space. A value of 1 allows the device to respond to memory space accesses. A value of 0 disables the device from responding to memory space accesses.	Yes	Yes	0
02	BME	Master Enable. A value of 1 allows the device to behave as a bus master. A value of 0 disables the device from generating bus master accesses.	Yes	Yes	0
03	SCYCE	Special Cycle. This bit is not supported.	Yes	No	0
04	MWIVE	Memory Write/Invalidate. This bit is not supported.	Yes	No	0
05	PSNPE	VGA Palette Snoop. This bit is not supported.	Yes	No	0
06	PERE	Parity Error Response. A value of 0 indicates that a parity error is ignored and operation continues. A value of 1 indicates that parity checking is enabled.	Yes	Yes	0
07	WCC	Wait Cycle Control. Control whether or not the device does address/data stepping. A 0 value indicates the device never does stepping. A value of 1 indicates that the device always does stepping. This value is hardwired to 0.	Yes	No	0
08	SERE	SERR# Enable. A value of 1 enables the SERR# driver. A value of 0 disables the driver.	Yes	Yes	0

Bit	Name	Function	Read	Write	Value after Reset
09	FBBE	Fast Back-to-Back Enable. Indicates what type of fast back-to-back transfers a Master can perform on the bus. A value of 1 indicates that fast back-to-back transfers can occur to any agent on the bus. A value of 0 indicates fast back-to-back transfers can only occur to the same agent as the previous cycle.	Yes	No	0
15-10	RSVD	Reserved	Yes	No	0

PCI Status Register (STS) Offset 06h

The PCI Status register is a read/write clear register containing the PCI status information. Most status bits within this register are designated as "write clear," meaning that in order to clear a given bit the bit must be written as a one. All bits written with a zero are left unchanged.

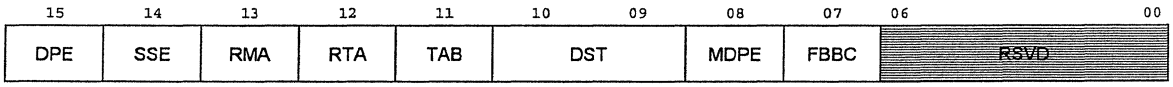


Figure 4-4: PCI Status Register Bits

Bit	Name	Function	Read	Write	Value after Reset
06-00	RSVD	Reserved	Yes	No	0
07	FBBC	Fast Back-to-Back Capable. When this bit is set to a 1, it indicates the adapter can accept fast back-to-back transactions. A 0 indicates the adapter cannot.	Yes	No	1
08	MDPE	Master Data Parity Error Detected. This bit is set to a 1 when three conditions are met: 1) the BCI-2004 asserted PERR# itself or observed PERR# asserted; 2) the BCI-2004 was the bus master for the operation in which the error occurred; 3) the Parity Error Response bit in the Command Register is set. Writing a 1 to this bit clears the bit (0).	Yes	Yes	0
10-09	DST	DEVSEL Timing. Indicates timing for DEVSEL# assertion. A value of 01 is medium.	Yes	No	01
11	TAB	Target Abort. When this bit is set to a 1, this bit indicates the BCI-2004 has signaled a target abort. Wiring a 1 to this bit clears the bit (0).	Yes	Yes	0
12	RTAB	Received Target Abort. When set to a 1, this bit indicates the BCI-2004 has received a target abort signal. Writing a 1 to this bit clears the bit (0).	Yes	Yes	0
13	RMAB	Received Master Abort. When set to a 1, this bit indicates the BCI-2004 has received a master abort signal. Writing a 1 to this bit clears the bit (0).	Yes	Yes	0

Bit	Name	Function	Read	Write	Value after Reset
14	SSE	Signaled System Error. When set to a 1, this bit indicates the BCI-2004 has reported a system error on the SERR# signal. Writing a 1 to this bit clear the bit (0).	Yes	Yes	0
15	DPE	Detected parity Error. When set to a 1, this bit indicates the BCI-2004 has detected a PCI bus parity error, even if parity error handling is disabled (the parity Error Response bit in the Command register is clear). One of three conditions can cause this bit to be set: 1) the BCI-2004 detected a parity error during a PCI address phase; 2) the BCI-2004 detected a data parity error when it was the target of a write; 3) the BCI-2004 detected a data parity error when performing a master read operation. Writing a 1 to this bit clears the bit (0).	Yes	Yes	0

Revision Identification Register (RID) Offset 08h

The Revision Identification Register contains the eight-bit, read-only revision identification number of the BCI-2004. This field is initially cleared. Write operations have no effect on this field.

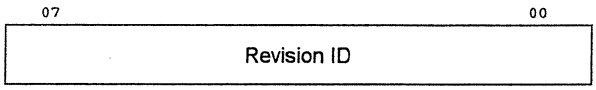


Figure 4-5: Revision Identification Register Bits

Bit	Name	Function	Read	Write	Value after Reset
07-00	RID	Revision ID. The revision level of the BCI-2004.	Yes	Local only	Current revision

PCI Class Code Register (CLCD) Offset 09-0Bh

The Class Code Register contains the BCI-2004 PCI class code. The field is divided into three one-byte fields as shown below.

Base Class	06h	Bridge Device
Sub-Class	80h	Other Bridge Type
Programming Information	00h	

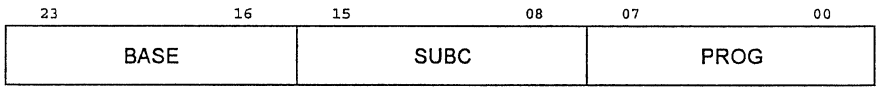


Figure 4-6: PCI Class Code Register Bits

Bit	Name	Function	Read	Write	Value after Reset
07-00	PROG	Specific register level programming interface (00h). No interface defined.	Yes	Local only	00
15-08	SUBC	Sub-class Encoding (80h). Other bridge device.	Yes	Local only	80h
23-16	BASE	Base Class Encoding. Bridge device.	Yes	Local only	06h

PCI Cache Line Size Register (CALN) Offset 0Ch

This register is hardwired to zero since the BCI-2004 does not use Memory Write and invalidate PCI bus cycle.

Figure 4-7: Cache Line Size Register

Bit	Name	Function	Read	Write	Value after Reset
07-00	CLS	Cache Line Size. System cache line size in units of 32-bit words. Not supported.	Yes	No	0

PCI Latency Timer Register (LAT) Offset 0Dh

The read/write latency timer register is used when the BCI-2004 is bus master. The register contains the number of bus clocks remaining for the BCI-2004 to maintain control of the bus. When the BCI-2004 is granted the bus and asserts PCI signal FRAME, the nonzero value for this register is internally decremented. Until the latency timer reaches zero, the BCI-2004 can ignore the removal of bus grant and may continue use of the bus for data transfers.

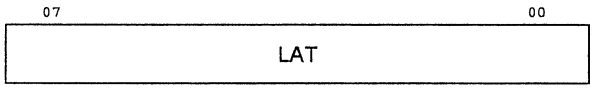


Figure 4-8: Latency Timer Register

Bit	Name	Function	Read	Write	Value after Reset
07-00	LAT	Latency Timer. Specifies in units of PCI bus clocks, the amount of time the BCI-2004, as a bus master, can burst data on the PCI bus.	Yes	Yes	0

PCI Header Type Register (HDR) Offset 0Eh

The Header Type register is an 8-bit register consisting of two fields: Read-only bits 6-0 define the format for bytes 10h through 3Fh of the device configuration header, and read/write bit 7 establishes the BCI-2004 as a single function device.

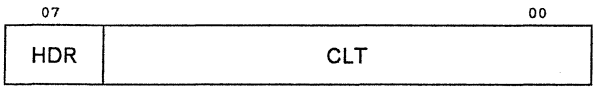


Figure 4-9: Header Type Register

Bit	Name	Function	Read	Write	Value after Reset
06-00	CLT	Configuration Layout type. Specifies the layout of bytes 10h through 3Fh in configuration space. Only encoding 0 is defined. All other encodings are reserved.	Yes	Local only	0
07	HDR	Header Type. A 1 indicates multiple functions, a 0 indicates a single function.	Yes	Local only	0

PCI Built-in Self Test Register (BIST) Offset 0Fh

The Built-in Self Test Register is used to specify self test which the BCI-2004 does not support.

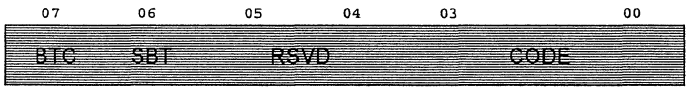


Figure 4-10: Built-in Self Test Register

Bit	Name	Function	Read	Write	Value after Reset
03-00	CODE	A value of 0 means the device has passed its test. Non-zero values mean the device failed. Device specific failure codes can be encoded in the non-zero value.	Yes	Local only	0
05-04	RSVD	Reserved, device returns 0.	Yes	No	0
06	SBT	PCI writes a 1 to invoke BIST. Generates an interrupt to local bus. Local bus resets the bit when BIST is complete. Software should fail device if BIST is not complete after 2 seconds.	Yes	Yes	0
07	BTC	Return 1 if device supports BIST. Return 0 if the device is not BIST compatible.	Yes	Local Bus	0

PCI Base Address Register for Memory Access to Runtime Registers (BADM)

Offset 10h

Base Address Register for Memory Access to Runtime Registers provides a mechanism for assigning memory space for the Local Configuration and Shared Runtime registers. The actual memory locations these registers respond to are determined by first interrogating this Base Address Register to ascertain the space required, and then writing to the register's high-order field to specify the physical location of the registers. Bit 0 is used to select memory space.

The size of the address space defined by this Base Address Register is determined by writing all ones to the register from the PCI bus and then reading the register back. The number of zeros contained in bits 31 through 4 reveals the amount of memory space required.

After the size of the address space has been determined, the system can allocate memory space for this region and assign it by writing back a value into the bits which contained ones in the Base Address Register. The value written back is the physical address assigned to the Local Configuration and Shared Runtime registers. For example, the Base Address Register returns FFFFFF80h and is then written with the value 00000300h. This means that the PCI operation registers can be selected for memory addresses between 00000300h through 0000037Fh for this example. The base address value must be on a natural binary boundary for the required size (e.g., 300h, 380h, 400h are valid; 338h is not valid.)

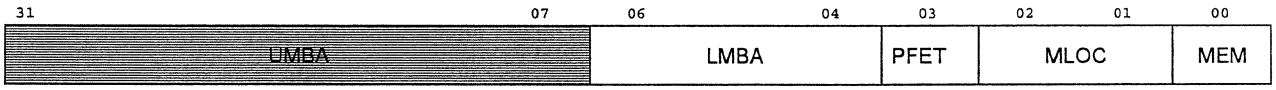


Figure 4-11: PCI Base Address Register for Memory Access to Runtime Registers

Bit	Name	Function	Read	Write	Value after Reset
00	MEM	Memory Space Indicator. A value of 0 indicates register maps into memory space. A value of 1 indicates the register maps into I/O space.	Yes	No	0
02-01	MLOC	Location of register: 00 Locate anywhere in 32-bit memory address space 01 Locate below 1 Mbyte memory address space 10 Locate anywhere is 64 bit memory address space 11 Reserved	Yes	No	0
03	PFET	Prefetchable. A value of 1 indicates there are no side effects on reads.	Yes	No	0

Bit	Name	Function	Read	Write	Value after Reset
06-04	LMBA	Lower Memory Base Address. Memory base address for access to runtime registers (default 128 bytes).	Yes	No	0
31-07	UMBA	Upper Memory Base Address. Memory base address for access to runtime registers.	Yes	Yes	0

Base Address Register for I/O Access to Runtime Registers (BADIO)

Offset 14h

Not used by the BCI-2004.

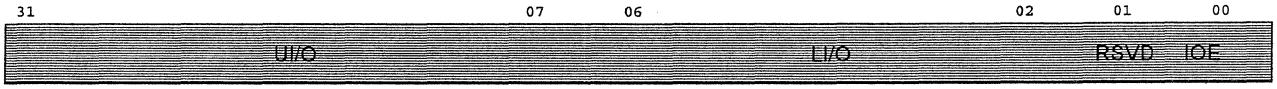


Figure 4-12: PCI Base Address Register for I/O Access to Runtime Registers

Bit	Name	Function	Read	Write	Value after Reset
00	MEM	Memory Space Indicator. A value of 0 indicates register maps into memory space. A value of 1 indicates the register maps into I/O space.	Yes	No	1h
01	RSVD	Reserved.	Yes	No	0
06-02	LI/O	Lower I/O Base Address. Base address for I/O access to runtime registers. Default is 128 bytes.	Yes	No	0
31-07	UI/O	Upper I/O Base Address. Base address for I/O access to runtime registers.	Yes	Yes	0

PCI Base Address Register for Memory Access to Local Address Space 0 (BADLA)

Offset 18h

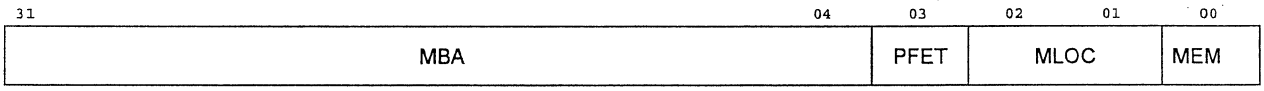


Figure 4-13: PCI Base Address Register for Memory Access to Local Address Space 0

Bit	Name	Function	Read	Write	Value after Reset
00	MEM	Memory Space Indicator. A value of 0 indicates register maps into memory space. A value of 1 indicates the register maps into I/O space.	Yes	No	0
02-01	MLOC	Location of register: 00 Locate anywhere in 32-bit memory address space 01 Locate below 1 Mbyte memory address space 10 Locate anywhere is 64 bit memory address space 11 Reserved	Yes	No	0
03	PFET	Prefetchable. A value of 1 indicates there are no side effects on reads.	Yes	No	0
31-04	MBA	Memory Base Address. Memory base address for access to local address space.	Yes	Yes	0

PCI Base Address Register (PCIBAD) Offset 1Ch, 20h, 24h, 28h, 2Ch

Figure 4-14: PCI Base Address Register

Bit	Name	Function	Read	Write	Value after Reset
31-00	RSVD	Reserved	Yes	No	0

PCI Expansion ROM Base Register (EXROM) Offset 30h

The 32-bit expansion base address ROM register provides a mechanism for assigning a space within physical memory for an expansion ROM. The use of this register is not required to support the functions of the BCI-2004.

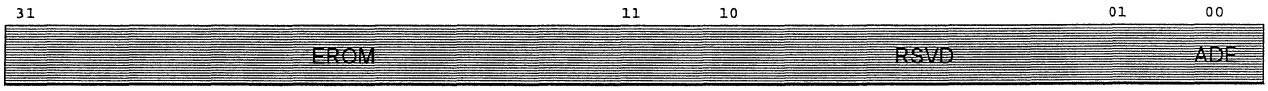


Figure 4-15: PCI Expansion ROM Base Register

Bit	Name	Function	Read	Write	Value after Reset
00	ADE	Address Decode Enable. A value of 1 indicates the device accepts accesses to the expansion ROM address. A value of 0 indicates the device does not accept accesses to expansion ROM space.	Yes	Yes	1
10-01	RSVD	Reserved	Yes	No	0
31-11	EROM	Expansion ROM Base Address (upper 21 bits)	Yes	Yes	0

PCI Interrupt Line Register (INTLN) Offset 3Ch

The Interrupt Line Register indicates the interrupt routing for the BCI-2004.

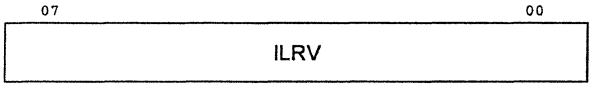


Figure 4-16: Interrupt Line Register

Bit	Name	Function	Read	Write	Value after Reset
07-00	ILRV	Interrupt Line Routing Value. Value indicates which input of the system interrupt controller(s) the device's interrupt line is connected to.	Yes	Yes	0

PCI Interrupt Pin Register (INTPIN) Offset 3Dh

The Interrupt Pin field is used to specify which PCI interrupt pin is connected to the BCI-2004 interrupt signal.

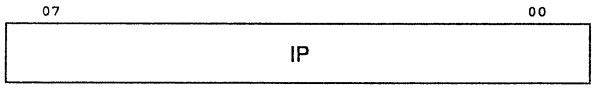


Figure 4-17: Interrupt Pin Register

Bit	Name	Function	Read	Write	Value after Reset
07-00	IP	Interrupt Pin Register. Indicates which interrupt pin the device uses. The following values are decoded: 0 = No interrupt pin 1 = INTA# 2 = INTB# 3 = INTC# 4 = INTD#	Yes	Local only	1h

PCI Min_Gnt Register (MINGNT) Offset 3Eh

The Minimum Grant field may be optionally used by the BCI-2004 when bus master to specify how long of a burst period is needed.

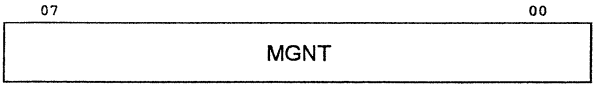


Figure 4-18: Min_Gnt Register

Bit	Name	Function	Read	Write	Value after Reset
07-00	MGNT	Min_Gnt. Used to specify how long a burst period the device needs, assuming a clock rate of 33 MHz. Value is multiple of 1/4 usec increments.	Yes	Local only	0

PCI Max_Lat Register (MAXLAT) Offset 3Fh

The Maximum Latency field may be optionally used by the BCI-2004 when bus master to specify how often the BCI-2004 needs PCI bus access.

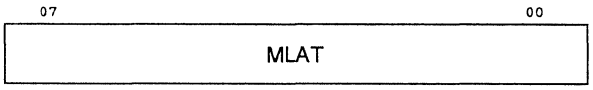


Figure 4-19: Max_Lat Register

Bit	Name	Function	Read	Write	Value after Reset
07-00	MLAT	Max_Lat. used to specify how often the device needs to gain access to the PCI bus. Value is multiple of 1/4 usec increment.	Yes	Local only	0

Local Configuration Registers

Figure 4-20 lists the local configuration registers.

Local Addr*	31 24 23 16 15 08 07 00	PCI Addr
80h	Local Address Range 0 (LAR0)	00h
84h	Local Base Address 0 ((LBA0)	04h
88h	Local Register (LR)	08h
8Ch	Local Register (LR)	0Ch
90h	Expansion PROM Address Range (EPAR)	10h
94h	Expansion PROM Base Address (EPBA)	14h
98h	Local Region Descriptor (LRD)	18h
9Ch	Direct Master Address Range (DMAR)	1Ch
A0h	Direct Master Base Address (DMBA)	20h
A4h	Direct Master Configuration Address (DMCA)	24h
A8h	Direct Master Control (DMC)	28h
ACh	Direct Master IO/CFG Address (DMIO)	2Ch

Shaded areas are not available for customer use.

Figure 4-20: PCI Local Configuration Registers

Local Address Range 0 Register (LAR0)

Local Offset 80h
PCI Offset 00h

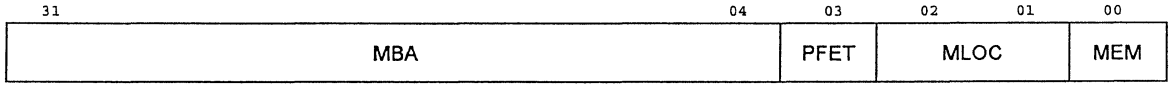


Figure 4-21: Local Address Range 0 Register

Bit	Name	Function	Read	Write	Value after Reset
00	MEM	Memory Space Indicator. A value of 0 indicates local address space 0 maps into PCI memory space. A value of 1 indicates address space 0 maps into PCI I/O space.	Yes	Yes	0
02-01	MLOC	If mapped into memory space, encoding is as follows: 00 Locate anywhere in 32-bit PCI address space 01 Locate below 1 Mbyte PCI address space 10 Locate anywhere is 64 bit PCI address space 11 Reserved If mapped into I/O space, bit 1 must be a 0, and bit 2 is included with bits 3 through 31 to indicate decoding range.	Yes	Yes	0
03	PFET	Prefetchable. If mapped into memory space, a 1 indicates that reads are pre-fetchable. If mapped into I/O space, bit 3 is included with bits 2 through 31 to indicate decoding range.	Yes	Yes	0
31-04	MBA	Specifies which PCI address bits will be used to decode a PCI access to local bus space 0. Each of the bits corresponds to an address bit. Bit 31 corresponds to address bit 31. A value of 1 should be written to all bits that should be included in decode and a 0 to all others (used in conjunction with PCI Configuration register 18h). The default is 2 Mbytes.	Yes	Yes	FFFE0000h

Local Base Address 0 Register (LBA0)

Local Offset 84h
PCI Offset 04h

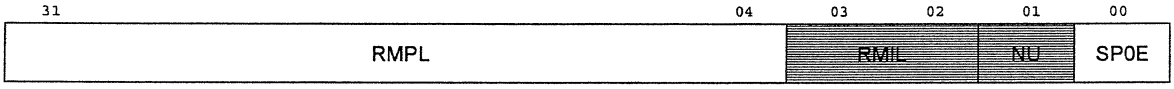


Figure 4-22: Local Base Address 0 Register

Bit	Name	Function	Read	Write	Value after Reset
00	SP0E	Space 0 Enable. A 1 value enables decode of PCI addresses for direct slave access to local space 0. A value of 0 disables decode.	Yes	Yes	1
01	NU	Not Used.	Yes	Yes	0
03-02		If local space 0 is mapped into memory space, these bits are not used. If local space 0 is mapped into I/O space, these bits are included with bits 4 through 31 for re-mapping.	Yes	Yes	0
31-04		Re-map of PCI Address to Local Address Space 0 into a local address space. The bits in this field re-map (replace) the PCI address bits used in decode as the local address bits.	Yes	Yes	0

Local Registers (LR)

Local Offset 88h, 8Ch
PCI Offset 08h, 0Ch

Figure 4-23: Local Register

Bit	Name	Function	Read	Write	Value after Reset
31-00	RSVD	Reserved.	Yes	No	FFh

Expansion PROM Address Range (EPAR)

Local Offset 90h
PCI Offset 10h

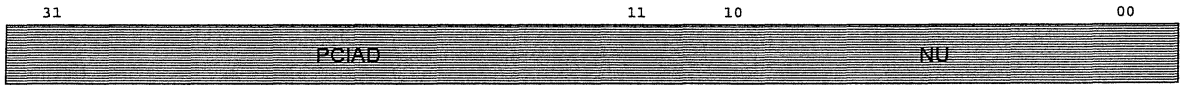


Figure 4-24: Expansion PROM Address Range

Bit	Name	Function	Read	Write	Value after Reset
10-00	NU	Not Used.	Yes	Yes	0
31-11	PCIAD	PCI Address Decode. Specifies which PCI address bits are used to decode a PCI to local bus expansion ROM. Each of the bits corresponds to an address bit. Bit 31 corresponds to address bit 31. A value of 1 should be written to all bits that should be included in decode and a 0 to all others. Used in conjunction with Expansion PROM Address Range (PCI Configuration register 30h). Default is 64 Kbytes.	Yes	Yes	0

Expansion PROM Base Address Register (EPBA)

Local Offset 94h
PCI Offset 14h

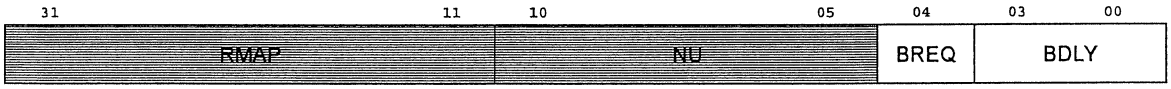


Figure 4-25: Expansion PROM Base Address Register

Bit	Name	Function	Read	Write	Value after Reset
03-00	BDLY	Direct Slave BREQo Delay Clocks. (Number of local bus clocks in which a Direct Slave HOLD request is pending and a Local Direct Master access is in progress and not being granted the bus (HOLDA) before asserting BREQo. Once asserted, BREQo remains asserted until the BCI-2004 receives HOLDA (LSB=8 clocks).	Yes	Yes	0
04	BREQ	Local Bus BREQo Enable. A 1 value enables assertion of the BREQo output.	Yes	Yes	0
10-05	NU	Not Used.	Yes	No	0
31-11	RMAP	Re-map of PCI Expansion ROM Space into a Local Address Space. The bits in this field re-map (replace) the PCI address bits used in decode as the local address bits.	Yes	Yes	0

Local Region Descriptor (LRD)

Local Offset 98h
PCI Offset 18h

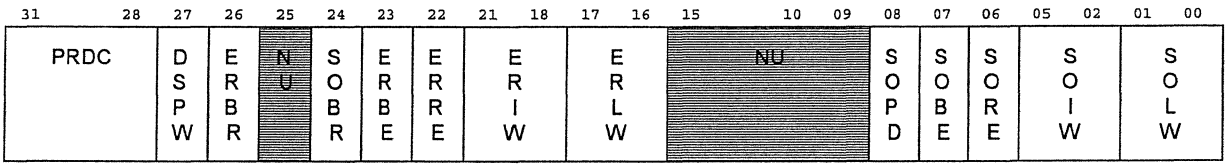


Figure 4-26: Local Region Descriptor Register

Bit	Name	Function	Read	Write	Value after Reset
01-00	SOLW	Memory Space 0 Local Bus Width. Programmable for Cx and Jx modes only. A value of 00 indicates a bus width of 8 bits, a value of 01 indicates a bus width of 16 bits, a value of 10 or 11 indicates a bus width of 32 bits. The bus width is forced to 16 bits for Sx mode.	Yes	Yes	Sx mode 01 Jx mode 11 Cx mode 11
05-02	SOIW	Memory Space 0 Internal Wait States (data to data).	Yes	Yes	0
06	SORE	Memory Space 0 Ready Input Enable. A 1 value enables Ready input. A value of 0 disables the Ready input.	Yes	Yes	1
07	SOBE	Memory Space 0 Bterm Input Enable. A 1 value enables Bterm input. A value of 0 disables the Bterm input.	Yes	Yes	0
08	SOPD	Memory Space 0 Prefetch Disable. A 1 value disables read prefetching.	Yes	Yes	1
15-09	NU	Not Used.	Yes	Yes	0
17-16	ERLW	Expansion ROM Space Local Bus Width. Programmable for the Cx and Jx modes only. A value of 00 indicates a bus width of 8 bits, a value of 01 indicates a bus width of 16 bits, a value of 10 or 11 indicates a bus width of 32 bits. The bus width is forced to 8 bits.	Yes	Yes	Sx mode 01 Jx mode 11 Cx mode 11
21-18	ERIW	Expansion ROM Space Internal Wait States (data to data).	Yes	Yes	0
22	ERRE	Expansion ROM Space Ready Input Enable. A 1 value enables Ready input. A value of 0 disable the Ready input.	Yes	Yes	0

Bit	Name	Function	Read	Write	Value after Reset
23	ERBE	Expansion ROM Space Bterm Input Enable. A 1 value enables Bterm input. A value of 0 disables the Bterm input.	Yes	Yes	0
24	SOBR	Memory Space 0 Burst Enable. A 1 value enables bursting. A value of 0 disables bursting.	Yes	Yes	1
25	NU	Not Used.	Yes	No	0
26	ERBR	Expansion ROM Space Burst Enable. A 1 value enables bursting. A value of 0 disables bursting.	Yes	Yes	0
27	DSPW	Direct Slave PCI Write Mode. A 0 indicates that the BCI-2004 should disconnect when the Direct Slave write FIFO is full. A 1 indicates that the BCI-2004 should de-assert TRDY when the write FIFO is full.	Yes	Yes	0
31-28	PRDC	PCI Target Retry Delay Clocks. Contains the value (multiplied by 8) of the number of PCI bus clocks after receiving a PCI-Local read or write access and not successfully completing a transfer. Only pertains to Direct Slave writes when bit 27 is set to 1.	Yes	Yes	15 (128 clocks)

Direct Master Address Range (DMAR)

Local Offset 9Ch
PCI Offset 1Ch

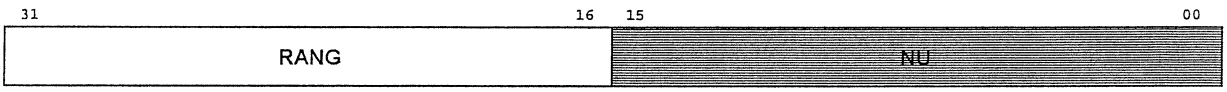


Figure 4-27: Direct Master Address Range

Bit	Name	Function	Read	Write	Value after Reset
15-00	NU	Not Used. (64 Kbyte increments)	Yes	No	0
31-16	RANG	Specifies which Local address bits are used to decode a Local to PCI bus access. Each of the bits corresponds to an address bit. Bit 31 corresponds to Address bit 31. A value of 1 should be written to all bits that should be included in decode and a 0 to all others.	Yes	Yes	8000h

Direct Master Base Address Register (DMBA)

Local Offset A0h
PCI Offset 20h

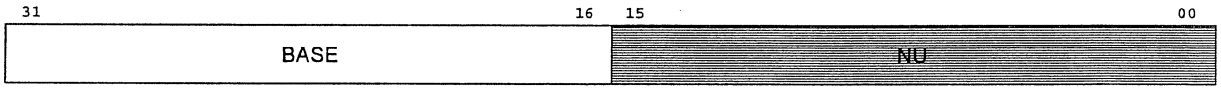


Figure 4-28: Direct Master Base Address Register

Bit	Name	Function	Read	Write	Value after Reset
15-00	NU	Not Used. (64 Kbyte increments)	Yes	No	0
31-16	BASE	Assigns a value to the bits used to decode a Local to PCI memory access.	Yes	Yes	8000h

Direct Master Configuration Address Register (DMCA)

Local Offset A4h
PCI Offset 24h

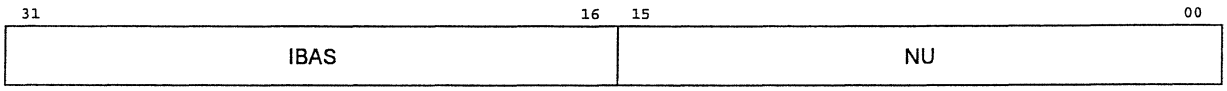


Figure 4-29: Direct Master Configuration Address Register

Bit	Name	Function	Read	Write	Value after Reset
15-00	NU	Not Used. (64 Kbyte increments)	Yes	No	0
31-16		Assigns a value to the bits used to decode a Local to PCI I/O or configuration access.	Yes	Yes	0000h

Direct Master Control (DMC)

Local Offset A8h
PCI Offset 28h

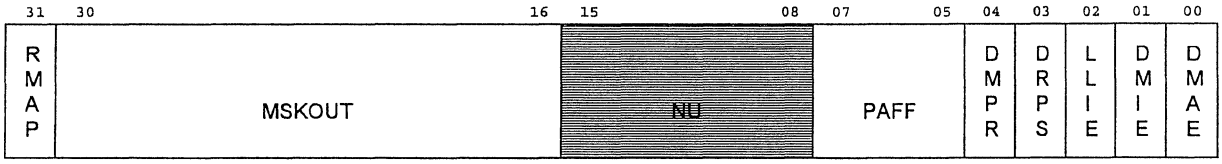


Figure 4-30: Direct Master Control Register

Bit	Name	Function	Read	Write	Value after Reset
00	DMAE	Direct Master Memory Access Enable. A 1 value enables decode of Direct Master memory accesses. A value of 0 disables decode of Direct master Memory accesses.	Yes	Yes	1
01	DMIE	Direct Master I/O Access Enable. A 1 value enables decode of Direct Master I/O accesses. A value of 0 disables decode of Direct Master I/o accesses.	Yes	Yes	0
02	LLIE	Local LOCK Input Enable. A 1 value enables LOCK input, enabling PCI Direct Master locked sequences. A value of 0 disables the Lock input.	Yes	Yes	0
03	DRPS	Direct master Read Prefetch Size Control. If this bit is set to a value of 0, the BCI-2004 continues to prefetch read data until the Direct Master access is finished. This may result in an additional 4 unneeded longwords being pre-fetched from the PCI bus. If this bit is set to a value of 1, the BCI-2004 reads up to 4 longwords from the PCI bus for each Direct Master burst read access. This mode must not be used for direct master burst reads that exceed 4 longwords.	Yes	Yes	0
04	DMPR	Direct Master PCI Read Mode. A value of 0 indicates that the BCI-2004 should release the PCI bus when the read FIFO becomes full. A value of 1 indicates that the BCI-2004 should keep the PCI bus and de-assert IRDY when the read FIFO becomes full.	Yes	Yes	0

Bit	Name	Function	Read	Write	Value after Reset
07-05	PAFF	Programmable Almost Full Flag. When the number of entries in the 8 deep direct master write FIFO exceed this value, the output pin DMFAF# is asserted low.	Yes	Yes	0
15-08	NU	Not Used.	Yes	No	0
30-16	MSK OUT	These bits are masked out by DMAR. Software should not write 1 to these bits.	Yes	Yes	0
31	RMAP	Re-map of Local to PCI Space into a PCI Address Space. This bit re-maps (replaces) the Local address bit used in decode as the PCI address bit.	Yes	Yes	0

Direct Master to PCI IO/CFG Address Register (DMIO)

Local Offset ACh
PCI Offset 2Ch

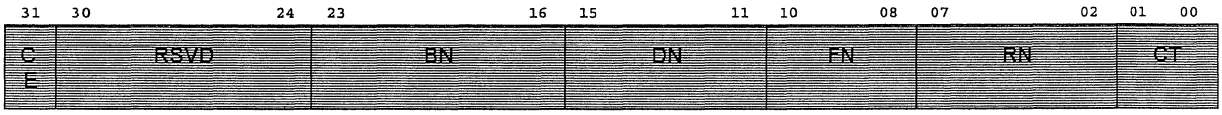


Figure 4-31: Direct Master to PCI IO/CFG Address Register

Bit	Name	Function	Read	Write	Value after Reset
01-00	CT	Configuration Type. 00 = Type 0, 01 = Type 1	Yes	Yes	0
07-02	RN	Register Number.	Yes	Yes	0
10-08	FN	Function Number.	Yes	Yes	0
15-11	DN	Device Number.	Yes	Yes	0
23-16	BN	Bus Number.	Yes	Yes	0
30-24	RSVD	Reserved.	Yes	Yes	0
31	CE	Configuration Enable. A value of 1 allows Local to PCI I/O accesses to be converted to a PCI configuration cycle. The parameters in this table are used to generate the PCI configuration address.	Yes	Yes	0

Shared Runtime Registers

Local Addr*	31 24 23 16 15 08 07 00	PCI Addr**
C0h	Mailbox Register 0 (MRB0)	40h
C4h	Mailbox Register 1 (MRB1)	44h
C8h	Mailbox Register 2 (MRB2)	48h
CCh	Mailbox Register 3 (MRB3)	4Ch
D0h	Mailbox Register 4 (MRB4)	50h
D4h	Mailbox Register 5 (MRB5)	54h
D8h	Mailbox Register 6 (MRB6)	58h
DCh	Mailbox Register 7 (MRB7)	5Ch
E0h	Local Doorbell Register (LDBR)	60h
E4h	PCI Doorbell Register (PDBR)	64h
E8h	Interrupt Control / Status (ICSR)	68h
ECh	EEPROM PCI I/O Control (EPIR)	6Ch

* Offset from chip select address.
** Offset from Runtime base address.

Shaded areas are not available for customer use.

Figure 4-32: Shared Runtime Registers

Mailbox Registers 0 Through 7 (MBR0 - 7)

Local Offset C0h,C4h,C8h,CCh,D0h,D4h,D8h,DCh
PCI Offset 40h,44h,48h,4Ch,50h,54h,58h,5Ch

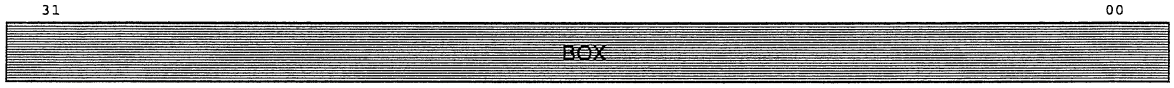


Figure 4-33: Mailbox Registers

Bit	Name	Function	Read	Write	Value after Reset
31-00	BOX	32-bit mailbox register.	Yes	Yes	0

Local Doorbell Register (LDBR)

Local Offset E0h
PCI Offset 60h

Figure 4-34: PCI to Local Doorbell Register

Bit	Name	Function	Read	Write	Value after Reset
31-00	BELL	Doorbell Register. A PCI master can write to this register and it generates a local interrupt to the local processor. The local processor can then read this register to determine which doorbell bit was asserted. The PCI master sets a doorbell by writing a 1 to a particular bit. The local processor can clear a doorbell bit by writing a 1 to that bit position.	Yes	Yes	0

PCI Doorbell Register (PDBR)

Local Offset E4h
PCI Offset 64h

Figure 4-35: Local to PCI Doorbell Register

Bit	Name	Function	Read	Write	Value after Reset
31-00	BELL	Doorbell Register. The local processor can write to this register and it generates a PCI interrupt. A PCI master can then read this register to determine which doorbell bit was asserted. The local processor sets a doorbell by writing a 1 to a particular bit. The PCI master can clear a doorbell bit by writing a 1 to that bit position.	Yes	Yes	0

Interrupt Control/Status Register (ICSR)

Local Offset E8h
PCI Offset 68h

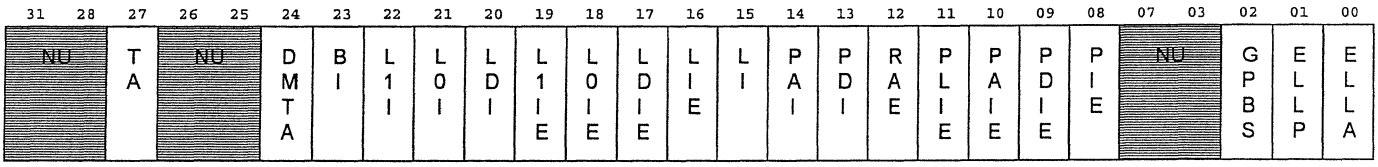


Figure 4-36: Interrupt Control/Status Register

Bit	Name	Function	Read	Write	Value after Reset
00	ELLA	Enable Local Bus LSERR#. A value of 1 enables the BCI-2004 to assert LSERR# interrupt output when the PCI bus Target Abort or Master Abort status bit is set in the PCI Status Configuration Register.	Yes	Yes	0
01	ELLP	Enable Local Bus LSERR# when a PCI parity error occurs during a BCI-2004 Master Transfer or a BCI-2004 Slave access.	Yes	Yes	0
02	GPBS	Generate PCI Bus SERR#. When this bit is 0, writing a 1 generates a PCI bus SERR#.	Yes	Yes	0
07-03	NU	Not Used.	Yes	No	0
08	PIE	PCI Interrupt Enable. A value of 1 enables PCI interrupts.	Yes	Yes	1
09	PDIE	PCI Doorbell Interrupt Enable. A value of 1 enables doorbell interrupts. Used in conjunction with PCI interrupt enable. Clearing the doorbell interrupt bits causing the interrupt clears the interrupt.	Yes	Yes	0
10	PAIE	PCI Abort Interrupt Enable. A value of 1 enables a master abort or master detect of a target abort to generate a PCI interrupt. Used in conjunction with PCI interrupt enable. Clearing the abort status bits clears the PCI interrupts.	Yes	Yes	0
11	PLIE	PCI Local Interrupt Enable. A value of 1 enables a local interrupt input to generate a PCI interrupt. Use in conjunction with PCI interrupt enable. Clearing the local bus cause of the interrupt clears the interrupt.	Yes	yes	0

Bit	Name	Function	Read	Write	Value after Reset
12	RAE	Retry Abort Enable. A value of 1 enables the BCI-2004 to treat 256 Master consecutive retries to a Target as a Target Abort. A value of 0 enables the BCI-2004 to attempt Master Retries indefinitely.	Yes	Yes	0
13	PDI	PCI Doorbell Interrupt. A value of 1 indicates that the PCI doorbell interrupt is active.	Yes	No	0
14	PAI	PCI Abort Interrupt. A value of 1 indicates that the PCI abort interrupt is active.	Yes	No	0
15	LI	Local Interrupt. A value of 1 indicates that the local interrupt is active.	Yes	No	0
16	LIE	Local Interrupt Enable. A value of 1 enables Local interrupts.	Yes	Yes	1
17	LDIE	Local Doorbell Interrupt Enable. A value of 1 enables doorbell interrupts. Used in conjunction with Local interrupt enable. Clearing the Local doorbell interrupt bits clears the interrupt.	Yes	Yes	0
18	L0IE	Local DMA Channel 0 Interrupt Enable. A value of 1 enables DMA channel 0 interrupts. Used in conjunction with Local interrupt enable. Clearing the DMA status bits clears the interrupt.	Yes	Yes	0
19	L1IE	Local DMA Channel 1 Interrupt Enable. A value of 1 enables DMA channel 1 interrupts. Used in conjunction with Local interrupt enable. Clearing the DMA status bits clears the interrupt.	Yes	Yes	0
20	LDI	Local Doorbell Interrupt. A value of 1 indicates that the Local doorbell interrupt is active.	Yes	No	0
21	L0I	DMA Channel 0 Interrupt. A value of 1 indicates that the DMA channel 0 interrupt is active.	Yes	No	0
22	L1I	DMA Channel 1 Interrupt. A value of 1 indicates that the DMA channel 1 interrupt is active.	Yes	No	0
23	BI	A value of 1 indicates that the BIST interrupt is active. The BIST (built in self-test) interrupt is generated by writing a 1 to bit 6 of the PCI Configuration BIST register. Clearing bit 6 clears the interrupt. Refer to the BIST register for a description of self test.	Yes	No	0
24	DMTA	A value of 0 indicates that a Direct Master was the bus master during a Master or Target Abort.	Yes	No	0

Bit	Name	Function	Read	Write	Value after Reset
26-25	NU	Not Used.	Yes	No	0
27	TA	A value of 0 indicates that a Target Abort was generated by the BCI-2004 after 256 consecutive Master retries to a Target.	Yes	Yes	0
31-28	NU	Not Used.	Yes	No	0

EEPROM PCI I/O Control Register (EPIR)

Local Offset ECh
PCI Offset 6Ch

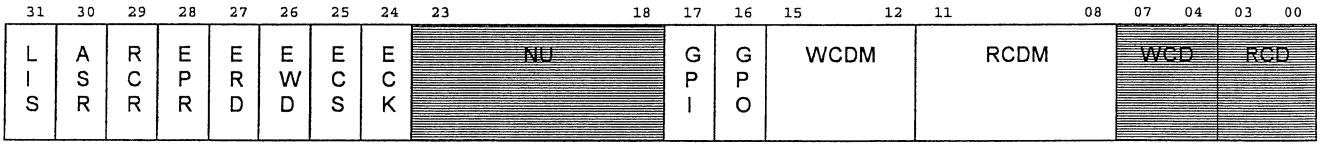


Figure 4-37: EEPROM PCI I/O Control Register

Bit	Name	Function	Read	Write	Value after Reset
03-00	RCD	PCI Read Command Code for DMA.	Yes	Yes	1110
07-04	WCD	PCI Write Command Code for DMA.	Yes	Yes	0111
11-08	RCDM	PCI Memory Read Command Code for Direct Master.	Yes	Yes	0110
15-12	WCDM	PCI Memory Write Command Code for Direct Master.	Yes	Yes	0111
16	GPO	General Purpose Output. A value of 1 causes the USER0 output to go high. A value of 0 causes the output to go low.	Yes	Yes	1h
17	GPI	General Purpose Input. A value of 1 indicates that USER1 input pin is high. A value of 0 indicates that USER1 pin is low.	Yes	No	-
23-18	NU	Not Used.	Yes	No	0
24	ECK	EEPROM Clock for Local or PCI Bus Reads or Writes to EEPROM. Toggling this bit generates an EEPROM clock. Refer to the manufacturer's data sheet for the particular EEPROM being used.	Yes	Yes	0
25	ECS	EEPROM Chip Select. For Local or PCI bus reads or writes to EEPROM, setting this bit to a 1 provides the EEPROM chip select.	Yes	Yes	0
26	EWD	Write Bit to EEPROM. For writes this output bit is the input to the EEPROM. It is clocked into the EEPROM by the EEPROM clock.	Yes	Yes	0

Bit	Name	Function	Read	Write	Value after Reset
27	ERD	Read EEPROM Data Bit. For reads, this input bit is the output of the EEPROM. It is clocked out of the EEPROM by the EEPROM clock.	Yes	No	--
28	EPR	EEPROM Present. A 1 in this bit indicates that an EEPROM is present.	Yes	No	0
29	RCR	Reload Configuration Registers. When this bit is 0, writing a 1 causes the BCI-2004 to reload the PCI configuration registers from EEPROM.	Yes	Yes	0
30	ASR	PCI Adapter Software Reset. A value of 1 written to this bit holds the local bus logic in the BCI-2004 reset and LRESETO# asserted. The contents of the PCI configuration registers and Shared Runtime Registers are not reset. Software Reset can only be cleared from the PCI bus.	Yes	Yes	0
31	LIS	Local Init Status. A 1 indicates that the local Init is done. Responses to PCI accesses are RETRYs until this bit is set. While input NB# is asserted low this bit is forced to 1.	Yes	Yes	0

Alpha Host Access to BCI-2004

Access to the BCI-2004 registers and Unibus devices are made via system-independent routines or by system-dependent I/O mapped direct access. If direct access to the BCI-2004 is desired on an Alpha platform, the addresses must be adjusted (swizzled) for use with the PCI bus. The adjustment consists of left shifting the address by five bits and setting the byte size of the access. This shifting of the address results in the 128K bytes of BCI-2004 address space requiring 2 Mbytes of PCI address space be mapped to the driver.

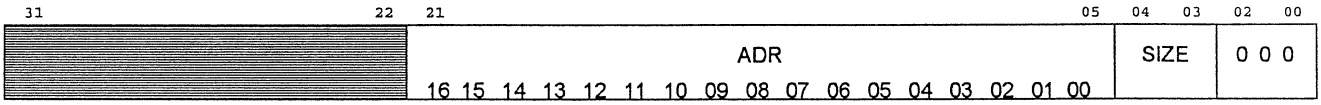


Figure 4-38: Alpha PCI Address Format

Bit	Name	Function
02-00		Always zero.
04-03	SIZE	04 03 Size Regs Unibus 0 0 8-bit X 0 1 16-bit X 1 0 24-bit 1 1 32-bit X
21-05	ADR	PCI Address.
31-22	N/A	Supplied by the operating system mapping.

Intel Host Access to BCI-2004

Access to the BCI-2004 registers and Unibus devices are made by operating system I/O read and write routines or by direct access memory mapped I/O.

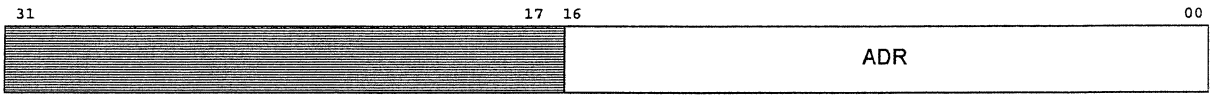


Figure 4-39: Intel PCI Address Format

Bit	Name	Function
16-00	ADR	PCI Address.
31-17	N/A	Supplied by the operating system mapping.

DMA Direct to PCI Address Format

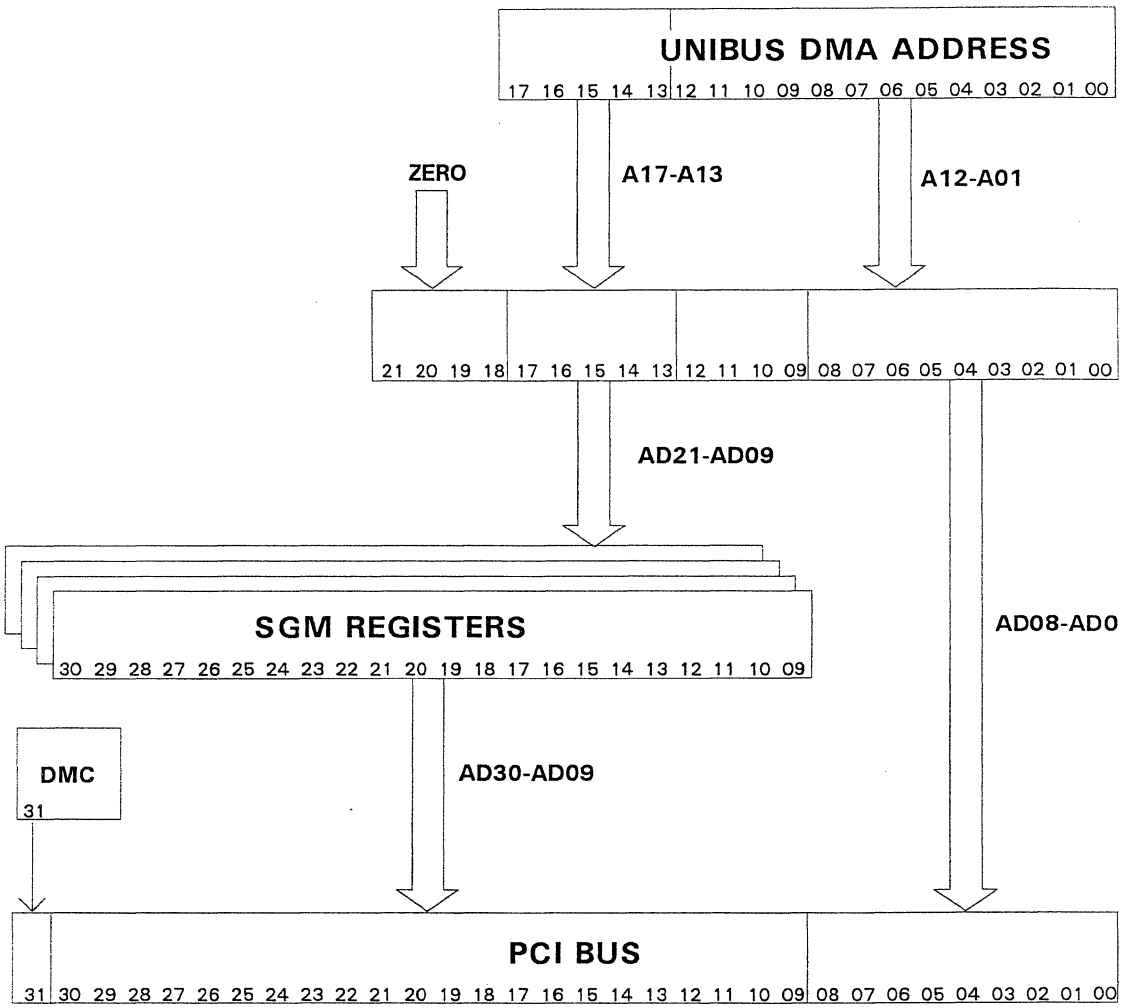


Figure 4-40: DMA Direct to PCI Address Format with UMRs Disabled

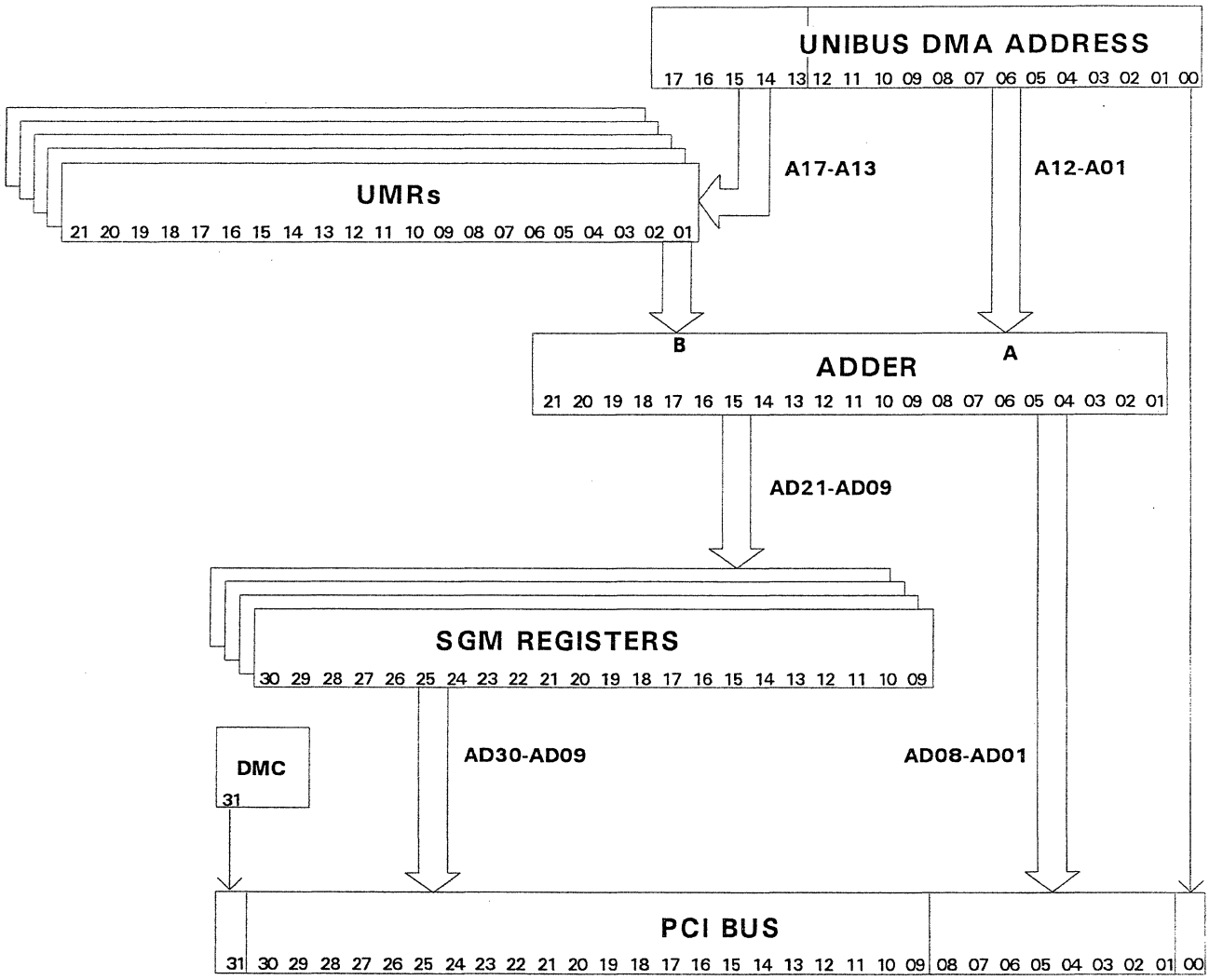


Figure 4-41: DMA Direct to PCI Address Format with UMRs Enabled

Local Register Addressing

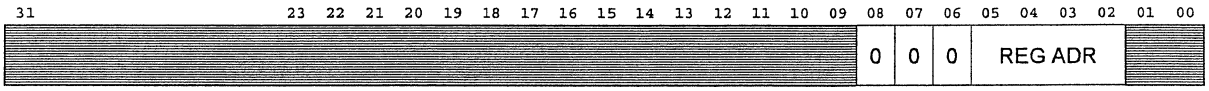


Figure 4-42: Local Register Addressing

Bit	Name	Function
01-00	NU	Not Used.
05-02	REG ADR	Register Address. These bits select 1 of 10 internal registers.
08-06	Always 0	
31-09	NU	Not Used

RAD 05	04	03	02	Register	Use
0	0	0	0	Control and status	Control and status
0	0	0	1	PCI Address Register	PCIADD
0	0	1	0	Unibus data	PIO read data and status
0	0	1	1	Unibus vector	Unibus interrupts
0	1	0	0	Unibus priority	Interrupt priority control
0	1	0	1	Unibus maintenance	Maintenance
0	1	1	0	Unibus address	Maintenance
0	1	1	1	Scatter/Gather Control & Status Register	SGCSR
1	0	0	0	Map Control Register	Map enable
1	0	0	1	Test Point Register	Maintenance

All internal registers are word addressable only.

Byte write operation to internal registers is not supported.

Table 4-1: Register Addresses

Unibus Registers

Local Addr	31 24 23 16 15 08 07 00	PCI Addr
00h	Control/Status Register (CSR)	00h
04h	PCI Address Register (PCIADD)	04h
08h	Bus Data Register (BDR)	08h
0Ch	Bus Vector Register (BVR)*	0Ch
10h	Bus Priority Register (BPR)	10h
14h	Unibus Maintenance Register (UMR)*	14h
18h	Unibus Address Register (UAR)	18h
1Ch	Scatter/Gather Control & Status Register (SGCSR)	1Ch
20h	Map Control/Status Register (MCSR)	20h
24h	Test Point Register (TPR)	24h

*This register is read only in normal mode.

Figure 4-43: Unibus Registers

Control and Status Register (CSR) — Space 0 Offset 00h

The Control and Status Register enables Unibus DMA and interrupt transfers, controls the PIO mode of operation, provides status of error conditions, and enables PCI interrupts. A host can read and write the CSR using 32-bit word transfers. Byte write operation to the CSR is not supported.

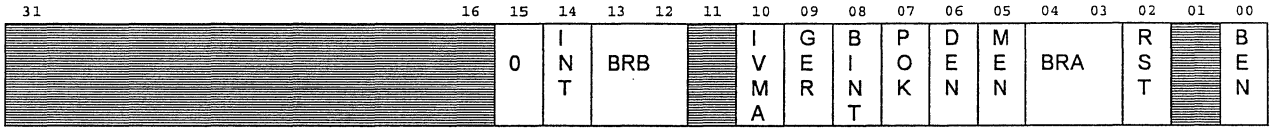


Figure 4-44: Control and Status Register

Bit	Name	Function	Read	Write	Value after Reset
00	BEN	Bus Enable. Read/write bit. Cleared by PCI RESET. Set when writing to CSR and bit ad00 is set. When set, enables Unibus address, data, and control signals onto and from the Unibus. When cleared, Unibus signals can be read but cannot control any operations. This bit must be set to perform any PCI PIO operations to the Unibus and DMA or interrupt operations.	Yes	Yes	0
01	NU	Not Used.			0
02	RST	Unibus INIT. Read/write bit. Cleared by PCI RESET. Set when writing to CSR and bit ad02 is set. When set, asserts signal INIT onto the Unibus, if UEN is set. When reading CSR, bit ad02 is set if signal INIT is asserted on the Unibus.	Yes	Yes	0
04-03	BRA	Bus Request A. These two bits select one of four Unibus interrupt request as a source for request A: 00 - BR4 01 - BR5 10 - BR6 11 - Not used	Yes	Yes	0

Bit	Name	Function	Read	Write	Value after Reset
05	MEN	Maintenance Enable. Read/write bit. Cleared by PCI RESET. Set when writing to CSR and bit ad05 is set. When set, enables software control of Unibus signals C0, C1, BG4, BG5, BG6, BG7, NPG, BR4, BR5, BR6, BR7, and NPR for operation verification purposes. Used in conjunction with UEN.	Yes	Yes	0
06	DEN	Unibus DMA Enable. Read/write bit. Cleared by PCI RESET. Set when writing to CSR and bit ad09 is set. When set, Unibus DMA operations are enabled. When cleared, Unibus DMA requests are not serviced.	Yes	Yes	0
07	POK	Power OK. Read only bit. When this bit is set, it reflects that Unibus signals ACLO and DCLO are not asserted indicating that all devices on the Unibus have power applied. When this bit is clear, it indicates that AC or DC power is not applied to all Unibus devices.	Yes	No	1
08	BINT	Bus Interrupt. This bit is set by a GRANT cycle when a Unibus device has requested an interrupt and bit 0 of the BPR is set, which also causes INT (bit 14) to set. This bit is cleared by writing a new value into the BPR register.	Yes	No	0
09	GER	Grant Error. Read/write bit. Cleared by PCI RESET. Set when Unibus signal SACK is not received within 10 microseconds of asserting NPG during the grant sequence of an NPR request and causes INT (bit 14) to set. Cleared by writing one to this bit in the CSR.	Yes	1	0
10	IVMA	Invalid Map Access. This bit is set when a Unibus DMA cycle attempts to access an invalid scatter/gather map register. If the IVEN bit in the SGCSR register is set, this bit causes the INT bit to set. Cleared by writing a one to this bit.	Yes	1	0
11	NU	Not used.	Yes	No	0
13-12	BRB	Bus Request B. These two bits select one of four Unibus interrupt request as a source for Request B: 00 - BR5 01 - BR6 10 - BR7 11 - Not used	Yes	Yes	Unknown

Bit	Name	Function	Read	Write	Value after Reset
14	INT	Interrupt. Read only. When set by IVMA, GER, or BINT, this bit indicates that the INT signal to the PLX is set and an interrupt request is present on the PCI bus. This bit can be cleared by removal of the IVMA, GER, or BINT bits.	Yes	No	
15	0	Read only. Read as zero.	Yes	No	
31-16	NU	Not Used.			

PCI Address Register (PCIADD) — Space 0 Offset 04h

The PCI Address Register is used for maintenance purposes to verify DMA address mapping. The contents of this register following a DMA cycle contains the mapped address as it would appear on the PCI bus.

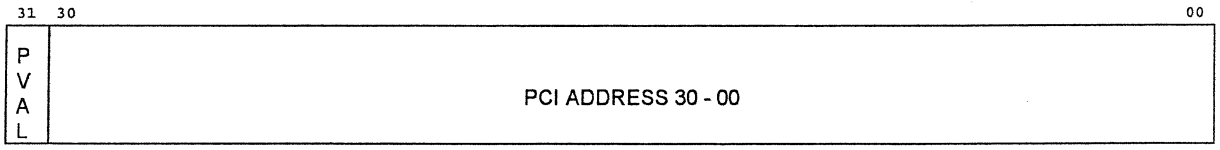


Figure 4-45: PCI DMA Address Register

Bit	Name	Function	Read	Write	Value after Reset
31	PVAL	Page Valid. This bit is set to 1 if the address is valid. If an attempt is made to reference an invalid scatter/gather map, the register contains the accessed map address, which is a value in the range of 10000h to 1FFF8h and IVMA is set in the CSR register.	Yes	No	0
30-0	PCIADD	PCI Address. Contains the PCI address bits 30-00 for the last Unibus DMA cycle.	Yes	No	0

Bus Data Register (BDR) Space 0 Offset 08h

The BDR is made accessible by software for maintenance purposes to verify the data storage ability of BDR. When not performing a maintenance function and in loosely coupled mode, BDR stores data from the host that is written to the Unibus during a PIO write operation or stores data from the Unibus that is read by the host during a PIO read operation.

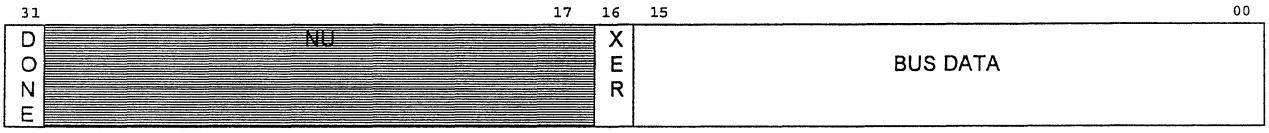


Figure 4-46: Bus Data Register

Bit	Name	Function	Read	Write	Value after Reset
15-00	D15-D00	Bus Data. Read/write. This register can be written into and read from in maintenance mode. When not in maintenance mode, Unibus data is stored in this register during PIO reads. 16-bit Unibus data is aligned with the host's lower 16-bit word. Unibus data bits 07-00 form the even byte and bits 08-15 form the odd Unibus byte. The value contained in the register is undefined after power is applied and before a Unibus read occurs. Data should be written to this register before starting Unibus write access.	Yes	Yes	0
16	XER	Transfer Error. Read-only for normal operations. Cleared by PCI RESET. Set when Unibus SSYN is not received within 10 microseconds of asserting Unibus signal MSYN during a PCI PIO Unibus access. Cleared after starting new Unibus cycle. Read/write in maintenance mode.	Yes	Maint	
30-17	NU	Not used.			
31	DONE	Done. This bit is set when a Unibus read or write cycle is completed. When set during a read, it indicates data is valid in bit 15-00. When set during a write, it indicates the Unibus write cycle is completed.	Yes	No	

Bus Vector Register (BVR) Space 0 Offset 0Ch

The Bus Vector Register is used to store a Unibus interrupt vector for reading by the host. The register can be written into by the host only when in maintenance mode to verify register operation.

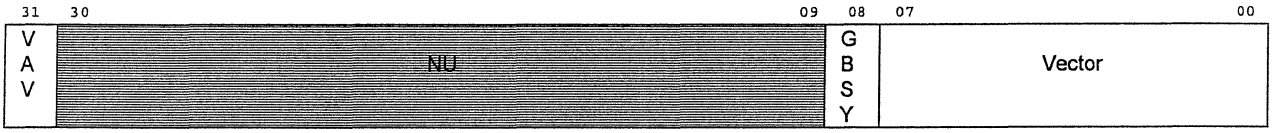


Figure 4-47: Bus Vector Register

Bit	Name	Function	Read	Write	Value after Reset
07-00	D09-D02	Vector Data. Read-only for normal operation. Reset by PCI RESET. The vector register contains the last Unibus interrupt vector and is read by the host following an interrupt to determine the service requested by a Unibus device. In maintenance mode, this is a read/write register. Data bits 09-02 are stored into PCI bits 07-00 respectively, when writing into the UVR. The contents are read into data bits 07-00, respectively, when reading the UVR.	Yes	No	0
08	GBSY	Grant Busy. Read only. When set, indicates a Unibus interrupt Grant cycle is in progress. Loop on this bit until clear and then proceed to check VAV bit. If VAV bit not set, it indicates a passive release occurred.	Yes	No	
30-09	NU	Not Used.			
31	VAV	Vector Valid. Read only. When set, data in bits 07-00 are valid.	Yes	No	

Bus Priority Register (BPR) — Space 0 Offset 10h

The Priority Register is used by the host to control the four Unibus interrupts. The register can be set to pass all four interrupts, no interrupts, or only those interrupts with a higher priority level than the value contained in the Priority Register. The Priority Register supports word operation only, byte operation is not supported.

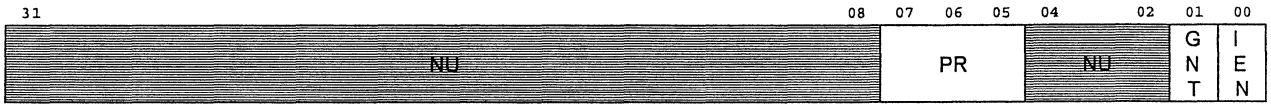


Figure 4-48: Bus Priority Register

Bit	Name	Function	Read	Write	Value after Reset
00	IEN	Interrupt Enable. Read/write bit. When set, enables an interrupt to be passed to the PLX if an interrupt is present on the Unibus and the interrupt level is greater than the value in bits 07-05 of the Priority register.	Yes	Yes	0
01	GNT	Grant. Write only. When set, causes a Unibus grant cycle to be performed if an interrupt is present on the Unibus and the interrupt level is greater than the value in bits 07-05 of the Priority register.	No	Yes	0
07-05	PR1,2,3	Priority. Read/write bit. Set by PCI RESET. Used to control Unibus interrupts priority. PR1 PR2 PR3 Priority Level Passed 0 X X Pass BR4, BR5, BR6,BR7 1 0 0 Pass BR5, BR6, and BR7 1 0 1 Pass BR6 and BR7 1 1 0 Pass BR7 1 1 1 Block all Unibus interrupts	Yes	Yes	0
31-08	NU	Not used.			0

Unibus Maintenance Register (UMR) Space 0 Offset 14h

The Unibus Maintenance Register is made accessible by software for maintenance purposes only. This register is used to verify Unibus control signals. The register can be written into when in maintenance mode.

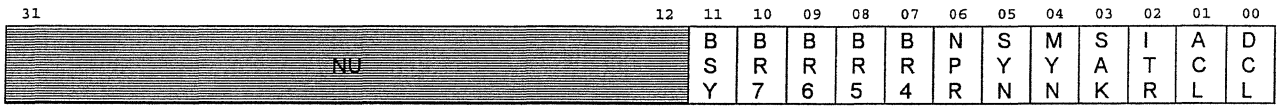


Figure 4-49: Unibus Maintenance Register

Bit	Name	Function	Read	Write	Value after Reset
00	DCL	Unibus DC Low (DCLO). Read/write. Cleared by PCI RESET. Set when writing to UMR and bit 00 is set in maintenance mode. When this bit is set, signal DCLO is asserted onto the Unibus. When reading UMR, bit 00 reflects the state of the DCLO signal on the Unibus.	Yes	Yes	0
01	ACL	Unibus AC Low. (ACLO). Read/write. Cleared by PCI RESET. Set when writing to UMR and bit 01 is set in maintenance mode. When this bit is set, Unibus signal ACLO is asserted on the Unibus. When reading UMR, bit 01 reflects the state of the ACLO signal on the Unibus.	Yes	Yes	0
02	ITR	Unibus INTR. Read/write bit. Cleared by PCI RESET. Set when writing to UMR and bit 02 is set in maintenance mode. When this bit is set, signal INTR is asserted onto the Unibus. When reading UMR, bit 02 reflects the state of the INTR signal on the Unibus.	Yes	Yes	0
03	SAK	Unibus SACK. Read/write bit. Cleared by PCI RESET. Set when writing to UMR and bit 03 is set in maintenance mode. When this bit is set, signal SACK is asserted onto the Unibus. When reading UMR, bit 03 reflects the state of the SACK signal on the Unibus.	Yes	Yes	0
04	MYN	Unibus Master Sync (MSYN). Read only bit. When reading UMR, bit 04 reflects the state of the MSYN signal on the Unibus.	Yes	No	

Bit	Name	Function	Read	Write	Value after Reset
05	SYN	Unibus Slave Sync (SSYN)). Read only bit. When reading UMR, bit 05 reflects the state of the SSYN signal on the Unibus.	Yes	No	
06	NPR	Non-processor Request (NPR). Read/write bit. Cleared by PCI RESET. Set when writing to UMR and bit 06 is set in maintenance mode. When this bit is set, signal NPR is asserted onto the Unibus. When reading UMR, bit 06 reflects the state of the NPR signal on the Unibus.	Yes	Yes	0
07	BR4	Bus Request 4 (BR4). Read/write. Cleared by PCI RESET. Set when writing to UMR and bit 07 is set in maintenance mode. When this bit is set, signal BR4 is asserted on the Unibus. When reading UMR, bit 07 reflects the state of the BR4 signal on the Unibus.	Yes	Yes	0
08	BR5	Bus Request 5 (BR5). Read/write. Cleared by PCI RESET. Set when writing to UMR and bit 08 is set in maintenance mode. When this bit is set, signal BR5 is asserted on the Unibus. When reading UMR, bit 08 reflects the state of the BR5 signal on the Unibus.	Yes	Yes	0
09	BR6	Bus Request 6 (BR6). Read/write. Cleared by PCI RESET. Set when writing to UMR and bit 09 is set in maintenance mode. When this bit is set, signal BR6 is asserted on the Unibus. When reading UMR, bit 09 reflects the state of the BR6 signal on the Unibus.	Yes	Yes	0
10	BR7	Bus Request 7 (BR7). Read/write. Cleared by PCI RESET. Set when writing to UMR and bit 10 is set in maintenance mode. When this bit is set, signal BR7 is asserted on the Unibus. When reading UMR, bit 10 reflects the state of the BR7 signal on the Unibus.	Yes	Yes	0
11	BSY	Unibus Busy. Read only bit. Cleared by PCI RESET. When reading UMR, bit 11 reflects the state of the BBSY signal on the Unibus. In maintenance mode, setting Unibus signal SACK clears BBSY. BBSY sets after SACK is removed when Unibus grants and SSYN are clear.	Yes	No	
31-12	NU	Not Used.			

Unibus Address Register (UAR) Space 0 Offset 18h

The Unibus Address Register is accessible by software for maintenance purposes to verify the data storage ability of UAR. In normal operations, UAR is used to start an access.

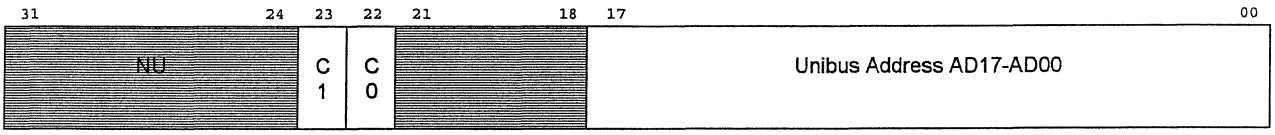


Figure 4-50: Unibus Address Register

Bit	Name	Function	Read	Write	Value after Reset
17-00	AD17-AD00	Unibus address. Read/write. These bits store Unibus address bits AD00 through AD17 when writing to the UAR.	Yes	Yes	
21-18	NU	Not Used.			
22	C0	Unibus C0. Read/write. The bit is set when bit 22 is set and writing to Unibus address register. It is cleared when writing to UAR and bit 22 is cleared. Specifies access type in conjunction with C1 as shown below. C1 C0 Operation 0 0 Read 0 1 Data-input-pause 1 0 Write word 1 1 Write byte	Yes	Yes	0
23	C1	Unibus C1. Read/write. The bit is set when bit 23 is set and writing to the Unibus address register. It is cleared when writing to UAR and bit 23 is cleared. Specifies access type in conjunction with C0. See bit 22.	Yes	Yes	0
31-24	NU	Not Used.			

Scatter/Gather Control & Status Register (SGCSR) Space 0 Offset 1Ch

The Scatter/Gather Control & Status Register consists of two bits which are used to control Scatter/Gather operations and interrupts.

Figure 4-51: Scatter/Gather Control & Status Register

Bit	Name	Function	Read	Write	Value after Reset
00	DIAG	Diagnostic. The effective PCI DMA address is placed into the PCIADD register with the PVAL bit forced to zero, the PCI DMA cycle is not started, and the Unibus DMA cycle is not completed, causing a Unibus timeout. The IVMA bit in the CSR is set if the accessed map is invalid. The function is for diagnostic use.	Yes	Yes	0
03-01	NU	Not Used			
04	IVEN	Interrupt Enable. When set, enables an interrupt to occur whenever an invalid scatter/gather map is accessed during a Unibus DMA operation.	Yes	Yes	0
31-05	NU	Not Used.			

MAP Control and Status Register (MCSR) Space 0 Offset 20h

The Map Control and Status Register

Figure 4-52: Map Control and Status Register

Bit	Name	Function	Read	Write	Value after Reset
04-00	NU	Not Used.			
05	MAP	Enables the relocation of 18-bit DMA addresses to 22-bit emulated memory addresses.	Yes	Yes	
31-06	NU	Not Used.			

Test Point Register (TPR) — Space 0 Offset 24h

This register is used with factory engineering test equipment and diagnostics. The use of this register is undefined and is intended to be altered to fit given engineering maintenance requirements. Diagnostics access this register when an error is detected to provide a scope sync.

Figure 4-53: Test Point Register

Bit	Name	Function	Read	Write	Value after Reset
31-00	NU	Not Used. Read/write	Yes	Yes	

Unibus Map Register, Lower (UMRLx) Space 0 Offset 100h to 1F8h

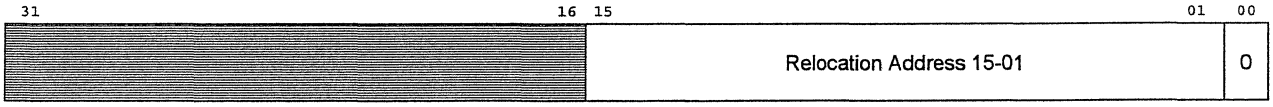


Figure 4-54: Unibus Map Register, Lower

Bit	Name	Function	Read	Write	Value after Reset
15-01		Relocation Address 15-01.	Yes	Yes	0
00	0	Always 0			0

Unibus Map Register, Upper (UMRUx) Space 0 Offset 104h to 1FCh

Figure 4-55: Unibus Map Register, Upper

Bit	Name	Function	Read	Write	Value after Reset
15-06	NU	Not Used.	Yes	Yes	0
05-00		Relocation Address 21-16.			0

Scatter/Gather Map Registers, Lower (SGMLx)

Space 0 Offset 10000h to 1FFF8h

There are 8192 Scatter/Gather Map Registers. If the UMRs are enabled, the 18-bit DMA address from the Unibus is widened to 22 bits before going to the scatter/gather stage. The upper 13 bits of the 22-bit DMA address are used to select a map register. The lower 22 bits of the selected map register provide the upper 22 bits of the PCI address. The lower 9 bits are passed on through from the Unibus. The low 9 bits from the UMR adder are used for the low 9 bits of the PCI address. Address bit 31 for the PCI bus is supplied by bit 31 of the DMC local configuration register. Since bit 31 is a static value, the DMA memory buffers must completely reside within a 2 GB space of memory.

The scatter/gather map registers allow Unibus DMA devices to view physical system memory as one contiguous area independent of the memory page size or page location.

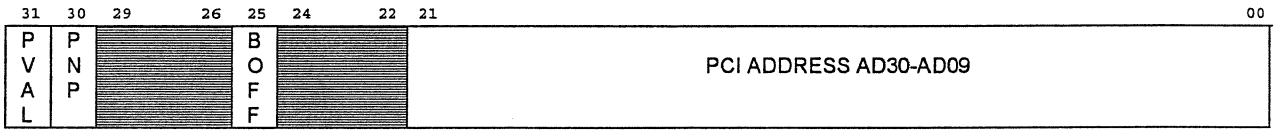


Figure 4-56: Scatter/Gather Map Register, Lower

Bit	Name	Function	Read	Write	Value after Reset
21-0	AD30-AD09	Address Bits AD30-AD09. Supplies the upper address bits to the PCI.	Yes	Yes	Unknown
24-22	NU	Not Used.	Yes	Yes	
25	BOFF	Byte Offset. Causes DMA addresses to be incremented by one. If a DMA crosses a page boundary, the next consecutive SGMR must also have this bit set. (If it doesn't, the results are unpredictable.) This bit must not be set when the Unibus UMRs are enabled.	Yes	Yes	Unknown
29-26	NU	Not Used.			
30	PNP	Page Not Present. When set, the adapter does not respond to DMA accesses to this page. This bit overrides bit 31. This emulates the function of the Map Register Disable bits in the UACR of the VAX780.	Yes	Yes	Unknown

Bit	Name	Function	Read	Write	Value after Reset
31	PVAL	Page Valid. When set, this be translates a Unibus physical address into PCI Physical address. For the Unibus, this is the address translated by the UMRs if they are enabled. When cleared, DMA access to this page is timed out, and IVMR is set in the CSR.	Yes	Yes	Unknown

Scatter/Gather Map Register, Upper (SGMUx)

Space 0 Offset 10004h to 1FFFCh

The Upper Scatter/Gather Map Register is reserved for future expansion.

Figure 4-57: Scatter/Gather Map Register, Upper

Bit	Name	Function	Read	Write	Value after Reset
31-00	NU	Not Used.			

System Address Allocation Charts

Offsets from Address Space 0 Base:

0	CSR
4	PCIADD
8	BDR
C	BVR
10	BPR
14	UMR
18	UAR
1C	SGCSR
20	MCSR
24	TPR
100-1FC	Unibus Map Registers
200-0FFFF	Not used
10000-1FFFC	Scatter/gather Map Registers

5 Troubleshooting

Logical provides a diagnostic to test the basic functionality of the BCI-2004 module. The diagnostic is available for use with numerous operating systems. Contact the factory for a version applicable to your platform.

Appendix A
PCI Local Bus Interface Connector Pin Assignments

This appendix lists the pin assignments for the PCI bus interface.

Pin	Signal	Pin	Signal
A1	TRST-L	B1	-12V
A2	+12V	B2	TCK-H
A3	TMS-H	B3	GND
A4	TDI-H	B4	TDO-H
A5	+5V	B5	+5V
A6	INTA-L	B6	+5V
A7	INTC-L	B7	INTB-L
A8	+5V	B8	INTD-L
A9		B9	PRSNT1-L
A10	+5V	B10	
A11		B11	PRSNT2-L
A12	GND	B12	GND
A13	GND	B13	GND
A14		B14	
A15	RST-L	B15	GND
A16	+5V	B16	CLK-H
A17	GNT-L	B17	GND
A18	GND	B18	REQ-L
A19		B19	+5V
A20	AD30-H	B20	AD31-H
A21	+3.3V	B21	AD29-H
A22	AD28-H	B22	GND
A23	AD26-H	B23	AD27-H
A24	GND	B24	AD25-H
A25	AD24-H	B25	+3.3V
A26	IDSEL-H	B26	C/BE3-L
A27	+3.3V	B27	AD23-H
A28	AD22-H	B28	GND
A29	AD20-H	B29	AD21-H
A30	GND	B30	AD19-H

Pin	Signal	Pin	Signal
A31	AD18-H	B31	+3.3V
A32	AD16-H	B32	AD17-H
A33	+3.3V	B33	C/BE2-L
A34	FRAME-L	B34	GND
A35	GND	B35	IRDY-L
A36	TRDY-L	B36	+3.3V
A37	GND	B37	DEVSEL-L
A38	STOP-L	B38	GND
A39	+3.3V	B39	LOCK-L
A40	SDONE-H	B40	PERR-L
A41	SBO-L	B41	+3.3V
A42	GND	B42	SERR-L
A43	PAR-H	B43	+3.3V
A44	AD15-H	B44	C/BE1-L
A45	+3.3V	B45	AD14-H
A46	AD13-H	B46	GND
A47	AD11-H	B47	AD12-H
A48	GND	B48	AD10-H
A49	AD09-H	B49	GND
A50	KEYWAY	B50	KEYWAY
A51	KEYWAY	B51	KEYWAY
A52	C/BE0-L	B52	AD08-H
A53	+3.3V	B53	AD07-H
A54	AD06-H	B54	+3.3V
A55	AD04-H	B55	AD05-H
A56	GND	B56	AD03-H
A57	AD02-H	B57	GND
A58	AD00-H	B58	AD01-H
A59	+5V	B59	+5V
A60	REQ64-L	B60	ACK64-L
A61	+5V	B61	+5V
A62	+5V	B62	+5V

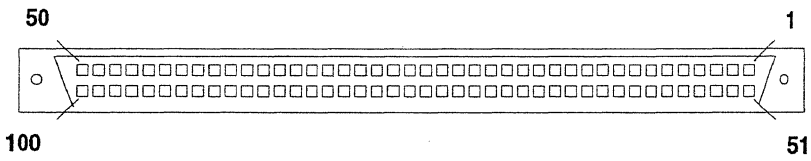
Appendix B
Unibus Connector
Pin Assignments

This appendix lists the pin assignments for the Unibus A and B connectors.

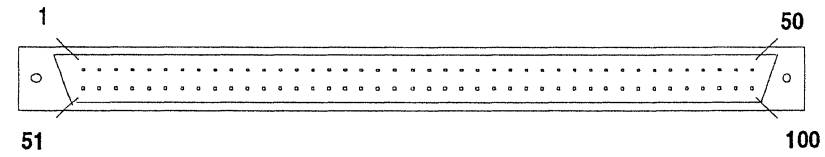
Unibus A		Unibus B	
Pin	**Signal**	**Pin**	**Signal**
AA1	INIT-L	BA1	BG6-H
AA2		BA2	
AB1	INTR-L	BB1	BG5-H
AB2	GND	BB2	GND
AC1	D00-L	BC1	BR5-L
AC2	GND	BC2	GND
AD1	D02-L	BD1	GND
AD2	D01-L	BD2	BR4-L
AE1	D04-L	BE1	GND
AE2	D03-L	BE2	BG4-H
AF1	D06-L	BF1	ACLO-L
AF2	D05-L	BF2	DCLO-L
AH1	D08-L	BH1	A01-L
AH2	D07-L	BH2	A00-L
AJ1	D10-L	BJ1	A03-L
AJ2	D09-L	BJ2	A02-L
AK1	D12-L	BK1	A05-L
AK2	D11-L	BK2	A04-L
AL1	D14-L	BL1	A07-L
AL2	D13-L	BL2	A06-L
AM1	PA-L	BM1	A09-L
AM2	D15-L	BM2	A08-L
AN1	GND	BN1	A11-L
AN2	PB-L	BN2	A10-L
AP1	GND	BP1	A13-L
AP2	BBSY-L	BP2	A12-L
AR1	GND	BR1	A15-L
AR2	SACK-L	BR2	A14-L
AS1	GND	BS1	A17-L
AS2	NPR-L	BS2	A16-L
AT1	GND	BT1	GND
AT2	BR7-L	BT2	C1-L
AU1	NPG-H	BU1	SSYN-L
AU2	BR6-L	BU2	C0-L
AV1	BG7-H	BV1	MSYN-L
AV2	GND	BV2	GND

Appendix C
Interconnect Cable
Pin Assignments

This appendix lists the pin assignments for the interconnect cable between the BCI-2004 controller and the CAU-2001-A Unibus module or the CPX-2003-A bulkhead panel. The connectors at both ends of the interconnect cable are 100-pin high density SCSI style cable plugs. The connectors on the modules are SCSI style receptacles, AMP part number 749076-9 or Thomas & Betts Ansley part number HFR100RA29BX1. The pin assignments are listed below.



100-pin High Density Receptacle



100-pin High Density Cable Plug

Connector J1

Signal	Pin	Pin	Signal
GND	1	51	GND
C0-L	2	52	MSYN-L
GND	3	53	GND
C1-L	4	54	SSYN-L
GND	5	55	GND
A16-L	6	56	A17-L
GND	7	57	GND
A14-L	8	58	A15-L
GND	9	59	GND
A12-L	10	60	A13-L
GND	11	61	GND
A10-L	12	62	A11-L
GND	13	63	GND
A08-L	14	64	A09-L
GND	15	65	GND
A06-L	16	66	A07-L
GND	17	67	GND
A04-L	18	68	A05-L
GND	19	69	GND
A02-L	20	70	A03-L
GND	21	71	GND
A00-L	22	72	A01-L
GND	23	73	GND
BG0-H	24	74	DCLO-L
GND	25	75	GND
BG1-H	26	76	BR0-L
GND	27	77	GND
NPG-H	28	78	BR1-L
GND	29	79	GND
SACK-L	30	80	NPR-L
GND	31	81	GND
D15-L	32	82	BBSY-L
GND	33	83	GND
D13-L	34	84	D14-L
GND	35	85	GND
D11-L	36	86	D12-L
GND	37	87	GND
D09-L	38	88	D10-L
GND	39	89	GND
D07-L	40	90	D08-L
GND	41	91	GND
D05-L	42	92	D06-L
GND	43	93	GND
D03-L	44	94	D04-L
GND	45	95	GND
D01-L	46	96	D02-L
GND	47	97	GND
INTR-L	48	98	D00-L
GND	49	99	GND
SPARE	50	100	INIT-L

Appendix D
Local DMA Registers

Local Addr*	31 24 23 16 15 08 07 00
100h	DMA Ch 0 Mode (D0MR)
104h	DMA Ch 0 PCI Address (D0PAR)
108h	DMA Ch 0 Local Address (D0LAR)
10Ch	DMA Ch 0 Transfer Byte Count (D0SIZ)
110h	DMA Ch 0 Descriptor Pointer (D0DP)
114h	DMA Ch 1 Mode (D1MR)
118h	DMA Ch 1 PCI Address (D1PAR)
11Ch	DMA Ch 1 Local Address (D1LAR)
120h	DMA Ch 1 Transfer Byte Count (D1SIZ)
124h	DMA Ch 1 Descriptor Pointer (D1DP)
128h	DMA Command / Status Register (DCSR)
12Ch	DMA Arbitration Register 0 (DAR0)
130h	DMA Arbitration Register 1 (DAR1)

* Offset from chip select address.

Shaded areas are not available for customer use.

Figure D-1: Local DMA Registers

DMA Channel 0 Mode Register (D0MR)

Local Offset 100h

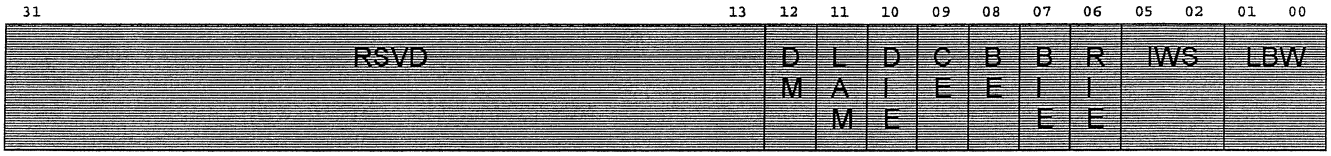


Figure D-2: DMA Channel 0 Mode Register

Bit	Name	Function	Read	Write	Value after Reset
01-00	LBW	Local Bus Width. This field is programmable for the Cx and Jx modes only. 00 8-bit bus width 01 16-bit bus width 10 or 11 32-bit bus width The bus width is forced to 16 bits for the Sx mode.	Yes	Yes	Sx mode 01 Jx mode 11 Cx mode 11
05-02	IWS	Internal Wait States (data to data).	Yes	Yes	0
06	RIE	Ready Input Enable. A 1 value enables Ready input. A value of 0 disables the Ready input.	Yes	Yes	0
07	BIE	Bterm Input Enable. A 1 value enables Bterm input. A value of 0 disables the Bterm input.	Yes	Yes	0
08	BE	Burst Enable. A 1 value enables bursting. A value of 0 disables bursting.	Yes	Yes	0
09	CE	Chaining. A 1 value indicates chaining mode is enabled. A 0 value indicates non-chaining mode is enabled.	Yes	Yes	0
10	DIE	Done Interrupt Enable. A 1 value enables interrupt when done. A 0 value disables interrupt when done.	Yes	Yes	0
11	LAM	Local Addressing Mode. A 1 value indicates local address LA (02-31) to be held constant. A 0 value indicates local address is incremented.	Yes	Yes	0

Bit	Name	Function	Read	Write	Value after Reset
12	DM	Demand mode. A value of 1 causes the DMA controller to operate in demand mode. In demand mode the DMA controller transfers data when its DREQ# input is asserted.. It asserts DACK# to indicate that the current local bus transfer is in response to the DREQ# input. The DMA controller transfers longwords (32 bits) of data. This may result in multiple transfers for an 8 or 16 bit bus.	Yes	Yes	0
31-13	RSVD	Reserved.	Yes	Yes	0

DMA Channel 0 PCI Address Register (D0PAR)

Local Offset 104h

Figure D-3: DMA Channel 0 PCI Address Register

Bit	Name	Function	Read	Write	Value after Reset
31-00	PAR	PCI Address Register. This indicates where in the PCI memory space the DMA transfers (reads or writes) start from.	Yes	Yes	0

DMA Channel 0 Local Address Register (D0LAR)

Local Offset 108h

Figure D-4: DMA Channel 0 Local Address Register

Bit	Name	Function	Read	Write	Value after Reset
31-00	LAR	Local Address Register. This indicates where in the local memory space the DMA transfers (reads or writes) start from.	Yes	Yes	0

DMA Channel 0 Transfer Size (Bytes) Register (D0SIZ)

Local Offset 10Ch

Figure D-5: DMA Channel 0 Transfer Size Register

Bit	Name	Function	Read	Write	Value after Reset
22-00	DSIZ	DMA Transfer Size (Bytes) . Indicates the number of bytes to be transferred during a DMA operation.	Yes	Yes	0
31-23	NU	Not Used.	Yes	Yes	0

DMA Channel 0 Descriptor Pointer Register (D0DP)

Local Offset 110h

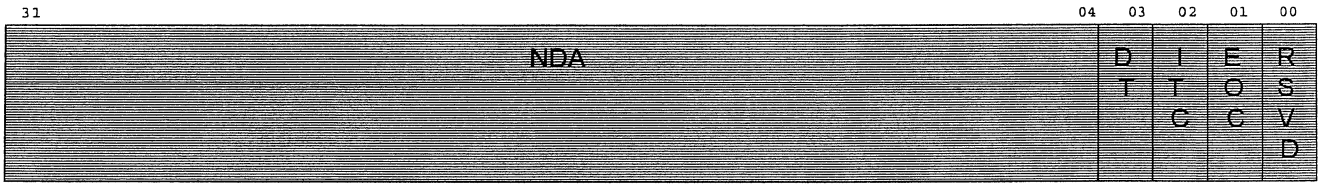


Figure D-6: DMA Channel 0 Descriptor Pointer Register

Bit	Name	Function	Read	Write	Value after Reset
00	RSVD	Reserved.	Yes	Yes	0
01	EOC	End of Chain. A 1 value indicates end of chain. A 0 value indicates not end of chain descriptor.	Yes	Yes	0
02	ITC	Interrupt after Terminal Count. A 1 value causes an interrupt to be generated after the terminal count for this descriptor is reached. A 0 value disables interrupts from being generated.	Yes	Yes	0
03	DT	Direction of Transfer. A 1 value indicates transfers from Local bus to PCI bus. A 0 value indicates transfers from PCI bus to Local bus.	Yes	Yes	0
31-04	NDA	Next Descriptor Address. Quad word aligned.	Yes	Yes	0

DMA Channel 1 Mode Register (D1MR)

Local Offset 114h

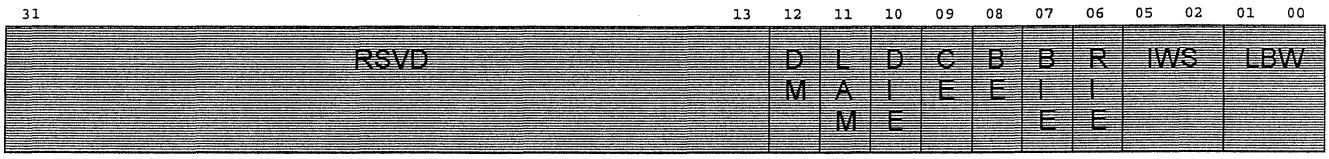


Figure D-7: DMA Channel 1 Mode Register

Bit	Name	Function	Read	Write	Value after Reset
01-00	LBW	Local Bus Width. This field is programmable for the Cx and Jx modes only. 00 8-bit bus width 01 16-bit bus width 10 or 11 32-bit bus width The bus width is forced to 16 bits for the Sx mode.	Yes	Yes	Sx mode 01 Jx mode 11 Cx mode 11
05-02	IWS	Internal Wait States (data to data).	Yes	Yes	0
06	RIE	Ready Input Enable. A 1 value enables Ready input. A value of 0 disables the Ready input.	Yes	Yes	0
07	BIE	Bterm Input Enable. A 1 value enables Bterm input. A value of 0 disables the Bterm input.	Yes	Yes	0
08	BE	Burst Enable. A 1 value enables bursting. A value of 0 disables bursting.	Yes	Yes	0
09	CE	Chaining. A 1 value indicates chaining mode is enabled. A 0 value indicates non-chaining mode is enabled.	Yes	Yes	0
10	DIE	Done Interrupt Enable. A 1 value enables interrupt when done. A 0 value disables interrupt when done.	Yes	Yes	0
11	LAM	Local Addressing Mode. A 1 value indicates local address LA (02-31) to be held constant. A 0 value indicates local address is incremented.	Yes	Yes	0

Bit	Name	Function	Read	Write	Value after Reset
12	DM	Demand mode. A value of 1 causes the DMA controller to operate in demand mode. In demand mode the DMA controller transfers data when its DREQ# input is asserted.. It asserts DACK# to indicate that the current local bus transfer is in response to the DREQ# input. The DMA controller transfers longwords (32 bits) of data. This may result in multiple transfers for an 8 or 16 bit bus.	Yes	Yes	0
31-13	RSVD	Reserved.	Yes	Yes	0

DMA Channel 1 PCI Address Register (D1PAR)

Local Offset 118h

Figure D-8: DMA Channel 1 PCI Address Register

Bit	Name	Function	Read	Write	Value after Reset
31-00	PAR	PCI Address Register. This indicates where in the PCI memory space the DMA transfers (reads or writes) start from.	Yes	Yes	0

DMA Channel 1 Local Address Register (D1LAR)

Local Offset 11Ch

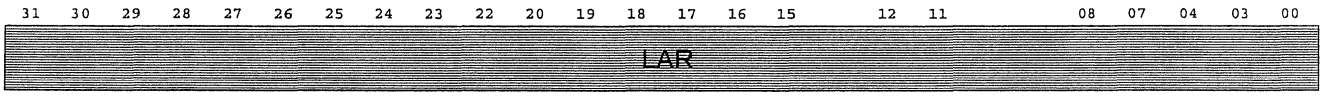


Figure D-9: DMA Channel 1 Local Address Register

Bit	Name	Function	Read	Write	Value after Reset
31-00	LAR	Local Address Register. This indicates where in the local memory space the DMA transfers (reads or writes) start from.	Yes	Yes	0

DMA Channel 1 Transfer Size (Bytes) Register (D1SIZ)

Local Offset 120h

Figure D-10: DMA Channel 1 Transfer Size Register

Bit	Name	Function	Read	Write	Value after Reset
22-00	DSIZ	DMA Transfer Size (Bytes) . Indicates the number of bytes to be transferred during a DMA operation.	Yes	Yes	0
31-23	NU	Not Used.	Yes	Yes	0

DMA Channel 1 Descriptor Pointer Register (D1DP)

Local Offset 124h

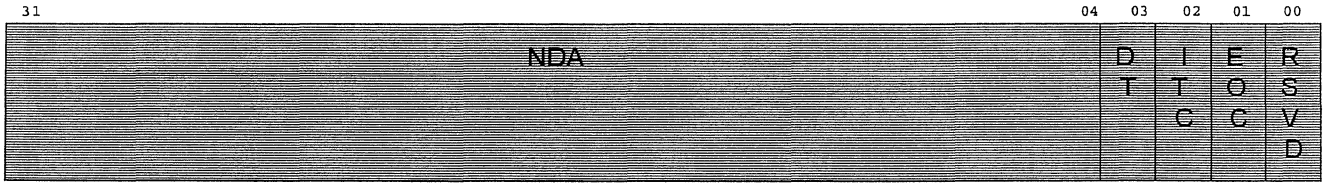


Figure D-11: DMA Channel 1 Descriptor Pointer Register

Bit	Name	Function	Read	Write	Value after Reset
00	RSVD	Reserved.	Yes	Yes	0
01	EOC	End of Chain. A 1 value indicates end of chain. A 0 value indicates not end of chain descriptor.	Yes	Yes	0
02	ITC	Interrupt after Terminal Count. A 1 value causes an interrupt to be generated after the terminal count for this descriptor is reached. A 0 value disables interrupts from being generated.	Yes	Yes	0
03	DT	Direction of Transfer. A 1 value indicates transfers from Local bus to PCI bus. A 0 value indicates transfers for PCI bus to Local bus.	Yes	Yes	0
31-04	NDA	Next Descriptor Address. Quad word aligned.	Yes	Yes	0

DMA Command/Status Register (DCSR)

Local Offset 128h

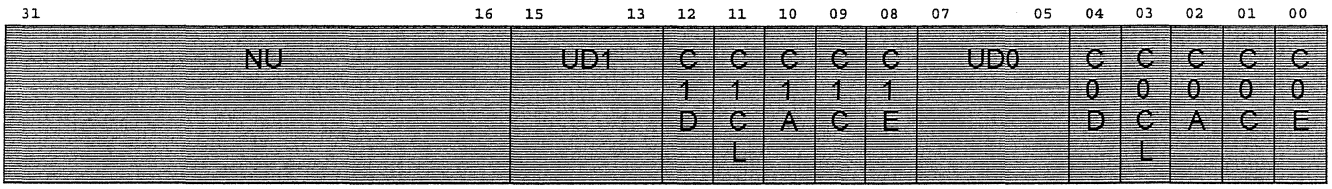


Figure D-12: DMA Command/Status Register

Bit	Name	Function	Read	Write	Value after Reset
00	C0E	Channel 0 Enable. A 1 value enables the channel to transfer data. A 0 value disables the channel from starting a DMA transfer and, if in the process of transferring data, suspends transfer (pause).	Yes	Yes	0
01	C0C	Channel 0 Control. Writing a 1 to this bit causes the channel to start transferring data if the channel is enabled.	No	Yes	0
02	C0A	Writing a 1 t this bit causes the channel to abort the current transfer. The channel enable bit must be cleared. The channel complete bit is et when the abort has completed.	No	Yes	0
03	C0CL	Writing a 1 to this bit clears channel 0 interrupts.	No	Yes	0
04	C0D	Channel 0 Done. A 1 value indicates this channel's transfer is complete. A 0 value indicates the channel transfer is not complete.	Yes	No	0
07-05	UD0	User Defined.	Yes	Yes	0
08	C1E	Channel 1 Enable. A 1 value enables the channel to transfer data. A 0 value disables the channel from starting a DMA transfer and, if in the process of transferring data, suspends transfer (pause).	Yes	Yes	0
09	C1C	Channel 1 Control. Writing a 1 to this bit causes the channel to start transferring data if the channel is enabled.	No	Yes	0

Bit	Name	Function	Read	Write	Value after Reset
10	C1A	Writing a 1 to this bit causes the channel to abort the current transfer. The channel enable bit must be cleared. The channel complete bit is set when the abort has completed.	No	Yes	0
11	C1CL	Writing a 1 to this bit clears channel 1 interrupts.	No	Yes	0
12	C1D	Channel 1 Done. A 1 value indicates this channel's transfer is complete. A 0 value indicates the channel transfer is not complete.	Yes	No	0
15-13	UD1	User Defined.	Yes	Yes	0
31-16	NU	Not Used.	Yes	No	0

DMA Arbitration Register 0 (DAR0)

Local Offset 12Ch

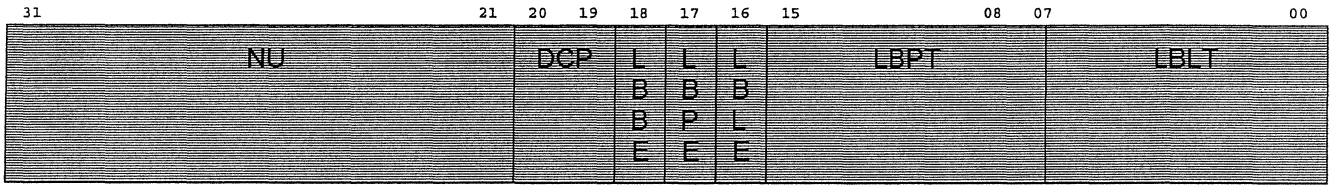


Figure D-13: DMA Arbitration Register 0

Bit	Name	Function	Read	Write	Value after Reset
07-00	LBLT	Local Bus Latency Timer. The number of local bus clock cycles before de-asserting HOLD and releasing the Local bus.	Yes	Yes	0
15-08	LBPT	Local Bus Pause Timer. The number of local bus clock cycles before re-asserting HOLD after releasing the Local bus.	Yes	Yes	0
16	BPLE	Local Bus Latency Timer Enable. A 1 value enables the latency timer.	Yes	Yes	0
17	LBPE	Local Bus Pause Timer Enable. A 1 value enables the pause timer.	Yes	Yes	0
18	LBBE	Local Bus BREQ Enable. A 1 value enables the local bus BREQ input. When the BREQ input is active, the BCI-2004 de-asserts HOLD and releases the Local bus.	Yes	Yes	0
20-19	DCP	DMA Channel Priority. 00 Rotational priority scheme 01 Channel 0 has priority 10 Channel 1 has priority 11 Reserved	Yes	Yes	0
31-21	NU	Not Used.	Yes	No	--

DMA Arbitration Register 1 (DAR1)

Local Offset 130h

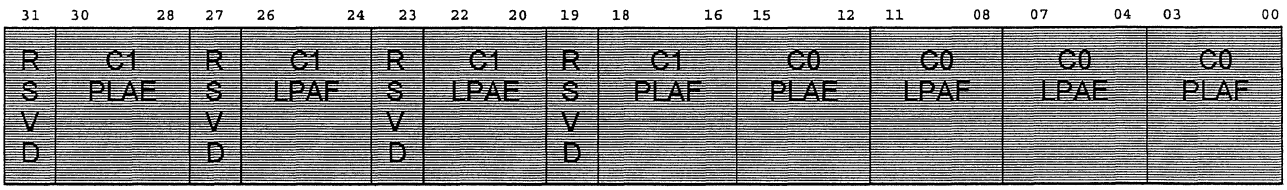
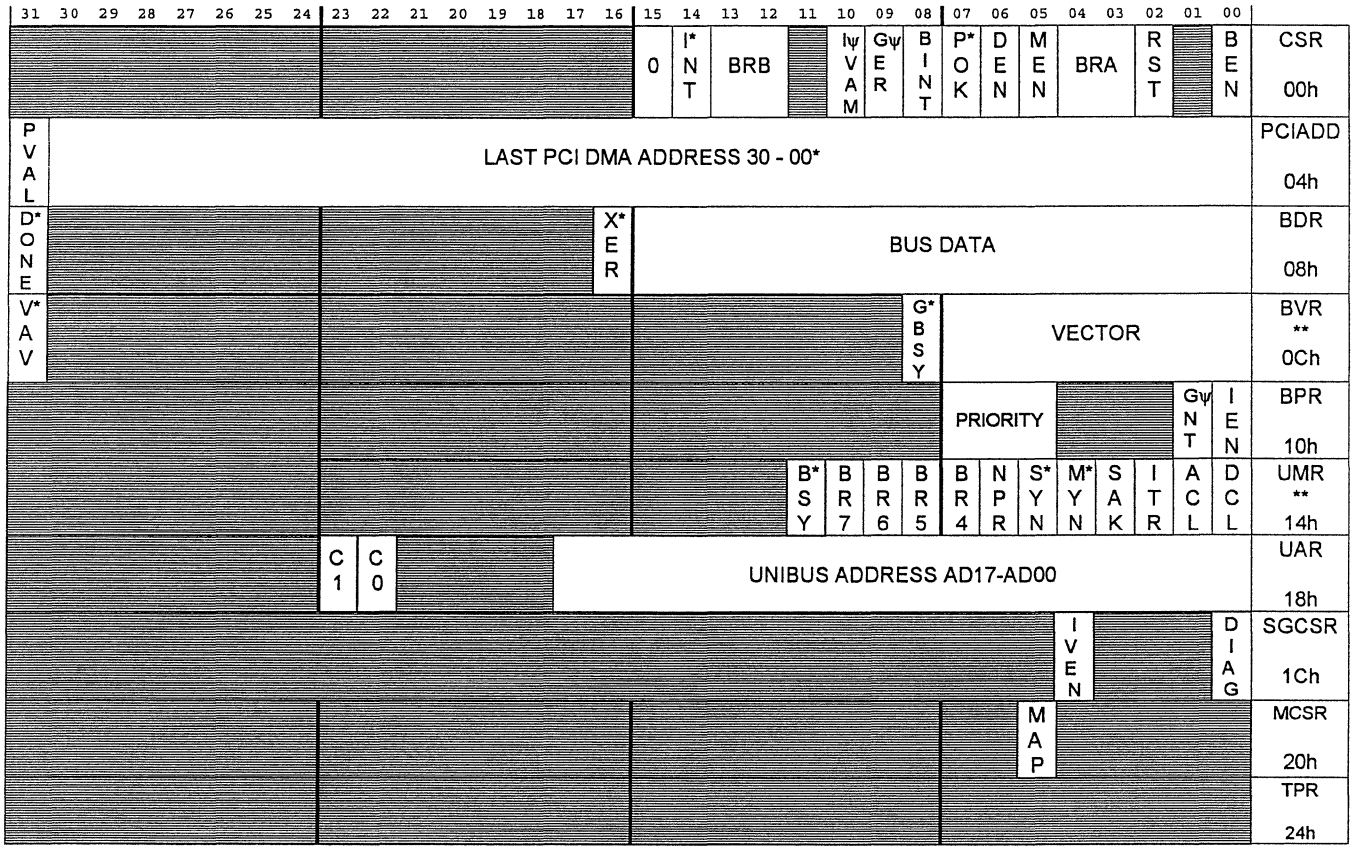


Figure D-14: DMA Arbitration Register 1

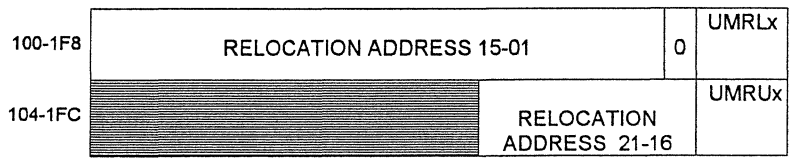
Bit	Name	Function	Read	Write	Value after Reset
03-00	C0PLAF	DMA Channel 0 PCI to Local Almost Full. The number of Full Entries (minus 1) in the FIF before requesting the local bus for Writes.	Yes	Yes	0
07-04	C0LPAE	DMA Channel 0 Local to PCI Almost Empty. The number of Empty Entries (minus 1J) in FIFO before requesting the local bus for Reads.	Yes	Yes	0
11-08	C0LPAF	DMA Channel 0 Local to PCI Almost Full. The number of Full Entries (minus 1) in the FIFO before requesting PCI bus for Writes.	Yes	Yes	0
15-12	C0PLAE	DMA Channel 0 PCI to Local Almost Empty. The number of Full Entries (minus 1) in the FIFO before requesting PCI bus for Reads.	Yes	Yes	0
18-16	C1PLAF	DMA Channel 1 PCI to Local Almost Full). The number of Full Entries (minus 1) in FIFO before requesting Local bus for Writes. (C1PLAF + 1) + (C1PLAE + 1) should be <= FIFO depth of 8.	Yes	Yes	0
19	RSVD	Reserved.	Yes	No	0
22-20	C1LPAE	DMA Channel 1 Local to PCI Almost Empty. The number of Empty Entries (minus 1) in the FIFO before requesting Local bus for Reads.	Yes	Yes	0
23	RSVD	Reserved.	Yes	No	0
26-24	C1LPAF	DMA Channel 1 Local to PCI Almost Full. The number of Full Entries (minus 1) in the FIFO before requesting PCI bus for Writes.	Yes	Yes	0

Bit	Name	Function	Read	Write	Value after Reset
27	RSVD	Reserved.	Yes	No	0
30-28	C1PLAE	DMA Channel 1 PCI to Local Almost Empty. The number of Empty Entries (minus 1) in the FIFO before requesting PCI bus for Reads.	Yes	Yes	0
31	RSVD	Reserved.	Yes	No	0

Appendix E
Reference Map of Control Registers



* This bit is read only
ψ Write one to clear
** Read only in normal mode.



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