The Multi-Application Computer

from Lockheed Electronics

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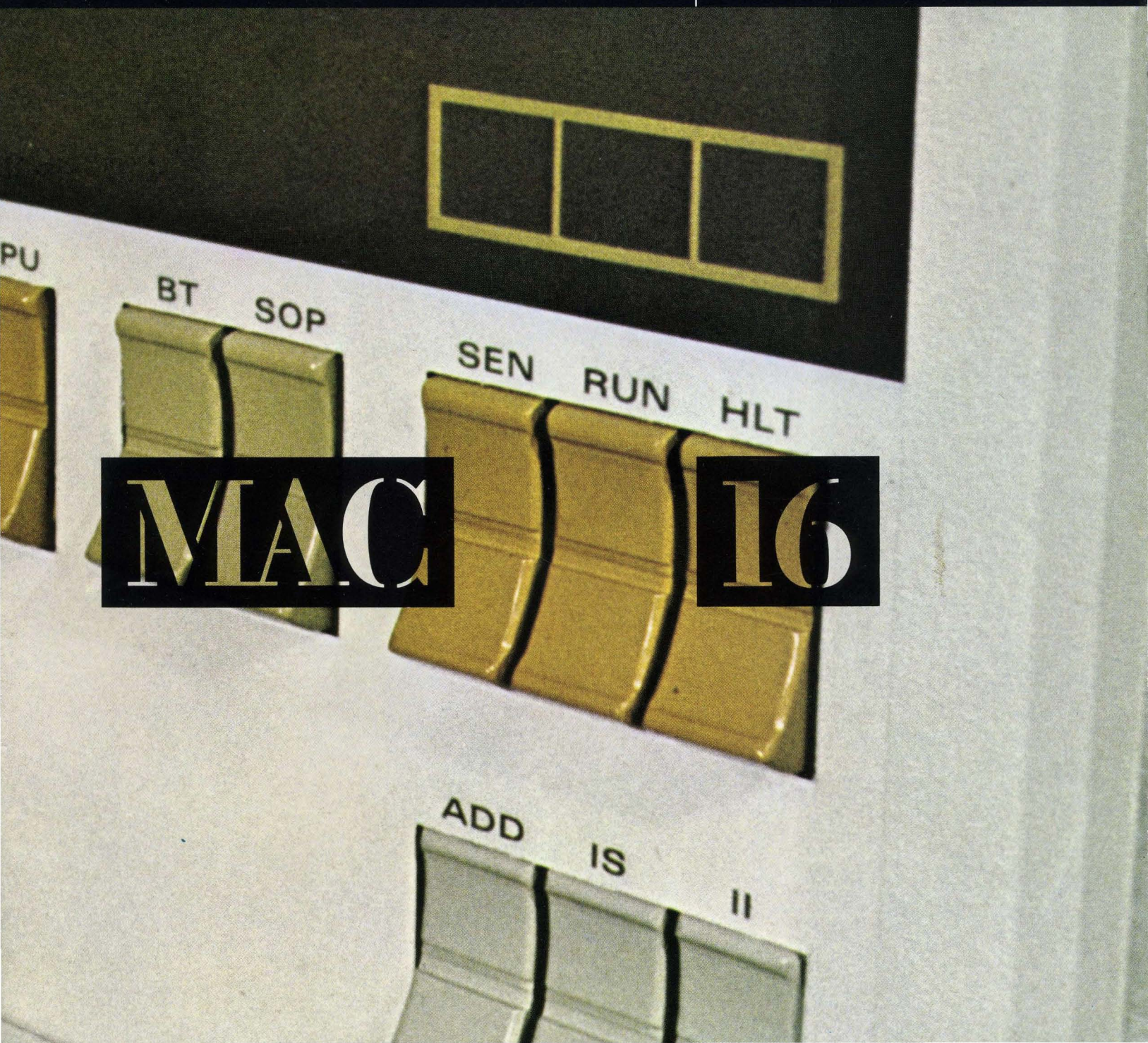


MAC 16

MAC 16 is more than another new, third-generation computer. It's a planned Multi-Application Computer, designed by Lockheed Electronics specifically for real-time digital systems. MAC is a computer with a purpose: to provide high performance yet economic solutions for today's computer-based system requirements. And with economy goes reliability, flexibility, and expandability.

Analysis of system problems dictated MAC features: a priority interrupt system in hardware to reduce programming and speed up real-time processing. A hierarchy of data channels for versatile I/O structure and high speed data transfer. And a set of 72 instructions designed for coding efficiency.

Here are features most often required: and MAC 16 has them all.

> One microsecond cycle time: for high speed computation and maximum data transfer rates.

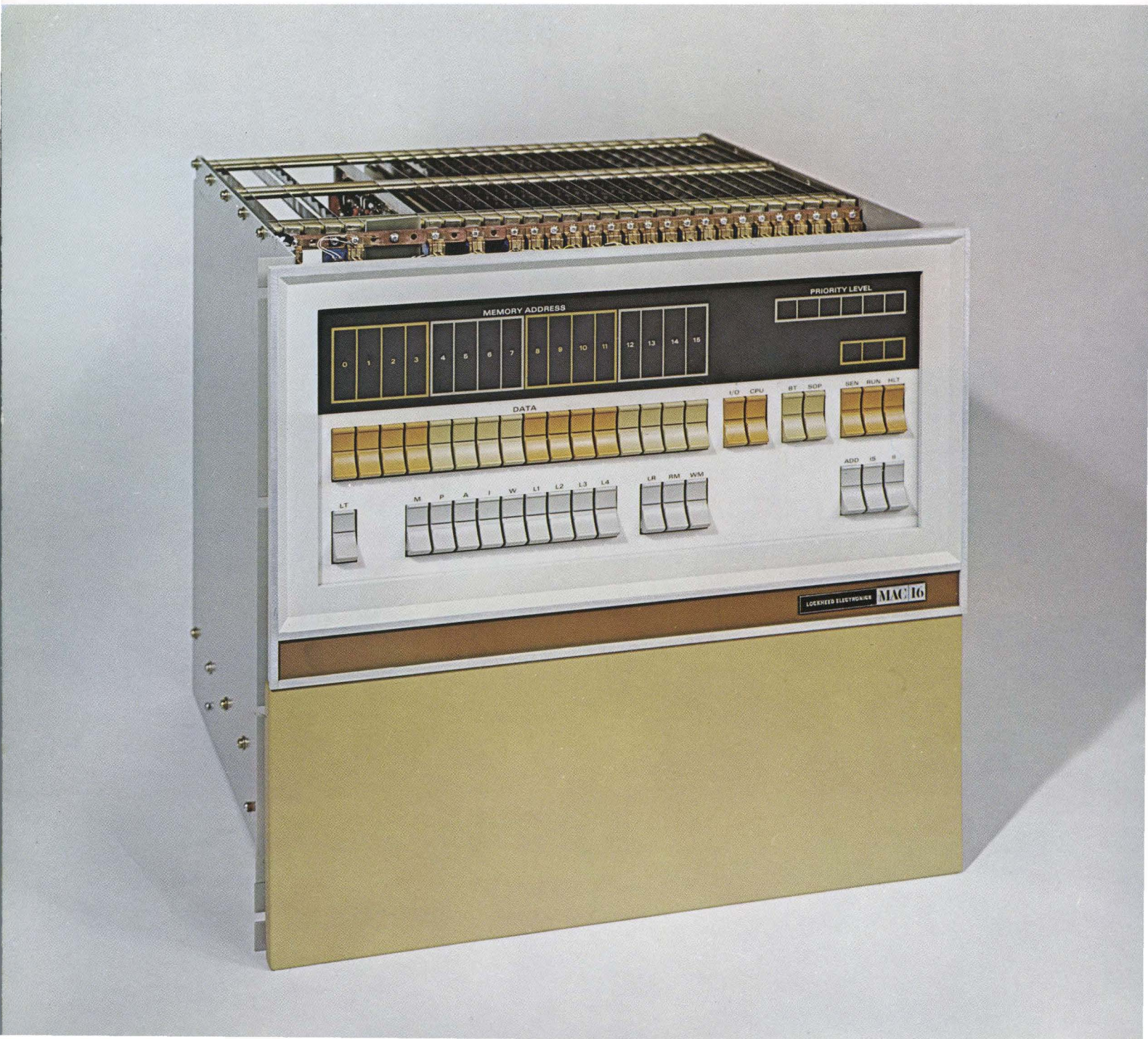
> 16-bit memory word size: for precision arithmetic, a practical instruction set and efficient byte handling.

> Priority Interrupt: a true-nested priority interrupt system for fast real-time response. An "Auto-Exec" hardware executive feature to minimize system monitors.

> Memory expansion: from 4K to 65K words with 8K in the mainframe.

> Three Data Channels: Programmed, Multiplexed, and Direct to memory with up to 255 device addresses.

> An Efficient Instruction Set: including byte handling; three-way non-destruct Compare, Test and Skip up to



15 instructions; fast shifts; hardware multiply / divide optional.

> Economic Processor Options: Power Fail-Safe, memory parity and protect, bootstrap, multiply/divide, priority interrupt expansion, and data channels which mount in the mainframe.

> Third Generation Software: FORTRAN IV, loaders, debugging and editing programs, utility routines, I/O drivers, and LEAP, a macro handling assembler that is a leap ahead of others for this class computer. And advanced off-line preparation and simulation of MAC 16 programs is provided by LEAPFORT and MACSIM.

MAC 16 is particularly well planned for the multiple unit system user. These are some features:

> Rack mounting: in 19″ RETMA rack with 17½″ front panel.

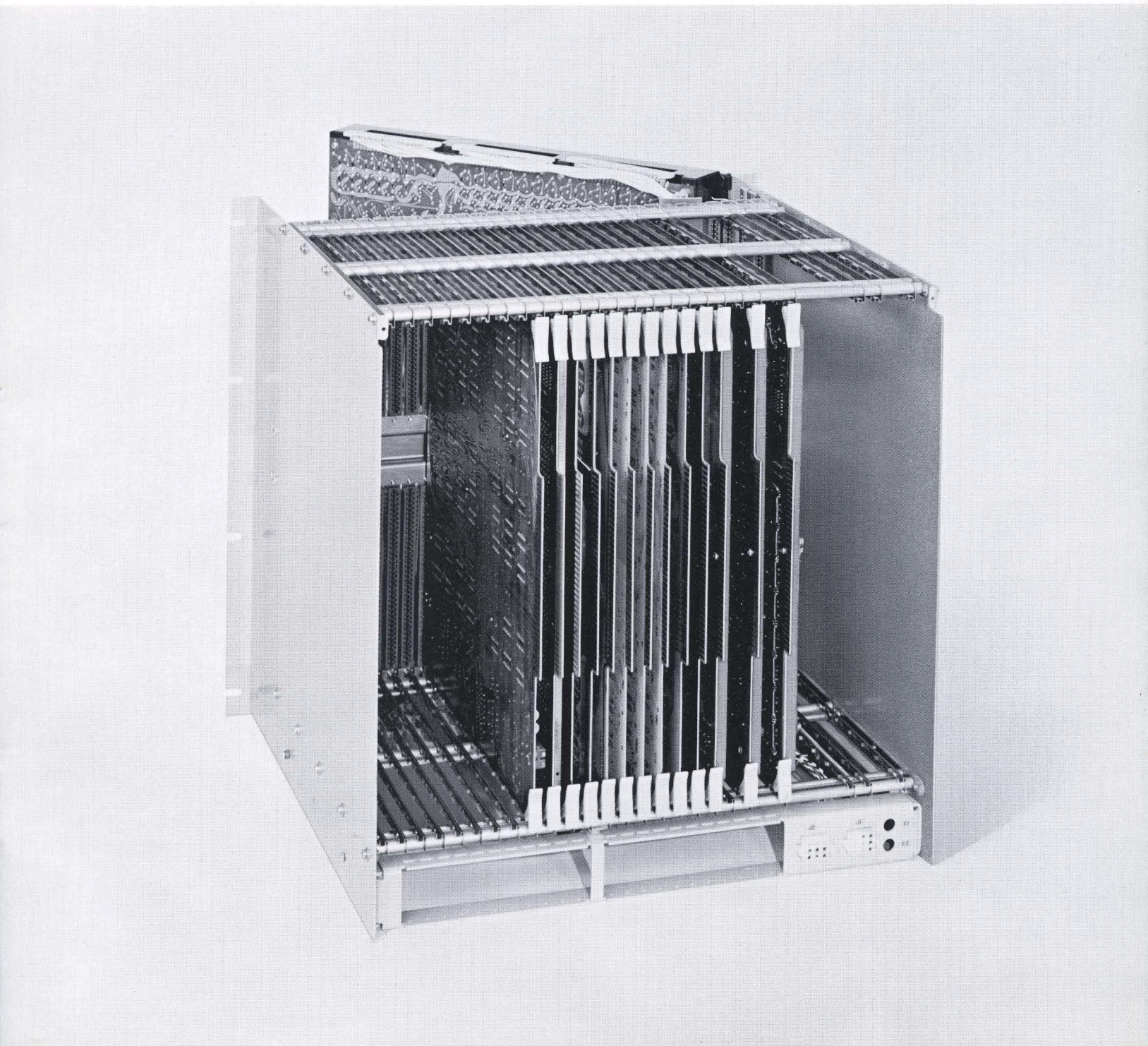
> Accessibility: a swing-out front panel exposes wiring to the front. A remotable control panel and extended test points on each card provide accessibility to the rear.

> Remotable control panel: the control panel design permits permanent relocation in a remote central console. Only simple cable extension is required.

> TTL IC logic: mounted on large PC boards for reliability and maximum packing density.

MAC is multi-application:

Data communication, acquisition, instrumentation, automatic test, and the entire spectrum of real-time control systems. MAC is ready to meet the challenge.



One Microsecond Memory with Modular Expansion

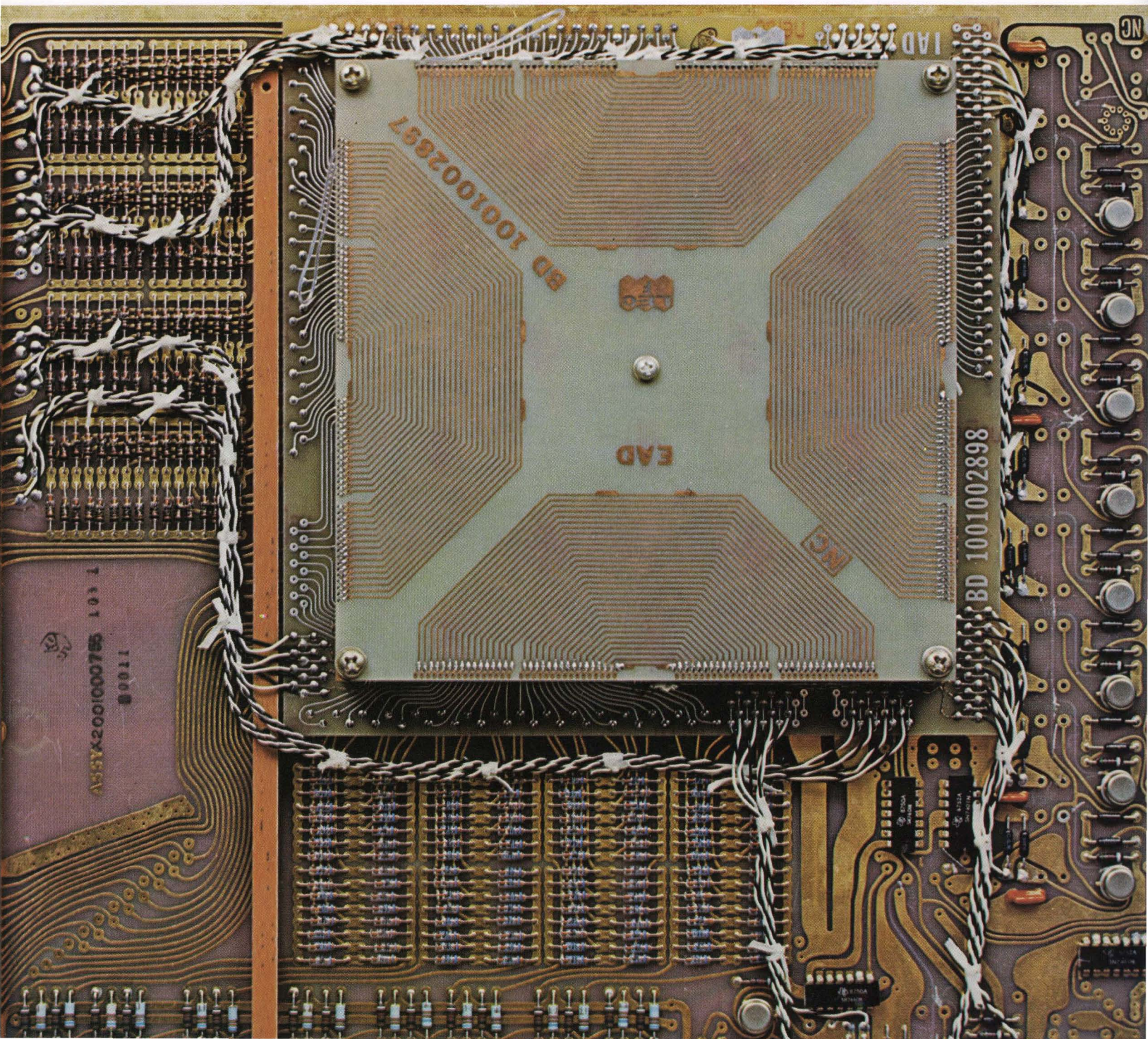
MAC 16 features a one microsecond memory cycle time; the basic computer system includes a memory module of 4,096 sixteen bit words. An 8,192 word memory capacity is provided within the processor mainframe and is supported by the power supply. Expansion is in 4K modules to a maximum of 65,536 words of addressable core memory.

Memory options available are parity check (a bit per byte) and write-protect in 4,096 word block allocations. Error detection by either option results in a processor interrupt.

Reliability and Quality, a Lockheed Hallmark

The heart of a computer is its memory. MAC 16 uses ferrite core memory modules adapted from the standard series of Lockheed memory systems. "Designed-in" reliability, far in excess of industry standards, is borne out by field-proven operation.

Since 1959, the Data Products Division of Lockheed Electronics has been a major supplier of ferrite cores, memory systems, and printed circuit boards to the electronics industry. Quality is our working philosophy and reliability a way of life. This emphasis, combined with an outstanding performance record of engineering advances, supports the MAC 16 computer system.



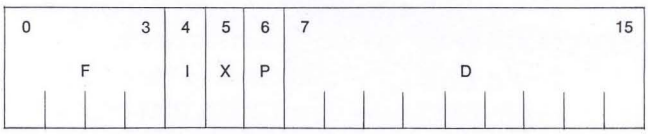
Multi-Application Processor Design

MAC 16 is designed with simple, clean internal architecture to simplify programming and data manipulation. Six 16-bit registers are used to implement MAC 16: accumulator, operand, memory address, memory word, instruction word, and program location counter. And an index register is associated with each of the four basic interrupt levels. The basic 4-bit Program Level Register is expanded to 64 bits as the priority interrupt system is augmented. One index register is added with each additional interrupt level.

Internal word formats are either a 15-bit binary data word plus sign bit, or two 8-bit bytes per word to facilitate USASCII character handling. Two's complement arithmetic is used. Memory pages are 512 words.

MAC 16 instruction words have two simple formats. Fifteen memory reference instructions have a 4-bit operation code, use a single bit each to specify indirect addressing, indexing, and base page location, and have a 9-bit address field. Thus, there are eight combinations to determine an effective memory address.

Memory Reference Instruction Word

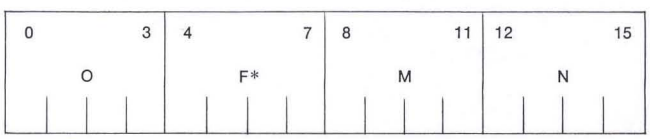


Local Page Addressing:
- Direct
- Direct with indexing
- Indirect
- Indirect, post-indexed

Base Page Addressing:
- Indirect
- Indirect, post-indexed
- Bi-level indirect
- Bi-level indirect, post-indexed

All other instructions have a format of four 4-bit fields. The most significant field in register reference instructions is always zero followed by the operation code. The two remaining fields, M and N, when used as a single field, specify device addresses or immediate 8-bit operands. When the M field is used in conjunction with the operation code, the N field specifies bit shifting, instruction skipping, or set/reset of the status bits.

Register Reference Instruction Word



Machine status and control is the function of six flip-flops in the MAC 16 processor. Each flip-flop has an associated indicator on the control panel. Two of the four status indicators are available for any use defined by the programmer; the other two are carry and overflow indicators. The machine control flip-flops are base page control and master interrupt inhibit.

The six status indicators can be set or reset, individually or in combination, by single instructions. A skip instruction is also associated with each of the six indicators; a load status instruction copies the indicators into the accumulator.

Multi-Application Configuration

MAC 16 is a computer to grow with. As requirements increase and programs get larger or peripherals are added, your MAC system can be reconfigured gracefully. Expansion options include memory modules, additional instructions, data channels and priority interrupt levels.

Space is reserved for controllers, processor options and up to 8K of memory in the basic computer. Additional teletype control, high speed paper tape reader/punch control, multiplexed data channel, multiply/divide, power fail-safe, memory parity and protect, automatic bootstrap and priority interrupt expansion are all designed for mainframe installation. The power supply, separate from the processor, will support a full load of mainframe options.

MAC 16 systems mount in user supplied 19" standard racks or in Lockheed enclosures. A desk console for the basic system or a 62" rack for larger systems is available.

Processor Options for Flexibility

True to its Multi-Application name, MAC 16 is available with processor options which match performance with system requirements.

The Hardware Multiply and Divide instructions execute in 9 and 12 microseconds respectively. The dividend and the product formed are 32-bit double words.

Power failure detection automatically stores the operational registers with an orderly shutdown to preserve the contents of memory. An elective to this option is automatic restart when normal power is restored.

The Memory Parity system generates or checks odd parity per byte on each transfer operation. The memory word with parity option consists of 16 data bits plus a parity bit per byte. Detection of a parity error causes a processor interrupt.

Memory Protection is provided in optional modules of 4,096 words. Protected and unprotected modules can be mixed in a single system. Attempts to write in a protected area will be inhibited and generate a processor interrupt.

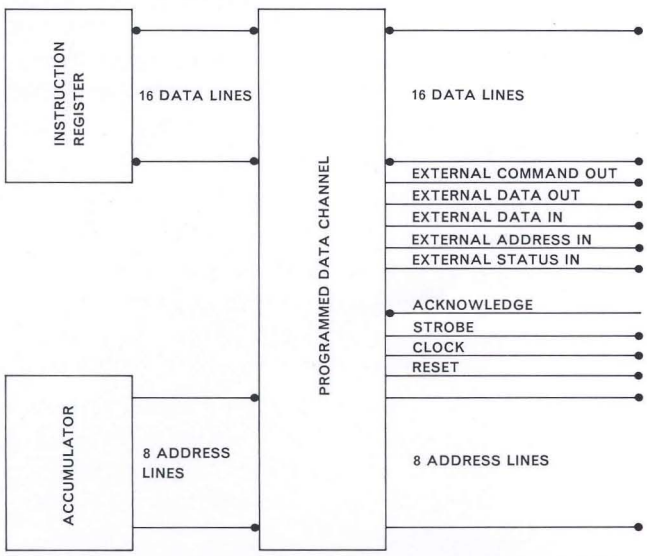
The Automatic Bootstrap option is a 63-word diode memory program for Teletype paper tape imput. The diode memory program is entered in core memory when the control panel Bootstrap switch is pressed. This feature simplifies system start-up by operating personnel.

Input/Output: the Measure of the Machine

Input/Output capabilities make MAC 16 outstanding among other computers. Low, intermediate, and high speed data transfers are permitted with the MAC 16 computer through the basic Programmed Data Channel, the optional Multiplex Data Channel and Direct Memory Access Channel. Data word rates up to 90 KHz, 333 KHZ, and 800 KHz are practical via these three input/output channels. All channels can transmit data in either word or byte mode. Each channel permits progressively higher system performance by providing a greater degree of independent and automatic control of data communication.

The Programmed Data Channel, basic to the MAC 16 computer, is used for input/output via the accumulator from low speed devices and for control of high speed peripheral devices connected to the optional high speed channels. The Programmed Data Channel is uniquely qualified for its assigned task through the organization of data, address, and function lines.

Programmed Data Channel Interface



The PDC is controlled by five instructions: Data In, Data Out, Address In, Command Out, and Status In. Each instruction is identified by a single line in the PDC to minimize decoding in peripheral device controllers.

The Status In instruction permits up to 4,080 external sense lines to be recognized. Address In results in immediate recognition of devices sharing a common interrupt; polling of devices is not required. Command Out removes the task of specifying functions from the address lines and permits 255 peripheral device controllers to be connected to the PDC and controlled directly.

Multiplex Data Channel

Input/Output capability is augmented by the addition of the optional Multiplex Data Channel. Sixteen device controllers can be connected to the MDC for transfer of data concurrently. Two operational modes can be specified under program control during MDC initialization. The normal mode permits data transfer and computation to be interleaved with up to 16 device controllers active. The burst mode permits data transfer from or to a single device controller at a word rate of 333 KHz.

The MDC allows either word or byte mode to be specified at time of initialization. In the byte operation mode, left and right bytes are packed or unpacked for input or output as a function of the MDC word buffer and byte logic. These functions are not required in the design of the external device controller. Controllers can be connected to either the PDC or MDC without modification as an aid to system re-configuration.

Direct Memory Access

Data transfers to memory concurrent with computation are possible in byte or word mode using a Direct Memory Access channel. The processor and Direct Memory Access channel access memory on an interleaved, cycle stealing basis. DMA data transfer rates up to 800 KHz are practical.

Basic DMA controls data transfers from and to a standard device controller. Through use of a Memory Priority Switch option an expanded configuration of four device controllers is possible. Interleaved, simultaneous operation of the four devices and priority among them is controlled by the memory switch hardware.

Device controllers connected to DMA contain a block length counter, address counter, DMA interface controls, and the necessary peripheral device controls. Operating parameters are established under program control via the PDC. Initialization of device controllers is accomplished with four instructions: Data In, Data Out, Command Out, and Status In.

Real-Time "Auto-Exec" System

Multi-programming requirements are met by the MAC "Auto-Exec" system, a true-nested priority interrupt system unique to small-scale computers. MAC 16 has four interrupt levels as a standard feature and can be expanded economically to 64 "Auto-Exec" levels.

Each additional "Auto-Exec" program interrupt level is implemented in an expandable Program Level Register. Each level is assigned a dedicated nest of four memory words. These four locations provide storage for the accumulator, index register, location counter, and status bits. The Auto-Exec system automatically stores and restores the operational registers when an interrupt occurs. The programmer is relieved of this task.

Instructions associated with the interrupt system allow the programmer to determine the current program level, set an interrupt, enable or disable the interrupt system, or jump with reset of the interrupt level. Interrupts can be initiated either internally or externally with response in six microseconds.

Priority levels within Auto-Exec can be dynamically allocated under program control. Job queues can be formed, split level tasks specified and privileged I/O assigned, all occurring at the hardware level and at hardware speeds. These features, with the re-entrant subroutine library, combine to form a true real-time system.

7

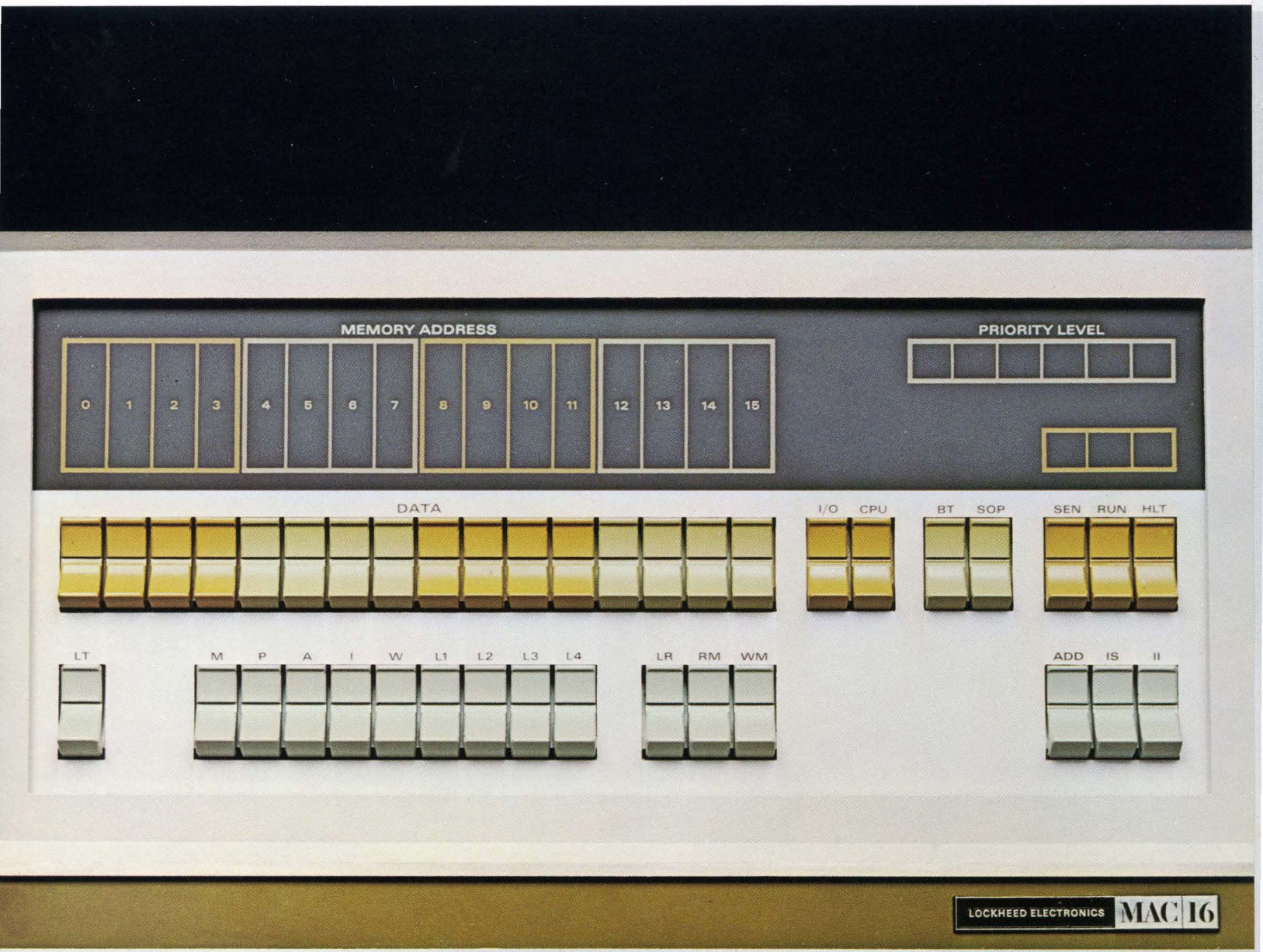
Convenient Control

The MAC 16 control panel was carefully planned for normal operation as well as console debugging. Switches are designed for rapid, positive action. An indicator lamp test switch is provided; a control panel lock is optional. Complete "state-of-the-machine" display is possible including all registers, program level, and status. Memory read/write, halt-on-address, and single step instruction switches facilitate program testing.

All indicators are rear illuminated for easy visual interpretation; eight alphabetic indicators define machine state and operating mode. Panel display is active when the computer is in the "run" mode. The panel can be located remote from the processor to adapt to special system requirements.

Large, Versatile Instruction Set

MAC 16 has a programmer-planned set of 72 instructions designed for coding efficiency. Test and Skip instructions permit skipping up to 15 instructions in sequence, not just one. The memory reference Compare and Skip instruction preserves the content of the accumulator and results in a three-way skip. Fast shift instructions are designed for easy bit manipulation. Multiple precision arithmetic is simplified by carry and overflow indicators. Byte oriented instructions are included for internal character handling. Optional hardware multiply/divide instructions are available. An efficient set of 5 input/output instructions facilitates data communication and transfer.



MAC 16 Instruction Set

	Mnemonic	Function	Time in Microseconds
Load and Store	LDA	Load A from memory	2
	LDX	Load Index from memory	3
	LAX	Load A from X + N	3
	LIX	Load A Indirect from (X) + N	4
	LDI	Load A Immediate Byte	1
	LSB	Load A Status Bits	1
	STA	Store A in memory	2
	STL	Store byte from A in left byte of memory	2
	STR	Store byte from A in right byte of memory	2
	STX	Store Index in memory	3
	SAX	Store A in X + N	3
	SIX	Store A Indirect in (X) + N	4
	SSB	Store A_{0-5} in Status Bits	1
Arithmetic	ADD	Add memory to A	2
	SUB	Subtract memory from A	2
	ADI	Add Immediate byte to A	2
	SBI	Subtract Immediate from A	2
	TWA	Two's complement of A	2
	ABA	Absolute Value of A	2
	ADC	Add carry to A	2
	MPY	Multiply A by memory (option)	9
	DIV	Divide A by memory (option)	12
Logic	ANA	AND memory with A	2
	ORA	OR memory with A	2
	ONA	One's complement of A	2
Shift	ALS	Shift A left arithmetically N bits, Save Carry	2-5
	ALI	Shift A left arithmetically N bits, Insert & Save Carry	2-5
	ARS	Shift A right arithmetically N bits, Save Carry	2-5
	ARI	Shift A right arithmetically N bits, Insert & Save Carry	2-5
	LLN	Shift A left logically open, N bits	2-5
	LLO	Shift A left logically open, N bits, Save Carry	2-5
	LLC	Shift A left logically closed N bits, Save Carry	2-5
	LLI	Shift A left logically N bits, Insert & Save Carry	2-5
	LRN	Shift A right logically open N bits	2-5
	LRO	Shift A right logically open N bits, Save Carry	2-5
	LRC	Shift A right logically closed N bits, Save Carry	2-5
	LRI	Shift A right logically N bits Insert & Save Carry	2-5
Jump	JMP	Jump unconditional	2
	JMM	Jump and mark	3
	JRL	Jump and reset level	2
	JMX	Jump unconditional to X+N	3
	JIX	Jump unconditional to X+N Indirect	4
	JMA	Jump unconditional to A, Save P+1 in A	2
Test and Skip N	SKP	Skip unconditional	2
	SNC	Skip on No Carry	2
	SNV	Skip on No Overflow	2
	SNH	Skip on not inhibit interrupt	2
	SNB	Skip if base page control is zero	2
	SNR	Skip if R is Zero	2
	SNS	Skip if S is Zero	2
	SKN	Skip if A is normalized	2
	SAN	Skip if A Negative	2
	SAZ	Skip if A zero	2
	SAG	Skip if A greater than zero	2
	SLZ	Skip if A less than zero	2
	SKX	Skip if X is zero	2
Index and Skip	INX	Increment Index by N and Skip if exceeded	3
	DNX	Decrement Index by N and Skip if exceeded	3
Compare Memory and Skip	CAA	Compare A with memory arithmetically and skip (3 way)	3
Increment Memory and Skip	INC	Increment memory and skip if zero	3
Register	CLA	Clear A	1
	XXA	Exchange A and X	3
	TSA	Transfer Data Entry Switch to A	1
	TLA	Transfer Current Program Level number to A	2
Control	NOP	No operation	2
	HLT	Halt	1
	TAL	Transfer A to Interrupt Priority Reg.	1
	SEX	Set all indicators: C, V, R, S, B, H	1
	REX	Reset all indicators: C, V, R, S, B, H	1
Device Control	ECO	External Command Out, Skip P+1 if acknowledged	3
	EAI	External Address In	3
	ESI	External Status In	3
Input/Output	EDI	External Data In, Skip P+1 if acknowledged	3
	EDO	External Data Out, Skip P+1 if acknowledged	3

System Software Designed for Programmers

Software for MAC 16 was created to meet multiple requirements of the user-programmer. Maximum efficiency is provided for the sophisticated user creating complex programs without impeding the occasional programmer having more straightforward tasks. Each of the system programs will operate on the minimum configuration: 4K words of memory and as ASR teletype.

LEAP, the MAC Assembler Program

Lockheed **E**lectronics **A**ssembly **P**rogram is perhaps the most advanced system available in today's small computer market. A two-pass assembler, LEAP provides automatic depaging of the object program at load time. Up to 200 symbols and literals can be defined when operating on a 4K system. Pseudo-operations are included to direct the assembly process, define constants and memory locations, reserve or clear storage areas, and to define external programs and data. Complex expressions, including parentheticals, can be used. Literals can specify a variety of numeric formats as well as character strings. And LEAP includes programmer defined macros. The programmer is aided by comprehensive error checking and alphabetized symbol table listing.

Program Loaders

The Extended Program Loader accepts the programs assembled by LEAP to provide program relocation, automatic depaging, and linking of associated programs and subroutine calls at load time. For maximum utilization of memory, LEAP also generates object code in Absolute Loader format. Both loaders incorporate checking features to guarantee accurate input.

Program Preparation on Large-Scale Computers

LEAPFORT, the MAC 16 LEAP assembler coded in USASA Standard FORTRAN IV, can be supplied to users having large-scale equipment at their disposal. LEAPFORT accepts MAC 16 LEAP source language and produces an assembled program which can be executed on the MAC 16 computer. Alternatively, simulation of MAC 16 operation using large-scale hardware is implemented by MACSIM, also coded in ASA FORTRAN. All features of MAC 16 processing are simulated including input/output and the interrupt system. Program execution time for the MAC 16 computer is tabulated and listed.

Used alone, LEAPFORT expedites program assembly for MAC 16 execution. Used together, LEAPFORT and MACSIM are valuable tools for complete advance preparation of user programs. On-line MAC 16 debugging time is minimized.

Programmer Aids

Tools-of-the-trade are also supplied in the MAC 16 software system. The source Tape Editor facilitates preparation and changes in symbolic language tapes. The Debug Program gives the user direct communication with the MAC 16 system and control of the program under test. Operating from the teletype, the Debug Program provides a printed record of all test activity. Time consuming

manipulation and inspection of the control panel during program test is virtually eliminated.

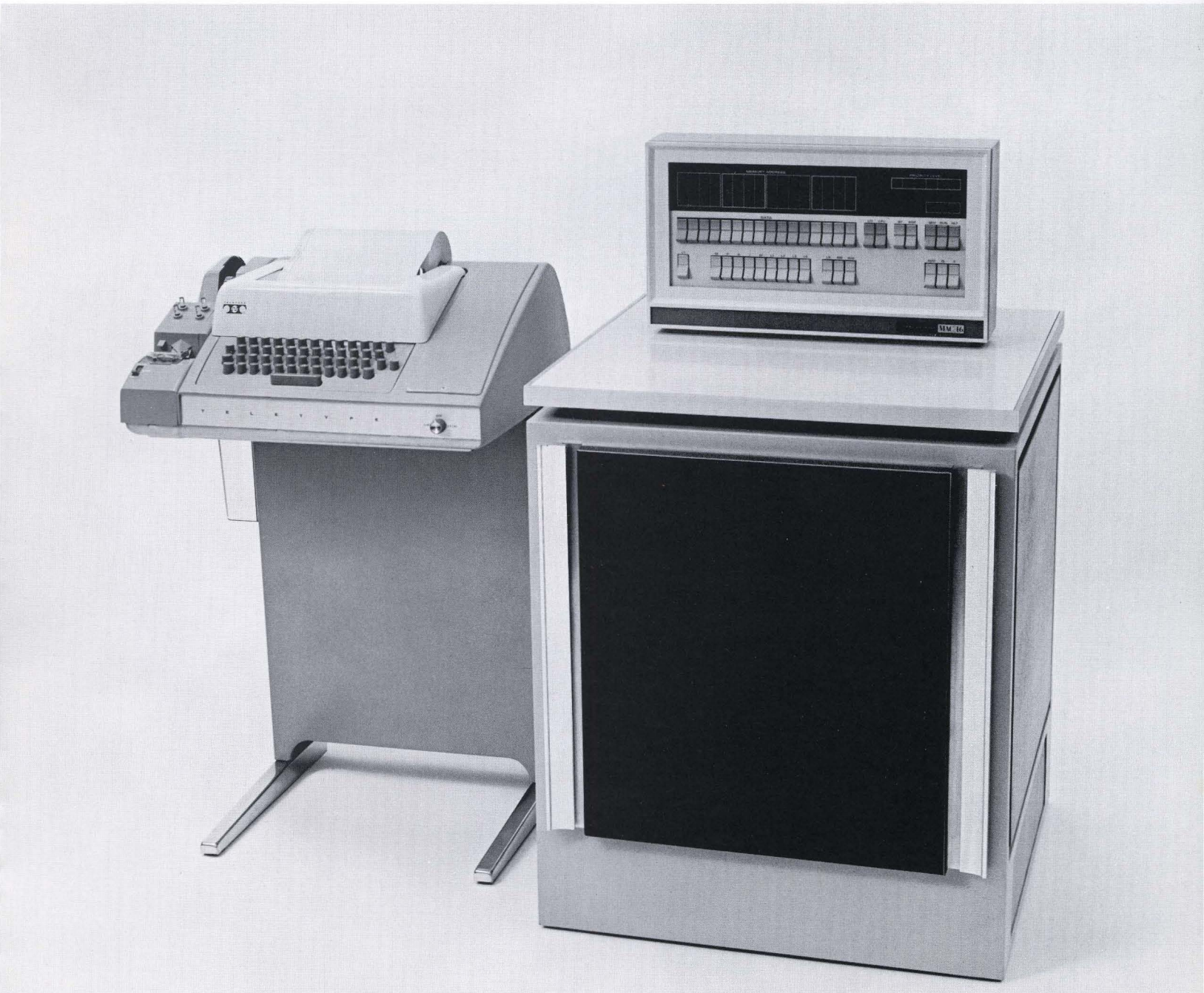
The MAC library includes program subroutines to meet a wide variety of user requirements. Major sections contain re-entrant subroutines for mathematical functions and conversion in fixed point, floating point, and double precision. Input/Output drivers for standard peripheral devices and utility programs are also included in the program library. Quick-check hardware diagnostic programs are supplied to test logic functions, memory operation, and peripheral devices. These programs provide a means of rapid isolation of machine malfunction.

System Documentation

A comprehensive set of technical publications has been prepared for users of the MAC 16 computer system. All aspects of theory and operation of hardware and related software systems have been clearly and accurately described. Emphasis has been placed on detailed, step-by-step operating instructions.

Customer Training and Service

The MAC 16 computer system is fully supported by Lockheed Electronics installation and warranty service. Customer training consisting of a one week course each in programming and in maintenance is provided at the manufacturing facility. A complete set of documentation manuals and system program tapes is included in each system shipment and supplied to individuals attending the training courses. Contract or on-call maintenance service is available from regional centers.



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