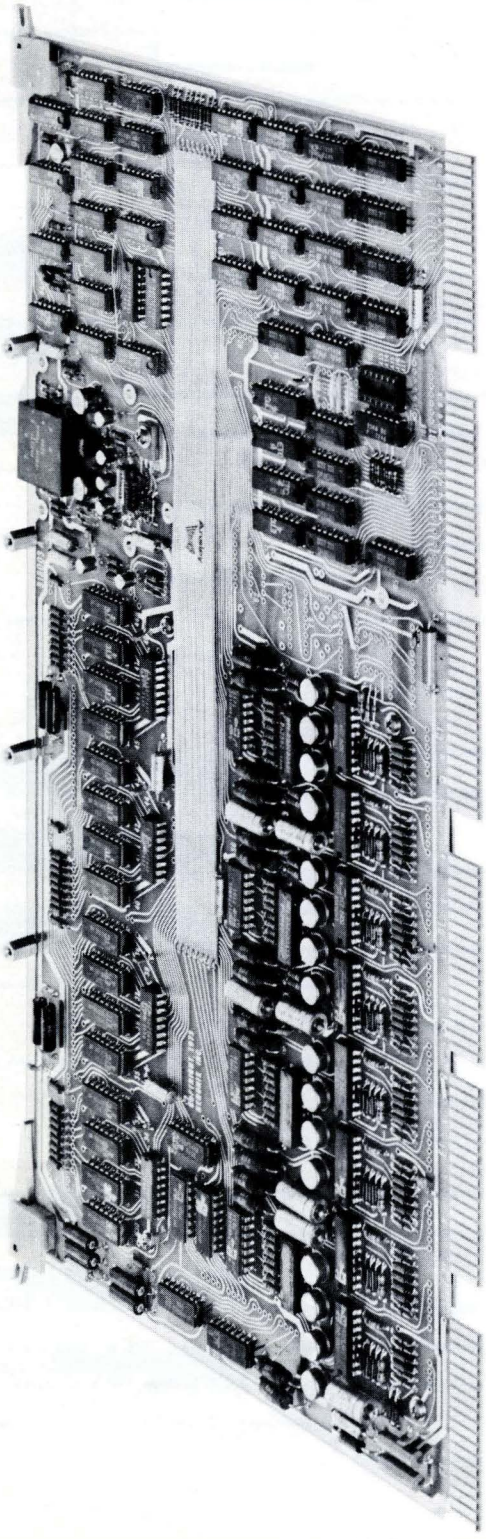
KERONIX PLUG COMPATIBLE CORE MEMORY SYSTEMS D SERIES ,
FULLY COMPATIBLE WITH DEC PDP-11[T.M.]
MM11-L MEMORY



Features:

Keronix plug-compatible D Series core memory systems offer:

- Reliable, virtually damage-proof circuitry
- 4Kx16 or 8Kx16 storage capacity on one single unit. Optional parity
- Operate with, or in place of, DEC MM11-L memory in PDP11 systems and ME11-L expansion chassis
- One 8K module requires only one connector slot to plug into and one adjacent slot for piggy-back memory magnetics (vs three connector slots for the MM11-L)
- Optional interleaving capability at no extra charge
- Exclusive unitized construction
- Thoroughly pre-tested. Each memory module goes through a minimum of 50 hours of power margining burn-in in a specially designed "exerciser", and 24 hours of computer run-in prior to release
- Simplified field service
- One-year warranty. Exchange-replacement boards available worldwide, usually within 24 hours.

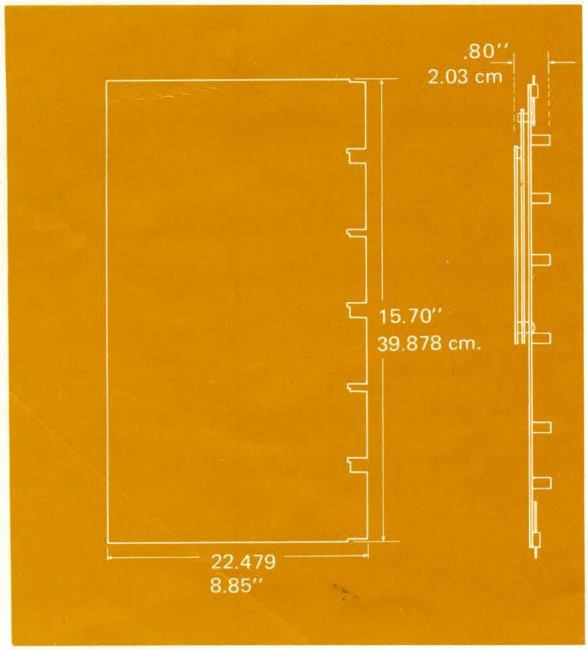
1752 Cloverfield Boulevard Santa Monica, California 90404
(213) 829-3594 TWX 910-343-6480

KERONIX INC.

D SERIES

Technical Specifications

TYPE:	3 wire - 3D coincident current.
CAPACITY:	8192 words x 16 bits.
FIELD EXPANSION:	Up to 124K of 16 bits in 8K or 4K increments.
SPEEDS:	Full cycle time 850 nanoseconds. 750 nanoseconds optional
CYCLES:	Read/Restore Clear/Write Read/Pause/Write
LOGIC INTERFACE:	Utilogic or TTL
VOLTAGE REQUIREMENTS:	+5vdc ± 5% 2.0a amp max. −15vdc±5% 3.5a max. at 850ns cycle. 4.5a max. at 750ns cycle
TEMPERATURE RANGE:	0°C to +60°C
DIMENSIONS:	See figure 1



For additional information please write or call
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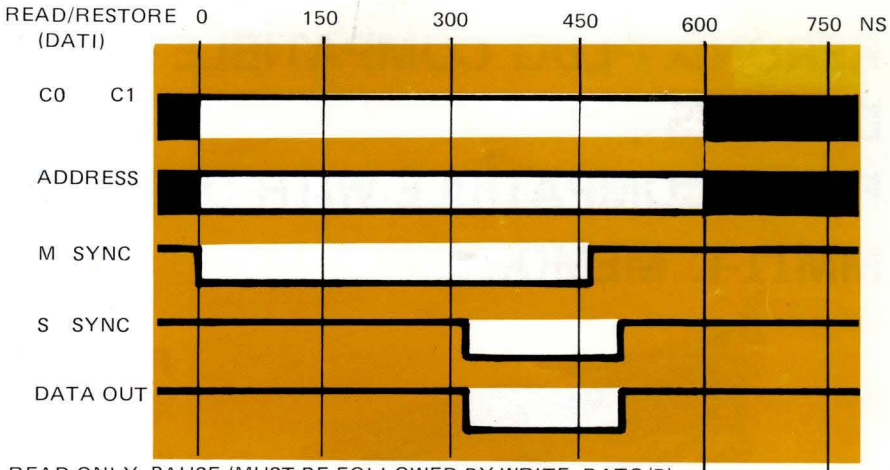
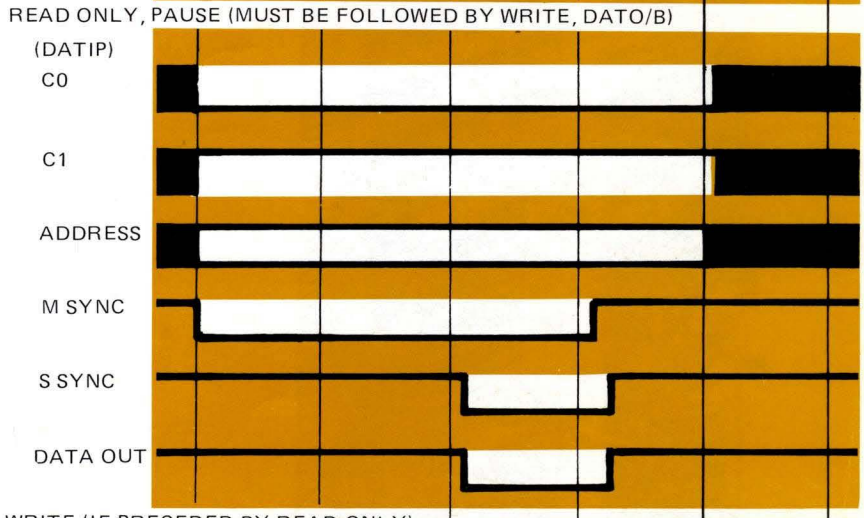
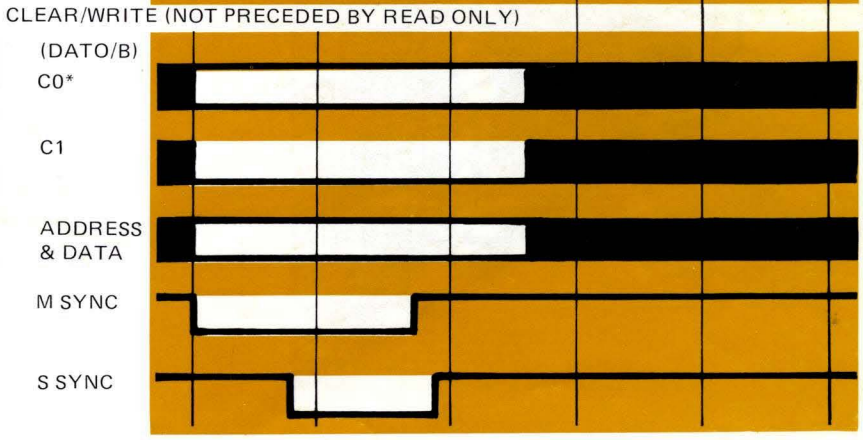




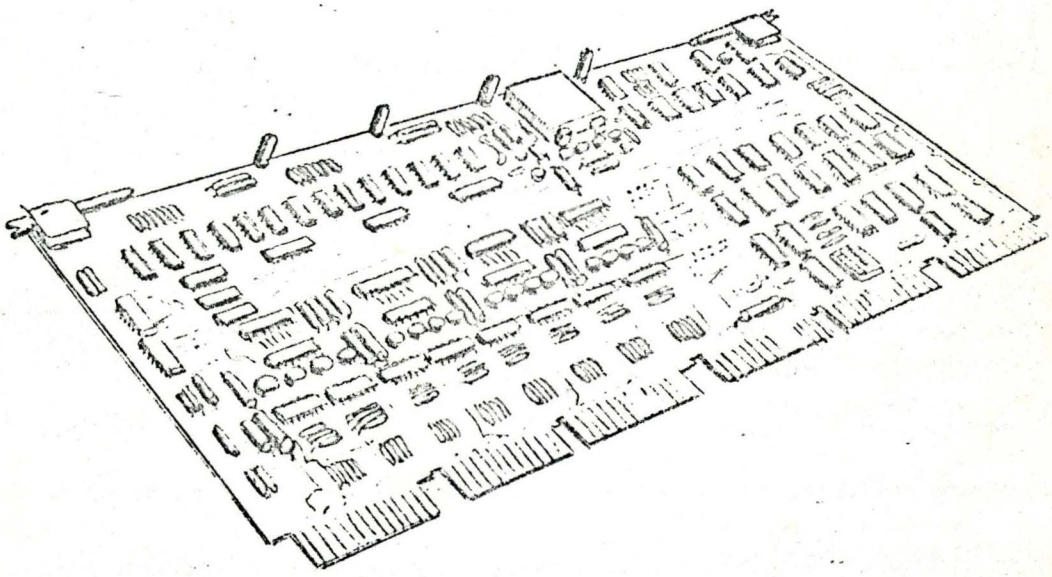


* CO LOW = WRITE FULLWORD
CO HIGH = WRITE BYTE, DETERMINED BY A00
BLACK BARS INDICATE UNDETERMINED OR NOT CRITICAL STATES.

KERONIX

TECHNICAL MANUAL

KERONIX 16K×16-D MEMORY SYSTEM REFERENCE AND INSTALLATION MANUAL



MARCH, 1975

KERONIX, INC. 1752 Cloverfield Boulevard ■ Santa Monica, Calif. 90404
(213) 829-3594 • TWX 910-343-6480

TABLE OF CONTENT

ILLUSTRATIONS

1.0 INTRODUCTION

This manual provides a physical description, specifications and installation procedures for the Keronix "16K-D" memory system.

The Keronix "16K-D" memory is compatible with the DEC MM11-L core memory used in the DEC PDP 11/05, PDP 11/10, PDP 11/40, and PDP 11/45 computer. It will also fit into the ME11-L expansion box. It plugs directly into the unibus connectors.

The Keronix "16K-D" memory provides 16K words of 32K byte capacity in only 2 card spaces. It does not contain parity option or status registers but is otherwise completely hardware and software compatible.

The Keronix "16K-D" memory is furnished with bank interleaving. The starting address may be specified at any 8K boundary. A special circuit allows for the de-selection of a portion of the upper memory to be used as device registers. An 18 bit address decoding allows the selection of up to 8 16K banks to a total of 128K 16 bit words. A bank selection switch on the circuit board determines the memory banks location in the address field.

2.0 PHYSICAL DESCRIPTION AND OPERATION

This section provides information about the physical layout of the memory system and a description of the operations.

In order to assure compatibility of the Keronix "16K-D" memory with the PDP-11 architecture the following specifications were applied.

A) The Keronix "16K-D" memory is mounted on a DEC compatible 6 connector board which will plug into the unibus connectors.

2.0 PHYSICAL DESCRIPTION AND OPERATION (cont'd)

B) Operation is in accordance with the DEC unibus philosophy of the master-slave relationship.

C) The bus driver and receiver interface circuits conform to the DEC unibus receiver and transmitter specifications.

D) All input and output signals are as defined for the PDP-11 unibus.

E) Bus grant continuity is provided on the memory by jumpering DK2 to DL2, DM2, to DN2, DP2 to DR2 and DS2 to DT2.

F) Power protection circuits are provided to assure memory integrity during a power failure.

G) A selectable portion of the upper memory may be reserved for device register addresses.

2.1 PHYSICAL LAYOUT AND DIMENSIONS

The Keronix "16K-D" memory system is mounted on a single DEC compatible hex wide printed circuit board. It will plug directly into the PDP-11 unibus. The core memory array is mounted on the back of the circuit board. Because of the overhang of the memory array the next card slot in the computer frame must be empty except for slot A and B.

For memory dimensions see Figure 1.

The overall dimensions are:

length	8.87 inches
width	15.72 inches
height	.825 inch

2.1 PHYSICAL LAYOUT AND DIMENSIONS (cont'd)

Each memory board is furnished with an insertion extraction lever mounted on each side of the board. This allows for easy insertion and extraction of the board.

2.2 MEMORY OPERATIONS

The memory operates only in slave mode on the PDP-11 bus. Its operations are specified by the memory address lines, 2 control lines and 16 bidirectional data lines.

The Keronix "16K-D" memory is capable of decoding 18 address lines. The lowest significant address bit A00L is only used during write byte operations to specify the upper or lower data byte. The next 13 address bits A01L through A14L are used to specify one of the 16.348 memory word locations. Address bit A15L, A16L and A17L are used to specify the bank locations in the address field.

The two control lines COL and CIL together with the least significant address bit A001 specify the operation to be performed by the memory system.

All signal lines are shown in their logical true state at which a logical "1" corresponds to 0V while a logical "0" corresponds to approximately +3V on the PDP-11 unibus.

2.1 MEMORY OPERATIONS (cont'd)

COL	CIL	A00L	CODE	OPERATION
0	0	X	DATI	Read full word from memory and restore memory content.
1	0	X	DATIP	Read full word from memory. Do not restore memory content.
0	1	X	DATO	Clear memory content and write new data into memory.
1	1	0	DATOB	Write new data into bit 15-8. Restore data in bit 07-00.
1	1	1	DATOB	Write new data into bit 07-00. Restore data in bit 15-08.

2.2.1 DATI READ FULL WORD

The memory will read data from the memory location specified at the leading edge of MSYN and transmit the data to the bus master with SSYN. The data on the bus will become true approximately at the same time as SSYN and remain true as long as SSYN remains true. SSYN is reset by the trailing edge of MSYN. Since the read-out of the data from the core stack destroyed the data content. A restore cycle is initiated automatically by the memory system. The memory will remain busy for approximately 900ns after the leading edge of MSYN. Data and SSYN is supplied to the bus by the memory approximately 330ns after the leading edge of MSYN.

2.2.2 DATIP READ AND PAUSE

This operation will proceed like the DATI operation except that the memory content is not restored after the readout. This operation must be followed by a DATO or DATOB operation to restore the memory content. The DATIP operation is used for read-modify-write operations by the computer.

The memory will remain busy for only about 500ns after the leading edge of MSYN.

2.2.3 DATO WRITE FULL WORD

The memory will store the data present at the leading edge of MSYN at the address location specified by the bus master. A SSYN signal is returned after about 150ns. This signal is reset after the trailing edge of MSYN. The memory location specified is first cleared by a dummy read operation and then loaded with the new data. If the previous operation was a DATIP read and pause operation the new data is loaded immediately.

The memory will remain busy for about 900ns for a write operation or about 600ns following a DATIP operation.

2.2.4 DATOB WRITE BYTE

This operation is performed in either of two ways depending on whether the operation was preceeded by a DATIP operation.

Only one byte of data specified by address bit A00L is to be changed in memory. The other byte shall remain undisturbed.

If the previous operation was not a

2.2.4 DATOB WRITE BYTE (cont'd)

DATIP the new byte of data is strobed into the memory buffer by the leading edge of MSYN. The memory performs a read operation at which the cores for the new data byte are cleared and the data is lost. The cores for the remaining data byte are also cleared but the data is saved in the second half of the data buffer. The whole memory word is then written back into the memory by a write operation. The memory will generate a SSYN signal after about 150ns and remain busy for about 900ns.

If the previous operation was a DATIP operation the new data byte is strobed into the memory buffer by the leading edge of MSYN. The remaining byte is not changed and should contain the data byte remaining from the last DATIP operation. The whole memory word is written immediately into the addressed location. The memory will generate a SSYN after about 150ns but will remain busy for only 600ns.

2.3 INTERLEAVING

Memory interleaving is a method of increasing data transfer rates between memory and high speed I/O devices.

This is accomplished by exchanging the highest (A15L) and the lowest (A01L) address bits. The highest address bit is normally used to select the memory bank which is to execute the operation. In successive addressing operations, which are most common, the least significant address bit is toggling at each operation. If the least

2.3 INTERLEAVING (cont'd)

significant address bit is used to select the memory banks, operations are switched from one bank to the other in each operation. This will increase the data transfer rate since while the first memory bank is still busy from the last operation, the second bank may be started with the next operation. The most significant address bit is wired to the least significant address input. This bit will switch operations between odd and even memory location. All even memory locations of both banks are loaded first, than all odd locations.

Interleaving is specified by 2 wire jumpers in the lower right hand corner of the memory board. The 2 wire jumpers are normally in the NO - NO location. To interleave 2 memory banks the jumpers should be removed and reinstalled in the YES - YES position.

Only 2 16K banks or 32K of memory may be interleaved. Any two banks in a system may be interleaved if the banks are of equal size (16K) and the number of banks is an even number.

2.4 BANK SELECTION

Each memory bank in the PDP-11 system must be specified as to where in the address field the memory is to be located.

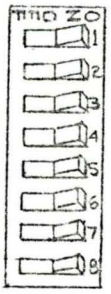
The bank location is specified by an 8 pole switch located in the lower

2.4 BANK SELECTION (cont'd)

right hand side of the printed circuit board. Only one switch should be on at any one time.

The basic PDP-11 computer furnished with a "Memory Management Card" may address up to 128K words of memory or 8 "16K-D" memory banks. Each memory bank must be separately specified as to its location in the address field.

The bank number on the unibus is specified by the 3 most significant address bits, A15L, A16L and A17L. The bank selection does not interfer with interleave which is separately specified.



8 Pole switch	Bank No.	Address Field
	0	0-16K (8-24K)
	1	16-32K (24-40K)
	2	32-48K (40-56K)
	3	48-64K (56-72K)
	4	64-80K (72-88K)
	5	80-96K (88-104K)
	6	96-112K (104-120K)
	7	112-128K (120-128K)

2.5 8K ADDRESS DISPLACEMENT

The Keronix "16K-D" memory may be placed at any 8K starting address. This is specified by the upper switch in the 7 pole switch module. With the first switch "on" the bank address specified by the first switch module is shifted 8K toward the top.

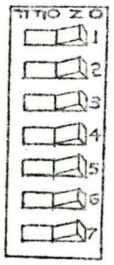
2.6 ADDRESS DISABLE FEATURE

A selectable amount of the uppermost memory locations may be deselected to be used for device register addresses.

2.6 ADDRESS DISABLE FEATURE (cont'd)

A switch module is provided to disable the desired amount of the upper memory. The memory board will not respond to a request if an address falls within the disabled portion of the memory.

Switch Module, 14 pin DIP switch



1	Displace bank address
2	Disable feature select
3	256 Words
4	512 Words
5	1K Words
6	2K Words
7	4K Words

2.7 POWER REQUIREMENT

The power voltages for the Keronix "16K-D" memory system are taken from the PDP-11 bus. No external power supply is required. The power supply pins for +5V, -15V and ground are supplied through the same pins as the DEC MM11-L.

The approximate power requirement of the "16K-D" memory is:

+5V	2.5A	
-15V	3.0A	Active worst case
-15V	.3	Standby

All voltages to be ±5%.

The worst case power was measured in an all zero data pattern with one memory cycle every 1.5 micro seconds.

3.0 SYSTEMS SPECIFICATIONS

Memory capacity	or	16348(16K) 16 bit words 32766(32K) 8 bit bytes
Cycle time		900 - 50ns
Access time		330 - 30ns
Temperature		0°C to 60°C
Humidity		10 to 90%
Dimensions	length	8.87 inch
	width	15.72 inch
	height	.825 inch

4.0 INSTALLATION

Every memory unit leaving the Keronix plant in Santa Monica is thoroughly tested before shipment. Each memory module goes through a minimum of 50 hours of power margining burn-in in a specially designed "exerciser" and 24 hours of computer run-in prior to release.

The memory unit is ready for installation and no problems are anticipated.

Before plugging the memory into the PDP-11 frame check for the following items:

A) Check if memory board was damaged during transit. If obvious damage is evident such as being crushed, punched, or otherwise broken, immediately consult the shipping company and Keronix.

B) Check if proper interleaving is specified.

4.0 INSTALLATION (cont'd)

C) Select the bank number on the selector switch.

D) Select address displacement and address deselection if required.

E) Be sure that power is switched off before plugging the memory board into the PDP-11 chassis.

F) Check the power supply voltages on +5 and -15V. Even though the Keronix memory uses much less power than comparable DEC memory the power supply may be overloaded.

G) Load normal bootstrap and use diagnostic programs to verify memory operations, before attempting to load the main programs.

If any problem develops please contact Keronix Inc. in Santa Monica, California.

4.1 PDP 11/05 OR PDP 11/10 INSTALLATIONS

This type of computer contains only 9 card slots. The maximum memory capacity is 32K.

The PDP 11/05 and the PDP 11/10 are available in 8K DEC versions. The PDP 11/05 is also available in a 16K DEC version. Both versions have different backpanel wirings. See Figure 5 for proper slot selection.

4.1.1 8K VERSION OF PDP 11/05 or PDP 11/10 EXPANSION TO 24K

This computer contains already an 8K DEC MM11-L memory. The memory on the computer may be expanded to 24K by the addition of a Keronix "16K-D" memory board. In order to specify the Keronix memory to start at 8K the "Displacement" wire jumper must be inserted. Alternately the DEC memory may be moved to the end of the memory field. The Keronix memory board is inserted into slot 3. See Fig. 5-A.

4.1.2 8K VERSION OF PDP 11/05 OR PDP 11/10 WITH 16K OR 32K MEMORY

This computer would contain only Keronix memory boards. The total memory capacity may be 32K with 2 memory boards or 16K with only one board. The Keronix memory boards are plugged into Slot 4 and 6. See Fig. 5-B. A portion of the upper memory may have to be deselected to allow for device register addresses.

4.1.3 16K PDP 11/05 VERSION WITH 16K or 32K MEMORY

This kind of computer may be expanded up to 32K of memory capacity by the addition of 2 Keronix "16K-D" memory banks. Note the 3 peripheral slots which become available through the smaller Keronix memory banks. The Keronix memory boards are plugged into slot 4 and 6. See Fig. 5-C. If the computer already contains a DEC MM11-L memory the Keronix memory module may be plugged into slot 3. The total memory capacity would increase to 24K.

4.2 PDP 11/40 and PDP 11/45 INSTALLATION

The Keronix "16K-D" memory may be used to replace the DEC MM11-L memory. This would increase the memory capacity by 8K. The Keronix Memory is installed in slot 2.

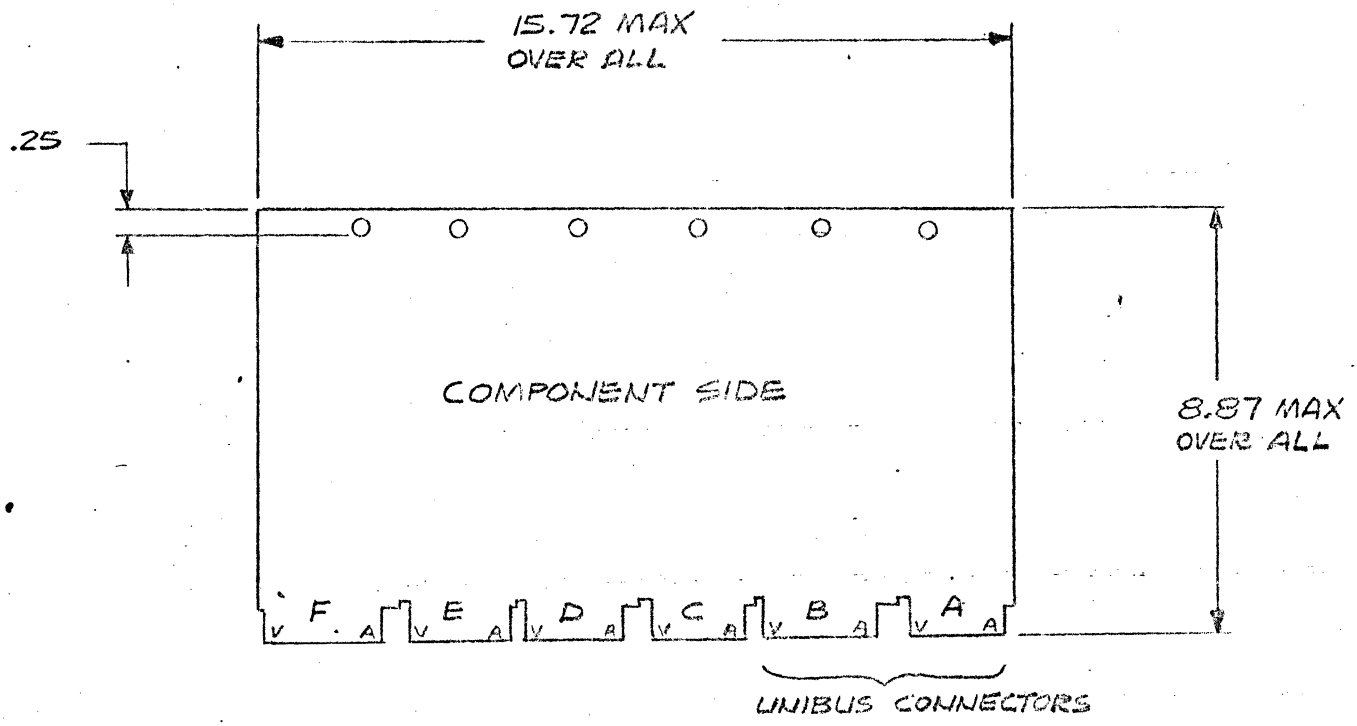
Alternately the Keronix "16K-D" memory may be plugged into any "small peripheral unit."

The slot immediately behind the memory must be empty except for connector A B and D. The Keronix memory is wired to provide bus grant continuity.

A bus grant continuity card must be inserted in connector D if the slot is unused. (See page 20).

Note: If grant continuity card (G 727) is used directly below the 16K x 16 D Memory, it must be cut to a maximum length of 1.1.

FIG 1 BOARD DIMENSIONS



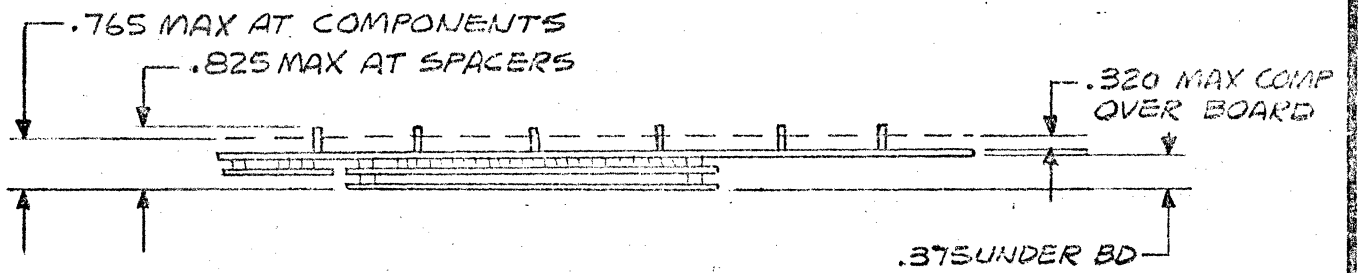
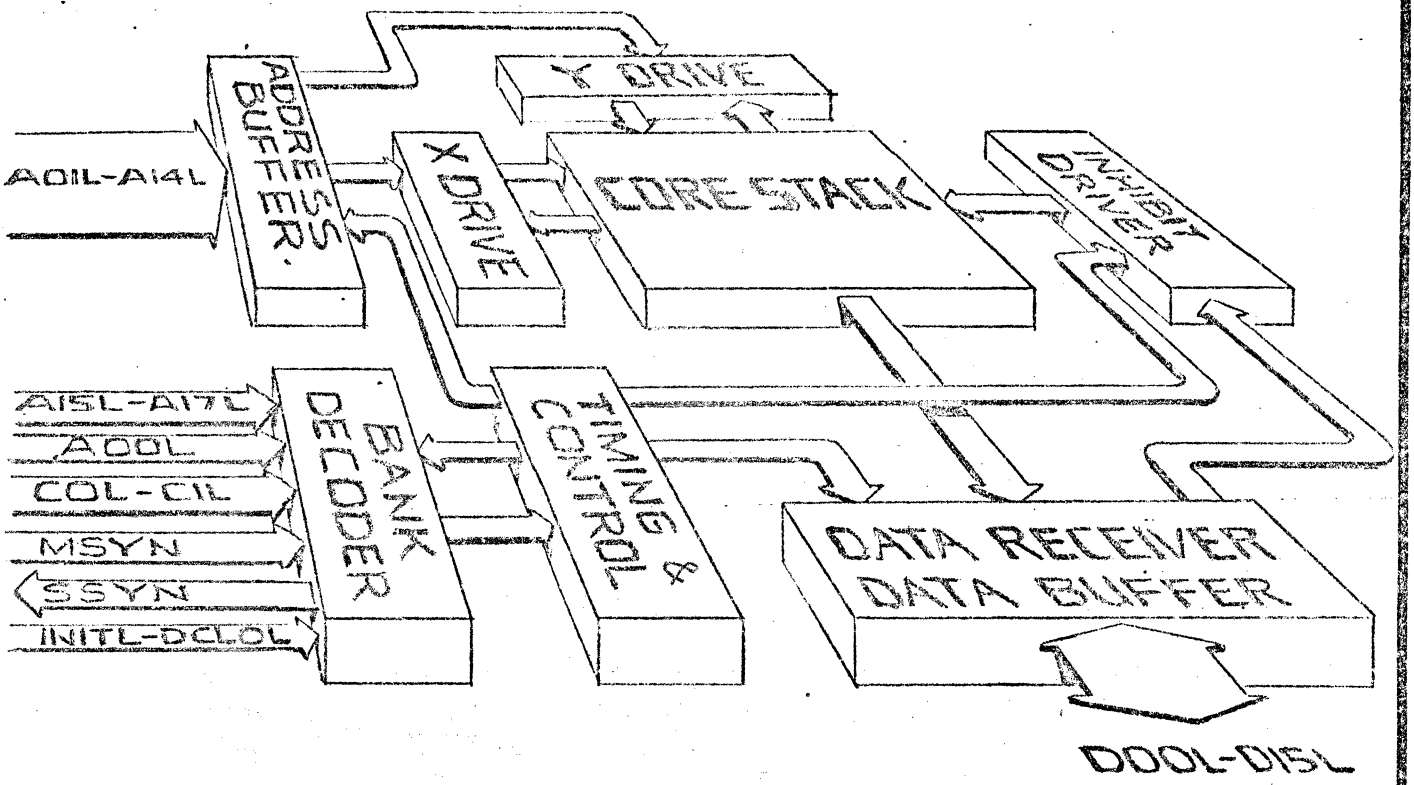


FIG. 2 BLOCK DIAGRAM



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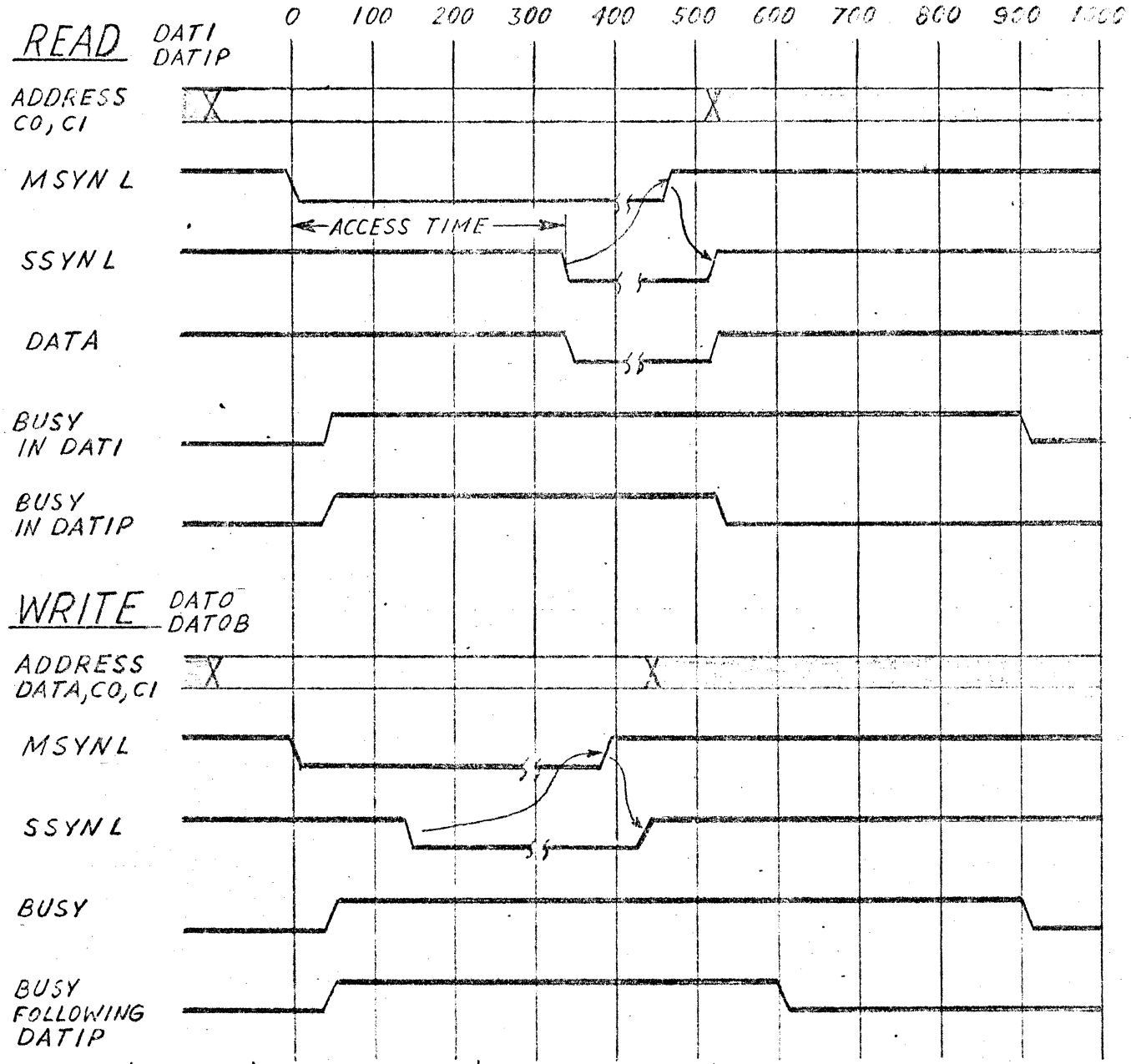
SANTA MONICA, CA. 90404

FIG. 3

TIMING DIAGRAM



COL	CIL	AOOL	OPERATION	
LOW	LOW	X	DATI	READ/RESTORE
HIGH	LOW	X	DATIP	READ AND PAUSE
LOW	HIGH	X	DATO	CLEAR/WRITE
HIGH	HIGH	LOW	DATOB	WRITE BYTE (BIT 15-08)
HIGH	HIGH	HIGH	DATOB	WRITE BYTE (BIT 07-00)

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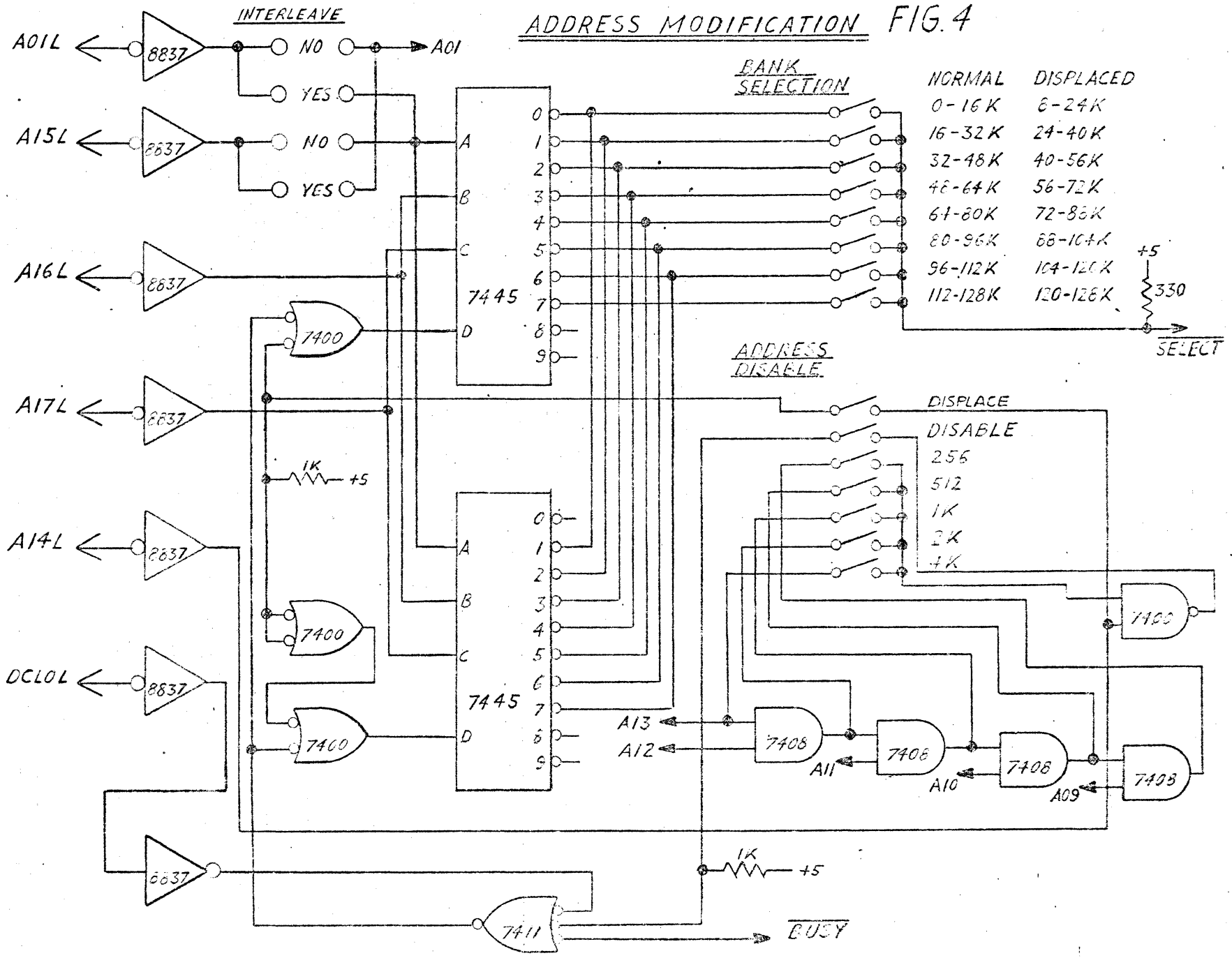
ADDRESS MODIFICATION FIG. 4



8K VERSION OF PDP 11/05 OR PDP 11/10 EXPANSION TO 24K

FIG5-A

	A	B	C	D	E	F
1	COMM.		PERIPHERAL			
2	MAINT.	MAINT.	PERIPHERAL			
3	KERONIX 16K-D					
4	UNIBUS TERM.		BUS GRANT			
5	UNIBUS TERM.		MEMORY STACK			
6	MEMORY DRIVER					
7	MEMORY CONTROL					
8	PROCESSOR					
9	PROCESSOR					

8K DEC MMII-L

8K VERSION OF PDP 11/05 OR PDP 11/10 WITH 16K OR 32K MEMORY

FIG5-B

	A	B	C	D	E	F
1	COMM.		PERIPHERAL			
2	MAINT.	MAINT.	PERIPHERAL			
3	UNIBUS TERM.		PERIPHERAL			
4	KERONIX 16K-D					
5	UNIBUS TERM.		BUS GRANT			
6	KERONIX 16K-D					
7			BUS GRANT			
8	PROCESSOR					
9	PROCESSOR					

16K POP 11/05 VERSION WITH 16K OR 32K KERONIX MEMORY

FIG5-C

	A	B	C	D	E	F
1	MAINT.	MAINT.	PERIPHERAL			
2	UNIBUS TERM.		PERIPHERAL			
3			PERIPHERAL			
4	KERONIX 16K-D					
5	UNIBUS TERM.		BUS GRANT			
6	KERONIX 16K-D					
7			BUS GRANT			
8	PROCESSOR					
9	PROCESSOR					

PDP-11/05

KERONIX

"D" MEMORY SYSTEM

Reference & Installation

Manual

January, 1974

KERONIX, INC.
(213) 829-3594
1752 CLOVERFIELD BLVD
SANTA MONICA, CA. 90404

ERRATA

On Sheets 10 and 11, Figures 3 and 4, it must be mentioned that where ever a "blank" slot is indicated that a grant continuity card G727 be inserted in Slot D.

1.0 INTRODUCTION

This manual relates the physical description, technical information and installation procedure for the D Memory System manufactured by KERONIX, INC. of Santa Monica, California. This memory is compatible with, and a replacement for, the DEC MM11-L core memory used in the DEC 11/05, 11/10, 11/40 and 11/45 systems and the ME11-L memory expansion box.

2.0 SYSTEM SPECIFICATIONS

2.1 Capacity

The capacity of the D memory is 8192 words by 16 bits. 18 bits is available as an option.

8192 word modules can be configured up to 131072 words of storage.

2.2 Cycle Time

The cycle time of the D memory is 850 ns. The time of 850 ns is for an uninterrupted Read/Write cycle. That is, DATI, DATO/B (not following a DATIP). The cycle time for a DATIP is 450 ns. The cycle time for a DATO/B (following a DATIP) is 450 nsec. For a DATO/B operation SSYN is returned 100 ns after MSYN. See Figure 1 for timing.

2.3 Access Time

Access time for the memory is 300 nsec. This time is measured from the leading edge of MSYN to the leading edge of SSYN at the memory connector (Figure 1).

2.4 Addressing

The D system is capable of decoding a memory address of 18 bits. The lowest order address bit is for byte control. 17 bits are for word and module selection; access to one of 131072 words.

A00L - Lowest order memory address bit. Used for byte control (upper or lower half of word).

A01L-A13L - Next 13 bits used to select one of 8192 words.

A14L-A17L - Last 4 bits used to select one of 16 memory modules (banks).

There are two selectable features concerned with memory addressing: paging and interleaving.

2.4.1 Paging

Paging is selecting which bank (8K module) of a memory system a specific memory is to be. It can be addressed as any one of 16 banks. Once it has been decided, it is only necessary to insert the proper jumpers in the paging plug. Logical selection of a memory is determined by the memory by comparing the upper 4 bits of the memory address with the jumper placement on the paging plug. See Figure 2.

2.4.2 Interleaving

Interleaving is a method of increasing data transfer rates between memory and an I/O device. It could be employed in conjunction with a high speed device such as a fixed head disc.

The idea behind interleaving is that while one memory module of a system is storing a data word another module can be started before the former is finished. Interleaving can only be done between physical modules, not within a module.

A method of interleaving is accomplished by exchanging, in two memories, two bits of the memory address. The bits involved are the least significant word selection bit, A01, and the least significant module selection bit, A14. As a result when the memory address is incremented (or decremented) and placed on the bus the memories see not the word selection being incremented, but the module selection bits (paged address) being toggled between two memory banks. Therefore, contiguous data words are alternately stored in two banks of memory. It is very important to note that only modules that have a single bit difference in the paged address can be interleaved. See Table 1.

The method of interleaving the KERONIX D memory is identical to that of the DEC MM11-L. It is done by jumper placement. See Figure 2.

The D memory is properly jumpered for interleaving by removing the jumpers in NO and placing jumpers in YES (2 jumpers in NO to 2 jumpers in YES between IC99 and IC100).

It is possible to interleave a KERONIX D with a DEC MM11-L.

2.5 Modes of Operation

The memory operation to be performed is determined at the leading edge of MSYNC by the states of bus lines COL, C1L and A00L.

COL	CIL	A00L	
0	0	0	DATOB (output bits 15-8)
0	0	1	DATOB (output bits 7-0)
0	1	0	DATIP
0	1	1	DATIP
1	0	0	DATO (output bits 15-0)
1	0	1	DATO (output bits 15-0)
1	1	0	DATI
1	1	1	DATI

2.6 Interface

2.6.1 The interface circuitry of the KERONIX D memory corresponds to the DEC Unibus receiver and transmitter characteristics.

2.6.2 Operation is in accord with the DEC Unibus philosophy of the master-slave relationship.

2.6.3 Memory Input/Output signals are as defined for the Unibus.

2.6.4 Bus Grant continuity is provided on the memory by jumpering DK2 to DL2, DM2 to DN2, DP2 to DR2 and DS2 to DT2.

2.7 Voltage-Current Requirements

	Standby	Zeroes	Ones
+5v	1.35a	1.35a	1.35a
-15v	.34a	3.2a*	.9a*

All voltages $\pm$5%

*Values are averaged over 850 ns cycle time.

The power pins of the D memory are compatible with the Unibus power pin assignments.

2.8 Operating Environment

The D memory is operable from 0°C to 60°C with 0 to 90% relative humidity.

3.0 PHYSICAL DESCRIPTION

The D Memory System is designed to fit into the DEC PDP 11/05, 11/10, 11/40 and 11/45 systems and the MEll-L memory expansion box. A single board replaces the 3 board arrangement of the MMll-L memory. It is not compatible with the BAll-ES expander box.

The core stack is a single planar array mounted on a DEC-compatible size hex printed circuit board. When the D memory is plugged into a DEC system it will occupy two slot positions. This is due to the height of the core array which is mounted on the back of the memory electronics board.

The dimensions of the D system are

8.85 in.(L) X 15.70 in. (W) X 0.8 in. (H)
= 111.2 cu. in.

4.0 INSTALLATION

PDP-11/05

The 11/05 is specified for the OEM market. There are two versions of the standard 11/05, 8K of DEC memory or 16K of DEC memory in the mainframe. See Figure 3.

For the 8K version a KERONIX D memory can be used in place of the DEC memory by plugging it into slot 6 (Figure 3). It is, also possible to add another 8K of memory to this version by inserting a D memory in slot 4. This arrangement leaves slots 1, 2 and 3 available for peripheral controllers. Slots 7 and 5 (except for the M930 terminator) must be left vacant due to the stack underhang. M930 terminators are plugged into A5-B5 and A3-B3.

The 16K DEC version can accommodate 24K of KERONIX memory. A D memory, replacing the DEC system, can be placed in slots 4 and 2. M930 terminators are placed in A5-B5 and A3-B3. Slot 1 is for a peripheral controller.

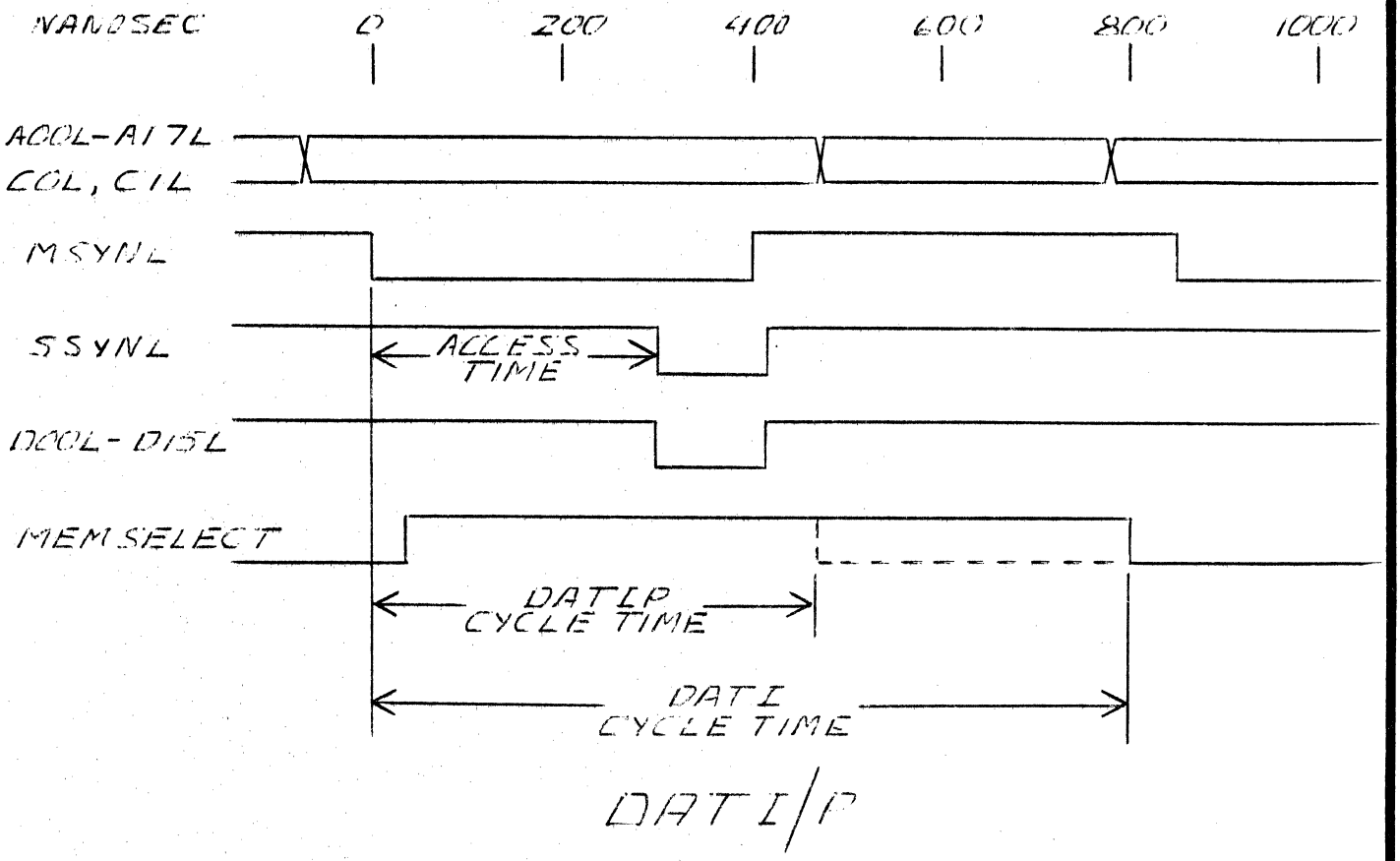
Configurations of KERONIX and DEC memories are shown in Figure 4.

PDP-11/10

The 11/10 is an end user directed system and is available with a maximum of 8K words in the mainframe. The placement of D memory is the same as for the 8K version of the 11/05.

PDP-11/40 and 11/45

In these systems the D memory can replace the DEC MM11-L memory by placing it in slot 2 of the memory system unit. The D can, also, be plugged into a small peripheral system unit in the 40 and 45 systems. It is necessary that the slot immediately behind the D memory be vacant in connectors C,D,E and F to accommodate the stack overhang. The D provides Bus Grant continuity and requires only the Unibus signals at connectors A and B and system unit power distribution.


NANOSEC
0
200
400
600
800
1000
AOOL-A17L
COL, C1L
MSYNL
SSYNL
ACCESS TIME
DOOL-D15L
MEMSELECT
DATIP CYCLE TIME
DATI CYCLE TIME
DATI/P

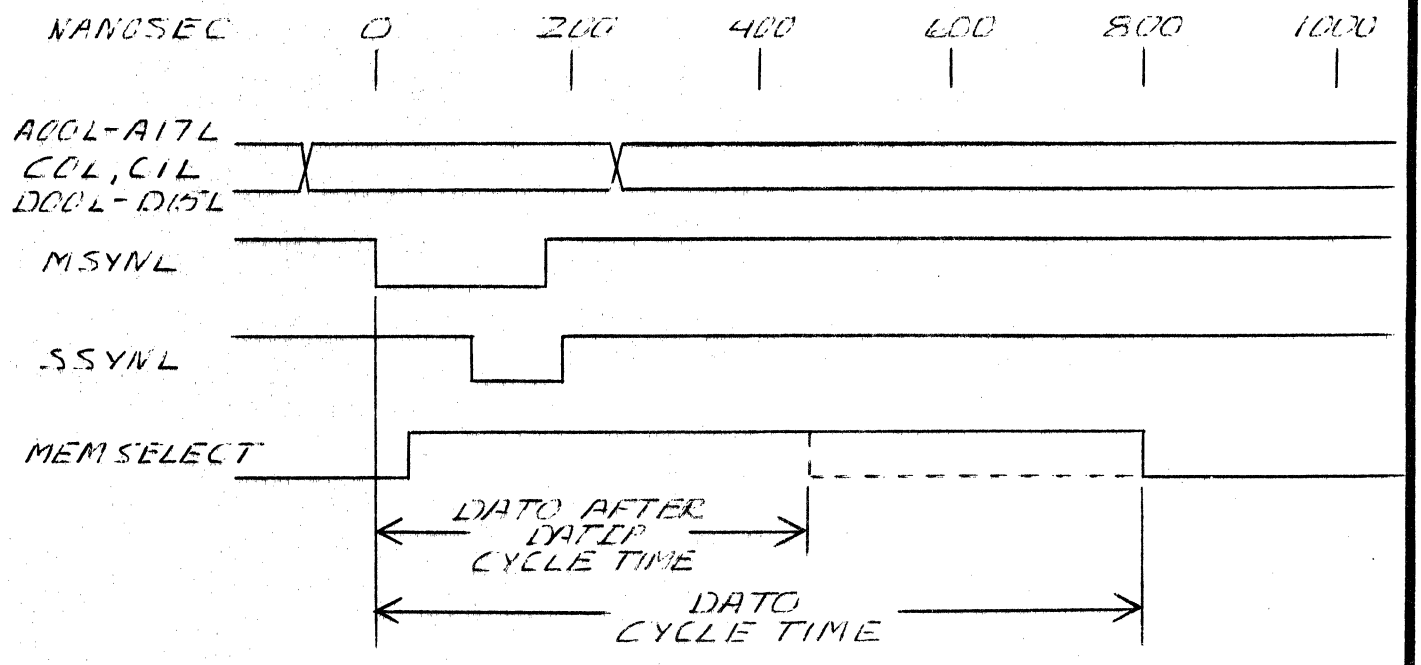
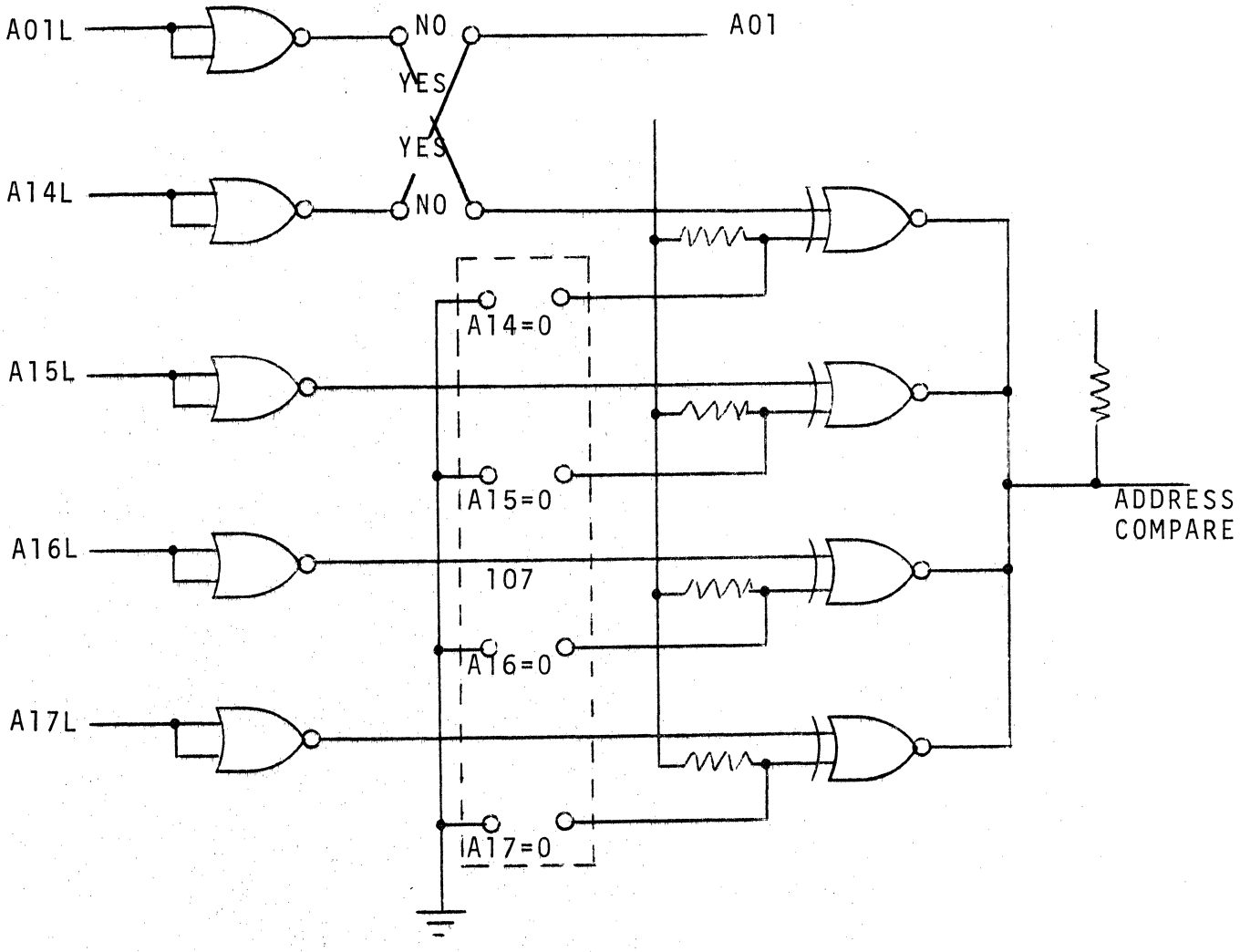

NANOSEC
0
200
400
600
800
1000
AOOL-A17L
COL, C1L
DOOL-D15L
MSYNL
SSYNL
MEMSELECT
DATO AFTER DATIP CYCLE TIME
DATO CYCLE TIME
DATO

FIGURE 1



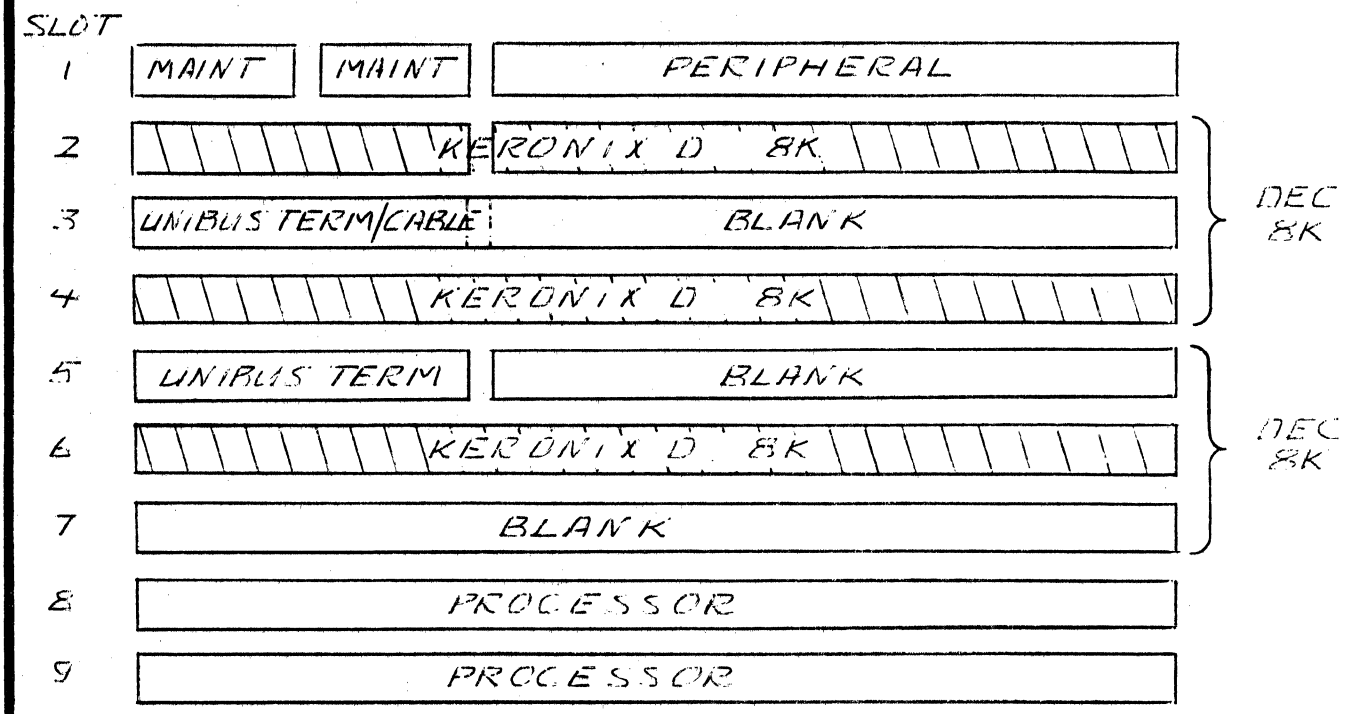
8K PAGING AND INTERLEAVING JUMPER PLACEMENT

FIGURE 2

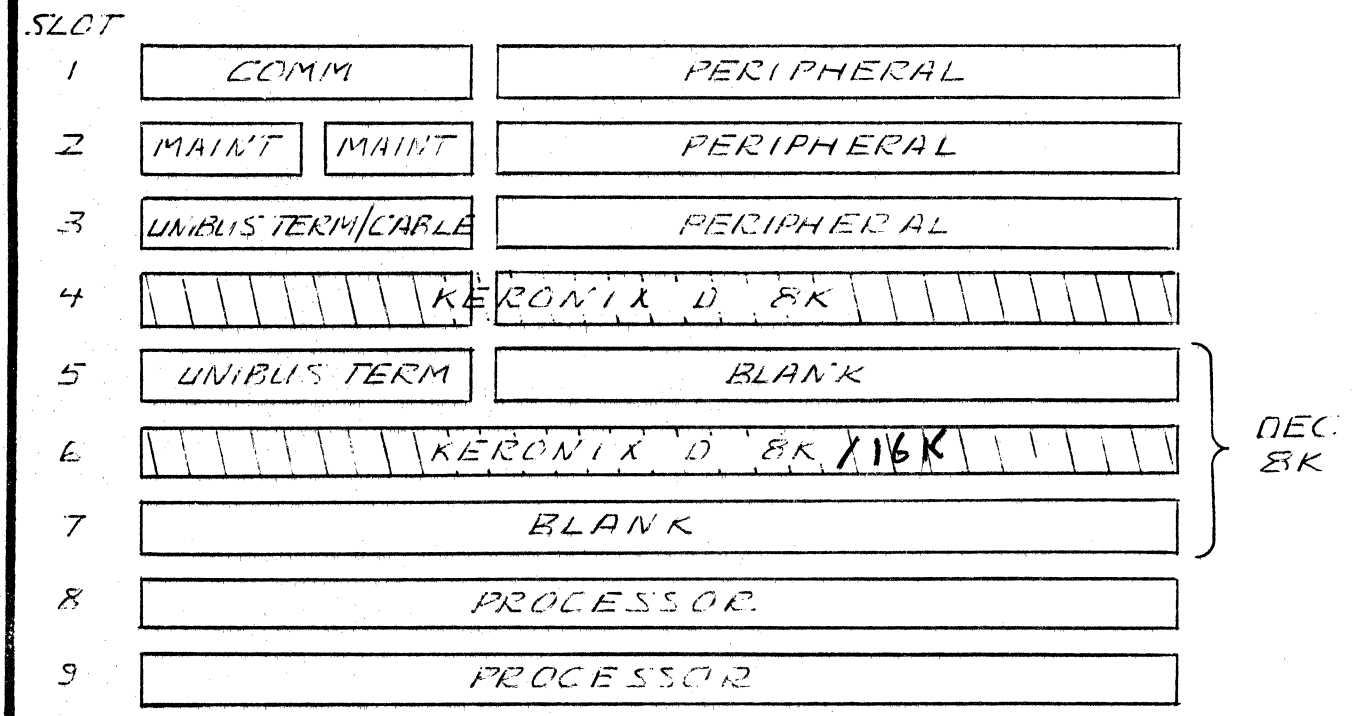
	Module X				Module Y				Interleave
Address Bits	17	16	15	14	17	16	15	14	
Paged 0 & 1	0	0	0	0	0	0	0	1	YES
Paged 2 & 3	0	0	1	0	0	0	1	1	YES
Paged E & F	1	1	1	0	1	1	1	1	YES
Paged 1 & 2	0	0	0	1	0	0	1	0	NO
Paged 4 & 6	0	1	0	0	0	1	1	0	YES
Paged 7 & F	0	1	1	1	1	1	1	1	YES

Examples of some paged addresses and the ability to interleave

TABLE 1

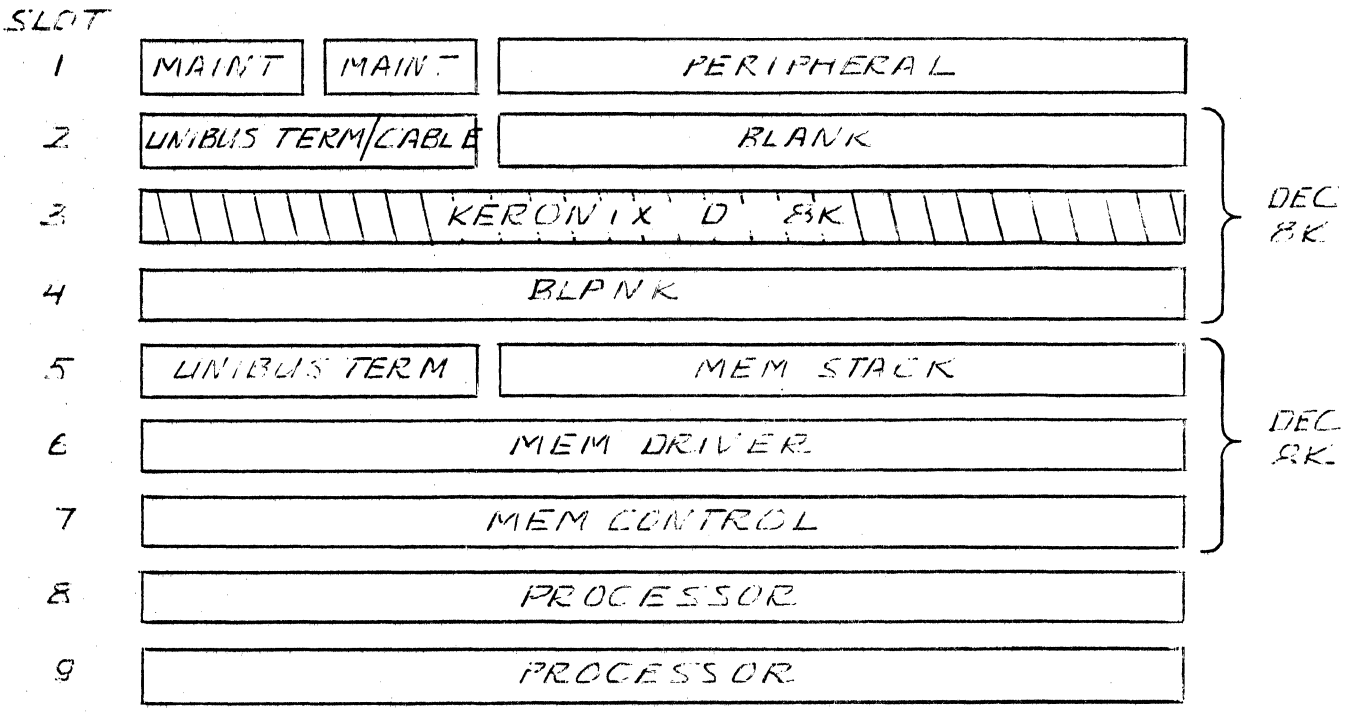


16K DEC CONFIGURATION WITH 24K KERONIX MEMORY

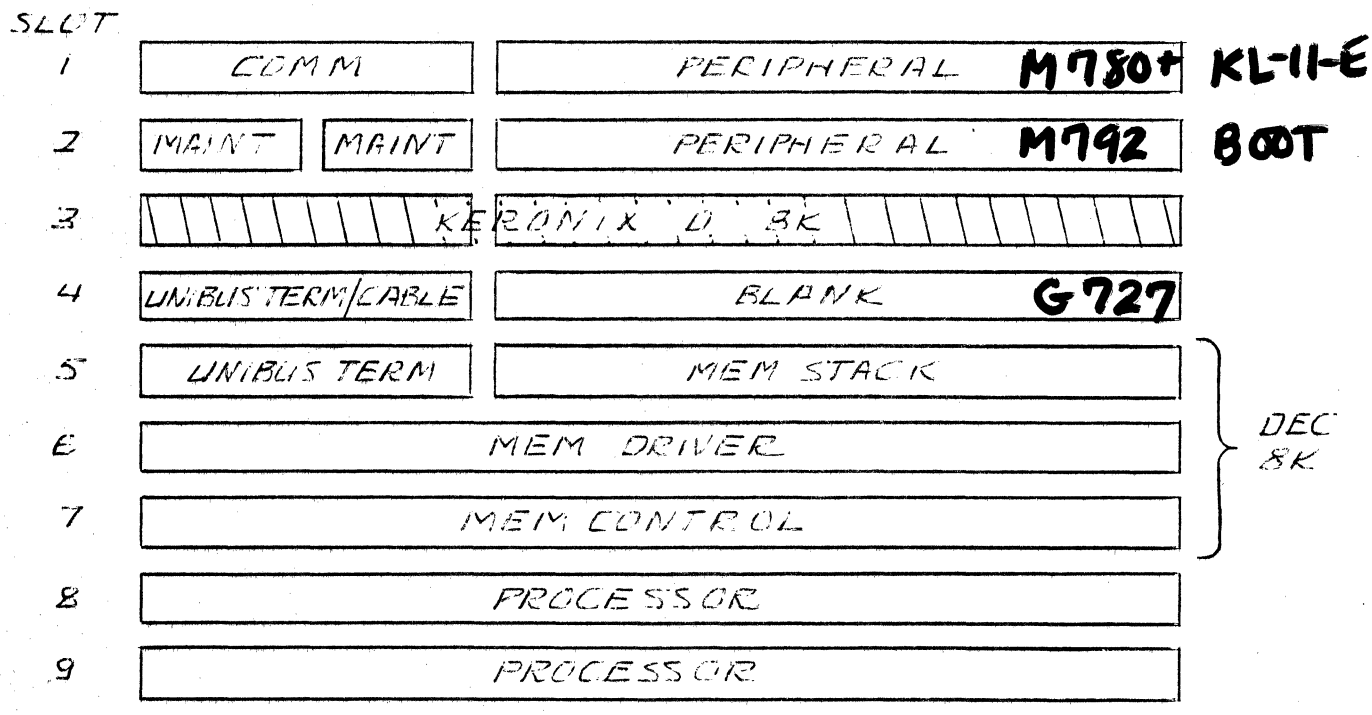


8K DEC CONFIGURATION WITH 16K KERONIX MEMORY

— FIGURE 3 —



16K DEC CONFIGURATION WITH 8K DEC AND 8K KERONIX



8K DEC CONFIGURATION WITH 8K DEC AND 8K KERONIX

— FIGURE 4 —

PAGE SELECTION INSTRUCTIONS FOR

KERONIX 8/4K X 16/18 "D" MEMORIES

8K SYSTEMS	DEVICE ADDRESS JUMPERS				
	A17-0	A16-0	A15-0	A14-0	A13-0
0-8K	IN	IN	IN	IN	N/A
8-16K	IN	IN	IN	OUT	"
16-24K	IN	IN	OUT	IN	"
24-32K	IN	IN	OUT	OUT	"
32-40K	IN	OUT	IN	IN	"
40-48K	IN	OUT	IN	OUT	"
48-56K	IN	OUT	OUT	IN	"
56-65K	IN	OUT	OUT	OUT	"
65-73K	OUT	IN	IN	IN	"
⋮					

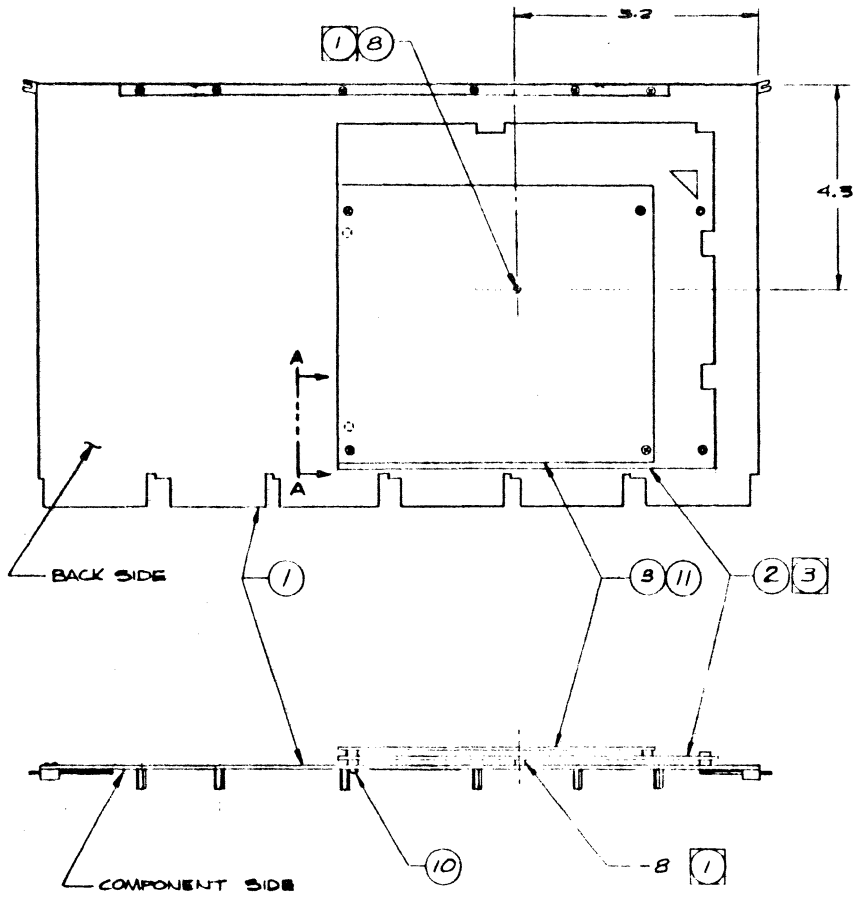
AND SO ON

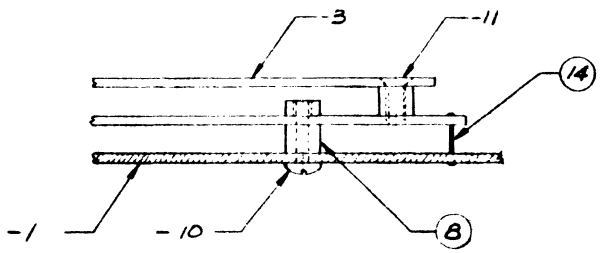
4K SYSTEMS	A17-0	A16-0	A15-0	A14-0	A13-0
0-4K	IN	IN	IN	IN	IN
4-8K	IN	IN	IN	IN	OUT
8-12K	IN	IN	IN	OUT	IN
12-16K	IN	IN	IN	OUT	OUT
16-20K	IN	IN	OUT	IN	IN
20-24K	IN	IN	OUT	IN	OUT
24-28K	IN	IN	OUT	OUT	IN
28-32K	IN	IN	OUT	OUT	OUT
32-36K	IN	OUT	IN	IN	IN
36-40K	IN	OUT	IN	IN	OUT
40-44K	IN	OUT	IN	OUT	IN
44-48K	IN	OUT	IN	OUT	OUT
48-52K	IN	OUT	OUT	IN	IN
⋮					

AND SO ON

TO INTERLEAVE A DEVICE WITH ANOTHER DEVICE OF SAME SIZE, REMOVE TWO JUMPERS MARKED NO AND INSTALL TWO JUMPERS MARKED YES.

LTR	DESCRIPTION	DATE	APP
A	ADDED NOTE 3	10/27/73	[illegible]
B	ITEM 5 (PAD, FOAM) HAS BEEN REMOVED, AND NOTE 2 DELETED. RETROFIT.	11/14/73	





SECTION "A-A"
SCALE: NONE

ITEM	QTY	PART NO	DESCRIPTION	R D.	MFR
17					
16					
15					
14	A/R		WIRE, BUSS, 24 AWG		
13					
12					
11	4		SCREW, 4-40 x 1/4, FLAT HD PHILIPS, STL, CAD PL		
10	4		SCREW, 4-40 x 5/16, PAN HD PHILIPS, STL, CAD PL		
9					
8	6	8880	SPACER, UNTHREADED, 1/8 I.D. x 1/4 O.D. x 1/8 LONG		AS SHOWN
7					
6					
5					
4					
3	1	816757	COVER, CORE PLATE		XEROX
[3] 2	1	816750	CORE BOARD ASSY (4 MIC) 16		XEROX
1	1	8801	ELECTRONIC BOARD ASSY		XEROX

[3] SEE SUPPLEMENT DWG 818012 WHEN USING CORE B 816751 OR 816751A

[1] BOND FIBRE SPACER (ITEM 8) TO BOARD (ITEM 1) WITH EPON RESIN 828 AND CURING AGENT U OR EQUIV.

NOTES: UNLESS OTHERWISE SPECIFIED

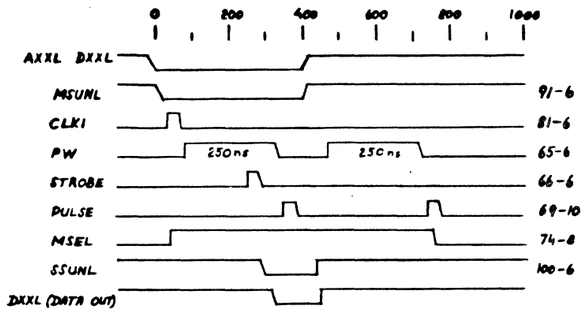
XERONIX, INC.

SCALE: 1/2	APPROVED BY:	DRAWN BY: LEWACK
DATE: 10/5/73		REVISED 11-14-73

TOP ASSEMBLY

STATUS: INITIAL	USED ON: 8K x 16D	SHEET 1 of 1	DRAWING NUMBER 8900 B

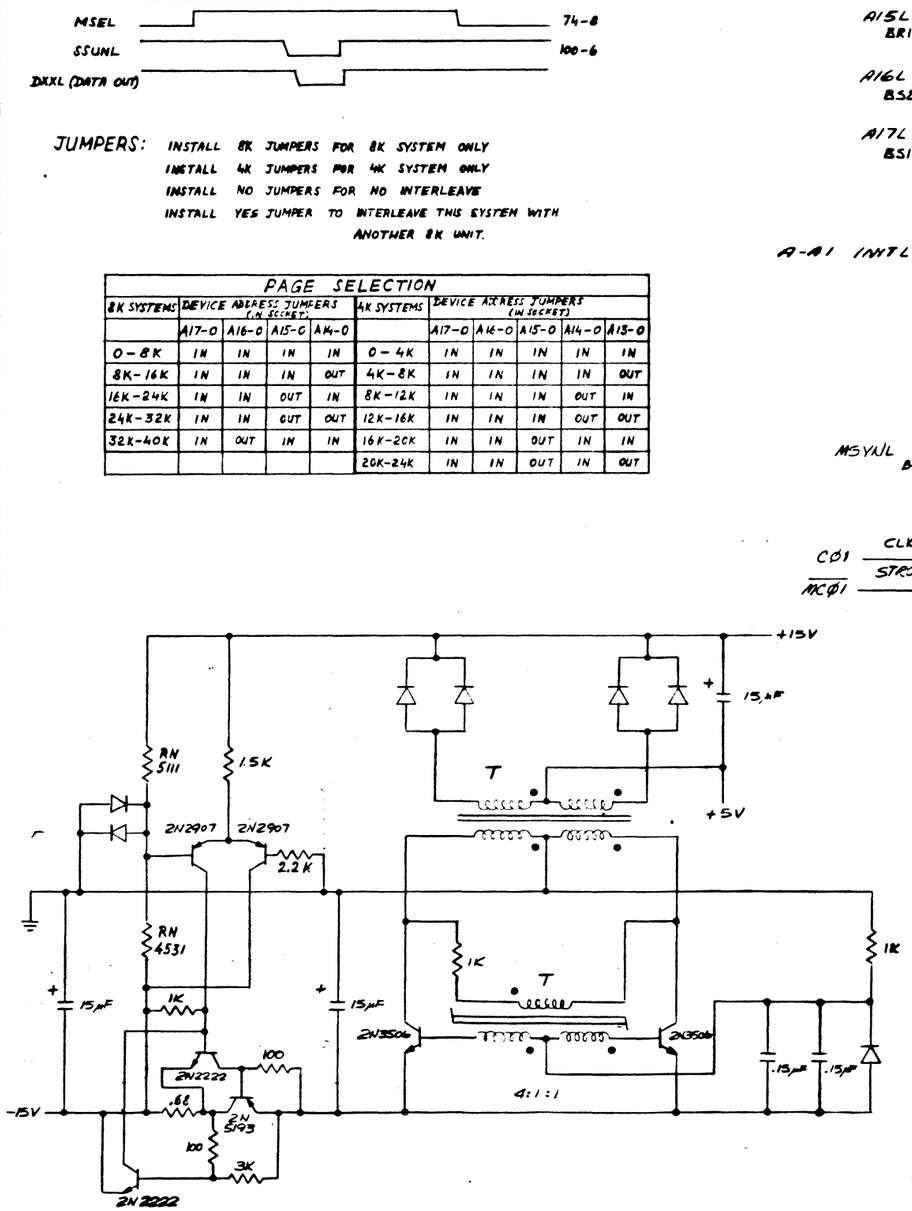
LTR	DESCRIPTION	DATE	APP
A	CIRCUITRY CHANGE	9/27/73	

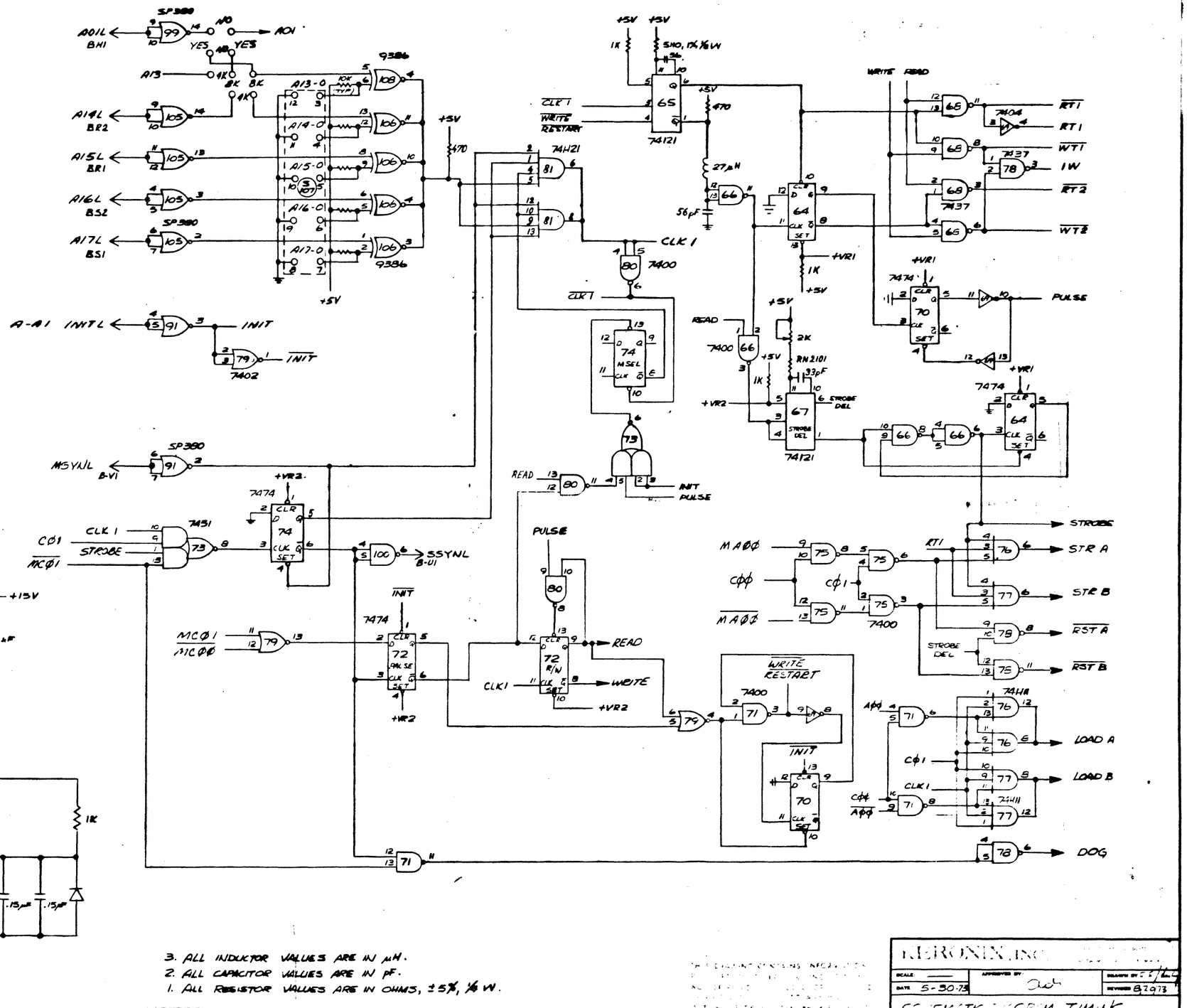


JUMPERS:
- INSTALL 8K JUMPERS FOR 8K SYSTEM ONLY
- INSTALL 4K JUMPERS FOR 4K SYSTEM ONLY
- INSTALL NO JUMPERS FOR NO INTERLEAVE
- INSTALL YES JUMPER TO INTERLEAVE THIS SYSTEM WITH ANOTHER 8K UNIT.

PAGE SELECTION

8K SYSTEMS	DEVICE ADDRESS JUMPERS (IN SOCKET)				4K SYSTEMS	DEVICE ADDRESS JUMPERS (IN SOCKET)				
	A17-0	A16-0	A15-0	A14-0		A17-0	A16-0	A15-0	A14-0	A13-0
0-8K	IN	IN	IN	IN	0-4K	IN	IN	IN	IN	IN
8K-16K	IN	IN	IN	OUT	4K-8K	IN	IN	IN	IN	OUT
16K-24K	IN	IN	OUT	IN	8K-12K	IN	IN	IN	OUT	IN
24K-32K	IN	IN	OUT	OUT	12K-16K	IN	IN	IN	OUT	OUT
32K-40K	IN	OUT	IN	IN	16K-20K	IN	IN	OUT	IN	IN
					20K-24K	IN	IN	OUT	IN	OUT

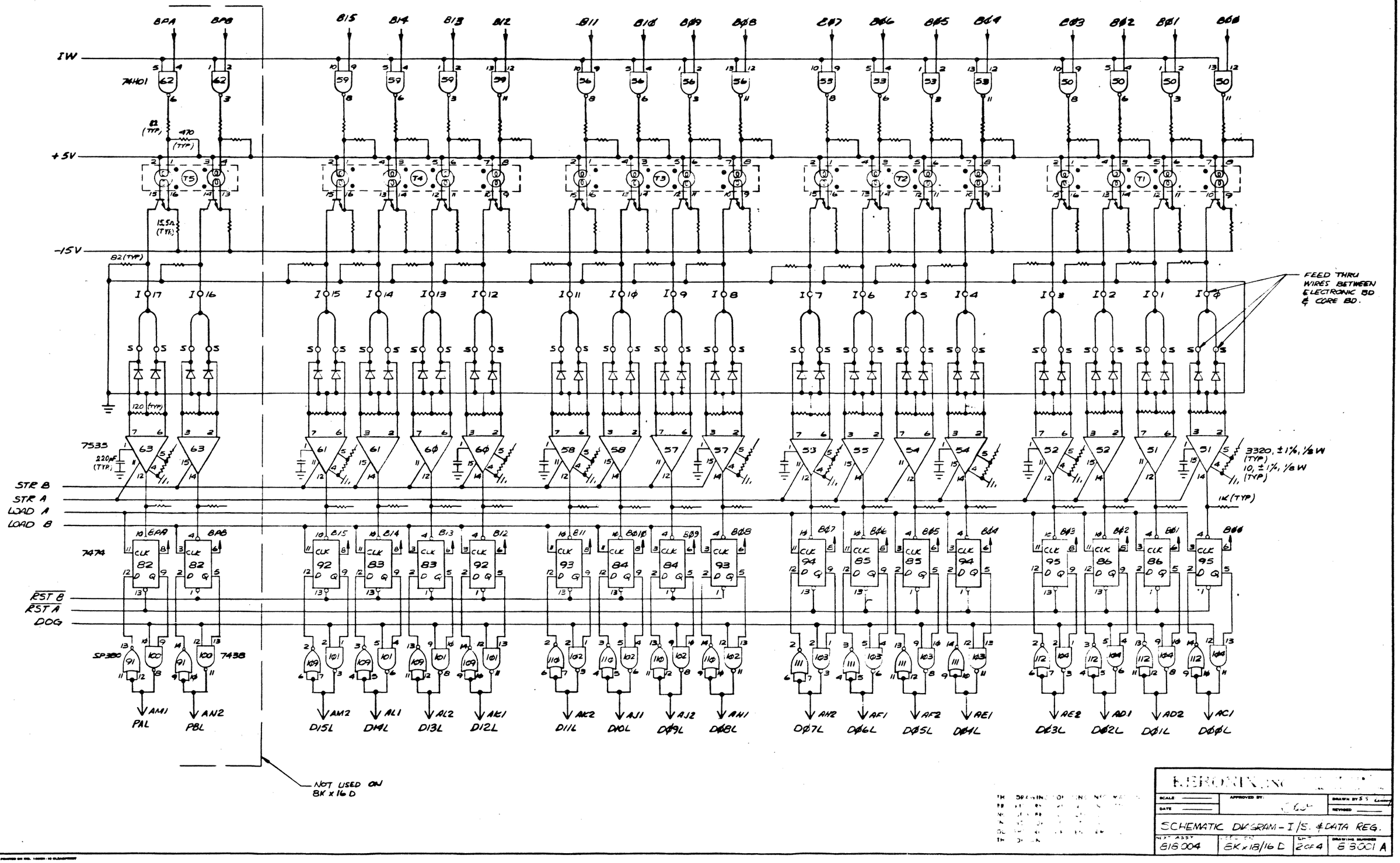




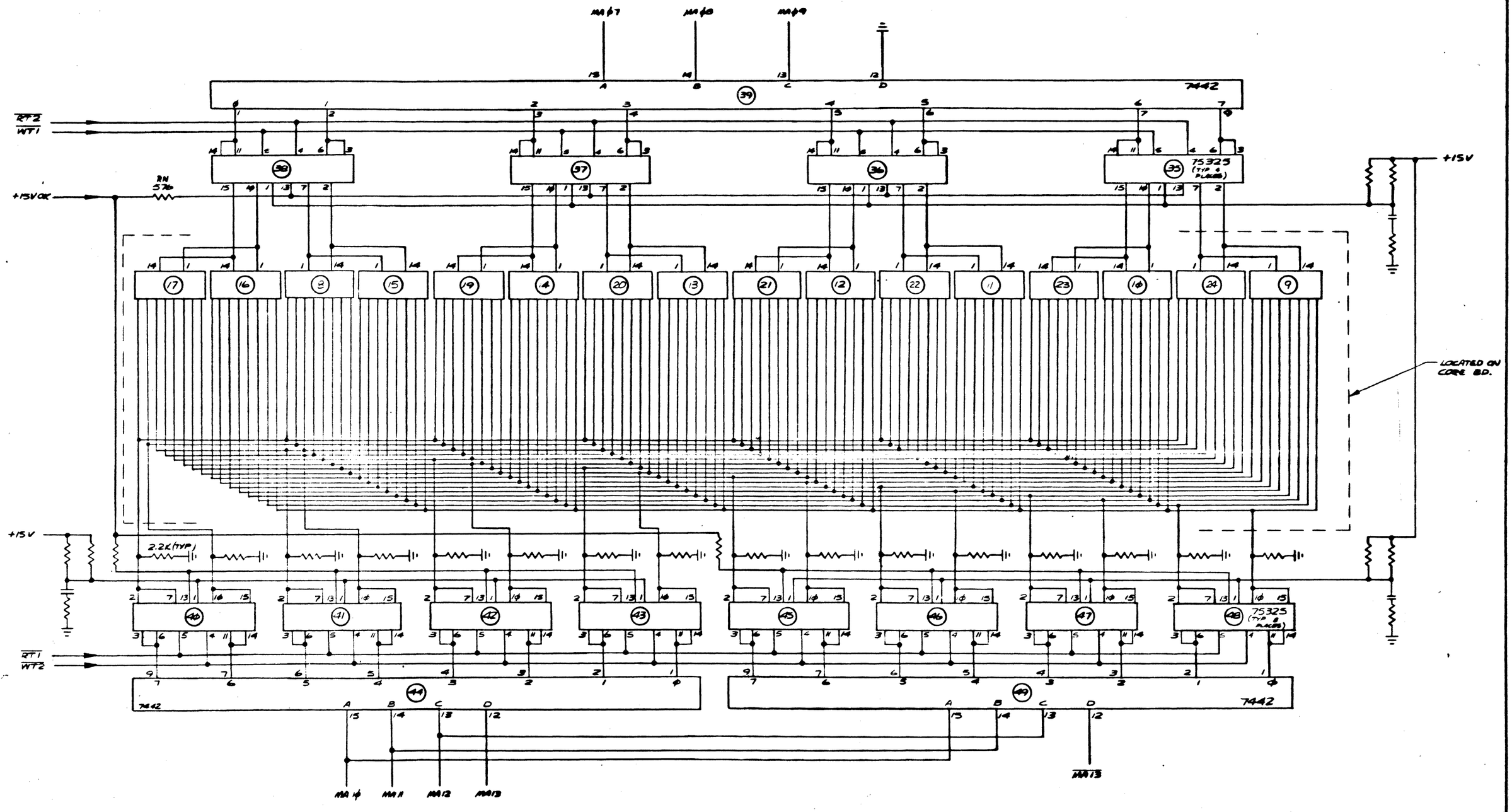
3. ALL INDUCTOR VALUES ARE IN µH.
2. ALL CAPACITOR VALUES ARE IN pF.
1. ALL RESISTOR VALUES ARE IN OHMS, ±5%, ½ W.

NOTES: UNLESS OTHERWISE SPECIFIED.

NERONIX, INC			
SCALE	APPROVED BY	DRAWN BY	
DATE 5-30-75		REVISED 8/29/73	
SCHEMATIC DIAGRAM-TIMING			
NEXT ASSY 818004	USED ON FM-5160D	SHT 1 OF 4	DRAWING NUMBER 818001 A



SCALE	APPROVED BY:	DRAWN BY S.S.	
DATE		REVISED	
SCHEMATIC DK SRAM - I/S. & DATA REG.			
NEXT ASSY 816004	USED ON 8K x 18/16 D	SHT 2 OF 4	DRAWING NUMBER 83001 A



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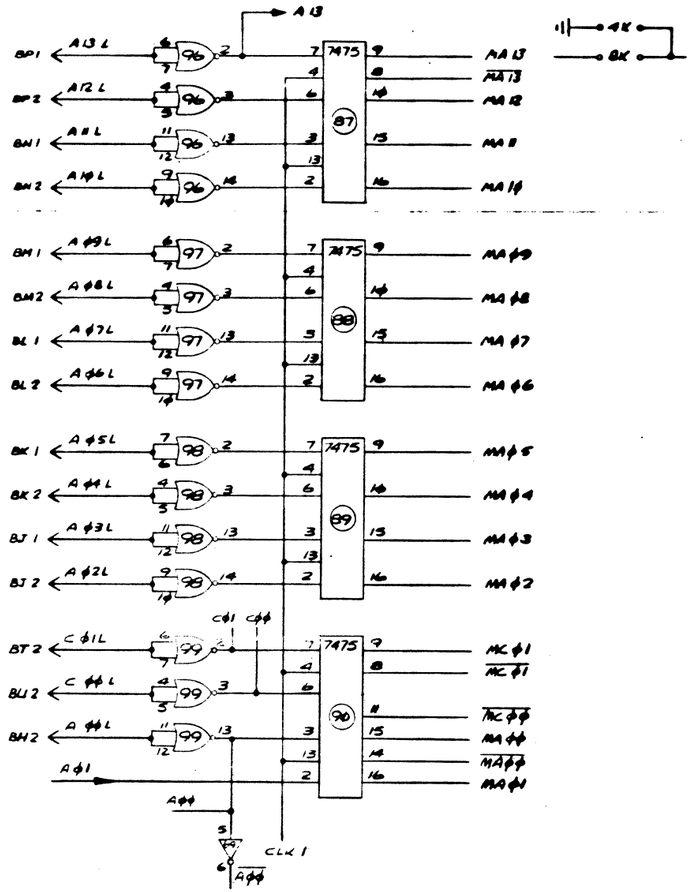
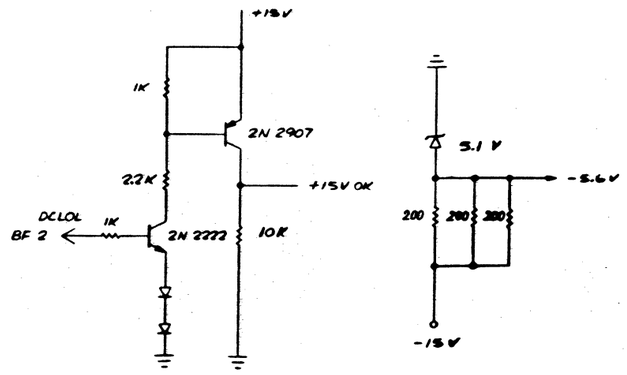
KERONIX, INC.

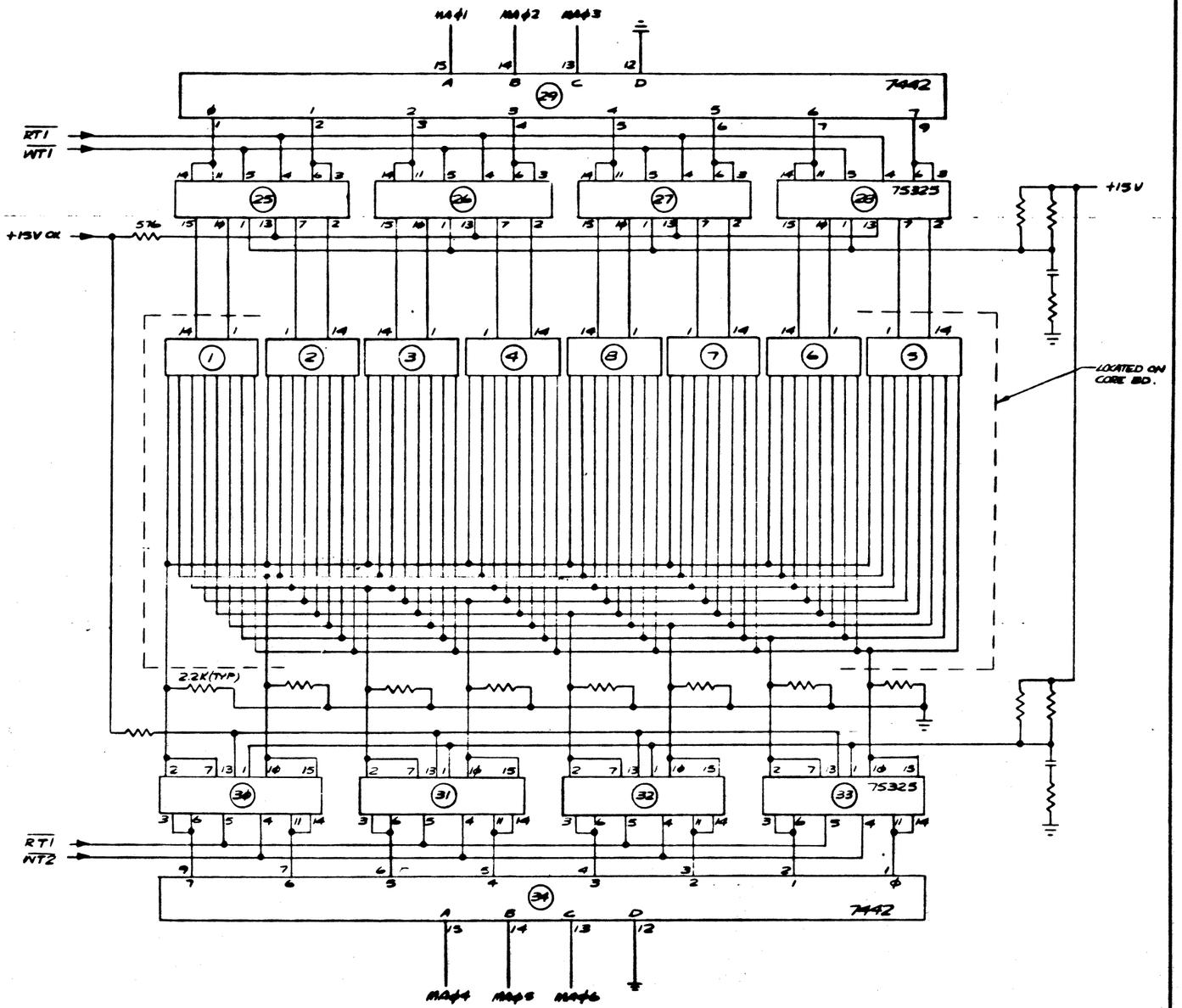
SCHEMATIC DIAGRAM – X DRIVE

SCALE	APPROVED BY	DRAWN BY
DATE		REVISED

ASSY	USED ON	SHT	DRAWING NUMBER
818004	8K x 18/16 D	3 of 4	818001 A







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KERONIX, INC.
1710 CLOVERFIELD BLVD.
SANTA MONICA CALIF. 90404

SCALE —
DATE —
APPROVED BY
DRAWN BY
REVISED

SCHEMATIC DIAGRAM - Y DRIVE

NEXT ASSY	USED ON	SHT	DRAWING NUMBER
818004	8K x 18/16 D	4 OF 4	818001 A