# Operation and Maintenance Manual

KENNEDY
A Division of Shugart Corporation

## Data Streamer™

# Model 6809

# Emulates IBM 8809

## FCC CERTIFIED COMPUTER EQUIPMENT

This equipment, freestanding with shielded Data and Control Cables, complies with Part 15, Subpart J of FCC Rules Governing Class A Computing Devices Operated In A Commercial Environment. However, the equipment generates radio frequency energy and, when operated in a residential area, the user must take adequate precautions against interference to radio communications.

# SECTION I
# APPLICATION DATA

## 1.1 INTRODUCTION

The Model 6809 is a low cost, streaming tape drive whose main application is as a backup to disk drives. The 6809 has two data transfer modes — the streaming mode and the start/stop mode. In the streaming mode the drive moves tape at 100 inches per second, transferring data at the rate of 160 kilobytes per second. In this mode gaps are generated on the fly, and starts and stops require repositioning cycles. In the start/stop mode the Model 6809 moves tape at 12.5 inches per second, transferring data at the rate of 20 kilobytes per second. In this mode the drive starts and stops in the gaps, and generally functions as a standard synchronous tape drive.

The Model 6809 contains the electronics required to generate and recover phase encoded, 1600 cpi data, complying with ANSI specifications and compatible with IBM standards. The formatting functions include the generation and detection of the PE ID burst, end-of-file tape marks, the detection of errors and the correction of single track errors, among others. The transport responds to commands such as read one block, read one file, in either forward or reverse directions, in high or low speeds. For ease of service and maintenance, front panel controlled diagnostics are provided to exercise the tape drive while off line. The diagnostics initiate tape motion in high or low speeds, forward or reverse directions.

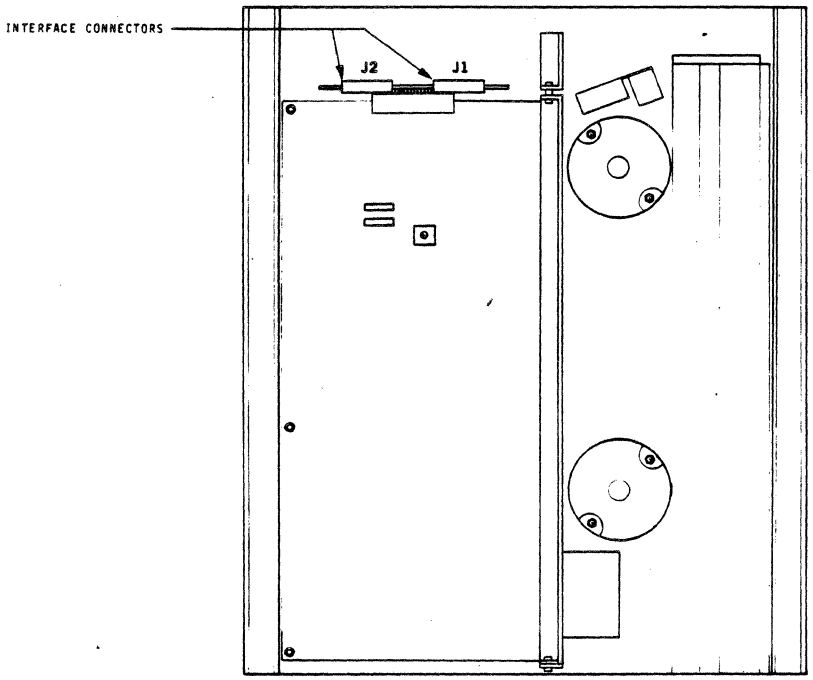
The high performance of the Model 6809 and its low cost have been achieved by the replacement of the capstan, its associated servo electronics and the tape buffering system (either the mechanical tension arms or the vacuum columns) with a single 8049 microprocessor and a single short travel tension arm. The microprocessor controls the servo performance, ramp duration, repositioning cycles, diagnostics and command interpretation as required for the operation of the Model 6809.

While every effort has been made to keep the interfacing of the Model 6809 as compatible as possible with the standard formatter interface, some minor differences do exist due to the additional functions of the 6809, and these must be accounted for when incorporating the 6809 into an existing system. These differences are described in section 1.3.

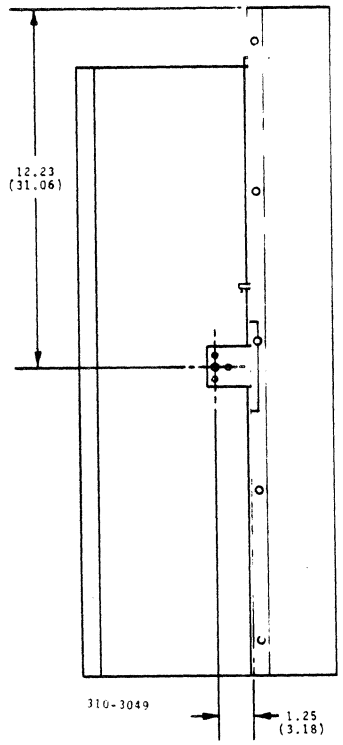
Figure 1-1 shows the outline and installation drawing of the Model 6809. Figure 1-2 shows the control panel functions during normal operation while figure 1-3 shows the control panel during Test Mode operation. Table 1-1 summarizes the electrical and mechanical specifications of the Model 6809.

Note: missing Pg 5 of 6 For
Servo/Control Bd.
TYPE 5926-001
Schematic Diagram
upon receiving From Kennedy
10-27-89

BACK VIEW




LFT SIDE VIEW



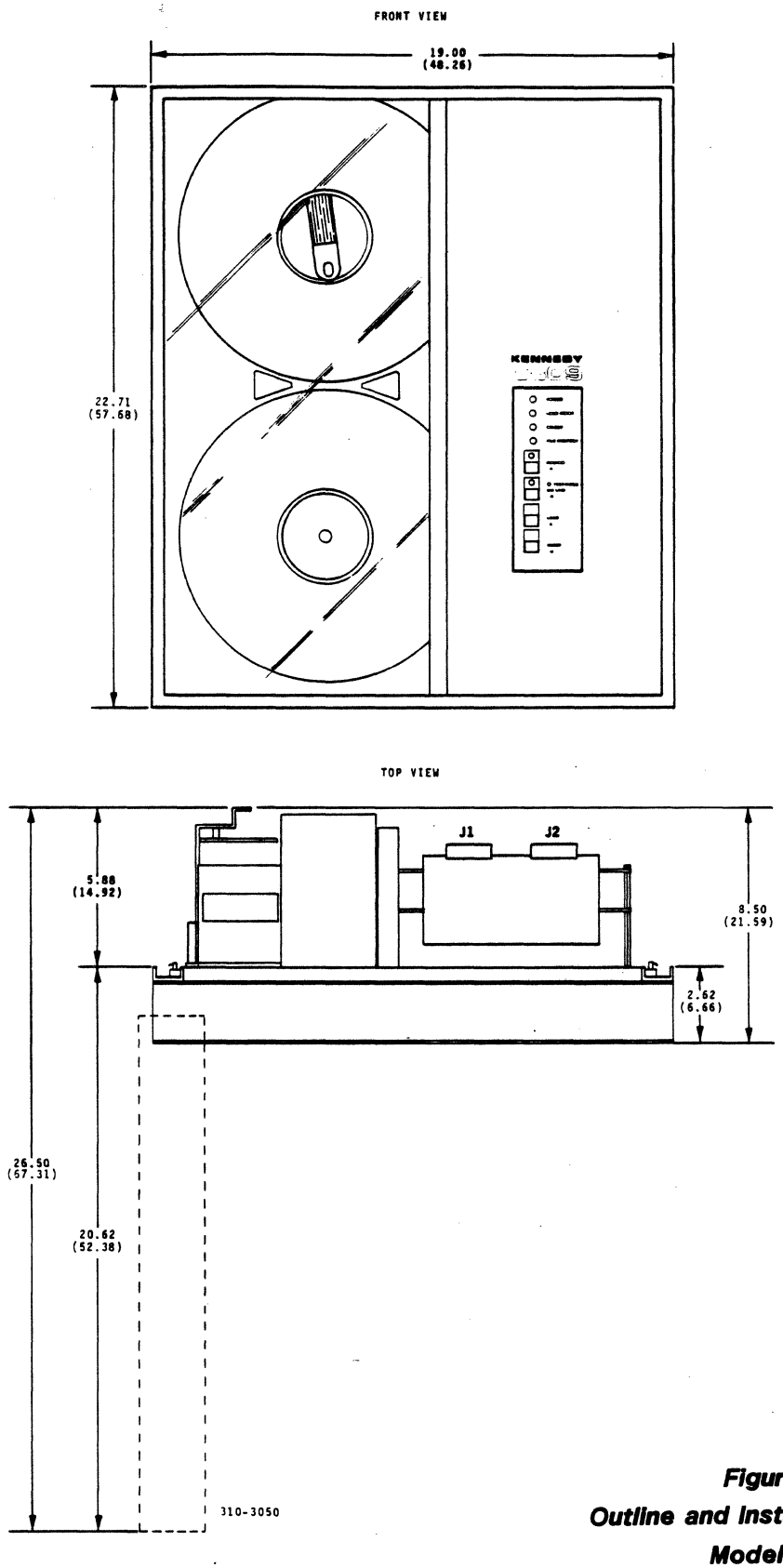



***Figure 1-1***
***Outline and Installation Drawing***
***Model 6809***

## 1.2 ELECTRICAL AND MECHANICAL SPECIFICATIONS

**Tape (computer grade)**

| | |
|---|---|
| Width | 0.5 inch (1.27 cm) |
| Thickness | 1.5 mil (0.038 mm) |
| Tension | 8.0 ounces (227 gm) |
| Reel diameter | to 10.5 inches (26.6 cm) |
| Capacity | 2400 feet (531.5 meters) |
| Reel hub | 3.69 inches (9.37 cm) diameter |
| Reel braking | dynamic |
| Recording mode (IBM compatible) | phase encoded |
| Tape drive | microprocessor controlled |

**Tape speed**

| | |
|---|---|
| Start/stop mode | 12.5 ips (31.75 cm/sec) |
| Streaming mode | 100 ips (254 cm/sec) |
| Instantaneous speed variation | 5% |
| Long term speed variation | 1% |
| Start/stop displacement, 12.5 ips | 0.19 inch (0.476 cm) |
| Start/stop time, 12.5 ips | 30 ms |
| Interrecord gap, short | 0.6 inch (1.52 cm) |
| Interrecord gap, long | 1.2 inches (3.05 cm) |
| Access time at 12.5 ips | |
| Read, short gap | 44 ms |
| Read, long gap | 92 ms |
| Write, short gap | 40 ms |
| Write, long gap | 88 ms |
| Read or write from BOT | 325 ms |
| Access time at 100 ips | |
| Read or write, short gap | 295 ms |
| Read or write, long gap | 301 ms |
| Read or write from BOT | 625 ms |
| Interrecord gap time | |
| At 12.5 ips, short gap | 48 ms |
| At 12.5 ips, long gap | 96 ms |
| At 100 ips, short gap | 6 ms |
| At 100 ips, long gap | 12 ms |

**Command reinstruct time (DBY false, 100 ips only)**

| | |
|---|---|
| Short gap, write mode | 4.0 ms |
| Long gap, write mode | 10.0 ms |
| Short gap, read mode | 6.0 ms |
| Long gap, read mode | 10.0 ms |

**Repositioning time, 100 ips only**

| | |
|---|---|
| Nominal | 870 ms |
| Maximum | 1035 ms |
| Rewind speed | 100 ips (254 cm/sec nominal) |

**Magnetic head assembly**

| | |
|---|---|
| Read to write gap | 0.15 inch (0.38 cm) |
| Interchannel error | 100 uinches (2.5 um) |
| Erase head | full width |
| Load point, end of tape detection | infrared |

**Transport dimensions (see figure 1-1)**

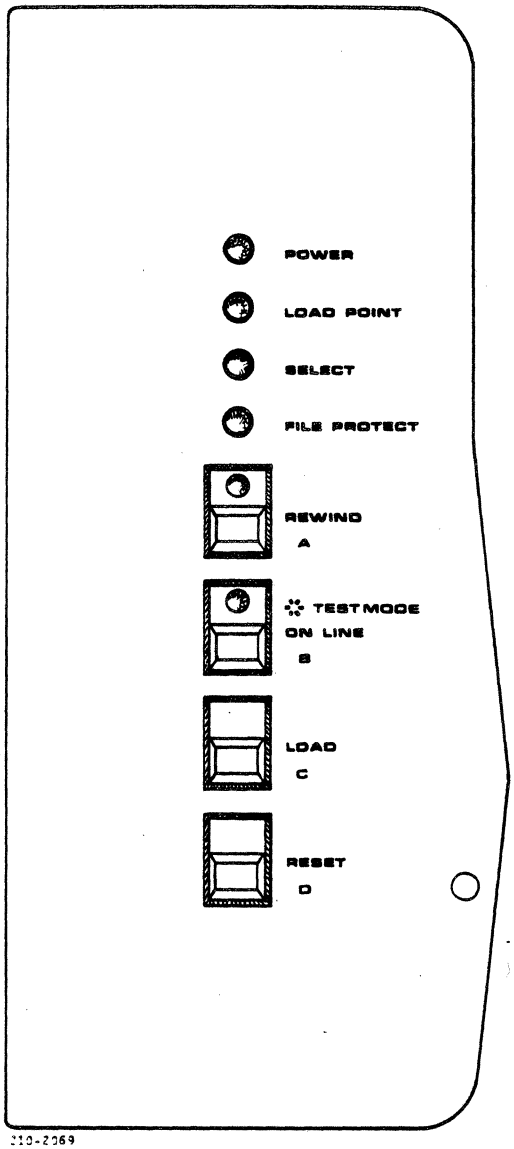
| | |
|---|---|
| Mounting | standard 19" (48.26 cm) rack |
| Height | 22.71 inches (57.68 cm) |
| Width | 19 inches (48.26 cm) |
| Depth from mounting surface | 5.88 inches (14.92 cm) |
| Depth, overall | 8.50 inches (21.59 cm) |
| Weight | 65 pounds (29.48 kg) |
| Shipping weight | 80 pounds (36.29 kg) |
| Operating temperature | $+2^{o}$ to $+50^{o}$C |
| Operating humidity (noncondensing) | 15% to 95% |
| Power requirements | 115 vac, 60 Hz |
| or single phase | 220/240 vac, 50 Hz |
| Maximum power used | 240 watts |

**Table 1-1**

**Model 6809 Tape Transport**
**Electrical and Mechanical Specifications**

**NOTE**

The normal functions of the control panels described below are shown in WHITE letters. The test mode functions are shown in RED letters.




POWER INDICATOR. Illuminated when power is applied to unit by depressing black rocker arm switch.

LOAD POINT INDICATOR. Illuminated when beginning of tape mark is detected.

SELECT INDICATOR. Illuminated when tape unit is on line and selected.

FILE PROTECT INDICATOR. Illuminated when a reel of tape without a write enabled ring is loaded.

REWIND (A). Depressing this pushbutton with unit off line causes it to rewind to load point. When depressed at load point this pushbutton initiates slow speed reverse tape motion, winding the tape onto the supply reel. During test mode this becomes pushbutton A.

ON LINE (B). Depressing this pushbutton once will place unit on line, enabling it to receive commands from the controller. Depressing the pushbutton again will take the unit off line. During test mode this becomes pushbutton B.

LOAD (C). Depressing this pushbutton will tension the tape and initiate a search for load point. This becomes pushbutton C during the test mode.

RESET (D). If unit is on line, depressing this pushbutton would cause it to go off line, and would reset all internal logic. If unit is in streaming mode depressing RESET would cause it to rewind to load point. This pushbutton clears any abnormal internal conditions. During the test mode this becomes pushbutton D.

ADDRESS SELECTION SWITCH (not shown). A thumbwheel switch, located on Servo/Control PC board at the rear of the unit, is used to assign the transport an address between 0 and 7, inclusively.

***Figure 1-2.***

***Model 6809 Controls and Indicators***

**NOTE**

Two Test Mode functions are accessible through the control panel: CALDAC, used to calibrate the D to A converters, and RUN, used to initiate off line tape motions. Only RED pushbutton designations apply during the Test Mode.

A. To enter Test Mode thread the tape and press pushbutton A. TEST MODE indicator will start blinking.

B. To enter RUN mode press pushbutton A again. Tape will advance to LOAD point and stop. The desired test may then be selected as tabulated below:

| TEST | PUSHBUTTON SEQUENCE |
|---|---|
| Low speed forward | AC |
| Low speed reverse | AA |
| High speed forward | CC |
| High speed reverse | CA |

Pressing pushbutton D once will terminate the selected test and exit the RUN mode. To select another test press pushbutton A to reenter RUN, then the pushbutton sequence tabulated above. Pressing pushbutton D twice will exit the Test Mode. The transport will respond by performing a LOAD sequence, and will then be ready to perform normal streaming operations.

C. To enter CALDAC enter Test Mode as described in step A and press pushbutton C. To load tape following CALDAC press the LOAD pushbutton.

***Figure 1-3.***

***Control Panel Test Mode Instructions***

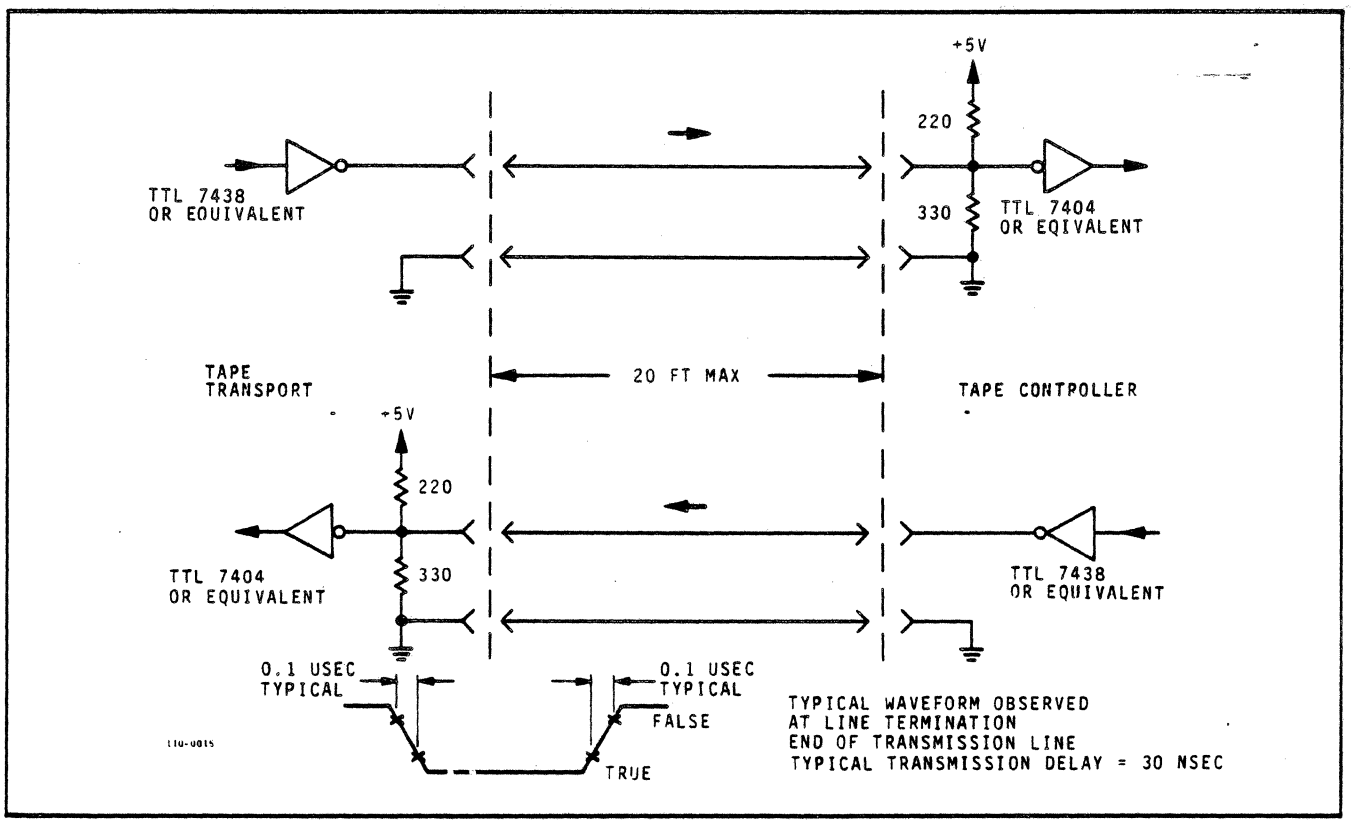



***Figure 1-4.***

***Typical Interface Configuration***

## 1.3 INTERFACE CHARACTERISTICS

The Model 6809 interface has been kept as consistent as possible with the previously used standard formatter interface. Due to inherent differences in the streaming mode, however, and the added functional flexibility of the Model 6809, some interface lines were modified. In particular, a High Speed line has been added to select high speed (100 ips) when true, low speed (12.5 ips) when false. Read Threshold 2 line has been redefined to select long gap (1.2") when true, short gap (0.6") when false. Modifying these lines and providing for the required software changes should allow the connection of the Model 6809 to any standard interface. It should also be noted that when the Command Reinstruct time (see section 1.8) is exceeded, Formatter Busy (FBY) will go true while Data Busy (DBY) will remain false, and the transport will automatically enter a repositioning cycle.

Two previously unavailable functions, Data Security Erase, and File Dump, were added to the Model 6809. Data Security Erase initiates a high speed erase from the point of the command to 1 meter beyond EOT. File Dump command initiates a high speed read of one complete file. The implementation of these functions is shown in table 1-3.

## 1.4 SIGNAL REQUIREMENTS

Signals from the controller to the Model 6809 must conform to the following specifications:

Levels: Low = true = 0 volt
High = false = +3 volts

Pulses: Low = true = 0 volt
High = false = +3 volts

Minimum pulse width: 1 microsecond

Edge transmission delay: no greater than 200 nsec over 20 foot cable

Output signals from the Model 6809 are driven by open collector type line drivers capable of sinking up to 36 ma (25 standard unit loads) in the low true state. The interface circuits are designed so that a disconnected wire results in a false signal. Figure 1-4 shows the line drivers and receivers configuration. The maximum recommended length of the interconnecting cables is 20 feet. The connector pin assignments are provided below.

## 1.5 INTERFACE INPUT SIGNALS (CONTROLLER TO TAPE TRANSPORT)

The following paragraphs describe the specifications and functions for each input signal required from the computer interface to the tape transport. Under the signal name are listed its mnemonic designation, the connector, active pin (and its associated ground pin) designations for its input signal line. Connector designations refer to the interface cable connector that mates with the corresponding card edge connector on the transport.

The pin numbers listed are for the two 50-pin "standard" ribbon cable connectors which will be provided with the unit. Table 1-3 summarizes the interface signals and pin numbers for the standard connectors.

**TRANSPORT ADDRESS**
TAD0, TAD1, TAD2 Level P1-46/45

The status of these lines determines which of up to eight transports are selected by the controller. The transport address is set by means of a thumbwheel switch located on the Servo/Control PC board at the rear of the transport. The following list defines the tape transport addresses produced as a result of the various TAD0, TAD1, TAD2.

| TAD0 | TAD1 | TAD2 | Address |
|---|---|---|---|
| 0 | 0 | 0 | SLT0 |
| 0 | 1 | 0 | SLT1 |
| 1 | 0 | 0 | SLT2 |
| 1 | 1 | 0 | SLT3 |
| 0 | 0 | 1 | SLT4 |
| 0 | 1 | 1 | SLT5 |
| 1 | 0 | 1 | SLT6 |
| 1 | 1 | 1 | SLT7 |

**INITIATE COMMAND**
GO Pulse P1-8/7

A pulse which initiates any command specified by the command lines described in the following paragraphs. Information on the command lines is copied in the corresponding formatter flip-flops on the trailing edge of the GO pulse. FBY is set true when the GO pulse is given with the selected transport ready.

**COMMAND LINES**

The levels on these lines issue a command to the formatter on the trailing edge of the GO pulse. The REV, WRT, WFM, HSP, ERASE, LGP and DEN levels must be held steady from 0.5 microsecond prior to the leading edge to 0.5 microsecond following the trailing edge of the GO pulse. See table 1-4 for Command Structure.

**REVERSE**
REV Level P1-18/17

A level which initiates reverse tape motion when true. When false, this level specifies forward tape motion.

**WRITE**
WRT Level P1-34/33

Write mode is specified when this level is true; read mode is specified when this level is false.

**WRITE FILE MARK**
WFM Level P1-42/41

When this level and WRT are true, the transport will write a file mark on the tape.

**ERASE**
ERASE Level P1-40/39

Setting ERASE, WFM, WRT and EDIT true initiates a data security erase, erasing tape continuously from point of issue to about 1 meter beyond EOT. A fixed erase is issued by setting ERASE, WRT and WFM true, causing about 3.75" of tape to be erased. A variable erase is initiated by setting ERASE and WRT true and is terminated by issuing LWD true. During variable erase the transport supplies Writes Strobes, to be used for distance measurement (each strobe is equivalent to 1 character space).

**EDIT**
EDIT Level P1-38/37

At present this line is used in conjunction with ERASE, WFM and WRT to initiate data security erase (see ERASE command).

**HIGH SPEED**
HSP Level P2-50/49

A level which causes the selected on line transport to operate in high speed mode.

**REWIND**
REW Pulse P1-20/19

A pulse which causes the selected on line transport to rewind to load point. This pulse does not cause FBY to go true.

**UNLOAD COMMAND**
UNL Pulse P2-24/23

This pulse causes the selected transport to go off line, rewind the tape, and when BOT is encountered, unload tape onto the supply reel.

**LAST WORD**
LWD Level P1-4/3

When this level is true during a write or erase command, it indicates that the next character to be strobed into the formatter is the last character of the record. LWD goes true when the last data character is placed on the interface lines.

**FORMATTER ENABLE**
FEN Level P2-18/17

When false, this level causes the system to revert to the quiescent state.

**LONG GAP**

| | | |
|---|---|---|
| LGP | Level | P1-36/35 |

A level which causes the selected (on line) transport to generate a 1.2" long IRG.

**WRITE DATA PARITY AND WRITE DATA LINES**

| | | |
|---|---|---|
| WP | Levels | P1-22/21 |
| W0 | | P1-10/9 |
| W1 | | P1-12/11 |
| W2 | | P1-30/29 |
| W3 | | P1-26/25 |
| W4 | | P1-6/5 |
| W5 | | P1-32/31 |
| W6 | | P1-28/27 |
| W7 | | P1-24/23 |

The 8 write data lines (9 in case of external parity option) are utilized to transmit write data from the controller to the formatter. W0 corresponds to the most significant bit and W7 to the least significant bit of each character.

The first character of a record should be available on these lines per time defined in table 1-1 after DBY goes true and should remain until the trailing edge of the first WSTR is issued by the formatter. The next character of information must then be placed on these lines within one-half a character period.

Subsequent characters of a record are processed in this manner until LWD is set true by the controller when the last character is transmitted.

## 1.6 INTERFACE OUTPUTS (TRANSPORT TO CONTROLLER)

The signals listed below are supplied from the transport to the controller interface and include decoded read data, formatting status and transport status indications.

**FORMATTER BUSY**

| | | |
|---|---|---|
| FBY | Level | P1-2/1 |

This level goes true on the trailing edge of the GO pulse when a command is issued by the controller. FBY goes false upon the completion of a block after Data Busy (DBY) goes false. In high speed mode FBY going true while DBY remains false indicates that the drive has entered a Reposition Cycle. Note that omitting Strap 11 on Servo/Control PC board ungates the GO pulse from FBY, allowing a command to be accepted with FBY true, provided that Data Busy DBY is false. This allows the next command to be accepted during the Repositioning Cycle.

**DATA BUSY**

| | | |
|---|---|---|
| DBY | Level | P2-38/37 |

This level goes true after the unit has ramped up to speed and the gap has been completed; DBY remains true until data transfer and the appropriate post record delay are completed.

**CORRECTED ERROR**

| | | |
|---|---|---|
| CER | Pulse | P2-42/41 |

When true, this pulse indicates that a single track dropout has been detected and the formatter is performing an error correction.

**HARD ERROR**

| | | |
|---|---|---|
| HER | Pulse | P2-12/11 |

When true, this pulse indicates that an uncorrectable read error has occurred and that the record should either be reread or rewritten.

**IDENTIFICATION**

| | | |
|---|---|---|
| IDENT | Level | P2-16/15 |

When true, this level identifies PE tapes. PE tapes are detectable in the read forward mode by the presence of an identification burst on the parity channel.

**FILE MARK**

| | | |
|---|---|---|
| FMK | Pulse | P2-14/13 |

File mark is pulsed when a file mark is detected on the tape during a read operation or during a write file mark operation. The FMK line will be pulsed after a complete file mark record has been read.

**ON LINE**

| | | |
|---|---|---|
| ONL | Level | P2-44/43 |

A level that is true when the on line flip-flop is set. When true, the transport is under remote control. When false, the transport is under local control.

**READY**

| | | |
|---|---|---|
| RDY | Level | P2-28/27 |

A level that is true when the tape transport is on tape; that is, when the initial load sequence is complete and the transport is not rewinding. When true, the transport is ready to receive a remote command.

**FILE PROTECT**

| | | |
|---|---|---|
| FPT | Level | P2-32/31 |

A level that is true when a reel of tape without a write-enable ring is mounted on the transport supply (or file) hub.

**LOAD POINT**

| | | |
|---|---|---|
| LDP | Level | P2-4/5 |

A level that is true when the load point marker is under the BOT sensor and the transport is not rewinding. After receipt of a motion command the signal will remain true until the load point marker leaves the BOT sensor area.

**END OF TAPE**

| | | |
|---|---|---|
| EOT | Level | P2-22/21 |

A level that is true when the EOT marker is detected in the forward direction. Goes false when the EOT marker is detected in reverse (REWIND).

**REWINDING**

| | | |
|---|---|---|
| RWD | Level | P2-30/29 |

A level that is true when the transport is engaged in a rewind operation or returning to the load point at the end of the rewind operation.

**WRITE STROBE**

| | | |
|---|---|---|
| WSTR | Pulse | P2-36/35 |

This line pulses each time a data character is written onto tape. WSTR samples the write data lines WP, W0-W7 from the controller and copies this information character by character into the formatter write logic. The first character should be available prior to the first write strobe pulse and succeeding characters should be set up within half a character period after the trailing edge of each write strobe pulse.

**READ STROBE**

| | | |
|---|---|---|
| RSTR | Pulse | P2-34/33 |

This line consists of a pulse for each character of read information to be transmitted to the controller. This signal should be used to sample the read data lines RDP, RD0-RD7.

**READ DATA LINES**

| | | |
|---|---|---|
| RP | Levels | P2-1/5 |
| R0 | | P2-2/5 |
| R1 | | P2-3/5 |
| R2 | | P1-48/47 |
| R3 | | P1-50/49 |
| R4 | | P2-6/5 |
| R5 | | P2-20/19 |
| R6 | | P2-10/9 |
| R7 | | P2-8/7 |

Each character read from tape is made available by parallel sampling the read lines with READ STROBE. Since the data remains on the read data lines for a full character period, the corresponding RSTR pulses are timed to occur at approximately the center of the character period.

**SPEED**

| | | |
|---|---|---|
| SPD | Level | P2-40/39 |

A level which, when true, indicates that selected transport is in high speed streaming mode.

## 1.7 INTERFACE SUMMARY

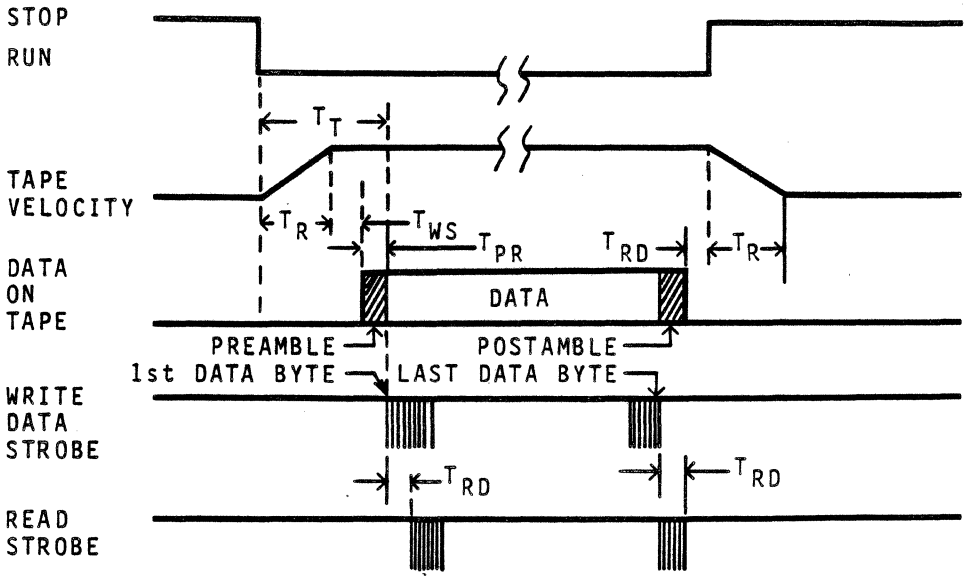
Table 1-2 lists the states of the command lines required to implement the different transport functions. Table 1-3 lists a summary of the 6809 standard two 50 pin connectors. The table includes the signal names, mnemonics and in/out designations. Figure 1-5 shows read-after-write timing relations for the normal start/stop mode.

| COMMAND | REV | WRT | WFM | ERASE | EDIT |
|---|---|---|---|---|---|
| READ FORWARD | H | H | H | H | H |
| *READ REVERSE | L | H | H | H | H |
| READ REVERSE EDIT | L | H | H | H | L |
| WRITE | H | L | H | H | H |
| WRITE FILE MARK | H | L | L | H | H |
| ERASE VARIABLE | H | L | H | L | H |
| ERASE (FILE LENGTH) | H | L | L | L | H |
| DATA SECURITY ERASE | H | L | L | L | L |
| SPACE FORWARD (1 BLOCK) | H | H | H | L | H |
| SPACE REVERSE (1 BLOCK) | L | H | H | L | H |
| SEARCH FILE FORWARD | H | H | L | H | H |
| SEARCH FILE REVERSE | L | H | L | H | H |
| SEARCH FILE FORWARD (IGNORE DATA) | H | H | L | L | H |
| SEARCH FILE REVERSE (IGNORE DATA) | L | H | L | L | H |

*Read Reverse applies to low speed mode only.

***Table 1-2***

***Model 6809 Functional Command Structure***




S=SPEED 1 PS
T=TIME IN SECONDS
$T_{PD}$=PREAMBLE DELAY= POSTAMBLE $\frac{.025}{S}$
$T_R$=RAMP TIME= $\frac{.375}{S}$
$T_{RD}$=READ DELAY= $\frac{.15}{S}$
$T_T$=TOTAL WRITE DELAY= $\frac{.475}{S}$
$T_{WS}$=WRITE START DELAY= $\frac{.075}{S}$

110-0193

***Figure 1-5.***

***Read After Write Timing***

| Pin SIG/GRD | Mnemonic | Signal | In/Out |
|---|---|---|---|
| **P1** | | | |
| P1-2/1 | FBY | Formatter Busy | Out |
| P1-4/3 | LWD | Last Word | In |
| P1-6/5 | W4 | Write Data 4 | In |
| P1-8/7 | GO | Initiate Command | In |
| P1-10/9 | W0 | Write Data 0 | In |
| P1-12/11 | W1 | Write Data 1 | In |
| P1-16/15 | | Not used | |
| P1-18/17 | REV | Reverse/Forward | In |
| P1-20/19 | REW | Rewind | In |
| P1-22/21 | WP | Write Data Parity | In |
| P1-24/23 | W7 | Write Data 7 | In |
| P1-26/25 | W3 | Write Data 3 | In |
| P1-28/27 | W6 | Write Data 6 | In |
| P1-30/29 | W2 | Write Data 2 | In |
| P1-32/31 | W5 | Write Data 5 | In |
| P1-34/33 | WRT | Write/Read | In |
| P1-36/35 | LGP | Long Gap | In |
| P1-38/37 | EDIT | Edit | In |
| P1-40/39 | ERASE | Erase | In |
| P1-42/41 | WFM | Write File Mark | In |
| P1-44/43 | | Not used | In |
| P1-46/45 | TAD0 | Transport Address 0 | In |
| P1-48/47 | R2 | Read Data 2 | Out |
| P1-50/49 | R3 | Read Data 3 | Out |
| **P2** | | | |
| P2-1/5 | RP | Read Data P | Out |
| P2-2/5 | R0 | Read Data 0 | Out |
| P2-3/5 | R1 | Read Data 1 | Out |
| P2-4/5 | LDP | Load Point | Out |
| P2-6/5 | R4 | Read Data 4 | Out |
| P2-8/7 | R7 | Read Data 7 | Out |
| P2-10/9 | R6 | Read Data 6 | Out |
| P2-12/11 | HER | Hard Error | Out |
| P2-14/13 | FMK | File Mark | Out |
| P2-16/15 | IDENT | ID Burst | |
| P2-18/17 | FEN | Formatter Enable | In |
| P2-20/19 | R5 | Read Data 5 | Out |
| P2-22/21 | EOT | End of Tape | Out |
| P2-24/23 | UNL | Unload Command | In |
| P2-28/27 | RDY | Ready | Out |
| P2-30/29 | RWG | Rewinding | Out |
| P2-32/31 | FPT | File Protect | Out |
| P2-34/33 | RSTR | Read Strobe | Out |
| P2-36/35 | WSTR | Write Strobe | Out |
| P2-38/37 | DBY | Data Busy | Out |
| P2-40/39 | SPD | Speed | Out |
| P2-42/41 | CER | Corrected Error | Out |
| P2-44/43 | ONL | On Line | Out |
| P2-46/45 | TAD1 | Transport Address 1 | In |
| P2-48/47 | TAD2 | Transport Address 2 | In |
| P2-50/49 | HSP | High Speed | In |

***Table 1-3***

***Model 6809 Interface Summary***

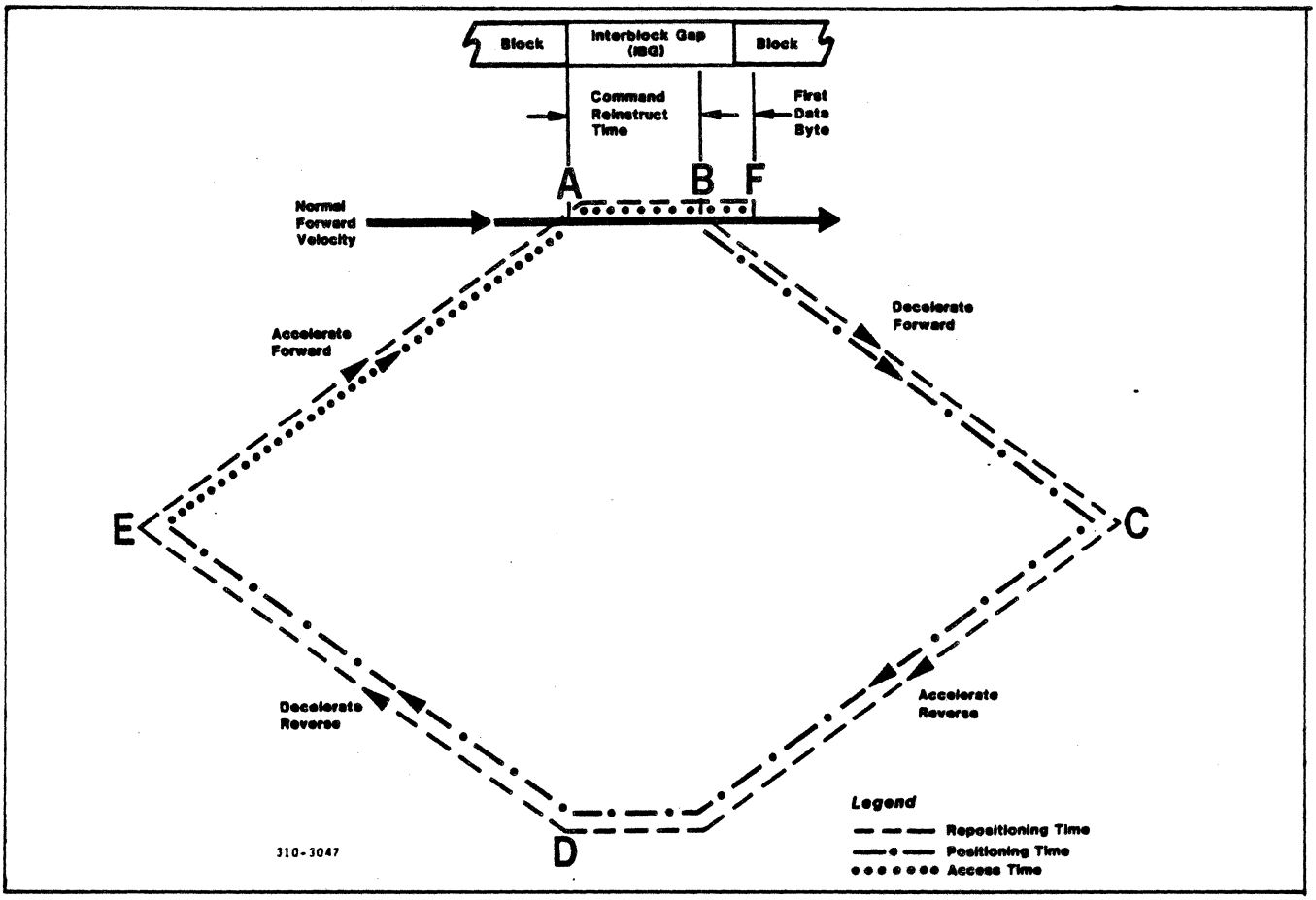



***Figure 1-6.***

***Repositioning Cycle***

## 1.8 STREAMING MODE TIMING CONSIDERATIONS

When in the streaming mode the Model 6809 requires approximately 300 msec to ramp to speed from a stopped state, moving about 15 inches of tape in the process. The prolonged ramp necessitates a repositioning cycle each time a command is not received during the allotted 4.0 msec period in the interrecord gap, called the Command Reinstruct Time. The Command Reinstruct Time and the repositioning cycle are illustrated in figure 1-6. The Command Reinstruct period starts when Formatter Busy (FBUS) goes false at the end of a block, shown as point A in the figure, and ends 4.0 msec later, when FBUS goes true again (point B). Note that the 4.0 msec Command Reinstruct Time can be extended to 10.0 msec by using the long gap mode. If a command is received between points A and B (GO pulse issued) the transport will acknowledge it by setting Formatter Busy (FBY) true and will continue streaming, provided the command is the same as the previous command. If no new command is received by point B, the transport will automatically reposition by first decelerating to a stop (point C on figure 1-6), accelerating backwards and passing over the interrecord gap D, then ramping down to a stop at E. At this point FBUS goes false and the transport waits for a command to be issued. When the next command is issued, the transport accelerates from point E to attain normal velocity and executes the command. The time between the stopped state (E) and the transfer of the first data byte (F) is defined as the Access Time. Access Times for both the streaming and start/stop modes are listed in table 1-5. The table also lists the interrecord gap times, the Command Reinstruct Time, and the Repositioning Time, defined as the time between the end of the Command Reinstruct Time (B) and the stopped state (E).

When a read reverse command is issued during an error recovery sequence, the transport decelerates to a stop at C, accelerates in reverse and reads the erroneous record. It starts decelerating when the block prior to the erroneous one is detected (A') and stops at point E'. Points A' and E' are in the same relation to the prior block as A and E to the erroneous block. The transport then awaits the next instruction, be it a reread, a rewrite, or an erase.

| FUNCTION | START/STOP | STREAMING |
|---|---|---|
| ACCESS TIME (E to A to F) | | |
| Read, Nominal (0.6" gap) | 44 ms | 295 ms |
| (1.2" gap) | 92 ms | 301 ms |
| From BOT | 325 ms (approximate) | 625 ms (approximate) |
| IBG TIME (A to B to F) | | |
| (0.6" gap) | 48 ms | 6 ms |
| (1.2" gap) | 96 ms | 12 ms |
| COMMAND REINSTRUCT TIME | | |
| Between write block or write tape mark | | |
| (0.6" gap) | | 3.5 ms |
| (1.2" gap) | | 10.0 ms |
| Between read blocks | | |
| (0.6" gap) | | 6.0 ms |
| (1.2" gap) | | 10.5 ms |
| *REPOSITIONING TIME (B to C to D to E) | | |
| | | 870 msec (nominal) |
| | | 1035 ms (worst case) |

*Repositioning time for error recovery is somewhat greater depending on length of record being read in reverse.

***Table 1-5.***

***Streaming and Start/Stop Timing Specifications***

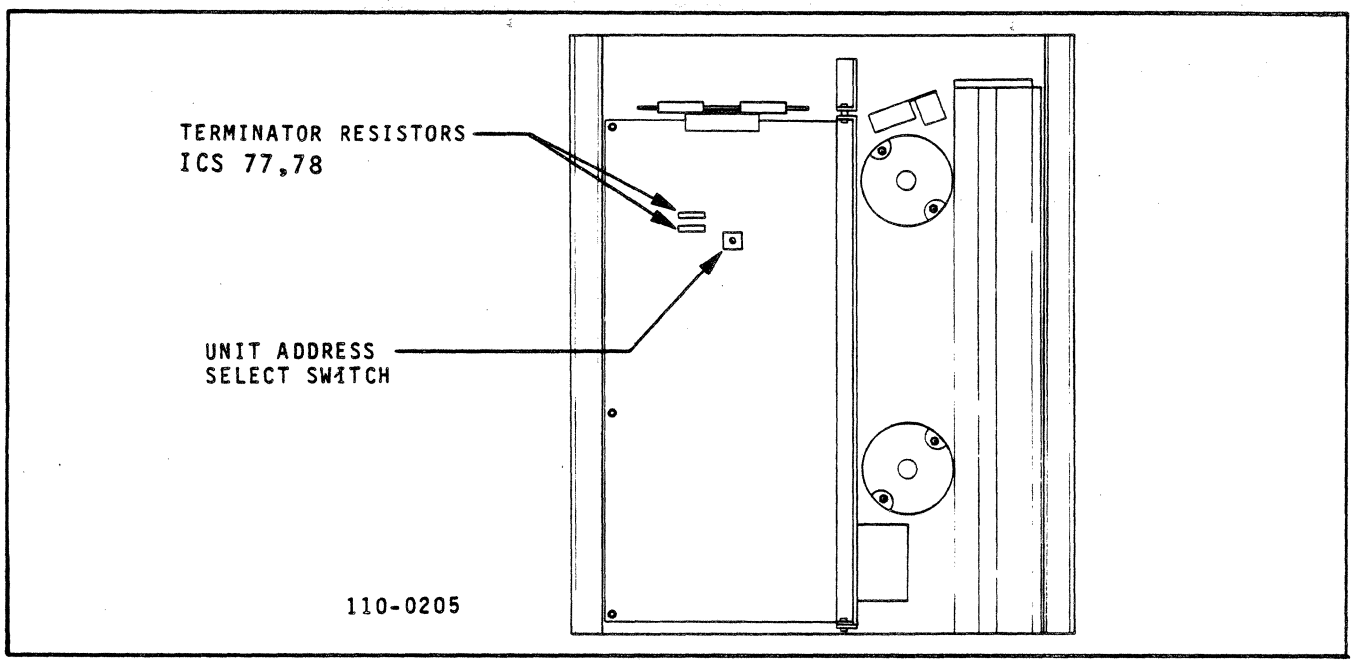



***Figure 1-7.***

***Address Switch and Terminator Location***

## 1.9 TRANSPORT DAISYCHAIN CONNECTION

Up to 8 transports may be connected in a daisychain configuration. To connect the transports in this fashion 2 daisychain cables, Kennedy Part Number 190-6999-xxx should be ordered. The first digit of the dash number indicates the number of transports to be connected by the cable. The last two digits of the dash number indicate the total length of the cable in feet. Thus cable part number 190-6999-420 would specify a 4 transport daisychain cable, 20 feet long with 4 feet between each transport and 4 feet between the first transport in the chain and the controller. The first connector on the cable, to be plugged to the controller, is a 50 pin connector Kennedy Part Number 121-0166-001. The connectors to be plugged to the transports are 50 pin connectors Kennedy Part Number 121-0162-002.

When a daisychain connection is used it is necessary to assign each transport with a different address number using the address selection switch located on the Servo/Control PC board at the rear of the unit, as shown in figure 1-7. The address assigned to the transport should be between 0 and 7. Single transports should always be assigned address 0. In addition the terminator resistors, located on ICs 77 and 78 on the Servo/Control board, as shown in figure 1-7, should be removed from all but the last transport in the daisychain. A daisychain configuration is shown in figure 1-8. Note that if the total cable length exceeds 20 feet, active repeaters must be used.

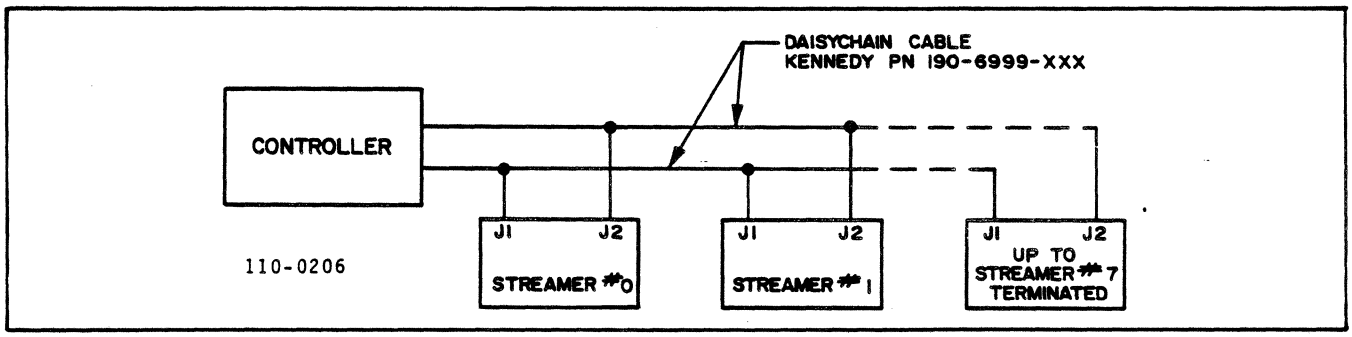



***Figure 1-8.***

***Daisychain Configuration***

# SECTION II

# INSTALLATION AND OPERATION

## 2.1 INSTALLATION

### 2.1.1 INSPECTION

Prior to installation, inspect thoroughly for foreign material that may have become lodged in the reel hubs and other moving parts.

### 2.1.2 MOUNTING

Physical dimensions and outline of the tape transport are shown in figure 1-1. The transport requires 22.7 inches vertical mounting space on the standard 19 inch rack. Transports in a system configuration should be arranged to require less than 20 feet of cabling between the tape controller and the furthest tape unit.

### 2.1.3 SERVICE ACCESS

Access to the transport electronics is available from the rear and sides of the unit when the unit is extended on its slides. To gain access to the PE Read and the Read Amplifier PC boards first remove the interconnect board, then the Servo/Control PC board retaining screws and standoffs, and swing the Servo/Control PC board open on its hinge. The PE Read is the top of the two exposed boards, the Read Amplifier is the lower of the two. Access to the Tape Tension PC board is gained by removing the PE Read and the Read Amplifier retaining nuts, and swinging the boards open, exposing the tape sensor assembly. The Voltage Regulator PC board is located between the two reel motors. The Power Amplifier PC board is attached to the heatsink assembly, to the left of the unit (when facing the unit from the rear). For servicing electronics test points are provided by standoff pins on the circuit boards, and are identified by upper case letters near each test point.

### 2.1.4 INTERCABLING

Installation of the unit requires two 50 line ribbon cables and connectors, matching the two edge connectors on the Interconnect PC board. Connector pin assignments are listed in table 1-3.

### 2.1.5 POWER CONNECTIONS

**CAUTION**

Before connecting the unit to the power source, make certain the line voltage is the correct voltage (115 or 230 vac) and that the proper fuse has been installed.

A power line module, including the power connector, voltage selector and the fuse, is accessible from the top of the unit. Voltage selection is accomplished by the insertion of the selector PC board in such a manner as to show the selected voltage designation through the plastic window. Note that the fuse must be removed prior to changing the voltage selection, and the properly rated fuse for the new voltage must then be installed.

A detachable power cord is supplied with the tape unit. The power cord is 9 feet long and has a NEMA three-prong (two power, one chassis ground) plug for connection to the power source.

## 2.2 OPERATION

### 2.2.1 INTERFACE

Before placing the unit in operation, make certain that the interface connection procedures outlined in Section I have been performed.

### 2.2.2 CONTROLS AND INDICATORS

Figure 1-2 lists the controls and indicators for the tape transport and describes the functions of each. The test panel controls are described in paragraph 4.7.

### 2.2.3 PRELIMINARY PROCEDURES

Before placing the unit in operation, proceed as follows:

a. Check the tape transport read/write head, erase head, capstan and idlers for any foreign material.

b. Check for correct line voltage and make sure that correct fuses are installed (paragraph 2.1.5).

c. Push primary power switch on.

### 2.2.4 TAPE THREADING

To thread the tape on the transport, proceed as follows:

a. Raise the latch of the quick-release hub and place the tape file reel to be used on the supply hub (figure 2-1) with the write-enable ring side next to the transport deck.

b. Hold the reel flush against the hub flange and secure it by pressing hub latch down.

c. Thread the tape along the path as shown by the threading diagram (figure 2-1).

d. Holding the end of the tape with a finger, wrap a few turns clockwise around the takeup reel hub.

2.2.5 TAPE LOADING

Pressing and holding the LOAD pushbutton for approximately 0.5 second energizes the reel servos and initiates a load sequence. Tape advances to the load point marker and stops.

If for some reason the load point marker is already past the sensor as, for example, in restoring power after a shutdown, tape continues to move for approximately 6 seconds and then automatically initiates rewind.

Once pressed, the LOAD switch is inactive until power has been turned off or tape is removed from the machine.

2.2.6 PLACING TAPE UNIT ON LINE

After the tape is properly threaded and has been loaded and brought to the load point, press the ON LINE pushbutton and check that ON LINE indicator illuminates. (The REWIND pushbutton is disabled when the tape unit is on line.) On line status enables the tape unit to be remotely selected and to perform all normal operations under remote control.

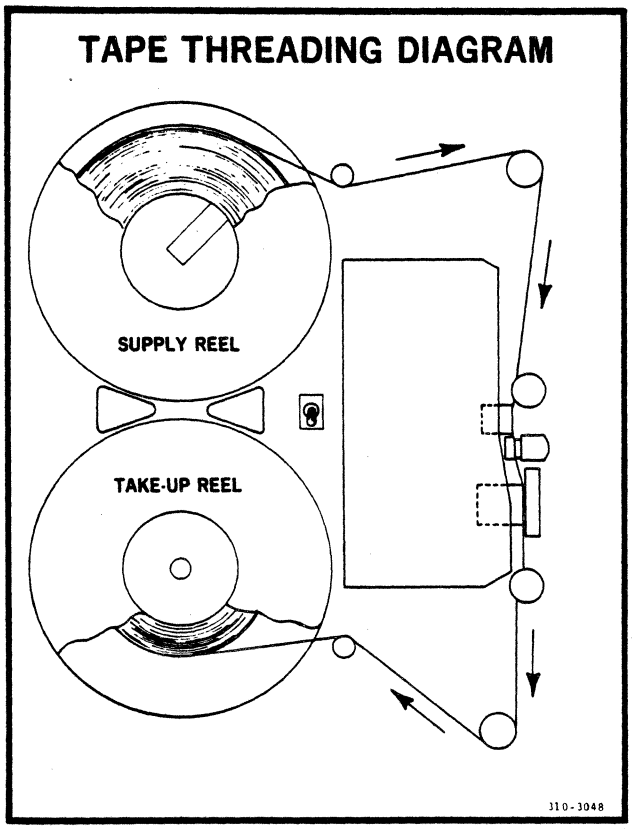



***Figure 2-1.***

***Tape Threading***

2.2.7 TAPE UNLOADING AND REWIND

Provision is made in the 6000 series transports for rewinding a tape to the load point under remote control. However, this operation may also be performed manually. Proceed as follows.

a. If the ON LINE indicator is illuminated, press the ON LINE pushbutton. Check that the indicator extinguishes when pressure is removed.

b. Press the REWIND pushbutton. The tape will now rewind to the load point marker.

c. After the tape has been positioned at the load point under remote or local control, press the REWIND pushbutton to unload the tape past the load point to the physical beginning of the tape.

**NOTE**

The rewind sequence cannot be stopped until the tape has rewound either to the load point or until tape is rewound onto the supply reel after an unload sequence.

2.2.8 POWER SHUTDOWN

A tape transport should not be turned off when tape is loaded and is past the load point marker. Kennedy transports are designed to prevent physical damage to the tape in the event of power failure, and to minimize operator error which could destroy recorded data. In the event of power failure during tape unit operation, manually wind the tape forward several feet before restoring power. When power has been restored, press the LOAD pushbutton. If load point is not reached within 6 seconds the tape will rewind, searching for load point. If desired, the tape can then be advanced to the data block nearest the point at which the power failure occurred, by initiating the appropriate control commands.

Although it is possible to develop procedures which would allow power shutdown between files or record blocks on a tape, this is not recommended. Where data files are short, it is preferable to use smaller tape reels.

# SECTION III

# THEORY OF OPERATION

## 3.1 INTRODUCTION

The Model 6809 is a microprocessor controlled tape drive that produces formatted phase encoded data. The microprocessor plays an important part in all aspects of transport operations, from command interpretation to reel motor control. The overall flow chart of the microprocessor program is shown in figure 3-1. Type 8039 microprocessor and its associated 4-K ROM are located on an Emulator board which produces the equivalent interconnection to the 8049 chip and plugs into the Servo/Control board. The Servo/Control board, the large board at the rear of the unit, includes the microprocessor network, the command interface, the entire write electronics and additional functions. Outputs from the Servo/Control board are supplied directly to the controller interface through the Interconnect board, and to the power amp, which provides the power inputs to the reel motors. Located below the Servo/Control board are two connected boards. The lower of the two is the Read Amplifier, containing the analog circuitry which amplifies the signals from the read head. The upper of the two boards is the PE Read, which processes the analog data, converts it to logic levels, performs error correction and supplies the decoded data to the controller. Additional electronic modules of the 6809 include the Voltage Regulator, the Tape Tension Sensor, the Control Panel and the Reel Sensor boards.

## 3.2 SERVO/CONTROL BOARD

### 3.2.1 INTRODUCTION

The Servo/Control board performs all control functions associated with the tape transport operation. Included on the board are the microprocessor network, which decodes the controller commands and initiates the required transport motions, and the PE data generation circuitry. Listed below are the functions performed by the board and the schematic page on which they appear.

| Servo/Control Page Number | Functions Performed |
|---|---|
| 1 | Front panel control<br>Power failure detection<br>Tape motion counter<br>File protect circuitry<br>Write/erase current drivers |
| 2 | Reel size sensor circuitry<br>Data I/O<br>Microprocessor network<br>Bus addressing<br>Takeup servo circuitry and DAC0 |
| 3 | BOT/EOT, on line interrupt generator<br>Takeup and supply reel DACS<br>Crystal clock and dividing network<br>Tension sensor circuitry<br>Supply servo control |
| 4 | Interrupt and I/O control<br>Inputs from controller<br>Outputs to controller<br>Address selection circuitry<br>Command decoding |
| 5 | Write data inputs<br>Phase encoding circuits<br>Formatting circuits<br>Write head drivers |
| 6 | Tape motion detection<br>Tape direction detection<br>Repositioning counter<br>Velocity counter |

### 3.2.2 MICROPROCESSOR INPUT/OUTPUT

Inputs and outputs to the microprocessor are supplied on two 8-bit wide ports, P1 and P2, and an 8-bit data bus. The ports are quasi-bidirectional while the bus is truly bidirectional. The bus is used for transmission of both external address and data. As an example assume that the microprocessor is given an instruction to monitor the transport control panel status lines, which are presented to bus buffer IC56 (page 2-A2, type 5426). In this case the address of IC56 (buffer 7) is presented on the data bus, is passed through bidirectional buffer IC85 (since READ/ is false), and is latched into IC47 on the trailing edge of Address Latch Enable ALE. The outputs of IC47 are decoded by IC31, a 3 to 8 decoder whose outputs are gated with the READ/ signal output by the microprocessor. READ7/ true at IC14-11 is used to enable buffer IC56, providing the control panel status information to the data bus, back to the microprocessor through IC85, which now operates in the read mode with data flowing toward the 8049 chip.

### 3.2.3 POWER UP SEQUENCE

During power up, until capacitor C8 charges up the output of IC109-1 will be low, generating Master Reset MRESET/ true to initialize the system's counters and flip-flops. The microprocessor P1-7 output is combined with the MRESET/ signal to generate PRESET/ true, the initializing signal used by the microprocessor itself to ensure power stability

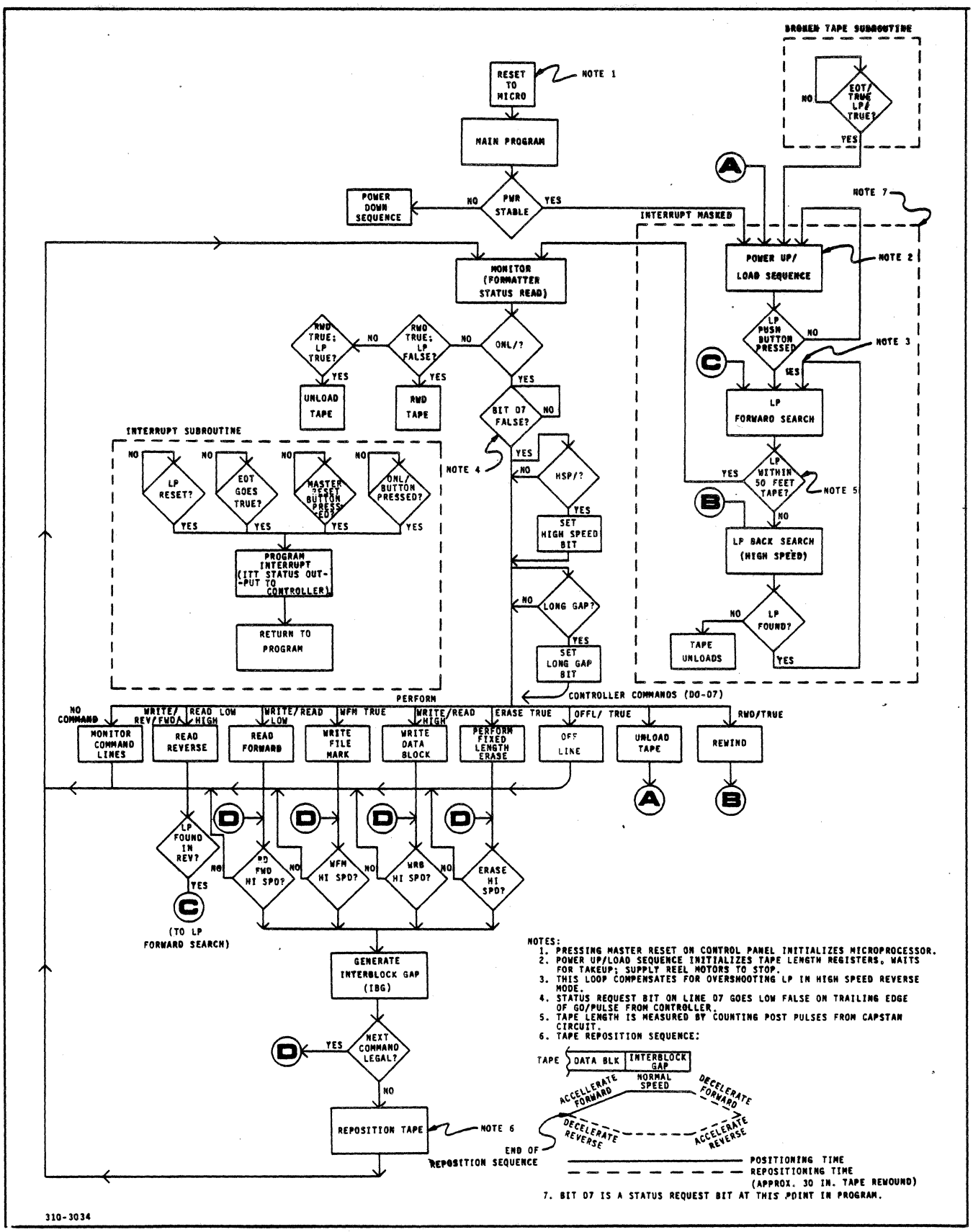



***Figure 3-1. Model 6809 Flowchart***

prior to the start of program execution. When PRESET/ goes false the MPU will test its T1 input (T1 low indicates stable power). If power is not stable the microprocessor jumps to a subroutine which performs an orderly power down sequence. Note that switch S2, located on the board, can also be used to issue a MRESET/ in case of an abnormal condition that arises while testing the unit. Warning of an imminent power failure is provided by the POWER DROPOUT signal, supplied by the Voltage Regulator board. The processor will then check for power stability and take appropriate action.

Crystal Oscillator and Divider Network
(Schematic Type 5426, page 3 of 6)

The master clock frequency of 10.24 MHz is supplied by a crystal oscillator consisting of IC6 and its associated circuitry. The master frequency is supplied to the microprocessor as XTL1. Additionally, it is divided by counters IC4, IC11, IC12, and IC13 to provide the other frequencies required by the unit. CLK1, used to clock the tape position counter, is 853 KC in high speed, 106.6 KC in low speed, and 20 KC during the ramp. Frequency 2F, used by the data encoding and decoding sections, is 320 KC during high speed operation and 40 KC during low speed operation.

### 3.2.4 MICROPROCESSOR SERVO CONTROL

The microprocessor receives reel size data, tape position data and tape speed data from the transport, synthesizes those and compares the derived information with a table stored in memory. It then outputs the required current information to the reel servos through a set of D to A converters.

The reel size is determined by a pair of LED/ photosensors located under the supply reel which detect reflections from the reel surface, determining whether a 10.5", an 8.5" or a 7" reel is mounted. The reel size plays an important function in determining the inertia factors.

The tape speed is determined by an optical tach rotated by the takeup tape roller. The optical tach output is picked up by two detectors, one of which is adjustable so that the signals at test points 11 and 12 are square waves that are 90 degrees out of phase with respect to each other. Direction of motion is determined by which of the two signals leads the other as shown by the output of flip-flop IC112-9 (low in forward direction). The tach outputs are digitized by a circuit consisting of ICs 113, 118, 87, 112 and 103 (page 6 of 6, type 5426 schematic). The stop bit is generated by a circuit consisting of a differentiator, a rectifier and an adder. The sinwt and coswt waveforms output by the optical encoder are differentiated by the input capacitors and two sections of IC104, producing a waveform proportional in amplitude to the angular frequency, and hence to tape velocity. The output of the differentiator stages are then rectified by the four sections of IC125, are added and supplied to an integrator stage which produces a DC level proportional to the tape velocity. The velocity profile can be monitored at Test Point 7. When the velocity profile approaches zero the circuit generates STOPPED/ true.

The circuit consisting of ICs 102, 124 and 100 forms the POST pulse on the leading edge of the POST square wave. Elapsed time between POST pulses is counted by the counter consisting of ICs 32 and 48. Upon the arrival of each POST signal the counters output is latched into IC49 and the counters are cleared. The POST pulse also sets flip-flop IC30, informing the CPU at P1-6 that the speed counter is ready to be read by the processor. The CPU then supplies READ6/ true to monitor the count, resetting IC30 and IC49.

A repositioning counter is used to identify the precise starting point of a high speed repositioning cycle. The counter consists of three 4-bit up/down counters in succession, ICs 121, 122 and 123 (see 5426 schematic, page 6-B3). The repositioning counter is clocked by POSTS and counts UP when the tape is moving forward and DOWN when the tape is moving in reverse. Recall that the repositioning cycle starts when a command is not received during the command reinstruct time at the end of a block. Whenever Data Detect goes low at the end of the block the output of IC97-11 goes low, setting IC32-6 low. The pulse generating network consisting of ICs 102-12, 102-15, 124 and 100 supplies a loading pulse one CLK1 wide to load the repositioning counter with all 0s. If repositioning is initiated during an erased segment of tape the loading pulse is generated by Data Busy DBY going false and that point would be identified as the starting point of the repositioning cycle. Once a repositioning cycle is started the tape ramps down to a stop while the counter is counting UP the number of elapsed POSTS. The tape then reverses direction and ramps backwards as the counter counts DOWN. When the counter returns to all 0s it outputs ZERO high to the microcomputer, indicating it has reached the starting point of the repositioning cycle.

The POST pulse is also used to clock the tape length counter. The counter is a 21 bit counter, whose least significant 5 bits consist of IC68 and IC54 (5426 schematic, page 1-D1). The remaining 16 bits of the up/down counter are internal to the processor. Each POST count is equivalent to 3/160 inches of tape, or 0.48 mm. The length counter is reset at load point or when the processor supplies DISABLE/ true, disabling the servos.

Using the tape position and reel size information as inertia indicators the microprocessor adds a friction constant, calculates the amount of current required to power the takeup reel to the desired speed and supplies the information to DAC0 (IC86, page 2-D3). Using the actual speed information the processor then supplies the output to DAC1 (IC72, page 3-B1). The analog outputs of the two DACs are summed and are supplied to the takeup reel servo. The supply servo responds to information supplied by the tension sensor. During the ramps, however, DAC2 supplies an

extra constant, provided by the processor, to ensure proper acceleration.

Tape tension information is supplied by the Position Sensor Type 5764 board, located beneath the PE Read. The position sensing circuit consists of an oscillator, including comparator IC1, whose frequency varies according to the position of the tension arm, which in turn varies the effective capacitance of the dashpot. The oscillator output is divided by decade counter IC2 and supplied to integrator IC3. The integrator output is averaged by the network consisting of R4, R5 and C8. The DC average is summed with an offset provided by R15, R17, is amplified and output to the Servo/Control board. Potentiometer R9 is adjusted to provide 0v output when the tension arm is centered in its arc.

### 3.2.5 INTERRUPTS

The MPU will be interrupted from its normal program flow whenever a loadpoint or end-of-tape marker is encountered. The Interrupt (INT/) is generated by circuitry that includes ICs 81, 92, 82, 45 and 69 (5426 schematic, page 3-A). If both LP and EOT indicators are activated, it signals broken tape and the MPU disables the servos and sets both reel motor brakes. An interrupt is also generated whenever the ONLINE pushbutton is pressed while the tape unit is selected and tape is loaded. In that case the MPU will output the transport status to the tape controller via buffer IC36 (page 4-C4). Pressing the control panel RESET pushbutton also causes an interrupt, stopping tape motion in the Test Mode and allowing a changing of test function.

### 3.2.6 CONTROLLER INTERFACE

When the tape unit is addressed, on line and selected, IC35 (page 4-C3) is constantly scanned by the MPU, looking for a command from the tape controller. New commands are latched into ICs 73 and 75 by the GO pulse, and are encoded by ROM IC74 (page 4-D3). The encoded commands are placed on the MPU bus by buffer IC35. FBUSY and RWDG are latched by the incoming control command and are subsequently reset by software control.

### 3.2.7 PHASE ENCODED DATA GENERATION

The 5426 board also includes the entire PE data generation circuitry. Write data in the form of logic levels, supplied from the controller interface, is converted into phase encoded data by the PE write circuits, using the crystal generated 2F frequency. The PE formatting circuits generate the writing of the preamble and postamble, and the ID burst on channel P.

During power up, IC93, IC52 and IC44 are pulsed low by MRESET/. This ensures that the syncronous logic in the write circuitry is properly initialized. Signal 2F is twice the write frequency: 40 kHz at 12.5 ips and 320 kHz at 100 ips. The write frequency is available at IC67 pin 8.

Upon reception of a write command the MPU will set DATA and WRITE ENABLE true, thereby putting a low on the S/ input of IC26 pins 2 and 3. The Q output of IC26 will then go high, enabling counters IC94 and IC98 to count up to 40 beginning with the next available clock pulse. At the same time the clear inputs of IC50 and IC52 will go high allowing the transfer of 40 0 characters per channel to the write head drivers.

On the count of 40, IC98 pin 12 will be true, thereby resetting IC26 pin 9. With the arrival of the next clock pulse IC10 pin 8 will go high, thus writing a 1 character on all channels.

The next clock pulse will force IC10 pin 8 low and IC92 pin 8 high. This allows transfer of data from the controller to the PE write electronics by means of the write strobe generated by IC43, IC2 and IC3.

Write parity can be internal or external; this is made possible by IC8 and jumper straps 7 and 8.

When the controller has written the desired amount of data it will issue a signal (LWD/) along with the last byte of data. The write control will then inhibit any further transfer of data by setting the clear inputs of IC40 and IC43 low. A 1 character is then written followed by 40 0s; at which point QD of IC98 will go true and place a low on IC26 pin 4. This results in loading the counters with zero and Q output of IC52 will go false on the next clock pulse, thereby clearing IC50 and IC52 pin 5. This completes the write cycle and the tape unit is now ready for the next command from the controller.

Jumper straps 1 through 6 are provided so that the user may choose which of the three optional channels will be written on during a filemark.

ID burst is written on channel P only. This is performed by IC42, IC25 and IC52.

The network consisting of flip-flop ICs 67, 2 and 43 is used to generate the two write clocks. One clock is used to strobe the write data into the write buffer consisting of ICs 23 and 40. The other is supplied to the controller as Write Strobe WSTR to synchronize the write data transfer to the transport.

Two crystal generated frequencies are used to derive the clocks: F0, a 2.56 MHz frequency used to clock the flip-flops, and F2, a frequency at twice the data rate, varying from 320 KHz for high speed to 40 KHz at low speed. Flip-flop IC67-5 is used to halve the data rate frequency during the ID burst, as required for writing the alternate 1s and 0s. During ID BURST false the 2F frequency is halved only by IC67-9, and the data rate clock is supplied to the 4 D-type flip-flops, each used to shift the clock by a single F0 period. The outputs of the flip-flops are gated through NAND gates IC42-3 and IC3-6 to produce the buffer clock and the Write Strobe, respectively. Note that while the two clocks share the same leading edge the buffer clock is a single F0 period long (0.4 usec) while the Write Strobe is 3 F0 periods long (1.2 usec).

## 3.3 READ AMPLIFICATION STAGES

The read signal output by the head is in the order of 2 to 3 millivolts. It is amplified by a preamplifier stage located on a mini PC board soldered directly to the head, eliminating any noise problems caused by wire leads. The preamp stage amplifies the read signal by a factor of 10 to 15, and the amplified signal is supplied to Read Amplifier type 6470, the lower of the two boards located below the Servo/Control board.

The Read Amplifier board amplifies the signal, peak detects, digitizes it and provides the Data Detect output. The Read Amplifier consists of nine identical channels; consequently only channel 3 will be described (see Read Amplifier type 6470, sheet 1 of 3). The signal from the preamplifier is supplied to an amplifier stage, IC38, whose output at test point 3 is adjusted by potentiometer R6 to 4v peak to peak. FET switch Q1 is used to adjust the gain for high and low speeds. At high speed the output of comparator IC23 swings to +15v, turning Q1 on and reducing the output gain to compensate for the higher head output. The amplifier output is differentiated by the network consisting of C8 and R11 (also R12 in high speed) and supplied to zero crossover detector IC12, providing peak detection for the input signal. The output of the crossover detector is filtered by Schmitt trigger IC4 and associated components, and is output to the PE Read board through connector J1, provided that Channel 3 Data Detect is true. Data Detect is generated by supplying the amplifier stage output to a pair of IC27 comparators. One input of each comparator is tied to a clipping level, normally 10% of the signal level. The clipping levels prevent base line noise from being interpreted as data, generating Data Detect true only when the signal exceeds the clipping levels.

## 3.4 PHASE ENCODED DATA RECOVERY

### 3.4.1 INTRODUCTION

The phase encoded data is located on PE Read type 5326. Phase encoded data is read using a single phase locking oscillator, nine parallel read channels, and a read envelope detection network. The phase locking oscillator tracks one of the data channels and provides the nine read channels with the clock used to synchronize data decoding. The read channels, in addition to decoding the data, deskew the data, detect single track errors and perform single track error correction. The data envelope network monitors the number of valid channels, inhibiting data recovery unless eight of the nine channels contain valid data. These functions are described in the following paragraphs.

### 3.4.2 PHASELOCK LOOP

THE CONCEPT

The phase lock loop generates the DATACLK, a clock at 32 times the input data rate, used to synchronize the data recovery functions. This frequency is derived using a voltage controlled oscillator whose center frequency is 32 times the data rate. The oscillator output is divided by 32 and its phase is compared with the phase of a reference data channel (channel 2 or channel P) during the data and a crystal derived frequency during the gaps. The output of the phase comparator is supplied to an integrating operational amplifier that supplies a corrective voltage to the input of the VCO. If the reference channel and the VCO output are in phase, no change in the corrective voltage will occur at the VCO input. If the VCO output lags the input reference channel, the op amp will provide increased output voltage which will increase the corrective voltage to the VCO until the phase lag is corrected. Similarly, if the VCO output leads the input data, the operational amplifier will reduce the corrective voltage input to the VCO until the oscillator slows down enough to match the input reference phase.

THE DETAILS
(Reference 5326 schematic, sheet 4 of 6)

Voltage Controlled Oscillator and Dividing Network

The main component of the tracking oscillator is the voltage controlled multivibrator IC3. The multivibrator center frequency is selected by capacitor C8 to be 32 times the high speed data rate. The output of IC3 is routed through ECL-TTL conversion network including Q2, and through IC10 NOR gate. In high speed HI/LO/ high passes the VCO output through IC109-5 and IC109-8 to become the DATACLK at 32 times the high speed data rate. In low speed the VCO output is divided by 8 through IC108 and is gated through IC109-3 by LO/HI/ high to become DATACLK at 32 times the low speed data rate. DATACLK is supplied to a dividing network consisting of D flip-flop IC14 and 4 bit counter IC7 in tandem. The frequency is divided by 2 to supply SCLK (16 x data), divided by 8 to supply RCLK (4 x data) and divided by 32 to supply the data rate frequency as one input to the phase comparator at IC9-11.

Reference Frequency Selector

The reference input of the phase comparator accepts one of three reference frequencies, 2F/2, DETP/, or DET2/, depending on the status of the DATA DET and SLT2/ lines. During the interrecord gap Data Detect DATADET, supplied from the control board at pin J1-11, is low, setting the B input of 4 to 1 multiplexed IC80 low, supplying the 2F frequency divided by 2 to the phase comparator.

When DATADET is true, indicating that read data is detected, SLT2/ line selects between DET2/ or DETP/, as the reference frequency. SLT2/ is generated by a flip-flop IC37. When DROP P and DROP 2, supplied from the channel P and channel 2 read channels, are both false, indicating neither channel has been dropped, SLT2/ will be low,

selecting channel 2 as the reference channel to the phase comparator. SLT2/ will go high only if channel 2 has been dropped and channel P is valid, in which case SLT2/ high will select channel P as the reference channel input to the phase comparator.

The Phase Comparator

The phase comparator consists of 2 D flip-flops on IC9, and associated gating. The reference frequency, usually DET2/ during the data block, is supplied to the clock input of the upper IC9 flip-flop. The output of the VCO is divided by 32 and supplied to the clock input of the lower IC9 flip-flop. If the VCO output frequency and the reference channel are in phase, both flip-flops are toggled to the set state simultaneously and are immediately reset following a propagation delay by NAND gate IC8-6.

When both flip-flops are reset, the Q output of the upper flip-flop sets the output of NAND gate IC8-3 high, the Q output of the lower flip-flop sets the output of IC8-8 low. Consequently the voltage divider network including resistors R3, R5, R6 and R4 provides about 6 volts at the summing point of the operational amplifier IC2. The noninverting input is supplied with 6.1 volts by the dividing network including R7, R11 and R12. In this case the output of the op amp supplies minimum current to summing transistor Q1 and no correction voltage change occurs across load resistors R14 and R13.

When the phase of the VCO output leads that of the reference channel, the lower IC9 flip-flop is set first, causing the output of nand gate IC8 to swing high for the duration of the phase delay, supplying 12 volts across the resistors at the inverting input of the op amp. This increases the positive feedback current of the op amp and reduces the output current to summing transistor Q1. As a result, the corrective voltage of the VCO is reduced until the output frequency slows down sufficiently for the phases to match. When the VCO output lags the reference channel, the upper D flip-flop will be set first and the output of NAND gates IC8-3, IC8-8 will be grounded for the duration of the phase delay. This will produce a negative feedback current, increasing the positive output current to summing transistor Q1. As a result the corrective voltage to the VCO will be increased until the VCO frequency speeds up sufficiently for the phases to match.

### 3.4.3 DROPOUT RESYNCHRONIZATION

THE CONCEPT

Either channel P or channel 2 are used as the reference channels for the tracking oscillator. Should a dropout occur in the reference channel, tracking is automatically switched to the alternate channel. Since a phase difference may exist between the tracking channel and its alternate due to skew, there may be a gap during the switching which could be interpreted by the phase comparator as a drastic slow down or speed up of data, and synchronization could be lost during the attempted correction. This condition is averted by a detection network that preloads the data counter during the switchover in reference channels, maintaining synchronization of tracking.

THE DETAILS
(reference schematic 5326, sheet 4 of 6)

DROP P and DROP 2 are connected to a flip-flop consisting of two segments of IC37. Normally, when both channels are read properly, the flip-flop output at IC37-10 would be low, generating SLT2/ true. SLT2/, supplied to multiplexer IC18, causes channel 2 data to be input to the tracking oscillator network. When a dropout occurs on channel 2, DROP 2 high clears flip-flop IC37 generating SLT2/ high. For one DATACLK period the inputs to exclusive OR gate IC17 would be opposite in polarity, generating a positive pulse. This pulse, indicating a switch over in tracking channels, clocks J-K flip-flop IC19 to the set state. The Q/ output of the flip-flop preloads the tracking oscillator dividing network (IC7, IC14) to maximum count minus one. The switchover pulse output by IC17-11 is also gated through IC5-8, IC109-11 (provided LOCK/ is false) and clears the phase-comparator flip-flops IC9, preventing excessive correction voltage from drastically altering the tracking oscillator frequency.

### 3.4.4 DATA DECODING, DESKEWING AND SINGLE TRACK ERROR DETECTION

Read data from the transport read amplifiers is supplied to nine parallel decoding channels, each consisting of a latch, a ROM, and a state counter. Using the counter outputs, the ROM distinguishes between data transitions and interphase transitions, and determines whether the data transitions occur within the required time frame. The ROM supplies three latched outputs: Shift In (SI), Error in Channel (EIN), and Transition Detect (TDET). SI is used to shift the data and EIN into the deskew register. EIN is also supplied to plurality check circuitry used to generate the data envelope. TDET is used to reset the state counter after each data transition.

The deskew register of each channel consists of a First In First Out (FIFO) register and associated logic. Data from the decoding latch and EIN, the latched error indication from the ROM, are entered into the parallel input of the deskew register each time the ROM supplies SI true. SI is generated only for actual data transitions, not for interphase transitions. When a data bit is shifted into the input of the deskew register, it bubbles to the register output. At the beginning of the preamble data is stored at the output of the deskew registers until all channels have a character at the output of the respective registers. At this point the Output Ready (OR) signals of all nine deskew registers become true and a Read Clock pulse (RDCLK) is generated to shift the data out of the registers. The all 1 character at the end of the preamble is used to align the data.

This is accomplished by delaying the Shift Out pulse of a channel that contains a 1 bit at the deskew register output until all channels contain a 1 bit at their outputs. At this time Shift Out is generated to shift the deskewed data of all nine channels to eight bit delay registers, used for postamble recognition. After eight clock periods the data is output to the interface, accompanied by a Read Data Strobe.

THE DETAILS
(schematic 5326 sheet 6 of 6)

Read Decoding and Error Detection

Since the nine decoding and deskewing networks are practically identical, only channel P will be described in detail. It will remain to the reader to translate IC reference numbers to the particular channel examined.

The PE decoding network consists of a hex D flip-flop latch (IC28), a ROM (IC29) and a six bit counter (IC30, IC31). Channel P read data is supplied from the read amplifiers at pin J1-12, is inverted (twice in read reverse mode) and is supplied to one latch input. One DATACLK pulse later (DATACLK is 32 x data rate) the read data is supplied to a ROM address input and is supplied to another latch input. The second latch supplies the data to another ROM address following a 1 DATACLK delay. The outputs of the two latches will be in the same state when no transition has occurred, and will be in the opposite state for 1 DATACLK period following each transition. The counter, also clocked by DATACLK, supplies the ROM with the count reference necessary to identify the time of occurrence of each data transition. This is accomplished by dividing each character frame into six states. Five states are a quarter of a character frame wide, and the sixth is one DATACLK period wide. When a transition occurs, the ROM identifies the transition as either valid data, an interphase transition, or an error transition, according to the time of its occurrence. Interphase transitions occur in states 2 and 3, between 25% or 75% of the character frame. Error transitions are defined as transitions occurring too early (during state one, within 25% of a character frame since the last data transition), or too late (when no transition has occurred within 125% of a character frame since the last data transition). Valid data transitions occur in state 4 and 5, between 75% and 125% of the frame. Another ROM input is the LOCK signal. LOCK stays true during gaps and during the initial portion of the preamble and goes false once eight valid preamble characters have been detected. During LOCK true the ROM identifies only zeros (negative going transitions) as data, and ones as interphase transitions. Thus the ROM locks into the data during LOCK true. During LOCK true no data is shifted into the deskew shift registers. The ROM provides three latched outputs:

a. Transition Detected TDET, used to reset the counter to count one following each data transition.

b. Error in Channel EIN, generated when an error has been detected.

c. Shift In SI, generated when a data character and a possible error indication are to be shifted into the deskew shift register.

Note that Transition Detected is used only to reset the counter after each data transition (not after interphase transitions). The latched ROM error output EIN is supplied from all channels to plurality detection circuitry that develops the data envelope.

The Deskew Register

The deskew register of channel P consists of FIFO IC32 and related logic. When the ROM generates a Shift In SI input, the read data from the decoding latch and a possible error indication EIN are shifted in parallel into the first register location. Once a bit is input into the register it will bubble to the output of the register and remain there until it is shifted out by a Shift Out SO signal from deskew control flip-flop IC33-5. When a data bit is present at the output of the FIFO, its Output Ready (OR) signal will become true. OR buffered by IC34-12 is supplied as Ready RDY. The RDY outputs of all nine FIFOs are wire ANDed, and consequently will stay low until all channels contain data at the output of their shift registers. When data is available on all channels, RDY will become true and a Read Clock (RDCLK) pulse will be generated. RDCLK will toggle the deskew control flip-flop of each channel simultaneously, shifting the data bit from the output of the deskew register. Actual data deskewing is accomplished by using the all 1 character at the end of the preamble. When channel P, for instance, detects its first 1 bit, the output of NAND gate IC45-12 will go low, inhibiting any RDCLK pulses from toggling the deskew control flip-flop IC33-5. The 1 bit will be stored at the output of the deskew shift register until the outputs of all nine channels contain 1 bits. At this time ENSYNC signal will go low, setting the output of NAND gate IC45-12 high again, and allowing the deskew control flip-flop to generate a Shift Out signal on the next RDCLK pulse. The deskewed data will then be shifted simultaneously from the FIFO outputs.

Data from the Q2 output of the FIFO is supplied to the D input of data flip-flop IC33-12. A zero bit will cause the flip-flop to toggle to the clear state, a 1 bit will cause the flip-flop to toggle to the set state whenever a Shift Out SO is generated by the deskew control flip-flop. The Q output of the flip-flop supplies the data to the delay register described below. It is also buffered by IC34-8 and is supplied as Detect 1 DET1. The Q/ output of the flip-flop is buffered and supplied as Detect 0 DET0. The DET1 outputs of all deskew registers are wire ANDed, as are the DET0 of all deskew registers. These signals are used in detecting the preamble and postambles.

When an erroneous data character is shifted to the output of the deskew shift register, the Q0 output of

the register goes high, is inverted by IC44-10 and sets both the Q and Q/ outputs of data flip-flop IC33-9 high. This is done to prevent a single track error from disrupting the synchronization process.

The Delay Register

The delay register of channel P consists of 8 bit shift register IC35. Data is input into the register from the Q output of data flip-flop IC33, and is clocked through by Read Clock RDCLK. The inverted data is output to the interface after eight clock counts at pin J3-10. Since the data supplied to the interface is delayed by eight count, it is also necessary to delay the Read Data Strobe by a similar count. This delay is provided to allow the postamble detection network sufficient time to recognize the postamble.

### 3.4.5 DATA READY GENERATION

THE CONCEPT

Data ready DRDY and Clear Data Ready CLRDRDY define the beginning and the end of actual read data, distinguishing the read data from the preamble and postamble. Data Ready DRDY goes true following the all 1 character at the end of the preamble, staying true until Read Enable RDEN goes low at the end of the block. Clear Data Ready CLRDRDY goes true after the detection of the all 1 character at the beginning of the postamble, and remains true until RDEN goes low. Data Ready DRDY true enables Read Strobe generation. The Read Strobe is terminated when Clear Data Ready CLRDRDY goes true. Consequently the Read Strobe is generated during valid data only and is inhibited during the preamble and the postamble. Enable Sync ENSYNC is another signal generated by the same network. ENSYNC goes true after eight preamble zeros have been detected and goes low on the all 1 character at the end of the preamble. ENSYNC is supplied to the deskew register network where it is used to delay the data at the output of the deskew registers until all channels contain a 1 bit at their outputs.

THE DETAILS
(reference sheet 6 of 6)

During the preamble of 40 zeros XDET0, the wire ANDed DET0 outputs of all the read stages, goes high. XDET0 is supplied to the input of eight bit shift register IC64, used as a zero counter. The counter is clocked by Read Clock RDCLK at the data rate and is reset each time XDET0 goes low, indicating a non zero character. After eight consecutive preamble zeros are read, the QH output of the zero counter IC64 will go high. QH high will activate NAND gate IC55-8 and set flip-flops IC36-4 and IC36-7. The latter flip-flop will generate ENSYNC high. Flip-flop IC36-4 will enable one input of NAND gate IC55-2. The gate will be activated when DET1 goes high during the all 1 character at the end of the preamble. The low output of this gate will reset ENSYNC low and will set flip-flop IC36-13, generating Data Ready DRDY true. Thus DRDY goes true after the last character of the preamble. DRDY true enables Read Strobe Delay counter IC35 initiating Read Strobe generation. DRDY will go false when Read Enable RDEN goes low at the end of the block.

The all 1 character marking the beginning of the postamble will generate DET1 true, activating OR gate IC46-8 and resetting zero counter IC64. The postamble zeros will then generate DET0 true and the zero counter will start counting. When seven consecutive postamble zeros have been counted the QG output of the zero counter will go high and NAND gate IC55-6 will be activated, setting flip-flop IC36-9. The Q output of the flip-flop will then generate Clear Data Ready CLRDRDY true. CLRDRDY is inverted and resets flip-flop IC21-13, which clears the Read Strobe timing counter IC20, inhibiting the Read Data Strobe.

### 3.4.6 READ CLOCK, READ STROBE GENERATION

THE CONCEPT

Read Clock RDCLK is the internal read clock supplied to the deskew and delay registers to shift out the data. It is also used in the preamble detection and error detection networks. A RDCLK pulse is generated each time a bit is available at the output of the nine deskew registers, indicated by RDY true.

Read Strobe RSTR is the read clock supplied to the interface. In essence it is a modified version of RDCLK. RSTR is delayed eight character counts to match the data delay. Its duration is precisely determined by a timing register according to tape speed, and it is suppressed during the preamble and the postamble.

THE DETAILS
(Schematic 5326, sheet 6 of 6)

RDY, the wire ANDed Output Ready Indications of the nine deskew registers, goes true whenever a byte is ready to be shifted out. RDY is gated through AND gate IC46-11, clocked through IC47-15 by DATACLK (32 x data rate) and presented to the J input of flip-flop IC19-1. This flip-flop is clocked by RCLK, a frequency at four times the data rate, supplied by the tracking oscillator network. Each time RDY goes true IC19 flip-flop is set by the next RCLK. The flip-flop is cleared by the following RCLK and remains cleared until RDY goes true again. Thus the flip-flop provides a pulse a quarter of a character in duration each time a byte is ready to be shifted out of the skew registers. The Q/ output of the flip-flop is inverted by IC13-11 and is supplied as RDCLK to the internal read circuits, to shift data out of the skew and delay registers of each channel.

Shift register IC35, in conjunction with flip-flop IC21, is used to provide an eight character delay for RDCLK to match the data delay. The register is enabled by DRDY true at the beginning of valid data (not preamble). After the eight count delay flip-flop IC21 presents a high input to shift register IC20, used

to determine read strobe duration. IC20 is clocked by SCLK, a crystal derived frequency at 16 x the data rate. Three SCLK pulses after IC20 is enabled its QC output goes high, initiating RSTR at output pin J3-8. In low speed operation RSTR is terminated after two SCLK pulses by QE high, which clears flip-flop IC21-13, which in turn clears IC20. The resultant RSTR pulses are approximately 6 usec long. In high speed operation RSTR terminates after five pulses (QH going high), generating RSTR approximately 1.8 usec long. CLRDRDY/ resets flip-flop IC21-13 through NOR gate IC24-12 when the postamble is detected, inhibiting RSTR/. CLRDY/ also inhibits RSTR when a file mark is detected.

### 3.4.7 HARD AND CORRECTABLE ERROR DETECTION AND FILE MARK DETECTION

THE CONCEPT

The error indications output by the read stage ROMs, EINP through EIN7, are supplied to a plurality network that determines, in case of an error, whether it is a single track error or a multiple track error. If it is a single track error, the output of a parity generator is supplied as Parity Correct PARCOR to the erroneous channel, to be substituted for the erroneous data, and a Correctable Error CER indication is supplied to the interface. If it is a multiple channel error, Hard Error HER is supplied to the interface, and the error cannot be corrected.

The output of the plurality network is also used to generate the LOCK signal. LOCK is set true at the beginning of a read operation, allowing the read channels to lock onto data transitions at the beginning of the preamble. After eight valid preamble characters have been detected, as indicated by the plurality network, LOCK is reset, since synchronization with data transitions has been established.

The plurality network is also used to detect the file mark. The file mark is detected when channels 2, 6 and 7 contain zeros while the remaining channels are quiescent.

THE DETAILS
(reference sheet 4 of 6)

The error indication outputs of each read stage are supplied to a plurality network consisting of ROM IC22 and associated gating. EIN0, EIN1 and EIN3 through 7 are supplied to the ROM inputs. EINP and EIN2 are supplied to a gating network which complements the ROM functions. If a maximum of one error is detected, the output of NOR gate IC5-6 goes high, indicating that at least eight channels are valid, thus signifying the beginning of the data envelope. This enables LOCK counter IC6. The counter is clocked by the data rate frequency supplied from the tracking oscillator network. After eight valid characters are detected, the QH output of the counter goes high and sets the flip-flop consisting of the two IC15 NOR gates, generating LOCK false. No error indications are generated until LOCK goes false, since LOCK false defines the completion of data synchronization. LOCK/ is supplied to one input of NAND gate IC24-6. The gate is activated during the block when the plurality network indicates a multiple channel error, setting the output of NOR gate IC5-6 low. The output of IC5-6 is inverted by IC56-8 and activates IC24-6, generating Hard Error HERR true. HERR true is one source of the hard error indication. It is gated through OR gate IC4-11 and inverter IC26-3 to supply HER true to the interface at pin J3-6. Another source of hard errors is supplied from parity check IC23 when even parity is detected. In that case the output of IC23-5 goes high and is clocked through counter IC25. Following an eight character delay, matching the output data delay, the 1Q7 output of the counter goes high to activate OR gate IC4-11, again supplying HER true to the interface. When the plurality circuitry detects an error and HERR is false, indicating that only one channel is in error, NAND gate IC15-13 is activated, its output going high. The output of the gate is supplied to delay counter IC25, forcing the 1Q7 output of the counter low (disabling the hard error indication). Following an eight character count the 2Q7 output of the counter goes high, supplying a Correctable Error CER indication to the interface at pin J3-4. During a correctable error the output of parity tree IC23 is inverted by IC13-3 and is supplied as Parity Correct PARCOR to the read stage of the erroneous channel, replacing the wrong data of channel with parity derived from the other eight channels.

A file mark is detected when a burst of zeros is read on channels 2, 6 and 7 and no data is recorded on the other channels. In this case the IC22-11 output of the plurality ROM goes high. This output activates AND gate IC24-8 if DET0 is true, DET1 is false, indicating that only zeros are being read on channels 2, 6 and 7. The output of IC24-8 then goes high, activating IC110-3 in low speed, IC110-6 in high speed, to supply FMRDET true to the interface at J3-2, and FMKPE true at J2-15 to the microprocessor.

# SECTION IV

# MAINTENANCE INSTRUCTIONS

## 4.1 GENERAL

Kennedy Company tape transports are highly reliable precision instruments that will provide years of trouble-free performance when properly maintained. A planned program of routine inspection and maintenance is essential for optimum performance and reliability. The units require very few adjustments and these should not be performed unless there is strong reason to believe they are required. All electrical adjustments are preset at the factory and should not require readjustment except after long periods of use.

## 4.2 PREVENTIVE MAINTENANCE

To assure continuing trouble-free operation a preventive maintenance schedule should be kept. The items involved are few and simple but very important to proper tape transport operation. The frequency of performance will vary somewhat with the environment and degree of use of the transport so a rigid schedule applying to all machines is difficult to define. The recommended periods below apply to units in constant operation in ordinary environments. They should be modified if experience shows other periods are more suitable.

### 4.2.1 DAILY CHECK

Visually check the machine for cleanliness and obvious misadjustment. If items in the tape path show evidence of dirt or oxide accumulation, clean thoroughly.

### 4.2.2 CLEANING

All items in the tape path must be kept scrupulously clean. This is particularly true of the head and guides. The inside of the dust cover must not be allowed to accumulate dirt since transfer to the tape will cause malfunction.

In cleaning it is important to be thorough yet gentle and to avoid certain dangerous practices.

#### 4.2.2.1 Head Cleaning

Oxide or dirt accumulations on the head surfaces are removed using a mild organic solvent and a swab. Q tips are convenient for this but must be used with caution. Be sure the wooden portion does not contact head surfaces. Access to the head is gained by lifting the head shield, as shown in figure 4-1.

An ideal solvent is 1.1.1 trichlorothane contained in the Kennedy K21 maintenance kit. However, others, such as isopropyl alcohol, will do.

**DO NOT USE**

acetone or lacquer
aerosol spray cans
rubbing alcohol

Do not use an excess of any solvent, and be extremely careful not to allow solvent to penetrate ball bearings of tension rollers, capstan, etc., since it will destroy their lubrication.

#### 4.2.2.2 Tape Path Cleaning

Other items in the tape path should be cleaned at the same time as the magnetic head. These include:

tension roller
tape guides
capstan roller

The techniques are similar to those outlined above for head cleaning.

#### 4.2.2.3 Other Cleaning

Use a vacuum cleaner to remove accumulations of dust inside the dust cover or elsewhere in the unit. Compressed air may be used if caution is exercised to avoid blowing dirt into bearings. Antistatic cleaners are available for cleaning the plexiglass dust cover window.

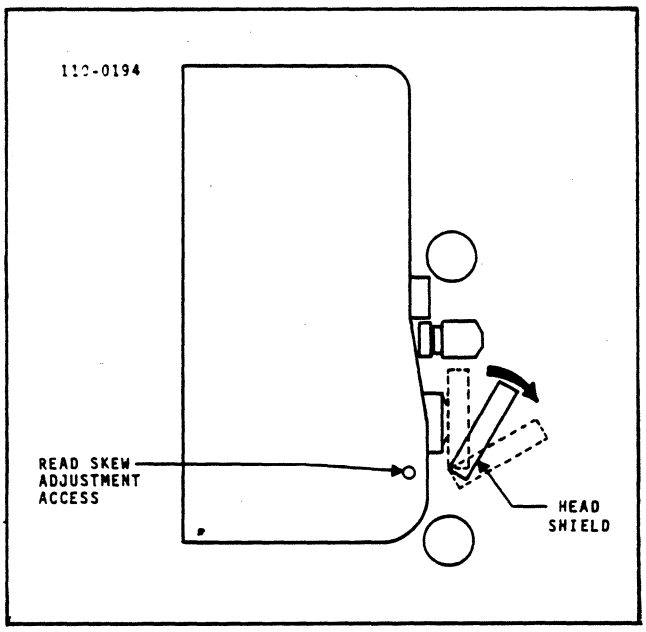



***Figure 4-1.***

***Opening Head Shield***

4.2.3 VISUAL CHECK

Check visually to determine if all appears to be right with the machine. It is helpful to run tape forward and reverse observing smooth tape motion, proper tension arm operation, etc. It is well to remember that if things look right they probably are right, and the converse.

## 4.3 ROUTINE ADJUSTMENT

There are no routine adjustments. Need for adjustment will be manifest if malfunction occurs. Under normal circumstances adjustment will be more likely to cause trouble than prevent it.

## 4.4 LUBRICATION

No bearing lubrication is required. All bearings are lubricated for life and introduction of oil may destroy their lubrication.

## 4.5 WEAR

Magnetic tape is an abrasive and in time wear will be noted on items over which the oxide surface slides.

4.5.1 HEAD WEAR

The ceramic coated head used in Kennedy Company machines should last the lifetime of the machine. It should not require replacement under normal operating conditions. Head wear is generally indicated by an increase in error rate. Confirmation is a sizable increase in output voltage as measured at the read amplifier.

4.5.2 GUIDE WEAR

Guides wear principally at the point of contact with the front guide surface. Since guides are symmetrical it is only necessary to loosen the guide mounting screw, rotate the guide, and tighten to present an unworn surface to the tape.

4.5.3 REEL HUB WEAR

Quick release hubs are adjustable to assure a firm clamping action. They are designed to make it impossible to mount a reel in a wrong or cocked position. If the locking action should become weak, the hub may be adjusted as described in paragraph 4.12. O ring clamps used in the hub may tend to hang up after long periods of use. This can be corrected as follows.

a. Remove O ring from hub.

b. Clean thoroughly with mild solvent.

c. Lubricate ring with silicone grease. Wipe off thoroughly, leaving a light lubricating film.

d. Snap O ring back in place.

## 4.6 PERIODIC INSPECTION

At regular intervals, approximately every two months, it is advisable to make a more thorough check of machine operating parameters. This will ensure that no progressive degradation will go unnoticed.

The Test Mode, accessed through the main control panel, facilitates these checks, allowing control of tape motion off line. Using the Test Mode or other appropriate means, check the following periodically:

DAC calibration
optical encoder phase
tension sensor calibration
read level
skew

Procedures for checking these and other items are given in this section, and a suggested sequence of adjustments is shown in table 4-1.

## 4.7 TEST MODE

In the Test Mode the Model 6809 can be tested and exercised while off line, saving valuable computer time and facilitating any adjustment or test procedure required. The Test Mode is accessed through the multipurpose, main control panel. Note that in the Test Mode only the RED pushbutton designations on the control panel apply. Two functions are available in the Test Mode: CALDAC, the DAC calibration function used while adjusting the servo controlling D/A converters, and the RUN function, used to exercise the tape deck in high or low speeds, in forward or reverse directions. To enter the Test Mode perform the following steps:

a. To enter Test Mode thread the tape and press pushbutton A. TEST MODE indicator will start blinking.

b. To enter RUN mode press pushbutton A again. Tape will advance to load point and stop. The desired test may then be selected as tabulated below:

| TEST | PUSHBUTTON SEQUENCE |
|---|---|
| Low speed forward | AC |
| Low speed reverse | AA |
| High speed forward | CC |
| High speed reverse | CA |

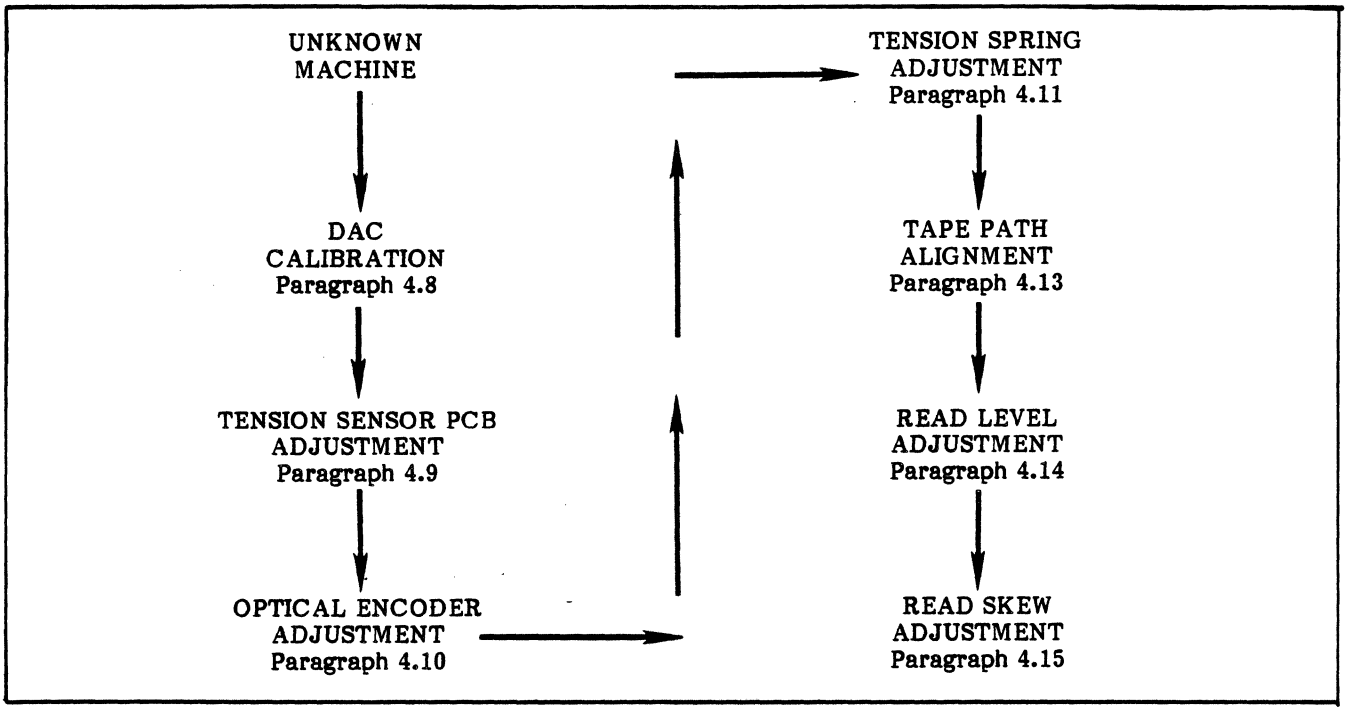



**Table 4-1**
**Adjustment Sequence**

Pressing pushbutton D once will terminate the selected test and exit the RUN mode. To select another test press pushbutton A to reenter RUN, then the pushbutton sequence tabulated above. Pressing pushbutton D twice will exit the Test Mode. The transport will respond by performing a load sequence and will then be ready to perform normal streaming operations.

c. To enter CALDAC enter Test Mode as described in step a and press pushbutton C. To load tape following CALDAC press the LOAD pushbutton.

## 4.8 DIGITAL TO ANALOG CONVERTER ADJUSTMENT PROCEDURE

Three D/A converters are used in the Model 6809 to convert the microprocessor output to servo driving signals. Should any misfunction occur in the servo system, follow the adjustment procedure outlined below.

Required equipment: digital voltmeter

a. Enter the CALDAC mode by first entering the Test Mode (see paragraph 4.7) then pressing pushbutton C (red letter designation).

b. Using the digital voltmeter, monitor pin 18 of each DAC (ICs 58, 72, and 86, type NE5018) and adjust its associated potentiometer (R100, R90, R98, respectively) until the output voltage measures +10v.

c. Exit the CALDAC mode by pressing pushbutton D.

## 4.9 TENSION SENSOR ADJUSTMENT PROCEDURE

The tape tension sensing electronics are located on Tape Tension Sensor PC board Type 5764, the small PC board bearing the servo damper. Should the tension arm not be centered during tape motion, or should it bottom out during the ramps, perform the following adjustment procedures on the Tape Tension Sensor.

Required equipment: voltmeter

a. Adjust tension assembly mounting bracket so that, with the piston in the extreme extended position, approximately 1/32" of the piston overlaps the copper wrap on the glass tube.

b. With the power ON, but with tape not threaded, connect voltmeter to test point A of Position Sensor Type 5764.

c. Adjust potentiometer R9 so that the voltage output at TPA measures 0v when the tension arm is centered in its arc.

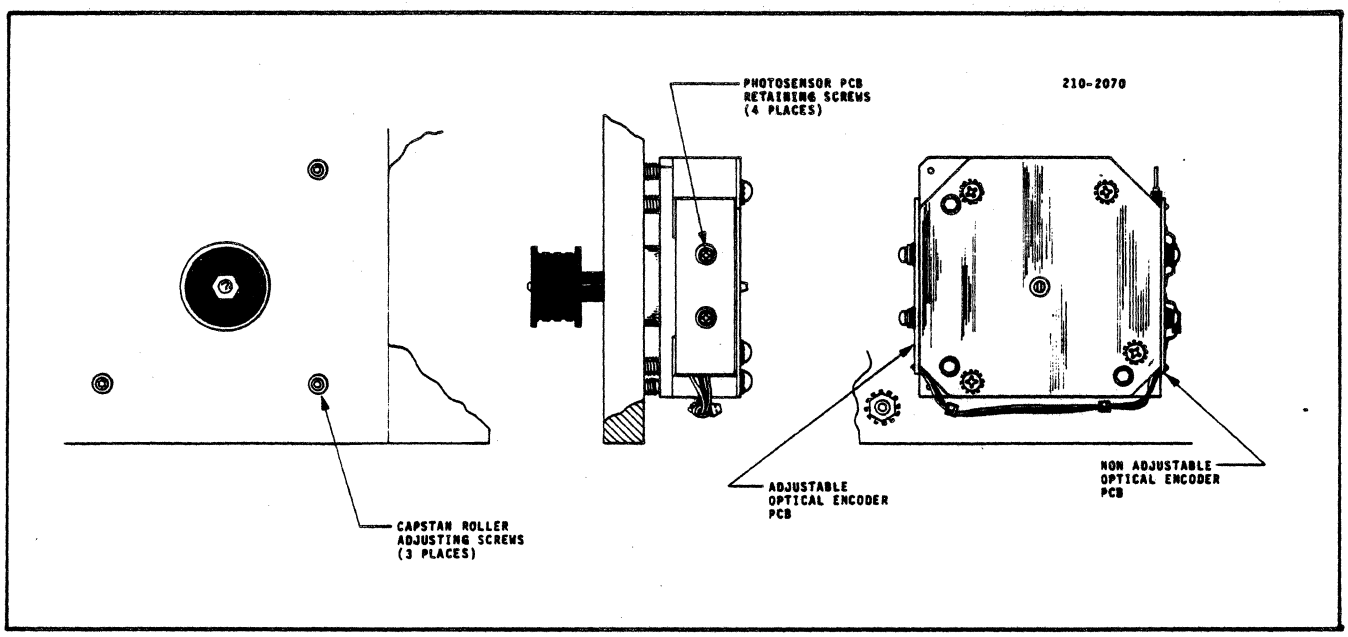



***Figure 4-2.***

***Capstan Assembly***

## 4.10 OPTICAL ENCODER ADJUSTMENT

The optical encoder provides the microprocessor with tape speed information. The encoding is accomplished by photo-transistors located on two small PC boards mounted on either side of the capstan assembly, as shown in figure 4-2. To adjust the encoder circuitry follow the procedure outlined below.

Required equipment: oscilloscope

a. Set the oscilloscope to 0.5 ms time base, 2v/division for both channels 1 and 2.

b. Initiate slow forward tape motion.

c. Adjust potentiometers R145 and R146 on Servo/Control Type 5426 PC board so that the waveforms at IC113-14 and IC113-8 measure 7.4v peak-to-peak on the oscilloscope.

d. Connect channel 1 probe to TP11 and channel 2 to TP12 on the Servo/Control board.

e. Loosen the retaining screws of the adjustable optical encoder PC board, shown in figure 4-2.

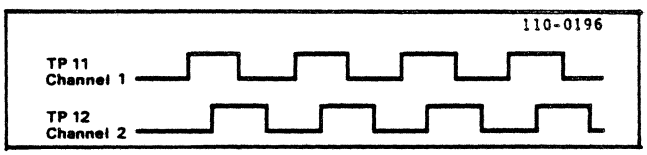



***Figure 4-3.***

***Optical Encoder Output***

f. Move the adjustable PC board in the vertical direction until quadrature is obtained (90 degree phase shift in the squarewave) between channels 1 and 2, as shown in figure 4-3. Retighten the PC board retaining screws. Verify that flip-flop IC112-9 output is LOW during FORWARD tape motion, HIGH in REVERSE tape motion.

## 4.11 TENSION ARM SPRING ADJUSTMENT PROCEDURE

1. Remove the nut securing dashpot cylinder to tension arm, as shown in figure 4-4. Loosen and remove Tape Tension PC board retaining screws, then remove entire tape tension sensing assembly, slipping the dashpot cylinder rod block off the tension arm shaft. Once the assembly is removed do not separate the cylinder from its glass tube, as each cylinder is made for a particular tube.

2. Load a full reel of tape onto the supply reel, and attach an 8 oz weight to the end of the tape. Next, place the tape over the tension arm roller, letting the weight hang a few inches below the roller, as shown in figure 4-5.

3. Loosen the spring locknut, shown in figure 4-4, and rotate the adjustment nut, shown in the same figure, until tension arm is centered in its arc. Make sure that the arm is not restrained by tape friction from moving freely by tapping lightly on the arm to loosen it.

4. Once the arm is centered in its arc tighten locknut securely.

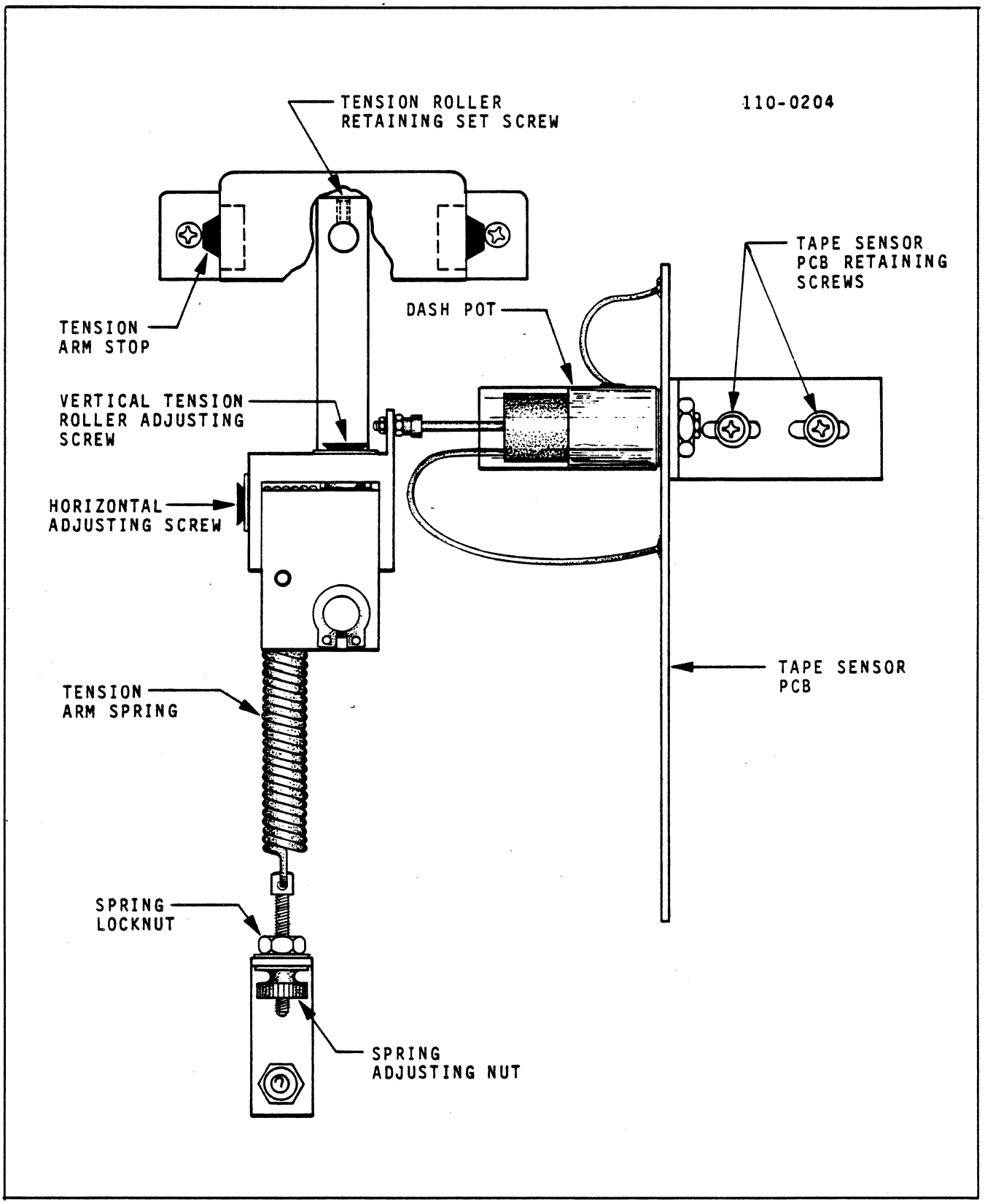



***Figure 4-4.***

***Tension Assembly***

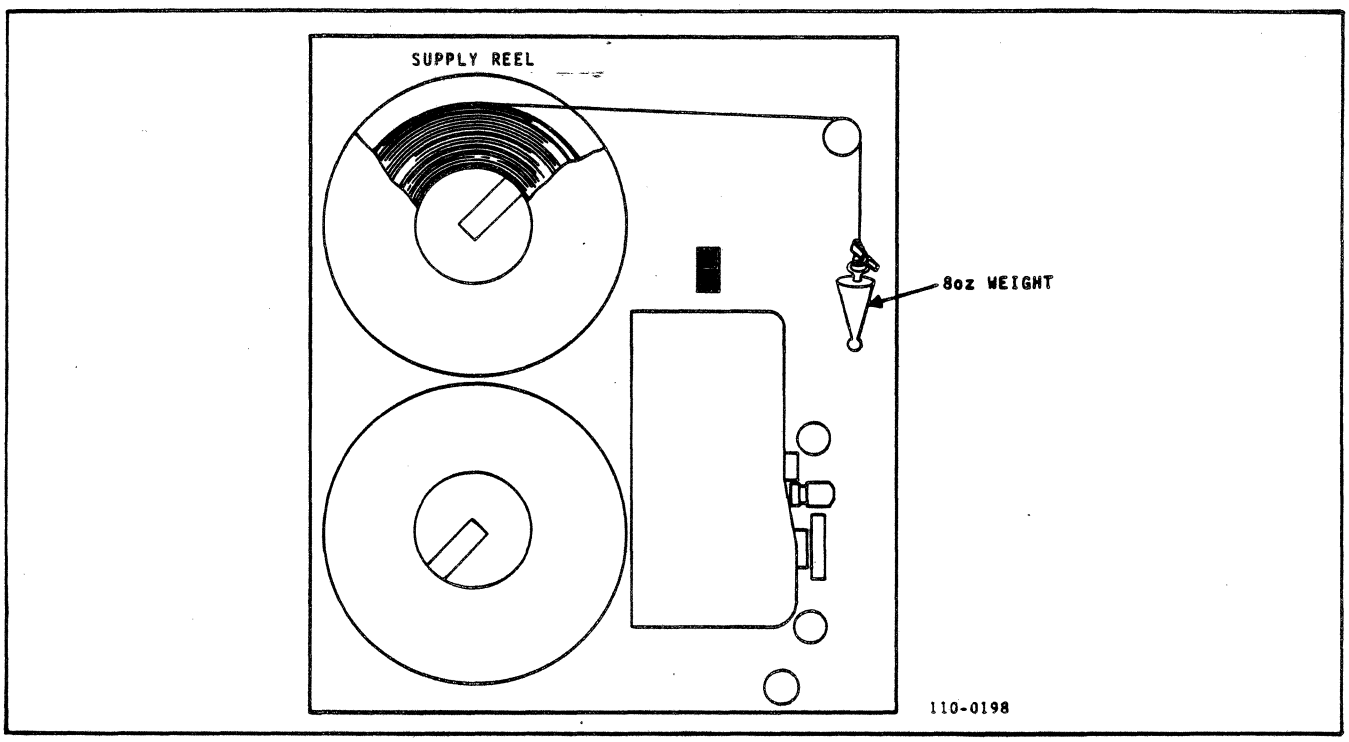



***Figure 4-5.***

***Spring Adjustment Set-up***

5. Replace tension sensing assembly by slipping dashpot cylinder block over the tension arm shaft and securing it with the truarc, then replace the PC board retaining screws. Do not tighten retaining screws initially, but swing tension arm back and forth in its arc, allowing the assembly to self-align. Ascertain that tension arm is stopped at the end of its swing without touching the dashpot glass tube. Adjust the tension assembly mounting bracket so that with the piston fully extended, approximately 1/32" of the piston overlaps the copper wrap of the tube. Secure retaining screws.

**NOTE**

This adjustment is designed to compensate for minor variations in spring tension only. Significant changes in spring tension, caused by prolonged wear, require the replacement of the spring.

## 4.12 HUB ALIGNMENT

4.12.1 HUB O RING ADJUSTMENT

Object: to lock tape reel firmly to the hub.

If the tape reel is loose with hub locked, check the condition of the neoprene O ring.

This O ring expands when the locking latch is depressed to secure reel to hub. If the O ring is not worn, but the reel won't seat firmly:

a. Loosen hub setscrew (see figure 4-6) until the inner hub rotates freely.

b. With the hub latch up, rotate inner hub clockwise while restraining the outer hub. This will exert more pressure on the O ring when the latch is depressed.

c. Place reel on hub and lock latch to determine whether more or less tightening is required.

**NOTE**

There are several holes in the bottom of the outer hub to accommodate the hub setscrew. Therefore, after adjustment is corrected, the hub must be turned slightly until the setscrew fits into one of these holes.

d. After the correct setting is found, retighten the hub setscrew.

4.12.2 O RING REPLACEMENT

a. Loosen setscrew until inner hub turns freely.

b. Unscrew inner hub from hub assembly.

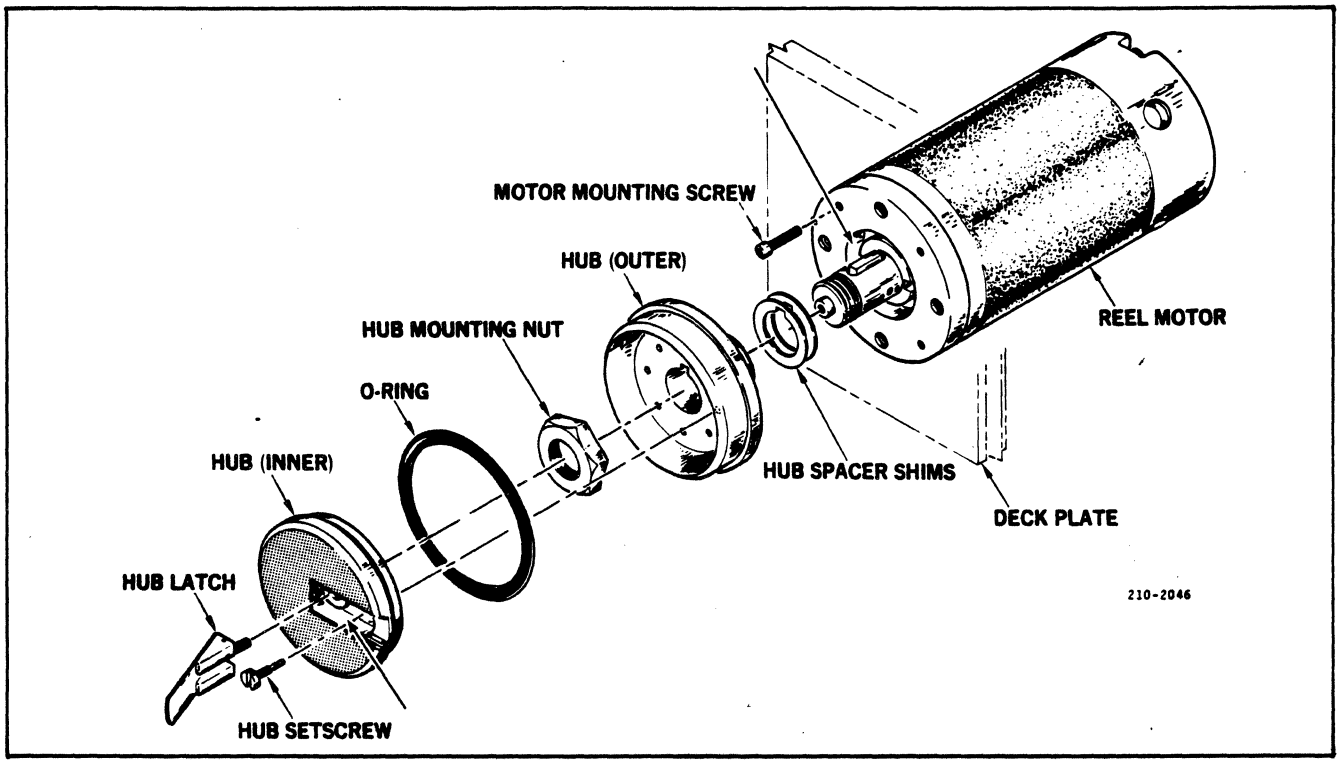



***Figure 4-6.***
***Hub Assembly***

c. Replace worn O ring with new O ring (Kennedy PN 125-0030-006). Prior to installing the new O ring, lubricate the ring with silicon grease and wipe, leaving a light lubricating film.

d. Replace inner hub and readjust O ring pressure according to paragraph 4.12.1.

## 4.13 TAPE PATH ALIGNMENT PROCEDURE

### 4.13.1 REEL CLEARANCE ADJUSTMENT/ HUB REPLACEMENT

Object: To maintain the proper tape path across the top of the hub reel mounting flange and the unpainted area on the deck plate (see figure 4-7). This measurement should be made with a vernier caliper. A special shim kit, Kennedy PN 198-0100-001 is available for spacing the hub assembly properly. To adjust the hub to deck distance, follow the procedure outlined below.

a. Loosen hub setscrew (see figure 4-6) and unscrew inner hub.

b. Insert special spanner wrench (Kennedy PN 154-0042-001) into setscrew holes to stabilize hub. Then remove the hub mounting nut with a socket wrench. Slide remaining portion of the hub assembly off the motor shaft.

c. Add or remove shims as required to obtain 0.325 inch distance from reel flange to the unpainted portion of the deck plate.

d. Reassemble hub assembly. Tighten nut to 20+/-5 in./lb torque.

### 4.13.2 TENSION AND CAPSTAN ROLLERS ALIGNMENT PROCEDURE

The tape path is adjusted in the factory and unless there is a very good reason to suspect that it is misaligned, the factory adjustment should not be

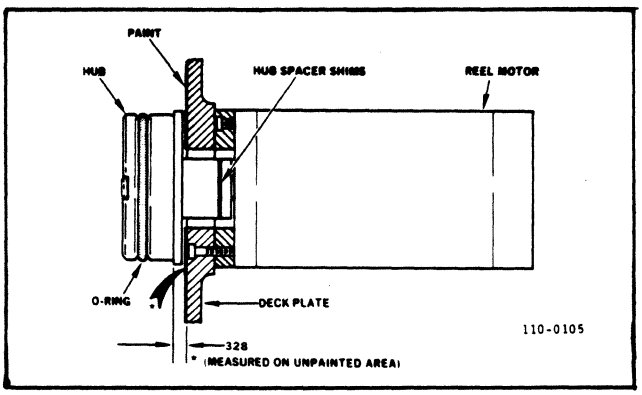



***Figure 4-7.***
***Reel Hub Assembly***

altered. It is recommended that the entire adjustment procedure be read carefully before any adjustments are attempted.

a. Prior to adjusting the tape path, check the tension arm spring setting, as described in paragraph 4.11.

b. Adjust both the tension and capstan rollers to be perpendicular to the deck plate using a machinist's block or a square. The tension roller is adjusted using an Allen wrench by rotating the vertical and horizontal adjustment screws accessible from the front of the deck, as shown in figure 4-2.

c. Load a reel of scratch tape and enter the Test Mode, as described in paragraph 4.7. Initiate slow forward tape motion.

d. Adjust the tape to deck distance using a tape height gauge (included in a K21 maintenance kit). The tension roller height is adjusted by loosening the roller retaining set screw (shown in figure 4-4) and then pulling or pushing the loosened roller until the tape barely touches the tape gauge. The capstan roller distance is adjusted by rotating all 3 adjustment screws equally.

e. Both the tension and capstan rollers may require further angular adjustment so that the tape rides in the center of both rollers without touching the flanges. Note that when adjusting tape path during FORWARD tape motion the HORIZONTAL adjustment of the TENSION roller, and the VERTICAL adjustment of the CAPSTAN roller have the greatest influence on tape path.

f. Once the tape path is adjusted in the forward direction load the remaining tape onto the takeup reel using the high speed forward command to achieve even tape packing.

g. Initiate slow speed reverse tape motion and adjust the angular roller orientation as necessary to center the tape in the rollers. Note that during REVERSE tape motion the VERTICAL adjustment of the TENSION roller and the HORIZONTAL adjustment of the CAPSTAN roller have the greatest influence on the tape path.

h. Recheck tape height and adjust as necessary, as described in step d.

i. The adjustment of the rollers in one direction will influence the adjustment in the opposite direction of tape motion. Consequently steps e through h may need to be repeated with increasing delicacy until proper tracking is achieved.

**NOTE**

When the tape path is properly aligned depressing the spring loaded side of the tape guides near the head would cause the tape to follow slightly in that direction.

## 4.14 READ GAIN ADJUSTMENT

This adjustment sets the gain of the read preamplifiers. Excessive gain would introduce noise while insufficient gain would cause an increase in dropouts. To set the correct gain levels follow the procedure outlined below.

Required equipment: oscilloscope
small screwdriver

a. Access to the read preamplifier adjusting components is gained by removing the retaining screws of the Servo/Control board, swinging it open and removing the shield located on the lower portion of Read Amplifier type 6470.

b. Mount a reel of tape previously recorded with an all 1's pattern and initiate forward motion at 12.5 ips. If using the Test Mode to initiate tape motion follow the instructions given in paragraph 4.7.

c. Attach the oscilloscope probe to the test point of one channel and adjust the associated potentiometer until the voltage output measures 4v peak to peak. The channels and their respective test points and potentiometers are tabulated below.

| Channel | Test Point | Potentiometer |
|---|---|---|
| 0 | 0 | R151 |
| 1 | 1 | R133 |
| 2 | 2 | R97 |
| 3 | 3 | R5 |
| 4 | 4 | R79 |
| 5 | 5 | R25 |
| 6 | 6 | R61 |
| 7 | 7 | R43 |
| P | P | R115 |

d. To insure that gain switching is functioning properly, reread the tape at high speed and ascertain that the gain is still 4v peak-to-peak for all channels.

e. Replace the amplifier shield and secure the Control/Servo PC board in place.

## 4.15 READ SKEW ADJUSTMENT

In deskewing the read gap the head is mechanically tilted to have its gap at an exact right angle to the tape. This is accomplished using a skewmaster tape (see maintenance tools).

Required equipment: oscilloscope
skewmaster tape

a. Enter the Test Mode, as described in paragraph 4.7.

b. Load skewmaster on transport. Be sure write enable ring is removed from reel.

c. Place channel 1 oscilloscope probe on TP4, and channel 2 probe on TP5 of the Read Amplifier module.

d. Initiate slow speed forward tape motion.

e. Adjust the skew adjustment screw on the head mounting plate (figure 4-1) until the signals from the two channels are in phase.

f. Remove the channel 1 probe and place on TP2, ascertaining that the channels are not one whole character out of phase.

## 4.16 FILE PROTECT MECHANISM ADJUSTMENT PROCEDURE

The file protect mechanism is adjusted in the factory and the adjustment need not be changed under normal circumstances. Should the mechanism need replacement, however, or should a need for adjustment arise due to another circumstance, follow the procedure outlined below.

a. The file protect pin travel between the completely open position and the completely drawn in position should be between 0.25 and 0.28 inch. Should pin travel fall outside these limits, loosen the two solenoid retaining screws, shown in figure 4-8, and adjust the solenoid position until the above travel criteria are met.

b. With the power OFF mount a reel of tape onto the supply reel with a file protect ring installed. Loosen the file protect assembly retaining screws, shown in figure 4-8 and adjust the assembly position so that the file protect pin is pushed in one-eighth inch by the file protect ring.

c. Turn the deck power ON and ascertain that the solenoid has drawn in the file protect pin sufficiently to clear the reel completely. Tighten file protect assembly retaining screws securely.

## 4.17 HEAD SHIELD ADJUSTMENT

A shield is located over the magnetic head surface to reduce write-read crosstalk. Its spacing, determined by a spring stop, is important. The spring stop is adjustable as follows:

a. Loosen stop screw with tape removed from deck.

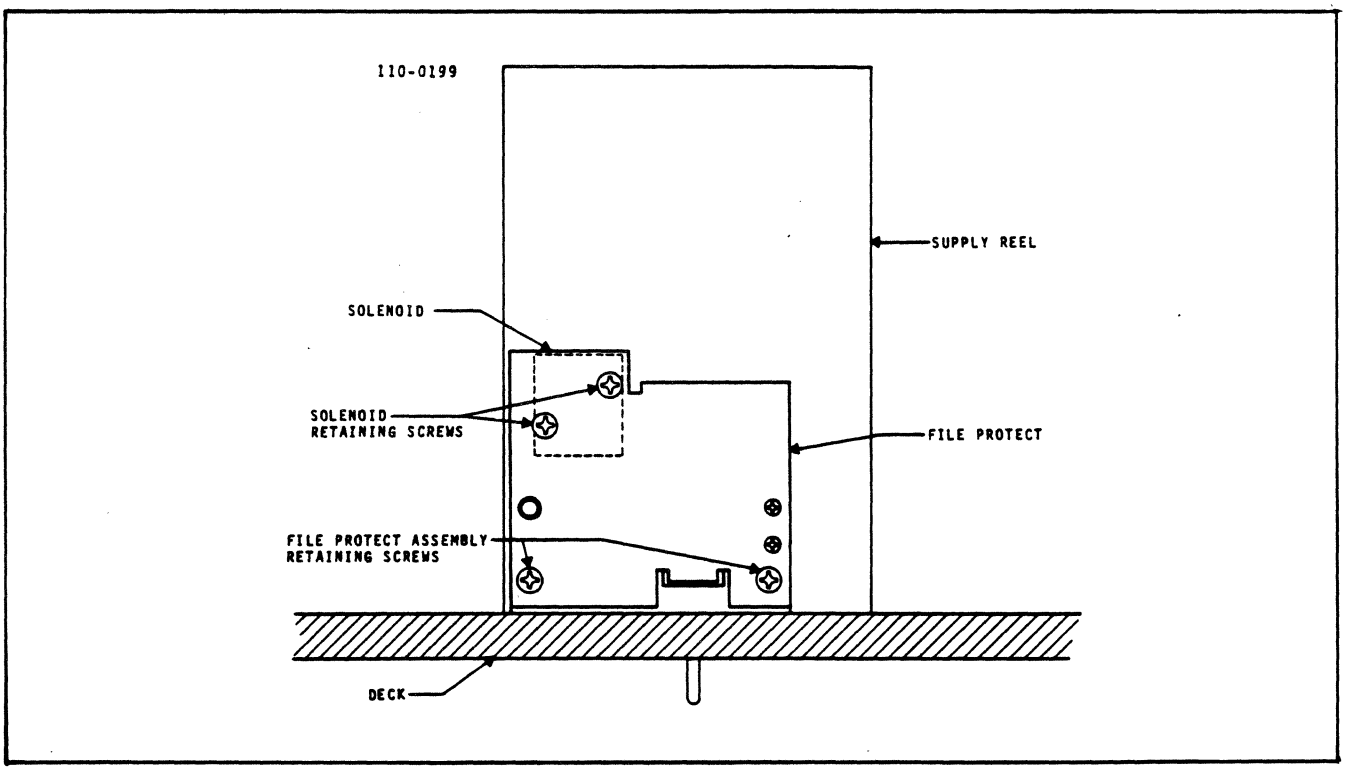



***Figure 4-8.***

***File Protect Assembly***

b. Insert three thicknesses of tape (0.006 inch) between shield surface and surface of head. Do not use feeler gauges, since they may scratch the head surface.

c. Press shield against tape firmly and tighten stop screw.

d. Remove tape pieces by lifting shield.

## 4.18 REPLACEMENT OF PARTS

In most instances assembly methods for parts replacement are obvious. Items in the tape path may require machine realignment if replaced. If only one item is replaced at a time the complete alignment procedure usually may be avoided. Examples follow.

4.18.1 HUB REPLACEMENT
(Refer to paragraph 4.13.1)

4.18.2 O RING REPLACEMENT
(Refer to paragraph 4.12.2)

4.18.3 REEL MOTOR REPLACEMENT
(Kennedy PN 190-5698-002)

a. To expose motor mounting screws, remove the hub assembly as described in paragraph 4.13.1.

b. Using a 5/32 inch Allen wrench, unscrew the four motor mounting screws and lift the reel motor out of the chassis.

4.18.4 MAGNETIC HEAD REPLACEMENT

Replacement heads are supplied as complete assemblies together with mounting plate.

a. Remove head cover.

b. Unplug head connectors.

c. Remove head mounting screw and remove head, passing connectors through the panel hole provided.

d. Be sure adjusting screw on replacement head is almost completely unscrewed.

e. Mount new head with mounting screw fairly loose. Screw in adjusting screw until point protrudes enough to engage its conical locating hole. Tighten mounting screw.

f. Plug in head.

g. Deskew the read head as described in the deskew adjustment procedure.

4.18.5 BOT/EOT SENSOR REPLACEMENT

a. Remove sensor assembly by unplugging and removing mounting screws. Since it will not pass through the hole provided, the connector must be removed by cutting the cable. Retain the connector.

b. Replacement sensors are provided with connector pins crimped to wires but with connector shell not installed.

c. Replace assembly, passing wires through hole provided. Replace screws.

d. Snap pins into connector shell in same color sequence as in the shell removed and plug in.

## 4.19 MAINTENANCE TOOLS

In addition to normal electronic tools and test gear (an oscilloscope, voltohmmeter, etc.) the following items should be available for service and repair.

Spanner wrench, Kennedy PN 154-0042-001

Set of nut drivers or open end wrenches

Phillips and standard screwdrivers

Skewmaster tape,
Kennedy PN 154-0036-001

Unflanged tension roller,
Kennedy PN 191-5484-001

Unflanged capstan roller,
Kennedy PN 191-5498-001

Maintenance kit, Kennedy PN 190-2324-001, containing:

Head cleaner

Hex socket keys: 7/64, 5/32, 1/8, 3/32

Lint-free swabs

Reflective marker strips

Magnasee visualizing solution

Loctite grade H

# SECTION VI

# SCHEMATIC DIAGRAMS

This section contains the schematic diagrams for the individual circuit cards used in the tape transport. The schematics are arranged in the order shown below. Electronics symbols used in the drawings conform to MIL-STD-18. Abbreviations conform to MIL-STD-12 unless otherwise specified.

## Schematic List

Voltage Regulator Type 5444

Microprocessor Emulator Type 5431

Servo/Control Type 5426

Power Amplifier Type 5503

Position Sensor Type 5764

Reel Size Sensor Type 5447

Control Panel Type 5145

Pre-Amplifier Type 5613-A

Read Amplifier Type 6470

PE Read Type 5326

Interconnect Type 5449

## Notes to the Schematics

Certain conventions have been observed in preparing schematics for this manual:

1. Resistor values are given in ohms. If wattage is unspecified the resistor may be either 1/4 or 1/2 watt.

2. Capacitor values may be given in picofarads or microfarads. Those values for which neither designation is provided are assumed to be obvious from circuit function. Filter capacitors on certain supply lines do not have logic significance. In general, they are not shown on schematics. On PC board silkscreens they are designated as CF.

3. Normally, IC power connections are on pins 14 (+5v) and 7 (ground) for 14 pin packages, and 16 (+5v) and 8 (ground) for 16 pin packages. Some ICs — 7476, 7492, 7493 for example — have power connections on pin 5 (+5v) and pin 10 (ground). Operational amplifiers in the 8 pin package have power connections on pin 4 (-Vcc) and pin 7 (+Vcc). Power connections are not shown unless they are nonstandard.

4. Where multiple inputs are tied together only one pin may be designated on the schematic.

5. Unused inputs that are tied high are not normally indicated unless the connection has logic significance.

6. From and to designations are intended to describe inputs and outputs only. The same signal may be connected to several other points not shown on a particular drawing.

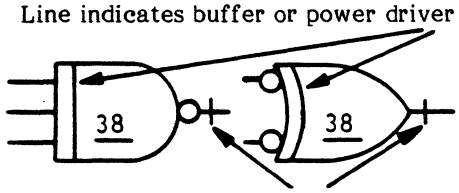
7. Positive logic is shown for all internal connections. Interface connections are zero true but the bar is omitted.

8. Integrated circuit symbols contain a circuit designator that corresponds to the number silkscreened onto the circuit module above an underlined number representing the IC type.

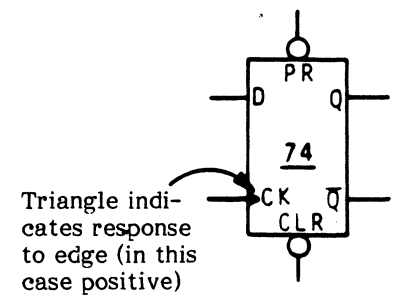
   The IC type number is abbreviated and omits the portions of the manufacturer's type number pertaining to case and vendor identification. Further, since the TTL 7400 series makes up most of the circuitry, the 74 is omitted on these. Thus a 00 designation indicates a 7400 quad two input NAND gate. T.I.'s complete part number is SN7400N. In multifunctional units in close proximity to each other the type designation may be omitted. The type designation may appear outside the symbol if the symbol is too small.

Military Standard 806C is the base for logic symbols. Additional conventions are shown below.

Line indicates buffer or power driver




Line indicates open collector



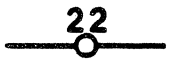

Triangle indicates response to edge (in this case positive)

9. Semiconductor types on schematics may be replaced by their functional equivalents. If not indicated, diodes are 1N914, NPN transistors are 2N2714, and PNP transistors are MPS6517.

10. Unless otherwise specified, light emitting diodes are FLV102 or equivalent.

11. Module connector pins are shown as


where no further connection is shown on the schematic, and as




when there is a connection shown.

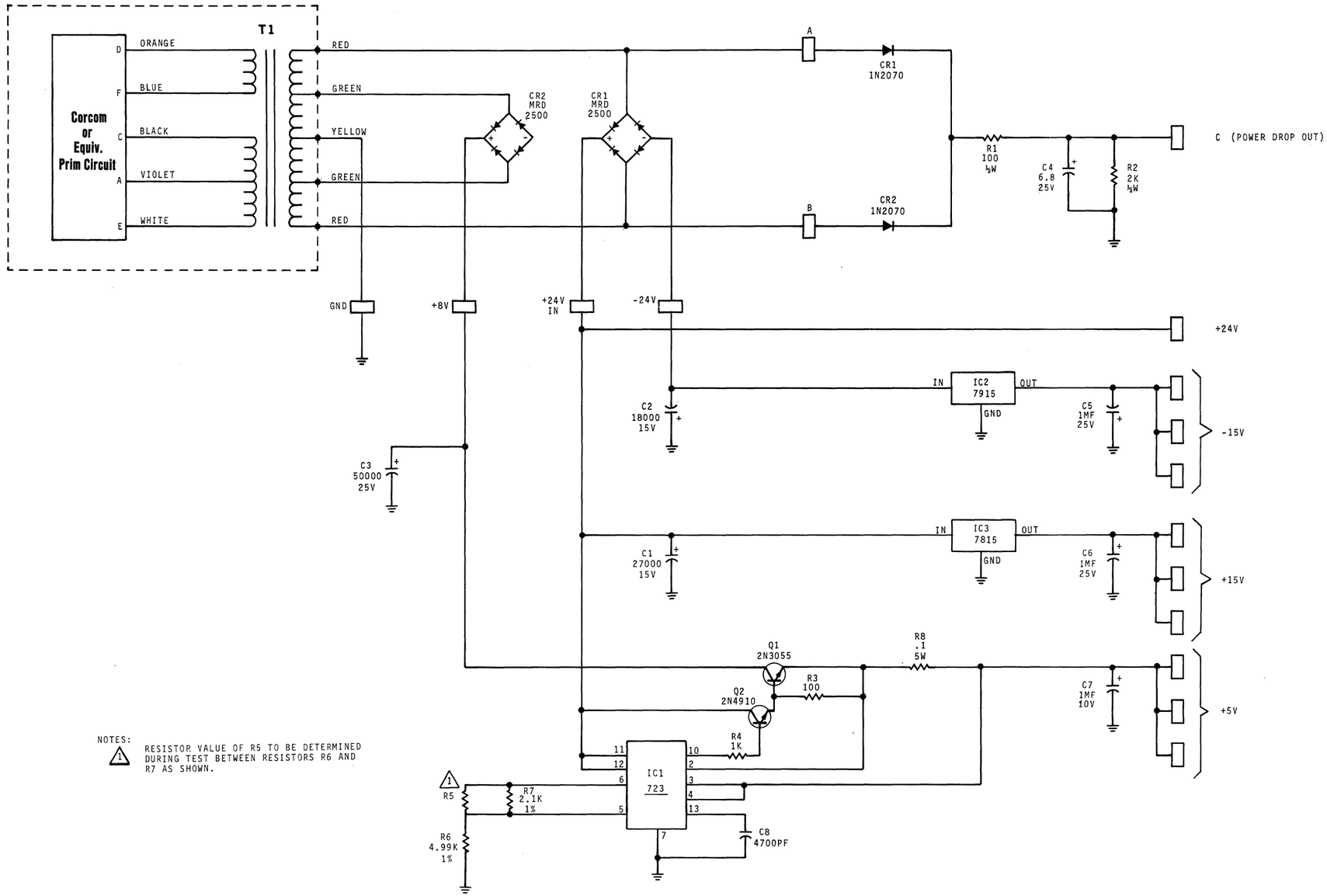
12. Where an input is represented by an arrow instead of a complete line, the input source is designated. Where outputs are so shown their destinations may not be shown.

13. Some schematics of modules include certain external elements which aid in understanding the circuit function. In this case all the connections to the element may not be shown in the interest of clarity.

14. 

designates a test point provided on the module. Letters proceed from top to bottom of card with the ground test point, if present, as the bottommost terminal.

15. Socket terminals are designated with numbers for component side connections and letters for circuit side connections when a double sided socket is used. These are the designations on the socket. When a single sided socket is provided, all connections are designated by letters regardless of which side of the board they lie on the etch. Letters follow the 22 pin alphabet, ABCDEFHJKLMNPRSTUVWXYZ; numbers are 1 through 22.

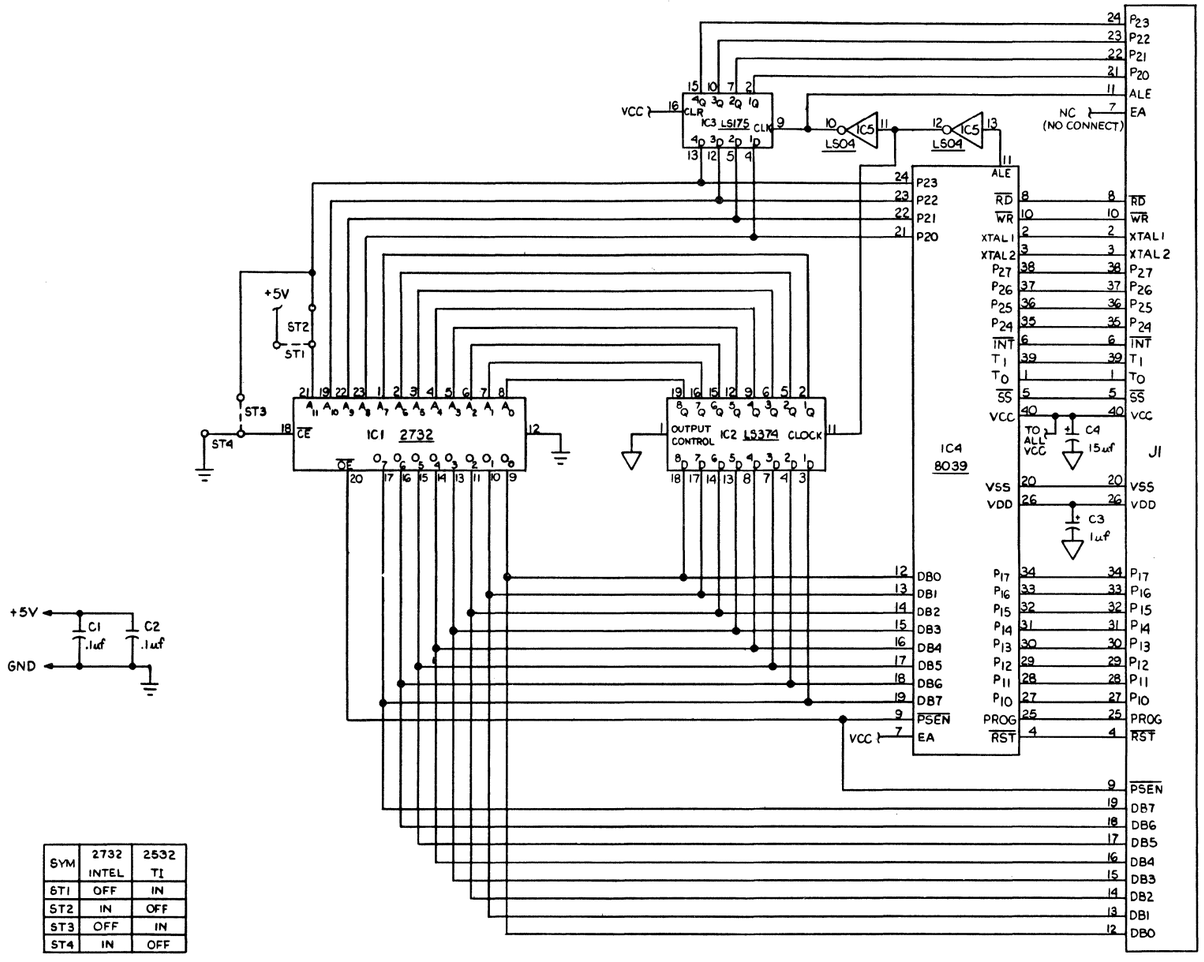



NOTES:

1. RESISTOR VALUE OF R5 TO BE DETERMINED DURING TEST BETWEEN RESISTORS R6 AND R7 AS SHOWN.

***Regulator Board***
***Type 5444***
***Schematic Diagram***

NOTES: UNLESS OTHERWISE SPECIFIED
1. 15 uf CAP IS 115-0199-156
2. 1 uf CAP IS 115-0199-105
3. DECOUPLING CAPS AS REQUIRED BETWEEN VCC AND GND (.1uf CKOS)




| SYM | 2732 INTEL | 2532 TI |
|---|---|---|
| ST1 | OFF | IN |
| ST2 | IN | OFF |
| ST3 | OFF | IN |
| ST4 | IN | OFF |

***Emulator Bd. - Data Streamer***
***Type 5431 R***
***Schematic Diagram***

3 4

A B C D

J6 5 POWER DROP OUT

R1 20.5K 1% R2 20.5K 1% R3 7.5K 1% R4 26.7K 1% R5 27K R24 28.7K 1% R25 4.87K 1% R27 10K R28 6.98K 1% R26 10K

J4 CONTROL PANEL 190-5145-001

RESET LOAD PB ON LINE RWD PB

(4/B2) RST.PB

R6 4.7K R7 4.7K R8 4.7K

RWD.PB (2/A2)
ONL.PB (2/A2)(3/A2
LD.PB (2/A2)

SLT 220 ONL 220 LP 220 RWDG 220 POWER 220 FPT 220

(4/B4) SLT1
(2/A3) ONL.LED
(3/A1)(2/A2) LP
(2/A3) RWD.LED

J7 FILE PROTECT ASSY 190-2641-006

CR1 1N2069 Q1 2N6038 R12 1K R13 4.7K

(2/A2) BKN
FPT SWITCH
FPT (2/A2)

J5 19 WRITE

(2/A3) WRTC

R29 220K R30 220K R33 1M R34 10K R36 1M R37 1M R38 10K C1 47pF C2 100pF C3 0.15 SW2 NC NO

R58 1K
HRESET (3/B3)(4/A1)(5/C1)

R39 10K
PRESET (2/C1)

C5 .027 R43 47K R44 220 R45 1K C6 1.5 35V Q2 2N6038 CR14 IN 758A CR15 1N914 WTCUR (5/D4)

C9 2.2 20V

Q3 2N4403 Q4 2N4401 R63 10K R64 270 R65 470

J8 1
J8 2

R40 3.3 K R41 1K R42 20K

CR25 1N914 R57 390K R148 10K R147 1M C8 4.7 10V

R23 1.5K ½W R31 100K CR11 1N914 CR12 1N914 R32 12K

R35 4.7 K

IC 120-8 (2/2D)
IC 120-1 (3/4C)

TP2

T1 (2/A1)

J3 B.O.T./E.O.T SENSOR ASSY 190-5906-001

(2/B1) PP1-7

R9 680 ½W

REF ONLY

TIL149 TIL149

C4 .022

68 191 54 191

(6/B3)(2/A4) FWD
(6/B4) POSTS

UP/DN LOAD CK RCK

F1 (3/A4)

(2/C2) DISABLE

MC14584

R10 62K R84 10K C65 .1 R11 62K R85 10K C66 .1

LP (2/A1)
EOT (2/A1)

TP3
TP4

+5V

| REF DESIGNATOR BLOCK | |
|---|---|
| LAST USED | NOT USED |
| C70 | C28,29 |
| CR29 | |
| Q4 | |
| R156 | R70 |
| IC126 | |
| Y1 | |
| TP12 | |
| SW2 | |

REPRESENTS RESISTOR TERMINATOR NETWORK IN A 16 PIN DIP PACKAGE. PIN 8 , GRD; PIN 16, +5V RENAC'D PART NO 149-0043-003. BECKMAN INST. PART NO 898-SR-220/330 OR EQUIV.

**Servo/Control Bd.**
**Type 5426,** AA
**Schematic Diagram**

1 2 3 4

A B C D

J3 REEL SIZE SENSOR 190-5447-001

R61 10K R59 4.7K R60 4.7K R62 10K

339 96 LS339 LS14 LS32 LS08 LS04 LS279 LS240 LS245 LS374 LS175 LS138 LS86 LS08 LS374

EOT (3/A1) BKN (1/A3) ONL.PB (3/A2)(1/A2) FPT (1/B4) RWD.PB (1/A2) LD.PB (4/B3) INIT

XTL2 T1 XTL1 PP2-7 PP2-6 PP2-5 PP2-4 PP2-3 PP2-2 PP2-1 PP1-7 PP1-6 PP1-5 PP1-4 PP1-3 PP1-1 PP1-0 PRESET INT

DATA BUSY (2/B4)(4/A4)(5/C1)(6/C2)

84 8049 READ WRITE ALE DISABLE (1/D1) DISABLE

HI.SPEED (3/D3) RAMP (3/A3) WRTC (1/B3) STOPLOCK (6/C3) ONL.LED (1/A3) RWD.LED (1/B3) VERASE (5/C1)

J5 7 LO HI SPEED J5 20 FWD FWD (1/D1)(6/B3) WR (3/B1)

READ B (3/B2)(4/B3) WRT2 (3/D2) WRT1 (3/D1)

J5 18 RAEN DATA BUSY (2/A1)(4/A4)(5/C2)(6/C2) WRITE ENABLE (5/C1) READY (4/A3) DATA (5/C1) WFMK (5/C1) ID BURST (5/C1)

F BUSY (4/B1) WR I/O (4/C4)

J5 1 CMP ID (5/C1) EVERASE (1/D3)(2/A1) LP DATA DETECT (6/C2)

READY (4/D3) READ6 (4/D3)(6/D2) RD I/O (4/A3) READ (4/D3)

D7 (3/B1) 6/C2 D6 (3/B1)(6/C2) D5 (3/B1)(6/C2) D4 (3/B1)(6/C2) D3 D2 D1 D0 (3/B1)(6/C2)

DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7 (6/C2)(4/D4) (4/D4)(6/C2)

R88 1K R87 1K C14 1000pF R89 10K R90 27K C11 0.01 C12 1000pF C13 51pF R86 20.5K 1% R81 20.5K 1% R82 10K R83 10K C26 22pF

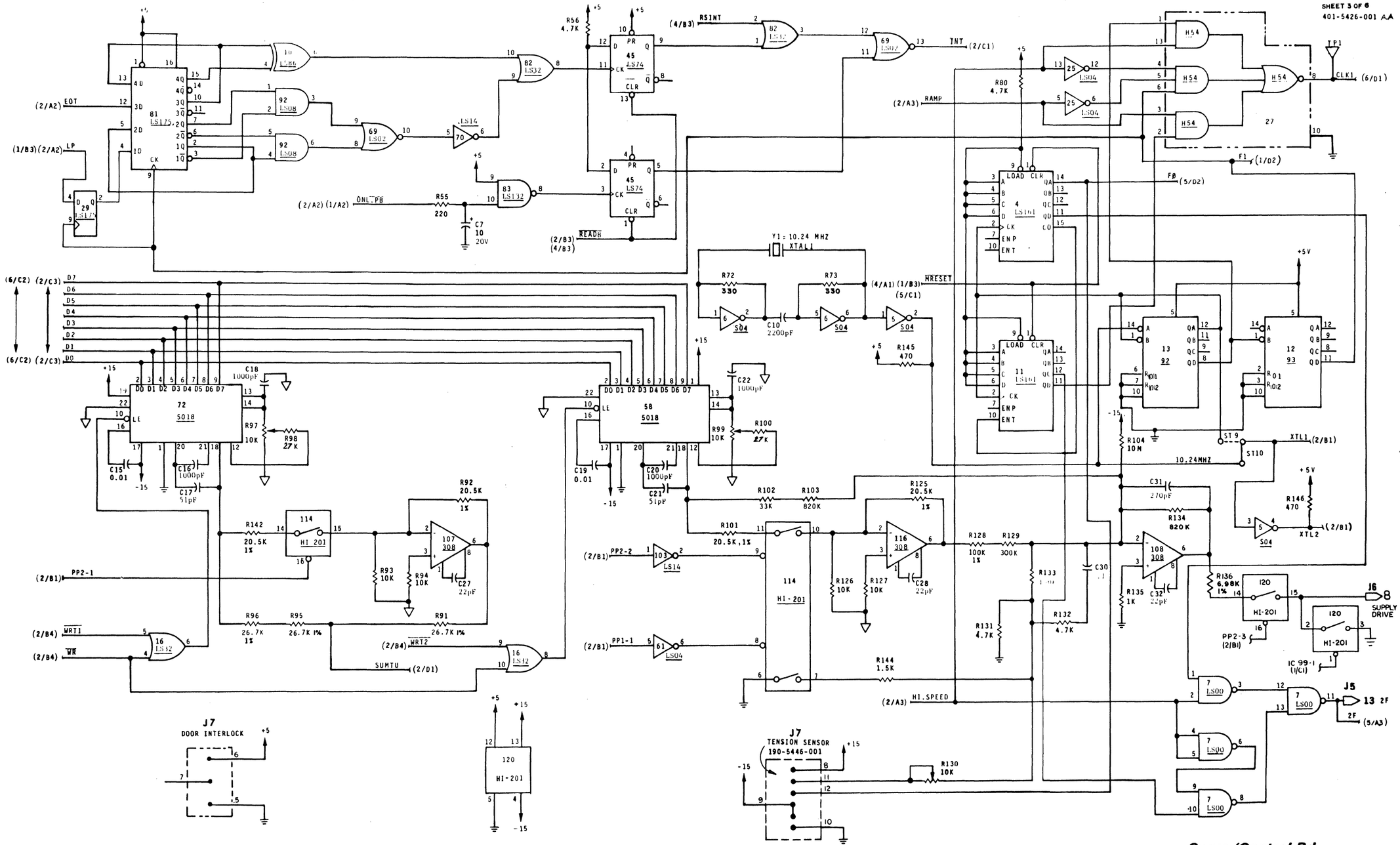
R76 56.2K 1% R77 47K C25 22pF R75 27K R74 4.7K J6 9 TAKEUP DRIVE HI-201 IC99-1 (1/C1) R78 47.5K 1% R79 90.9K 1% SUMTU (3/D2)

+5 +15 -15

***Servo/Control Bd.***
***Type 5426, AA***
***Schematic Diagram***

1 2 3 4

A B C D




***Servo/Control Bd.***
***Type 5426,*** AA
***Schematic Diagram***

1 2 3 4

A B C D

J5 9 MRESET

4C4 (LPI) 13 64 LS04 12 LSO4

19 LS08 6 — 106 LSO0 8

20 LS74 (PR, CK, CLR, D, Q)

(3/B3)(1/B3) (6/C1) MRESET

19 LS08 3

GO

13 CLR 20 LS74 PR 10

11 61 LS04 10

LS04 64 8

105 LS32 R

J1 FEN 48

GND 3,11,13, 15,17,19, 21,23,25,27, 29,34,38,42, 44,46

GO 45

TAD 2 49

TAD 1 50

TAD 0 47

T78 T77

LONG GAP 36

HIGH SPEED 33

REWIND 35

OFF LINE 31

ERASE 41

WFM 39

REV/FWD 37

WRITE/READ 40

EDIT 43

(4/C3) RW

59 LS74 (PR, CK, CLR, D, Q)

34 LS08 3 — 34 LS08 11

TP9

(2/C4) READY

ST11

88 H21 6

18 LS32 8 — 126 LS08 3

IC35-11

28 LS08 3

(2/B4) F BUSY

61 LS04 4

59 LS74 (PR, CK, CLR, D, Q)

105 LS32 11

19 LS08 8

+5

90 121 (A1, A2, B)

C34 470pF

(2/C2) RD I/O

R140 220

C33 10 35V

22 LS14 — 22 LS14

38 38 11

R141 4.7K

R137 4.7K

38 38 6

(1/A2) RST.PB

106 LSO0 6

62 LS08 — 62 LS08 — 76 LS02

126 LS08 8

106 LSO0 3

18 LS32 6

126 LS08 3

RWDG (4/A4)

OFF LINE

75 LS174 (CK, D5, D6, D4, D3, D1, D2, Q8, Q6, Q4, Q3, Q1, Q2)

74 S287 (S1, S2, H, G, F, E, D, C, B, A, DO4, DO3, DO2, DO1)

SW1

91 LS138 (G1, C, A, B, G2A, G2B, Y0–Y7)

76 LS02 — 105 LS32 — 89 LS02

TP8

(4/A2) RW

14 LS32 — 14 LS32

(2/C4) WR I/O

(2/C1) ZERO (6/B4)

IC(28-1)

S04

2A1 2A2 2A3 2A4 1A1 1A2 1A3 1A4 (35 LS244) 1Y1 1Y2 1Y3 1Y4 2Y1 2Y2 2Y3 2Y4

36 LS374 (8D, 7D, 6D, 5D, 4D, 3D, 2D, 1D, 8Q, 7Q, 6Q, 5Q, 4Q, 3Q, 2Q, 1Q)

DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 (2/C2)(6/C2)

60 LS74 (PR, CK, CLR, D, Q)

R138 4.7K

63 LS74 (PR, CK, CLR, D, Q)

RSINT (3/A2)

RSINT (2/A2)

(2/B3) (3/B2) READ8

34 LS08 6

60 LS74 (PR, CK, CLR, D, Q)

TP10

(2/A1) (2/B4) (5/C1) (6/C2) DATA BUSY

38 38 — 61 LS04 — 21 38 — 37 38

J1

2 F BUSY

4 DATA BUSY

6 RWDG

RWDG (4/D2)

8 ON LINE

9 FILE PROTECT

5 EOT

7 LP

SLT1 (1/A3)

10 HIGH SPEED1

J5 5 SLT1

J1 12 READY

LPI (4A1)

J5 3 IDENT

16 WHER

106 LSO0 — 19 LS08

(2/C3) READ 13

READ6 — READ7

(2/C2) (6/D2) (2/C2)

**Servo/Control Bd.**
**Type 5426, AA**
**Schematic Diagram**

SHEET 5OF6
401-5426-001AA

1 2 3 4

A B C D

J1

WD0 30
WD1 28
WD2 26
WD3 24
WD4 20
WD5 16
WD6 22
WD7 18
WDP 14
LWD 32

IC 78

(2/C4) WFMK
(2/B4) (4/A4) (6/C2) (2/A1) DATA BUSY
(1/B3) (3/B3) (4/A1) MRESET
(2/C4) DATA
(2/A3) V ERASE
(2/C4) WRITE ENABLE
(2/C1) EVERASE
(2/C4) ID BURST

J2

0 1 2 3 4 5 6 7 P

CR2 IN914 … CR24 IN914
R14 390 1/2W … R54 390 1/2W

R143 2.2K

WTCUR (1/C4)
J1 WSTR

2F (3/D4)
F8 (3/A4)

+5

**Servo/Control Bd.**
**Type 5426, AA**
**Schematic Diagram**

1 2 3 4

A B C D

J1
CAPSTAN ASSY (REF)
190-5379-001

J3

J6

TIL148 TIL148

R2 10 · C1 6.8 · 220 · 220

R121 2.2K · R122 2.2K · R123 330 · R124 330 · R145 50K 5.1K · R146 50K 5.1K · R119 · R120 · POST1

C24 560 · C69 560 · R71 100K · R149 100K · R117 62K

R151 6.98K 1% · R152 6.98K 1% · R153 6.98K 1% · R154 6.98K 1% · R70 390K · R150 390K

CR26 1N914 · CR27 1N914 · CR28 1N914 · CR29 1N914

R155 4.87K · R156 4.87K

C70 0.1 · R68 4.87K · R105 150K · R106 1K · R69 62K · R66 4.7K · R67 STARP

TP7 · TP11 · TP12 · TP6

STOPPED (2/B1)

C38 - C43 C46 - C52, C55, C58 - C66 .01 · C35 10 · C44, C54, C57 .01 · C36 10 · C53, C56 .01 · C37 10 · C45 .01

GND

R118 62K · C68 470 · R114 62K · R115 10K · R110 62K · R109 4.7K · R116 2K

C67 470 · R111 62K · R112 10K · R107 4.7K · R108 62K · R113 2K

$\overline{T9}$ (2/C1)

POST5 (1/D1) · POST5

ZERO (4/C3)

FWD (2/A4) (1/D1)

STOPLOCK (2/A3)

PP2-7 (2B2)

DATA BUSY (2/B4)(4/A4)(5/C1) (2/A1)

DATA DETECT (2/C1)

J5 17 REN

PP1-6 (2/B1)

READ6 (2/C2) (4/D3)

CLK1 (3/A4)

(2/C3)(3/B1)

D0 D1 D2 D3 D4 D5 D6 D7

**Servo/Control Bd.**
**Type 5426,** AA
**Schematic Diagram**

SHEET 1 OF 6
401-5926-001 C

1 2 3 4

A B C D

J6 5 POWER DROP OUT

R1 20.5K 1% R2 20.5K 1% R3 7.5K 1% R4 26.7K 1% R5 27K R24 28.7K 1% R25 4.87K 1% R26 10K R27 10K R28 6.98K 1%

103 339

GND

RESET LOAD PB ON LINE RWD PB

(4/B2) RST.PB

R6 4.7K R7 4.7K R8 4.7K

RWD.PB (2/A2)
ONL.PB (2/A2)(3/A2
LD.PB (2/A2)

J4 CONTROL PANEL 190-5145-001

SLT ONL LP RWDG POWER FPT 220

(4/B4) SLT1
(2/A3) ONL.LED
(3/A1)(2/A2) LP
(2/A3) RWD.LED

63 06

J7 FILE PROTECT ASSY 190-2641-006

CR1 1N2069 Q1 2N6038 R12 1K R13 4.7 K

(2/A2) BKN

104 LS00 63 06

FPT SWITCH

114 LS04 FPT (2/A2)

J5 19 WRITE

105 LS08

126 074 R42 20K R40 3.3 K R41 1K

(2/A3) WRTC

C1 47pF R29 220K R30 220K SW2 RESET NC NO

115 339 C2 100pF R33 1M CR13 1N914 R34 10K R36 1M R37 1M C3 0.15 R38 10K

R58 1K MRESET (3/B3)(4/A1)(5/C1)

R39 10K

50 07 PRESET (2/C1)

R35 4.7K

76 LS14 TP2

3 38

87 LS32 T1 (2/A1)

IC 120-8 (2/2D)
IC 120-1 (3/4C)

CR25 1N914 R57 390K R148 10K R147 1M C8 4.7 10V

R23 R31 100K CR11 1N914 CR12 1N914 R32 12K

103 339

C5 .027 R43 47K R44 220 R45 1K C6 1.5 35V C9 2.2 20V

126 074 CR14 IN 758A CR15 1N914 Q2 2N6038 WTCUR (5/D4)

J3 E.O.T./E.O.T SENSOR ASSY 190-5906-001

R9 680 ½W REF ONLY TIL149 TIL149

(2/B1) PP1-7

88 LS132 C4 .022

J8 1

Q3 2N4403 R63 10K R64 270 Q4 2N4401 R65 470

J8 2 ERASE

74 191 62 191

(6/B3)(2/A4) FWD
(6/B4) POSTS
RCK

48 LS175 117 LS86 F1 (3/A4)

17 LS86 S04 1 LS08 34 LS74

+5V

MC14584

R10 62K C65 .1 R84 10K R11 62K R85 10K C66 .1

LF EOT

46 LS132 TP3 LF (2/A1) TP4 EOT (2/A1)

(2/C2) DISABLE 88 LS132 75 LS02

| REF DESIGNATOR BLOCK | |
|---|---|
| LAST USED | NOT USED |
| C70 | C23, 29 |
| CR29 | |
| Q4 | |
| R156 | R70 |
| IC 126 | |
| Y1 | |
| TP12 | |
| SW2 | |

REPRESENTS RESISTOR TERMINATOR NETWORK IN A 16 PIN DIP PACKAGE. PIN 8, GRD; PIN 16, +5V. KENNEDY PART NO 149-0043-003. BECKMAN INST. PART NO 898-5R-220/330 OR EQUIV.

+5V 220 330

**Servo/Control Bd.**
**Type 5926-001**
**Schematic Diagram**

1 2 3 4

A B C D

J3 REEL SIZE SENSOR 190-5447-001

R61 10K R59 4.7K R60 4.7K R62 10K

339 339

EOT (3/A1) BKN (1/A3) ONL.PB (3/A2)(1/A2) FPT (1/B4) RWD.PB (1/A2) LD.PB (1/A2) RSINT (4/B3)

64 LS240 90 LS245 10 LS245 77 LS374 51 LS175 78 5018 22 LS138 24 LS374

HI.SPEED (3/D3) RAMP (3/A3) WRTC (1/B3) STOPLOCK (6/C3) ONL.LED (1/A3) RWD.LED (1/B3) VERASE (5/C1)

J5 7 LO HI SPEED

J5 20 FWD FWD (1/D1)(6/B3)

WK (3/B1)

READ B (3/B2)(4/B3)

WRT2 (3/D2) WRT1 (3/D1)

J5 18 RAEN

DATA BUSY (2/A1)(4/A4)(5/C2)(6/C2)

WRITE ENABLE (5/C1) READY (4/A3) DATA (5/C1) WFMK (5/C1) ID BURST (5/C1)

WR I/O (4/C4)

F BUSY (4/B1)

J5 15 PP2-6 DATA BUSY (2/B4)(4/A4)(5/C1)(6/C2)

J6 PP2-5 3 PP2-4 2

J5 11 PP1-5 J6 1 PP1-4

89 8039 READ WRITE ALE

DISABLE (1/D1) J6 6 DISABLE

READY (4/D3) READ6 (4/D3)(6/D2) RD I/O (4/A3)

R88 1K R87 1K

J5 1 CHP ID EVERASE (5/C1) LP (1/D3)(2/A1)

DATA DETECT (6/C2)

+5V

XTL2 T1 XTL1 PP2-7 PP2-3 PP2-2 PP2-1 PP1-7 PP1-6 PP1-3 PP1-1 PRESET (1/C3) INT (3/A3) STOPPED (6/A3) (3/D2) TP (6/B3)

R76 56.2K 1% SUMTU (3/D2) R75 27K R74 4.7K J6 9 TAKEUP DRIVE HI-201 IC99-1 (1/C1)

R78 47.5K 1% R79 90.9K 1%

R77 47K C25 22pF

R86 20.5K 1% R81 20.5K 1% R82 10K R83 10K C26 22pF

C13 51pF C14 1000pF R89 10K R90 27K C11 0.01 C12 1000pF

+15 -15

**Servo/Control Bd.**

**Type 5926-001**
**Schematic Diagram**

1 2 3 4

A B C D

(2/A2) EOT
(1/B3)(2/A2) LP
(2/A2)(1/A2) ONL.PB
(2/B3)(4/B3) READ6
(4/B3) RSINT
(2/C1) INT
(2/A3) RAMP
(5/D2) F0
(1/D2) F1
(6/D1) CLK1
Y1 = 10.24 MHZ XTAL1
(4/A1)(1/B3)(5/C1) MRESET
(6/C2)(2/C3) D7 D6 D5 D4 D3 D2 D1 D0
(2/B1) PP2-1
(2/B4) WRT1
(2/B4) WR
(2/B4) WRT2
SUMTU (2/D1)
(2/B1) PP2-2
(2/B1) PP1-1
(2/A3) HI.SPEED
XTL1 (2/B1)
10.24MHZ
XTL2 (2/B1)
PP2-3 (2/B1)
IC 99-1 (1/C1)
J5 13 2F
2F (5/A3)
J6 SUPPLY DRIVE
+5V

R56 4.7K
R55 220
C7 10 20V
R72 1.5K
R73 1.5K
C10 2200pF
R145 470
R80 4.7K
C18 1000pF
C15 0.01
C16 1000pF
C17 51pF
R97 10K
R98 27K
C22 1000pF
R100 27K
C19 0.01
C20 1000pF
C21 51pF
R99 10K
R92 20.5K 1%
R142 20.5K 1%
R93 10K
R94 10K
C27 22pF
R96 26.7K 1%
R95 26.7K 1%
R91 26.7K 1%
R102 33K
R103 820K
R101 20.5K,1%
R125 20.5K 1%
R126 10K
R127 10K
C28 22pF
R144 1.5K
R128 100K 1%
R129 300K
R133 150K
R131 4.7K
R132 4.7K
C30 .1
R104 10M
C31 270pF
R134 820K
R135 1K
C32 22pF
R136 8.2K
R146 470
R130 10K

86 LS175
48 LS175
17 LS86
94 LS08
94 LS08
75 LS02
LS14
87 LS32
88 LS132
49 LS74
87 LS32
75 LS02
H54
H54
H54
33
LS04
LS04
LOAD CLR 4 LS161
LOAD CLR 18 LS161
65 5018
52 5018
20 92
19 93
109 HI-201
121 308
122 308
123 308
97 HI-201
97 HI-201
97 HI-201
LS04
LS14
LS32
LS00
LS00
LS00
LS00

J7 DOOR INTERLOCK
J7 TENSION SENSOR 190-5446-001

**Servo/Control Bd.**
**Type 5926-001**
**Schematic Diagram**

1 2 3 4

A B C D

J5 9 MRESET

4C45 LPI 5 82 LS04 6

12 LS08 6 — 4,5

91 LS00 8 — 9,10

27 LS74 (PR, D, CK, CLR, Q, Q̄) — 2,3,1,4,5,6

(3/B3)(1/B3) (5/C1) MRESET

12 LS08 3 — 1,2

60

27 LS74 (CLR, D, CK, PR, Q) — 13,12,11,10,9,8

11 40 10 LS04

LS04 9 82 8

92 LS32 8 — 9,10

92 LS32 11 — 13,12

IC 39 -11

13 LS08 6 — 4,5

40 LS04 4 — 3

(2/B4) F BUSY

38 LS74 (PR, D, CK, CLR, Q, Q̄) — 10,9,11,13,12,8

40 LS04 12 — 1

12 LS08 8 — 9,10

R140 220

C33 10 35V

(1/A2) RST.PB

14 LS14 4 — 3

14 LS14 6 — 5

41 38 11 — 13,12

91 LS00 6 — 5,4

R141 4.7K

R137 4.7K

41 38 6 — 4,5

+5

J1 FEN 48

GND 3,11,13, 15,17,19, 21,23,25,27, 29,34,38,42, 44,46

GO 45

55 LS08 8 — 9,10

55 LS08 11 — 12,13

66 LS02 1 — 2,3

TP8

55 LS08 6 — 4,5

105 LS08 3 — 2,1

91 LS00 3 — 1,2

40 LS04 8 — 9

SW1

11 LS32 6 — 4,5

TAD 2 49

TAD 1 50

TAD 0 47

82 LS04 — 13,12 / 1,2 / 11,10

93 LS138 (G1, C, A, B, G2A, G2B, Y0–Y7) — 6,16,3,2,1,4,5,15,14,13,12,11,10,9,7

220/330 70 — 9,10,11,12

220/330 83 — 14,15,1,2,3

LONG GAP 36

HIGH SPEED 33

REWIND 35

OFF LINE 31

ERASE 41

WFM 39

REV/FWD 37

WRITE/READ 40

EDIT 43

66 LS02 10 — 9,8

66 LS02 13 — 11,12

92 LS32 3 — 2,1

92 LS32 6 — 4,5

80 LS02 13 — 11,12

80 LS02 10 — 9,8

80 LS02 4 — 5,6

80 LS02 1 — 3,2

66 LS02 4 — 5,6

67 LS174 (CK, D6, D4, D3, D1, D2, Q6, Q4, Q3, Q1, Q2) — 9,13,14,11,6,3,4,12,15,10,7,2,5

54 S287 (S1, S2, H, G, F, E, D, C, B, A, D04, D03, D02, D01) — 13,14,15,1,2,3,4,7,6,5,9,10,11,12

(2/C4) READY

TP9

79 A21 6 — 1,5,2

(2/C2) RD I/O

69 121 (A1, A2, B, Q) — 3,4,5,9,14,6,11

C34 470pF

+5

R138 4.7K

81 LS74 (CLR, D, CK, PR, Q) — 13,12,11,10,9,8

41 38 8 — 9,10

68 LS74 (PR, D, CK, CLR, Q, Q̄) — 4,2,3,1,5,6

RSINT (3/A2)

RSINT (2A2)

READ8

(2/B3) (3/B2)

25 LS08 11 — 13,12

25 LS08 3 — 2,1

81 LS74 (PR, D, CK, CLR, Q) — 4,2,3,1,5

(4/A2) RW

8 LS32 3 — 1,2

8 LS32 6 — 4,5

53 LS74 (PR, D, CK, CLR, Q, Q̄) — 10,12,11,13,9,8

53 LS74 (CLR, D, CK, PR, Q, Q̄) — 1,2,3,4,5,6

(2/C4) WR I/O

IC 13-4

5 S04 8 — 9,8

7ERO (6/B4)

39 LS244 (1A1–1A4, 2A1–2A4, 1Y1–1Y4, 2Y1–2Y4) — 18,17,14,13,8,7,4,3 / 2,4,6,8,11,13,15,17 / 9,12,7,14,5,16,3,18 / 11,8,13,6,15,4,17,2

26 LS374 (1D–8D, 1Q–8Q, CK) — 3,4,7,8,13,14,17,18 / 2,5,6,9,12,15,16,19 / 11

DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 (2/C2)(6/C2)

91 LS00 11 — 12,13

READ 13

(2/C3)

12 LS08 13 — 12,11

READ6 12

READ7 13

(2/C2) (6/D2) (2/C2)

TP10

(2/A1) (2/B4) (5/C1) (6/C2) DATA BUSY

41 38 3 — 1,2

40 LS04 12 — 13

42 38 3 — 2,1

57 38 3 — 13,12

57 38 6 — 4,5

42 38 6 — 4,5

42 38 8 — 10,9

57 38 8 — 12,13

42 38 11 — 13,12

J1

2 F BUSY

4 DATA BUSY

6 RWDG

8 ON LINE

9 FILE PROTECT

5 EOT

7 LP

SLT1 (1/A3)

10 HIGH SPEED1

J5 5 SLT1

J1 12 READY

LPI 5 4A1

J5 3 IDENT

***Servo/Control Bd.***
***Type 5926-001***
***Schematic Diagram***

1 2 3 4

A B C D

J1
CAPSTAR ASSY (REF)
190-5579-001

J3

J6

J5

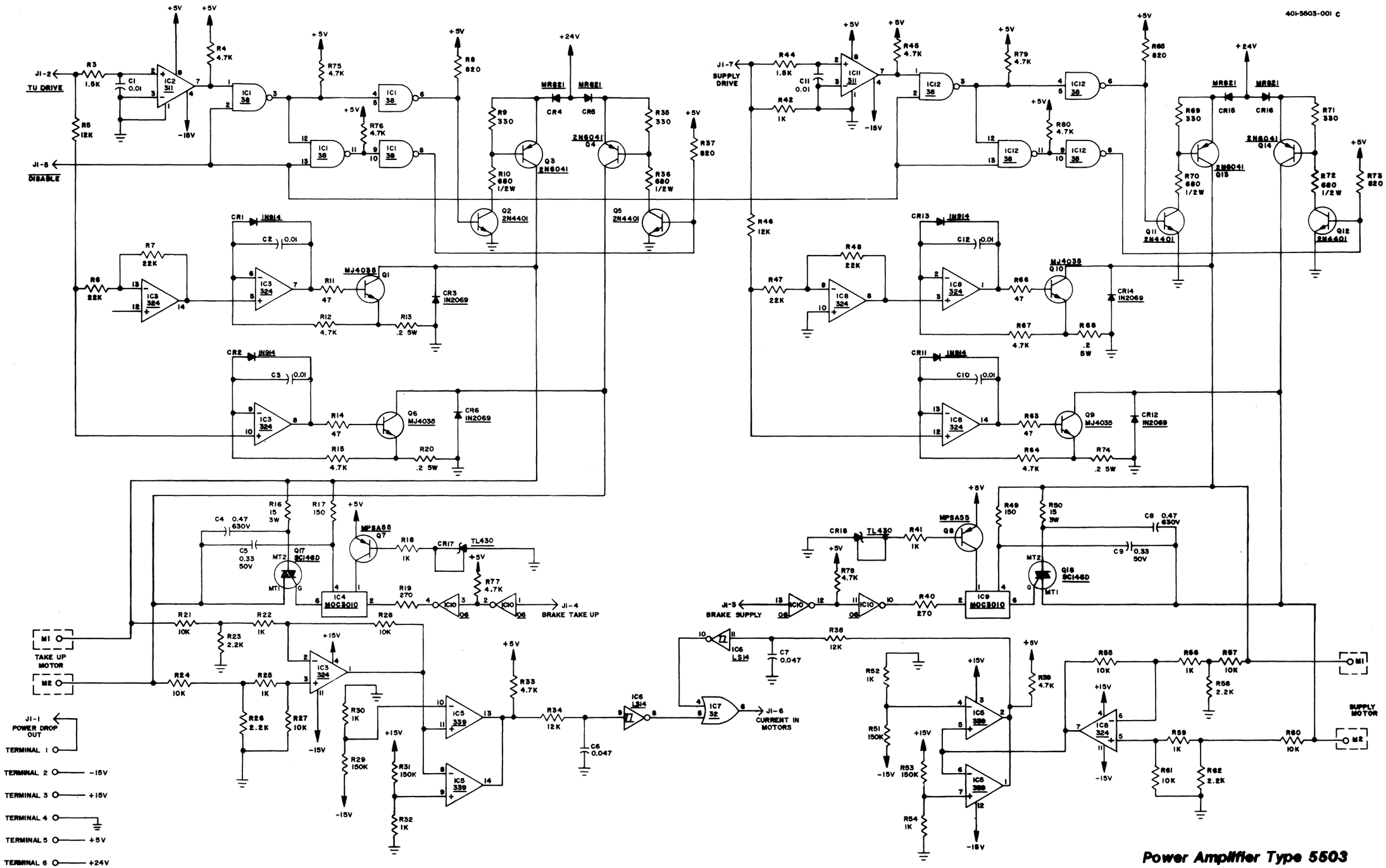
TP5 TP6 TP7 TP11 TP12

R2 10
C1 6.8
TIL148
220
R123 330
R121 2.2K
R122 2.2K
R124 330
R157 20K
R158 20K
R119 10K
R120 10K
POST1
C24 560
C69 560
R71 100K
R149 100K
R117 62K
R118 62K
C68 470
R114 62K
R115 10K
R110 62K
R109 4.7K
R116 2K
C67 470
R111 62K
R112 10K
R108 62K
R113 2K
R107 4.7K
R152 6.98K 1%
R151 6.98K 1%
R154 6.98K 1%
R153 6.98K 1%
R150 390K
R70 390K
R155 4.87K
R156 4.87K
C70 0.1
R68 4.87K
R105 150K
R106 1K
R69 62K
R66 4.7K
CR26 1N914
CR27 1N914
CR28 1N914
CR29 1N914
STOPPED (2/81)
C38 - C43
C46 - C52, C55,
C58 - C66
.01
C35 10
C44, C54,
C57 .01
C36 10
C53,
C56 .01
C37 10
C45 .01
GND
POSTS (1/D1)
POSTS
FWD (2/A4) (1/D1)
ZERO (4/C3)
STOPLOCK (2/A3)
DATA BUSY (2/B4)(4/A4)(5/C1) (2/A1)
DATA DETECT (2/B2)
PP1-6 (2/B1)
PP2-7 (2B2)
READ6 (2/C2) (4/D3)
CLK1 (3/A4)
DO (2/C3) (3/B1)
D1
D2
D3
D4
D5
D6
D7
(2/C3) (3/B1)
T9 (2/C1)
J5 17 REN

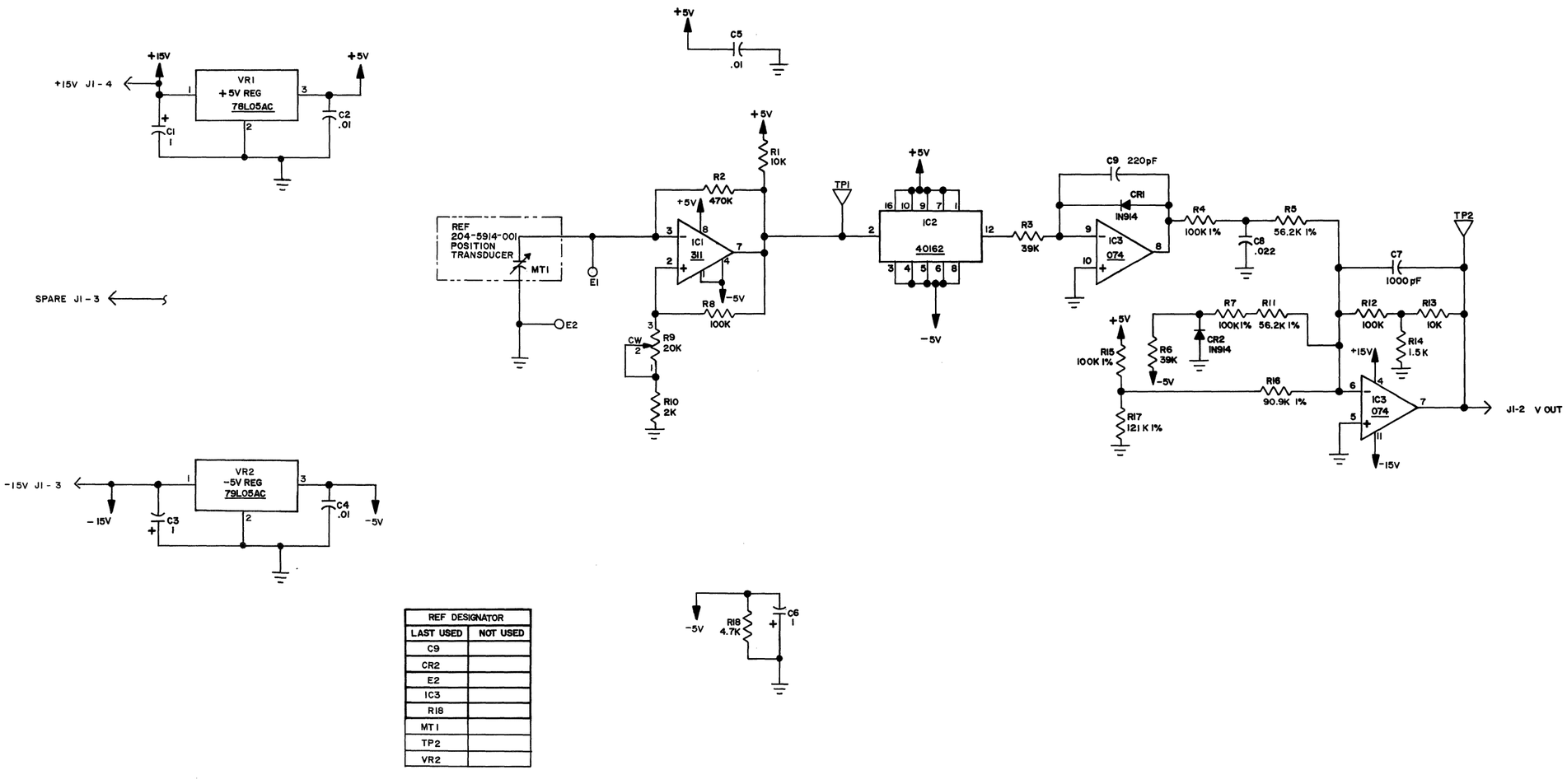
23 LS161
36 LS161
37 LS374
34 LS74
118 LS74
LS04
LS08
LS32
LS00
LS374
LS74

**Servo/Control Bd.**
**Type 5926-001**
**Schematic Diagram**

401-5503-001 C

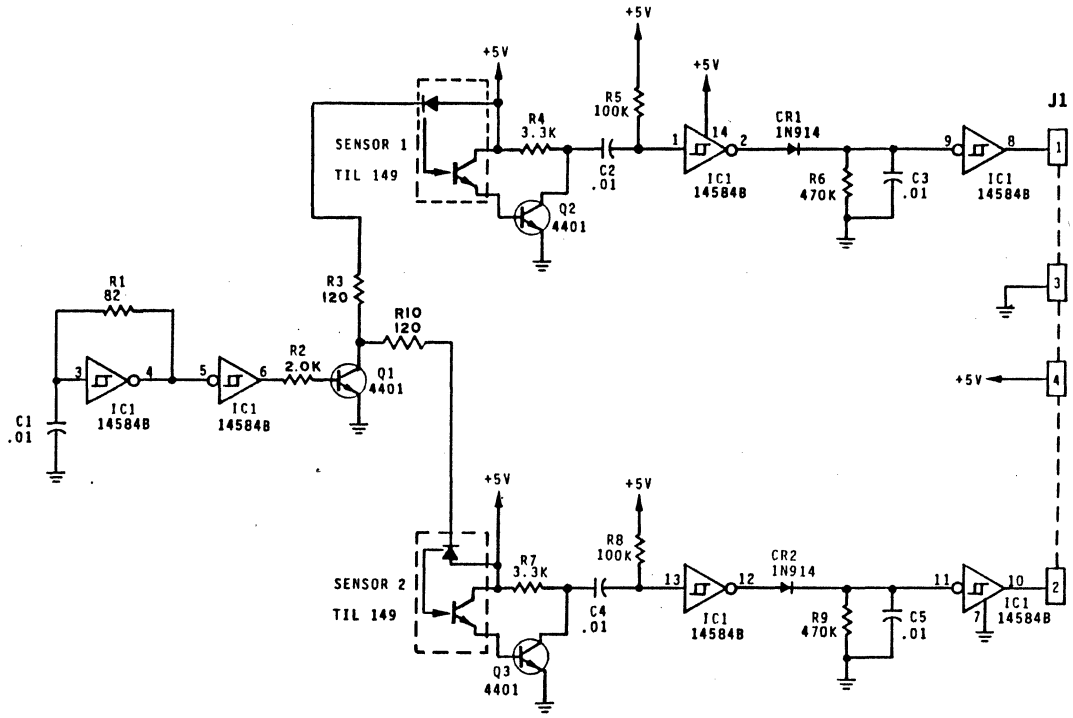



**Power Amplifier Type 5503**
**Schematic Diagram**




| REF DESIGNATOR | |
|---|---|
| LAST USED | NOT USED |
| C9 | |
| CR2 | |
| E2 | |
| IC3 | |
| R18 | |
| MT1 | |
| TP2 | |
| VR2 | |

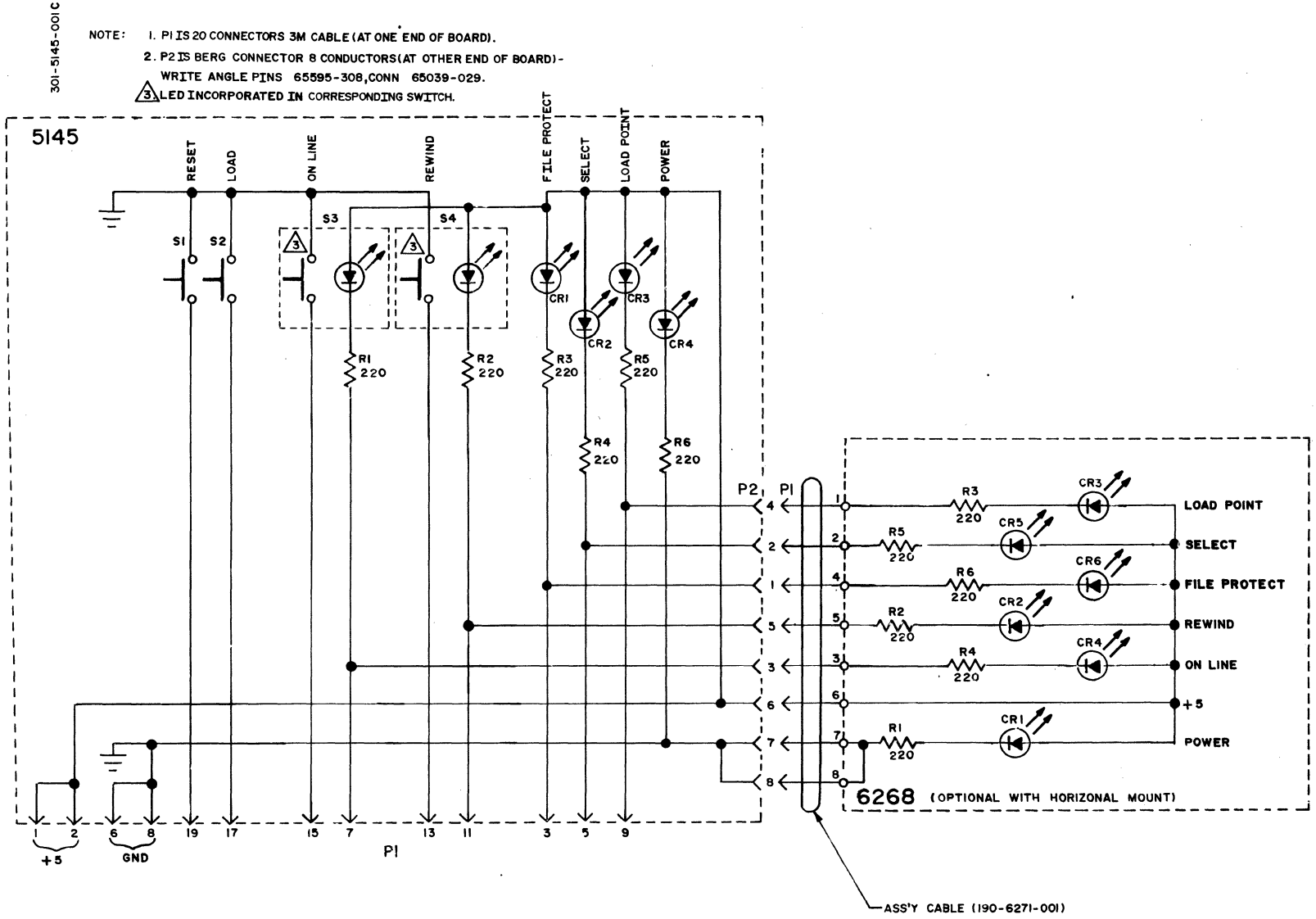
***Position Sensor***
***Type 5764***
***Schematic Diagram***

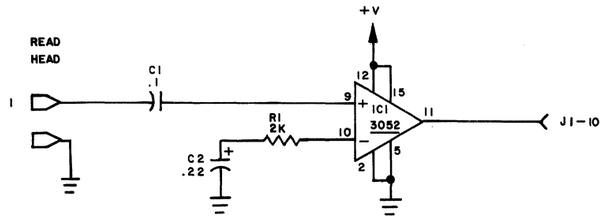


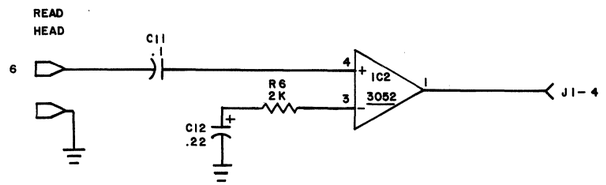

| REF DESIGNATOR BLOCK | |
|---|---|
| LAST USED | NOT USED |
| IC1 | |
| R10 | |
| C5 | |
| Q3 | |
| J1 | |
| | |

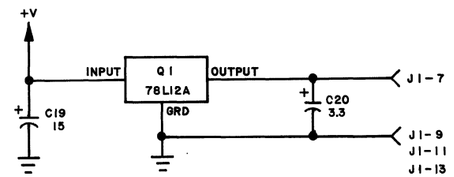
***Reel Sensor***
***5447 Schematic***

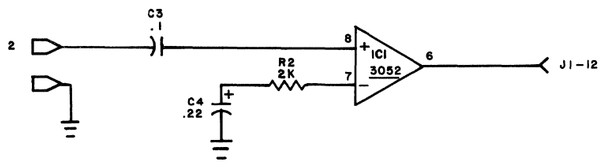
# Control Panel
## Type 5145
## Schematic Diagram

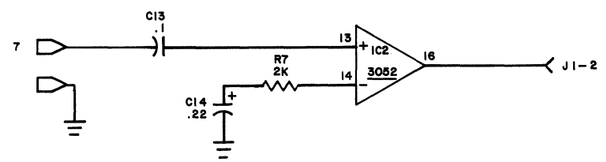


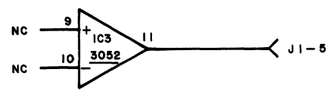


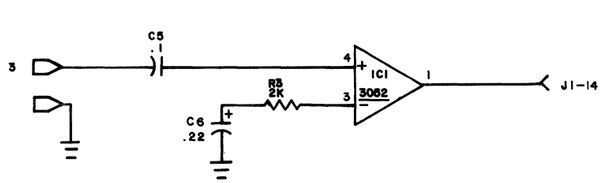



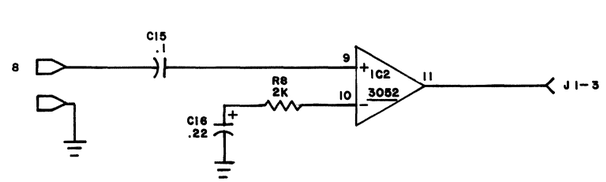



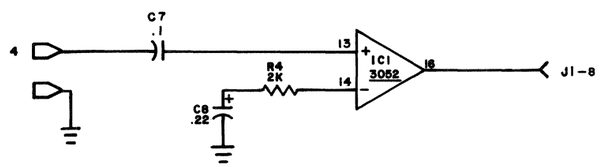



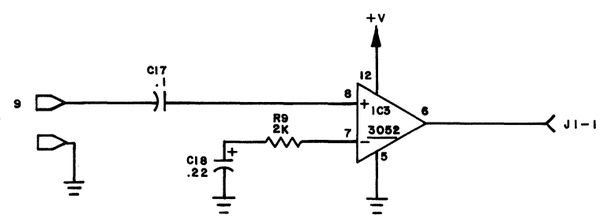



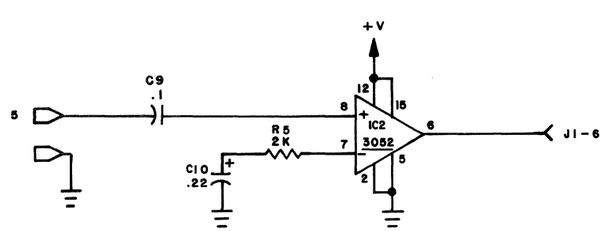




| REFERENCE DESIGNATORS | |
|---|---|
| LAST USED | NOT USED |
| IC3 | |
| C20 | |
| R9 | |
| J1 | |
| Q1 | |
| | |

***Pre-Amp***
***Type 5613-A***
***Schematic Diagram***

401-6470-001F

CH.3

CH.5

CH.7

WRT J1/14

J1/15 HIGH SPEED

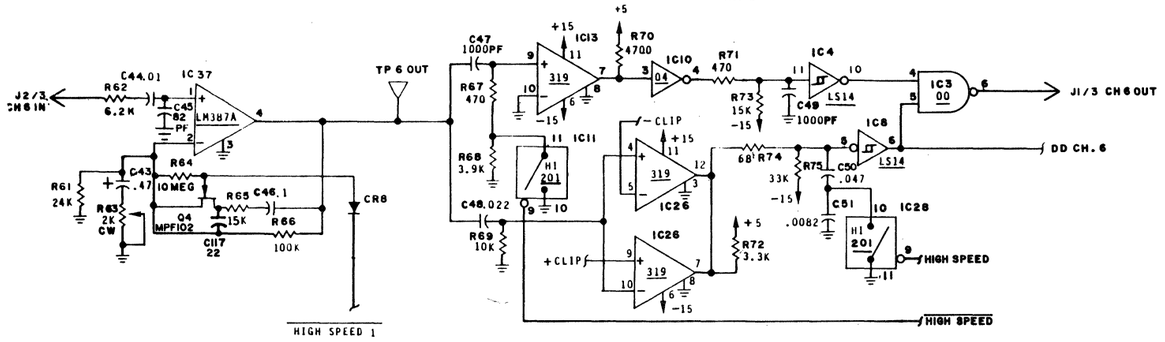
J1/13

J1/11 DATA DETECT

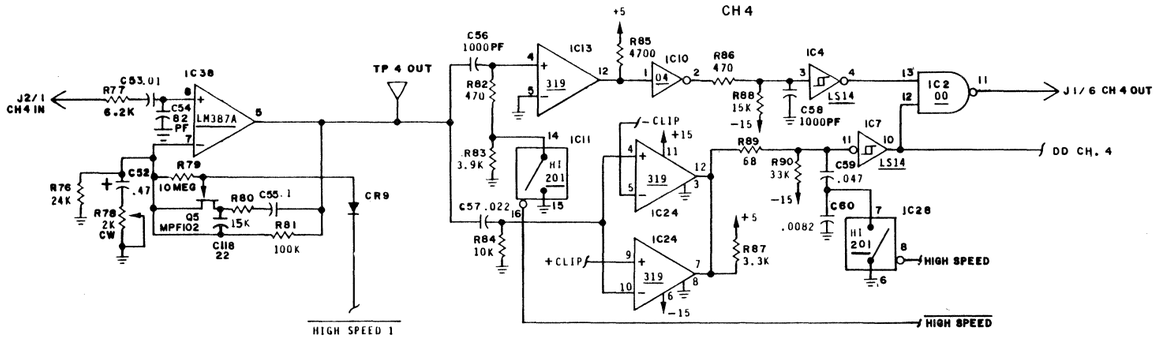
| REFERENCE DESIGNATION LAST USED | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| R | C | CR | IC | Q | J | P | L | TP | | |
| 151 | 122 | 13 | 40 | 9 | 3 | | | 7 | | |
| REFERENCE DESIGNATION NOT USED | | | | | | | | | | |
| R | C | CR | IC | Q | J | P | L | T | | |
| | | | | | | | | | | |
| | | | | | | | | | | |
| | | | | | | | | | | |
| | | | | | | | | | | |

***Read Amplifier***
***Type 6470 L***
***Sheet 1 of 3***

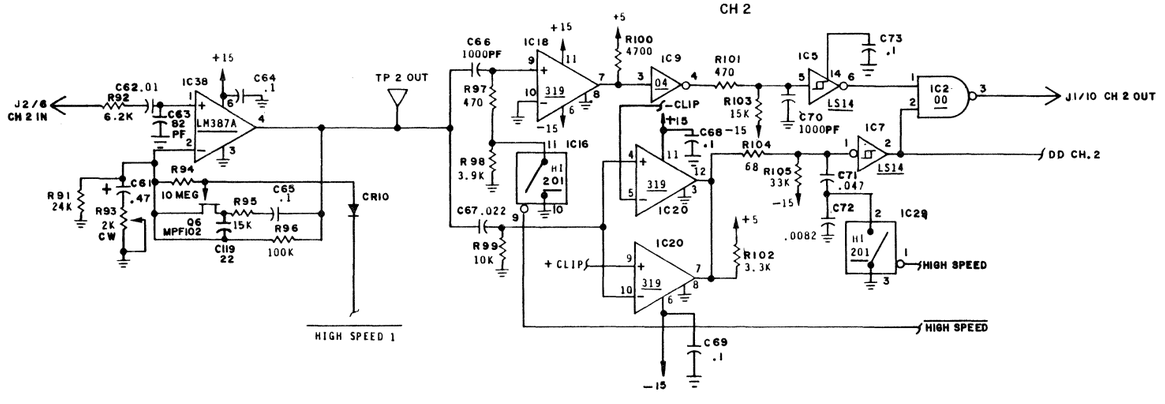
CH 6

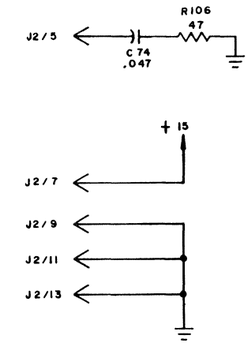


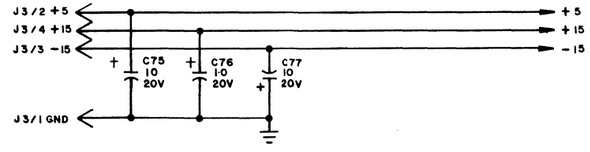

CH 4



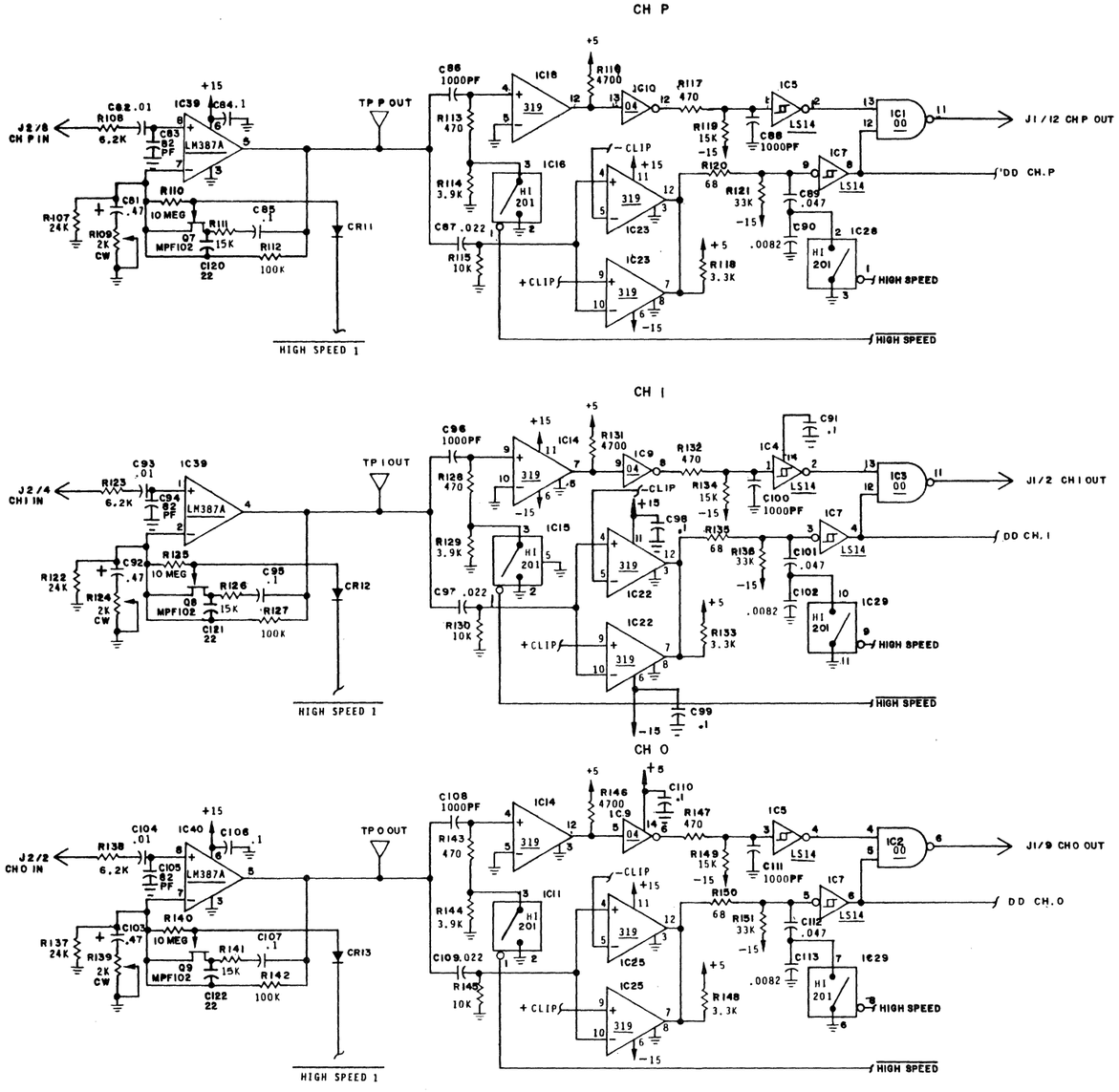

CH 2



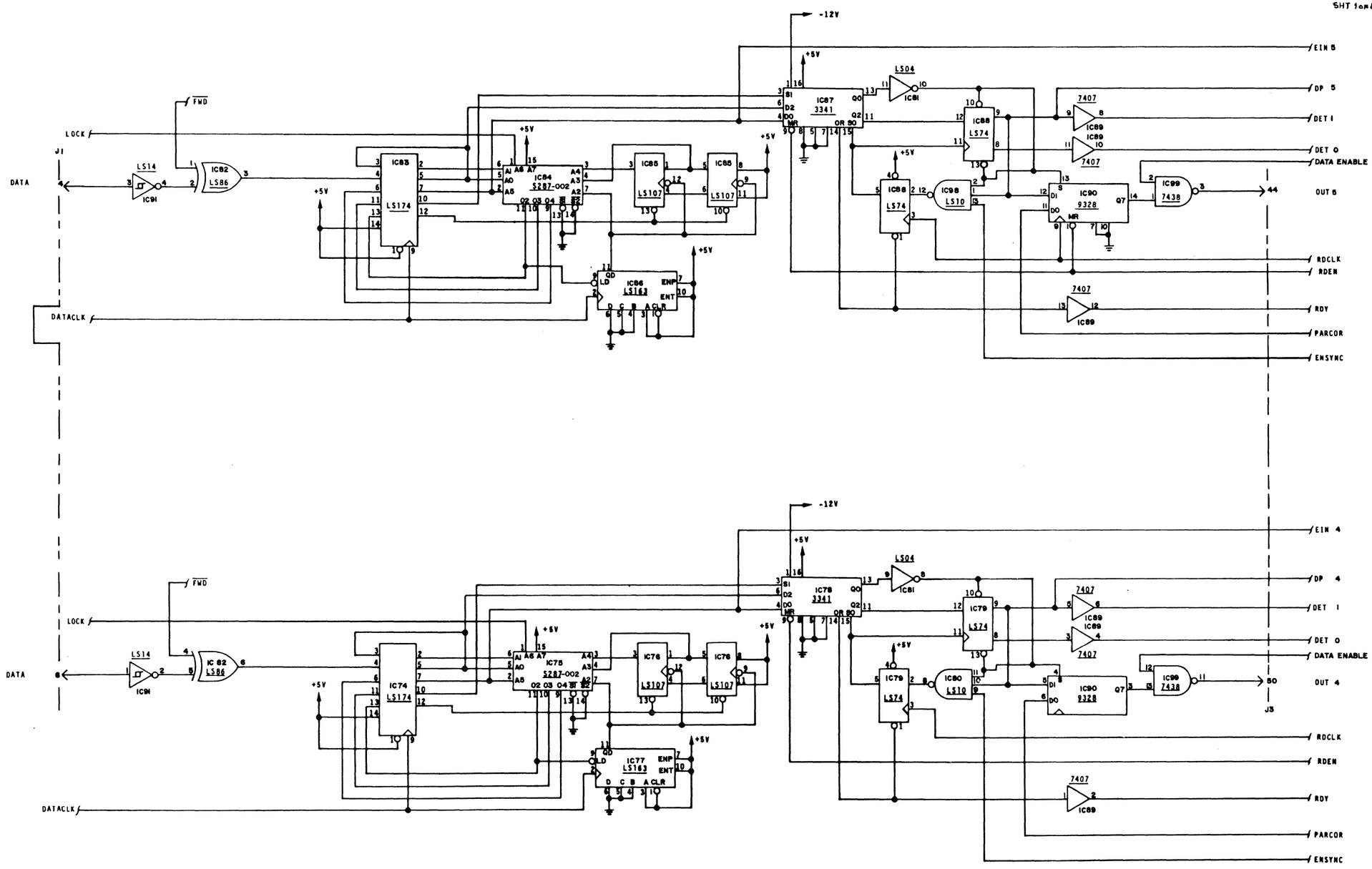




***Read Amplifier***
***Type 6470 L***
***Sheet 2 of 3***



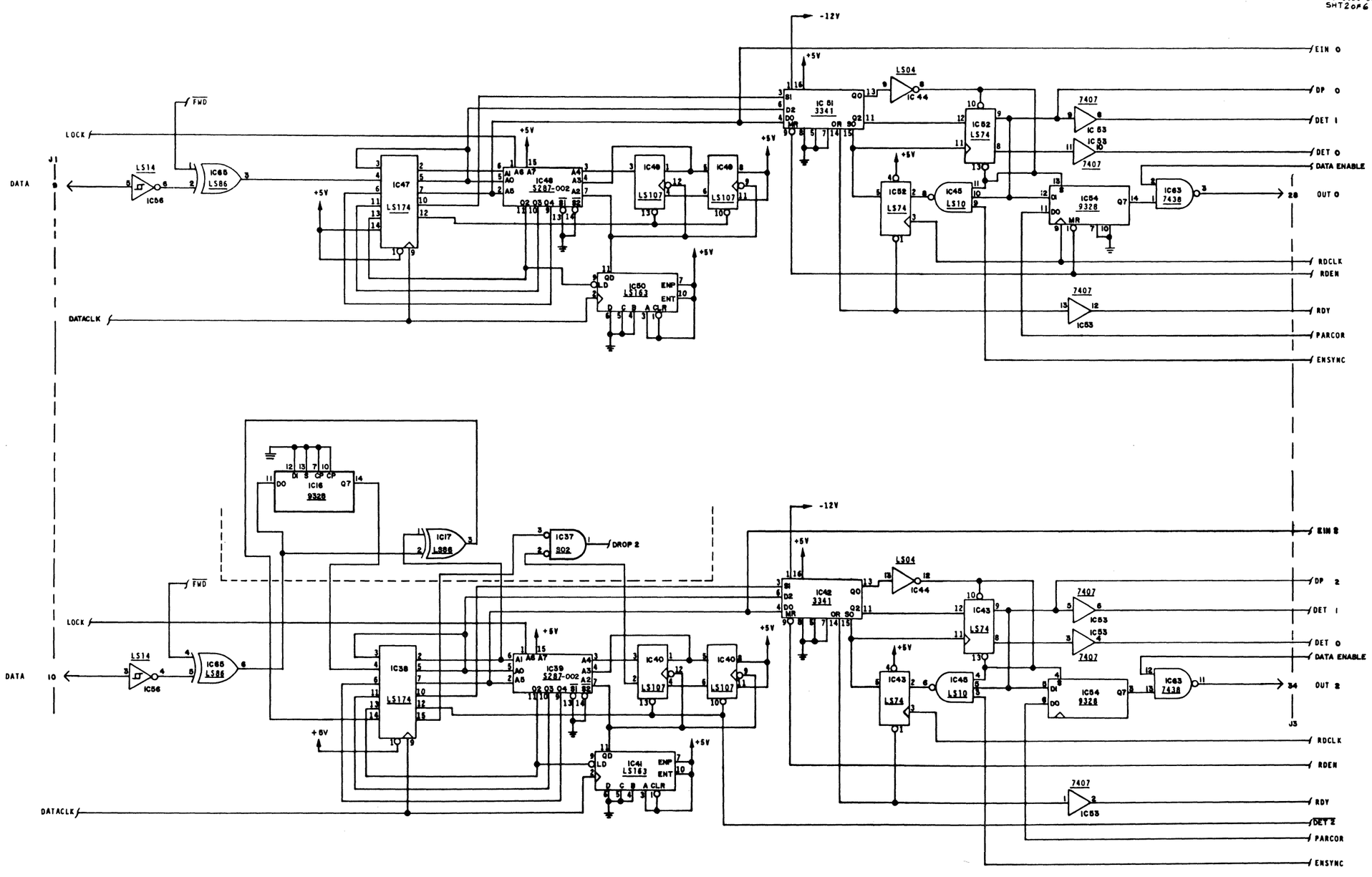

***Read Amplifier***
***Type 6470 L***
***Sheet 3 of 3***

401-5326-001 J
SHT 1 of 6



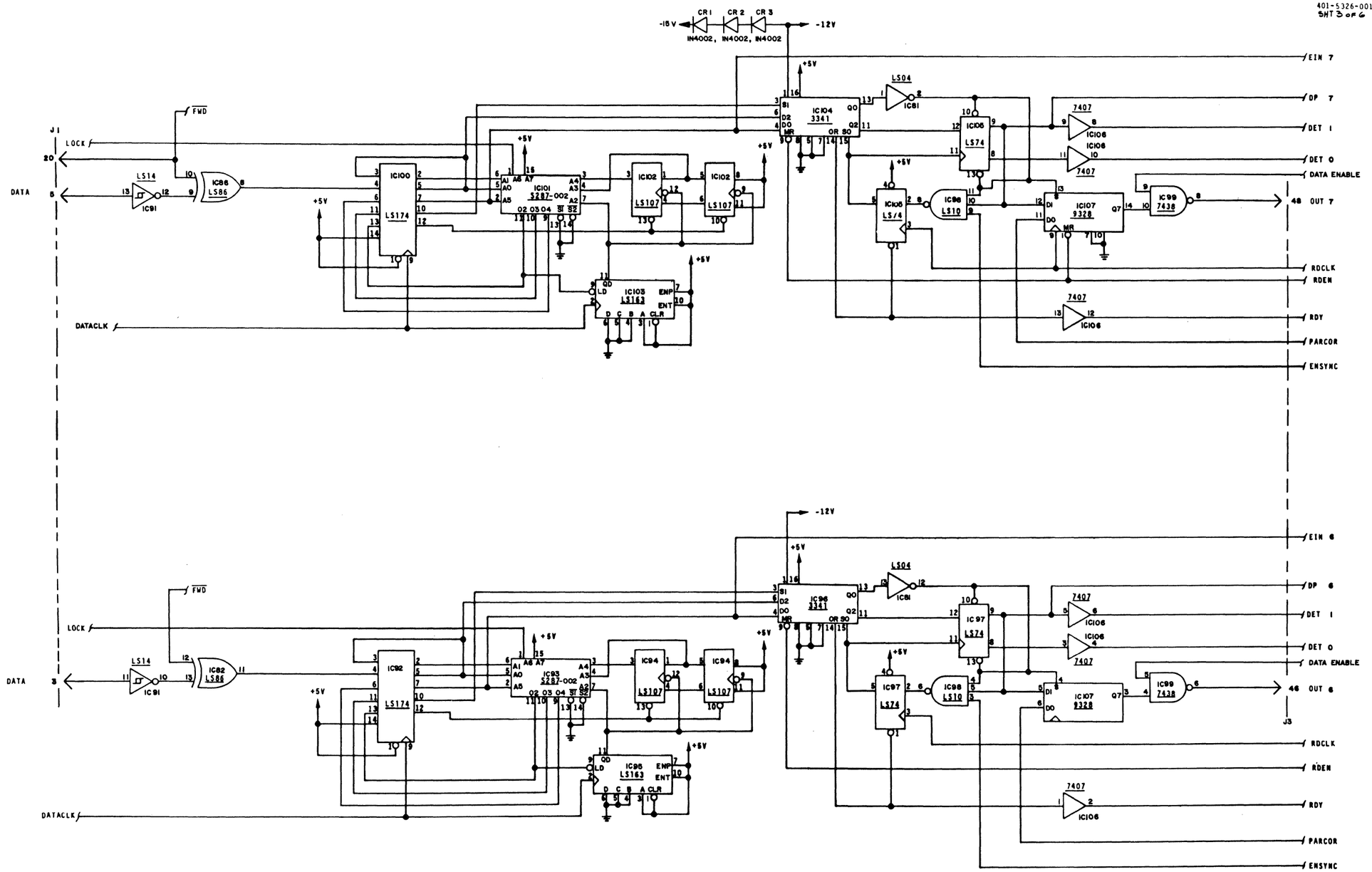

***P.E. Read***
***Type 5326 K***
***Schematic Diagram***

401-5326-001 J
SHT 2 OF 6



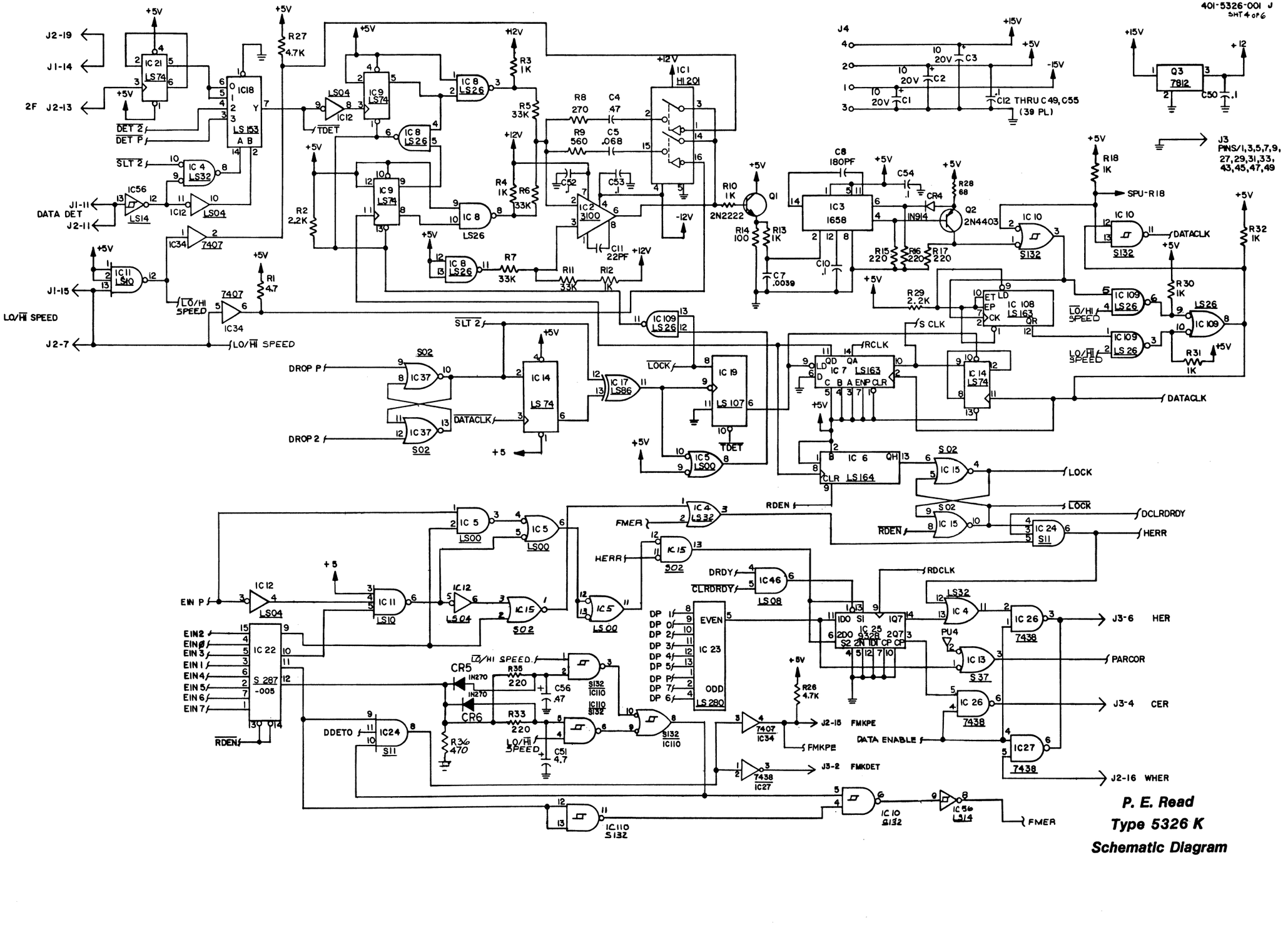

***P.E. Read***
***Type 5326 K***
***Schematic Diagram***

401-5326-001 J
SHT 3 OF 6



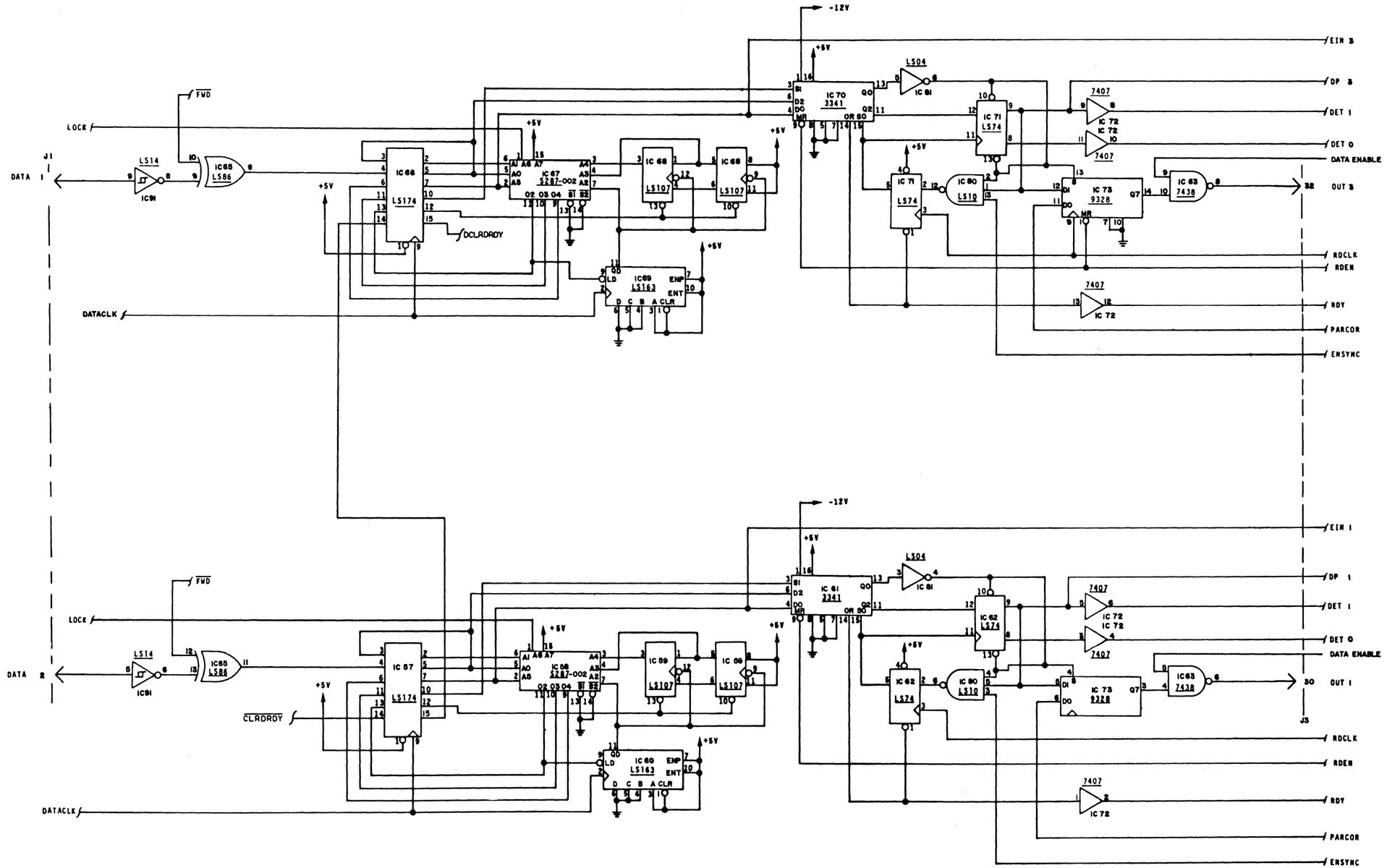

***P.E. Read***
***Type 5326 K***
***Schematic Diagram***

401-5326-001 J
SHT 4 OF 6



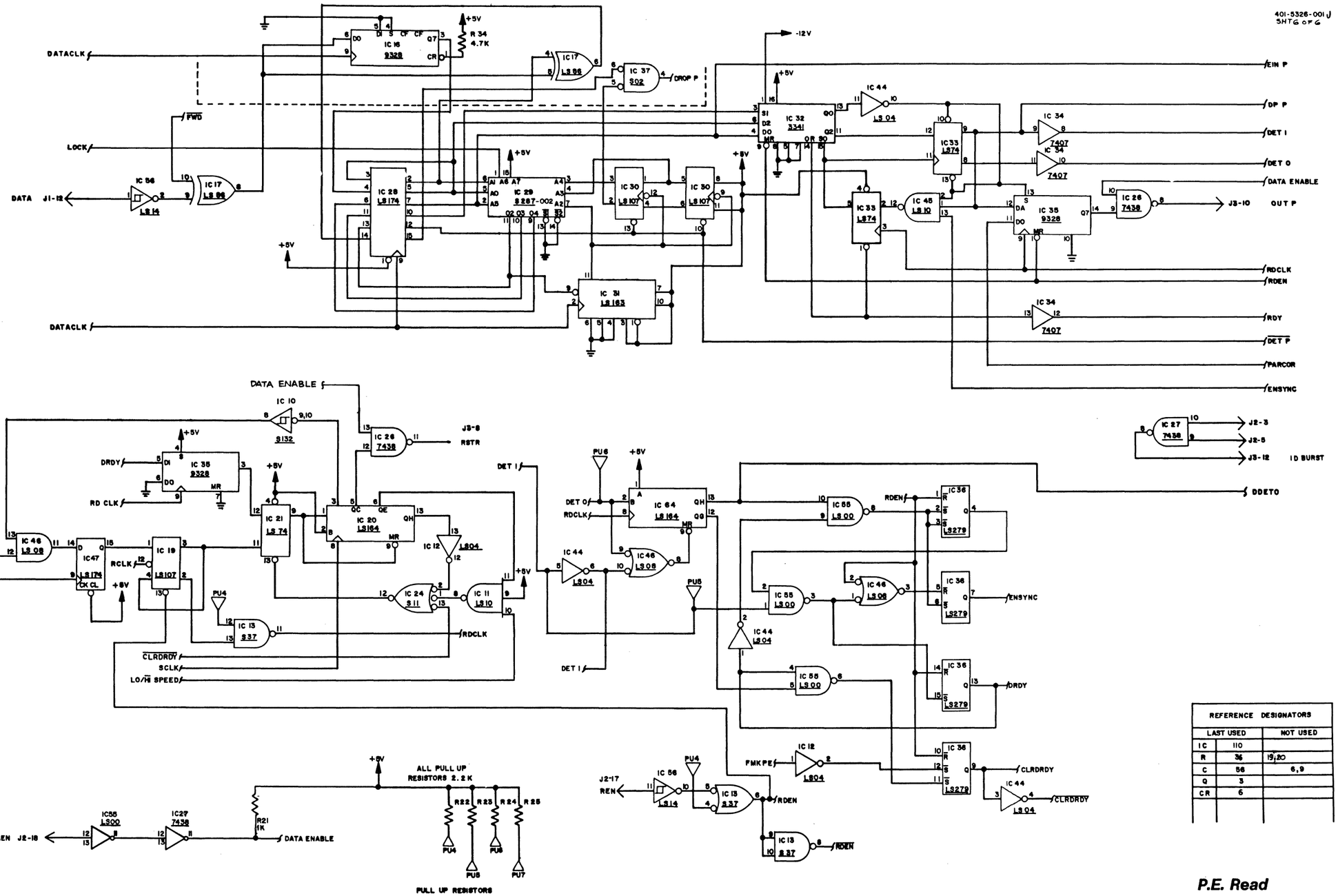

**P. E. Read**
**Type 5326 K**
**Schematic Diagram**

401-5326-001 J
SHT 5 OF 6




***P.E. Read***
***Type 5326 K***
***Schematic Diagram***

401-5326-001 J
SHTG OF 6



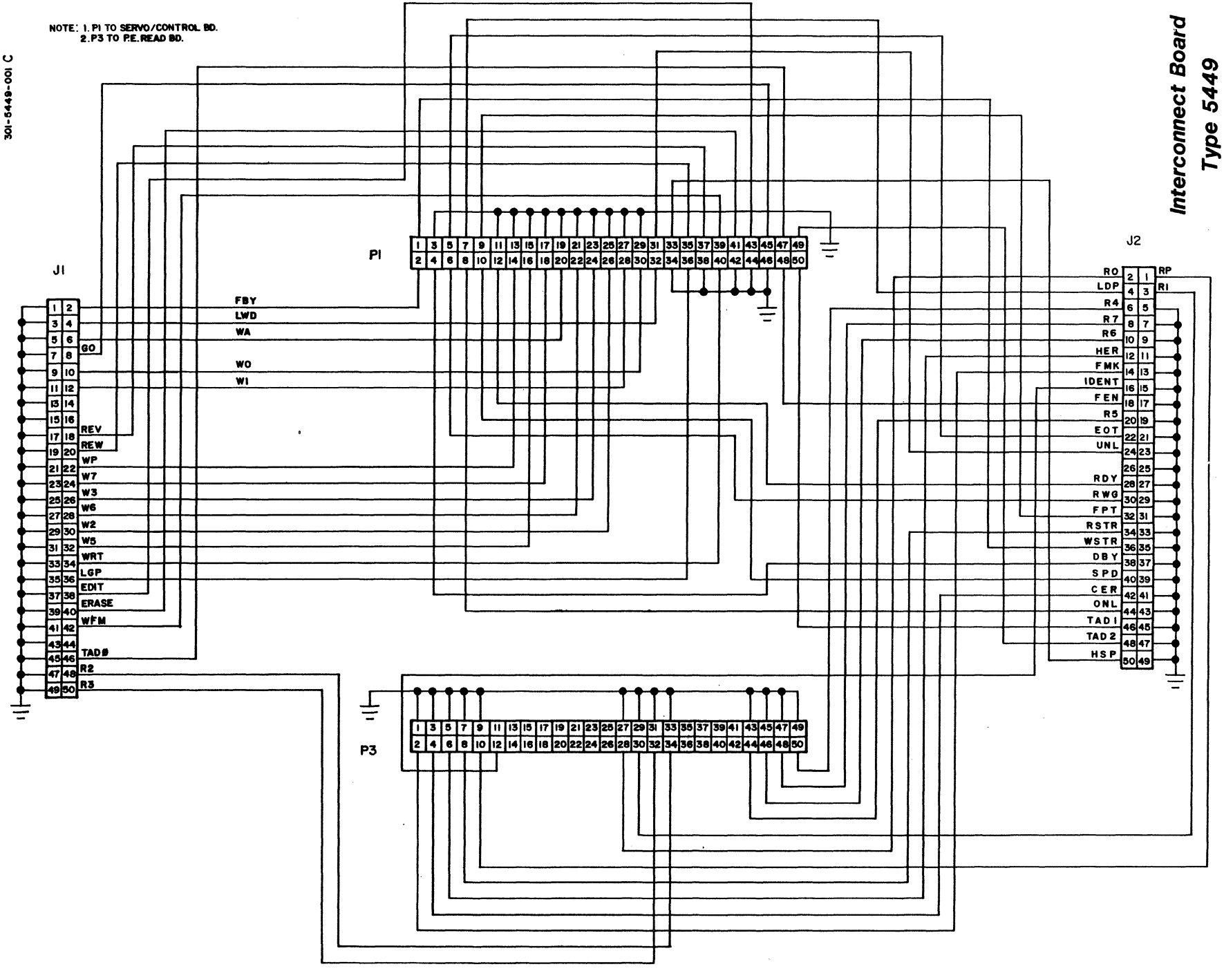

| REFERENCE DESIGNATORS | | |
|---|---|---|
| LAST USED | | NOT USED |
| IC | 110 | |
| R | 36 | 19,20 |
| C | 56 | 6,9 |
| Q | 3 | |
| CR | 6 | |
| | | |

***P.E. Read***
***Type 5326 K***
***Schematic Diagram***

# Interconnect Board Type 5449 Schematic Diagram

NOTE: 1. P1 TO SERVO/CONTROL BD.
2. P3 TO P.E. READ BD.

301-5449-001 C



# Warranty

The Company warrants its devices against faulty workmanship or the use of defective materials (except in those cases where the materials are supplied by OEM) for a period of one year from the date of shipment to OEM, with the exception of $\frac{1}{4}$" cartridge products which are warranted for a period of ninety (90) days.

The liability of the Company under this warranty is limited to replacing, repairing, or issuing credit (at the Company's discretion) for any devices which are returned by OEM during such period provided that (a) the Company is promptly notified in writing upon discovery of such defects by OEM; (b) the defective unit is returned to the Company, transportation charges prepaid by OEM; and (c) the Company's examination of such unit shall disclose to its satisfaction that such defects have not been caused by misuse, neglect, improper installation, repair alteration or accident.

Kennedy Company is continually striving to provide improved performance, value and reliability in its products and reserves the right to make these changes without being obligated to retrofit delivered equipment.

**KENNEDY**
*A Division of Shugart Corporation*