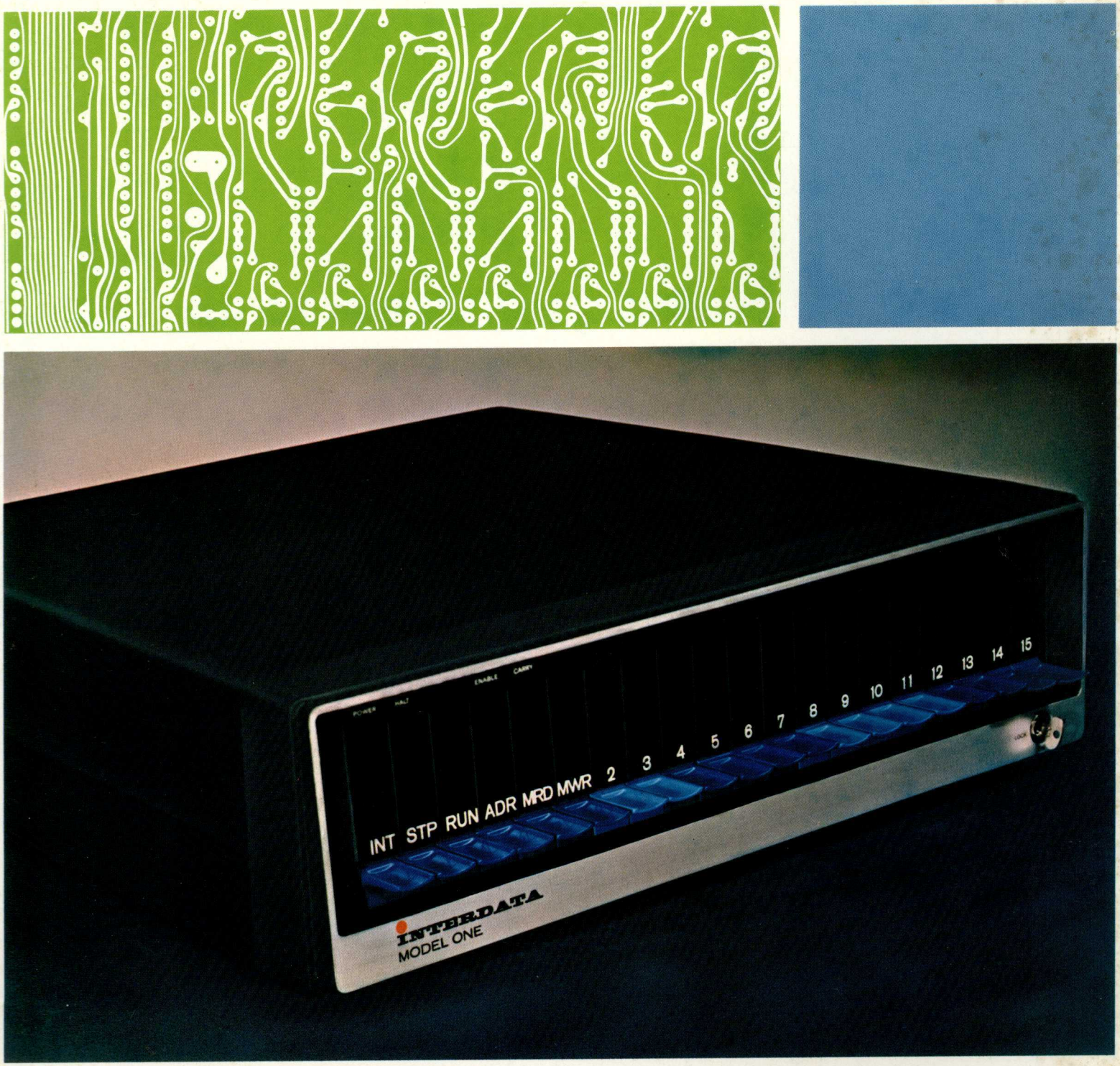


The Model One

INTERDATA®

Introduction

The INTERDATA Model 1 is a low cost computer designed specifically for use in dedicated application areas. The Model 1 was conceived from the same philosophy which made the INTERDATA Models 3 and 4 so successful. That approach was to utilize the latest state-of-the-art technology, coupled with advanced product architecture, to provide the user with the highest performing computer per dollar.

As a worldwide leader in the small computer industry, INTERDATA enjoys a position of prominence as a major supplier of small and medium size computer systems of the highest possible quality. This widespread acceptance by the user community is one of many reasons why you should consider INTERDATA first, before committing yourself to the purchase of ***any*** *computer.*

Model 1 Processor General Features

The INTERDATA Model 1 Processor is a physically small, high-speed, application-oriented, modular processor designed to provide maximum computing power at minimum cost to the user. Modular construction is used for ease of maintenance and to facilitate system configuration expansion to meet the future needs of the user. The Model 1 Processor is excellent for applications in diverse fields such as industrial monitoring and control, process control, data collection and data communications.

The Processor uses **eight and sixteen-bit instructions** for efficient coding and optimum core utilization in this class of mini-computers. Many of the instructions contain test and skip options for effective byte handling and loop control. Powerful **bit manipulating instructions** efficiently handle bit processing. A powerful **auto-indexing** feature enables the system to use a maximum of 8,192 index registers.

The memory system uses highly reliable **2,048 byte core modules** and is expandable to 16,384 bytes, with parity as an option. The cycle time is one microsecond. Plug-compatible, 2,048 byte, **Read-Only-Memory modules** may be intermixed with core modules for ultra-reliable, inexpensive and non-volatile program storage. The memory system is organized into 256 byte pages. Two pages, the Current Page and Page Zero, are directly addressable by the Primary Instruction Word. All remaining pages are addressed indirectly.

A Power Fail Safe option is provided for the prevention of data or program loss as a result of failures in the primary power source.

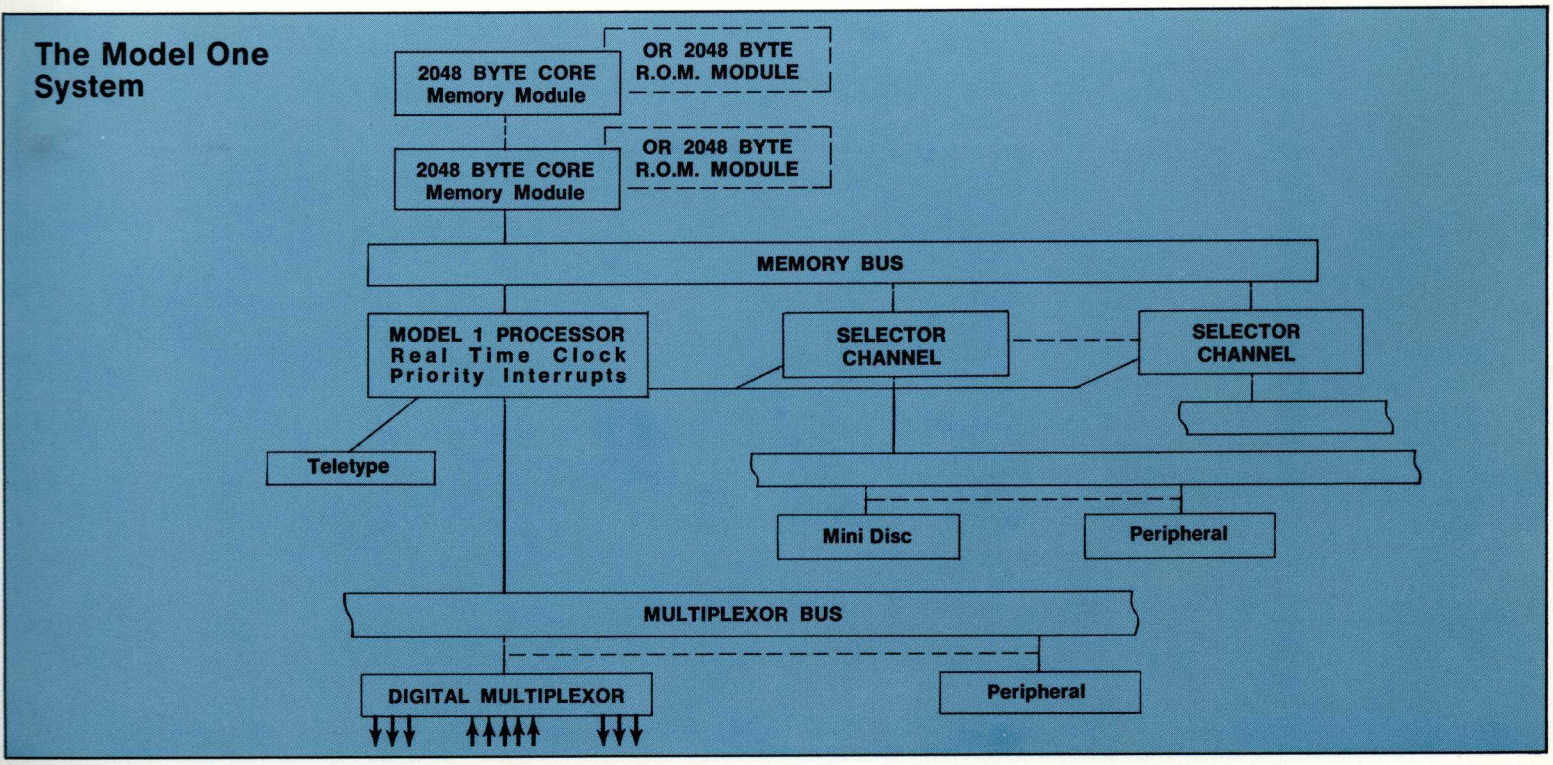
There are several ways for handling input/output transfers between the Model 1 Processor and up to 256 devices. The instruction set includes eight instructions for input/output in addition to Read Block, Write Block, and the Pulsed I/O instruction. The **Read Block and Write Block** instructions can transfer data at speeds up to 400,000 bytes per second. **The Pulsed I/O instruction** can specify any combination of three control pulses, thus providing a convenient and economical way for special interface design. For simultaneous input/output transfers and processing, up to a maximum of four **Direct Memory Access (DMA) Channels** can be added to the Processor. The DMA Channels cycle steal memory and operate at a maximum rate of 500,000 bytes per second. Two kinds of DMA Channels are available: The high speed **Selector Channel** using standard INTERDATA Device Controllers, and a **Universal Direct Memory Access Channel** for applications involving custom channel design.

The Model 1 Processor contains **four hardware priority external interrupt lines** as standard items. Four additional External Interrupt Lines are available as an option. All interrupt lines are individually maskable.

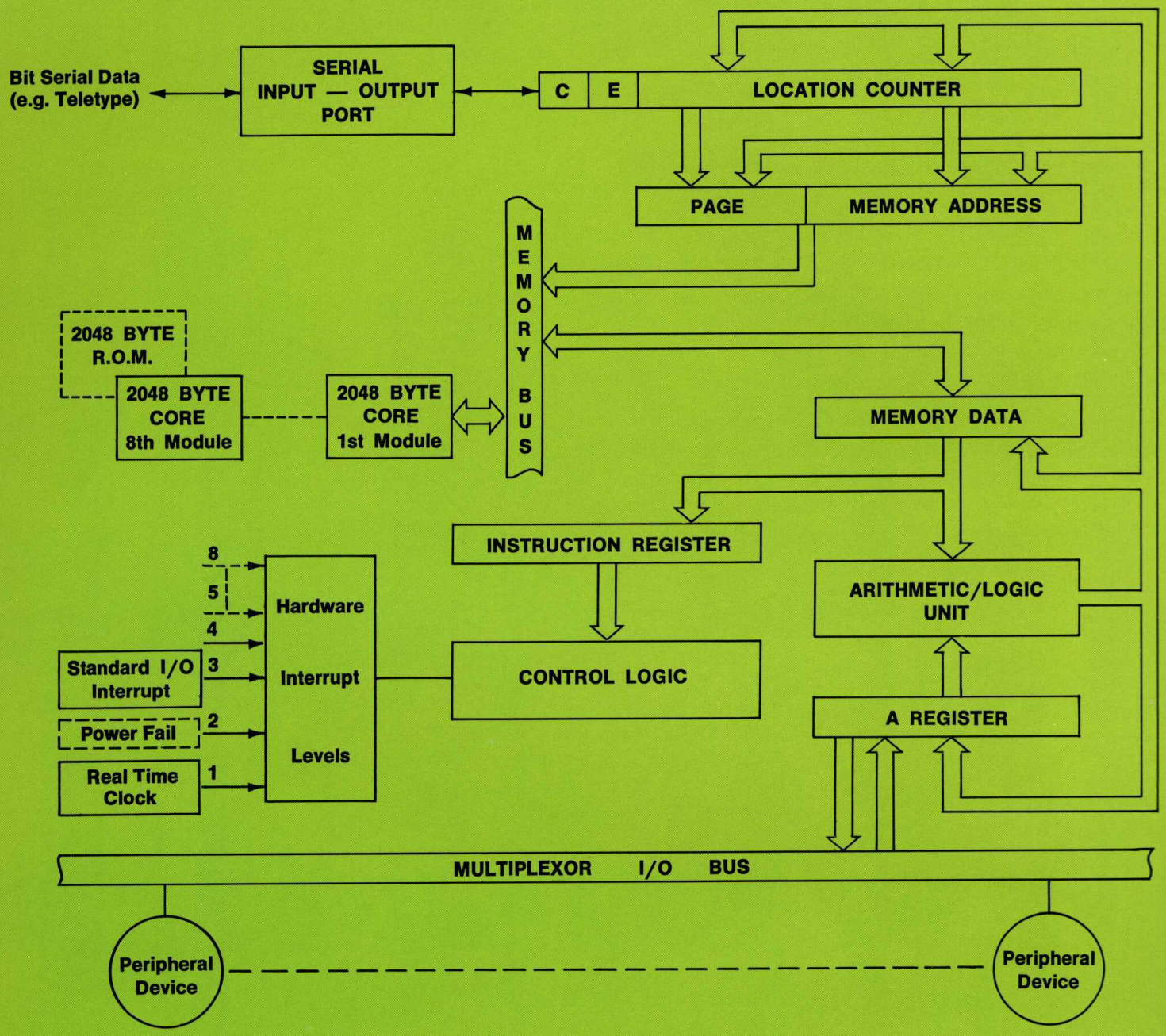
There is a **serial I/O port** on the standard Model 1 Processor which handles bit serial data streams such as those from Teletypewriters. The Processor uses the standard **one millisecond real time clock** to control the serial I/O port on input or output as well as providing a real time interrupt for application oriented software. The serial I/O port is interrupt driven and does not lock up the processor when it is in use.

The I/O Bus of the Model 1 Processor is hardware plug compatible with the I/O Bus of other INTERDATA Processors. A full line of peripheral controllers and system modules are available to support the Model 1 Processor.

The Model One System



The Model 1 Block Diagram



Block Diagram Description

The Model 1 Processor is an 8-bit parallel stored program processor which contains seven internal registers. All data transfers within the system are executed over 8-bit parallel paths.

Location Counter Bits 2:15 contain the memory location of the next program instruction to be executed. Bit 0 corresponds to the Carry flag which is used during arithmetic, shift, and certain bit and control instructions. Bit 1 corresponds to the External Interrupt Enable flag.

Page Register The Page Register contains the 6-bit memory page address.

Address Register The Address Register contains the memory byte address within a page.

Memory Data The Memory Data Register buffers data from the addressed memory location. It contains the second operand on arithmetic and logical instructions.

Accumulator The Accumulator Register contains the first operand on arithmetic and logical instructions and receives the result of such instructions. All bytes transferred over the Multiplexor Bus are transferred through the A Register.

Instruction Register The Instruction Register contains the current Program Instruction Word.

Word Formats and Instruction Set:

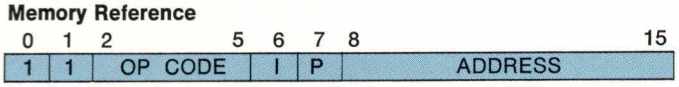
The Model 1 instructions fall into two broad categories:

Short Form (one byte)

Long Form (two bytes)

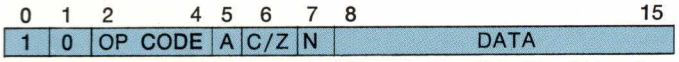
SIX INSTRUCTION FORMATS EXIST:

Memory Reference



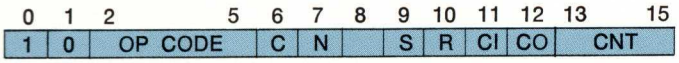
I = Indirect bit P = Page bit

Immediate



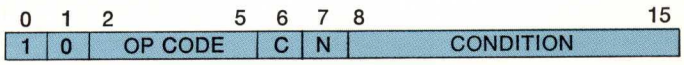
A = Result is not placed in A Register Z = Skip if not Zero*
C = Skip if no Carry* N = Skip if not Negative

Shift and Rotate



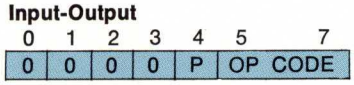
C = Skip if no Carry N = Skip if not Negative S = Shift
R = Rotate CI = Carry In CO = Carry Out CNT = Count

Command and Test



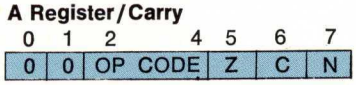
C = Skip if no Carry N = Skip if not Negative

Input-Output



P = Pulsed I/O

A Register/Carry



If A Register is referenced by OP CODE:

C = Skip if Carry is not set.

N = Skip if not Negative

Z = Skip if not Zero

If Carry is referenced by OP CODE:

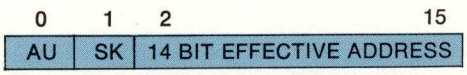
C = Test Carry Z & N = Carry modification codes

* Depends on OP CODE

Memory Referenced instructions operate in a paged memory environment. Each memory page contains 256 8-bit bytes of storage. The primary instruction word contains an 8 bit address and 2 bits to identify one of four possible addressing modes; DIRECT IN PAGE ZERO, DIRECT IN CURRENT PAGE, INDIRECT THROUGH PAGE ZERO, OR INDIRECT THROUGH THE CURRENT PAGE.

Indirect Memory Referenced instructions allow for a powerful auto-indexing feature with skip on page boundary capability. Any pair of adjacent bytes in core may be used as auto-index registers. If the most significant bit, bit 0 (AU) of the effective address is a one, the low order byte of the address is incremented before it is used. If bit 1 (SK) is also set the next instruction in the program is skipped when the auto index register crosses a page boundary.

The effective address in indirect addressing:



AU = Auto indexing SK = Skip Instruction

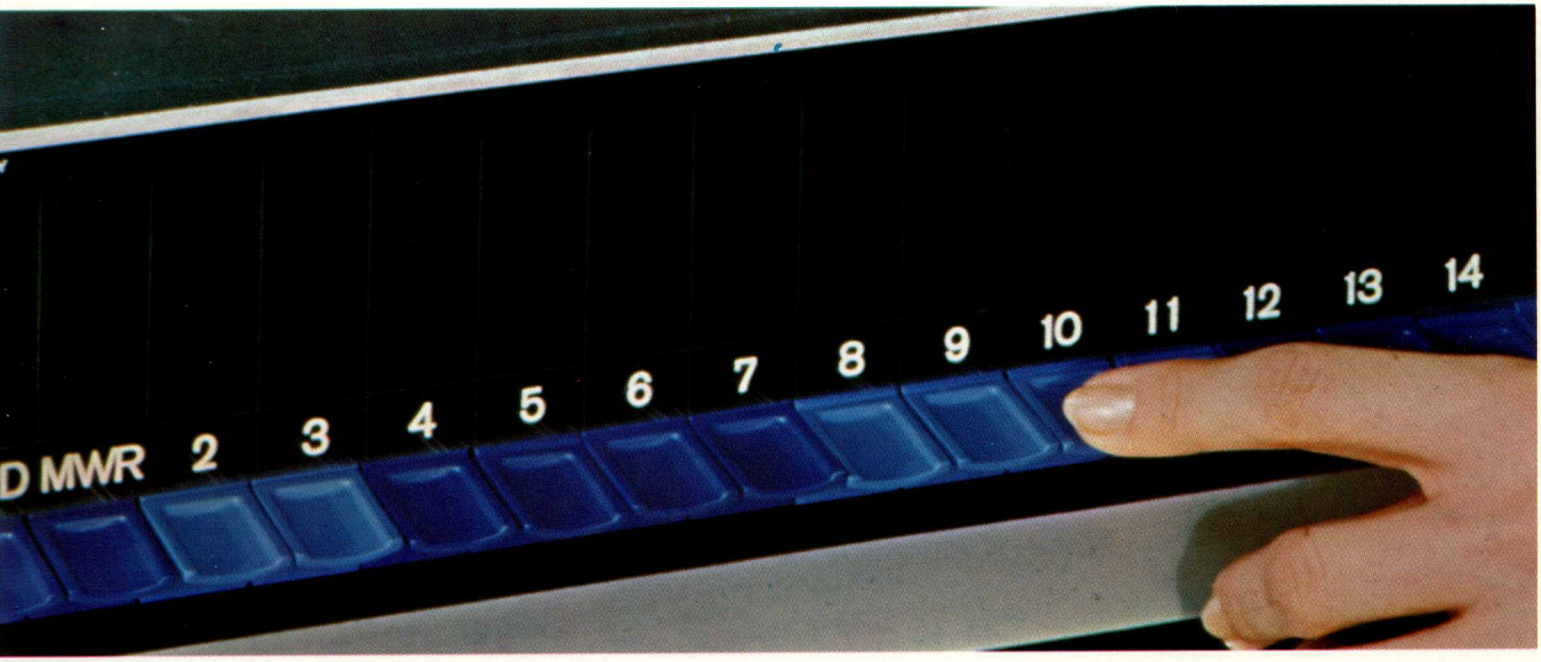
The Immediate Instructions reference the operand (DATA) directly as part of the instruction word, with a very powerful feature: depending on certain resultant conditions, the next instruction can be skipped and the result can be saved in the A Register or discarded.

The Shift and Rotate instructions are very flexible, and have full control over Carry In and Carry Out to facilitate multiple precision operations.

The Command and Test instructions enable the programmer to create or check a large number of conditions in the Processor.

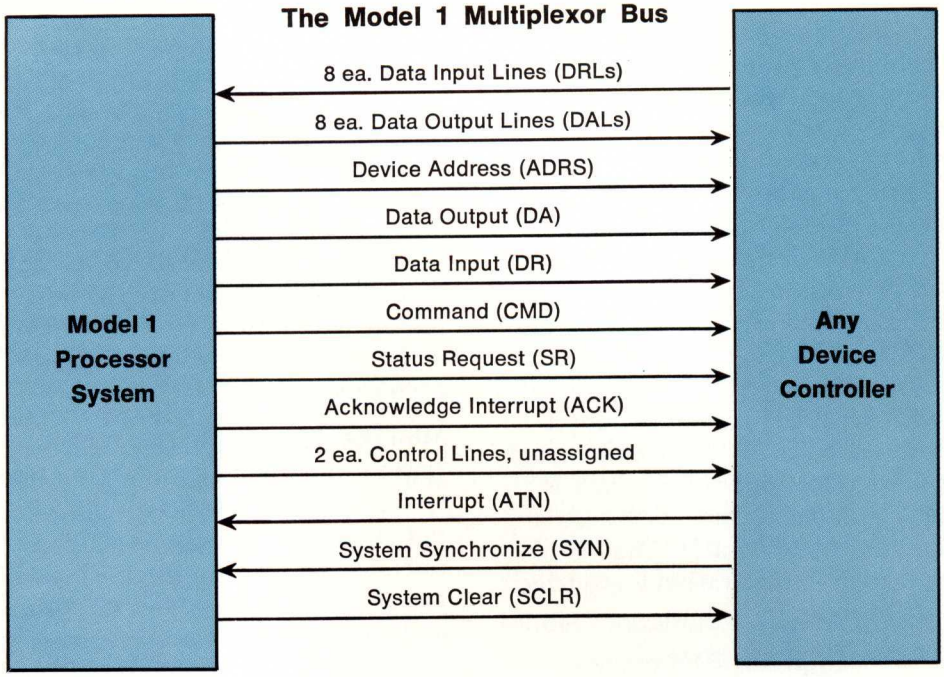
The Input-Output instructions facilitate byte transfers to and from the Processor, control command lines to the device, monitor status lines from the device and identify the source of interrupts in the input-output environment. The Pulsed I/O instruction eases timing problems in custom interface design for most applications.

The A Register/Carry instructions provide the programmer with a flexible tool to make decisions on the result of the previous operation.



List of Instructions

Class	Instruction	Mnemonic
Memory Reference	Add	A
	And	N
	And Bit	NB
	Branch & Link	BAL
	Branch on Condition	B
	Compare Equal	CE
	Compare Low	CL
	Exclusive Or	X
	Increment Core & Skip If Zero	ISZ
	Increment Core & Skip If Not Zero	INZ
	Load	L
	Or	O
	Or Bit	OB
	Read Block	RB
	Subtract	S
	Store	ST
	Write Block	WB
Immediate	Add Immediate	AI
	And Immediate	NI
	Compare Equal Immediate	CEI
	Compare Low Immediate	CLI
	Exclusive or Immediate	XI
	Load Immediate	LI
	Or Immediate	OI
	Subtract Immediate	SI
Shift and Rotate	Rotate	RT
	Shift	SH
Command and Test	Command	C
	Test	T
Input-Output	Address	ADR
	Acknowledge Interrupt	AK
	Output Command	OC
	Pulsed I/O	PIO
	Read Block	RB
	Read Data	RD
	Read Data & Skip	RDS
	Sense Status	SS
	Write Block	WB
	Write Data	WD
	Write Data & Skip	WDS
A Register/Carry	Add A to A	AA
	Add 1 to A	AO
	Complement A	CA
	Complement Carry	CC
	Clear A	CLR
	No Operation	NOP
	Reset Carry	RC
	Set Carry	SC
	Test and Skip	TS



The Model 1's Input-Output Characteristics

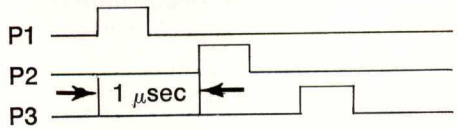
Full compatibility with all system modules and device controllers that are designed for INTERDATA systems makes the Model 1 Processor the easiest machine to interface.

The basic Model 1 Input-Output system includes four hardware priority interrupts, which is expandable to eight, and is supported by both byte and block oriented instructions. When expanding the system, the expansion slots can be used for either memory or input-output modules, resulting in efficient utilization of rack space. The Multiplexor Bus is byte (8 bit) oriented, and request/response in nature, to allow simple, straight forward and reliable interface operation. The Model 1 Processor can communicate with up to 256 devices either in the Interrupt Control or Status Monitored Mode.

The Multiplexor Bus consists of 27 lines: 8 Data Request Lines (DRL), 8 Data Output Lines (DAL), 8 Control Lines, and the System Synchronize (SYN), Interrupt (ATN) and System Clear (SCLR) lines. The System Synchronize (SYN) signal is a response generated after a control line activates. Each control line has a specific task, e.g.: control line 0 (ADRS) gates a device address from the Data Output Lines (DAL) to address a device controller. Other control lines initiate the functions of Data Output (DA), Data Request (DR), Command byte to the device (CMD), Status Request from a device (SR), and Acknowledge Interrupt (ACK). Unlike the other control signals, the "Acknowledge Interrupt (ACK)" daisy chains through all controllers, the highest priority first, checking for software enabled and queued interrupts. If there is one pending, the device number is automatically returned to the Processor making interrupt controlled input output easy for the programmer.

The "Pulsed I/O" instruction generates any combination of three pulses (P1, P2 and P3) as specified by the instruction itself. This feature can simplify timing logic in interface design. The pulses are 0.5 μsec in duration, and are 1 μsec apart, leading edge to leading edge.

Pulses generated by the "Pulsed I/O" instruction



For applications requiring either high transfer rates or simultaneous input-output and computing capability, up to four Selector Channels may be added to the Model 1 system. The Selector Channels transfer blocks of data between memory and the input-output device, independently from the Processor, on a true core cycle stealing basis. The transfer can approach a rate of 500,000 bytes per second and is terminated with an interrupt to the Processor. A Universal Direct Memory Access Channel is also provided for Model 1 systems for applications involving customized channel designs.

Model 1 Peripherals

An outstanding line of peripherals is behind the Model 1. All system modules and device controllers that were designed for the Models 2, 3 and 4 are also plug and hardware compatible with this Processor. Each of these modules and device controllers are total designs, to handle not only conversions, buffering, timing, device commands and status, but also interrupts that can be enabled or disabled by the program. This broad line of peripherals includes peripherals that INTERDATA developed and optimized for applications, such as the Digital Multiplexor for industrial monitoring and control. The following is an example of what is available for the Model 1:

Digital Multiplexor: This provides a very economical set of modular building blocks to monitor or control up to 2048 lines with a single controller using input or output modules of 128 lines. These modules can be intermixed in any fashion. The Digital Multiplexor utilizes a biased core technique to insure absolute DC isolation from the sense contact and an excellent common mode transient response and DC offset capability. These features make the unit particularly suitable for use in noisy environments.

Cassette Tape System: This system provides a reliable and inexpensive substitute for paper tape input-output equipment. The transfer rate is 300 characters per second, with up to 250K bytes of storage for each cassette.

Mini Disc System: This is a rugged, reliable and inexpensive mass storage system with 51.2K bytes of storage per disc. Up to two discs can be operated on each controller. Average access time is 8.5 milliseconds and the transfer rate is 60K bytes per second. The unit operates over a wide temperature range.

Drums and Magnetic Tapes: Fast access bulk storage media is offered in 131KB to 8.3MB sizes. Average transfer rates are 230KB/second with 8.7 and 17.4 microsecond average access times. IBM compatible seven and nine track tape transports are available for the Model 1 with 25 ips speed and densities of 556 and 800 bpi.

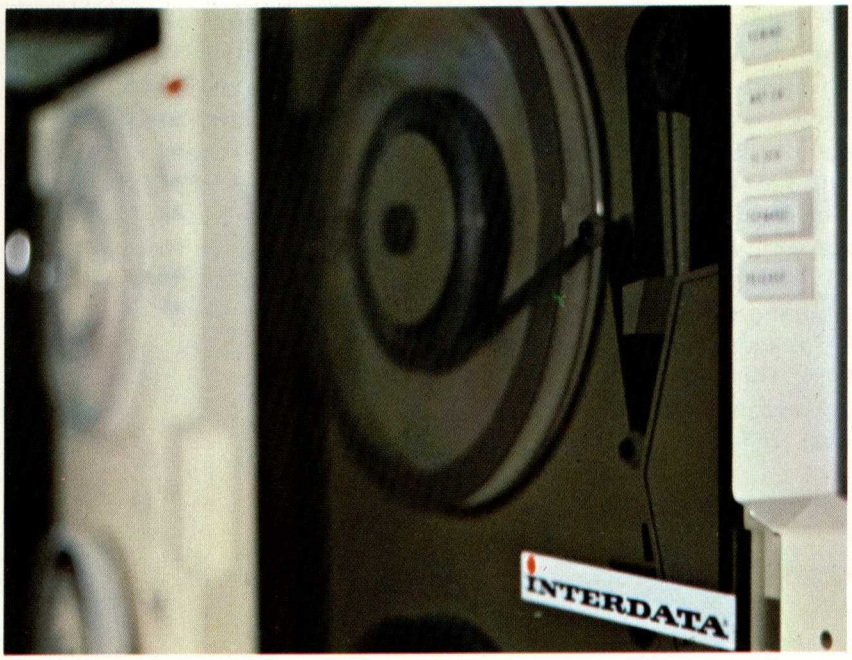
Data Communications Equipment: Character buffered adapters are available with various options to Bell 103, 201, 202, 301 Data Sets and the 801 Automatic Dialer to provide a broad capability for remote applications with synchronous or asynchronous communications requirements.

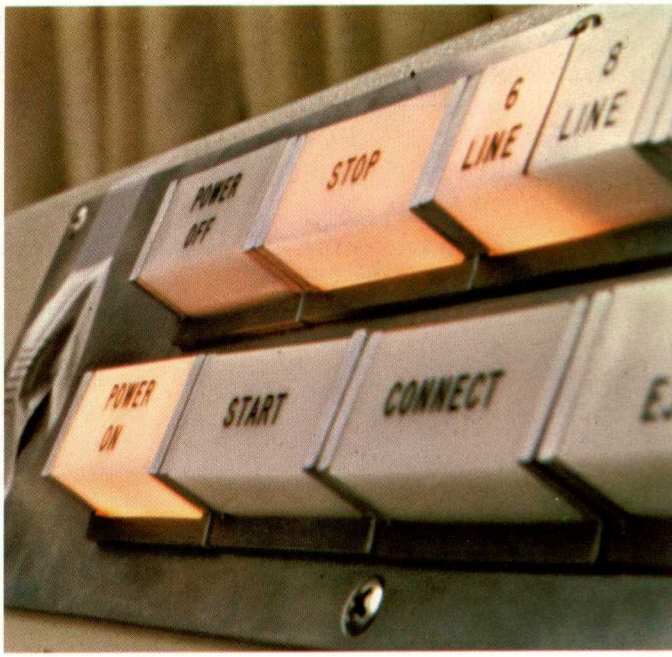
Paper Tape Equipment: A 300 cps Reader and 60 cps Punch are offered for the Model 1, individually, or as a complete package. Fan-fold tape is featured as the software media.

Line Printer: The Line Printer provides 300 lpm capability with 132 columns per line and 64 characters. Ideally suited to fulfill your high speed listing requirements.

Card Reader: A 200 cpm reader is provided for card oriented input systems.

System Modules: These modules provide the user with a group of general interfaces to reduce or eliminate design effort. As an example, modules are provided to handle 8 bit or 16 bit parallel input or output, manual data entry and decimal indicators in 4 or 8 decades.





Model 1 Software

The Model 1 is supported with a total programming package to make the programmer's job easier. Basic software tools are not the only ones provided. In addition to the Assembler, Editor, Debug, Loader and Diagnostic packages, INTERDATA provides a Monitor that ties all these software packages together into a total entity. Application programs, like the Events Monitor are also here — to make **your** job easier. INTERDATA has not forgotten its present users, however. For their convenience, a Model 1 Simulator and Assembler is ready to be run on Models 3, 4 and 5.

Assembler: The Model 1 Assembler allows the user to write efficient and time-saving symbolic programs, which can be translated into Model 1 machine coding. The Assembler accepts a source deck or tape consisting of user-coded instructions, and outputs a source listing and a binary program object tape which can be loaded and executed by the Model 1 Loader.

The Assembler is designed to operate with a minimum of 4K bytes of memory. Assemblies are completed with 2 passes of the source medium through the resident assembler. The Assembler can be adapted to any configuration of I/O devices to optimize assembly speed. In addition to op-code mnemonics, the assembler has the capability of accepting up to 6 characters in user symbols. It can also decode instruction modifier mnemonics and has a flexible constant definition format.

Model 1 Text Editor: The Model 1 Text Editor is a support program for the Assembler used in the preparation and update of source program tapes. It is an interactive, teletype controlled program, but can use the high speed paper tape devices for input and output. The functions include adding, modifying, deleting and copying of paper tape records. Tapes can be punched in assembly format or non-edited format for use as input for user programs. The Text Editor keyboard commands easily facilitate error correction and record or character manipulation.

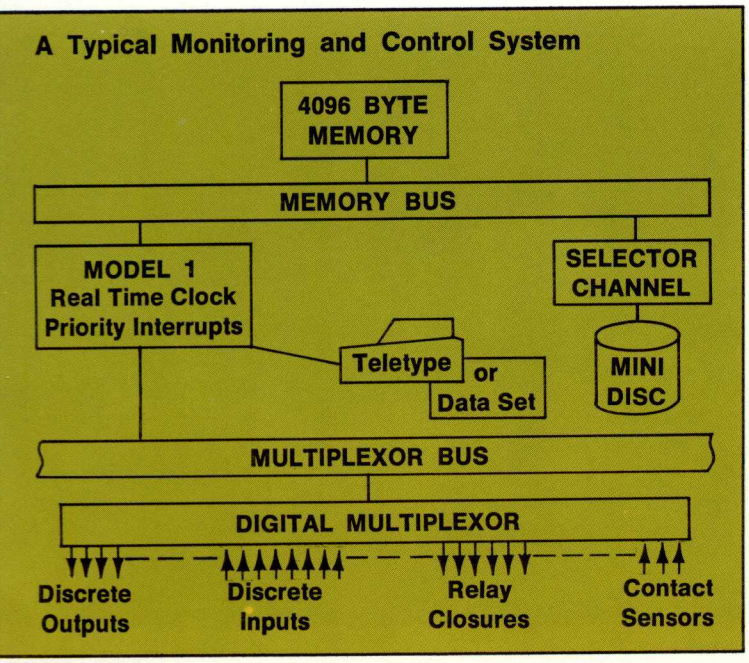
Model 1 Debug (Club): Model 1 Debug (Club) is an interactive hexadecimal debugging aid that contains many valuable program testing features. Among these are the display and modification of memory locations, and, the accumulator. Also included is a breakpoint feature which allows the user to set, reset, and recognize breakpoints throughout his logic and enter his program at any point.

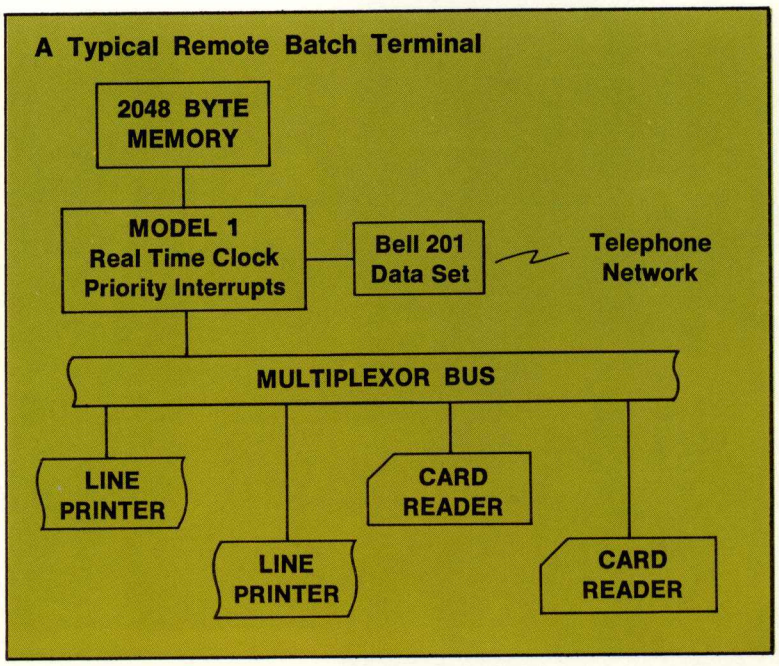
Model 1 Loader: The Model 1 loader is a page-relocatable re-entrant program which loads absolute object tapes output from the Assembler. The Loader itself is loaded by a bootstrap loader in core. The Model 1 Loader performs a check sum on tapes it loads and automatically transfers to the start of the user program.

Model 1 Diagnostics: The Model 1 Processor and Memory Test is a diagnostic which checks the execution and validity of all Model 1 machine instructions including modifiers and core memory with worst case patterns. Error messages result from any hardware discrepancies. The program repeats execution until halted or an error is discovered. Test programs are also provided for the peripheral devices to validate the controller's and device's operational status.

Model 1 Monitor: This Monitor will handle the loading of main programs and subroutine packages via on-line user requests. Additionally I/O Control is available to the user to provide I/O operations with software buffering by means of simple user I/O requests, plus a set of interrupt driven I/O drivers to perform I/O operations on all Model 1 supported peripheral devices.

A separate program will be available to generate the Model 1 Monitor tape for particular hardware configurations.





Events Monitor: This system will allow the user to specify an array which will contain preset data values for the external devices it wishes to monitor. The system will continuously check to determine if the value read differs from the preset value by more than a user specified tolerance and if so, it will transfer control through a vector table to a user specified routine to take action. The tolerance values are preset and contained in an array of a size equal to the preset data values. All of these values can be modified by the user via Teletype commands. In case of an error condition, control may be given to the teletype, or return to the events monitor.

Model 3, 4, 5 / Model 1 Assembler: This program assembles Model 1 symbolic code into Model 1 object code as was described for the Model 1 Assembler. This software however runs on the INTERDATA Models 3, 4 and 5 with 8K bytes of memory for the convenience of these users.

Model 1 Simulator: This interactive software package enables the user to execute and test Model 1 object programs on an INTERDATA Model 3, 4 and 5 Processor with 8K bytes of memory. This program has also been provided for the convenience of these users.

Supporting the Customer

INTERDATA provides training courses on a year-round basis at several levels: system planning seminars, maintenance, and programming. If desired, special courses are presented at the customer's own facility.

Field Service: INTERDATA maintains Field Service Engineers across the country with headquarters in each of the regional sales offices. All of the INTERDATA field service personnel are factory trained and have experience with dozens of installations. At the INTERDATA factory, back-up service is available and a repair depot is maintained there for logic boards and memory packages.

In the field, maintenance personnel are equipped with complete sets of spares and with specialized diagnostic equipment.

Working behind all this, is the factory Quality Control team which maintains exacting standards for production and final checkout. A customer's system is given hours of running tests and then, finally, "baked" in a heat chamber for a number of additional hours before the system is certified and shipped.

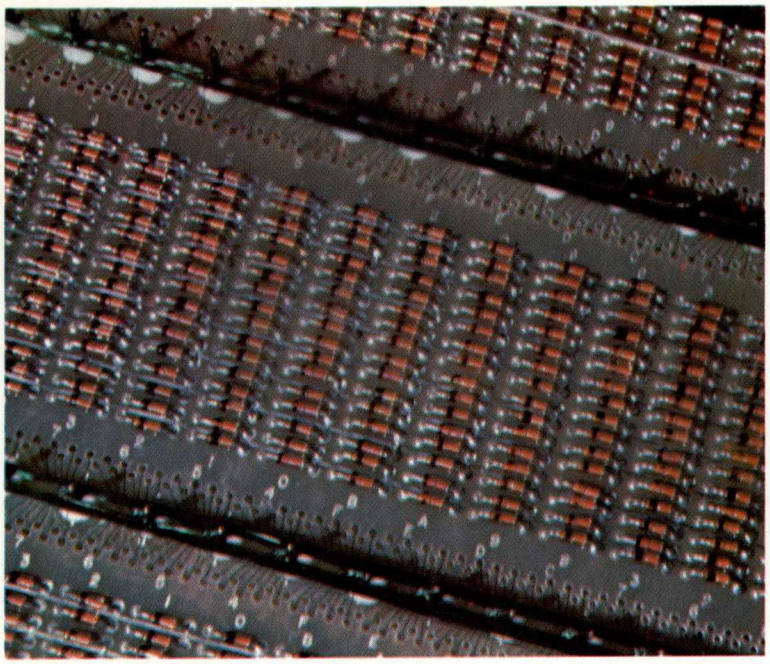
Locations and phone numbers for Field Service offices are listed on the back cover of this brochure.

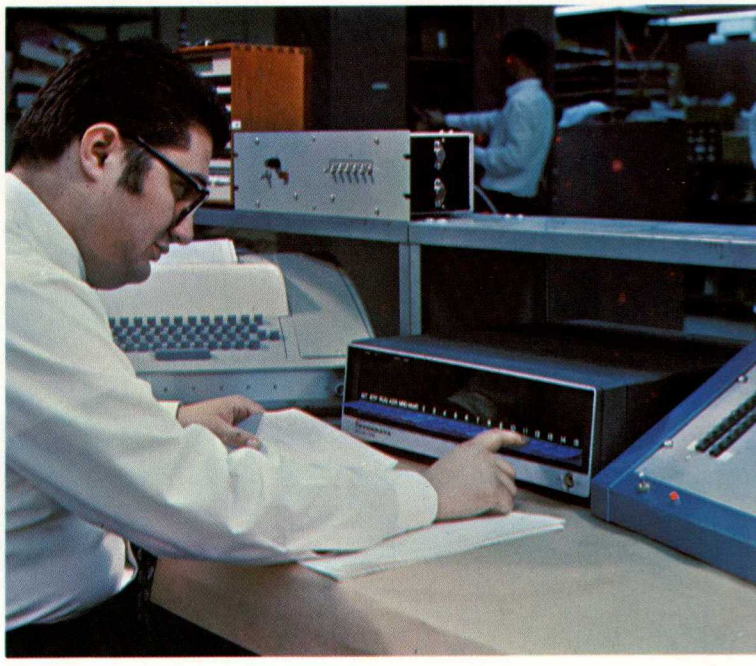
Training Center: INTERDATA takes customer training very seriously. A group of professional instructors is maintained for this purpose. The people on the training staff have all had prior experience in the training of computer personnel in military and civilian schools. Hundreds of customer engineers have already been successfully trained by this staff.

Systems Engineering: In many instances where the needs of the application go beyond standard hardware and software, customers have looked to INTERDATA for special assistance. An experienced team is now organized to furnish this support, whether it be a contract for special hardware, or a special software package.

The application team is made up of communications experts, programmers, analog specialists and control specialists. They are an elite group in terms of capability and experience. Where a problem requires a special interface, the solution can often be built quickly and at a nominal expense from off-the-shelf modules.

Interchange: The INTERDATA user's group is an active and growing association. By sharing software and special interfaces, customers gain a valuable "second level" of support.





Model 1 Specifications

Word Size: 8 bits
Arithmetic: Two's complement
Number of Internal Registers: 7
Number of Instructions: 47
Addressing Modes: Direct, Indirect with auto indexing
Immediate Instructions: Standard
Typical Execution Times:

A Register & Carry Instructions:	1 μsec
Memory Reference Instructions:	3 μsec
Immediates:	2 μsec
Bit Operations:	2.5 μsec
Input-Output:	2 μsec

Memory Size: 2048 words expandable to 16,384 words
Memory Cycle: 1 μsec
Read-Only-Memory: available in modules of 2048 words
Interrupts: 4 hardware levels standard, expandable to 8
Maximum Number of Input-Output Devices: 256
Input-Output Transfer Rates:

Programmed:	83,000 bytes/sec
Read/Write Block:	400,000 bytes/sec
Selector Channel:	500,000 bytes/sec

Power Fail Protection: optional
Real Time Clock: standard, 1 millisecond interrupts
Logic: DTL, TTL, MSI used; 0 volt to +5 volts, positive logic
Dimensions: 5¼" H x 17½" W x 17" D, RETMA standard
Cooling: Filtered forced air
Relative Humidity: 0% to 90% without condensation, operating
Temperature Range: 0° C to 50° C Operating
Weight: 45 lbs.
Power: 115 vac ±10% 50/60 Hz single phase, 150 watts
Interrupt Controlled Serial I/O Port: Standard
Human Engineered Display with Key Lock: Standard

Domestic Offices

EASTERN REGION

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60 Hickory Drive,
Waltham, Mass. 02154
(617) 899-6287

1800 North Kent St.
Arlington, Va. 22210

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