iSBC 108A/116A™
COMBINATION MEMORY AND I/O EXPANSION BOARDS HARDWARE REFERENCE MANUAL

Manual Order Number: 9800862-01

Intel Corporation, 3065 Bowers Avenue, Santa Clara, California 95051

Additional copies of this manual or other Intel literature may be obtained from:

Literature Department
Intel Corporation
3065 Bowers Avenue
Santa Clara, CA 95051

A142/1179/5K FL

PREFACE

This manual provides general information, installation, principles of operation, and service information for the iSBC 108A/116A Combination Memory and I/O Expansion Boards. Additional information is available in the following document: *Intel MULTIBUS Interfacing,* Application Note AP-28.

This manual is divided into the following chapters and appendixes:

- "Introduction", which describes the iSBC 108A/116A Combination Memory and I/) Expansion Boards and their features.
- "Preparation For Use", which describes unpacking, installation, and how to configure the boards.
- "Programming Information", which describes the programming for the USART and PPI.
- "Principles of Operation", which describes how the circuits operate.
- "Service Information", which lists the replaceable parts and contains the circuit schematics.
- "Appendix A", which contains the mnemonics list.
- "Appendix B", which describes the differences in the jumper configurations for the old style boards and the new A versions.

CONTENTS

TABLES

ILLUSTRATIONS

CHAPTER 1
GENERAL INFORMATION

1-1. INTRODUCTION

The iSBC 108A/116A Combination Memory and I/O Expansion Boards (figure 1-1) are members of a complete line of iSBC 80/86 Memory and I/O expansion boards designed to interface directly with any iSBC 80/86 Single Board Computer via the system bus. The iSBC 108A/116A board provides up to 16K bytes of RAM and up to 32K bytes of ROM or up to 16K bytes of PROM capacity, as well as parallel and serial I/O ports.

1-2. DESCRIPTION

The iSBC 108A board and iSBC 116A board contain 8K and 16K bytes, respectively. Both boards provide up to 32K of ROM or up to 16K bytes of PROM, and also include 48 parallel I/O lines controlled by two Intel 8255A Programmable Peripheral Interface (PPI) devices, and a single serial I/O port implemented with an Intel 8251A Universal Synchronous/Asychronous Receiver/Transmitter (USART). Eight user-configurable interrupt lines are also provided.

The iSBC 108A/116A modules are designed for installation in a standard iSBC 604/614 Modular Backplane and Cardcage with an iSBC 80/86 Single Board Computer, or for use with an Intellec System.

1-3. SERIAL I/O PORT

A serial I/O interface, programmable for most synchronous or asynchronous serial data transmission protocols, is provided onboard by an Intel 8251A Universal Synchronous/Asynchronous Receiver/Transmitter. In the synchronous mode, the following functions are programmable.

a. Character length
b. Sync character (or characters)
c. Parity

In the asynchronous mode, the following functions are programmable:

a. Character length
b. Baud rate factor (clock divide ratios of 1, 16, or 64)
c. Stop bits
d. Parity

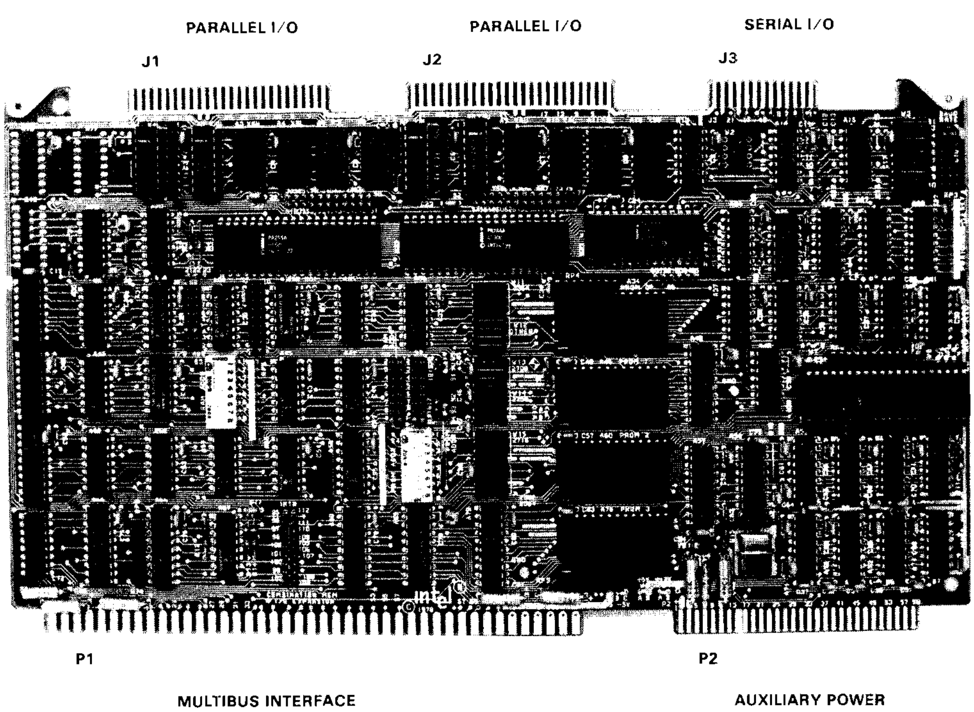


Figure 1-1. iSBC 108A/116A™ Module

In both synchronous and asynchronous modes, the serial I/O port features half- or full-duplex double-buffered transmit or receive capability. In addition, USART error detection circuits can check for parity, overrun, and framing errors. The USART may be jumpered to use external clock signals or the on-board baud rate generator. The USART communicates with peripheral devices through a 26-pin edge connector.

1-4. PARALLEL I/O PORTS

The iSBC 108A/116A modules each include two Intel 8255A Programmable Peripheral Interfaces that control three 8-bit I/O ports each, giving six programmable parallel I/O ports on board. System software can configure the ports in combinations of bi-directional and unidirectional input/output and can configure two ports as status registers or I/O registers. Sockets are provided for user-installed driver or terminator devices to suit a particular user application. The six I/O ports communicate with peripheral devices through two 50-pin edge connectors.

1-5. INTERRUPTS

Six jumper-programmable interrupts are available from the I/O ports, two from each 8255A PPI device, and two from the 8251A USART. The parallel I/O interrupts may be configured to generate interrupts when certain flag bits are set in the status register, and the serial I/O interrupts may be configured to generate interrupts when the transmit or receive buffers are ready for new data, or when the transmitter is empty. Two other interrupts are available, both of which accept signals from user-designated peripheral devices via edge connectors J1 and J2. One of these interrupts may be jumpered to an interval timer, which supplies 1 ms interrupt signals.

1-6. EQUIPMENT SUPPLIED

The following are supplied with the iSBC 108A/116A Combination Memory and I/O Expansion Boards:

a. Schematic Diagram, dwg. no. 2002298

b. Assembly Drawing, dwg. no. 1002296.

1-7. SPECIFICATIONS

Specifications for the iSBC 108A/116A modules are listed in table 1-1.

Table 1-1. Specifications.

MEMORY ADDRESSING	
ROM/PROM:	8K or 16K bytes of ROM/PROM or 32K bytes of ROM starting at any jumper-selectable base address on a 4K byte boundary. Refer to paragraph 2-8 for further details. NOTE: All PROM/ROM addresses must reside in one of thirty two 32K pages within a one megabyte address range of X0000H to X7FFFH or X8000H to XFFFFH (where X = 0 to F).
RAM:	8K or 16K segments starting at any jumper-selectable base address on a 4K boundry. Refer to paragraph 2-8 for further details. NOTE: All RAM addresses must reside in one of thirty two 32K pages within a one megabyte address range of X0000H to X7FFFH or X8000H to XFFFFH.
Memory Response Time:	(see below)

Memory	Access (ns)	Cycle (ns)
RAM	450 max*	580 max*
PROM/ROM	450 max	635 max

*without refresh contention

Table 1-1. Specifications (Continued)

I/O Addressing:

Port	PPI 1A	PPI 1B	PPI 1C	PPI 2A	PPI 2B	PPI 2C	8255A No. 1 Control	8255A No. 2 Control	USART Data	USART Control
Address	XX4	XX5	XX6	XX8	XX9	XXA	XX7	XXB	XXC	XXD

NOTE: XX is two hex digits assigned by jumper selection.

I/O TRANSFER RATE

Parallel: Read or Write acknowledge time 575 ns max

Serial: (USART)

Frequency (kHz) (Jumper Selectable)	Baud Rate (Hz) Synchronous	Asynchronous (Program Selectable) ÷ 16	÷ 64
307.2		19200	4800
153.6	—	9600	2400
76.8	—	4800	1200
38.4	38400	2400	600
19.2	19200	1200	300
9.6	9600	600	150
4.8	4800	300	75
6.98	6980	—	110

SERIAL COMMUNICATIONS CHARACTERISTICS

Synchronous: 5-8 bit characters
Automatic Sync Insertion

Asynchronous: 5-8 bit characters
Break characters generation and detection
1, 1-1/2, or 2 stop bits
False start bit detectors

INTERRUPTS: Eight interrupt request lines may originate from the Programmable Peripheral Interface (4 lines), the USART (2 lines) or user specified devices via the I/O edge connector (2 lines) or Interval Timer.

INTERRUPT REGISTER ADDRESSES

Interrupt Mask Register	XX1
Interrupt Status Register	XX0

NOTE: XX is any two hex digits assigned by jumper selection.

TIMER INTERVAL: 1.003 ms ± 0.1% when 110 Baud Rate is selected
1.042 ms ±0.1% for all other Baud Rates

Table 1-1. Specifications (Continued)

INTERFACES

Bus: All signals TTL compatible

Parallel I/O: All signals TTL compatible

Serial I/O: RS232C

Interrupt Requests: All TTL compatible

CONNECTORS

Interface	No. of Pins	Centers (in.)	Mating Connectors
Bus (P1)	86	0.156	CDC VPB01E43A00A1
Parallel I/O	50	0.1	3M 3415-000 or TI H312125
Serial I/O	26	0.1	3M 3462-000 or TI H312113
Aux Power (P2)	60	0.1	AMP PE5-14559 or TI H311130

NOTE: Connector heights and wire-wrap pin lengths are not guaranteed to conform to Intel OEM packaging.

PHYSICAL CHARACTERISTICS

Width: 12.00 in. (30.48 cm)

Height: 6.75 in. (17.15 cm)

Depth: 0.50 in. (1.27 cm)

Weight: 14 oz. (397.3 gm)

ELECTRICAL CHARACTERISTICS

Average DC Current:

	No EPROM or Terminators	4 2708's and 8 Terminators	4 2716's and No Terminators	4 2732's and No Terminators	Aux Power RAM Accessed	Aux Power No RAM Access
V_{DD} = +12 ±5%	250 mA	520 mA	250 mA	250 mA	175 mA	20 mA
V_{CC} = +5 ±5%	2.9 A	3.6 A	3.3 A	3.5 A	0.45 A	0.45 A
V_{BB} = -5 ±5%	—	180 mA	—	—	3 mA	3 mA
V_{AA} = -12 ±5%	70 mA	70 mA	70 mA	70 mA	—	—

AUXILIARY POWER: An Auxiliary Power Bus is provided to allow separate power to RAM for systems requiring battery backup of read/write memory, Selection of this Auxiliary RAM Power Bus is made via jumpers on the board.

MEMORY PROTECT: An active-low TTL compatible MEMORY PROTECT signal is brought out on the Auxiliary connector which, when asserted, disables Read/Write access to RAM memory on the board. This input is provided for the protection of RAM contents during system power-down sequences.

Table 1-1. Specifications (Continued)

LINE DRIVERS AND TERMINATORS

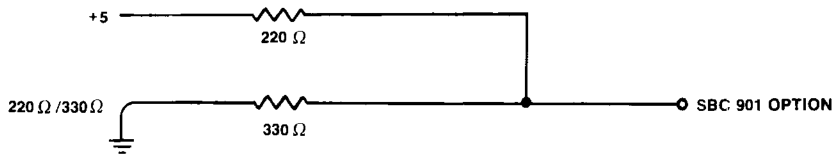
I/O Drivers: The following line drivers and terminators are all compatible with the I/O driver sockets on the iSBC 108A/116A boards.

Driver	Characteristic	Sink Current (mA)	Driver	Characteristic	Sink Current (mA)
7438	I,OC	48	7409	NI,OC	16
7437	I	48	7408	NI	16
7432	NI	16	7403	I,OC	16
7426	I,OC	16	7400	I	16

NOTE: I = inverting; NI = non-inverting; OC = open collector.

Ports 1 and 4 have 25 mA totem-pole drivers and 1 kΩ terminators.

I/O Terminators: Terminators: 220Ω/330Ω divider or 1 kΩ pull-up.



Bus Drivers:

Function	Characteristic	Sink Current (mA)
Data	Tri-State	32
Acknowledge	Tri-State	32

ENVIRONMENTAL

Operating Temperature: 0°C to +55°C.

Humidity: To 90% noncondensing.

CHAPTER 2
PREPARATION FOR USE

2-1. INTRODUCTION

This chapter provides instructions for installing the iSBC 108A/116A Combination Memory and I/O Expansion Boards. These instructions include unpacking and inspection; installation considerations such as power and cooling requirements, physical dimensions, and bus interface requirements; jumper configurations; optional battery back-up power and memory protect connections; board installation; and programming considerations.

2-2. UNPACKING AND INSPECTION

Inspect the shipping carton immediately upon receipt for evidence of mishandling during transit. If the shipping carton is severely damaged or water-stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is not present when the carton is opened and the contents of the carton are damaged, keep the carton and packing materials for the agent's inspection.

For repairs to a product damaged in shipment, contact the Intel MCD Technical Support Center (see paragraph 5-4) to obtain a Repair Authorization Number and further instructions. A purchase order will be required to complete the repair. A copy of the purchase order should be submitted to the carrier with your claim.

It is suggested that the salvageable shipping cartons and packing material be saved for future use if the product must be shipped.

2-3. INSTALLATION CONSIDERATIONS

The iSBC 108A/116A boards are designed to interface with an Intel iSBC 80/86 Single Board Computer based system or an Intel Intellec System. Important installation and interfacing criteria are presented in the following paragraphs.

2-4. POWER REQUIREMENT

Power requirements for the iSBC 108A/116A boards are specified in table 1-1. For installation in an iSBC 80/86 Single Board Computer based system, ensure that the system power supply has sufficient +5V, -5V, -12V, and +12V current capacity to accommodate the additional requirement. For installation in an Intellec system, calculate the total +5V, +12V, and -12V current requirements for the standard modules and all installed optional modules. Ensure that the additional current requirement will not exceed the capacity of the Intellec System power supplies.

NOTE

If Intel 2708 PROMs are installed, the iSBC 108A/116A boards cannot be used in the Intellec System.

2-5. COOLING REQUIREMENT

The iSBC 108A/116A boards dissipate 370 gram/calories per minute (1.5 BTU/minute) and adequate circulation of air must be provided to prevent a temperature rise above 55°C (131°F). The Intel System 80/86 enclosures and the Intellec System include fans to provide adequate intake and exhaust of ventilating air.

2-6. PHYSICAL DIMENSIONS

Physical dimensions of the iSBC 108A/116A boards are as follows:

a. Width: 30.48 cm (12.00 inches)

b. Depth: 17.15 cm (6.75 inches)

c. Thickness: 1.27 cm (0.50 inch)

2-7. BUS INTERFACING REQUIREMENTS

The iSBC 108A/116A boards are designed for installation in a standard Intel iSBC 604/614 Modular Backplane and Cardcage or in the Intellec System motherboard. As shown in figure 1-1, edge connector P1 provides interface to the Multibus system bus. Connector P1 pin assignments are listed in table 2-1 and descriptions of the signal functions are given in table 2-2. Edge connector P2 is an auxiliary power input described in paragraph 2-29. Connector P2 pin assignments are listed in table 2-3. As shown in figure 1-1, edge connectors J1 and J2 provide connections for the Parallel I/O Ports. Connector J1 and J2 pin assignments are listed in table 2-4 and 2-5 respectively. As shown in figure 1-1, edge connector J3 provides a connection for the serial I/O port. Connector J3 pin assignments are listed in table 2-6.

NOTE

When the iSBC 108A/116A board is installed in an Intellec System, it is necessary to configure the Intellec CPU module for qualified memory write command.

Table 2-1. Connector P1 Pin Assignments

PIN*	SIGNAL	FUNCTION	PIN*	SIGNAL	FUNCTION
1	GND	Ground	44	ADRF/	Address Bus
2	GND		45	ADRC/	
3	+5 VDC	Power input	46	ADRD/	
4	+5 VDC		47	ADRA/	
5	+5 VDC		48	ADRB/	
6	+5 VDC		49	ADR8/	
7	+12 VDC		50	ADR9/	
8	+12 VDC		51	ADR6/	
9	−5 VDC		52	ADR7	
10	−5 VDC		53	ADR4/	
11	GND	Ground	54	ADR5/	
12	GND		55	ADR2/	
13	BCLK/	Bus Clock	56	ADR3/	
14	INIT/	System Initialize	57	ADR0/	
15			58	ADR1/	
16			59		
17	BUSY/	Bus Busy	60		
18			61		
19	MRDC/	Memory Read Command	62		
20	MWTC/	Memory Write Command	63		
21	IORC/	I/O Read Command	64		
22	IOWC/	I/O Write Command	65		
23	XACK/	Transfer Acknowledge	66		
24	INH1/	RAM Inhibit	67	DAT6/	Data bus
25	AACK/	Advanced Acknowledge	68	DAT7/	
26	INH2/	ROM/PROM Inhibit	69	DAT4/	
27			70	DAT5/	
28	ADR10/	Address Bus	71	DAT2/	
29			72	DAT3/	
30	ADR11/		73	DAT0/	
31			74	DAT1/	
32	ADR12/		75	GND	Ground
33	INTR/	Direct Interrupt Request	76	GND	
34	ADR13/	Address Bus	77		
35	INT6/	Interrupt request on level 6	78		
36	INT7/	Interrupt request on level 7	79	−12 VDC	Power input
37	INT4/	Interrupt request on level 4	80	−12 VDC	
38	INT5/	Interrupt request on level 5	81	+5 VDC	
39	INT2/	Interrupt request on level 2	82	+5 VDC	
40	INT3/	Interrupt request on level 3	83	+5 VDC	
41	INT0/	Interrupt request on level 1	84	+5 VDC	
42	INT1/	Interrupt request on level 0	85	GND	Ground
43	ADRE/	Address Bus	86	GND	

*All unassigned pins are reserved.

Table 2-2. Multibus Signal Functions

Signal	Functional Description
AACK/	*Advance Acknowledge:* This signal is issued by the iSBC 108A/116A board in response to a read or write command. The AACK/ signal allows the system controller to proceed with the current instruction cycle.
ADRO/-ADRF/ ADR10/-ADR13/	*Address:* These 20 lines transmit the address of the memory location or I/O port to be accessed. ADRF/ is the most significant bit except where ADR10/ through ADR13/ are used. ADR10/ through ADR13/ are transmitted only by those bus masters capable of addressing beyond 64K of memory. In this case, ADR13/ is the most significant bit.
DAT0/-DAT7/	*Data:* These eight bidirectional data lines transmit and receive information to and from the addressed memory location or I/O port. DAT7/ is the most significant bit.
INH1/	*Inhibit RAM:* Prevents RAM from responding to a bus access. Allows a PROM module to overlay RAM.
INH2/	*Inhibit PROM:* Prevents ROM/PROM from responding to a bus access. Allows auxiliary ROM to overlay normal ROM.
INIT/	*Initialization:* Resets the entire system to a known internal state.
INT0/-INT7/	*Interrupt:* These eight lines are used for system interrupt requests.
INTR/	*Interrupt Request:* Supports coded interrupt requests in special applications of interrupt structure.
IORC/	*I/O Read Command:* Indicates that the address of an I/O port is on the system address lines and that the output of that port is to be read (placed) onto the system data lines.
IOWC/	*I/O Write Command:* Indicates that the address of an I/O port is on the system address lines and that the contents on the system data lines are to be accepted by the addressed port.
MRDC/	*Memory Read Command:* Indicates that the address of a memory location is on the system address lines and that the contents of that location are to be read (placed) onto the system data lines.
MWRC/	*Memory Write Command:* Indicates that the address of a memory location is on the system address lines and that the contents on the system data lines are to be written into that location.
XACK/	*Transfer Acknowledge:* Indicates that the addressed memory location or I/O port has completed the specified read or write operation. That is, data has been placed onto or accepted from the system data lines.

The ac and dc characteristics of the RAM boards are presented in tables 2-7 and 2-8 respectively. The bus exchange timing for memory and I/O read and write operations is shown in figure 2-1.

2-8. JUMPER CONFIGURATIONS

The iSBC 108A/116A boards provide the user with the capability of selecting the I/O base address, the RAM/PROM base addresses, the RAM/PROM page, clock frequency, system interrupts, and serial and parallel I/O interface protocols. Tables 2-9 through 2-19 list the jumper selections.

Study the tables carefully. If the default (factory configured) jumper wiring is appropriate for a specific function, no further action is needed for operation with that function. If, however, a different

Table 2-3. Connector P2 Pin Assignments

Pin*	Signal	Function
1	GND	Auxillary Common
2	GND	
3	+5 Aux	Auxillary battery backup supply
4	+5 Aux	
7	-5 Aux	
8	-5 Aux	
11	+12 Aux	
12	+12 Aux	
20	MEM PROT/	Memory Protect. This externally supplied signal prevents access to RAM during battery backup operation.

*All unassigned pins are reserved.
A protective keying slot is provided between pins 15-16 and 17-18 on P2.

Table 2-4. Connector J1 Pin Assignments

Pin	Signal	Function
1	GND	Ground
2	BIT 7	Port 2 — Bit 7. Input or Output Data Bit
3	GND	Ground
4	BIT 6	Port 2 — Bit 6. Input or Output Data Bit
5	GND	Ground
6	BIT 5	Port 2 — Bit 5. Input or Output Data Bit
7	GND	Ground
8	BIT 4	Port 2 — Bit 4. Input or Output Data Bit
9	GND	Ground
10	BIT 3	Port 2 — Bit 3. Input or Output Data Bit
11	GND	Ground
12	BIT 2	Port 2 — Bit 2. Input or Output Data Bit
13	GND	Ground
14	BIT 1	Port 2 — Bit 1. Input or Output Data Bit
15	GND	Ground
16	BIT 0	Port 2 — Bit 0. Input or Output Data Bit
17	GND	Ground
18	BIT 3	Port 3 — Bit 3. Input or Output Data Bit
19	GND	Ground
20	BIT 2	Port 3 — Bit 2. Input or Output Data Bit
21	GND	Ground
22	BIT 1	Port 3 — Bit 1. Input or Output Data Bit
23	GND	Ground
24	BIT 0	Port 3 — Bit 0. Input or Output Data Bit
25	GND	Ground
26	BIT 4	Port 3 — Bit 4. Input or Output Data Bit
27	GND	Ground
28	BIT 5	Port 3 — Bit 5. Input or Output Data Bit
29	GND	Ground
30	BIT 6	Port 3 — Bit 6. Input or Output Data Bit
31	GND	Ground
32	BIT 7	Port 3 — Bit 7. Input or Output Data Bit
33	GND	Ground
34	BIT 7	Port 1 — Bit 7. Input or Output Data Bit
35	GND	Ground
36	BIT 6	Port 1 — Bit 6. Input or Output Data Bit
37	GND	Ground
38	BIT 5	Port 1 — Bit 5. Input or Output Data Bit
39	GND	Ground
40	BIT 4	Port 1 — Bit 4. Input or Output Data Bit
41	GND	Ground
42	BIT 3	Port 1 — Bit 3. Input or Output Data Bit
43	GND	Ground
44	BIT 2	Port 1 — Bit 2. Input or Output Data Bit
45	GND	Ground
46	BIT 1	Port 1 — Bit 1. Input or Output Data Bit
47	GND	Ground
48	BIT 0	Port 1 — Bit 0. Input or Output Data Bit
49	GND	Ground
50	EXT INTR1/	External Interrupt. Externally produced interrupt.

Table 2-5. Connector J2 Pin Assignments

Pin	Signal	Function
1	GND	Ground
2	BIT 7	Port 5 — Bit 7. Input or Output Data Bit
3	GND	Ground
4	BIT 6	Port 5 — Bit 6. Input or Output Data Bit
5	GND	Ground
6	BIT 5	Port 5 — Bit 5. Input or Output Data Bit
7	GND	Ground
8	BIT 4	Port 5 — Bit 4. Input or Output Data Bit
9	GND	Ground
10	BIT 3	Port 5 — Bit 3. Input or Output Data Bit
11	GND	Ground
12	BIT 2	Port 5 — Bit 2. Input or Output Data Bit
13	GND	Ground
14	BIT 1	Port 5 — Bit 1. Input or Output Data Bit
15	GND	Ground
16	BIT 0	Port 5 — Bit 0. Input or Output Data Bit
17	GND	Ground
18	BIT 3	Port 6 — Bit 3. Input or Output Data Bit
19	GND	Ground
20	BIT 2	Port 6 — Bit 2. Input or Output Data Bit
21	GND	Ground
22	BIT 1	Port 6 — Bit 1. Input or Output Data Bit
23	GND	Ground
24	BIT 0	Port 6 — Bit 0. Input or Output Data Bit
25	GND	Ground
26	BIT 4	Port 6 — Bit 4. Input or Output Data Bit
27	GND	Ground
28	BIT 5	Port 6 — Bit 5. Input or Output Data Bit
29	GND	Ground
30	BIT 6	Port 6 — Bit 6. Input or Output Data Bit
31	GND	Ground
32	BIT 7	Port 6 — Bit 7. Input or Output Data Bit
33	GND	Ground
34	BIT 7	Port 4 — Bit 7. Input or Output Data Bit
35	GND	Ground
36	BIT 6	Port 4 — Bit 6. Input or Output Data Bit
37	GND	Ground
38	BIT 5	Port 4 — Bit 5. Input or Output Data Bit
39	GND	Ground
40	BIT 4	Port 4 — Bit 4. Input or Output Data Bit
41	GND	Ground
42	BIT 3	Port 4 — Bit 3. Input or Output Data Bit
43	GND	Ground
44	BIT 2	Port 4 — Bit 2. Input or Output Data Bit
45	GND	Ground
46	BIT 1	Port 4 — Bit 1. Input or Output Data Bit
47	GND	Ground
48	BIT 0	Port 4 — Bit 0. Input or Output Data Bit
49	GND	Ground
50	EXT INTR2/	External Interrupt. Externally produced interrupt.

Table 2-6. Connector J3 RS232C Signal Interface

J3 Pin	RS232C Pin	Signal Mnemonic	Definition
1	14	STXD	Secondary Transmit Data. Same as TXD except STXD is a secondary signal.
2	1	FGD	TTY Frame Ground. (Optional jumper plug)
3	15	XMIT CLK	Transmit Clock. External input clock signal for transmit data timing.
4	2	TXD	Transmit Data. Data transmitted from data terminal to data set.
5	16	SRXD	Secondary Receive Data. Same as RXD except SRXD is a secondary signal.
6	3	RXD	Receive Data. Data received by data terminal from data set.
7	17	REC CLK	Receive Clock. External input clock signal for receive data timing.
8	4	RTS	Request To Send. Control signal from data terminal to data set; sets data set in transmit mode.
9	18	—	Not used on iSBC 108A/116A boards.
10	5	CTS	Clear To Send. Control signal from data set to data terminal to indicate that data set is ready to transmit data; enables TXD output mode.
11	19	SRTS	Secondary Request To Send. Same as RTS except SRTS is a secondary signal.
12	6	DSR	Data Set Ready. Indicates to data terminal that data set is connected to a communications channel; i.e., data set is not in Test, Talk, or Dial mode and timing and/or answer signals have been completed.
13	20	DTR	Data Terminal Ready. Indicates to data set that data terminal is ready to transmit or receive data.
14	7	SGD	Signal Ground.
15	21	—	Not used on iSBC 108A/116A boards.
16	8	CD	Carrier Detect. Signal from data set; indicates that data set is receiving a suitable signal.
17	22	RI	Ring Indicator. Signal from data set; indicates that ringing signal has been received from a communications channel.
18	9	—	Not used for RS232C.
19	23	—	TTY Adapter PWR (-12V). (Optional jumper plug)
20	10	—	Not used for RS232C.
21	24	DTE TXC	Data Terminal Equipment Transmit Clock. Output from serial I/O port to data set to provide clock signal to transmitting signal converter.
22	11	—	TTY Adapter PWR (+12V). (Optional jumper plug)
23	25	—	TTY Adapter PWR (+5V). (Optional jumper plug)
24	12	—	Not used for RS232C.
25	N/C	SGD	Signal Ground.
26	13	SCTS	Secondary Clear To Send. Same as CTS except SCTS is a secondary signal.

NOTES:
1. J3 pins 9, 15, 18, 20, and 24 are not used by iSBC 108A/116A boards.
2. Pin numbers refer to board connector pins only, they are not necessarily the same on the mating connectors.

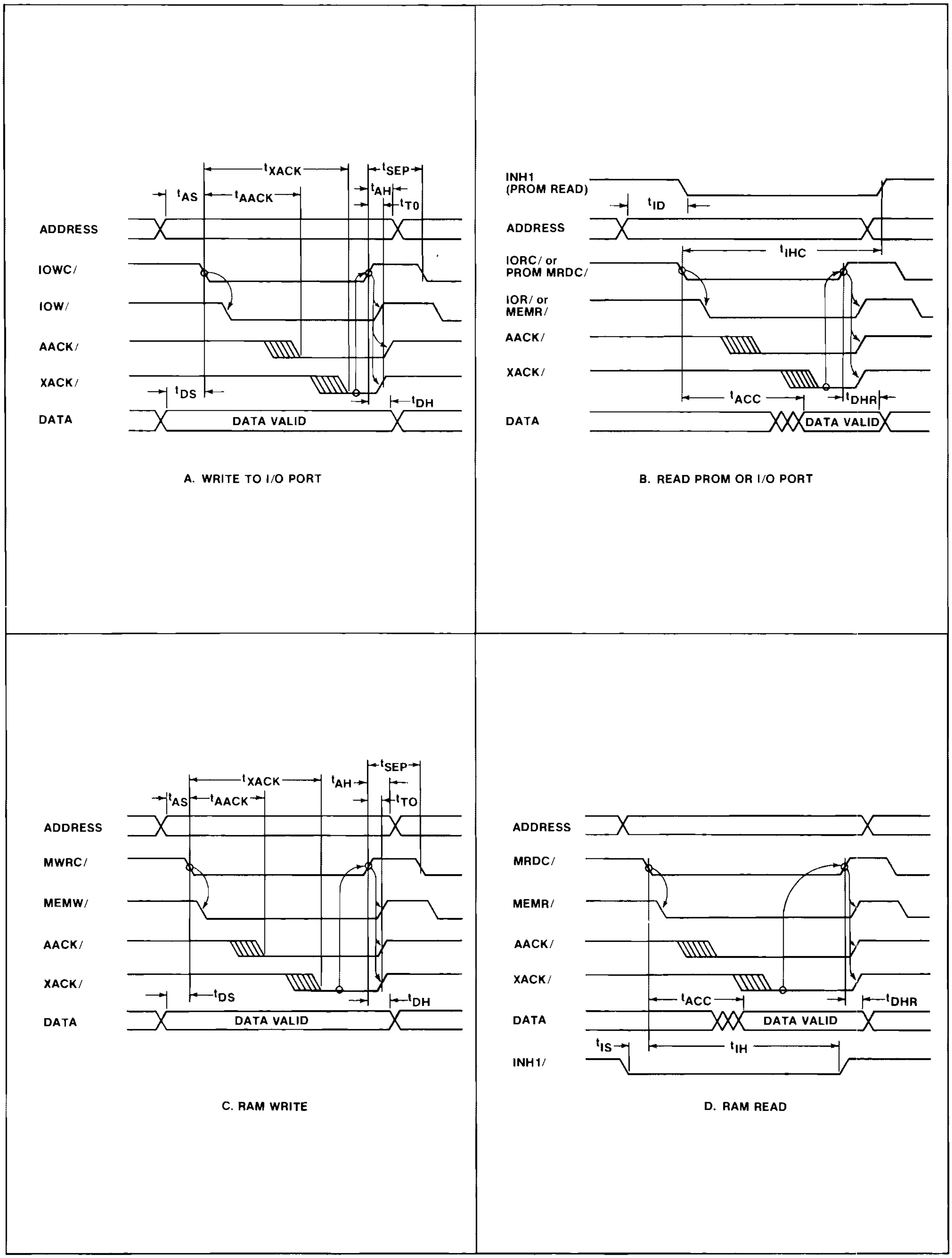


Figure 2-1. iSBC 108A/116A™ Board Read/Write Timing

configuration is required, remove the default jumpers and install appropriate optional jumper(s) as required. Clarification of jumper-selectable options is given in the following paragraphs.

NOTE

The iSBC 108A/116A boards do not support the Multibus interface serial bus priority scheme. The two signals used in this scheme, BPRN/ and BPRO/, are propagated through pins 15 and 16 of the Multibus interface (P1). Since these two pins are not connected on the iSBC 108A/116A boards an external jumper must be provided to route BPRN/ to a master module further down in the serial bus priority scheme.

2-9. RAM, ROM/PROM PAGE SELECT

Each iSBC combination memory and I/O board, in a one megabyte system, may be assigned to a specific 64K byte block of memory called a "page." In such a system there is a total of 16 pages, each page occupying 64K bytes of system memory. Note that RAM and ROM/PROM may be assigned to different pages. The pages are designated, in hexadecimal notation, 0 through F, with page 0 being the lowest page and page F being the highest or top page.

Two jumpers are used to assign the page for RAM and two jumpers are used to assign the page for ROM/PROM. The board is shipped from the factory with both RAM and ROM/PROM assigned to page 0 (0-64K).

Table 2-7. iSBC 108A/116A™ Board AC Characteristics

Parameter	RAM Read/Write		ROM Read		I/O Read/Write		Description	Remarks
	Min ns	Max ns	Min ns	Max ns	Min ns	Max ns		
T_{AS}	50		50		50		Address Setup to Command	
T_{DS}	-125				50		Write Data Setup to Command	
T_{AACK}	30	115	80	190	80	190	Command to AACK	Jumper W1 A-G
T_{XACK}		525	450	575		575	Command to XACK	Jumper W1 C-H
T_{XACK2}		525	540	660		660	Command to XACK	Jumper W1 E-H
T_{AH}	0		0		50		Address Hold Time	
T_{DH}	0				50		Write Data Hold Time	
T_{DHR}	0		0		0		Read Data Hold Time	
T_{TO}		55		60		60	Acknowledge Turn Off	
T_{ACC}		450		450		280	Access Time to Data	
T_{CY}		580	510	635			Minimum Cycle Time	$T_{XACK} + T_{TO}$
T_{SEP}	100		100		865		Command Separation	Parallel Port Read/Write
T_{SEP2}					100		Command Separation	Serial Port Read (For serial Port Write see Note 1)
T_{RD}	0	545					Refresh Delay Time	
T_{RI}	11.6 µS	12.5 µS					Refresh Interval	12 µS Typical
T_{ID}				63			Address to INH1/	
T_{IS}	-50						Inhibit Setup Time	
T_{IH}	465						Inhibit Hold Time (RAM)	To block XACK/
T_{IHC}			475				Inhibit Hold Time (ROM)	

	Min (ms)	Max (ms)		
T_{IHV1}	1.002	1.004	Interval Timer Interrupt Period	Baud Rate = 110
T_{IHV2}	1.041	1.043	Interval Timer Interrupt Period	Baud Rate ≠ 110

1. Serial I/O Port:

During Initialization — all Writes to the Control Port: t_{SEP} = 2.85 µS

After Initialization in Asynchronous Mode — all Writes to the Control Port: t_{SEP} = 3.66 µS

After Initialization in Synchronous Mode — all Writes to the Control Port: t_{SEP} = 6.92 µS

All Writes to the Data Port: Dependent upon baud rate since TX Rdy must be true

Table 2-8. iSBC 108A/116A™ Board DC Characteristics

SIGNALS	SYMBOL	PARAMETER DESCRIPTION	TEST CONDITIONS	MIN.	MAX.	UNITS
INHI/	V_{OL}	Output Low Voltage	I_{OL} = 16 mA		0.4	V
	V_{OH}	Output High Voltage	OPEN COLLECTOR			
	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.4V		2.0	mA
	I_{IH}	Input Current at High V	V_{IN} = 5.5V		1	mA
	*C_L	Capacitive Load			22	pF
INTR/ INTO/-INIT/	V_{OL}	Output Low Voltage	I_{OL} = 16 mA		0.4	V
	V_{OH}	Output High Voltage	OPEN COLLECTOR			
	*C_L	Capacitive Load			18	pF
EXT INT 1/ EXT INT 2/	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.4V		−6.6	mA
	I_{IH}	Input Current at High V	V_{IN} = 5.5V		1.75	mA
	*C_L	Capacitive Load			18	pF
PORT D4, D8 BIDIRECTIONAL DRIVERS	V_{OL}	Output Low Voltage	I_{OL} = 25 mA		0.45	V
	V_{OH}	Output High Voltage	I_{OH} = -10 mA	2.4		V
	V_{IL}	Input Low Voltage			0.95	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.45V		−5.1	mA
	I_{IH}	Input Current at High V	V_{IN} = 5.25V		0.60	mA
	*C_L	Capacitive Load			18	pF
8255A DRIVER/ RECEIVER	V_{OL}	Output Low Voltage	I_{OL} = 1.7 mA		0.45	V
	V_{OH}	Output High Voltage	I_{OH} = − 200 μA	2.4		V
	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	*C_L	Capacitive Load			18	pF
RS232C Inputs	V_{TH}	Input High Threshold Voltage		1.75	2.25	V
	V_{TL}	Input Low Threshold Voltage		.75	1.25	V
	I	Input Current	V_I = +3V	+.43		mA
			V_{IN} = -3V	-.43		mA
RS232C Outputs	V_O	High Level Output Voltage		9.0		V
	V_O	Low Level Output Voltage		-9.0		V
	I_{OS+}	High Level SS Output Current		-6.0	-12.0	mA
	I_{OS-}	Low Level SS Output Current		6.0	12.0	mA

*Capacitance values are approximations only.

Table 2-8. iSBC 108A/116A™ Board DC Characteristics (Continued)

SIGNALS	SYMBOL	PARAMETER DESCRIPTION	TEST CONDITIONS	MIN.	MAX.	UNITS
ADR0/-ADRF/ IOWC/, IORC/ MWTC/, MRDC/ INH2/, INIT/	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.5V		−0.4	mA
	I_{IH}	Input Current at High V	V_{IN} = 2.7V		50	μA
	*C_L	Capacitive Load			18	pF
AACK/ XACK/	V_{OL}	Output Low Voltage	I_{OL} = 32 mA		0.4	V
	V_{OH}	Output High Voltage	I_{OH} = −5.2 mA	2.4		V
	I_{LH}	Output Leakage High	V_O = 2.4V		40	μA
	I_{LL}	Output Leakage Low	V_O = 0.4V		−40	μA
	*C_L	Capacitive Load			15	pF
DAT0/-DAT7/	V_{OL}	Output Low Voltage	I_{OL} = 32 mA		0.45	V
	V_{OH}	Output High Voltage	I_{OH} = −5 mA	2.4		V
	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.45V		−0.2	mA
	I_{LH}	Output Leakage High	V_O = 5.25V		50	μA
	*C_L	Capacitive Load			18	pF
MEMORY PROTECT/	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.4V		−0.9	mA
	O_{IH}	Input Current at High V	V_{IN} = 5.5V		20	μA
	*C_L	Capacitive Load			18	pF
ADR10/-ADR13/	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.5V		−0.6	mA
	I_{IH}	Input Current at High V	V_{IN} = 2.7V		50	μA
	*C_L	Capacitive Load			18	pF

*Capacitance values are approximations only.

To change the page selection, several jumper wires must be changed. All jumper wire connections for page assignment of RAM and ROM/PROM are listed in table 2-9. Figure 2-2 shows the locations of the jumper pads and switches used in the assignment of RAM and ROM/PROM page selection and base address selection.

2-10. RAM BASE ADDRESS

Jumper 89-90 or jumper 90-91, shown on figure 2-2, restricts read/write memory (RAM), installed on the board, to the lower 32K segment or upper 32K segment of a page of addressable memory space. The iSBC 108A/116A boards are shipped with the lower 32K segment of page Zero selected. Refer to table 2-10 for details of RAM base address selection.

Switch S3 establishes the RAM base address and the number of contiguous addressable 4K blocks within the selected 32K segment. Each OFF position enables one 4K block; the lowest numbered switch position establishes the RAM base address. The iSBC 108A/116A boards are shipped with the RAM address set to 4000H.

Notice in table 2-10 that switch S3 on the iSBC 108A/116A boards, respectively, must have two or four OFF switch positions to accommodate the appropriate number of 4K blocks of RAM. Because of the 32K segment restrictions imposed by jumper 89-90 or 90-91, base addresses 7000 and F000 are not allowed for the iSBC 108A board, base addresses 5000H, 6000H, 7000H, D000H, E000H, and F000H are not allowed for the iSBC 116A board.

2-11. ROM/PROM BASE ADDRESS

Jumper 92-93 or jumper 93-94, shown on figure 2-2, restricts optional ROM/PROM installed on the board to the lower 32K segment or the upper 32K segment of a page of addressable memory space.

NOTE

When using Intel 2364 ROMs, jumper 92-93-94 is not used.

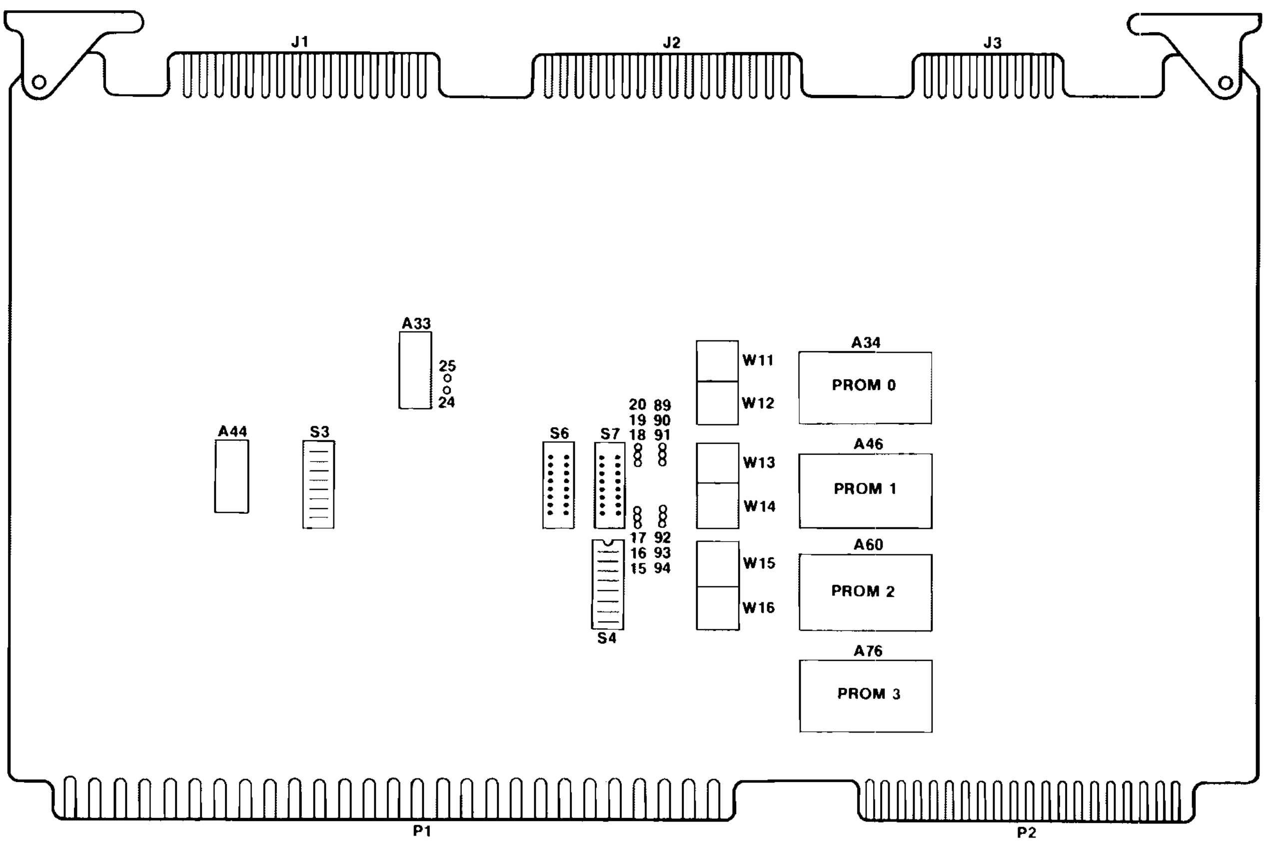


Figure 2-2. RAM and ROM/PROM Page and Base Address Jumper and Switch Locations

Table 2-9. Page Select Jumper Connections

Selected Page (Range)	RAM Jumper S6	ROM/PROM Jumper S7
0 (0—64K) or 8 (512—576K)	*1-9	*1-9
1 (64—128K) or 9 (576—640K)	1-8	1-8
2 (128—192K) or A (640—704K)	1-7	1-7
3 (192—256K) or B (704—768K)	1-6	1-6
4 (256—320K) or C (768—832K)	1-5	1-5
5 (320—384K) or D (832—896K)	1-4	1-4
6 (384—448K) or E (896—960K)	1-3	1-3
7 (448—512K) or F (960—1024K)	1-2	1-2
Pages 0-7 (0—512K)	*19-20	*16-17
Pages 8-F (512—1024K)	18-19	15-16

*Denotes factory-wired default configuration.

1. All pins on right side of arrays S6 and S7 are tied together and labelled Pin 1. Use pin directly opposite desired pin for jumpering.

Table 2-10. RAM Base Address Selection

*Base Address	Jumper	***S3 Switches	
		108A	116A
X0000	89-90	1	1
X1000	89-90	2	2
X2000	89-90	3	3
X3000	89-90	4	4
X4000	**89-90	**5	**5
X5000	89-90	**6	**6
X6000	89-90	7	**7
X7000	89-90	8	**8
X8000	90-91	1	1
X9000	90-91	2	2
XA000	90-91	3	3
XB000	90-91	4	4
XC000	90-91	5	5
XD000	90-91	6	6
XE000	90-91	7	7
XF000	90-91	8	8

*High order position selected by Page jumper.

**Denotes factory-wired default configuration.

***Each switch that is in the off position enables a 4K block of memory.

Table 2-11. ROM/PROM Base Address Selection

*Base Address	†Jumper	***Switch S4
X0000	92-93	1
X1000	**92-92	**2
X2000	92-93	3
X3000	92-93	4
X4000	92-93	5
X5000	92-93	6
X6000	92-93	7
X7000	92-93	8
X8000	93-94	1
X9000	93-94	2
XA000	93-94	3
XB000	93-94	4
XC000	93-94	5
XD000	93-94	6
XE000	93-94	7
XF000	93-94	8

†Not used when 2364 ROM is installed.

*High order position selected by page jumper.

**Denotes factory-wired default configuration.

***Each switch that is in the off position enables a 4K block of memory.

The iSBC 108A/116A boards are shipped with the lower 32K segment of page zero selected. Refer to table 2-11 for details of ROM/PROM base address selection.

There are four IC sockets to accommodate up to 4K of ROM/PROM using Intel 2308, 2708, or 2758 chips; up to 8K of ROM/PROM using Intel 2316E or 2716 chips; up to 16K of ROM/PROM using Intel 2332 or 2732 chips; up to 32K of ROM using Intel 2364 chips. Switch S4 establishes the 4K block(s) of ROM/PROM within the 32K segment selected by jumper 92-93 or 93-94.

NOTE

When using Intel 2364 chips, switch S4 establishes the 8K blocks of ROM within the selected 64K page.

As shown in table 2-12, each OFF position of S4 selects one 4K block (8K block for 2364 ROM). Thus, one OFF position is required for 2308/2708/2758 ROM/PROM, two OFF positions are required for 2316E/2716 ROM/PROM, and four OFF positions are required for 2332/2732/2364 ROM/PROM.

If 2316E/2716/2332/2732 chips are installed, the 4K blocks need not be contiguous. In this case however, the user must ensure that the same PROM(s) is not selected twice. If 2364 chips are installed, the 8K blocks need not be contiguous. Again, the user must ensure that the same PROM is not selected twice, e.g. if 2332/2732 chips are installed, switch S4 position 1 and 5 cannot both be used.

2-12. ROM/PROM TYPE SELECTION

Four 28 pin ROM/PROM sockets are provided on board. In the factory-wired configuration, these four sockets have a shorting plug in position 1 and 2, making them 24 pin sockets. (They are also renumbered for 24 pin use.) The factory-wired configuration provides space for four 2708 1K byte PROMs or four 2308 ROMs. By changing jumpers, the user may reconfigure the board for Intel 2758 PROMS, 2716 PROMS, 2316E ROMs, 2732 PROMs, 2332 ROMs, or 2364 ROMs, increasing the memory capacity from 4K bytes to a maximum of 32K bytes. The following paragraphs will explain the modifications necessary to change the ROM/PROM type.

Table 2-12. ROM/PROM Configuration vs. Address Space

INTEL 2708/2758 PROM/2308 ROM								
Switch S4 Positions Set To Off	Jumper 92-93				Jumper 93-94			
	A34 PROM 0	A46 PROM 1	A60 PROM 2	A76 PROM 3	A34 PROM 0	A46 PROM 1	A60 PROM 2	A76 PROM 3
1	0000-03FF	0400-07FF	0800-0BFF	0C00-0FFF	8000-83FF	8400-87FF	8800-8BFF	8C00-8FFF
2	1000-13FF	1400-17FF	1800-1BFF	1C00-1FFF	9000-93FF	9400-97FF	9800-9BFF	9C00-9FFF
3	2000-23FF	2400-27FF	2800-2BFF	2C00-2FFF	A000-A3FF	A400-A7FF	A800-ABFF	AC00-AFFF
4	3000-33FF	3400-37FF	3800-3BFF	3C00-3FFF	B000-B3FF	B400-B7FF	B800-BBFF	BC00-BFFF
5	4000-43FF	4400-47FF	4800-4BFF	4C00-4FFF	C000-C3FF	C400-C7FF	C800-CBFF	CC00-CFFF
6	5000-53FF	5400-57FF	5800-5BFF	5C00-5FFF	D000-D3FF	D400-D7FF	D800-DBFF	DC00-DFFF
7	6000-63FF	6400-67FF	6800-6BFF	6C00-6FFF	E000-E3FF	E400-E7FF	E800-EBFF	EC00-EFFF
8	7000-73FF	7400-77FF	7800-7BFF	7C00-7FFF	F000-F3FF	F400-F7FF	F800-FBFF	FC00-FFFF
INTEL 2716 PROM/2316E ROM								
1	0000-07FF	0800-0FFF			8000-87FF	8800-8FFF		
2			1000-17FF	1800-1FFF			9000-97FF	9800-9FFF
3	2000-27FF	2800-2FFF			A000-A7FF	A800-AFFF		
4			3000-37FF	3800-3FFF			B000-B7FF	B800-BFFF
5	4000-47FF	4800-4FFF			C000-C7FF	C800-CFFF		
6			5000-57FF	5800-5FFF			D000-D7FF	D800-DFFF
7	6000-67FF	6800-6FFF			E000-E7FF	E800-EFFF		
8			7000-77FF	7800-7FFF			F000-F7FF	F800-FFFF

Table 2-12. ROM/PROM Configuration vs. Address Space (Continued)

Switch S4 Positions Set To Off	Jumper 92-93				Jumper 93-94			
	A34 PROM 0	A46 PROM 1	A60 PROM 2	A76 PROM 3	A34 PROM 0	A46 PROM 1	A60 PROM 2	A76 PROM 3
INTEL 2332 ROM/2732 PROM								
1	0000-0FFF				8000-8FFF			
2		1000-1FFF				9000-9FFF		
3			2000-2FFF				A000-AFFF	
4				3000-3FFF				B000-BFFF
5	4000-4FFF				C000-CFFF			
6		5000-5FFF				D000-DFFF		
7			6000-6FFF				E000-EFFF	
8				7000-7FFF				F000-FFFF
INTEL 2364 ROM								
1	0000-1FFF							
2		2000-3FFF						
3			4000-5FFF					
4				6000-7FFF				
5	8000-9FFF							
6		A000-BFFF						
7			C000-CFFF					
8				E000-FFFF				

2-13. JUMPER CHANGES FOR 2758 PROM. The jumper block in position W13 must be moved to position W14 (see figure 2-2 for location). If the power reduction option is to be used, additional jumpers must be added or removed. See paragraph 2-18.

2-14. JUMPER CHANGES FOR 2316E ROM AND 2716 PROM. The jumper block in position W13 must be moved to position W15 (see figure 2-2 for location). If the power reduction option is to be used (2716 only) additional jumpers must be added and removed. See paragraph 2-18.

2-15. JUMPER CHANGES FOR 2332 ROM. The jumper block in position W13 must be moved to position W16 (see figure 2-2 for location). The jumper between jumper posts 24 and 25 must be removed (see figure 2-2 for location).

2-16. JUMPER CHANGES FOR 2732 PROM. The jumper block in position W13 must be moved to position W16 (see figure 2-2 for location). If the power reduction option is to be used, additional jumpers must be added and removed. See paragraph 2-18.

2-17. JUMPER CHANGES FOR 2364 ROM. The jumper block in position W12 must be moved to position W11. The jumper block in position W13 must be moved to position W16 and the jumper between jumper posts 24 and 25 must be removed. The shorting pin in positions 1 and 2 of sockets A34, A46, A60, and A76 must be removed (see figure 2-2 for locations).

2-18. PROM POWER REDUCTION OPTION. When the power reduction option is used with the 2716, 2732, and 2758 PROM, the access timing must be changed. Remove the jumper between jumper posts 24 and 25. Remove the jumper at W1 from C-H (see figure 2-3 for location) and place at W1 jumper E-H. This completes the PROM power reduction.

NOTE

If the PROM being used has a CE to output delay (t_{CE}) of 390 ns or less (e.g. the 2716-2) it is not required to change the XACK timing jumper (W1).

2-19. I/O BASE ADDRESS

The interrupt, timer, and serial and parallel port functions are accessed by the bus master with I/O Read and I/O Write Commands. These commands are relative to an 8-bit (12-bit in an 8086-based system) hexadecimal base address that is a multiple of 16H. Jumper 86-87 or 87-88 (see figure 2-3 for location) restricts the board to the lower or upper 128 system I/O addresses in an 8-bit I/O address. In the 12-bit I/O address, jumper 86-87 or 87-88 restricts the board to the lower or upper 128 system I/O addresses within one of 16 I/O location pages. The pages are restricted to the lower or upper eight pages by jumper 21-22 or 22-23 (see figure 2-3 for location). Refer to table 2-13 for details of selections for the 8-bit I/O base address selection and table 2-14 for the I/O page selection.

Jumper pad S2 provides eight possible jumper configurations for selecting the desired I/O base address within the upper or lower 128 system addresses selected by jumper 87-88 or 88-89. Jumper pad S5 provides eight possible jumper configurations for selecting the desired I/O page within the upper or lower eight pages. An additional jumper position is provided at jumper pad S5 (8-bit) for use when an eight bit address is selected. The iSBC 108A/116A boards are shipped with the I/O base address D0H selected (8-bit addressing enabled).

EXAMPLE

8-bit mode Desired base address: 60H
Jumper: 86-87, S2 1-3 and S5 1-2

12-Bit mode Desired base address: 9B0H
Jumper: 22-23, S5 1-9 and 87-88, S2 1-6

Table 2-13. I/O Base Address Selection

I/O Base Address [1,4]	Jumper Connection	Jumper Pad S2 Connection [3]	I/O Base Address [1,4]	Jumper Connection	Jumper Pad S2 Connection [3]
X00	86-87	1-9	X80	87-88	1-9
X10	86-87	1-8	X90	87-88	1-8
X20	86-87	1-8	XA0	87-88	1-7
X30	86-87	1-6	XB0	87-88	1-6
X40	86-87	1-5	XC0	87-88	1-5
X50	87-86	1-4	XD0 [2]	87-88 [2]	1-4 [2]
X60	86-87	1-3	XE0	87-88	1-3
X70	86-87	1-2	XF0	87-88	1-2

[1] Default jumper S5 1-2 enables 8-bit addressing. For 12-bit addressing, remove S5 1-2 and see Table 2-14.

[2] Default (factory) configuration.

[3] All pins on right side of array S2 are connected together and labeled pin 1. Any of the pin 1s may be used for jumpering.

[4] X = Page address selection.

Table 2-14. I/O Page Selection

I/O Page Selection [1]	Jumper Connection	Jumper Pad S5 Connection [2]	I/O Page Selection [1]	Jumper Connection	Jumper Pad S5 Connection [2]
0X0	21-22 [3]	1-10	8X0	22-23	1-10
1X0	21-22	1-9	9X0	22-23	1-9
2X0	21-22	1-8	AX0	22-23	1-8
3X0	21-22	1-7	BX0	22-23	1-7
4X0	21-22	1-6	CX0	22-23	1-6
5X0	21-22	1-5	DX0	22-23	1-5
6X0	21-22	1-4	EX0	22-23	1-4
7X0	21-22	1-3	FX0	22-23	1-3

[1] X = base address selection.

[2] All pins on right side of array S5 are connected together and labeled pin 1. Any of the pin 1s may be used for jumpering.

[3] Default (factory) configuration.

2-20. ADVANCED ACKNOWLEDGE

After issuing a Read or Write Command, the bus master requires a Transfer Acknowledge (XACK/) or an Advanced Acknowledge (AACK/) response from the addressed board. The response (XACK/ or AACK/) informs the bus master of the status of the read or write operation.

All systems can use the XACK/ signal. However, in some systems, use of the AACK/ signal may increase the system throughput. *Use of the AACK/ signal is not recommended.*

NOTE

The iSBC 108A/116A boards will not generate an acknowledge (XACK) if a write to PROM is attempted. This must be taken into consideration when debugging a system with an ICE in-circuit emulator.

Jumper W1 (see figure 2-3 for location) establishes the AACK/ and XACK/ timing for I/O and PROM addressed commands. The default wiring is for use with the iSBC 80/86 system processors. Any AACK/ or XACK/ timing other than that provided by the factory default wiring is at the discretion of the user. Refer to table 2-15 for AACK/ and XACK/ timing options.

Table 2-15. AACK/ and XACK/ Jumper Selection

Jumper Pad W1	Command to AACK/ Delay (n sec)	
	Min	Max
*A-G	80	190
B-G	126	233
C-G	172	278
D-G	217	324
E-G	262	369
F-G	AACK Disabled	
Jumper Pad W1	**Command to XACK/ Delay (n sec)**	
	Min	Max
A-H	360	480
B-H	405	530
*C-H	450	575
D-H	495	620
E-H	540	660
F-H	XACK Disabled	

*Denotes factory wired default configuration.

2-21. SERIAL I/O PORT

The iSBC 108A/116A series boards contain a serial I/O port that may be configured to conform to user serial data transmission protocols. Jumpers are provided to select internal or external clock sources, baud rate, interrupt sources, and operation as a data terminal or as a data set. Jumpers connect the baud rate clock to the DTE TXC line, or activate the STXD output via Port XA of the parallel I/O interface.

2-22. CLOCK SOURCE. Jumpers select either onboard or external clock signals for the transmitter clock (TXC) and receiver clock (RXC) via pins J3-3 and J3-7 respectively. The factory-wired default configuration supplies the onboard baud rate clock to TXC and RXC via jumpers 9-10 and 8-7, respectively. (See figure 2-4 for location). By connecting jumper 11-10, an external Transmit Clock signal is applied to TXC. Jumper 6-7 supplies an external Receiver Clock to RXC.

2-23. BAUD RATE. In the Synchronous Mode, the baud rate is selected by jumper wiring alone. In the Asynchronous Mode, the baud rate is selected by jumper wiring in conjunction with software control. Refer to paragraph 3-5 for details of software modification of baud rates. Jumper pad S1 and jumpers 1-2 and 3-5 (see figure 2-4 for location), select baud rates. The factory-wired default settings are: for jumper pad S1, jumper 4-1 and jumper 1-2 and 3-5 open. Refer to table 2-16 for specific baud rate jumper information.

2-24. SERIAL I/O INTERRUPTS. Two serial I/O interrupts, SIOR1 and SIOT1, may be controlled by jumper selection. The factory-wired default jumper 85–84 applies RXR (Receiver Ready) to the SIOR1 line. SIOR1 may be disabled by deleting this jumper and connecting jumper 83-84. The factory-wired default jumper 81–79 applies TXR (Transmitter Ready) to the SIOT1 line. To apply TXE (Transmitter Empty) to this interrupt line, delete jumper 81–79 and add jumper 80–79. To disable SIOT1 delete jumper 81–79 and add jumper 82–79. See figure 2-3 for jumper locations.

2-25. DATA SET/DATA TERMINAL CONFIGURATION. The serial I/O interface may be configured as a data terminal or as a data set. The factory default configuration is for the serial I/O to be configured as a data terminal for operation in conjunction with an external data set (e.g. a Modem). For certain applications, it may be necessary to convert to data set operation in conjunction with an external data terminal (e.g. a CRT). To convert to data set operation, proceed as follows:

a. Remove DIP header jumper assembly from W3.

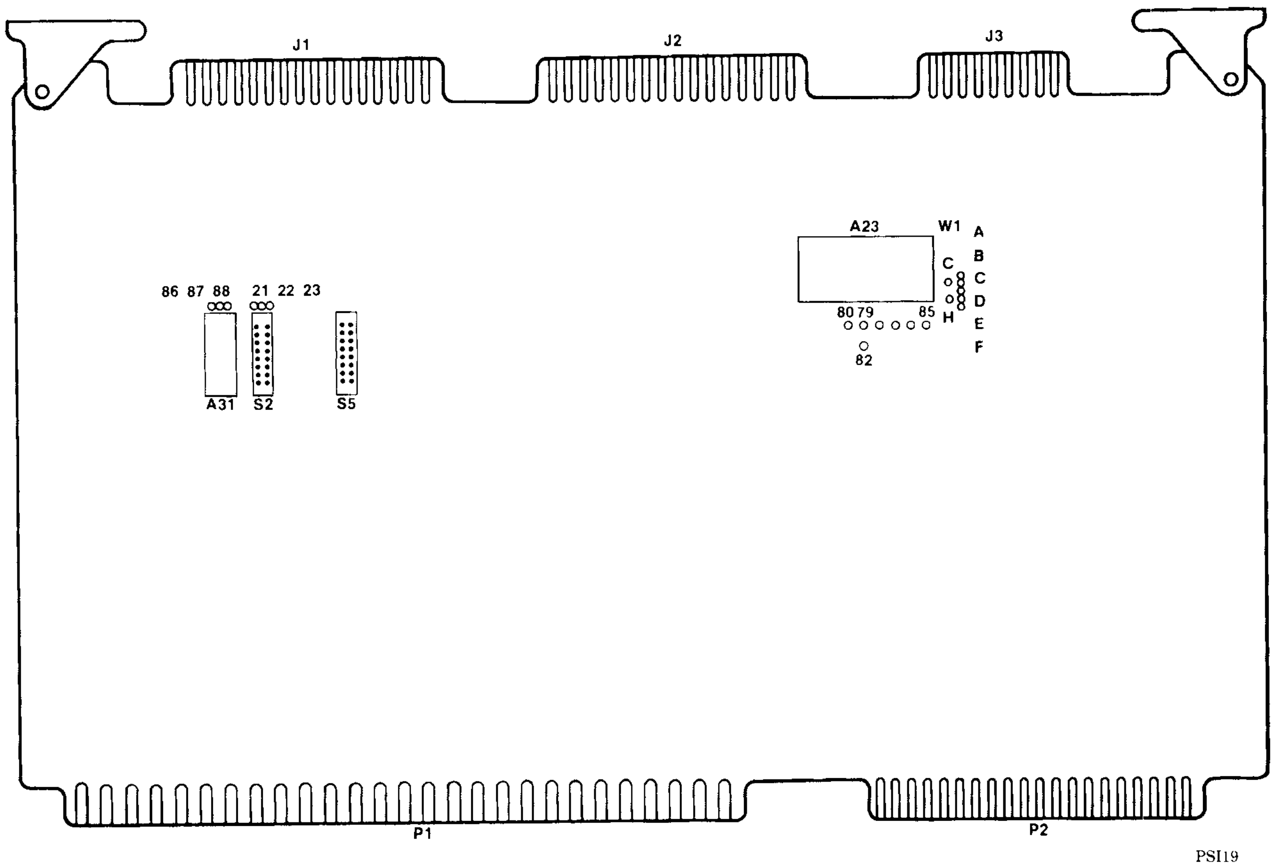


Figure 2-3. Jumper Option Locations

Table 2-16. Baud Rate Select Jumpers

Baud Rate (X)			Jumper Connection S1 [4]	Other Jumper Connection [1]
Synchronous Mode (X)	Asynchronous Mode [3] X/16	Asynchronous Mode [3] X/64		
307.2K	19.2K	4.8K	3-1	—
153.6K	9.6K	2.4K	4-1 [2]	—
76.8K	4.8K	1200	5-1	—
38.4K	2.4K	600	6-1	—
19.2K	1200	300	7-1	—
9.6K	600	150	8-1	—
4.8K	300	75	9-1	—
6.98K	—	110	9-1 [1]	1-2 3-5

[1] Jumper 9-1 on S1 normally produces a 4.8K baud rate; adding jumper 1-2 produces a 6.98K baud rate divisible to 110 baud for teletype use. Jumper 3-5 is used to correct the interval timer divide ratio.

[2] Denotes factory wired default configuration.

[3] The divisor is software-selected. Refer to paragraph 3-5.

[4] All pins on left side of array S1 are connected together and labeled pin 1. Any of the pin 1s may be used for jumpering.

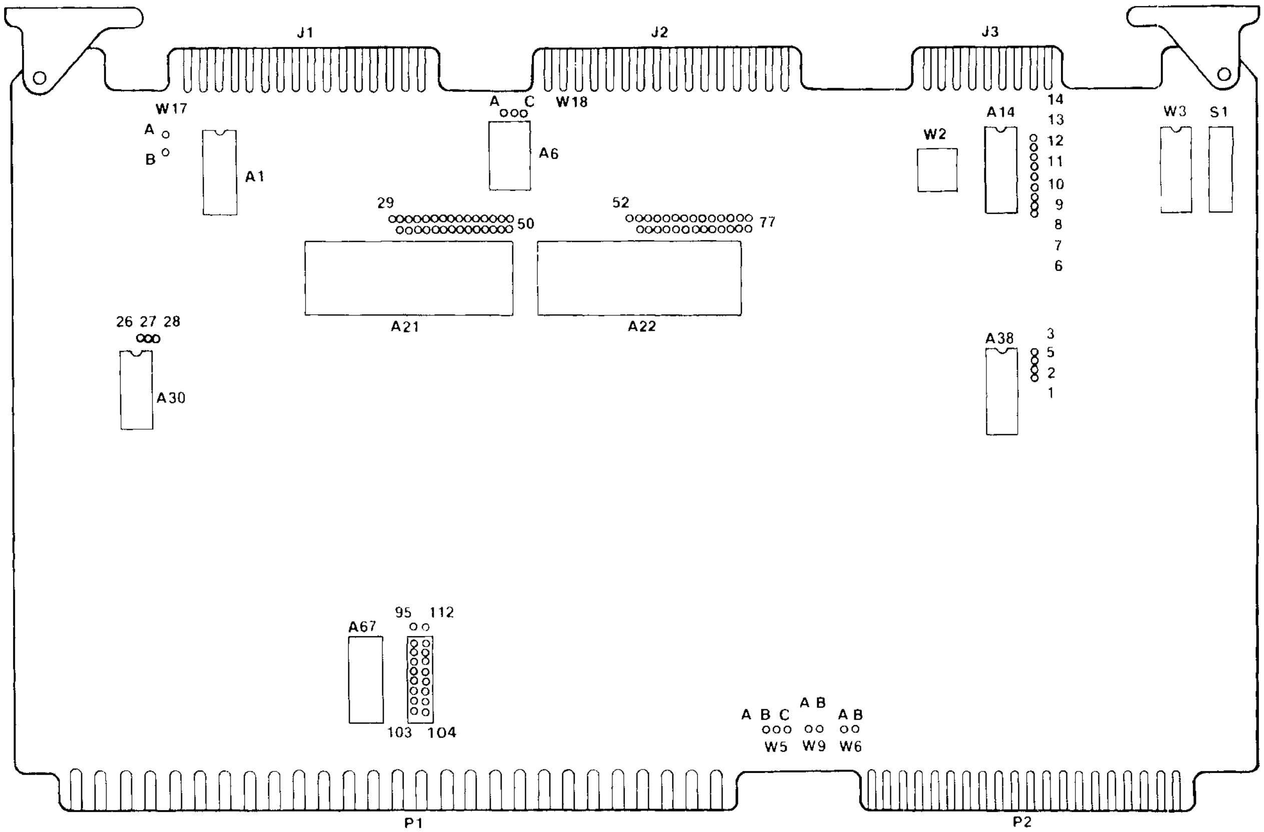


Figure 2-4. Jumper locations for Clock Source, Baud Rate, Interrupts, Parallel I/O Ports, and Power Options

Table 2-17. Clock Path Options

Option	Baud Rate	Ext Clk	Jumper	W3
DTE TXC	9-10*	11-10	14-13*	1-18*
STXD	9-10	11-10	12-13	9-10
*Indicates factory-wired default configuration.				

b. Wire a DIP header jumper assembly so that the following signals are reversed: (1) TXD and RXD, (2) RTS and CTS, (3) DSR and DTR. Other signals may need to be reversed depending on the particular application.

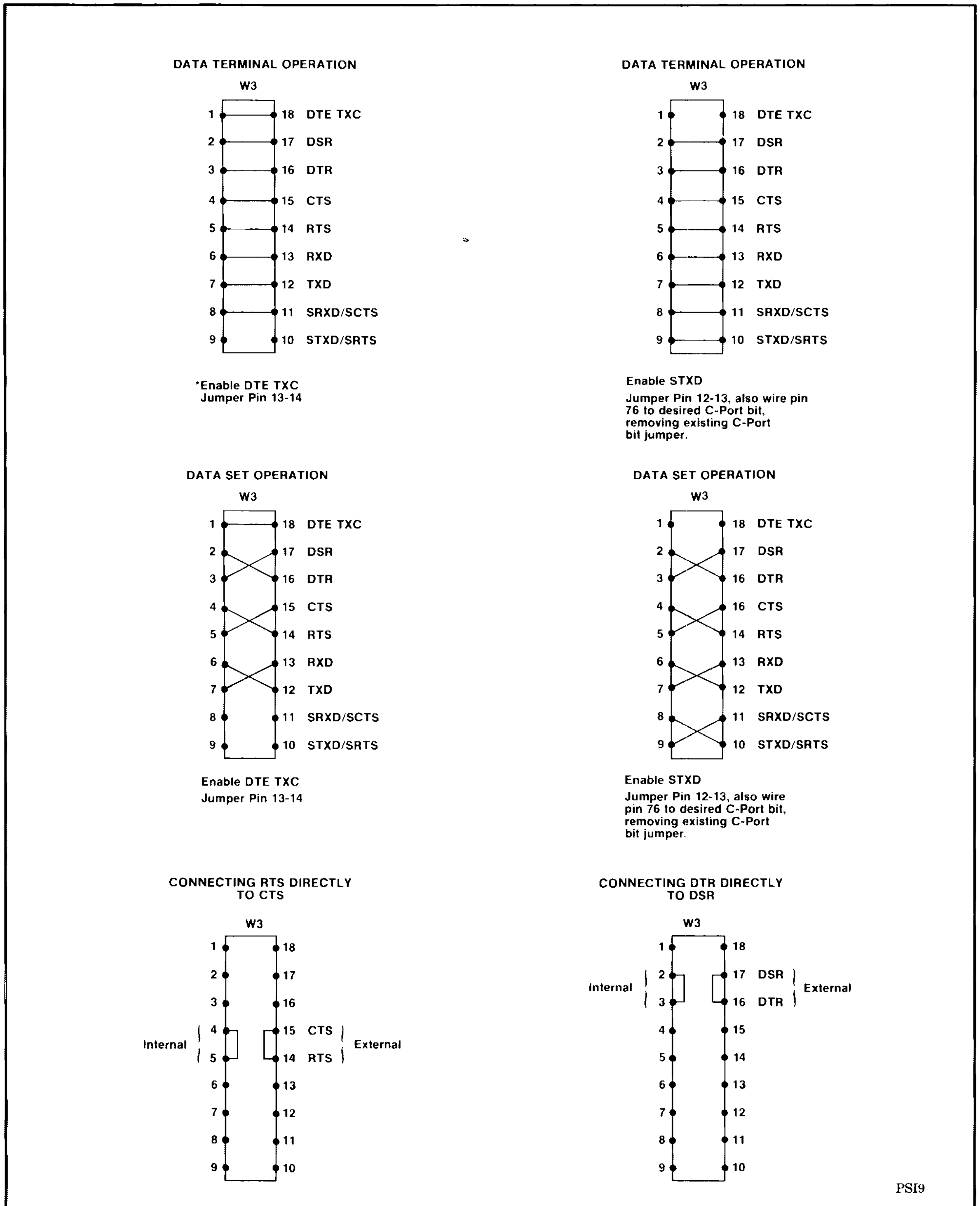
c. Place reconfigured DIP header jumper assembly in W3.

Figure 2-5 illustrates several optional configurations for serial I/O operation.

2-26. CLOCK PATH OPTIONS. The clock frequency supplied to pin 9 (TXC) of the 8251A, whether the baud rate clock or an external clock signal, may be connected to either the DTE TXC pin of J3 or the STXD pin of J3. The jumpers necessary for these connections are listed in table 2-17. Note that the selection of either the STXD or DTE TXC option disallows the other.

2-27. PARALLEL I/O PORTS

Each of the two 8255A Programmable Peripheral Interface devices on the board has its own associated jumpers. These jumpers, in combination with the programming considerations listed in paragraph 3-16, allow the user many possible configurations of signal paths. For this reason, the programming alternatives must be examined before jumper configuration takes place.



*DENOTES FACTORY WIRED DEFAULT CONFIGURATION

Figure 2-5. DIP Header Jumper W3 Configurations

Jumper posts 29 through 51 are associated with Port X+6 on device A21; jumper posts 52 through 74 are associated with Port X+A on device A22, and jumper posts 75 through 78 are associated with signals from connector J3 and the 8251A serial I/O device. Ports X+6 and X+A are factory-wired in a default configuration with 11 jumpers. These jumpers connect bits 0 through 7 of Port X+6 to J1 and bits 0 through 7 of Port X+A to J2, disable the four parallel I/O port interrupt lines PIOA1, PIOA2, PIOB1, and PIOB2, and enable the bidirectional bus drivers A1, A2, A7, and A8 for output operation.

NOTE

Table 2-18 provides a list of 21 configurations of a single 8255A device, and table 2-19 details the jumper wiring required for each configuration. Figure 2-4 shows the location of the jumpers.

2-28. INTERRUPTS

Eight interrupts are available on the board, labeled INR0/ through INR7/. INR1/ and INR2/ are generated by the 8251A serial I/O device (from signals SIOT1 and SIOR1), INR3/, INR4/, INR5/, and INR6/ are generated by the two 8255A parallel I/O devices (using signals PIOA1 and PIOB1 from A21 and PIOA2 and PIOB2 from A22). INR7/ is an external interrupt from pin J2-50. INR0/ may be generated by either the Interval Timer A39-6 signal, or by the external interrupt pin J1-50, selectable by jumper wiring. The factory-wired default configuration, which specifies the interrupt signal from the Interval Timer, is jumper 28-27. To enable the external interrupt from J1-50, replace jumper 28-27 with jumper 26-27.

As illustrated in figure 2-6, jumper pins 95 through 103 are dedicated to interrupt signals INR0/ through

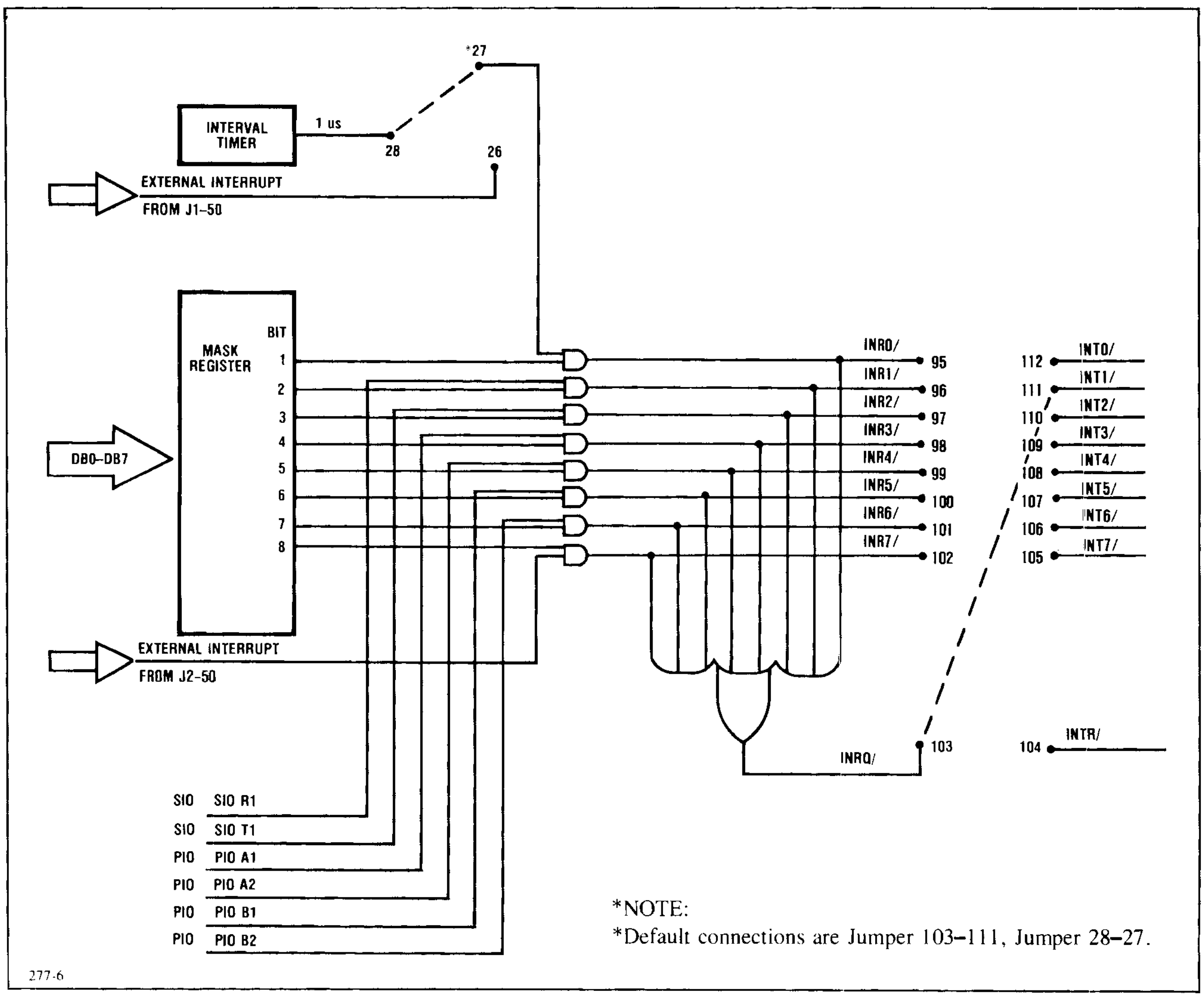


Figure 2-6. iSBC 108A/116A™ Board Interrupt Signals

INR7/ and the system interrupt request INRQ/. A corresponding series of jumper pins, 104 through 112, are dedicated to pins on connector P1. The location of these pins is shown in figure 2-4. Any interrupt request signal can be wired to any available interrupt jumper pin. The factory-wired default configuration is jumper 103-111, which places the interrupt request INRQ/ signal at pin 42 of P1 which is INT1.

2-29. AUXILIARY POWER

Auxiliary power can be provided, via 60-pin double-sided edge connector, P2, to protect memory contents in case of main power failure. This supply must deliver +5V, -5V, and -12V for the RAM array, the clock generator A58, the Dynamic RAM Controller A50, and associated support logic.

Once an appropriate power supply has been provided at connector P2, the auxiliary power is enabled by removing jumpers W5, W6, and W9. Figure 2-4 shows the location of the jumpers.

In order to protect the module against improper installation of the connector on P2, a keyslot is provided between pins 15-16 and 17-18.

2-30. TELETYPE ADAPTOR POWER

Inserting a jumper pack in W2 supplies +5V, -12V, and +12V to connector J3 for use with an iSBC 530 TTY adaptor. Figure 2-4 shows the location of W2.

CAUTION

Ensure that connector J3 is properly installed. If J3 is installed backwards, the I/O device may be damaged.

2-31. ADDITIONAL POWER CONNECTION OPTIONS

Adding a jumper between pins A and B at W17 supplies +5V to J1-50 for use by the user. If the jumper at W17 is installed, pin 26 must be left unconnected.

Table 2-18. Parallel I/O Configuration Key

CON.	X+4 AND X+8	X+5 AND X+9	PORT X+6 AND X+A COMMENTS
1	MODE 0-I	MODE 0-I/O	Bidirectional I/O
2	MODE 0-O	MODE 0-I/O	Bidirectional I/O
3	MODE 0-I	MODE 1-I/O	Bit 0 ($INTR_B$) to PIOB2; Bit 7 unused
3A	MODE 0-I	MODE 1-I/O	Bit 0 ($INTR_B$) to PIOB2; Bit 7 unused
4	MODE 0-I	MODE 1-I/O	Bit 0 ($INTR_B$) to PIOB2; Bit 7 unused
5	MODE 0-O	MODE 1-I/O	Bit 0 ($INTR_B$) to PIOB2; Bit 7 unused
5A	MODE 0-O	MODE 1-I/O	Bit 0 ($INTR_B$) to PIOB2; Bit 7 unused
6	MODE 0-O	MODE 1-I/O	Bit 0 ($INTR_B$) to PIOB2; Bit 7 unused
7	MODE 1-I	MODE 0-I/O	Bit 3 ($INTR_A$) to PIOA2
7A	MODE 1-I	MODE 0-I/O	Bit 3 ($INTR_A$) to PIOA2
8	MODE 1-I	MODE 0-I/O	Bit 3 ($INTR_A$) to PIOA2
9	MODE 1-O	MODE 0-I/O	Bit 3 ($INTR_A$) to PIOA2
9A	MODE 1-O	MODE 0-I/O	Bit 3 ($INTR_A$) to PIOA2
10	MODE 1-O	MODE 0-I/O	Bit 3 ($INTR_A$) to PIOA2
11	MODE 1-I	MODE 1-I/O	Bit 0 ($INTR_B$) to PIOB2; Bit 3 ($INTR_A$) to PIOA2
12	MODE 1-I	MODE 1-I/O	Bit 0 ($INTR_B$) to PIOB2; Bit 3 ($INTR_A$) to PIOA2
13	MODE 1-O	MODE 1-I/O	Bit 0 ($INTR_B$) to PIOB2; Bit 3 ($INTR_A$) to PIOA2
14	MODE 1-O	MODE 1-I/O	Bit 0 ($INTR_B$) to PIOB2; Bit 3 ($INTR_A$) to PIOA2
15	MODE 2-B	MODE 0-I/O	Bit 0 is OPEN; Bit 3 ($INTR_A$) to PIOA2
16	MODE 2-B	MODE 0-I/O	Bit 0 is OPEN; Bit 3 ($INTR_A$) to PIOA2
17	MODE 2-B	MODE 1-I/O	Bit 0 ($INTR_B$) to PIOB2; Bit 3 ($INTR_A$) to PIOA2
I = INPUT O = OUTPUT I/O = BIDIRECTIONAL INPUT/OUTPUT			

Table 2-19. Parallel I/O Configuration List

8255A #2 A22 (PORTS X+8, X+9, X+A)						
CONFIGURATION NUMBER	INSTALL AT X+A		DELETE JUMPER	ADD JUMPER	FINAL JUMPER CONFIGURATION	X+A PINS
	DRIVERS	TERM.				
1	As Required	As Required	52-53	53-54	53-54 61-62 71-72 59-60 63-64 57-58 65-66 55-56 67-68 69-70 73-74	C_0 (J2-24) C_4 (J2-26) C_1 (J2-22) C_5 (J2-28) C_2 (J2-20) C_6 (J2-30) C_3 (J2-18) C_7 (J2-32)
2	As Required	As Required	— —	— —	52-53 61-62 71-72 59-60 63-64 57-58 65-66 55-56 67-68 69-70 73-74	See Configuration 1
3	A10	A9	52-53 61-62 63-64 59-60 67-68 57-58 69-70 55-56 73-74	53-54 62-63 64-74 60-69 55-68 58-67 59-70	53-54 62-63 71-72 60-69 64-74 58-67 65-66 55-68 59-70	C_0 (PIOB2) C_4 (J2-24) C_1 (J2-22) C_5 (J2-18) C_2 (J2-32) C_6 (J2-20) C_3 (J2-28) C_7 OPEN
3 Alternate Configuration	A9	A10	52-53 55-56 63-64 65-66 73-74	53-54 64-74 55-66	53-54 61-62 71-72 59-60 64-74 57-58 55-66 67-68 69-70	C_0 (PIOB2) C_4 (J2-26) C_1 (J2-32) C_5 (J2-28) C_2 (J2-20) C_6 (J2-30) C_3 (J2-18) C_7 OPEN
4	A10	A9	52-53 55-56 63-64 67-68	53-54 64-74 55-68	53-54 61-62 71-72 59-60 64-74 57-58 65-66 55-68 69-70	C_0 (PIOB2) C_4 (J2-26) C_1 (J2-22) C_5 (J2-28) C_2 (J2-32) C_6 (J2-30) C_3 (J2-18) C_7 OPEN
5	A10	A9	63-64 61-62 67-68 59-60 69-70 57-58 73-74 55-56	64-74 62-63 55-68 60-69 59-70 58-67	52-53 62-63 71-72 60-69 64-74 58-67 65-66 55-68 59-70	See Configuration 3
5 Alternate Configuration	A9	A10	63-64 55-56 65-66 73-74	64-74 55-66	52-53 61-62 71-72 59-60 64-74 57-58 55-66 67-68 69-70	See Configuration 3 Alternate
6	A10	A9	63-64 55-56 67-68	53-54 64-74 55-68	52-53 61-62 71-72 59-60 64-74 57-58 65-66 55-68 69-70	See Configuration 4
7	A10	A9	52-53 59-60 71-72 57-58 63-64 55-56 65-66 67-68 69-70	53-54 60-69 57-64 58-67 59-66 56-63 55-68 70-71	53-54 61-62 57-64 60-69 59-66 58-67 55-68 56-63 70-71 73-74	C_0 (J2-30) C_4 (J2-26) C_1 (J2-28) C_5 (J2-18) C_2 (J2-32) C_6 (J2-20) C_3 (PIOA2) C_7 (J2-24)

Table 2-19. Parallel I/O Configuration List (Continued)

8255A #2 A22 (PORTS X+8, X+9, X+A)						
CONFIGURATION NUMBER	INSTALL AT X+A DRIVERS	INSTALL AT X+A TERM.	DELETE JUMPER	ADD JUMPER	FINAL JUMPER CONFIGURATION	X+A PINS
7 Alternate Configuration	A9	A10	52-53 61-62 71-72 69-70	53-54 62-69 70-71	53-54 62-69 63-64 59-60 65-66 57-58 67-68 55-56 70-71 73-74	C_0 (J2-24) C_4 (J2-18) C_1 (J2-22) C_5 (J2-28) C_2 (J2-20) C_6 (J2-30) C_3 (PIOA2) C_7 (J2-32)
8	A10	A9	52-53 59-60 71-72 69-70	53-54 60-69 70-71	53-54 61-62 63-64 60-69 65-66 57-58 67-68 55-56 70-71 73-74	C_0 (J2-24) C_4 (J2-26) C_1 (J2-22) C_5 (J2-18) C_2 (J2-20) C_6 (J2-30) C_3 (PIOA2) C_7 (J2-32)
9	A10	A9	71-72 61-62 63-64 59-60 65-66 55-56 67-68 69-70	61-64 62-67 59-66 60-63 55-68 56-69 70-71	52-53 62-67 61-64 60-63 59-66 57-58 55-68 56-69 70-71 73-74	C_0 (J2-26) C_4 (J2-20) C_1 (J2-28) C_5 (J2-24) C_2 (J2-32) C_6 (J2-30) C_3 (PIOA2) C_7 (J2-18)
9 Alternate Configuration	A9	A10	71-72 57-58 69-70	70-71 58-69	52-53 61-62 63-64 59-60 65-66 58-69 67-68 55-56 70-71 73-74	C_0 (J2-24) C_4 (J2-26) C_1 (J2-22) C_5 (J2-28) C_2 (J2-20) C_6 (J2-18) C_3 (PIOA2) C_7 (J2-32)
10	A10	A9	71-72 55-56 69-70	70-71 56-69	52-53 61-62 63-64 59-60 65-66 57-58 67-68 56-69 70-71 73-74	C_0 (J2-24) C_4 (J2-26) C_1 (J2-22) C_5 (J2-28) C_2 (J2-20) C_6 (J2-30) C_3 (PIOA2) C_7 (J2-18)
11	A10	A9	52-53 59-60 71-72 55-56 63-64 67-68 69-70 73-74	53-54 60-69 64-74 56-59 55-68 70-71	53-54 61-62 64-74 60-69 65-66 57-58 55-68 56-59 70-71	C_0 (PIOB2) C_4 (J2-26) C_1 (J2-22) C_5 (J2-18) C_2 (J2-32) C_6 (J2-30) C_3 (PIOA2) C_7 (J2-28)
12	A10	A9	52-53 59-60 71-72 57-58 63-64 55-56 67-68 69-70 73-74	53-54 60-69 64-74 58-67 55-68 56-69 70-71	53-54 61-62 64-74 60-69 65-66 58-67 55-68 56-69 70-71	C_0 (PIOB2) C_4 (J2-26) C_1 (J2-22) C_5 (J2-18) C_2 (J2-32) C_6 (J2-20) C_3 (PIOA2) C_7 (J2-24)
13	A10	A9	71-72 55-56 63-64 67-68 69-70 73-74	64-74 56-69 55-68 70-71	52-53 61-62 64-74 59-60 65-66 57-58 55-68 56-69 70-71	C_0 (PIOB2) C_4 (J2-26) C_1 (J2-22) C_5 (J2-28) C_2 (J2-32) C_6 (J2-30) C_3 (PIOA2) C_7 (J2-18)
14	A10	A9	71-72 61-62 63-64 59-60 67-68 55-56 69-70 73-74	64-74 62-67 55-68 60-63 70-71 56-69	52-53 62-67 64-74 60-63 65-66 57-58 55-68 56-69 70-71	C_0 (PIOB2) C_4 (J2-20) C_1 (J2-22) C_5 (J2-24) C_2 (J2-32) C_6 (J2-30) C_3 (PIOA2) C_7 (J2-18)

Table 2-19. Parallel I/O Configuration List (Continued)

8255A #2 A22 (PORTS X+8, X+9, X+A)

CONFIGURATION NUMBER	INSTALL AT X+A DRIVERS	INSTALL AT X+A TERM.	DELETE JUMPER	ADD JUMPER	FINAL JUMPER CONFIGURATION	X+A PINS
15	A10	A9	52-53 59-60 71-72 55-56 63-64 65-66 67-68 69-70 73-74	59-66 60-63 55-68 53-58 70-71 56-69	59-66 61-62 55-68 60-63 70-71 57-58 53-58 56-69	C_0 OPEN C_4 (J2-26) C_1 (J2-22) C_5 (J2-24) C_2 (J2-32 C_6 (J2-30) C_3 (PIOA2) C_7 (J2-18)
16	A10	A9	52-53 59-60 71-72 55-56 63-64 69-70 73-74	70-71 60-63 53-58 56-59	65-66 61-62 67-68 60-63 70-71 57-58 53-58 56-69	C_0 OPEN C_4 (J2-26) C_1 (J2-22) C_5 (J2-24) C_2 (J2-20) C_6 (J2-30) C_3 (PIOA2) C_7 (J2-18)
17	A10	A9	52-53 59-60 71-72 55-56 63-64 67-68 69-70 73-74	64-74 60-63 55-68 56-69 70-71	64-74 61-62 65-66 60-63 55-68 57-58 70-71 53-58 56-69	C_0 (PIOB2) C_4 (J2-26) C_1 (J2-22) C_5 (J2-24) C_2 (J2-32) C_6 (J2-30) C_3 (PIOA2) C_7 (J2-18)

8255A #1 A21 (PORTS X+4, X+5, X+6)

CONFIGURATION NUMBER	INSTALL AT X+6 DRIVERS	INSTALL AT X+6 TERM.	DELETE JUMPER	ADD JUMPER	FINAL JUMPER CONFIGURATION	X+6 PINS
1	As Required	As Required	30-31	29-30	29-30 38-39 40-41 36-37 42-43 34-35 44-45 32-33 46-47 48-49 50-51	C_0 (J1-24) C_4 (J1-26) C_1 (J1-22) C_5 (J1-28) C_2 (J1-20) C_6 (J1-30) C_3 (J1-18) C_7 (J1-32)
2	As Required	As Required	— —	— —	30-31 38-39 40-41 36-37 42-43 34-35 44-45 32-33 46-47 48-49 50-51	See Configuration 1
3	A4	A3	30-31 38-39 42-43 36-37 46-47 34-35 48-49 32-33 50-51	29-30 39-42 43-45 37-38 32-47 35-36 36-49	29-30 39-42 40-41 37-48 43-50 35-46 44-45 32-47 36-49	C_0 (PIOB1) C_4 (J1-24) C_1 (J1-22) C_5 (J1-18) C_2 (J1-32) C_6 (J1-20) C_3 (J1-28) C_7 OPEN
3 Alternate Configuration	A3	A4	30-31 32-33 42-43 44-45 50-51	29-30 43-50 32-45	29-30 38-39 40-41 36-37 43-50 34-35 32-45 46-47 48-49	C_0 (PIOB1) C_4 (J1-26) C_1 (J1-32) C_5 (J1-28) C_2 (J1-20) C_6 (J1-30) C_3 (J1-18) C_7 OPEN
4	A4	A3	30-31 32-33 42-43 46-47	29-30 43-50 32-47	29-30 38-39 40-41 36-37 43-50 34-35 44-45 32-47 48-49	C_0 (PIOB1) C_4 (J1-26) C_1 (J1-22) C_5 (J1-28) C_2 (J1-32) C_6 (J1-30) C_3 (J1-18) C_6 OPEN

Table 2-19. Parallel I/O Configuration List (Continued)

8255A #1 A21 (PORTS X+4, X+5, X+6)						
CONFIGURATION NUMBER	INSTALL AT X+6		DELETE JUMPER	ADD JUMPER	FINAL JUMPER CONFIGURATION	X+6 PINS
	DRIVERS	TERM.				
5	A4	A3	42-43 38-39 46-47 36-37 48-49 34-35 50-51 32-33	43-50 39-42 32-47 37-48 36-49 35-46	30-31 39-42 40-41 37-38 43-50 35-46 44-45 32-47 36-49	See Configuration 3
5 Alternate Configuration	A3	A4	42-43 32-33 44-45 50-51	43-50 32-45	30-31 38-39 40-41 36-37 43-50 34-35 32-45 46-47 48-49	See Configuration 3 Alternate
6	A4	A3	42-43 32-33 46-47	29-30 43-50 32-47	30-31 38-39 40-41 36-37 43-50 34-35 44-45 32-47 48-49	See Configuration 4
7	A4	A3	30-31 36-37 40-41 34-35 42-43 32-33 44-45 46-47 48-49	29-30 36-48 34-43 35-46 36-45 33-42 32-47 40-49	29-30 38-39 34-43 36-48 36-45 35-36 32-47 32-42 40-49 50-51	C_0 (J1-30) C_4 (J1-26) C_1 (J1-28) C_5 (J1-18) C_2 (J1-32) C_6 (J1-20) C_3 (PIOA1) C_7 (J1-24)
7 Alternate Configuration	A3	A4	30-31 38-39 40-41 48-49	29-30 39-48 40-49	29-30 39-48 42-43 36-37 44-45 34-35 46-47 32-33 40-49 50-51	C_0 (J1-24) C_4 (J1-18) C_1 (J1-22) C_5 (J1-28) C_2 (J1-20) C_6 (J1-20) C_3 (PIOA1) C_7 (J1-32)
8	A4	A3	30-31 36-37 40-41 48-49	29-30 37-48 40-49	29-30 38-39 42-43 37-48 44-45 34-35 46-47 32-33 40-49 50-51	C_0 (J1-24) C_4 (J1-26) C_1 (J1-22) C_5 (J1-18) C_2 (J1-20) C_6 (J1-30) C_3 (PIOA1) C_7 (J1-32)
9	A4	A3	40-41 38-39 42-43 36-37 44-45 32-33 46-47 48-49	38-43 39-46 36-45 37-42 32-37 33-48 40-49	30-31 39-46 38-43 37-42 36-45 34-35 32-47 33-48 40-49 50-51	C_0 (J1-26) C_4 (J1-20) C_1 (J1-28) C_5 (J1-24) C_2 (J1-32) C_6 (J1-30) C_3 (PIOA1) C_7 (J1-18)
9 Alternate Configuration	A3	A4	40-41 34-35 48-49	40-49 35-48	30-31 38-39 42-43 36-37 44-45 35-48 46-47 32-33 40-49 50-51	C_0 (J1-24) C_4 (J1-26) C_1 (J1-22) C_5 (J1-28) C_2 (J1-20) C_6 (J1-18) C_3 (PIOA1) C_7 (J1-32)
10	A4	A3	40-41 32-33 48-49	40-49 33-48	30-31 38-39 42-43 36-37 44-45 34-35 46-47 33-48 40-49 50-51	C_0 (J1-24) C_4 (J1-26) C_1 (J1-22) C_5 (J1-28) C_2 (J1-20) C_6 (J1-30) C_3 (PIOA1) C_6 (J1-18)

Table 2-19. Parallel I/O Configuration List (Continued)

8255A #1 A21 (PORTS X+4, X+5, X+6)						
CONFIGURATION NUMBER	INSTALL AT X+6		DELETE JUMPER	ADD JUMPER	FINAL JUMPER CONFIGURATION	X+6 PINS
	DRIVERS	TERM.				
11	A4	A3	30-31 36-37 40-41 32-33 42-43 46-47 48-49 50-51	29-30 37-48 43-50 33-36 32-47 40-49	29-30 38-39 43-50 37-48 44-45 34-35 32-47 33-36 40-49	C_0 (PIOB1) C_4 (J1-26) C_1 (J1-22) C_5 (J1-18) C_2 (J1-32) C_6 (J1-30) C_3 (PIOA1) C_7 (J1-28)
12	A4	A3	30-31 36-37 40-41 34-35 42-43 32-33 46-47 48-49 50-51	29-30 37-48 43-50 35-46 32-47 33-42 40-49	29-30 38-39 43-50 37-48 44-45 35-46 32-47 33-42 40-49	C_0 (PIOB1) C_4 (J1-26) C_1 (J1-22) C_5 (J1-18) C_2 (J1-32) C_6 (J1-20) C_3 (PIOA1) C_7 (J1-24)
13	A4	A3	40-41 32-33 42-43 46-47 48-49 50-51	43-50 33-48 32-47 40-49	30-31 38-39 43-50 36-37 44-45 34-35 32-47 33-48 40-49	C_0 (PIOB1) C_4 (J1-26) C_1 (J1-22) C_5 (J1-28) C_2 (J1-32) C_6 (J1-30) C_3 (PIOA1) C_7 (J1-18)
14	A4	A3	40-41 38-39 42-43 36-37 46-47 32-33 48-49 50-51	43-50 39-46 32-47 37-42 40-49 33-48	30-31 39-46 43-50 37-42 44-45 34-35 32-47 33-48 40-49	C_0 (PIOB1) C_4 (J1-20) C_1 (J1-22) C_5 (J1-24) C_2 (J1-32) C_6 (J1-30) C_3 (PIOA1) C_7 (J1-18)
15	A4	A3	30-31 36-37 40-41 32-33 42-43 44-45 46-47 50-51	36-45 37-42 32-47 30-35 40-49 33-48	36-45 38-39 32-47 37-42 40-49 34-35 30-35 33-48	C_0 OPEN C_4 (J1-26) C_1 (J1-28) C_5 (J1-24) C_2 (J1-32) C_6 (J1-30) C_3 (PIOA1) C_7 (J1-18)
16	A4	A3	30-31 36-37 40-41 32-33 42-43 48-49 50-51	40-49 37-42 30-35 33-48	44-45 38-39 46-47 37-42 40-49 34-35 30-35 33-48	C_0 OPEN C_4 (J1-26) C_1 (J1-22) C_5 (J1-24) C_2 (J1-20) C_6 (J1-30) C_3 (PIOA1) C_7 (J1-18)
17	A4	A3	30-31 36-37 40-41 32-33 42-43 46-47 48-49 50-51	43-50 37-42 32-47 33-48 40-49	43-50 38-39 44-45 37-42 32-47 34-35 40-49 30-35 33-48	C_0 (PIOB1) C_4 (J1-26) C_1 (J1-22) C_5 (J1-24) C_2 (J1-32) C_6 (J1-30) C_3 (PIOA1) C_7 (J1-18)

Changing the jumper at W18 from A-B to B-C, supplies +5V to J2-50 for use by the user.

CAUTION

If J1-50 and J2-50 have +5V enabled, ensure that connectors J1 and J2 are properly installed. If installed backwards, damage may result.

The -5V Aux to the RAMs can be supplied from the Multibus interface (P1 pins 9 and 10) or it can be supplied by the -12V from the Multibus interface (P1 pins 79 and 80) via VR1 when Auxiliary power is not used. To supply the -5V Aux from the Multibus interface, remove the jumper from pins B-C at W5 and add a jumper from pins B-A at W5. To supply the -5V Aux from the -12V input, place the jumper from pins B-C at W5 (this is the factory default wiring).

2-32. COMPONENT INSTALLATION

The iSBC 108A/116A boards require certain user-furnished and installed devices appropriate to the user's desired configuration. The following paragraphs detail specifications and instructions for installation of these devices.

2-33. ROM/PROM

Four sockets are provided for user installation of ROM or PROM memory devices. At the users discretion, 1K byte devices, such as the Intel 2708, 2758 PROMs, 2k byte devices, such as the Intel 2716 PROM, 4k byte devices, such as the Intel 2732 PROM, of 8k byte devices, such as the Intel 2364 ROM may be installed. Certain modifications necessary for installation of the PROMs or ROMs are described in paragraph 2-12. Only one type of ROM or PROM may be installed.

2-34. LINE DRIVERS/TERMINATORS

Eight sockets are provided for user-supplied and installed line driver/terminator networks apropriate to the user's application. These sockets correspond to the parallel I/O ports X+5, X+6, X+9, and X+A.

If the port is to be an input port, the proper termination package should be installed. Figures 5-3 and 5-4 illustrate two packages used for this purpose, the iSBC 902 pull-up network and the iSBC 901 terminator package. If the port is to be an output port, the proper line driver should be chosen from table 2-21.

Four sockets are provided with Intel 8226 bidirectional bus drivers installed. The user may want to replace these with user supplied non-inverting Intel 8216 bidirectional bus drivers.

2-35. RISE TIME/NOISE CAPACITORS

Eye pads are provided so that rise time/noise control capacitors may be installed as required on the individual serial I/O drivers. The selection of capacitor values is at the option of the user and is normally a function of the particular environment. The location of these eye pads are as follows:

Capacitor	Fig. 5-1	Fig. 5-2
C10	ZD3	6ZD6
C13	ZD3	6ZC4
C14	ZC3	6ZC4
C15	ZD2	6ZC4
C16	ZC2	6ZC4

Table 2-20. Parallel I/O Line Drivers

Driver	Characteristic	Sink Current (ma)
7438	I, OC	48
7437	I	48
7432	NI	16
7426	I, OC	16
7409	NI, OC	16
7408	I, OC	16
7403	I, OC	16
7400	I	16

NOTE:
I — Inverting; NI — Not Inverting; OC — Open Collector

2-36. SERIAL I/O PORT CABLING

The serial I/O interface uses a 26-pin double-sided PC edge connector (J3) to connect with external I/O devices via a flat cable. Suitable edge connectors are listed in table 1-1.

2-37. PARALLEL I/O PORT CABLING

The six parallel I/O ports use two 50-pin double-sided PC edge connectors (J1 and J2) to connect with external I/O devices via a flat cable. Suitable cable connectors are listed in table 1-1.

2-38. BOARD INSTALLATION

CAUTION

Always turn off the computer power (and battery backup power, if used) before installing or removing the iSBC 108A/116A board. Failure to observe this precaution may result in damage to the board.

In an iSBC 80/86 Single Board Computer based system, install the board in any slot that has not been wired for a dedicated function. In an Intellec system, install the board in any slot except slots 1 and 2. Ensure that the auxiliary connector P2 (if used) mates with the user-installed mating connector.

CHAPTER 3
PROGRAMMING INFORMATION

3-1. INTRODUCTION

The iSBC 108A/116A modules include the following programmable devices:

a. Two Intel 8255A PPI (Programmable Peripheral Interface) devices that control six parallel I/O ports.

b. One Intel 8251A USART (Universal Synchronous/Asynchronous Receiver/Transmitter) device that controls a serial I/O port.

3-2. I/O BASE ADDRESS

The bus master communicates with the 8215A USART and the 8255A PPIs through I/O Read and I/O Write Commands. The I/O addresses used for these commands are relative to an 8-bit base address (x) (12-bit base address (xx) in an 8086-based system) that is a multiple of 10H. The I/O base address is configured at the factory to 0D0; however, this address may be reconfigured as detailed in paragraph 2-19.

3-3. I/O ADDRESS ASSIGNMENT

Sixteen I/O addresses are used by the iSBC 108A/116A boards. Eight are associated with the 8255A PPI devices, four are associated with the 8251A USART devices, four are associated with the Interrupt Mask Register, the Interrupt Status Register and the Interval Timer. Table 3-1 lists these I/O addresses.

3-4. 8251A USART PROGRAMMING

The serial I/O port is controlled by an Intel 8251A USART device. The USART converts parallel output data into virtually any serial output data format (including IBM Bi-Sync) for half- or full-duplex operation. The USART also converts serial input data into parallel data format.

Prior to starting data transmission or receiving data, the USART must be loaded with a set of control words. These control words, which define the complete functional operation of the USART, must immediately follow a reset (internal or external) operation. A control word is either a Mode instruction or a Command instruction. Since these words structure the USART's internal logic, all programming must be completed before data transactions are initiated.

3-5. MODE INSTRUCTION FORMAT

The Mode instruction word defines the general characteristics of the USART and must follow a reset operation (internal or external). Once the Mode instruction has been written into the USART, sync

Table 3-1. I/O Address Assignment

Function	Base*+Displacement		READ/WRITE
Interrupt Status Register	XX	0	R
Interrupt Mask Register	XX	1	R/W
Reset Timer Interrupt	XX	2	W
Reset Timer, Initialize Mask	XX	3	W
Parallel I/O Port	XX	4	R/W
Parallel I/O Port	XX	5	R/W
Parallel I/O Port	XX	6	R/W
A21 PPI Device Control	XX	7	W
Parallel I/O Port	XX	8	R/W
Parallel I/O Port	XX	9	R/W
Parallel I/O Port	XX	A	R/W
A22 PPI Device Control	XX	B	W
USART Data Port	XX	C or E	R/W
USART Control Port	XX	D or F	R/W

*These hexadecimal digits are selected by jumper wiring; refer to paragraph 2-19 for further details.

characters or Command instructions may be inserted. The Mode instruction word defines the following:

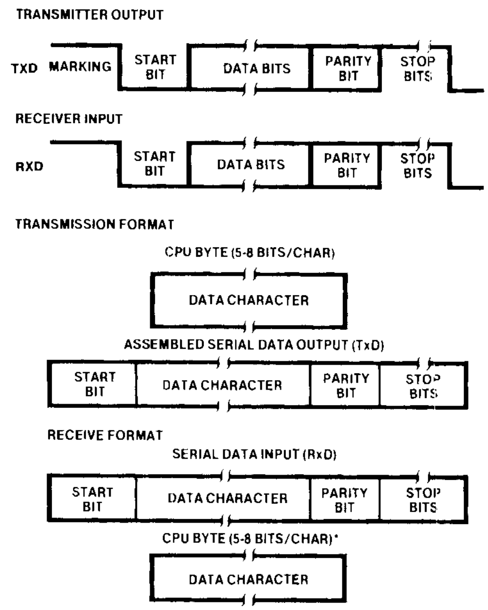
a. For the Synchronous Mode:
   (1) Character Length
   (2) Parity enable
   (3) Even/odd parity generation and check
   (4) External sync detect
   (5) Single or double character synchronization.

b. For the Asynchronous Mode
   (1) Baud rate factor (X/1, X/16, X/64)
   (2) Character length
   (3) Parity enable
   (4) Even/odd parity generation and check
   (5) Number of stop bits

Instruction word and data transmission formats for synchronous and asynchronous modes are shown in figures 3-1 through 3-4.

3-6. SYNCHRONIZATION CHARACTERS

Synchronization characters are written to the USART in the Synchronous Mode only. The USART can be programmed for either one or two synchronization characters; the format of the synchronization characters is at the option of the programmer.



*Note: If character length is defined as 5, 6, or 7 bits, the unused bits are set to "zero".

Figure 3-2. Asynchronous Mode Protocol

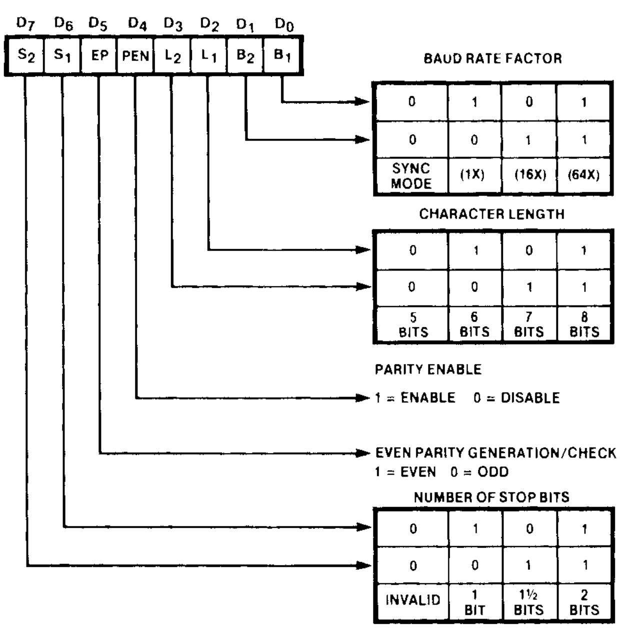


Figure 3-1. Mode Instruction Format, Asynchronous Mode

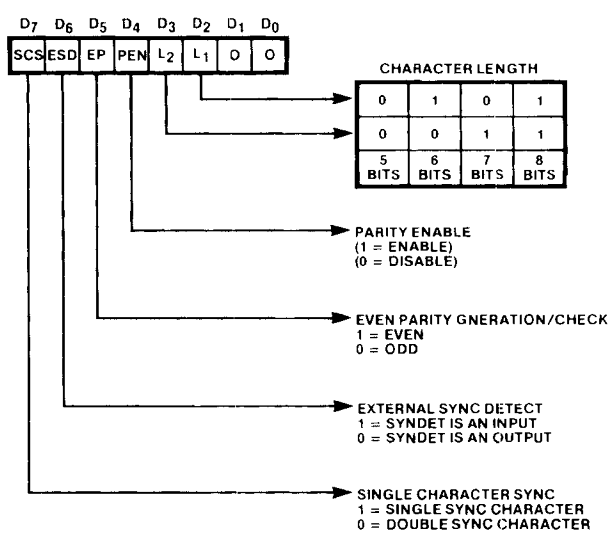


Figure 3-3. Mode Instruction Format, Synchronous Mode

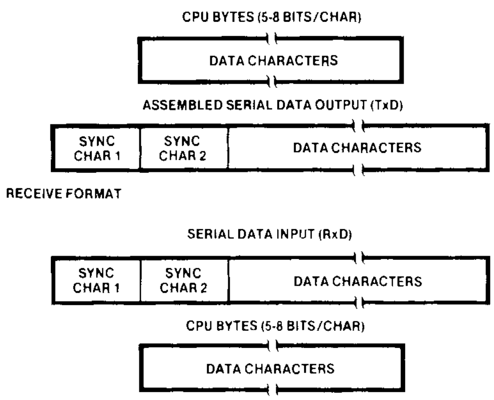


Figure 3-4. Synchronous Mode Protocol

3-7. COMMAND INSTRUCTION FORMAT

The Command instruction word, shown in figure 3-5, controls the operation of the USART. A Command instruction must follow the MODE and/or Synchronization words. Once the Command instruction is written, data may be transmitted or received by the USART.

It is not necessary for the Command instruction to precede all data transactions; only transmissions that require a change in operating format need this instruction. Refer to figure 3-5 for the Command Instruction Format. The Command instruction can be written to the USART at any time after the Mode Word has been written.

After initialization, always read the chip status and check for the TXRDY bit before writing data words to the USART. This ensures that any prior input is not over-written and lost.

3-8. RESET

To change the Mode instruction word, the USART must receive a reset command. The next word written to the USART after a reset command is assumed to be a Mode instruction. Similarly, for the synchronous mode, the next word after a Mode instruction is assumed to be one or more synchronization characters. All control words written into the USART after the Mode instruction (and/or the synchronization character) are assumed to be Command instructions.

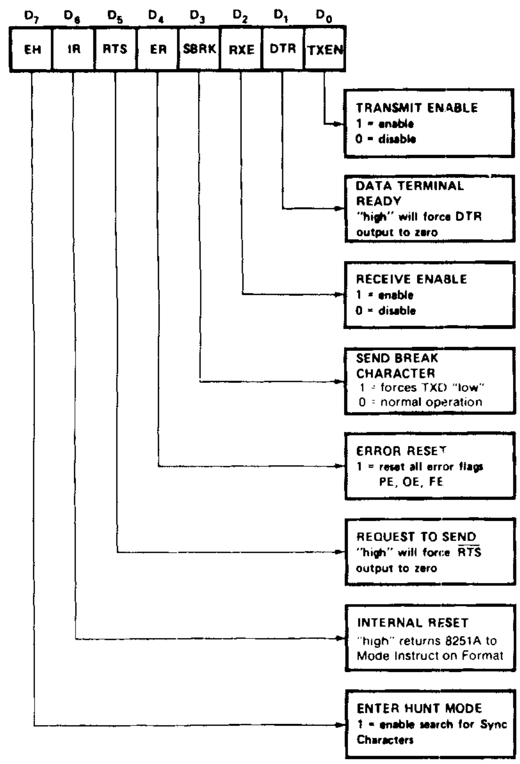


Figure 3-5. USART Command Instruction

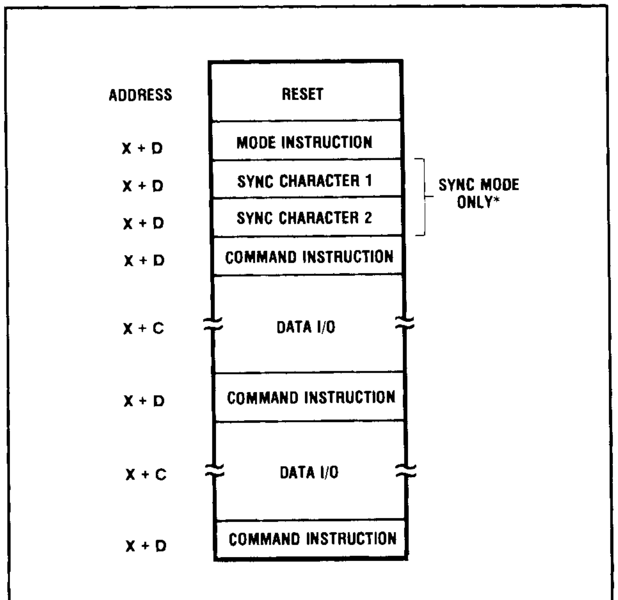
Note that the USART may be reset by bit 6 (IR) in the Command instruction, or by a high logic level at the RESET pin (system reset).

3-9. ADDRESSING

The USART is accessed by the programmer as two I/O ports. The first port is defined as X+C or X+E and is used to read or write data to or from the USART. The other port, X+D or X+F, is used to write Mode instructions, Command instructions, and Synchronization characters to the USART, or to read status. The I/O base address, X, is jumper-defined. Refer to paragraph 2-19 for details of I/O base address assignment, and to table 3-1 for I/O address assignment.

3-10. INITIALIZATION

A typical USART initialization and I/O data transaction sequence is illustrated in figure 3-6. The USART is initialized with the following steps:



*The second sync character is skipped if Mode instruction has programmed USART to single character internal sync mode. Both sync characters are skipped if Mode instruction has programmed USART to async mode.

Figure 3-6. Typical USART Initialization and Data I/O Sequence

a. Reset the USART. This may be done by bringing the RESET pin to a high logic level or by writing a Command instruction with bit 6 set (IR = 1) to port X+D or X+F.

b. Write a Mode instruction appropriate to the desired serial data transaction protocol. Refer to figures 3-1 and 3-3 for effects of setting/resetting particular bits.

c. If Synchronous operation has been specified, the USART will expect one or two Synchronization words immediately following the Mode instruction.

d. Write an appropriate Command instruction, setting or resetting selected bits according to the details illustrated in figure 3-5.

e. Begin data transaction.

3-11. OPERATION

Normal operating procedures use data I/O read and write, status read, and Mode and Command instruction write operations. Programming and addressing procedures for these functions are summarized in the following paragraphs.

Note that after the USART has been initialized, the status of the TXRDY bit must be checked *before* writing data to the USART. The TXRDY bit *must* be *true* to prevent overwriting and subsequent loss of data words. The TXRDY bit is inactive until initialization has been completed; do not check until after the Command word has been written. This concludes the initialization procedure.

Prior to any change in operating formats, a new Command word must be written to the USART, with Command bits set or reset as appropriate to the new format.

3-12. DATA INPUT/OUTPUT. For data receive or transmit operations perform a read or write operation, respectively. Figure 3-6 shows the typical sequence of instruction words, synchronization characters, and data words used—in data I/O operations.

During normal transmit operations, the USART generates a Transmit Ready (TXRDY) signal that indicates that the USART is ready to accept a data character for transmission. TXRDY is automatically reset when a character is loaded into the USART from the bus master.

Similarly, during a normal receive operation, the USART generates a Receive Ready (RXRDY) signal, which indicates that a character has been received and is ready for input to the main processor. RXRDY is automatically reset when a character is read by the bus master.

Note that while the receiver runs continuously, RXRDY will be asserted only when the RXE (Receiver Enable) bit is set in the preceding Command instruction. The TXRDY (Transmitter Ready) signal is asserted only when CTS/ is low, the Data buffer is empty, and the TXE (Transmit Enable) bit has been set in the preceding Command instruction.

3-13. STATUS READ. The bus master can determine the status of a serial I/O port by issuing an I/O Read Command to the upper address (X+D or X+F). The format of the Status Word is shown in figure 3-7. Before data transactions are initiated, the TXRDY bit should be examined.

3-14. 8255A PPI PROGRAMMING

The iSBC 108A/116A modules provide six parallel 8-bit I/O ports controlled by two Intel 8255A Programmable Peripheral Interfaces. These ports, addressed as Ports X+4, X+5, X+6, X+8, X+9, and X+A, are configured into different operating modes by a program Control word. The following paragraphs

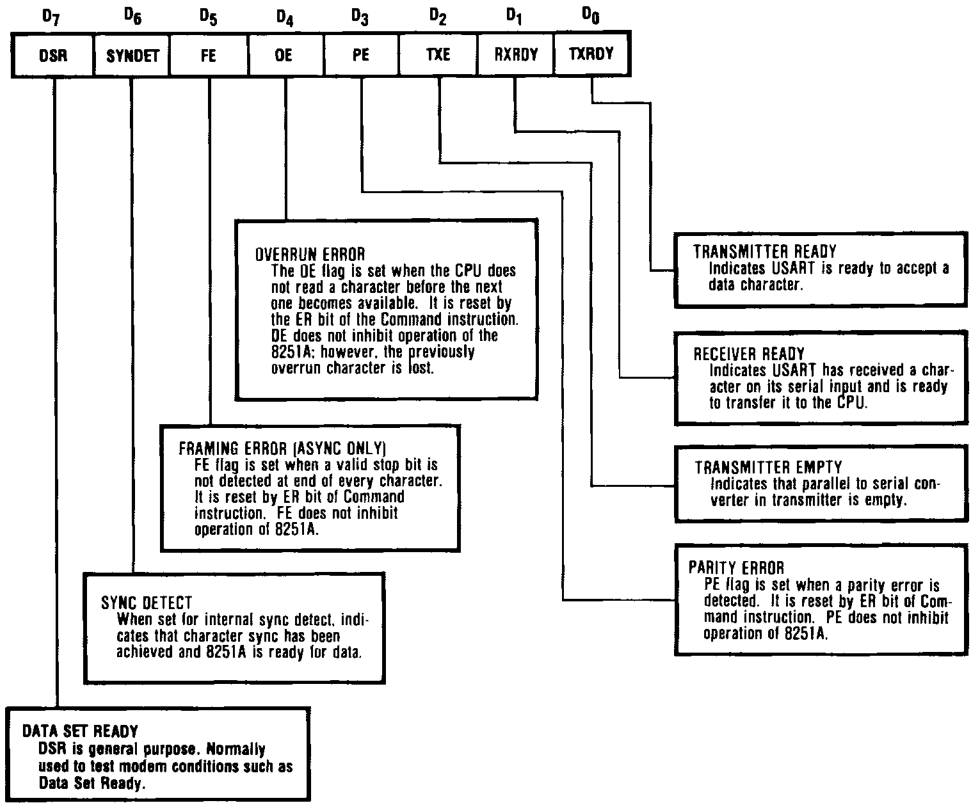


Figure 3-7. USART Status Read Format

describe the programming and operation of the 8255A PPI devices.

3-15. CONTROL WORD

The 8255A PPI devices are programmed with a Control word written into address X+7 or X+B. The bits of this word configure the three ports on each device for various types of input and/or output operation. The bit significance of the Control word is illustrated in figure 3-8.

3-16. MODE SELECTION

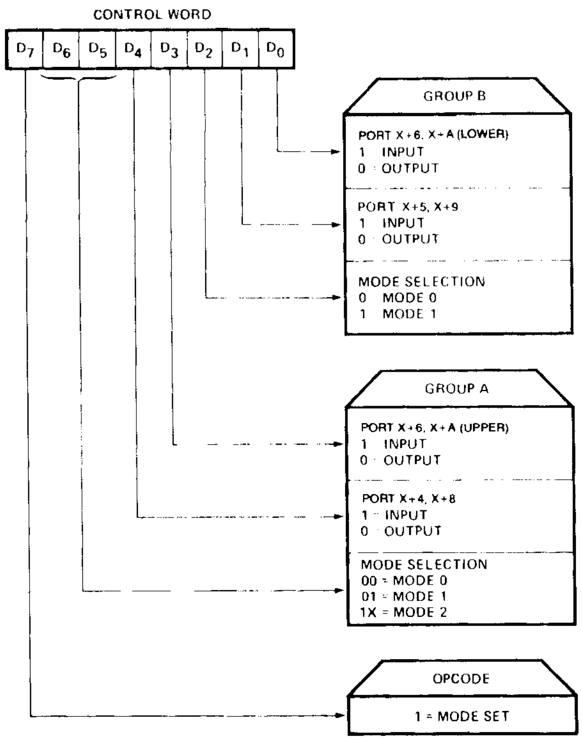
As detailed in table 3-2 and figure 3-9, there are three modes of operation for the 8255A ports:

a. Basic Input/Output
b. Strobed Input/Output
c. Bi-Directional Input/Output

The modes for Ports X+4 and X+5, and for Ports X+8 and X+9 may be separately defined, while Ports X+6 and X+A are configured to conform to Ports X+4, X+5, and Ports X+8, X+9 definitions, respectively. Figure 3-9 illustrates the port configuration in all three modes. Table 3-3 gives the definition for each pin of the three 8-bit ports in all three modes. By making reference to these, and to table 3-2, the programmer can choose the appropriate port configuration.

3-17. ADDRESSING

The ports of the two 8255A devices are addressed as Ports X+4, X+5, and X+6, and as X+8, X+9, and X+A. The I/O base address 'X' is jumper selectable. Refer to paragraph 2-19 for details of I/O base address selection. Address bits AB1 and AB0 are internally decoded to select individual ports within the 8255A. Two Chip Select signals, SPO1/ and SPO2/, specify device A21 or A22 respectively. Table 3-4 summarizes 8255A basic operation and addressing. Addresses of the Control Word Registers for devices A21 and A22 are X+7 and X+B, respectively.



277-12

Figure 3-8. 8255A Control Word Format

3-18. INITIALIZATION

When the RESET input goes to a high logic level, all ports on A21 or A22 will be configured in the Input mode. Once the RESET signal is removed, the Input mode may be used without further programming. If another port configuration is desired, a Control word may be written to the 8255A at any time.

3-19. OPERATION

When configured for Mode 0 operation, all three ports on each 8255A are available as simple 8-bit I/O ports. In Modes 1 and 2, signals to or from Port X+6 or X+A are used as parallel I/O protocol signals. Input or Output operation is specified by the Control Word. Table 3-4 lists bits set/reset during Read, Write, and Control operations.

In Mode 1 Input mode, Ports X+4 or X+8 and Port X+5 or X+9 are used as 8-bit I/O ports and Port X+6 or X+A bits are used as flag bits for these ports. PC4 and PC2 are used to strobe data into ports X+4 or X+8, or ports X+5 or X+9, respectively. Once data is latched into X+4 or X+8, PC5 is activated. PC1 is activated when data is latched into X+5 or X+9. Refer to table 3-3 for further details.

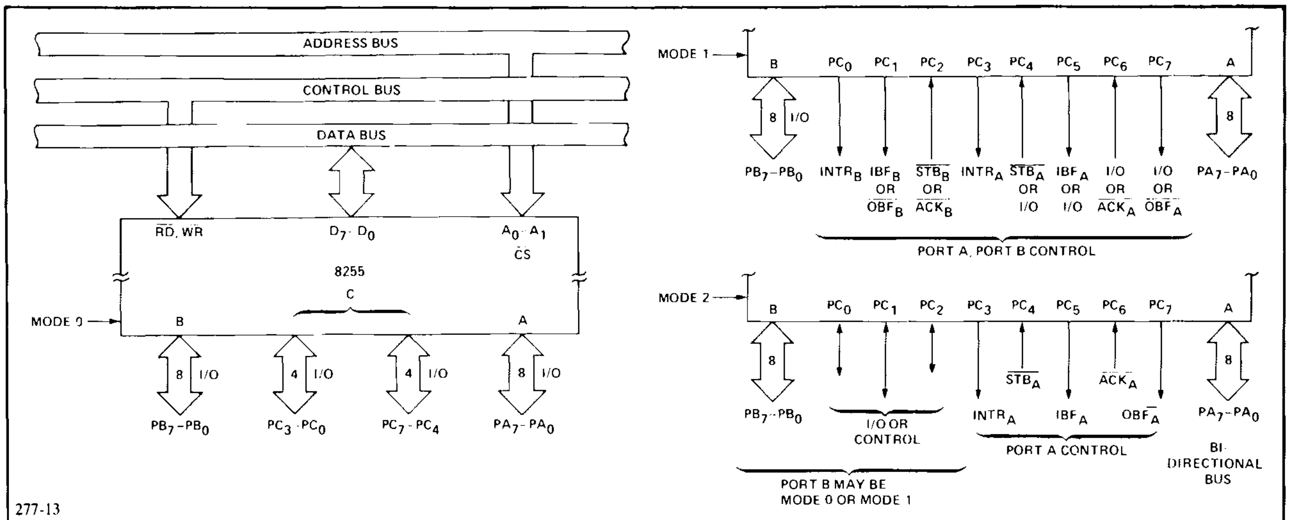
Table 3-2. 8255A Operational Modes

Mode 0 — Basic Input/Output
Two 8-bit ports Two 4-bit ports with bit set/reset capability Outputs are latched Inputs are not latched
Mode 1 — Strobed Input/Output
One or two strobed ports Each Mode 1 port contains: 8-bit data port 3 control lines Interrupt support logic Any port may be input or output If one Mode 1 port is used, the remaining 13 lines may be configured in Mode 0. If two Mode 1 ports are used, the remaining 2 bits may be input or output with bit set/reset capability.
Mode 2 — Strobed Bidirectional Bus
One bidirectional bus which contains: 8-bit bidirectional bus supported by Port A 5 control lines Interrupt support logic Inputs and outputs are latched The remaining 11 lines may be configured in either Mode 0 or Mode 1.

If data has been latched in and is available to read, an interrupt bit is set. Bit PC3 generates an interrupt for Port X+4 or X+8; bit PC0 generates an interrupt for Port X+5 or X+9.

In the Mode 1 Output mode, bits PC1 and/or PC7 specify that the bus master has written data to be transmitted to the I/O ports X+5 or X+9, and X+4 or X+8, respectively. The peripheral device acknowledged reception by resetting bits PC2 and/or PC6. Following this acknowledgement, interrupts are generated at bits PC0 and/or PC3 to alert the bus master that new data may be written.

In Mode 2, Bi-Directional Input-Output, only Port X+4 or X+8 is involved in data transactions. PC5 indicates that data has been received from the peripheral device. PC7 indicates that the output buffer has new data for the peripheral device. When PC6 goes active (low), data is transmitted. When PC4 is active (low), data is loaded into the input buffer. PC3 is activated as an interrupt to alert the bus master that data has been received or sent.



NOTE:
Port A = Ports X+4 and X+8 Port B = Ports X+5 and X+9 Port C = Ports X+6 and X+A

Figure 3-9. Mode/Register Format

Table 3-3. Mode Definition Summary Table

	MODE 0		MODE 1		MODE 2
	IN	OUT	IN	OUT	GROUP A ONLY
PA_0	IN	OUT	IN	OUT	Bidirectional
PA_1	IN	OUT	IN	OUT	Bidirectional
PA_2	IN	OUT	IN	OUT	Bidirectional
PA_3	IN	OUT	IN	OUT	Bidirectional
PA_4	IN	OUT	IN	OUT	Bidirectional
PA_5	IN	OUT	IN	OUT	Bidirectional
PA_6	IN	OUT	IN	OUT	Bidirectional
PA_7	IN	OUT	IN	OUT	Bidirectional
PB_0	IN	OUT	IN	OUT	MODE 0 OR MODE 1 ONLY
PB_1	IN	OUT	IN	OUT	
PB_2	IN	OUT	IN	OUT	
PB_3	IN	OUT	IN	OUT	
PB_4	IN	OUT	IN	OUT	
PB_5	IN	OUT	IN	OUT	
PB_6	IN	OUT	IN	OUT	
PB_7	IN	OUT	IN	OUT	
PC_0	IN	OUT	$INTR_B$	$INTR_B$	I/O
PC_1	IN	OUT	IBF_B	OBF_B	I/O
PC_2	IN	OUT	STB_B	ACK_B	I/O
PC_3	IN	OUT	$INTR_A$	$INTR_A$	$INTR_A$
PC_4	IN	OUT	STB_A	I/O	STB_A
PC_5	IN	OUT	IBF_A	I/O	IBF_A
PC_6	IN	OUT	I/O	ACK_A	ACK_A
PC_7	IN	OUT	I/O	OBF_A	OBF_A

NOTE:

Bits PA_{0-7}= Port X+4 or X+8
Bits PB_{0-7}= Port X+5 or X+9
Bits PC_{0-7}= Port X+6 or X+A

Table 3-4. Basic 8255A Operation

Input Operation (Read)		Port Select		Read/Write		Chip Select
From	To	A0	A1	RD/	WR/	CS/
Port X+4 X+8	Data Bus	0	0	0	1	0
Port X+5 X+9	Data Bus	1	0	0	1	0
Port X+6 X+A	Data Bus	0	1	0	1	0
Output Operation (Write)						
From	To					
Data Bus	Port X+4 X+8	0	0	1	0	0
Data Bus	Port X+5 X+9	1	0	1	0	0
Data Bus	Port X+6 X+A	0	1	1	0	0
Data Bus	Control X+7 X+B	1	1	1	0	0
Disable Function						
Chip Deselected		X	X	X	X	1
Illegal Condition		1	1	0	1	0

3-20. PORT X+6 AND X+A BIT SET/RESET

Any of the eight bits of Port X+6 or X+A can be Set or Reset using a single Control Word. This Control Word, illustrated in figure 3-10, may be written to the 8255A at any time, and will Set/Reset bits whether the port is used for status flags or I/O transactions.

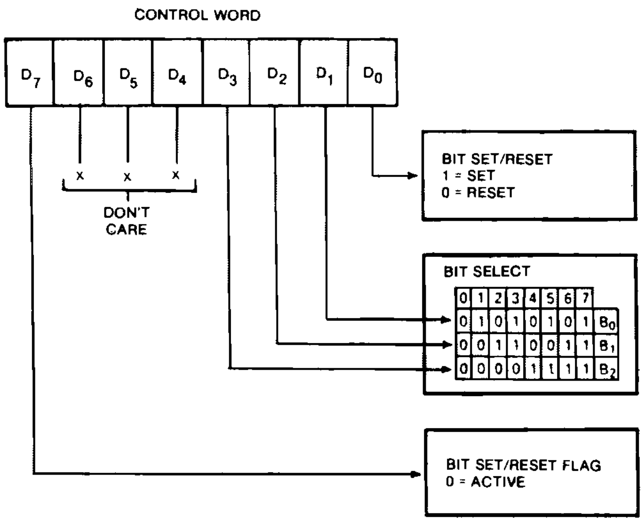
3-21. STATUS READ. In Modes 1 and 2, the data lines of Port X+A and X+6 reflect certain conditions and signal states, according to the details given in figure 3-11. The set or reset condition of these bits may be noted by a simple read of Port X+6 or X+A, and by analyzing these bits in conjunction with the signals sent to the 8255A PPI device. Data transmission protocols may be maintained or changed as desired.

3-22. INTERRUPT STATUS MASK

When an 8-bit word is written to the I/O address X+1, the Interrupt Mask Register, the word is latched into the register and is ANDed with interrupt signals from eight sources to produce system interrupt signals INT0/-INT7/. Any bit set in the Interrupt Mask Word enables system interrupts for that interrupt request line. A correlation of data bits and interrupt requests is provided in Figure 3-12.

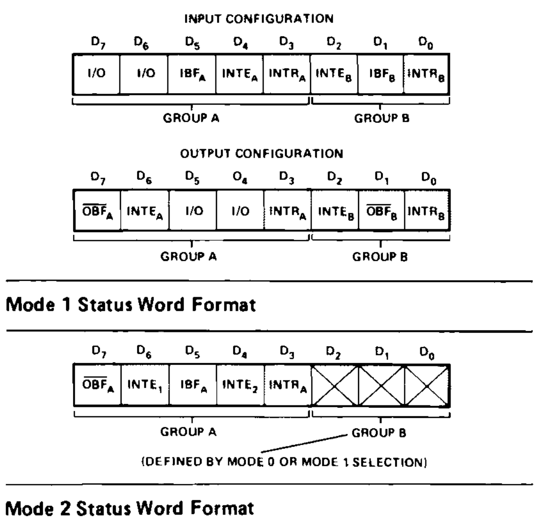
The interrupt mask itself may be read by an I/O read (IOR/ active) to I/O address X+1. When reading this address, note that the multiplexors that propagate the mask invert it. The masked status can be read from the mask gates, and this is done by a read to I/O address X+0.

The Interval Timer provides an interrupt pulse every millisecond. It may be reset by doing an I/O write to location X+2 (the data written is unimportant). When I/O address X+3 is specified, a write will reset the Interval Timer and load the Interrupt Mask Register.



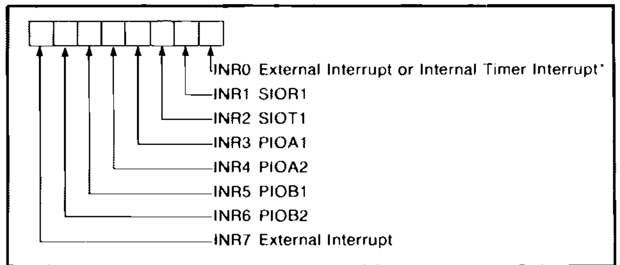
277-14

Figure 3-10.
Ports X+6 and X+A Bit Set/Reset Control Word



277-15

Figure 3-11. 8255A Status Read Format



*[1]This option is jumper-selectable as follows: jumper connection 26-27 for External Interrupt, 28-27 for Internal Timer Interrupt.

277-17

Figure 3-12. Interrupt Mask Word Format

CHAPTER 4
PRINCIPLES OF OPERATION

4-1. INTRODUCTION

This chapter provides a functional description and a circuit analysis of the iSBC 108A/116A Combination Memory and I/O Expansion Boards. Figure 4-1 is a simplified functional block diagram that illustrates the interaction of the functional blocks.

4-2. FUNCTIONAL DESCRIPTION

A brief description of the functional blocks comprising the iSBC 108A/116A boards are given in the following paragraphs. A detailed circuit analysis is given beginning with paragraph 4-10.

4-3. ROM/PROM MEMORY

IC sockets A34, A46, A60, and A76 are provided for user installation of ROM/PROM chips. Jumpers are provided to accommodate up to 16K of PROM or up to 32K of ROM.

4-4. RAM MEMORY

The RAM memory is contained in device locations A59, A61-63, and A71-74. 8K or 16K of RAM memory is supplied on the iSBC 108A/116A boards respectively. Control of the RAM memory is implemented with an Intel 8202 Dynamic RAM controller. The RAM base address and boundary are established with jumpers and switches.

4-5. PROGRAMMABLE PERIPHERAL INTERFACE

The 8255A Programmable Peripheral Interface (PPI) is a general purpose programmable I/O component that interfaces peripheral equipment to the system bus. The iSBC 108A/116A modules include two 8255A PPI's. Each PPI controls three 8-bit ports and develops two interrupt requests.

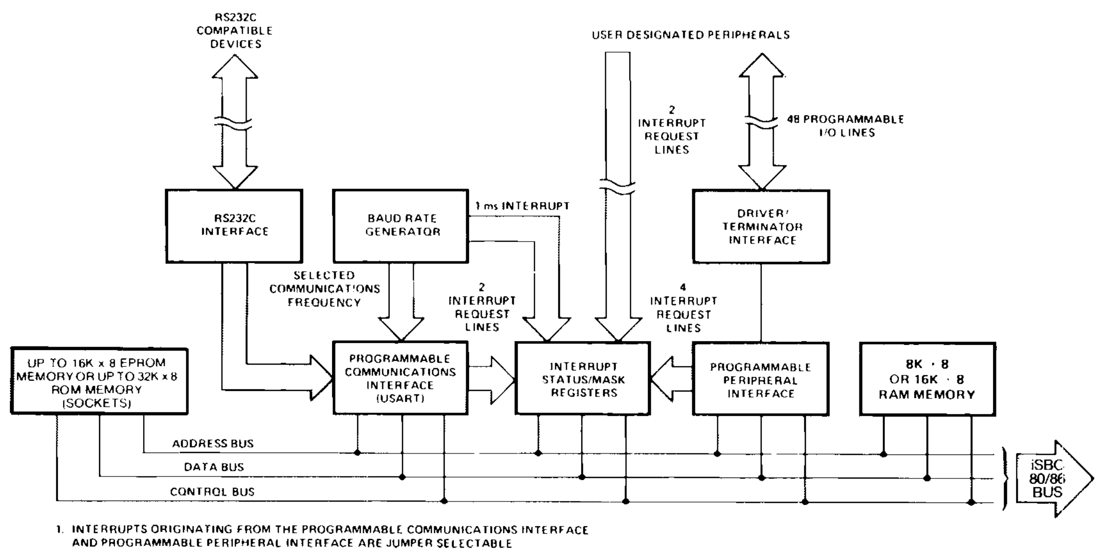


Figure 4-1. iSBC 108A/116A™ Board Functional Block Diagram

4-6. DRIVER/TERMINATOR INTERFACE

Four Intel 8226 Bidirectional Bus Drivers are supplied in sockets. Eight additional sockets are provided for user supplied and installed line driver/terminator networks appropriate to the user's application. When data enters or leaves the six parallel I/O ports, it passes through the line driver/terminators.

4-7. PROGRAMMABLE COMMUNICATIONS INTERFACE

The 8215A Universal Synchronous/Asynchronous Receiver/Transmitter (USART) provides serial I/O. The RS232 interface can be configured (by jumper wiring) as a Data Set or a Data Terminal. Synchronous or Asynchronous mode, character length, number of stop bits, even or odd parity, and baud rates are all programmable. In the Synchronous Mode either internal or external synchronization can be selected. However, the iSBC 108A/116A boards do not support external sync. The USART develops two interrupts (SIOT1 and SIOR1).

4-8. BAUD RATE GENERATOR

The Baud Rate Generator provides jumper selectable baud rates to the USART. In the Asynchronous Mode, the jumper selected baud rate can be divided by 1, 16, or 64 by software control. In addition, the Baud Rate Generator supplies the timing pulses for the 1 ms interval timer.

4-9. INTERRUPT STATUS/MASK REGISTERS

The Mask Register stores the bit pattern for masking the interrupts. A logic "one" programmed into a Mask Register bit enables that interrupt source.

The Mask Register and the Interrupt Status Register can be read under program control. The results of reading the Mask Register are inverted from the mask that was written to the Mask Register.

4-10. CIRCUIT ANALYSIS

The schematic diagram for the iSBC 108A/116A boards is given in figure 5-2. The schematic diagram consists of nine sheets, each of which includes grid coordinates. Signals that transverse from one sheet to another are assigned grid coordinates at both the signal source and signal destination. For example, the grid coordinates 2ZB1 locate a signal source (or signal destination as the case may be) on sheet 2 zone B1.

Both active-high and active-low signals are used. A signal mnemonic that ends with a virgule (e.g., DAT7/) denotes that the signal is active low ($\leq$ 0.4V). Conversely, a signal mnemonic without a virgule (e.g., ALE) denotes that the signal is active high ($\geq$ 2.0V).

4-11. MULTIBUS INTERFACE CIRCUITS

The major functions of the bus interface are shown in figure 5-2 sheet 2. The data input lines DAT0/ through DAT7/, from the Multibus interface, are buffered and inverted by transceiver A70 (Intel 8287 device). The outputs of the transceiver go to the internal data bus. The direction of the data transfer is controlled by the "T" input. When T is at a high level, A0-A7 are inputs and B0-B7 are the outputs. When T is at a low level, B0-B7 are inputs and A0-A7 are the outputs. The "CS" input, when low, enables the transceiver.

The address lines ADR0/ through ADRF/ are buffered and inverted by Input Buffers A68 and A69. These signals are applied to the internal address bus as address bits AB0 through ABF. Address bit lines ADR10/ through ADR13/ are buffered by A66. These signals are decoded and used to select the page address of the RAM and ROM/PROM.

The following system control signals are buffered by IC's A65 and A66:

a. RESET is generated by inverting INIT/ at A65 -7; RESET is inverted at A65-14 to obtain RESET/.
b. IOW/ is generated by buffering IOWC/ at A66 -14.
c. MRD/ is generated by buffering MRDC/ at A66 -18.
d. MWR/ is generated by buffering MWTC/ at A66 -16.
e. INH2 is generated by inverting INH2/ at A65 -9.
f. IOR/ is generated by buffering IORC/ at A66 -3.

4-12. I/O ADDRESS DECODE

The I/O address decoder can be jumper wired for 8- or 12-bit I/O addressing. Address bits AB8, AB9, ABA, and ABB or ABB/ are decoded by A32 (sheet 3) and jumper pad S5 (sheet 3) to select the high order bits of the 12-bit I/O base address. The output from S5 enables decoder A31.

NOTE

When 8-bit I/O addressing is used, the enable to the decoder A31 is grounded by a jumper so that A31 is always enabled.

Address bits AB4, AB5, AB6, and AB7 or AB7/ are decoded by A31 and jumper pad S2 to produce IOSEL/.

IOSEL/ enables the I/O function decoder A36. IOSEL/ is also ANDed with IOR or IOW at A30-11 (sheet 2) to produce IOP SEL at A30 -6. IOP SEL enables the Acknowledge Generator A24 (sheet 6) and also develops the BSEL/ signal at A43-4. The BSEL/ signal enables the bus transceiver A70 (sheet 2) so that data can be written or read from the bus.

4-13. I/O FUNCTION DECODER

The IOSEL/ signal being active low, enables I/O Function Decoder A36 (sheet 3). Address lines AB2 and AB3 are decoded by A36 to define the function to be performed. Table 3-1 lists the I/O address assignments.

4-14. RAM ADDRESS DECODE

Address bits A10/, A11/, and A12/ are decoded by A47 (sheet 3) and jumper pad S6 (sheet 3). The output from S6 is ANDed with A13 or A13/ at AND gate A35-5 to select a 64k byte page in the 1-megabyte address space. Address bits ABC, ABD, ABE, and ABF or ABF/, and switch S3's outputs are decoded by A45 (sheet 3) to select a block of memory in a 64k byte memory space. The output from A45 is ANDed at A35-5 with the S6 output, address bit A13 or A13/, and INH1 to produce RAM CS. INH1 is used to block a RAM access from the Multibus interface.

RAM CS is ANDed at A20 -11 (sheet 2) with MRD to produce QMRD/. QMRD/ enables the output from the RAM output latch A57 (sheet 5). RAM CS is also ANDed at A40 -3 (sheet 5) with MEMORY PROTECT/, from connector P2, to enable the Dynamic RAM Controller chip A50.

4-15. PROM ADDRESS DECODE

Address bits A10/, A11/, and A12/ are decoded by A47 and jumper pad S7 (sheet 3). The output from S7 is ANDed with A13 or A13/ at AND gate A35-6 to select a 64k byte page in the 1-megabyte address space. Transformed address bits TAD1, TAD2, TAD3, TAD4, and switch S4's output are decoded by A56 to select a block of memory in a 64K memory space.

Signals TAD1-TAD3 normally connect, via W12, to address bits ABC-ABE, respectively. Signal TAD4 is normally connected to either ABF or ABF/ via W12, PAD 1, and jumper pins 92, 93, 94. This allows PROM address selection in 4K blocks.

When 2364 ROMs are installed, jumper block W12 is removed and W11 is installed. This connects TAD1 - TAD3 to address bits ABD-ABF, respectively, and grounds TAD4. This configuration allows PROM address selection in 8K blocks.

The output from A56 is ANDed at A35-6 with the S7 output, address bits A13 or A13/, and INH2 to produce PSEL. INH2 is used to block a PROM/ROM access from the Multibus interface.

PSEL is inverted at A44-10 (sheet 2) to produce INH1/, which is placed on the Multibus via open collector driver A54-6. INH1/ is inverted at A44-8 to produce INH1, which is used to block the RAM selection. PSEL is also ANDed with MRD at A30 -8 to produce PREQ/. PREQ/ enables the PROMs and the PROM output buffer A48 (sheet 4). PREQ also enables A30 -6 (sheet 2) to activate the acknowledge generator via IOP SEL. BSEL/ is asserted via A43-4 by IOP SEL.

4-16. ROM/PROM LOGIC

The signal, PREQ, enables decoder A36 (sheet 4) to select one of the four ROMs. The ROM data output buffer A48 is also enabled by PREQ/. The address bits used for decoding which ROM is to be selected depends upon the ROM size. Jumpers W11-W16 connect the proper address lines to decoder A36. Address lines AB0-ABC are routed through jumpers W11-W16 to the ROM sockets to select the location in the selected ROM to be read out and placed on the data bus.

Jumper 24-25 (sheet 4) is normally installed, forcing the output of A33 -8 low. This places the ROMs/PROMs in the active mode. When jumper 24-25 is removed, A33 -8 normally is high. This places the ROMs/PROMs in the standby power mode. When a PROM/ROM read takes place, PREQ/ becomes active which in turn forces A33-8 low. This low on A33 -8 places the ROMs/PROMs in the active mode until the read is complete.

4-17. CLOCK LOGIC

The on-board clock generator A58 (sheet 5) is an Intel

8224 device operating at 22.1184 MHz. The OSC output is used to clock the dynamic RAM controller A50 and shift register A24 (sheet 6). The Dynamic RAM Controller supplies the timing signals for RAM read/write operations and memory refresh. The shift register is used to develop the user selectable timing for the AACK/ and XACK/ signals.

The 22.1184 MHz signal is divided by 9 in A58 to produce the phase 2 TTL clock signal which is used to clock the Intel 8251A USART A23 (sheet 6). The phase 2 TTL clock signal is also divided by 2 by flip flop A39 (sheet 5) to produce the BDCLK (baud clock) signal. This BDCLK signal is applied to the baud rate generator circuits A27 and A28 (sheet 6) to develop the jumper selectable baud rates.

4-18. RAM CONTROLLER

The Dynamic RAM Controller A50 (sheet 5) provides for address decoding, multiplexing, and all the timing needed to refresh the RAMs.

OR gate A41-6 is used to block the WE (write enable) signal to the RAMs during an inhibited memory cycle. Note that INH1 must remain stable during the entire memory cycle to guarantee the integrity of the stored data.

Data latch A57, on the data output of the RAMs, is a transparent latch that is used to optimize the RAM data access time. This latch stores the data present at the output of the RAMs when XACK/ goes low.

An external MEMORY PROTECT/ signal from P2-20 is ANDed with RAM CS at A40-3 to prevent read/write operations when the MEMORY PROTECT/ signal is active.

4-19. BAUD RATE GENERATOR

The baud rate provided for the 8215A USART is generated from the BD CLK signal by two binary dividers A27 and A28 (sheet 6). The outputs from these binary dividers are applied to jumper pad S1. One of these outputs can be used to clock the 8251A USART (refer to paragraph 2-23 for jumper details).

The divide ratio of A27 can be modified from 16 to 11 by connecting jumper pins 1 and 2. This provides a frequency of 6.98 kHz at S1-9 in order to produce a baud rate of 110 (USART programmed for a divide ratio of 64).

Binary divider A26 develops an output signal every 1 millisecond. This 1 millisecond interval signal is used to clock interval timer latch A39-3 (sheet 9). Note that if the divide ratio of A27 is modified by jumpering pins 1 and 2, the divide ratio of A26 must also be modified to maintain a 1 millisecond period. This is done by connecting jumper pins 3 and 5.

4-20. ACKNOWLEDGE GENERATOR

The acknowledge timing generator A24 and the output flip flop A25 (sheet 6) are enabled by the IOP SEL signal. The IOP SEL signal is generated any time an I/O read or write command is sent and the selected I/O address is on the address bus, or the ROM/PROM is selected for a read.

The acknowledge timing generator A24 is clocked every 45 nanoseconds by the OSC signal from A49-11 (sheet 5). The outputs from the acknowledge timing generator are user selectable by jumper wiring (refer to paragraph 2-20 for further details). Note that the AACK and XACK signals for a RAM access are generated by A50 (sheet 5) and gated to the AACK/ and XACK/ signal lines through A38.

4-21. SERIAL I/O PORT

The serial I/O port on the iSBC 108A/116A boards is controlled by an Intel 8251A Universal Synchronous/Asychronous Receiver/Transmitter and its associated support logic (A23 sheet 6).

The logical operation of the 8251A USART is determined by its programming and by its jumper configuration. It may be programmed for virtually any serial data transmission protocol currently in use, including IBM Bi-Sync. Since the USART's internal logic is structured according to its programming, a set of control words must be sent out by the CPU to initialize the 8251A to support the desired communications format. These control words will program the desired baud rate, character length, number of stop bits, Synchronous or Asynchronous Modes, and even or odd parity. In the Synchronous Mode, options are also provided to select the sync characters.

Once programmed, the 8251A is ready to perform its data transactions. The TXR output is raised high to signal the CPU that the 8251A is ready to receive a character. The signal (TXR) is reset automatically when the bus master writes a character into the USART. Conversely, the RXR output is raised high to indicate that a complete character has been received from an external I/O device. RXR is reset automatically by the subsequent read from the bus master.

The 8251A cannot begin transmission until the TXEN (Transmitter Enable) bit is set in the Command Instruction and it has received a CTS (Clear to

Send) input. The TXD output will be held in the marking state upon RESET.

The RS232 interface logic may be connected for either Data Set or Data Terminal operation by rewiring the jumpers installed in W3. Refer to paragraph 2-25 for jumper details.

Note that programming and jumper wiring both affect the internal logic of the USART. Therefore, it is necessary that programming considerations and jumper considerations are compatible when planning a particular configuration.

The 8251A USART is provided with two interrupt lines, SIOR1 and SIOT1. In the factory-wired default configuration, these two interrupts are jumper-wired to the pins bearing RXR (Receiver Ready) and TXR (Transmitter Ready), respectively. Refer to paragraphs 2-21 and 2-24 for further details on serial I/O jumper configuration.

4-22. PARALLEL I/O PORTS

The six 8-bit parallel I/O ports (sheets 7 and 8) on the iSBC 108A/116A boards are controlled by two Intel 8255A Programmable Peripheral interface devices. Ports X+4 and X+8 may be programmed for input, output, or bidirectional data transactions; port X+5 and X+9 may be programmed for input or output operation; and ports X+6 and X+A may be programmed for use as input or output ports, or, alternately, as control/status signals. Refer to paragraph 3-14 for further details regarding 8255A PPI Programming.

The two 8255A devices are selected with two signals, SPO2/ to specify device A22, and SPO1/ to specify device A21. Address bits AB0 and AB1 are used, in conjunction with IOR/ and IOW/ and the chip select signal SPO1/ or SPO2/, to define the direction of data flow for read or write operations. These operations are described in table 3-2.

To initialize A21 or A22, RESET is brought high. This clears all internal registers, including the Control Register. The Control Register is initialized according to the considerations described in figure 3-8; however, all three ports will now be configured in the Input Mode, and if there are no other considerations, the correct port may be addressed and data transactions may take place.

If, however, other data protocols must be observed, the Control Word specifies whether or not inputs are latched (outputs are always latched) and defines the configuration of ports X+6 and X+A as control signal lines or I/O lines. Refer to figure 3-9 for details of the control signals present at ports X+A and X+6 in this configuration. These control signals and/or I/O lines are available to the programmer through a normal read of ports X+A and X+6.

Ports X+6 and X+A include jumper connections that allow user-selectable routing of signals. Refer to paragraph 2-27 for further details on user configurations of these jumpers, as well as the factory-wired default mode. Two jumper pins, 71 and 74, are dedicated to interrupt lines PIOA2 and PIOB2, respectively; two other pins, 40 and 50, are dedicated to interrupt lines PIOA1 and PIOB1, respectively. Refer to the following paragraph for further details.

4-23. INTERRUPT LOGIC

The interrupt logic consists of a mask register latch (A51, sheet 9), a set of interrupt mask AND gates (A52, A53), status/mask input multiplexers (A29, A42), a priority encoder (A64), a set of 9 open collector bus drivers (A54, A55), and an interval timer interrupt latch (A39-6).

There are four operations that involve the interrupt circuits:

a. Write mask status into the mask register
b. Read mask status
c. Read masked interrupt status
d. Reset interval timer interrupt latch (This operation is performed as a write)

In each operation, the interrupt select line SINT/ must be true (active low). This select line is generated by the I/O address decode logic in the interface.

The interval timer latch A39-6 is clocked set at 1 ms intervals. It must then be reset by a write to X+2, where X is the jumper-selected I/O base address. The active-low output of the interrupt mask gate is routed to these three locations:

a. It is supplied to the A inputs of the status/mask multiplexer, A29, A42. These masked interrupt bits can then be read by the bus master via the bidirectional data buffer at the interface. The interrupt status bits are inverted at the multiplexer so that they are active-high on the iSBC internal data bus.
b. The masked interrupt bits are ORed at A64. The output, system Interrupt Request INRQ/, is active when any one of the interrupt bits is true. INRQ/ is dedicated to jumper pin 103. The factory-wired default configuration is jumper 103-111.
c. The masked interrupt bits may be jumper wired to the P1 interrupt pins. This provides maximum freedom in priority handling configurations.

Note that the mask bits are inverted by the multiplexers A29 and A42. They are active-low on the system data bus.

The interrupt request ORing circuit (priority encoder A64) is disabled whenever the mask register is written into or whenever the internal timer is reset. These two conditions are represented by SINT/ and IOW/ both being active (low). This causes the low-to-high transition of the INRQ/ line needed by edge-triggered devices.

The system address assignments for each of these operations is given in table 4-1.

Table 4-1. Interrupt Logic Operations

Function	Address AB0, AB1	R/W Command
1. Write Interrupt Mask	1	IOW/
2. Read Mask (Inverted)	1	IOR/
3. Read Masked Status	0	IOR/
4. Reset Interval Timer	2*	IOW/

NOTE:
*The interval timer can also be reset at the same time the mask register is loaded by using 3.

When SINT/ and IOW/ are both low and AB0 is high, the contents of the data bus are written into the interrupt mask register A51. The output bits of A51, which always reflect the register's contents, are applied to the interrupt mask gates. Both the inputs and outputs of A51 are true when at a high logic level. A mask bit must be set to 1 to enable the corresponding interrupt status bit.

Eight interrupt lines are ANDed with the mask register outputs at gates A52 and A53. For those mask bits that are set, the corresponding interrupt path is enabled. Seven of the interrupt lines are controlled by fixed sources; two are from parallel I/O interface group 1 (PIO A1 and B1), two are from parallel I/O interface group 2 (PIO A2 and B2), two are from the serial I/O interface (SIOR1 and SIO1), and one is provided via J2-50 by a user-selected external source (external interrupt 2). The eighth interrupt can be supplied by another external source (via J1-50) or by the interval timer interrupt circuit. This choice is made by the user through jumper selection. The interval timer latch is selected by a jumper at pins 27-28, which is the default selection. The external source is specified as the source by a jumper at pins 26-27.

CHAPTER 5
SERVICE INFORMATION

5-1. INTRODUCTION

This chapter provides service diagrams and service repair assistance instructions for the iSBC 108A/116A boards.

5-2. SERVICE DIAGRAMS

The iSBC 108A/116A board parts location and schematic diagrams are given in figures 5-1 and 5-2, respectively. Each sheet of the schematic diagram is marked with grid coordinates. Signals that transverse from one sheet to another are assigned grid coordinates at both the signal source and destination. For example, the grid coordinates 2ZD8 locate a signal source or destination on sheet 2 in Zone D8.

Both active-high (positive-true) and active-low (ground-true) signals appear on the schematics. To avoid confusion as to the meaning of these signals, the following convention is used. The mnemonic for each active-low signal is terminated by a slash (e.g., A10/). Such references indicate that the signal level is low when the condition is true (active). A mnemonic without a slash (e.g., INH2) refers to an active-high signal. These references indicate that the signal level is high when the condition is true (active).

5-3. REPLACEABLE PARTS

Table 5-1 provides a list of user-replaceable parts for the iSBC 108A/116A boards. Table 5-2 indentifies and locates the manufacturers specified in the MFR CODE column in table 5-1. Intel parts that are available on the open market are listed in the MFR CODE column as "COML"; every effort should be made to obtain these parts from a local (commercial) distributor.

5-4. SERVICE AND REPAIR ASSISTANCE

United States customers can obtain service and repair assistance from Intel by contacting the MCD Technical Support Center in Santa Clara, California at one of the following numbers:

Telephone:

From Alaska or Hawaii Call—
(408) 987-8080

From locations within California call toll free—
(800) 672-3507

From all other U.S. locations call toll free—
(800) 538-8014

TWX: 910-338-0029 or 910-338-0255

TELEX: 34-6372

Always contact the MCD Technical Support Center before returning a product to Intel for service or repair. You will be given a "Repair Authorization Number", shipping instructions, and other important information which will help Intel provide you with fast, efficient service. If the product is being returned because of damage sustained during shipment from Intel, or if the product is out of warranty, a purchase order is necessary in order for the MCD Technical Support Center to initiate the repair.

In preparing the product for shipment to the MCD Technical Support Center, use the original factory packaging material, if available. If the original packaging is not available, wrap the product in a cushioning material such as Air Cap TH-240 (or equivalent) manufactured by the Sealed Air Corporation, Hawthorne, N.J., and enclose in a heavy-duty corrugated shipping carton. Seal the carton securely, mark it "FRAGILE" to ensure careful handling, and ship it to the address specified by MCD Technical Support Center personnel.

NOTE

Customers outside of the United States should contact their sales source (Intel Sales Office or Authorized Intel Distributor) for directions on obtaining service or repair assistance.

Table 5-1. User-Replaceable Parts List

Reference Designation	Part Description	Mfr. Code	Part No.	Quantity
A1,2,7,8	4-Bit Bidirectional Bus Driver	INT	8226	4
A13,14	Quad Line Receiver	TI	SN75189AN	2
A15	Quad Line Driver	TI	SN75188N	1
A19,37	Hex Inverters	TI	SN7404N	2
A20,30,38,49	Quad 2-Input Positive NAND Gate	TI	SN74S00N	4
A21,22	Parallel I/O Peripheral Interface	INT	8255A	2
A23	Serial I/O Peripheral Interface	INT	8251A	1
A24	Hex D-Type Flip-Flop	TI	SN74S174	1
A25,39	Dual D-Type Flip-Flop	TI	SN74LS74AN	2
A26,27,28	Synchronous 4-Bit Counter	TI	SN74LS161AN	3
A29,42	Quad Data Selector	TI	SN74LS258N	2
A31, 32, 47	3-to-8 Line Decoder	TI	SN74S138N	3
A33	Quad 2-Input Pos AND Gate	TI	SN74S08N	1
A35	Dual 5-Input Pos NOR Gate	TI	SN74S260N	1
A36	Dual 2-to-4 Line Decoder	TI	SN74S139N	1
A40,52,53	Quad 2-Input Pos NAND Gate	TI	SN74LS00N	3
A41	Quad 2-Input Pos OR Gate	TI	SN7432N	1
A43	Quad 2-Input Pos NOR Gate	TI	SN74S02N	1
A44	Hex Inverter	TI	SN74S04N	1
A45,56	1-of-8 Data Select	TI	SN74S151N	2
A48	Octal Tristate Buffer	TI	SN74LS244N	1
A50	Dynamic RAM Controller	INT	8202	1
A51	Octal D-Type Flip-Flop	TI	SN74LS273	1
A54,55	Hex Buffer/Driver	TI	SN7407N	2
A57	Octal Transparent Latch	TI	SN74LS373N	1
A58	Clock Generator and Driver	INT	8224	1
A64	8-to-3 Priority Encoder	TI	SN74148N	1
A65,68,69	Inverting Octal Bus Driver	TI	SN74S240N	3
A66	Octal Buffer and Line Driver	TI	SN74S241N	1
A67	Tristate Hex Inverter	NAT	DM8098N	1
A70	Octal Inverting Transceiver	INT	8287	1
C1-9,11,12,17,19-28, 31-50, 52-62,64,66-69, 71,75-80,83,89-95,97-99	Capacitor, .1uf,+80-20%,50V	COML	OBD	76
C51	Capacitor, .001uf,±20%,50V	COML	OBD	1
C84	Capacitor, .33uf,+80-20%,50V	COML	OBD	1
C63	Capacitor, 10Pf,±5%,500V	COML	OBD	1
C65,70,85,96	Capacitor, .01uf,+80-20%,50V	COML	OBD	4
C72-74,81,82,86,88	Capacitor, 22uf,Tant,15V	COML	OBD	7
C87	Capacitor, 4.7uf,Tant,10V	COML	OBD	1
R1,2,6,8,12,15	Composition Resistor, 1K,1/4w,5%	COML	OBD	6
R3,4,7,9	Composition Resistor,10K,1/4w,5%	COML	OBD	4
R5,13,14	Composition Resistor,430Ω,1/4w,5%	COML	OBD	3
R11	Composition Resistor,5.1K,1/4w,5%	COML	OBD	1
RP1,2	Resistor Package,1K,2%,10 pin	BECK	785-1-R1K	2
RP3,5-7	Resistor Package,10K,2%,10 pin	BECK	785-1-R10K	4
RP4,9	Resistor Package,2.2K,2%,8 Pin	BECK	764-1-R2.2K	2
RP8	Resistor Package,22K,2%,8 Pin	BECK	764-1-R22K	1
S3,4	Switch, DIP, 8-Position	CTS	206-8	2
W2	Socket, IC, 8-Pin	AUG	508-AG37D	1
W3	Socket, IC, 18-Pin DIP	TI	C-84-18-02	1
W11/W12,W13/W14, W15/W16,XA1,XA2, XA7,XA8	Socket, 16-Pin DIP	TI	C-84-16-02	7
XA3-6,XA9-12	Socket, 14-Pin DIP	TI	C-84-14-02	8
XA34,XA46,XA60,XA76	Socket, 28-Pin DIP	TI	C-84-28-02	4
XA50	Socket, IC, 40-Pin, Side Wipe	BUR	DIL 40P-3	1
Y1	Crystal 22.1184 MHz (Fundamental)	CTS	H3W	1

Table 5-1. User-Replaceable Parts List (Continued)

Reference Designation	Part Description	Mfr. Code	Part No.	Quantity
—	Connector, Shorting Plug, 4 Pos.	AUG	8136-475G4	2
—	Connector, Shorting Plug, 8 Pos.	AUG	8136-475G8	1
—	Connector, Socket, 2 Pos. Shorting	AMP	530153-2	4
—	Connector, Wafer Header	AMP	87227-4	8
—	Pin, Shorting, 2 Pos.	AUG	8136-651P2	4
—	Post, Wire Wrap	AMP	87022-1	73

Table 5-2. List of Manufacturers' Codes

Mfr. Code	Manufacturer	Address	Mfr. Code	Manufacturer	Address
INT	Intel Corporation	Santa Clara, CA	BECK	Beckman Instruments	Fullerton, CA
TI	Texas Instruments	Dallas, TX	CTS	CTS Corporation	Elkhart, IN
NAT	National Semiconductor Corp.	Santa Clara, CA	AUG	Augut, Inc.	Attleboro, MA
			BUR	Burndy Corp.	Norwalk, CT
COML	Any Commercial Source — Order by Description		AMP	Amp. Incorporated	Harrisburg, PA

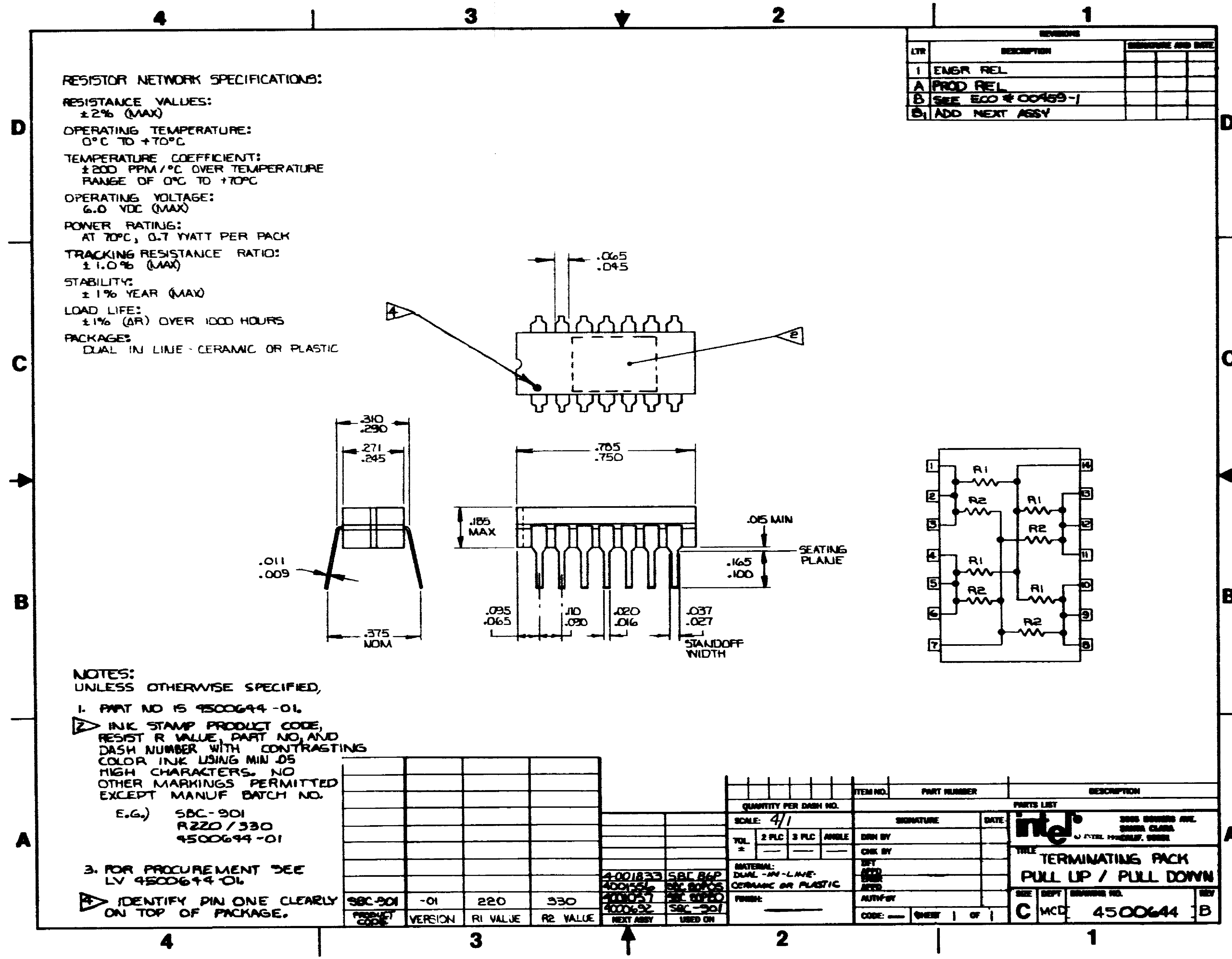


Figure 5-4. iSBC 901™ Termination Package

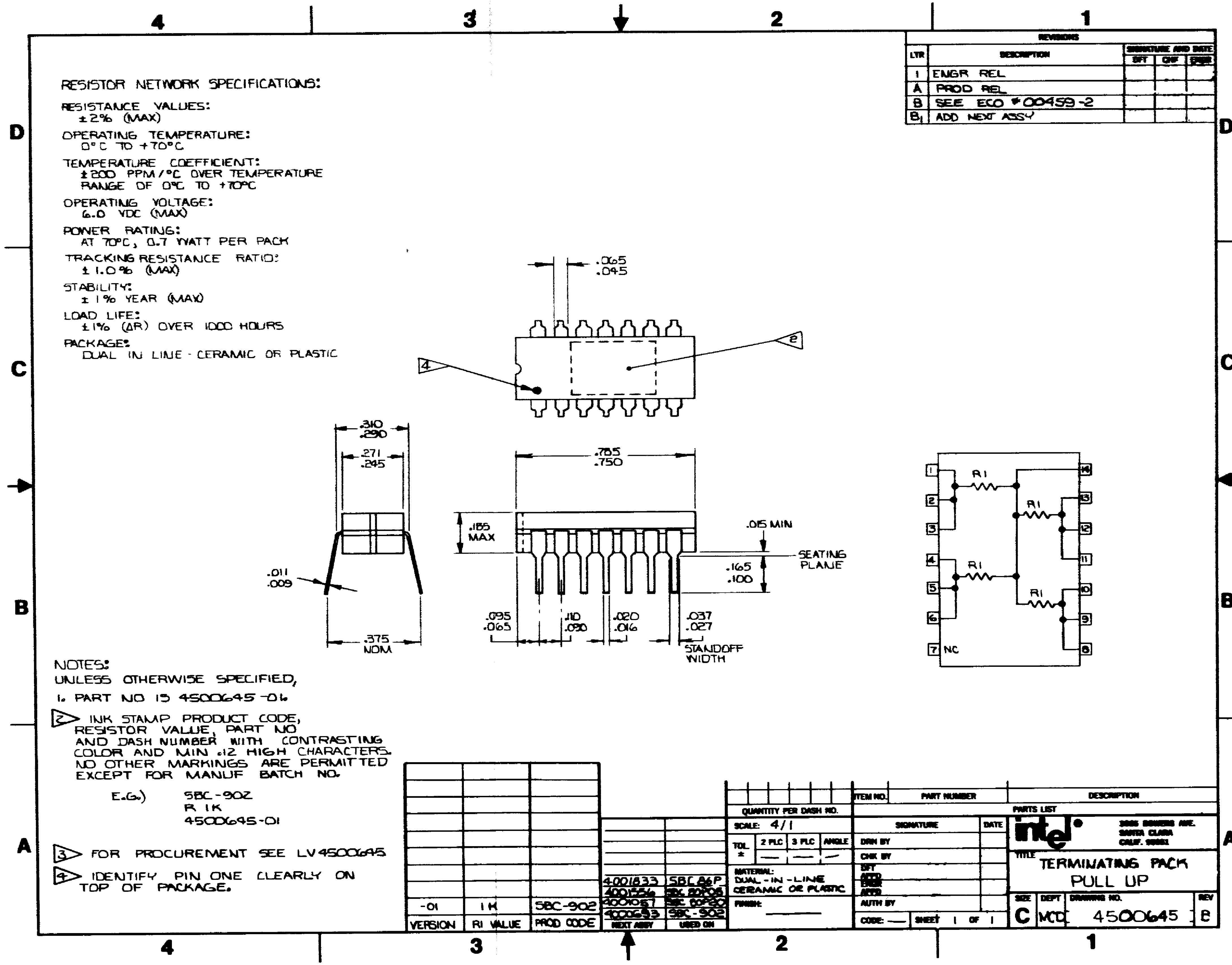


Figure 5-3. iSBC 902™ Termination Package

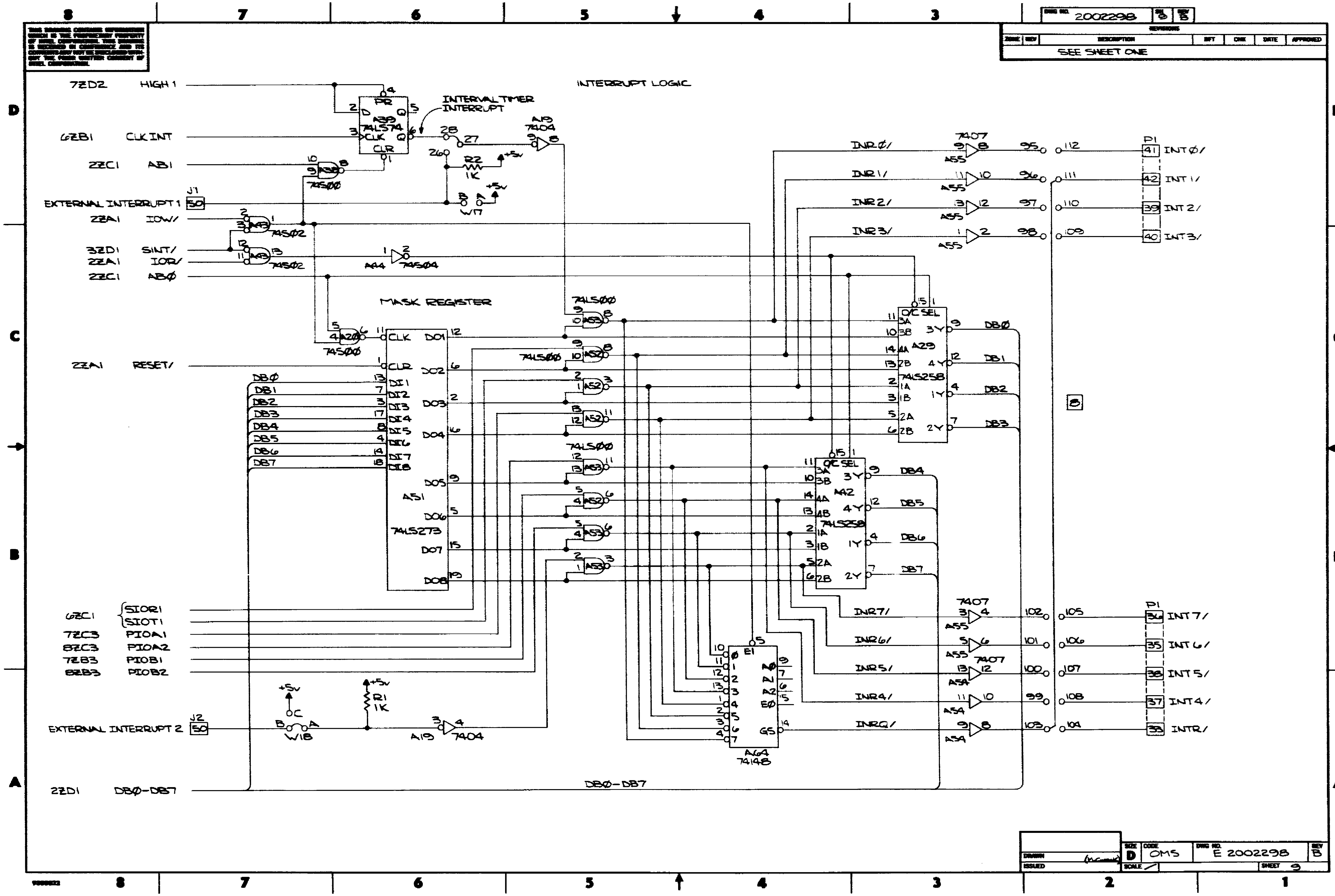


Figure 5-2. iSBC 108A/116A™ Board Schematic Diagram (Sheet 9 of 9)

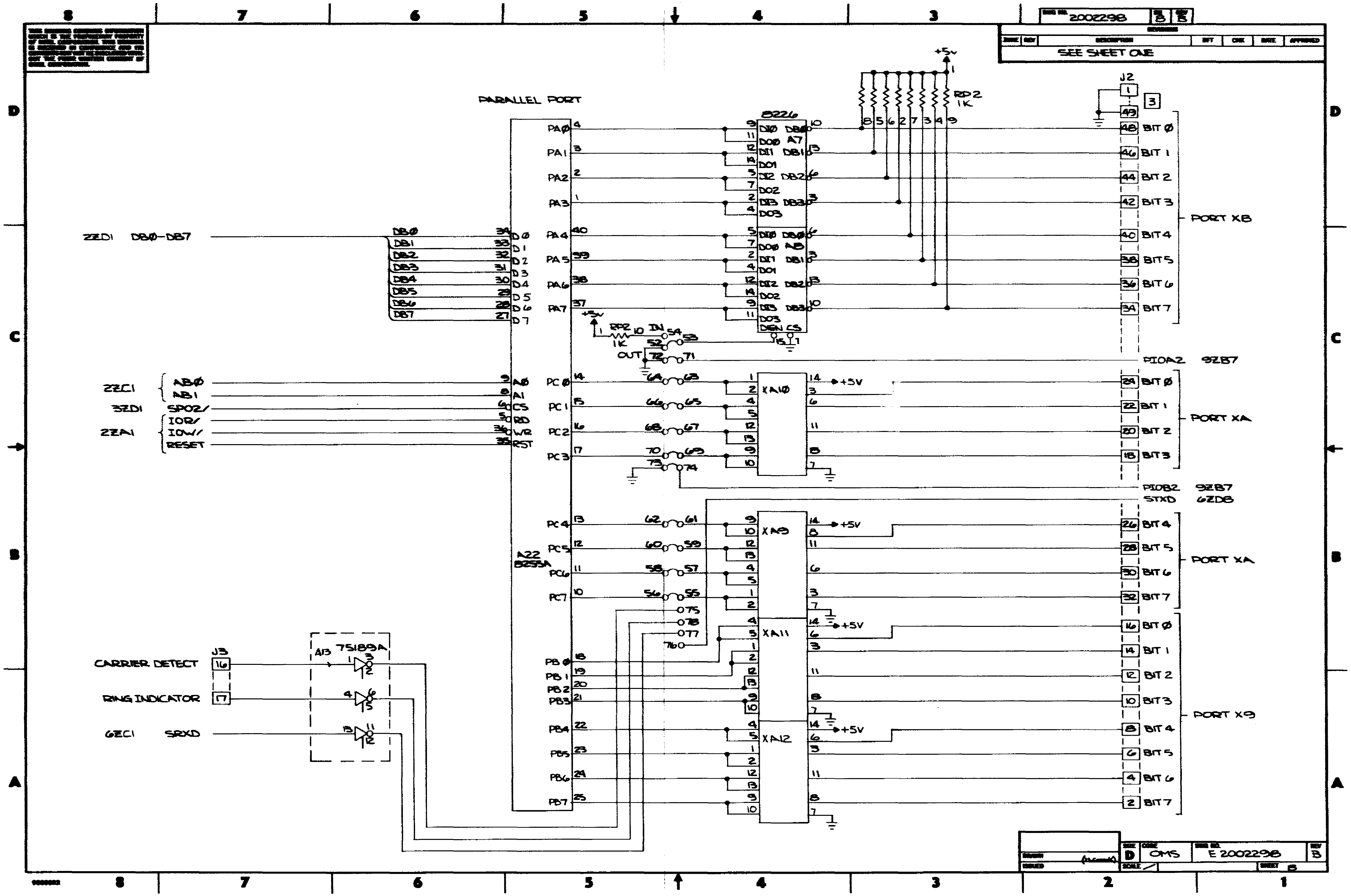


Figure 5-2. iSBC 108A/116A™ Board Schematic Diagram (Sheet 8 of 9)

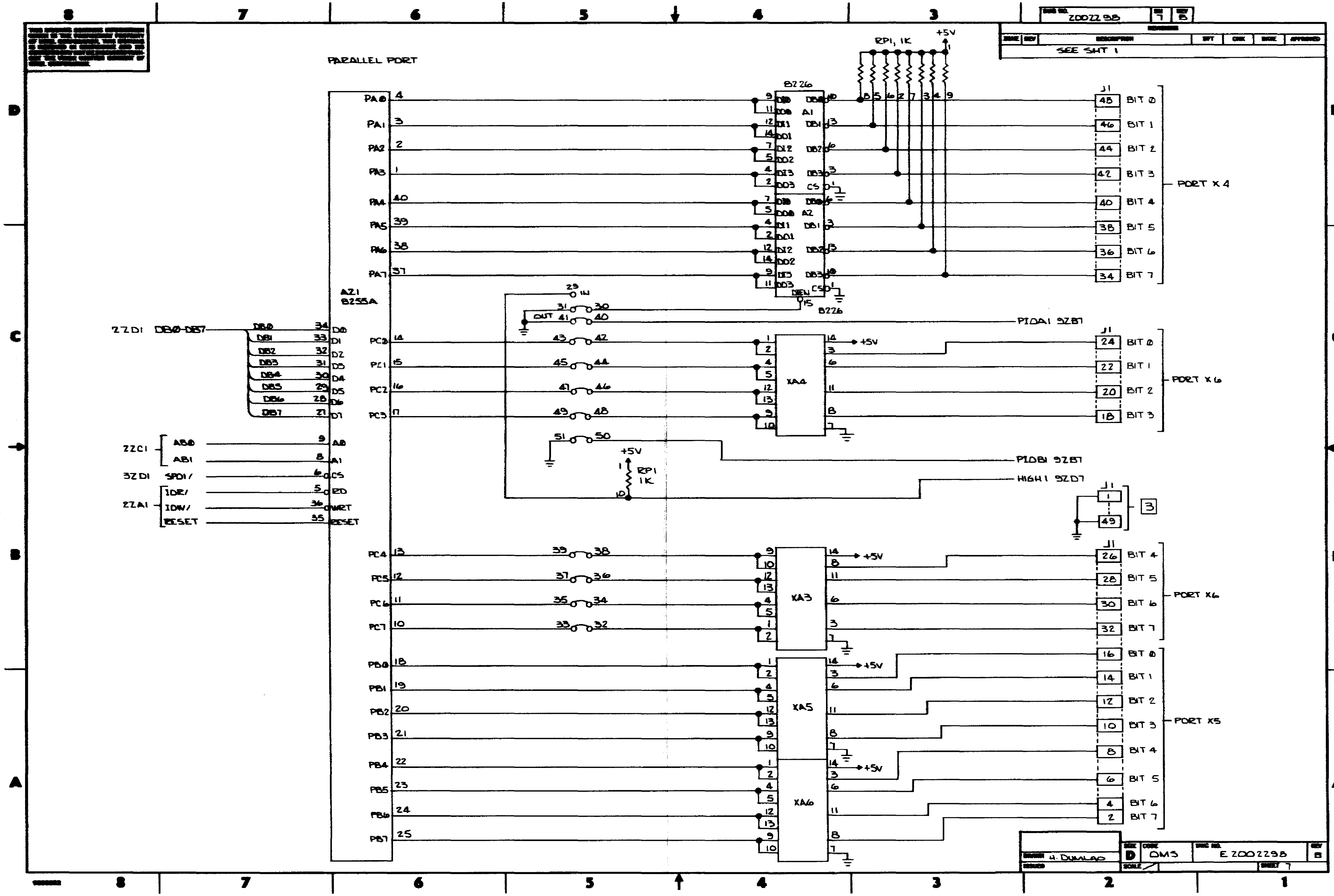


Figure 5-2. iSBC 108A/116A™ Board Schematic Diagram (Sheet 7 of 9)

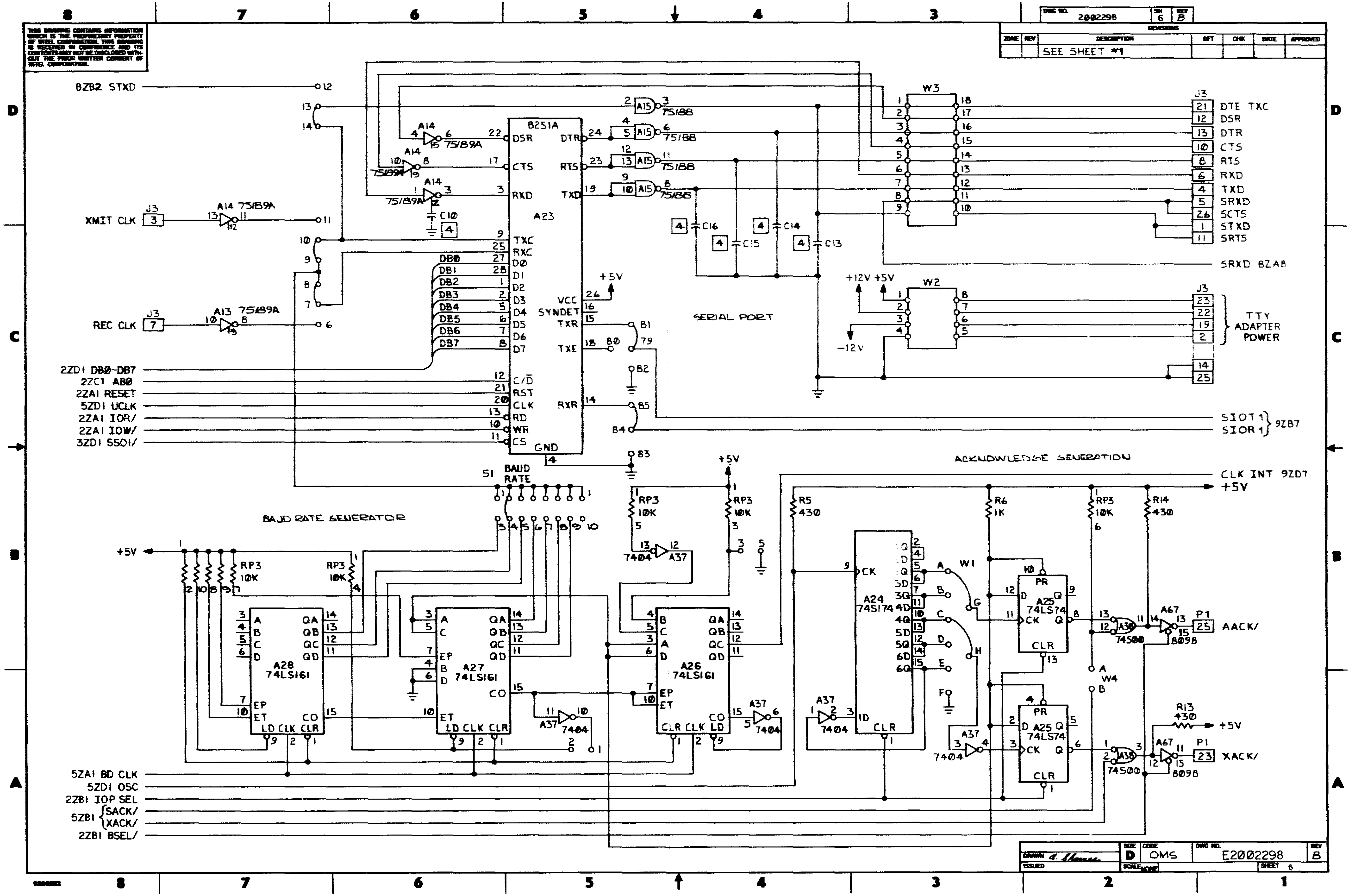


Figure 5-2. iSBC 108A/116A™ Board Schematic Diagram (Sheet 6 of 9)

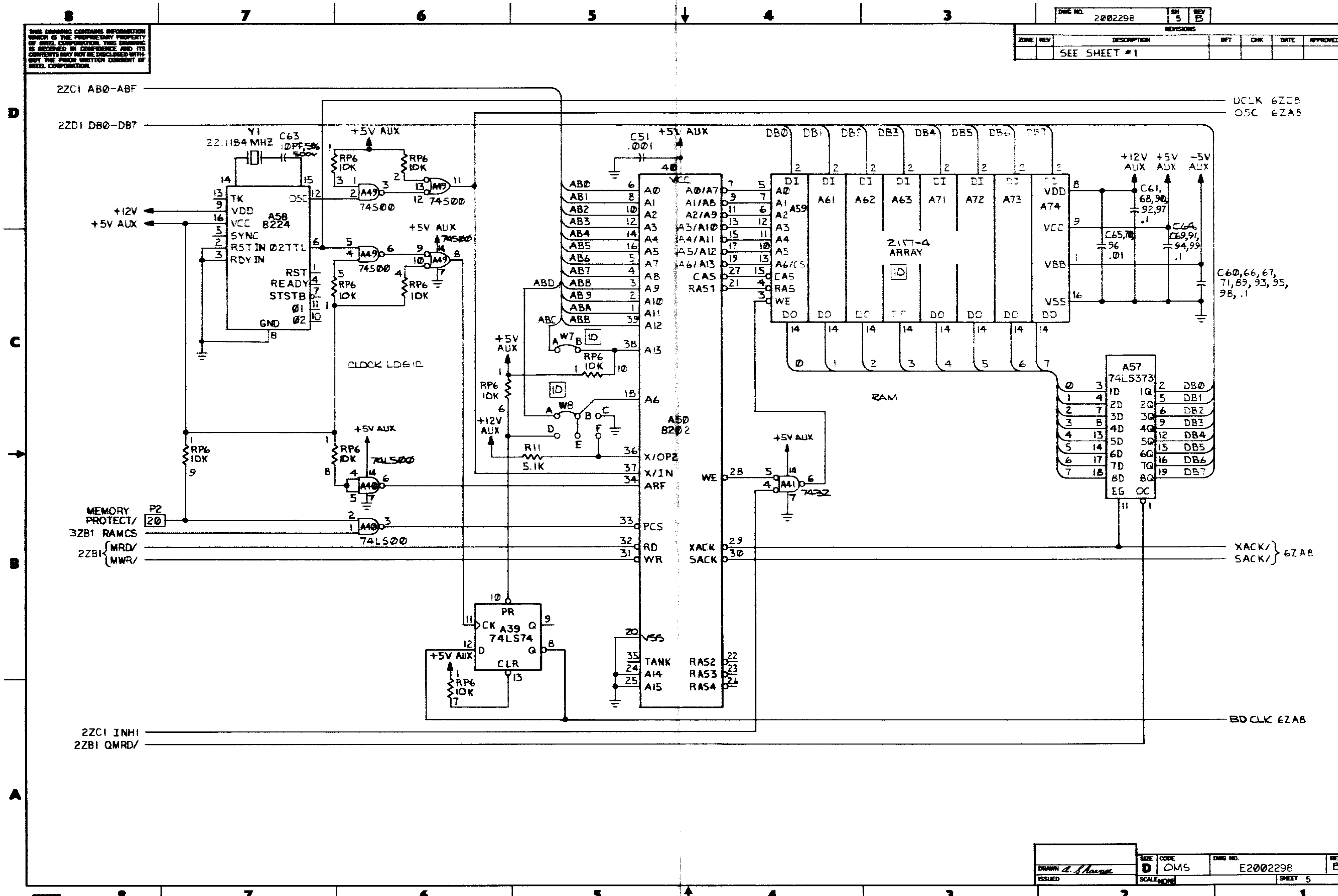


Figure 5-2. iSBC 108A/116A™ Board Schematic Diagram (Sheet 5 of 9)

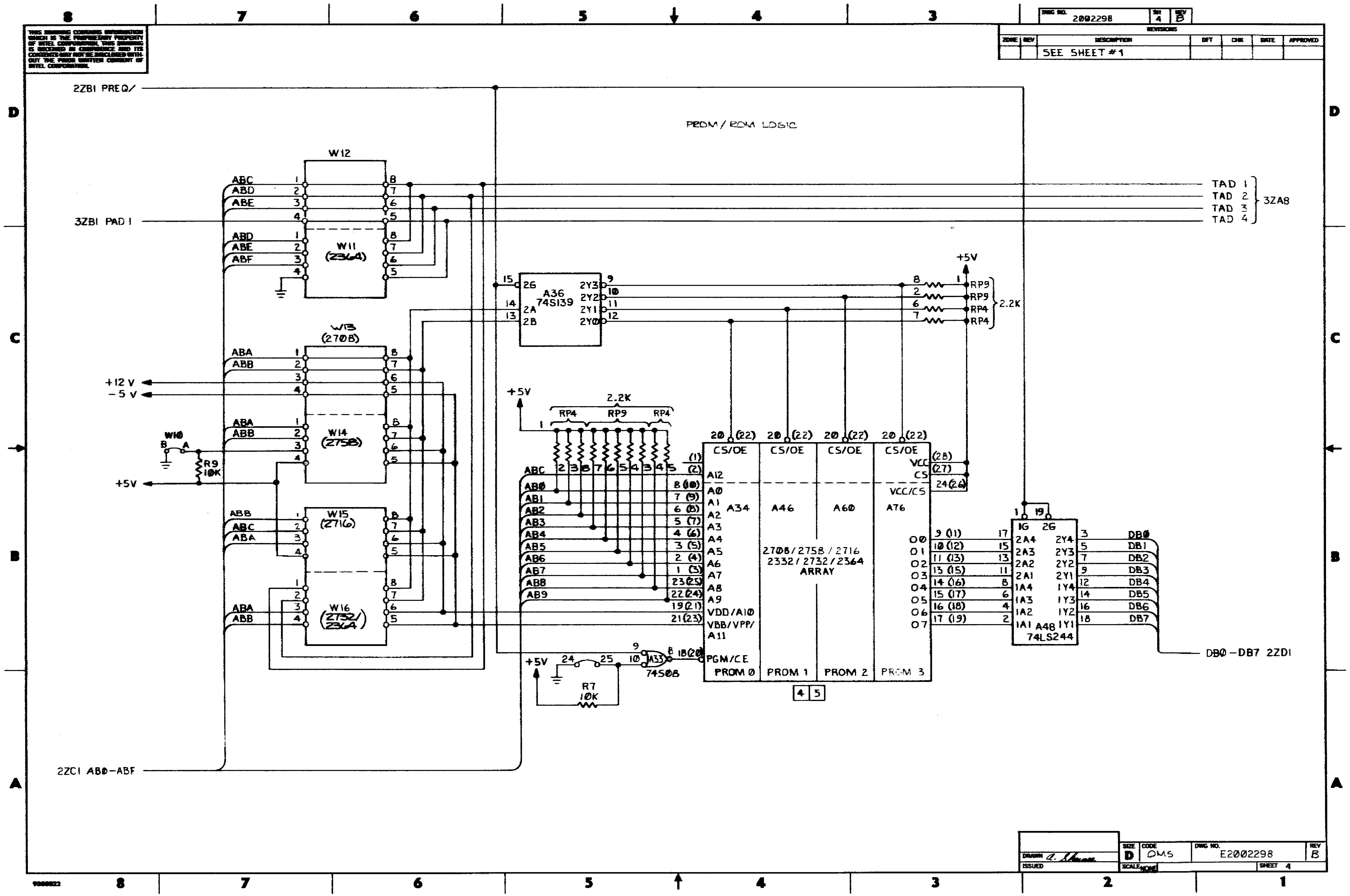


Figure 5-2. iSBC 108A/116A™ Board Schematic Diagram (Sheet 4 of 9)

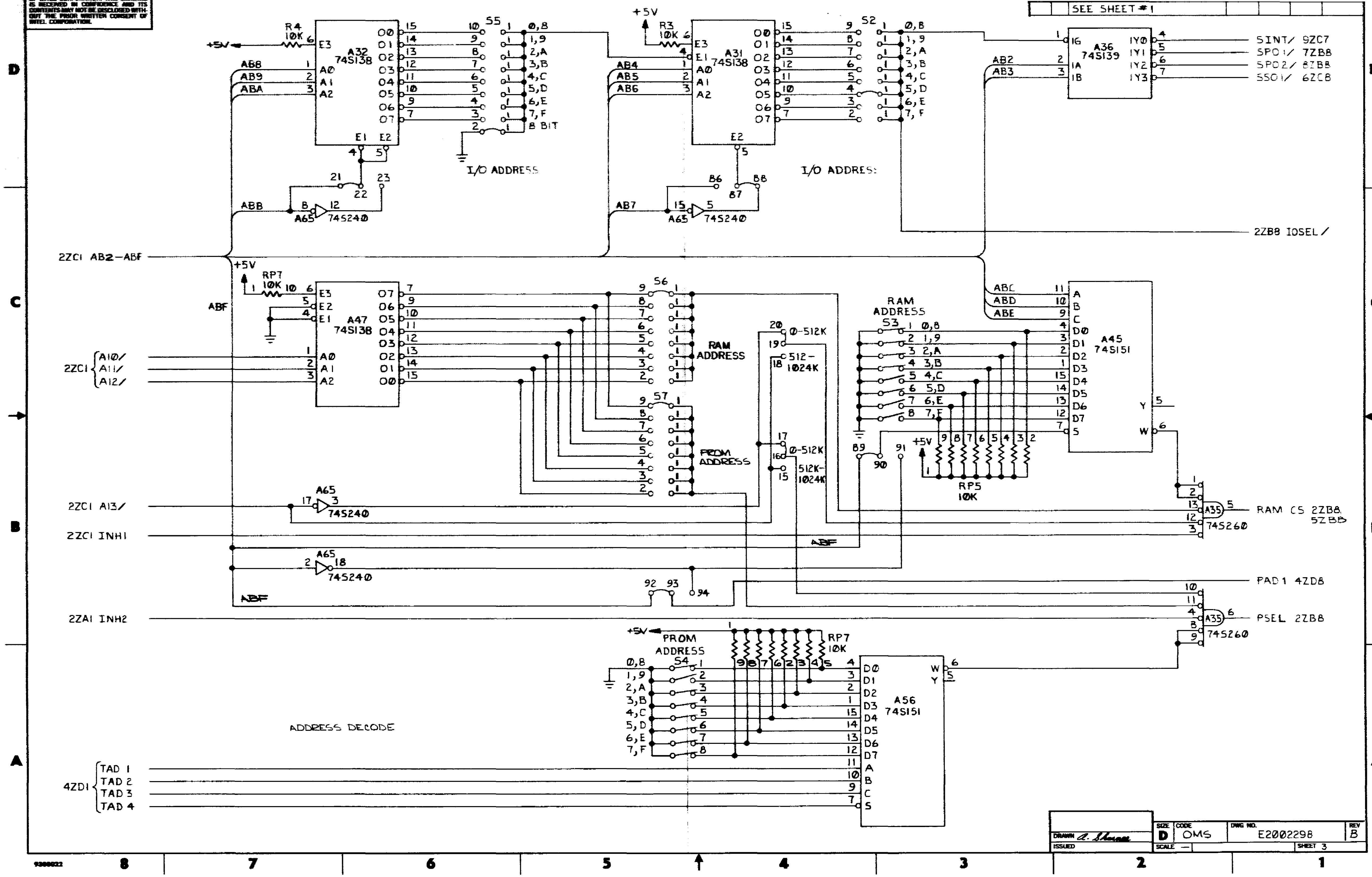


Figure 5-2. iSBC 108A/116A™ Board Schematic Diagram (Sheet 3 of 9)

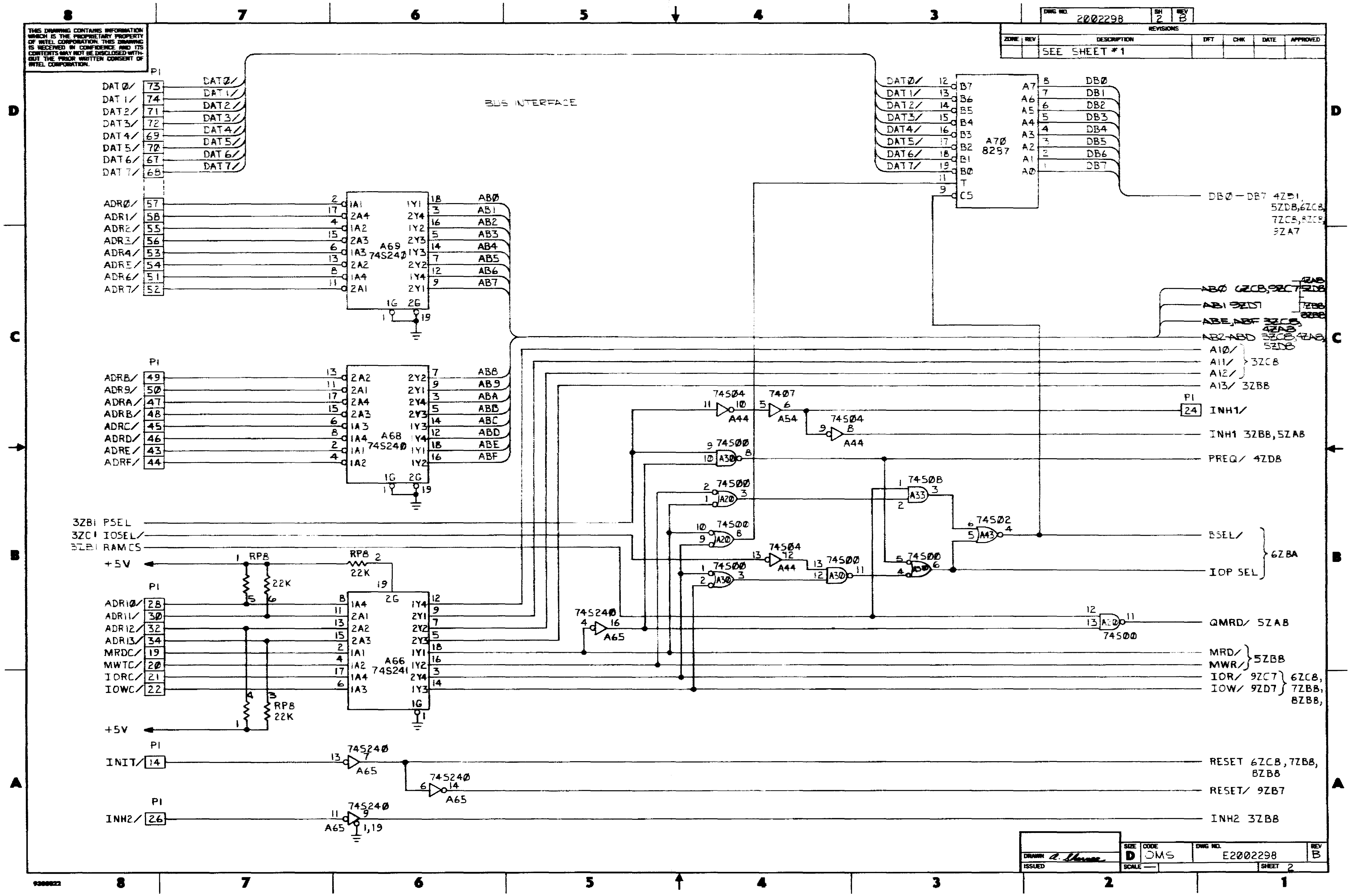


Figure 5-2. iSBC 108A/116A™ Board Schematic Diagram (Sheet 2 of 9)

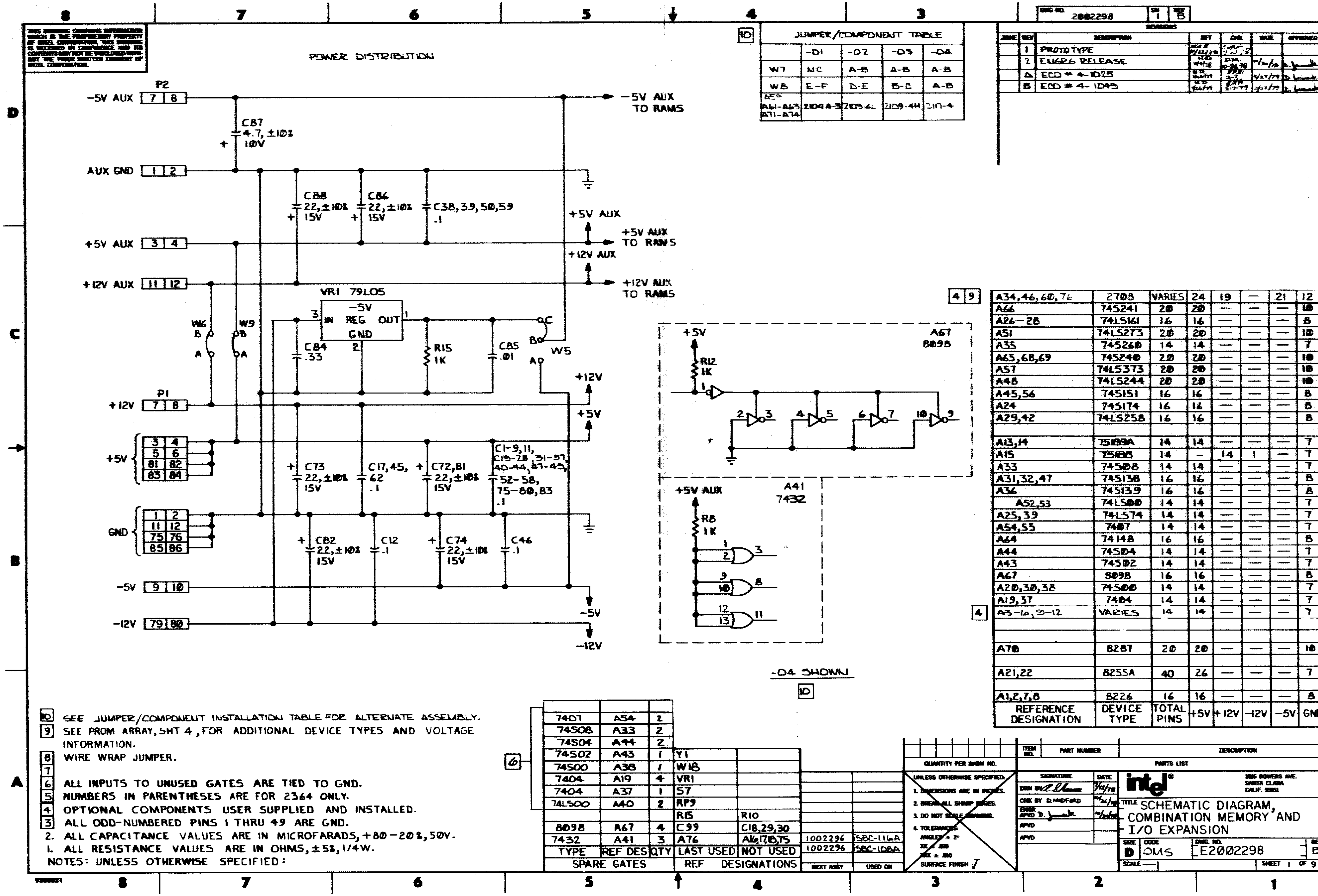


Figure 5-2. iSBC 108A/116A™ Board Schematic Diagram (Sheet 1 of 9)

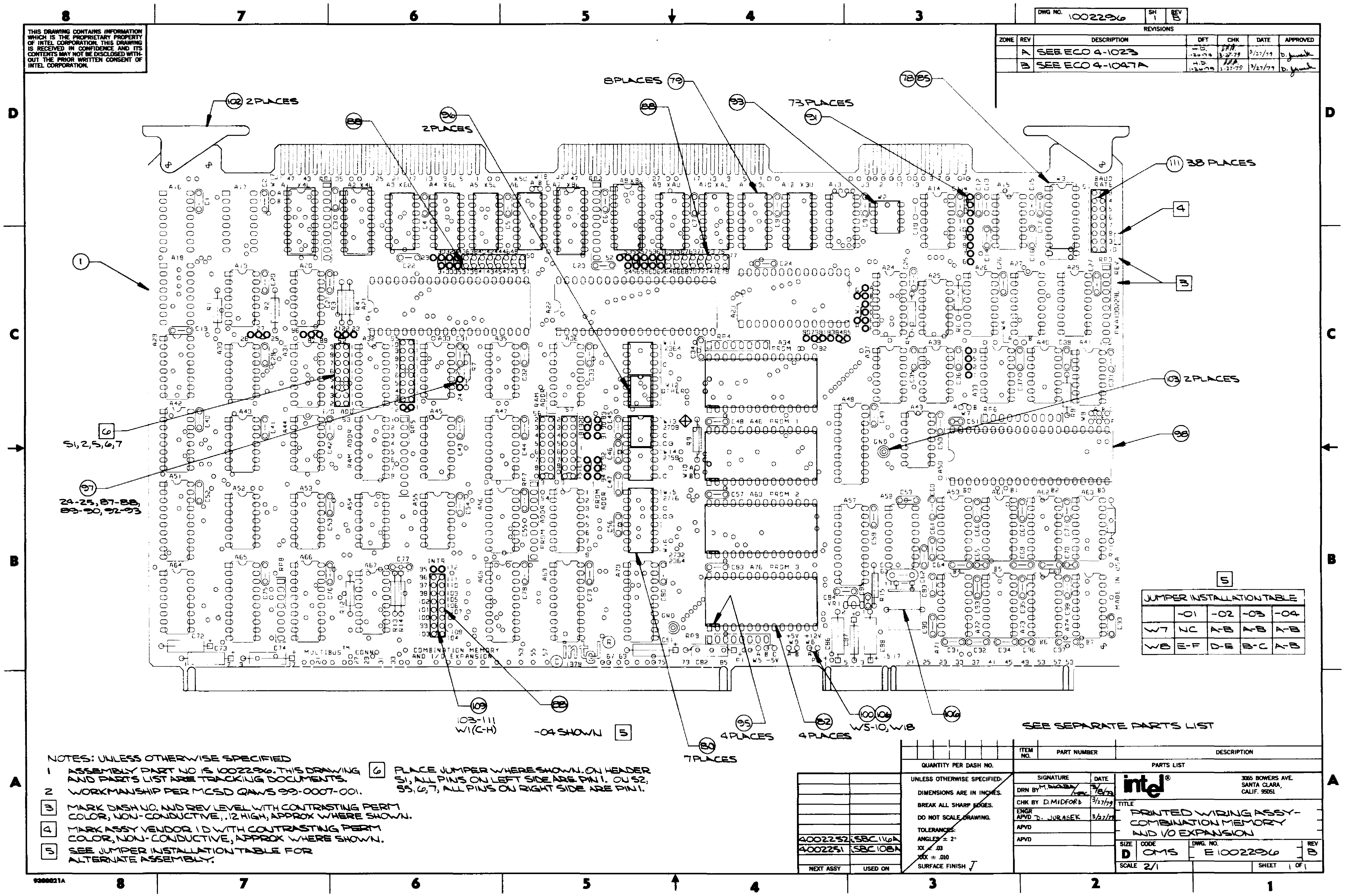


Figure 5-1. iSBC 108A/116A™ Board Parts Location

APPENDIX A
MNEMONICS

AACK	Advanced Acknowledge
AB0-AB13	Address Bit 0 - Address Bit 13 (Hex)
ADR0-ADR13	Bus Address Bit 0 - Bus Address Bit 13 (Hex)
BDCLK	Baud Clock
BSEL	Board Select
CLK INT	Clock Interrupt
CTS	Clear To Send
DAT0-DAT7	Bus Data Bit 0 - Bus Data Bit 7
DB0-DB7	Data Bit 0 - Data Bit 7
DSR	Data Set Ready
DTE TXC	Data Terminal Equipment Transmit Clock
DTR	Data Terminal Ready
HIGH1	A Pull-up
INH1	Inhibit 1 - RAM Inhibit
INH2	Inhibit 2 - PROM Inhibit
INIT	Initialize (Reset)
INTR	Interrupt
INT0-INT7	Vectored Interrupt Level 0 - Vectored Interrupt Level 7
IOP SEL	I/O and PROM Select
IOR	I/O Read
IORC	Bus I/O Read Command
IOSEL	I/O Select
IOW	I/O Write
IOWC	Bus I/O Write Command
MRD	Memory Read
MRDC	Bus Memory Read Command
MWR	Memory Write
MWTC	Bus Memory Write Command
OSC	Oscillator
PAD1	PROM Address 1
PIOA1	Parallel I/O Port A, Interrupt 1
PIOA2	Parallel I/O Port A, Interrupt 2
PIOB1	Parallel I/O Port B, Interrupt 1
PIOB2	Parallel I/O Port B, Interrupt 2
PREQ	PROM Request
PSEL	PROM Select
QMRD	Qualified Memory Read
RAM CS	RAM Chip Select
RESET	Board Reset
RTS	Request To Send
RXD	Receive Data
SACK	System Acknowledge (RAM Advance Acknowledge)
SCTS	Secondary Clear To Send
SINT	Select Interrupt
SIOR1	Serial I/O, Receive Interrupt 1
SIOT1	Serial I/O, Transmit Interrupt 1
SPO1	Select Parallel I/O 1
SPO2	Select Parallel I/O 2
SRTS	Secondary Request To Send
SRXD	Secondary Receive Data
SSO1	Select Serial I/O 1
STXD	Secondary Transmit Data
TAD1-TAD4	Transformed Address 1 - Transformed Address 4
TXD	Transmit Data
UCLK	USART Clock
XACK	Transfer Acknowledge
XMIT CLK	Transmit Clock

APPENDIX B
JUMPER CONFIGURATION

Table B-1. Jumper Configuration Changes from iSBC 108/116™ Boards to iSBC 108A/116A™ Boards

Jumper	New Function	Old Function	Comments
1,2,3,5-14,26-112	No change		
4	Pin eliminated	Baud rate generator option	Jumper overrides default PC board trace. See paragraph 2-23.
15-20	Mem. upper address bit decode	RS232 Port Conf.	RS232 Port Conf. now controlled by a single jumper block (W3). See paragraph 2-21.
21,22,23	I/O upper address bit decode	RS232 Port Conf.	
24,25	PROM standby power option	RS232 Port Conf.	
"W" Jumper Blocks			
W1	No change in function	I/O and PROM XACK & AACK Enable	Pin assignments changed. New wire wrap. See para. 2-20.
W2	TTY adaptor power	PROM type select	PROM select now done with jumpers W11-W16. See paragraph 2-12.
W3	RS232 port configuration	PROM type select	
W4	Eliminated	PROM type select	
W5	Added pin	Aux. power supply enable	Extra pin added for on board regulator. See paragraph 2-31.
W6	No change	Aux. power supply enable	
W7	RAM component type selection	RAM ACK timing	RAM TAACK is nonselectable on A version boards. See paragraph 2-20.
W8	RAM component type selection	RAM refresh	RAM component type is not a user option
W9	No change	Aux. power supply enable	
W10	2758 Configuration jumper	RAM component type selection	
W11-W16	PROM type selection	none	jumper blocks
W17,18	+5V to J1 and J2	none	wire jumper
"S" Jumpers			
S1	No change	Baud Rate Selection	shape of array changed
S2	No change	I/O Base Address Select	shape of array changed
S5	I/O base address select	none	enlarged address space
S6	RAM base address select	none	
S7	ROM base address select	none	
Switches			
S3	No change	RAM base address selection	location changed slightly
S4	No change	ROM base address selection	location changed slightly

intel®

REQUEST FOR READER'S COMMENTS

Intel Corporation attempts to provide documents that meet the needs of all Intel product users. This form lets you participate directly in the documentation process.

Please restrict your comments to the usability, accuracy, readability, organization, and completeness of this document.

1. Please specify by page any errors you found in this manual.

2. Does the document cover the information you expected or required? Please make suggestions for improvement.

3. Is this the right type of document for your needs? Is it at the right level? What other types of documents are needed?

4. Did you have any difficulty understanding descriptions or wording? Where?

5. Please rate this document on a scale of 1 to 10 with 10 being the best rating. ____________

NAME ______________________________ DATE ____________

TITLE ______________________________

COMPANY NAME/DEPARTMENT ______________________________

ADDRESS ______________________________

CITY ______________________ STATE ______ ZIP CODE ________

Please check here if you require a written reply. ☐

WE'D LIKE YOUR COMMENTS . . .

This document is one of a series describing Intel products. Your comments on the back of this form will help us produce better manuals. Each reply will be carefully reviewed by the responsible person. All comments and suggestions become the property of Intel Corporation.

NO POSTAGE
NECESSARY
IF MAILED
IN U.S.A.

BUSINESS REPLY MAIL

FIRST CLASS PERMIT NO. 1040 SANTA CLARA, CA

POSTAGE WILL BE PAID BY ADDRESSEE

Intel Corporation
Attn: Technical Publications
3065 Bowers Avenue
Santa Clara, CA 95051