iSBC® 552 ETHERNET COMMUNICATIONS CONTROLLER HARDWARE REFERENCE MANUAL

Intel Corporation, 3065 Bowers Avenue, Santa Clara, California 95051

Order Number: 122141-002

iSBC® 552 ETHERNET COMMUNICATIONS CONTROLLER HARDWARE REFERENCE MANUAL

Order Number: 122141-002

Intel Corporation, 3065 Bowers Avenue, Santa Clara, CA 95051

Additional copies of this manual or other Intel literature may be obtained from:

Literature Department
Intel Corporation
3065 Bowers Avenue
Santa Clara, CA 95051

Intel retains the right to make changes to these specifications at any time, without notice. Contact your local sales office to obtain the latest specifications before placing your order.

Intel Corporation makes no warranty of any kind with regard to this material, including, but not limited to, the implied warranties of merchantability and fitness for a particular purpose. Intel Corporation assumes no responsibility for any errors that may appear in this document. Intel Corporation makes no commitment to update nor to keep current the information contained in this document.

Intel Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in an Intel product. No other circuit patent licenses are implied.

The following are trademarks of Intel Corporation and its affiliates and may only be used to identify Intel products:

BITBUS
COMMputer
CREDIT
Data Pipeline
Genius
i
$\overset{\vartriangle}{\imath}$
I^2ICE
ICE
iCS
iDBP
iDIS
iLBX
$\mathrm{i_m}$
iMMX
Insite
int$_e$l
int$_e$lBOS
Intelevision
int$_e$ligent Identifier
int$_e$ligent Programming
Intellec
Intellink
iOSP
iPDS
iRMX
iSBC
iSBX
iSDM
iSXM
KEPROM
Library Manager
MCS
Megachassis
MICROMAINFRAME
MULTIBUS
MULTICHANNEL
MULTIMODULE
Plug-A-Bubble
PROMPT
Promware
QueX
QUEST
Ripplemode
RMX/80
RUPI
Seamless
SOLO
SYSTEM 2000
UPI

Ethernet is a trademark of Xerox Corporation.

A1356/485/2.5/SVP/KH
SINGLE BOARD COMPUTERS

REV.	REVISION HISTORY	DATE	APPD.
-001	Original issue.	3/84	L.K.
-002	Changed all reference to 8 MHz operating frequency to 6 MHz operating frequency. General updating, all pages.	4/85	L.K.

PREFACE

This manual describes the iSBC 552 Ethernet Communications Controller. The manual is divided into the following four chapters:

Chapter 1, "General Information," provides a general description of the board and summarizes board specifications.

Chapter 2, "Installation Information," provides receiving instructions for the board, discusses installation requirements, including board dimensions, power and cooling requirements, physical interfaces, interface timing, jumper installation, additional memory installation, transceiver cable installation, and grounding.

Chapter 3, "Operation," describes board operations and functional interfaces and defines the board's input/output signals.

Chapter 4, "Programming Information," provides programming information for the iSBC 552 board.

Appendix A, "Service Diagrams," provides a component location diagram and schematic diagram for the iSBC 552 board.

The following documents provide additional reference information for the iSBC 552 board and its components. It is strongly recommended that the user become familiar with the iAPX Data Sheet, order number 210451-003. This document provides detailed information for programming the 80186 microprocessor.

Intel MULTIBUS® specification, order number 9800683-004
Ethernet Data Link and Physical Layer Specification, Version V2
(Intel/DEC/XEROX)
Microsystem Components Handbook, (Intel) order number 230843-001
LAN Components User's Manual, (Intel) order number 230814-001
IEEE P802 Local Area Network Standard Project, Logical Link Control Sublayer,
Parts A, B, C, May 7, 1982

TABLE OF CONTENTS

PAGE

CHAPTER 1. GENERAL INFORMATION

CHAPTER 2. INSTALLATION INFORMATION

CHAPTER 3. OPERATION

PAGE

CHAPTER 4. PROGRAMMING INFORMATION

TABLE OF CONTENTS

PAGE

APPENDIX A. SERVICE DIAGRAMS

FIGURES

TABLES

CHAPTER 1.
GENERAL INFORMATION

1.1 INTRODUCTION

This manual describes the iSBC 552 Ethernet Communications Controller and is intended to help users install, program, and operate the iSBC 552 board. The manual is not intended to be a theory of operation manual. Any theory of operation information presented is limited to that directly relating to the topics discussed in the manual.

1.2 iSBC®552 BOARD DESCRIPTION

The iSBC 552 board is an intelligent single-board computer board configured as an Ethernet communication controller module for MULTIBUS board systems.

Figure 1-1 shows the interconnection of several Ethernet workstations and the role of the iSBC 552 controller in that total system environment. Each workstation is a computer system that has a host CPU board, MULTIBUS memory and an iSBC 552 board. The iSBC 552 board allows the host to gain access to the Ethernet channel and to translate the serially formatted data of the transceiver to a data format acceptable to the host.

Once started by a command from the host the receiving process requires no further host intervention while it detects the beginning of packets, performs address checking, and moves data.

In a transmit process the iSBC 552 board, upon command from the host, moves data from the memory, gains access to the serial link, formats the data into packets and addresses the packets for the designated station. Once started by the host command, the transmit process requires no further host intervention while it moves data.

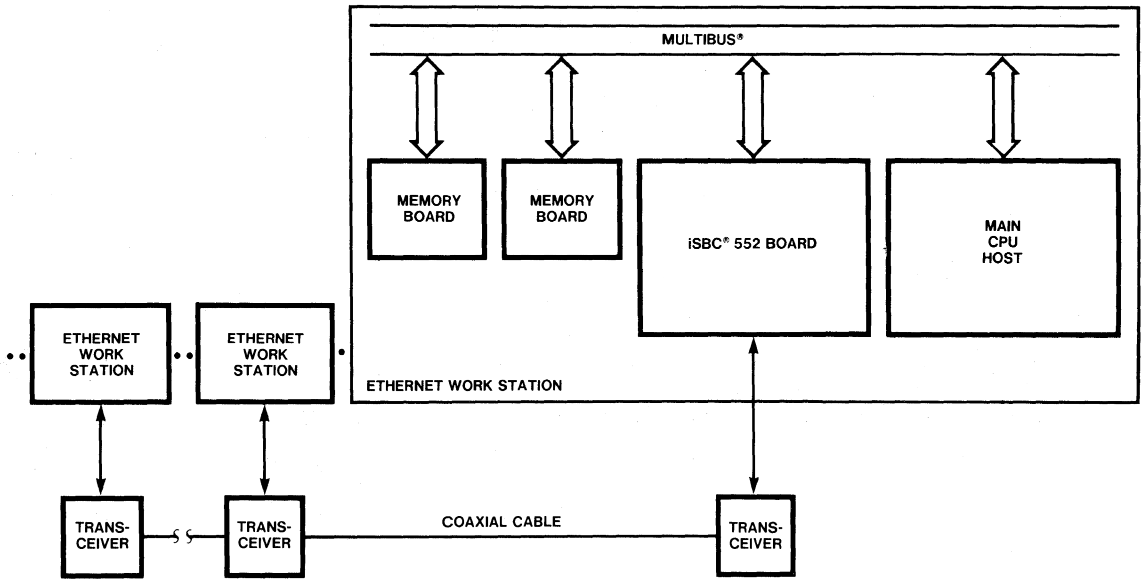


Figure 1-1. The iSBC® 552 Board and the Ethernet MULTIBUS® System 122141-1

The iSBC 552 board has on-board an 80186 microprocessor running at 6 MHz. The 80186 moves control information and data between the MULTIBUS memory and the on-board memory that is also accessible to the 82586 Local Communications Controller (LCC). The 80186 can access the entire 16M byte MULTIBUS memory map through a movable window in its local memory map and can also perform I/O on the MULTIBUS throughout the entire 64K byte space. The 82586 LCC runs as a co-processor sharing a common bus with the 80186. The LCC can access only memory local to the iSBC 552 board.

The 82586 LCC and the 82501 Ethernet Serial Interface (ESI) supply the majority of the Ethernet communication functions for the iSBC 552 board. The 82501 ESI decodes the incoming Manchester-formatted data from the Ethernet transceiver to NRZ serial data for processing on the iSBC 552. The ESI also encodes outgoing NRZ serial data to Manchester data for the Ethernet transceiver.

The iSBC 552 board has provision for two types of memory, RAM and EPROM. The RAM memory is used for serial link data buffering and control structures for the 82586 LCC. The EPROM contains the 80186 firmware. Six pairs of byte-wide sockets are provided for the memory. One of the six pairs is used exclusively for EPROMs. A second pair is used exclusively for RAMs. The remaining four pairs are jumper selectable for either PROMs or RAMs and are used for memory expansion.

The operating cycles of the iSBC 552 board are discussed in Chapter 3. Programming of the boards components is described in Chapter 4.

The iSBC 552 board is functionally compatible with the Intel iSBC 550A board. All functions of the iSBC 550A may be supported by the iSBC 552 board.

1.3. SPECIFICATIONS

Table 1-1 lists the iSBC 552 board specifications.

Table 1-1. iSBC® 552 Board Specifications

Data Transfer	8 or 16-bits.
Average Throughput	250K Bytes/Second (450ns, 16 bit system memory and no MULTIBUS contention).
Transceiver Interface	
Transmit Data Rate	10M bits/second.
Signal Levels	Series 10,000 ECL-compatible.
Host Interrupts	One MULTIBUS non-bus vectored interrupt for use in system/host handshaking.
MULTIBUS Interface	The iSBC 552 board conforms to all AC and DC requirements outlined in Intel MULTIBUS Specification, except for the following signals: Signal — iSBC Board — MULTIBUS Spec. DAT0*- DAT7* — I_{IH} = 180µA — I_{IH} = 125µA
DC Power Required	All voltages supplied by the MULTIBUS interface. + 5.0V ± 5%, 5.9A maximum +12.0V ± 5%, 0.5A maximum
Environmental	
Temperature	0 to 55°C operating -40 to 65°C non-operating
Humidity	5% to 90% operating 5% to 95% non-operating

CHAPTER 2.
INSTALLATION INFORMATION

2.1 INTRODUCTION

This chapter presents installation information for the iSBC 552 board. It describes receiving procedures and installation requirements, such as board dimensions, operating voltage, and jumper installation. It also provides interface timing and signal characteristics as well as procedures for installing the internal transceiver cable and additional on-board memory.

NOTE

A signal name/mnemonic followed by an asterisk indicates that signal is active in its low state.

2.2 SUPPLIED EQUIPMENT

Table 2-1 lists the equipment supplied by Intel and the user for iSBC 552 installation.

The user supplied EPROMs and RAMs are used in the iSBC 552 boards local memory array. A minimum of two EPROMs and two RAMs are required. Additional memory EPROMs or RAMs can be added (see Section 2.4.8).

Table 2-1. Equipment Supplied and Furnished

Part Number	Part	Quantity
Intel Supplied Equipment		
114496-003	iSBC 552 Ethernet Controller Board	1
User-Supplied Equipment		
2764-2	(8Kx8) UV Erasable PROM (or equivalent)	2 minimum 10 maximum
or 27128-2	(16Kx8) UV Erasable PROM (or equivalent)	2 minimum 10 maximum
2186-30	8192x8-Bit Integrated RAM (or equivalent)	2 minimum 10 maximum

2.3 RECEIVING

Inspect the shipping carton immediately upon receipt for evidence of mishandling during transit. If the shipping carton is severely damaged or waterstained, request the carrier's agent be present when the carton is opened. If the carrier's agent is not present when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

Save the salvageable shipping cartons and packing materials if the product must be reshipped.

United States customers can obtain service and repair assistance by contacting the Intel Product Service Hotline in Phoenix, Arizona. Customers outside the United States should contact their sales source (Intel Sales Office or authorized distributor) for service information and repair assistance.

Before calling the Product Service Hotline you should have the following information available:

1. Date you received the product.
2. Complete product part number (including dash number). This identification number is (on a white tag on the board).
3. Product serial number is on a white tag on the board.
4. Shipping and billing address.
5. If your Intel product warranty has expired, you must provide a purchase order number for billing.
6. If you have an extended warranty agreement, be sure to advise the Hotline personnel of this agreement.

Use the following telephone numbers for contacting the Intel Product Service Hotline:

U.S. Eastern Region	(602) 869-4045
U.S. Central Region	(602) 869-4392
U.S. Western Region	(602) 869-4951
International	(602) 869-4862

Always contact the Product Service Hotline before returning a product to Intel for repair. You will be given a repair authorization number, shipping instructions, and other important information, which helps Intel provide fast, efficient service. If returning the product because of damage sustained during shipment, or if the product is out of warranty, you must give Intel a purchase order before repairs can be initiated.

In preparing the product for shipment to the repair center, use the original factory packing material if possible. If the material is not available, wrap the product in a cushioning material such as Air Cap TH-240 (manufactured by the Sealed Air Corporation, Hawthorne, New Jersey). Then, enclose the wrapped product in a heavy-duty corrugated shipping carton and label it "FRAGILE" to ensure careful handling. Ship the carton only to the address specified by Product Service Hotline personnel.

2.4 INSTALLATION REQUIREMENTS

Sections 2.4.1 through 2.4.11 outline and describe the iSBC 552 board's installation requirements. The areas covered are listed below:

Section	Heading
2.4.1	Outline Dimensions
2.4.2	Power Requirements
2.4.3	Cooling Requirements
2.4.4	Physical Interfaces
2.4.5	MULTIBUS Interface Timing
2.4.6	Transceiver Interface Timing
2.4.7	iSBC 552 Jumper Intallations
2.4.7.1	Base Address Assignment Jumpers
2.4.7.2	Interrupt Jumpers
2.4.7.3	MULTIBUS Arbitration Jumpers
2.4.7.4	Firmware Jumpers
2.4.7.5	Memory Type and Memory Size Jumpers
2.4.7.6	Miscellaneous Jumpers
2.4.8	Additional Memory Installation
2.4.9	Transceiver Cable Installation
2.4.10	Installing the iSBC 552 Board on the MULTIBUS
2.4.11	Grounding

2.4.1 Outline Dimensions

Figure 2-1 shows the outline dimensions of the iSBC 552 board and locates some of the primary components of the board. The following components are located:

1. The 80186 16-Bit Microprocessor at U11.
2. The 82586 Local Communicator Controller at U25.
3. The 82501 Ethernet Serial Interface at U12.
4. The local memory array (U1 through U6, U18 through U23).
5. MULTIBUS connectors P1 and P2.
6. Ethernet connector J1.
7. Jumper stake pins starting at E1 and ending at E134 (not all E numbers are used).

2.4.2 Power Requirements

All operating power for the iSBC 552 board is supplied by the MULTIBUS interface. Power requirements are as follows:

Volts	Current (Max)	Power (Max)
+ 5.00V ± 5.0% +12.00V ± 5.0%	5.9Amps 0.5Amps	30.9W 6.3W

The iSBC 552 board can use an off-board uninterrupted power source (UPS), described in the Intel MULTIBUS specification. The two MULTIBUS signals, PFIN* (Power Fail Interrupt) and MPRO* (Memory Protect) are supported by the iSBC 552. PFIN* controls the 80186 processors NMI (Non-Maskable Interrupt) line and MPRO* is gated to the CEN (Chip Enable) input of the Local Bus Controller located at U13. MPRO* prevents access to the local memory when activated.

If a UPS is used, the +5V battery voltage plane must be disconnected from the standard +5V plane by removing the wires between E32 and E33 and between E39 and E40.

2.4.3 Cooling Requirements

When installed in its operating environment, adequate air circulation must be provided to prevent a temperature rise above 55°C (131.2°F).

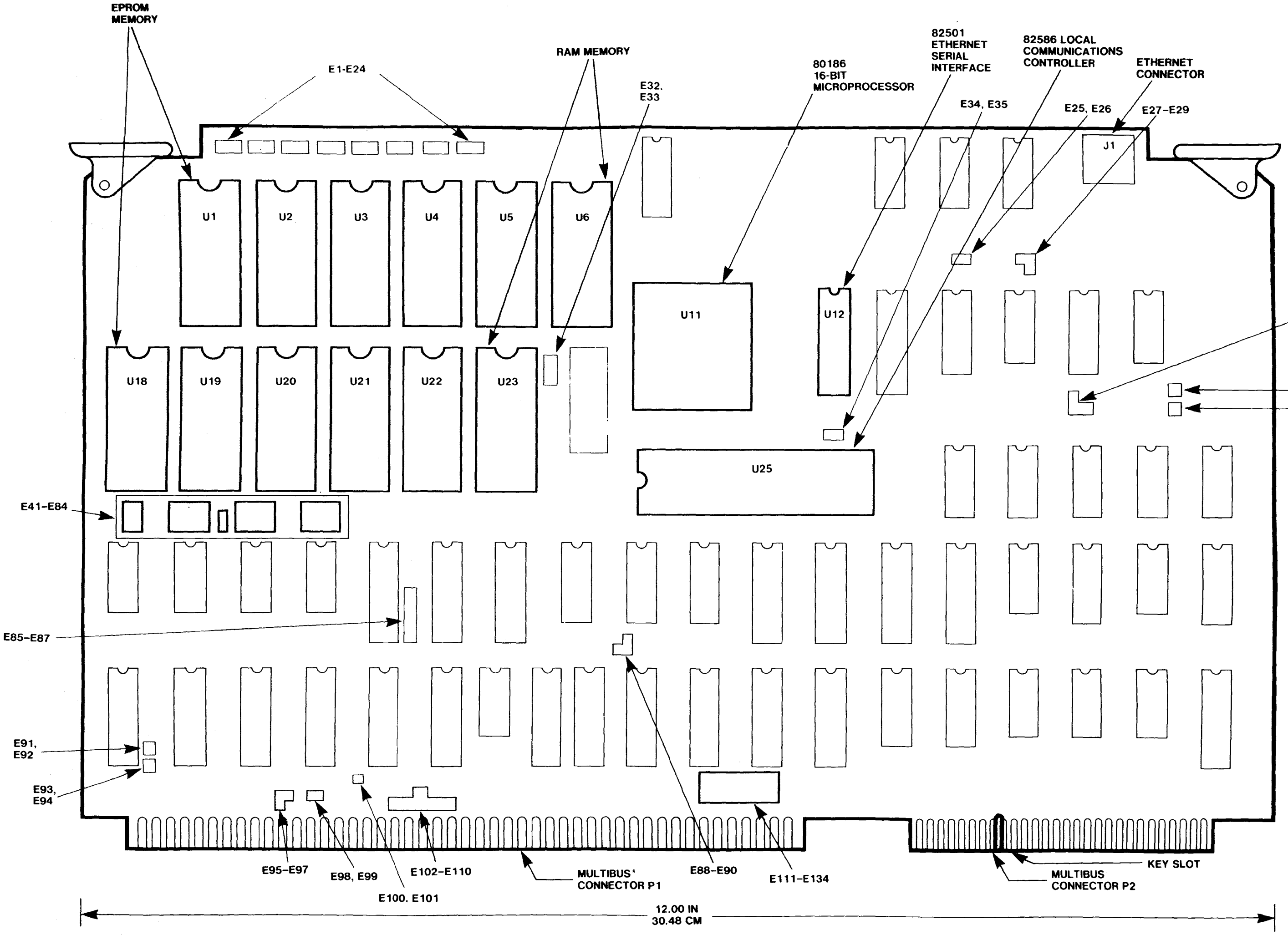


Figure 2-1. iSBC® 552 Board, Outline Drawing and Component Location

122141-2

2.4.4 Physical Interfaces

The iSBC 552 board connects to its system through three connectors: MULTIBUS connectors P1 and P2 and transceiver cable connector J1. Table 2-2 shows the pin assignments for MULTIBUS connectors P1 and P2, Table 2-3 lists the signal levels for the MULTIBUS signals, and Table 2-4 lists the compatible MULTIBUS connectors. (Table 3-1 describes MULTIBUS signal functions.)

The iSBC 552 board communicates with the Ethernet serial link through the Transceiver Cable, connected to J1. Table 2-5 shows the pin assignments for connector J1; Table 2-6 defines the signal levels. (Table 3-2 describes the signal functions.) Section 2.4.9 tells how to install the transceiver cable at connector J1.

Table 2-2. MULTIBUS® Connectors P1 and P2 Pin Assignments

P1	Mnemonic	Description	P1	Mnemonic	Description
1	GND	Signal Ground	2	GND	Signal Ground
3	+5V	+5 VDC	4	+5V	+5 VDC
5	+5V	+5 VDC	6	+5V	+5 VDC
7	+12V	+12 VDC	8	+12V	+12 VDC
9	-	Not Connected	10	-	Not Connected
11	GND	Signal Ground	12	GND	Signal Ground
13	BCLK*	Bus Clock	14	INIT*	Initialize
15	BPRN*	Bus Priority In	16	BPRO*	Bus Priority Out
17	BUSY*	Bus Busy	18	BREQ*	Bus Request
19	MRDC*	Memory Read Command	20	MWTC*	Memory Write Command
21	IORC*	I*O Read Command	22	IOWC*	I/O Write Command
23	XACK*	Transfer Acknowledge	24	INH1	Not Used
25	NC	Not Connected	26	INH2	Not Used
27	BHEN*	Bus High Enable	28	ADR10*	Address Bit 10
29	CBRQ*	Common Bus Request	30	ADR11*	Address Bit 11
31	CCLK*	Constant Clock	32	ADR12*	Address Bit 12
33	INTA	Not Used	34	ADR13*	Address Bit 13
35	INT6*	Interrupt Request 6	36	INT7*	Interrupt Request 7
37	INT4*	Interrupt Request 4	38	INT5*	Interrupt Request 5
39	INT2*	Interrupt Request 2	40	INT3*	Interrupt Request 3
41	INT0*	Interrupt Request 0	42	INT1*	Interrupt Request 1
43	ADRE*	Address Bit E	44	ADRF*	Address Bit F
45	ADRC*	Address Bit C	46	ADRD*	Address Bit D
47	ADRA*	Address Bit A	48	ADRB*	Address Bit B
49	ADR8*	Address Bit 8	50	ADR9*	Address Bit 9
51	ADR6*	Address Bit 6	52	ADR7*	Address Bit 7
53	ADR4*	Address Bit 4	54	ADR5*	Address Bit 5
55	ADR2*	Address Bit 2	56	ADR3*	Address Bit 3

Table 2-2. MULTIBUS® Connectors P1 and P2 Pin Assignments (Cont'd.)

P1	Mnemonic	Description	P1	Mnemonic	Description
57	ADR0*	Address Bit 0	58	ADR1*	Address Bit 1
59	DATE*	Data Bit E	60	DATF*	Data Bit F
61	DATC*	Data Bit C	62	DATD*	Data Bit D
63	DATA*	Data Bit A	64	DATB*	Data Bit B
65	DAT8*	Data Bit 8	66	DAT9*	Data Bit 9
67	DAT6*	Data Bit 6	68	DAT7*	Data Bit 7
69	DAT4*	Data Bit 4	70	DAT5*	Data Bit 5
71	DAT2*	Data Bit 2	72	DAT3*	Data Bit 3
73	DAT0*	Data Bit 0	74	DAT1*	Data Bit 1
75	GND	Signal Ground	76	GND	Signal Ground
77	--	Not Connected	78	--	Not Connected
79	-12V	-12 VDC	80	-12V	-12 VDC
81	+5V	+5 VDC	82	+5V	+5 VDC
83	+5V	+5 VDC	84	+5V	+5 VDC
85	GND	Signal Ground	86	GND	Signal Ground

P2	Mnemonic	Description	P2	Mnemonic	Description
1	GND	Signal Ground	2	GND	Signal Ground
3	+5 VB	+5 Volts Battery	4	+5 VB	+5 Volts Battery
5	--	Not Connected	6	--	Not Connected
7	--	Not Connected	8	--	Not Connected
9	--	Not Connected	10	--	Not Connected
11	--	Not Connected	12	--	Not Connected
13	--	Not Connected	14	--	Not Connected
15	--	Not Connected	16	--	Not Connected
17	--	Not Connected	18	--	Not Connected
19	PFIN*	Power Fail Interrupt	20	MPRO*	Memory Protect
21	GND	Signal Ground	22	GND	Signal Ground
23	--	Not Connected	24	--	Not Connected
25	--	Not Connected	26	--	Not Connected
27	--	Not Connected	28	--	Not connected
29	--	Not Connected	30	--	Not Connected
31	--	Not Connected	32	--	Not Connected
33	--	Not Connected	34	--	Not Connected
35	--	Not Connected	36	--	Not Connected
37	--	Not Connected	38	AUX RESET*	Auxiliary Reset
39	--	Not Connected	40	--	Not Connected
41	--	Not Connected	42	--	Not Connected
43	--	Not Connected	44	--	Not Connected
45	--	Not Connected	46	--	Not Connected
47	--	Not Connected	48	--	Not Connected
49	--	Not Connected	50	--	Not Connected
51	--	Not Connected	52	--	Not Connected
53	--	Not Connected	54	--	Not Connected
55	ADR16*	Address Bit 16	56	ADR17*	Address Bit 17
57	ADR14*	Address Bit 14	58	ADR15*	Address Bit 15
59	--	Not Connected	60	--	Not Connected

Table 2-3. MULTIBUS® Interface (P1 and P2) Signal Levels

Bus Signals	I_{OL} MIN(ma)	I_{OH} MIN(μa)	I_{IL} Max(ma)	I_{IH} Max(μa)
DAT0* - DATF* (16 lines)	16.0	-2000	-0.8	125
ADR0*-ADRB*	16.0	-2000	-0.8	125
BHEN* (21 lines)				
MRDC*, MWTC*	32.0	-2000	-2.0	125
IOWC*	32.0	-2000	-2.1	125
IORC*	32.0	-2000	-2.0	125
XACK*	32.0	-2000	-2.0	125
BCLK*	48.0	-3000	-2.0	125
BREQ*	10.0	- 200	2.0	50
BPRO*	3.2	- 200	-3.2	100
BPRN*	3.2	- 200	-3.2	100
BUSY*, CBRQ*	20.0	–	-2.0	60
INIT*	32.0	–	-2.0	60
CCLK*	48.0	-3000	-2.0	125
INTO*-INT7* (8 lines)	16.0	–	-1.6	40

Table 2-4. Compatible MULTIBUS® Connectors

Function	# of Pins	Centers Inches	Connector Type	Vendor	Vendor #	Intel #
MULTIBUS Connector (P1)	43/86	0.156	Soldered	VIKING ELFAB	2KH43*9AMK12 BS1562D43PBB	102247-001
MULTIBUS Connector (P1)	43/86	0.156	Wirewrap See Notes 1, 2	ELFAB ELDAC ELFAB ELDAC	BW1562D43PBB 3370860540201 BW1562A43PBB 337086540202	102248-001 102273-001[3]

Table 2-4. Compatible MULTIBUS® Connectors (Cont'd.)

Function	# of Pins	Centers Inches	Connector Type	Vendor	Vendor #	Intel #
Auxiliary Connector (P2)	30/60	0.1	Soldered[1]	ELFAB EDAC	BS1020A30PBB 345060524802	102238-001
Auxiliary Connector (P2)	30/60	0.1	Wirewrap See Notes 1,2	TI VIKING EDAC ELFAB	H421121-30 3KH30*9JNK 345060540201 BW1020530PBB	102241-001

Notes:

1. Connector heights are not guaranteed to conform to Intel packaging equipment.
2. Wirewrap pin lengths are not guaranteed to conform to Intel packaging equipment.
3. Connector has mounting ears that have 0.128 in. mounting holes.

Table 2-5. Transceiver Interface Connector J1 Pin Assignments

Pin	Mnemonic	Description	Pin	Mnemonic	Description
1	TRMT (+)	Transmit (+)	2	TRMT (-)	Transmit (-)
3	RCV (+)	Receive (+)	4	RCV (-)	Receive (-)
5	CLSN (+)	Collision Presence (+)	6	CLSN (-)	Collision Presence (-)
7	GND	Power Return	8	GND	Power Return
9	+12V	Power	12	+12V	Power

Table 2-6. Transceiver Interface Signal Levels

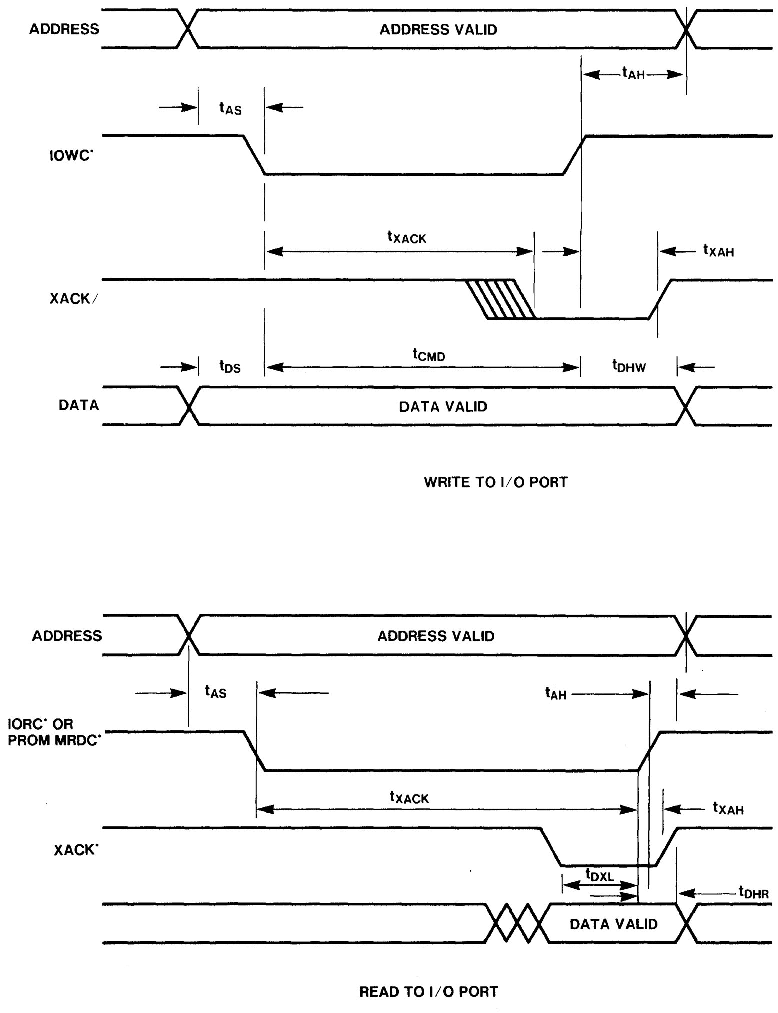
Mnemonic	Level
TRMT (+), TRMT (-) RCV (+), RCV (-) CLSN (+), CLSN (-)	All signals are Series 10,000 ECL compatible

2.4.5 MULTIBUS® Interface Timing

Figure 2-2 shows the MULTIBUS interface timing. Table 2-7 defines the timing parameters shown in Figure 2-2.

Table 2-7. MULTIBUS® Timing Parameters

Symbol	Parameter	Time (in Nanoseconds)	
		Min	Max
t_{AS}	Address Setup Time	50	
t_{AH}	Address Hold Time	50	
t_{ID}	Inhibit Delay	-	100
t_{XACK}	Acknowledge Time	1.5	8µs
t_{XAH}	Acknowledge Hold Time	0	65
t_{DS}	Write Data Setup Time	50	–
t_{CMD}	Command Pulse Width	100	–
t_{DHR}	Read Data Hold Time	0	65
t_{DHW}	Write Data Hold Time	50	–
t_{DXL}	Read Data Set Up Time to XACK	0	–

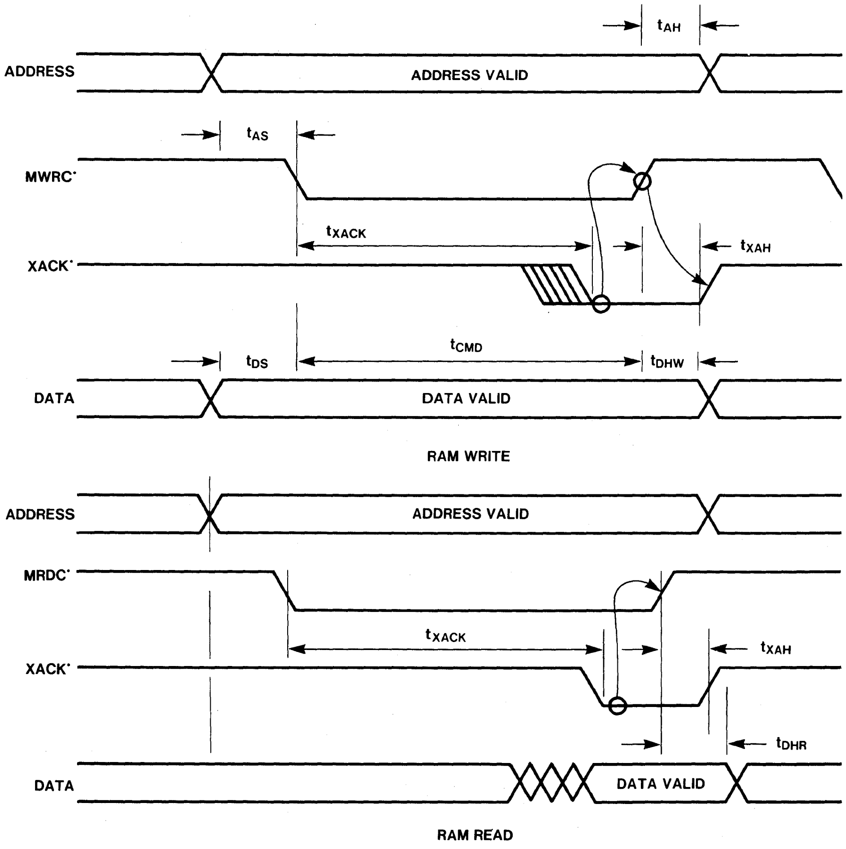


WRITE TO I/O PORT

READ TO I/O PORT

Figure 2-2. MULTIBUS® Timing Diagram (1 of 2)

122141-3a



RAM WRITE

RAM READ

Figure 2-2. MULTIBUS® Timing Diagram (2 of 2)

122141-3b

2.4.6 Transceiver Interface Timing

Table 2-8 defines the Ethernet transceiver timing parameters shown in Figure 2-3.

Table 2-8. Transceiver Interface Timing Parameters

Symbol	Parameter	Time in Nanoseconds	
		Min	Max
t_{TPCB}	Bit Cell Center to Bit Cell Boundary of Transmit Pair Data	49.5	50.5
t_{TPCC}	Bit Cell Center to Bit Cell Center of Transmit Pair Data	99.5	100.5
t_{TPF}	Transmit Pair Data Fall Time	1.0	5.0
t_{TPR}	Transmit Pair Data Rise Time	1.0	5.0
t_{RPW}	Receive Pair Signal Pulse Width of First Negative Pulse	30.0	50.0
t_{RPR}	Receive Pair Signal Rise Time at ±0.2V	–	15.0
t_{RPF}	Receive Pair Signal Fall Time at ±0.2V	–	15.0
t_{RPC}	Receive Pair Signal Bit Cell Time	99.0	101.0
t_{RPCB}	Receive Pair Signal Bit Cell Center to Bit Cell Boundary, allowing for timing distortion		
	In Preamble	35.0	65.0
	In Data	30.0	70.0
t_{RPCC}	Receive Pair Signal Bit Cell Center to Bit Cell Center, allowing for timing distortion		
	In Preamble	70.0	130.0
	In Data	60.0	140.0
t_{RPZ1}	Receive Pair Signal Return to Zero Level from Last Valid Positive Transition	250.00	5µsec
t_{RI}	Receive Idle Time Before the Next Reception Can Begin		8µsec
t_{CPH}/t_{CPL}	Collision Pair Signal Transition Time	40.0	–
t_{CPW}	Collision Pair Signal Pulse Width of First Negative Pulse (at -0.25V differential signal)	15.0	–
t_{CPC}	Collision Pair Signal Cycle Time	86.0	118.0
t_{CPR}	Collision Pair Signal Rise Time at ±0.2V	–	15.0
t_{CPF}	Collision Pair Signal Fall Time at ±0.2V	–	15.0

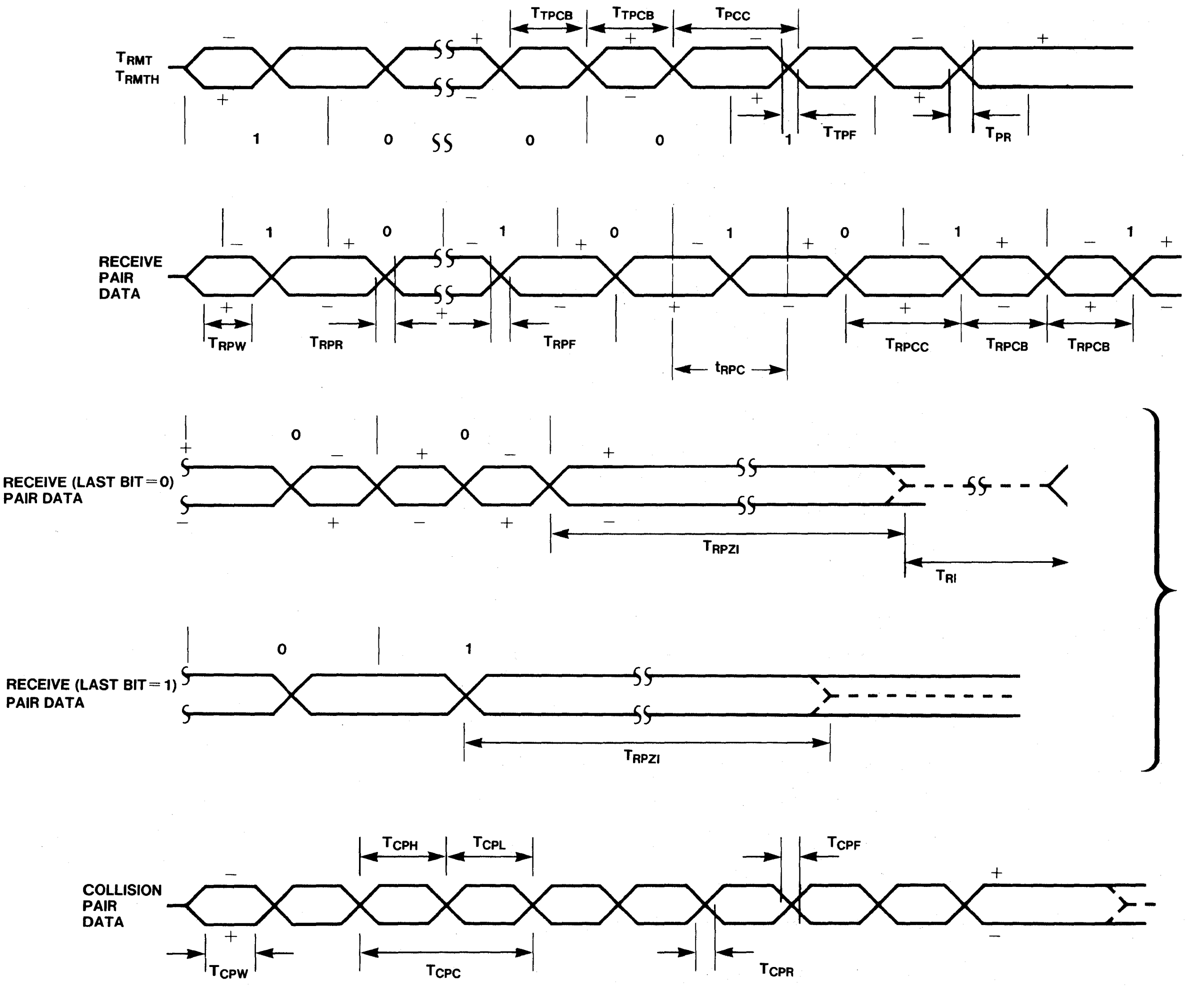


Figure 2-3. Transceiver Interface Timing Diagram

122141-4

2.4.7 iSBC® 552 Jumper Installations

The iSBC 552 board can be configured for various applications. The board contains a number of stake pins which can be jumpered together for the various configurations. Sections 2.4.7.1 through 2.4.7.5 discuss the jumpering of the iSBC 552 board.

2.4.7.1 Base Address Assignment Jumpers

As described in Chapter 4 of this manual, the iSBC 552 board occupies four adjacent 8-bit write-only ports in the MULTIBUS I/O space. The base address for these ports is jumper-selectable. For an 8-bit I/O, the base address can be located on any 4-byte boundary between 00(H) and FC(H). For a 16-bit I/O, the base address can be located on any 4-byte boundary, from 0000(H) to FFFC(H). The desired address, keeping in mind the 4 byte boundary can be set by installing the jumpers shown in Table 2-9. Table 2-10 shows 14 examples (seven for 8-bit transfers, seven for 16-bit transfers) of how the jumpers are installed for the addresses designated in the table. The default configurations are 8-bit I/O with a base address of A8(H).

Table 2-9. Port Base Address Jumpers

Jumpers	Function
E70 to E55*	Sets Bit 2 in Port Base Address low for 8- and 16-bit data transfers. See Table 2-10.
E41 to E55	Sets Bit 2 in Port Base Address high for 8- and 16-bit data transfers. See Table 2-10.
E71 to E56	Sets Bit 3 in Port Base Address low for 8- and 16-bit data transfers. See Table 2-10.
E42 to E56*	Sets Bit 3 in Port Base Address high for 8- and 16-bit data transfers. See Table 2-10.
E72 to E57*	Sets Bit 4 in Port Base Address low for 8- and 16-bit data transfers. See Table 2-10.
E43 to E57	Sets Bit 4 in Port Base Address high for 8- and 16-bit data transfers. See Table 2-10.
E73 to E58	Sets Bit 5 in Port Base Address low for 8- and 16-bit data transfers. See Table 2-10.
E44 to E58*	Set Bit 5 in Port Base Address high for 8- and 16-bit data transfers. See Table 2-10.
E74 to E59*	Set Bit 6 in Port Base Address low for 8- and 16-bit data transfers. See Table 2-10.

Table 2-9. Port Base Address Jumpers (Cont'd.)

Jumpers	Function
E45 to E59	Sets Bit 6 in Port Base Address high for 8- and 16-bit data transfers. See Table 2-10.
E75 to E60	Sets Bit 7 in Port Base Address low for 8- and 16-bit data transfers. See Table 2-10.
E46 to E60*	Sets Bit 7 in Port Base Address high for 8- and 16-bit data transfers. See Table 2-10.
For 16-Bit I/O Addressing (see Note 1)	
E77 to E62	Sets Bit 8 in Port Base Address low for 16-bit data transfers. See Table 2-10.
E47 to E62	Sets Bit 8 in Port Base Address high for 16-bit data transfers. See Table 2-10.
E78 to E63	Sets Bit 9 in Port Base Address low for 16-bit data transfers. See Table 2-10.
E48 to E63	Sets Bit 9 in Port Base Address high for 16-bit data transfers. See Table 2-10.
E79 to E64	Sets Bit 10 in Port Base Address low for 16-bit data transfers. See Table 2-10.
E49 to E64	Sets Bit 10 in Port Base Address high for 16-bit data transfers. See Table 2-10.
E80 to E65	Set Bit 11 in Port Base Address low for 16-bit data transfers. See Table 2-10.
E50 to E65	Sets Bit 11 in Port Base Address high for 16-bit data transfers. See Table 2-10.
E81 to E66	Sets Bit 12 in Port Base Address low for 16-bit data transfers. See Table 2-10.
E51 to E66	Sets Bit 12 in Port Base Address high for 16-bit data transfers. See Table 2-10.
E82 to E67	Sets Bit 13 in Port Base Address low for 16-bit data transfers. See Table 2-10.
E52 to E67	Sets Bit 13 in Port Base Address high for 16-bit data transfers. See Table 2-10.
E83 to E68	Sets Bit 14 in Port Base Address low for 16-bit data transfers. See Table 2-10.
E53 to E68	Sets Bit 14 in Port Base Address high for 16-bit data transfers. See Table 2-10.
E84 to E69	Sets Bit 15 in Port Base Address low for 16-bit data transfers. See Table 2-10.

Table 2-9. Port Base Address Jumpers (Cont'd.)

Jumpers	Function
E54 to E69	Sets Bit 15 in Port Base Address high for 16-bit data transfers. See Table 2-10.

Notes:

1. Bits 8 through 16 must be recognized for 16-bit I/O addressing. For these bits to be recognized, pin E61 must be connected to E76. For 8-bit I/O addressing, this jumper is removed.

* Indicates default connection.

Table 2-10. Port Base Address Selection Examples

Address Bit	Jumper	Base Address						
		4(H)	8(H)	C(H)	A8(H)	F4(H)	F8(H)	FC(H)
		8 Bit I/O Transfer						
2	E41 to E55 (Active)	I	-	I	-	I	-	I
	E70 to E55 (Inactive)	-	I	-	I	-	I	-
3	E42 to E56 (Active)	-	I	I	I	-	I	I
	E71 to E56 (Inactive)	I	-	-	-	I	-	-
4	E43 to E57 (Active)	-	-	-	-	I	I	I
	E72 to E57 (Inactive)	I	I	I	I	-	-	-
5	E44 to E58 (Active)	-	-	-	I	I	I	I
	E73 to E58 (Inactive)	I	I	I	-	-	-	-
6	E45 to E59 (Active)	-	-	-	-	I	I	I
	E74 to E59 (Inactive)	I	I	I	I	-	-	-
7	E46 to E60 (Active)	-	-	-	I	I	I	I
	E75 to E60 (Inactive)	I	I	I	-	-	-	-

Note: I = Installed, - = Not Installed

Table 2-10. Port Base Address Selection Examples (Cont'd.)

Address Bit	Jumper	Base Address						
		4(H)	A8(H)	258(H)	A23C(H)	D5AC(H)	ED14(H)	FFF0(H)
		16 Bit I/O Transfer						
2	E41 to E55 (Active)	I	-	-	I	I	I	-
	E70 to E55 (Inactive)	-	I	I	-	-	-	I
3	E42 to E56 (Active)	-	I	I	I	I	-	-
	E71 to E56 (Inactive)	I	-	-	-	-	I	I
4	E43 to E57 (Active)	-	-	I	I	-	I	I
	E72 to E57 (Inactive)	I	I	-	-	I	-	-
5	E44 to E58 (Active)	-	I	-	I	I	-	I
	E73 to E58 (Inactive)	I	-	I	-	-	I	-
6	E45 to E59 (Active)	-	-	I	-	-	-	I
	E74 to E59 (Inactive)	I	I	-	I	I	I	-
7	E46 to E60 (Active)	-	I	-	-	I	-	I
	E75 to E60 (Inactive)	I	-	I	I	-	I	-
8	E47 to E62 (Active)	-	-	-	-	I	I	I
	E77 to E62 (Inactive)	I	I	I	I	-	-	-
9	E48 to E63 (Active)	-	-	I	I	-	-	I
	E78 to E63 (Inactive)	I	I	-	-	I	I	-
10	E49 to E64 (Active)	-	-	-	-	I	I	I
	E79 to E64 (Inactive)	I	I	I	I	-	-	-
11	E50 to E65 (Active)	-	-	-	-	-	I	I
	E80 to E65 (Inactive)	I	I	I	I	I	-	-
12	E51 to E66 (Active)	-	-	-	-	I	-	I
	E81 to E66 (Inactive)	I	I	I	I	-	I	-
13	E52 to E67 (Active)	-	-	-	I	-	I	I
	E82 to E67 (Inactive)	I	I	I	-	I	-	-
14	E53 to E68 (Active)	-	-	-	-	I	I	I
	E83 to E68 (Inactive)	I	I	I	I	-	-	-
15	E54 to E69 (Active)	-	-	-	I	I	I	I
	E84 to E69 (Inactive)	I	I	I	-	-	-	-

Note: I = Installed, - = Not Installed

2.4.7.2 Interrupt Jumpers

The iSBC 552 board can generate an interrupt on any one of eight MULTIBUS interrupt lines. Table 2-11 lists the interrupt jumper used to select the appropriate lines. Section 3.5.3 describes the interrupt sequence.

Table 2-11. Interrupt Jumpers

Jumpers	Function
E102 to E110	Selects INT7 to the MULTIBUS Interface.
E103 to E110	Selects INT6 to the MULTIBUS Interface.
E104 to E110*	Selects INT5 to the MULTIBUS Interface.
E105 to E110	Selects INT4 to the MULTIBUS Interface.
E106 to E110	Selects INT3 to the MULTIBUS Interface.
E107 to E110	Selects INT2 to the MULTIBUS Interface.
E108 to E110	Selects INT1 to the MULTIBUS Interface.
E109 to E110	Selects INT0 to the MULTIBUS Interface.

Note: * Indicates default connection

2.4.7.3 MULTIBUS® Arbitration Jumpers

Connection of the MULTIBUS arbitration signals CBRQ* (Common Bus Request) and BPRO* (Bus Priority Out) are jumper selectable using the MULTIBUS arbitration jumper shown in Table 2-12. After the iSBC 552 board acquires the MULTIBUS interface it may hold it until the on-board processor reaches a wait or idle state if the jumper between E91 and E92 is installed. If this jumper is not installed and CBRQ* is active, the iSBC 552 board surrenders the MULTIBUS at the end of the current bus cycle.

Table 2-12. MULTIBUS® Arbitration Jumpers

Jumpers	Function
E 96 to E 95*	Connects CBRQ* (Common Bus Request) to the MULTIBUS Interface from the 8289 Bus Arbiter (on the iSBC 552 board).
E 96 to E 97	Removes CBRQ from the MULTIBUS Interface and grounds the CBRQ* pin on the 8289 Bus Arbiter.
E 98 to E 99*	Connects BRPO* (Bus Priority Out) to the MULTIBUS Interface from the 8289 Bus Arbiter.
E 92 to E 91*	Connects ANYRQST (pin 14) of the 8289 Bus Arbiter to ground.

Note: * Indicates default connections

2.4.7.4 Firmware Jumpers

Three SCP registers located at U41, U42 and U60 are the means by which the host communicates to the iSBC 552 board. The SCP high register (U42) and the SCP mid register (U41) have all eight inputs connected directly to the least significant half of the MULTIBUS. The low SCP register (U60) has each of its eight inputs jumpered to a logic high, a logic low or to the lower half of the MULTIBUS data bus with the jumpers shown in Table 2-13. These jumpers allow the user firmware various options. When using these jumper options on the low SCB register the MULTIBUS must perform a write cycle to that port in order to latch the jumpered inputs to the low SCP register. Section 3.2 further describes the SCP registers.

Table 2-13. Firmware Jumpers

Jumpers	Function
E126 to E134	Ties SCP0 (Bit 0) to ground.
E126 to E118	Ties SCP0 (Bit 0) to MULTIBUS data bus.
E125 to E133	Ties SCP1 (Bit 1) to ground.
E125 to E117	Ties SCP1 (Bit 1) to MULTIBUS data bus.
E124 to E132	Ties SCP2 (Bit 2) to ground.
E124 to E116	Ties SCP2 (Bit 2) to MULTIBUS data bus.
E123 to E131	Ties SCP3 (Bit 3) to ground.
E123 to E115	Ties SCP3 (Bit 3) to MULTIBUS data bus.
E122 to E130	Ties SCP4 (Bit 4) to ground.
E122 to E114	Ties SCP4 (Bit 4) to MULTIBUS data bus.
E121 to E129	Ties SCP5 (Bit 5) to ground.
E121 to E113	Ties SCP5 (Bit 5) to MULTIBUS data bus.
E120 to E128	Ties SCP6 (Bit 6) to ground.
E120 to E112	Ties SCP6 (Bit 6) to MULTIBUS data bus.
E119 to E127	Ties SCP7 (Bit 7) to ground.
E119 to E111	Ties SCP7 (Bit 7) to MULTIBUS data bus.

Note: No connection = a high, the default condition.

2.4.7.5 Memory Type and Memory Size Jumpers

The memory type and memory size jumpers are discussed in Section 2.4.8.

2.4.7.6 Miscellaneous Jumpers

Table 2-14 lists and defines the functions of 11 pairs of miscellaneous jumpers.

Table 2-14. Miscellaneous Jumpers

Jumpers	Function
MULTIBUS Master Jumpers	
E 93 to E 94	When the iSBC 552 board is a MULTIBUS master, this jumper installation allows the 10 MHz TRANSMIT CLOCK of the 82501 Ethernet Serial Interface (on the iSBC 552 board) to become the MULTIBUS BCLK signal. BCLK is used to synchronize bus contention logic.
E 100 to E101	When the iSBC 552 board is a MULTIBUS master, this jumper installation allows the 10 MHz TRANSMIT CLOCK of the 82501 Ethernet Serial Interface to become the MULTIBUS CCLK signal. CCLK* is BCLK inverted.
Battery Backup Jumpers	
E 32 to E 33* and E 39 to E 40*	These jumpers are installed in the as-delivered configuration (default) of the iSBC 552 board. Both jumpers must be removed if the iSBC 552 board is used in a MULTIBUS battery backup configured system.
Factory Test Jumpers	
E 30 to E 31* E 25 to E 26* E 34 to E 35*	These jumpers are used for factory testing. They are installed by the factory and should not be removed by the user.
Wait State Jumpers	
E 27 to E 28	Allows the 80186 microprocessor on the iSBC 552 board to run at zero wait states when accessing RAMs.
E 28 to E 29*	Causes the 80186 microprocessor on the iSBC 552 board to generate one wait state when accessing RAMs.
Timeout Jumper	
E 25 to E 26*	When this jumper is installed a ready to the 80186 processor will be generated after 5 to 10 ns (if no ready has been received during the present cycle).
Timeout Interrupt Jumper	
E 36 to E 37	If installed, this jumper causes an interrupt (INT2) to the 80186 processor whenever a timeout occurs.
E 37 to E 38*	Ground interrupt (INT2) to the 80186 when timeout interrupt option is not used.

Note: * Indicates default connection

2.4.8 Additional Memory Installation

The iSBC 552 board local memory array consists of six pairs of 28-pin sockets, U1/U18, U2/U19, U3/U20, U4/U21, U5/U22 and U6/U23. Socket pair U1/U18 is used only for EPROMs. Socket pair U6/U12 can be used only for RAMs. The remaining four socket pairs can be used for either EPROMs or RAMs as desired, by installing several jumpers.

The memory array can accept 8K x 8 iRAMs (Intel 2186-30 or equivalents); and either 64K (Intel 2764-2 or equivalents) or 128K (Intel 27128-2 or equivalents) EPROMs. Jumpers must be installed depending on the type of memory device that occupies a particular socket pair and the capacity of the device. Capacities may vary between RAMs and PROMs. Table 2-15 lists the jumpers. Figure 2-4 shows the memory array.

Table 2-15. Memory Type and Memory Size Jumpers

Memory Type Jumpers		
Socket Pair	for PROMs	for RAMs
U5/U22	E20 to E21 E23 to E22	E20 to E19 E23 to E24
U4/U21	E14 to E15 E16 to E17	E14 to E13 E17 to E18
U3/U20	E 8 to E 9 E10 to E11	E 8 to E 7 E11 to E12
U2/U19	E 2 to E 3 E 4 to E 5	E 2 to E 1 E 5 to E 6
Memory Size Jumpers		
PROM Size	RAM Size	Jumpers
64K	64K	E88 to E89, E86 to E85*
128K	64K	E90 to E89, E86 to E85
128K	128K	E86 to E87 No connection for E88, E89 and E90

Note: * Indicates default condition

The first RAMs are installed in socket pair U6/U23. The first PROMs are installed in socket pair U1/U18. Additional RAMs or EPROMs are installed in the memory expansion sockets (see Figure 2-4). If additional RAMs are installed they should be installed in the following order:

First Additional Pair	U5/U22
Second Additional Pair	U4/U21
Third Additional Pair	U3/U20
Fourth Additional Pair	U2/U19

If additional EPROMs are installed they should be installed in the following order:

First Additional Pair	U2/U19
Second Additional Pair	U3/U20
Third Additional Pair	U4/U21
Fourth Additional Pair	U5/U22

CAUTION

When installing RAM/iRAM devices in a low humidity environment, always ground yourself before handling the devices. This precaution ensures a static charge buildup is not dissipated through or around the devices.

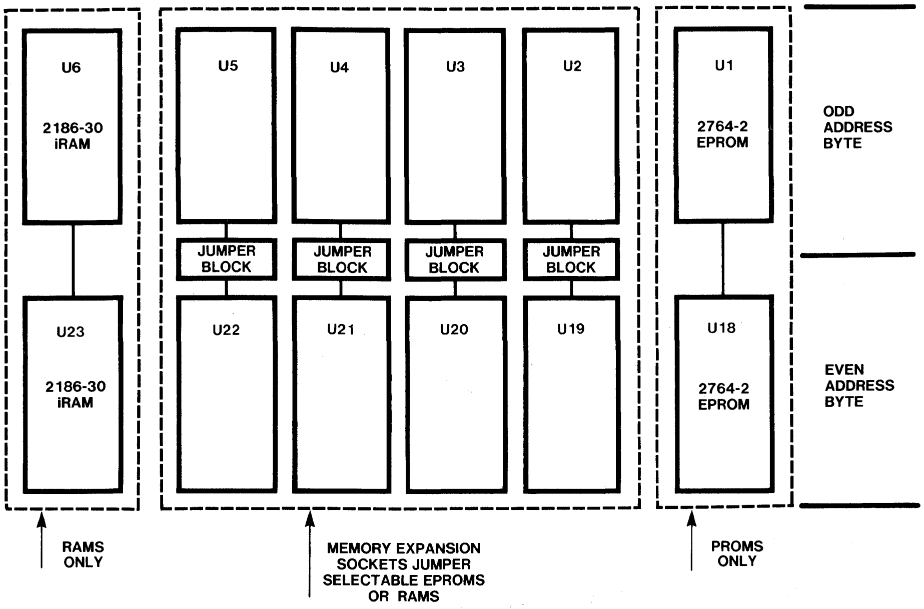


Figure 2-4. iSBC® 552 Board Local Memory Array

2.4.9 Transceiver Cable Installation

A user-furnished cable is required to connect the iSBC 552 board to the Ethernet. Figure 2-5 shows a typical cable assembly. Figure 2-6 shows how the iSBC 552 can be connected and grounded.

The mating connector for the iSBC 552 board transceiver interface is an AMP 87631-5. The internal transceiver cable should be mounted to the chassis connector panel using the sliding lock post (Cinch D53018) called out in the Ethernet specification (see Figure 2-6).

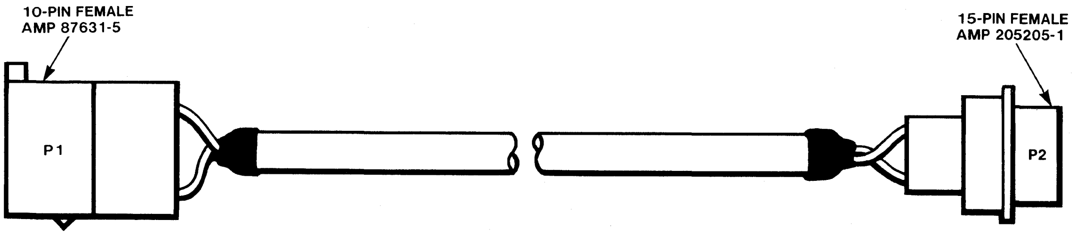


Figure 2-5. Ethernet Internal Transceiver Cable

122136-57

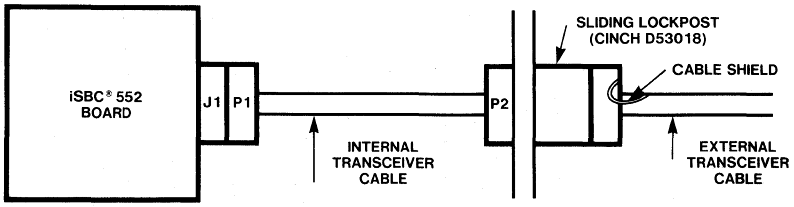


Figure 2-6. The iSBC® 552 Transceiver Grounding

122141-6

2.4.10 Installing the iSBC® 552 Board on the MULTIBUS®

The iSBC 552 board can be installed or removed from a system only after power-down. Ethernet transceivers are designed to power-up and power-down without introducing noise on the coaxial cable; therefore, transceivers may be connected to or disconnected from the iSBC 552 board at any time.

The iSBC 552 board can be installed in any standard MULTIBUS chassis. The board includes a large number of stake pins which allow the installation of a wide variety of jumpers. Some of these jumpers are default jumpers, those installed by the factory, and these should not be removed. Table 2-16 lists these jumpers.

Table 2-16. Default Jumpers

Jumpers	Reference Table
E25 to E26	See Table 2-14
E28 to E29	See Table 2-14
E30 to E31	See Table 2-14
E32 to E33	See Table 2-14
E34 to E35	See Table 2-14
E38 to E39	See Table 2-14
E42 to E56	See Table 2-9
E44 to E58	See Table 2-9
E46 to E60	See Table 2-9
E55 to E70	See Table 2-9
E57 to E72	See Table 2-9
E59 to E74	See Table 2-9
E95 to E96	See Table 2-12
E98 to E99	See Table 2-12
E104 to E110	See Table 2-11

The remaining jumpers are installed by the user to suit unique user iSBC 552 board configurations before the board is installed in a chassis. The jumper options available to the user for configuration of the board are shown below:

Options	See Section	See Table
Port base address jumpers	2.4.7.1	2-9,2-10
Interrupt jumpers	2.4.7.2	2-11
MULTIBUS arbitration jumpers	2.4.7.3	2-12
Firmware jumpers	2.4.7.4	2-13
Memory type/size jumpers	2.4.7.5	2-15
Miscellaneous jumpers	2.4.7.5	2-14

After installing the required jumpers the iSBC 552 board can be installed in the MULTIBUS chassis.

After the board is installed in the chassis, install the user-supplied internal transceiver as described in Section 2.4.9. Proper grounding of the installation should be verified as specified in Section 2.4.11. This completes the installation.

2.4.11 Grounding

The iSBC 552 transceiver interface has no chassis ground connection, only a signal ground connection. Reliable operation and Ethernet compatibility require that the shield of the external interface cable attached to the transceiver be connected to that station chassis ground. This connection can be made when using the internal interface cable described in Section 2.4.9 by ensuring that the shield of the external transceiver cable (see Figure 2-6) is electrically connected to the external transceiver cable connector and the slide lock mechanism. The slide lock on the station's locking post must be securely closed during operation.

CHAPTER 3.
OPERATION

3.1 INTRODUCTION

This chapter describes the operating characteristics of the iSBC 552 board. It includes a functional operating description of the board, a block diagram (Figure 3-1), an explanation of the operating cycles, and a description of the input and output signals of the board.

3.2 FUNCTIONAL DESCRIPTION

The main processor on the iSBC 552 board is an 80186 16-bit microprocessor which is software compatible with the 8086 microprocessor. The iSBC 552 application does not use all features of the 80186. A description of the features being used is presented below.

Because the 80186 processor is operated in the maximum mode, two external Bus Controllers are used. The 8288 Bus Controller U50 supplies MULTIBUS control signals, and another controller, U13, supplies local bus control signals.

The asynchronous ready logic of the 80186 is used and the chip select logic partially used.

The clock generator of the 80186 is used in the frequency mode. The DMA controller is not used. The interrupt controller is used in the non-RMX fully nested mode. Control information and data is transferred from the master processor board (Host) to the iSBC 552 board via the MULTIBUS common memory. The iSBC 552 has 256K bytes of local memory space that is mapped into the MULTIBUS memory space. By moving this 256K window around the iSBC 552 can access the full 16M bytes of MULTIBUS memory. The 80186 can also perform I/O on the MULTIBUS throughout the entire 64K-byte space.

The 82586 Local Communications Controller (LCC) and the 82501 Ethernet Serial Interface (ESI) supply the majority of the iSBC 552 board's Ethernet communications functions. The 82501 performs Manchester encoding/decoding of the transmitted/received frames, and provides the electrical interface to the transceiver cable.

The 82586 LCC runs as a coprocessor with the 80186 micropocessor and provides the intelligence for implementing the Ethernet data link functions.

The multiplexed AD bus ties together the two processors (the 82586 and the 80186), and the rest of the board. The AD bus is latched to provide both the local address bus (LADR) using ALE* and the MULTIBUS address bus (ADR) using MBALE. The local address bus signals are decoded to generate local chip selects. The AD bus is also buffered with bidirectional drivers to provide the local data bus (LDAT) and the MULTIBUS data bus (DAT).

Six pairs of 28-pin byte-wide sockets are provided for the local memory array. The upper pair of sockets (Ul/U18) is used only for PROMs and lower pair (U6/U23) is used only for RAMS. The four remaining socket pairs are jumper-selectable for either EPROMs or RAMs. The sockets are paired to obtain the full 16 bits of data. In each pair one device contains the high or odd byte, the other the low or even byte. None of on-board memory is available as a MULTIBUS resource.

The 80186/82586 interface is through a memory structure residing in the RAM portion of the local memory. The memory structure includes serial link data and control instructions for the 82586. The PROM portion is where the 80186 firmware resides.

The Ethernet station address PROM (U38) resides at Programmable Base Address (PBA) +8O(H) through PBA + BE(H). This PROM has 32 bytes. The first 6 bytes are the station address; the next 10 bytes are zero, and the next 2 are the CRC (Cyclic Redundundcy Check) of the first 16 bytes and are used for test purposes to verify PROM integrity. Because the station address PROM is an 8-bit device on a 16-bit data bus, the data appears on even addresses.

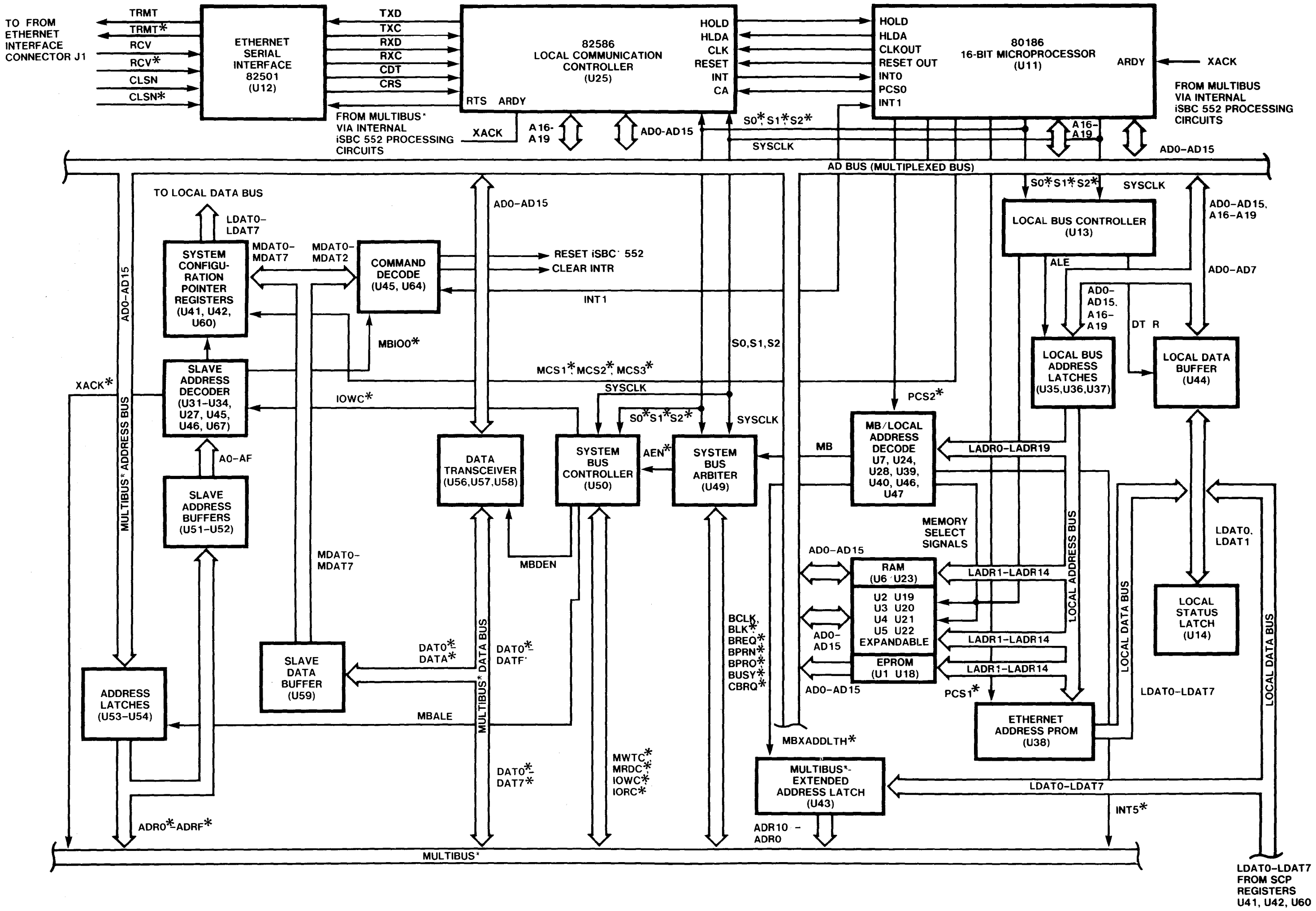


Figure 3-1. iSBC® 552 Ethernet Communications Controller Block Diagram

122141-7

NOTE

The Programable Base Address is set up by programming the 80186. See the iAPX 186 Data Sheet for more details.

The iSBC 552 board functions as a slave in the MULTIBUS I/O space. The MULTIBUS address lines are buffered at U51 and U52 (see Figure 3-1) and then decoded in either 8- or 16-bit mode in the slave mode decoder (U31 -U34). The lower data byte is also buffered from the MULTIBUS in slave mode.

The flag-byte circuitry is a means of communication between the iSBC 552 boards 80186 processor and the off-board processor. The 80186 generates a jumper selectable interrupt to the MULTIBUS, when it needs to gain the attention of the host.

Through I/O writes to the iSBC 552 slave flag byte port, the MULTIBUS may reset its own interrupt, reset the iSBC 552 board, or generate an interrupt to the iSBC 552 board. The slave flag byte port is located at the MULTIBUS I/O slave address + 0. The data bits are defined as follows:

o Data Bit 0	= Reset iSBC 552
o Data Bit 1	= Channel attention (interrupt iSBC 552)
o Data Bit 2	= Reset MULTIBUS interrupt
o Data Bits 3 - 7	= Don't care

A 4-bit latch (U14) is used as a status latch on the iSBC 552 board. It is a write only latch located in the local memory map at PBA + 100(H). A Light Emitting Diode (LED), a loopback and two spare bits are connected to this latch. Data Bit 0 controls the on-board LED (bit 0 low, LED on). Data Bit 1 controls the loopback signal to the 82501 ESI (bit 1 low, loopback signal active).

The System Configuration Pointer (SCP) registers are the means by which the system host communicates with the iSBC 552 board. The SCP registers, three 74S373 octal-D-type latches, are located at U41, U42, and U60. These latches may be written only from the MULTIBUS and read only on the local data bus. The mid and high registers have all eight inputs connected to the least significant half of the MULTIBUS data bus whereas the low register has jumpered inputs to allow user firmware-strapping options. See Table 2-13. The 80186 reads these registers by accessing MCS 1, 2, or 3 for SCP low, mid or high, respectively. The mapping of these registers into the MULTIBUS I/O address space is described in Chapter 4.

3.3 iSBC® 552 OPERATING CYCLES

The iSBC 552 board has seven primary operating cycles:

1. MULTIBUS master read cycle.
2. MULTIBUS master write cycle.
3. Local read cycle.
4. Local write cycle.
5. MULTIBUS slave write cycle.
6. Ethernet coprocessor write cycle.
7. Ethernet coprocessor read cycle.

Sections 3.3.1 through 3.3.6 describe these cycles.

3.3.1 MULTIBUS® Read Cycle

Figure 3-1 shows the various iSBC 552 circuit blocks described in this and the following sections. The 80186 Microprocessor (U11) asserts its status and address lines to initiate a MULTIBUS read cycle. The address decode block determines if the address is in the MULTIBUS window. If it is, the system bus arbiter (U49) is activated and a bus request is made. If the bus is acquired, control command signals from the system bus controller (U50) will be enabled onto the MULTIBUS by the MBAEN* signal from the arbiter. This signal also enables the output of the MULTIBUS address latches. An XACK* (System Acknowledge) from the MULTIBUS to the processors (82586 or 80186) will end the cycle and allow the Bus Arbiter to release the bus.

The iSBC 552 board incorporates a local timeout circuit to prevent an off-board access from causing the 80186 processor to enter a continuous wait state if no

XACK* is received from the MULTIBUS. After the timeout has expired (approximately 4 to 6 ms), a TIMEOUT* signal becomes active, allowing the processor to complete the cycle and release the bus.

3.3.2 MULTIBUS® I/O Read Cycle

At power-up, the iSBC 552 board disables any I/O operations to the MULTIBUS interface. This allows the 80186 microprocessor to be programmed internally, without generating I/O cycles on the MULTIBUS interface. During any 80186 I/O cycle to internal register, the MULTIBUS I/O must be disabled. If the MULTIBUS I/O is enabled, any I/O cycle will be a MULTIBUS cycle. The MULTIBUS I/O can be enabled by issuing a memory write to the iSBC 552 memory-mapped I/O location PBA +104. The MULTIBUS I/O can be disabled by issuing a memory write to the iSBC 552 memory-mapped I/O location PBA +106 (see Table 4-1).

3.3.3 MULTIBUS® Write Cycle

MULTIBUS write cycles are similar to MULTIBUS read cycles except that the system bus controller asserts a write command instead of a read command and the direction of data through the data transceivers (U56, U57 and U58) reverses.

3.3.4 Local Read Cycle/Local Write Cycle

A local read cycle is a read cycle whose address is not within the MULTIBUS window. The local bus controller (U13) (see Figure 3-1) is enabled. The MB/Local Address Decode block further decodes the address to select the correct memory or memory-mapped I/O location. If it is a memory-mapped I/O cycle, the Local Data buffer (U44) is enabled. If it is not a memory-mapped I/O cycle the selected device drives directly onto the AD bus. Ready circuitry generates ARDY for the 80186 and the 82586. If the cycle is to a RAM location, one wait-state is generated. If the cycle is not to a RAM location, no wait states are generated. Write cycles are similar to read cycles, except that write commands rather than read commands are generated by the local bus controller.

3.3.5 MULTIBUS® Slave Write Command

In a slave write command cycle the MULTIBUS address lines ADRO*-ADRF* are buffered by the Slave Address Buffers (U51 and U52) and decoded by the Slave Address Decoders (U31 through U34) to see if a match occurs with a jumper-selectable slave address. If a match occurs and IOWC* is active, the lower eight bits on the MULTIBUS data bus are written to the selected port (see Section 4.2.3). The iSBC 552 board also generates XACK* to the MULTIBUS. Only byte-write may be performed, and byte swap circuitry must be provided by the master doing the write operation. As shown in Figure 3-1, the slave interface circuity is independent of the local bus of the iSBC 552 board. This means slave write can occur while the processor is busy with something else.

3.3.6 Ethernet Coprocessor Cycle

An 82586 LCC cycle is initiated when the 80186 processor issues a Channel Attention (CA) signal to the LCC. The processor uses its PSC0* line as channel attention. In response to the 80186 channel attention request, the LCC asserts HOLD. The 80186 internally arbitrates the request and releases the bus with HLDA (Hold Acknowledge). The 82586 proceeds with its read or write cycle. When finished, the 82586 removes HOLD; in response, the 80186 removes HLDA. The 80186 can regain access of the bus at any time by removing HLDA.

3.4 MULTIBUS® TRANSFERS

The iSBC 552 board's 80186 microprocessor can perform a string move between the MULTIBUS memory and the on-board buffer RAM of the iSBC 552 board at the rate of one transfer every 1.125 ms. That rate assumes zero wait-state MULTIBUS memory and no bus contention. If the system memory is 16 bits wide the transfer rate is 14.2M bits/second. If typical MULTIBUS memory boards (16 bits, 450 ns cycle times) are installed in the system, with the iSBC 552 board, the transfer rate drops to one transfer every 1.625 ms or 9.84M bits/second, assuming no bus contention. Because the iSBC 552 board does not lock the bus or provide highest bus priority, bus contention will most likely occur, and the 9.84M bits/second transfer rate will not be sustained for long periods. The transfer rate for the iSBC 552 board in a unique system depends upon that system's configuration (the number and type of modules on the MULTIBUS).

3.5 FUNCTIONAL INTERFACES

The iSBC 552 has two functional interfaces: the MULTIBUS interface through edge connectors P1 and P2, and the transceiver interface, through connector J1. Section 3.5.1 provides a functional description of the MULTIBUS interface. Sections 2.4.4 and 2.4.5 describe the physical and electrical characteristics of the MULTIBUS interface. Section 3.5.2 is a functional description of the transceiver interface. Sections 2.4.4 and 2.4.6 describe the physical and electrical characteristics of the transceiver interface.

3.5.1 MULTIBUS® Interface

The interface between the MULTIBUS and the iSBC 552 board is through edge connectors P1 and P2 on the iSBC 552 board. Table 3-1 defines the iSBC 552 board's input and output signals at the MULTIBUS interface. (MULTIBUS connector pin assignments are shown in Table 2-2; MULTIBUS timing is shown in Figure 2-2 and Table 2-7.)

Table 3-1. MULTIBUS® Signal Descriptions

Signal	I/O**	Functional Description
ADRO* -ADRF* ADR10*-ADR13*	I/O	Address. These 20 lines transmit the address of the memory location or I/O port to be accessed. For memory access, ADR0* (when active) enables the even byte bank (DAT0*-DAT7*) on the MULTIBUS; i.e., ADR0* is active for all even addresses. 13* is the most significant address bit for 20-bit addressing.
ADR14*-ADR17*		Address bits ADR14* through ADR17* are the four most significant bits in 24-bit addressing.
BCLK*	I	Bus Clock. Used to synchronize the bus contention logic on all bus masters.
BHEN*	O	Byte High Enable. When active low, enables the odd byte bank (DAT8* - DATF*) onto the MULTIBUS.
BPRN*	I	Bus Priority In. When low indicates to a particular bus master that no higher priority bus master is requesting use of the bus. BPRN* is sychronized with BCLK*.

Table 3-1. MULTIBUS® Signal Descriptions (Cont'd.)

Signal	I/O**	Functional Description
BPRO*	O	Bus Priority Out. In serial priority resolution schemes, BPRO* must be connected to the BPRN* input of the bus master with the next lower priority. On the iSBC 552 board this output can be disconnected by a jumper.
BREQ*	O	Bus Request. In parallel priority resolution schemes, BREQ* indicates that a particular bus master requires control of the bus for one or more data transfers. BREQ* is synchronized with BCLK*.
BUSY*	I/O	Bus Busy. Indicates that the bus is in use and prevents all other bus masters from gaining control of the bus. BUSY* is synchronized with BCLK*.
CBRQ*	I/O	Common Bus Request. Indicates that a bus master wants control of the bus but does not presently have control. As soon as the bus master gets control of the bus, the requesting bus controller raises the CBRQ* signal.
CCLK*	O	Constant Clock. Provides a clock signal of constant frequency for use by other system modules.
DAT0*-DATF*	I/O	Data. These 16 bidirectional data lines transmit and receive data to and from the addressed memory location. DATF* is the most significant bit. For data byte operations, DAT0* - DAT7* is the even byte and DAT8*-DATF* is the odd byte.
INH1*		Not used.
INH2*		Not used.
INIT*	I	Initialize. Resets the entire system to a known internal state.
INTA*		Not used.
INT0*-INT7*	O	Interrupt Request. These eight lines transmit interrupt requests to the appropriate interrupt handler. INT0* has the highest priority. INT5* is the default used for the iSBC 552 board.

Table 3-1. MULTIBUS® Signal Descriptions (Cont'd.)

Signal	I/O**	Functional Description
IORC*	O	I/O Read Command. Indicates that the address of an I/O port is on the MULTIBUS address lines and that the output of that port is to be read (placed) onto the MULTIBUS data lines.
IOWC*	O	I/O Write Command. Indicates that the address of an I/O port is on the MULTIBUS address lines and that the contents on the MULTIBUS data lines are to be accepted by the addressed port.
LOCK*		Not used.
MRDC*	O	Memory Read Command. Indicates that the address of a memory location is on the MULTIBUS address lines and that the contents of that location are to be read (placed) on the MULTIBUS data lines.
MWTC*	O	Memory Write Command. Indicates that the address of a memory location is on the MULTIBUS address lines and that the contents on the MULTIBUS data lines are to be written into that location.
XACK*	I/O	Transfer Acknowledge. Indicates that the address memory location or device has completed the specified operation. That is, data has been placed onto or accepted from the MULTIBUS data lines.

Notes: * = Low level signal.
** O = Output from the iSBC 552 board.
I = Input to the iSBC 552 board.

3.5.2 Transceiver Interface

The iSBC 552 board communicates with the serial link of the Ethernet through the transceiver interface (connector J1). Table 3-2 lists and defines the transceiver interface signals. Chapter 2 gives pin assignments, signal levels, and interface timing. The data transfer rate through the interface is 10M bits/second.

Table 3-2. Transceiver Interface Signal Descriptions

Signal	I/O**	Functional Description

TRMT(+)
TRMT(-)
	O	Transmit Data Pair. These Two lines generate a differential signal that drives the interface cable with Manchester data.

RCV(+)
RCV(-)
	I	Receive Data Pair. This is a differentially-driven input to the iSBC 552 board where Manchester data is received from the transceiver. The first transition is negative-going, indicating the beginning of a data frame.

CLSN(+)
CLSN(-)
	I	Collision Input Pair. The collision presence signal is a 10 MHz ± 5% square wave generated by the transceiver whenever data frames are superimposed in the coaxial cable.

3.5.3. Host Interrupt

The iSBC 552 board uses an interrupt signal to gain the attention of the MULTIBUS host CPU (see Section 4.4.4).

The iSBC 552 board generates a nonbus-vectored, level-triggered interrupt on the MULTIBUS interrupt line (INT0* through INT 7*) for which the board has been set up (see Section 2.4.7.2 and Table 2-11). The interrupt can be set only by the iSBC 552 boards 80186 microprocessor. It can be reset by either the 80186 or by a MULTIBUS master capable of performing I/O writes.

CHAPTER 4.
PROGRAMMING INFORMATION

4.1 INTRODUCTION

This chapter describes the various iSBC 552 board programming considerations. Board addressing is discussed as is programming of the 80186 16-bit Microprocessor and the 82586 Local Communications Controller (LCC).

4.2 iSBC® 552 BOARD ADDRESSING

The 80186 microprocessor, running at 6 MHz, provides the intelligence for the iSBC 552 board. The 80186 moves control information and serial link data between the MULTIBUS memory and the on-board 82586 LCC accessible memory. The 80186 can access the entire 16M byte MULTIBUS memory map through a movable window in the local memory map, and can perform I/O on the MULTIBUS interface through its entire 64K byte space. The following section describes the iSBC 552 board's addressing considerations.

4.2.1 Memory Addressing

When used as a MULTIBUS master, the iSBC 552 can access the full 16M Byte MULTIBUS address space from 000000(H) through FFFFFF(H). This use of the full address space can be accomplished by latching a MULTIBUS 64K low boundary address into the MULTIBUS Extended Address Latch (U43) (see Figure 3-1). The latch is located at the PBA (Programmable Base Address) plus 102(H). The local memory is mapped to create a 256K Byte window to the MULTIBUS located between 80186 local address 80000(H) and BFFFF(H) (see Figure 4-1). The total MULTIBUS address space may be addressed by moving this 256K byte window on 64K boundaries. Data transfers are either 8 or 16 bits. The iSBC 552 uses byte swap circuitry to speed up data transfers during 8-bit data transfers.

4.2.2 I/O Addressing

As a MULTIBUS master, the iSBC 552 board can access all of the 64K Byte MULTIBUS I/O space from 0000(H) to FFFF(H). Data transfers can be either 8 or 16 bits.

During bus cycles to internal registers, the 80186 processor signals the operation externally. Because of this condition, MULTIBUS I/O operations must be disabled during 80186 internal operations. MULTIBUS I/O is disabled after a reset. Software control is accomplished by memory write operations to PBA + 104 and PBA + IOG (see Table 4-1).

When used as a slave, the iSBC 552 board occupies four adjacent 8-bit ports in the MULTIBUS I/O map. The base port address and 8 or 16 bit addressing are jumper-selectable. See Tables 2-9 and 2-10 as well as Section 4.2.3 for more information on base port address selection.

The iSBC 552 port functions are as follows:

Base Address +0 =	Flag byte registers or Command Port (MULTIBUS write only).
Base Address +1 =	System Configuration Pointer (SCP), low byte (MULTIBUS write only).
Base Address +2 =	SCP, middle byte (MULTIBUS write only).
Base Address +3 =	SCP, high byte (MULTIBUS write only).

The hardware determined bit assignments for these ports are restricted to the command port. The bit assignments are as follows:

DAT0 = 1	Reset iSBC 552 board.
DAT1 = 1	Channel attention (interrupt iSBC 552 Board).
DAT2 = 1	Reset MULTIBUS interrupt.
DAT3 - DAT7	Don't care.

The least significant bit of the 24-bit SCP value corresponds to the least significant bit of the 8-bit port of the Base Address (BA) + 1. The most significant bit of the SCP value corresponds to the most significant bit of the 8-bit port at BA + 3.

Reading any of these ports by MULTIBUS yields indeterminate data.

4.2.3 Base Address Assignment

As described in Section 4.2.2 the iSBC 552 board occupies four adjacent 8-bit write-only ports in MULTIBUS I/O space. The base address for these ports is optional, as is 8- or 16-bit compatibility (see Section 2.4.7.1). For 8-bit I/O the base address is located on any 4-byte boundary between 00(H) and FC(H). For 16-bit I/O the base address can be located on any 4-byte boundary between 0000(H) and FFFC(H). These options are selected by installing jumpers on the iSBC 552 board (see Tables 2-9 and 2-10). The default configuration for the board is an 8-bit I/O and a base port address of A8(H).

4.2.4 iSBC® 552 Memory Map

The iSBC 552 board is completely memory-mapped (see Table 4-1 and Figure 4-1). A 74LS139 (U46) two-to-four line decoder decodes local address bits 18 and 19 to divide the 1M byte 80186 memory space into 256K byte quadrants. The upper quadrant, 768K (C0000(H)) to 1M (100000(H)), and the lower quadrant, 0 to 256K (3FFFF(H)), are reserved solely for local memory. Quadrant 2, between 256K (40000(H) and 512K (7FFFF(H)), is for memory-mapped I/O; quadrant 3, 512K (80000(H)) to 768K (BFFFF(H)), is used as the 256K window to the 16M Byte MULTIBUS interface.

4.2.5 Summary of Addressing

The following list summarizes the iSBC 552 addressing considerations:

1. The 80186 processor's 1M byte memory address space is divided into four quadrants. The quadrant boundaries and other functions are as follows:

Quadrant	Boundaries	Function
1	00000(H) - 3FFFF(H)	RAM local memory space
2	40000(H) - 7FFFF(H)	On-board memory mapped I/O
3	80000(H) - BFFFF(H)	256K byte MULTIBUS window
4	C0000(H) - FFFFF(H)	EPROM memory space

Table 4-1. iSBC® 552 Board Memory Map

80186 Chip Selects	Address	Function
MCS0	Not used	Not Used
MCS1	Within on-board	Byte 0 of SCP (Read Only)
MCS2	memory mapped	Byte 1 of SCP (Read Only)
MCS3	I/O Space	Byte 2 of SCP (Read Only)
PCS0	PBA + 00 (H)	82586 channel attention
PCS1	PBA + 80 (H)	Byte 1 of the Ethernet node address
(Read	PBA + 82 (H)	Byte 2 of the Ethernet node address
Only)	PBA + 84 (H)	Byte 3 of the Ethernet node address
	PBA + 86 (H)	Byte 4 of the Ethernet node address
	PBA + 88 (H)	Byte 5 of the Ethernet node address
	PBA + 8A (H)	Byte 6 of the Ethernet node address
	PBA + 8C (H)	Byte 7 of the Ethernet node address
	PBA + 8E (H)	Byte 8 of the Ethernet node address
	:	:
	:	:
	:	:
	:	:
	PBA + B0 (H)	Byte 25 of the Ethernet node address
	PBA + B2 (H)	Byte 26 of the Ethernet node address
	PBA + B4 (H)	Byte 27 of the Ethernet node address
	PBA + B6 (H)	Byte 28 of the Ethernet node address
	PBA + B8 (H)	Byte 29 of the Ethernet node address
	PBA + BA (H)	Byte 30 of the Ethernet node address
	PBA + BC (H)	Byte 31 of the Ethernet node address
	PBA + BE (H)	Byte 32 of the Ethernet node address
PCS2	PBA + 100 (H)	Data Bit 0, LED off
(Write		Data Bit 1, 82501 loopback
Only)	PBA + 102 (H)	MULTIBUS extended address latch
	PBA + 104 (H)	MULTIBUS I/O enable
	PBA + 106 (H)	MULTIBUS I/O disable
	PBA + 108 (H)	MULTIBUS interrupt disable
	PBA + 10A (H)	MULTIBUS interrupt enable
PCS3 - 6	Not used	Not used

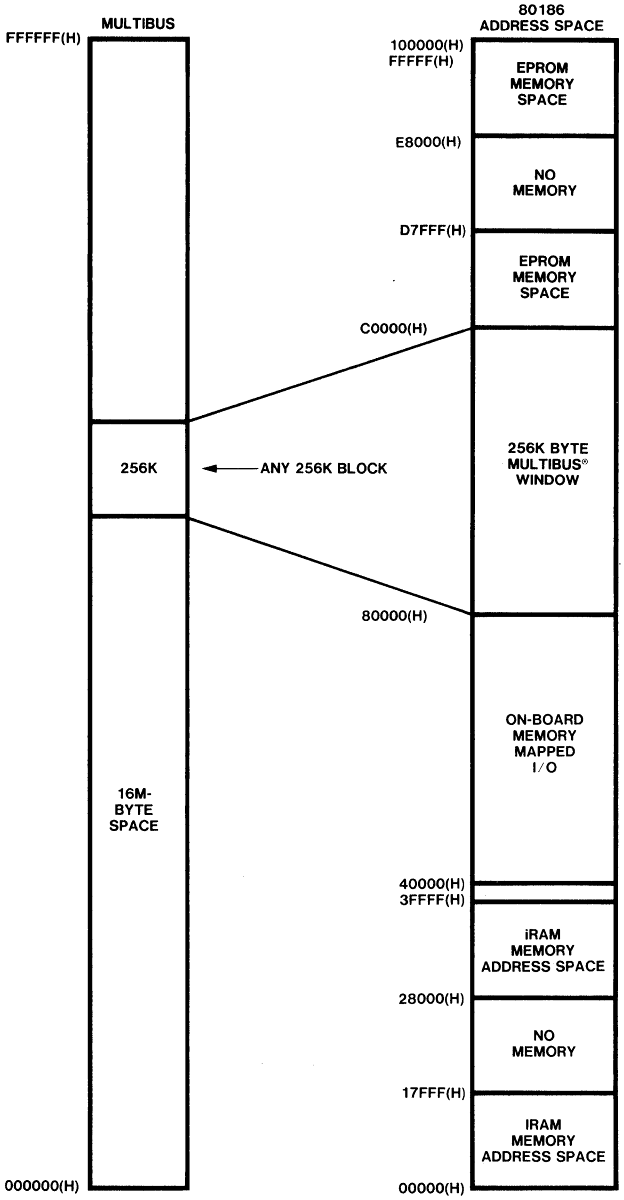


Figure 4-1. iSBC® 552 Board Memory Map

2. The iSBC 552 board occupies four adjacent 8-bit write-only ports in MULTIBUS I/O space. Base addresses for these ports are user selectable. Port addressing is–

8-bit I/O -	Any 4-byte boundary between 00(H) and FC(H).

16-bit I/O	–	Any 4-byte boundary between 0000(H) and FFFC(H).
Default Configuration	–	8-bit I/O at A8(H).

3. The iSBC 552 local I/O is memory mapped by programming the 80186 internal control registers (MPCS and PACS). The PCS and MCS lines should be programmed within the local address range of 40000(H) to 7FFFF(H).

4. To ensure one-wait state insertion, RAM is accessed between 0 and 3FFFF(H). To ensure 0-wait states EPROM is accessed between C0000(H) and FFFFF(H).

5. The Ethernet station address PROM will reside at PBA + 80(H) through PBA + BE(H).

4.3 80186 PROGRAMMING

The following sections describe 80186 programming. The iAPX 186 Data Sheet, can be consulted for more detailed information.

4.3.1 80186 Base Architecture

The 80186 base architecture has 14 registers as shown in Figures 4-2 and 4-3. These registers are grouped into the following categories.

o General Registers	Eight 16-bit general purpose registers that contain arithmetic and logical operands. Four of these (AX, BX, CX, and DX) can be used as 16-bit registers or split into pairs of 8-bit registers.
o Segment Registers	Four 16-bit special purpose registers that select, at any given time, the segments of memory that are immediately addressable for code, stack, and data.

o Base and Index Registers — Four of the general purpose registers may also be used to determine offset addresses of operands in memory. The registers may contain base addresses or indexes to particular locations within a segment. The addressing mode selects the specific registers for operand and address calculations.

o Status and Control Registers — Two 16-bit special purpose registers that record or alter certain aspects of the 80186 processor state. One of these registers is the Instruction Pointer Register, which contains the offset address of the next sequential instruction to be executed. The other register is the Status Word Register, which contains status and control flag bits. See Figures 4-2 and 4-3.

The Status Word records specific characteristics of the results of logical and arithmetic instructions (Bits 0,2,4,6,7, and 11) and controls 80186 operation within a given operating mode (Bits 8,9, and 10). The Status Word Register is 16-bits wide. Table 4-2 gives the Status Word functions.

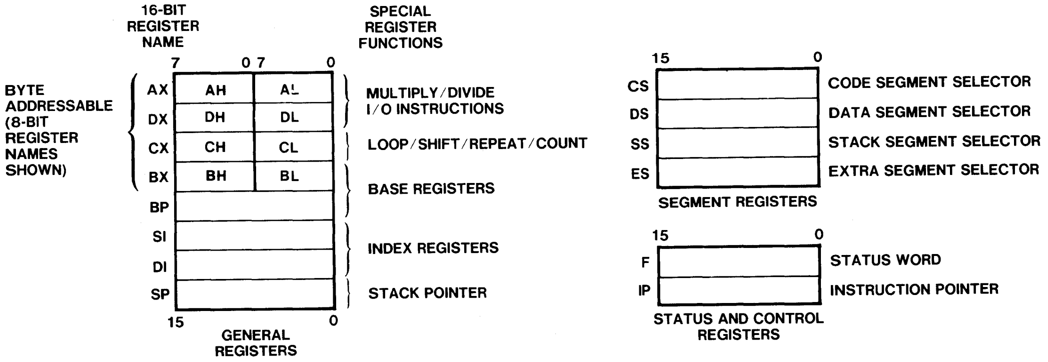


Figure 4-2. 80186 General Purpose Register Set

122141-9

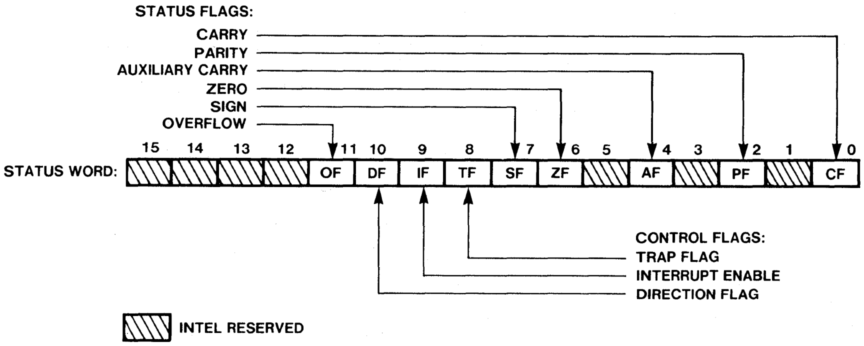


Figure 4-3. Status Word Format 122141-10

Table 4-2. Status Word Bit Functions

Bit Position	Name	Function
0	CF	Carry Flag - Set on high order bit carry or borrow; cleared otherwise.
2	PF	Parity Flag - Set if low-order 8 bits of result contain an even number of "1" bits; cleared otherwise.
4	AF	Auxiliary Carry - Set on carry from or borrow to the low order 4 bits of AL; cleared otherwise.
6	ZF	Zero Flag - Set if result is 0; cleared otherwise.
7	SF	Sign Flag - Set equal to high-order bit of result (0 if positive, 1 if negative).
8	TF	Single Step Flag - Once set, a single step interrupt occurs after the next instruction executes. TF is cleared by the single step interrupt.
9	IF	Interrupt Enable Flag - When set, maskable interrupts cause the CPU to transfer control to an interrupt vector specified location.
10	DF	Direction Flag - Causes string instruction to auto decrement the appropriate index register when set. Clearing DF causes auto increment.
11	OF	Overflow Flag - Set if the signed result cannot be expressed within the number of bits in the destination operand; cleared otherwise.

The instruction set is divided into seven categories: data transfer. arithmetic, shift/rotate/logical, string manipulation, control transfer, high level instructions, and processor control. These categories are summarized in Table 4-3.

An 80186 instruction can reference anywhere from zero to several operands. An operand can reside in a register, in the instruction itself, or in memory.

Table 4-3. Instruction Set

	GENERAL PURPOSE	FLAG OPERATIONS	
MOV	Move byte or word	STC	Set carry flag
PUSH	Push word onto slack	CLC	Clear carry flag
POP	Pop word off stack	CMC	Complement carry flag
PUSHA	Push all registers on stack	STD	Set direction flag
POPA	Pop all registers from stack	CLD	Clear direction flag
XCHG	Exchange	STI	Set interrupt enable flag
XLAT	Translate byte	CLI	Clear interrupt enable flag
INTPUT/OUTPUT		NO OPERATION	
IN	Input byte or word	NOP	No operation
OUT	Output byte or word		
ADDRESS OBJECT		HIGH LEVEL INSTRUCTIONS	
LEA	Load effective address	ENTER	Format stack for procedure entry
LDS	Load pointer using DS	LEAVE	Restore stack for procedure exit
LES	Load pointer using ES	BOUND	Detects values outside prescribed range
FLAG TRANSFER		EXTERNAL SYNCHRONIZATION	
LAHF	Load AH register from flags	HLT	Halt until interrupt or reset
SAHF	Store AH register in flags	WAIT	Wait for TEST pin active
PUSHF	Push flags onto stack	ESC	Escape to extension processor
POPF	Pop flags off stack	LOCK	Lock bus during next instruction
ADDITION		LOGICALS	
ADD	Add byte or word	NOT	"Not" byte or word
ADC	Add byte or word with carry	AND	"And" byte or word
INC	Increment byte or word by 1	OR	"Inclusive or" byte or word
AAA	ASCII adjust for addition	XOR	"Exclusive or" byte or word
DAA	Decimal adjust for addition	TEST	"Test" byte or word

Table 4-3. Instruction Set (Cont'd.)

MULTIPLICATION		SHIFTS	
MUL	Multiply byte or word unsigned	SHL/SAL	Shift logical/arithmetic left byte or word
IMUL	Integer multiply byte or word	SHR	Shift logical right byte or word
AAM	ASCII adjust for multiply	SAR	Shift arithmetic right byte or word
SUBTRACTION		ROTATES	
SUB	Subtract byte or word	ROL	Rotate left byte or word
SBB	Subtract bye or word with borrow	ROR	Rotate right byte or word
DEC	Decrement byte or word by 1	RCL	Rotate through carry left byte or word
NEG	Negate byte or word	RCR	Rotate through carry right byte or word
CMP	Compare byte or word		
AAS	ASCII adjust for subtraction		
DAS	Decimal adjust for subtraction		
DIVISION		CONDITIONAL TRANSFERS	
DIV	Divide byte or word unsigned	JA/JNBE	Jump if above/not below nor equal
IDIV	Integer divide byte or word	JAE/JNB	Jump if above or equal/not below
AAD	ASCII adjust for division	JB/JNAE	Jump if below/not above nor equal
CBW	Convert byte to word	JBE/JNA	Jump if below or equal/not above
CWD	Convert word to doubleword	JC	Jump if carry
MOVS	Move byte or word string	JE/JZ	Jump if equal/0
INS	Input bytes or word string	JG/JNLE	Jump if greater/not less nor equal
OUTS	Output bytes or word string	JGE/JNL	Jump if greater or equal/not less
CMPS	Compare byte or word string	JL/JNGE	Jump if less/not greater nor equal
SCAS	Scan byte or word string	JLE/JNG	Jump if less or equal/not greater
LODS	Load byte or word string	JNC	Jump if not carry
STOS	Store byte or word string	JNE/JNZ	Jump if not equal/not zero
REP	Repeat	JNO	Jump if not overflow
REPE/ REPZ	Repeat while equal/0	JNP/JPO	Jump if not parity/parity odd
		JNS	Jump if not sign
REPNE/ REPNZ	Repeat while not equal/not 0	JO	Jump if overflow
		JP/JPE	Jump if parity/parity even
		JS	Jump if sign
ITERATION CONTROLS		UNCONDITIONAL TRANSFERS	
LOOP	Loop	CALL	Call Procedure
LOOPE/ LOOPZ	Loop if equal/0	RET	Return from procedure
		JMP	Jump
LOOPNZ LOOPNE/	Loop if not equal/not 0	JCXZ	Jump if register CX = 0
INTERRUPTS			
INT	Interrupt		
INTO	Interrupt if overflow		
IRET	Interrupt return		

4.3.2 Addressing Modes

Memory is organized in sets of segments. Each segment is a linear continuous sequence of up to 64K (2^{16}) 8-bit bytes. Memory is addressed using a two-component address (a pointer) that consists of a 16-bit base segment and a 16-bit offset. The 16-bit base values are contained in one of four internal segment registers (code, data, stack, or extra). The physical address is calculated by shifting the base value LEFT by four bits and adding the 16-bit offset value to yield a 20-bit physical address (see Figure 4-4). This allows for a 1M byte address size.

All instructions that address operands in memory must specify the base segment and the 16-bit offset value. For speed and compact instruction encoding, the segment register used for physical address is implied by the addressing mode used (see Table 4-4). The rules shown in Table 4-4 follow the way programs are written: as independent modules that require areas for code and data, a stack, and access to external data areas.

Special segment override instruction prefixes allow the implicit segment register selection rules to be overridden for special cases. The stack, data, and extra segments may coincide for simple programs.

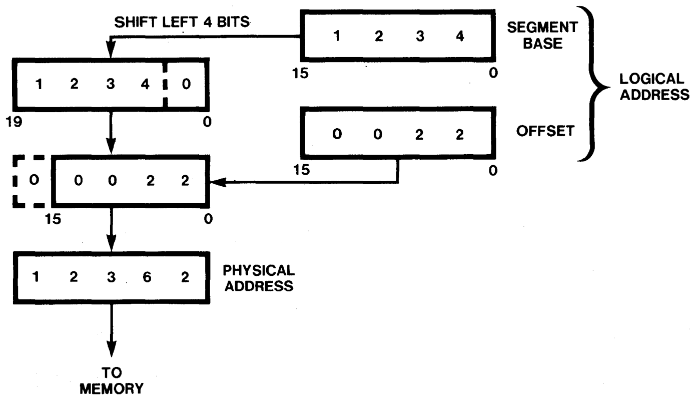


Figure 4-4. Two Component Address

122141-11

Table 4-4. Segment Register Selection Rules

Memory Reference Needed	Segment Register Used	Implicit Segment Selection Rule
Instructions	Code (CS)	Instruction prefetch and immediate data.
Stack	Stack (SS)	All stack pushes and pops: any memory references that use the BP Register as a base register.
External Data (Global)	Extra (ES)	All string instruction references that use the DI register as an index.
Local Data	Data (DS)	All other data references.

The 80186 provides eight kinds of addressing modes to specify operands. Two of the eight addressing modes are for instructions that operate on register or immediate operands:

- o Register Operand Mode. The operand is located in one of the 8- or 16-bit general registers.

- o Immediate Operand Mode. The operand is included in the instruction.

Six modes are provided to specify the location of an operand in a memory segment. A memory operand address consists of two 16-bit components: a segment base and an offset. The segment base is supplied by a 16-bit segment register either implicitly chosen by the addressing mode or explicitly chosen by a segment override prefix. The offset, also called the effective address, is calculated by summarizing any combination of the following three address elements:

- o The **displacement** (an 8- or 16-bit immediate value contained in the instruction).
- o The **base** (contents of either the BX or BP base registers).
- o The **index** (contents of either the SI or DI index registers).

Any carry over from the 16-bit addition is ignored. Eight-bit displacements are sign extended to 16-bit values.

Combinations of the three address elements define the six remaining memory addressing modes, described below:

- Direct Mode: The operand's offset is contained in the instruction as an 8- or 16-bit displacement element.
- Register Indirect Mode: The operand's offset is in one of the registers SI, DI, BX, or BP.
- Based Mode: The operand's offset is the sum of an 8- or 16-bit displacement and the contents of a base register (BX or BP).
- Indexed Mode: The operand's offset is the sum of an 8- or 16-bit displacement and the contents of an index register (SI or DI).
- Based Indexed Mode: The operand's offset is the sum of an 8-or 16-bit displacement and the contents of an index register.
- Based Indexed Mode with Displacement: The operand's offset is the sum of a base register's contents, an index register's contents, and an 8- or 16-bit displacement.

4.3.3 Data Types

The 80186 directly supports the following data types:

- Integer. A signed binary numeric value contained in an 8-bit byte or a 16-bit word. All operations assume a 2's complement representation. Signed 32 and 64-bit integers are supported using the iAPX 186/20 Numeric Data Processor.
- Ordinal. An unsigned binary numeric value contained in an 8-bit byte or a 16-bit word.
- Pointer. A 16- or 32-bit quantity composed of a 16-bit offset component or a 16-bit segment base component, in addition to a 16-bit offset component.
- String. A continuous sequence of bytes or words. A string may contain from 1 to 64K Bytes.
- ASCII. A byte representation of alphanumeric and control characters using the ASCII standard of character representation.
- BCD. A byte (unpacked) representation of the decimal digits 0-9.
- Packed BCD. A byte (packed) representation of two decimal digits (0-9). One digit is stored in each nibble (4 bits) of the byte.

- Floating-Point. A signed 32-, 64-, or 80-bit real number representation. (Floating-point operands are supported using the iAPX 186/20 Numeric Data Processor configuration).

In general, individual data elements must fit within defined segment limits.

4.3.4 I/O Space

The I/O space consists of 64K 8-bit or 32K 16-bit ports. Separate instructions address the I/O space with either an 8-bit port address specified in the instruction or a 16-bit port address specified in the DX register. Eight-bit port addresses are zero extended so that A_{15}-A_8 are low. I/O port addresses 00F8(H) through 00FF(H) are reserved.

4.3.5 80186 Clock Generator

The 80186 clock generator is used in the frequency mode. A 12 MHz crystal is connected to the crystal inputs. The three 80186 timers are available and can be used. The timer inputs and outputs are not supported, however, and only internal interrupts are allowed.

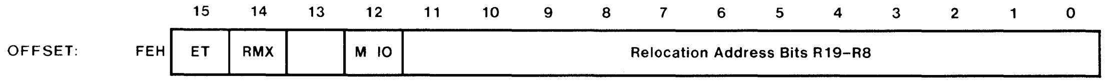
4.3.6 Reset Logic

The 80186 processor reset logic is used with the addition of some external logic to do power-on resets and normal board resets.

4.3.7 Internal Peripheral Interface

All iAPX 186 integrated peripherals are controlled via 16-bit registers contained within an internal 256-byte control block. This control block may be mapped into either memory or I/O space. Internal logic recognizes the address and responds to the bus cycle. During bus cycles to internal registers, the bus controller signals the operation externally (i.e. the RD, WR status address, data, etc., lines are driven as in a normal bus cycle) but D_{15-0}, SRDY, and ARDY are ignored. The base address of the control block must be on an even 256-byte boundary (i.e., the lower 8 bits of the base address are all 0s). All of the defined registers within this control block may be read or written by the 80186 CPU at any time. The location of any register contained within the 256-byte control block is determined by the current base address of the control block.

The control block base address is programmed via a 16-bit relocation register contained within the control block at offset FEH from the base address of the control block (see Figure 4-5). The address provides the upper 12 bits of the base address of the control block. Note that mapping the control register block into an address range corresponding to a chip-select range is not recommended. In addition, bit 12 of this register determines whether the control block will be mapped into I/O or memory space. If this bit is 1, the control block will be located in memory space, whereas if the bit is 0, the control block will be located in I/O space. If the control register block is mapped into I/O space, the upper four bits of the base address must be programmed as 0 (because I/O addresses are only 16 bits wide).



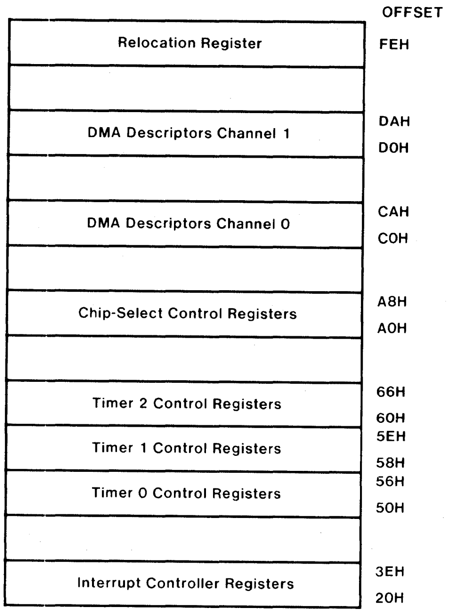
ET = ESC Trap No ESC Trap (1 0)
M IO = Register block located in Memory I O Space (1 0)
RMX = Normal Interrupt Controller mode iRMX compatible
Interrupt Controller mode (0 1)

122136-2

Figure 4-5. Relocation Register

In addition to providing relocation information for the control block, the relocation register contains bits that place the interrupt controller.into iRMX mode and cause the CPU to interrupt upon encountering ESC Instructions. At RESET, the relocation register is set to 20FFH. This causes the control block to start at FF00H in I/O space. An offset map of the 256-byte control register block is shown in Figure 4-6.

The integrated iAPX 186 peripherals operate semi-autonomously from the CPU. Access to them for the most part is via software read/write of the control and data location in the control block. Most of these registers can be both read and written. A few dedicated lines, such as interrupts and DMA request, provide real-time communication between the CPU and peripherals. as in a more conventional system utilizing discrete peripheral block.


OFFSET
Relocation Register
FEH
DMA Descriptors Channel 1
DAH
D0H
DMA Descriptors Channel 0
CAH
C0H
Chip-Select Control Registers
A8H
A0H
Timer 2 Control Registers
66H
60H
Timer 1 Control Registers
5EH
58H
Timer 0 Control Registers
56H
50H
Interrupt Controller Registers
3EH
20H

122136-3

Figure 4-6. Internal Register Map

4.3.8 Midrange Memory Chip Select

The iAPX 186 contains logic that provides programmable chip-select generation for both memories and peripherals. In addition, the 80186 can be programmed to provide READY (or WAIT state) generation. It can also provide latch address bits A1 and A2. The chip-select lines are active for all memory and I/O cycles in their programmed areas, whether they are generated by the CPU or by the integrated DMA unit.

The iAPX 186 provides 6 memory chip select outputs for 3 address areas: upper memory, lower memory, and midrange memory. One each is provided for upper memory and lower memory, while four are provided for midrange memory chip select.

The range for each chip select is user-programmable and can be set to 2K, 4K, 8K, 16K, 32K, 64K, 128K (plus 1K and 256K for upper and lower chip selects). In addition, the beginning or base address of the midrange memory chip select may also be selected. Only one chip select at a time may be programmed as active for any memory location at a time. All chip select sizes are in bytes, whereas iAPX 186 memory is arranged in words. This means that if, for example, 16 64K x 1 memories are used, the memory block size will be 128K, not 64K.

The iAPX 186 provides a chip select (UCΩ*) for the top of memory. The top of memory is usually used as the system memory because after reset the iAPX 186 begins executing at memory location FFFF0H.

The upper limit of memory defined by this chip select is always FFFFFH, while the lower limit is programmable. By programming the lower limit, the size of the select block is defined. Table 4-5 shows the relationship between the base address selected and the size of the memory block obtained. In the iSBC 552 configuration UCS is programmed for zero wait states; the size of the memory block is a "don't care."

Table 4-5. UMCS Programming Values

Starting Address (Base Address)	Memory Block Size	UMCS Value (Assuming R0=R1=R2=0)
FFC00	1K	FFF8H
FF800	2K	FFB8H
FF000	4K	FF38H
FE000	8K	FE38H
FC000	16K	FC38H
F8000	32K	F838H
F0000	64K	F038H
E0000	128K	E038H
C0000	256K	C038H

In the iSBC 552 configuration, the lower memory chip select (LCS*), is not programmed because it is not used.

The iAPX 186 provides four memory chip select lines that are active in a user-locatable memory block. This block can be located anywhere in the iAPX 186 1M byte memory address space exclusive of the areas defined by UCS* and LCS*. Both the base address and size of this memory block are programmable.

The size of the memory block defined by the mid-range select lines as shown in Table 4-6, is determined by bits 8-14 of the MPCS register (see Figure 4-7). This register is at location A8H in the internal control block. One and only one of bits 8-14 must be set at a time. Otherwise, the MCS* lines operate unpredictably. Each of the four chip-select lines is active for one of the four equal contiguous divisions of the mid-range block. Thus, if the total block size is 32K, each chip select is active for 8K of memory, with MCS0 being active for the first range and MCS3 being active for the last range.

Table 4-6. MMCS Programming Values

Total Block Size	Individual Select Size	MMCS Bits 8-14
8K	2K	0000001B
16K	4K	0000010B
32K	8K	0000100B
64K	16K	0001000B
128K	32K	0010000B
256K	64K	0100000B
512K	128K	1000000B

		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OFFSET:	A8H	1	M6	M5	M4	M3	M2	M1	M0	EX	MS	1	1	1	R2	R1	R0

122136-6

Figure 4-7. MPCS Register

The EX and MS bits in the MPCS relate to peripheral functionality as described in Section 4.3.9 and Table 4-8.

The base address of the midrange memory block is defined by bits 9-15 of the MMCS register (see Figure 4-8). This register is at offset A6H in the internal control block. These bits correspond to bits A19-A13 of the 20-bit memory address. Bits A12-A0 of the base address are always 0. The base address may be set at any integer multiple of the size of the total memory block selected. For example, if the midrange block size is 32K (or the size of the block for which each MCS* line is active is 8K), the block could be located at 10000H or 18000H, but not at 14000H, because the first few integer multiples of a 32K memory block are 0H, 8000H, 10000, 18000H, etc. After reset, the contents of both of these registers is undefined. However, none of the MCS* lines will be active until both the MMCS and MPCS registers are accessed.

	15						9						3			0
OFFSET: A6H	U	U	U	U	U	U	U	1	1	1	1	1	1	R2	R1	R0
	A19						A13									

122136-7

Figure 4-8. MMCS Register

MMCS bits R2-R0 specify READY mode of operation for all midrange chip selects. All devices in midrange memory must use the same number of WAIT states.

4.3.9 Peripheral Chip Selects

The iAPX 186 can generate chip selects for up to seven peripheral devices. These peripheral chip selects (PCS) are active for seven continuous blocks (of 128 bytes) above a programmable base address. This base address may be located in either memory or I/O space.

Seven CS lines called PCS0*-6* are generated by the iAPX 186. The base address is user-programmable; however it can only be a multiple of 1K Bytes - i.e., the least significant 10 bits of the starting address are always 0.

PCS5* and PCS6* can also be programmed to provide latched address bits A1,A2. If so programmed, they cannot be used as peripheral selects. These outputs can be connected directly to the A0, A1 pins used for selecting internal registers of 8-bit peripheral chips. This scheme simplifies the hardware interface because the 8-bit registers of peripherals are treated simply as 16-bit registers located on even boundaries in I/O space or memory space where only the lower 8-bits of the register are significant: the upper 8-bits are "don't cares."

The starting address of the peripheral chip-select block is defined by the PACS (Peripheral Address Chip Select) register (see Figure 4-9). This register is located at offset A4H in the internal control block. Bits 15-6 of this register correspond to bits 19-10 of the peripheral chip select block's 20-bit Programmable Base Address (PBA). Bits 9-0 of the PBA of the peripheral chip-select block are all zeros. If the chip-select block is located in I/O space, bits 12-15 must be programmed zero, because the I/O address is only 16 bits wide. Table 4-7 shows the address range of each peripheral chip select with respect to the PBA contained in PACS register.

		15									6	5		3			0
OFFSET:	A4H	U	U	U	U	U	U	U	U	U	U	1	1	1	R2	R1	R0
		A19									A10						

Figure 4-9. PACS Register

122136-8

Table 4-7. PCS Address Ranges

PCS Line	Active Between Locations	
PCSO	PBA	PBA + 127
PCS1	PBA + 128	PBA + 255
PCS2	PBA + 256	PBA + 383
PCS3	PBA + 384	PBA + 511
PCS4	PBA + 512	PBA + 639
PCS5	PBA + 640	PBA + 767
PCS6	PBA + 768	PBA + 895

The user should program bits 15-6 to correspond to the desired peripheral base location. PACS bits 0-2 are used to specify READY mode for PCS0*-PCS3*. For iSBC 552 operation, the PCS lines' address range should be within the on-board memory mapped I/O space.

The mode of operation of the peripheral chip selects is defined by the MPCS register (which is also used to set the size of the mid-range memory chip-select block as shown in Figure 4-7). This register located at offset A8H in the internal control block. Bit 7 is used to select the function of PCS5* and PCS6*, while bit 6 is used to select whether the peripheral chip selects are mapped into memory or I/O space. Table 4-8 describes the programming of these bits. After reset, the contents of both the MPCS and the PACS registers are undefined, however, none of the PCS lines are active until both of the MPCS and PACS registers are accessed.

MPCS bits 0-2 are used to specify READY mode for PCS4* - PCS6*.

Table 4-8. MS, EX Programming Values

Bit	Description
MS	1 = Peripherals mapped into memory space 0 = Peripherals mapped into I/O space
EX	0 = 5 PCS* lines; A1, A2 provided 1 = 7 PCS* lines; A1, A2 not provided

4.3.10 READY Generation Logic

Because the 82586 coprocessor does not have internal ready logic, the 80186 internal ready logic is unused. All chip selects are programmed with zero wait states, and an external ready is required. The external ready is generated by logic or the iSBC 552 board that selects between MULTIBUS acknowledge XACK* and local (iSBC 552 ready). Local ready has no wait states for PROM, and all peripheral chip selects operate with zero wait states.

4.3.11 Interrupt Control

The interrupt control registers are the control words for the four external inputs of the 80186. Figure 4-10 shows the format of the INT0 and INT1 Control registers. Figure 4-11 shows the format of the INT2 and INT3 Control registers. In cascade mode or special fully nested mode, the control words for INT2 and INT3 are not used.

15	14		7	6	5	4	3	2	1	0
0	0	• • • • • •	0	SFNM	C	LTM	MSK	PR2	PR1	PRO

Figure 4-10. INT0/INT1 Control Register Formats 122136-11

15	14		5	4	3	2	1	0
0	0	• • • • • • •	0	LTM	MSK	PR2	PR1	PRO

Figure 4-11. INT2/INT3 Control Register Formats 122136-12

The bits in the various control registers are encoded as follows:

PRO-2: Priority programming information. Highest priority = 000; lowest priority = 111.

LTM: Level-trigger mode bit: 1 = level triggered; 0 = edge-triggered. Interrupt input levels are active high. In level-triggered mode, an interrupt is generated whenever the external line is high. In edge-triggered mode, an interrupt will be generated only when this level is preceded by an inactive-to-active transition on the line. In both cases, the level must remain active until the interrupt is acknowledged.

MSK: MSK bit: 1 = mask; 0 = nonmask.

C: Cascade mode bit: 1 = cascade; 0 = direct.

SFNM: Special fully nested mode bit: 1 = SFNM.

To ensure interrupt recognition from the MULTIBUS to the iSBC 552, INT1 must be in the edge-triggered mode.

4.4 82586 PROGRAMMING

Sections 4.4.1 through 4.5.8 describe the commands, data structures and techniques by which the 80186 controls and uses the 82586. The emphasis here is not on any particular action command, but rather on how the 82586 LCC is controlled.

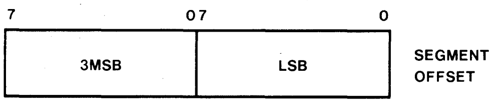
The 82586 has of two major internal processors: the Command Unit (CU) and the Receive Unit (RU). The 80186 exercises indirect control over them. Each unit accepts commands during a ready state. Although they are almost always ready, a delay might occur if the unit is busy responding to another internally generated request. Both units are multitasked units with non-preemptive scheduling, although buffer switching tasks preempt the RU and CU.

All control structures are memory resident; thus, all communications between the 80186 and the 82586 takes place via shared memory structures. There is no I/O port access to the 82586.

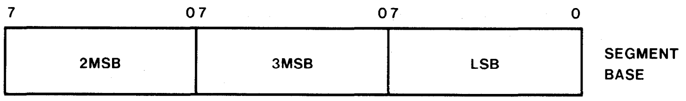
4.4.1 Memory Addressing Formats

The 82586 accesses memory by 24-bit addresses. In the iSBC 552 application only the lower 20 bits are used. There are two types of 24 bit addresses: real addresses and segmented addresses. A real address is a single 24-bit entity. It is used primarily to address transmit and receive data buffers. A segmented address uses a 24-bit base and a 16-bit offset. The segmented address is used for all Command Blocks, Buffer Descriptors, Frame Descriptors, and System Control Blocks (SCBs). In general, only the offset portion of the addressed entry is specified in the block. The base for all offsets is the same (that of the SCB). The diagrams below detail the memory address formats used. The LSB is the least significant byte of the address, 3MSB is the next most significant byte, and 2MSB, if present, is the next most significant byte.

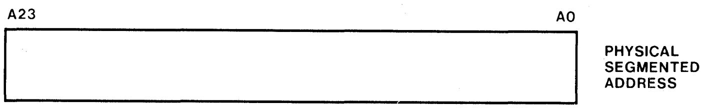
Command Structure Addressing:



122136-21

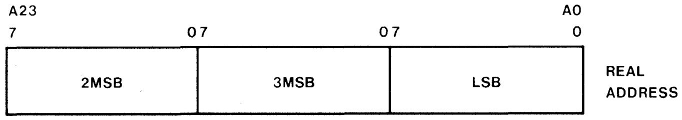


122136-22



122136-23

Physical (Real) Data Buffer Addressing:



122136-20

4.4.2 The System Control Block (SCB)

The SCB is a memory block that is shared by the 80186 and 82586. It forms the communication link between the 80186 and the 82586. Such communication involves–

- o Commands issued by the 80186.
- o Status reporting from the 82586.

The 80186 delivers Control commands to the 82586 by writing them into the SCB and asserting Channel Attention (CA). The 82586 examines the command, performs whatever action is required, and clears the command. Control commands perform four types of tasks:

- o Control operation of the Command Unit (CU).

- Control reception of packets by the Receive Unit (RU).
- Acknowledge events that caused an interrupt.
- Resetting the chip.

The SCB controls the command unit by specifying the address of the Command Block List (CBL) and by starting, suspending, resuming, or aborting CB command execution. It controls the receive unit by specifying the address of the Receive Packet Area (RPA), and by enabling, suspending, resuming, or aborting packet reception.

The SCB is also used for reporting status to the 80186. There are four types of status information contained in the SCB. The first type describes the cause(s) of the currently pending interrupt (events). The second indicates the status of the CU. The third indicates the status of the RU. The fourth contains corrupted receive frame statistics collected by the 82586.

Four events saved by the 82586 are–

- The completion of an action command by the CU.
- The reception of a frame by the RU.
- The CU becoming not ready.
- The RU becoming not ready.

The acknowledgement of events by the 80186 is the only means by which interrupts are cleared. Note that if not all events are acknowledged by the CA, the INT signal is reissued after processing the CA. Also, if a new event occurs while the interrupt is set, the interrupt is momentarily cleared in order to trigger edge-triggered input interrupt controllers.

The 80186 commands the 82586 to examine the SCB via the CA line. This signal is falling edge triggered and is latched by the 82586. The latch is cleared by the 82586 as part of the SCB examination process, prior to reading the SCB.

The format of the SCB is shown in Figure 4-12. Definition of the blocks in Figure 4-12 is as follows:

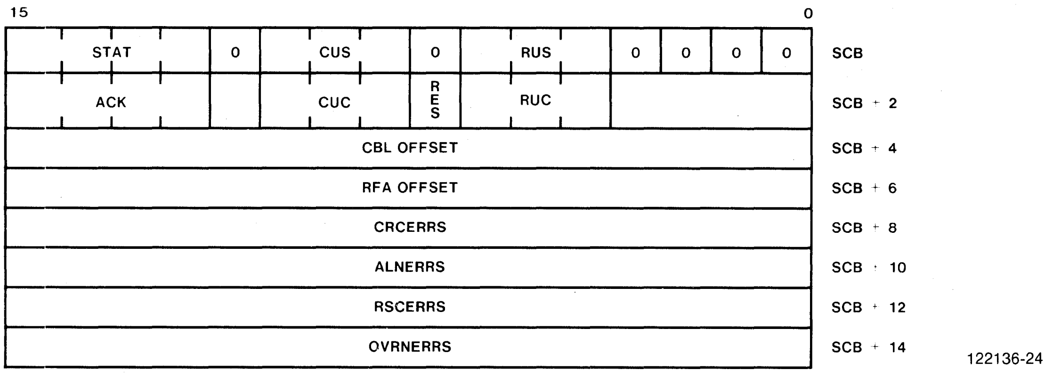


Figure 4-12. The System Control Block Format

STAT -

Indicates the status of the 82586. This word is modified only by the 82586. Defined bits are–

Bit 15 CX – A command in the CBL having its 'I' (interrupt) bit set has been executed.

Bit 14 PR – A packet has been received.

Bit 13 CNR – The CU became not ready.

Bit 12 RNR – The RU became not ready

Bits 8-10 CUS – The status of the CU. Valid values are–
(3 bits)

0 – Idle.
1 – Suspended.
2 – Ready.
3-7 – Unused.

Bits 4-6 RUS – This field contains the status of the RU. Valid values are–
(3 bits)

0 – Idle.
1 – Suspended.
2 – No Resources.

3 – Unused.

4 – Ready.

5-7 – Unused.

Command

Specifies the action to be performed as a result of the CA. This word is set by the 80186 and cleared by the 82586. Bits are defined as follows:

Bit 15 ACK-CX – Acknowledges the command executed event.

Bit 14 ACK-PR – Acknowledges the packet received event.

Bit 13 ACK-CNR– Acknowledges that the command unit became not ready.

Bit 12 ACK-RNR– Acknowledges that the receive unit became not ready.

Bits 8-10 CUC – This field contains the command to the unit. Valid values
(3 bits) are –

0 – NOP (does not alter current state of the unit).

1 – Start execution of the first command on the CBL. If a command is in execution, then complete it before starting the new CBL. The beginning of the CBL is in CBL OFFSET.

2 – Resume command unit operation by executing the next command. This operation assumes that the command unit has been previously suspended.

3 – Suspend the execution of commands on CBL after execution of the current command is complete.

4 – Abort current command immediately.

5-7 – Illegal for use. The effect is exactly as NOP.

Bits 4-6 RUC – This field contains the command to the receive unit. Valid
(3 bits) values are–

0 – NOP (does not alter current state of unit).

1 – Start packet reception. If a packet is being received, then complete reception before starting. The begin-

ning of the RFA (the RDL) is contained in RFA OFFSET.

2 – Resume packet reception (only when in suspended state).

3 – Suspend packet reception. If a packet is being received, then complete its reception before suspension.

4 – Abort receiver operation immediately.

5-7– Illegal for use. The effect is exactly as NOP.

Bit 7 RES – Reset chip (logically the same as hardware RESET).

CBL Offset – This 16-bit quantity specifies the offset portion of the address for the first command block on the CBL. It is accessed only if CUC = Start.

RFA OFFSET – This 16-bit quantity specifies the offset portion of the address for the RPA. It is accessed only if RUC = Start.

CRCERRS Counter – This 16-bit quantity contains the number of aligned packets discarded because of a CRC error. This counter is updated, if needed, in all RU states.

ALNERRS Counter – This 16-bit quantity contains the number of misaligned packets discarded. This counter is updated, if needed, in all RU states.

RSCERRS Counter – This 16-bit quantity contains the number of good packets discarded because there were no resources to receive them. Packets intended for a host whose RU is in the No Receive Resources state, fall into this category. This counter is updated only if the RU is in the No Resources state.

OVRNERRS Counter – This 16-bit quantity contains the number of packets that are known to be lost due to a lack of local system bus availability.

If the traffic problem period lasts for more than one packet, the packets that follow the first one are lost without any indicator and are not counted. This counter is updated, if needed in all RU states.

Error Counter Operation

- The 80186 clears all error counters prior to initiating the 82586. The 82586 updates these counters by reading them, adding one and writing back to their SCB positions. Multiple errors cause all relevant counters to update.

- The counters after reaching the value of FFFFH do not wrap around to zero. They will stay at FFFFH unless modified by the 80186.

- The 82586 will update all the statistical counters after every packet.

- The 82586 performs the read counter/increment/write counter operation without relinquishing the bus. This is done to ensure that no logical contention exists between the 82586 and the 80186. In a dual port memory configuration, the 80186 should perform no write operation to a counter unless the counter is in the FFFFH state. Otherwise, it is possible that the write operation will be overwritten by the 82586 that has recently read "old" information from the counter. Because the 82586 does not write to the counter when the FFFFH state is reached, the 80186 may safely reset the counter.

Software Reset Operation

Upon reading a Reset bit in the SCB command word, the 82586 –

- Terminates the Transmit and Receive processes.
- Ignores the remaining SCB command field.
- Clears the SBC command word.
- Resets the chip.

After the 82586 clears the SCB command word, the reset effectively starts. Note that INT is not raised. To trigger the initialization procedure, the 80186 must wait at least 10 system clocks before issuing the CA to the 82586.

4.4.2.1 Control Command Semantics

Control Commands are submitted independently to the RU and CU. The explanation below applies for both RU and CU control commands.

The commands are treated by the 82586 in two phases. The first phase is CONTROL COMMAND ACCEPTANCE. Its termination is indicated by the 82586 clearing the SCB command word. Acceptance is complete after the 82586 has responded to the 80186's request, read the command from the SCB command word, and performed the required activities (which depend on the state of the CU or RU).

The second phase, CONTROL COMMAND EXECUTION, is performed as soon as the current CU or RU activity (at CB or PD level) is finished. For the CU, it happens when the Command Block currently in execution is completed. For the RU, it happens when the packet currently in reception has ended.

Both the CU and RU have a pointer to the next CB (for CU) or RPD (for RU). NEXT CB points to the Command Block to be executed after the current CB is completed. NEXT RPD points to the RPD to be set up after the present packet is received.

4.4.2.2 Control Command Effects

Start – This command specifies the list of CBs or RPDs. The NEXT CB or NEXT RPD pointer is always updated. If the unit is not active during acceptance (i.e., the CU is not executing CBs or the RU is not receiving a packet), the next CB or RPD is immediately set up. In this case, the acceptance and execution phases overlap. If the unit is active during acceptance, the next CB or RPD will be set up at the end of the current activity (execution phase). In all cases, the next state of the units is READY.

Abort – At acceptance time, this command causes the immediate termination of CU or RU activities. End of execution is signalled by the CU or RU entering its idle state.

Suspend - This command is ignored if the unit is not READY at acceptance time. If the unit is READY, the present activity is completed (CB execution for CU and packet reception for RU), and the unit becomes suspended.

Resume - This command is ignored if the unit is not SUSPENDED. If during acceptance, the unit is not active (CB execution for CU, packet reception for RU), then NEXT CB or NEXT RPD is set up. Otherwise, the NEXT CB or NEXT RPD is set up at the end of the current activity. In any case, the new state of CU or RU after execution is READY.

At the end of the activity (CB completion or reception of a packet completed), the CU or RU assesses its situation based upon E and S bit status. If EL is set, the last CB or RPD was exhausted. The CU becomes IDLE or the RU enters its No Resources state, regardless of any other factor. If S is set, the unit becomes suspended.

Requests Remembered from Acceptance Time

- o If a Suspend is requested, the unit becomes SUSPENDED.
- o If a Start is requested, the unit enters its READY state and CB or RPD setup follows.
- o If no request is pending, CB or RPD setup follows per the Command Block List or Receive Frame List.

4.4.2.3 Rules for Using Control Commands

Handshake

The 80186 writes the control command to the SCB command word, then causes a falling edge to the CA input.

The 82586, after a finite but undefined number of clocks, recognizes the CA transition and performs its control command acceptance procedure, as described in Section 4.4.2.7 (for the CU) or Section 4.4.3 (for the RU). At the end of the sequence, the 82586 clears the whole SCB command word and places current CU and RU status into the SCB.

At this time, the 80186 is allowed to issue the next control command to the 82586.

A new accepted control command cancels a previous control command that was accepted and awaits execution. Note that a NOP control command does not cancel previous commands, thereby allowing interrupts to be acknowledged without disturbing CU and RU operation.

Normal Operation

The 80186 is notified that the control command was accepted by the 82586. This notification is signalled by the 82586 clearing the SCB command word.

The execution of control commands may be deferred because of the CU and RU being active (CB execution or packet reception) at command acceptance time.

When control command execution is complete, the new status of the CU and RU is reported.

The only state transitions that are specifically signalled, with interrupt to the 80186, are RU and CU becoming not READY. Interrupt also happens at the completion of a CB (with I-bit set) and after completing reception of a packet.

4.4.2.4 The Command Unit

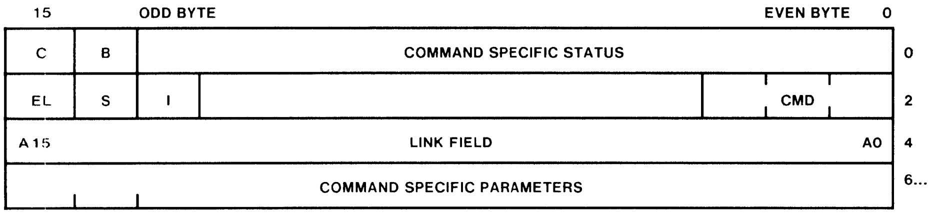
The CU is responsible for handling commands from the 80186. These commands fall into two categories: control and action. This section is concerned primarily with control commands and the generic class of action commands. Action commands are discussed in detail in Section 4.5.

Control commands are the means by which the 80186 controls the CU's execution of action commands. Action commands are located in CBs, then linked together to form the CBL. The CBL may contain one or more CBs. The last CB is indicated by the End List (EL) bit in the CB being a one. The CU starts at the beginning of the CBL and executes the commands, one at a time, until it reaches the CB where EL = 1.

4.4.2.5 Command Blocks

Action commands are organized in CBs. The beginning of the CBL is defined by the CBL OFFSET in the SCB and its end is indicated by the EL bit (EL = 1) in the last CB.

The generalized form of the command block is –



122136-25

where

STATUS – This 14-bit field contains the command results. It is set at the same time as the C bit. The field is not valid until C = 1.

Bit 13 – Indicates that the command was executed without error. If one, then no error occurred (command executed 0). If zero, then an error did occur and the remaining bits should be consulted to discover what the problem was.

Bit 12 – If set, indicates that the command was abnormally terminated due to CU Abort control command. If one, the command was aborted and, if necessary, should be repeated. If bit 12 is 0, the command was not aborted.

LINK FIELD – A 16-bit pointer to the next command block.

EL – If set, this bit indicates that this command block is the last on the CBL.

S – If set to 1, the CU is suspended upon completion of this CB.

I – If set to 1, the 82586 generates an interrupt after command execution is completed. If I is not set to 1, the CX bit is not set.

CMD – A 3-bit field that specifies the op code of the command. See Section 4.5 of this manual.

Bits 4-12 – Reserved.

C – This bit indicates the execution status of the command. The 80186 initially sets it to zero when the CB is placed on the CBL. Following a command execution, the 82586 sets it to one.

B – This bit indicates that the 82586 is currently executing this command. It is initially set to 0 by the 80186. The 82586 sets it to one when execution begins and to 0 when execution is complete.
Note that the C and B bits are modified in one operation.

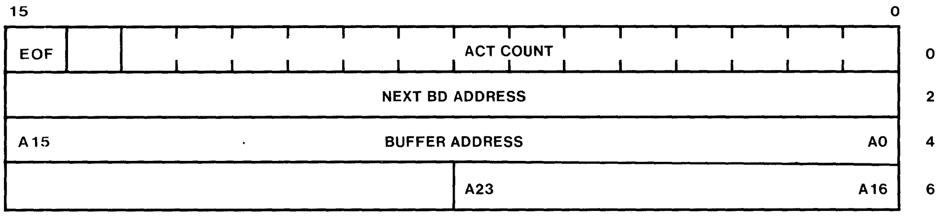
COMMAND SPECIFIC PARAMETERS – This is a variable length field that contains parameters for and/or results from the command. Its length and contents are command dependent.

CBs are chained together to form the CBL. When searching the CBL after an interrupt, the 80186 can remove any block with C = 1, since execution is complete. The forward link in the last CB may be used to form a cyclic list.

4.4.2.6 Transmit Buffer Descriptor

The transmit command accesses user data found in buffers for Transmit operations. Each buffer is described by a Transmit Buffer Descriptor (TBD). TBDs are used with Transmit commands to contain user data that is to be sent. The TBDs are linked together to form a packet. They are automatically prefetched by the CU as required. Each command may contain zero or more TBDs.

The format of the TBD is–



122136-26

where

EOF – This bit indicates that this TBD is the last one associated with the packet being transmitted. The bit is set by the 80186 before transmitting.

ACT–COUNT – The 14-bit quantity that specifies the number of bytes in the buffer that holds information for the current buffer. It is set by the 80186 before transmit.

NEXT BD ADDRESS– The offset portion of the address of the next TBD on the list. It is meaningless if EOF = 1.

BUFFER ADDRESS – The starting address of the memory area that contains the data to be sent. This address is a 24-bit physical address. In WORD mode the buffer address must be even.

4.4.2.7 Command Unit Control

The CU may be in one of three major states during normal operation. These states are –

IDLE – In this state the CU has no action commands to execute, although it responds to control commands. The CU is initialized to IDLE.

SUSPENDED – This state is similiar to IDLE, except that the CU may become READY by a Resume command. It remembers the state of the CBL list. The CU comes to this state only via a Suspend control command or by executing a CB with S = 1.

READY – In this state, the CU is executing commands on the CBL.

The following events (a, b, or c) cause the CU to change states:

a. All Control Commands. The control commands are:

NOP – This command is ignored by the CU.

SUSPEND – This command suspends operation of the CU when the currently executing command is complete.

RESUME – This command returns the CU to the READY state from the SUSPENDED STATE.

START – This command gives the CU a new CBL to work on.

ABORT – This command stops the CU immediately. Execution of commands is stopped.

b. Action command (whose CB has S = 1) has been executed.

c. The end of the CBL is reached.

Multiple events may occur concurrently.

SET UP CB means start processing the next command in the queue. REQUEST SUSPEND means the suspend will be executed as soon as the currently executed command is furnished.

Most transitions do not cause interrupts. In actual operation, CX interrupts are the most common. When the 80186 receives an interrupt, it examines the CBL and removes all CBs with C = 1. The 80186 should always keep the pointer to the first unexecuted CB.

After the initialization process is complete (see Section 4.4.6), the CU issues a command executed (CX) and a CU not ready interrupt. The 80186 must be expecting such interrupts at the end of the initialization process.

Table 4-9 shows the CU activities at the end of control command execution time.

Table 4-9. CU Activities Performed at the End of Execution

EL Bit	S Bit	Request	Next State	Action
0	0	None	Ready	Set UP CB
0	0	Suspend	Suspended	CNR Interrupt
0	1	None	Suspended	CNR Interrupt
0	1	Suspend	Suspended	CNR Interrupt
1	0	None	Idle	CNR, CX Interrupt
1	0	Suspend	Idle	CNR, CX Interrupt
1	1	None	Idle	CNR, CX Interrupt
1	1	Suspend	Idle	CNR, CX Interrupt

Note: After a CB with I-bit set is completed, CX interrupt is generated.

4.4.3 The Receive Unit

The RU handles all activities related to packet reception. It operates independently of the CU, although it does use the CU to communicate with the 80186. The RU manages a pool of free space called the RPA that consists of two lists: Received Packet List (RPL) and Free Packet List (FPL). The SCB points to the RPL and the last packet in the RPL points to the FPL.

The Free Packet List (FFL) consists of two lists. The first lists free Receive Packet Descriptors (RPD), called the Receive Descriptor List (RDL). The second lists free buffers called the Free Buffer List (FBL). Each free buffer is described by Receive Buffer Descriptor (RBD) (see Figure 4-13). The Root of the FBL is the first RFD on the RDL .

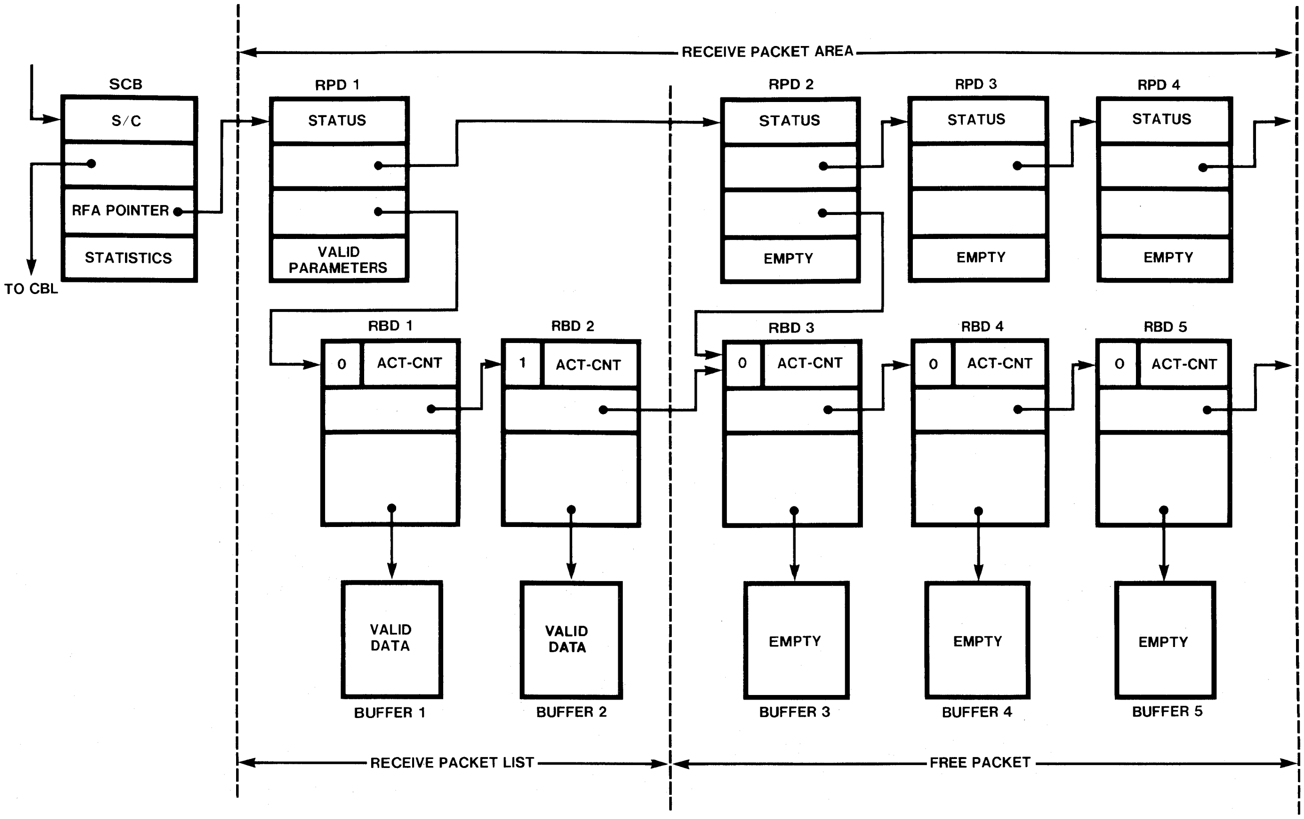


Figure 4-13. Receive Frame Area

122136-27

The address of the Receive Frame Area (RFA) (the first RFD on the RDL) is given to the RU by the 80186 issuing a SCB. One RFD is used for each received packet and as many RBDs (actually the buffers associated with each) as are required to contain the packet.

When either list is exhausted the RU notifies the 80186 and enters the No Resources state.

4.4.3.1 The Receive Packet Descriptor

Each received packet is described by one Received Packet Descriptor. The RPD at the head of the RDL is used.

The format of the receive packet descriptor is –

15		ODD BYTE	EVEN BYTE	0	
C	B	STATUS			0
EL	S				2
A15		LINK ADDRESS		A0	4
A15		BD-PTR		A0	6
2ND BYTE			1ST BYTE	MC	8
		DESTINATION ADDRESS			10
NTH BYTE					12
2ND BYTE			1ST BYTE		14
		SOURCE ADDRESS			16
NTH BYTE					18
2ND BYTE		TYPE FIELD	1ST BYTE		20

122136-28

where

STATUS – The results of the receive packet descriptor operation. Defined bits are –

Bit 13 – Packet received without errors.
Bit 12 – Reserved – unused.

Bit 11 – CRC error in an aligned packet.
Bit 10 – Alignment error (CRC error in misaligned packet).
Bit 9 – Ran out of buffer space.
Bit 8 – DMA overrun.
Bit 7 – Packet too short.
Bit 6 – No EOF flag (for bitstuffing only).
Bit 0-5 – Reserved - unused.

RPDs with Bit 13 not equal to one will occur only if the SAVE-BAD PACKET configuration option is selected. Otherwise all packets with errors will be discarded, although statistics will be kept on them.

Link Address – The 16-bit pointer to the next RPD. The Link Address of the last packet can be used to form a cyclic list.

EL – If set, this bit indicates that this RPD is the last one on the RDL.

S – If set, suspend the RU after receiving this packet.

C – This bit indicates the completion of packet reception. It is set by the 82586.

B – This bit indicates that the 82586 is currently receiving this packet or that the 82586 is ready to receive the packet. It is initially set to zero by the 80186. The 82586 sets it to 1 when reception set up begins, and to 0 upon completion. The C and B bits are set in one operation.

BD-PTR – The offset portion of the address of the first RBD containing packet data. BD-PTR = 0FFFFH indicates no RBD.

MC – Multicast bit.

DESTINATION ADDRESS – The contents of the destination address of the receive packet. The field is 0 to 6 bytes long.

SOURCE ADDRESS – The contents of the source address field of the received packet. It is 0 to 6 bytes long.

Type Field – The contents of the type field of the received packet. It is 2 bytes long.

NOTES:

1. The last four fields will not be used when the 82586 is configured to locate address/control in the data buffers (AC-LOC=1).

2. The last four fields are packed; i.e., one field immediately follows the next.

The receive buffers can be different lengths. The 82586 will place no more bytes into a buffer than the associated RBD indicates. The 82586 will prefetch the next RBD in time to use it.

Before starting the RU, the 80186 must place the pointer to the FBL in the BD-PTR field of the first RPD. All remaining BD-PTR fields for subsequent RPDs should be FFFFH.

If the RPD and the associated receive buffers are not reused (packet is well received or the 82586 works in a mode where it saves bad packets), the 82586 writes to the BD-PTR field of the next RPD, which is the address pointer of the next free RBD.

4.4.3.2 Receive Buffer Descriptor (RBD)

The information field of a packet is not part of a RPD, but is accessed with a special pointer to a separate block in order to provide the flexibility of separating the control from the information. The packet's information field is placed in a set of buffers that are chained by a sequence of RBDs. An RPD points to the first RBD, and the last RBD is flagged with an EOF set to one. The format of the receive buffer descriptor format is–

15				0	
EOF	F	ACT COUNT			0
NEXT BD ADDRESS					2
A15		BUFFER ADDRESS		A0	4
			A23	A16	6
EL		SIZE			8

122136-29

where

EOF – Indicates that this is the last buffer related to the packet. It is cleared by the 80186 before starting the RU and written by the 82586 at the end of reception of the packet.

F – Indicates that this buffer has already been used. The actual count has no meaning unless the F bit equals one. This bit is cleared by the 80186 before starting the RU, and set by the 82586 after the associated buffer has already been used.

ACT COUNT – This 14 bit quantity indicates the number of meaningful bytes in the buffer. It is cleared by the 80186 before starting the RU and written by the 82586 after the associated buffer has been used. In general, after the buffer is full, ACT COUNT value equals the size field of the same buffer. For the last buffer packet, ACT COUNT may be less than the buffer size. Note that if the Actual Count is odd (in word mode), garbage will be written to the 82586 into the high byte of the last word.

NEXT BD ADDRESS – The offset portion of the address of the next RBD on the list. It is meaningless if EL = 1.

BUFFER ADDRESS – The starting address of the memory area that contains the data that was received. This is a 24-bit physical address. In word mode, the buffer address must be even.

EL – Indicates that the associated buffer to this RBD is last in the FBL.

SIZE – This 14-bit quantity indicates the size, in bytes, of the associated buffer. In word mode, the quantity must be even.

4.4.3.3 Receive Unit Control

The RU may be in one of four states:

These states are–

IDLE – In this state the RU does not respond to packets on the serial link and does not modify any data structures. The RU is initialized to this state.

SUSPENDED – This state is similiar to IDLE, except that the RU may become READY by means of a Resume command. It remembers the state of the RPA lists. It comes to this state via a SUSPEND control command or use of a RPD with S = 1.

NO RESOURCES – In this state, the RU is looking for packets on the serial link, but has no buffers in which to store them. The RU will keep statistics on how many packets were lost.

READY – In this state, the RU looks for packets, but has buffers in which to store them.

In each of these states, the RU may or may not be receiving a packet. The situation in which a packet is being received is called RU Actively Receiving. If the RU is READY and Actively Receiving, the packet is stored in the RPA buffers. If the RU is not READY (IDLE, SUSPENDED, or NO RESOURCES), the packet is discarded. The RU still maintains statistics on CRC, Alignment, or Overrun errors for discarded packets, although the packets themselves are lost.

The following events may cause the RU to change states:

a. All Control Commands, which are the following:

NOP – This command is ignored by the RU.

SUSPEND – This command suspends operation of the RU when the packet reception is completed.

RESUME – This command causes RU transition from SUSPENDED state to READY state.

START – This command gives the RU a new RPA to work on. The RU is exited to READY state.

ABORT – This command stops the RU immediately. Reception of any packet is stopped and the CU goes into the IDLE state.

b. A packet is received using a RPD with S = 1.

c. The end of the RDL or FBL is reached.

Most transitions do not cause interrupts. Most interrupts are caused by packets being received. When the 80186 gets a PR interrupt, it should scan down the RDL, removing all RPDs where C = 1. There may be more than one RPD. The 80186 should keep a pointer to the head of the RDL.

The RU Not Ready (RNR) interrupt might be caused by a control command issued by the 80186 to the RU, reception of a packet using a RPD with S = 1, or the exhaustion of either (or both) the RDL or FBL.

By testing the S and EL bits of the last RFD, the 80186 can identify the reason for the RNR interrupt.

Table 4-10 shows the RU activities at control command execution time.

Regardless of its state, the RU looks for start requests at the end of a receive packet. This guarantees that packets are housed either in the old RPA or entirely in the new RPA. A sharp transition takes place at the end of the receive packet from the old RPA to the new RPA.

Table 4-10. RU Activities Performed at the End of Execution

EL Bit	S Bit	Request	Next State	Action
0	0	None	Ready	Set up RPD
0	0	Suspend	Suspended	RNR interrupt
0	0	Start	Ready	Set Up RPD
0	1	None	Suspended	RNR interrupt
0	1	Suspend	Suspended	RNR interrupt
0	1	Start	Suspended	RNR interrupt
1	0	None	No resources	RNR interrupt
1	0	Suspend	No resources	RNR interrupt
1	0	Start	Ready	Set up RPD
1	1	None	Idle	RNR interrupt
1	1	Suspend	Idle	RNR interrupt
1	1	Start	Ready	Set up RPD

Note: After a packet is received, an FR interrupt is generated.

Note that the process of starting the RU takes time. During this time, receive packets may be lost due to a temporary lack of memory resources. This situation may arise even if the previous RPA has enough resources to contain the incoming packet.

Depending on the 82586 internal state, the RSCERR or OVRNERR counters in SBC are updated. CRCERR and ALNERR counters are updated as usual.

4.4.4 Interrupt Operation

The INT pin is used to notify the 80186 about one or more of the following events:

- A command in the CB with its I bit set was executed (CX interrupt).
- A packet was received (PR interrupt).
- The CU became Not Ready (CNR interrupt).
- The RU became Not Ready (RNR interrupt).

4.4.4.1 Interrupt Request Sequence

Once an event requiring an interrupt has occurred, the following sequence is performed by the 82586:

1. INT pin is set to its low level (inactive).

2. The status word in SCB is written, denoting the source of the interrupt (CX, PR, CNR, or RNR interrupt), together with the states of the CU and RU.

3. INT pin is raised (set to active).

4.4.4.2 Interrupt Servicing by the 80186

Upon detecting a rising edge on the INT pin, the 80186 may perform its interrupt service routine, as follows:

1. Saves registers.

2. Waits until the SCB command word is all 0's.

3. Reads SCB STATUS field.

4. Determines the cause(s) of the interrupt and the states of the CU and RU.

5. Processes each interrupt cause and determines the next control commands for the CU and RU.

6. Writes Interrupt Acknowledge bits to the processed interrupt requests together with the next control commands for CU and RU.

7. Issues a CA falling edge to the 82586.

8. Restores registers and exits interrupt routines.

4.4.4.3 82586 Response to CA

Upon detecting a falling edge on its CA input, the 82586 performs the CA acceptance sequence, as follows:

1. Determines which interrupt requests were acknowledged by the 80186. For each of them, the 82586 clears the corresponding interrrupt request bit in the SCB status word.

2. Performs the control command acceptance procedure.

3. Sets INT pin low.

4. Writes the SBC status word indicating the unacknowledged interrupt request, and newly-generated interrupt requests, together with the CU and RU states.

5. Sets the INT pin high if any interrupt request bit is active.

4.4.4.4 Initialization Procedure

82586 Actions

- After Reset (either hardware or software), the 82586 sets the INT pin to a low level (inactive).

- The 82586 waits for a CA high-to-low transition.

- When CA makes its high-to-low transition, the initialization procedure is performed. Upon completion, the CX (Command Executed) and CNR (CU became Not Ready) interrupts are written to the SCB status word, together with the status of CU and RU (both are idle).

- The 82586 then sets the INT pin to HIGH.

80186 Actions

- 80186 should expect interrupts as part of the 82586 initialization procedure.
- The 80186 writes the control commands for the CU and RU (typically STARTing both) and acknowledges the CX and CNR interrupts.
- It issues a CA to the 82586 and the INT/CA handshake mechanism keeps rolling on by itself.

4.4.5 Interaction between Control and Action Commands

4.4.5.1 82586 Channel Attention (CA)

The CU is responsible for control command acceptance, following the falling edge on the CA input. The CU first finishes all its higher priority activities and only then accepts the control commands.

Higher priority CU activities that delay CA acceptance are –

- Transmit BD prefetch.
- Transmit buffer switching.
- Current CB command completion.

The 82586 will accept a CA prior to the set up of the next CB in the CBL.

The CU recognizes an RU control command and notifies the RU. The RU first finishes all higher priority activities, and only then accepts the control command.

Higher priority RU activities that delay CA acceptance are –

- Receive BD prefetch.
- Receive buffer switching.
- Receive end of packet processing.

Only after the CU and RU have accepted the control command is the SCB command word cleared. At that time the 80186 may issue the next CA to the 82586.

In the 82586, the CA falling edge is detected and latched. The 82586 cleared the latch before reading the SCB control command. A new CA, given to the 82586 before the SCB command word is cleared, may be lost if the latch is cleared before being serviced. The user must refrain from such violations.

The 82586 does not wait until reception or transmission ends to process a CA. The SCB related operations are carried out on an interleaved basis with the transmission or reception process.

4.4.5.2 Critical Regions in the Interface to the 80186

Common Bus Operation

When the 82586 and the 80186 reside on the same system bus, the bus acquisition and release is governed by the HOLD/HLDA protocol. This scheme ensures that only one bus master at a time owns the bus.

The 82586 performs its bus accesses to a descriptor in memory without relinquishing the bus. This results in a certain number of system clocks where the system bus is owned by the 82586, but no bus activity occurs.

The only way the 80186 can force the 82586 off the bus during descriptor processing is to drop HLDA. In this case, the 80186 and any other master peripheral must refrain from modifying the 82586 memory control structure.

The affected descriptors are –

- Command Blocks.
- Receive Packet Descriptors.
- Transmit Buffer Descriptors.
- Receive Buffer Descriptors.
- System Control Blocks.

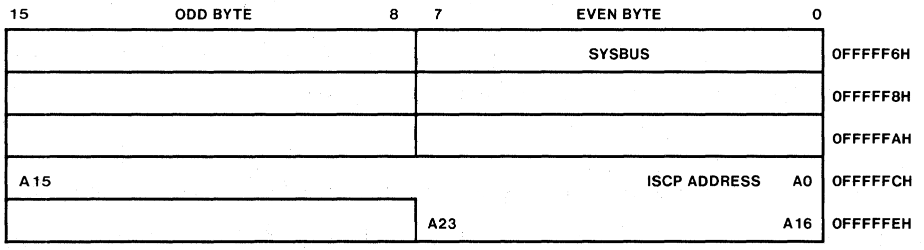
4.4.6 Initialization and Configuration

The 82586 accesses the Initialization Root as part of the initialization sequence begun after CA is asserted for the first time following a RESET. The Initialization Root consists of two data structures addressed via two pointers: the System Configuration Pointer (SCP) and the Intermediate System Configuration Pointer (ISCP).

The primary purpose of this process, in addition to getting the 82586 into a stable state, is to locate the SCB and thus define the 64K byte page in which all command/control structures are located.

4.4.6.1 The System Configuration Pointer

The SCP begins at a location 0FFFF6H and is the only fixed address data structure in an 82586 system. Its purpose is to specify the width of the data bus used by the 82586 (8 or 16-bits), as well as the location of the ISCP. The SCP for the 82586 shares the location 0FFFF6H with the SCPs of all other master peripherals. The format of the SCP is –



122136-30

where

SYSBUS – Specifies whether the system data bus available to the 82586 is 8 bits or 16 bits wide. A 1 indicates 8 bits and a 0 indicates 16 bits. During the first read operation from the SCP, the 82586 assumes a byte wide bus, reading the SYSBUS byte. The bus width goes into effect immediately after SYSBUS is read.

ISCP ADDRESS – A 24-bit quantity that is the physical address of the ISCP.

4.4.6.2 The Intermediate System Configuration Pointer

The ISCP specifies the SCB's location. Usually, all Master peripherals in a system share the same ISCP address. The SCP is often in ROM with the ISCP in RAM. The 80186 loads the address of the SCB (or an equivalent data structure) for each master peripheral into the ISCP and asserts the peripheral's CA. The 82586 then begins the initialization procedure to fetch the address of the SCB via the SCP and ISCP.

The SCB's base address is also the base address of all Command Blocks, Packet Descriptors, and Buffer Descriptors (but not buffers) in the system. All such data structures must exist in a 64K byte segment. The format of the ISCP is–

15	ODD BYTE	8	7	EVEN BYTE	0	
				BUSY		ISCP
A15	SCB OFFSET				A0	ISCP + 2
A15				SBC BASE	A0	SCP + 4
			A23		A16	ISCP + 6

122136-64

where

BUSY – Indicates that the 82586 is being initialized. It is set to 01H by the 80186 before its first CA to the 82586. It is cleared by the 82586 after the SCB base address and offset are read. Note that the most significant byte of the first word of the ISCP is not modified when BUSY is cleared.

SCB OFFSET – This 16-bit quantity specifies the offset portion of the SCB's address.

SCB BASE – This 24-bit quantity specifies the base portion of the address of the SCB. The base of the SCB is also the base of all 82586 CBs and BDs.

NOTE

All descriptors (segment addresses) must start at even addresses in word mode.

4.4.6.3 Initialization Procedure

The 80186 sets up the SCP, ISCP, and the SCB structures. It also sets BUSY to 01H. The initialization procedure is started by the CA following a RESET. This CA causes the 82586 to access the SCP at locations 0FFFF6H (see Figure 4-14). The SYSBUS byte is fetched in byte mode. Once the bus width is determined, all further memory transfers will be at the specified bus width. After the SCP is addressed, the 82586 fetches the ISCP. The 82586 saves the base of the SCB (that is, the base of all control blocks), as well as the SCB address. It clears busy, sets CX=1 and CNR=1 in the SCB, clears the SCB command word, signals an interrupt to the 80186 and waits for a CA.

Prior to the CA, the RESET configures the 82586 to the operational mode compatible with the Ethernet standard. Only Broadcast Address is accepted by the 82586 until an Individual Address is set up. If necessary parameters can be changed with a CONFIGURE Command,

4.4.7 Configuration

Operation parameters are loaded into the 82586 via the configure command.

FIFO Limit

Specifies the point in the FIFO at which the 82586 requests the bus in order to transfer data to/from its internal FIFO from/to memory.

SRDY/ARDY

Selects between synchronous ready function and asynchronous ready function.

0 ARDY – Asynchronous Ready; i.e., the Ready signal is internally synchronized by the 82586, adding one wait state to the 82586 bus cycle.

1 SRDY – Synchronous Ready; i.e., the Ready signal is externally synchronized.

Save-Bad Packet

Specifies whether errored packets (CRC error, Alignment error, etc.) are to be discarded (0) or saved (1). In Save Bad-Packet mode, the Receive Packet Descriptor, as well as the Receive Buffer Descriptors and Receive Buffers, are NOT reused for the next packet. In the complementary mode, all the descriptors and buffers used for bad packets are reused thus, leaving no information about the lost packet except for statistical tally updates.

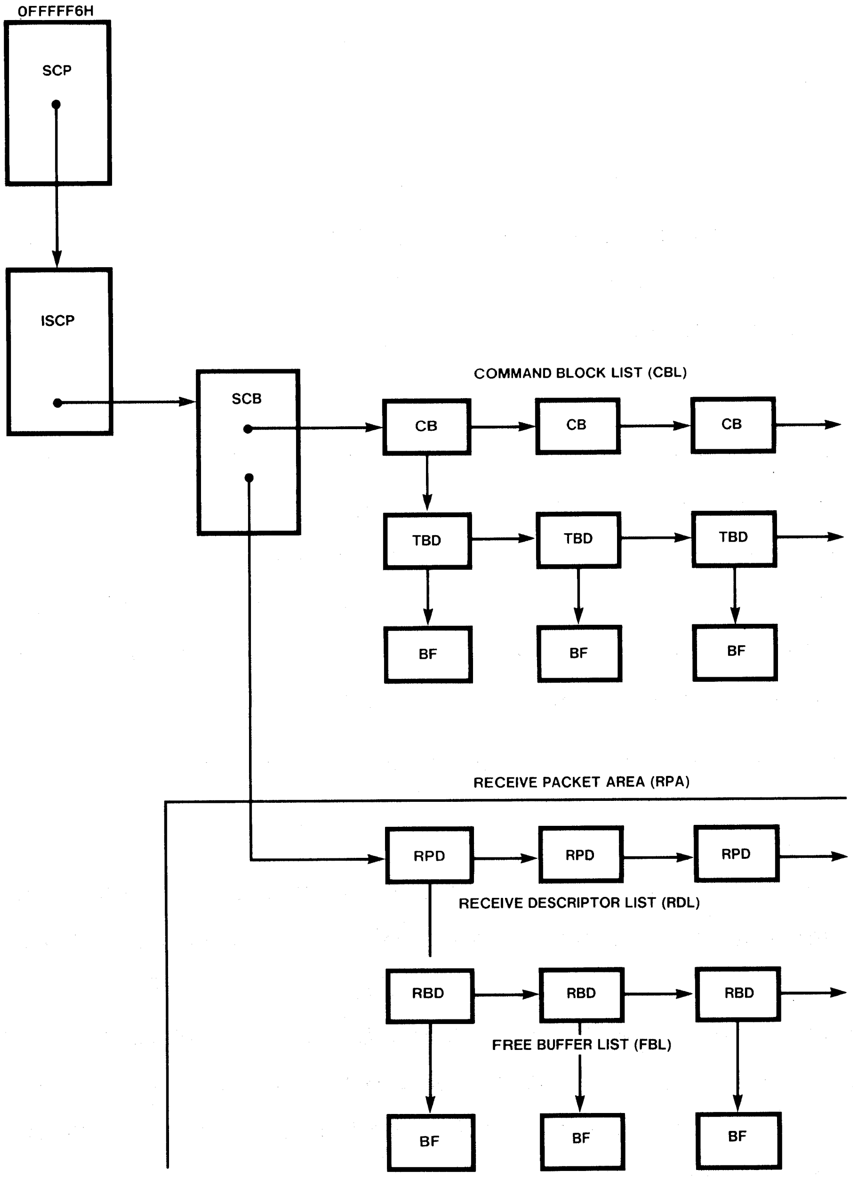


Figure 4-14. The Shared 82586/80186 Memory Structure

122136-31

Address Length

Determines the length (in bytes) of the address to which the 82586 refers. This includes source, destination, multicast, or broadcast addresses.

Address/Control Field Location

0 – Address and control type are located in consecutive bytes in the descriptor.

1 – The whole packet is located in the data buffers. Source address insertion by the transmitting the 82586, is disabled.

INT-Loopback (Internal Loopback)

When set, the 82586 disconnects itself from the serial wire and logically connects TxD to RxD and TxC to TRC. TxC must still be supplied by the user. Internally, TxC is divided by 4, slowing down the serial bit rate enough to enable 82586 operation in full duplex mode. This action alters the effective values of all configure command parameters defined in terms of TxC. Note that the INT-Loopback bit set, at the same time as EXT-Loopback, causes the 82586 to operate in Internal Loopback Mode.

EXT-Loopback (External Loopback)

The 82586 will receive and transmit simultaneously, at full rate, a packet limited to 18 bytes (including the Packet Check Sequence). This capability allows checking of external hardware as well as the serial link to the transceiver. Because the transmitted data for Ethernet transceivers is fed back via the receive pair, practically nothing has to be done to perform EXT Loopback. For other transceiver types, the user is responsible for external transmit-receive interconnection.

Note that the INT Loopback bit overrides the EXT Loopback bit.

Linear Priority

The linear priority bits define the amount of delay (expressed in Slot Time period units) that a station will delay transmission after Interpacket Spacing.

For linear priority greater than zero, the 82586 checks the Carrier Sense of the timeout completion. If the station senses a carrier, it assumes that a higher priority station (with a lower linear priority number) grabbed the link and withholds itself from transmission.

Exponential Priority

This number provides priority by affecting the average Exponential Backoff delay. If

EP – is the exponential priority number,

N – is the number of collisions,

r – is random number multiplicant of the Slot Time,

then r is chosen randomly according to the following:

$$0 \; r \; 2^{(N+EP,\ 10)}$$

Thus, for EP = 0, we simply get the Ethernet Exponential Backoff Delay.

Exponential Backoff Method

Determines when to start the backoff timeout:

0 – According to the three–company standard, exponential backoff occurs immediately after the jamming, concurrent with Interpacket spacing.

1 – Exponential backoff starts after the deferring period expires. This method prevents inefficiency and throughput loss at short topologies and low bit rates where Interpacket Spacing may be longer than the Slot Time.

Interframe Spacing

Specifies the time (in TxC units) the 82586 must wait after detecting loss of Carrier Sense before it can begin transmission or reception of a packet. The minimum value is 32 and any value less than that defaults to 32. However, during DUMP STATUS command execution, the original configuration number is read out.

Slot Time

The network Slot Time number or the number of TxC cycles in the Slot Time. This value is the basis for backoff delay generation. Zero Slot Time number will be interpreted by the 82586 as 2048.

Promiscuous Mode

If configured to Promiscuous Mode, the 82586 accepts packets independently of the Destination Address.

Broadcast Disable

Disables the reception of packets with an even Broadcast Address via the multicast mechanism. Promiscuous Mode bit overwrites the Broadcast Disable Mode.

Manchester/NRZ

Specifies whether NRZ or Manchester encoding/decoding is to be performed:

0 – NRZ.

1 – Manchester.

Note that in Manchester mode there is a need for external receive clock recovery logic for the receive data.

Transmit on No CRS (Carrier Sense)

If set, allows transmission even if there is no CRS back from the transceiver. Important for transceivers (non–Ethernet) that do not feed back the transmitted signals via the receive pair.

No CRC (Cyclic Redundancy Check) Insertion

0 – CRC is inserted at the end of the packet.

1 – No CRC insertion (allows higher level CRC generation).

CRC–16/CRC-32

0 – 32–bit Autodin-II CRC.

1 – 16–bit CCITT CRC.

Bitstuffing/EOC

0 – End of Carrier (EOC) Framing.

1 – Bitstuffing Framing, with HDLC type start of packet/end of packet delimiters.

Padding

Only valid if Bitstuffing is set. If set to padding mode, the 82586 automatically appends flags to frames shorter than a Slot Time period. Thus the activity on the link will be for at least one Slot Time period.

CRS-Filter

Specifies the required minimal width of CRS, in TxC cycle units, before it is recognized as being Carrier Sense. The Carrier Sense Expired state is recognized immediately.

Internal CRS

Specifies whether Carrier Sense is to be generated internally or externally (via CRS pin).

0 – External.
1 – Internal.

CDT-Filter

Specifies for externally generated Collision Detect the required width of CDT, in TxC cycle units, before Collision Detect will be treated as a collision.

Internal CDT

Specifies whether Collision Detect is to be generated internally or externally (via the CDT pin).

0 – External.
1 – Internal.

Operates only with transceivers that do not feed back transmitted data on the receive pair, but can sense some other station data.

Min Packet Length

The minimum packet length in bytes. No packet that is shorter than the minimum will be accepted by the 82586.

NOTE

> Apart from this mechanism other limitations on the minimum packet length exist.
>
> First, packets shorter than 6 bytes (even in Save Bad Packet Mode, Promiscuous Mode, address length of 0) are discarded. No status is reported on such received packets.
>
> Second, for AC-LOC=0 (when Address Control Location implies data separated from control), also packets shorter than 2 x ADDR-LEN + 2 (not including the Packet Check Sequence) are discarded.

Preamble Length

Selects the length of the preamble including BOF, as follows

00 – 2 bytes.
01 – 4 bytes.
10 – 8 bytes.
11 – 16 bytes.

Number of Retries

The number of retries after collision that the 82586 will perform before the transmit attempt is aborted.

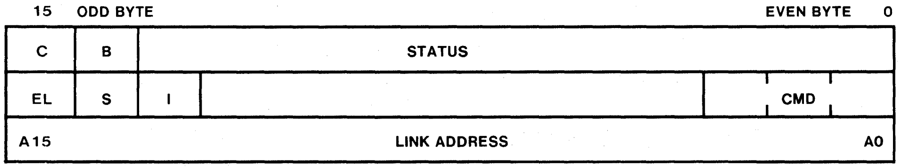
4.5 Action Commands

The action commands reside in the CBL. The general action command structure is described in Section 4.4.2.5. The three types of action commands are–

1. 82586 configuration and setup.
2. Transmission.
3. Diagnostics oriented.

4.5.1 NOP

This command results in no action by the 82586 except for that performed in normal command processes. It is present as an aid to CBL manipulation. The format of the NOP command is–



122136-32

where

LINK ADDRESS, EL, – As per standard CBs (see Section 4.4.2.5).
B, C, I, S

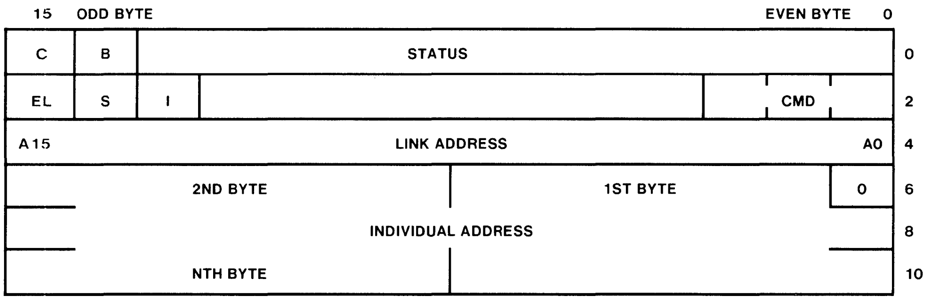
CMD – The NOP command. Value: 0H.

STATUS – Bits 12, and 13 as per standard CBs (see Section 4.4.2.5).

4.5.2 Individual Address Set-Up

This command is used to load the 82586 with the Individual Address. This address is used by the 82586 for recognition of the Destination Address and an insertion of the Source Address.

The individual address Set-Up format is–



122136-33

where

LINK ADDRESS, EL, B, C, I, S – As per standard CBs (see Section 4.4.2.5).

CMD – The Address Set-up command. Value: 1H.

STATUS – Bits 12 and 13 as per standard CBs (see Section 4.4.2.5).

NOTE

After RESET, prior to Individual Address Set-Up Command execution, the 82586 assumes the Broadcast Address as the Individual Address in all cases.

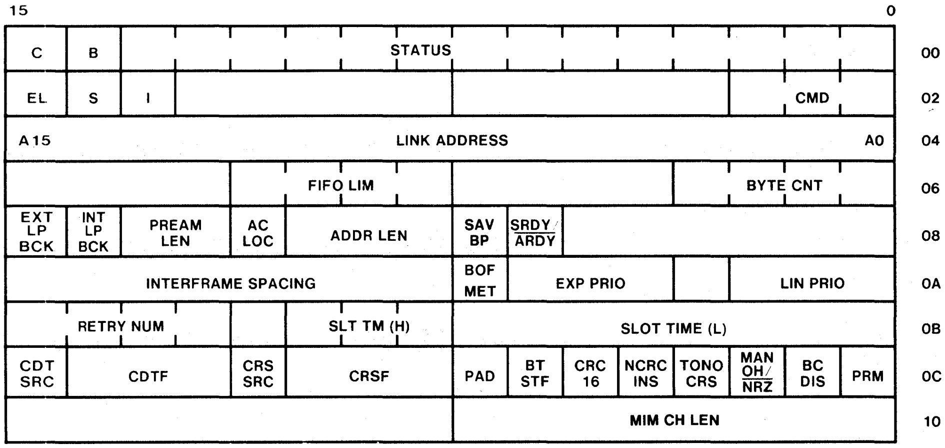
The Individual Address least significant bit must be 0 for Ethernet (see the Command Structure). However, no enforcement of 0 is provided by the 82586. Thus, Individual Address with Least significant bit 1 is a valid Individual Address in all aspects.

INDIVIDUAL ADDRESS – The individual address of the node.

4.5.3 Configure

The Configure Command is used to load the 82586 with its operating parameters. The Configure Command allows only part of the parameters to be changed by specifying a byte count of less than 12. Any number larger than 12 will be truncated to 12. Any number less than four will be rounded to four.

The format of the Configure command is–



15															0	
C	B	STATUS														00
EL	S	I											CMD			02
A15 LINK ADDRESS A0																04
				FIFO LIM								BYTE CNT				06
EXT LP BCK	INT LP BCK	PREAM LEN		AC LOC	ADDR LEN			SAV BP	SRDY/ARDY							08
INTERFRAME SPACING								BOF MET	EXP PRIO				LIN PRIO			0A
RETRY NUM					SLT TM (H)			SLOT TIME (L)								0B
CDT SRC	CDTF			CRS SRC	CRSF			PAD	BT STF	CRC 16	NCRC INS	TONO CRS	MAN OH/NRZ	BC DIS	PRM	0C
								MIM CH LEN								10

122136-34

where

Link Address
EL,B,C,I,S – As per standard CBs (see Section 4.4.2.5)..

Status – Bits 12 and 13 as per standard CBs (see Section 4.4.2.5).

CMD – The configure CMD value: 2H.

Byte 1: Byte CNT (Bits 0-3) –Byte count. Number of bytes, including this one, that holds parameters to be changed.

– Byte count. Number of bytes, including this one, that holds parameters to be configured.

NOTES:

1) If programmed to odd number in the word mode, the last byte is truncated.

2) A number smaller than four is interpreted as four.

3) A number greater than 12 is interpreted as 12.

Byte 2: FIFO-LIM (Bits 0-3) – FIFO LIMIT value.

Byte 3: SRDY/ARDY (Bit 6)

0 – SRDY/ARDY pin operates as ARDY (internal synchronization).

1 – SRDY/ARDY pin operates as SRDY (external synchronization).

SAV BF (Bit 7)

0 – Received bad packets are not saved in the memory.

1 – Received bad packets are saved in the memory.

Byte 4: ADR LEN – Number of address bytes.
(Bits 0-2)

NOTE: 7 is interpreted as 0.

AC-LOC (Bit 3)

0 – Address and Type Fields are separated from data and are associated with Transmit Command Block or RPD. For a transmitted packet, the Source Address is generated by the 82586.

1 – Address and Type Fields are part of the transmit/receive data buffers, including the Source Address.

PREAM-LEN – Preamble Length, including Beginning of Packet indicator.
(Bits 4-5)

00 - 2 bytes.
01 - 4 bytes.
10 - 8 bytes.
11 - 16 bytes.

INT LP BCK – Internal Loopback.
(Bit 6)

EXT LPBCK – External Loopback.
(Bit 7)

Note that Bits 6 and 7 configured to 1, cause Internal Loopback.

Byte 5: LIN-PRIO – Linear Priority.
(Bits 0-2)

EXP-PRIO – Exponential Priority.
(Bits 4-6)

BOF-MET (Bit 7) – Exponential Backoff Method:

0 – Ethernet.

1 – Short Topology and/or Low Bit Rate (Interpacket Spacing Shorter than the Slot Time).

Byte 6: INTERFRAME SPACING – Number that indicates the Interpacket Spacing in TxC period units.

Note that a number smaller than 32 is interpreted as 32.

Byte 7: SLOT TIME (L) – Slot Time Number, low byte.

Byte 8: SLT-TM (H) (Bits 0-2) – Slot Time Number, high byte.

Note that (1) Slot Time is the Slot Time number of TxC period units, and (2) Slot Time Number of zero is interpreted as 2048 (2^{11}).

RETRY-NUM– (Bits 4-7) Number of transmission retries on collisions.

where

Byte 9: PRM (Bit 0) – Promiscuous mode:

0 – Non–Promiscuous address filtering mode.

1 – Promiscuous Mode.

BC–DIS (Bit 1) – Broadcast Disable

0 – Broadcasted packets accepted.

1 – Broadcasted packets rejected.

MANCH/NRZ (Bit 2) – Manchester or NRZ encoding/decoding.

0 – NRZ.

1 – Manchester.

TONO-CRS – Transmit or No Carrier Sense:
(Bit 3)
0 – Cease transmission if CRS goes inactive during packet transmission (after preamble is sent).
1 – Continue transmission even if there is no Carrier Sense.

NCRC-INS – No CRC Insertion:
(Bit 4)
0 – 82586 generates and appends FCS to transmitted packets.

CRC-16 – CRC Type:
(Bit 5)
0 – 32 bit Autodin II CRC polynomial.
1 – 16 bit CCITT CRC polynomial.

BT-STF – Bitstuffing:
(Bit 6)
0 – End of Carrier Mode (Ethernet).
1 – HDLC like Bitstuffing mode.

PAD – Padding:
(Bit 7)
0 – No padding.
1 – Perform padding by transmitting flags for the rest of the slot time.

Note that PAD has meaning only for Bitstuffing. In EOC mode, PAD value is internally enforced to zero.

where

Byte 10: CRSF – Carrier Sense Filter Bits.
(Bits 0-2)

CRS-SRC – Carrier Sense Source:
(Bit 3)
0 – Carrier Sense Signal externally generated.
1 – Carrier Sense Signal internally generated.

CDTF (Bits 4-6) – Collision Detect Filter Bits.

CDT-SRC (Bit 7) – Collision Detect Source:
0 – Collision Detect Signal externally generated.
1 – Collision Detect Signal internally generated.

Byte 11: MIN-FRM-LEN – Minimum number of bytes in a packet. Packets shorter than the MIN FRM LEN are treated as bad packets.

Configuration Defaults

The reset configures the 82586 to be compatible with the Ethernet Specifications. The configuration defaults are –

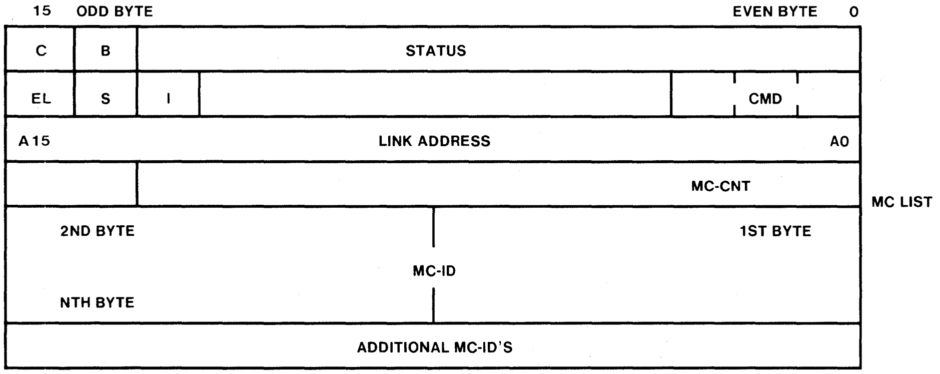
FIFO LIMIT	= 8
SRDY/ARDY	= 0
SAVE BAD FRAME	= 0
ADDRESS LENGTH	= 6
ADDRESS/CONTROL	= 0
FIELD LOCATION	= 0
INT LOOPBACK	= 0
EXT LOOPBACK	= 0
LINEAR PRIORITY	= 0
EXPONENTIAL BACKOFF METHOD	= 0
EXPONENTIAL PRIORITY	= 0
INTERFRAME SPACING	= 96
SLOT TIME	=512
PROMISCUOUS MODE	= 0
BROADCAST DISABLE	= 0
MANCHESTER/NRZ	= 0
TRANSMIT ON NO CRS	= 0
NO CRC INSERTION	= 0
CRC-16/CRC-32	= 0
BITSTUFFING/EOC	= 0
PADDING	= 0

CRS FILTER	= 0
INTERNAL CRS	= 0
INTERNAL CDT	= 0
MIN-FRAME-LENGTH	= 64
PREAMBLE LENGTH	= 2
NUMBER OF RETRIES	= 15

4.5.4 Multicast Set-Up Command

This command loads the 82586 with the Multicast-IDs that should be accepted. This command resets the current filter and reloads it with the specified Multicast-IDs.

The format of the Multicast Address Set-Up command format is–



122136-35

where

LINK ADDRESS, EL,B,C,I,S – As per standard CBs (see Section 4.4.2.5).

STATUS – Bits 12,13 per standard CBs (see Section 4.4.2.5).

CMD – The Multicast Address Setup command value: 3H.

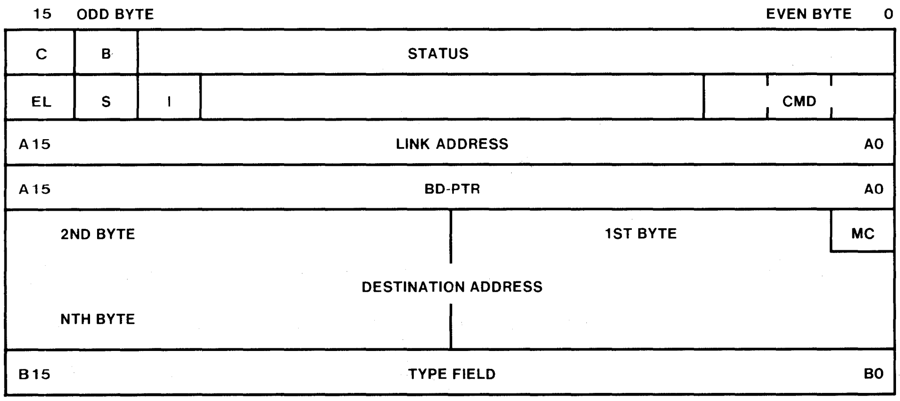
MC-CNT – This 14-bit field indicates the number of bytes in the MC LIST field. The MC-CNT must be a multiple of the ADDR-LEN; otherwise, the 82586 truncates the MC-CNT to the nearest ADDR-LEN multiple. MC-CNT=0 implies reset of the HASH table, which is equivalent to disabling of the Multicast filtering mechanism.

MC LIST – A list of Multicast Addresses to be accepted by the 82586. The least significant bit of each MC address must be 1. Note that the list is compacted; i.e., the most significant byte of the next address is immediately followed by the least significant byte of the next address.

4.5.5 Transmit Command

This command transmits a packet of user data onto the serial link.

The format of a transmit command is–



122136-36

where

LINK ADDRESS, EL, B,C,I,S – As per standard CBs (see Section 4.4.2.5).

STATUS – The defined bits are –

Bits 12,13 – As per standard CBs (see Section 4.4.2.5).

Bit 10 – No Carrier Sense signal during transmission. The Carrier Sense signal is monitored from the end of Preamble transmission until the end of Packet Check Sequence for TONO-CRS = 1 (Transmit On No Carrier Sense Mode) This bit indicates that transmission has been executed despite CRS nonexistence. For TONO-CRS=0 (Ethernet) mode, this bit also indicates unsuccessful transmission (transmission stopped when lack of Carrier Sense has been detected).

Bit 9 – Transmission unsuccessful (stopped) due to Loss of Clear to Send signal.

Bit 8 – Transmission unsuccessful (stopped) due to DMA Underrun; i.e., data not supplied from the system for transmission.

Bit 7 – Transmission Deferred; i.e., transmission was not immediate due to 82586 deferring transmission as a result of previous link activity.

Bit 6 – Heartbeat. Indicates that after previously performed transmission, and before the recently performed transmission (Interpacket Spacing), CDT signal was monitored as being active. This indicates that the Ethernet Transceiver Collision Detect Logic performs correctly.

The Heartbeat is monitored during the Interpacket Spacing Period.

Bit 5 – Transmission attempt stopped due to many collisions. This happens if the number of retries is exhausted.

Bits 3-0 – Number of collisions experienced by recently transmitted packet.

CMD – The TRANSMIT command: 4H.

BD-PTR – The offset portion of the address of the first TBD containing transmit data. BD-PTR=OFFFFH indicates no TBD is used.

Destination Address – Contains the packet Destination Address. The least significant bit (MC) indicates the address type:

MC = 0: Individual Address.
MC = 1: Multicast or Broadcast Addresses.
If the destination Address bits are all 1s, this is a Broadcast Address.

Type Field – The contents of this field are user-defined.

1. The DESTINATION ADDRESS and the TYPE FIELD are packed; i.e., the TYPE-FIELD's least significant byte immediately follows the DESTINATION ADDRESS's most significant byte.

2. The DESTINATION ADDRESS and TYPE FIELD are not used when the 82586 is configured to AC-LOC=0.

3. For AC-LOC=1 transmit buffers shorter than ADDR-LEN are invalid. The transmission is aborted by DMA Underrun.

4. Packets that are aborted in the middle of transmission (can result from any reason indicated by any of the STATUS bits 8, 9, 10, and 12) are jammed).

5. Jamming Rules:

a. Jamming will not start before completion of preamble transmission.

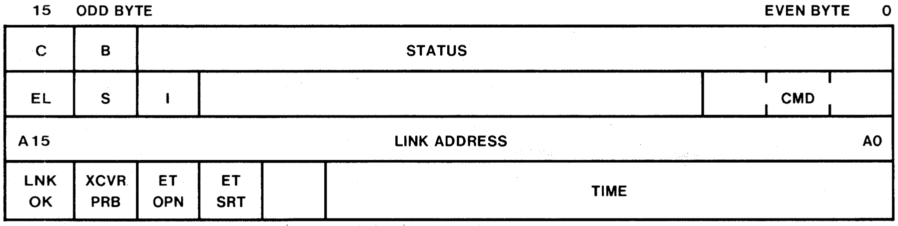
b. Collision detected during transmission of the last 11 bits will not result in jamming.

If the collision is detected during the transmission of the last bit or later, the collision will not be reported, and retransmission will not take place. This may happen for invalid packet, which is shorter in length than the Slot Time.

4.5.6 TDR

This command performs a Time Domain Reflectometer test on the serial line. By performing the command, the user is able to identify short or opens and their location on the network. Along with transmission of All Ones, the 82586 triggers an internal timer. This timer measures the time elapsed from transmission start until "echo" is obtained. Echo is indicated by Collision Detect going active or the Carrier Sense signal dropping.

The format of the TDR command is –



122136-37

where

Link Address, EL, B,C,I,S – As in standard CBs (see Section 4.4.2.5).

STATUS – Bits 12 and 13 per standard CBs (see Section 4.4.2.5).

CMD – The TDR command value: 5H.

TIME – An 11-bit field that specifies the number of TxC cycles that elapsed before "echo" was observed. All 1s indicates no echo.

NOTE

Because the network consists of various elements such as transceiver links, transceivers, Ethernet, and repeaters, the TIME is not exactly proportional to the problem distance.

The accuracy of problem location is 0.5 Vs/fs where:
Vs is the wave propogation speed on the link;
fs is the serial clock frequency.

LNK-OK (Bit 15) – No link problem identifed. TIME = 7FFH.

XCVR-PRB (Bit 14) – Transceiver Link Problem identified.
LNK-OK=O. TIME = 7FFH.

ET-OPN (Bit 13) – Open on the Ethernet link identified LNK-OK=0.

ET-SRT (Bit 12) – Short on the Ethernet link identified. LNK-OK=0.

4.5.7 Dump Status

This command causes the contents of various 82586 registers to be placed in memory. It is supplied as an 82586 self diagnostic tool and as an access to registers of interest to the user.

The DUMP STATUS command format is–

15 ODD BYTE				EVEN BYTE 0
C	B	STATUS		
EL	S	I		CMD
A15	LINK ADDRESS			A0
A15	BUF PTR			A0

122136-38

where

Link Address, EL, B,C,I,S – As in standard CBs (see Section 4.4.2.5).

CMD – The DIAGNOSE command value: 6H.

STATUS – Bits 12,13 per standard CBs (see Section 4.4.2.5).

BUF-PTR – This 16-bit quantity specifies the offset portion of the memory address which points to the top of the buffer allocated for the dumper registers content.

NOTE

The user of the DUMP STATUS command must allocate a 170 byte buffer.

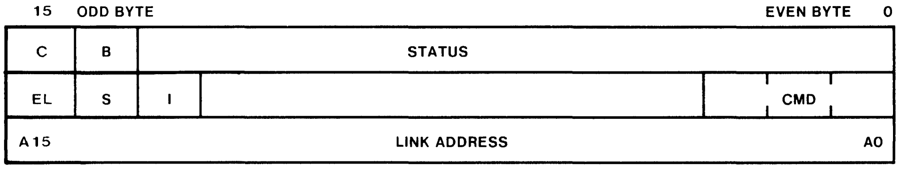
4.5.8 Diagnose

The Diagnose command checks the internal 82586 timer hardware, which includes:

- o Exponential Backoff Random Number Generator (Free Run Counter)
- o Exponential Backoff Timeout Counter
- o Slot Time Period Counter
- o Collision Number Counter
- o Exponential Backoff Shift Register

- Exponential Backoff Mask Logic.
- Timer Trigger Logic.

The DIAGNOSE command format is–



122136-39

where

Link Address, EL, B,C,I,S – As in standard CBs (see Section 4.4.2.5).

STATUS – Bits 12 and 13 per standard CBs (see Section 4.4.2.5).

CMD – The DIAGNOSE command value: 7H.

The DIAGNOSE command is performed in two phases:

1. Counters Test

   The Free Run, Exponential Backoff Timeout, Slot Time and Collision Counters are checked. Misinterpretation of stuck in state counter as a positive result is avoided by checking the counters when peforming transition.

   The test is performed in the following steps:

   a. All counters are RESET at once.

   b. Count.

c. Stop counting when the Free Run counter (10 bits), Exponential Backoff Counter (10 bits), wrap from all 1s to All 0s. Simultaneously, the Slot Time counter switches from 01111111111 to 10000000000 and the collision counter (4 bits) wraps from all 1s to All 0s.

Note that counting is stopped if any of the three longer counters wrap, as described above.

d. The 10 least significant bits (if they exist) are checked to see if they are all 0s.

If the PHASE 1 passes successfully, all the counters count properly, including the Free Run Counter.

2. Trigger Logic Test

a. Reset the Exponential Backoff Shift Register and all the counters.

b. Internally configure the Exponential Backoff logic as follows:

SLOT TIME	= 8H
LIN-PRIO	= 2H
EXP-PRIO	= 1H
BOF-MET	= 0H.

c. Internally emulate transmission and collision.

d. Check to see if the most significant bit of Exponential Backoff Shift Register is 1. If not, go back to Step c. If yes, continue.

e. Check the Mask Logic Output for all 1s (the Free Run Counter is all 1s at this point and the Exponential Backoff Shift Register is also all 1s).

If the result is positive, passed status is issued, otherwise, a failed status is issued.

APPENDIX A.
SERVICE DIAGRAMS

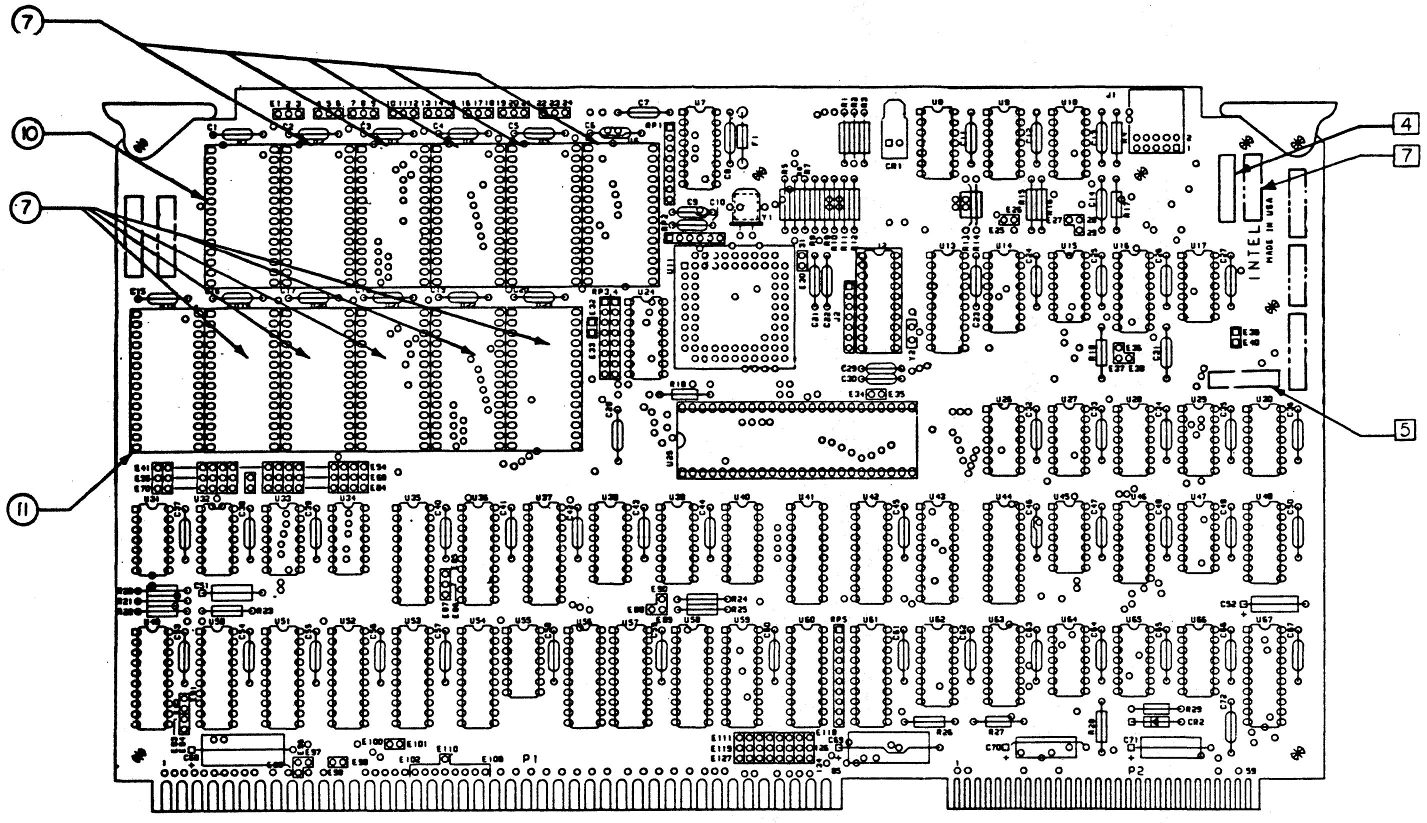
A.1 INTRODUCTION

This appendix provides a parts location diagram and a schematic diagram for the iSBC 552 Ethernet Communication Controller Board.

A.2 SCHEMATIC DIAGRAM

The schematic diagram of the iSBC 552 board (Figure A-2) is current when the manual is printed. However, minor revisions to the diagram may occur between manual printings. Therefore, Intel provides photocopies of the current schematic diagram with the board when it is shipped from the factory. That diagram should be inserted in this manual for future reference. In most instances the diagram shipped with the board will be identical to the one printed in the manual.

REVISIONS							
REV	DESCRIPTION	DFT	DATE	CHK	DATE	APVD	DATE
A	ECO1215C25		[illegible]		[illegible]	Rayo	[illegible]



COMPONENT SIDE

NOTES: UNLESS OTHERWISE SPECIFIED:

1. WORKMANSHIP PER INTEL 99-0007-001.
2. MAXIMUM HEIGHT OF COMPONENTS SHALL BE .40 INCH FROM BOARD SURFACE.
3. MAXIMUM HEIGHT OF LEADS ON SOLDER SIDE SHALL BE .09 INCH FROM BOARD SURFACE.

4. MARK 'PBA' ITEM NUMBER PER INTEL STANDARD 164997 APPROXIMATELY WHERE SHOWN.

5. MARK ASSEMBLY VENDOR IDENTIFICATION IN CONTRASTING PERMANENT COLOR, NON-CONDUCTIVE, .08 INCH MINIMUM HIGH CHARACTERS APPROXIMATELY WHERE SHOWN.

6. INSTALL/DELETE ALL JUMPERS AS PER WIRE LIST.

7. REMOVE OR OBLITERATE ANY EXISTING PRODUCT CODE MARKING,
AND MARK PRODUCT CODE PER INTEL MARKING STANDARD 164997 APPROXIMATELY WHERE SHOWN.

ITEM NO.	DESCRIPTION
QUANTITY PER DASH NO.	PARTS LIST

UNLESS OTHERWISE SPECIFIED:
1. DIMENSIONS ARE IN INCHES.
~~2. BREAK ALL SHARP EDGES.~~
3. DO NOT SCALE DRAWING.
~~4. TOLERANCES:~~
~~ANGLES ±~~
~~.XX ±~~
~~.XXX ±~~

SIGNATURE	DATE
DRN BY P. Trevino	[illegible]
CHK BY Rayo Obispo	[illegible]
ENGR APVD Rayo Obispo	[illegible]
APVD	
APVD	

intel®
3065 BOWERS AVE
SANTA CLARA
CALIF. 95051

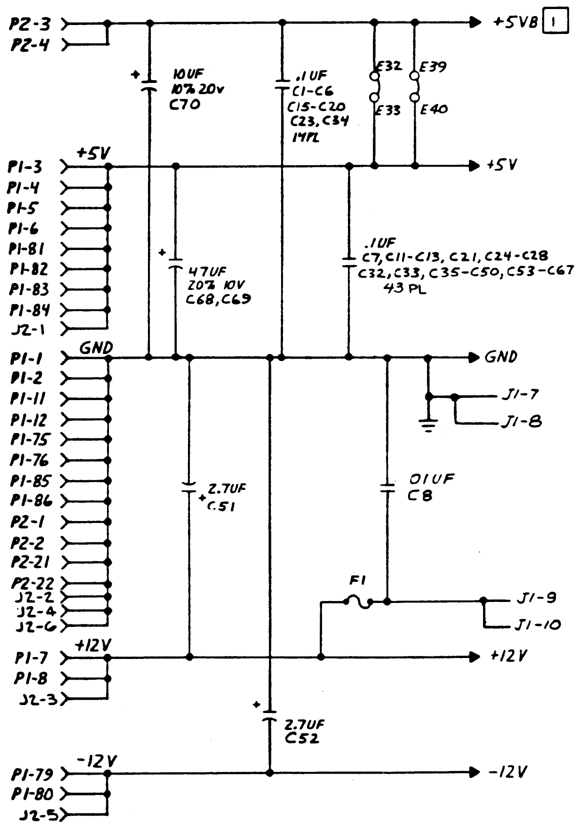
TITLE ASSY DWG
iSXM 552

SIZE	DCLC	CL CODE	RLSE LVL	DOCUMENT NUMBER	REV
D	12	0501	---	115584	A

SCALE NONE SHEET 1 OF 1

Figure A-1. iSBC® 552 Assembly Drawing

REVISIONS							
REV	DESCRIPTION	DFT	DATE	CHK	DATE	APVD	DATE
A	EC01215025		2/22/85				



NOTES: UNLESS OTHERWISE SPECIFIED.

1 INDICATES VCC PIN OF I.C. CONNECTED TO +5VB.

MEMORY TYPE OPTIONS					
LOCATION PAIR	DEVICE TYPE	JUMPERS			
		FROM	TO	FROM	TO
U2	PROM	E2	E3	E4	E5
U19	iRAM	E2	E1	E6	E5
U3	PROM	E8	E9	E10	E11
U20	iRAM	E8	E7	E12	E11
U4	PROM	E14	E15	E16	E17
U21	iRAM	E14	E13	E3	E17
U5	PROM	E20	E21	E22	E23
U22	iRAM	E20	E19	E24	E23

MEMORY SIZE DECODE OPTIONS					
PROM DEVICE	iRAM DEVICE	JUMPERS			
		FROM	TO	FROM	TO
8K X 8	8K X 8	E88	E89	E86	E85
16K X 8	8K X 8	E90	E89	E86	E85
16K X 8	16K X 8	—	—	E86	E87

MULTIBUS ARBITRATION OPTIONS			
		JUMPERS	
		FROM	TO
CBRQ*	TO GND	E96	E97
	TO MULTIBUS	E96	E95
BPRO*	TO MULTIBUS	E98	E99
	N/C	N/C	N/C
ANY RQ	TO GND	E92	E91
	PULL UP	N/C	N/C

MULTIBUS INTERRUPT OPTIONS		
INTERRUPT	JUMPERS	
	FROM	TO
INTØ*	E110	E109
INT1*	↑	E108
INT2*		E107
INT3*		E106
INT4*		E105
INT5*		E104
INT6*	↓	E103
INT7*	E110	E102

RAM WAIT STATE GEN.		
WAIT STATES	JUMPERS	
	FROM	TO
Ø	E28	E27
1	E28	E29

CTS* OPTIONS		
CTS* CONNECTION	JUMPERS	
	FROM	TO
GND	E34	E35
PCM	—	—

* INDICATES INVERTED SIGNALS.

DEVICE TABLE						
REF DES	DEVICE TYPE	POWER PINS				UNUSED LOGIC ELEMENT OUTPUT PINS
		GND	+5v			
U9.U64.U65	74S00	7	14			
U26	74S02	7	14			U26-13
U15.U45.U66	74S04	7	14			U15-2,12; U66-8,12; U45-12
U27	74F08	7	14			
U17	74S11	7	14			U17-6,12
U28	74S32	7	14			
U29	74S51	7	14			U29-8
U10	74F74	7	14			
U47	74LS74	7	14			
U30	74LS132	7	14			
U7,U24	74F138	8	16			
U40	74LS138	8	16			
U46	74S139	8	16			
U39	74S157	8	16			
U14	74LS175	8	16			
U67	74S240	10	20			
U52.U51.U59	74LS240	10	20			
U44	74LS245	10	20			
U31-U34	74LS266	7	14			U31-3,4
U62.U63	74LS283	8	16			
U38	74S288	8	16			
U41.U42.U60	74LS373	10	20			
U43	74LS374	10	20			
U48	74368	8	16			
U16	74LS123	8	16			
U11	80186	26,60	9,43			
U25	82586	12,24	36,48			
U12	82501	10	20			
U35-U37	8282	10	20			
U53.U54.U61	8283	10	20			
U13.U50	8288	10	20			
U49	8289	10	20			
U1-U6,U18-U23	2764	14	28			
	2186	14	28			
U56-U58	8303	10	20			
U8	7406	7	14			U8-2,4,6,8,10
U55	74128	7	14			U55-13

REFERANCE DESIGNATIONS	
LAST USED	NOT. USED
R29 E134 U67 C72 P2 J2 RP5	

ITEM NO.	DESCRIPTION
QUANTITY PER DASH NO.	PARTS LIST

UNLESS OTHERWISE SPECIFIED:
1. DIMENSIONS ARE IN INCHES.
2. BREAK ALL SHARP EDGES.
3. DO NOT SCALE DRAWING.
4. TOLERANCES:
ANGLES ±
XX ±
XXX ±

SIGNATURE	DATE
DRN BY	9/22/84
CHK BY	10/9/84
ENGR APVD	10/9/84
APVD	
APVD	

intel®
3065 BOWERS AVE
SANTA CLARA
CALIF. 95051

TITLE
SCHEMATIC, iSXM 552

SIZE	DCLC	CL CODE	RLSE LVL	DOCUMENT NUMBER	REV
D	12	0100		115587	A

SCALE NONE SHEET 1 OF 6

Figure A-2. iSBC® 552 Schematic Diagram (Sheet 1 of 6)

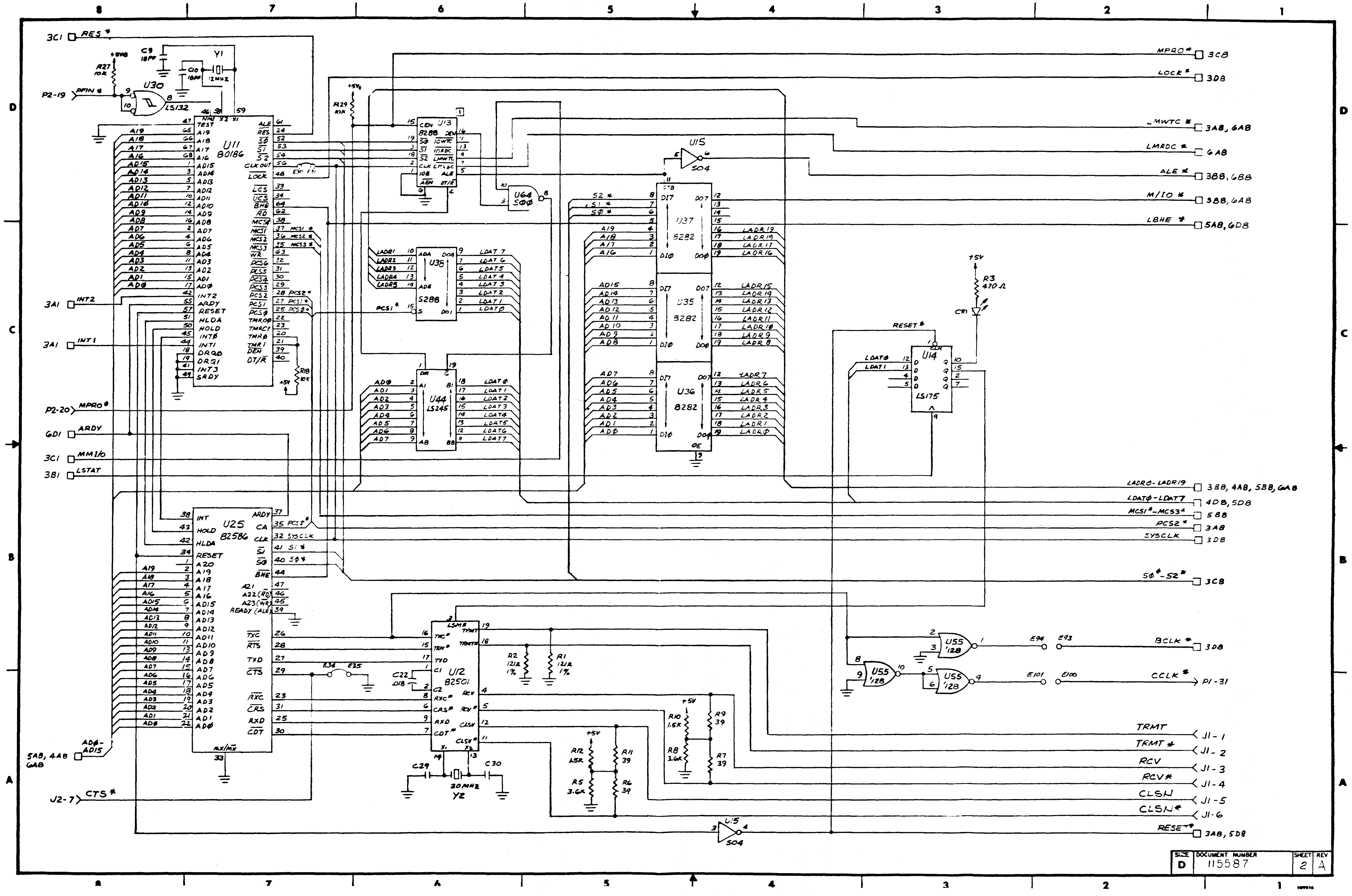


Figure A-2. iSBC® 552 Schematic Diagram (Sheet 2 of 6)

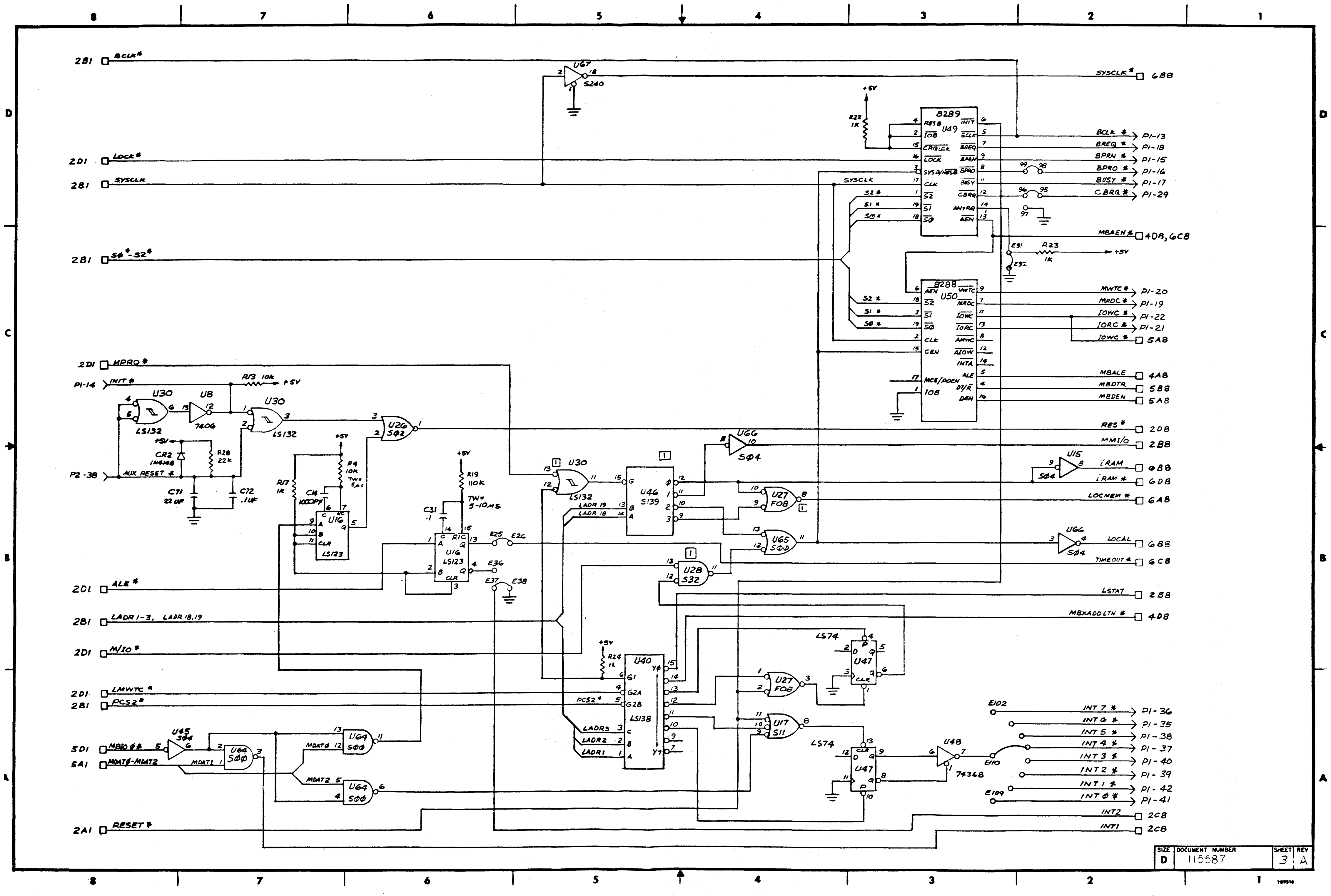
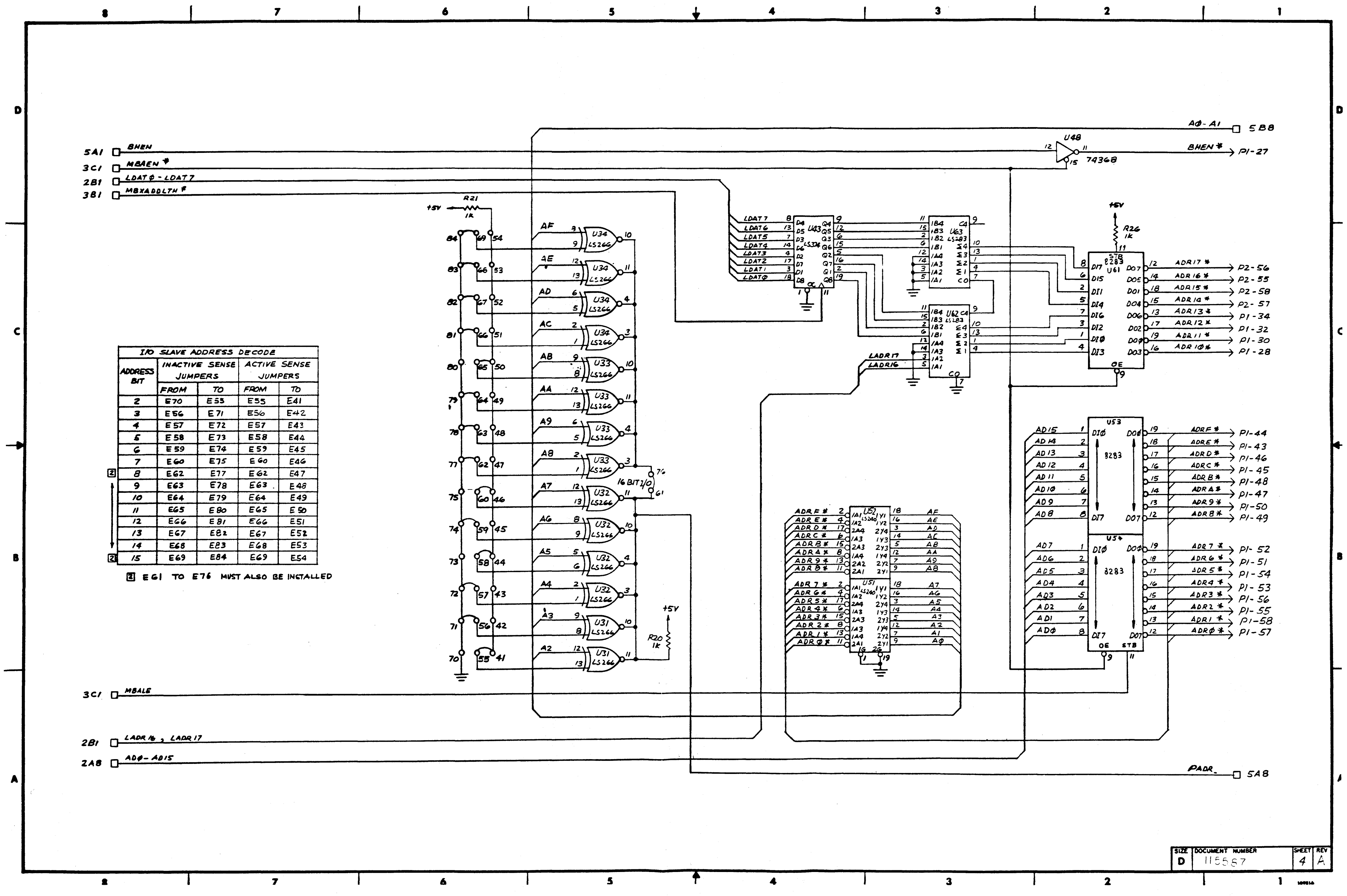


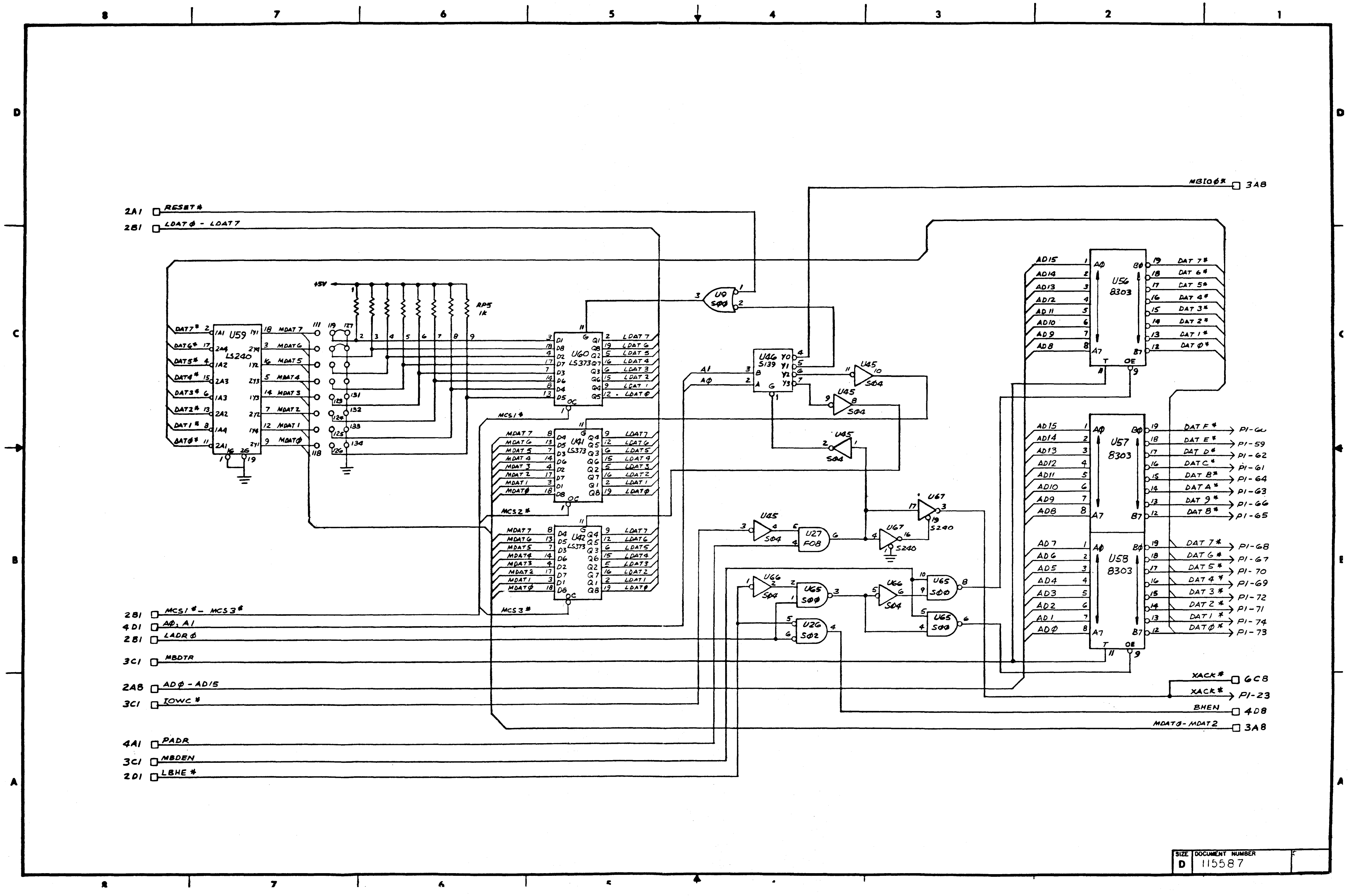
Figure A-2. iSBC® 552 Schematic Diagram (Sheet 3 of 6)



I/O SLAVE ADDRESS DECODE				
ADDRESS BIT	INACTIVE SENSE JUMPERS		ACTIVE SENSE JUMPERS	
	FROM	TO	FROM	TO
2	E70	E55	E55	E41
3	E56	E71	E56	E42
4	E57	E72	E57	E43
5	E58	E73	E58	E44
6	E59	E74	E59	E45
7	E60	E75	E60	E46
2 8	E62	E77	E62	E47
9	E63	E78	E63	E48
10	E64	E79	E64	E49
11	E65	E80	E65	E50
12	E66	E81	E66	E51
13	E67	E82	E67	E52
14	E68	E83	E68	E53
2 15	E69	E84	E69	E54

2 E61 TO E76 MUST ALSO BE INSTALLED

Figure A-2. iSBC® 552 Schematic Diagram (Sheet 4 of 6)



A-2. iSBC® 552 Schematic Diagram (Sheet 5 of 6)

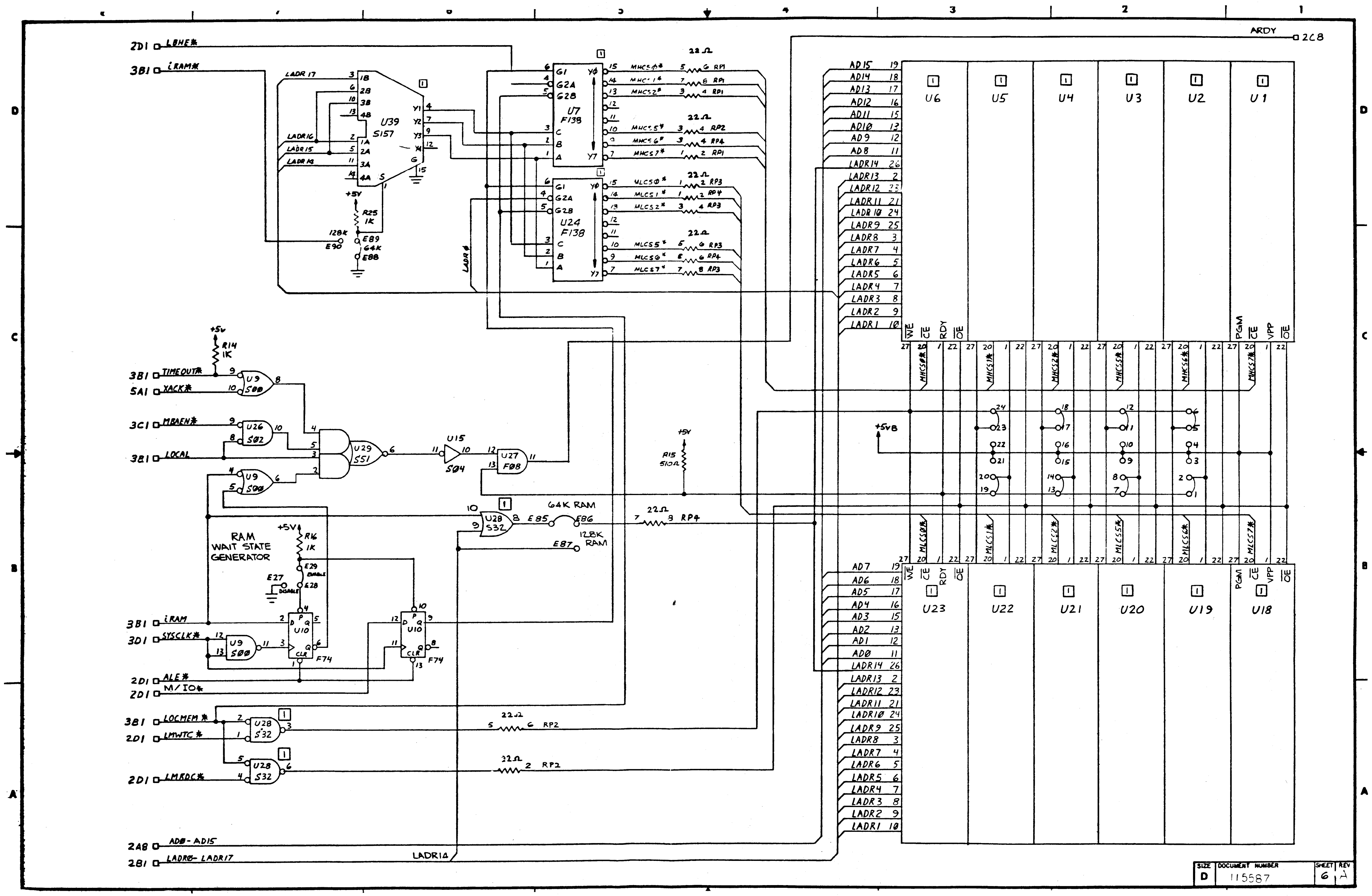


Figure A-2. iSBC® 552 Schematic Diagram (Sheet 6 of 6)

intel®

iSBC® 552 Ethernet Communications Controller
Hardware Reference Manual
122141-002

REQUEST FOR READER'S COMMENTS

Intel's Technical Publications Departments attempt to provide publications that meet the needs of all Intel product users. This form lets you participate directly in the publication process. Your comments will help us correct and improve our publications. Please take a few minutes to respond.

Please restrict your comments to the usability, accuracy, readability, organization, and completeness of this publication. If you have any comments on the product that this publication describes, please contact your Intel representative. If you wish to order publications, contact the Intel Literature Department (see page ii of this manual).

1. Please describe any errors you found in this publication (include page number).

____
____
____
____
____
____

2. Does the publication cover the information you expected or required? Please make suggestions for improvement.

____
____
____
____
____

3. Is this the right type of publication for your needs? Is it at the right level? What other types of publications are needed?

____
____
____
____
____
____

4. Did you have any difficulty understanding descriptions or wording? Where?

____
____
____
____

5. Please rate this publication on a scale of 1 to 5 (5 being the best rating).______________

NAME ______________________________ DATE ______________

TITLE ____

COMPANY NAME/DEPARTMENT ______________________________

ADDRESS ____

CITY ______________ STATE ______________ ZIP CODE ______________

(COUNTRY)

Please check here if you require a written reply. □

WE'D LIKE YOUR COMMENTS ...

This document is one of a series describing Intel products. Your comments on the back of this form will help us produce better manuals. Each reply will be carefully reviewed by the responsible person. All comments and suggestions become the property of Intel Corporation.

Intel Corporation
Attn: Technical Publications M/S 6-2000
3065 Bowers Avenue
Santa Clara, CA 95051

INTEL CORPORATION, 3065 Bowers Avenue, Santa Clara, California 95051 (408) **987-8080**

Printed in U.S.A.