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Attachment Controller 2

INTRODUCTION

The Attachment Controller 2 is a double controller that is used with the ideographic work station feature and the MLCA (multiline communications adapter). The attachment controllers are located between the System/34 channel and the I/O attachments. The cards used for the attachment controllers and their locations are shown in the figure.

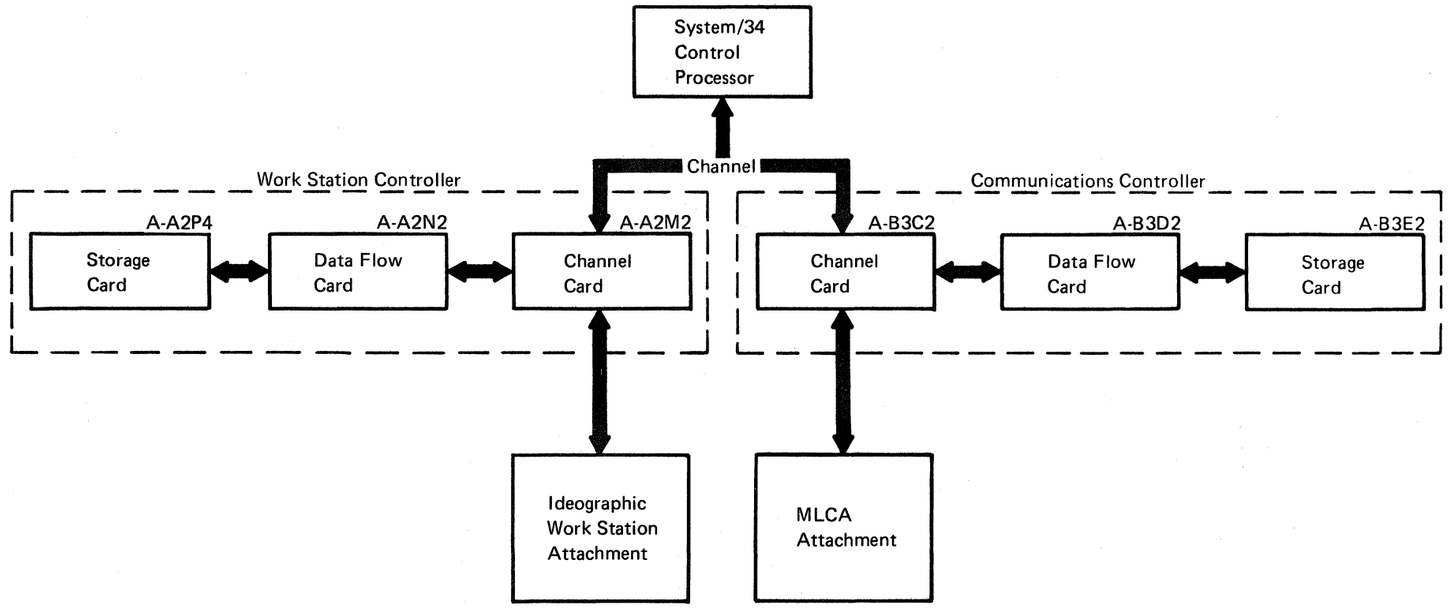
The channel cards connect the attachment controllers to the System/34 channel and supply the control logic and the lines that connect to the attachments.

The data flow cards contain the processing units and the storage interface.

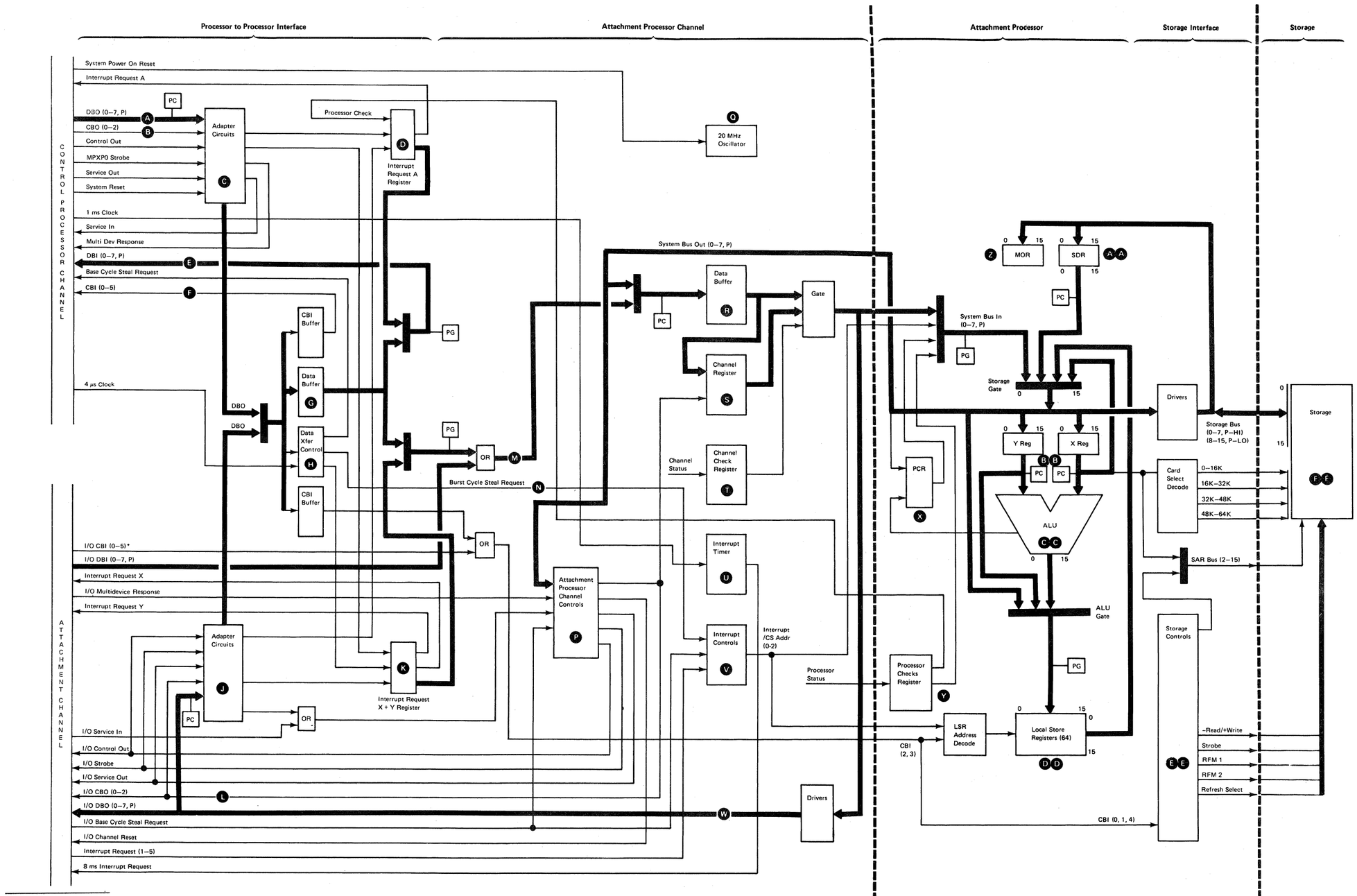
The storage cards supply 32K of 2-byte words for the ideographic work station feature and 16K of 2-byte words for the MLCA.

Generally, the Attachment Controller 2 supplies:

- Sixteen-bit ALU and data flow
- Eight bits of data on both the DBI (data bus in) and the DBO (data bus out)
- Sixty-four, 16-bit general-purpose registers
- Five interrupt levels and branch and link
- Maintenance of odd-numbered parity throughout the data flow
- Storage addressing lines for a maximum of 64K, 2-byte words
- Cycle steal
- Addresses for a maximum of 14 I/O devices



DATA FLOW



[1]I/O CBI bits 0 through 4 connect to the controller through the data flow card.

Channel Card | Data Flow Card | Storage Card

FUNCTIONAL UNITS

Processor-to-Processor Interface

The processor-to-processor interface is the logic that attaches the control processor to the attachment processor channel. This logic controls all communication between the control processor and the attachment processor. This communication is in the form of interrupts, data transfers, and I/O instructions. The processor-to-processor interface includes the control processor channel adapter circuits, the attachment processor channel adapter circuits, data buffers, data transfer controls, and interrupt request registers.

Control Processor Channel Adapter (C)

These circuits do the following:

- Synchronize the control processor with the processor-to-processor interface
- Increase the power of the DBO
- Check parity
- Decode device addresses

The control processor channel adapter circuits let the control processor channel communicate with the attachment processor through control lines and data buses. The 'control out', 'service out', and 'strobe' lines signal the adapter circuits when data is available on the DBO or when the data should be on the DBI. The 'service in' and 'multidevice response' lines signal the control processor channel that the data on the DBO has been received or that data is available on the DBI.

Command Bus Out (B)

The command bus out (CBO) is a 3-bit bus that specifes the type of I/O operation to execute. The attachment controller commands are:

Bits 0 1 2	Command
0 0 0	SCSSB (sense cycle steal status byte)
0 0 1	SILSB (sense interrupt level status byte)
0 1 0	CSACK (cycle steal acknowledge)
0 1 1	Not used
1 0 0	I/O load
1 0 1	I/O sense
1 1 0	I/O control load
1 1 1	Not used

Data Bus Out (A)

The data bus out (DBO) is a 9-bit bus (0 through 7, P) that is used in the following ways:

- During control out of an SILSB command, DBO bits 0 through 3 contain the interrupt level.
- During control out of any I/O command other than SILSB, DBO bits 0 through 3 contain the device address and bits 4 through 7 contain the command modifier.
- During control out of a CSACK command, the DBO contains the cycle steal address of the device selected to perform the base cycle steal.
- During service out of an I/O load or I/O control load command, the DBO contains data.
- During service out of a CSACK command, the DBO contains data.

Data Buffer (G)

The data buffer contains two 1-byte buffers that are used when moving data and status information between the control processor channel and the attachment processor channel.

Data Transfer Control (H)

The data transfer control logic controls the movement of data between the control processor and the attachment processor. The data is moved by single byte base cycle steal between the control processor and the processor-to-processor interface and moved by single byte burst cycle steal between the attachment processor and the processor-to-processor interface. The cycle steals are started by I/O commands from either processor.

The data transfer control logic contains the following:

- A byte counter to control the number of bytes moved. This counter can be set to any value from 0 through 511.
- A buffer full latch to indicate when a byte of data is in the data buffer. This latch signals the receiving processor that data is available.
- A cycle steal pacer to control the speed of the data movement between the two processors. The 4-microsecond clock from the control processor is used to delay the base cycle steal requests to the control processor. The length of the delay is set by an I/O command to the processor-to-processor interface.

Command Bus In (F)

The command bus in (CBI) is a 6-bit bus that supplies control information to the control processor channel. The CBI bits have the following meanings:

Bit	Meaning		
0	0	=	Base cycle steal high byte (WR not incremented)
	1	=	Base cycle steal low byte (WR incremented)
1	0	=	Base cycle steal sense
	1	=	Base cycle steal load
2, 3	00	=	Base cycle steal WR4 on interrupt level 4
	01	=	Base cycle steal WR5 on interrupt level 4
	10	=	Base cycle steal WR6 on interrupt level 4
	11	=	Base cycle steal WR7 on interrupt level 4
4	0	=	Control storage
	1	=	Main storage
5	1	=	Parity error (even parity)

The CBI is active during I/O commands and base cycle steal operations.

Data Bus In (E)

The data bus in (DBI) is a 9-bit bus (0-7, P) that is used in the following ways:

- During I/O sense commands, the DBI contains data or sense information.
- During base cycle steal operations, the DBI contains data.
- During SILSB and SCSSB commands, the DBI contains sense information.

Interrupt Request A Register (D)

The interrupt request A register supplies the 'interrupt request A' line to the control processor. This interrupt can be set by any of the following conditions:

- Attachment processor condition A, and attachment processor condition B. These conditions are set by the attachment processor and are anded with an enable/disable latch.
- Data transmission operation end condition. This condition is anded with an enable/disable latch and set by the processor-to-processor interface.

  This interrupt indicates to the control processor that the data transfer byte counter has reached zero (the data transmission between the control processor and the attachment processor has completed).
- Attachment controller processor check condition. This condition is anded with an enable/disable latch and set by the attachment controller hardware. This interrupt indicates to the control processor that the attachment processor has stopped because of an error.
- Control processor condition. This condition is set by the control processor for diagnostic purposes only.

Attachment Processor Channel Adapter (J)

These circuits do the following:

- Synchronize the attachment processor channel with the processor-to-processor interface
- Increase the power of the DBO
- Check parity
- Decode device addresses

The attachment processor channel adapter circuits let the attachment processor channel communicate with the control processor through control lines and data buses. These circuits control the execution of I/O commands and data transmissions from the attachment processor. The processor-to-processor interface receives and executes commands from the attachment processor. These commands are:

- I/O load
- I/O control load
- I/O sense

Interrupt Request X and Y Register (K)

The interrupt request X and Y register supplies two interrupt requests to the attachment controller channel. The interrupt request X can be set by any of the following conditions:

- Control processor condition A, control processor condition B, and control processor condition C. These conditions are set by the control processor and are anded with enable/disable latches.
- Data transmission operation end condition. This condition is anded with an enable/disable latch and set by the processor-to-processor interface hardware. This interrupt indicates to the attachment processor that the data transfer byte counter has reached zero (the data transmission between the control processor and the attachment processor has completed).
- Attachment processor condition. This condition is set by the attachment processor for diagnostic purposes only.

The interrupt request Y can be set by either of the following conditions:

- Attachment processor condition. This condition is set by the attachment processor.
- Control processor condition. This condition is set by the control processor.

Attachment Processor Channel

The attachment processor channel contains the logic that moves the data and commands between the attachment processor, the attachment processor storage, the processor-to-processor interface, and the I/O device.

Odd-numbered parity is maintained on the channel data buses. Parity is checked at the output of the system bus out and the DBI gate.

The attachment processor channel circuits do the following:

- Move data between the attachment processor storage and the I/O device by using base cycle steal mode or I/O storage instructions.
- Move data between the attachment processor storage and the processor-to-processor interface by using burst cycle steal mode.
- Move data between the attachment processor local storage registers (LSRs) and the processor-to-processor interface or I/O device (I/O immediate instructions).
- Control the channel or I/O functions that may or may not include data movement (I/O control load and I/O control sense instructions).

The attachment processor channel supplies controls for the following:

- I/O instructions (immediate, storage, and jump)
- Interrupts (five levels)
- Burst cycle steal (processor-to-processor interface only)
- Base cycle steal (I/O devices)
- Error detection

Attachment Processor Channel Controls (P)

The attachment processor channel, using the channel sequencer, controls the data transfer between the processor-to-processor interface and the I/O device attached to the channel. The logic controls the decode of the system bus out to generate the CBO bits.

The control lines function as follows:

- The 'I/O control out' line signals the attachment that the 'I/O DBO' and 'I/O CBO' lines are valid. When the 'I/O control out' and the 'I/O service out' lines are active at the same time, a blast condition is indicated, which forces all attachments off the channel.
- The 'I/O service out' line signals the attachment that the 'I/O DBO' lines are valid if data is being sent from the channel to the processor-to-processor interface or I/O device. If data is sent to the channel from an attachment, the 'I/O service out' line signals the processor-to-processor interface or I/O device that the channel has received the data.
- The 'I/O service in' line signals the channel that the command byte has been received by the attachment or that sense data on the 'I/O DBI' lines is valid.

I/O Data Bus In (M)

The I/O data bus in (DBI) is a 9-bit bus (0-7, P) that is the result of the dot OR of the DBI from the processor-to-processor interface and the DBI from the I/O device. The I/O DBI supplies data and status information to the attachment processor channel. The I/O DBI contains:

- Data or sense information during I/O sense instructions
- Data during cycle steal operations
- Sense information during SILSB and SCSID instructions

I/O Command Bus In (N)

The I/O command bus in (CBI) is a 6-bit bus that supplies control information to the attachment processor channel. The CBI is the result of the dot or of the CBI from the processor-to-processor interface and the CBI from the I/O device. The bus is active during I/O instructions and cycle steal operations. Bits 0, 1, 2, and 3 of the I/O CBI control cycle steal and local storage register (LSR) selection. Bits 2 and 3 select the work register that contains the address where data is to be loaded or sensed for cycle steal operations.

The I/O CBI bits have the following meaning:

Bit	Meaning		
0	0	=	Cycle steal high byte (WR not incremented)
	1	=	Cycle steal low byte (WR incremented)
1	0	=	Cycle steal sense
	1	=	Cycle steal load
2, 3	00	=	Select WR4 (see note)
	01	=	Select WR5 (see note)
	10	=	Select WR6 (see note)
	11	=	Select WR7 (see note)
4	1	=	Required for cycle steal operations and indicates invalid DBI parity during sense instructions
5	1	=	DBO parity error (even-numbered parity)

Note: These work registers are selected by interrupt level 1 during burst cycle steal mode and by interrupt level 4 during base cycle steal mode.

I/O Command Bus Out (L)

The I/O command bus out (CBO) is a 3-bit bus that specifies the type of I/O operation to execute. The attachment processor commands are:

Bits 0 1 2	Command
0 0 0	Sense cycle steal identification (SCSID)
0 0 1	Sense interrupt level status byte (SILSB)
0 1 0	Cycle steal acknowledge (CSACK)
0 1 1	I/O branch on condition
1 0 0	I/O load
1 0 1	I/O sense
1 1 0	I/O control load
1 1 1	I/O control sense

I/O Data Bus Out (W)

The I/O data bus out (DBO) is a 9-bit bus (0-7, P) that is used in the following ways:

- During control out of an SILSB command, I/O DBO bits 0 through 3 contain the interrupt level.
- During control out of any I/O command other than SILSB, I/O DBO bits 0 through 3 contain the device address and bits 4 through 7 contain the command modifier.
- During control out of a CSACK command, the I/O DBO contains the cycle steal address of the device selected to perform the base cycle steal.
- During service out of an I/O load or I/O control load command, the I/O DBO contains data.
- During service out of a CSACK command, the I/O DBO contains data.

Data Buffer (R)

The attachment processor channel data buffer is used as an immediate storage register for all data that passes through the channel. The buffer is controlled by channel clocks and control lines.

Channel Register (S)

The channel register is used for diagnostic purposes. During I/O instructions this register contains the attachment device address in bits 0 through 3 and the I/O command bus out in bits 5 through 7. During base cycle steal operations, the channel register stores the device ID of the I/O attachment. When an error occurs, this information can be stored in a local storage work register for later diagnostic use.

Channel Check Register (T)

The channel check register is an 8-bit register that stores the error status of the channel hardware. The information stored in this register can be moved to a local store work register for later diagnostic use.

The channel check register bits have the following meanings:

Bit	Meaning
0	DBO parity check
1	Invalid device address
2	DBI parity check
3	I/O time-out
4	Not used
5	System bus out parity check
6	Cycle steal operation (The check occured during a cycle steal operation.)
7	Not used

Interrupt Timer (U)

A fixed interval interrupt timer can be used to generate an interrupt request from the channel logic on 8-millisecond intervals. The 1-millisecond clock from the control processor channel is used to drive the interrupt timer. The timer interrupt request can be enabled, disabled, and reset by I/O instructions from the attachment processor.

Interrupt Controls (V)

The interrupt control logic controls the five levels of the interrupt request, the base cycle steal request from the I/O device, and the burst cycle steal request from the processor-to-processor interface.

The priority of interrupts is as follows:

1. Interrupt level 0 processing (machine check)
2. Burst cycle steal
3. Base cycle steal
4. Interrupt level 1 processing
5. Interrupt level 2 processing
6. Interrupt level 3 processing
7. Interrupt level 4 processing
8. Interrupt level 5 processing
9. Main level processing

Interrupt level status can be stored in a local store work register for diagnostic use.

20 mHz Oscillator (Q)

The 20 mHz oscillator supplies the attachment processor two nonoverlapping clocks. Eight of these clocks are generated and used by the controller.

Attachment Processor

The attachment processor can operate on either 1 or 2 bytes of data. The instruction that is being executed determines the number of bytes and the path of the data.

Odd-numbered parity by byte is maintained in the data flow. Parity generating stations are at the output of the status gate and the ALU gate. Parity is checked at the storage data register, the X-register, and the Y-register. Parity is also checked on the data going into the microoperation register (MOR) and the storage address register (SAR) bus. The MOR parity check is done by the storage data register (SDR) parity check logic and the SAR parity check is done when the storage address is loaded into the X-register.

Storage Controls (E) (E)

The storage controls activate the proper control signals for storage read/write operations. These controls also contain a refresh address counter and refresh control logic that is used to refresh the dynamic storage. The output of the refresh address counter (7 bits) is gated to the storage address bus during refresh operations.

Microoperation Register (Z)

The microoperation register is a 16-bit register that holds each controller instruction as it is taken from storage. The instruction is decoded to control the data flow, for example, gate selection, arithmetic and logic unit operations, and local storage register selection.

Processor Checks Register (Y)

The processor checks register stores the error status of the attachment processor. When a hardware error occurs in the attachment processor, a bit is set on in this register to indicate the error. If this error cannot be recovered from, an instruction is executed to activate the processor check line going to the interrupt request A register in the processor-to-processor interface. The processor-to-processor interface interrupts the control processor to indicate that the attachment processor has stopped. This register can be stored in an LSR work register by an I/O instruction for diagnostic use.

The processor checks register bits have the following meanings:

Bit	Meaning
0	SDR parity check
1	MOR parity check
2	Y-register parity check
3	X-register parity check
4	Not valid storage address or SAR parity check
5	3-second time-out or SAR parity check
6, 7	Not used

Controller Storage (F) (F)

Controller storage contains either 16K or 32K addresses of read/write storage; each address is 2 bytes wide. The storage cells within the controller storage are dynamic (the cells must be refreshed to maintain valid data).

The controller storage is loaded from the CP control storage or MSP main storage during IPL. When controller storage is loaded, it contains the microcode that is used to support the attachment.

X-Register and Y-Register (B) (B)

These registers are two 1-byte registers (X-high, X-low, and Y-high, Y-low). The four registers form a buffer input to the arithmetic and logic unit (ALU). The X-high and Y-high registers are input to the ALU high, and the X-low and Y-low are input to the ALU low.

The X-registers are used as buffers for the base constants into the ALU and as a register for the 16-bit storage address.

The Y-registers are used as buffers for changing constants into the ALU.

Arithmetic and Logic Units (C) (C)

The attachment processor contains two arithmetic and logic units (ALUs). ALU high uses bits 0 through 7 when 2-byte data fields are used. ALU low uses bits 8 through 15 when either 1-byte or 2-byte data fields are used. The ALUs always send 2 bytes of data to the local storage register (LSR) input bus. When 2 bytes are used in the ALU operation, both bytes (high and low) are placed on the LSR input bus and are, at the same time, written into bits 0 through 7 and bits 8 through 15 of the LSR. When the ALU output is only 1 byte, the byte is sent to both the high and low LSR input bus lines. In these cases, the instruction selects only 1 byte to be written into an LSR.

Any data sent to the ALU is first loaded into the X- and Y-registers. The X-registers supply the data for one operand, and the Y-registers supply the data for the other operand that is used in the current ALU operation. The instruction and its function determine if 1 or 2 bytes are affected by the ALU.

The ALU does arithmetic operations wtih two 16-bit words, one 16-bit word plus or minus one 8-bit byte, or one 8-bit byte plus or minus one 8-bit byte. The logical/arithmetic 1 instruction is used for 8-bit by 8-bit arithmetic operations. The logical/arithmetic 2 instruction is used for 16-bit by 16-bit arithmetic and 16-bit by 8-bit arithmetic operations.

Instructions that cause an increase or decrease of the X-register contents are executed by resetting the Y-high and Y-low registers and then forcing a carry in to the ALU. This causes only the X-register to be affected by the instruction.

Storage Data Register (A) (A)

The storage data register (SDR) is a 16-bit register that is an immediate buffer for all instructions and data bytes taken from storage. Each instruction is 2 bytes wide. The SDR high order bits (0 through 7) are gated through the storage gate to X-register high and Y-register high and then to the ALU. The SDR low order bits (8 through 15) are gated to X-register low and Y-register low and then to the ALU.

Local Storage Registers (D) (D)

The attachment processor uses the local storage registers (LSRs) as:

- Data buffers and address registers for storage
- Operand registers for internal calculations
- I/O control registers that can be loaded from the I/O attachments or from which data can be sent to the I/O attachments

The local storage register stack contains sixty-four 16-bit registers. Bits 0 through 7 of each register are the high local storage register and bits 8 through 15 of each register are the low local storage register.

The 64 local storage registers are divided into six interrupt level groups with each group containing eight registers. Two of the eight register groups contain the microaddress registers (MAR) and microaddress backup registers (MAB), which supply the address pointers to the microcode for each interrupt level. The MAR contains the address of the next instruction to be executed. The MAB contains the return address when a branch and link instruction is executed. Interrupt level 0 and main program level share the same local storage register group.

Processor Condition Register (X)

The processor condition register (PCR) contains the processor conditions that are tested by the jump-on-condition instruction. The processor condition register is changed by system reset, program loading, or instructions that change register bits. These conditions are changed by the instructions that perform the add, subtract, test mask, compare immediate, subtract immediate, and R1-linked-with-R2 functions.

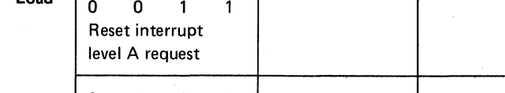
PROCESSOR-TO-PROCESSOR INTERFACE OPERATIONS

Control Processor Commands

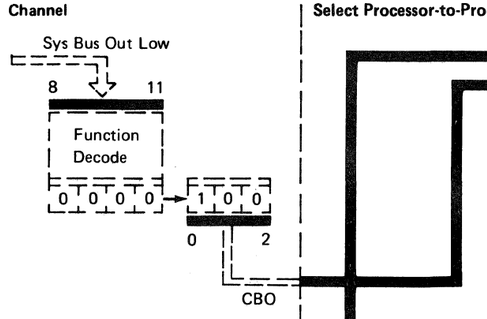
The processor-to-processor interface recognizes the following I/O immediate commands from the control processor:

- I/O load
- I/O control load
- I/O sense
- Sense interrupt level status byte (SILSB)

These commands are decoded from the function field (bits 8 through 11) and sent to the processor-to-processor interface on CBO bits 0 through 2. The format of the I/O immediate command is:



I/O Load Command



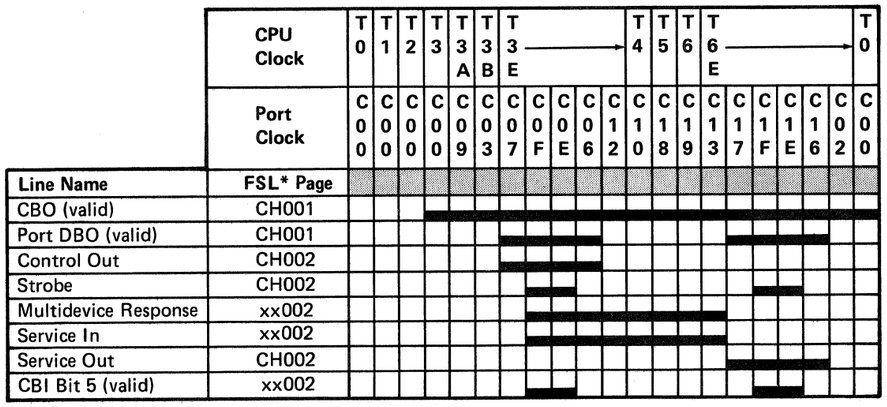
Select Processor-to-Processor Interface

Send Data Byte to Processor-to-Processor Interface

DBO 0-7

Modifier 4-7

CCB 0 1 2	CCB 3 4 5 6	DBO Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
100 I/O Load	0 0 0 0 Load CP CBI buffer			CP CBI bit 2	CP CBI bit 3	CP CBI bit 4	CP CBI bit 0	Select operation end to CP	Select operation end to attachment processor
	0 0 0 1 Load data buffer 1	DBO bits to data buffer 1							
	0 0 1 0 Load data buffer 2	DBO bits to data buffer 2							
	0 0 1 1 Reset interrupt level A request								
	0 1 0 1 Load attachment processor CBI buffer	CBI bit 0	CBI bit 1	CBI bit 2	CBI bit 3				Data count bit 0
	0 1 1 0 Enable interrupt level A conditions				Condition B	Condition A	Attachment processor processor check	Cycle steal operation end	Master enable
	0 1 1 1 Disable interrupt level A conditions				Condition B	Condition A	Attachment processor processor check	Cycle steal operation end	Master disable

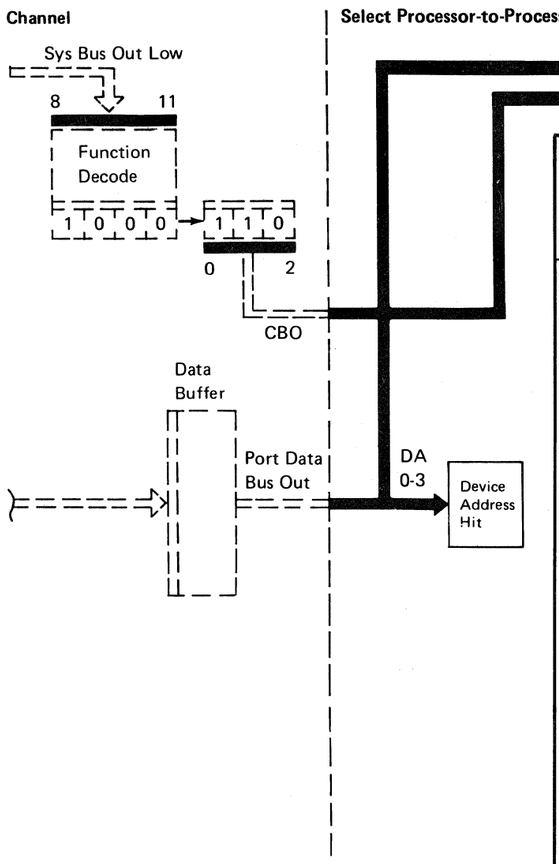


*xx = FB for MLCA
xx = WC for work station attachment B

Modifier Port DBO 4 5 6 7	Port DBO Bit	Command	Action Taken	FSL[1] Page
0 0 0 0	2-7	Load control processor CBI buffer	Loads the control processor CBI buffer or selects operation end	xx004
0 0 0 1	0-7	Load data buffer 1	Loads control processor DBO bits 0-7 into data buffer 1	xx004
0 0 1 0	0-7	Load data buffer 2	Loads control processor DBO bits 0-7 into data buffer 2	xx004
0 0 1 1		Reset interrupt level A request	Resets the interrupt level A latch	xx004
0 1 0 1	0-3, 7	Load attachment processor CBI buffer	Loads the attachment processor CBI buffer and the high-order bit of the byte counter	xx004
0 1 1 0	3-7	Enable interrupt level A conditions	Sets the enable interrupt latches for interrupt level A request	xx004
0 1 1 1	3-7	Disable interrupt level A conditions	Resets the enable interrupt latches for interrupt level A request	xx004

[1]xx = FB for MLCA; WC for work station attachment B

I/O Control Load Command



CCB	CCB	DBO							
0 1 2	3 4 5 6	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
110 I/O Control Load	0 0 0 0 Reset processor-to-processor interface								
	0 0 0 1 Set IMPL controls	Set reset key latch	Set load key latch	Set CE start latch	Set spare latch				
	0 0 1 0 Load byte counter or start CS xfer	DBO bits to byte counter							
	0 0 1 1 Load cycle steal pacer or SILSB response bits	Pacer bit 0	Pacer bit 1			SILSB response bit 0	SILSB response bit 1	SILSB response bit 2	SILSB response bit 3
	0 1 0 1 Load CP interrupt level or set diagnostic controls	Decrement byte counter	Control processor interrupt level						Set test mode
	0 1 1 0 Reset interrupt level A conditions	Reset operation end condition	Reset processor check condition			Reset condition B	Reset condition A	Diagnostic set CP condition	Diagnostic reset CP condition
	0 1 1 1 Set attachment processor interrupt conditions					Set level Y condition	Set level X condition C	Set level X condition B	Set level X condition A

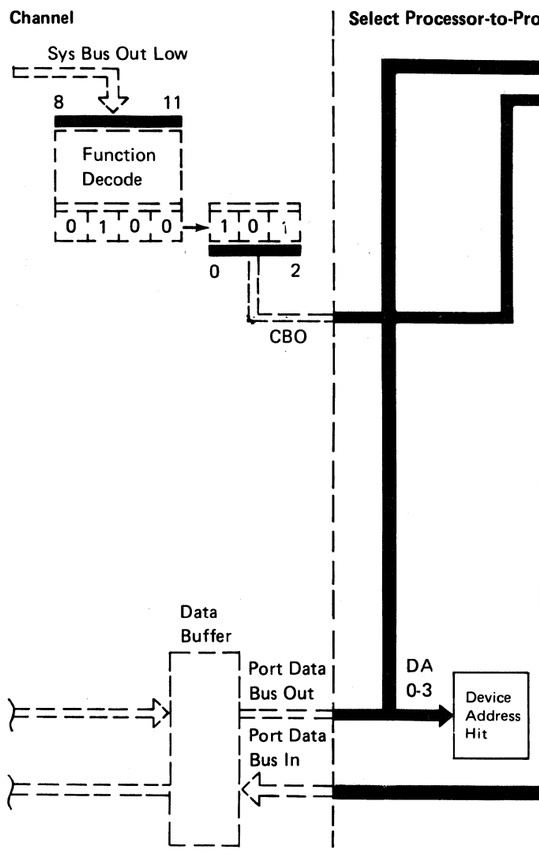
	CPU Clock	T0	T1	T2	T3	T3A	T3B	T3E →	T4	T5	T6	T6E →	T0
	Port Clock	C000	C000	C000	C009	C003	C007	C00F C00E C006 C012	C110	C118	C119	C113 C117 C11F C11E C116 C002	C000
Line Name	**FSL* Page**												
CBO (valid)	CH001				▬	▬	▬	▬ ▬ ▬ ▬	▬	▬	▬	▬ ▬ ▬ ▬ ▬ ▬	▬
Port DBO (valid)	CH001						▬	▬ ▬ ▬ ▬				▬ ▬ ▬ ▬ ▬ ▬	
Control Out	CH002						▬	▬ ▬ ▬ ▬					
Strobe	CH002							▬ ▬				▬ ▬	
Multidevice Response	xx002							▬ ▬ ▬ ▬	▬	▬	▬	▬ ▬ ▬ ▬ ▬ ▬	
Service In	xx002							▬ ▬ ▬ ▬	▬	▬	▬	▬ ▬ ▬ ▬ ▬ ▬	
Service Out	CH002											▬ ▬ ▬ ▬ ▬ ▬	
CBI Bit 5 (valid)	xx002							▬ ▬ ▬ ▬				▬ ▬ ▬ ▬ ▬ ▬	

*xx = FB for MLCA
xx = WC for work station attachment B

Modifier Port DBO 4 5 6 7	Port DBO Bit	Command	Action Taken	FSL[1] Page
0 0 0 0		Reset processor-to processor interface	Resets all latches and registers in the processor-to-processor interface, except the device address register, the CP interrupt level register, and the SILSB response bit register	
0 0 0 1	0-3	Set IMPL controls	Sets the reset key latch, the load key latch, the CE start latch and the spare latch	xx008
0 0 1 0	0-7	Load byte counter and start cycle steal transmission	Loads DBO bits 0-7 into the byte counter and starts a cycle steal transmission	xx006
0 0 1 1	0, 1, 4-7	Load cycle steal pacer or SILSB response bits	Loads DBO bits 0 and 1 into the cycle steal pacer register and DBO bits 4-7 into the SILSB response bit register	xx006 xx002
0 1 0 1	0-3, 7	Load CP interrupt level and set diagnostic controls	Loads DBO bits 1-3 into the CP interrupt level register and activates the processor-to-processor diagnostic line	xx002
0 1 1 0	0, 1, 4-7	Reset interrupt level A conditions	Resets condition latches for interrupt level A request	xx004
0 1 1 1	4-7	Set attachment processor programmable interrupt conditions	Sets condition latches for interrupt levels X and Y	xx010

[1]xx = FB for MLCA; WC for work station attachment B

I/O Sense Command



CCB 0 1 2	CCB 3 4 5 6	DBO Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
101 I/O Sense	0 0 0 0 Sense data buffer 1	Data buffer 1							
	0 0 0 1 Sense data buffer 2	Data buffer 2							
	0 0 1 0 Sense interrupt level A status	Operation end	Attachment processor processor check	Condition A	Condition B	Cycle steal buffer full		CP condition	
	0 1 0 0 Sense PPI configuration					First priority PPI	Second priority PPI	Third priority PPI	Fourth priority PPI

Note: PPI is processor-to-processor interface.

	CPU Clock	T 0	T 1	T 2	T 3	T 3 A	T 3 B	T 3 E →	T 4	T 5	T 6	T 6 E →	T 0
	Port Clock	C 0 0	C 0 0	C 0 0	C 0 0	C 0 9	C 0 3	C 0 7 C 0 F C 0 E C 0 6 C 1 2	C 1 0	C 1 8	C 1 9	C 1 3 C 1 7 C 1 F C 1 E C 1 6 C 0 2	C 0 0
Line Name	**FSL* Page**												
CBO (valid)	CH001				▬	▬	▬	▬ ▬ ▬ ▬ ▬	▬	▬	▬	▬ ▬ ▬ ▬ ▬ ▬	▬
Port DBO (valid)	CH001							▬ ▬ ▬ ▬ ▬				▬ ▬ ▬ ▬ ▬ ▬	
Control Out	CH002							▬ ▬ ▬ ▬ ▬					
Strobe	CH002							▬ ▬ ▬				▬ ▬ ▬	
Multidevice Response	xx002							▬ ▬ ▬ ▬ ▬	▬	▬	▬	▬	
Service In	xx002							▬ ▬ ▬ ▬ ▬	▬	▬	▬	▬	
Service Out	CH002							▬ ▬ ▬ ▬ ▬	▬	▬	▬	▬ ▬ ▬ ▬ ▬ ▬	
CBI Bit 5 (valid)	xx002							▬ ▬				▬ ▬ ▬ ▬	

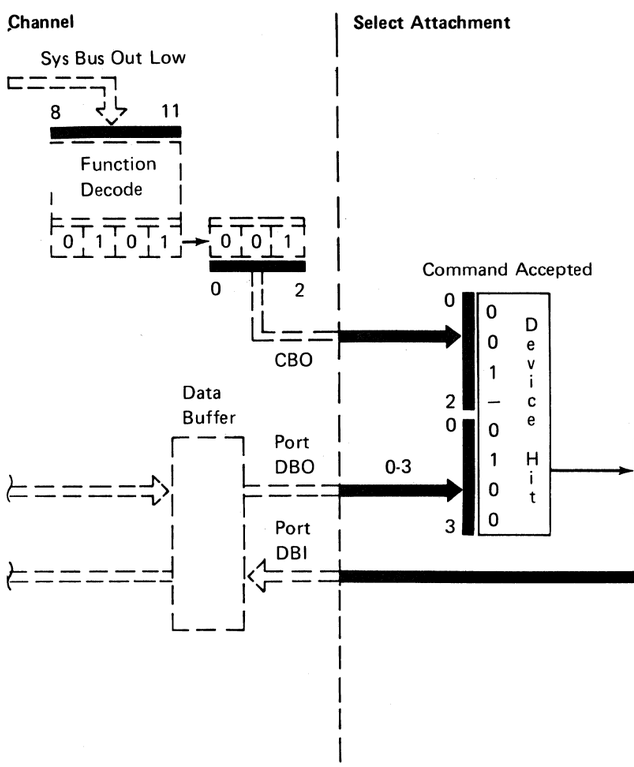
* xx = FB for MLCA
xx = WC for work station attachment B

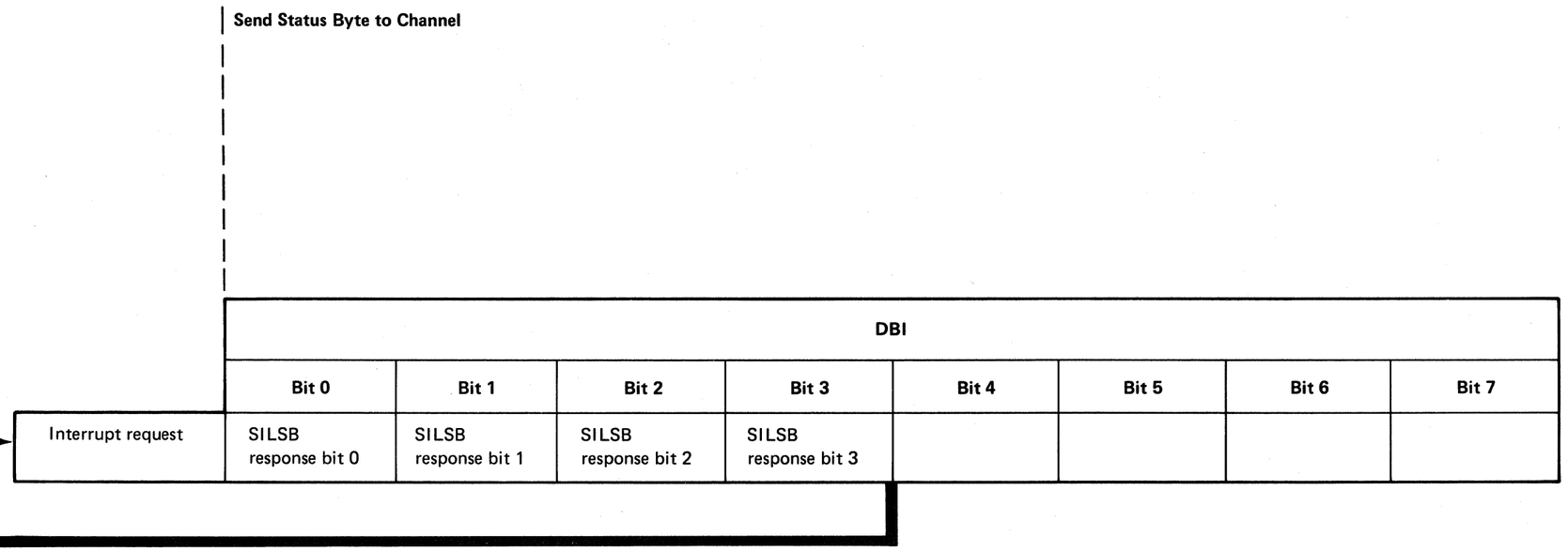
Modifier Port DBO 4 5 6 7	Port DBO Bit	Command	Action Taken	FSL[1] Page
0 0 0 0	0-7	Sense data buffer 1	Gates the contents of data buffer 1 to the channel on port DBI	xx004
0 0 0 1	0-7	Sense data buffer 2	Gates the contents of the data buffer 2 to the channel on port DBI	xx004
0 0 1 0		Sense interrupt level A status	Senses the following interrupt level A conditions:	xx004
	0		Operation end	
	1		Attachment processor processor check	
	2		Condition A	
	3		Condition B	
	4		Cycle steal buffer full	
	6		CP condition	
0 1 0 0		Sense AC[2] configuration	Senses the number of ACs installed	xx004
	4		First priority AC	
	5		Second priority AC	
	6		Third priority AC	
	7		Fourth priority AC	

[1]xx = FB for MLCA; WC for work station attachment B
[2]AC = Attachment controller 2

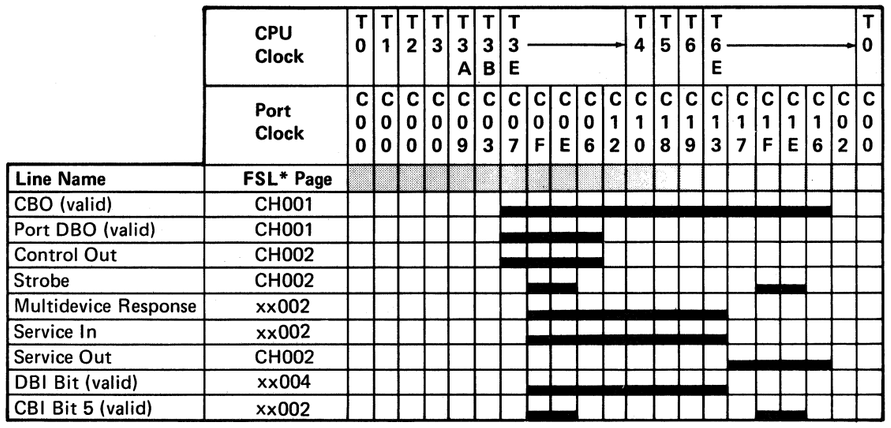
Sense Interrupt Level Status Byte Command

On a sense interrupt level status byte (SILSB) command, the processor-to-processor interface activates one of four programmable SILSB response bits.





	DBI							
	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Interrupt request	SILSB response bit 0	SILSB response bit 1	SILSB response bit 2	SILSB response bit 3				



CPU Clock	T0	T1	T2	T3	T3A	T3B	T3E →					T4	T5	T6	T6E →						T0
Port Clock	C000	C000	C000	C009	C003	C007	C00F	C00E	C006	C012	C010	C018	C019	C013	C017	C01F	C01E	C016	C002	C000
Line Name	**FSL* Page**																				
CBO (valid)	CH001																				
Port DBO (valid)	CH001																				
Control Out	CH002																				
Strobe	CH002																				
Multidevice Response	xx002																				
Service In	xx002																				
Service Out	CH002																				
DBI Bit (valid)	xx004																				
CBI Bit 5 (valid)	xx002																				

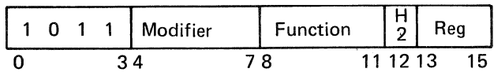
*xx = FB for MLCA
xx = WC for work station attachment B

Attachment Processor Commands

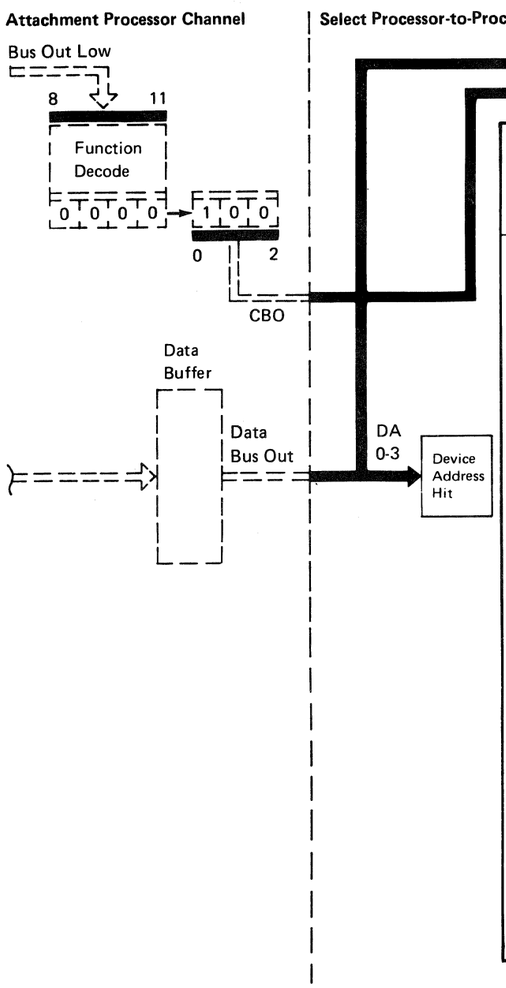
The processor-to-processor interface recognizes the following I/O immediate commands from the attachment processor:

- I/O load
- I/O control load
- I/O sense

These commands are decoded from the function field (bits 8 through 11) and sent to the processor-to-processor interface on CBO bits 0 through 2. The format of the I/O immediate command is:



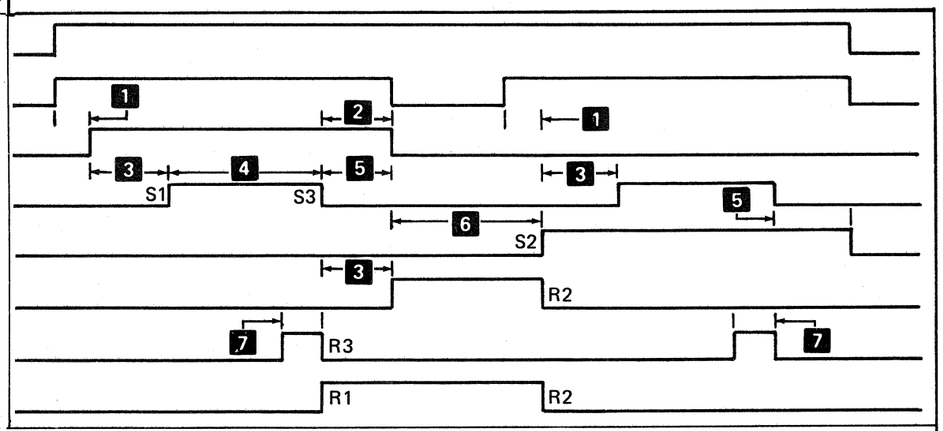
I/O Load Command



CCB 0 1 2	CCB 3 4 5 6	DBO Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
100 I/O Load	0 0 0 0 Load CP CBI buffer			CP CBI bit 2	CP CBI bit 3	CP CBI bit 4	CP CBI bit 0	Operation end to CP	Operation end to attachment processor
	0 0 0 1 Load data buffer 1	DBO bits to data buffer 1							
	0 0 1 0 Load data buffer 2	DBO bits to data buffer 2							
	0 0 1 1 Reset interrupt level X request								
	0 1 0 0 Reset interrupt level Y request								
	0 1 0 1 Load attachment processor CBI buffer	CBI bit 0	CBI bit 1	CBI bit 2	CBI bit 3				Data count bit 0
	0 1 1 0 Enable interrupt level X conditions		Condition C	Condition B	Condition A		Reserved	Cycle steal operation end	Master enable
	0 1 1 1 Disable interrupt level X conditions		Condition C	Condition B	Condition A		Reserved	Cycle steal operation end	Master disable

IO Load Command (continued)

Line Name	FSL* Page
I/O CBO valid	xx014
I/O DBO valid	xx012
I/O Control Out	xx014
I/O Strobe	xx014
I/O Service Out	xx014
I/O CBI Valid	xx004
I/O CBI Bit 5 Valid	xx008
I/O Service In	xx008



Note: The lines shown on these timing charts are available at card tab pins, but, except for the control processor commands, there is no way that the program or the command can be placed in a loop to scope the lines.

* xx = FB for the MLCA
xx = WC for the work station attachment B

1 = 100 ns minimum

2 = 200 ns minimum

3 = 200 ns

4 = 400 ns

5 = 200 ns minimum
= 500 ns maximum

6 = 200 ns minimum
= 1 μs maximum

7 = 100 ns

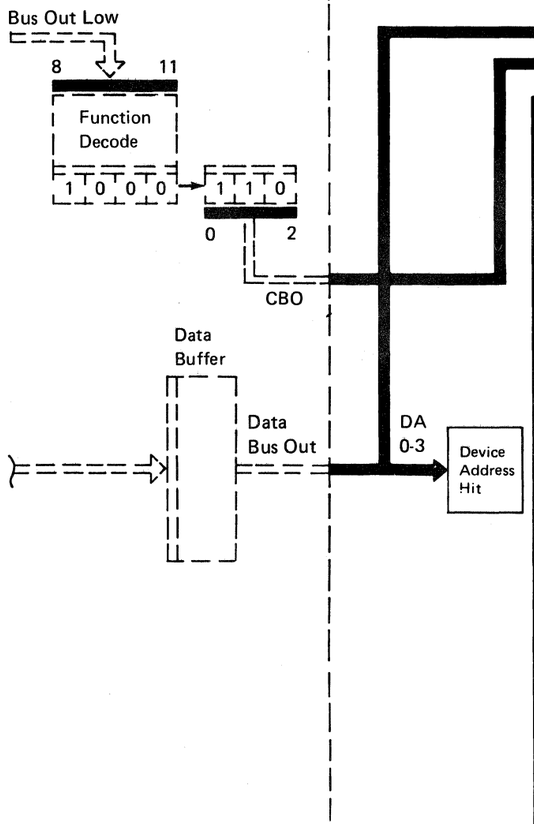
S(n) = Stimulus (n)

R(n) = Response to stimulus (n)

Modifier Port DBO 4 5 6 7	Port DBO Bit	Command	Action Taken	FSL[1] Page
0 0 0 0	2-7	Load control processor CBI buffer	Loads the control processor CBI buffer and selects operation end interrupt	xx004
0 0 0 1	0-7	Load data buffer 1	Loads I/O DBO bits 0-7 into data buffer 1	xx004
0 0 1 0		Load data buffer 2	Loads I/O DBO bits 0-7 into data buffer 2	xx004
0 0 1 1		Reset interrupt level X request	Resets the 'interrupt level X request' latch	xx010
0 1 0 0		Reset interrupt level Y request	Resets the 'interrupt level Y request' latch	xx010
0 1 0 1	0-3, 7	Load attachment processor CBI buffer	Loads the attachment processor CBI buffer and the high-order bit of the byte counter	xx004
0 1 1 0	3-7	Enable interrupt level X conditions	Sets the enable interrupt latches for interrupt level X request	xx010
0 1 1 1	3-7	Disable interrupt level X conditions	Resets the enable interrupt latches for interrupt level X request	xx010

[1]xx = FB for MLCA; WC for work station attachment B

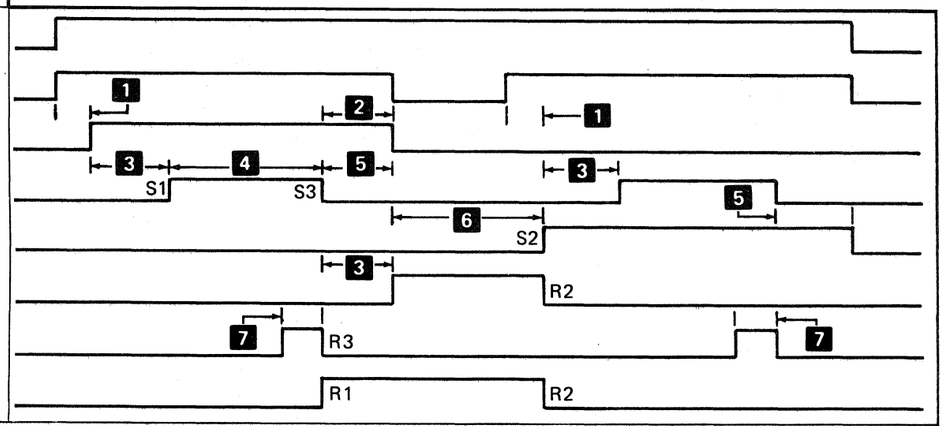
I/O Control Load Command



CCB 0 1 2	CCB 3 4 5 6	DBO Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
110 I/O Control Load	0 0 0 0 Reset processor-to-processor interface								
	0 0 0 1 Set spare latch				Set spare latch				
	0 0 1 0 Load byte counter/ start CS xfer	DBO bits to byte counter							
	0 0 1 1 Load cycle steal pacer	Pacer bit 0	Pacer bit 1						
	0 1 0 1 Set interrupt level A condition/enable/ disable cycle steal	Disable cycle steal			Enable cycle steal	Set level A condition B	Set level A condition A		
	0 1 1 0 Reset interrupt level X conditions	Operation end	Reserved	Attachment processor condition			Condition C	Condition B	Condition A
	0 1 1 1 Interrupt level Y controls		Reset level Y condition	Set level Y condition		Reset CP condition	Master disable	Master enable	Set level Y condition

I/O Control Load Command (continued)

Line Name	FSL* Page
I/O CBO valid	xx014
I/O DBO valid	xx012
I/O Control Out	xx014
I/O Strobe	xx014
I/O Service Out	xx014
I/O CBI Valid	xx004
I/O CBI Bit 5 Valid	xx008
I/O Service In	xx008



Note: The lines shown on these timing charts are available at card tab pins, but, except for the control processor commands, there is no way that the program or the command can be placed in a loop to scope the lines.

* xx = FB for the MLCA
xx = WC for the work station attachment B

1 = 100 ns minimum

2 = 200 ns minimum

3 = 200 ns

4 = 400 ns

5 = 200 ns minimum
= 500 ns maximum

6 = 200 ns minimum
= 1 μs maximum

7 = 100 ns

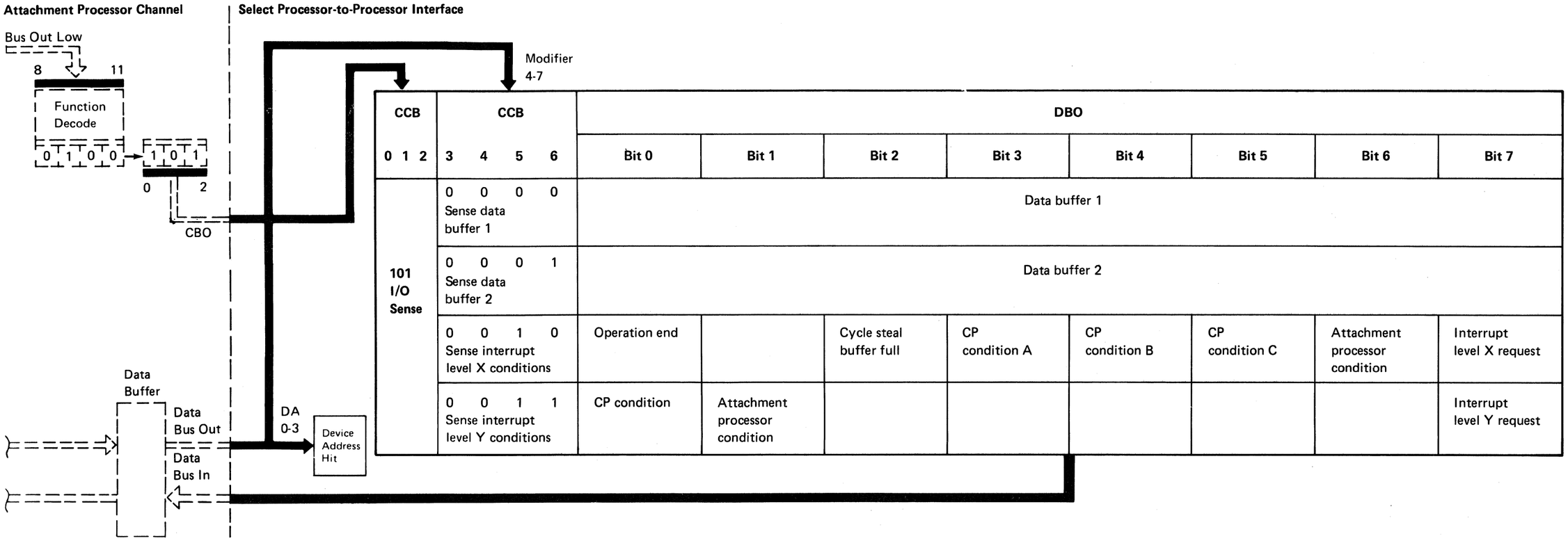
S(n) = Stimulus (n)

R(n) = Response to stimulus (n)

Modifier Port DBO 4, 5, 6, 7	Port DBO Bit	Command	Action Taken	FSL[1] Page
0 0 0 0		Reset processor-to-processor interface	Resets all latches and registers in the processor-to-processor interface, except the device address register, the CP interrupt level register, and the SILSB response bit register	
0 0 0 1	3	Set spare latch	Sets the spare latch	xx008
0 0 1 0	0-7	Load byte counter and start cycle steal transfer	Loads DBO bits 0-7 into the byte counter and starts a cycle steal transfer	xx006
0 0 1 1	0-1	Load cycle steal pacer	Loads DBO bits 0 and 1 into the cycle steal pacer register	xx006
0 1 0 1	0, 3-5	Set interrupt level A conditions Enable/disable cycle steal	Sets condition latches for interrupt level A and enables or disables a cycle steal transfer	xx004
0 1 1 0	0-2, 5-7	Reset interrupt level X conditions	Resets condition latches for interrupt level X request	xx010
0 1 1 1	1, 2, 4-7	Interrupt level Y controls	Sets/resets latches used with interrupt level Y request	xx010

[1]xx = FB for MLCA; WC for work station attachment B

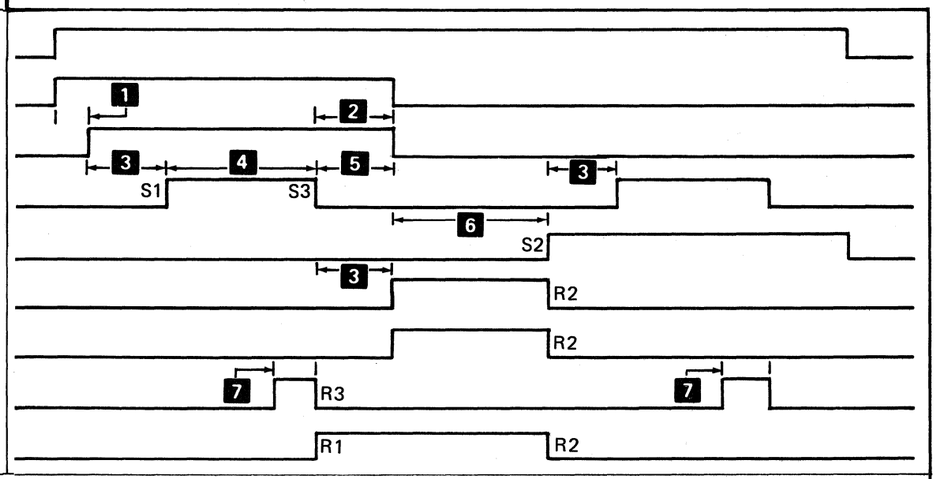
I/O Sense Command



CCB 0 1 2	CCB 3 4 5 6	DBO Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
101 I/O Sense	0 0 0 0 Sense data buffer 1	Data buffer 1							
	0 0 0 1 Sense data buffer 2	Data buffer 2							
	0 0 1 0 Sense interrupt level X conditions	Operation end		Cycle steal buffer full	CP condition A	CP condition B	CP condition C	Attachment processor condition	Interrupt level X request
	0 0 1 1 Sense interrupt level Y conditions	CP condition	Attachment processor condition						Interrupt level Y request

I/O Sense Command (continued)

Line Name	FSL* Page
I/O CBO valid	xx014
I/O DBO valid	xx012
I/O Control Out	xx014
I/O Strobe	xx014
I/O Service Out	xx014
I/O CBI Valid	xx004
I/O DBI Valid	xx010
I/O CBI Bit 5 Valid	xx008
I/O Service In	xx008



Note: The lines shown on these timing charts are available at card tab pins, but, except for the control processor commands, there is no way that the program or the command can be placed in a loop to scope the lines.

*xx = FB for the MLCA
xx = WC for the work station attachment B

1 = 100 ns minimum

2 = 200 ns minimum

3 = 200 ns

4 = 400 ns

5 = 200 ns minimum
= 500 ns maximum

6 = 200 ns minimum
= 1 μs maximum

7 = 100 ns

S(n) = Stimulus (n)

R(n) = Response to stimulus (n)

Modifier Port DBO 4, 5, 6, 7	Port DBO Bit	Command	Action Taken	FSL[1] Page
0 0 0 0	0-7	Sense data buffer 1	Gates the contents of the data buffer 1 to the channel or port DBI	xx004
0 0 0 1	0-7	Sense data buffer 2	Gates the contents of the data buffer 2 to the channel on port DBI	xx004
0 0 1 0		Sense interrupt level X conditions	Senses the following interrupt level X conditions:	xx010
	0		Operation end	
	2		Cycle steal buffer full	
	3		CP condition A	
	4		CP condition B	
	5		CP condition C	
	6		Attachment processor condition	
	7		Interrupt level X request	
0 0 1 1		Sense interrupt level Y conditions	Sense the following interrupt level Y conditions:	xx010
	0		CP condition	
	1		Attachment processor condition	
	7		Interrupt level Y request	

[1]xx = FB for MLCA; WC for work station attachment B

Data Transfer Modes

Data transfer between control storage or main storage and the attachment processor storage is done by cycle steal operations. Single byte base cycle steal is used to send data between control storage or main storage and the processor to processor interface. Single byte burst cycle steal is used to send data between the attachment processor storage and the processor-to-processor interface. Either the control processor or the attachment processor can start a cycle steal operation by sending the following instructions to the processor-to-processor interface:

- IOL0: Load control processor CBI buffer
- IOL5: Load attachment processor CBI buffer
- IOCL2: Load data counter/start cycle steal

A maximum of 511 bytes of data can be transmitted during one cycle steal operation.

When the IOCL2 command is sent, the processor-to-processor interface sets the 'data transfer active' latch and activates the 'cycle steal request' line to the transmitting processor (base cycle steal request to the control processor or cycle steal request to the attchment processor). This signals the transmitting processor to start the cycle steal operation. The first byte of data that is received is loaded into one of two data buffers in the processor-to-processor interface, which sets the 'buffer full' latch associated with that data buffer. The transmitting processor then sends the second byte of data, which is loaded into the other data buffer, and sets the 'buffer full' latch. When both buffer full latches are set, the processor-to-processor interface deactivates the 'cycle steal request' line to the transmitting processor. As soon as the first buffer full latch is set, the 'cycle steal request' line to the receiving processor is activated. This signals the receiving processor that a byte of data is available in the processor-to-processor interface.

The receiving processor then starts the cycle steal operation. This operation takes the first byte of data from the processor-to-processor interface data buffer and resets the 'buffer full' latch. As soon as a reset 'buffer full' latch is sensed the 'cycle steal request' line to the transmitting processor is again activated causing the transmitting processor to send the third byte of data to the processor-to-processor interface. This sequence between the processor-to-processor interface and the two processors continues until the data counter is zero (at which time the 'data transfer active' latch is reset). The operation end interrupt will be sent to the selected processor after both 'buffer full' latches and the 'data transfer active' latch are reset.

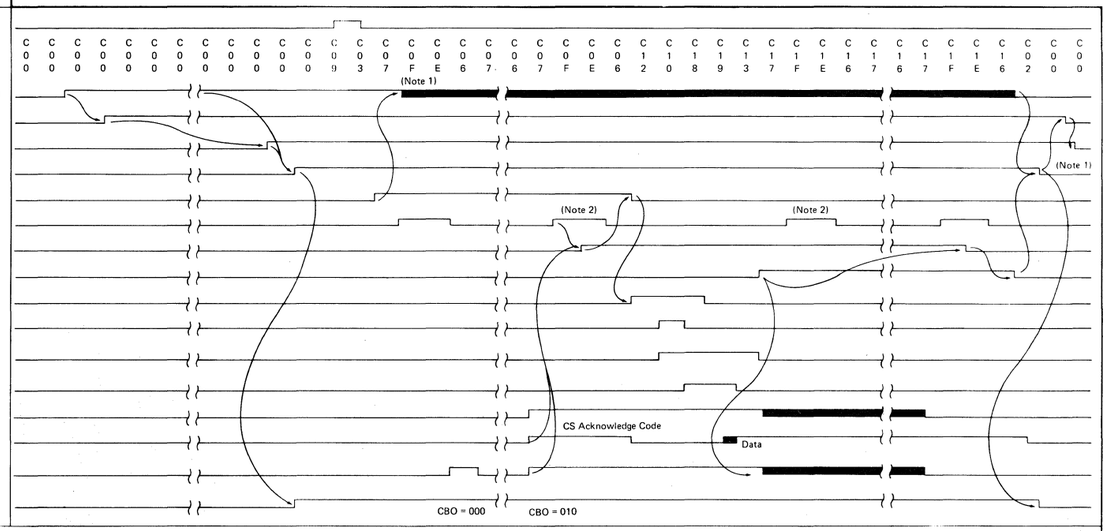
The processor-to-processor interface permits a temporary stop of data transmission during a cycle steal operation. The control processor can disable/enable cycle steals by activating the 'inhibit base cycle steal request' line. The attachment processor can cause a temporary stop during a cycle steal by sending the I/O instruction (IOCL5) to the processor-to-processor interface. Either processor can stop a cycle steal operation by sending an IOL0 instruction to the processor-to-processor interface. If the IOL0 instruction is used, the operation end interrupt will not be sent to either processor.

The processor-to-processor interface can control the data transfer rate by using the cycle steal pacer. The pacer is a 2-bit counter driven by the 4-microsecond clock from the control processor. The data transfer rate is controlled by the reset value of the 2-bit counter. One of four pacer counter values can be loaded during initialization of the processor-to-processor interface.

The pacer controls the data transfer rate by delaying the base cycle steal request to the control processor. The times per byte for data transfers between the control processor and the processor-to-processor interface for the four pacer values are as follows: 4.4 microseconds (no delay), 12 microseconds, 16 microseconds, and 20 microseconds.

Base Cycle Steal (Control Processor to Processor-to-Processor Interface) Bidirectional

Line Name	Sequence of Occurrence	FSL Page
T3 Lth		
C-Times (port clocks)		PC526
Base Cycle Steal Request*	1	CH009
Latched Block Processor Clock	2	PC508
T7 Pwrd	3	PC110
Base Cycle Mode (base cycle steal lth)	4	PC534
Control Out Pwrd	7	PC510
Strobe Pwrd	10	PC510
Service In*	11	PC518
Service Out Pwrd	16	PC510
Storage Cycle Request	12	PC508
Clock SAR and X Reg (T8 time)	13	PC142
Storage Cycle Time** (storage function)	14	PC012
CSY Trigger to Channel	15	PC030
Command Bus In (CBI) Valid*	8	
DBO (MPXPO bus out)	6	PC506
DBI (MPXPO data in) Valid (if applicable)*	9	
Command Bus Out (CBO)	5	PC542

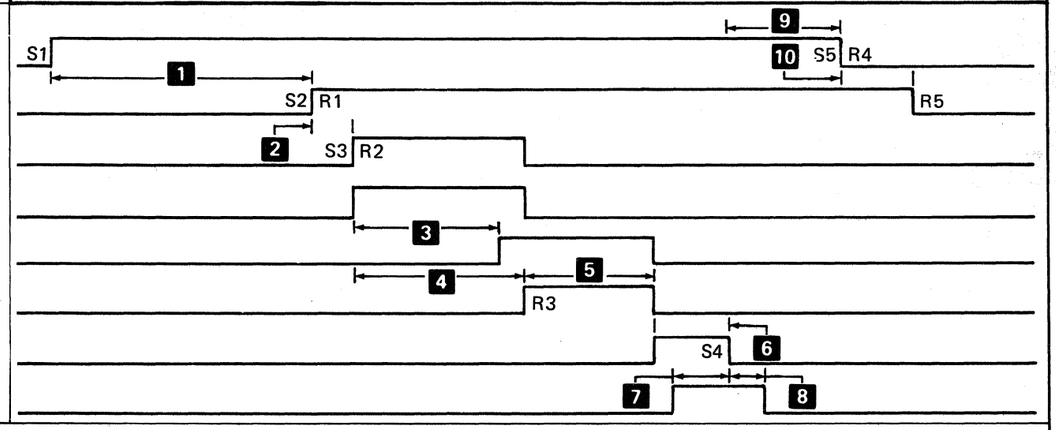


Notes:
1. This example shows only one base cycle steal occurring. The entire handshaking sequence would occur again if 'base cycle steal request' remained active beyond the time shown (provided no disk cycle steals were requested).
2. If the I/O device responds to 'control out pwrd' and 'service out pwrd' in synchronous operation, one strobe will occur under 'service out pwrd' and two strobes will occur under 'control out pwrd'. Otherwise, up to 7 strobes may occur in each portion of the sequence for asynchronous operation. If 8 strobes occur, a time-out occurs and a blast is generated.

*Signifies signals for the device attachment to the base port card.
**The 'storage cycle time' consists of the time for loading the storage address register (T8), the time for accessing storage (X CSY Tgr), and a time for storing data to the I/O attachment.

Burst Cycle Steal (Attachment Processor to Processr-to-Processor)

Line Name	FSL* Page
BPC Powered	xx006
Burst Mode Operation	xx006
Burst Cycle Steal Request	xx006
I/O CBI Valid	xx004
I/O DBI Valid	xx010
CSY Trigger	xx016
I/O Strobe	xx014
I/O DBO Valid	xx006



Note: The lines shown on these timing charts are available at card tab pins, but there is no way that the program or the command can be placed in a loop to scope the lines.

*xx = FB for the MLCA
xx = WC for the work station attachment B

1 = 700 ns minimum

2 = 100 ns maximum

3 = 400 ns maximum (for writing into storage)

4 = 950 ns maximum

5 = 300 ns

6 = 200 ns

7 = 150 ns
8 = 100 ns
} (for reading from storage)

9 = 700 ns maximum

10 = 400 ns maximum

Control Processor Interrupts

The control processor receives interrupts from the processor-to-processor interface on the 'interrupt A request' line. This line is made active by conditions that are controlled by I/O commands or by the hardware. These conditions are:

- Two conditions that are controlled by I/O commands from the attachment processor
- One condition that is controlled by I/O commands from the control processor
- Two conditions that can occur in the hardware

The control processor controls the reset of all the latches that can cause the 'interrupt A request' line to be active.

Attachment Processor Conditions

Either of these two conditions needs a series of latches to be turned on.

- The control processor turns on the 'enable/disable attachment processor condition A or condition B' latch and the 'master enable/disable' latch by using an IOL6 command.
- The attachment processor turns on the 'attachment processor' latch.

Control Processor Conditions

This condition is used for diagnostic purposes and does not have an enable/disable latch.

- The control processor, using an IOCL6 command, turns on the 'control processor condition' latch.
- The control processor, using an IOL6 command, turns on the 'master enable/disable' latch.

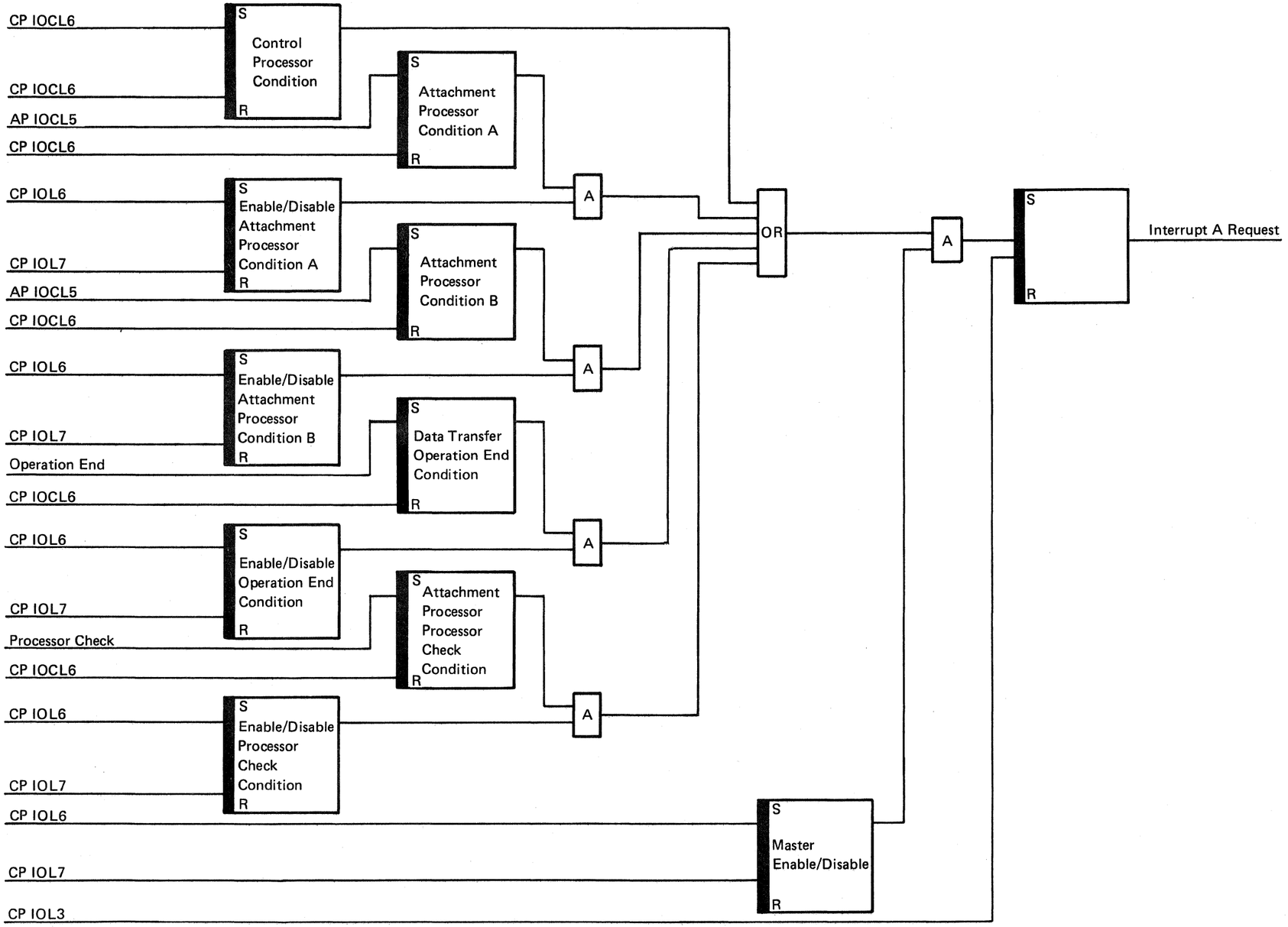
Hardware Conditions

The two conditions that can occur in the hardware are:

- Operation end interrupt: This interrupt indicates that a data transmission has been completed without a hard error.
  - The operation end interrupt turns on the 'data transfer operation end condition' latch.
  - The control processor, using an IOL6 command, turns on the 'enable/disable' latch and the master 'enable/disable' latch.
- Processor check interrupt: This interrupt indicates that the attachment processor has stopped running because of a hard error.
  - The processor check signal line turns on the 'attachment processor check condition' latch.
  - The control processor, sending an IOL6 command, turns on the 'enable/disable' latch and the 'master enable/disable' latch.

Resetting the 'Interrupt A Request' Line

The control processor must wait until any one of the latches turned on in the process of activating the interrupt is reset. Then the processor, using an IOL3 command, resets the 'interrupt A request' line.



AP = Attachment Processor
CP = Control Processor

Attachment Processor Interrupts

The attachment processor receives interrupts from the processor-to-processor interface through two lines, 'interrupt X request' and 'interrupt Y request'. The following information describes the conditions needed to activate either of these interrupt request lines.

Interrupt X Request

This line is made active by conditions that are controlled either by I/O commands or by the hardware. These conditions are:

- Three conditions that are controlled by I/O commands from the control processor
- One condition that is controlled by an I/O command from the attachment processor
- One condition that is made active by the hardware

The attachment processor controls the reset of all the latches that can cause the 'interrupt X request' line to be active.

Control Processor Conditions

Any of the three conditions needs a series of latches to be turned on.

- The attachment processor, using an IOL6 command, turns on one of the 'enable/disable' latches and the 'master enable/disable' latch.
- The control processor, using an IOCL7 command, turns on the suitable 'control processor condition' latch.

Attachment Processor Conditions

This condition does not have an 'enable/disable' latch.

- The attachment processor, using an IOCL7 command, turns on the 'attachment processor condition' latch.
- The attachment processor, using an IOL6 command, turns on the 'master enable/disable' latch.

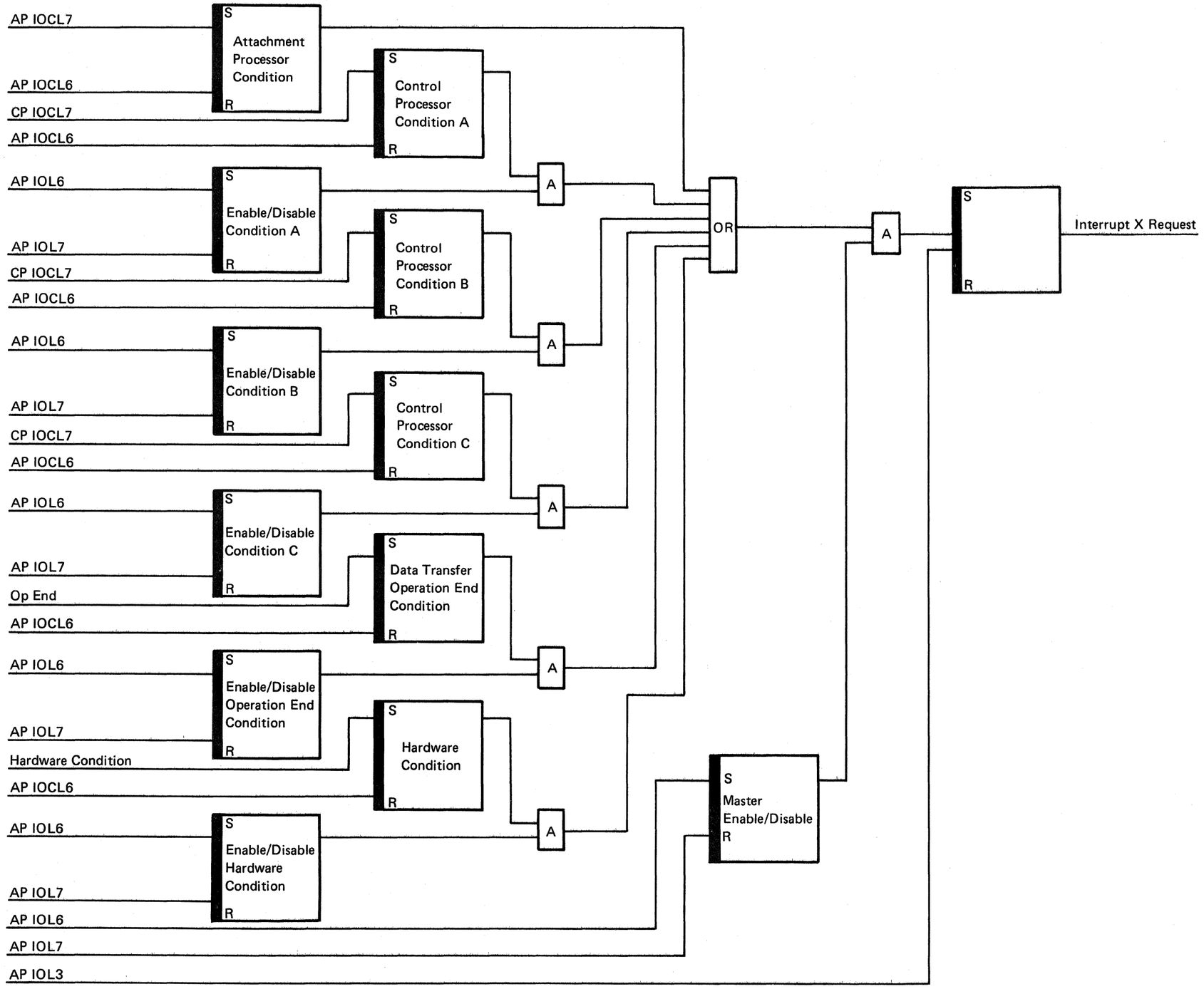
Hardware Condition

An operation end interrupt causes this condition. The interrupt indicates that a data transmission has been completed without a hard error.

- The operation end interrupt turns on the 'data transfer operation end condition' latch.
- The attachment processor, using an IOL7 command, turns on the 'enable/disable operation end condition' latch and the 'master enable/disable' latch.

Resetting the 'Interrupt X Requst' Line

The attachment processor must wait until any one of the latches turned on in the process of activating the interrupt is reset. Then the processor, using an IOL3 command, resets the 'interrupt X request' line.



AP = Attachment Processor
CP = Control Processor

Interrupt Y Request

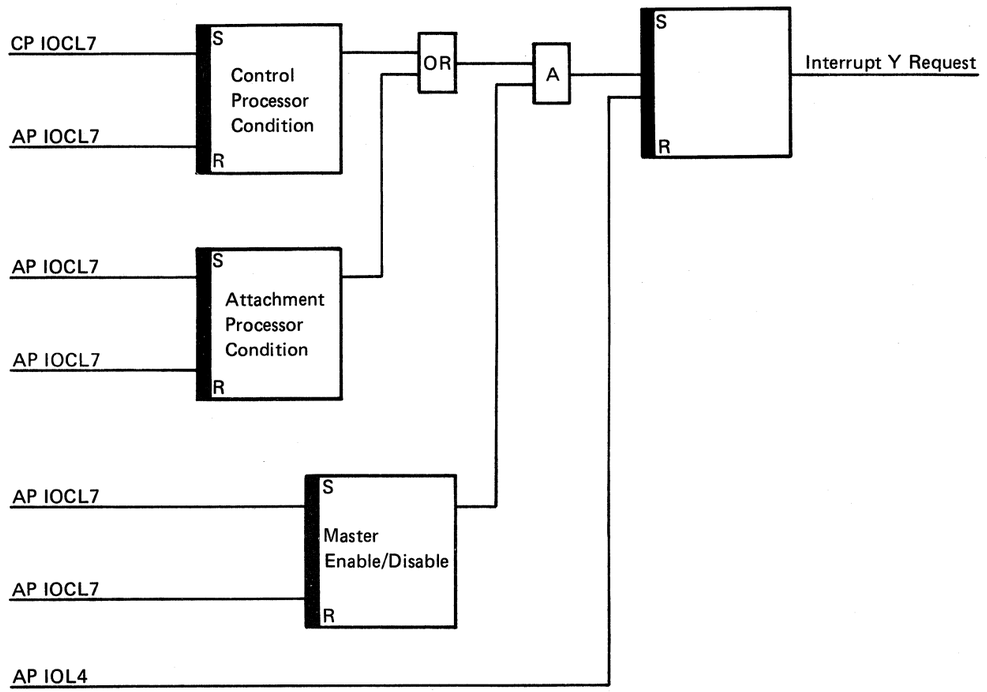
This line is made active by conditions that are controlled by an I/O command sent by either the control processor or the attachment processor.

The attachment processor controls the reset of the latches that can cause the 'interrupt Y request' line to be active.

- Control processor
  - The control processor, using an IOCL7 command, turns on the 'control processor condition' latch.
  - The attachment processor, using an IOCL7 command, turns on the 'master enable/disable' latch.
- Attachment processor
  The attachment processor, using an IOCL7 command, turns on the 'attachment processor condition' latch and the 'master enable/disable' latch.

Resetting the 'Interrupt Y Request' Line

The attachment processor, must wait until either of the latches turned on in the process of activating the interrupt is reset. Then the processor using an IOL4 command, resets the 'interrupt Y request' line.



AP = Attachment Processor
CP = Control Processor

ATTACHMENT PROCESSOR CHANNEL OPERATIONS

Commands

The two instructions that communicate with the processing unit, the channel, the processor-to-processor interface (PPI), and the I/O attachment are:

- I/O immediate
- I/O storage

When executing the I/O command, the processing unit selects WR0 low from the local storage register stack for the current interrupt level and sends its contents to the channel.

The format of WR0 low is:

	WR0 Low Bits	
Device	**0-3**	**4-7**
	Hexadecimal Address	
Channel	0	0
Communications	8	0
Work station attachment	C	0
PPI	F	0

The address part of WR0 low is exchanged for the interrupt level hexadecimal value on a sense interrupt level status byte command. The instruction modifier field (bits 4 through 7 of the I/O instruction) and the device address link together and are sent over the 'data bus out' lines to the correct I/O attachment.

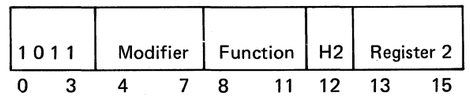
The channel register stores the last command and device address sent by the channel. This information is not destroyed after an error is sensed, and a sample can be taken by the interrupt level 0 (machine check) routine to determine which device caused the error.

The processing unit operates with odd parity; the channel, however, can be set to either even- or odd-numbered parity (see *I/O Load or I/O Control Load* later in this section).

The I/O attachments use the 'CBI bit 4' line to indicate not valid parity on the 'data bus out' lines.

I/O Immediate

I/O Load or I/O Control Load (IOL, IOCL)



This part of the I/O immediate instruction moves 1 byte of data or control information from a local storage register to the I/O attachment.

Modifier (Bits 4 through 7): The modifier bits are specified for the device and are sent to the I/O attachment with the command. These bits specify what is to be done with the data byte.

Function (Bits 8 through 11): The function bits are sent to the channel where they are decoded as either the load or control load command. This command is then sent to the I/O attachment on the 'command bus out' lines.

Bits 8 through 11 = 0000 for IOL

Bits 8 through 11 = 1000 for IOCL

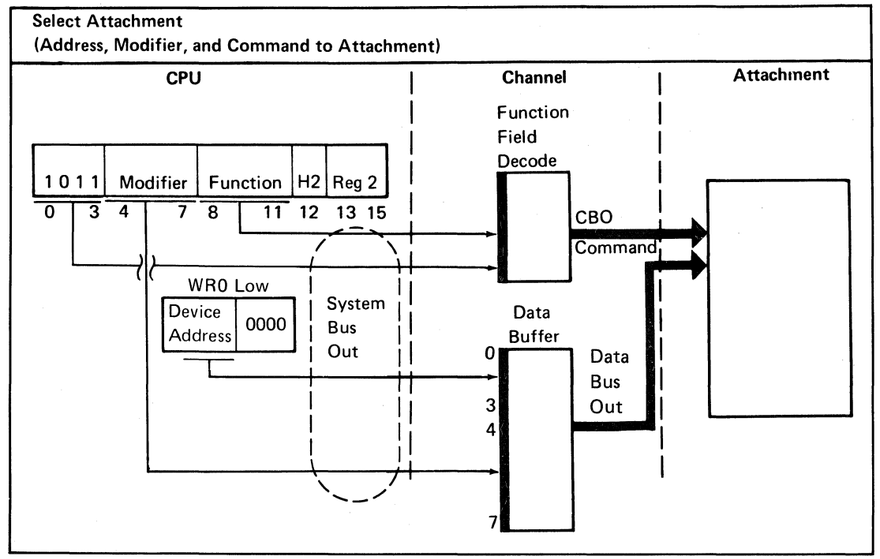
H2 (Bit 12): Selects the low- or high-order byte of the selected local storage register of the current interrupt level:

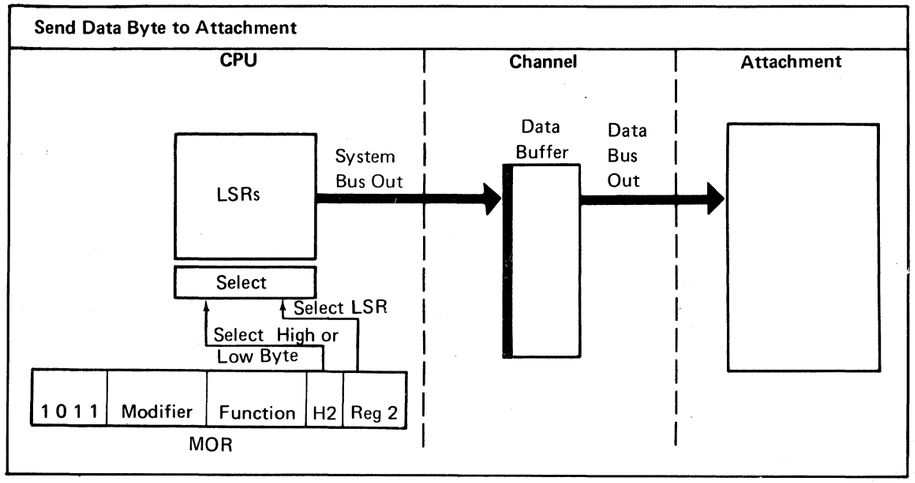
H2 = 0: Low-order byte

H2 = 1: High-order byte

Register 2 (Bits 13 through 15): Selects one of the eight work registers in the local storage register stack for the current interrupt level. The selected register contains the byte of data or control information that is to be sent to the I/O attachment.

Assemble Address and Command in Channel	Select I/O Attachment; Send Command and Modifier to Attachment on CBO and Data Bus Out





I/O Sense or I/O Control Sense (IOS, IOCS)

1011	Modifier	Function	H2	Register 2
0 3	4 7	8 11	12	13 15

This part of the I/O immediate instruction moves 1 byte of data or status type information from the I/O attachment to a local storage register.

Modifier (Bits 4 through 7): The modifier bits are specified for the device and are sent to the I/O attachment with the command. These bits specify which data byte is to be sent.

Function (Bits 8 through 11): The function bits are sent to the channel where they are decoded as either the sense or control sense command. This command is then sent to the I/O attachment on the 'command bus out' lines.

Bits 8 through 11 = 0100 for IOS

Bits 8 through 11 = 1100 for IOCS

H2 (Bit 12): This bit is used to select the low- or high-order byte of the selected local storage register:

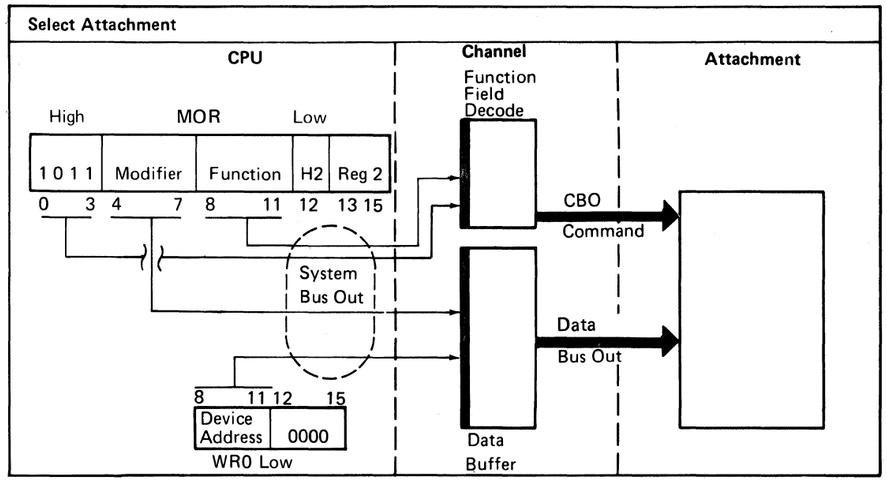
H2 = 0: Low-order byte

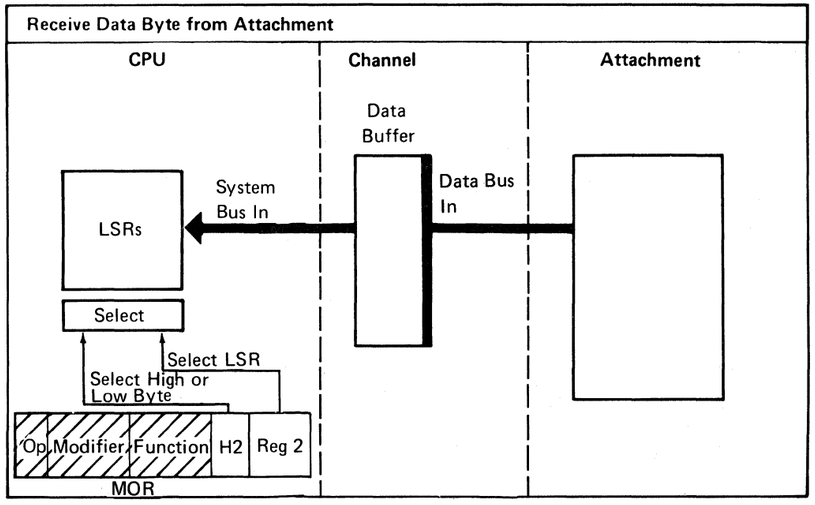
H2 = 1: High-order byte

Register 2 (Bits 13 through 15): Selects one of the eight work registers in the local storage register stack for the current interrupt level. The byte of data being sent from the I/O attachment is placed in this local storage register.

Assemble Address and Command in Channel

Select I/O Attachment; Send Command and Modifier to Attachment on CBO and Data Bus Out





Sense Interrupt Level Status Byte (SILSB)

1011	Modifier	Function	H2	Register 2
0 3	4 7	8 11	12	13 15

This function of the I/O immediate instruction moves 1 byte of status information from the I/O attachment to the selected local storage register. This status byte determines which devices are requesting service on a given interrupt level.

Modifier (Bits 4 through 7): The modifier bits are sent to the I/O attachment with the command.

Function (Bits 8 through 11): The function bits are sent to the channel where they are decoded along with the operation code as a sense interrupt level status byte command. This command is then sent to the I/O attachment on the 'command bus out' lines.

Bits 8 through 11 = 0101

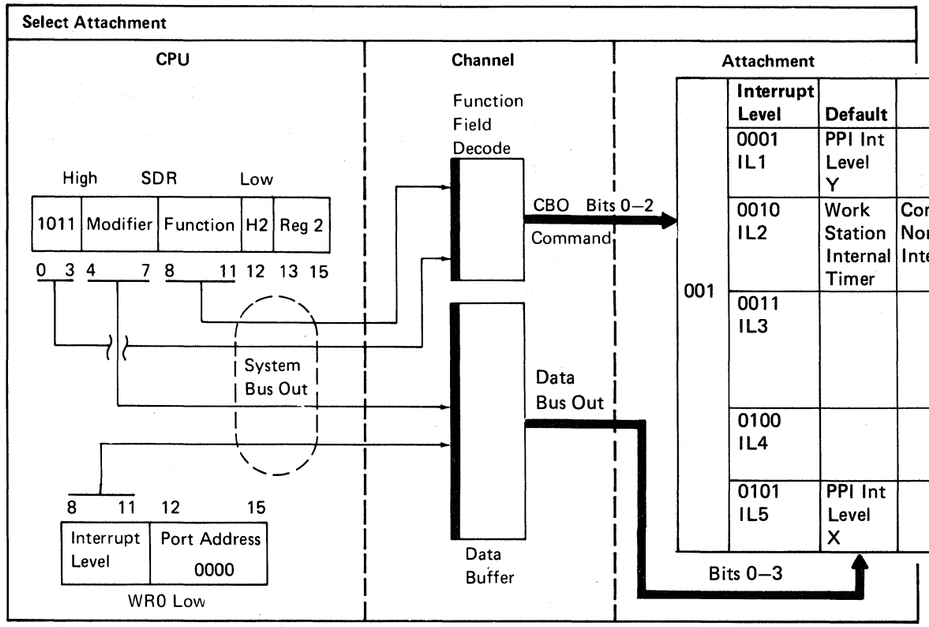
H2 (Bit 12): Selects the low- or high-order byte of the selected LSR of the current interrupt level:

H2 = 0: Low-order byte

H2 = 1: High-order byte

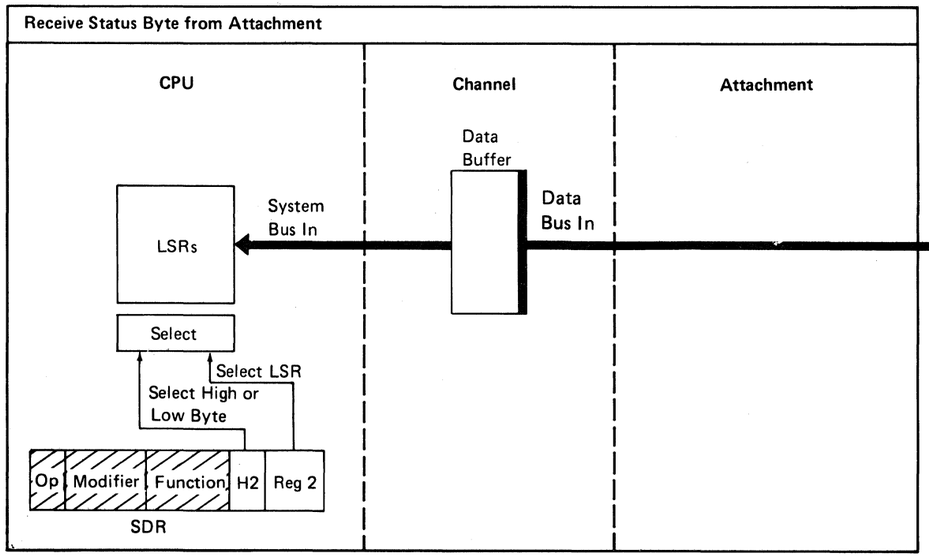
Register 2 (Bits 13 through 15): Selects one of the eight work registers in the local storage register stack for the current interrupt level. The selected register stores the byte of status (information containing the device causing the interrupt level) received from the I/O attachment.

WR0 Low (Bits 8 through 11): Contains the interrupt level hexadecimal value used by the I/O attachment to select the status byte of information to be stored in the selected local storage register.



Interrupt Level	Default	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
0001 IL1	PPI Int Level Y								
0010 IL2	Work Station Internal Timer	Comm-80 Nontime-out Interrupt							
0011 IL3			Comm-40 Nontime-out Interrupt	Comm-20 Nontime-out Interrupt Work Station	Comm-10 Nontime-out Interrupt				
0100 IL4						Comm-80 Time-out Interrupt	Comm-40 Time-out Interrupt	Comm-20 Time-out Interrupt	Comm-10 Time-out Interrupt
0101 IL5	PPI Int Level X								

Send Status Byte to Channel



Note: A more complete description of the sense interrupt level status byte command may be found under *Commands* in the *Channel* section of this manual.

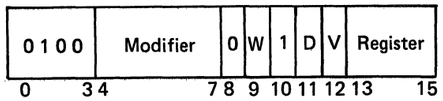
I/O Storage (WTCL, WTCH, RDCL, RDCH)

WTCL (I/O load from storage low)

WTCH (I/O load from storage high)

RDCL (I/O store to storage low)

RDCH (I/O store to storage high)



This instruction moves 1 byte of data between storage and the I/O attachment.

Modifier (Bits 4 through 7): Specifies the control field for the I/O attachment.

The field is moved to the attachment through the channel. Bit 4 of this field is used in the processor to select the high- or low-order byte of storage.

Bit 8: Changes the operation code (bits 0 through 3). Bit 8 is always a 0.

W (Bit 9): Identifies the direction the data is to be moved.

W = 0: Read data from stroage and move it to the I/O attachment

W = 1: Write data to storage from the I/O attachment

D Bit 11: Indicates if the address in the local stroage register (specified by bits 13 through 15) is to be increased or decreased.

D = 0: Increase the selected local storage register by the value of field V

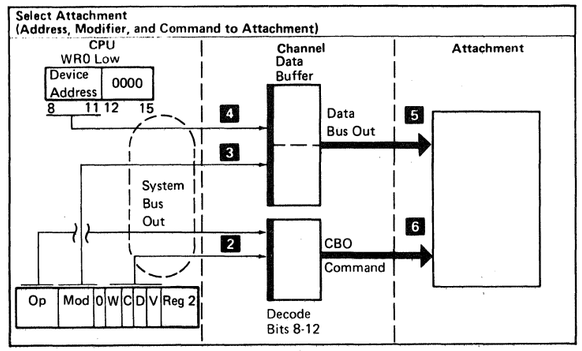
D = 1: Decrease the selected local storage register by the value of field B

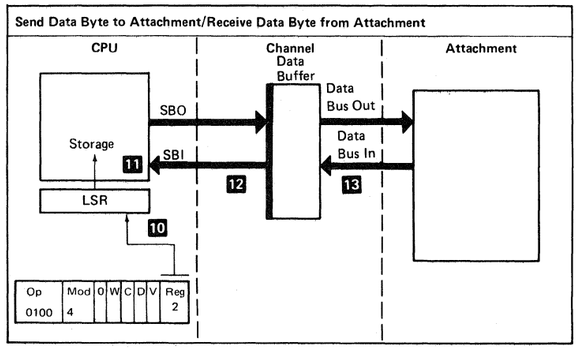
Note: Bits 8 through 11 are sent to the channel where they are decoded as either the load command or the sense command. The command is then sent to the I/O attachment on the 'command bus out' lines.

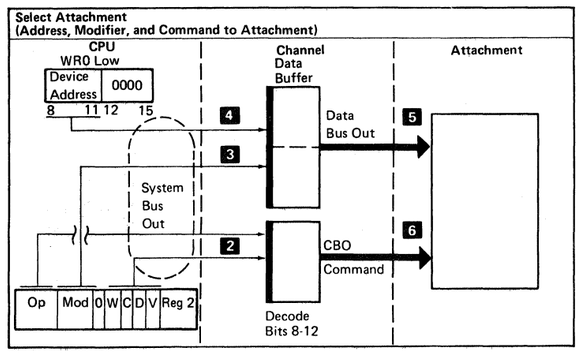
V(Bit 12): Indicates the amount the address in the local storage register (specified by bits 13 through 15) should be increased or decreased. If V = 0, the address in the selceted local storage register is not changed. If V = 1, the address in the selected local storage register is decreased or increased by 1, as specified by the bit setting of field D.

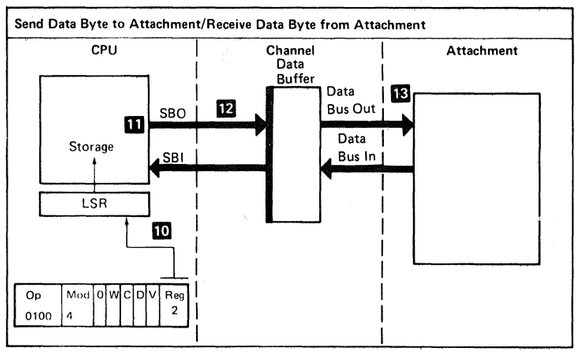
Register 2 (Bits 13 through 15): Selects one of the eight local stroage registers assigned to the present interrupt level that contains the storage address needed to move the data. The address in the specified local storage register may be updated as specified by bit 11 (field D) and bit 12 (field V).

Bits 4 8 9 10 11 12	Mnemonic	Description
0 0 1 1 0 1	RDCL	I/O store to storage, increase register 2 by 1
1 0 1 1 0 1	RDCH	
0 0 1 1 1 1	RDCL	I/O store to storage, decrease register 2 by 1
1 0 1 1 1 1	RDCH	
0 0 1 1 0 0	RDCL	I/O store to storage, no change to register 2
1 0 1 1 0 0	RDCH	
0 0 0 1 0 1	WTCL	I/O load from storage, increase register 2 by 1
1 0 0 1 0 1	WTCH	
0 0 0 1 1 1	WTCL	I/O load from storage, decrease register 2 by 1
1 0 0 1 1 1	WTCH	
0 0 0 1 0 0	WTCL	I/O load from storage, no change to register 2
1 0 0 1 0 0	WTCH	

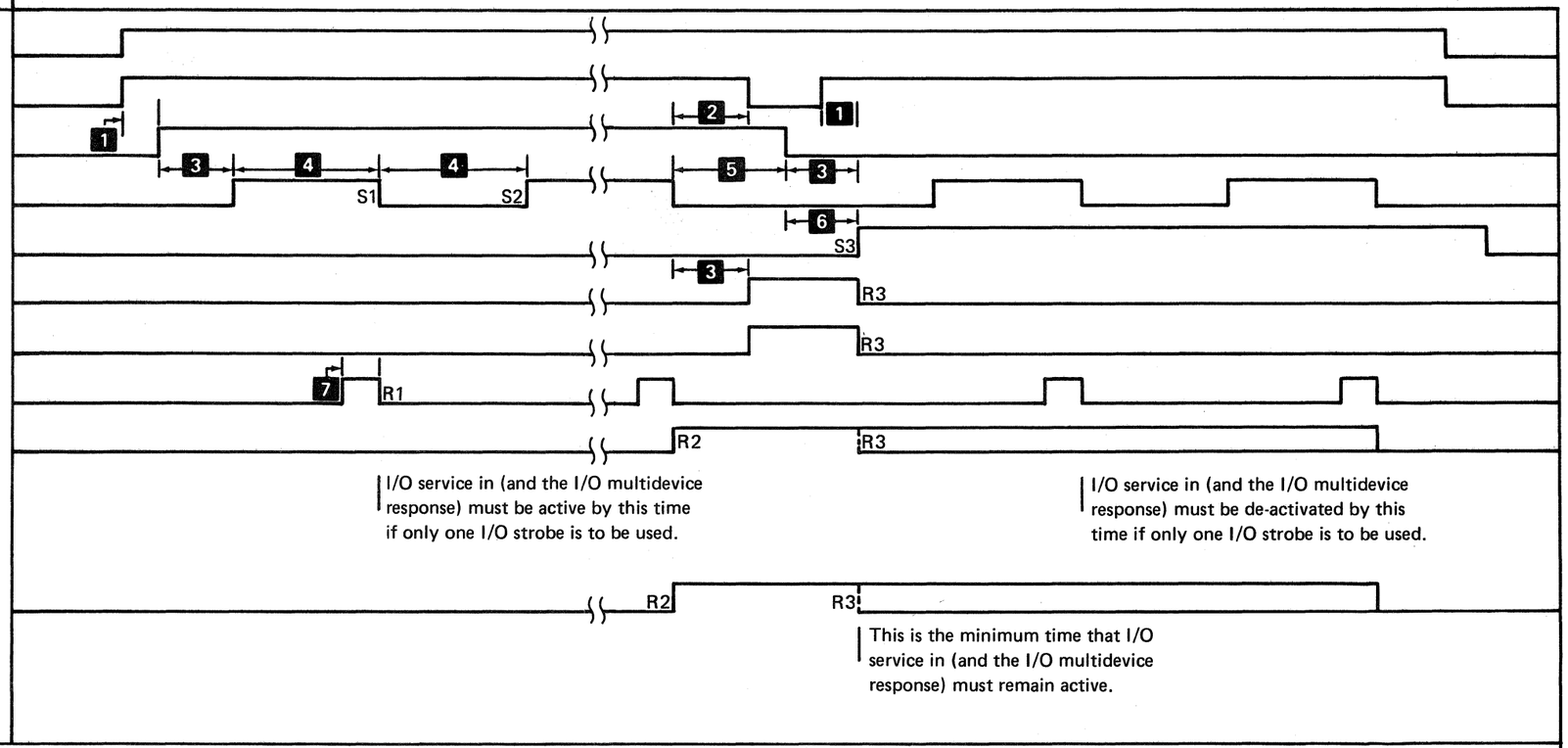








Line Name	FSL* Page
I/O CBO Valid	xx014
I/O DBO Valid	xx012
IYO Control Out	xx014
I/O Strobe	xx014
I/O Service Out	xx014
I/O CBI Valid	xx004
I/O DBI Valid	xx010
I/O CBI Bit 5 Valid	xx008
I/O Service In	xx008
I/O Multidevice Response (if applicable)	xx014



1 = 100 ns minimum

2 = 200 ns minimum

3 = 200 ns

4 = 400 ns

5 = 200 ns minimum
= 500 ns maximum

6 = 200 ns minimum
= 2μs maximum

7 = 100 ns

S(n) = Stimulus (n)

R(n) = Response to stimulus (n)

Note: The lines shown on these timing charts are available at card tab pins, but there is no way that the program or the command can be placed in a loop to scope the lines.

*xx = FB for the MLCA
xx = WC for the work station attachment B

Base Cycle Steal

The attachment controller logic permits the controller to receive base cycle steal requests from up to seven I/O attachments at the same time. The I/O attachments have specific priority levels of cycle steal assigned to them.

During the first part of the cycle steal sequence, the channel executes a sense cycle steal ID (SCSID) command to determine which of the I/O devices is requesting a cycle steal. The I/O attachments requesting a cycle steal respond by making their ID bits active on the DBI. (There are seven identification bits, numbered 1 through 7, with 1 being the highest priority.)

After the channel senses the identification bits, it responds with a cycle steal acknowledge (CSACK). The ID bit for the I/O attachment with the highest priority is made active on the DBO. The I/O attachment that received its ID bit on the DBO responds by making the 'service in' line active. The remainder of the cycle steal sequence is the same as the sequence for an I/O command.

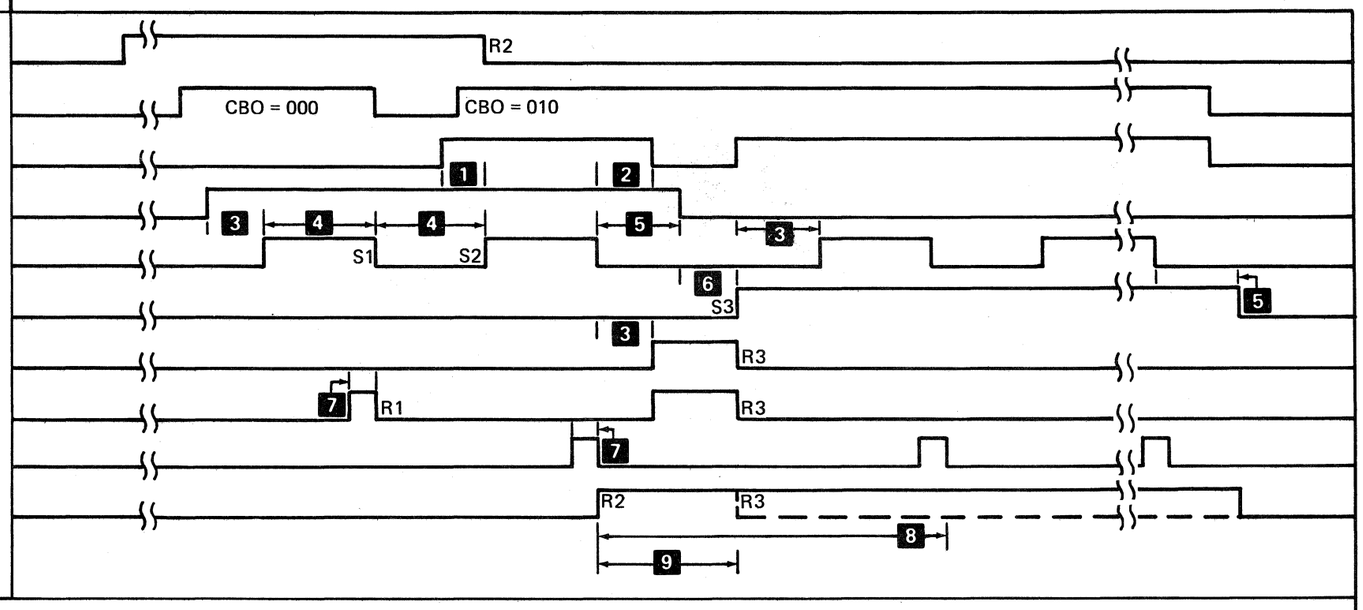
The following table shows the codes used for the acknowledgment of base cycle steal. The table also shows the priorities assigned to those codes.

DBI Input Bits Available During an SCSID Command	DBO Codes Used for Acknowledgment
0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7
* 1 * * * * * *	1 1 0 0 0 0 0 0
* 0 1 * * * * *	1 0 1 0 0 0 0 0
* 0 0 1 * * * *	1 0 0 1 0 0 0 0
* 0 0 0 1 * * *	1 0 0 0 1 0 0 0
* 0 0 0 0 1 * *	1 0 0 0 0 1 0 0
* 0 0 0 0 0 1 *	1 0 0 0 0 0 1 0
* 0 0 0 0 0 0 1	1 0 0 0 0 0 0 1
0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

*The condition of this bit is not important.

Base Cycle Steal (continued)

Line Name	FSL* Page
Base Cycle Steal Request	xx022
I/O CBO Valid	xx014
I/O DBO Valid	xx012
I/O Control Out	xx014
I/O Strobe	xx014
I/O Service Out	xx014
I/O CBI Valid	xx004
I/O DBI Valid	xx010
I/O CBI Bit 5 Valid	xx008
I/O Service In	xx008



1 = 100 ns minimum

2 = 200 ns minimum

3 = 200 ns

4 = 400 ns

5 = 200 ns minimum
= 500 ns maximum

6 = 200 ns minimum
= 2 μs maximum

7 = 100 ns minimum

8 Service in must not be active by this time if only one strobe is desired.

9 Minimum time that service in must remain active.

S(n) = Stimulus (n)

R(n) = Response to stimulus (n)

Note: The lines shown on these timing charts are available at card tab pins, but there is no way that the program or the command can be placed in a loop to scope the lines.

*xx = FB for the MLCA
xx = WC for the work station attachment B

Interrupts

The attachment processor sequentially executes instructions. The sequence can be changed by a branch instruction, a jump instruction, or by a change in the interrupt level. To control the program, the attachment processor uses the main program level, six levels of interrupts, and two levels of cycle steal requests.

The priorities specified for interrupt and cycle steal requests are:

Priority	Interrupt Level or Cycle Steal Request
1	Interrupt
2	Burst cycle steal
3	Base cycle steal
4	Interrupt level 1
5	Interrupt level 2
6	Interrupt level 3
7	Interrupt level 4
8	Interrupt level 5
9	Main program level

Either an I/O adapter or the processor-to-processor interface can make an interrupt request by activating an interrupt request line. When an interrupt request line becomes active, the priority of that interrupt level determines if the processor will take action on the interrupt or continue executing the program at the present interrupt level. If an incoming interrupt request has higher priority than the interrupt level on which the processor is operating (and interrupts are enabled) the processor starts executing instructions on the higher priority interrupt level.

Because interrupt levels have priority assigned to them, any interrupt request whose priority level is lower than the level being operated on in the processor must wait. Having completed all higher level interrupts, the processor completes the lower level interrupt requests.

When not operating on interrupts, the attachment processor executes instructions on the main program level.

Associated with the main program level and each interrupt level is a group of eight, 16-bit work registers and two address registers in the local storage register (LSR) stack. Interrupt level 0 and the main program level share the same group of work registers. The two address registers are the MAR and the MAB. The MAR stores the address of the instruction being executed at present. When a return instruction is issued, the MAB stores the next sequential instruction address after a branch and link instruction.

Local Storage Register (LSR) Operational Use	LSR Address in Hexadecimal	LSR Name
Main program level	00	WR0
or	01	WR1
Machine check 0	02	WR2
	03	WR3
	04	WR4
	05	WR5
	06	WR6
	07	WR7
MAR or MAB stack 1	08	MAR (main)
	09	MAB (main)
	0A	MAR (MC)
	0B	MAB (HC)
	0C	MAR interrupt level 1)
	0D	MAB (interrupt level 1)
	0E	MAR (interrupt level 2)
Interrupt level 1	10	WR0
and	11	WR1
Burst cycle steal	12	WR2
	13	WR3
	14	WR4 or CS0
	15	WR5 or CS1
	16	WR6 or CS2
	17	WR7 or CS3
Interrupt level 2	18	WR0
	19	WR1
	1A	WR2
	1B	WR3
	1C	WR4
	1D	WR5
	1E	WR6
	1F	WR7

Local Storage Register (LSR) Operational Use	LSR Address in Hexadecimal	LSR Name
Interrupt level 3	20	WR0
	21	WR1
	22	WR2
	23	WR3
	24	WR4
	25	WR5
	26	WR6
	27	WR7
MAR or MAB	28	MAR (interrupt level 3)
stack 2	29	MAB (interrupt level 3)
	2A	Spare
	2B	Spare
	2C	MAR (interrupt level 4)
	2D	MAB (interrupt level 4)
	2E	MAR (interrupt level 5)
	2F	MAB (interrupt level 5)
Interrupt level 4	30	WR0
and	31	WR1
Base cycle steal	32	WR2
	33	WR3
	34	WR4 or CS0
	35	WR5 or CS1
	36	WR6 or CS2
	37	WR7 or CS3
Interrupt level 5	38	WR0
	39	WR1
	3A	WR2
	3B	WR3
	3C	WR4
	3D	WR5
	3E	WR6
	3F	WR7

Because there is a specified group of registers for each interrupt level, no data is lost when an interrupt is stopped to permit a higher level interrupt to operate. All the interrupt levels use the same processor condition register, therefore, the contents of this register must be kept at the start of the interrupt and returned when the interrupt is complete.

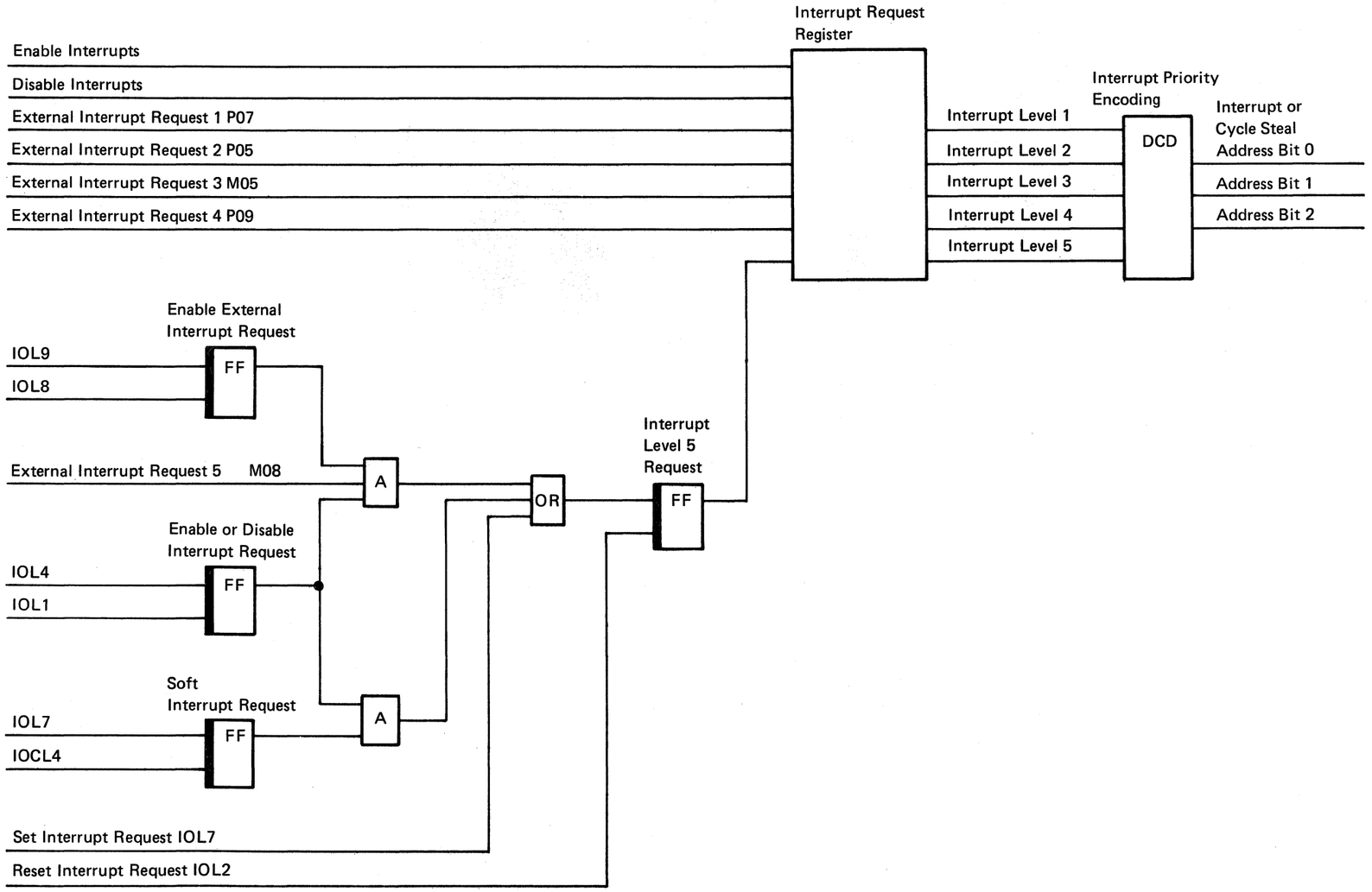
See the logic in the following figure:

Note that the processor can enable or disable interrupt levels 1 through 5. The interrupt level 5 request latch can be activated in three different ways: the latch can be turned on by an external interrupt and also by either of two separate I/O commands.

Fixed-Interval Timer

An 8-millisecond timer permits interrupt requests to be received at the attachment processor at specified intervals. The 8-millisecond, fixed-interval timer receives input from the 1-millisecond clock in the control processor channel. The fixed-interval timer is enabled, disabled, or reset by I/O instructions from the attachment processor.

The output of the fixed-interval timer is available on a tab pin on the card so it can be used with any of the five external interrupt request lines.



STORAGE INTERFACE

The controls for the storage in the attachment processor include signals for reading, writing, and refreshing the information already in storage. The storage interface can address a maximum of 64K words of storage. These words are 2 bytes in length. The storage data bus is 2 bytes wide and is used for both reading and writing. All information is read from storage 2 bytes at a time; writing into storage can be either 1 or 2 bytes at a time.

The following table describes the signals on the interface:

Line Name	Purpose of the Line
Storage data bus	This 2-byte wide bus is used for both reading and writing in storage. The bus carries 16 data bits plus two parity bits.
SAR bus	This 14-bit bus is used to address storage. The seven high-order bits are used only for reading and writing. The seven low-order bits are used for reading and writing and also for refreshing the information already in storage.
Read/ Write	This line indicates to storage the type of operation to be performed.
RFM 1 and 2	This 2-bit bus is used to select either the high byte, or both bytes on the storage data bus during a write operation. During a read operation, both lines of the bus are active. The bus is not active while storage is being refreshed.
Strobe	This line is used as a gate for reading and is only active during read operations.
Refresh select	This line is used to request a stroage cycle to refresh storage. The line is not active during read and write operations.
Card select	There are four card select lines. These lines are used to select one of four 16K (2-bytes wide) blocks of storage. The select lines are only active during read or write operations and only one line is active at a time.

Read Cycle

The sequence for read operation is shown in the following timing chart:

Line Name	FSL* Page	Cycle Timing
Card Select	xx032	T=0, T1, T2
SAR Valid	xx034	T3, T4
RFM 1 and 2	xx036	T5, T6
Read	xx036	T7, T8
Strobe	xx036	T9, T10
Storage Data Valid	xx040	T11, T12

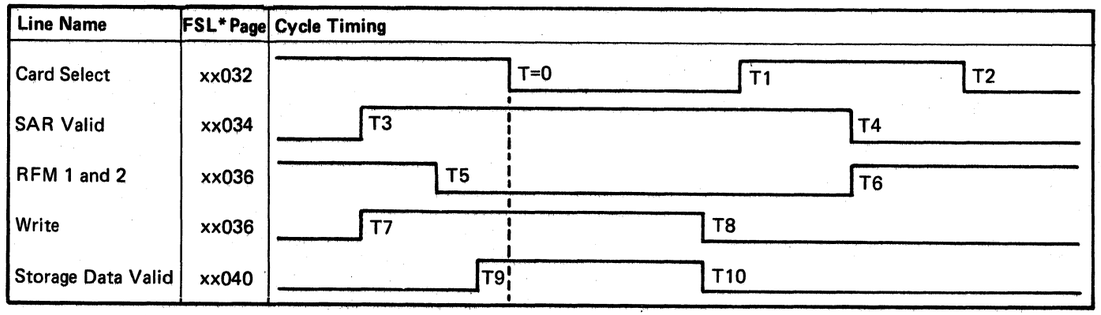
*xx = FB for the MLCA
xx = WC for the work station attachment B

Timing from T=0:

	Minimum	Maximum
T1	+280 ns	+320 ns
T2	+480 ns	
T3	- 35 ns	
T4	+350 ns	
T5	- 35 ns	
T6	+350 ns	
T7	-100 ns	
T8	+350 ns	
T9	- 35 ns	
T10	+320 ns	
T11		+230 ns
T12	+280 ns	

Write Cycle

The sequence for a write operation is shown in the follwing timing chart:



Timings from T=0

	Minimum	Maximum
T1	+180 ns	+220 ns
T2	+380 ns	
T3	-100 ns	
T4	+290 ns	
T5	- 35 ns	
T6	+290 ns	
T7	- 80 ns	
T8	+180 ns	
T9	- 40 ns	
T10	+180 ns	

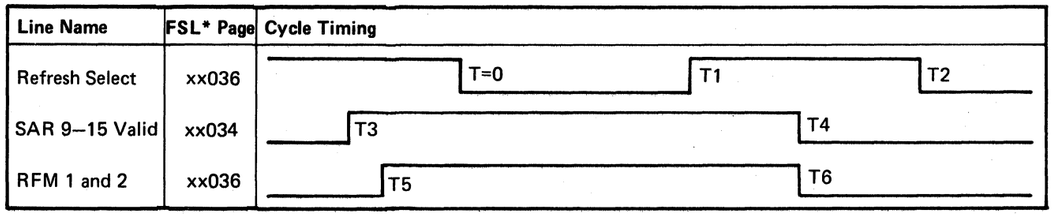
*xx = FB for the MLCA
xx = WC for the work station attachment B

Refresh Cycles

The attachment processor controls the refresh cycles needed by the storage card. The refresh cycles occur at a rate of 128 cycles per 2-millisecond period. The addresses in storage that are being refreshed are supplied by SAR bits 9 through 15. Other conditions needed for the refresh cycles are:

- RFM 1 and 2 not active
- Strobe not active
- Read active

The sequence for a refresh cycle is shown in the following timing chart:



Timing from T=0

	Minimum	Maximum
T1	+180 ns	+220 ns
T2	+380 ns	
T3	- 35 ns	
T4	+280 ns	
T5	-100 ns	
T6	+280 ns	

Adjusting Storage Size

Two pins on the data flow card adjust the attachment processor for the amount of storage needed for the work station or the MLCA. The adjustment is made by either grounding a pin or leaving the pin an open circuit.

Purpose	Maximum Storage	Open Circuit or Ground Pin Number and Location Pin 1 (D05)	Pin 2 (D02)
MLCA	16K (32 KB)	Open	Open
Work Station	32K (64 KB)	Open	Ground

If the processor attempts to address a location in storage that has an address larger than the maximum address as selected by the pins, the attachment processor indicates an invalid address check.

ERROR CONDITIONS

This section covers the following error conditions in the attachment controller:

- DBO parity errors
- Attachment processor channel errors
- Attachment processor errors
- Blast conditions

DBO Parity Checks

The processor-to-processor interface checks the parity of information passing through the DBO on the control processor channel and also the information passing through the I/O DBO on the attachment processor channel. Wrong (even) parity on the control processor channel causes bit 5 of the CBI to be active at strobe time. Wrong (even) parity on the attachment processor channel causes bit 5 of the I/O CBI to be active.

Checks on the Attachment Processor Channel

When the channel senses an error, it sets a bit in the channel check register and activates the 'channel check' line to the attachment processor. When an error is sensed, the channel register stores the address of the I/O attachment or the processor-to-processor interface in the last command executed by the channel.

The errors the channel can sense and the bits turned on in the channel error byte are shown in the following table:

Channel Error Byte

Bit	Error	Cause
0	Data bus out parity check	An atachment sensed wrong parity on the DBO bus.
1	Invalid device address	The channel put an address on the DBO bus, but no response came from the attachment in the specified time. (The channel activated the 'control out' line to address an attachment and the attachment did not respond by activating the 'service in' line on or before the seventh strobe pulse.)
2	Data bus in parity check	The channel sensed wrong parity while receiving data from an I/O attachment or the processor-to-processor interface.
3	I/O time-out check	The channel sensed an error in a normal channel sequence. This check occurs if an attachment does not de-activate the 'service in' line on or before the seventh strobe pulse after the 'service out' line becomes active.
4	Not used	
5	System bus out parity check	Wrong parity was sensed in the data sent from the attachment processor to the channel. (This includes data from storage during a cycle steal.)
6	Cycle steal operation check	Signals that a processor or channel check occured during a cycle steal operation.
7	Not used	

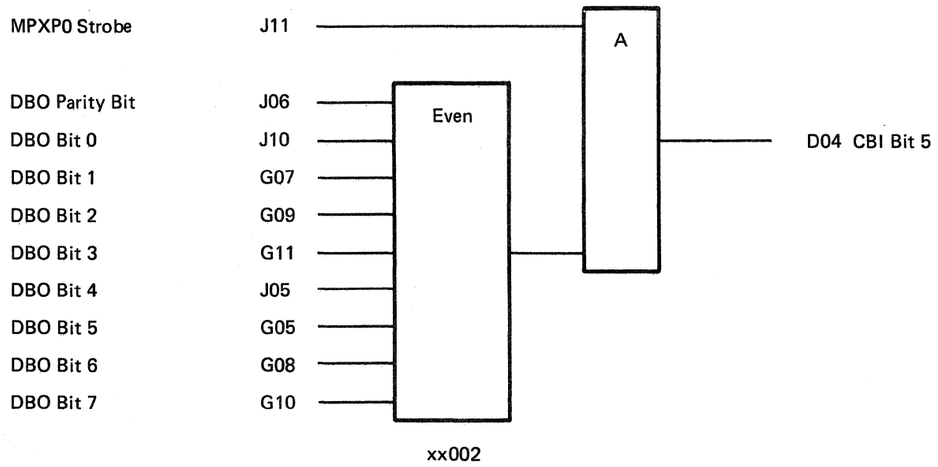
Blast Conditions

Either one of two checks causes a blast condition to occur. These checks are:

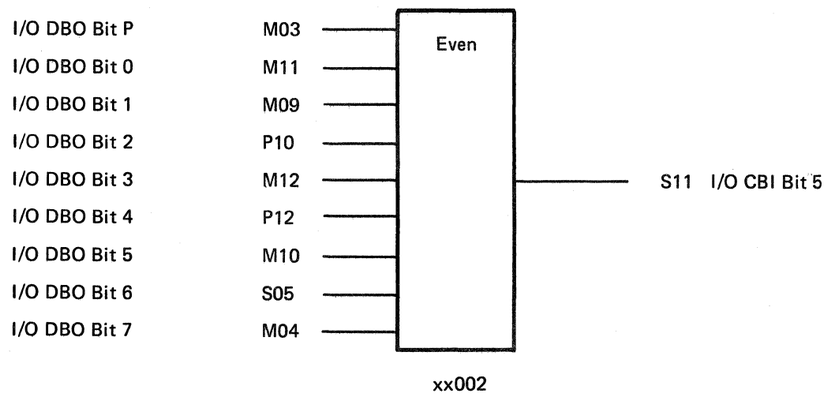
- Time-out check
- Invalid device address check

The blast condition resets all the I/O devices by activating the 'control out' line and the 'service out' line at the same time. The blast condition remains active until the processor starts to execute the next instruction.

Parity Check on the Control Processor Channel



Parity Check on the Attachment Processor Channel



xx = FB for the MLCA
xx = WC for the work station attachment B

Attachment Processor Checks

A hardware error in the attachment processor sets a bit in the processor check register. The checks that the attachment processor can sense are shown in the following table, which shows the contents of the processor check byte.

Bit	Error	Cause
0	Storage data register parity check	Parity in the storage data register is not correct.
1	Microoperation register parity check	Parity in the microoperation register is not correct.
2	Y-register parity check	Parity in the Y-register is not correct.
3	X-register parity check	Parity in the X-register is not correct.
4	Invalid storage address or storage address register parity check	Storage was addressed outside its limits. (See note.)
5	3-second time-out or storage address register parity check	The parity check program remained in a loop for more than 3 seconds. (See note.)
6	Unused	
7	Unused	

Note: Bits 4 and 5 have special meaning when they are combined.

Decode of Bits 4 and 5

Bit 4	Bit 5	Error
0	0	= No check
0	1	= 3-second time-out
1	0	= Invalid address check
1	1	= Storage address register parity check

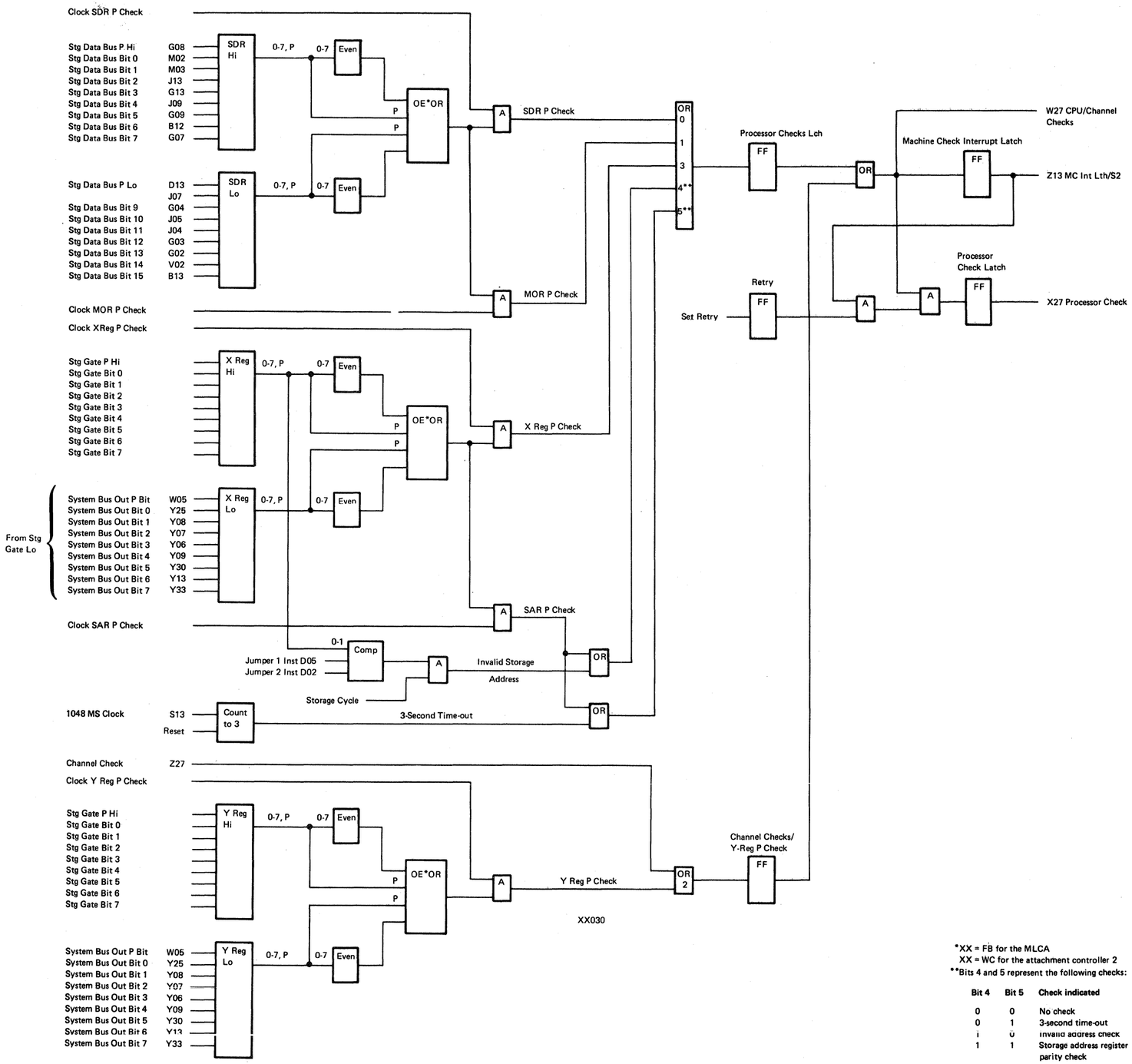
The figure, *Attachment Processor Checks*, shows the logic for generating attachment processor checks similar to an interrupt level 0 (machine check) condition.

The status of the retry latch controls the response of the attachment processor to a machine check. When the retry latch is active, a machine check activates the 'processor check' line, and the processor stops. When the retry latch is reset, a machine check causes the attachment processor to start executing instructions on interrupt level 0 (machine check level). If a second hardware error occurs while the processor is operating on the machine check level, the 'processor check' line is activated and the processor stops immediately.

The output of the processor check latch, the 'processor check' line, is one of of several input lines to interrupt A request register in the processor-to-processor interface. Interrupt A, in sequence, causes an interrupt request to the control processor.

To recover from a processor check, the control processor must perform an IPL.

Attachment Processor Checks

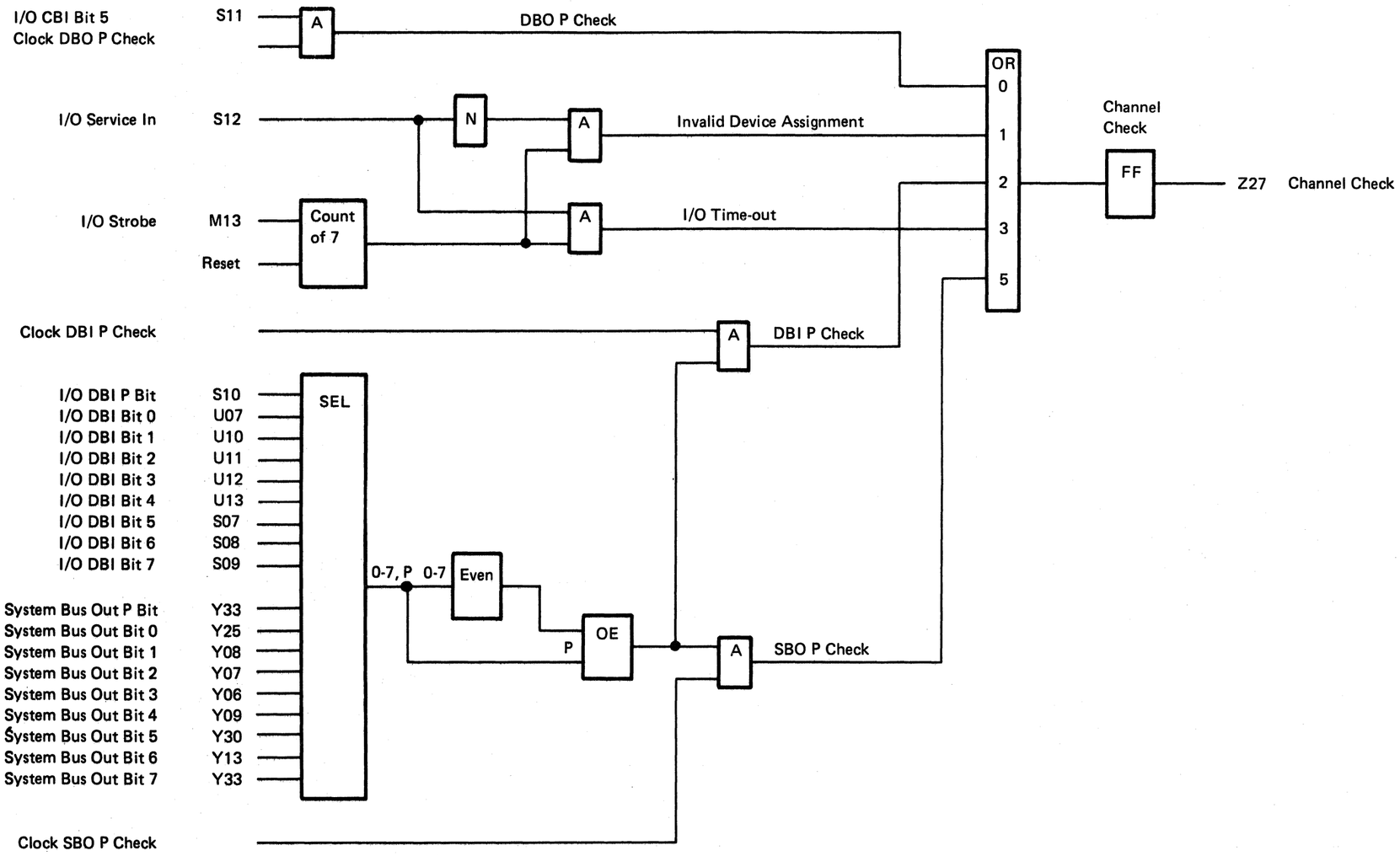


*XX = FB for the MLCA
XX = WC for the attachment controller 2

**Bits 4 and 5 represent the following checks:

Bit 4	Bit 5	Check indicated
0	0	No check
0	1	3-second time-out
1	0	Invalid address check
1	1	Storage address register parity check

Attachment Processor Channel Checks



XX012

*XX = FB for the MLCA
XX = WC for work station attachment B

Note: Channel check bits 4 and 7 are unused. Channel check bit 6 (cycle steal operation check) does not set the channel check latch but is set in the channel check register when either a channel check or a processor check occurs during a cycle steal operation.

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