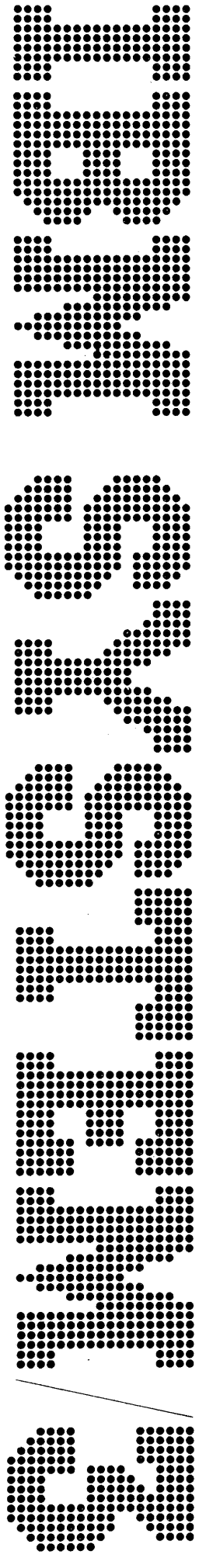

IBM System / 3
Serial Input / Output Channel
Original Equipment
Manufacturers Information

This publication provides information for designers and manufacturers who intend to connect their input/output equipment to the IBM System/3 Serial Input/Output Channel (SIOC). The functions of the interface lines and their electrical and timing requirements, as well as the signal sequences and the required response sequences, are described in detail. Programming information is also given to show the interaction between channel commands and device responses.

First Edition (March 1971)

Changes are continually made to the specifications herein; any such change will be reported in subsequent versions or Technical Newsletters. IBM reserves the right to make performance and specification changes at any time. Information contained herein is current as of March 1971.

A Reader's Comment Form is provided at the back of this publication. If the form has been removed, comments may be addressed to IBM Corporation, Product Publications, Department 245, Rochester, Minnesota 55901.

Preface

The IBM System/3 Serial Input/Output Channel (SIOC) communicates with its attached devices via a number of specific signal sequences. The SIOC, in turn, expects similar sequences. Designers, engineers, and other engineering people who wish to connect non-IBM devices to this channel must, therefore, design an electronic attachment (termed "control unit", or "I/O device" in this manual) that can decode the channel signal sequences and respond accordingly. IBM responsibilities to such an attachment are defined in the *IBM Multiple Supplier Bulletin,* 120-6648. The information in this publication can help engineers design a control unit that will act as a standard interface for the System/3 SIOC.

The signal sequences are described in detail and recommendations are given when the designer has a choice of several responses and/or sequencing methods. Programming aspects are covered only to the extent necessary for understanding the interaction between program and addressed device.

The material is so arranged that the reader is led from the initiation of a data transfer operation to its termination; cross references to exceptions are given so that deviation from the general guiding principles is avoided. It is assumed that the reader is familiar with the terminology commonly used in logic design.

For further information on System/3 refer to the *IBM System/3 Bibliography,* GC20-8080, and the *IBM Field Engineering Maintenance Diagrams,* SY31-0275.

Contents

ANSCII	American National Standard Code for Information Interchange
APL	Advance Program Level
BCD	Binary Coded Decimal
CPU	Processing Unit
DBO	Data Bus Out
DTR	Data Transfer Register
EBCDIC	Extended Binary Coded Decimal Interchange Code
EOT	End of Transmission
EPO	Emergency Power Off
I/O	Input/Output
LCR	Length Count Register
LIO	Load Input/Output
LSR	Local Store Register
SIO	Start Input/Output
SIOC	Serial Input/Output Channel
SNS	Sense Input/Output
TIO	Test Input/Output

SYSTEM/3 SERIAL INPUT/OUTPUT CHANNEL (SIOC)

The flexibility of a data processing system is determined mainly by the number of different input/output (I/O) devices that can be attached to it. The SIOC gives System/3 this desired flexibility by permitting any number of different I/O devices to be attached to System/3. It's all made possible by a serial I/O channel concept.

The SIOC is an electronic unit that directs the flow of information, as specified by a stored program, between the connected input/output devices and the processor main storage. This same stored program specifies the channel activity by using standard instructions that are common to all channel-connected devices. The SIOC decodes these instructions and places them on a common bus as a series of signal sequences. The addressed device responds with a signal sequence that tells the program whether the issued instruction can be executed and, if not, why it can't be executed. When an instruction is accepted, the device is logically connected on the interface and data transfer then begins. The data transfer is controlled by the device and the channel and the processor main storage by means of interlocked requests and responses.

The relative freedom of the SIOC from the design peculiarities of an attached device is obtained by the standardized instructions and responses, that is, by the signal sequences the SIOC sends out and expects to receive. In other words, all SIOC attached devices "understand" these sequences and must be able to respond similarly.

Thus, input/output devices that are intended to operate on System/3 SIOC must work through a control unit that decodes the channel sequences and, conversely, encodes the device responses. This control unit may be housed within the device, or it may be designed as a separate unit to be shared by any number of individual I/O devices. Only one control unit can be physically attached to the SIOC at a time, but any number of devices can be attached to the control unit. Only one device may operate at a time, but all devices may be controlled with a common program. In this manual, any device, be it I/O device or control unit, is referred to as the attached I/O device.

PHYSICAL DESCRIPTION

The SIOC uses MST-1 logic circuitry located in the System/3 Processing Unit (CPU), and allows communication between the CPU and an attached I/O device at the maximum rate of 50,000 characters per second. The electronics of the attached I/O device must be designed to be compatible with the SIOC. One 192 pin connector, connects the interface signals (control, sense, and data) between the SIOC and the attached I/O device. The (SIOC) 192 pin connector is connector A, while the mating attached device 192 pin connector (on the I/O cable) is connector B (Figure 1-1).

There are cross-connections (I/O identification jumpers) within the attaching connector which provide for program I/O identification of the attached device. See Figure 1-2 for 'I/O identification Jumper' information.

Each device attached to the SIOC must have its own cable and connector, and its own power supply. The circuitry at the attached device interface must be compatible with the SIOC.

A SIOC indicator on the CPU console turns on when the I/O device attached to the SIOC requires attention.

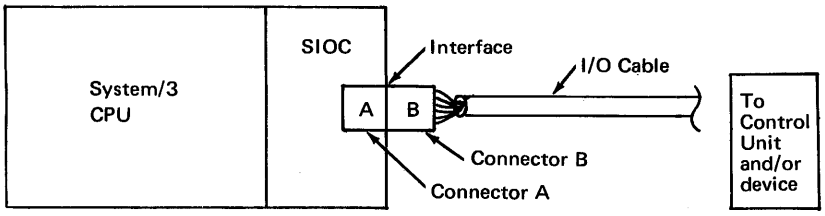

Figure 1-1. SIOC and Cable and Attached I/O Device

PROGRAMMING CONSIDERATIONS

Instructions

Information transfer between the SIOC and the I/O device is controlled by five instructions which are issued by the processing unit (CPU). These instructions are:

Test I/O (TIO)–Advance Program Level (APL)

The TIO and APL instructions test for SIOC not ready or SIOC busy.

Load I/O (LIO)

The LIO instruction sends control information from the CPU to the SIOC. The control information prepares the SIOC for read or write data transfer.

Sense I/O (SNS)

The SNS instruction brings control, sense, diagnostic, and status information from the SIOC and the I/O device to the CPU.

Start I/O (SIO)

The SIO instruction is sent to the SIOC to set up SIOC controls. The SIO signals the SIOC to set or reset interrupts and interrupt requests, and remove the SIOC from the busy state. An SIO also initiates reading from or writing to the attached device.

Cycle Controls

These controls are activated by either an SIO read or an SIO write instruction and provide the necessary controls to transfer data between the I/O device and CPU storage. The SIOC must be in one of these modes to honor any service requests from the attached device.

In the read mode, a service request results in one data byte being transferred to the SIOC data transfer register from the device. When this is completed, the SIOC issues a service response signal indicating to the I/O device that the data has been accepted and that the status of the input data lines can be changed. After emitting the service response signal, the SIOC circuitry requests a CPU I/O cycle. When it's granted, the contents of the data transfer register are transmitted to a storage location determined by the address contained in the SIOC LSR (local storage register). This LSR is located in the CPU. It may take up to 20 microseconds for the I/O cycle to be granted.

After the transfer is completed, the SIOC circuitry updates the contents of the SIOC LSR. It is either incremented or decremented by "1". This is controlled by the I/O function register and is determined by the order in which the I/O device transfers data. The SIOC continues accepting and transferring data in this manner until an end of transfer signal is received from the I/O device or an overflow from the SIOC LCR (length count register) occurs. This stops the transfer of data and the SIOC is removed from the busy state. A write mode cycle steal is similarly initiated by service request. In this mode of operation, data is also retrieved from CPU storage by priority request–cycle steal through the DBO register. The data (a single byte) is inserted into the SIOC data transfer register and a service response is issued to the I/O device. This response indicates that data, as a result of the current service request, is available. Depending on the activity of other devices operating with the CPU, the service response may be activated between 6 to 20 microseconds after the service request was received. Service requests are honored until the I/O device transmits an EOT (End of Transmission) signal or until a LCR zero (overflow) occurs. When the latter condition exists, the transfer of data stops and the SIOC is removed from the busy state.

I/O Function Register

This register has 16 bits and is loaded by an LIO instruction. The pattern loaded is defined by the attached I/O device and must be loaded prior to executing the program associated with the device.

Length Count Register (LCR)

The LCR is loaded by an LIO instruction with a number equal to 256 minus the number of desired bytes transferred by I/O cycle stealing during a read operation or a write operation. Thus the LCR limits the maximum number of bytes transferred per record to 256. As each cycle steal is taken, the LCR is stepped once. When the LCR equals zero (LCR overflow), the read or write operation stops.

The contents of the LCR can be stored in core for testing purposes, with an SNS instruction. An overflow from the LCR is stored in the length count equals zero latch and can be sensed by an SNS instruction.

I/O Select Register

This register issues one to sixteen separate I/O device control signals. The register is loaded by an SIO instruction and its contents are transmitted to the I/O device via the unit 1, unit 2, or one of 14 I/O select lines. Signals on these lines exists for approximately 6 microseconds. If required by the I/O device, 'I/O select 1' can be latched up. In this situation the I/O device resets this latch with 'I/O transfer line 2'.

The function of these select lines is determined by how they are used or not used in the device.

I/O Transfer Line Latches

Eleven I/O transfer lines communicate various I/O conditions from the device to the SIOC and the CPU, as assigned and defined by the I/O device.

The logical conditions existing on the lines are stored in CPU storage with an SNS instruction and can be tested with TBN and TBF instructions. If the 'I/O transfer line 1' is active when tested, a 6 microsecond reset transmission error signal is issued to the I/O device. This signal can be used in the device to reset error conditions.

Setting the assigned bits in the I/O function register, allows latching of pulses which occur on specified I/O transfer lines. I/O transfer lines 1 and 2 can also be selected by the I/O function register to generate an end of transfer signal. This signal renders the SIOC not busy and generates the I/O disconnect signal. Flexibility in using these signal lines is provided because of the differing requirements of the devices to be attached. The manner in which these signal lines are used is determined by the individual I/O devices.

Data Transfer Register

The 9 position data transfer register (DTR) stores one byte of data (8 bits plus parity). This byte is transferred from the I/O device to the CPU core storage during a read operation, and from the CPU core storage to the I/O device during a write operation. Data transfer is normally accomplished by cycle steal but the ability to load and store the DTR with LIO and SNS instructions is provided.

The LIO instruction can be used, if required, by an attaching I/O device to make the first data byte available in the data transfer register before issuing an SIO write instruction. The SNS transfer register instruction is provided for diagnostic testing and is not used for normal data transfer.

The DTR operates in even or odd parity mode as required by the attached I/O device. The DTR mode is controlled by the I/O function register, byte 2, bit 4. An error causes a data transfer parity check.

The parity check circuit checks this register for odd or even parity. The I/O function register determines whether odd parity or even parity causes a data transfer parity check.

Interrupt Request

The CPU program can be interrupted by the SIOC so that I/O devices requiring the CPU to process transferred data can select certain time dependent I/O functions, such as, stacker selection in a reader sorter. The EOT or length count overflow signals, which remove the SIOC from the busy state, set the interrupt pending condition within the SIOC. This condition can also be set by the SIO instruction. If the interrupt enable latch is set, the SIOC initiates an interrupt request; otherwise, the interrupt pending condition is stored within the SIOC. This condition can be sensed by the SNS instruction. The interrupt request can be set by issuing an enable interrupt SIO instruction while the interrupt pending status exists. The SIOC interrupt routine is entered immediately upon request. Delays in this routine occur only when the I/O devices request I/O cycles.

SIOC INTERFACE

This section describes the I/O interface lines. For a description of how they are used to perform control, sense, and data transfer, see *Interface Signal Sequences*. The I/O interface has two types of lines: output lines (from the SIOC to device) and input lines (from the device to SIOC). Figure 1-2 identifies these lines and describes their use.

Interface lines from Device to the SIOC	Connector contact number	Use
I/O Transfer 1 I/O Transfer 2 I/O Transfer 3 I/O Transfer 4 I/O Transfer 5 I/O Transfer 6 I/O Transfer 7 I/O Transfer 8 I/O Transfer 9 I/O Transfer 10 I/O Transfer 11	R02 R03 R04 R05 R06 R07 R08 R09 R10 R11 A11	These 11 lines from the device to the SIOC can be tested by the CPU program. These lines can indicate any type of I/O status required by the I/O device.
I/O Ready	D02	This line from the device to the SIOC indicates when a I/O select attachment signal and either a read or write call has been accepted by the device. Activity on this line can be sampled by the CPU to indicate that the I/O device has responded and is ready to transfer data. If the I/O unit does not respond, the SIOC can be removed from the busy state with an SIO (CPU instruction).
I/O Attention	D03	This line active turns on the system I/O attention indicator and the SIOC indicator in the CPU when the SIOC is addressed. When this condition exists, the SIOC appears not ready and does not accept read or write instructions until the operator intervenes.
I/O Identification 1 Jumper I/O Identification 2 Jumper I/O Identification 4 Jumper I/O Identification 8 Jumper	E02 E03 E04 E05	These four lines from the device to the SIOC are activated by jumpers in the device half of the 192 pin connector. The jumpers provide program identification of the attached device (one of 16 possiblilites).
Device Attached Jumper	E06	This line from the device to the SIOC is a jumper from pins E06 to F06 in the device half of the 192 pin connector. This jumper allows the CPU program to test whether or not an I/O device is attached.
CPU Reset Jumper	E07	This line from the device to the SIOC is a jumper in the device half of the 192 pin connector. When this jumper is connected from E07 to F07 this line is at a negative 'C' level while active. When this jumper is omitted, this line is at a positive 'C' level while active.
I/O Input 7 I/O Input 6 I/O Input 5 I/O Input 4 I/O Input 3 I/O Input 2 I/O Input 1 I/O Input 0 I/O Input P	H05 H06 H07 H08 H09 H10 H11 H12 H13	These 9 lines from the device to the SIOC carry the 8 data bits and a check bit. To be effective these lines must be active when service request is issued and remain active until service response is received.
End of Transmission	J04	This line indicates to the SIOC that the last character has been transmitted or received by the attached device. This signal removes the SIOC from the busy state; subsequent data transfers must be initiated by another SIO (CPU instruction). This signal can also be used to set the SIOC interrupt request latch under control of the I/O function register.

Figure 1-2. (Part 1 of 4). I/O Interface Lines

Interface Lines from Device to the SIOC	Connector contact number	Use
Single Character Transfer	J05	If only a single character is transmitted, the single character transfer line can be used to remove the SIOC from the busy condition after the transfer is complete. This line must be made active at the same time service request is active. During a read operation the SIOC is set to the not busy state after the service response is issued. During a write operation the first data byte is present on the data output lines at the time write call is active; therefore activity on the single character transfer line indicates that this byte has been received and the SIOC is set to the not busy condition.
Service Request	J06	This line indicates to the SIOC that the I/O unit is ready to receive or transmit a byte. This line remains active for at least 2 microseconds or until a service response is received.
I/O Selecting Unit	J07	This line must be active when the I/O device is sending or receiving data. When no signal is present on this line, the service request latch in the SIOC is held reset and cannot respond to a service request.

Interface Lines from the SIOC to the Device	Connector pin number	Use
I/O Output P I/O Output 0 I/O Output 1 I/O Output 2 I/O Output 3 I/O Output 4 I/O Output 5 I/O Output 6 I/O Output 7	A10 A02 A03 A04 A05 A06 A07 A08 A09	These 9 data lines from the SIOC to the device carry the 8 data bits and a check bit. Data gated on these lines, as a result of a service request from the I/O device, is valid for 4 microseconds, before the setting of service response in the SIOC. This information remains on these lines until the next service request is received.
I/O Attach Read Call	D04	This line indicates the SIOC is in the read mode and also indicates to the I/O device that the SIOC is either ready to receive data, or is in the process of receiving data. This line remains active until reset by either an end of transfer signal or an overflow (length count =0) in the SIOC length count register.
I/O Write Call	D05	This line indicates to the I/O device that the SIOC is active because of an SIO instruction, and either is ready to write data or is in the process of writing data. This line remains active until reset by either an end of transfer signal or by a service request that follows an SIOC length count register overflow (length count = 0).
Select I/O Attach	D06	This line indicates that the SIOC is in either a read or write mode. It is set by either a CPU read or write SIO (start I/O) instruction and remains active until reset by either an EOT or a length count register overflow (length count = 0). This line is also active for about 6 microseconds when either a unit 1 or unit 2 control signal is issued.
Service Response	D07	This line indicates to the I/O device that the data being transferred has been either accepted or is available on the I/O output lines during either a read operation or a write operation. This signal can be reset with the leading edge of the service request signal or approximately 6 microseconds after service request has dropped as determined by programming of the I/O function register.

Figure 1-2. (Part 2 of 4). I/O Interface Lines

Interface Lines from the SIOC to the Device	Connector contact number	Use
Reset Transfer Error	D08	This line is active for about 6 microseconds if the I/O transfer 1 condition exists when an SNS transfer line instruction is executed.
Process Meter	D09	This line indicates the CPU use meter is running and can be used by the I/O device to condition its use meter.
Process Check	D10	This line indicates either a parity check condition occurred in the SIOC or a CPU check stop exists. If a CPU check stop activates this signal, a system reset is required to restart. An SIO (CPU instruction) can be used to deactivate this line if it is activated by a parity error detected in the SIOC adapter.
CPU Is Stopped	D11	This line active indicates the CPU processor clock is stopped because of either a processor check or an I/O check. A system reset is required to remove this active condition. This signal is also made active whenever the I/O channel processor run signal is inactive.
I/O CPU Reset	E08	This line has either a plus or minus level during power on reset when the program load key on the CPU operator console, or the system reset key on the CPU CE console is pressed. The polarity of this signal is determined by jumpering in the 192 pin connector.
CPU Emergency Off Switch In CPU Emergency Off Switch Out	E09 F09	These lines are connected in the CPU through the Emergency Power Off (EPO) switch. If the EPO switch is pulled, the connection opens. The I/O device uses these lines to connect into their power control circuits. This enables the EPO switch, if pulled, to drop power on the CPU, SIOC, and I/O device.
I/O Disconnect	J08	This line indicates either the end of transfer or length count overflow (length count = 0) wants to disconnect the SIOC from the device. This signals the I/O device that the transfer of data has ended and will not be resumed until the SIOC has been reactivated with an SIO (CPU start I/O instruction). This is controlled by the I/O function register. The I/O function register (slave bit) also permits the I/O device to control the I/O disconnect signal. In this situation, activity on I/O transfer lines 3, 4, 6, or 7 conditions the I/O disconnect signal. The I/O disconnect signal can be reset by I/O transfer line 3 or 5 from the I/O device, or it can exist for a duration of about 6 microseconds.
Unit 1 Control Unit 2 Control I/O 14 Select I/O 13 Select I/O 12 Select I/O 11 Select I/O 10 Select I/O 9 Select I/O 8 Select I/O 7 Select I/O 6 Select I/O 5 Select I/O 4 Select I/O 3 Select I/O 2 Select I/O 1 Select	H04 T04 T05 T06 T07 T08 T09 T10 T11 T12 T13 J09 J10 J11 J12 J13	These 16 I/O select lines control functions in the I/O devices. These lines are active for about 6 microseconds when selected. When selected, I/O select 1 can be latched up by the I/O function register. I/O transfer line 2 is then used to reset this latch.

Figure 1-2. (Part 3 of 4). I/O Interface Lines

Grounds	Connector Ground Contact Number
Ground 1	C02 through C11 and B02 through B11
Ground 2	S02 through S11 and F02 through F08
Ground 3	K04 through K13 and G04 through G13
Ground 4	X04 through X13

Figure 1-2. (Part 4 of 4). I/O Interface Lines

INTERFACE SIGNAL SEQUENCES

All activity on the SIOC is started, continued, and ended by interface signal sequences. The attached device must be able to understand the signal sequences from the SIOC; the attached device must also respond to the SIOC with acceptable sequences. This section describes the interlocking of these interface signal sequences, which cause either a read operation from the attached device to the SIOC, or a write operation from the SIOC to the attached device. Figure 2-1 and 2-2 used together show the interface signal sequences.

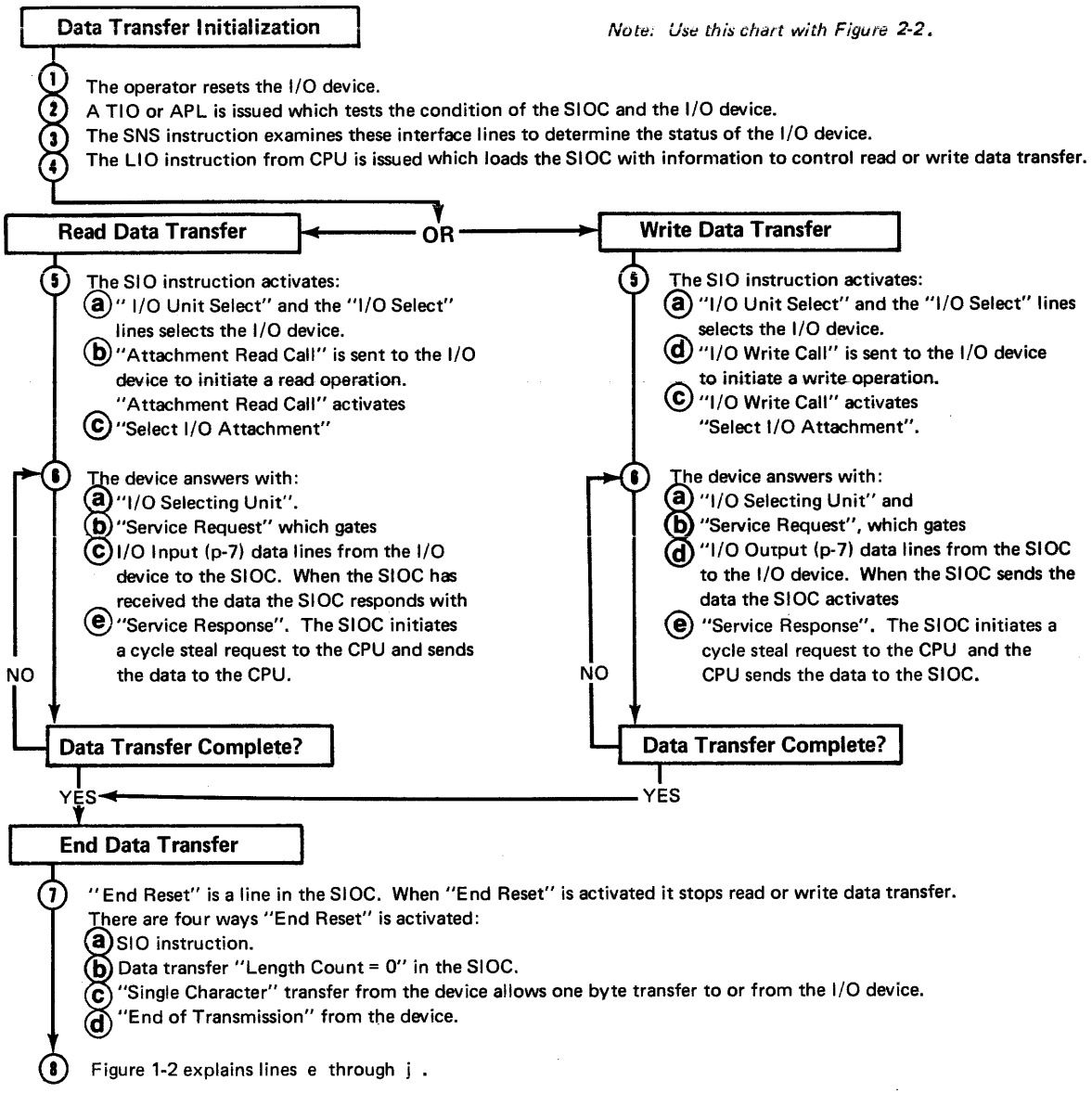

Figure 2-1. Interface Signal Sequence (flowchart)

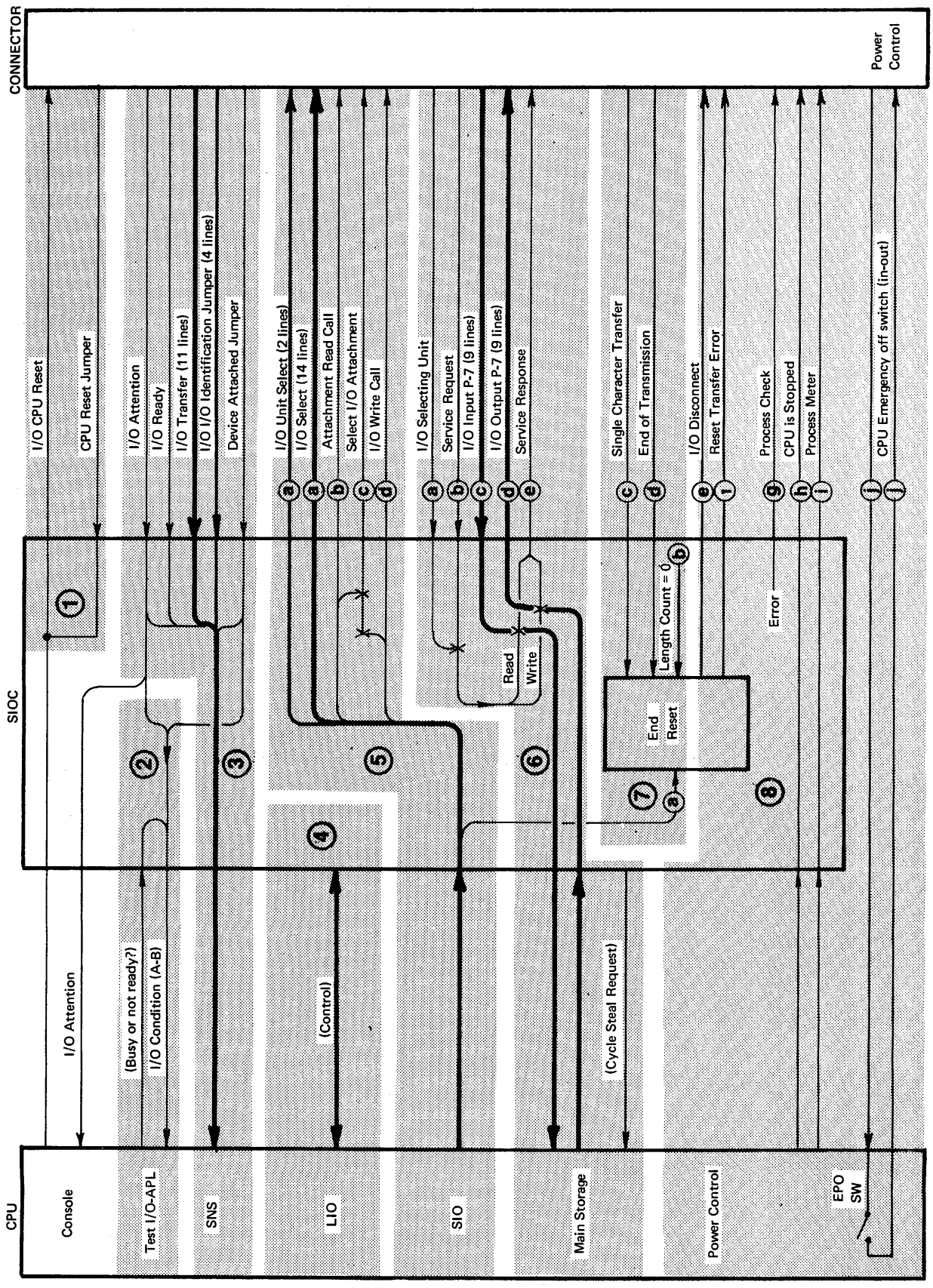

Figure 2-2. Interface Signal Sequence (sequence chart)

Data Lines

The basic unit of information in the System/3 and the SIOC is the data byte. Each data byte has 8 bits (two hexadecimal characters). The 'I/O Output' (P-7) interface lines carry a data byte from the SIOC to the attached I/O device. The 'I/O Input' (P-7) interface lines carry a data byte from the attached I/O device to the SIOC. The information on each group of lines is organized in such a manner that line 7 carries the low-order or lowest binary value bit (as shown in Figure 2-3), line 0 carries the high-order or highest binary value bit, and line P carries the parity bit. The information on each group of lines can also be EBCDIC (Extended Binary Coded Decimal Interchange Code), BCD (Binary Coded Decimal) or ANSCII (American National Standard Code for Information Interchange) as shown in Figure 2-3. These three different codes can be translated by System/3 programming when used by the SIOC and attached I/O device.

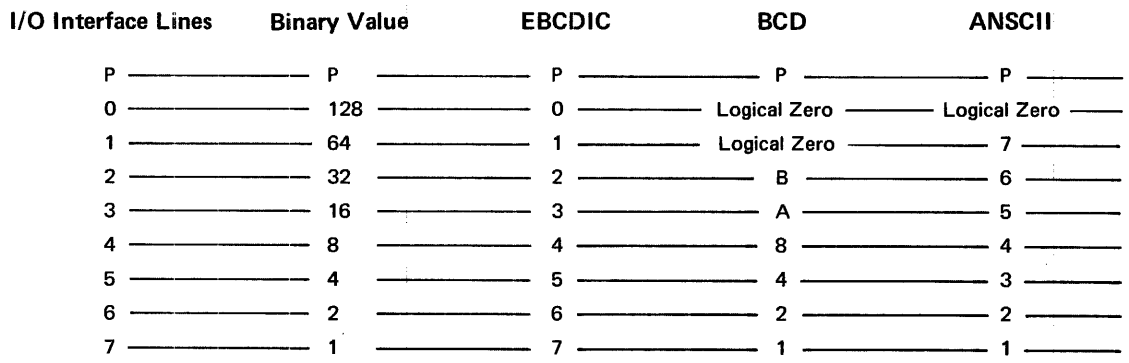

Figure 2-3. Organization of Data on the I/O Interface Lines

INTERFACE LINE DRIVERS

The driver requires an MST input, and gives a "C" level output, and is designed to drive a coax line up to 100 feet long. The coax line must have a characteristic impedance between 90 and 100 ohms. The maximum line resistance that can be driven is 33 ohms, which includes all contact resistance and all external and internal cable resistance. The output line is inactive when driver power is off. The signal output from the driver may be grounded without damage to the driver. Figure 3-1 shows driver characteristics.

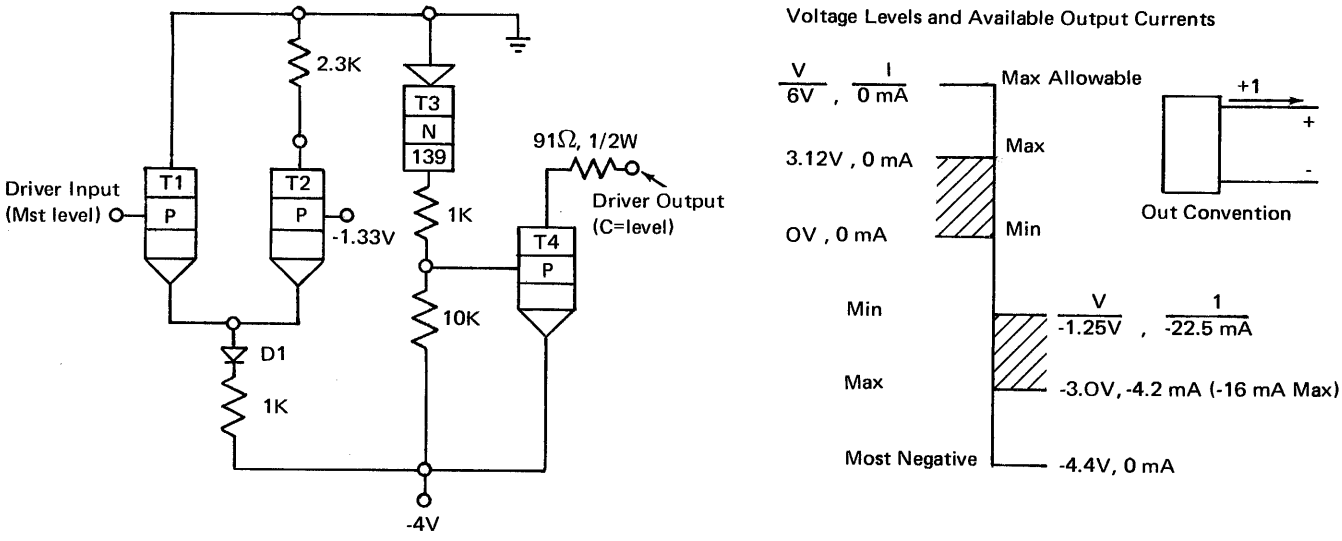

Figure 3-1. Interface Line Driver

INTERFACE LINE RECEIVERS

The receiver accepts a "C" level input, and gives an MST output, and is designed for use with lines which have a characteristic impedance between 90 and 100 ohms. The signal input to the receiver may be grounded without damage to the receiver. Figure 3-2 shows receiver characteristics.

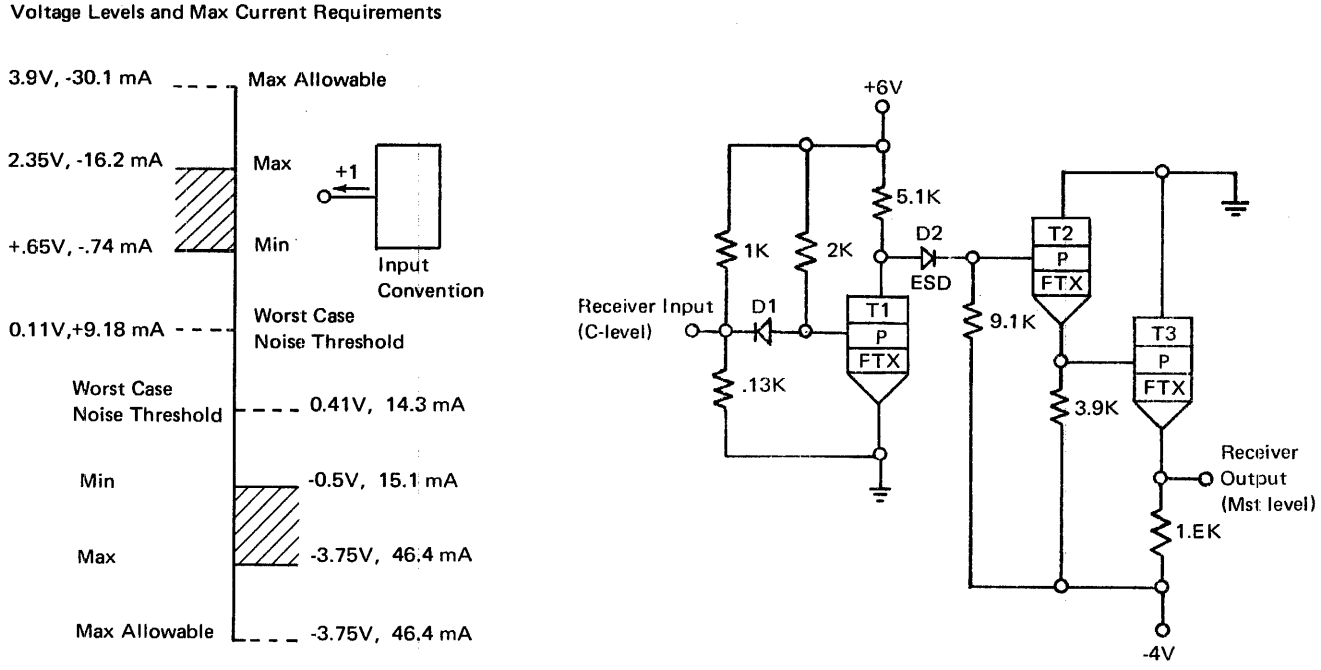

Figure 3-2. Interface Line Receiver

INTERFACE CONNECTORS

Two styles of connector are used to connect the SIOC to the attached device: A-style and B-style (Figure 3-3). The styles pertain to the connector mating. Electrically the same, they are equipped with identical serpent contacts, but are mirror images of each other and match only in one position.

The connectors are identified by the color of their half-sockets; A-style is light gray and B-style is black. A proper match is achieved only between connectors of different color (A to B, B to A). The connector on the CPU is light gray, therefore the connector of the attaching cable must be black. Cables can be coupled to temporarily bypass a unit. Figure 3-3 shows serpent contact numbering. All signal leads are accompanied by a ground lead to which the cable shield (for the coaxial cables) or ground wire (for flat cables or twisted pairs) is connected. Figure 3-4 shows the details and parts number of the SIOC device cable assembly.

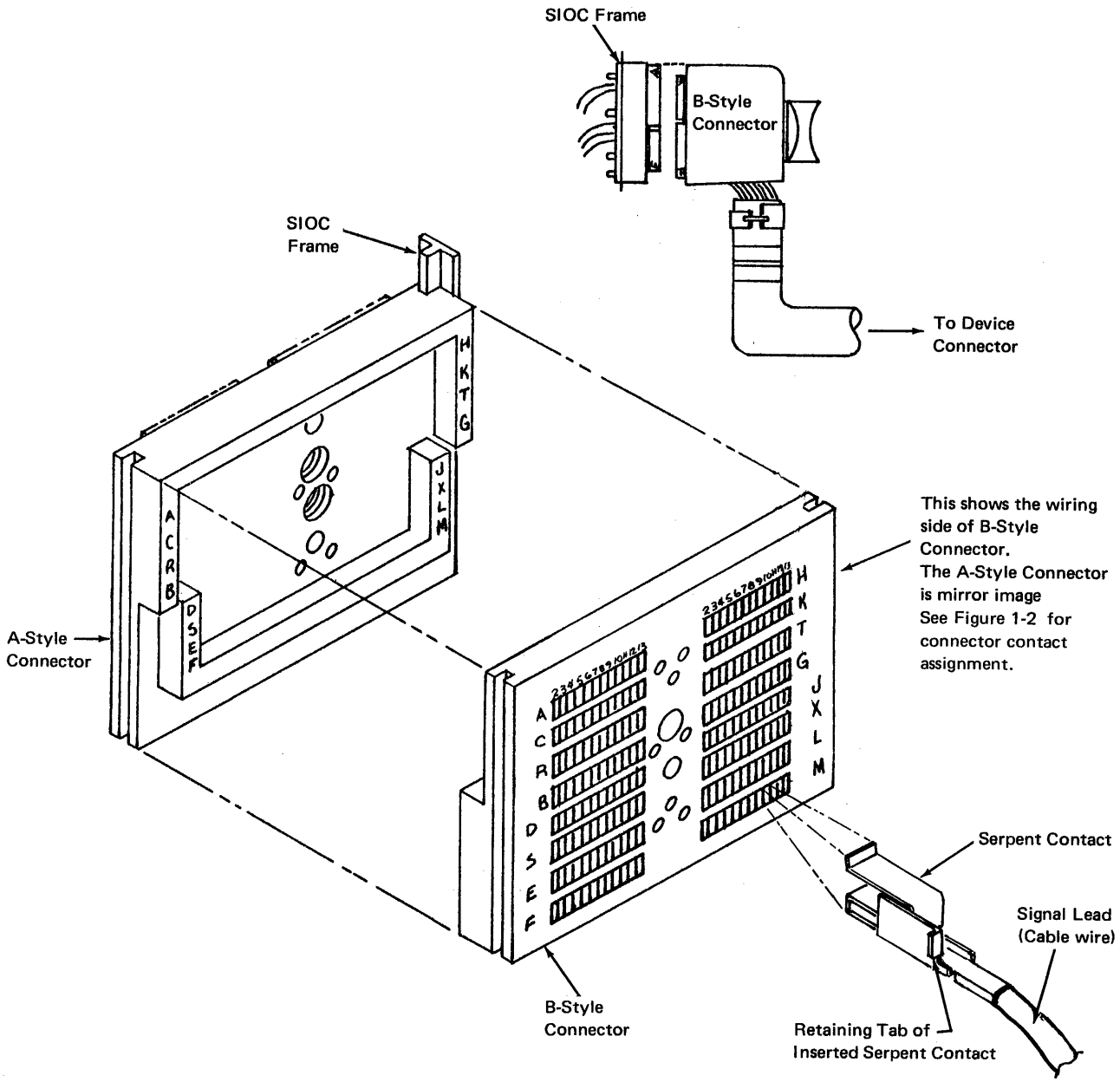

Figure 3-3. SIOC Connectors

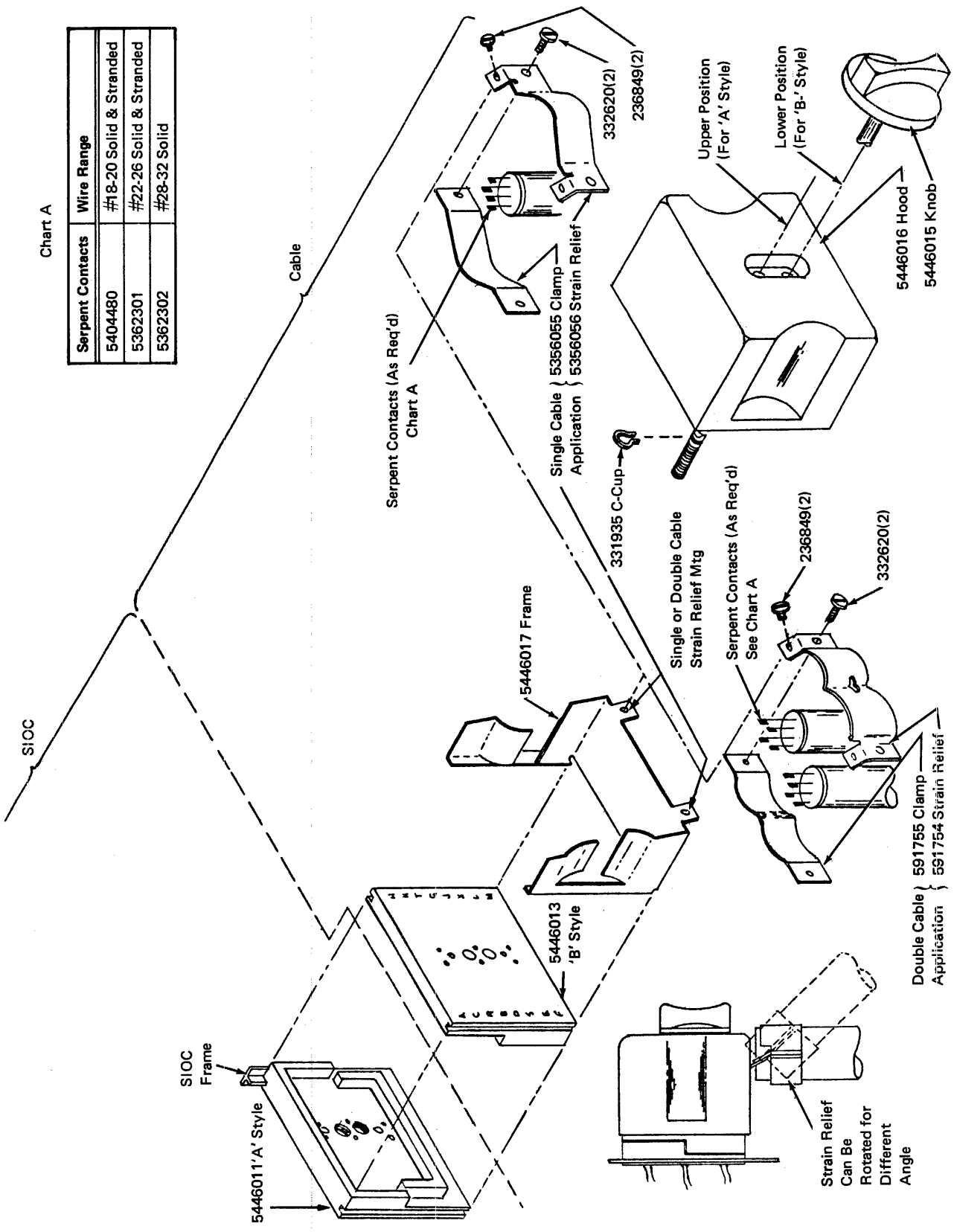

Figure 3-4. SIOC to Device Interface Cable Assembly Details

Assembling Connector Cable-half

1. The serpent contacts (Figure 3-5) should be crimped on the leads first, then the hood should be slipped over the cable.

2. After the hood is on, the contacts can be inserted into the mating socket from the rear. Each contact must be correctly located, both physically and electrically, before it is pushed into the opening.

   a. Physical location: The guide edge of the contact must slide into the guide groove of the mating socket housing; the retaining tab will then be diagonally opposite the groove. Push the contact to latch into place.

   b. Electrical location: The letter of the row and the number of the column (row A column 2, row A column 3, row A column 4) for each line must connect to the corresponding line in the SIOC connector. See Figure 1-2 for connector contact assignment.

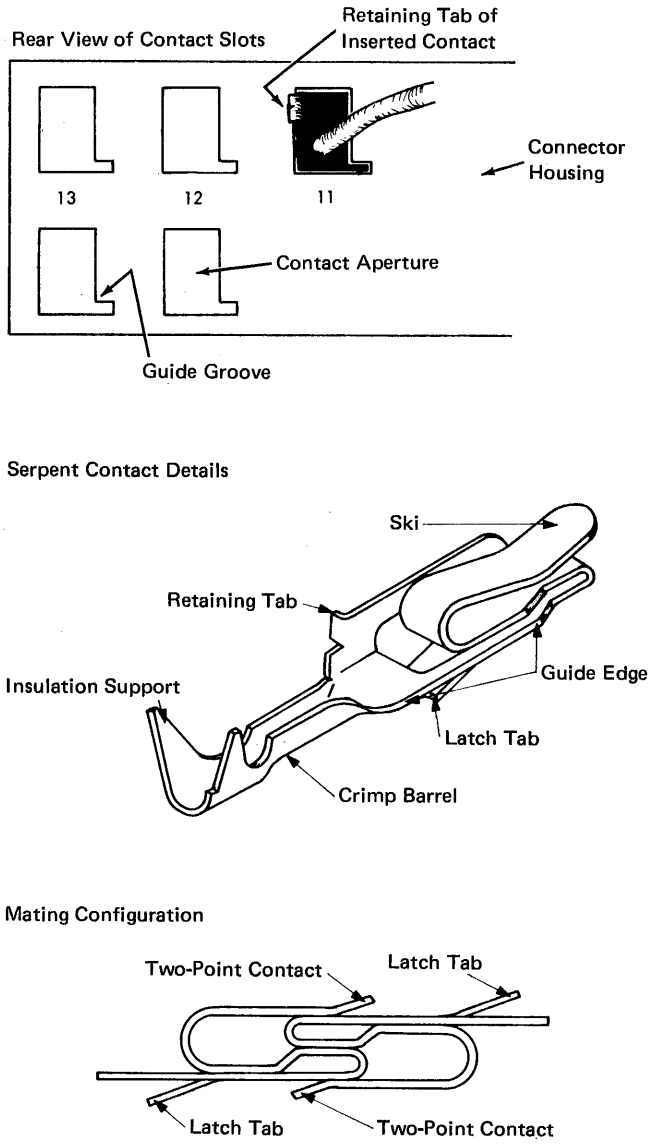

Figure 3-5. Serpent Contact Details

Serpent Contact Resistance

The serpent contacts are made of phosphor-bronze and are gold-plated. The contact-to-contact resistance, including two crimps and mated contacts, will not exceed the resistance shown in Figure 3-6.

The contacts are not designed for current interruption; however, a maximum current of 6 amperes can be sustained.

Resistance	Serpent Contact Wire Size
0.020 ohm	AWG 22 (0,325 mm^2) and thicker
0.030 ohm	AWG 24 to 26 (0,205 to 0,128 mm^2)
0.040 ohm	AWG 28 to 30 (0,080 to 0,051 mm^2)

Figure 3-6. Serpent Contact Resistance

Serpent Contacts (Crimp-Barrel Size)

These contacts are used in both the A-style connector and the B-style connector. The contacts are identical in contact size and shape, but are available in different crimp-barrel sizes to accommodate different wire sizes (Figure 3-7). When preparing a cable-half assembly, use the correct size contacts.

Wire Size	Serpent Contact
AWG 18 to 20 (0,824 to 0,519 mm^2)	Part 5404480
AWG 22 to 26 (0,325 to 0,128 mm^2)	Part 5362301
AWG 28 to 30 (0,080 to 0,051 mm^2)	Part 5362302

Figure 3-7. Serpent Contact Crimp-Barrel Sizes

The attached device has its own power supply. However, the attached device power can be under control of the CPU emergency power off (EPO) switch. Two wires are connected to the CPU's normally closed EPO switch and are routed directly to the SIOC connector block (Figures 1-2 and 2-2).

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