IBM Maintenance Library

Printer Attachment for System/3: Theory of Operation

Preface

This manual explains the operation of the IBM 5203 Printer Attachment.

Other manuals needed to understand and service the printer attachment are:

- The *IBM Maintenance Library 5203 Printer Attachment for System/3: Diagrams*, SY31-0240.
- The *IBM 5203 Printer, Field Engineering Theory of Operation Manual*, SY33-1045.
- The *IBM 5203 Printer, Field Engineering Maintenance Manual*, SY33-1046.
- The *IBM 5410 Central Processing Unit, Field Engineering Theory of Operation Manual*, SY31-0207.
- The *IBM Maintenance Library 5410 Processing Unit for System/3: Diagrams*, SY31-0202.
- The *IBM 5410 Central Processing Unit, Field Engineering Maintenance Manual*, SY31-0244.

For machine characteristics, refer to the *IBM System/3 Installation Manual – Physical Planning*, GA21-9084.

First Edition

Some illustrations in this manual have a code number in the lower corner. This is a publishing control number and is not related to the subject matter.

Changes are continually made to the specifications herein; any such change will be reported in subsequent revisions or technical newsletters.

A Reader's Comment Form is at the back of this publication. If the form has been removed, comments may be addressed to IBM Corporation, Product Publications, Department 245, Rochester, Minnesota 55901.

Contents

Abbreviations

ALU	Arithmetic Logic Unit
APL	Advance Program Level
CC	Character Counter
CPU	Processing Unit
DA	Device Address
DBI	Data Bus In
DBO	Data Bus Out
EOL	End of Line
HAR	Hammer Address Register
I/O	Input/Output
LIO	Load Input/Output
LPDAR	Line Printer Data Address Register
LPIAR	Line Printer Image Address Register
LPM	Lines Per Minute
LSR	Local Store Register
M	Mechanical Position
MAP	Maintenance Analysis Procedure
MST	Monolithic Systems Technology
PC	Print Cycle Steal
POR	Power On Reset
PSS	Print Subscan
SDR	Storage Data Register
SIO	Start Input/Output
SLD	Solid Logic Dense
SNS	Sense
SS	Single Shot
TIO	Test Input/Output
TP	Test Point
UCS	Universal Character Set
UPC	Unprintable Character
WO	With Out

The IBM 5203 Printer Attachment provides a means for the attached 5203 Printer to use the facilities of the IBM 5410 Processing Unit (CPU) to communicate with main storage. The attachment provides the communication lines between the printer and the CPU and controls the transfer of all information between the two (Figure 1-1).

The attachment circuitry is MST-1 logic, physically located on gate A, board B1 in the 5410 CPU. The control interface lines between the attachment board and the electronics board are SLD-100 levels. Conversion to MST occurs at the attachment board.

The communications path between the CPU and the printer attachment is through the I/O channel. Using this channel, data and control information is transferred from the CPU, and status is sent to the CPU under control of stored program instructions.

During the process of exchanging information, the printer and CPU operate together in multiplexer mode. This means the information transfer takes place between CPU cycles on a priority basis with other devices.

By means of a fixed-cycle steal priority, I/O cycles may be interleaved between any two CPU cycles to fetch or store data to and from the attachment. The 5203 Printer Attachment may be granted as many as three I/O cycles in a row.

5203 LINE PRINTER

- The 5203 Line Printer has 96, 120, or 132 print positions.
- Four print positions are served by one print hammer.
- The printer has four mechanical print positions per print line.
- The printer uses a type chain that travels at a constant speed.
- The printer has a paper-handling tapeless carriage.

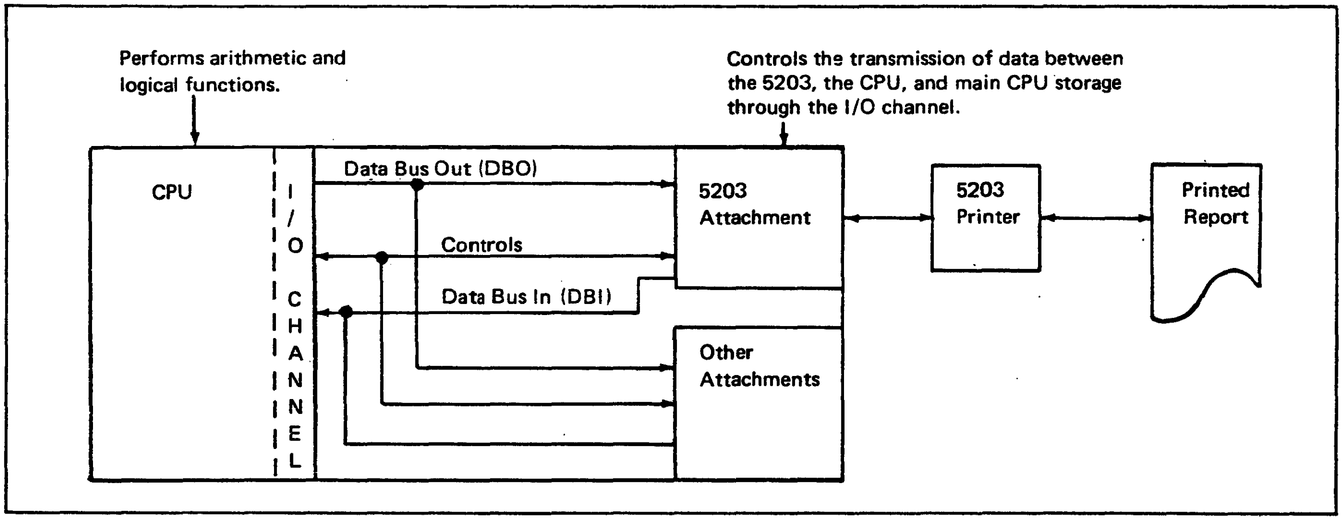

Performs arithmetic and logical functions.
Controls the transmission of data between the 5203, the CPU, and main CPU storage through the I/O channel.
CPU
I/O CHANNEL
Data Bus Out (DBO)
Controls
Data Bus In (DBI)
5203 Attachment
Other Attachments
5203 Printer
Printed Report

Figure 1-1. 5203 Data Flow

The Printer

The standard printer has 96 print positions, with a 100 LPM throughput, and a paper-handling tapeless carriage controlled by the attachment. Features available are 200 and 300 LPM throughput, 120 print positions, 132 print positions, a dual feed carriage, and a universal character set. This manual describes the 132-position printer unless otherwise stated.

The printer uses a 240-character type chain. A set of 48 characters repeated five times on the chain permits the rated throughput on the 100, 200, and 300 LPM models. A universal character set (UCS) of 120 characters repeated twice on the chain results in reduced throughput. The standard printer uses 24 hammers spaced four print positions apart. The four positions are called the four mechanical positions M1-M4. The hammers are held in one M position until all 48 characters are optioned to print. Then they are cam driven to cover the other three print positions ('hammer shift clutch' line to printer) under control of the attachment. With the UCS feature, the hammers are held in one position until end of line is detected by the attachment. The chain travels at a constant speed and is not stopped during printing. This means that a character is impressed as well as rubbed off on the form.

The printer supplies timed pulses to the attachment. One of these pulses is the home pulse which marks the beginning of each character set. Following the home pulse, another pulse is sent when character 1 is aligned with print position 1. This is the first subscan pulse. With a 48-character set, 144 subscan pulses are sent before the next home pulse occurs; this means that three subscan pulses are sent for each character. The home pulse, in conjunction with the character set and subscan pulses, allows the attachment to trace each character in relation to optioned positions.

Carriage

The carriage is a tapeless device controlled by the printer attachment circuitry. Forms movement is synchronized to the print line by the carriage emitter which generates a pulse for each line of print.

Before starting a print operation, the number of printable lines used is loaded into a carriage forms length register. Carriage motion, space or skip, is determined by the start I/O instruction.

Printer Timing Devices

The printer informs the using system about all mechanical motions that the system must take into consideration to exert logical control. The printer indicates the chain slug alignments (options to print), and mechanical position (M position). There are four basic timing devices. These are:

1. The incrementer emitter.
2. The chain emitter.
3. The UCS emitter (UCS feature).
4. The carriage emitter.

The actual timing devices are magnetic emitters, (chain, UCS, and carriage), and a photo cell (incrementer emitter). The magnetic emitters consist of transducers which sense that a timing slot, or steel tip passes by.

Incrementer Emitter

The incrementer uses a slot wheel that exposes or covers a light source as the incrementer rotates. A photo cell opposite the light generates a pulse each time the light beam hits the photo cell. These pulses are sent to a counter in the attachment to determine the mechanical position of the hammer unit.

Chain Emitter

The chain is driven by a three-phase synchronous motor via gears and a cog belt (Figure 1-2). One of the gear shafts bears the chain timing drum. This drum is divided into 144 evenly spaced slots. A 145th slot resides between the 144th and the first slot; this 145th slot represents the home pulse.

The gear ratio is such that the chain timing drum completes five revolutions for each chain revolution. This means the home pulse appears before each of the five (standard 48) character sets and each home pulse is then followed by subscan pulses. There are 144 subscan pulses: three subscans are required to offer one character to each print position and, since the basic character set consists of 48 different characters, we have 48 x 3 = 144 subscans per character set.

If this pulse scheme is examined independent of character sets, it is obvious there are three subscan pulses for every character on the chain; the chain is composed of 240 character positions. The chain drum performs five revolutions for each chain revolution (for each passing of 240 characters), so it generates five times 144 subscan pulses which results in 720 subscan pulses. Dividing these 720 subscan pulses by 240 characters results in three pulses per character as required; however, the five home pulses are used as such only with the standard character set.

Emitter (UCS Feature)

Any character set larger than 48 different characters is defined as a universal character set (UCS). The size of the set may vary from 49 to 120 different characters per set, with some graphics repeated until a 120 - character set is defined.

Whenever any type of UCS chain is installed on the printer, an additional chain drum is installed; this "drum" consists of a gear driven shaft with a steel tip attached (UCS emitter). This steel tip rotates 6 times per chain revolution (Figure 1-2) supplying 6 UCS home pulses. One chain emitter pulse and one UCS home pulse coincide once per chain revolution and this pulse is recognized as the home pulse. A microswitch activated by a stud on the UCS cartridge indicates to the attachment that single home pulses must be ignored because a UCS chain is installed.

Carriage Emitter

A carriage emitter pulse is generated during every carriage operation as each printable line is passed. The attachment counts the number of pulses and stops the carriage clutch as required.

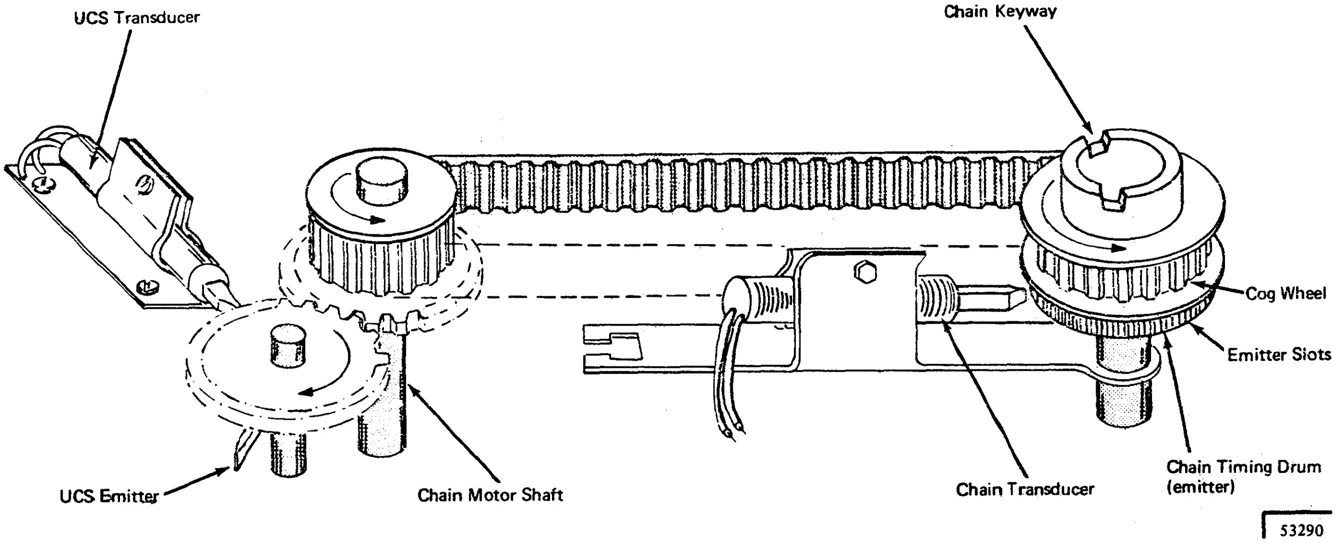


Figure 1-2. Chain and UCS Emitter

5203 PRINCIPLES OF CHAIN PRINTING

- One print cycle consists of 4 mechanical positions (M positions) for printing one line.
- The printer attachment options 132 print positions in one print cycle (132 position feature).
- The printer has 33 print hammers (132 position feature).
- A hammer bar moves the hammers to M positions 1, 2, 3, and 4.
- The printer attachment options 33 hammers to all 48 characters to fire in one M position.
- The printer attachment options 33 print positions (addresses) to print in one M position.
- A subscan is the time required to option one-third of the hammers (11) with 11 print positions.
- A scan is the time required to option all 33 hammers with 33 print positions (three subscans).
- 50 scans option 48 characters for one M position. The last 2 scans are for checking.
- The UCS feature needs 121 or fewer scans.

Theory

Like many chain printers, the distance between one type slug on the chain and its adjacent slug is 50% + 0.0005" greater than between adjacent print positions (Figure 1-3). This arrangement offers these combined advantages:

1. Because of sequential alignment, simultaneous printing in adjacent positions is avoided.
2. Sufficient compare time is available to determine whether or not a hammer should be fired.

Because we have a continuously moving type chain, we need some means of determining when to fire a particular hammer to print the proper character. Using Figure 1-4 as reference, observe the relationship between the moving type chain and the print-hammer positions. The figure shows the character A aligned with print position 1. In the 5203, if the character A is aligned to print in print position one, an I in print position 13 is the next character aligned to print. Between the A alignment and the I alignment, the chain will travel 0.004 inch. On Models 1 and 2, this makes 31 microseconds available to determine whether or not a hammer should be fired. The time is decreased to 19.39 microseconds on the Model 3.

Incrementer and Hammer Alignment

The following is a description of hammer incrementing and aligning that applies to the 5203 Printer (four-position hammer unit) with 132 print positions and 33 hammers.

Home position after power-on or error-reset operation places the hammers in the extreme right position of the incrementer (M4).

The print operation begins with hammer 1 facing print position 4, hammer 2 facing print position 8, hammer 3 facing print position 12, etc. (Figure 1-4). First, consider that 44 print positions become aligned during one subscan (one third of the 132 print positions).

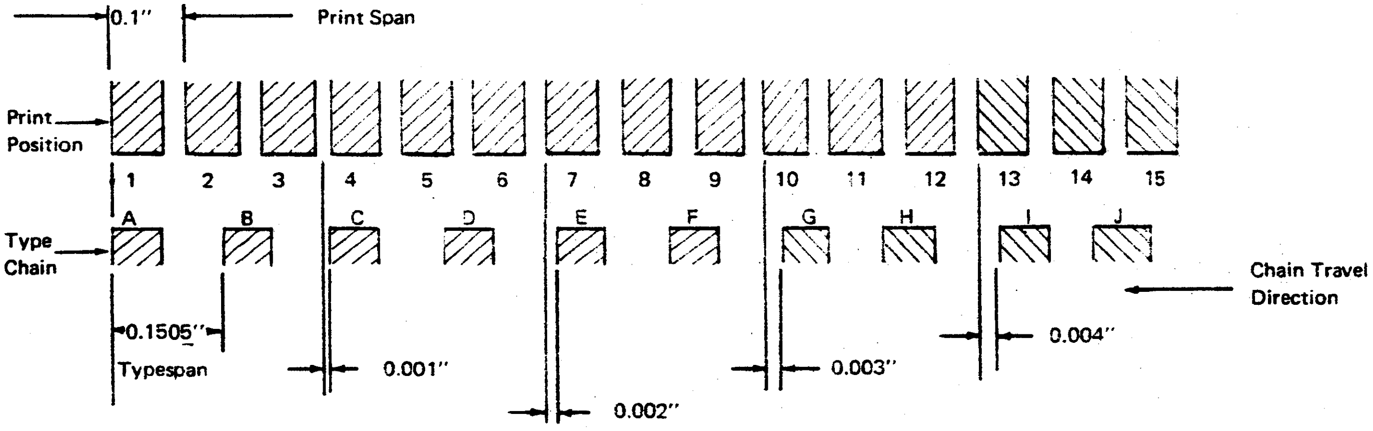


Figure 1-3. Actual Print Scan to Type Span Relationship

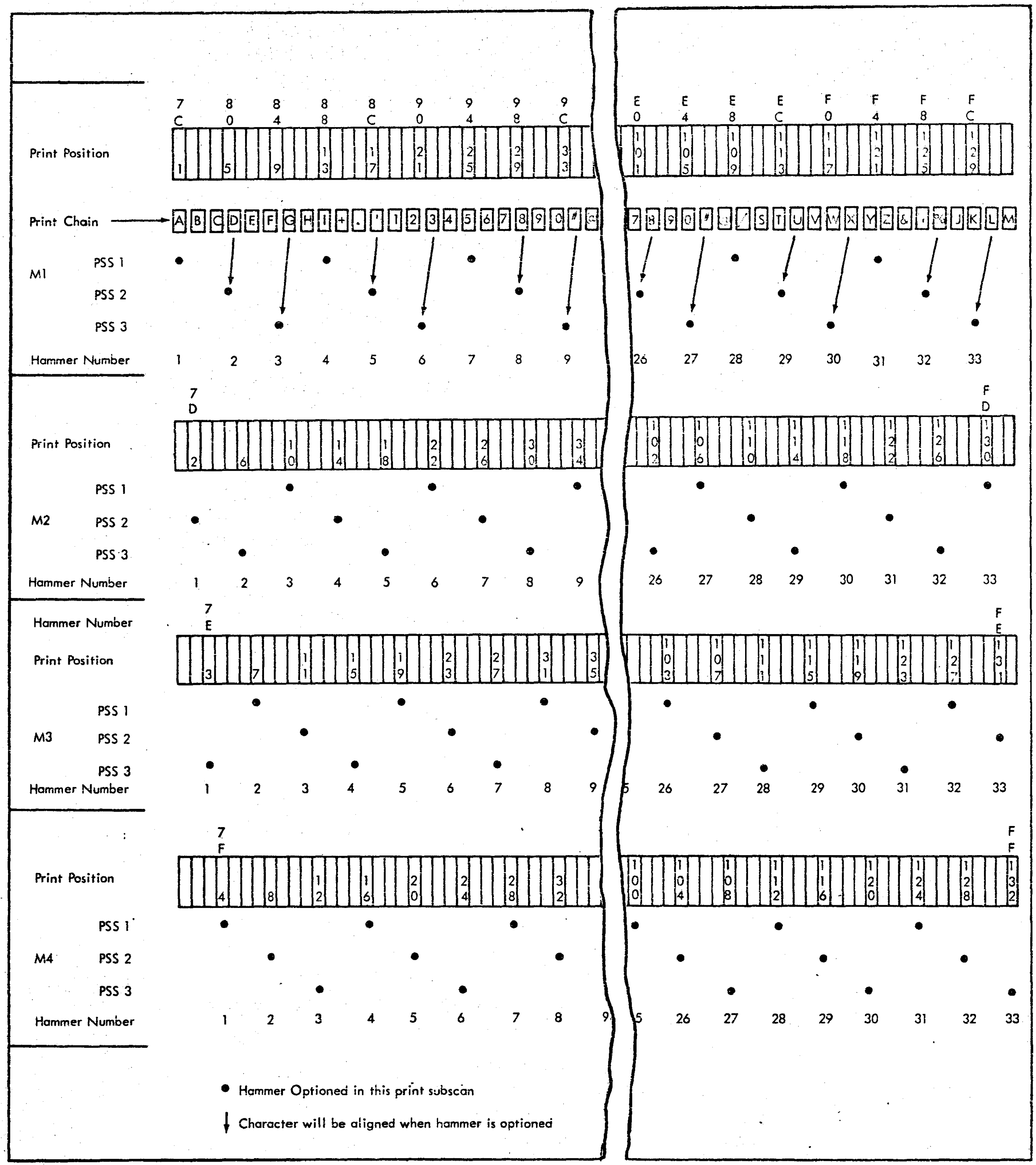

Print Position
Print Chain
M1
PSS 1
PSS 2
PSS 3
Hammer Number
M2
M3
M4
A B C D E F G H I + . (1 2 3 4 5 6 7 8 9 0 # @
7 8 9 0 # % / S T U V W X Y Z & , % J K L M
● Hammer Optioned in this print subscan
Character will be aligned when hammer is optioned

Figure 1-4. 5203 Printing Sequence

Because there is only one hammer for every 4 print positions, only 11 of the 44 print positions that become aligned can be optioned to print during each subscan. In one print scan, 33 print positions are optioned to print. A print scan must be taken for each character in the particular character set being used. For example, if the character set contains 48 characters, 48 print scans (144 subscans) must be taken to option each of the 33 print positions. Optioning each of the 33 print positions that face a hammer to every character in the character set, is called an *increment scan.* The initial increment scan with the hammers in mechanical position 4 (M4) is called *increment scan 4.* At the end of increment scan 4, the hammers are decremented (moved left one print position) so that hammer 1 faces print position 3, hammer 2 faces print position 7, hammer 3 faces print position 33, etc. The hammers are now facing a second group of 33 print positions. Again, a print scan is taken for each character in the character set. This sequence is called *increment scan 3.*

At the end of increment scan 3, the hammers are decremented so that hammer 1 faces print position 2, hammer 2 faces print position 6, hammer 3 faces print position 10, etc. The hammers are now facing a third group of 33 print positions. Again, a print scan is taken for each character in the character set. This sequence is called *increment scan 2.*

Finally, the hammers are decremented so that hammer 1 faces print position 1, hammer 2 faces print position 5, hammer 3 faces print position 9, etc. When the print scans are complete for increment scan 1, all of the 132 print positions have been optioned to print every character in the character set, and a print line is complete.

If the 200 or 300 LPM feature is installed, the sequence for the next print line is similar, but the increment scans are reversed. Because hammer 1 was facing print position 1 at the end of the previous print line, the next print line starts with increment scan 1. Then increment scans 2, 3, and 4, and another print line is complete. Because hammer 1 is facing position 4, this print line will start with increment scan 4. When increment scan 4 is complete, the hammers are decremented so that hammer 1 faces print position 3, hammer 2 faces print position 7, etc. Increment scan 3 is followed by increment scan 2, which, in turn, is followed by increment scan 1. For increment scan 1, hammer 1 is again facing print position 1. Thus, printing of the lines alternates between a progression (1, 2, 3, 4) and a regression (4, 3, 2, 1) of the increment scans.

If the printer and attachment are 100 LPM, the hammers are returned to M position 4, after printing in M position 1. This is done before a new print line is started. Increment scans will always regress (4, 3, 2, 1).

It is now apparent that 4 increment scans are required for one complete line of print. Using a character set of 48 characters, 192 print scans (576 subscans) are required to print one line. A position in the print line is printed only when the hammer faces the position and the correct character is aligned.

Subscans

For this explanation of subscans, assume a 200 line-per-minute printer with 132 positions (33 hammers) and assume that the hammer unit is at position M1.

Subscan 1 starts when any chain character (in this case an A) is aligned with print position 1 (Figure 1-4). (It does not matter which character starts scan 1, because all characters become aligned with print position 1.) Subscan 1 lasts until the next character on the chain is aligned with print position 2. During subscan 1, the first alignment occurs at print position 1, the next alignment occurs at the third position (counting from 1) which is print position 4, and so forth. Thus, the alignment progresses through the following print positions: 1, 4, 7, 10, 13, 16, 19, 22, 25, etc. Figure 1 - 4 shows that hammers are allocated to print positions 1, 5, 9, 13, 17, 21, 15, 29, etc. Note that the alignment is useful only for positions 1, 13, 25, 37, etc. ending with position 121 during subscan 1. This means that of the 44 theoretical alignments to print that occur during subscan 1, only 11 useful options to print occur. Three subscans provide 33 options to print. This can be seen by examining the next subscan in detail. During subscan 2, chain characters are aligned with print positions 2, 5, 8, 11, 14, 17, etc. (with every third position). Again, only 11 print positions (5, 17, 29, 41 and every subsequent 12th position) are aligned while hammers are in position for printing.

By now, the scanning scheme should be apparent; three subscans are required to offer a single character to 33 print positions. Since three subscans make up one print scan, 48 print scans are required to offer each character contained in a 48 character set to the 33 print positions. For this reason, 48 print scans (or more with UCS feature) are termed one increment scan, or M position. To print an entire 132-position print line requires 4 increment scans = 192 print scans = 576 subscans (based on a 48 character set).

Our explanation started with the hammer unit at position M1; note that the first 48 print scans (the first increment scan) occurred without cam motion. The clutch now unlocks the cam and the hammer bar begins to move until the next M position, M2, is reached. This lasts long enough to allow the next 48 print scans. After three positions have passed, the right home position (M4) is reached, and forms movement can be initiated. Then, the same action occurs right to left. It can now be seen that the printer must signal the attachment (1) when a useful option to print exists (the PSS chain emitter), and (2) when the hammers have moved to the next M position (increment emitter). The attachment can then tell the CPU to compare the chain character with the character in storage and decide whether or not to print.

INSTRUCTION FORMAT

I/O Instruction Format

The CPU stored program uses five I/O instructions to control the printer attachment:

1. Start I/O
2. Load I/O
3. Test I/O
4. Advance Program Level
5. Sense I/O

Op Code

The first byte of each instruction is the op code. During the I-OP cycle, the CPU decodes the op code and informs the printer attachment of the presence of the instruction. This information is sent to the attachment on the channel tag out lines 'SNS instr', 'LIO instr', 'TIO instr'. and 'SIO instr'. The channel uses the 'TIO instr' tag lines for both test I/O and advance program level instructions.

Q Byte

The second byte of each instruction is the Q byte. During the I-Q cycle, this byte is placed on the DBO lines at clock 5 time. All attachments on the channel receive the Q byte and check its parity (correct parity is odd) for all I/O instructions regardless of the condition of the I/O device or the device address of the Q byte.

Parity

If an attachment finds the parity of the Q byte is even, it raises both 'I/O condition A' and 'I/O condition B' at clock 5 of the I-Q cycle.

Start I/O (SIO) Instruction

- Three bytes make up the SIO instruction.
- The SIO instruction selects the line printer whenever the device address equals E (hexadecimal).
- The SIO instruction can select either the right or the left carriage.
- The N field of the SIO instruction specifies one of the following operations:
  1. Space only.
  2. Print and space.
  3. Skip only.
  4. Print and skip.
- Both carriages can operate simultaneously (with dual feed carriage feature installed), but a separate SIO instruction is required for each carriage.

The SIO instruction is composed of three bytes (Figure 1-5). The first byte is the op code, an F3 (hexadecimal). The second byte contains the device address (a hexadecimal E for the line printer), a primary or secondary modifier (M bit), and an N field. The third byte specifies carriage spacing.

Q Byte Description

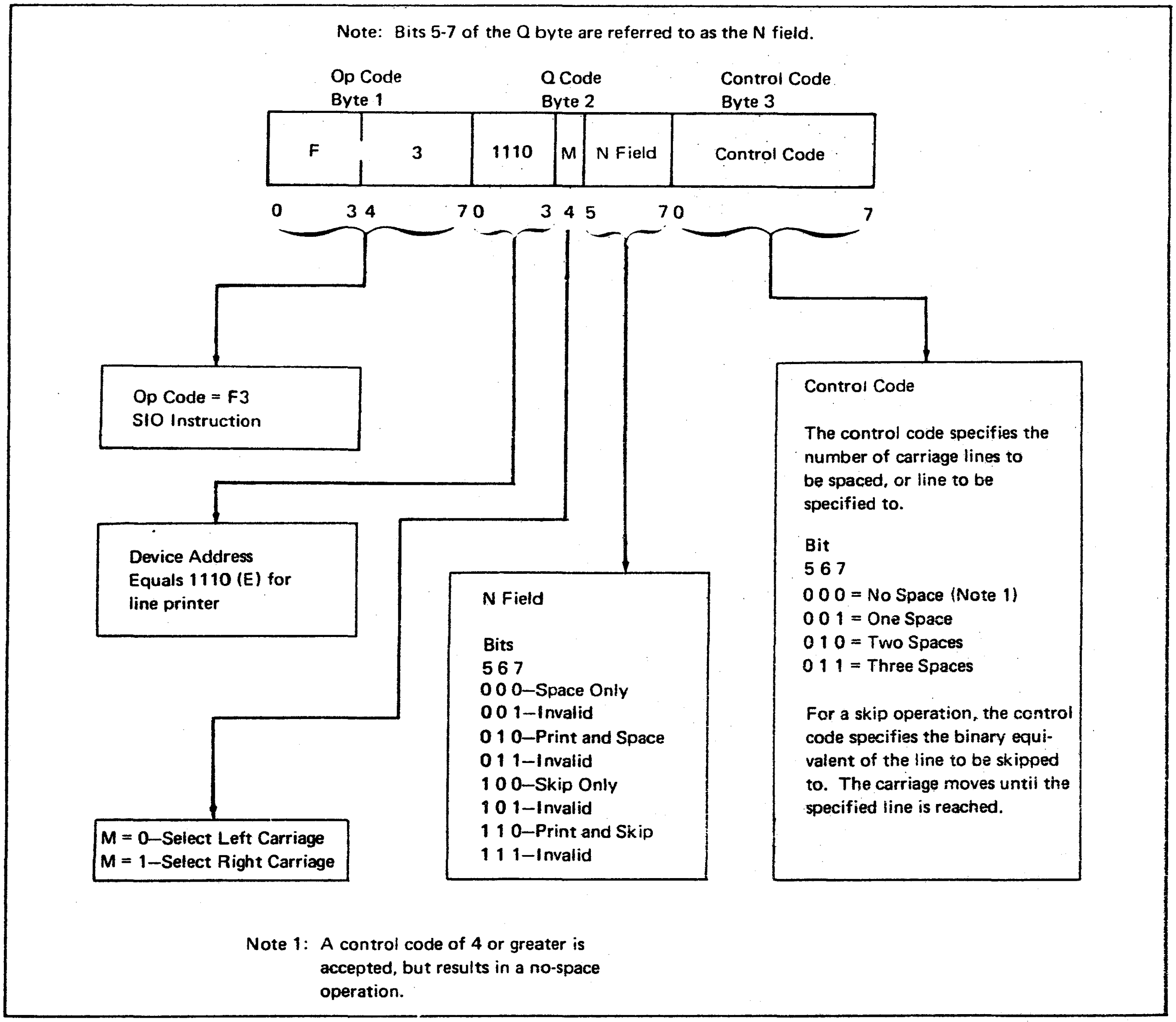
Bits 0-3 specify the device address of the line printer. Bit 4 is the M field and specifies the carriage used—an M bit of 0 specifies the left carriage, and an M bit of 1 specifies the right carriage.

Note: If the dual feed carriage feature is *not* installed, an M field of 1 results in a processor check stop and the INV-Q light comes on.

Bits 5-7 hold the N field. Refer to Figure 1-5 for the N field code. An invalid N field causes a processor check stop, and causes the INV-Q light to come on.

Control Code

The control code specifies carriage spacing. A 0, 1, 2, or 3 specifies the carriage to space 0, 1, 2, or 3 spaces, respectively. A control code of 4 or greater is accepted, but results in a space 0 operation.



Note: Bits 5-7 of the Q byte are referred to as the N field.

Op Code = F3
SIO Instruction

Device Address
Equals 1110 (E) for
line printer

M = 0—Select Left Carriage
M = 1—Select Right Carriage

N Field

Bits
5 6 7
0 0 0—Space Only
0 0 1—Invalid
0 1 0—Print and Space
0 1 1—Invalid
1 0 0—Skip Only
1 0 1—Invalid
1 1 0—Print and Skip
1 1 1—Invalid

Control Code

The control code specifies the number of carriage lines to be spaced, or line to be specified to.

Bit
5 6 7
0 0 0 = No Space (Note 1)
0 0 1 = One Space
0 1 0 = Two Spaces
0 1 1 = Three Spaces

For a skip operation, the control code specifies the binary equivalent of the line to be skipped to. The carriage moves until the specified line is reached.

Note 1: A control code of 4 or greater is accepted, but results in a no-space operation.

Figure 1-5. SIO Instruction Format

For a skip operation, the control code specifies the binary equivalent of the line to which the form must skip. The carriage moves the form until the specified line is reached.

Parity and Error Conditions

The SIO instruction must maintain odd parity. If even parity is detected by the attachment circuitry, a processor check stop occurs and the DBO parity light comes on. The attachment ignores the instruction and sets a No-Op status bit if a device error exists when the SIO instruction is received. Program interlock occurs whenever a printer busy condition is detected, or operator intervention is required as indicated by the I/O attention light.

Load I/O (LIO) Instruction

- Three or four bytes make up the LIO instruction (direct addressing, 4 bytes; indexing, 3 bytes).
- The LIO instruction selects the line printer when the device address equals E (hexadecimal).
- The M field of the LIO is insignificant (that is, not necessary to select a carriage).
- The N code of the LIO instruction is used to:

  1. Select the forms length register in the attachment to be loaded, or
  2. Select the LPIAR in the CPU for preloading, or
  3. Select the LPDAR in the CPU for preloading.

The LIO instruction is composed of 3 bytes if the op code indicates indexing, or 4 bytes if the op code indicates direct addressing (Figure 1-6). The first byte is the op code. The second byte contains the device address (a hexadecimal E for the printer), a primary or secondary modifier (M bit—not significant for this instruction), and an N field. The third, or third and fourth, specifies one of the following:

1. The address of the storage location containing the forms length.
2. The storage location of the data (address) to be placed in the selected LSR.

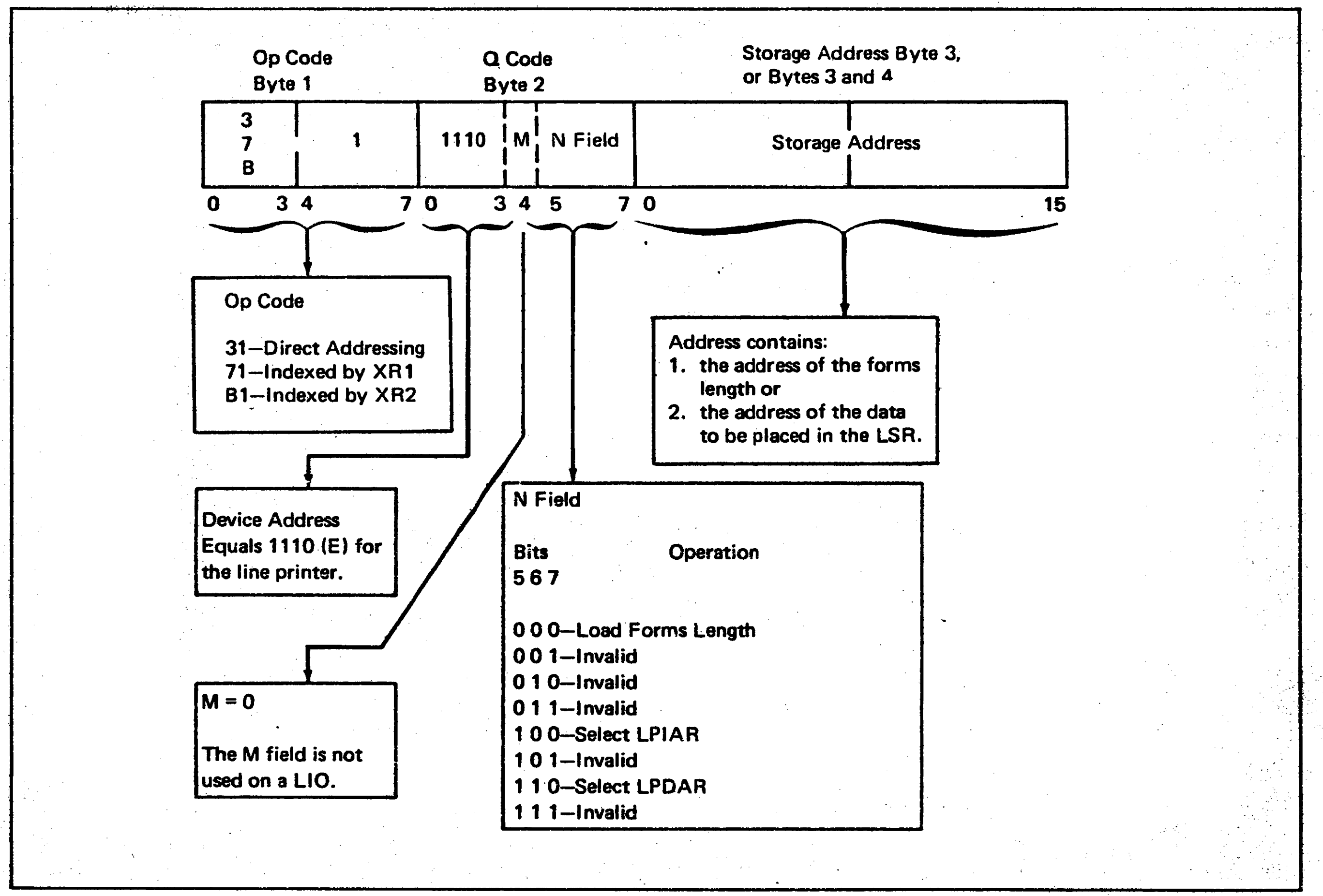


Figure 1-6. LIO Instruction Format

Q Byte Description

Bits 0-3 specify the address of the line printer. Bit 4 is the M field and is not used for an LIO instruction.

Bits 5-7 are the N field. Refer to Figure 1-6 for the N code. An invalid N field causes a processor check stop, and causes the INV-Q light to come on.

Storage Address Description

The storage address portion contains the storage address of the 2-byte main storage field where information specified by the N field is located. If the N field specifies that the forms-length registers are to be loaded, (1) the data at the specified address is placed into the right-carriage forms length register (dual carriage feature) and (2) the data at the specified address minus 1 is placed into the left-carriage forms length register. If the N field specifies the preloading of the line printer data address register (LPDAR), the 2-byte field specified is placed into the LPDAR. If the N field specifies preloading the line printer image address register (LPIAR), the 2-byte field specified is placed in the LPIAR.

LSR Main Storage Areas

The core area addressed by the two address registers is as follows:

- 48 character set image must be in the 48 bytes of core location XV00 through XV2F.
- 120 character set image must be in the 120 bytes of core location XW00 through XW77.
- Line printer data for 96 print positions must be in the 96 bytes of core location XX7C through XXDB.
- Line printer data for 120 print positions must be in the 120 bytes of core location XY7C through XYF3.
- Line printer data for 132 print positions must be in the 132 bytes of core location XZ7C through XZFF.
- The addresses XV, XW, XX, XY, or XZ are assigned by the programmer and may or may not be the same.

The line printer data field in core beginning at location XX7C corresponds character to character to the print line beginning at print position one.

Parity and Error Conditions

The LIO instruction is accepted only if the printer is not busy. A parity error detected by the attachment results in a processor check stop, and the DBO parity check light comes on. If the No-Op status bit is on from a previous SIO instruction, the instruction is ignored by the attachment.

Test I/O (TIO) Instruction

- Three or four bytes make up the TIO instruction (direct addressing 4 bytes, indexing 3 bytes).
- The TIO instruction selects the line printer when the device address equals E (hexadecimal).
- Either the right or the left carriage is selected during the TIO instruction execution.
- The N code of the TIO instruction specifies a test for one of the following:

1. Not ready.
2. Print buffer busy.
3. Carriage busy.
4. Printer busy.

The TIO instruction is composed of three or four bytes (Figure 1-7). The first byte is the op code. The second byte contains the device address (a hexadecimal E for the line printer), a primary or secondary modifier (M bit), and an N field. The third byte, or third and fourth bytes, contains the branch to address if the N field condition is met.

Q Byte Description

Bits 0-3 specify the data address of the line printer. Bit 4 is the M field and specifies the carriage used. An M bit of 0 specifies the left carriage, and an M bit of 1 specifies the right carriage.

Bits 5-7 are the N field. Refer to Figure 1-7 for the N field code. An invalid N field causes a processor check stop, and the INV-Q light comes on. The N field contains the condition code that determines the test to be performed.

Storage Address Description

The storage address portion of the TIO instruction contains the branch to address if the condition tested for (as specified by the N field) is met.

Parity and Error Conditions

The TIO instruction must maintain odd parity. A parity error detected by the attachment results in a processor check stop, and the DBO parity check light comes on. If the No-Op status bit is on from a previous LIO instruction, the instruction is ignored by the attachment.

Advance Program Level (APL) Instruction

- Three bytes make up the APL instruction (bytė 3 not used).
- The APL instruction selects the line printer whenever the device address equals E (hexadecimal).
- Either the right or the left carriage is selected during the APL instruction execution.
- The N code of the APL instruction specifies a test for one of the following:

  1. Not ready.
  2. Print buffer busy.
  3. Carriage busy.
  4. Printer busy.

- The APL instruction is used on machines that have the dual program feature installed.
- The format of the APL instruction is similar to the TIO instruction.

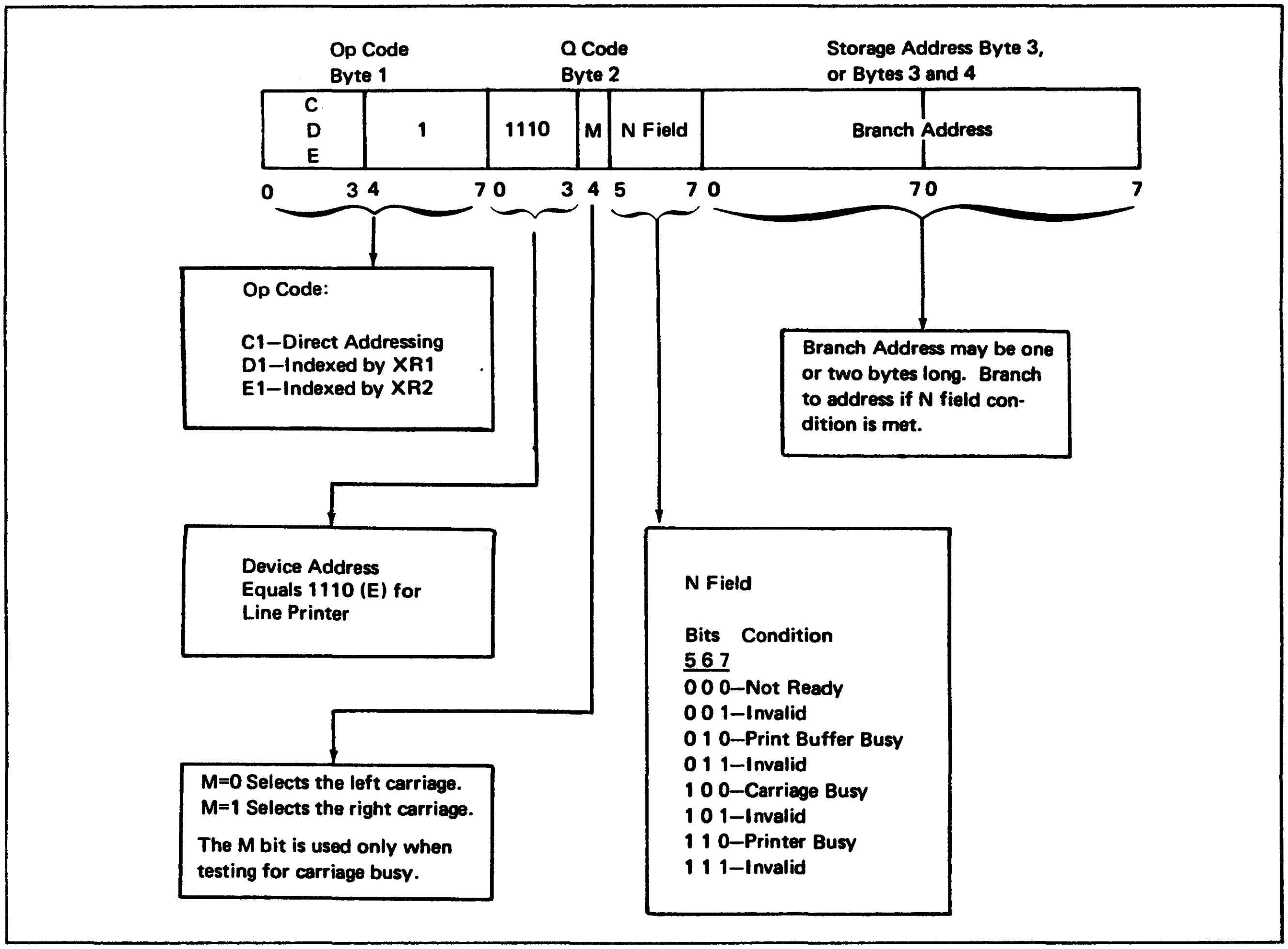


Figure 1-7. TIO Instruction Format

The APL instruction is composed of three bytes (Figure 1-8). The first byte is the op code, an F1 (hexadecimal) for an APL instruction. The second byte contains the device address (a hexadecimal E for the line printer), a primary or secondary modifier (M bit), and an N field. The third byte is not used.

If the Dual Program Feature is installed in the CPU, the APL instruction determines whether the program should proceed to the next sequential instruction or change levels.

Q Byte Description

Bits 0-3 specify the address of the line printer. Bit 4 is the M field and specifies the carriage used. An M bit of 0 specifies the left carriage, and an M bit of 1 specifies the right carriage.

Bits 5-7 are the N field. Refer to Figure 1-8 for the N field code. An invalid N field causes a processor check stop and the INV-Q light comes on. The N field contains the condition code that determines the test to be performed.

Storage Address Description

The storage address portion of the APL instruction is not used; that is, it is ignored by both the CPU and the attachment.

Parity and Error Conditions

Odd parity must be maintained in the APL instruction. A parity error detected by the attachment results in a processor check stop, and the DBO parity check light comes on. If the No-Op status bit is on from a previous APL instruction, the instruction is ignored by the attachment.

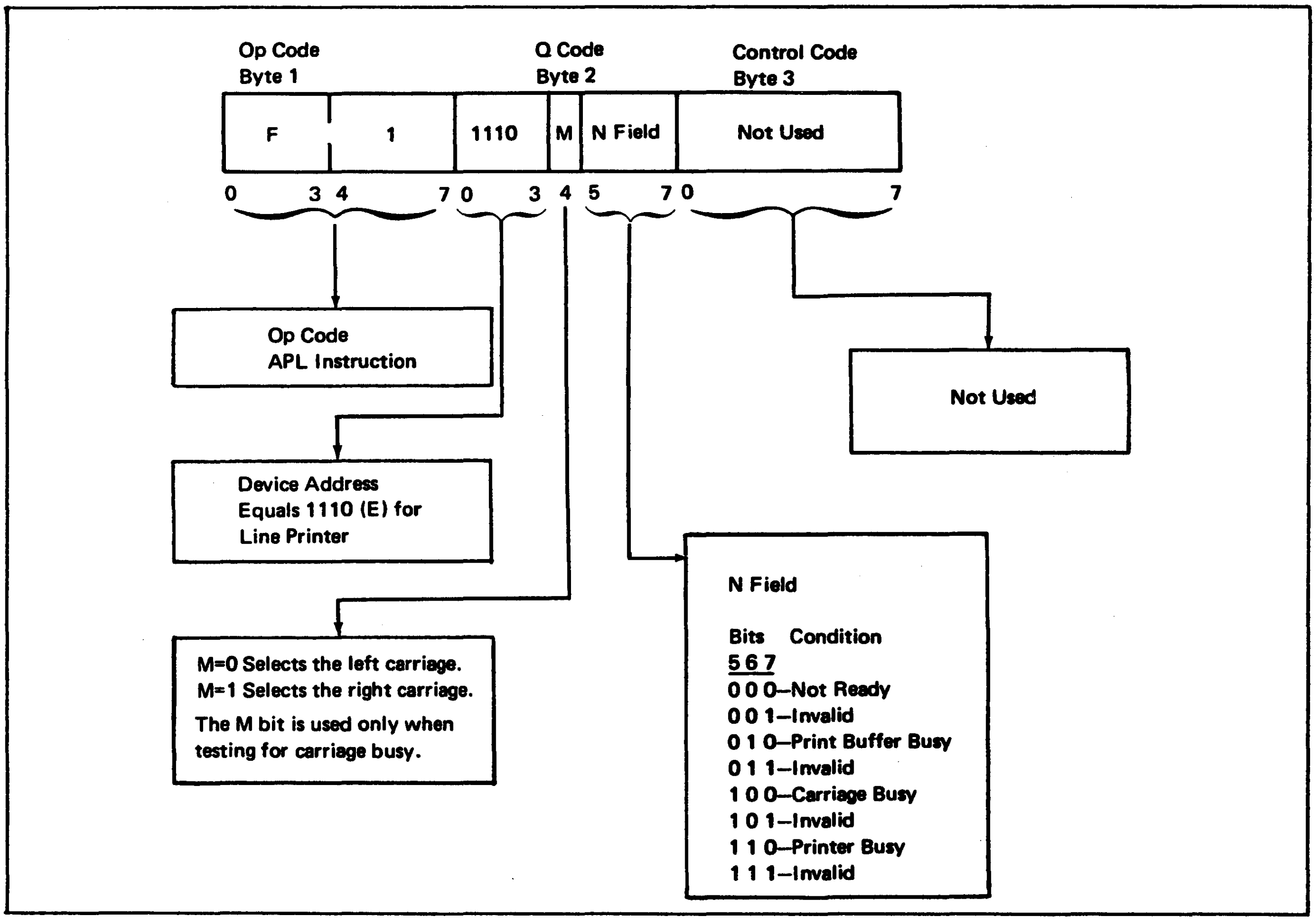


Figure 1-8. APL Instruction Format

Sense I/O (SNS) Instruction

- Three or four bytes make up the SNS instruction (direct addressing 4 bytes, indexing, 3 bytes).

- The SNS instruction selects the line printer whenever the device address equals E (hexadecimal).

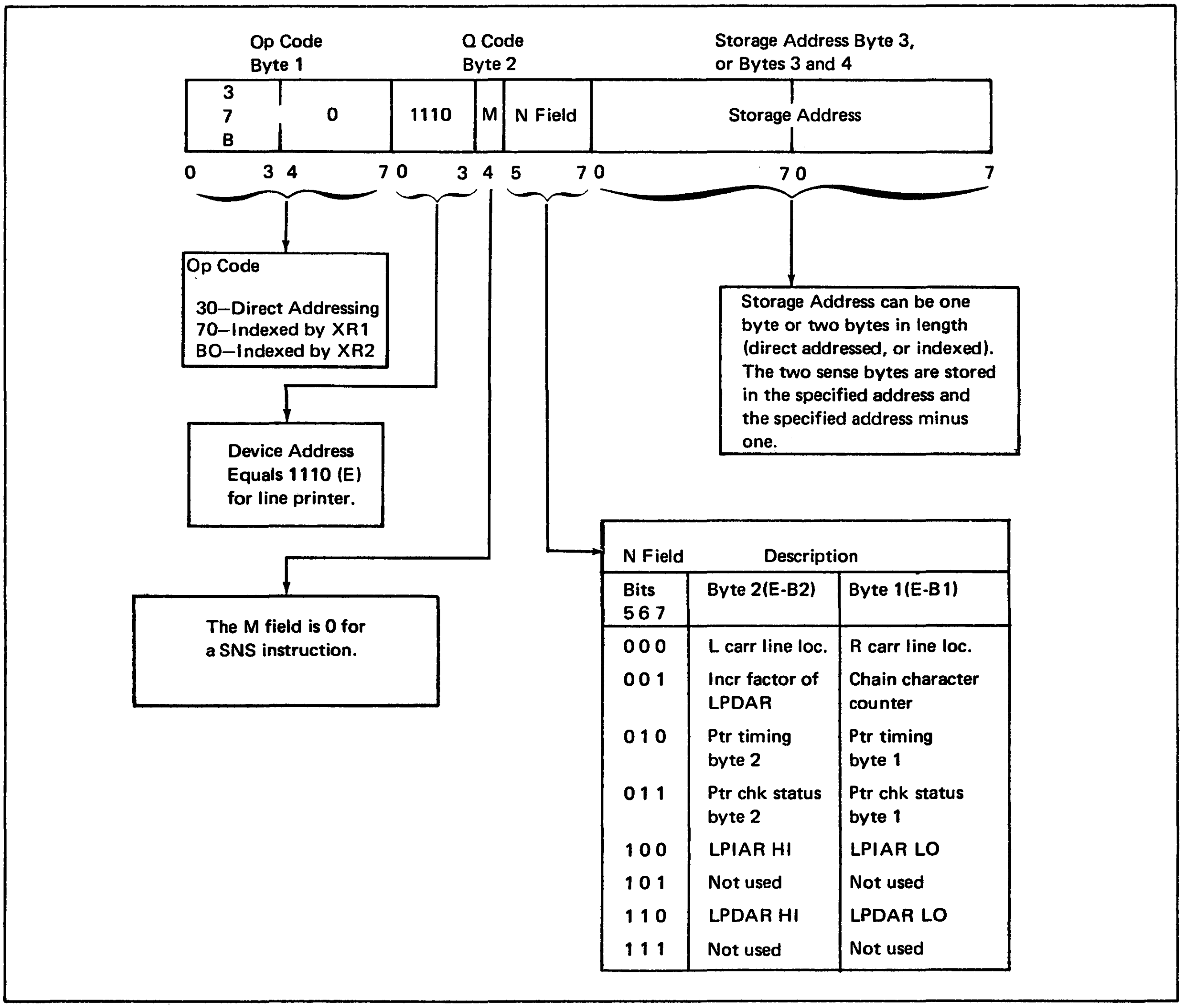
- The M field of the SNS instruction is insignificant (that is, not necessary to select a carriage).

- The N code of the SNS instruction is decoded to obtain the following sense information:

  1. Right or left carriage line location.
  2. The increment factor of the LPDAR.
  3. The value in the chain character counter.
  4. Printer timing bytes.
  5. Printer check status bytes.
  6. LPIAR or LPDAR high or low order bytes.

- The SNS instruction can be used at any time, whether the printer or attachment is busy or not.

The SNS instruction is composed of three or four bytes (Figure 1-9). The first byte is the op code. The second byte contains the device address (a hexadecimal E for the line printer), a primary or secondary modifier (M bit–not significant for this instruction), and an N field. The third, or third and fourth bytes, contains the address of the storage area in which sense bytes will be stored.



The M field is 0 for a SNS instruction.

Storage Address can be one byte or two bytes in length (direct addressed, or indexed). The two sense bytes are stored in the specified address and the specified address minus one.

N Field	Description	
Bits 5 6 7	Byte 2(E-B2)	Byte 1(E-B1)
0 0 0	L carr line loc.	R carr line loc.
0 0 1	Incr factor of LPDAR	Chain character counter
0 1 0	Ptr timing byte 2	Ptr timing byte 1
0 1 1	Ptr chk status byte 2	Ptr chk status byte 1
1 0 0	LPIAR HI	LPIAR LO
1 0 1	Not used	Not used
1 1 0	LPDAR HI	LPDAR LO
1 1 1	Not used	Not used

Figure 1-9. SNS Instruction Format

Q Byte Description

Bits 0-3 specify the data address of the line printer. Bit 4 (M field) is not used for an SNS instruction.

Bits 5-7 are the N field. Refer to Figure 1-9 for the N field code. An invalid N field causes a processor check stop, and the INV-Q light comes on.

Storage Address Description

The storage address portion of the instruction contains the storage address of the 2-byte field in main storage where the sense information specified by the N field is to be stored. Byte 1 is stored at the storage address specified. Byte 2 is stored at the storage address specified minus 1.

The following is a breakdown of each byte specified by the N field:

N Code 0: 000–Carriage print line location. This instruction should be preceded by a TIO for busy to ensure that the carriage location sensed is static.

N Code 1: 001–These bytes are provided for MTAP diagnostics.

Byte 1–When not printing, this is the value of the chain character counter indicating the character in print position one.

When printing, this is the value of the chain character counter indicating the character in the next print position being addressed.

Note: Because the chain character counter is being advanced asynchronously to the SNS instruction, an SNS made at the time the chain character counter is in transition from one count to another may result in an invalid count.

Byte 2–This indicates the binary amount to add to or subtract from the LPDAR when printing.

N Code 2: 010–Printer timing. These bytes are provided for MTAP diagnostics.

Byte 1 Bit 0: Hammer increment clutch–indicates clutch control is active in the attachment. The SNS bit is not latched.

Bit 1: Print start SS–incrementer emitter pulse indicating hammers are positioned to print in new dwell. The SNS bit is not latched.

Bit 2: Left or right carriage clutch–indicates that one or both of the clutch controls are active in the attachment. The SNS bit is not latched.

Bits 3-5: These bits correspond to the first, second, and third print cycle steals respectively. The bits are latched and reset with the SNS instruction.

Bit 6: Hammer set pulse–timing pulse which turns the hammer driver latches on. The bit is latched and reset with the SNS instruction.

Bit 7: Right shift position–output of reed relay that senses when the hammer unit is in the extreme right position. The SNS bit is not latched.

Byte 2 Bit 0: Left or right carriage emitter–indicates the forms have moved from one print line to the next print line for each emitter pulse. The SNS bit is not latched.

Bit 1: Execute print latch–defines the execution time of the print instruction. The SNS bit is not latched.

Bit 2: Chain emitter–includes home pulse. Chain emitter pulse has been received from the printer indicating alignment to print. The bit is latched and reset with the SNS instruction.

Bit 3: PSS1 pulse–this is the first of three subscans in any given print scan. The SNS bit is not latched.

Bit 4: Print time–indicates chain synchronization with the instruction. The SNS bit is not latched.

Bit 5: CE sense bit–not latched.

Bit 6: Mechanical position one–hammer unit is at leftmost mechanical position. The SNS bit is not latched.

Bit 7: Home gate–indicates the end of a character set on the chain installed. The SNS bit is not latched.

N Code 3: 011–Printer check status. These bytes are for program interrogation. The SNS bits are latched and reset by pressing the printer start key or the system check reset key, unless otherwise noted.

Byte 1 Bit 0: Chain sync check–indicates the loss of synchronization between the chain and the chain character counter.

Bit 1: Incrementer sync check–indicates the loss of synchronization between the incrementer and the mechanical position counter.

Bit 2: Thermal check–indicates excessive temperature in the hammer area. The SNS bit is not latched.

Bits 3 and 4: Not used.

Bit 5: 48 character set chain–indicates that the standard 48 character set chain is installed. The SNS bit is not latched.

Bit 6: Unprintable character–indicates that an unprintable character exists in the print data area. The SNS bit is latched and reset with each new SIO print instruction.

Bit 7: CE sense bit–this bit can be temporarily wired at the board level to monitor available signals. The SNS bit is not latched.

Byte 2 Bit 0: Carriage sync check–indicates loss of synchronization between the forms line, and the carriage line counter. This condition occurs as a result of a missing carriage emitter pulse.

Bit 1: Carriage space check–indicates that the carriage has moved farther than the command specified. This condition occurs as a result of an extra chain emitter pulse.

Bit 2: Forms jam check–indicates paper is not feeding properly.

Bit 3: Incrementer failure check–indicates the hammer incrementing unit failed to respond when the clutch control was activated.

Bit 4: CE sense bit latched–this bit can be temporarily wired at the board level to monitor available signals.

Bit 5: Hammer echo check–indicates improper response of hammer driver during print time.

Bit 6: Any hammer on check–indicates a hammer or the check circuit is defective, when not in print time.

Bit 7: No-Op–indicates that the instruction was accepted but not executed because of an error. This condition is reset with an SNS instruction.

N Code 4: 100–Selects the LPIAR (selects the LSR used as the line printer image address register).

N Code 5: 101–Invalid.

N Code 6: 110–Selects the LPDAR (selects the LSR used as the line printer data address register).

N Code 7: 111–Invalid.

Parity and Error Conditions

The SNS instruction which is accepted at all times by the printer attachment

Parity and Error Conditions

The SNS instruction, which is accepted at all times by the printer attachment, must maintain odd parity. A parity error detected by the attachment results in a processor check stop, and the DBO parity check light comes on. If the no-op status bit is on from a previous SNS instruction, the attachment ignores the current instruction.

Section 1. Printer

DATA BUS OUT REGISTER

- The data bus out (DBO) register has nine flip latches.
- All print data from the CPU enters the attachment through the data bus out register setting the appropriate flip latches.
- The latches remain set if there is a parity error, so the CE can observe the contents of the register.
- Data from the data bus out register loads the data register, carriage space-skip register, carriage forms length register, Q register, and the hammer address register.

Circuit Objectives

Refer to FEMD 4-015 and Figure 2-1. The DBO register output follows the input. The latches remain set if a parity check occurs so the CE can observe the contents of the register.

DATA REGISTERS 1 AND 2

- The data registers sample the DBO register to store and decode cycle steal data.
- The data registers have a total of eleven flip latches (eight for storing a data character and three for decoding).

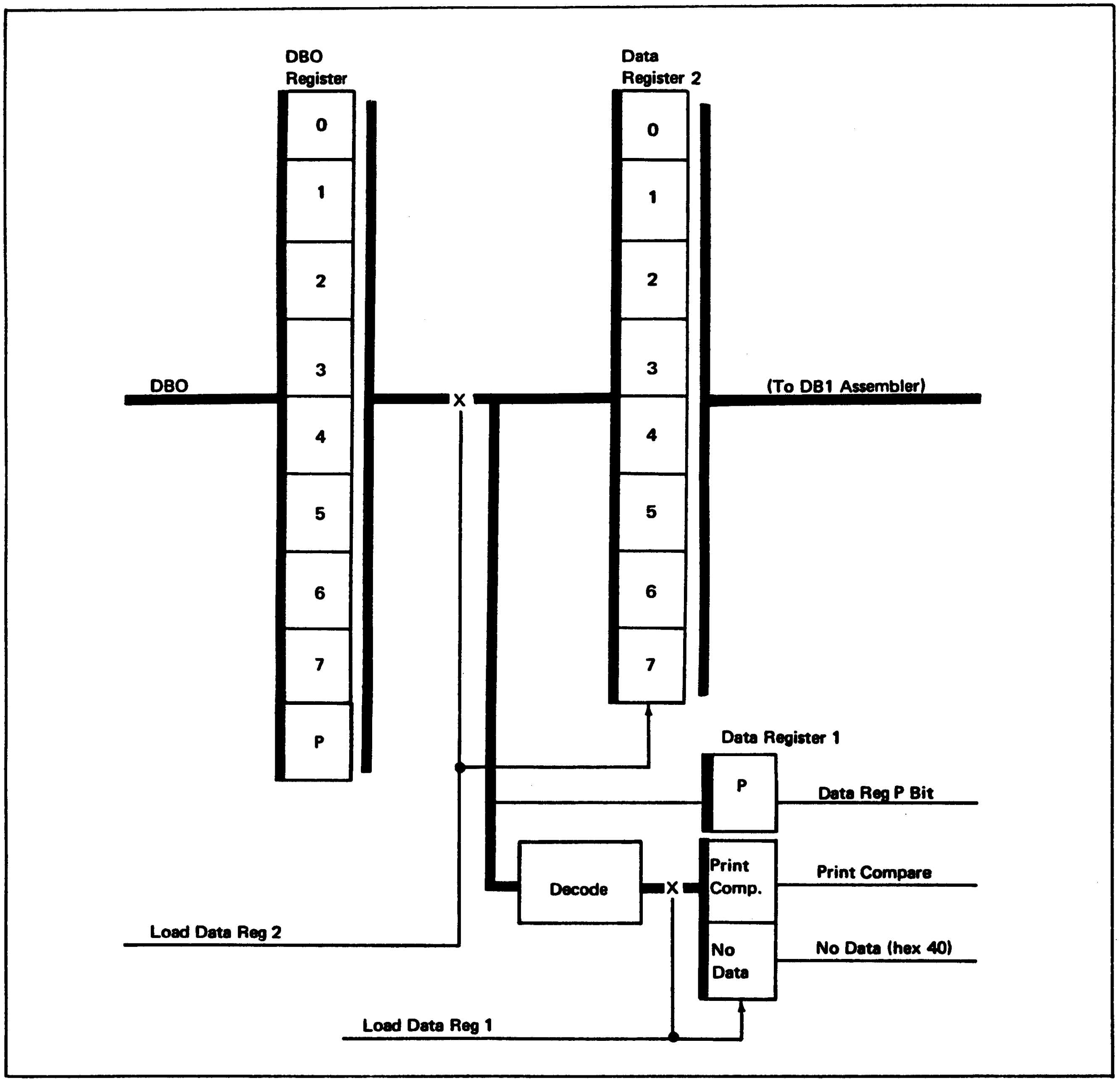


Figure 2-1. DBO and Data Register

- On print cycle steal zero:

  1. Data register 2 stores the main storage address of the first data character to be optioned for printing.
  2. Data register 2 preloads the hammer address register with the same data character address.

- On print cycle steal one:

  1. Data register 2 stores a data character from the main storage location addressed by the LPDAR.
  2. Data register 1 decodes it to see if it is a blank (hexadecimal 40) or data.

- On print cycle steal two:

  1. Data register 2 places the data character in the data bus in (DBI) assembler.
  2. Data register 1 decodes the results of ALU subtraction to check for a print compare (no bits active).

Circuit Objectives

Refer to FEMD 4-015 and Figure 2-1. The data register flip latches are set by the outputs of the data bus out flip latches and by activating the 'load data reg 1' or 'load data reg 2' lines.

During PC0, the data register accepts the main storage address of the character that is going to be optioned first for printing. The data register latches are set by 'load data reg 2' at 'sample DBO cl 3'. At clock 4, the data address is loaded into the hammer address register.

During PC1, the data character to be optioned for printing is loaded into the data register. Data register latches are set by 'load data reg 2' at 'sample DBO cl 5'. At the same time, the data character is decoded to see if it is a blank character (hexadecimal 40). If it decodes as a hexadecimal 40, the 'no data' data register latch is set. Setting this latch activates 'pc group end' and no more print cycles are taken. If any code other than a hexadecimal 40 is decoded, the 'no data' latch does not set and PC2 will be requested.

During PC2, the data character is put into the DBI assembler at 'pc2 ● cl 1' and taken to the A register in the CPU. An image character, addressed by the LPIAR, is subtracted in the ALU from the A-register character and the results are returned to the data register. At 'sample DBO cl 5' the 'load data reg 1' line is activated to decode the results of this subtraction. If all the returning data bits are inactive, the 'compare' latch in the data register sets and 'print compare' becomes active. If any of the returning data bits are active, the 'compare' latch will not be set and 'pc group end' will become active, and no more cycle steals will be taken.

If the 'compare' latch was set, PC3 occurs and the character is printed.

Q REGISTER

- Consists of a six-position Q register, a four-position status register, and a Q byte decode.
- The six-position Q register samples the DBO register to determine the contents of the Q byte of the instruction.
- The four-position status register records whether or not (1) the left carriage is busy, (2) the right carriage is busy, (3) the print buffer is busy, and (4) the printer is ready at the time the Q register is loaded.
- The Q byte decode decodes the outputs of the Q register and the status register.

The Q register (Figure 2-2) decodes the instruction Q byte to determine printer status and to select the appropriate printer response.

During the I-Q cycle, the Q register samples the Q byte data stored in the DBO register. The printer DA bits are decoded and recorded as one bit in the Q register.

The status register is also sampled during the I-Q cycle. Conditions checked for are left carriage busy, right carriage busy, print buffer busy, and printer ready. The outputs of the Q register and the status register are decoded to determine the channel condition (A or B) and the appropriate select or sense lines are activated in the attachment.

Circuit Objectives

Refer to FEMD 4-020. At sample DBO clock 5 time of an I-Q cycle, 'sample Q byte' is activated. With this line active, the contents of both the Q register and status register are sampled and decoded. The appropriate select, sense, and condition lines are activated in the Q byte decode circuits.

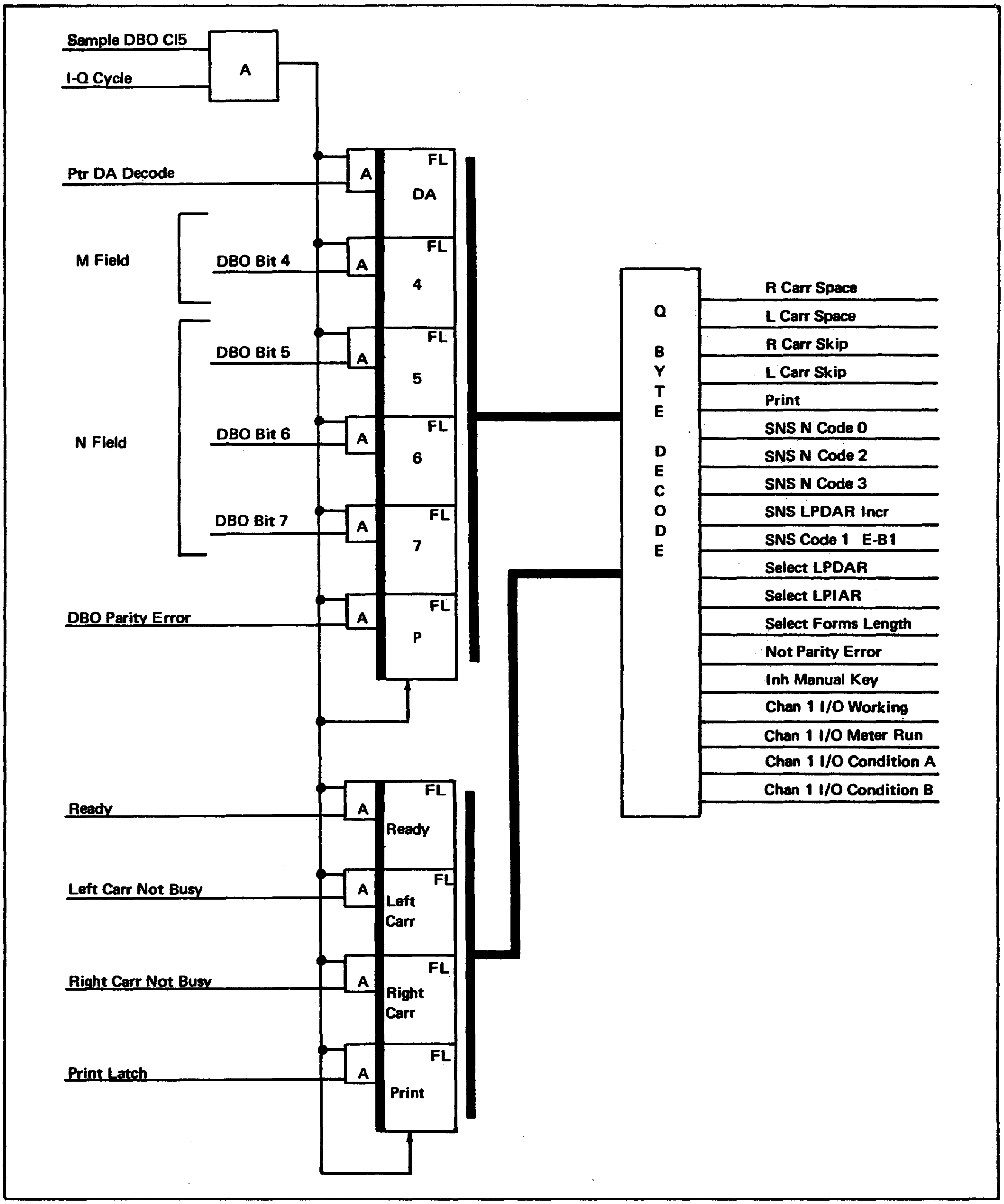


Figure 2-2. Q Register and Decode

SENSE BIT ASSEMBLER

- The SNS bit assembler contains the status of the printer attachment logic.
- The SNS bits are placed in the DBI assembler and sent to the CPU on E-B cycles.

The sense bit assembler (Figure 2-3) gates the status of the printer attachment logic circuitry. This status information is available at any time an SNS instruction is received by the printer. The SNS is accepted by the attachment whether or not the printer is busy. The status is decoded into DBI SNS bits, placed in the DBI assembler, and sent to the CPU.

Circuit Objectives

Refer to FEMD 4-025 through 4-045.

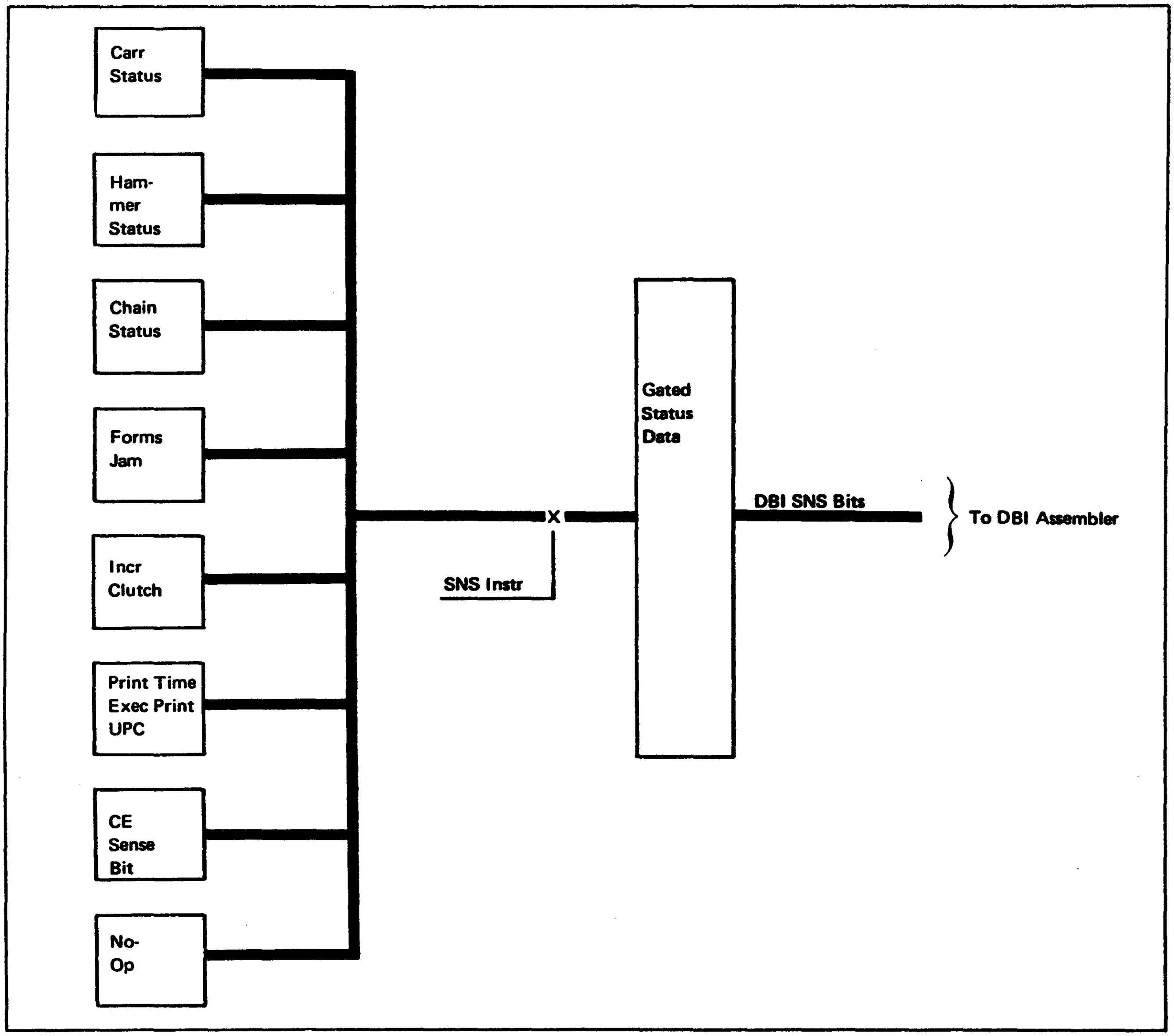


Figure 2-3. Sense Bit Assembler

DATA BUS IN ASSEMBLER

- The data bus in (DBI) assembler consists of eight latches. These latches are encoded to combine the data SNS bits that are sent to the CPU into separate data bytes.

- All data bytes sent to the CPU pass through the DBI assembler. For example:

1. Sense bits.
2. Data register bits.
3. LPDAR increment bits.
4. LPDAR preload bits.
5. Carriage line bits.
6. CC shift bits.

Circuit Objectives

See Figure 2-4. Data lines entering the DBI assembler are gated to set the appropriate flip latches. Upon activating the channel gate line, the channel DBI lines are made active.

Refer to FEMD 4-050 through 4-060.

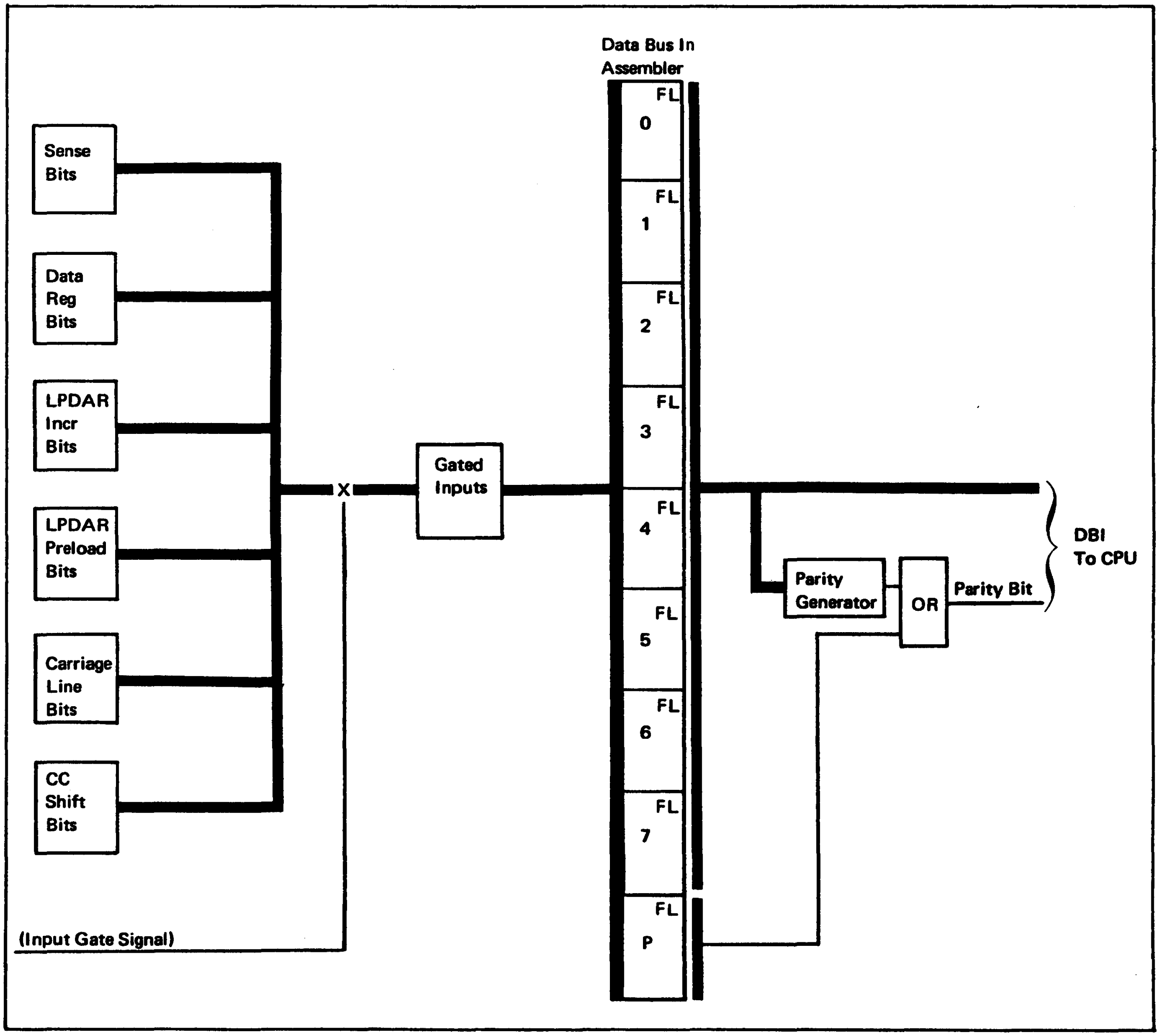


Figure 2-4. Data Bus In Assembler

CYCLE STEAL COUNTER

The cycle steal counter has two triggers that determine the proper print cycle steal latch (PC0 through PC3).

The print cycle steal counter ensures that the correct sequence of cycle steals is maintained. Print cycle steals occur in groups of 3, 2, or 1, depending on the attachment, detecting one of the following conditions:

1. Change of mechanical position.
2. Data found.
3. Data not found.
4. Print compare.
5. No print compare.

The triggers in the cycle steal counter keep track of which cycle steal is in process and which one should be next. The counter turns on the print cycle latches (PC0, PC1, PC2, and PC3). Refer to Figure 2-5.

Circuit Objectives

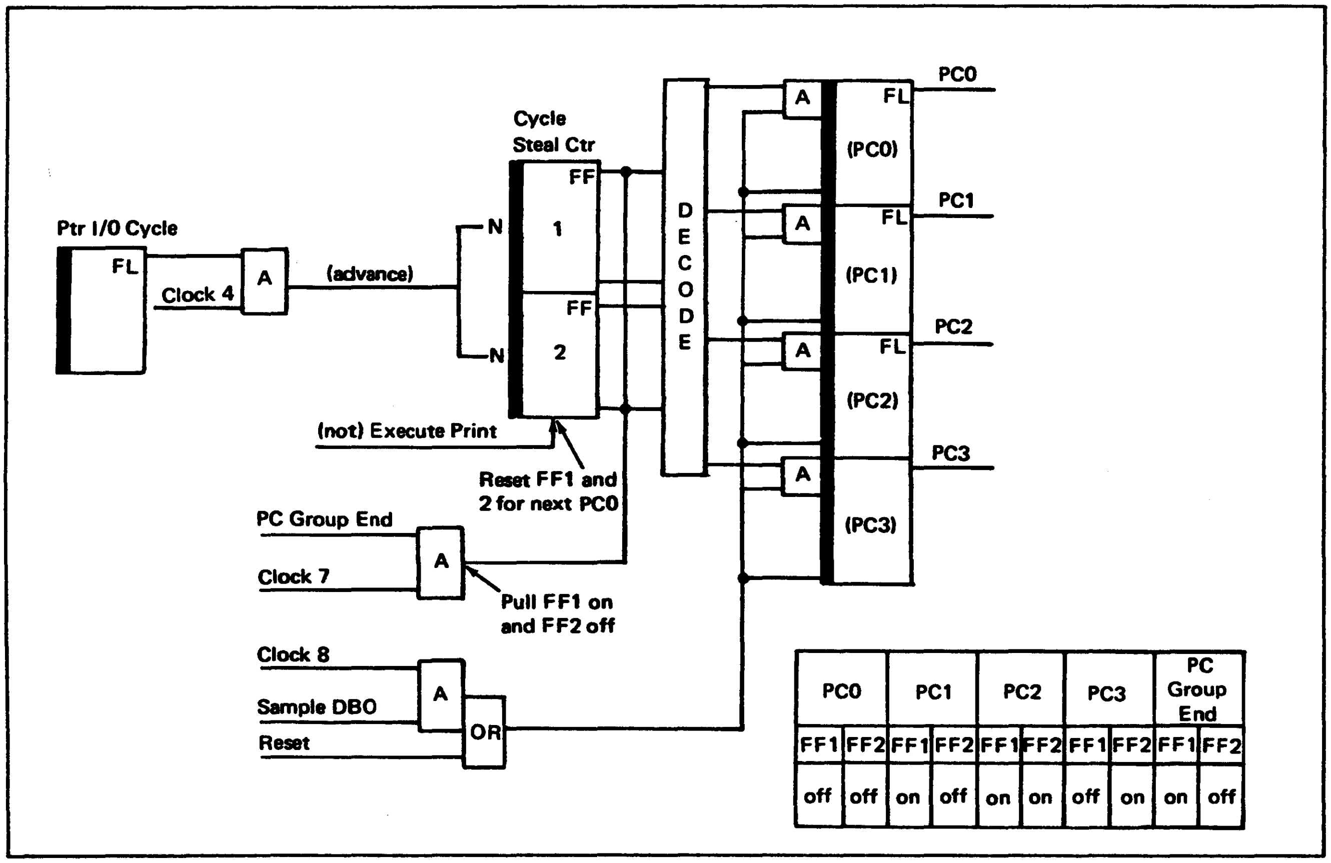
Both cycle steal triggers are reset off by (not) 'execute print' when (because of a change in M position) the next cycle steal taken will be PC0. During clock 4 of PC0, trigger 1 is turned on to ensure that the next cycle steal taken will be PC1. The same sequence is repeated for PC2 and PC3, if requested. At the end of a PC group, 'PC group end' is brought up at clock 7 to turn trigger 1 on and turn trigger 2 off. This starts the next group of cycle steals, starting with PC1. This sequence is repeated until the next change in mechanical position.

Refer to FEMD 4-070.

PRINT SUBSCAN COUNTER

- The print subscan counter is a three-position trigger ring that identifies the print subscan in process.

- A chain emitter pulse from the printer advances the print subscan counter.



PC0		PC1		PC2		PC3		PC Group End	
FF1	FF2	FF1	FF2	FF1	FF2	FF1	FF2	FF1	FF2
off	off	on	off	on	on	off	on	on	off

Figure 2-5. Cycle Steal Controls

The print operation is divided into four increment print scans (one in each of the four mechanical print positions). Each increment print scan has 50 print scans. Each print scan is further divided into three subscans. The print subscan trigger ring (Figure 2-6) identifies the subscan in process. Each ring position corresponds to one of the three subscans of a print scan. At the start of any subscan, the trigger ring identifies which of the first three print positions has a type-array character aligned with it. When the attachment receives a print subscan (PSS) emitter pulse from the printer, the subscan ring advances. The PSS pulses are generated from a magnetic emitter in conjunction with a drum with 144 equally-spaced slots around its circumference. A pulse is generated by each slot to identify the start of each subscan within the print line. An additional slot (145th) is located halfway between the 144th slot and the first slot. The 145th slot (home pulse) identifies the next emitter pulse as representing the first character on the chain. The first emitter pulse after the home pulse indicates that a character is aligned with print position one.

Circuit Objectives

Refer to FEMD 4-080. The PSS counter ring is advanced by '320 Ns Chain emitter' and (not) '300 micro S home gate'. The PSS counter ring is reset by 'reset CC'.

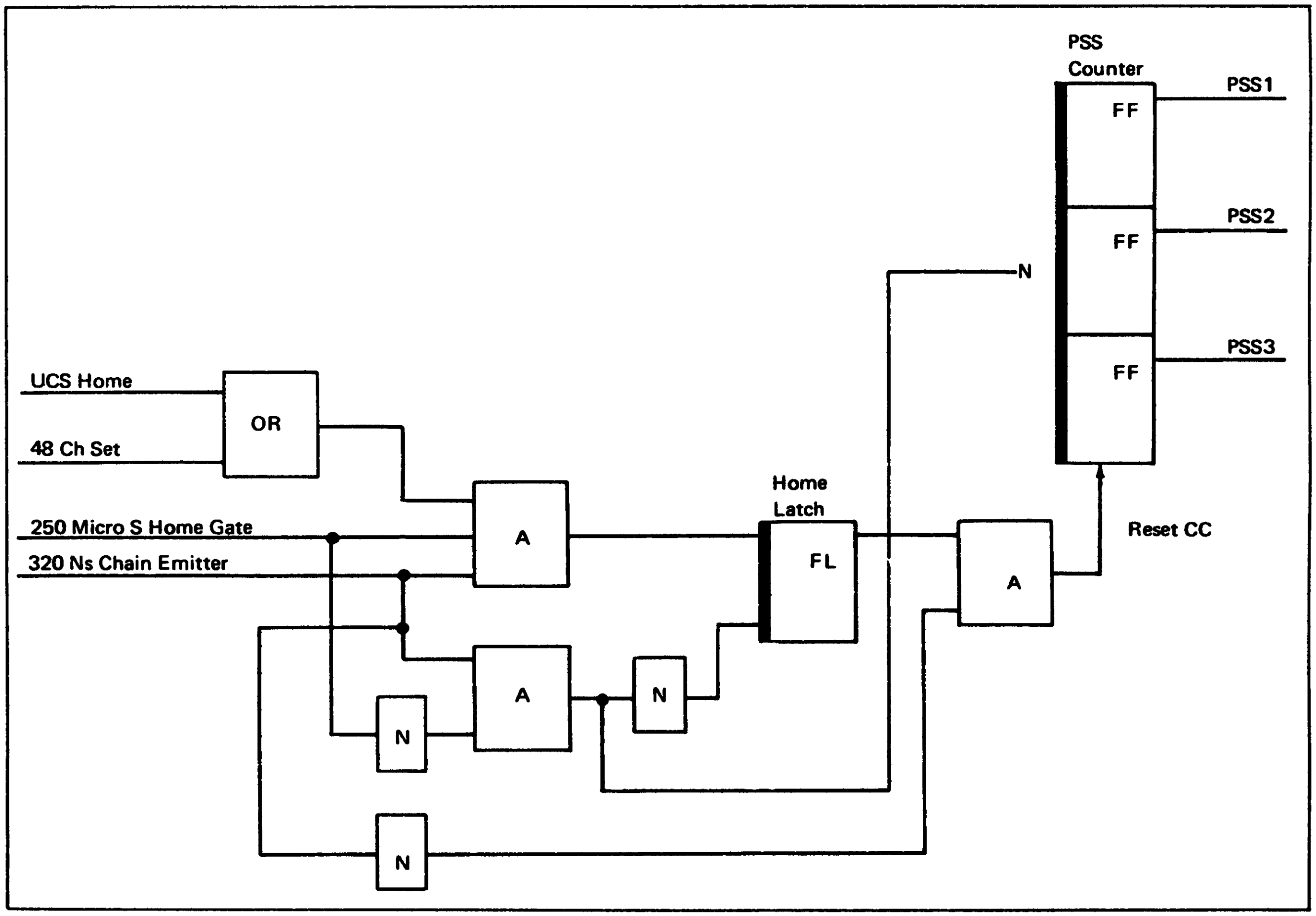


Figure 2-6. PSS Counter

MECHANICAL POSITION COUNTER

- The mechanical position counter (M counter) has six triggers.
- The triggers are advanced by the 'print start' singleshot at the completion of each mechanical print position change in the printer.
- M counter output is decoded to determine the mechanical position (M position) of the incrementer cam.
- M counter output is decoded along with the print subscan to determine the initialization value of the four-bit shift register (see "Chain Character Counter"), and develop hammer clock times.
- The M position is decoded to determine what bit structure is to be preloaded into the LPDAR in order to determine the first print position to be optioned for printing.

The mechanical position counter (M counter) keeps track of the mechanical position (M position) of the incrementer cam. Every time the M position (M1 through M4) of the incrementer cam is changed, the print start emitter generates a pulse to advance the M counter triggers (Figure 2-7).

Circuit Objectives

Refer to FEMD 4-085. The 100 line per minute machines print in one direction (M4-M1). The M counter is advanced by 'print start ss'. The output of the counter triggers is decoded into M positions.

Printing always starts in M4 on a 100 line per minute machine. At the end of the print line, the incrementer cam moves the hammer unit from M1 to M4 in preparation for the next print line.

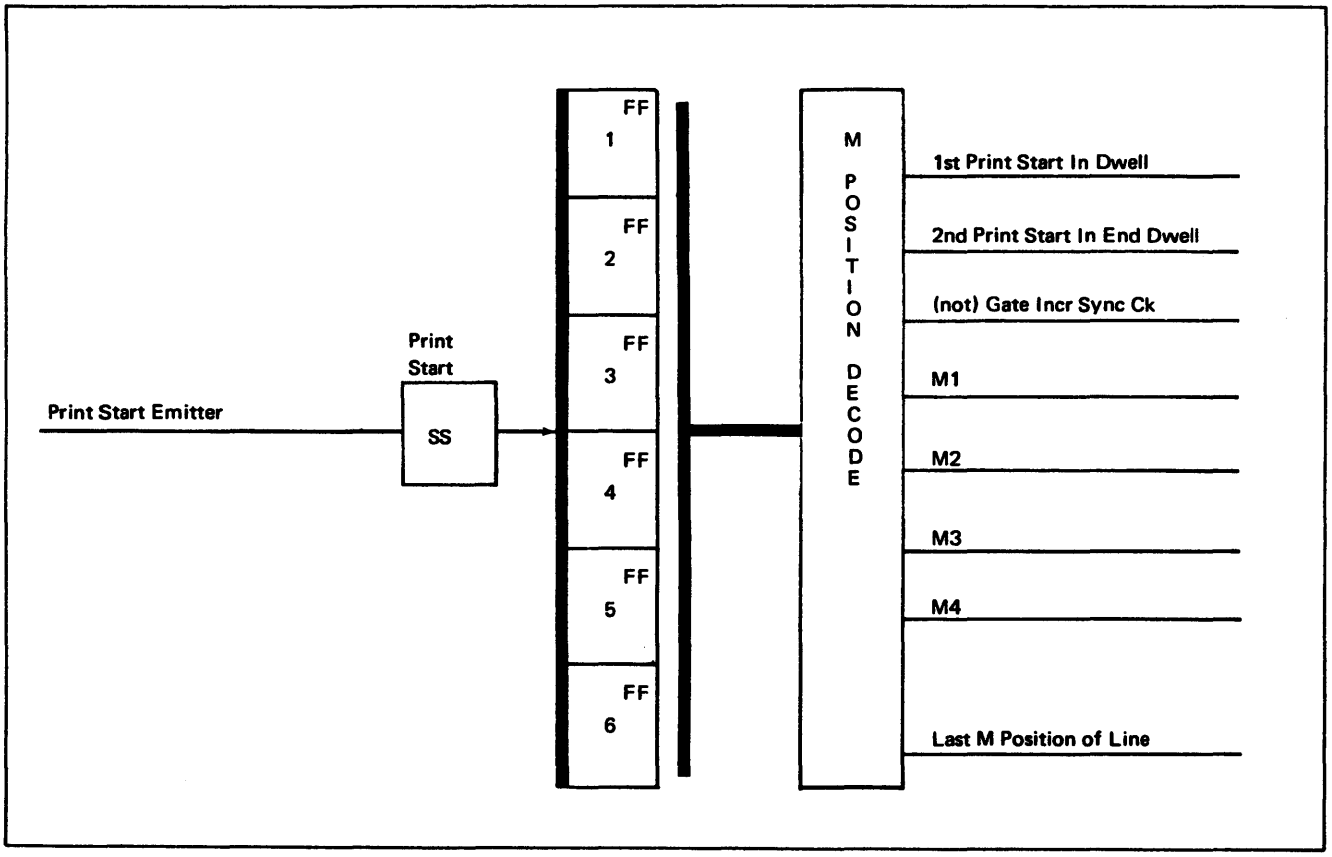


Figure 2-7. M Position Counter and Decode

SCAN COUNTER

Note: The following description of the scan counter is for the standard 48 character set only. For information about the scan counter for UCS machines, refer to "Chapter 4. Universal Character Set."

- The scan counter is a six-stage binary counter.
- Triggers are reset off after printing.
- A CC shift at the start of print subscan one (PSS1) advances the counter.
- The scan counter reaching 45, or 42 on a Model 3, decodes a signal to pick the carriage clutch.
- The scan counter reaching 50 signals the end of printing for that mechanical position.
- The scan counter reaching 57 picks the incrementer clutch. (A count of 57 is reached only for the first line of printing in the last M position on a single space operation or for every line in the last M position on a double or triple space operation.)

Scan counter triggers (Figure 2-8) are reset off after a print operation. During a print operation, the counter is advanced every PSS1 pulse. The outputs of this counter indicate when (during a print operation) the carriage operation is to be started, when the incrementer clutch is to be picked, and signal the end of printing.

Circuit Objectives

Refer to FEMD 4-090. The binary scan counter is advanced by activating 'cc shift' every PSS1 pulse with 'print time' active.

Scan counter outputs are decoded to develop pulses that control the carriage and incrementer clutches, and to determine the end of printing for that increment scan.

CHAIN CHARACTER COUNTER

The chain character counter (Figure 2-9), which consists of the following four units working together as a single functioning unit, indicates which chain character is properly aligned for printing:

1. Character counter,
2. 7-bit shift register,
3. 4-bit shift register, and
4. Adder.

Character Counter

The character counter (CC) is a seven-bit binary counter. It indicates which chain character is aligned with print position 1.

The character counter triggers are reset to their on state at home time (145th slot on the chain timing drum) by 'reset CC'.

The value in the character counter is used as a base for determining which chain characters are to be optioned during a print operation. The first CC shift pulse that follows a home pulse advances the counter by a count of one. This turns all the character count triggers off. (The character counter, which runs continuously, is advanced by a count of one each PSS1 time by the CC shift pulse.) Each time the character counter advances, its binary value equals the low order byte of the main storage chain image address; the addressed storage location contains the character that is *aligned with print position 1.*

7-Bit Shift Register, 4-Bit Shift Register, Adder

These three components act as a single sub-unit within the chain character counter. A character count increment preload value is derived by adding a decode of the M position to the PSS counter value. Each chain emitter pulse gates the character counter value into the 7-bit shift register and preloads the character count increment value into the 4-bit shift register. (This always occurs, whether or not a print operation is in process.) The preload value, when added to the 7-bit shift register, indicates which chain character is aligned with the first print position *to be optioned in a subscan.*

During print operations, the print cycle latch is turned on at the start of the first subscan. This gates seven shift pulses to the 7-bit shift register and to the 4-bit shift register. The low order positions of the 7-bit and 4-bit registers are shifted through the adder. The adder output is shifted, bit by bit (clock 1-7), back into the 7-bit shift register. At the end of this shift operation, the 7-bit shift register contains a factor equal to the low order byte of the address of the chain character that is aligned to print.

The value stored in the 7-bit shift register is transferred to the LPIAR at the *beginning* of the PC1s that follow (eleven in all for a subscan), the 'shift gate' latch allows seven shift pulses to the 7-bit and 4-bit shift registers. A value of 8 is loaded into the 4-bit shift register each time the 7-bit and 4-bit register values are added together, adding 8 to the value accumulated in the 7-bit register. This modifies the 7-bit register by +8 for each of the eleven PC1s, and results in every eighth character being addressed.

The value in the 7-bit shift register has no further use at the end of this print subscan. Its value will be re-established by means of the CC value at the start of the following subscan.

Circuit Objectives

Refer to FEMD 4-095.

The 7-bit shift register is modified: (1) before the first print cycle steal of a subscan to initialize the CC shift register, and (2) during every print cycle steal one (PC1). The shift register is initialized once and incremented by +8 eleven times (a total of twelve increments per subscan).

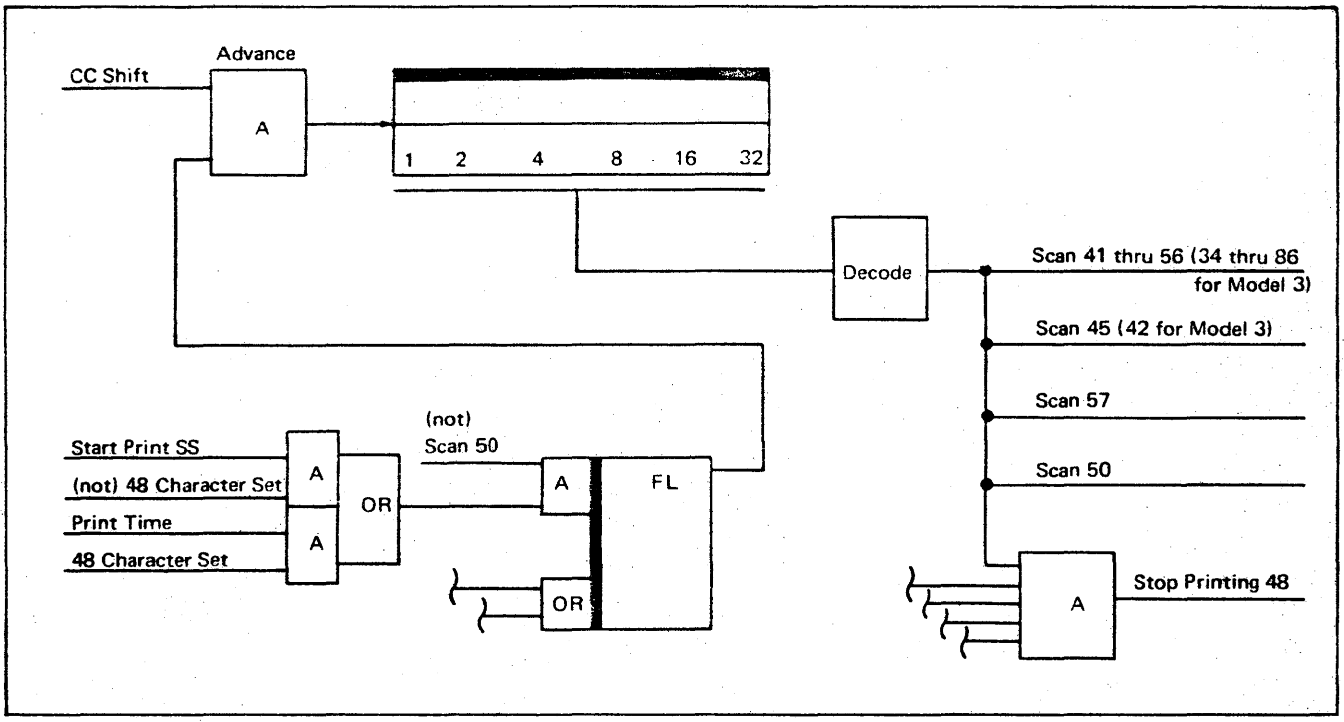


Figure 2-8. Scan Counter

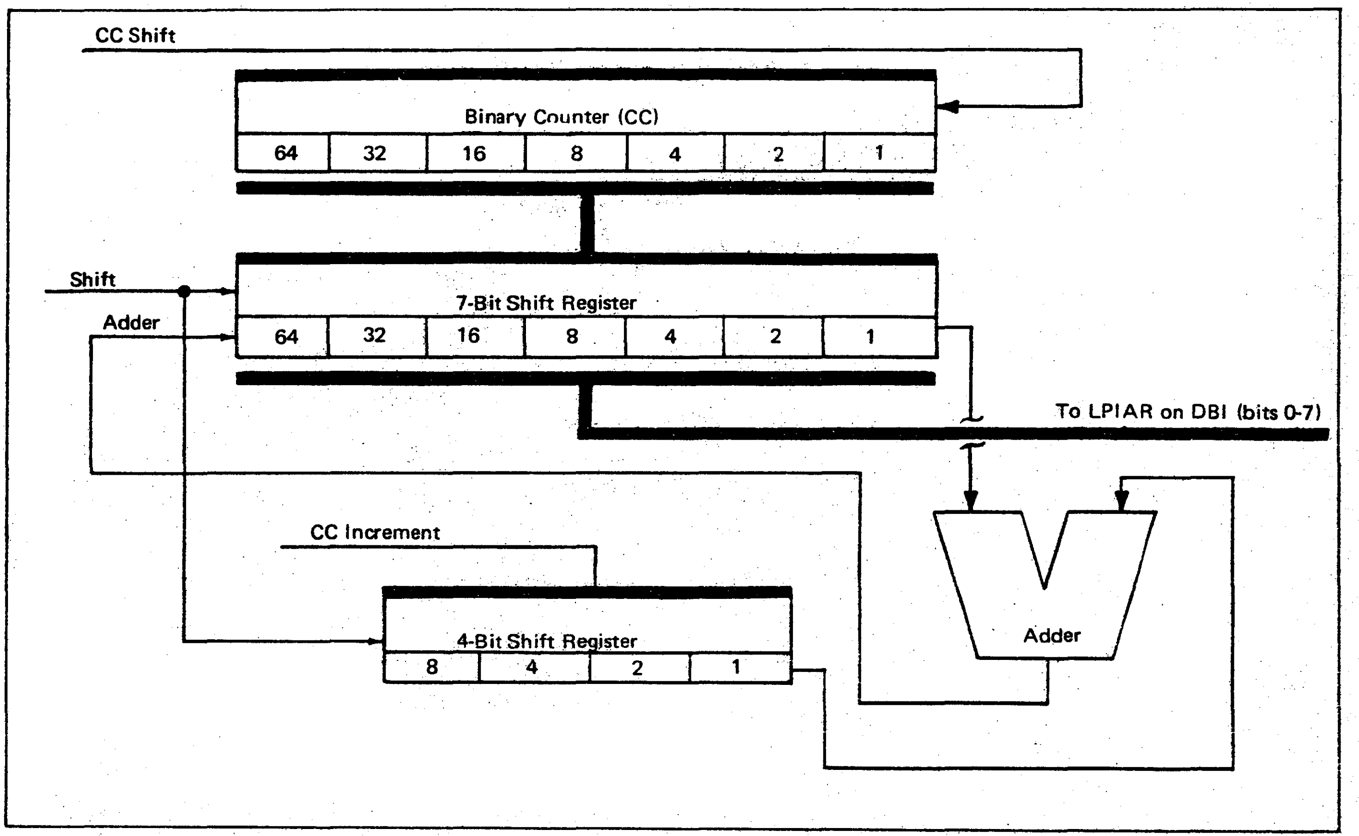


Figure 2-9. Chain Character Counter, and Modified Character Count

The character counter (CC) is advanced by each PSS1 pulse that activates 'cc shift'. The output of the character counter is parallel loaded into the 7-bit shift register with every 'chain em ss w-o home' pulse.

The advance pulse for the 7-bit register is a 'shift' pulse. During an initial modification, the 'shift' pulse is activated by 'ptr cyc req' ANDed with 'chan 1 early phase C', and (not) 'clock 0'. The shift pulse is activated once for each clock time (1-7) supplying seven shift pulses for each trigger in the register. During a modification in print cycle steal one, 'clock 0' and 'PC1' activate 'shift' instead of 'ptr cyc req', by turning on the 'shift gate' latch.

The 4-bit shift register is loaded with an increment value, which is derived from a decode of the mechanical position and the print subscan during an initializing operation. During an increment by +8, the eight trigger is turned on by 'clock 0' and 'PC1'. The same shift pulse that advances the 7-bit shift register advances the 4-bit shift register.

The adder adds the outputs of the two shift registers serially (bit by bit), low order bits first. Results of the adder are shifted, bit by bit, back into the 7-bit shift register. Zeros are entered into the adder from the 4-bit shift register into the last three positions to be added to the 7-bit register.

The added value of the two shift registers is shifted through the 7-bit register. The resulting byte of data is passed through the DBI assembler to be put on the channel to the LPIAR.

Overflow

Overflow may or may not occur:

1. Overflow occurs whenever the increment factor added to the position of the character on the chain (40-47 for a standard character set) results in the addressing of a character in the next set of characters on the chain. To be addressed correctly, this character must be referred to by its correct position on the chain. A 48-character set is repeated five times on a chain. Each of the 48 characters corresponds to one address in the LPIAR data area in main storage (address XX00 through XX2F hexadecimal).

   To prevent the addressing of a character in the next character set on the chain (the address would be greater than 47), a decode of 40 through 47 out of the 7-bit shift register turns on the 'potential overflow' latch.

   The low order positions of the 4-bit and 7-bit shift registers are shifted through the adder. The adder output is shifted, bit by bit (clock 1-7), back into the 7-bit shift register (any carries from the adder are placed in the 'carry' trigger and added the next shift pulse). At clock 4 time, the +8 trigger values of the 4-bit and 7-bit shift registers are present at the adder input and the result of the addition is present at the output of the adder. With the 'potential overflow' latch on, and no adder output, the 'overflow' trigger is gated on. Turning the 'overflow' trigger on holds the high order trigger (trigger 64) reset for the next four shift pulses. This forces zeros to be entered in the four high order positions of the 7-bit register. For example, assume a 48-character set with the 7-bit register containing a value of 45 and the 4-bit register incrementing by +8:

```
0101101   (45)
   1000   (+8)
0110101   (53)
  ↑
  └────────── (No adder output causes overflow
              trigger to be set.)
```

The 53 causes an overflow condition because the highest position addressed in a 48-character set is 47 (0 is the first character count on the chain). The 'overflow' trigger is set, in this case, forcing zeros to be set into the four high order positions of the 7-bit shift register.

```
0101101   (45)
   1000   (+8)
───────
0000101   (5)
```

The 5 causes the fifth position of the next set of characters on the chain to be addressed.

2. Overflow does not occur if the increment factor added to the position of the character on the chain (40 through 47 for a standard character set) results in the addressing of a character in the present character set on the chain. To prevent addressing a character in the next character set, a decode of 40 through 47 out of the 7-bit shift register turns on the 'potential overflow' latch. The low order positions of the 4-bit and 7-bit shift registers are shifted through the adder. The adder output is shifted, bit by bit (clock 1-7), back into the 7-bit shift register (any carries from the adder are placed in the 'carry' trigger and added during the next shift pulse). At clock 4 time, the 8 trigger of the 4-bit shift register and the 8 trigger of of the 7-bit shift register values are present at the adder input and the result of the addition is present at the output of the adder. With the 'potential overflow' latch on and an adder output, the 'overflow' trigger is not gated on. This allows the updated value to shift into the 7-bit shift register from the adder.

For example, assume a 48-character set with the 7-bit shift register containing a value of 45 and the 4-bit shift register incrementing by 2: (PSS counter and M counter give initialization factor to 4-bit shift register).

```
0101101   (45)
0000010   (+2)
───────
0101111   (47)
   ↑
   └────────── (Adder output causes 'overflow'
               trigger not to be set.)
```

The 47 will not cause an overflow. The 'overflow' trigger will not be set. The true value of the 7-bit shift register and the 4-bit shift register will be added in the adder and shifted into the 7-bit shift register.

HAMMER CLOCK

- The hammer clock is started by a chain emitter pulse.
- The hammer clock furnishes timing pulses to fire the eleven hammers that are optioned during a subscan.
- The hammer clock is preloaded in a manner that compensates for the variable-length mechanical delay in hammer-to-chain character alignment.

The hammer clock (Figure 2-10) is a modified binary counter. The clock, which runs only when it is being used, is preloaded and started by a chain emitter pulse. The clock then runs for 11 cycles (the duration of the subscan), optioning one hammer each clock cycle.

The hammer clock is preloaded and started to one of four hammer clock times (clock 1, 2, 3, or 4) from a decode of the PSS counter and M position counter. This happens because each hammer clock time is 7.75 microseconds long, or 4.85 microseconds on Model 3, which equals 0.001 inch of print chain movement. When a chain emitter pulse is received to start a subscan in the attachment, the character optioned to print may be 0.001 inch, 0.002 inch, or 0.003 inch from being aligned. Therefore, the hammer clock must be preloaded to one of the four possible starting points (Figure 2-10).

Each clock cycle consists of four hammer clock times.

Hammer Clock 1 Time

1. Develops sample echo check pulses to sample whether or not a hammer driver in the printer was fired.
2. Gates writing into the hammer check LSR, if this hammer driver being serviced is fired.
3. Clears one of four LSR words at the beginning of subscan 1, of print scan 1.

Hammer Clock 2 Time

1. Clears one of four LSR words at the beginning of subscan 1, of print scan 1.
2. Gates readout of the Hammer Check LSR during reset time on Model 3 only. This indicates whether the hammer should be reset in this scan or not.

Hammer Clock 3 Time

1. Develops a pulse to load the hammer address register.
2. Turns off the 'lockout' trigger to allow print cycle . steals.
3. Clears one of four LSR words at the beginning of subscan 1, of print scan 1.

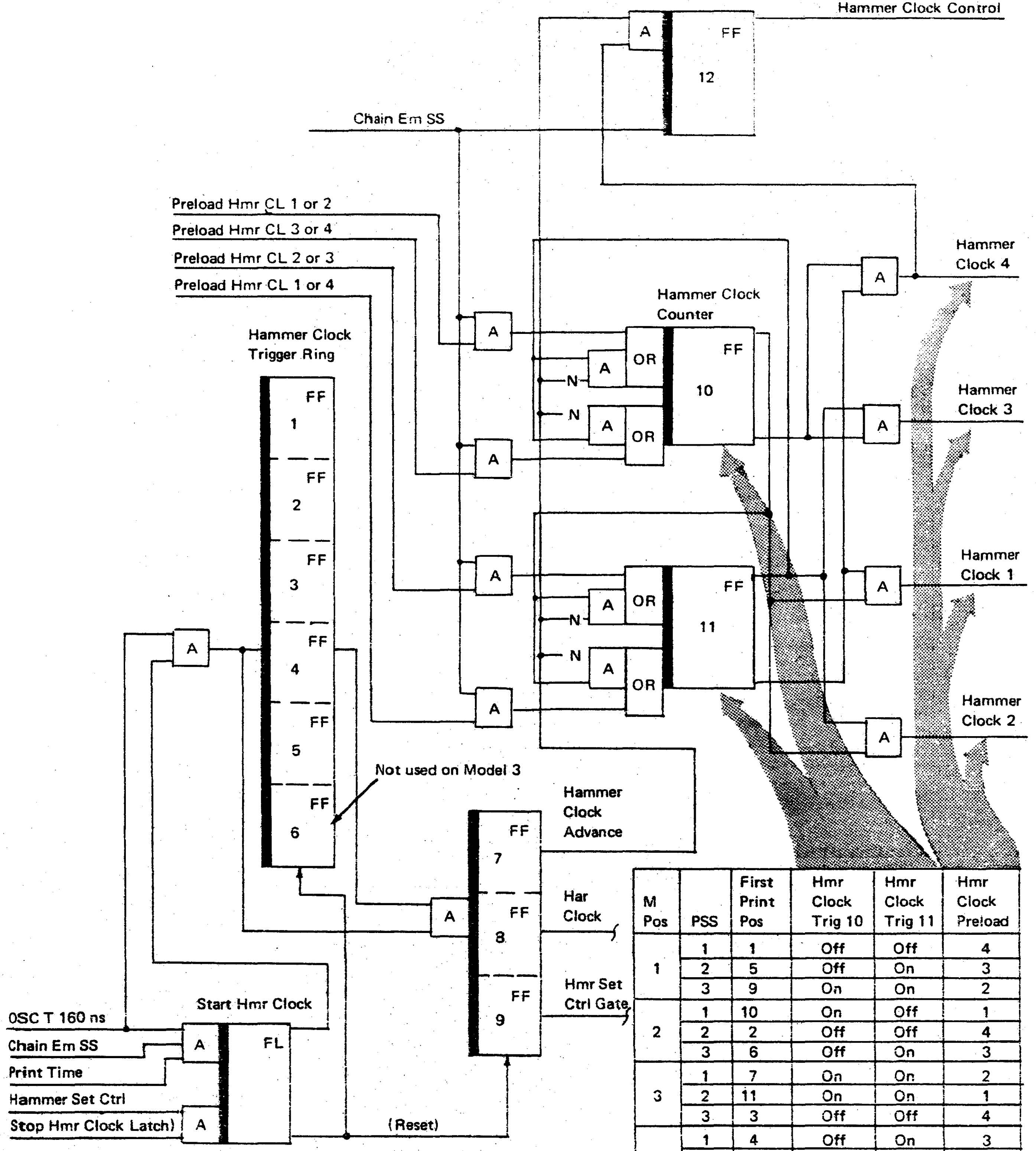
Hammer Clock 4 Time

1. Gates readout of the hammer check LSR. This tells whether or not the hammer driver being serviced was fired on the previous subscan.
2. Clears one of the four LSR words at the start of subscan 1, print scan 1.
3. Develops hammer set control pulses. The hammer set control pulse is the actual time that the hammer driver is optioned to be fired. Eleven of these pulses are generated each print subscan (on a 132 print position printer). Therefore, during each print scan (that is, during three consecutive subscans), 33 hammer set control pulses are generated and all 33 hammers are optioned to be fired.

Circuit Objectives

Refer to FEMD 4-100.

With the 'print time' trigger on and with the 'chain em ss w-o home' line ANDed with 'osc T 160 ns', the 'start hmr clock' latch is turned on. At the same time, the 'chain em ss w-o home' line preloads hammer clock triggers 10 and 11 to the value decoded from the PSS and the M position counter. The print chain and the hammer clock are now synchronized. The hammer clock runs for 11 cycles (1 subscan). When the last hammer driver is optioned to print, the 'hammer set control' pulse along with 'first 12 prt pos' line turns on the 'stop hmr clock' latch. This resets the 'start hmr clock' latch, and stops the hammer clock.



M Pos	PSS	First Print Pos	Hmr Clock Trig 10	Hmr Clock Trig 11	Hmr Clock Preload
1	1	1	Off	Off	4
	2	5	Off	On	3
	3	9	On	On	2
2	1	10	On	Off	1
	2	2	Off	Off	4
	3	6	Off	On	3
3	1	7	On	On	2
	2	11	On	On	1
	3	3	Off	Off	4
4	1	4	Off	On	3
	2	8	On	On	2
	3	12	On	Off	1

Figure 2-10. Hammer Clock

HAMMER ADDRESS REGISTER

- The hammer address register consists of six flip latches which store the address of the hammer to be fired.
- The hammer address is decoded into the corresponding X and Y address lines.
- The addressed X and Y lines select the hammer latch in the printer and the hammer check LSR in the attachment.

The hammer address register (Figure 2-11) stores the address of the next print position to be optioned for printing. This address is decoded to address the hammer just optioned.

The address is decoded into one X address line and one Y address line. Output from the addressed lines is sent (1) to the printer to select the hammer to be fired, and (2) to the hammer check LSR to set a latch corresponding to the hammer to be fired.

Circuit Objectives

Refer to FEMD 4-110.

Activating 'load HAR' loads the contents of the data register into the hammer address register

The address is decoded and the correct hammer X and hammer Y address lines are made active.

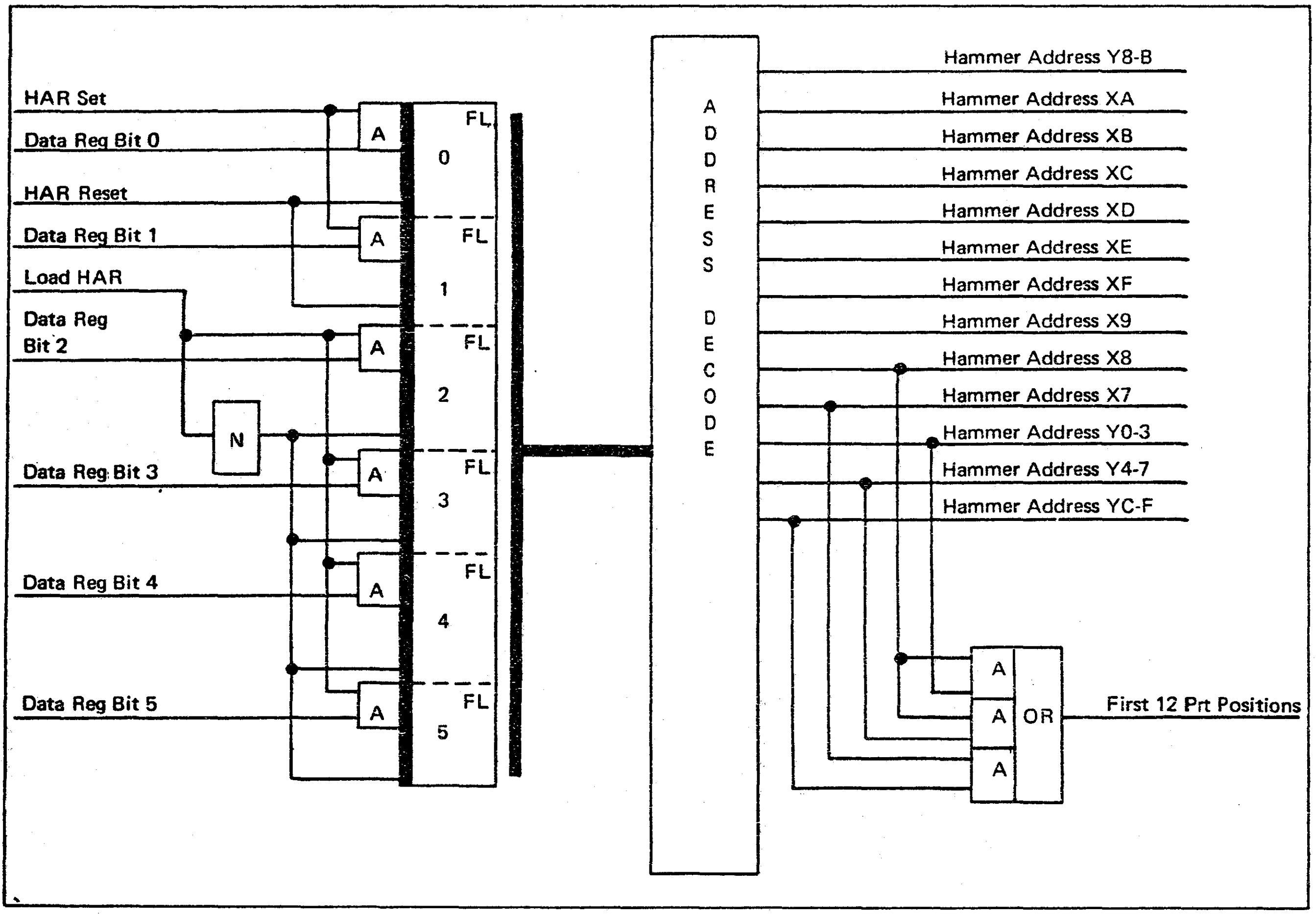


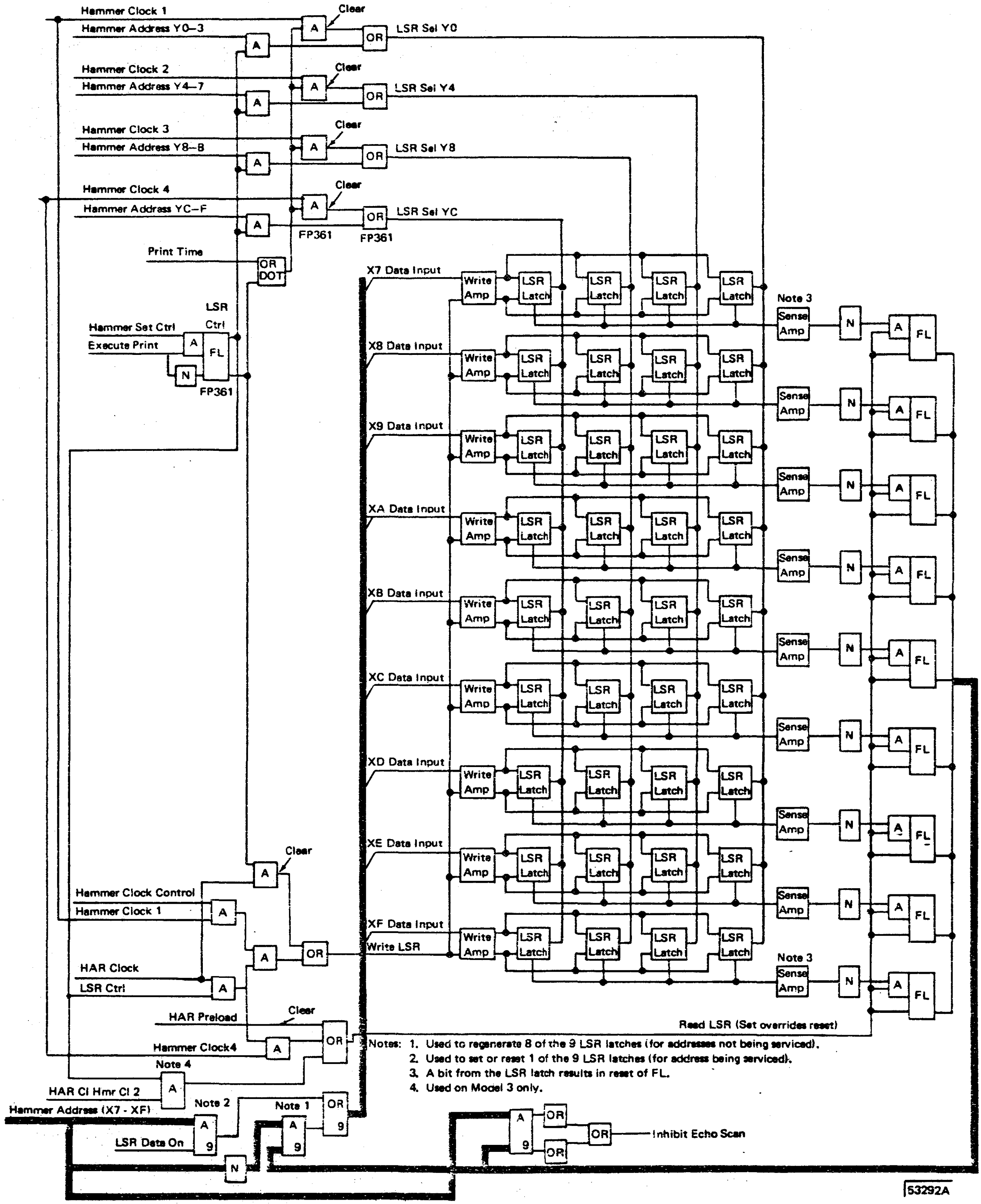
Figure 2-11. Hammer Address Register

HAMMER CHECK LSR

- The hammer check LSR consists of 36 LSR latches and 9 flip latches.
- Three LSR latches are not used. Each remaining LSR latch indicates whether or not a corresponding hammer has fired.
- The flip latches hold 9 LSR latch outputs that are used for regenerating the LSR.
- The LSR latches are arranged in a 4 x 9 matrix.
- The LSR output ('inhibit echo scan') prevents the checking of a hammer during a scan in which the hammer has been reset.
- The hammer address register and decoded address lines select the latch that corresponds to the hammer being serviced.
- The LSR is cleared at the beginning of each mechanical position.

Until the hammer driver has been reset, the hammer check LSR (Figure 2-12) indicates that the hammer driver was turned on. When a hammer driver is fired during a print scan (print scan X), the attachment tries to determine, during the next print scan (print scan X+1), whether or not the hammer driver was turned off. However, during this cycle, the hammer driver is turning off and the echo circuit output is undefined because driver turn-off is relatively slow. Therefore, checking must be inhibited during this scan (print scan X+1). Inhibiting this check is the hammer check LSR function.

The hammer check LSR indicates that a hammer driver was turned off during print scan X+1. At print scan X+2 (after the hammer driver has had time to turn off) the hammer driver is checked to determine whether or not it is off.



Notes: 1. Used to regenerate 8 of the 9 LSR latches (for addresses not being serviced).
2. Used to set or reset 1 of the 9 LSR latches (for address being serviced).
3. A bit from the LSR latch results in reset of FL.
4. Used on Model 3 only.

Figure 2-12. Hammer Check LSR

Circuit Objectives

Refer to FEMD 4-120 and 4-125.

The LSR latches are grouped in a 4 x 9 matrix. This provides four, 9-position LSR words made of any combination of LSR latches (cells) being on or off. An LSR word can be written or read (Figure 2-12).

When writing an LSR latch:

1. One of the four active hammer address Y lines (LSR select Y lines) becoming active selects one of the four 9-celled LSR words.
2. Any one of the nine active hammer address X (X data input) lines becoming active selects one of nine latches corresponding to the hammer being serviced.
3. A write LSR pulse sets the gated latches. A write pulse serves all nine cells, but only the addressed cell is changed.

When reading the LSR:

1. One of the four hammer address Y lines (LSR select Y lines) becoming active selects the LSR word and gates its output to the 9 flip latches.
2. A read pulse sets the flip latches.

When clearing the LSR:

1. A read pulse with no Y select pulse resets the flip latches. This degates any data input lines.
2. The hammer clock control trigger is off and print time is active.
3. A hammer clock cycle gates each one of the Y select lines. With 'print time' on and the 'LSR ctrl' latch off, a write pulse in each of four hammer clock cycles resets all the LSR latches.

The effective output of the hammer check LSR is the line, 'inhibit echo scan'. With this line active, a hammer driver is not checked on the scan in which it is reset.

CARRIAGE SPACE-SKIP REGISTER

- The carriage space-skip register consists of eight flip latches.
- It tells the carriage how many lines to space or the line to which the carriage should skip.
- The eight-position register is set to the control field of an SIO instruction.
- Outputs are compared to the space counter to stop the printer carriage on a space operation.
- Outputs are compared to the line counter to stop the printer carriage on a skip operation.

The carriage space-skip register consists of eight flip latches (Figure 2-13). Seven latches are for data, and the eighth indicates a carriage data parity error at the DBO register. The first seven latches store the control field for either an SIO carriage space instruction or an SIO carriage skip instruction. This tells the carriage how many lines to space or skip.

Circuit Objectives

Refer to FEMD 4-210.

During a channel I-R cycle of a start I/O instruction, the carriage space-skip register is set at 'DBO clock 5' time. It is set to the contents of the DBO register, which contains the control field of the instruction.

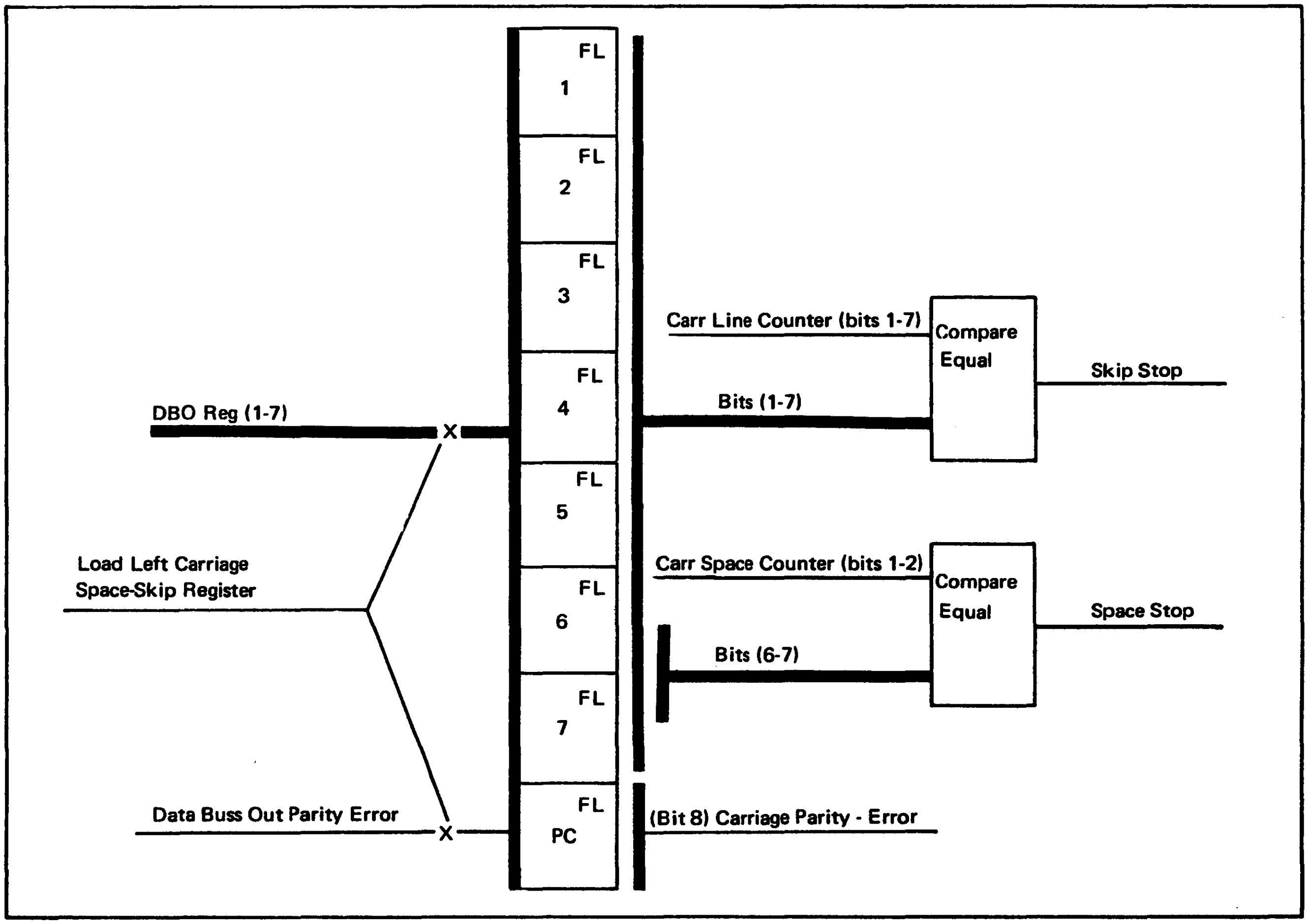

FL 1
FL 2
FL 3
FL 4
FL 5
FL 6
FL 7
FL PC
DBO Reg (1-7)
Load Left Carriage Space-Skip Register
Data Buss Out Parity Error
Carr Line Counter (bits 1-7)
Bits (1-7)
Compare Equal
Skip Stop
Carr Space Counter (bits 1-2)
Bits (6-7)
Compare Equal
Space Stop
(Bit 8) Carriage Parity - Error

Figure 2-13. Carriage Space-Skip Register

Space Operation

On a space operation, bits six and seven can be set. Bit 7 and not bit 6 equals single space. Bit 6 and not bit 7 equals a double space. Bit 6 and 7 equal triple space. Not bit 6 and not bit 7 equal zero space. A control code of four (any bit other than bit 6 or 7) is permitted, but results in a space zero operation. Bit 6 and 7 output is compared to the space counter to develop space stop, which, in turn, degates the carriage clutch.

Skip Operation

On a skip operation, bits 1 through 7 can be set to specify the binary equivalent of any line, 1 through 112. The carriage skips until the specified line is reached. The outputs of bits 1 through 7 are compared with the line counter to develop skip stop, which, in turn, degates the carriage clutch.

CARRIAGE FORMS LENGTH REGISTER

- The carriage forms length register consists of eight flip latches.
- It tells the carriage the length of the forms to be printed.
- The eight-position register is loaded with data from the storage location specified by the address portion of a load I/O instruction.

The carriage forms length register consists of eight flip latches (Figure 2-14), seven for data and one to indicate a forms data parity error at the DBO register. The first seven latches have stored in them the forms length, from the storage location specified in the address portion of a load I/O instruction. This tells the carriage the length of the forms being used.

Circuit Objectives

Refer to FEMD 4-215.

At 'sample DBO cl 5' time, during the E-B2 cycle of an LIO instruction, the carriage forms length register is loaded with the contents of the DBO register. The output is compared to the line counter on a manual restore operation. When they compare equal, the next verified carriage emitter pulse degates the carriage clutch and sets the line counter to one. The data in the forms length register remains a constant value until altered by another load I/O instruction.

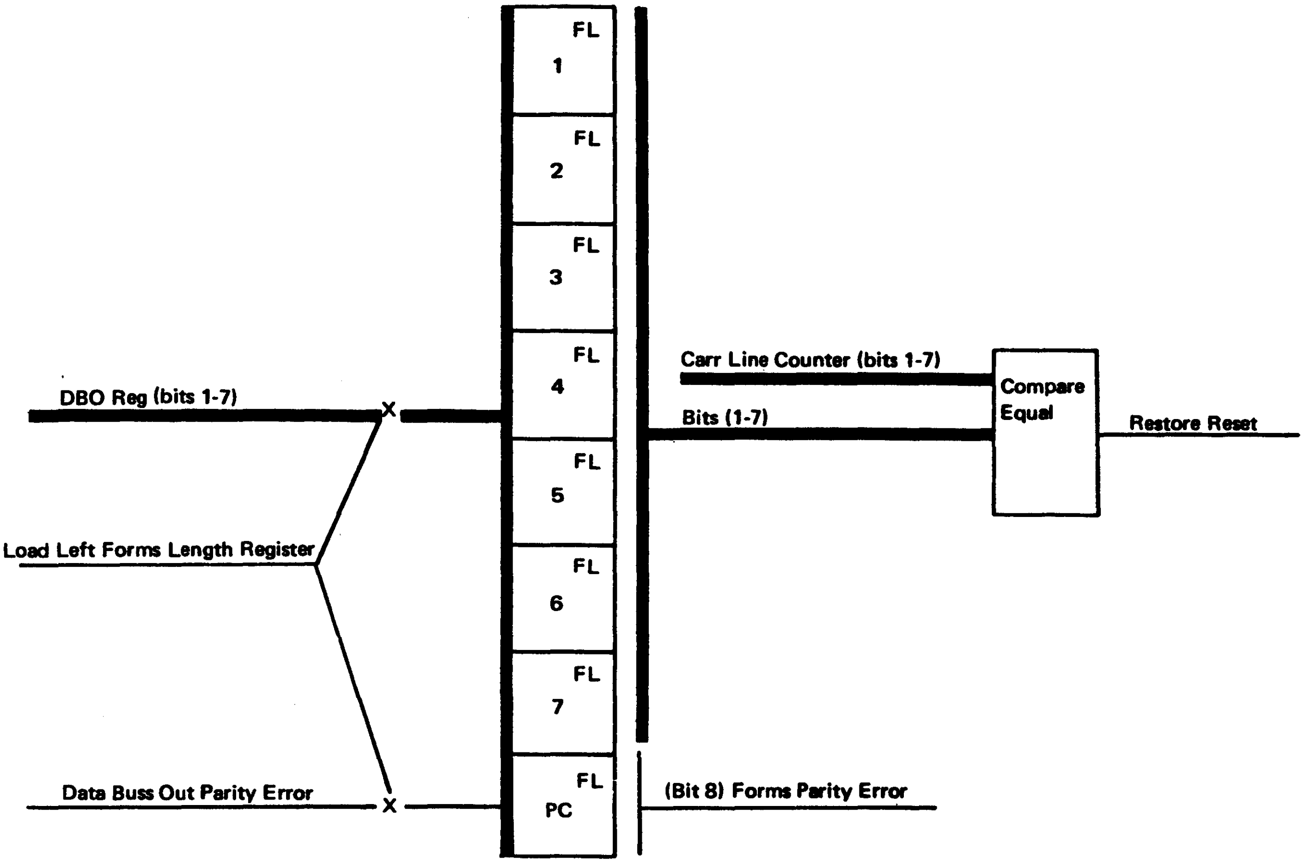

FL 1
FL 2
FL 3
FL 4
FL 5
FL 6
FL 7
FL PC
DBO Reg (bits 1-7)
Load Left Forms Length Register
Data Buss Out Parity Error
Carr Line Counter (bits 1-7)
Bits (1-7)
Compare Equal
Restore Reset
(Bit 8) Forms Parity Error

Figure 2-14. Carriage Forms Length Register

CARRIAGE LINE COUNTER

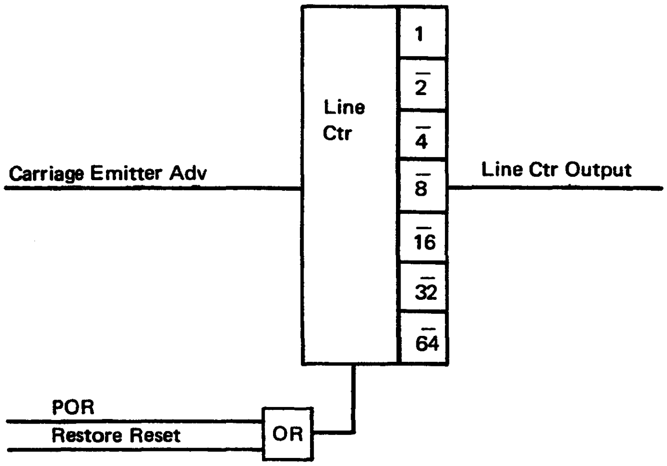
- The line counter consists of seven binary triggers.
- The counter accumulates the number of lines printed, spaced, and skipped.
- The counter triggers are reset on.
- The counter advances a value of one for every carriage emitter pulse.

The line counter (Figure 2-15), a 7-position modified binary counter, accumulates the number of carriage lines spaced or skipped on each form. The counter contents are compared to see if they are equal to the carriage space-skip register on a skip operation, or equal to the forms length register on a manual restore operation, to stop the carriage. When the contents of the line counter equals that of the forms length register, the next verified emitter pulse resets the line counter to one.

Circuit Objectives

Refer to FEMD 4-220.

The line counter triggers are all reset on (Figure 2-15). This gives an output decode of one. The counter is advanced by one as each carriage emitter pulse is sensed.



Line Counter Decode

Note 2 → Bit 1

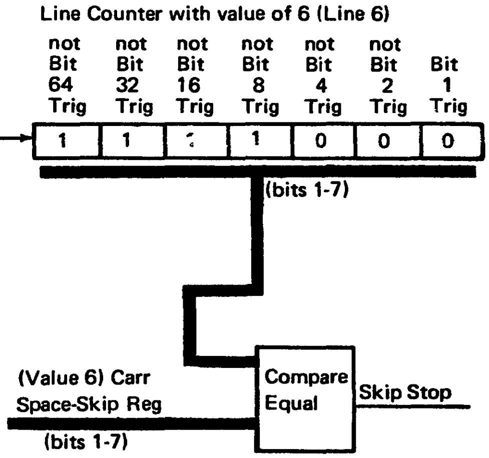
Note 1 → 1

Print Line # (value in counter) → 1

Trig On = 1
Trig Off = 0

Note 3 → 112

Line Counter Trigger Name	not Bit 64	not Bit 32	not Bit 16	not Bit 8	not Bit 4	not Bit 2	Bit 1
1	1	1	1	1	1	1	1
2	1	1	1	1	1	0	0
3	1	1	1	1	1	0	1
4	1	1	1	1	0	1	0
5	1	1	1	1	0	1	1
6	1	1	1	1	0	0	0
7	1	1	1	1	0	0	1
8	1	1	1	0	1	1	0
9	1	1	1	0	1	1	1
10	1	1	1	0	1	0	0
11	1	1	1	0	1	0	1
102	0	0	1	1	0	0	0
103	0	0	1	1	0	0	1
104	0	0	1	0	1	1	0
105	0	0	1	0	1	1	1
106	0	0	1	0	1	0	0
107	0	0	1	0	1	0	1
108	0	0	1	0	0	1	0
109	0	0	1	0	0	1	1
110	0	0	1	0	0	0	0
111	0	0	0	1	0	0	1
112	0	0	0	1	1	1	0
Binary Value with trigger on	not 64	not 32	not 16	not 8	not 4	not 2	1



Note 1. All triggers reset on (line 1).
Note 2. All triggers except bit one trigger represent a no bit condition when on.
Note 3. Form length over 112 not used.

Figure 2-15. Carriage Line Counter

CARRIAGE SPACE COUNTER

- The carriage space counter consists of two binary triggers.
- The counter accumulates the number of lines spaced.

The carriage space counter accumulates a total of the lines spaced on a carriage space operation. The two-position counter is reset on (a value of 3) when the carriage stops after any carriage operation. On a space operation (space 1, 2, 3), the counter advances by a count of one for each carriage emitter pulse. As the counter is advanced it is compared to the carriage space-skip register (spaces to be skipped). When equal, the space stop line becomes active, degating the carriage clutch (Figure 2-16).

Circuit Objectives

Refer to FEMD 5-215.

The counter is reset on at the end of any carriage operation. The carriage emitter advances the counter by a count of one as each line is spaced. On a space operation, the space counter outputs are ANDed with the carriage space-skip register bits 6 and 7 to generate a carriage stop.

SPACE CHECK COUNTER

- The space check counter consists of two binary triggers.
- The counter is reset on at the end of a carriage operation.
- The counter is used to detect a carriage runaway condition.
- The counter records how many times the first line of a form is passed in one carriage operation.

The space check counter is used to detect a carriage runaway condition (Figure 2-17). Every time line 1 is sensed and the carriage clutch remains picked, the counter advances one count. Two advances cause a carriage space check indication. For example, if the forms length is indicated in the forms length register as 40 lines and an SIO is to skip to line 50, a carriage runaway condition would result because of the carriage searching continuously for line 50. The space check counter prevents this because each time line 1 of a form is sensed, the space check counter advances by one. If the counter advances twice (line 1 passes twice in one carriage operation), the 'space count' latch is turned on. The 'space count' latch going on resets the 'carriage space' and the 'carriage skip' latches. This degates the carriage clutch, stops carriage motion, stops the carriage runaway condition, and sets the carriage space check SNS bit.

Circuit Objectives

Refer to FEMD 5-215.

The 'carr cl' line going inactive from a previous operation sets the space check counter. As 'L line 1' is activated (passing line one on a form), the counter is advanced one. If 'L line 1' is activated a second time and the 'carr cl' line remained active, the space counter trigger #2 turns off. Trigger #2 output ANDed with 'carr cl' turns on the 'space count' latch. This resets the 'space' latch, the 'skip' latch, and sets the carriage space check SNS bit.

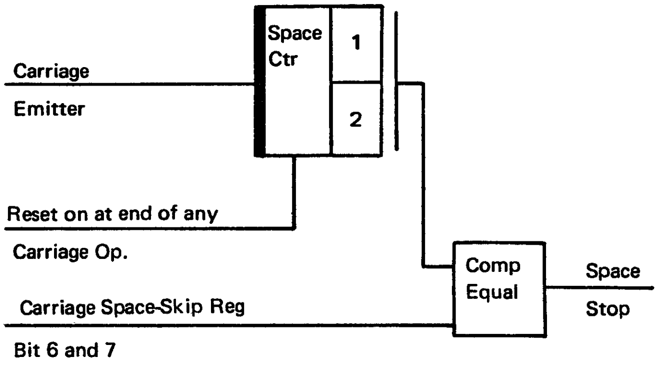

Space Ctr
1
2
Carriage Emitter
Reset on at end of any Carriage Op.
Comp Equal
Space Stop
Carriage Space-Skip Reg Bit 6 and 7

Figure 2-16. Carriage Space Counter

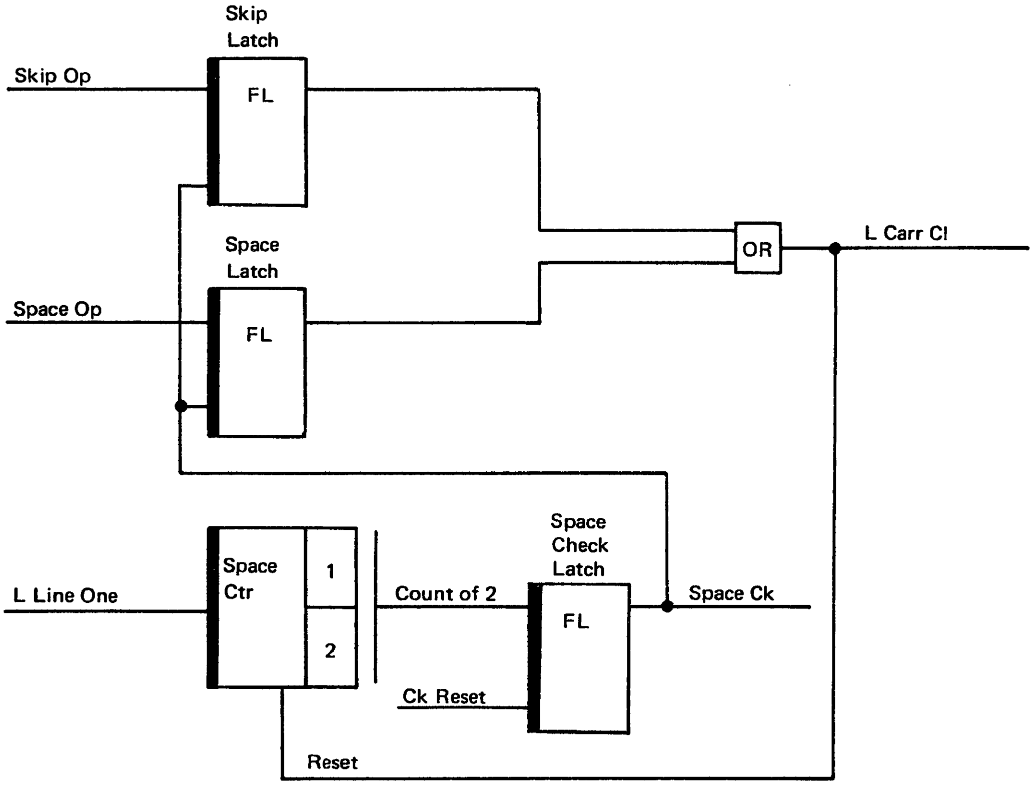


Figure 2-17. Space Check Latch

CARRIAGE OSCILLATOR

- The oscillator converts a 160 nanosecond input to a 49.92 microsecond output.

- The outputs:

  1. Drive the emitter generate counter and carriage moving counter.
  2. Step the home gate singleshot reset ring.

The carriage oscillator converts the 160 ns oscillator pulses from the CPU to 49.92 us. pulses, and uses them to drive the emitter generate counter, drive the carriage moving counter, and step the reset ring for the 'home gate' singleshot (Figure 2-18).

The carriage oscillator consists of 12 binary triggers stepped as a modified binary counter, 4 AND circuits, 1 latch, and 1 inverter. The oscillator runs continually with system power up (free running).

Circuit Objectives

Refer to FEMD 4-220.

The line 'osc T 160 ns' from CPU is fed ungated to the carriage oscillator counter. The counter runs continuously and gives a 49.92 us. output line called 'osc T 49.92 us.'.

CARRIAGE MOVING COUNTER

- The carriage moving counter consists of nine binary triggers.

- It prevents printing for 12 ms after a carriage operation.

- It degates any false emitter pulse (noise) for approximately 5 ms after the carriage clutch is picked.

- It is used for every carriage operation (space, skip, restore).

The carriage moving counter is a 9-position modified binary counter (Figure 2-19). All triggers are reset on. The counter starts when the carriage clutch is picked. The counter degates any carriage emitter pulse from being sensed by the emitter generate circuits for approximately 5 ms after the carriage clutch is picked. It is then reset by a verified emitter pulse and starts to count out. The verified emitter pulse is gated to the carriage controls. If the counter is allowed to continue counting (no emitter pulse to reset it because the carriage clutch has latched up), the counter continues counting for approximately 12 ms and resets the 'carriage moving' latch. This time allows the forms to settle down before printing the next line.

Circuit Objectives

Refer to FEMD 4-220.

The counter triggers (Figure 2-19) are reset on by 'start reset-sys ck reset', or 'carriage moving', or 'verified carr em', ANDed with 'reset control'. The counter is stepped by the carriage 'osc T 49.92 us.' pulse ANDed with 'carriage moving'. It counts to 5 ms and turns on the 'accept emitter' latch. If there is an emitter pulse (carriage moving from one line to another), the counter is reset by 'verified carr em'. If the carriage clutch latches up, the counter continues until trigger #14 is turned off (12 ms). Trigger #14 off ANDed with 'verified carr em' inactive turns off the 'carriage moving' latch. The 'carriage moving' line becoming inactive resets the carriage moving counter.

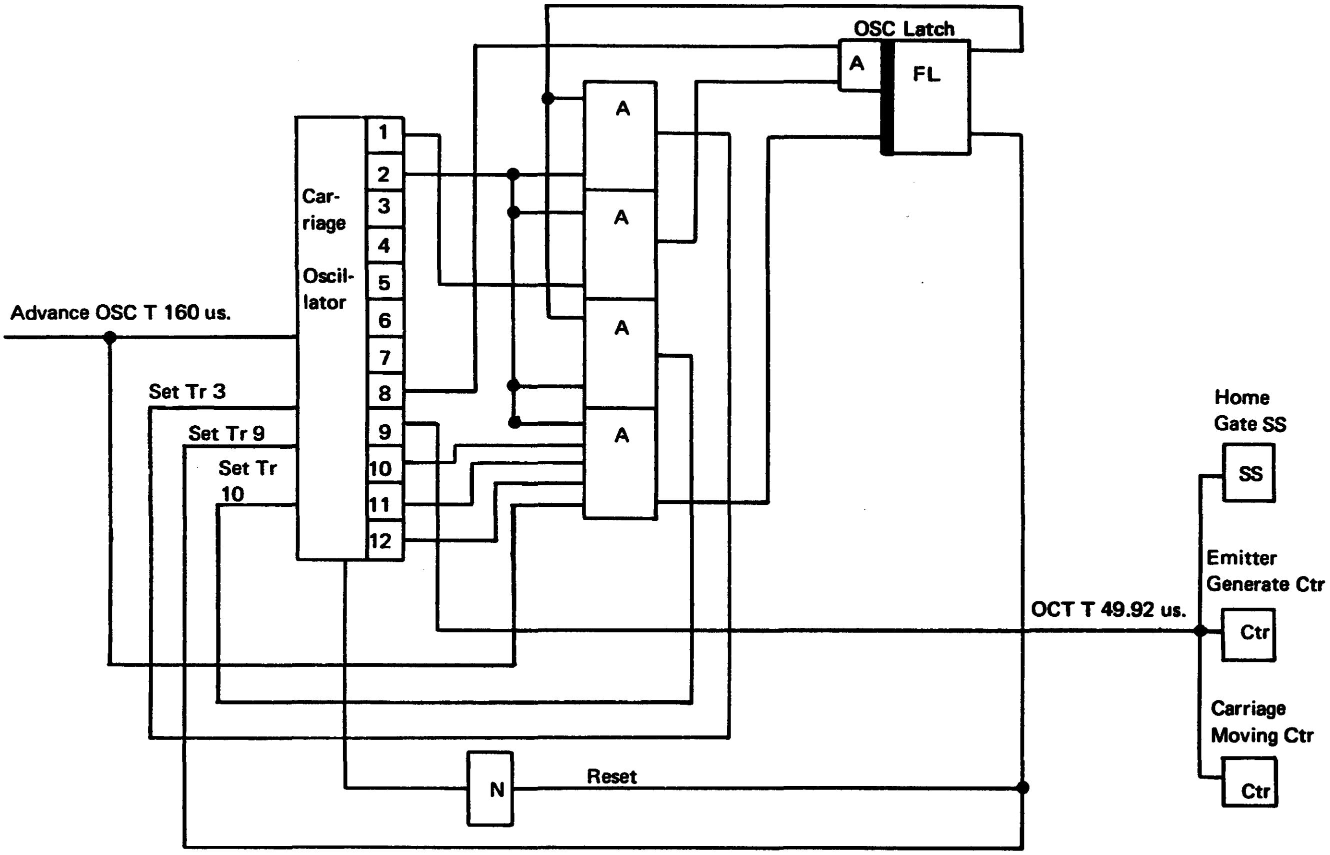


Figure 2-18. Carriage Oscillator

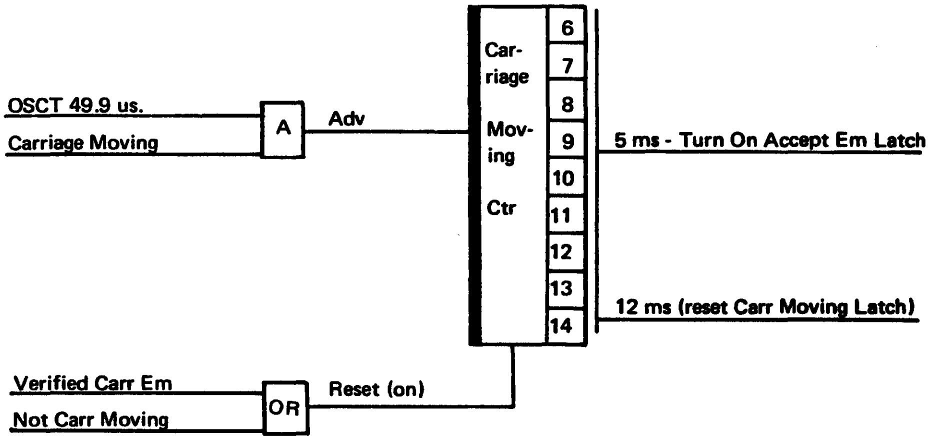


Figure 2-19. Carriage Moving Counter

EMITTER GENERATE COUNTER

- The emitter generate counter consists of three binary triggers.
- The counter:

  1. Ignores a false carriage emitter pulse.
  2. Generates a pulse detection gate to look for an extra emitter pulse.
  3. Generates a verified carriage emitter pulse.

On every carriage operation, the emitter generate counter (1) receives a carriage emitter pulse from 0.5 ms to 1 ms in duration, (2) checks to see if it is an actual emitter pulse and not noise (an extraneous signal on the carriage emitter line of a duration less than 25 us.), (3) delays it for 0.125 ms, and (4) then converts it to a verified emitter pulse 25 us. in duration. The verified emitter pulse steps the space control and line counters.

The emitter generate counter consists of three binary triggers. During carriage operation, approximately 5 ms after the carriage clutch is picked, a pulse on the carriage emitter line and a carriage oscillator pulse step the counter by one. If the pulse on the carriage emitter line becomes inactive with a count of one, the emitter pulse is considered to be a noise pulse and the counter is reset (Figure 2-20, insert A). If the counter is allowed to continue to count to 1 on, 2 off, and 3 on, the outputs provide a gate to the extra emitter detection circuit (Figure 2-20, insert B). As the counter continues to count to 1 off, 2 off, 3 on, the output generates a verified carriage emitter pulse (Figure 2-20, insert C).

Circuit Objectives

Refer to FEMD 4-220.

The 'accept emitter' line active ANDed with 'carr em' turns on the 'emitter unverified' latch. The 'emitter unverified' latch active ANDed with carriage oscillator pulses advances the emitter generate counter. A counter output of not 1, 2, and 3 ANDed with 'carr em' not active resets the 'emitter unverified' latch and the emitter generate counter (false emitter pulse). The other reset is the 'res em gen' line active, which is the normal reset (Figure 2-20).

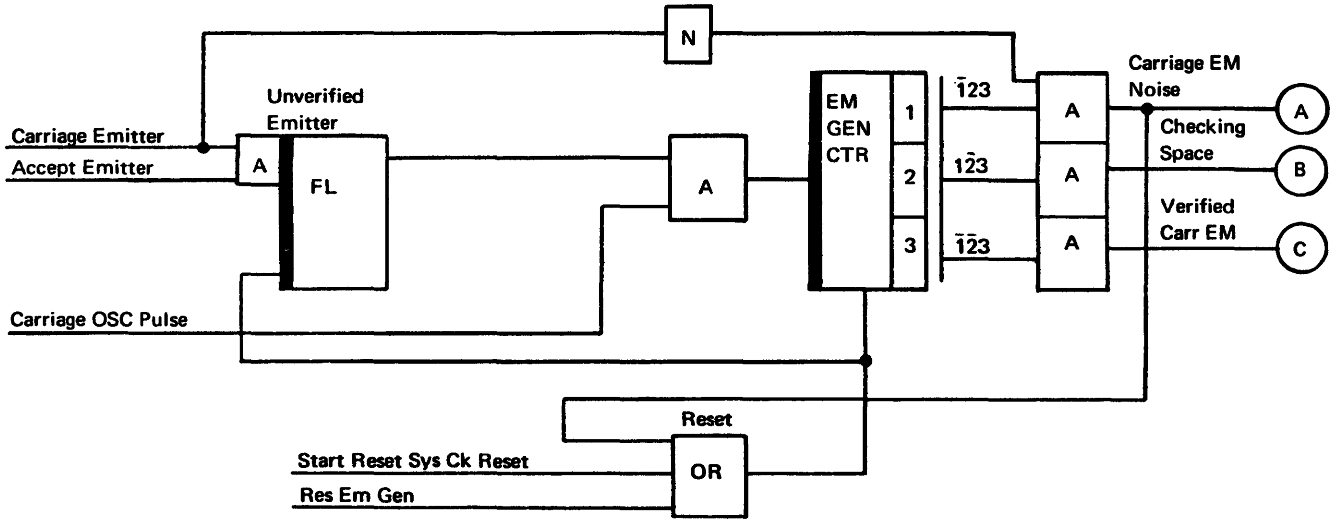


Figure 2-20. Emitter Generate Counter

Chapter 3. Principles of Operation

This chapter describes the electrical operation of the IBM 5203 Printer Attachment. References are made throughout the chapter to the maintenance diagrams in the Field Engineering Maintenance Diagram manual (FEMD). All logic names used in the circuit descriptions appear as they do in the maintenance diagrams.

The following description of the print operation has been divided into the chronological sequence of events needed to print one line of information. The "Print Operation" flowchart in the *Field Engineering Maintenance Diagrams* manual shows the entire print operation. Use this flowchart with this text to better understand the print operation.

PRINT OPERATION

Before printing, three load I/O and one start I/O instruction must be given (one start I/O instruction is needed for each line to be printed). The three load I/O instructions given are:

1. Load the main storage address of the chain image into the LPIAR in the CPU.
2. Load the main storage address of the data to be printed into the LPDAR in the CPU.
3. Load the forms length into the forms length register in the printer attachment.

When the chain image has been loaded into main storage, and the data to be printed has been assembled in the line printer data area of main storage, the start I/O instruction is given. This instruction contains the carriage information and initiates the print operation.

After the start I/O instruction has been initiated, print cycle steals occur. You must thoroughly understand print cycles to understand the print operation.

Print Cycle Steals

- The I/O cycles for the printer attachment are print cycle steals.

- Each print cycle steal is an individually requested I/O cycle.

- During the I/O cycle, normal CPU processing is suspended temporarily and the attachment controls the CPU registers, main storage, and the ALU.

- The printer attachment uses four different types of I/O cycles (print cycle steals) to generate a line of print.

Print cycle steals are individual CPU cycles requested by the attachment. During these cycles the CPU registers, main storage, and the ALU are controlled by the attachment circuitry. Print cycles occur in groups of three or fewer with an initial cycle steal (PC0) taken each time the mechanical (M) position of the incrementer cam is changed.

Cycle steals must be requested individually and are sequential, PC1 through PC3. A device of higher priority can take intervening cycle steals without affecting the sequence of print cycle steals.

A print cycle group end occurs when the last cycle steal of a particular print cycle group is completed. A print cycle group ends after one cycle steal if the character in the Data Register is a blank, after two cycle steals if the character in the Data Register is not a compare, or after three cycle steals if the character is printed.

Initial Cycle Steal (PC0)

- Request a print cycle steal.

- Take print cycle steal zero (PC0) to preload the low order byte of the LPDAR with the address of the first print position to be optioned in an M position.

After receiving the start I/O instruction from the CPU, the printer attachment requests a cycle steal (PC0) to preload the low order byte of the LPDAR with the address of the first print position to be optioned.

3

The low order byte of the LPDAR is preloaded with an address of 7C (hexadecimal) if the incrementer cam is in the M1 position. If the incrementer cam is in the M4 position, the low order byte of the LPDAR is preloaded with a 7F (hexadecimal). At CPU clock 0 time, the low order byte of the LPDAR is sent to the CPU and is returned to the data register in the attachment at 'sample DBO cl 3' time. At CPU clock 4 time, it is transferred into the hammer address register by activating the 'load HAR' line. This preloads the hammer address register with the address in main storage where the data for the first hammer to be optioned to print is located.

Circuit Objectives

Refer to FEMD 5-010.

Initialize Attachment Circuitry

- Receive a PSS1 pulse.
- Advance the chain character counter.
- Advance the scan counter.
- Activate the hammer clock.
- Synchronize the printer to the attachment.

The magnetic emitter on the print chain constantly generates pulses while the chain is moving. These pulses develop PSS1, PSS2, and PSS3 pulses in the attachment.

During PC0, the 'PC0 control' latch is turned on. The first PSS1 that occurs after PC0 control has been set activates the 'cc shift' line and turns on the 'print time' latch. This synchronizes the printer to the attachment for one increment scan. The 'cc shift' line advances the character counter and the scan counter. 'Print time' turns on the 'start hmr clock' latch and starts the hammer clock. 'Print time' also turns the 'print cycle request' latch on, and initiates print cycle steals. This sequence is repeated at the start of three more increment scans to complete one print line.

Circuit Objectives

Refer to FEMD 5-020.

First Cycle Steal (PC1)

- Request a print cycle steal.
- Load the data register in the attachment with a data character from main storage.
- Decode the data character to determine if it is anything other than a blank.
- If the data character is not a blank, inhibit incrementing the LPDAR.
- Load the LPIAR in the CPU with the data character from the chain character counter.

A request for print cycle steal one (PC1) must now be made to bring a data character from main storage to the attachment data register. When the cycle steal is granted, a data character from main storage, addressed by the preloaded address in the LPDAR, is sent and stored in the attachment data register.

The data register decodes the character to determine if it is anything other than a blank (hexadecimal 40). If the data character is not a blank, the 'no data' line in the data register is not activated and another cycle steal is taken to determine if it is to be printed. The 'no data' line inactive will also activate the 'chan 1 inhibit LSR load' line, which prevents incrementing the LPDAR in the CPU. It is necessary to retain the present address in the LPDAR in the event that the same data area will be addressed on the following cycle steal (PC2 to check for print compare).

A hexadecimal 40 found in the data register means:

1. This position has either been printed or is a blank.
2. The 'chan 1 inhibit LSR load' line would not be activated.
3. The LPDAR is incremented (the next address to be optioned for printing).
4. The 'PC group end' line is activated and no more cycle steals are taken in this group (for this print position with the chain character being optioned).

Also, during PC1 (at clock 1 and 2 time), the LPIAR in the CPU is loaded with the character contained in the 7-bit shift register of the chain character counter. The character is placed in the DBI assembler. At 'clock 0', the 'select LPIAR to load CC' line is activated and the character is sent to the CPU.

Circuit Objectives

Refer to FEMD 5-030.

Second Cycle Steal (PC2)

- Request a print cycle steal (if data was found during PC1).
- Load the B register in the CPU with a character from main storage addressed by the preloaded LPIAR.
- Load the A register in the CPU with the character to be printed, stored in the data register in the printer attachment.
- Subtract the A register from the B register in the ALU.
- Load the results of the subtraction into the printer attachment data register.
- Decode the results of the subtraction to see if the character is to be printed (print compare).
- If it is a print compare, inhibit the LPDAR from incrementing. Another cycle steal will be requested at that address.
- Activate the hammer fire buffer.

A request for a second print cycle stead (PC2) is needed to determine whether or not the character stored in the data register matches the chain character over that print position, and whether or not the character can be printed. Upon granting the cycle steal, the CPY loads the B register with a character from main storage addressed by the preloaded LPIAR. The character stored in the printer attachment data register is placed on data bus in and loaded into the A register in the CPU. The parity bit for this character is not regenerated. Parity was checked when the character was received in the data register in the attachment during PC1. The character is sent back to the CPU exactly as it was received.

The A-register character is subtracted from the B-register character in the ALU. Results of this subtraction are placed on data bus out and transferred to the attachment data register. The contents of the data register are decoded to determine if the data character is a zero (A register minus B register = 0).

If the data character is zero, the 'print compare' line is activated. One more print cycle steal is requested to write a hexadecimal 40 into the location in main storage of the data character with the 'print compare'.

The 'print compare' line active will activate the 'chan 1 inhibit LRS load' line to prevent incrementing the LPDAR in the CPU. It is still necessary to retain the present address in the LPDAR so it can be used during PC3. If a 'print compare' is detected during PC2, the 'print compare' line will activate the 'hmr fire bfr' trigger.

If the data character decoded in the data register is not a zero, the 'print compare' line is not activated. Therefore, PC2 cannot activate 'chan 1 inhibit LSR load' line. The LPDAR is now incremented to the next address to be optioned for printing. The 'PC group end' line is activated and no more cycle steals are taken for this print position with the chain character being optioned.

Circuit Objectives

Refer to FEMD 5-040.

Third Cycle Steal (PC3)

- Request a print cycle steal (if 'print compare' became active during PC2).
- Block reading into the B register in the CPU so that it will contain a zero.
- Load the A register in the CPU with a blank (hexadecimal 40).
- Add the A register to the B register in the ALU [A (Hex 40) + B (zero) = Hex 40].
- Place the hexadecimal 40 in the main storage location of the character to be printed.
- Increment the LPDAR.

A request for a third print cycle steal (PC3) is needed to blank out the main storage location of the character to be printed. This character is blanked out so that the next time the LPDAR addresses this position, a blank is decoded on PC1. A blank decoded tells the attachment that this position has been printed. This reduces the number of cycle steals required when the remaining chain characters are optioned for printing. The 'PC group end' line is activated and no more cycle steals are taken for this print position for the chain character being optioned.

To blank out the core position that has been set up for printing, it is necessary to write a blank (hexadecimal 40) into the main storage in that position. The 'PC3' line active activates the 'chan 1 block SDR' line to prevent loading anything into the B register (in the CPU) leaving its contents all zero.

A hexadecimal 40 is generated by ANDing 'PC3 cl 1' with 'print compare' and gating it to the DBI assembler. The hexadecimal 40 is loaded into the A register in the CPU. The A register is added to the B register in the ALU. Adding the hexadecimal 40 to zero results in the hexadecimal 40 being loaded into main storage in the location of the data character (addressed by the LPDAR) that has been set up for printing.

The LPDAR is incremented (to the next address to be optioned for printing) during PC3. 'PC group end' is activated and no more print cycle steals are taken in this group.

Circuit Objectives

Refer to FEMD 5-050.

Hammer Firing

- Decode the hammer address register into one X and one Y address line.
- Activate the selected X and Y address lines in the printer and in the hammer check LSR in the attachment.
- With the X and Y address lines and the hammer set pulse active, the selected hammer driver turns on and the hammer fires.
- Check that the hammer driver has turned on.
- Check that the hammer driver has turned off.

The hammer address register was loaded with the address in the LPDAR either as the result of PC0 or PC group end followed by a 'load HAR' pulse.

The address in the hammer address register is decoded into one X address line and one Y address line. The two selected address lines are taken to the printer to select a hammer driver latch and the hammer check LSR in the attachment.

At 'hammer clock 4' time in the attachment, the 'hammer set' pulse is activated if the hammer fire buffer trigger is on. The 'hammer set' pulse is taken to the printer and to all of the hammer latches. It ANDs with the latch that has the X and Y address lines active and turns on the latch. With the latch set, the hammer fires.

Each hammer driver is addressed once during every print scan. Each time it is addressed, a hammer driver is deactivated by the 'hammer reset' pulse unless a character is to be printed in that position. If a character is to be printed in that position, a hammer is activated by the 'hammer set' pulse. Two checks are made on every hammer fired: (1) a check to ensure the hammer driver turned on, and (2) a check to ensure that it has turned off. The check to see if the hammer driver turned on is made during the same print scan that sets up the hammer to print (print scan X). An inactive 'hammer off echo' line from the printer indicates the hammer driver turned on. The hammer driver is left on for that print scan (scan X). During print scan X + 1, the hammer driver is addressed again and turned off.

The check to see if the hammer driver has turned off occurs two print scans later (print scan X + 2). The check to see if the hammer has turned off cannot be made on the next print scan after the hammer driver has fired (print scan X + 1) because the response from the hammer driver that generates the 'hammer off echo' line is still on because of a long period of reset delay. If the 'hammer off echo' line is active at scan X + 2, the hammer has turned off.

On Model 3 printers, the reset of the hammer drivers is different from the Models 1 and 2. Since a print scan in the Model 3 is only 0.729 millisecond, and the hammer drivers must be left on about 1.2 milliseconds, a hammer driver set on in one scan cannot be reset when it is addressed again in the next scan. The hammer driver is actually reset about one and two-thirds scans after it is set.

A reset time in Model 3 printers is developed in each hammer clock cycle and this is used to decode the X and Y address lines of the hammer being set to a different X and Y line during reset time. For example, the X and Y line used to set hammer driver 2 is decoded to the X and Y line necessary to reset hammer driver 9. The hammer driver set in a scan is prevented from being reset in the same scan. This is done by bringing up 'Inhibit Echo Scan' in a similar method as when it is used to prevent echo checking.

Refer to "Hammer Check LSR" for more information.

Circuit Objectives

Refer to FEMD 5-060.

Hammer Driver Reset (No Data, or No Print Compare)

- Each hammer driver is reset during every print scan unless it was turned on in that print scan.

- Hammer drivers that are reset on a print scan are checked to make sure they are off.

A reset pulse is sent to every hammer driver during every print scan except the print scan in which a hammer driver turned on. The 'hmr fire bfr' trigger controls the times that reset pulses are sent. The trigger is set at 'PC2' and 'print compare'. At this time, the attachment sends 'hammer set' pulses to the hammer drivers. The trigger is reset during PC1 when no data is found (the 'no data' line active), or during PC2 when no print compare is found (the 'print compare' line inactive). When the 'hmr fire bfr' trigger is off, the 'hammer off' line is active. At 'hammer clock 4', the 'hammer set ctrl' is activated. This pulse ANDed with 'hammer off' activates 'hammer reset'. The reset pulse is taken to the printer to reset the hammer drivers.

On Model 3, the 'Hammer Reset' pulse is activated by (not) 'Inhibit Echo Scan' at 'Hmr Cl 3' time just before the 'Reset Time' latch is reset.

An active hammer echo line from the printer ('hammer off echo') received as a result of resetting the hammer drivers, indicates the hammer drivers are off.

Circuit Objectives

Refer to FEMD 5-075.

Cycle Regeneration and Ending Operation

- Determine the following:

  1. Is one of the last three hammers addressed?
  2. Is it PSS3?
  3. Have all 50 print scans been taken?
  4. Is this the last mechanical position?

After a hammer driver has been fired and checked, the printer attachment must determine exactly where it is in the print cycle. The attachment must make four decisions before it can branch back into the logical flow of the print operation:

1. Is hammer 31, 32, or 33 addressed (120 print positions)?
2. Is it PSS3?
3. Have all 50 print scans been taken?
4. Have all the mechanical positions been serviced?

The flowchart in the *Field Engineering Maintenance Diagrams* manual (FEMD 5-070) illustrates the branching conditions.

Unprintable Character

- An unprintable character (UPC) is any character that is optioned for printing but does not appear in the chain image area in main storage.

- An unprintable character sets a sense bit in the SNS bit assembler, but will not be detected unless an SNS instruction is given.

The UPC is a character addressed by the LPDAR and optioned for printing for which no print compare occurs during PC2. The UPC is optioned for printing on all 48 print scans, and remains to be optioned for the 50th print scan. At this time, however, the print line is complete and no more print options are taken in this mechanical position. The UPC is detected and a sense bit is set. An SNS instruction must be given to alert the program of the UPC. Without an SNS instruction, the sense bit remains undetected. It remains active until it is reset by the next SIO instruction.

On machines with standard 48-character sets, there is no reduction in throughput caused by unprintable characters.

Circuit Objectives

Refer to FEMD 5-095.

On a machine with a standard 48-character set, if 'PC1 data cl 7' is active at 'scan 50', the UPC latch sets. At 'SNS • N code 3 • cl 1' with 'UPC' active, the UPC sense bit 'DBI SNS bit 6' is gated through the SNS bit assembler into the DBI assembler.

CARRIAGE OPERATIONS

Carriage Space

- The number of lines to be spaced is gated into the carriage space-skip register from the DBO register.

- The number of lines spaced is stored in the carriage space counter.

- When the carriage space-skip register and the carriage space counter compare, 'space stop' is activated and the carriage is stopped.

A carriage space operation initiated by an SIO instruction from the CPU is controlled by the 5203 attachment. When the binary value of space 0, 1, 2, or 3 in the carriage space-skip register equals the count in the carriage space counter, the carriage space operation is stopped.

For more information, refer to "Start I/O Instruction."

During an SIO space instruction, the control code of the instruction contains the number of lines to be spaced (0, 1, 2, or 3).

Note: A space control code of 4 or higher results in a space of zero.

The control code is sent over the DBO, and at clock 5 time of the channel I-R cycle, the DBO register is gated into the carriage space-skip register. The carriage space-skip register now contains the number of lines to be spaced. At clock 8 of the channel I-R cycle, the print trigger is turned on. This indicates the printer will print a line before spacing. At the end of the channel I-R cycle, the space latch is turned on to initiate a space after the print cycle has been completed. The carriage control latch is turned on whenever the following conditions are met:

1. '48 character set'
2. 'last M position of line'
3. 'scan 45'
4. (not) 'forms jam'

This allows the 'carriage clutch control' line, along with the space latch on, to gate the carriage clutch and turn on the carriage moving latch. The carriage clutch is picked and the carriage and forms advance. A carriage emitter pulse is sent from the printer to the attachment for each line that the carriage and forms advance. Each carriage emitter pulse resets the carriage moving counter and advances the carriage space counter by one count. The carriage space-skip register and the carriage space counter are compared each time a line is spaced. When they compare equal, the 'space stop' line is activated. This degates the carriage clutch (the clutch latches up and the carriage and forms stop moving), and resets the space latch. The carriage moving counter then counts down for 12 ms and resets the carriage moving latch. (This allows time for all carriage parts to stop moving.) The carriage moving latch being off activates the 'carriage not busy' line, and the printer is ready to accept another instruction.

Circuit Objectives

Refer to FEMD 5-210.

Carriage Skip

- The carriage line number to be skipped to is gated into the carriage space-skip register from the DBO register.
- The line counter contains the binary value of the carriage form line being skipped.
- When the carriage space-skip register and the carriage line counter compare equal, skip stop is activated and the carriage is stopped.

A carriage skip operation initiated by an SIO instruction from the CPU is controlled by the 5203 attachment. When the binary value of the form line to be skipped to in the carriage space-skip register equals the count in the line counter, the carriage skip operation is stopped.

Refer to "Start I/O Instruction" for more information.

During an SIO skip instruction, the control code for the instruction contains the number of the form line to be skipped to.

Note: A code of 0 will be accepted, but causes no carriage motion.

The control code is sent to the DBO. And at clock 5 time of the channel I-R cycle, the DBO register is gated into the carriage space-skip register. The carriage space-skip register now contains the line to be skipped to. At clock 8 of the channel I-R cycle, the print trigger is turned on. This tells the printer to take a print cycle before skipping. At the end of the channel I-R cycle, the skip latch is turned on to tell the carriage that a skip is to be taken after the print cycle is completed. The carriage clutch control latch is turned on when the following conditions are met:

1. '48 character set'
2. 'last M position of line'
3. 'scan 45'
4. (not) 'forms jam'

This allows the carriage clutch control line, along with the space latch on, to gate the carriage clutch and turn on the carriage moving latch. The carriage clutch is picked, and the carriage and forms advance. A carriage emitter pulse is sent from the printer to the attachment for each line that the carriage and forms advance. Each carriage emitter pulse resets the carriage moving counter and advances the carriage line counter by one count. The carriage space-skip register and the carriage line counter are compared each line skipped. When the compare equal, the 'skip stop' line is activated. This action degates the carriage clutch (the clutch latches up and the carriage and forms stop moving), and resets the skip latch. The carriage moving counter then counts down for 12 ms and resets the carriage moving latch. (This allows time for the carriage parts to stop moving.) The carriage moving latch being off activates the 'carriage not busy' line, and the printer is ready to accept another instruction.

Manual Carriage Operations

Manual Space

- Pressing the space key on the printer console initiates a single line carriage space when the printer is in a not ready state.

When the space key is pressed, the manual space latch is turned on. The manual space latch turns on the manual space trigger. Turning the manual space trigger on activates the 'manual carriage op' line. 'Manual carriage op' ANDed with 'carriage clutch control' activates the 'carr cl' line. This picks the carriage clutch and turns on the carriage moving latch. The carriage is now moving and the carriage moving counter is started. A verified emitter pulse resets the manual space trigger and the carriage moving counter. Turning off the manual space trigger deactivates 'manual carriage op', which degates the clutch. This stops the carriage after one line has been spaced.

If there are no more carriage emitter pulses to reset the carriage moving counter, the counter runs for 12 ms and resets the 'carriage moving' latch. This allows the printer to become not busy, and another printer function can be initiated.

Circuit Objectives

Refer to FEMD 5-220.

Manual Restore

- Pressing the restore key on the printer console initiates a carriage restore to line one of the next form.

Pressing the restore key sets the manual restore latch; releasing the key resets the manual restore latch. The manual restore latch turns on the manual restore trigger. Turning the manual restore trigger on activates the 'manual carriage op' line. 'Manual carriage op' ANDed with 'carriage clutch control' activates the 'carr cl' line. This picks the carriage clutch, and turns on the carriage moving latch. The carriage is now moving and the carriage moving counter is started. As the carriage searches for line one and the verified emitter pulses are sensed, the carriage moving counter is reset and then restarted. The line counter and the forms length register are continually being compared. A compare equal of the line counter and the carriage forms length register turns on the line compare latch. This indicates the carriage is at the last line of the form. The carriage must move one more line to be at line one. This is accomplished by waiting for another verified pulse to reset the line compare latch. The line compare latch going off turns off the restore reset trigger, which activates the 'restore reset' line. The 'restore reset' line has two functions:

1. It resets the line counter to one, and the line counter output being one resets the restore reset trigger on.
2. The restore reset line turns off the manual restore trigger.

The manual restore trigger going off deactivates the 'manual carriage op' line, which degates the carriage clutch.

By receiving no more emitter pulses, the carriage moving counter that was reset with each verified emitter pulse is allowed to run for 12 ms; it then resets the carriage moving latch. The carriage moving latch going off allows the printer to drop busy, and another print function can be initiated.

Circuit Objectives

Refer to FEMD 5-220.

I/O INSTRUCTIONS

Start I/O Instruction

- Initiates a printer operation.
- Consists of an I-Q and an I-R cycle in the attachment.
- During the I-Q cycle, the Q byte of the instruction is decoded and the condition code is sent back to the CPU.
- The I-R cycle decodes the control code to load the carriage space-skip register.
- The print latch is turned on during the I-R cycle.

3

The start I/O (SIO) instruction initiates the print operation. The line printer data area in main storage, addressed by the LPDAR, is printed because an SIO instruction has been issued. One SIO instruction is required for each line of print.

Two cycles are generated in the printer attachment by the SIO instruction. The first is an I-Q cycle to interrogate the Q byte of the instruction and determine the condition code of the printer attachment. The I-R cycle loads the carriage space-skip register with the information on how far to space or skip. It also turns on the print latch.

I-Q Cycle

During the I-Q cycle the following events occur:

1. The device address is decoded.
2. The print buffer and carriage are checked to see if they are busy.
3. The condition code is determined and sent to the CPU.
4. The M and N fields of the Q code are interrogated.
5. Either the space or skip latch is set in the carriage circuitry.

An SIO instruction sent by the CPU is received by all attached I/O devices. Therefore, each I/O attachment must decode the device address (DA) in the Q code of the instruction to determine if the SIO is for him. At the same time, the attachment interrogates its circuitry to see if it is busy. If the DA is for the attachment, and if the attachment is not busy, a condition code of B is sent back to the CPU. This tells the CPU that the SIO was accepted and an attachment (printer) I/O operation starts.

If the printer attachment decodes the DA in the SIO instruction as an E (the DA for the printer), and the printer and the carriage are not busy, a condition code of B is sent to the CPU.

After the condition code of B is determined by the attachment, the M and N fields of the Q code are interrogated to determine carriage information. Without a condition code of B the attachment stops further operations. The M field of the Q code selects a carriage (a 0 selects the left carriage, and a 1 selects the right carriage). The N field determines if the carriage is to:

1. Space only, or
2. Print and space, or
3. Skip only, or
4. Print and skip.

With a carriage selected, and one of the above conditions, either the space or skip latch in the carriage circuits is set.

I-R Cycle

During the I-R cycle, the carriage space-skip register (of the carriage selected by the M field) is loaded with how far the carriage should space or skip. At this time, the carriage has all the data it needs for the print operation.

At clock 8 time, the 'print' latch is set. This completes the SIO instruction and the attachment can now take cycle steals and begin the print operation.

Circuit Objectives

Refer to FEMD 5-310.

I-Q Cycle

When the SIO instruction is sent, the following lines are activated:

1. The 'I-Q cycle' line from the CPU activates the 'I-Q cycle' line in the attachment.
2. The 'SIO instr' line from the CPU activates the 'SIO instr' line in the attachment.
3. The Q code is put on data bus out and placed in the DBO register.

The device address is decoded. If an E (DBO bits 0, 1, and 2 active and DBO bit 3 inactive) is decoded, the 'ptr DA decode' line is activated. At 'sample DBO cl 5' time, the Q byte is loaded into the Q register.

The status of the printer attachment (busy or not busy) is determined in the Q register. The 'printer not busy' line is active if the 'right carr not busy' and 'left carr not busy' lines are active (carriages not moving) and the 'print buffer not busy' line is active ('print latch' not set).

At 'sample DBO cl 5' time, the 'ptr DA decode' latch is set. The output of the latch ANDs with 'SIO instr' to activate the 'SIO • ptr DA' line. With this line and the 'printer not busy' line active, the 'chan 1 I/O condition B' line is activated.

The M field of the Q code is decoded to activate either 'select right carr' or 'select left carr.' 'Q bit 4' active selects the right carriage; 'not Q bit 4' active selects the left carriage.

The N field of the Q code is decoded to activate one of the following:

1. 'SIO space command'
2. 'SIO skip command'
3. 'print' and 'SIO space command'
4. 'print' and 'SIO skip command'

Refer to Figure 3-1 for the Q byte decode for the above carriage commands.

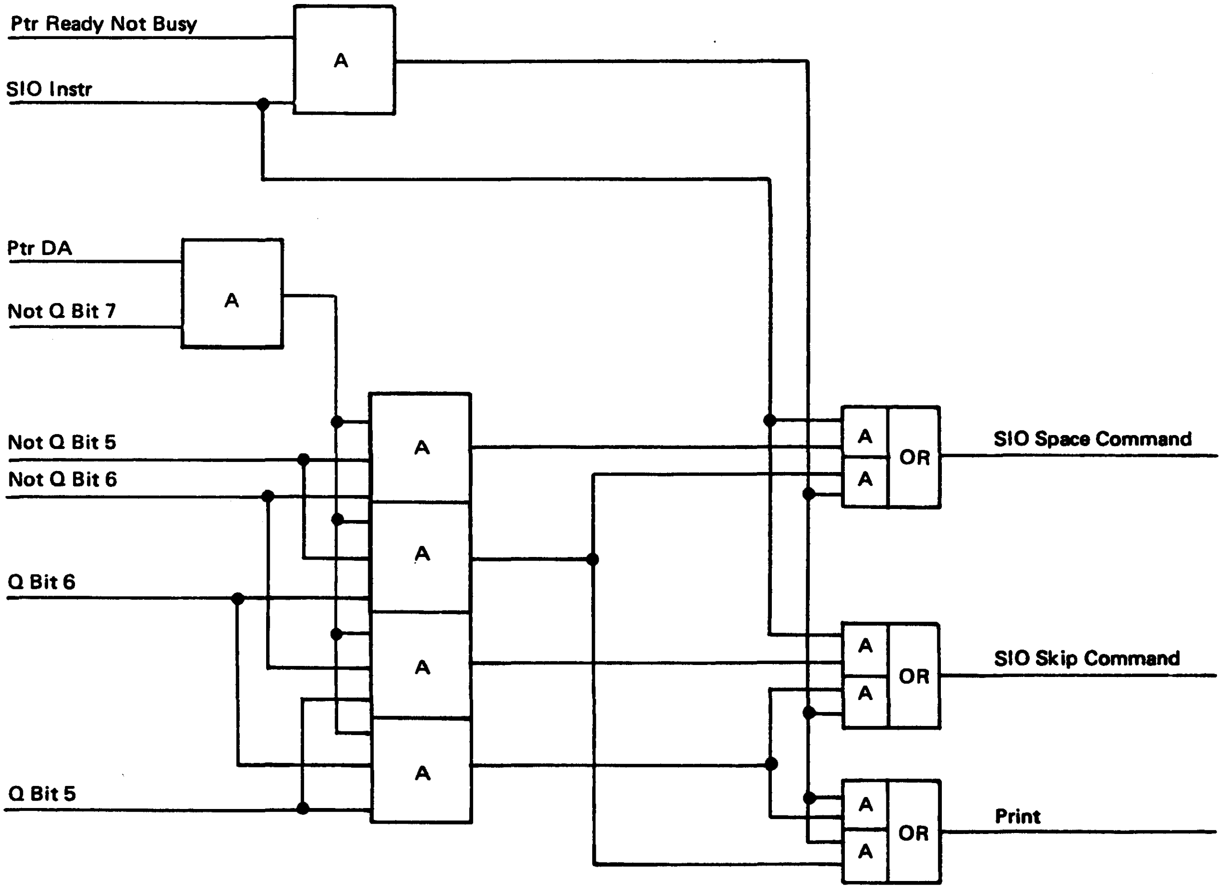
With a carriage selected, and either 'SIO space command' or 'SIO skip command' active, either the 'space' latch or the 'skip' latch in the carriage circuits is set.

I-R Cycle

Upon the completion of the I-Q cycle, the 'I-R cycle' line from the CPU activates the 'I-R cycle' line in the printer attachment.

At 'sample DBO cl 5' time of the I-R cycle, the 'load right (or left) carr data bfr' line is activated. This line active gates the DBO bits (containing the amount to space or skip) into the carriage space-skip register.

At clock 8 time of the I-R cycle, the 'print' latch is turned on.



Space = Not Q Bit 5, Not Q Bit 6, Ptr DA • Not Q Bit 7
Space and Print = Not Q Bit 5, Q Bit6, Ptr DA • Not Q Bit 7
Skip = Not Q Bit 6, Q Bit 5, Ptr DA • Not Q Bit 7
Skip and Print = Q Bit 5, Q Bit 6, Ptr DA • Not Q Bit 7

Figure 3-1. Start I/O N Field Q Byte Decode

Load I/O Instruction

- Consists of an I-Q cycle and two E-B cycles.
- The I-Q cycle decodes the Q byte of the instruction and sends the condition code back to the CPU.
- Three load I/O instructions are required before printing to:

1. Load the forms length into the carriage forms length register(s).
2. Load into the LPIAR the address where the chain image can be found in main storage.
3. Load into the LPDAR the address where the data to be printed can be found in main storage.

The load I/O (LIO) instruction is used to prepare for a print operation. Three LIO instructions are necessary before a print operation can take place. One LIO instruction is necessary to load the forms length into the carriage forms length register(s). A second LIO instruction selects and loads the LPIAR, and a third selects and loads the LPDAR. By loading the LPIAR and LPDAR we are specifying the area in main storage to be addressed by them during the print operation.

I-Q Cycle

The I-Q cycle for the LIO instruction is basically the same as for the SIO instruction. (Refer to "SIO Instruction, I-Q Cycle.") The device address is decoded, the printer is checked to see if it is busy, and the condition code is determined and sent to the CPU. The M field in the Q byte of the LIO is insignificant. The N field of the LIO is interrogated to determine if it is to load the carriage forms length register, select and load the LPIAR, or select and load the LPDAR.

E-B Cycles

During the first E-B cycle (E-B1), the forms length is loaded into the right carriage forms length register. During the second E-B cycle (E-B2), the forms length is loaded into the left carriage forms length register.

The LPIAR or LPDAR are selected and loaded during E-B1 and E-B2.

Circuit Objectives

Refer to FEMD 5-330.

The circuit objectives for the LIO instruction are similar to those of an SIO instruction. 'LIO instr' and 'I-Q cycle' lines are sent to the attachment along with the Q byte. The attachment activates its 'LIO instr' and 'I-Q cycle' lines. The Q byte enters the DBO register.

The device address is decoded and at 'sample DBO cl 5' time the Q byte is shifted into the Q register for decoding. The status of the printer, busy or not busy, is determined in the Q register and the condition code is sent to the CPU. A condition code of B (correct device and printer not busy) causes the attachment to decode the N field and inform the CPU that the LIO has been accepted.

The N field of the Q byte of a LIO is decoded to determine what it is to do (Figure 3-2):

1. Load the carriage forms length register.
2. Select the LPIAR for update.
3. Select the LPDAR for update.

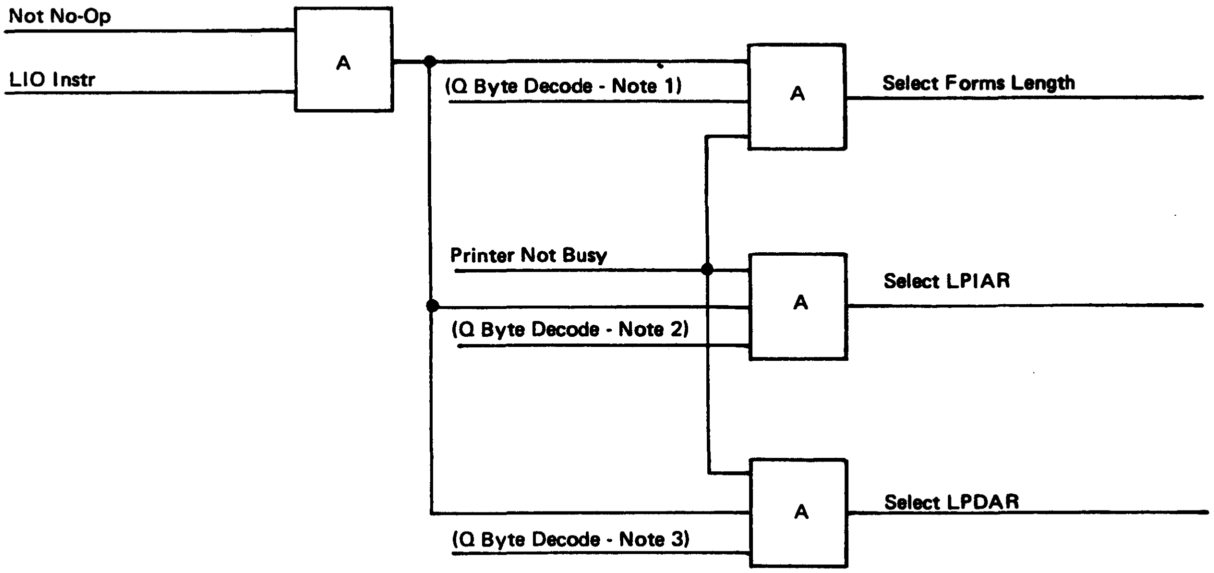
Test I/O Instruction

- Consists of an I-Q cycle.
- During the I-Q cycle, one of four conditions is tested for and the condition code sent to the CPU determines the results.
- The four conditions that can be tested for are:

1. Not ready, not no-op.
2. Print buffer busy.
3. Carriage busy.
4. Printer busy.

The test I/O (TIO) instruction is used to determine if either the printer attachment or the printer is busy or ready. There are four conditions that can be tested by a TIO instruction. These are:

1. Is the printer ready,
2. Is the print buffer busy,
3. Is the carriage busy, or
4. Is the printer busy?



Q Byte Decode
Note 1: Not Q Bit 5, Not Q Bit 6, and Ptr DA • Not Q Bit 7 (N code 0)
Note 2: Not Q Bit 6, Q Bit 5, and Ptr DA • Not Q Bit 7 (N code 4)
Note 3: Q Bit 5, Q Bit 6, and Ptr DA • Not Q Bit 7 (N code 6)

Figure 3-2. Load I/O N Field Q Byte Decode

I-Q Cycle

The TIO instruction consists solely of an I-Q cycle in the attachment. The I-Q cycle is similar to that of the SIO or LIO instructions. The difference is that in the other instructions, a condition code of B means that the carriages are not busy and that the print buffer is not busy. The TIO instruction checks to see if either carriage or the print buffer is busy, or if the printer is ready or busy; a condition code of A (not B) means that the condition checked for is met. A condition code of B in a TIO means that the condition tested was not met.

With a condition code of B, we can proceed on to the next instruction.

Note: The TIO checks for a busy or a not ready situation. A condition code of A tells us that the printer or attachment is indeed busy or not ready. Therfore, with a condition code of B the device checked (printer, carriage, or attachment) is ready for a new instruction. Although we check for a condition code of A with a TIO instruction, a condition code of B means that we can proceed to another operation the same as in a SIO or LIO instruction.

Circuit Objectives

Refer to FEMD 5-350.

The circuit objectives of the TIO are similar to those of the SIO and LIO. 'TIO instr' and 'I-Q cycle' lines are sent to the attachment from the CPU along with the Q byte. The attachment activates its 'TIO instr' and 'I-Q cycle' lines. The Q byte enters the DBO register.

The device address is decoded. At 'sample DBO cl 5' time the Q byte is loaded into the Q register. The M field is decoded to determine which carriage (if any) is to be tested. A 'Q bit 4' active selects the right carriage, and a 'not Q bit 4' active selects the left carriage.

The N field of the Q byte is decoded to determine which condition is to be tested for. Refer to Figure 3-3 for the Q byte of the conditions to be tested for.

Advance Program Level Instruction

- Consists of an I-Q cycle.
- During the I-Q cycle, one of four conditions is tested for and the condition code sent back to the CPU determines the results.
- The four conditions that can be tested for are:

  1. Ready.
  2. Print buffer busy.
  3. Carriage busy.
  4. Printer busy.

- The Advance Program Level instruction is similar to the Test IO instruction.

The Advance Program Level instruction is used primarily with the dual program feature. It is similiar to and tests for the same conditions that the test IO instruction does. The Advance Level Program (APL) instruction checks for:

1. Is the printer ready,
2. Is the print buffer busy,
3. Is the carriage busy, or
4. Is the printer busy?

The APL instruction loops until the condition being checked for no longer exists. A blank Q code is recognized as an automatic APL instruction. This condition is termed an automatic APL and is the same as a no-op.

I-Q Cycle

The APL instruction consists solely of an I-Q cycle in the attachment. The I-Q cycle is similar to that of a TIO instruction. A condition code of A means that the condition being checked for is busy. The APL instruction loops until the condition being checked is not busy and a condition code of B is activated.

Circuit Objectives

Refer to FEMD 5-350.

The circuit objectives of the APL instruction are similiar to those of the TIO instruction. The 'TIO instr' line sent to the attachment is decoded in the attachment as 'TIO-APL instr.' Therefore, the attachment uses the same circuitry for both instructions. Refer to "Test I/O Instruction" circuit objectives.

Sense I/O Instruction

- Interrogates the status of the printer attachment logic.
- Consists of an I-Q cycle and two E-B cycles.
- The I-Q cycle decodes the Q byte and sends a condition code of B back to the CPU.
- It is always accepted by the attachment whether it is busy or not.
- The two E-B cycles are taken to check for the condition called for in the N field of the Q byte.
- The sense information is sent back to the CPU.

The sense I/O (SNS) instruction interrogates the status of the printer attachment logic and sends the sense information back to the CPU. The SNS instruction is a diagnostic tool, but may be used at any time. It is always accepted by the printer attachment whether the attachment is busy or not; therefore, a condition code of B is always returned to the CPU during the I-Q cycle.

I-Q Cycle

The I-Q cycle for the SNS instruction differs from that of the other instructions only in the way the condition code is determined. The SNS instruction does not check for any busy conditions during the I-Q cycle. A condition code of B is always decoded in the Q register decode circuits. The device address is decoded and the N field of the Q byte is interrogated in the same manner as the rest of the instructions. The M field is insignificant in a SNS instruction.

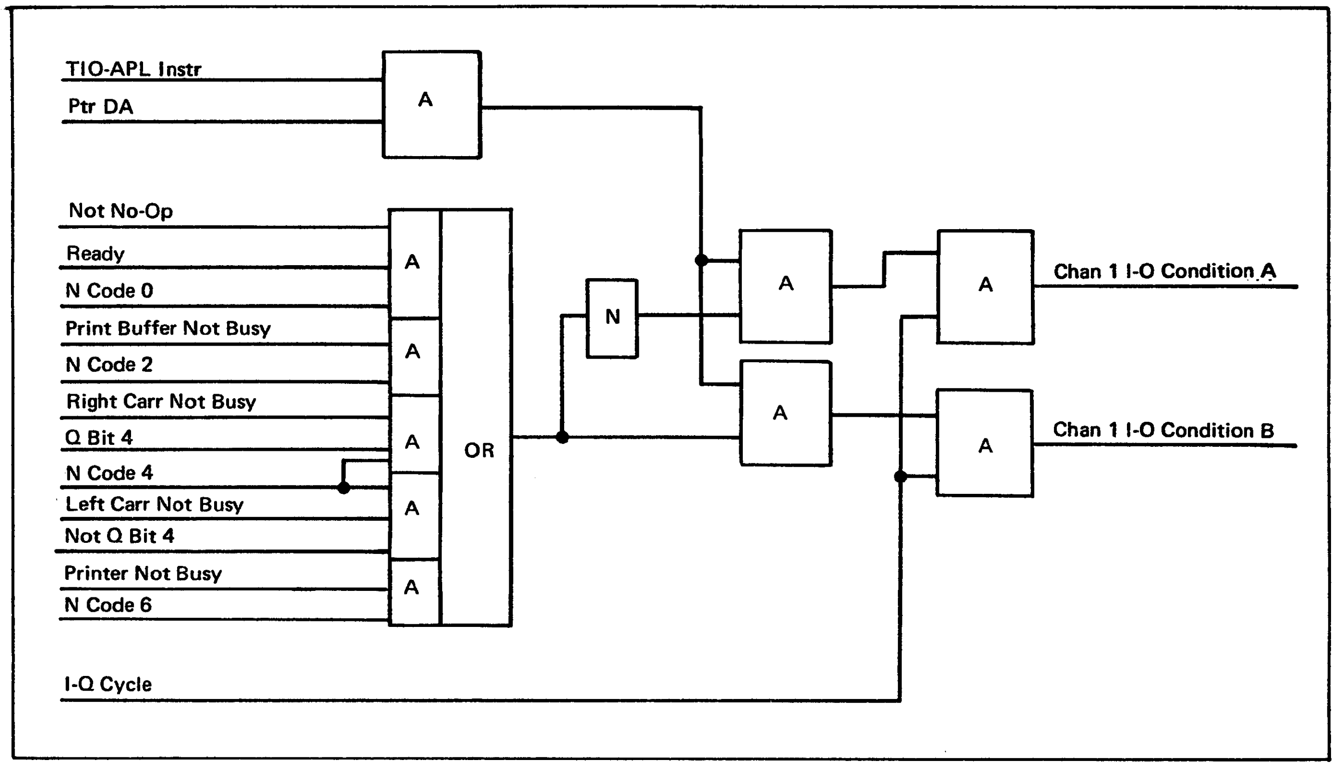


Figure 3-3. Test I/O N Field Q Byte Decode

E-B Cycles

The N field of the Q byte and the E-B cycle (E-B1 or E-B2) determines the condition to be sensed. A register is selected in the CPU or the attachment by the N field and the E-B cycle. If an attachment register is selected, its contents are put on data bus in and taken to the CPU. The selected register can be interrogated in the CPU by the program for the diagnostic value it contains.

Circuit Objectives

Refer to FEMD 5-370.

'SNS instr' and 'I-Q' cycle lines are sent from the CPU to activate the 'SNS instr' and 'I-Q cycle' lines in the attachment. The Q byte is also sent to the attachment and stored in the DBO register.

The device address is decoded and at 'sample DBO cl 5' time, the Q byte is loaded into the Q register. A condition code of B is sent to the CPU.

The N field of the Q code is decoded. The 'E-B1 cycle' from the CPU activates the 'E-B1 cycle' line in the attachment. At this time the condition specified by the N field is checked for (refer to the chart on FEMD 5-370). If the contents of a register are specified, they are placed on data bus in and taken to the CPU. If a register in the CPU is to be selected, the select lines in the attachment are raised and taken to the CPU.

During the second E-B cycle, the CPU activate the 'E-B2 cycle' line. The sequence of events for the E-B2 cycle are the same as those for the E-B1 cycle.

Special features available for the IBM 5203 Line Printer Attachment are:

- Dual Feed Carriage
- 120 Print Positions
- 132 Print Positions
- 200 LPM Throughput
- Universal Character Set (UCS)

All FF (Field Feature) B/Ms for the 5203 attachment must be installed along with the concurrent 5203 printer FF B/M.

DUAL FEED CARRIAGE

This feature provides simultaneous feeding of two non-overlapping sets of forms. The left carriage is standard, and the right carriage can be field installed.

Each carriage can move independently of the other. A separate SIO instruction is required for each carriage. Dual circuitry is provided for in the attachment FF B/M by adding two MST cards. These cards include an additional:

1. Carriage space-skip register
2. Carriage forms length register
3. Carriage line counter
4. Carriage space counter
5. Carriage moving counter
6. Carriage manual controls
7. Space check counter
8. Emitter generate counter

120 AND 132 PRINT POSITIONS

The standard 96 print positions can be increased to 120 or 132 print positions by installing the 120 or 132 print position feature B/M. The print operation in the attachment remains the same, except for two functions:

1. Inhibit cycle steal 2 and 3 after the hammer address register decodes the last existent hammer address in any subscan. This prevents CPU cycle steals because they are not needed.
2. Degate the hammer echo samples when the hammer address register decodes the first nonexistent hammer address. Hammer echo checks are not needed for nonexistent hammer positions.

When the hammer address register addresses hammers 1, 4, 7, 10, etc. during a subscan, the output of the register is decoded. If it decodes hammers 1-24, the attachment is allowed to take necessary cycle steals, and to echo-check the hammer drivers. If the hammer address register decodes hammers 25, 26, or 27 (nonexistent in 96 print position machine), cycles 2 and 3, and echo-checking, are prevented for the remaining portion of this subscan. In the case of 120 print position operations, cycle steals and echo-checking are prevented for a decode of hammers 29, 30, or 31.

Circuit Objectives

Refer to FEMD 4-110.

The 'last feature address' latch is turned on when an existent hammer is addressed during any print subscan. The 'last feature address' latch is not turned on when the address register is loaded with the address of the first nonexistent hammer address (25, 26, or 27 for 96 positions, or 29, 30, or 31 for 120 positions). This does two things:

1. The 'force PC grp end' latch is turned on. This ANDed with 'PC1' resets the 'request time' latch and PC2 and PC3 of this PC group, and the remaining groups of this subscan are not taken. The 'force PC group end' also allows update of the LPDAR, during PC1, by degating 'chan 1 inhibit LSR load'.
2. The 'feature inhibit scan' latch is turned on. This degates the 'sample echo check' for the remaining addressed nonexistent hammer positions.

The 'force grp end' latch is reset at the beginning of the next subscan with 'chain em ss w-o home'. The 'feature inhibit scan' latch is turned off with 'first 12 prt positions' ANDed with 'hammer clock 1', 'hammer clock control', and 'HAR clock'.

200 LPM

The 5203 throughput can be changed from 100 LPM to 200 LPM, or from 200 LPM to 100 LPM, by changing a jumper wire and the incrementer cam.

The M position counter operates differently for 200 line per minute machines than for 100 line per minute machines. The 200 LPM machines print in both directions, whereas, the 100 LPM machines print in one direction only. Alternate lines start printing in either M1 or M4. The M position counter steps in both directions (M1, M2, M3, M4, M4, M3, M2, M1, M1, M2, etc.).

300 LPM

The 5203 throughput can be increased to 300 LPM by installing the 300 LPM Field Feature Bills of Material on both the printer and attachment.

UNIVERSAL CHARACTER SET

Any character set with more than 48 different characters is defined as a universal character set (UCS). The UCS feature expands the 48-character set to a character set with 49 to 120 different characters.

An MST card located at B1 L4 of CPU controls the UCS in the 5203 attachment. The 5203 has an additional emitter (UCS emitter) and microswitch installed. The microswitch is activated by a stud on the UCS chain cartridge. This switch indicates to the attachment that the UCS feature is installed on the 5203. These functions are installed with the UCS feature B/M. Three functions of the 5203 attachment are changed by the UCS feature:

1. Operation of the 'home' latch is changed. With the standard 48-character set, the home latch is turned on at the beginning of every character set (5 times per chain revolution). This resets the character counter to prepare for the following character set. With UCS, the 'home' latch is turned on once per chain revolution. This is accomplished by receiving 6 UCS emitter pulses, and 5 chain emitter pulses per chain revolution. The pulses coincide once per chain revolution, turning on the 'home' latch. This resets the character counter to prepare for the following UCS character set.

   Circuit Objectives: Refer to FEMD 4-080. The 'home' latch is turned on once per chain revolution. 'UCS home' ANDed with '320 NS chain em' and '250 micros home gate' turn on the 'home' latch. Turning on the 'home' latch brings up the 'reset cc' line which resets the character counter.

2. In UCS, the scan counter reaching 48 will not stop printing. The scan counter begins with the first PSS1 pulse after a print start ss pulse. The scan counter's only function is to define the inhibit range (scans 41-56 for Models 1 and 2; scans 34-86 for Model 3) of the incrementer clutch (prevents clutch nipping). Printing in any of the four M positions is stopped when all the data in the print image for that M position has been printed (detected by unprinted data circuit). The incrementer clutch is then energized and the hammers are shifted to the next M position.

Circuit Objectives: Refer to FEMD 4-300. To stop printing (subscans) in any M position with UCS, the 'begin last scan' latch is turned on at the beginning of each print scan by 'PC1' ANDed with 'PSS1' and 'first 12 print positions'. If 'unprinted data' becomes active, the 'begin last scan' latch is reset, and another scan is taken. If the 'unprinted data' line does not reset the 'begin last scan' latch by the end of a scan, the 'stop printing UCS' line becomes active. The 'stop printing UCS' line active does two things:

a. It resets the 'execute print' latch to stop printing.
b. It turns on the 'EOL' latch if 'last M pos of line' is not active. This turns on the 'incr clutch' latch, and the hammers are shifted to the next M position.

3. In UCS the character counter is not reset five times per chain revolution (before each 48 characters) as it is for the 48-character set. In UCS the character counter is reset twice per chain revolution (once before each character set): once with the home latch (home latch is turned on once per chain revolution with UCS), and once with the 119 ck count trigger.

Circuit Objectives: Refer to FEMD 4-095. Two resets to the character counter are generated each chain revolution (2 UCS character sets per chain).

a. Turning on the 'home' latch activates the 'reset cc' line, which resets the character counter.
b. Activating the 'cc 119 check count' line turns on the 'cc bit 8' latch. With this latch on, and all the other cc latches on (count 119 all latches on but the #8), the next 'cc shift' turns off all the latches stepping the cc to zero.

Overflow (UCS)

Overflow may or may not occur:

1. Overflow occurs whenever the increment value added to the position of the character on the chain (112 through 119 for UCS) results in the addressing of a character in the next set of characters on the chain. To be addressed correctly, this character must be referred to by its correct position on the chain. A UCS character set is repeated twice on a chain. Each of the 120 characters corresponds to one address in the LPIAR data area in main storage (XX00 through XX77 hexadecimal). To prevent the addressing of a character in the next character set on the chain (the address would be greater than 120 for UCS), a decode of 112 through 119 out of the 7-bit shift register turns on the potential overflow latch.

The low order positions of the 4-bit and 7-bit shift registers are shifted through the adder. The adder output is shifted, bit by bit (clock 1-7), back into the 7-bit shift register (any carries from the adder are placed in the carry trigger and added the next shift pulse). At clock 4 time, the 8 trigger values of the 4-bit and 7-bit shift registers are present at the adder input and the result of the addition is present at the output of the adder. With the 'potential overflow' latch on, and an adder output, the overflow trigger is gated on. Turning the overflow trigger on holds the high order trigger (trigger 64) reset for the next four shift pulses. This forces zeros to be entered in the four high order positions of the 7-bit shift register.

For example, assume a UCS with the 7-bit shift register containing a value of 116 and the 4-bit shift register incrementing by +8:

```
1110100   (116)
0001000   (+8)
─────────────
1111100   (124)
   ↑
   └──────── (Adder output causes overflow
              trigger to be set.)
```

The 124 causes an overflow condition because the highest position addressed in a UCS is 119 (0 is the first count on the chain). The overflow trigger is set, in this case, forcing zeros to be set into the four high order positions of the 7-bit shift register:

```
1110100   (116)
0001000   (+8)
─────────────
0000100   (4)
```

The 4 causes the fourth position of the next set of characters on the chain to be addressed.

2. Overflow does not occur if the increment factor added to the position of the character on the chain (112 through 119 for UCS) results in the addressing of a character in the present character set on the chain. To prevent addressing a character in the next character set, a decode of 112 through 119 out of the 7-bit shift register turns on the 'potential overflow' latch. The low order positions of the 4-bit and 7-bit shift registers are shifted through the adder. The adder output is shifted, bit by bit (clock 1-7), back into the 7-bit shift register (any carries from the adder are placed in the 'carry' trigger and added during the next shift pulse). At clock 4 time the 8 trigger values of the 4-bit and 7-bit shift register values are present at the adder input and the result of the addition is present at the output of the adder. With the 'potential overflow' latch on and no adder output, the 'overflow' trigger is not gated on. This allows the updated value to shift into the 7-bit shift register from the adder.

For example, assume a UCS with the 7-bit shift register containing a value of 116 and the 4-bit shift register incrementing by 2 (PSS counter and M counter give initialization factor to 4-bit shift register):

```
1110100   (116)
0000010   (+2)
-------
1110110   (118)
   ↑
   └──────────── (No adder output causes over-
                  flow trigger not to be set.)
```

The 118 will not cause an overflow. The overflow trigger will not be set. The true value of the 7-bit shift register and the 4-bit shift register will be added in the adder and shifted into the 7-bit shift register.

Circuit Objectives

Refer to FEMD 4-095.

Chapter 5. Power Supplies and Controls

The 5203 printer attachment receives all of its logic voltages from the 5410 CPU. Four voltages are furnished by the CPU. These are:

1. -4 Vdc for control logic.
2. +6 Vdc to convert from SLD logic to MST logic.
3. Ground.
4. 7.25 Vac for printer console lights.

Voltages generated in the printer attachment are:

1. -1.35 Vdc (reference).
2. -0.9 Vdc (a plus level).
3. -1.8 Vdc (a minus level).

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Chapter 6. Console and Maintenance Features

This chapter is not applicable to this manual. Refer to the *IBM 5410 Central Processing Unit Field Engineering Theory of Operations* manual for the description of keys and indicator lights associated with the 5203 printer.

6

Appendix A. Unit Characteristics

For machine characteristics, refer to the *IBM System/3 Installation Manual–Physical Planning,* Form A21-9084.

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