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IBM Series/1
General Purpose Interface Bus (GPIB) Adapter - RPQ D02118
Custom Feature

First Edition (December 1978)

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Preface

The term "General Purpose Interface Bus" (GPIB) is commonly used to identify the Institute of Electrical and Electronics Engineers Standard 488 as approved in 1975 (IEEE 488-1975). This interface standard was established to facilitate the interconnection of programmable instrumentation and other system components.

This publication describes the IBM Series/1 GPIB Adapter, RPQ D02118, and the associated GPIB Adapter Cable, RPQ D02119, both of which are custom features designed for use with the IBM Series/1. The intended audience for this publication is customer executives, programmers, and maintenance personnel who will be able to use this information to order products, prepare machine language code, and supplement other maintenance aids.

The subject matter is presented in three chapters and seven appendixes. Chapter 1 introduces the RPQs and summarizes the implementation of the digital interface described within the IEEE Standard 488-1975. Chapter 2 describes the commands and functions used by the GPIB Adapter. Chapter 3 contains installation planning information.

Appendix A contains an ASCII to hexadecimal conversion chart. Appendix B contains a problem determination flow chart. Appendix C contains line definitions. Appendix D contains ASCII codes for specification command and address groups. Appendix E contains diagnostic command information. Appendix F contains supplementary programming notes. Appendix G contains a glossary of terms.

Prerequisite Publication

IEEE Standard Digital Interface for Programmable Instrumentation, IEEE Std 488-1975/ANSI MC 1.1-1975—published by the Institute of Electrical and Electronics Engineers, Incorporated, 345 East 47 Street, New York, New York 10017.

Related Publications

IBM Series/1 4955 Processor and Processor Features Description, GA34-0021
IBM Series/1 4953 Processor and Processor Features Description, GA34-0022
IBM Series/1 System Summary, GA34-0035
IBM Series/1 Customer Site Preparation Manual, SA34-0050

Additional publications are listed in the *IBM Series/1 Graphic Bibliography*, GA34-0055.

Contents

Chapter 1. Introduction

The IBM Series/1 General Purpose Interface Bus (GPIB) Adapter, RPQ D02118, and the GPIB Adapter Cable, RPQ D02119, provide an interface for attaching up to fourteen digital I/O devices to an IBM Series/1 processor. The I/O devices to be attached to the Series/1 must conform to the requirements described in the IEEE Standard 488-1975. This equipment could include printers, plotters, graphic display units, card readers, and programmable laboratory equipment such as digital voltmeters, signal generators, and frequency analyzers.

The GPIB Adapter, RPQ D02118, is comprised of a single circuit card which is inserted into the Series/1 processor or the I/O expansion unit in a position appropriate for an RPQ (see Figure 1-1). The GPIB Adapter Cable, RPQ D02119, is a 4-meter cable which plugs into the adapter card and provides the connector for attaching conforming I/O devices to the Series/1 (see Chapter 3, Installation Planning).

Configuration

Within the system created by interconnecting devices on this interface, there are three major roles: controller, talker, and listener. The primary function of the controller is interface management via interface messages. The primary function of a talker is to act as a source of device-dependent data. The primary function of the listener is to act as a receiver of device-dependent data.

The GPIB adapter is always the controller and has the ability to assign to itself the role of either talker or listener. Assignment of active roles of devices that have the latent ability to be talkers or listeners is done by the GPIB adapter through its ability to send interface messages.

The maximum instantaneous data rate that can be achieved by the GPIB Adapter is 65 kilobytes per second. Throughput, however, can vary and is largely dependent upon the block size of the data which is transferred.

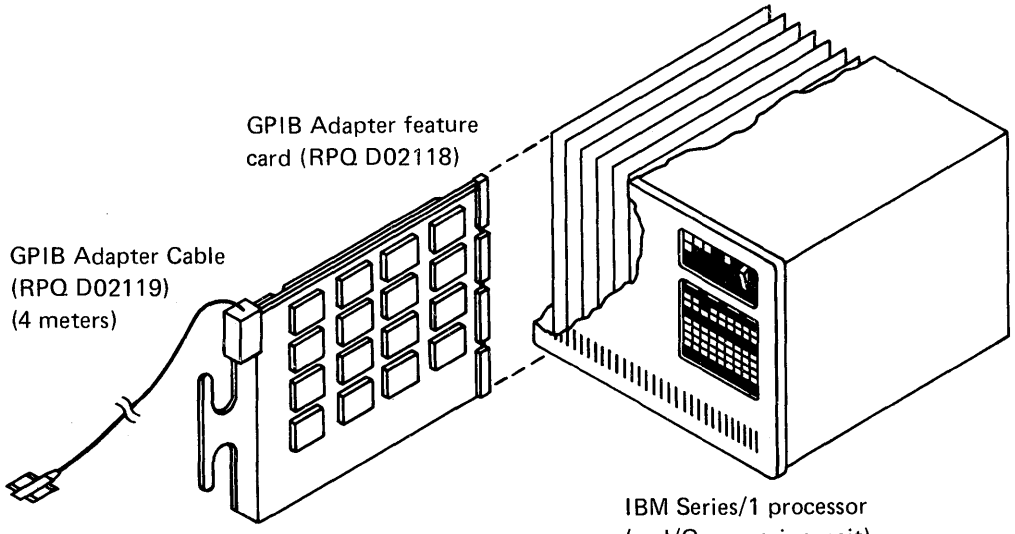


Figure 1-1. GPIB Adapter and Cable

Interface

The interface is made up of a 16-line bidirectional bus (see Figure 1-2). This bus includes:

- Five dedicated general management lines
- Three dedicated byte transfer lines
- Eight parallel data lines

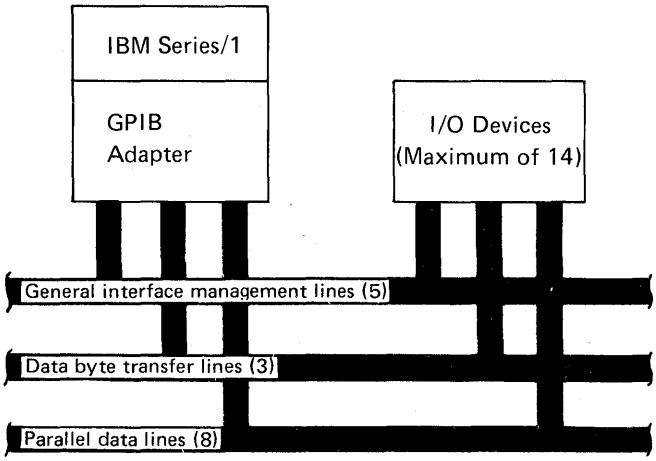


Figure 1-2. Interface structure

The five dedicated general interface management lines are:

- Attention (ATN)—activated by the controller (GPIB Adapter) to indicate control information on the data lines. When this line is not active, information on the bidirectional bus is programming information or device-dependent data.
- Interface Clear (IFC)—activated by the controller (GPIB Adapter) to place the interface and all interconnected devices in a quiescent condition.
- Service Request (SRQ)—activated by a device to indicate the need for service.
- Remote Enable (REN)—activated by the controller (GPIB Adapter) to enable devices on the interface to respond to programming messages.
- End or Identify (EOI)—activated with the last byte of data to indicate the end of a transfer sequence by the GPIB Adapter or an I/O device.

The three dedicated byte transfer lines are:

- Data Valid (DAV)—activated by a talker to indicate the validity of data on the bus.
- Not Ready for Data (NRFD)—activated by a listening device to prevent the transfer of data.
- Not Data Accepted (NDAC)—activated by a listening device to cause the talker to keep the data on the bus and to hold DAV active.

The eight parallel data lines pass device-dependent data and interface management messages.

Implementation of IEEE Standard 488-1975

The GPIB Adapter implements the interface standards of the IEEE Standard 488-1975. The GPIB Adapter utilizes controller interface functions C1, C2, C3, C4, and C25. These functions are described as follows:

C1 GPIB Adapter is the only allowed system controller and provides the control for the generation of the Interface Clear (IFC) and the Remote Enable (REN) interface messages.

C2 This interface function allows the GPIB Adapter the capability to generate the Interface Clear (IFC) message.

C3 This interface function allows the GPIB Adapter the capability to generate the Remote Enable (REN) message.

C4 This interface function allows the GPIB Adapter to respond to Service Requests (SRQ) that are generated by the devices attached to the interface bus. The GPIB Adapter synchronously responds to an active Service Request (SRQ) and generates an attention interrupt to the processor if the adapter is not busy.

C25 This interface function allows the GPIB Adapter to send interface messages, conduct parallel polls, conduct serial polls, and take control synchronously. As controller in charge, it cannot receive control from, or pass control to, another device or itself.

Interface functions are implemented as described in the following:

- Source Handshake (SH1) interface function is used to control the initiation, transmission, and termination of multiline messages in combination with AH1.
- Acceptor Handshake (AH1) interface function in combination with SH1 is used to control the initiation, reception, and termination of

multiline messages. In combination with the SH1 function, AH1 function guarantees an asynchronous transfer of each message byte between a single sending device and one or more receiving devices.

- Talker (T8) interface function is capable of sending configuration and programming information to devices on the interface. This function restricts the GPIB Adapter from responding to a serial poll or being configured in the talk only mode.
- Listener (L4) interface function is capable of receiving device-dependent data as a multiline message from other devices. The GPIB Adapter inhibits configuration in the listen only mode.
- Service Request (SR0) interface function inhibits the GPIB Adapter from generating a Service Request interface message.
- Remote Local (RL0) interface function inhibits the GPIB Adapter from responding to the Remote Enable (REN), Go to Local (GTL), or Local Lock Out (LLO) interface messages. This is consistent with the concept of the GPIB Adapter being the only permitted active controller.
- Parallel Poll (PP0) interface function inhibits the GPIB Adapter from responding to a Parallel Poll sequence because the GPIB Adapter is the only permitted controller.
- Device Clear (DC0) interface function inhibits the GPIB Adapter from responding to a Device Clear message because the GPIB Adapter is the only permitted controller.
- Device Trigger (DT0) interface function inhibits the GPIB Adapter from responding to a Group Execute Trigger (GET) message. This also is consistent with the concept that the GPIB Adapter can be the only active controller.

Data is transferred on the bus in either 7-bit (ASCII) or 8-bit binary format. Data/information/addresses should be right justified by byte in Series/1 main storage. The rate of transfer is determined by the speed with which the sending device (talker) places each byte on the bus (DAV active) and the effective data rate at which the slowest of all receivers (listener) accepts the data byte (NDAC inactive), up to a maximum instantaneous data rate of 65 kilobytes/second. (Data rate is largely dependent upon the block size of the data transferred.)

Chapter 2. Programming and Operations

This chapter describes the I/O commands, control words, and operations which the processor uses to transfer data to and from the attachment. It includes descriptions of the Operate I/O instruction and its associated commands, status words, and condition codes.

The processor initiates I/O operations by issuing an Operate I/O instruction, and then it uses the processor I/O channel to transfer data to and from the attachment. The Operate I/O instruction is a privileged instruction. Its effective address (the combination of the R2 and address fields) points to an immediate device control block (IDCB) in main storage. The IDCB contains an I/O command, a device address, and an immediate data field (see Figure 2-1). The command defines the type of I/O operation; the GPIB device address identifies the device on which the operation is to be performed. The use of the information in the immediate data field depends on the mode of operation. For direct program control (DPC) operations, the immediate data field is used as a data word; for cycle-steal operations, this field points to a device control block (DCB) that contains additional information needed to perform the operation. The IDCB must be on a fullword boundary. Refer to the *IBM Series/1 4955 Processor and Processor Features Description*, GA34-0021, or the *IBM Series/1 4953 Processor and Processor Features Description*, GA34-0022, for a more detailed description.

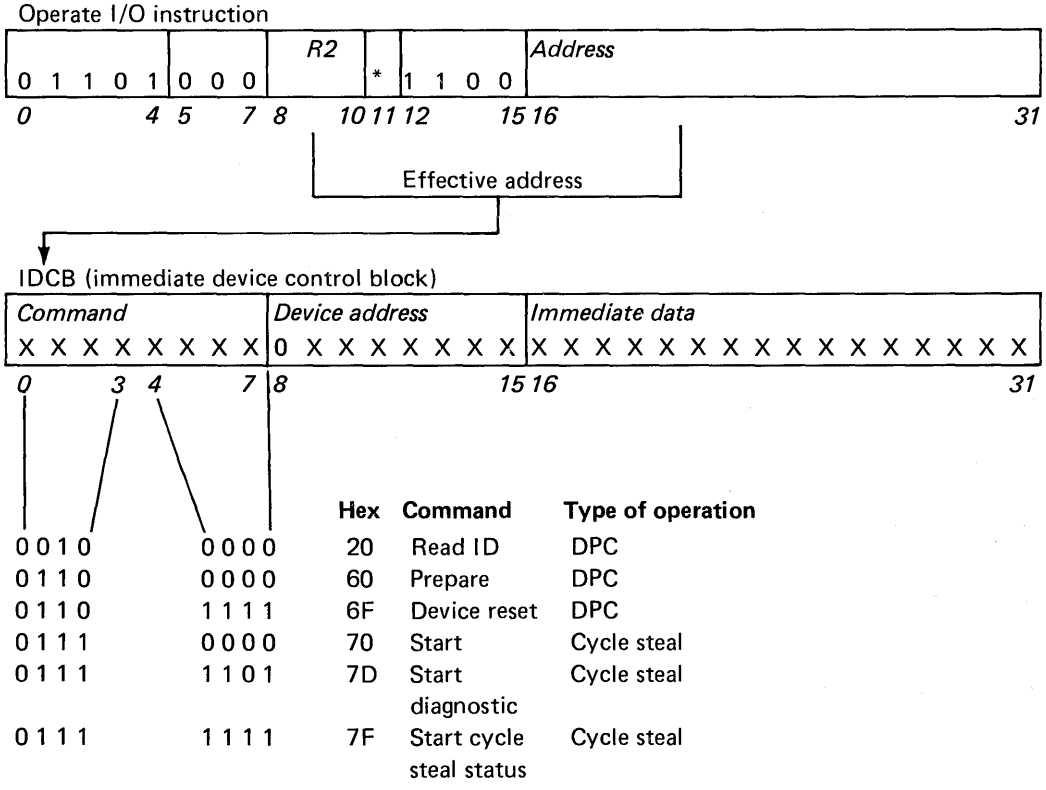


Figure 2-1. Operate I/O instruction and IDCB formats

Direct Program Control (DPC)

A command executed under direct program control causes an immediate transfer of data or control information to or from the attachment. This attachment recognizes only the following DPC-type commands:

Command	Hex	IDCB Immediate Data Field Contents
Read ID	20	Device ID word
Prepare	60	Interrupt parameters
Device Reset	6F	Zeros

An Operate I/O instruction must be executed for each of the above commands. Each execution consists of the following events (see Figure 2-2).

1. The Operate I/O instruction points to an IDCB in main storage. 1
2. The I/O channel uses the IDCB's device-address field 3 to select the device, and the command field 2 to determine the operation to perform.
3. The processor transfers the contents of the immediate data field to the attachment, or transfers information from the attachment to the immediate data field, depending on the command being executed. 4
4. The attachment sends a condition code to the level status register (LSR) in the processor. 5

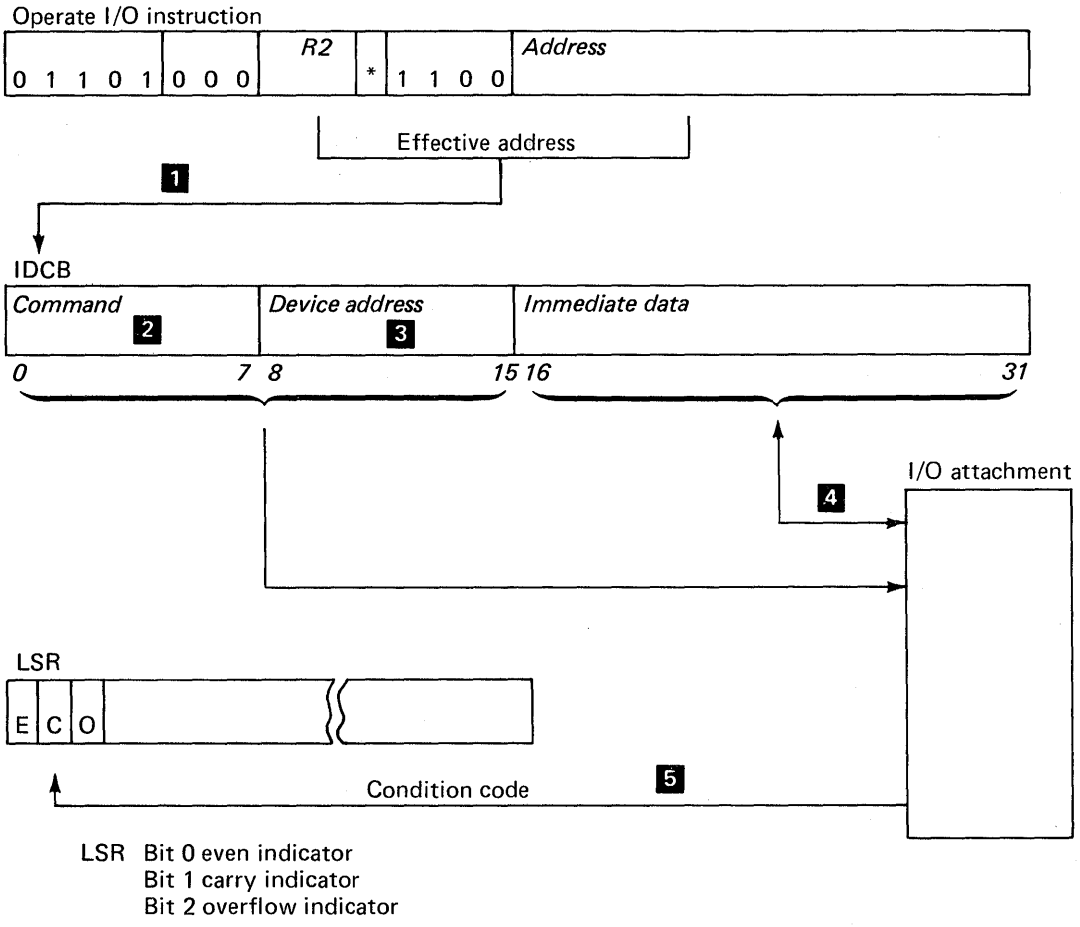


Figure 2-2. Direct program control I/O operation

Read ID Command

The Read ID command transfers an identification (ID) word from the attachment to the immediate data field of the IDCB. For this attachment, the ID word is X'0706'.

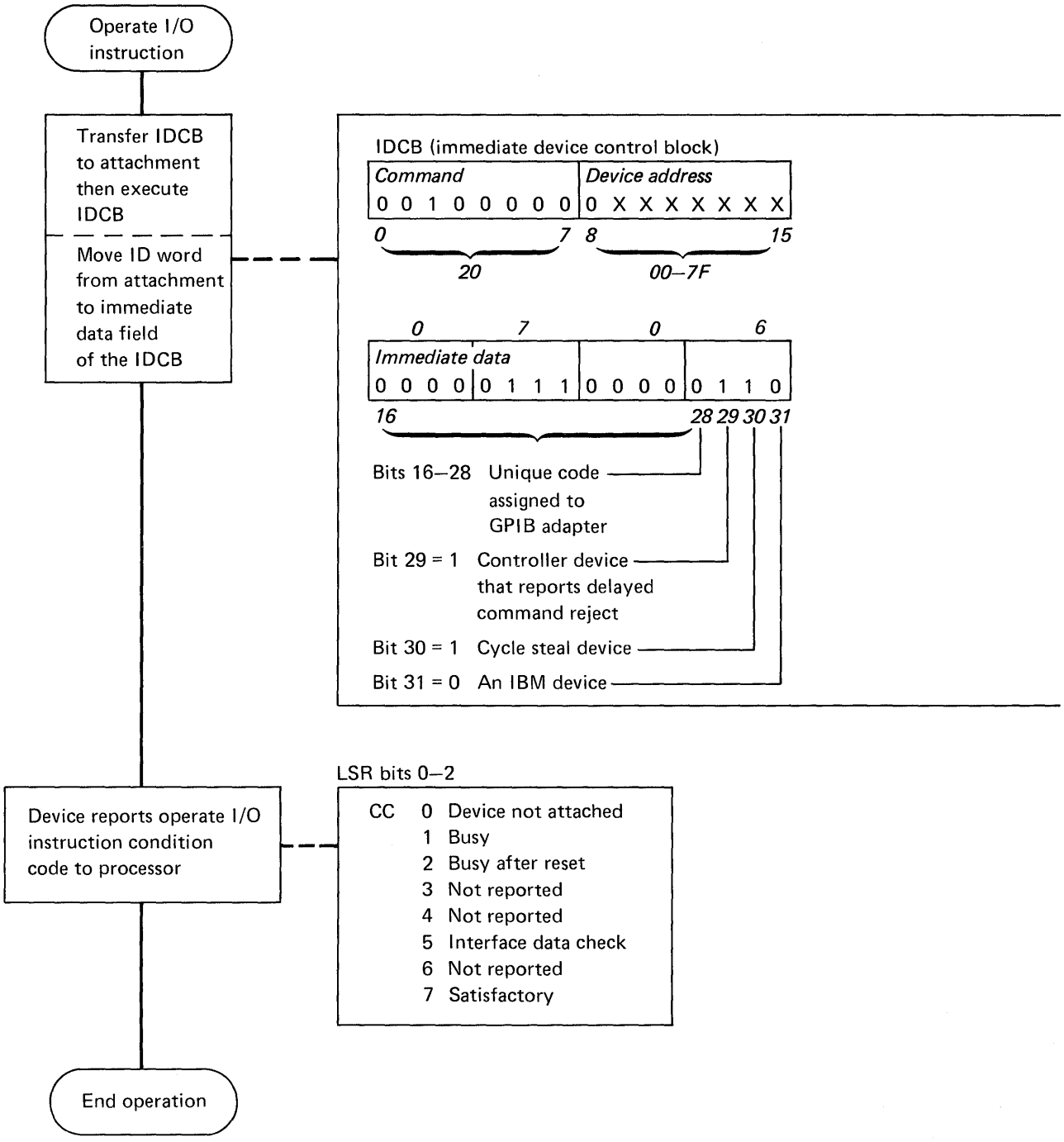


Figure 2-3. Read ID command operation

Prepare Command

Before the attachment can request interrupts, the processor must supply interrupt parameters. The user places these parameters in the IDCB's immediate data field. The Prepare command transfers the parameters to the attachment. The parameters include an interrupt-enable bit to control whether or not the device is allowed to interrupt, and the priority-interrupt level to which the attachment requests interrupt service.

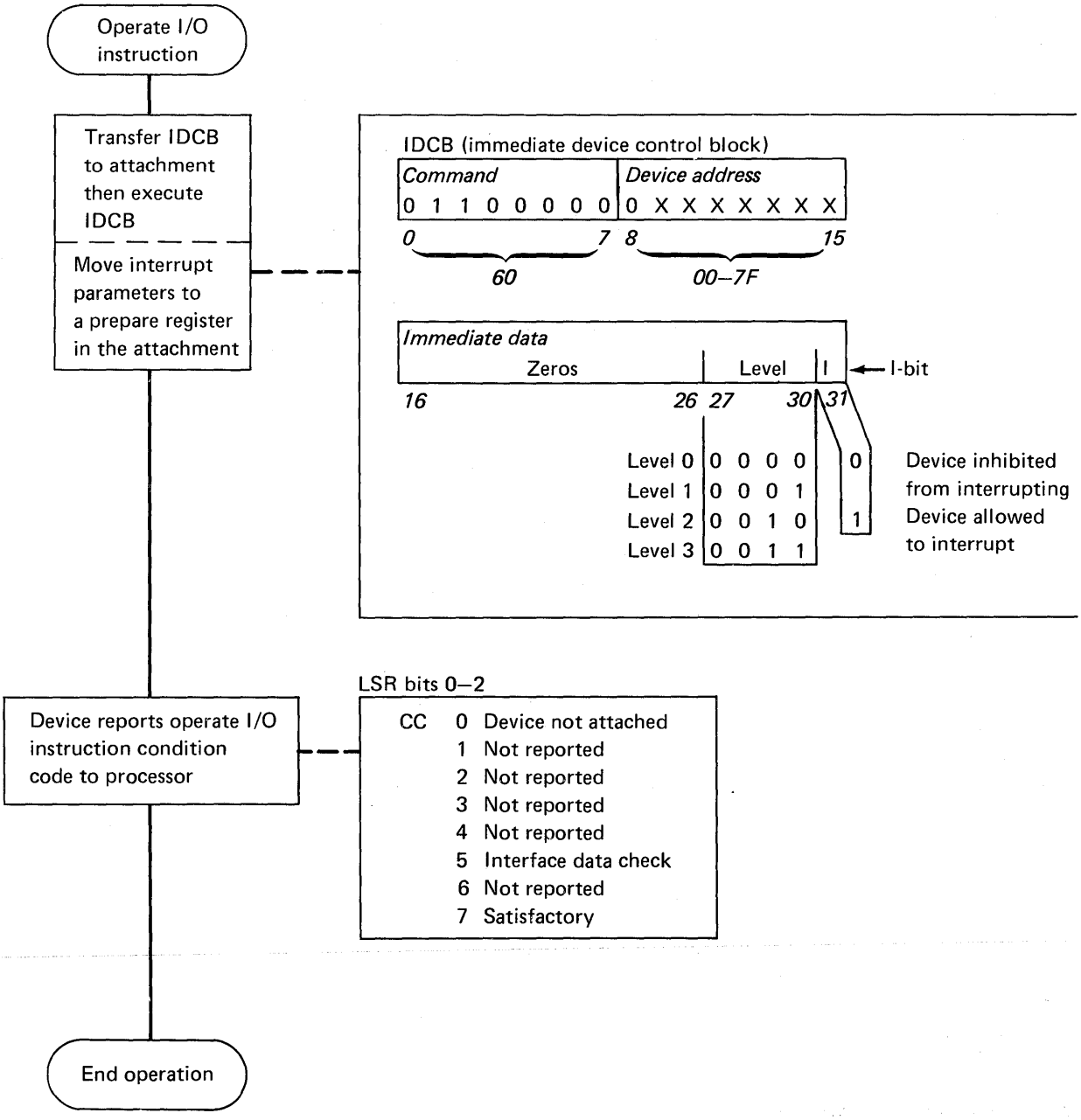


Figure 2-4. Prepare command operation

Device Reset Command

The Device Reset command resets the addressed attachment. Any pending interrupt or busy condition is cleared. The device interrupt-enable bit, the assigned priority level, and the residual address (cycle steal status word 0) are not affected. In addition, the GPIB Adapter generates an IFC message to all devices, forcing the GPIB interface to a known quiescent state.

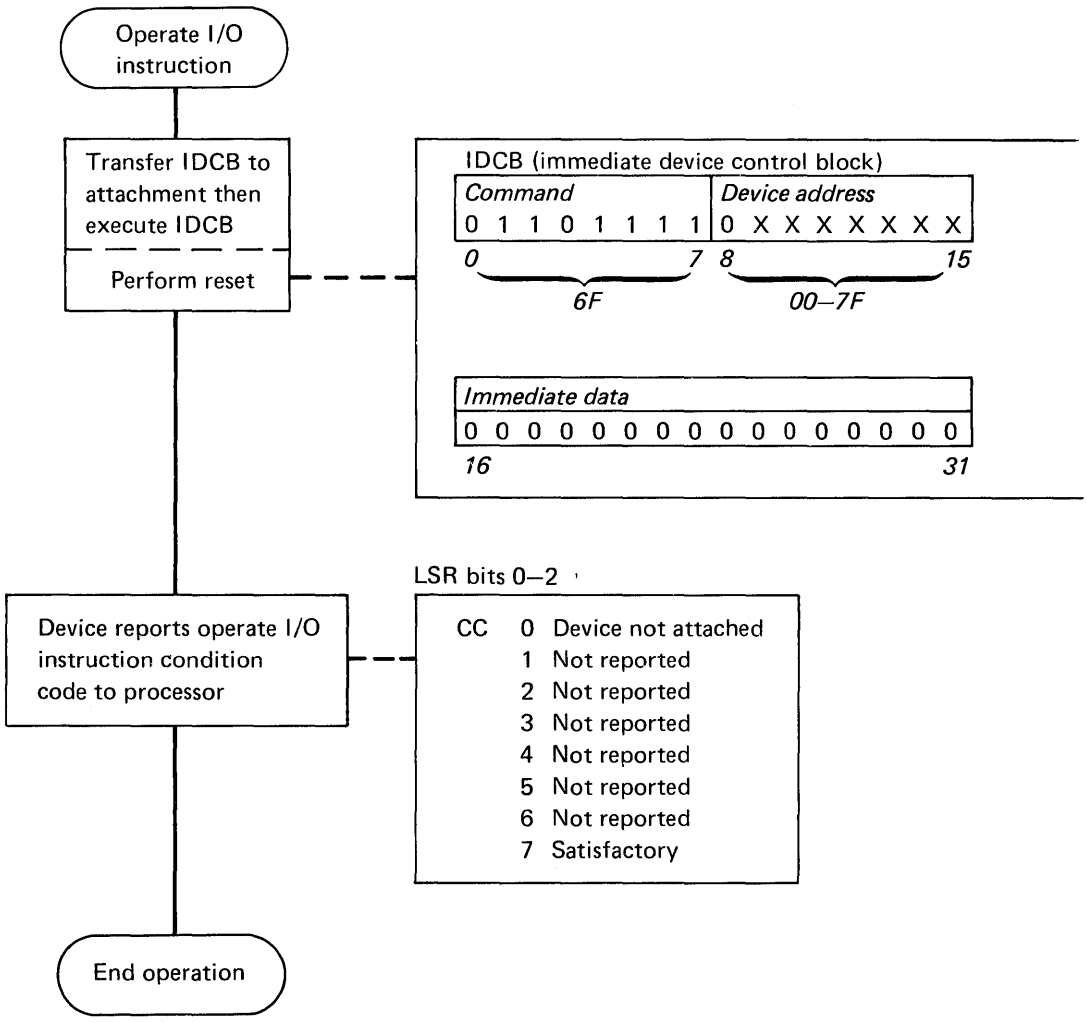


Figure 2-5. Device reset command operation

Cycle Steal

Command execution in cycle steal mode permits overlapping of I/O and other processor operations. The processor transfers the IDCB under direct program control (DPC) from processor storage to the attachment (see Figure 2-6) 1. After the attachment accepts the IDCB:

1. It returns an Operate I/O condition code to the processor 2. The processor is now freed to continue with other operations.
2. The attachment uses the information in the IDCB to execute the command. The IDCB immediate data field contains the address of an 8-word device control block (DCB) defining the operation.
3. The attachment steals the DCB words 3 and data 4 needed to perform the command.
4. Each data transfer reduces a preset byte count in DCB word 6.
5. When the data transfer ends (byte count equals zero), the attachment sends an interrupt request to the processor.

The processor then accepts the interrupt condition code and an interrupt ID word from the attachment.

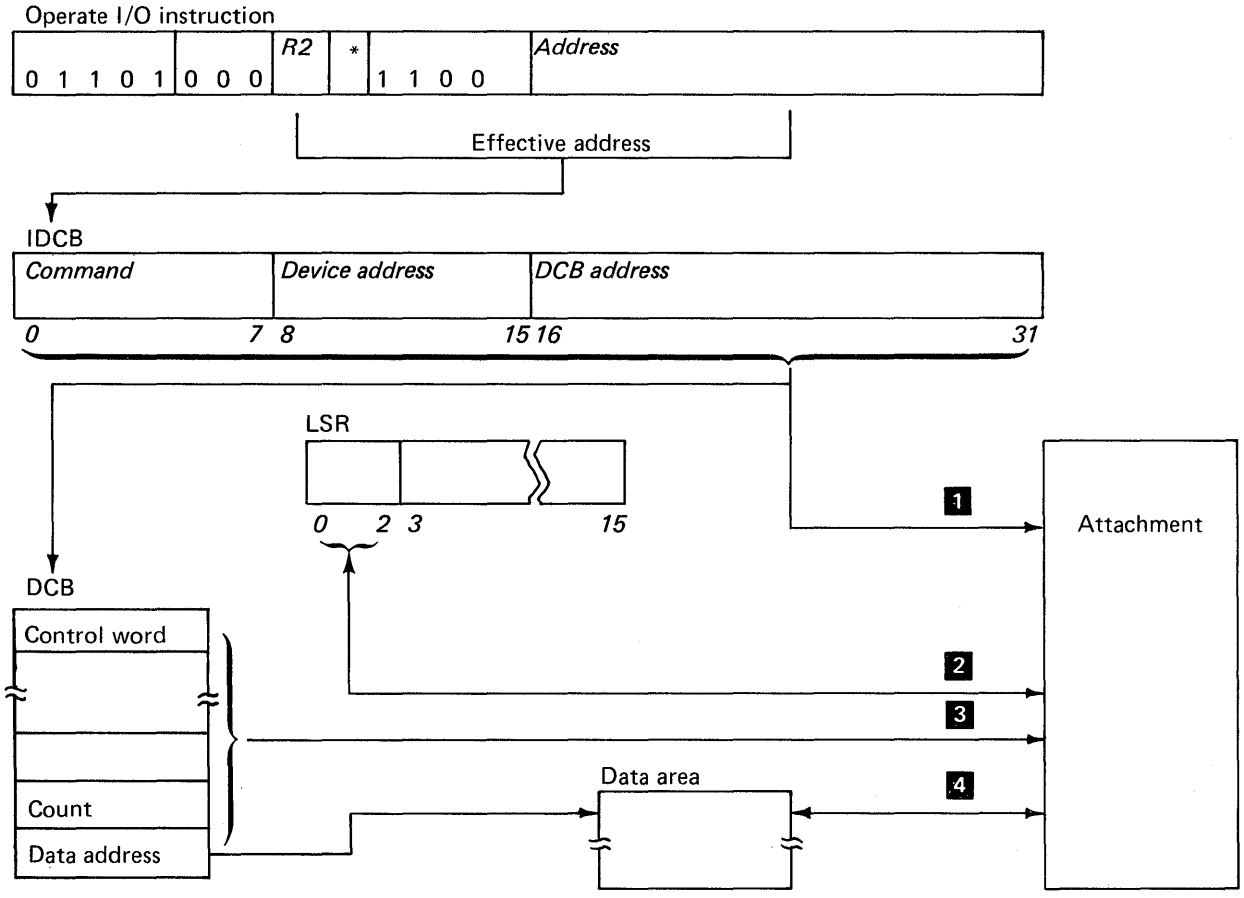


Figure 2-6. Cycle steal operation

Device Control Block (DCB)

Word		
0	Control word	
1	End of string terminator	Reserved
2	Not used (must = 0)	
3	Not used (must = 0)	
4	Residual status block address	
5	DCB chain address	
6	Byte count	
7	Data address	

DCB Word 0—Control Word

CF	PCI	IF	XD	SE	Addr key	EOS	TO	EOI	Device operation
0	1	2	3	4	5 6	7	8	9	10 11 15

Bit 0 Chaining flag. This bit equal to one indicates a DCB chaining operation. After completing the current DCB operation, the attachment will not interrupt but will cycle steal the next DCB pointed to by the chain address contained in word 5 of the current DCB.

Bit 1 PCI bit is not used and must be zero.

Bit 2 Input flag (IF). This bit indicates to the attachment the direction of the data transfer. If the bit equals zero, data transfer is from main storage to the attachment (output). If the bit equals one, data transfer is from attachment to main storage (input).

Bit 3 XD bit is not used and must be zero.

Bit 4 Suppress exception (SE). If this bit is equal to one, the device will suppress the reporting of exception conditions due to incorrect length records (ILR) when using the EOS or EOI terminator conditions in the Read Data or Read Monitor commands. This bit equal to one in any other command will cause a DCB Specification Check condition.

Bits 5–7 Cycle steal address key. This is a program-assigned three-bit processor storage protect access key used by the attachment during data transfers for storage access authorization. (Not used on 4953 processor.)

Bit 8 End of string terminator (EOS). The EOS bit specifies if an end of string terminator byte will be used to indicate completion of the data transfer (DCB word 1 bits 0–7). The EOS terminator allows variable length data transfers to be received without specifying exact transfer byte counts. However, byte count mismatches between received byte counts and DCB specified byte counts when using the EOS terminator will cause an exception condition, which may be suppressed by using the SE bit.

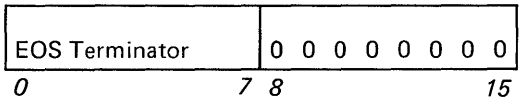
Bit 9 Timer override (TO). An exception interrupt will occur if the data transfer does not complete in 15 milliseconds and bit 9 is equal to a zero. With bit 9 equal to a one, the attachment will wait indefinitely for the data transfer to complete.

Bit 10 End or identify (EOI). Bit 10 equal to a one will cause the EOI line to be raised with the transfer of the last byte of data during a Write Data command. During a Read Data command the EOI bit may be used to monitor the EOI line to terminate the data transfer. This allows variable length data transfers to be received without specifying exact transfer byte counts. However, byte count mismatches between received byte counts and DCB specified byte counts when using the EOI terminator will cause an exception condition, which may be suppressed by using the SE bit.

Bits 11–15 Identify the operation to be performed

00001	Write Interface Clear (IFC)
00010	Write Remote Enable (REN)
00011	Write Configure
00100	Write Data
00101	Write Parallel Poll Enable (PPE)
00110	Write Parallel Poll Disable (PPD)
00111	Write Parallel Poll Unconfigure (PPU)
01000	Write Parallel Poll (PPL)
01001	Write Serial Poll Enable (SPE)
01010	Write Serial Poll Disable (SPD)
01011	Write Selected Device Clear (SDC)
01100	Write Device Clear (DCL)
01101	Write Group Execute Trigger (GET)
01110	Write Go To Local (GTL)
01111	Write Local Lock Out (LLO)
10001	Read Data
10010	Read Serial Poll Results (SPL)
10011	Read Parallel Poll Results (PPL)
10100	Read Monitor

DCB Word 1—End of String Terminator Word



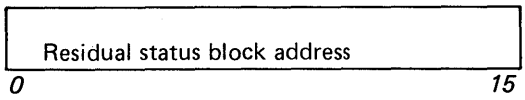
Bits 0–7 The configuration of these bits will be compared with incoming data, a match indicates completion of the data transfer. (The EOS terminator should be right justified by byte.)

Bits 8–15 Not used, must be zero.

DCB Word 2—Not Used, must be zero

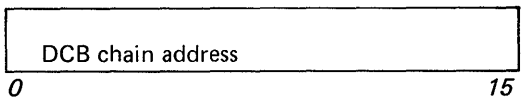
DCB Word 3—Not Used, must be zero

DCB Word 4—Residual Status Block Address



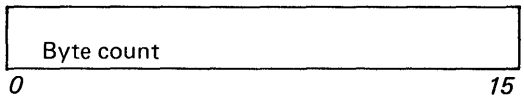
The residual status block address points to the starting location in main storage of residual status for each DCB that has the suppress exception (SE) bit (bit 4 of DCB word 0) equal to a one. The address must be even or a DCB specification check will result.

DCB Word 5—DCB Chain Address



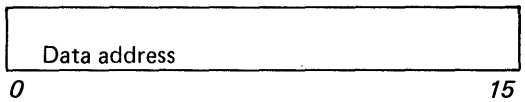
The DCB chain address word specifies the main storage address of the next DCB in the chain. To chain DCBs, set the chaining flag bit in the DCB control word (DCB word 0 bit 0) to a one. The address must be an even number or a DCB specification check will result.

DCB Word 6—Byte Count



The byte count word contains a 16-bit unsigned integer representing the number of data bytes to be transferred for the current DCB. Count is specified in bytes with a range of 0 to 65,535 (X'0000' to X'FFFF').

DCB Word 7—Data Address



The data address word contains the starting main storage address for the data transfer. This starting address may be even or odd when required for data transfers.

Cycle Steal Sequence

Figure 2-7 shows a typical execution sequence of a cycle steal type operation. This sequence applies to Start and Start Cycle Steal status commands.

Start Command

The Start command initiates I/O operations that transfer data to or from processor storage in cycle steal mode. The control information and parameters required for a particular operation must be stored in the DCB associated with each start command.

The operations that are initiated with a Start command are summarized in Figure 2-8 and discussed in the subsequent explanations.

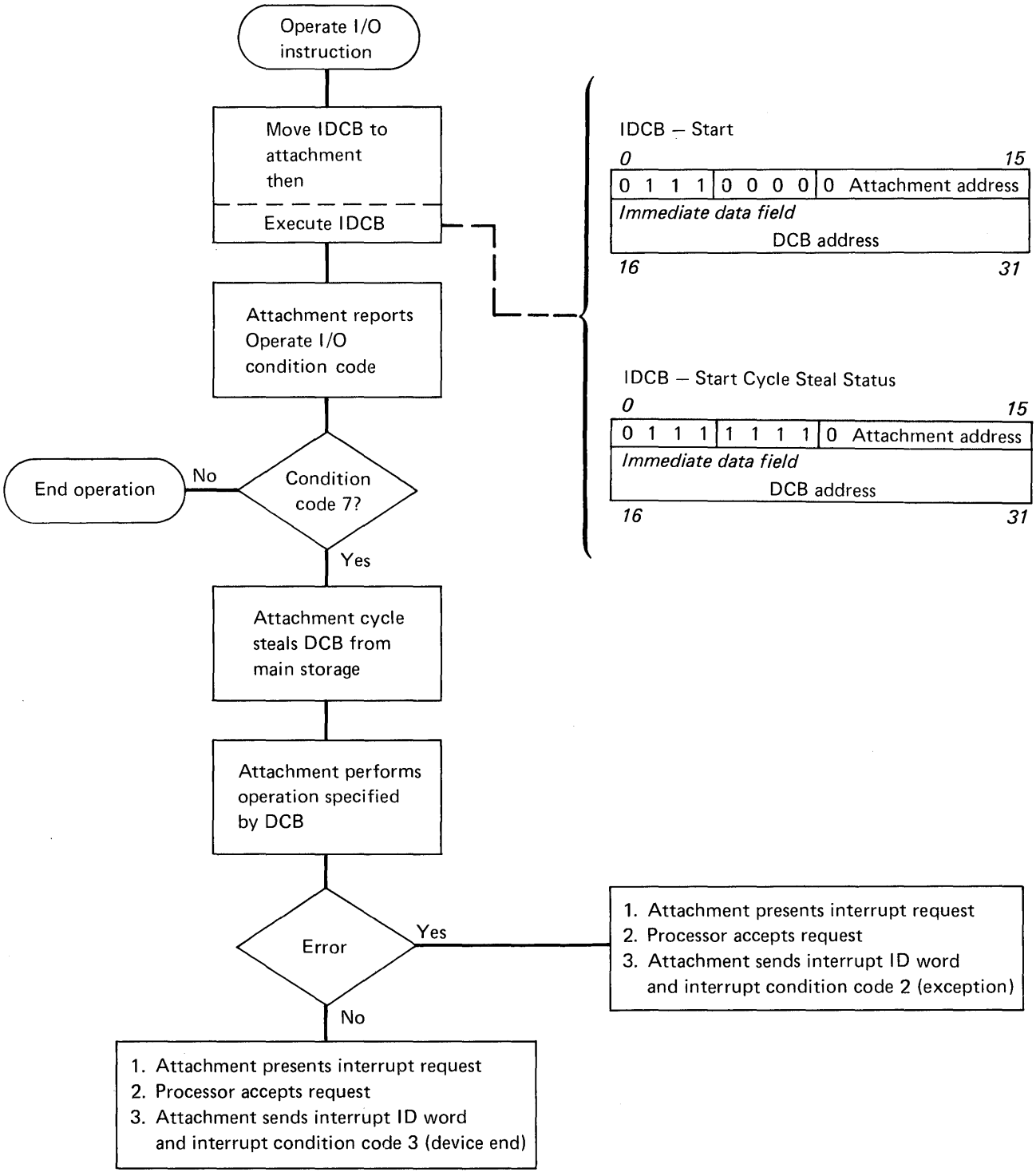


Figure 2-7. Start and Start Cycle Steal Status commands sequence

Bus Initialization Operations

Operation	Bits 11–15 of DCB Word 0	Description of the Operation
Write Interface Clear (IFC)	00001	causes the bus to go into a quiescent state.
Write Remote Enable (REN)	00010	places addresses on the bus. These addresses will allow the specified devices to respond to further operations.

Information Exchange Operations

Operation	Bits 11–15 of DCB Word 0	Description of the Operation
Write Configure	00011	used to transfer configuration information and/or device programming information (if less than 50 bytes) on the bus.
Write Data	00100	places device programming information or data on the bus for those devices addressed as listeners.
Write Parallel Poll Enable (PPE)	00101	puts those devices whose listen addresses are contained in the data area into a response mode.
Write Parallel Poll Disable (PPD)	00110	used to selectively disable those devices whose listen address appears in the data area from participating in a parallel poll sequence.
Write Parallel Poll Unconfigure (PPU)	00111	causes all devices which are currently able to respond to a parallel poll to be forced into a parallel poll idle state.
Write Parallel Poll (PPL)	01000	conducts a parallel poll for those devices configured during the write (PPE) command. One byte of status is returned.
Write Serial Poll Enable (SPE)	01001	provides the devices whose talk addresses are contained in the data area with the capability to present status.
Write Serial Poll Disable (SPD)	01010	disables the serial poll status reporting ability of the devices.
Write Selected Device Clear (SDC)	01011	causes those devices whose addresses that are contained in the data area to be reset.
Write Device Clear (DCL)	01100	causes all devices to be reset.
Write Group Execute Trigger (GET)	01101	causes those devices whose listen addresses are contained in the data area to have their predefined basic operation initiated.
Write Go To Local (GTL)	01110	causes those devices whose listen addresses are contained in the data block to respond to both the interface messages and panel controls.
Write Local Lock Out (LLO)	01111	causes the devices to respond only to interface control messages (not panel controls).
Read Data	10001	allows data to be transferred from a device on the bus into Series/1 main storage.
Read Serial Poll Results (SPL)	10010	reads the results of the latest serial poll into Series/1 main storage (one byte per device).
Read Parallel Poll Results (PPL)	10011	reads the result of the latest parallel poll into Series/1 main storage (one byte).
Read Monitor	10100	allows data to be transferred/monitored between devices on the bus.

Figure 2-8. Summary of operations

Write Interface Clear (IFC)

The Write Interface Clear operation will cause the bus to go into a quiescent state. DCB words 6 and 7 are not checked. (The IFC operation is automatically generated at power on.)

Write Remote Enable (REN)

The Write Remote Enable operation allows those devices, whose listen addresses are specified in the data area pointed to by DCB word 7, to respond to further operations. DCB word 6 (byte count) must equal the number of listen addresses specified from X'0001' to X'000E' (decimal 1 to 14). A DCB specification check will be returned for all other byte counts.

The following is an example of the coding that would be contained in the data area pointed to by Write Remote Enable DCB word 7. DCB word 6 of this example would contain X'000A'.

The data area would be:

Hexadecimal		ASCII	
30	35	0	5
31	32	1	2
33	36	3	6
37	39	7	9
38	34	8	4

Programming Note: Any device which is connected on the interface and which utilizes the Write Remote Enable operation code must be sent this operation code whenever the interface is being used. This procedure must be followed even when that particular device will remain inactive. The Write Remote Enable operation code remains active on the interface only until a Write Interface Clear operation occurs. Consequently, for continued bus activity after a Write IFC operation, another Write Remote Enable operation code must be issued.

Write Configure

The Write Configure operation is used to transfer configuration information and optional device programming information (if less than 100 bytes) on the bus. The data area that is pointed to by DCB word 7 would contain, first, configuration information, followed by an information terminator (X'222C'), then programming information, followed by an information terminator (X'222C'), alternately until the end of the data transfer, indicated by a data block terminator (X'223A'). The byte count in DCB word 6 must be between X'3' and X'64' (decimal 3 to 100), inclusive. The value of this count should allow for configuration information, programming information, and terminators. Any other byte count will cause a DCB specification check.

The following is an example of the coding that would be contained in the data area pointed to by Write Configure DCB word 7. DCB word 6 of this example would contain X'000A'.

The data area would be:

Hexadecimal		ASCII	
3F	35	?	5
33	22	3	"
2C	31	,	1
30	48	0	H
22	3A	"	:

External device address functions are:

External device address		
Hexadecimal	**ASCII**	**Function**
3F	?	Universal bus unlisten command
35	5	Configuration device address
33	3	Configuration device address
22	"	Terminator
2C	,	Terminator
31	1	Program information
30	0	Program information
48	H	Program information
22	"	Data block terminator
3A	:	Data block terminator

The X'3F' (?) is a special interface message to reset all listeners on the interface. The X'35' (5) and X'33' (3) are the listeners that will receive the

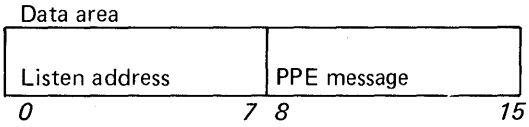
program information X'31 30 48' (10H). (See Appendix F, "Programming Notes", for further information.)

Write Data

The Write Data operation will cause device programming or data to be sent from main storage data area pointed to by DCB word 7 to those devices addressed as listeners.

Write Parallel Poll Enable (PPE)

The Write Parallel Poll Enable operation will automatically execute a PPC operation. In the data area specified by DCB word 7 the first byte of data will contain a listen address followed by a PPE message byte for each device. The PPE message will configure the listeners to respond to a Parallel Poll operation on the eight parallel data lines as follows:



PPE message bits	Meaning
8–11	These bits form a unique code (0110) identifying this as a Parallel Poll Enable operation
12	This is used to define to the adapter which line level (0 or 1) is to be considered the active level for this device.
13, 14, 15	The value on these lines defines which Data Line will be used by a device to request service.

Value on lines 13, 14, 15	Line to be used to request service
0 0 0	Data line 1
0 0 1	Data line 2
0 1 0	Data line 3
0 1 1	Data line 4
1 0 0	Data line 5
1 0 1	Data line 6
1 1 0	Data line 7
1 1 1	Data line 8

The data address specified in DCB word 7 may start on an even or odd byte storage boundary.

Write Parallel Poll Disable (PPD)

The Write Parallel Poll Disable (PPD) operation is used to selectively disable those devices whose listen addresses appear in the data area specified in DCB word 7 from participating in a parallel poll sequence. If during a parallel poll sequence two devices are sharing a parallel data line, by initiating a PPD operation to disable one of the devices and then issuing a Write Parallel Poll, the device that needs servicing can be determined.

Write Parallel Poll Unconfigure (PPU)

The Write Parallel Poll Unconfigure will cause all devices which are currently able to respond to a parallel poll to be forced into a parallel poll idle state. DCB words 6 and 7 are not used.

Write Parallel Poll

The Write Parallel Poll performs a parallel poll of the devices that were previously enabled to respond (by a PPE) and stores this information byte in the attachment. It takes a Read Parallel Poll Result to transfer this information byte into main storage.

Write Serial Poll Enable (SPE)

The Write Serial Poll Enable (SPE) will do a serial poll of each of the devices whose talk address is contained in the data area and stores this information in the attachment. It takes a Read Serial Poll Results (SPL) to transfer the results into main storage. The data area start address is contained in DCB word 7.

DCB word 6 (byte count) must equal the number of talk addresses specified from X'0001' to X'000E' (decimal 1 to 14). A DCB specification check will be returned for all other byte counts.

Write Serial Poll Disable (SPD)

The Write Serial Poll Disable will disable the serial poll status reporting ability of the devices previously enabled. The SPD operation should be issued after a SPE operation to ensure that a talker does not talk with status information.

Write Selected Device Clear (SDC)

The Write Selected Device Clear will cause those devices whose listen addresses are contained in the data area to be internally reset or initialized (depending on the device). The starting address of the data area is contained in DCB word 7. DCB word 6 (byte count) must equal the number of listen addresses specified from X'0001' to X'000E' (decimal 1 to 14). A DCB specification check will be returned for all other byte counts.

Write Device Clear (DCL)

The Write Device Clear (DCL) will cause all devices to be initialized. The initialized state is device-dependent.

Write Group Execute Trigger (GET)

The Write Group Execute Trigger (GET) causes those devices whose listen addresses are contained in the data area specified by DCB word 7 to have their predefined basic operation initiated (depending on the device).

Write Go To Local (GTL)

The Write Go To Local (GTL) causes those devices whose listen address is contained in the data area specified by DCB word 7 to be placed in a state where the device is capable to respond to both interface messages and the device panel controls.

Write Local Lock Out (LLO)

The Write Local Lock Out (LLO) disables the use of the device panel controls of previously configured listeners.

Read Data

The Read Data allows data to be transferred from a device (previously addressed as a talker) on the bus into main storage. Any device addressed as a listener will receive the data transfer also.

Read Serial Poll Results (SPL)

The Read Serial Poll Results (SPL) reads the results of the latest serial poll that was stored in the attachment by the SPE operation into main storage. The data block in main storage will contain first the talk address followed by a status byte for that talk address and so forth. DCB word 6 (byte count) must equal even byte counts from X'0002' to X'001C' (decimal 2 to 28). A DCB specification check will be returned for all other byte counts.

Programming Note: If no Write (SPE) was issued prior to the Read (SPL), an exception interrupt will be issued. Cycle steal Status Word 3 will have bit 06 on.

Read Parallel Poll Results (PPL)

The Read Parallel Poll Results reads the result of the latest Write Parallel Poll (PPL) into main storage. The following is the configuration of this byte:

Bit 0 = Data line 8
Bit 1 = Data line 7
Bit 2 = Data line 6
Bit 3 = Data line 5
Bit 4 = Data line 4
Bit 5 = Data line 3
Bit 6 = Data line 2
Bit 7 = Data line 1

Read Monitor

The Read Monitor allows data to be transferred between devices on the bus. One device must have been previously addressed as a talker and at least one as a listener by a Write Configure operation.

Start Cycle Steal Status Command

The Start Cycle Steal Status Command initiates a cycle steal operation to obtain residual parameters from the attachment if the previous cycle steal operation terminated due to an error, exception condition, or any time residual status is desired.

Cycle Steal Status Word 0—Residual Address

The Residual Address word contains the main storage address of the last attempted cycle steal transfer associated with a Start command. If an error occurs during a Start Cycle Steal Status operation, this address is not altered. The residual address may be a data address, a DCB address, or a residual status block address and is cleared only by a power on reset.

Cycle Steal Status Word 1—Residual Byte Count

The Residual Byte Count word is the byte count of the last cycle steal operation less the number of bytes successfully transferred.

Cycle Steal Status Word 2—Reserved

Cycle Steal Status Word 3—Reserved

Cycle Steal Status Word 4—Error Status

Bit 0	Bus timed out on Acceptor Handshake. The attachment was attempting to receive data from the bus.
Bit 1	Reserved
Bit 2	Bus timed out on Source Handshake. The attachment was attempting to send data to the bus.
Bit 3	Reserved
Bit 4	The attachment was receiving data from the bus and waiting for an end-of-string character. The byte count became exhausted before the end-of-string character was encountered.
Bit 5	The attachment was receiving data from the bus and the byte count became exhausted before the EOI line was raised concurrent with a byte transfer.
Bit 6	A Read Serial Poll was issued before a Write Serial Poll Enable
Bit 7	A Read Parallel Poll was issued before a Write Parallel Poll Enable.
Bit 8	The IFC operation failed to clear the bus.
Bit 9	Invalid data block terminator.
Bit 10	Erroneous IFC detected.
Bits 11–15	Not used.

Cycle Steal Status Word 5

This word shows the status of the bus after a power-on reset.

Bit 0 = Data line 8
Bit 1 = Data line 7
Bit 2 = Data line 6
Bit 3 = Data line 5
Bit 4 = Data line 4
Bit 5 = Data line 3
Bit 6 = Data line 2
Bit 7 = Data line 1
Bit 8 = IFC line
Bit 9 = ATN line
Bit 10 = REN line
Bit 11 = EOI line
Bit 12 = SRQ line
Bit 13 = NRFD line
Bit 14 = NDAC line
Bit 15 = DAV line

Cycle Steal Status Word 6

This word shows the current status of the bus.

Bit 0 = Data line 8
Bit 1 = Data line 7
Bit 2 = Data line 6
Bit 3 = Data line 5
Bit 4 = Data line 4
Bit 5 = Data line 3
Bit 6 = Data line 2
Bit 7 = Data line 1
Bit 8 = IFC line
Bit 9 = ATN line
Bit 10 = REN line
Bit 11 = EOI line
Bit 12 = SRQ line
Bit 13 = NRFD line
Bit 14 = NDAC line
Bit 15 = DAV line

Cycle Steal Status Word 7

This word contains the ASCII address (bits 9–15) of the device on the interface which most recently posted active status during the Write Serial Poll Enable command.

Cycle Steal Status Word 8

Bits 0–3 indicate the cause of the DCB specification check.

Bits 0–3

0000	Not used
0001	Odd DCB address
0010	Invalid PCI bit
0011	Invalid IF bit
0100	Invalid XD bit
0101	Invalid SE bit
0110	Invalid EOS bit
0111	Invalid timer bit
1000	Invalid EOI bit
1001	Non-zero unused word
1010	Odd RSB address
1011	Odd chaining address
1100	Invalid byte count
1101	Invalid command code for configuration
1110	Not used
1111	Not used

Cycle Steal Status Word 9

Not used.

Cycle Steal Status Word 10

This word will contain the starting address of the last DCB used by the attachment.

Condition Codes

Operate I/O

Condition codes are reported after execution of each Operate I/O instruction. See Figure 2-9. The appropriate condition code is transferred into the even, carry, and overflow bit positions of the level status register (LSR) in the processor.

Command	CC0	CC1	CC2	CC3	CC4	CC5	CC6	CC7
Read ID	X	X	X			X		X
Prepare	X					X		X
Device reset	X							X
Start	X	X	X			X		X
Start cycle steal status	X	X	X			X		X

CC Value	*Meaning*
0	Device not attached
1	Busy
2	Busy after reset
3	Command reject
4	Intervention required (not reported)
5	Interface data check
6	Controller busy (not reported)
7	Satisfactory

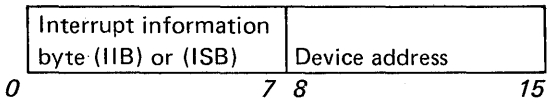
Figure 2-9. Condition code responses to Operate I/O instructions

Interrupt

Interrupt condition codes pertain to operations that continue beyond execution of the Operate I/O instruction (such as cycle stealing of data). The condition codes reported are:

CC Value	*Meaning*
2	Exception
3	Device end
4	Attention
6	Attention and Exception

Along with the interrupt condition code the attachment also transfers an interrupt ID word to the processor. Bits 0–7 of the interrupt ID word comprise an interrupt information byte (IIB). Bits 8–15 are the device address.



For a condition code of 3 (device end), bit 0 of the IIB equal to one indicates that an error retry has occurred. When a condition code of 4 (attention) or 6 (attention and exception) occurs, bit 1 of the IIB equal to one indicates that a device has requested service.

For interrupt condition code of 2 the IIB has a special format and is called an interrupt status byte (ISB). The ISB is coded as follows:

Bit 0 *Device dependent status available.* When set to one this bit signifies that further status is available. This status is obtained using the Start Cycle Steal Status command. This bit is one for incorrect length records and when an error was encountered during execution of the on-line diagnostic test.

Bit 1 *Delayed command reject.* This bit is set to one if the device cannot execute the command due to one of the following conditions:

1. The IDCB contains an incorrect parameter. Examples are (a) an odd-byte DCB address, or (b) an incorrect function/modifier combination.
2. The present state of the device, such as 'not ready' condition, prevents execution of an I/O command specified in the IDCB.

Delayed command reject is set in the ISB only if the device cannot report an appropriate I/O instruction condition code for the condition. The operation is terminated. DCB is not fetched.

Bit 2 *Incorrect length record.* This bit is set to one when the attachment encounters a mismatch between byte count and actual record length after beginning execution of the DCB. This exception condition may be suppressed by using the SE bit.

Bit 3 *DCB specification check.* This bit is set to one when the device cannot execute a command due to an incorrect parameter specification in the DCB. Examples are:

1. An odd-byte DCB chaining or status address.
2. The byte count is odd for a word-only device.
3. An odd-byte data address for a word-only device.
4. An invalid command or invalid bit settings in the control word.
5. An incorrect count.

The operation is terminated.

Bit 4 *Storage data check.* This error condition applies to cycle steal output operations only. If the bit is set to one, it indicates that the main storage location accessed during the current output cycle contained bad parity. Parity in main storage is not corrected. The attachment terminates the operation. The bad parity data is not transferred to the I/O data bus. No machine check condition occurs.

Bit 5 *Invalid storage address.* When set to one, this bit indicates that during a cycle steal operation, the attachment has presented a main storage address that is outside the storage size of the system. The operation immediately terminates.

Bit 6 *Protect check.* When set to one, this bit indicates that the attachment attempted to access a main storage location and presented an incorrect address key.

Bit 7 *Interface data check.* When set to one, this bit indicates that a parity error is detected on the I/O interface during a cycle steal data transfer. The operation immediately terminates.

Residual Status Block (RSB)

When suppress exception (SE) bit (bit 4 of DCB word 0) is used, automatic logging of status information is provided by storing information called the residual status block into main storage. DCB word 4 provides the starting main storage address for the residual status block. Note that a residual status block is stored even if there are no exception conditions to be suppressed. There are five residual status block words for this attachment and the meanings are as follows:

Residual Status Block Word 0—This word will reflect the unused byte count during cycle steal operations.

Residual Status Block Word 1—This word contains the RSB flags. Bit assignments are:

Bit 0	End of Chain Indicator—This bit signifies the last OIO of the chaining operation.
Bits 1–14	Will be zero.
Bit 15	No Exception—This bit will be 1 if no errors were found during the execution of this OIO.

Residual Status Block Word 2—Reserved

Residual Status Block Word 3—Reserved

Residual Status Block Word 4—Reserved

Chapter 3. Installation Planning

Physical Configuration

The circuit card for the GPIB Adapter (RPQ D02118) is housed within the Series/1 processor or the I/O expansion unit in a position appropriate for a device attachment. See Figure 3-1.

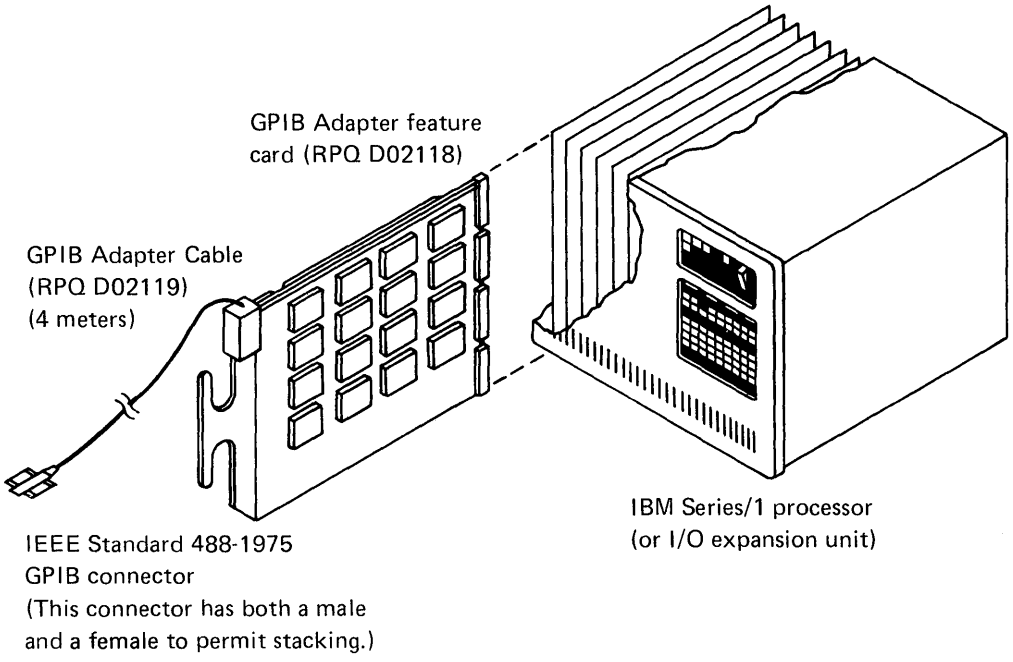


Figure 3-1. GPIB adapter

Cabling

The GPIB Adapter cable (RPQ D02119) is a 4-meter cable. It may be used only from the attachment card to a single I/O device. Additional cabling to extend the GPIB interface to other I/O devices will not be supplied by the IBM Corporation; it must be acquired and maintained by the user. Total cable length must not exceed the lesser of 20 meters or two meters times the number of devices attached.

Note: Internal cable routing in a 1.8 meter rack, with the processor mounted at the top, would use a maximum cable length of 2.5 meters (8.2 feet). See Figure 3-2.

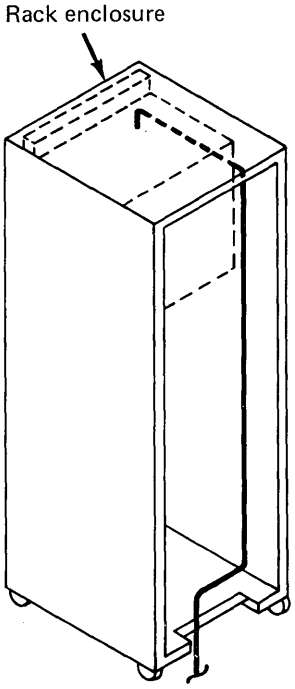
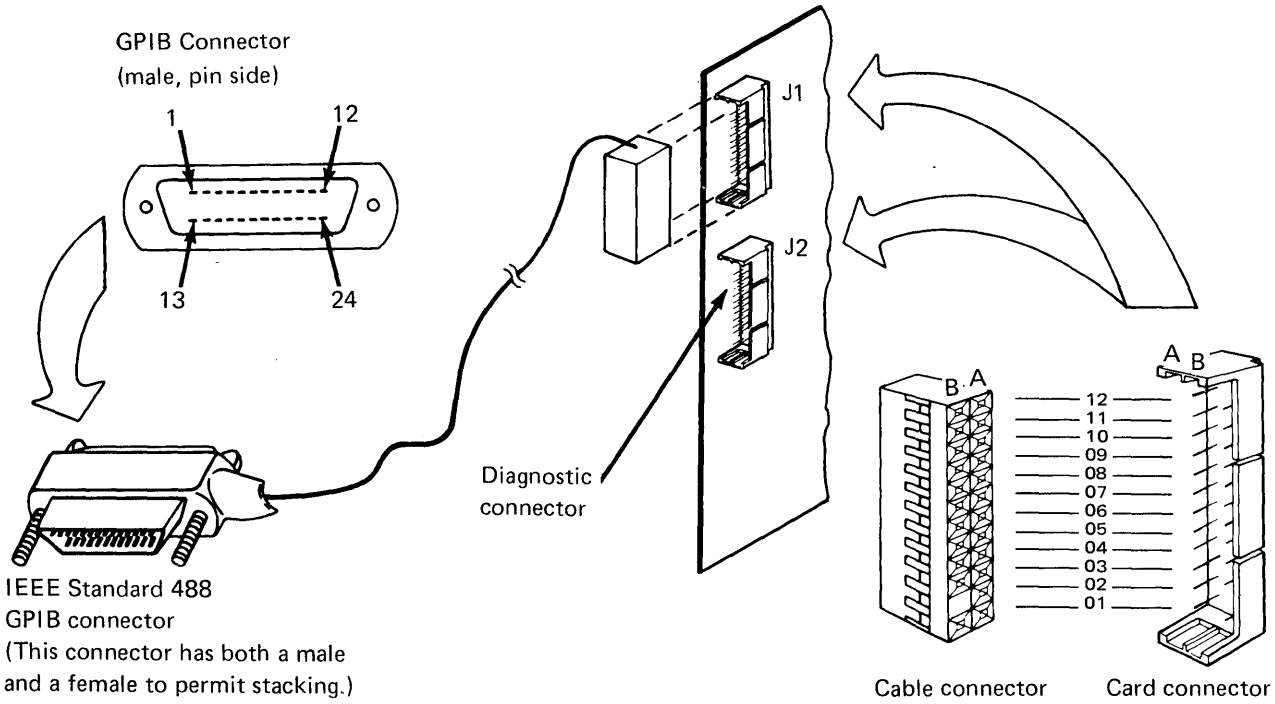


Figure 3-2. Cable routing

Cable Connections

Cable connection information, including pin designations, is given in Figure 3-3.



GPIB connector pins	Line name	J1 & J2 connector pins
1	DIO 1	A12
2	DIO 2	A11
3	DIO 3	A10
4	DIO 4	A09
5	End or Identify (EOI)	A08
6	Data Valid (DAV)	A07
7	Not Ready for Data (NRFD)	A06
8	Not Data Accepted (NDAC)	A05
9	Interface Clear (IFC)	A04
10	Service Request (SRQ)	A03
11	Attention (ATN)	A01
12	Shield (ground)	B02
13	DIO 5	B12
14	DIO 6	B11
15	DIO 7	B10
16	DIO 8	B09
17	Remote Enable (REN)	B08
18	DAV Ground	B07
19	NRFD Ground	B06
20	NDAC Ground	B05
21	IFC Ground	B04
22	SRQ Ground	B03
23	ATN Ground	B01
24	Logic Ground	A02

Figure 3-3. Cable connections

Appendix A. ASCII Conversion Chart

ASCII character	Hexadecimal equivalent
NUL	00
SOH	01
STX	02
ETX	03
EOT	04
ENQ	05
ACK	06
BEL	07
BS	08
HT	09
LF	0A
VT	0B
FF	0C
CR	0D
SO	0E
SI	0F
DLE	10
DC1	11
DC2	12
DC3	13
DC4	14
NAK	15
SYN	16
ETB	17
CAN	18
EM	19
SUB	1A
ESC	1B
FS	1C
GS	1D
RS	1E
US	1F

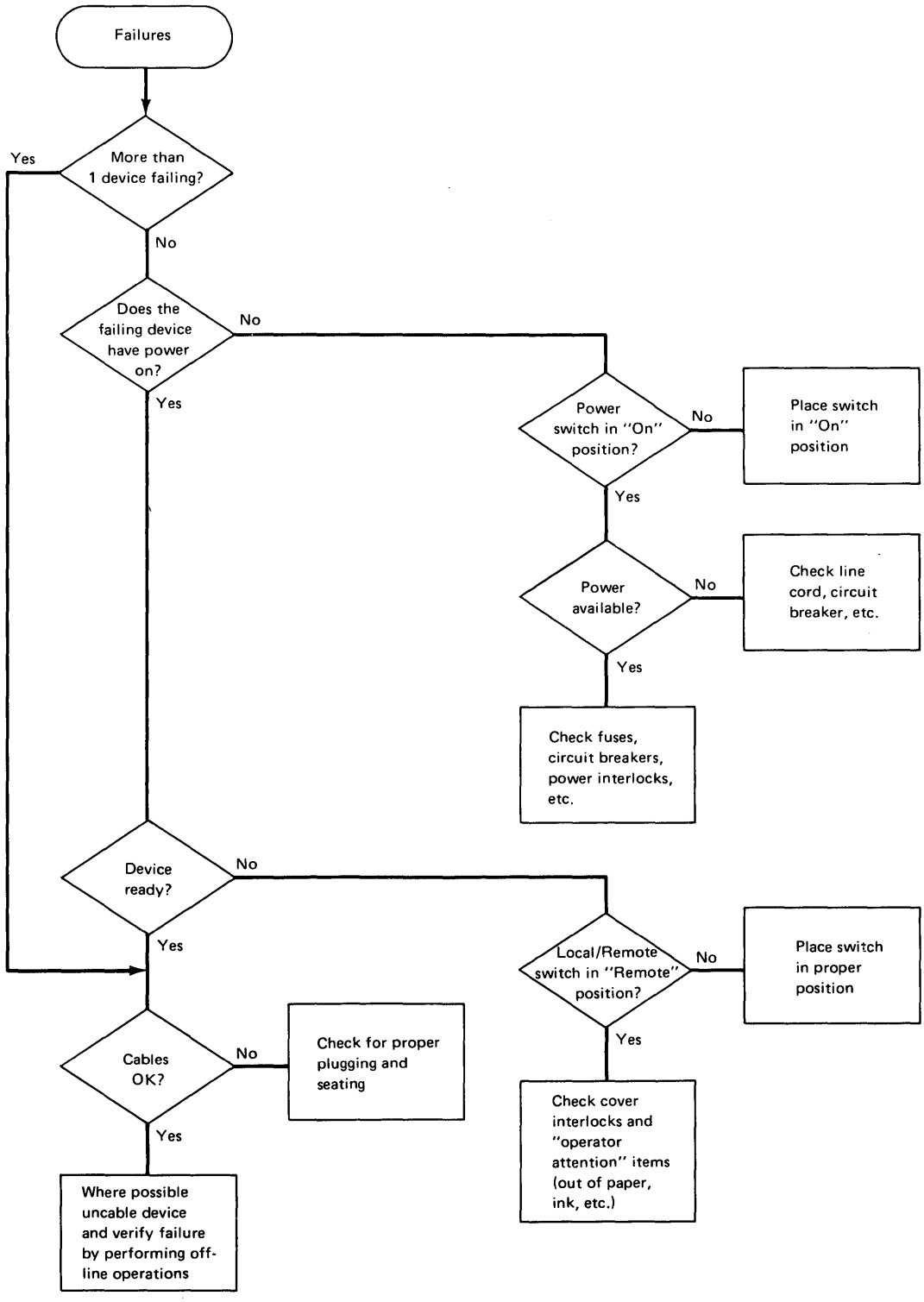
ASCII character	Hexadecimal equivalent
SP	20
!	21
"	22
#	23
$	24
%	25
&	26
'	27
(	28
)	29
*	2A
+	2B
,	2C
–	2D
.	2E
/	2F
0	30
1	31
2	32
3	33
4	34
5	35
6	36
7	37
8	38
9	39
:	3A
;	3B
<	3C
=	3D
>	3E
?	3F

ASCII character	Hexadecimal equivalent
@	40
A	41
B	42
C	43
D	44
E	45
F	46
G	47
H	48
I	49
J	4A
K	4B
L	4C
M	4D
N	4E
O	4F
P	50
Q	51
R	52
S	53
T	54
U	55
V	56
W	57
X	58
Y	59
Z	5A
[	5B
\	5C
]	5D
^	5E
_	5F

ASCII character	Hexadecimal equivalent
`	60
a	61
b	62
c	63
d	64
e	65
f	66
g	67
h	68
i	69
j	6A
k	6B
l	6C
m	6D
n	6E
o	6F
p	70
q	71
r	72
s	73
t	74
u	75
v	76
w	77
x	78
y	79
z	7A
{	7B
|	7C
}	7D
~	7E
DEL	7F

(X'3F') ? is a special interface message to reset all listeners on the interface.
(X'5F') _ is a special interface message to reset all talkers on the interface.

Appendix B. Problem Determination



Appendix C. Line Definitions

Bus Management Lines

Attention (ATN). A controller generated signal that indicates that configuration information is appearing on the interface.

End Or Identify (EOI). A signal used by a talker to indicate the last byte of a block of information.

Interface Clear (IFC). A controller generated signal that clears the interface and puts all devices in a known quiescent mode of operation.

Remote Enable (REN). A controller generated signal that enables devices to be remotely controlled by the interface controller.

Service Request (SRQ). A device generated signal used to inform the controller that service is required.

Handshake Lines

Data Valid (DAV). A signal line issued by the talker when all active devices have indicated a 'ready to accept data' mode of operation.

Not Data Accepted (NDAC). A signal line issued by the listener when it is ready to accept the next byte of information.

Not Ready For Data (NRFD). A signal issued by a listener when it is not ready to accept the next byte of information.

Data Lines

Data Lines 1 Through 8 (DIO 1–DIO 8). Bidirectional signal lines used to transfer all information over the interface. DIO 8 is the most significant bit and DIO 1 is the least significant bit.

Appendix D. Specification Command and Address Groups

Primary Commands

ASCII Codes X'00' to X'5F'

Group	ASCII codes	Examples
Addressed Command Group	X'00' to X'0F'	line feed, carriage return, null
Univeral Command Group	X'10' to X'1F'	home, clear screen
Listen Address Group	X'20' to X'3E'	
Unlisten Address	X'3F'	
Talk Address Group	X'40' to X'5E'	
Untalk Address	X'5F'	

Secondary Command

ASCII Codes X'60' to X'7F'

Appendix E. Diagnostic Commands

Diagnostic commands are used to verify correct operation of the GPIB Adapter. These commands are executed during the diagnostic MAP sequence and provide actual attachment internal testing results. The following commands compose the diagnostic command group.

Diagnostic 1

This command causes an internal microdiagnostic test to be performed on the microprocessor, the memory modules, and the Series/1 interface modules.

Diagnostic 2

This command causes an internal microdiagnostic test to be performed on the device-dependent logic which is associated with the GPIB Adapter operation.

Diagnostic 3

This command causes a microdiagnostic test to be performed on the GPIB Adapter driver/receiver modules. This test manipulates actual bus signal lines and should be used only with the IEEE-488 devices disconnected.

Diagnostic 4

This command causes a microdiagnostic test to be performed on the GPIB Adapter associated cable. This test requires that a cable wrap connector be installed and all devices be removed from the interface.

Diagnostic Read Jumpers

This diagnostic command is used to confirm that the jumpers have been installed correctly on the attachment card.

Diagnostic Patch Command

This command is used to modify attachment storage.

Note: Since this command will modify the attachment function, it should be used only under direct authorization of Series/1 product engineering, General Systems Division of the IBM Corporation.

Diagnostic Command Structure

These commands operate under the cycle steal mode and should be generated and executed as described in the cycle steal portion of this document. The DCB structure should be as follows:

Word	
0	Control word
1	Reserved (must = 0)
2	Reserved (must = 0)
3	Reserved (must = 0)
4	Reserved (must = 0)
5	Reserved (must = 0)
6	Byte count
7	Data address

DCB Word 0—Control Word

0	0	1	0	0	Addr key	0	0	0	Diag. operation
0	1	2	3	4	5 6 7	8	9	10	11 15

Bit 0 This bit is not used and must be zero.

Bit 1 This bit is not used and must be zero.

Bit 2 Input flag (IF). This bit is used and must be one.

Bit 3 This bit is not used and must be zero.

Bit 4	This bit is not used and must be zero.
Bits 5–7	Cycle steal address key. This is a program-assigned 3-bit processor storage protect access key used by the attachment during data transfers for storage access authorization.
Bit 8	This bit is not used and must be zero.
Bit 9	This bit is not used and must be zero.
Bit 10	This bit is not used and must be zero.
Bits 11–15	Identify the diagnostic operation to be performed: 11010 Diagnostic Read Jumper 11011 Diagnostic Patch Command 11100 Diagnostic 1 11101 Diagnostic 2 11110 Diagnostic 3 11111 Diagnostic 4

DCB Word 1—Not Used, Must be Zero

DCB Word 2—Not Used, Must be Zero

DCB Word 3—Not Used, Must be Zero

DCB Word 4—Not Used, Must be Zero

DCB Word 5—Not Used, Must be Zero

DCB Word 6—Byte Count

The following hex codes are required for the associated command. All other codes will result in a DCB specification check.

Diagnostic 1	X'000C'
Diagnostic 2	X'0004'
Diagnostic 3	X'0004'
Diagnostic 4	X'0004'
Diagnostic Read Jumper	X'0002'
Diagnostic Patch	X'XXXX'

DCB Word 7—Data Address

The data address word contains the starting main storage address for the data transfer. This starting address must be located on an even word boundary in Series/1 main storage.

Diagnostic Command Results

After completion of a diagnostic command, the microdiagnostic testing results can be interpreted to determine correct functional operation. The results of each diagnostic command are as follows.

Diagnostic 1

Yields six words of status in the following format:

Word 1—Channel Test Word 1
- Pass—X'5555'
- Fail—X'D555'

Word 2—Channel Test Word 2
- Pass—X'AAAA'
- Fail—X'2AAA'

Word 3—Memory Module 1 Test
- Pass—Part number of memory module 1
- Fail—X'FXXX'

Word 4—Memory Module 2 Test
- Pass—Part number of memory module 2
- Fail—XFXXX'

Word 5—Memory Module 3 Test
- Pass—Part number of memory module 3
- Fail—X'FXXX'

Word 6—Memory Test Results on Module 4
- Pass—X'0000'
- Fail—X'XXXX' (non-zero)

Diagnostic 2

Yields two words of status in the following format:

Word 1—Device Logic Test Word 1
- Pass—X'0000'
- Fail—X'1XXX'

Word 2—Device Logic Test Word 2
- Pass—X'0000'
- Fail—X'1XXX'

Diagnostic 3

Yields two words of status in the following format:

Word 1—Device Logic Test Word 1
- Pass—X'0000'
- Fail—X'1XXX'

Word 2—Device Logic Test Word 2
- Pass—X'0000'
- Fail—X'XXXX'

Diagnostic 4

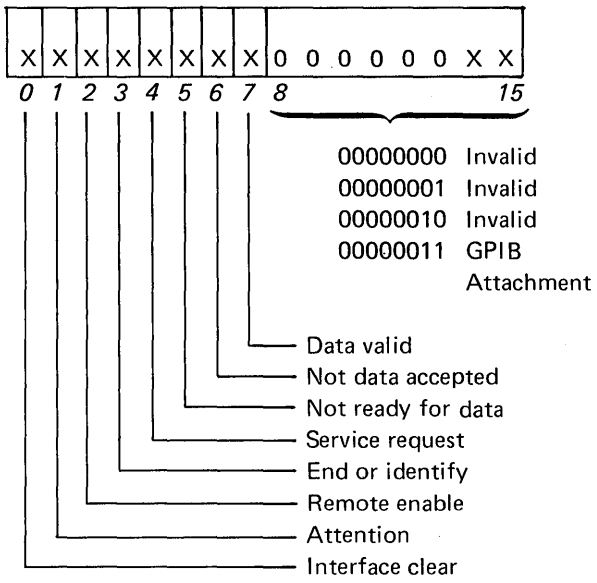
Yields two words of status in the following format:

Word 1—Device Logic Test Word 1
Pass—X'0000'
Fail—X'1XXX'

Word 2—Device Logic Test Word 2
Pass—X'0000'
Fail—X'XXXX'

Diagnostic Read Jumper

Yields one word of status in the following format:



Appendix F. Programming Notes

Note 1

If the data area pointed to by DCB word 7 contains the listen address of a device which is not attached to the bus (that is, an invalid listen address), the following conditions hold true. (Examples have SE=0.)

Condition 1

The data block specifies an invalid listen address as the only receiver of the programming information located in the data block of the Write Configure operation. When the Write Configure operation attempts to send programming information to this invalid address, the GPIB Adapter will time out on a source handshake.

An exception interrupt will be issued with ISB bit 0 on (additional status available). Cycle steal status word 4 will have bit 2 on (bus timed out on source handshake). Hence, no data transfers.

Condition 2

The data block is large enought to dictate use of the Write Configure operation followed by a Write Data operation, and the invalid listen address specified in the Write Configure operation is the only device to receive the programming information transmitted by the Write Data operation. The Write Configure operation will execute with no error; however, the Write Data operation will fail when the GPIB Adapter times out on a source handshake.

An exception interrupt will be issued with ISB bit 0 on (additional status available). Cycle steal status word 4 will have bit 2 on (bus timed out during source handshake).

Condition 3

Two or more devices are to receive the programming information in the Write Configure or Write Data operations and the listen address of one of the devices is incorrectly specified in the Write Configure operation. Since at least one device will handshake all programming information, the execution of this operation will end normally. However, the device whose listen address was incorrect will not perform the operation, and an undetected (from the GPIB Adapter view) error will have occurred.

Example:

Suppose the entire bus network is composed of the GPIB Adapter and two plotters (ASCII listen addresses 3 and 4). Both devices should receive the programming information with the following Write Configure operation data:

```
?U34",XYZTL!":
```

where:

?	is the universal unlisten address
U	is the GPIB Adapter talk address
3	is plotter #1 listen address
4	is plotter #2 listen address
XYZTL!	is programming information to both plotters

However, an invalid address (7) is specified in the Write Configure operation data block:

```
?U37",XYZTL!":
```

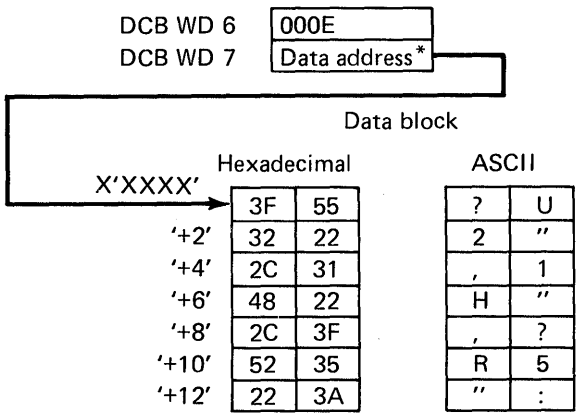
In this case, the device listen address 7 (a non-existent device for this example) will receive the programming information instead of device listen address 4 (plotter #2). The Write Configure operation will execute properly with device listen address 3 (plotter #1). Condition code 7 (satisfactory) and device end will be reported; however, plotter #2 will have remained inactive.

Condition 4

The invalid listen address is a listener for the data transfer which will occur between some instrument on the bus other than the GPIB Adapter and another listen address. The data transfer will occur on the Read Monitor operation following the Write Configure, and the incorrect listen address will go undetected because the GPIB Adapter is listening on the bus. The same conditions hold true if the data transfer is from an instrument on the bus to Series/1 main storage. No error will be detected; however, GPIB activity may be invalid.

Note 2

If the Write Configure is to address an instrument other than the GPIB Adapter as a talker, this must be done in the following manner: The talker address must occur in the last group of configuration information before the colon. The Write Configure can be followed by a Read Monitor or Read Data, depending on what the Write Configure is telling the instrument to do.



*The data block address may start on an even or odd byte storage boundary.

The Unlisten command is sent out over the bus. The device whose listen address is X'32' (ASCII 2) receives programming data X'3148' (ASCII 1H). The same device (listen address = X'32' (ASCII 2); talk address = X'52' (ASCII R)) is then addressed to talk to the device whose listen address is X'35' (ASCII 5). The data transfer between device talk address R and device listen address 5 will not occur until a start I/O Read type command occurs such as Read (Data) or Read (Monitor).

Chaining is supported and if the SE bit is on, retries and status storing will be performed. If the timer override bit is on, the default time-out will be overridden.

Appendix G. Glossary

Certain Series/1 terminology associated with GPIB carries different meanings than when ordinarily used in Series/1 architecture. This Glossary defines some terms in the context designated by IEEE Standard 488, 1975.

controller. A device that has the capability of configuring the interface by dictating which devices are active, which device is the talker, and which devices are the listeners.

Note. The IBM Series/1 GPIB Adapter has been designed such that it always remains the system controller and the controller-in-charge. No other controller may be active on the interface with this adapter.

end-of-string (EOS) termination. A program controlled byte used to specify the end of an information transfer. This terminator allows the GPIB Adapter to accept or monitor variable length transfers without knowing exact transfer byte counts.

interface. The actual GPIB communication pathway from the Series/1 to controllable instruments.

listener. A controller or active device on the interface that has been configured to accept information from the interface.

talker. A controller or active device on the interface that has been configured to source information to the interface. Only one talker can be active at any time.

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