UNCLASSIFIED

INSTRUCTION BULLETIN

BULLETIN NO. 232

64^2 MEMORY MAINTENANCE

64^2 MEMORY MAINTENANCE ADJUSTMENT PROCEDURES

July, 1958

MILITARY PRODUCTS DIVISION

INTERNATIONAL BUSINESS MACHINES CORPORATION

KINGSTON, NEW YORK

IBM KINGSTON TECHNICAL PUBLICATIONS

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FOREWORD

The information contained herein supersedes the related text on adjustment procedures in the Preliminary Maintenance Data Book on Core Memory, and in T.O. 31P2-2FSQ7-142, dated April 1, 1957.

This bulletin is intended to be self-contained with regard to adjustment procedures only. It includes the detailed adjustment procedures necessary for properly setting up an oscilloscope, for retuning the memory, and for ensuring that the spare clock conforms to the memory timing of the computer.

Where outside references are required, the reader is directed, in the text, to the applicable Instruction Bulletin.

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ADJUSTMENT PROCEDURES

1. TUNING PROCEDURE FOR X10 OSCILLOSCOPE PROBE

In order to make certain the oscilloscope probe does not produce distortion when the oscilloscope is used for critical measurements, it is necessary to check and, if needed, to adjust the linearity before making such measurements. The procedure for tuning the probe is as follows:

1. Connect the probe to the CAL OUT output on the oscilloscope.
2. Set the VOLTS/CENT control at 0.05 and the SQUARE WAVE GENERATOR for 2V.
3. Set the oscilloscope SYNC control to INTERNAL, and adjust the sweep until one complete cycle is displayed.
4. Using a small screwdriver, adjust the probe-adjusting screw until the waveform displayed on the oscilloscope screen is a perfect square wave.
5. If the probe adjustment cannot produce the display of a perfect square wave, try adjusting another probe. If the display is still unsatisfactory, try another oscilloscope.

2. VOLTAGE CALIBRATION OF TEKTRONIX OSCILLOSCOPE, TYPE 545

2.1 Calibration Equipment Requirements

To ensure that the oscilloscope will accurately measure the currents present when tuning core memory, it should be equipped with graticule 3033583 and calibrated with Oscilloscope Calibrator FR-112/FSQ (delay-line scope calibrator), Part No. 3204011. The calibrator is adjusted to deliver a pulsed output of 2V amplitude.

2.2 Procedure

To calibrate the oscilloscope, proceed as follows:

Note

The calibrator must be placed on a level support to ensure satisfactory operation of a mercury-wetted relay contained in the unit.

1. Apply power to the oscilloscope and the calibrator, and allow enough time for the circuits to stabilize.

2. Set the PULSE AMPLITUDE control on the oscilloscope calibrator to the value specified on the calibration chart. This sets the amplitude of the output voltage.

3. Set the OUTPUT PULSE SELECTOR to the + position.

4. Rotate the VOLTAGE AMPLITUDE potentiometer until the meter indicates the value specified on the calibration chart.

5. Rotate the VIBRATOR control in the clockwise direction until the vibrator can be heard; then advance the control approximately 30 degrees beyond this point. This is a more reliable point for vibrator operation. The calibrator output is now a 2V, 2 usec pulse.

6. Check the d-c balance of the vertical amplifier in the oscilloscope as follows:

   a. Rotate the VARIABLE VOLTS/CM control back and forth, and watch the trace for a vertical shift.

   b. Slowly turn the DC BAL adjustment until the trace remains steady while the VARIABLE VOLTS/CM control is rotated.

7. Using a tuned X10 probe, calibrated as described in paragraph 1, connect the oscilloscope to the calibrator. Set the oscilloscope controls to the following:

   a. Set trigger slope to plus, INTERNAL.

   b. Set the sweep control for 0.5 usec/cm.

   c. Set the vertical voltage selector to 0.05V/cm and the VARIABLE control to the extreme clockwise position (CALIBRATED).

   d. Set the INPUT SELECTOR switch to the DC position.

Note

To avoid excessive parallax when observing waveforms, use a hood over the face of the oscilloscope to accurately position the operator's head.

8. Display the pulse on the oscilloscope. Set the focus and intensity controls to obtain a clear, sharp trace. Set the astigmatism control for an even trace. Use the vertical positioning control to place the dot, which designates the start of a trace, so that the top of the dot just touches the bottom centimeter scribe line. This establishes the d-c ground level. (See fig. 1.)

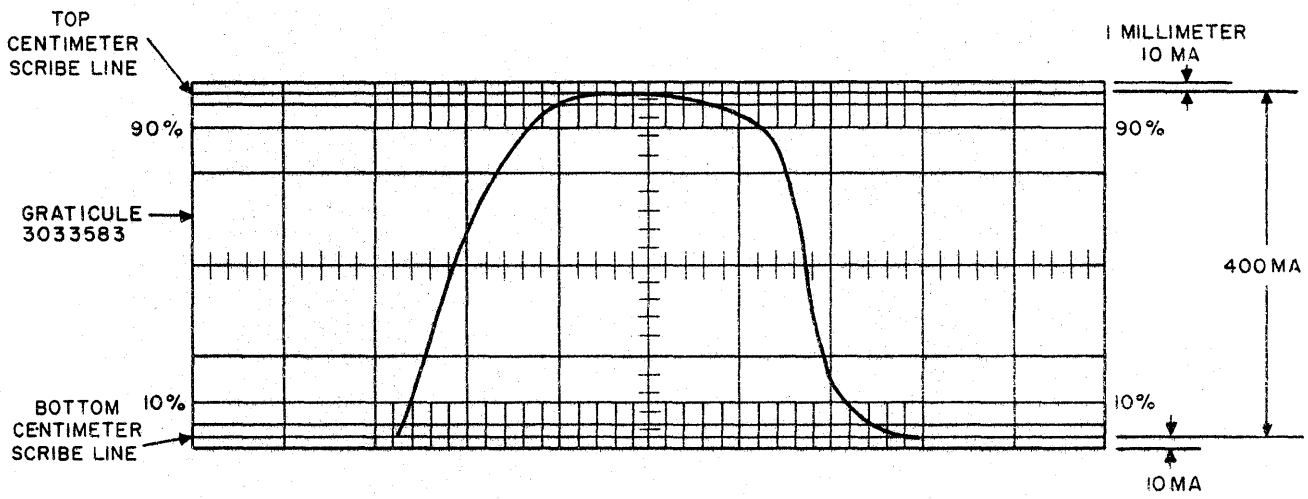


FIGURE 1. POSITIVE CALIBRATION WAVEFORM

9. Using a screwdriver, adjust the gain control, which is accessible through the preamplifier front panel, until the peak of the wave just touches the top centimeter scribe line. When it is considered that the vertical voltage selector setting of 0.05V/cm takes into account the X10 attenuation of the probe, it can be seen that the oscilloscope is effectively calibrated for 0.5V/cm, which is the equivalent of 100 ma/cm when measuring core memory currents. Use these control settings when measuring DPD and MGG current pulses.

10. Check the negative calibration, using the same procedure as that for the positive calibration, except that the OUTPUT PULSE SELECTOR on the calibrator is set to minus and the oscilloscope trigger slope control is set to MINUS, INTERNAL. The bottom of the dot should just touch the top centimeter scribe line, and the bottom of the waveform should touch the bottom centimeter scribe line. (See fig. 2.) If the voltage calibration is correct, the negative and positive calibration pulses will produce the same vertical deflection. If the deflections are not equivalent, tag the oscilloscope for repair, and calibrate another one.

2.3 Function of Special Graticule (3033583)

The graticule affords a valuable aid in making the core memory current measurements accurately. As shown in figures 1 and 2, the nominal value of 400 ma is equal to 4 centimeters of scope deflection. The upper and lower parts of the graticule have additional millimeter subdivisions that are each equal to 10 ma. Hence, an oscilloscope reading which deflects between the uppermost and lowermost lines represents 420 ma, and 2 millimeters (subdivisions) removed from each of these points represents 380 ma. As a result, measurements in the range 380 ma to 420 ma can be read with a high degree of accuracy. The other significant divisions on the graticule are the scribed lines that correspond to the 90% and 10% points for rise and fall time measurements, as shown.

3. SWEEP CALIBRATION OF TEKTRONIX OSCILLOSCOPE, TYPE 545

In order to ensure the reliability of oscilloscope time measurements, it is necessary to check the sweep accuracy of the oscilloscope before using it. The Tektronix Time Mark Generator, Type 180 (3033323), is used for this purpose. The time-mark generator is a highly accurate crystal-controlled pulse generator used to adjust sweep length and to check the sweep linearity. To calibrate the sweep length, proceed as follows:

1. Apply power to the oscilloscope and the time-mark generator, and allow sufficient time for the circuits to stabilize.

2. Set the oscilloscope SYNC control to INTERNAL, the TIME/CM to 0.1 MICROSECOND/CM, and the trigger control to AC FAST. The sweep multiplier is variable in steps. Set the sweep multiplier to the 2 to 5 position.

3. Connect the probe, calibrated as described in paragraph 1, to the time-mark generator output located just below the 1 MICROSECOND switch.

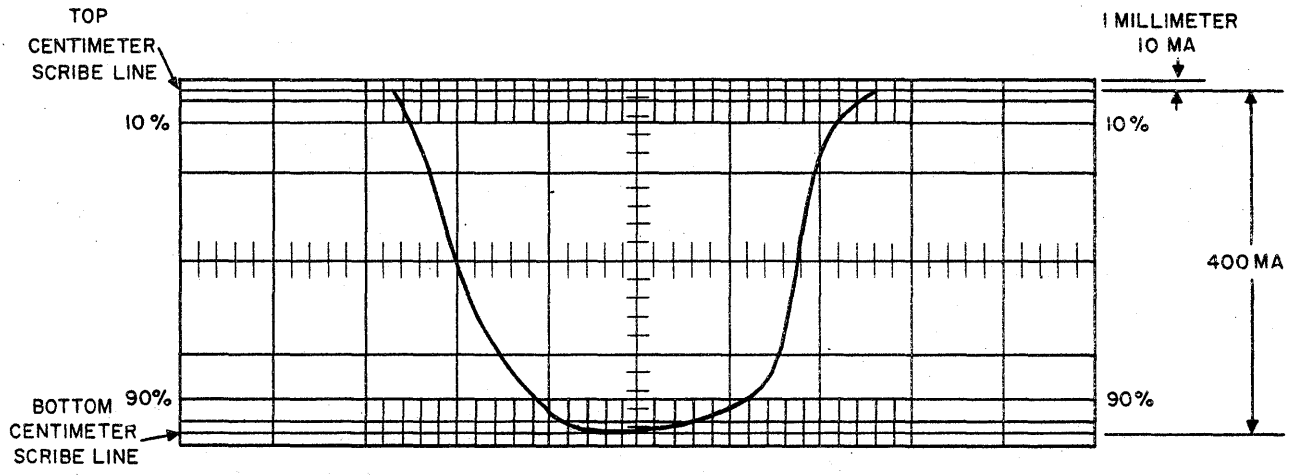


FIGURE 2. NEGATIVE CALIBRATION WAVEFORM

4. Set the input attenuator on the vertical amplifier so that the pulses are of a large amplitude. Position the pulses so that they just touch the center line of the graticule. (See fig. 3.)

Note

For greater accuracy when adjusting the sweep or making time measurements, use a hood. This positions the operator's head in the same place each time a waveform is observed. To avoid parallax, the reflection of the eye should be centered at the point where the waveshape is being read.

5. Adjust the variable sweep control unitl the pulses are exactly 2 centimeters apart. The sweep is now calibrated for 0.5 usec/cm. Do not touch sweep adjustments after the sweep is calibrated. This setting permits accurate observation of the memory clock timings.

6. If the pulses do not fall on the appropriate scribed lines for the entire length of the sweep, the sweep is not linear. Tag the oscilloscope for repair, and calibrate another one.

4. CORE MEMORY TUNING PROCEDURE

4.1 General

The tuneup procedures described in this paragraph are used to increase the reliability of the computer by re-establishing the optimum conditions necessary for trouble-free core memory operation. Three conditions may make it necessary to retune the core-memory circuits:

a. Changes in operating currents because of aging of components as determined by the lowering of margins, or by unreliable memory operation.

b. Replacement of pluggable units, such as digit plane drivers (DPD's), memory gate generators (MGG's), or spare clocks.

c. Accidental detuning of the original potentiometer settings.

It is recommended, where memory tuning is indicated, that two men be assigned to the task. This arrangement will ensure the high degree of accuracy required for observing all pertinent data.

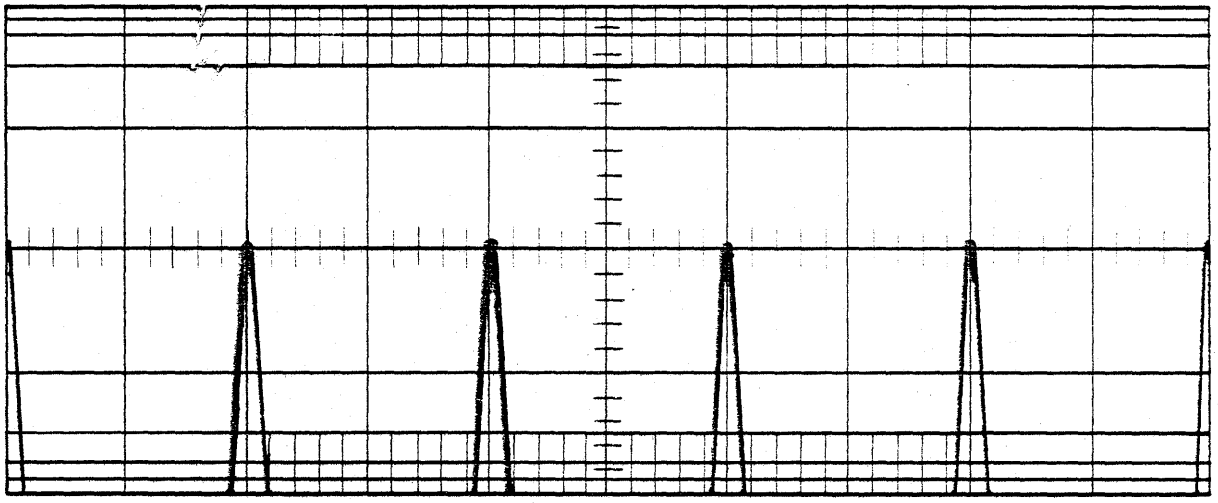


FIGURE 3. SWEEP CALIBRATION WAVEFORM

4.2 Pre-Tuneup Procedure

Note

The tuneup procedure may take as long as a full day to complete; therefore, approval for the adjustment must be obtained from the Technical Assistant or the Group Manager. Do not proceed with the tuneup until all troubles have been cleared in the computer, the core memory circuits, and the power supplies.

1. Check all supply voltages at PCD unit 63, especially the -300V line, and adjust if necessary.

2. Using program MC 1 MEM 01, check the operation of the Central Computer and the core memory, and correct all troubles.

3. The following equipment will be required:

   a. Oscilloscope - Tektronix 545 (3080475)

   b. Preamplifier - Tektronix 53/54 K (3080476)

   c. Probe - Tektronix 510 A (3033788)

   d. Hood - Tektronix H510 (3033343)

   e. Graticule - 3033583 (refer to 2.3 for explanation of the graticule markings).

   f. Sync test lead - Use one as short as possible to minimize noise pickup.

4. Calibrate the probe and oscilloscope as outlined in paragraphs 1, 2, and 3.

4.3 Tuning Procedure

The memory tuning procedure consists of checking the memory timing pulses, adjusting the DPD and MGG currents, and running memory programs to determine the most reliable point of operation.

To check memory timing and to adjust the DPD and MGG currents, use program MEMORY PM 7. This program has been written for the express purpose of providing clean and reliable scope patterns for these tests. In all such tests, the core memory record sheet or, if available, the most recent preventive maintenance chart (see fig. 1 of Instruction Bulletin 231) must be used as the source for proper reference data. A sample of the core memory record sheet available at earlier sites is shown in figure 4; for later sites, in figure 5.

CORE MEMORY RECORD SHEET

COMPUTER_____ SITE_____

MEMORY TIMINGS WITH RESPECT TO CLEAR MEMORY CONTROLS (7AEA5 OR 10AEA5)

Timing Pulse
Start Mem.
Set Read
Sample
Clr. Read
Set Inh.
Set write
Clr. Write
Clr. Inh.

Mem. I P. U. & Pin	Mem. I	Mem. I Spare
7ACB2		
7ACA2		
7ACJ1		
7ACE5		
7BCE5		
7BCC1		
7BDB4		
7BDE8		

Mem. II Pulse & P. U.	Mem. II	Mem. II Spare
10ACB2		
10ACA2		
10ACJ1		
10ACE5		
10ACE5		
10BCC1		
10BDB4		
10BDE8		

Pluggable Unit Serial Numbers

P. U. Type	Mem. I	Mem. I Spr.	Mem. II	Mem. II Spr.
MPD#1 - 7091				
MPD#2 - 7092				
MPD#3 - 7093				

Current Amplitudes

Current	Mem. I	Mem. II
Read		
Write		
Inhibit		

Spare Plane

Plane numbers		

Average terminating Resistors

	X Odd	X Even	Y Odd	Y Even
Mem. I				
Mem. II				

If at any time a change is made that affects the above information:

1. Enter old and new information on the incident report.
2. Change this chart.
3. Notify your technical assistant.

Original copy completed by_____ Date_____

FIGURE 4. CORE MEMORY DATA RECORD SHEET (EARLIER TYPE)

THE TEST AREA CORE MEMORY RECORD

_____ ADS CC ☐ / DC ☐ _____ COMPUTER ☐ A / ☐ B MEMORY ☐ 1 / ☐ 2

1. MPD Timings (with respect to CLR Mem.)

Pulse	Pin Loc. Mod & Pin	MPD in Mem.	MPD Spr.
Start Mem.	ACB2		
Set Read	ACA2		
Sample	ACJ1		
Cl. Read	ACE6		
Set Inh.	BCE5		
Set Write	BCC1		
Cl. Write	BDB4		
Cl. Inh.	BDE8		

2. Current Amplitudes

Read _____ MA.
Write _____ MA.
Inhibit _____ MA.

3. PU Serial Numbers

PU Type	In Mem.	Spare
MPD #1-7091		
MPD #2-7092		
MPD #3-7093		

4. Average Terminating Resistors

X-odd Address _____
X-even Address _____
Y-odd Address _____
Y-even Address _____

5. Spare Plane

Plane Number _____

1. Have any particular bits or any memory locations been especially troublesome? If so, explain.

2. Have you noticed any cores with unusual peaking characteristics? If so, which cores?

3. Have you any information on this memory that should be made known to the Site? If so, explain.

4. Comments

TEST AREA # _____ DATE _____ SIGNED _____

APPROVED _____

This form should be completed prior to shipment of the computer. Two copies of it and two copies of margin to failure print-outs for the Memory should be sent to Manager, Field Technical Assistance, Department 912.

FIGURE 5. CORE MEMORY DATA RECORD SHEET (CURRENT TYPE)

Note

If adjustments are made to obtain better operating points, a new record should be made and added to the reference data (core memory record sheet or preventive maintenance chart) that is then being used as the standard. Record the date and the names of the personnel responsible for the new adjustment.

The following procedures provide the pertinent details for loading the special program, checking memory timing, checking adjustment of the DPD and MGG currents, and verifying the results by balancing margins. They must be performed in the order given.

4.3.1 Loading of Special Program

Load program MEMORY PM 7 as follows:

1. For memory 1, set the core-memory-assignment switch to REVERSE; for memory 2, set the core-memory-assignment switch to NORMAL.

2. Set the test memory switch to ASSIGNED.

3. Depress the MASTER RESET pushbutton and then the LOAD FROM CARD READER pushbutton.

This program will be used for all the subsequent checks unless otherwise noted.

4.3.2 Check of Memory Timing (Clock)

Since this check is included in the preventive maintenance chart on a periodic basis, it is less likely that this area requires adjustment as contrasted with the other memory adjustments. A check of timing, therefore, is left to the discretion of the Field Engineer contingent on the preventive maintenance time schedule. If preventive maintenance has not been performed initially, or if considerable time has elapsed since this check was last made, it is deemed advisable to check timing as follows:

1. Using the calibrated oscilloscope and probe (sweep setting 0.5 usec/cm, vertical setting 1.0V/cm), set the sync control to EXTERNAL and connect a sync lead to 7AEA5 for memory 1 or 10AEA5 for memory 2. In the subsequent steps, only memory 2 is referred to although the same techniques apply to memory 1.

2. Depress the LS toggle switch of the A register.

3. Connect the scope probe to pin 10 ADB1 (clear-memory-controls), and position the displayed pulse on the vertical line of the graticule to the extreme left of the scope. All timing readings will be taken with respect to this pulse.

4. Record as accurately as possible the time between the clear-memory-controls pulse and the following pulses:

Start-memory	10ACB2
Set-read	10ACA2
Sample	10ACJ1
Clear-read	10ACE5
Set-inhibit	10BCE5
Set-write	10BCC1

5. At this point, it will be necessary to change the external sync to the set-write pulse. Connect the sync lead to pin 10BCC1, but do not readjust the triggering level as this may cause an erroneous reading.

6. Position the set-write pulse at the left edge of the scope, and record the times of the following pulses with reference to the set-write pulse:

Clear-write	10BDB4
Clear-inhibit	10BDE8

Since the clear-write and clear-inhibit pulse timings are with reference to set-write pulse, the sum of the set-write pulse time (with respect to clear-memory controls) and clear-write pulse time (with respect to set-write pulse) gives the timing of clear-write with respect to clear-memory-controls. In like manner, the sum of set-write pulse time and clear-inhibit pulse time gives the timing of clear-inhibit pulse with respect to clear-memory-controls. If there is a discrepancy between the observed readings and the reference data, reset the memory clock delay line taps to correct it, and remeasure the clock timing.

4.3.3 Adjustment of DPD Currents

Adjust the DPD currents as follows:

1. Depress the LS toggle switch of the A register to provide the correct pattern for checking the inhibit currents.

2. Using the calibrated oscilloscope and probe, set the sweep to 1.0 usec/cm and the vertical setting to .05V/cm. Connect the scope probe across one of the inhibit winding terminating resistors (fig. 6). These resistors are located on both sides YA and YB of the memory array. The position of each resistor corresponds to the position of its associated DPD pluggable unit on modules 7B and 9B for memory 1 and modules 10B and 12B for memory 2. As shown in figure 6, two resistors in parallel comprise the terminating load resistance for each of the individual

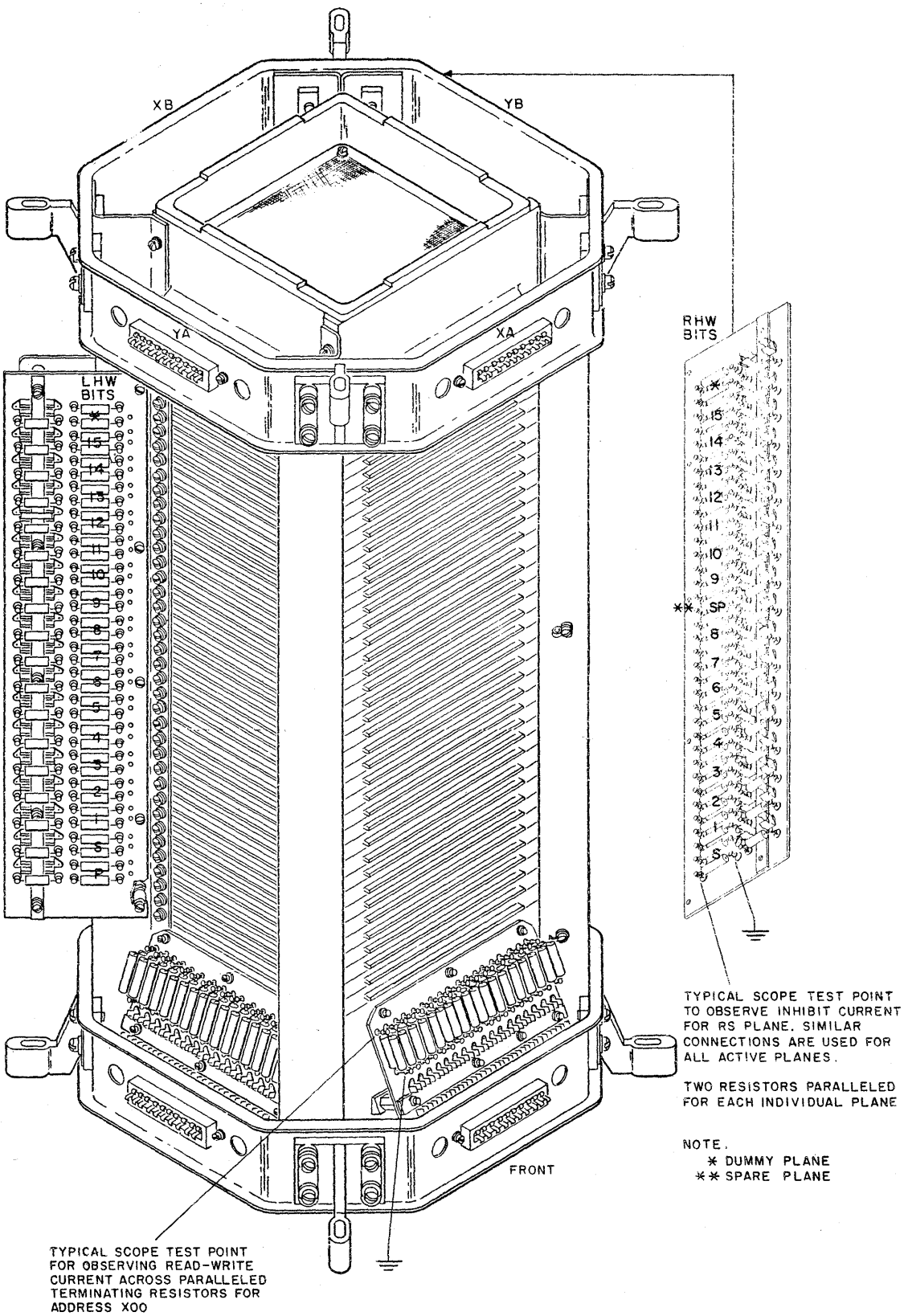


FIGURE 6. INHIBIT AND DRIVE CURRENT TERMINATING RESISTORS

inhibit windings. The parallel resistor combinations are further identified with their associated plane bit designation. The spare plane (if it is not being used) and the dummy plane terminating resistors have no voltage developed across them and should not be scoped.

3. Measure and adjust the output of all DPD's to the inhibit current value recorded in the reference data sheet.

4.3.4 Adjustment of Read-Write Currents

Upon completion of the DPD adjustments, proceed to adjust the read-write currents as follows:

1. Depress the L1 toggle switch of the A register to provide the correct pattern for checking the read-write currents. (All other toggle switches must be in their normal, released position.)

2. Refer to the core memory record sheet for the average drive lines specified therein.

Note

When the preventive maintenance schedule (see fig. 5 of Instruction Bulletin 231) is in effect at a site, the drive line terminating resistors will be periodically checked for accuracy. Under these conditions, there is no need to know the average lines since any address may be scoped.

3. Connect the scope probe to the average line terminating resistors. (See fig. 6 for a typical connection.) To assist in identifying the actual location of the average line terminating resistors, the physical layout of the terminating resistor mounting boards consistent with their octal address designations is illustrated in figure 7.

4. Adjust the potentiometers located on the MGG pluggable units to the current amplitude value noted in the reference data sheet. The MGG pluggable units are assigned as follows:

X read odd - pluggable unit 10CD

X write odd - pluggable unit 10CF

X read even - pluggable unit 10CH

X write even - pluggable unit 10CK

Y read odd - pluggable unit 12AD

Y write odd - pluggable unit 12AF

Y read even - pluggable unit 12AH

Y write even - pluggable unit 12AK

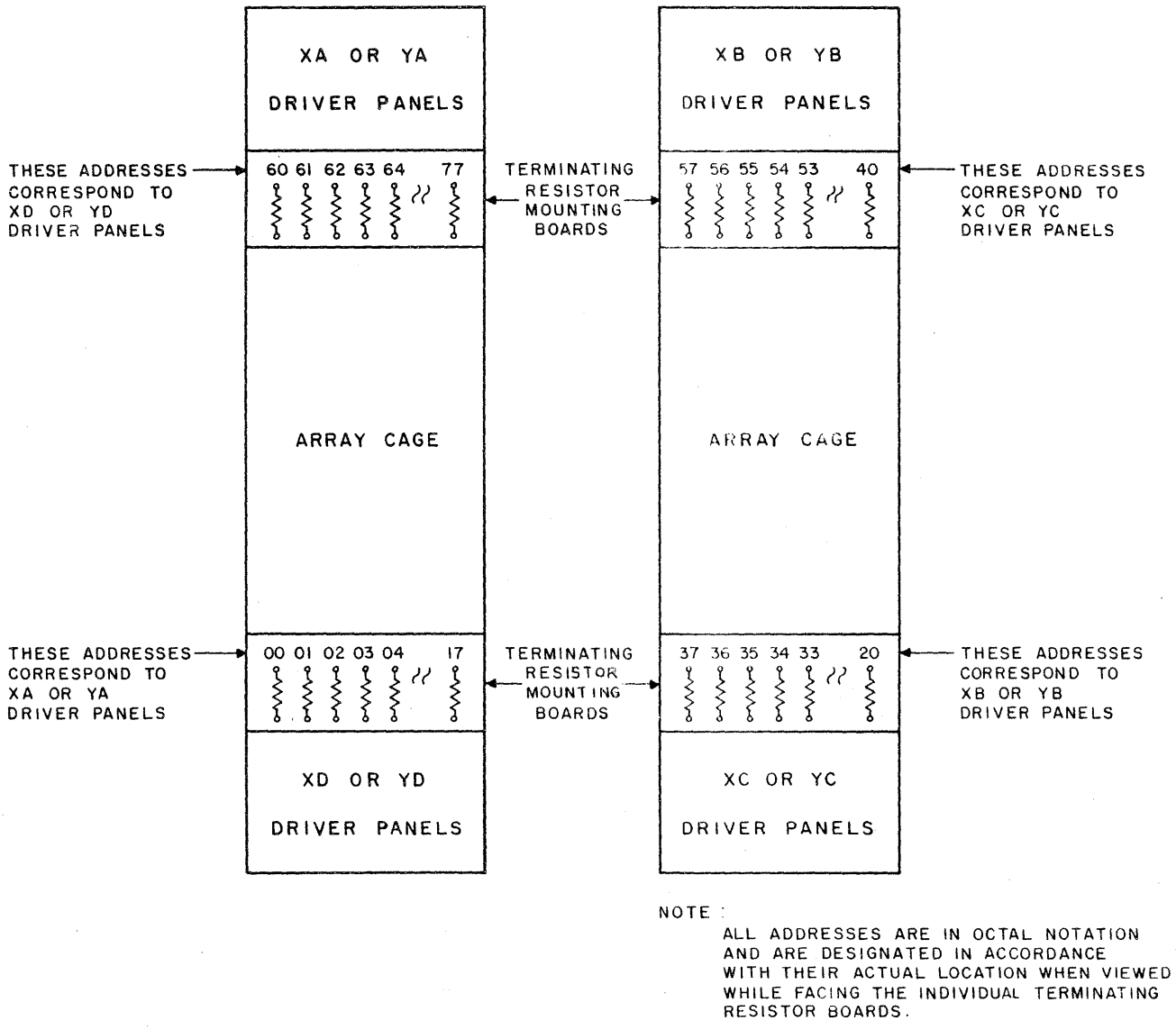


FIGURE 7. LOCATION OF DRIVE LINE TERMINATING RESISTORS

5. Recheck and retune the read-write currents after the first adjustments are completed. This readjustment is necessary because of the interaction between MGG's.

4.3.5 PRF Test

Upon completion of the read-write current adjustments, inspect the pulse repetition frequency (PRF) envelope to assure balance between the area of the read and the area of the write current as follows (for a complete explanation of the significance of this test, refer to the subject matter on PRF Conditions in Instruction Bulletin 230):

1. Depress the L2 toggle switch of the A register. (All other toggle switches must be in their normal released position.) This will permit the reading and writing of 0's along the Y lines at a 6-usec rate.

2. Connect the scope probe to one of the average Y lines, and set the sweep to 500 usec/cm, internally synchronized, and the vertical sensitivity to 0.1V/cm (or, if desired, .05V/cm).

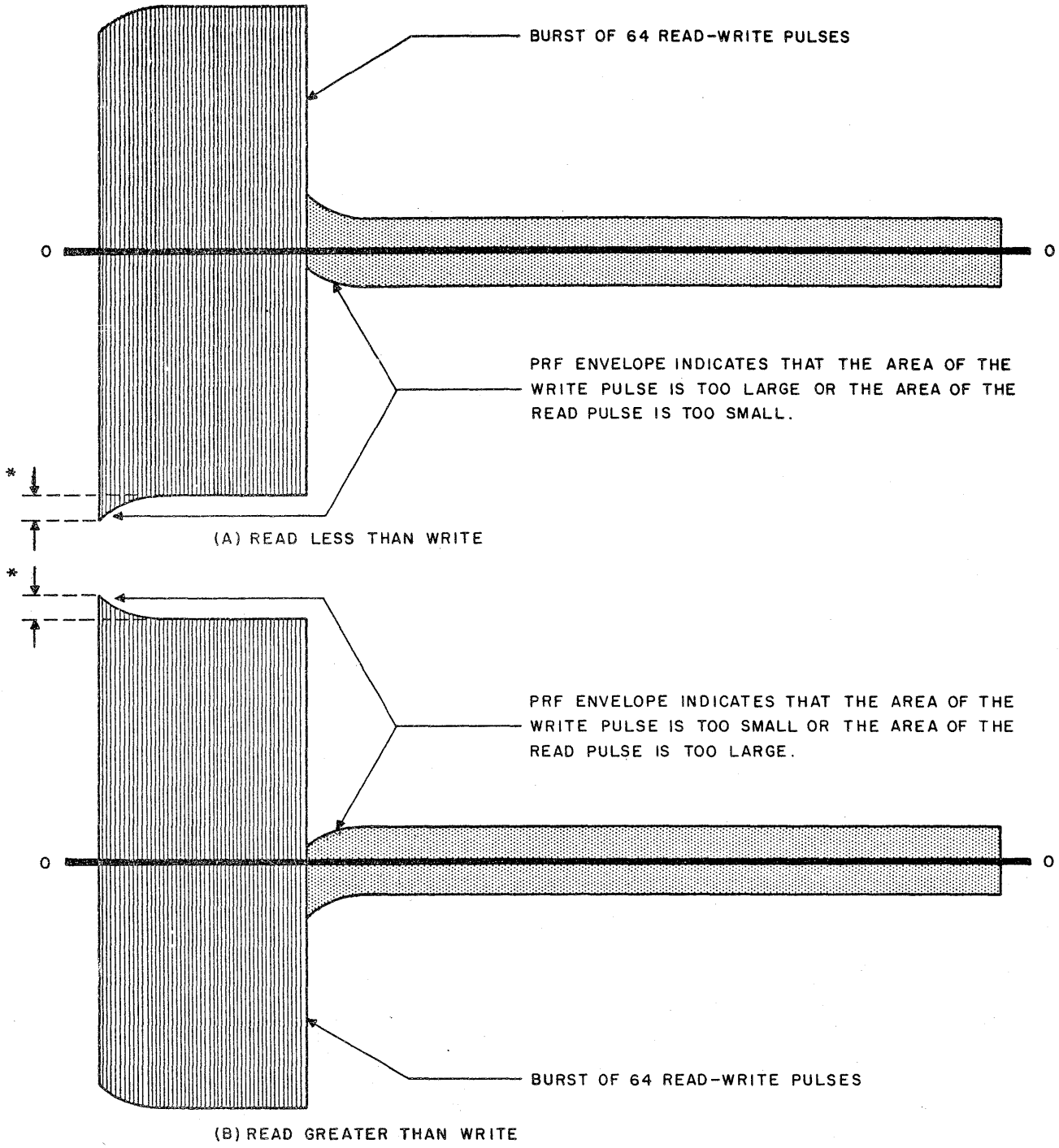
3. Observe the PRF envelope, and note any unbalance. Figure 8 shows two examples of unbalance which may be observed in the PRF envelope. In both examples, the maximum allowable deviation in the area shown exceeds 5 ma. If either of these conditions exists, the following corrective action should be instituted:

   a. If read is less than write (A in fig. 8), it means that the write area must be reduced by moving the clear-write tap in 10BD so that clear-write occurs 0.02 usec earlier. Observe the PRF envelope for improvement; if it is insufficient, repeat the tap adjustment process until balance is achieved, provided the width of the write pulse, measured between the 90% points, is at least 1.2 usec.

   b. If read is greater than write (B in fig. 8), it means that the write area must be increased by moving the clear-write tap in 10BD so that clear-write occurs 0.02 usec later. Observe the PRF envelope for improvement; if it is insufficient, repeat the tap adjustment process until balance is achieved. If it has been found necessary to move write later in the cycle, it is possible that the inhibit current no longer overlaps the write current properly. This condition must be checked for as follows:

      Observe the inhibit current. This current may be obtained by scoping across any one of the inhibit winding terminating resistors (fig. 6).

      Compare the inhibit and write currents to ensure that the end of inhibit occurs at the same time or later than the end of write. If not, the inhibit current must be



NOTE:
* THE MAXIMUM ALLOWABLE DEVIATION FOR A BALANCED CONDITION IS 5 MA, AS MEASURED BETWEEN THE POINTS INDICATED BY THE DASHED LINES.

FIGURE 8. PRF ENVELOPE

timed to comply with this requirement. To time the inhibit current, move the clear-inhibit tap on 10BD as necessary to obtain the proper time relationship with write. Under no circumstances, however, must the end of inhibit current extend beyond 6.6 usec from clear-memory-controls.

4. Depress the L3 toggle switch of the A register. (All other toggle switches must be in their normal, released position.) This will permit observation of the PRF envelope along the X line.

5. Connect the scope probe to one of the average X lines, and observe the PRF envelope for any unbalance. Since the clock timings have been checked and adjusted in step 3 above for the Y lines, it should also be considered to be correct for the X lines because the clock timings are common to both X and Y lines. Therefore, if any unbalance is noted, it is invariably due to current variations between the X and Y MGG's. Recheck the MGG adjustments using the techniques outlined in 4.3.4.

4.3.6 Check of Sample Time

Scope the sense amplifier test point as follows:

1. Set the scope vertical setting to 2V/cm, and the sweep setting to 0.5 usec/cm.

2. Depress the L1 toggle switch of the A register. (All other toggle switches must be in their normal, released position.)

3. Connect the scope probe to pin G2 of any one of the sense amplifiers. The sense amplifiers are located in 7 AF through 7 AY, and 9 CG through 9 CY for memory 1; 10 AF through 10 AY, and 12 CG through 12 CY for memory 2.

4. Examine the waveform for proper sample time as depicted in figure 9. If the sample is not in the same relative position shown, change the sample delay tap (7ACJ1 or 10ACJ1) on the memory clock to comply.

4.3.7 Balancing the Margins

Verify the results of the tuning by running program MC1 MEM 01 while applying margins to the -300V B1, B2 line for memory 1; or to the -300V E1, E2 line for memory 2. Application of positive excursions to the B1 or E1 line decreases the write current, whereas a negative excursion increases the write current. Application of a positive excursion to the B2 or E2 line decreases the read current, whereas a negative excursion increases the read current. With SENSE switch 1 depressed, the program will cause a printout at both positive and negative margins. If the tuning is correct, failures will not occur for marginal checking (MC) excursions of ±20V minimum. If the read or write excursions are unblanaced, all the applicable MGG's should be adjusted (refer to

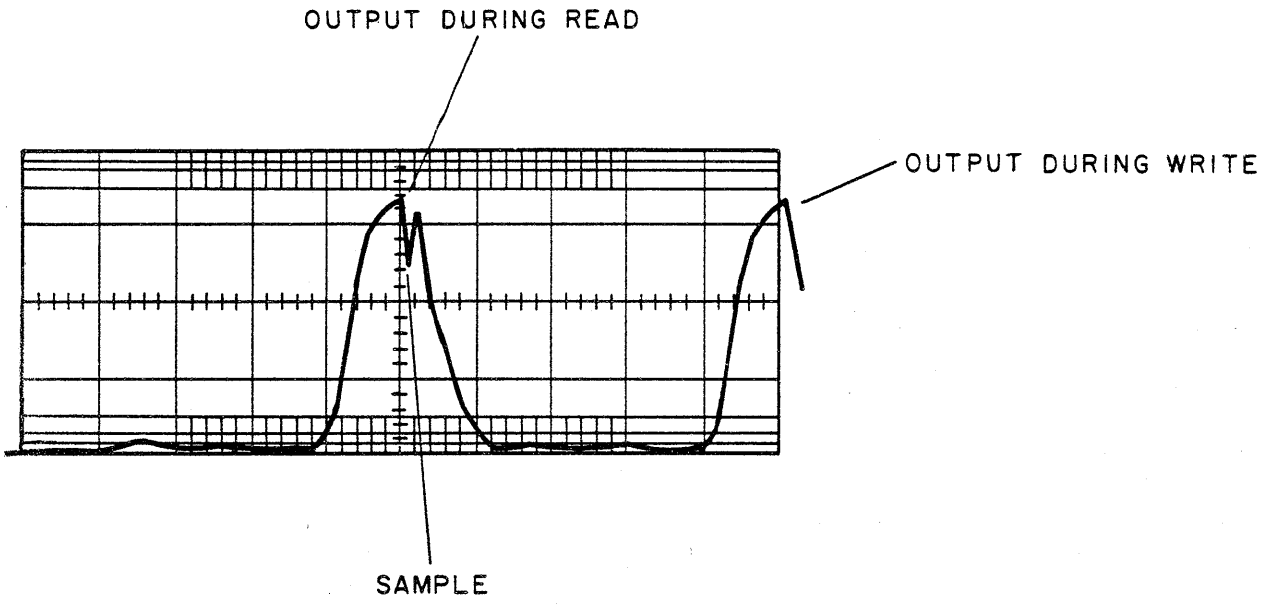


FIGURE 9. SENSE AMPLIFIER OUTPUT

procedure in 4.3.4) in small increments by a like amount. The direction of adjustment is determined as follows:

1. If the positive excursion is greater than the negative, decrease all affected MGG currents a like amount.

2. If the negative excursion is greater than the positive, increase all the affected MGG's a like amount.

When making these adjustments, extreme care should be taken that the margins are shifting in the right direction. This will be determined by repeating the MC routine. If the margins are decreasing, adjust the MGG's in the opposite direction. Recheck the PRF envelope as prescribed in 4.3.5.

Note

The procedures listed may have to be performed more than once to provide the optimum operating points for the MGG's. If failures are indicated in the MC excursion ranges below ±16V, component failure may be suspected. Corrective maintenance techniques should be employed to detect the faulty circuits. These circuits should be replaced, and a new tuneup performed. MGG currents should be adjusted until marginal checking indicates margins of ±20V or better. Record any changes in the applicable reference data (core memory record or preventive maintenance chart) sheet.

5. SPARE CLOCK ADJUSTMENTS IN DRIVER PANEL TESTER

5.1 Purpose

The purpose of this procedure is to provide a method for independently checking and adjusting the spare clock on the driver panel tester to conform to the memory timing of the computer. Since the clock comprises three pluggable units, a considerable saving of computer time is realized in the process. In addition, this procedure may be extended to include the retiming of repaired clocks.

5.2 Procedure

5.2.1 General

The procedure involves an initial check of the timings of the memory clock in the computer, which are then used as the standard for adjusting the spare clock in the driver panel tester. In order to facilitate a rapid comparison of the timings, it is necessary to record all pertinent data in the chart shown in figure 10. This chart identifies the clock's three pluggable unit types consistent with the pulse test point locations within them and provides a cross-reference between the memory clock timings (designated machine timing in the chart) and the spare clock pulse timings encountered on the driver panel tester. Since it is conceivable that the spare clock's timing may have to be altered, provisions are made in the chart to record the initial reading (in the start column), any

CLOCK		COMPUTER A☐ B☐ MEMORY 1☐ 2☐	DRIVER PANEL TESTER TIMING				
PU TYPE	PULSE	MACHINE TIMING	START	CHANGE 1	CHANGE 2	CHANGE 3	FINAL
7091	SET-READ 10ACA2	____USEC	____USEC				____USEC
	SAMPLE 10ACJ1	____USEC	____USEC				____USEC
	CLEAR-READ 10ACE5	____USEC	____USEC				____USEC
	OUTPUT 10ACG1	____USEC	____USEC				____USEC
7092	SET-INHIBIT 10BCE5	____USEC	____USEC				____USEC
	SET-WRITE 10BCC1	____USEC	____USEC				____USEC
	OUTPUT 10BCA3	____USEC	____USEC				____USEC
7093	CLEAR-WRITE 10BDB4	____USEC	____USEC				____USEC
	CLEAR-INHIBIT 10BDE8	____USEC	____USEC				____USEC
	OUTPUT 10BDE5	____USEC	____USEC				____USEC

FIGURE 10. CLOCK TIMING, COMPUTER VS DRIVER PANEL TESTER

subsequent readings due to adjustment (change 1, change 2, etc.), and the value representative of the final adjustment.

5.2.2 Detailed Instructions

To achieve compatible timing with the memory in use, it is necessary to know the inherent machine timing. The source for this information may be a recent preventive maintenance chart. If this is unavailable, or if considerable time has elapsed since preventive maintenance was last performed, it is advisable to check memory timing following the procedures outlined in 4.3.1 and 4.3.2. In addition to these timings, record the output timing for each of the clock's three pluggable units. All measurements should be made in the order shown in figure 10. The timings thus obtained (using the procedures of 4.3.2) are referenced to clear-memory-controls with the exception of clear-write, clear-inhibit, and output (10BDE5), which are referenced to set-write. In order to duplicate the test conditions available in the driver panel tester, all pulses (except those referenced to set-write) must use start-memory as the reference. To obtain this information from the measured data requires a simple conversion, as follows: assume the start-memory and set-read pulses are timed, respectively, at 0.8 usec and 1.0 usec (when both are referred to clear-memory-controls); therefore, set-read (1.0 usec) is delayed 0.2 usec with respect to start-memory (0.8 usec). It is this value (0.2 usec) that must be recorded for the set-read pulse. A similar conversion permits the sample, clear-read, output (10ACG1), set-inhibit, set-write, and output (10BCA3) pulses to be referenced to start-memory. Conversion is not required, however, for clear-write, clear-inhibit, and output (10BDE5) since these pulses are referenced to set-write and must be recorded exactly as measured. When the machine timings are recorded in the spaces provided (fig. 10), proceed to time the spare clock in the driver panel tester, as follows:

1. Set up the oscilloscope with the time-mark generator as described in paragraph 3.

2. Place the spare 7091 unit in the E location on the driver panel tester, and bring up module power on the tester.

3. Measure the spare clock timings, and record them in the appropriate (start) column of figure 10.

4. Remove the unit, and make a note of the delay taps employed.

5. Compare the recorded readings in the machine timing and start columns. If they differ, calculate the magnitude of difference and compensate for it by unsoldering and moving the appropriate wire, corresponding to the pulse under test, to the desired delay tap.

6. Reinsert the pluggable unit, and recheck the timings. Record these timings in the column change 1.

If they still differ from the machine timings, calculate the difference, remove the unit, and readjust the appropriate delay taps. Recheck the timings, and record them in the column change 2. Repeat this procedure, as necessary, to obtain readings that correspond as closely as possible to the machine timings. Record the timings after each change in the proper column (add additional columns if necessary).

Note

It may be necessary to juggle the settings considerably in order to achieve the desired result. Attempt, if possible, to keep the tap on the delays that have 0.02-usec divisions (these are used for the sample pulse on the 7091 unit and the clear-write pulse on the 7093 unit) toward the center of the delay line so that, when the spare clock is finally installed in the computer, the 0.02-usec taps are available in either direction for memory tuning.

7. Repeat steps 1 through 6 for the 7092 unit in location P, and for the 7093 unit in location R of the driver panel. When these tests are completed, the spare clock timing should approximate the machine timing.

8. The spare clock is now ready to be checked out in the computer for a final system test. Before this is done, it is necessary to check the position of the sample pulse using the computer clock. This can best be observed by running program MEMORY PM 7 (refer to 4.3.1) and scoping the G2 test point of any sense amplifier, as described in 4.3.6. Remove the three pluggable units that constitute the computer clock, install the corresponding type units for the spare clock, and proceed as follows:

   a. Observe the position of the sample pulse using the test techniques noted above. If it is not in the same relative position, change the sample delay tap on the memory clock to comply.

   b. Run MC1 MEM 01 to prescribed margins. A failure of MC1 MEM 01 in option 7 indicates clear-write may have to be moved. This can be accomplished by running program MEMORY PM 7 and following the procedure outlined in 4.3.5.