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INSTRUCTION BULLETIN

BULLETIN NO. 230

64^2 MEMORY MAINTENANCE

64^2 MEMORY
ANALYSIS OF MAINTENANCE TECHNIQUES

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FOREWORD

This Instruction Bulletin represents the first of a series of four Instruction Bulletins, numbered 230, 231, 232, and 233. They contain, in a convenient reference package, the pertinent maintenance information necessary to ensure the continued reliability of the 64^2 core memory element in the field.

Although each Instruction Bulletin is designed to be self-contained with regard to the subject matter covered, the Field Engineer should familiarize himself initially with the contents of all four Instruction Bulletins in the series. This is recommended because in equipment as complex as memory there are many functions which are interrelated, and for which there are no clear-cut lines of demarcation. As a result, there are many items which are either cross-referenced directly or others, such as illustrations, which may be used as alternate references, if desired. In this manner, maximum benefit can be derived from the practical information presented.

The information contained herein supersedes the related text on maintenance techniques in the Preliminary Maintenance Data Book on Core Memory, and in T. O. 31P2-2FSQ7-142, dated April 1, 1957.

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SECTION 1

INTRODUCTION

1.1 SCOPE

This Instruction Bulletin provides the information necessary for attaining a working knowledge of the 64^2 core memory element. It embodies the pertinent details pertaining to: physical configuration, maintenance programming, troubleshooting techniques, and analysis of subtle electrical characteristics. Specifically, these topics appear as follows:

Section 2 contains a pictorial layout of the physical components that constitute the 64^2 core memory element. Each component is then broken down into its constituent parts and identified.

Section 3 contains pertinent data relating to the identification and use of currently available maintenance programs. In addition, it incorporates an analysis of printouts and a discussion of marginal checking consistent with the concept of margin balancing.

Section 4 contains a logical troubleshooting procedure supported by numerous photographic references of waveforms obtained with a working memory.

Section 5 identifies the subtle type of electrical characteristics which may easily be overlooked in analyzing memory malfunctions.

SECTION 2

PHYSICAL LAYOUT

2.1 IDENTIFICATION OF CORE MEMORY ELEMENT COMPONENTS

This section is intended to be self-explanatory since it features the physical layout of the core memory element in pictorial form. A logical sequence is employed commencing with the overall front and back views of the core memory element in figures 2-1 and 2-2. A basic description of the other illustrations follows.

The memory array and its component details are shown separately in figures 2-3 through 2-6, foldouts. A further breakdown of the memory array is made in figures 2-7 and 2-8. The former figure illustrates the typical connections on a core memory plane (plane 5 is used as an example), while the latter figure depicts the physical lines in octal notation to facilitate finding the exact physical location for any given octal address.

Figure 2-9 provides the front and rear views of the memory driver panel consistent with the identification of the components associated with the specific addresses provided by the memory driver panel. In this example, XA or YA memory driver panels are illustrated; however, the circuitry is similar for all memory driver panels with the exception of the addresses assigned to each. These addresses are identified in figure 2-9.

Figure 2-10 provides a detailed modular breakdown of units 7 or 10, 9 or 12, –and tables 2-1 through 2-6 provide a further breakdown of the individual modules within these units. Fully identified are the circuit functions, location of applicable logic, the inputs and outputs for each individual pluggable unit, and any pertinent remarks that are helpful in better understanding the pluggable unit function.

Figure 2-11 shows the components, particularly of the DPD decoupling circuitry, in the Z module.

FIGURE 2-1. CORE MEMORY ELEMENT, PLUGGABLE UNIT SIDE

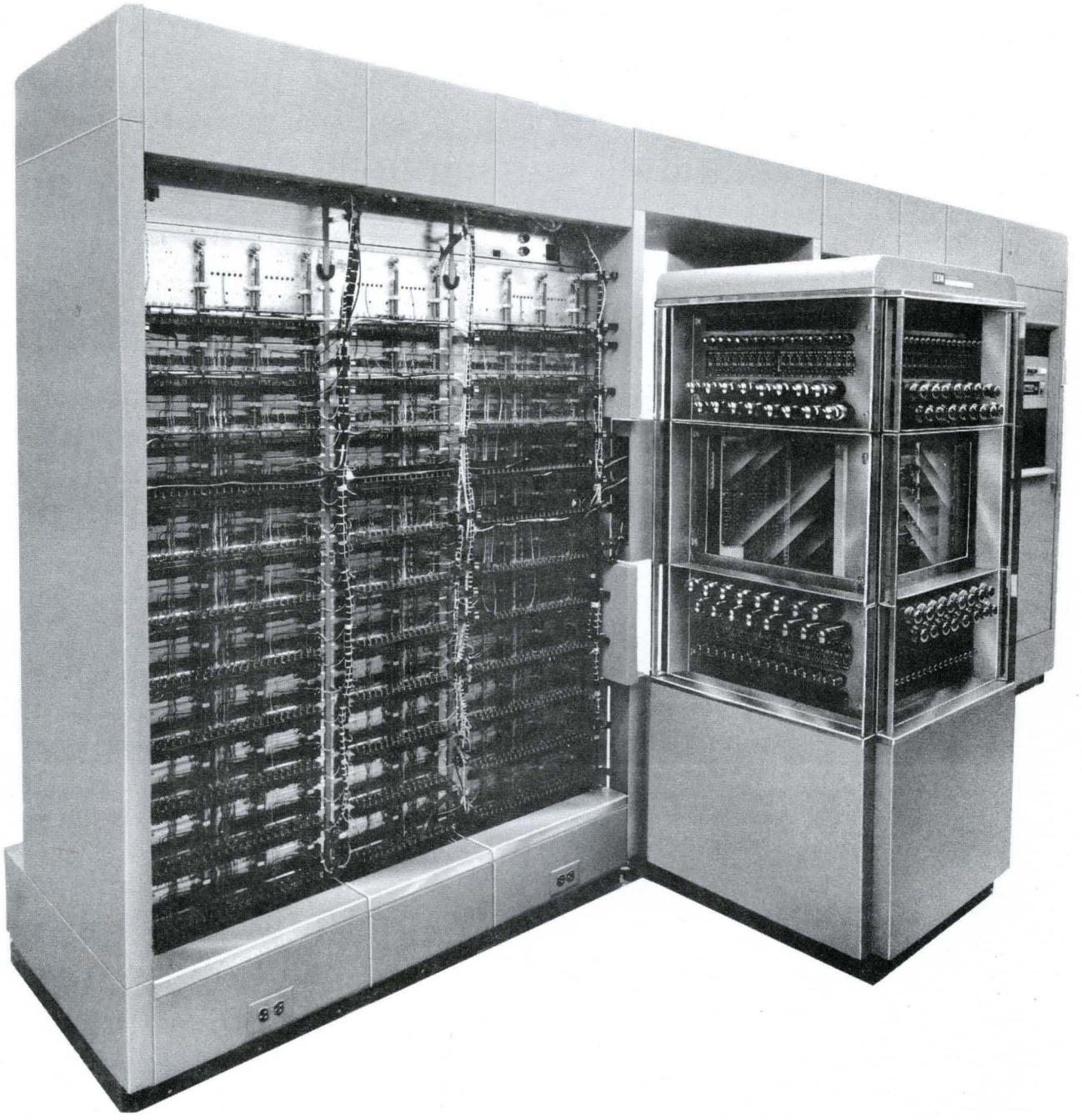


FIGURE 2-2. CORE MEMORY ELEMENT, WIRING SIDE

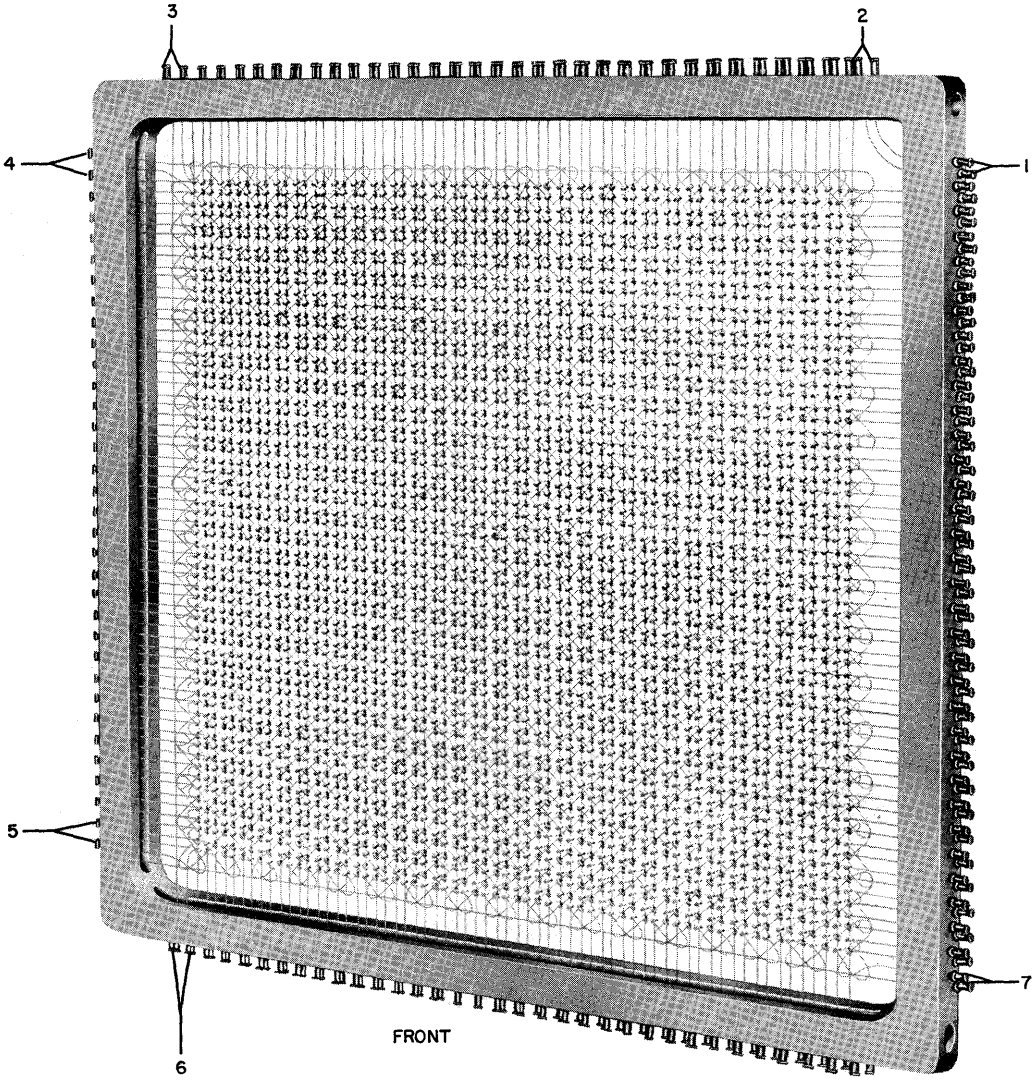
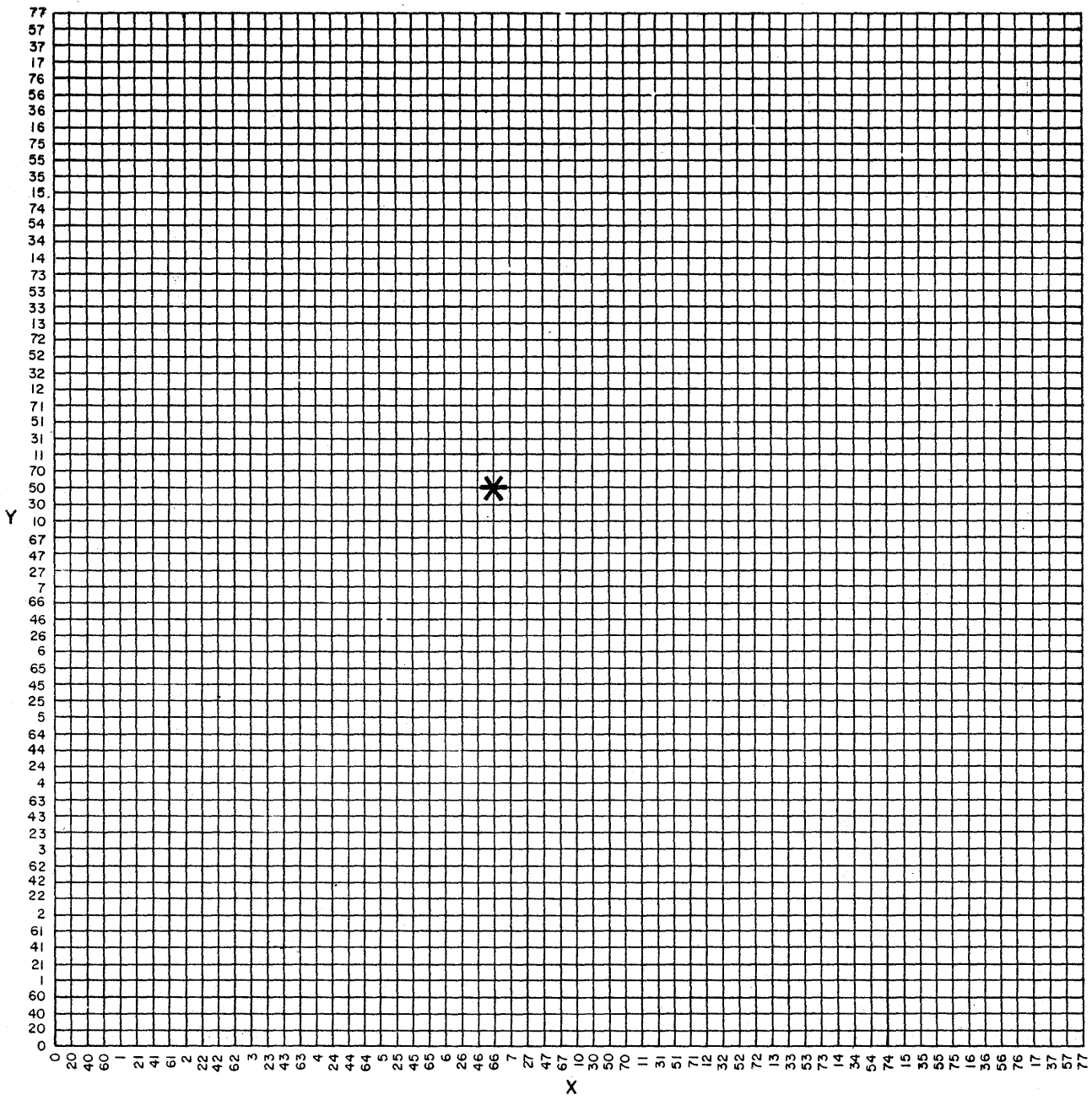


FIGURE 2-7. FERRITE CORE MEMORY PLANE

Note: The following legend is based on the analyzation of an odd plane (plane 5). A similar analysis is applicable between the corresponding numbers of all other active planes.

1. Connection from DPD for the inhibit winding of plane 6.
2. Jumper from plane 5 to the inhibit winding of plane 6.
3. Inhibit winding connection for plane 5 jumpered from plane 6.
4. Sense winding connection for plane 5.

5,6,7. Jumpers within plane 5.



NOTE : * THIS ADDRESS IS 5066. IT CORRESPONDS TO THE INTERSECTION OF THE Y LINE (OCTAL 50) AND THE X LINE (OCTAL 66). ANY OTHER ADDRESS MAY BE LOCATED IN THE SAME MANNER.

FIGURE 2-8. ADDRESS SELECTION

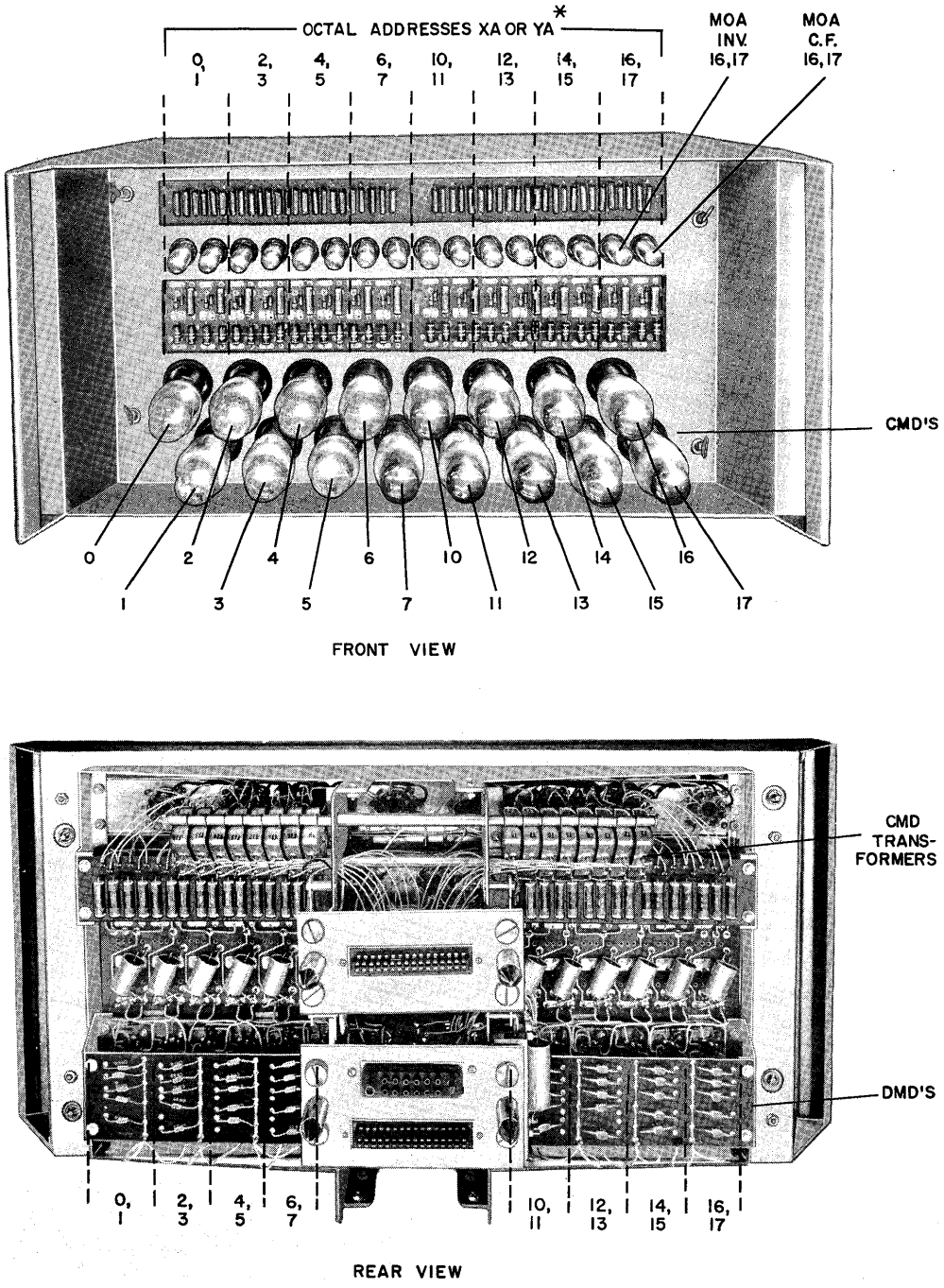


FIGURE 2-9. MEMORY DRIVER PANEL, ADDRESS LOCATIONS

Note: * The memory driver panel circuitry demonstrated is similar for

XB or YB (octal addresses 37-20)

XC or YC (octal addresses 57-40)

XD or YD (octal addresses 60-77)

Unit 7 or 10

PU	Modules A	Modules B	Modules C
C	Memory pulse distributor number 1 (clock)	Memory pulse distributor number 2 (clock)	MGG X read odd
D	Inhibit gate gen left half-word	Memory pulse distributor number 3 (clock)	
E	Clr mem control PA's sample left half-word	Spare	MGG X write odd
F	Sense ampl bit L15	Digit plane driver bit L15	
G	L14	L14	MGG X read even
H	L13	L13	
J	L12	L12	MGG X write even
K	L11	L11	
L	L10	L10	X read gate gen X write gate gen
M	L9	L9	Spare
N	L8	L8	Spare
P	L7	L7	X MAR 2^0
R	L6	L6	PCF X MAR 2^0, 2^1
S	L5	L5	X MAR 2^1
T	L4	L4	X MAR 2^2
U	L3	L3	PCF X MAR 2^2, 2^3
V	L2	L2	X MAR 2^3
W	L1	L1	X MAR 2^4
X	LS	LS	PCF X MAR 2^4, 2^5
Y	Parity	Parity	X MAR 2^5

Unit 9 or 12

Modules A	Modules B	Modules C	PU
MGG Y read odd	Spare	Spare	C
	Spare	Inhibit gate gen right half-word	D
MGG Y write odd	Spare	Spare	E
	Spare	Sample gate gen	F
MGG Y read even	Digit plane driver bit R15	Sense ampl bit R15	G
	R14	R14	H
MGG Y write even	R13	R13	J
	R12	R12	K
Y read gate gen Y write gate gen	R11	R11	L
Spare	R10	R10	M
Spare	R9	R9	N
Y MAR 2^6	R8	R8	P
PCF Y MAR 2^6, 2^7	R7	R7	R
Y MAR 2^7	R6	R6	S
Y MAR 2^8	R5	R5	T
PCF Y MAR 2^8, 2^9	R4	R4	U
Y MAR 2^9	R3	R3	V
Y MAR 2^{10}	R2	R2	W
PCF Y MAR 2^{10}, 2^{11}	R1	R1	X
Y MAR 2^{11}	RS	RS	Y

FIGURE 2-10. LAYOUT OF MEMORY PLUGGABLE UNITS

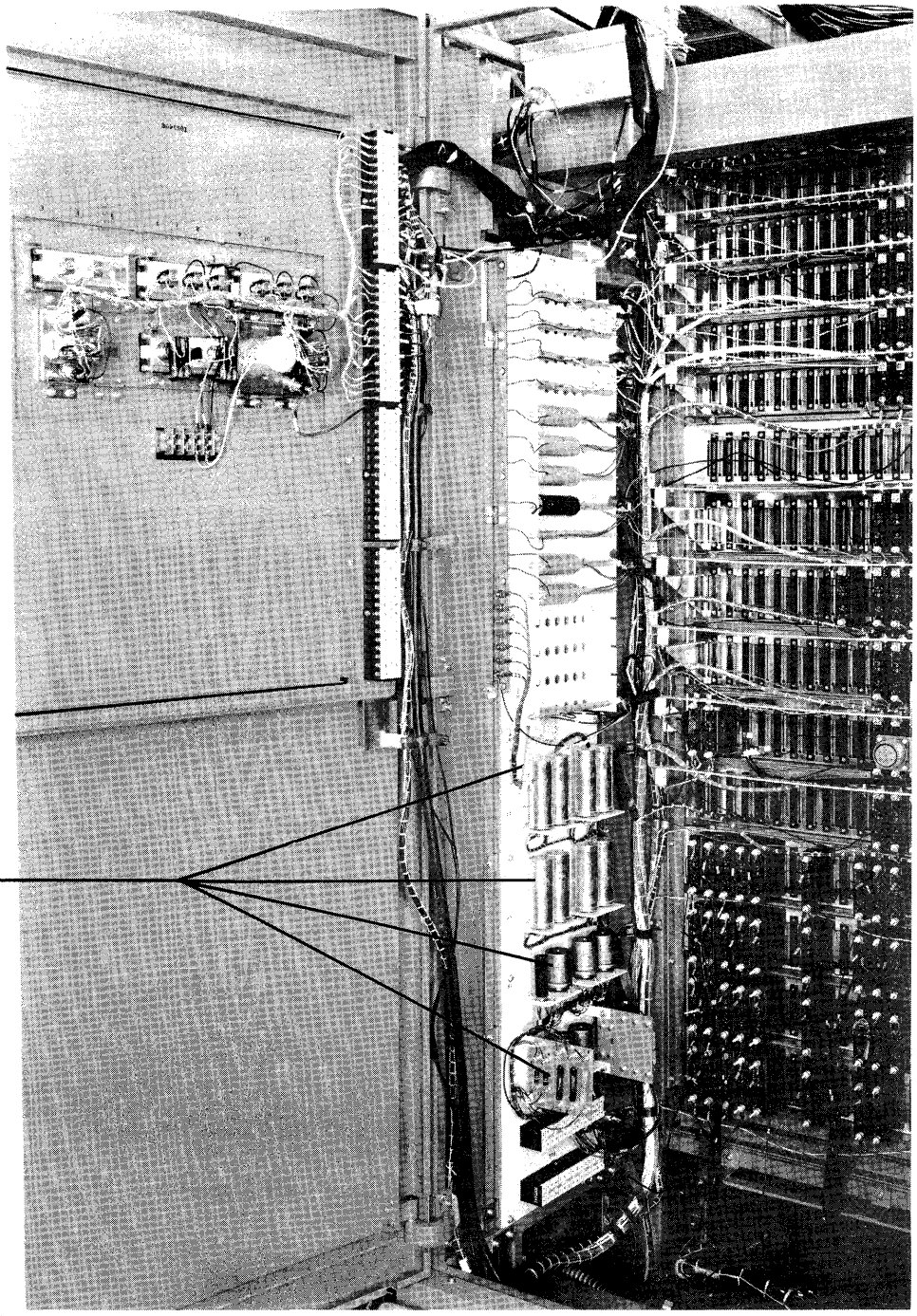


FIGURE 2-11. Z MODULE, INTERNAL VIEW

TABLE 2-1. CIRCUIT IDENTIFICATION, UNIT 7 OR 10, MODULE A

PU	Circuit	Logic Location	Input(s)		Output(s)		Remarks
			Designation	Pin	Designation	Pin	
C	Memory pulse distributor number 1 (clock)	0.1.4 A-4	Start memory	B2	Set read Sample Clear read To memory pulse distributor 2	A2 J1 E5 G1	
D	Inhibit gate gen left half-word	0.1.4 D-2	Set inhibit Clear inhibit Clr mem controls	A1 A5 B1	Inhibit gate	H6	
E	Clr mem controls PA's Sample left half-word RD	0.1.4 C-5 D-1	Clr mem controls Sample left half-word	A5 H6	Clear inhibit & sample gate gen Clear Y MAR, read & write gate gen Clear X MAR, read & write gate gen Sample left half-word	A6 B8 F5 H3	
F	Sense ampl bit L15	0.1.6 A-8 to E-8	Output of Plane 3 Sample pulse	A1,A2 A5,A6 H5	Sense ampl test-point Output to memory buffer	G2 H8	
G	L14		Plane 5				
H	L13		Plane 7				
J	L12		Plane 9				
K	L11		Plane 11				
L	L10		Plane 13				
M	L9		Plane 15				
N	L8		Plane 17				
P	L7		Plane 19				
R	L6		Plane 21				
S	L5		Plane 23				
T	L4		Plane 25				
U	L3		Plane 27				
V	L2		Plane 29				
W	L1		Plane 31				
X	LS		Plane 33				
Y	Parity		Plane 35				

TABLE 2-2. CIRCUIT IDENTIFICATION, UNIT 7 OR 10, MODULE B

PU	Circuit	Logic Location	Input(s)		Output(s)		Remarks
			Designation	Pin	Designation	Pin	
C	Memory pulse distributor number 2 (clock)	0.1.4 A-3	From memory pulse distributor number 1	F1	Set inhibit Set write To memory pulse distributor 3	E5 C1 A3	
D	Memory pulse distributor number 3 (clock)	0.1.4 A-2	From memory pulse distributor number 2	A5	Clear inhibit Clear write	E8 B4	
E	Spare						
F	Digit plane driver bit L15	0.1.6 A-4 to E-4	Level from memory buffer Inhibit gate	A6 A7	Signal to inhibit winding of Plane 3 via Plane 4	F6	
G	L14				of Plane 5 via Plane 6		The inhibit signal path for the left half-word is as follows:
H	L13				of Plane 7 via Plane 8		From Pin F6 of the DPD pluggable unit to an even-numbered plane on the array, then to the desired odd-numbered plane immediately above it and through all the cores in the desired plane, back down to the even-numbered plane from which point it is routed to the inhibit current terminating resistor.
J	L12				of Plane 9 via Plane 10		
K	L11				of Plane 11 via Plane 12		
L	L10				of Plane 13 via Plane 14		
M	L9				of Plane 15 via Plane 16		
N	L8				of Plane 17 via Plane 18		
P	L7				of Plane 19 via Plane 20		
R	L6				of Plane 21 via Plane 22		
S	L5				of Plane 23 via Plane 24		
T	L4				of Plane 25 via Plane 26		
U	L3				of Plane 27 via Plane 28		
V	L2				of Plane 29 via Plane 30		
W	L1				of Plane 31 via Plane 32		
X	LS				of Plane 33 via Plane 34		
Y	Parity				of Plane 35 via Plane 36		

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TABLE 2-3. CIRCUIT IDENTIFICATION, UNIT 7 OR 10, MODULE C

PU	Circuit	Logic Location	Input(s)		Output(s)		Remarks
			Designation	Pin	Designation	Pin	
C D	MGG X read odd	0.1.5 D-16	Read gate MAR FF	A1 A2	Conditions the read cathode of all the odd number X-CMD's	F5	The lower half of the PU contains the adjustment controls
E F	MGG X write odd	0.1.5 D-16	Write gate MAR FF	A1 A2	Conditions the write cathode of all the odd number X-CMD's	F5	The lower half of the PU contains the adjustment controls
G H	MGG X read even	0.1.5 E-16	Read gate MAR FF	A1 A2	Conditions the read cathode of all the even number X-CMD's	F5	The lower half of the PU contains the adjustment controls
J K	MGG X write even	0.1.5 E-16	Write gate MAR FF	A1 A2	Conditions the write cathode of all the even number X-CMD's	F5	The lower half of the PU contains the adjustment controls
L	X read gate gen X write gate gen	0.1.4 D-4	Clr mem controls Set read Clear read Set write Clear write	F5 B1 B3 H7 H5	X read gate X write gate	B8 H4	
M	Spare						
N	Spare						
P	X MAR 2^0	0.1.5 A-16	Clr mem controls Load MAR bit 15	A6 A2	MAR 2^{-0} partially conditions X even MGG's MAR 2^0 to PCF	F5 A7	The load MAR input may be a pulse from any of the following sources: a. address register b. program counter c. I-O address counter
R	PCF X MAR 2^0, 2^1	A-15	MAR 2^0 MAR 2^1	A7 F7	MAR 2^0 partially conditions X odd MGG's MAR 2^1 to DMD in driver panel	C5 G1	
S	X MAR 2^1	A-15	Clr mem controls Load MAR bit 14	A6 A2	MAR 2^1 to PCF MAR 2^{-1} to DMD in driver panel	A7 F5	
T	X MAR 2^2	A-14	Clr mem controls Load MAR bit 13	A6 A2	MAR 2^2 to PCF MAR 2^{-2} to DMD in driver panel	A7 F5	
U	PCF X MAR 2^2, 2^3	A-13	MAR 2^2 MAR 2^3	A7 F7	MAR 2^2 to DMD in driver panel MAR 2^3 to DMD in driver panel	C5 G1	
V	X MAR 2^3	A-13	Clr mem controls Load MAR bit 12	A6 A2	MAR 2^3 to PCF MAR 2^{-3} to DMD in driver panel	A7 F5	
W	X MAR 2^4	A-12	Clr mem controls Load MAR bit 11	A6 A2	MAR 2^4 to PCF MAR 2^{-4} to DMD in driver panel	A7 F5	
X	PCF X MAR 2^4, 2^5	A-11	MAR 2^4 MAR 2^5	A7 F7	MAR 2^4 to DMD in driver panel MAR 2^5 to DMD in driver panel	C5 G1	
Y	X MAR 2^5	A-10	Load MAR bit 10	A6 A2	MAR 2^5 to PCF MAR 2^{-5} to PCF	A7 F5	

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TABLE 2-4. CIRCUIT IDENTIFICATION, UNIT 9 OR 12, MODULE A

PU	Circuit	Logic Location	Input(s)		Output(s)		Remarks
			Designation	Pin	Designation	Pin	
C D	MGG Y read odd	0.1.5 D-9	Read gate MAR FF	A1 A2	Conditions the read cathode of all the odd number Y-CMD's	F5	The lower half of the PU contains the adjustment controls
E F	MGG Y write odd	0.1.5 D-9	Write gate MAR FF	A1 A2	Conditions the write cathode of all the odd number Y-CMD's	F5	The lower half of the PU contains the adjustment controls
G H	MGG Y read even	0.1.5 E-9	Read gate MAR FF	A1 A2	Conditions the read cathode of all the even number Y-CMD's	F5	The lower half of the PU contains the adjustment controls
J K	MGG Y write even	0.1.5 E-9	Write gate MAR FF	A1 A2	Conditions the write cathode of all the even number Y-CMD's	F5	The lower half of the PU contains the adjustment controls
L	Y read gate gen Y write gate gen	0.1.4 D-3	Clr mem controls Set read Clear read Set write Clear write	F5 B1 B3 H7 H5	Y read gate Y write gate	B8 H4	
M	Spare						
N	Spare						
P	Y MAR 2^6	0.1.5 A-9	Clr mem controls Load MAR bit 9	A6 A2	MAR 2^6 partially conditions Y even MGG's MAR 2^6 to PCF	F5 A7	The load MAR input may be a pulse from any one of the following sources: a. Address register b. Program counter c. I-O address counter
R	PCF Y MAR 2^6, 2^7	A-8	MAR 2^6 MAR 2^7	A7 F7	MAR 2^6 partially conditions Y odd MGG's MAR 2^7 to DMD in driver panel	C5 G1	
S	Y MAR 2^7	A-8	Clr mem controls Load MAR bit 8	A6 A2	MAR 2^7 to PCF MAR 2^{-7} to DMD in driver panel	A7 F5	
T	Y MAR 2^8	A-7	Clr mem controls Load MAR bit 7	A6 A2	MAR 2^8 to PCF MAR 2^{-8} to DMD in driver panel	A7 F5	
U	PCF Y MAR 2^8, 2^9	A-6	MAR 2^8 MAR 2^9	A7 F7	MAR 2^8 to DMD in driver panel MAR 2^9 to DMD in driver panel	C5 G1	
V	Y MAR 2^9	A-6	Clr mem controls Load MAR bit 6	A6 A2	MAR 2^9 to PCF MAR 2^{-9} to DMD in driver panel	A7 F5	
W	Y MAR 2^{10}	A-5	Clr mem controls Load MAR bit 5	A6 A2	MAR 2^{10} to PCF MAR 2^{-10} to DMD in driver panel	A7 F5	
X	PCF Y MAR 2^{10}, 2^{11}	A-4	MAR 2^{10} MAR 2^{11}	A7 F7	MAR 2^{10} to DMD in driver panel MAR 2^{11} to DMD in driver panel	C5 G1	
Y	Y MAR 2^{11}	A-3	Clr mem controls Load MAR bit 4	A6 A2	MAR 2^{11} to PCF MAR 2^{-11} to PCF	A7 F5	

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TABLE 2-5. CIRCUIT IDENTIFICATION, UNIT 9 OR 12, MODULE B

PU	Circuit	Logic Location	Input(s)		Output(s)		Remarks
			Designation	Pin	Designation	Pin	
C	Spare						
D	Spare						
E	Spare						
F	Spare						
G	Digit plane driver bit R15	0.1.6 A-2 to E-2	Level from memory buffer Inhibit gate	A6 A7	Signal to inhibit winding of Plane 4 via Plane 3	F6	
H	R14				of Plane 6 via Plane 5		The inhibit signal path for the right half-word is as follows:
J	R13				of Plane 8 via Plane 7		From pin F6 of the DPD pluggable unit to an odd-numbered plane on the array then to the desired even-numbered plane immediately below it and through all the cores in the desired plane, back up to the odd-numbered plane from which point it is routed to the inhibit current terminating resistor.
K	R12				of Plane 10 via Plane 9		
L	R11				of Plane 12 via Plane 11		
M	R10				of Plane 14 via Plane 13		
N	R9				of Plane 16 via Plane 15		
P	R8				of Plane 20 via Plane 19		
R	R7				of Plane 22 via Plane 21		
S	R6				of Plane 24 via Plane 23		
T	R5				of Plane 26 via Plane 25		
U	R4				of Plane 28 via Plane 27		
V	R3				of Plane 30 via Plane 29		
W	R2				of Plane 32 via Plane 31		
X	R1				of Plane 34 via Plane 33		
Y	RS				of Plane 36 via Plane 35		

TABLE 2-6. CIRCUIT IDENTIFICATION, UNIT 9 OR 12, MODULE C

PU	Circuit	Logic Location	Input(s)		Output(s)		Remarks
			Designation	Pin	Designation	Pin	
C	Spare						
D	Inhibit gate gen right half-word	0.1.4 D-2	Set inhibit Clear inhibit Clr mem controls	A1 A5 B1	Inhibit gate	H6	
E	Spare						
F	Sample gate gen	0.1.4 D-2	Clr mem controls Inhibit sample Clear write Sample pulse	B1 C7 A5 A8	Sample right half-word Sample left half-word	F7 F5	
G	Sense ampl bit R15	0.1.6 A-6 to E-6	Output of Plane 4 Sample pulse	A1,A2 A5,A6 H5	Sense ampl test-point Output to memory buffer	G2 H8	
H	R14		Plane 6				
J	R13		Plane 8				
K	R12		Plane 10				
L	R11		Plane 12				
M	R10		Plane 14				
N	R9		Plane 16				
P	R8		Plane 20				
R	R7		Plane 22				
S	R6		Plane 24				
T	R5		Plane 26				
U	R4		Plane 28				
V	R3		Plane 30				
W	R2		Plane 32				
X	R1		Plane 34				
Y	RS		Plane 36				

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SECTION 3

PROGRAMMING

3.1 MAINTENANCE PROGRAM ANALYSIS

There are varied maintenance programs available for testing the core memory element. Each has been written to provide a specific analysis of equipment performance. As a result, they run the gamut in size and scope from small and simple, to large and complex, depending upon their objective.

To obtain maximum benefit from these memory programs requires an awareness not only of their existence but, more important, of their intended functions and assumptions. Although detailed information regarding any memory program is provided in the program writeup, a brief functional description of the memory programs currently in use is provided in table 3-1. Program identification in this table is limited to the basic program type without reference to the latest level.

TABLE 3-1. MEMORY MAINTENANCE PROGRAMS

Program Type	Function
MC 1 MEM 01	This is the major memory program. It is designed to test the overall reliability of the core memory element including all the lines within the MC group 1. It is loaded into one core memory and conducts checks on the second core memory. Each core is tested with worst patterns. The program contains 11 routines designed to test the memory under the most stringent conditions. For example, in the PRF routine, the IO register is used to read all 0's into memory at a 6 usec rate; failure here may indicate that the areas under the read and write currents are not equal, or that the timing is incorrect at the end of the memory cycle due to improper setting of the clear-inhibit and clear-write pulses.
MC MEM PAR 01	This program is designed to supplement MC-1 MEM 01. It tests only the parity plane, and its associated sense amplifier and digit plane driver. It contains a PRF and four worst pattern tests on the parity bit. Marginal checks are performed only using the -150 C1 (SA) and -300 A1 (DPD) lines. It has all the SENSE switch options of MC-1 MEM 01 except X printout suppression.

TABLE 3-1. MEMORY MAINTENANCE PROGRAMS (cont'd)

Program Type	Function
MEMORY 04	This is a general reliability type program which is loaded into and tests the same memory. As a result, no automatic margins are applied because the program is in the memory under test. Since only one memory is used, it is very useful during installation. From experience, this program has detected some errors missed by MC-1 MEM 01. The possible reasons advanced for this phenomenon follow: a. MEM 04 uses three start-memory pulses: from the program counter, address register, and IO address counter. MEM 01, however, uses only the latter two to start the memory under test. b. MEM 04 in spot checking for worst patterns and relocating itself may set up unique PRF conditions. c. MEM 04 reads in information from the card reader on a staggered basis (exercises memory in a manner similar to program MEM 06).
MEMORY 05	This program is designed to detect failures due to faulty peaking cores; that is, if all other programs work and this one fails, it is an indication to check the cores. It loads into one memory and checks the other. It is the only memory program that uses drums. It applies margins only to the -150 C1 (SA CF) -300 B1 (write MGG's) and -300 B2 (read MGG's) MC lines. It sets up PRF conditions using patterns consisting of read 0-write 1 and read 1-write 0 at a rate that is less than 10 usec due to the use of drums.
MEMORY 06	This program was designed primarily to detect low frequency oscillation in the sense amplifiers. It does this by operating the sense amplifiers at a 6 usec rate, then by idling them for varying periods of time, and then by operating them again at a 6 usec rate. The time delay is varied by maintenance console switches. Two memories are necessary. No margins are applied.

3.2 MARGINAL CHECKING

3.2.1 General

The marginal checking facilities built into the computer are used to provide a high degree of reliability in the core memory element circuits. Marginal checking is performed by varying a supply voltage to a group of circuits. The variation of the supply voltage is called an excursion. The magnitude of an excursion necessary to produce operational circuit failure is called a margin.

3.2.2 Marginal Checking Facilities for Memory

The marginal checking lines for the core memory element are summarized in table 3-2. As shown, the circuit groups are divided equally between memory 1 and memory 2. This circuit group breakdown serves only to differentiate between the two memories for identification purposes; for example, -300B1 (memory 1) corresponds directly to -300E1 (memory 2); 150A1 (memory 1) corresponds directly to 150D1 (memory 2); 90C1 (memory 1) corresponds directly to 90F1 (memory 2); etc.

TABLE 3-2. MEMORY MARGINAL CHECKING LINES

Unit	MC Group	Circuit Group	Lines
MEMORY 1	1	A	1 through 6
		B	1 through 6
		C	1 through 6
MEMORY 2	1	D	1 through 6
		E	1 through 6
		F	1 through 6

3.2.3 Effect of Excursions on Memory Marginal Checking (MC) Lines

The memory MC lines may be functionally divided into two basic categories: diagnostic lines and system lines. A description of each follows:

a. A diagnostic line is one whose printout usually indicates that the circuit to which an excursion is applied is defective and the associated pluggable unit is to be replaced as the initial corrective step. All of the MC lines fall into this category with the exception of three system lines to be discussed later. One of the most important diagnostic lines is the DPD -300A1 (D1) line. For this line, a negative excursion (which is the only one applied) causes the inhibit current to decrease in amplitude slightly; however, its principal effect is reduction of the inhibit current pulse width. As a result, when failure occurs, it is usually due to improper overlap of inhibit current on write current.

b. The system lines encompass three MC lines; -150 C1 (F1), -300B1 (E1), and -300 B2 (E2). The effect of excursions on these lines will be discussed separately:

1. An excursion on the -150 C1 (F1) line tends to vary the sense amplifier voltage level of the waveshape appearing at pin G2. Hence, a positive excursion picks up noise or 0 as a 1. A negative excursion has the effect of dropping a 1.

2. An excursion on the -300 B1 (E1) line varies the MGG write currents as follows: A positive excursion has the effect of decreasing the write current approximately 1 ma/volt. A negative excursion has the effect of increasing the write current approximately 1 ma/volt.

3. An excursion on the -300 B2 (E2) line varies the MGG read currents in the same direction and by the same amounts as noted above for the write currents.

3.2.4 Balance of Read and Write MGG Margins

During normal operation (DCS, DCA, or any program), the read or write currents may increase above their nominal values due to PRF conditions (refer to 5.5 for detailed explanation). This means that the read and write currents due to program content vary

in a manner similar to that experienced while applying excursions to the -300 B1 (E1) and -300 B2 (E2) MC lines. This fact serves to emphasize the importance of maintaining read and write margins that are larger than the excursions produced by the program.

If time is available, it is not sufficient to maintain the -300 B1 (E1) and -300 B2 (E2) MC lines at prescribed margins. Instead, the margins should be made as high as possible by generally striving for the following goals:

1. Try to obtain a large spread; that is, -35V + 45V is equal to a spread of 80V.

2. Consistent with the large spread, try for balanced margins; that is, -40V + 40V represents a perfect balance with the spread remaining at 80V.

To fully understand the underlying principles involved, some practical applications are considered in table 3-3. This table lists four sets of margins that provide widely separated examples of conditions that may be encountered. For each particular set of margins an analysis is made in the remarks column regarding which of the margins is considered more preferable and the reason for its selection.

The conclusions to be drawn from table 3-3 are that when balancing margins, the choice should be predicated on obtaining the highest margins in both directions. For unbalanced margins, it must be recognized that it is always the lower of the two margins that is the critical factor in determining equipment susceptibility to failure.

TABLE 3-3. ANALYSIS OF BALANCING MARGINS

Applied Margins	*Read Current Variation	Remarks
-35V, +45V (unbalanced) -40V, +40V (balanced)	435 ma, 355 ma 440 ma, 360 ma	The balanced margins are preferred since a large voltage spread is maintained permitting adequate and identical current variations in either direction. This is the ideal condition.
+25V, -25V (balanced) +30V, -50V (unbalanced)	375 ma, 425 ma 370 ma, 450 ma	In this case, it would be preferable to keep the unbalanced margins since the lower margin in the unbalanced set (+30V) provides a greater voltage variation than the corresponding margin in the balanced set (+25V). In addition, the larger spread permits a greater variation on the higher side as well.

TABLE 3-3. ANALYSIS OF BALANCING MARGINS (cont'd)

Applied Margins	*Read Current Variation	Remarks
+35V, -35V (balanced) +30V, -50V (unbalanced)	365 ma, 435 ma 370 ma, 450 ma	In this case, although there is a greater spread with the unbalanced margins, the balanced margins are preferred because for the lower margin obtainable in either case, the +35V permits a greater safety margin than does the +30V.
-35V, +45V (unbalanced) -30V, +50V (unbalanced)	435 ma, 355 ma 430 ma, 350 ma	In this case, there are two unbalanced margins with identical spreads. It would be preferable to keep the -35V, +45V margins because for the lower margin obtainable in either case, the -35V permits a greater safety margin than does the -30V.

*Based on an initial adjustment of read current equal to 400 ma, and the assumption that a negative excursion of 1V is equal to a 1 ma increase in current, and that a positive excursion of 1V is equal to a 1 ma decrease in current.

3.2.5 Analysis of Printouts

3.2.5.1 Practical Considerations

From experience, it has often proven advantageous to take the following action when confronted with printouts while running MC-1 MEM 01:

1. If it begins to printout, it is advisable to continue the program through to its completion. In this manner, a complete picture of the situation is made available before instituting corrective measures.

2. If, in a certain routine, a printout to prescribed is difficult to analyze, it is recommended that a higher margin be applied manually. This procedure may then provide a printout in a different routine that is easier to diagnose.

3. If an addressing failure results in a printout, it may be difficult to analyze. Under these conditions, memory driver panel replacement or substitution is recommended.

3.2.5.2 Typical Printouts

Typical printouts with and without margins are exemplified in figure 3-1. They are representative of the printouts obtained when the printer panel is wired for an octal split.

PRINTOUT	17777	1,2	0. 000 000 000 000 000	0. 100 000 000 000 000
EXPLANATION	Y X ADDRESS OF FAILING LOCATION	CONDITION LIGHTS THAT GO ON AT TIME OF FAILURE. THEY SHOW ROUTINE BEING RUN	THESE ARE THE CONTENTS OF THE FAILING LOCATIONS. FROM THIS, THE BITS IN ERROR CAN BE DETERMINED	

LEGEND:
(ABOVE) PRINTOUT WITH NO APPLIED MARGINS
(BELOW) IN ADDITION TO THE ABOVE TYPE OF INFORMATION, THE FOLLOWING PRINTOUT IS ALSO PROVIDED IF MARGINS ARE APPLIED AT THE TIME OF FAILURE

PRINTOUT	02566	1	,B,,,,	,23,,,	+090	−018
EXPLANATION	THIS IS THE STEP BRANCHED FROM AT TIME OF FAILURE; IT ALSO SHOWS ROUTINE BEING RUN SINCE IT IS FOUR LESS THAN NORMAL ERROR HALT FOR THAT ROUTINE. IN THIS EXAMPLE, 02572 IS THE ERROR HALT FOR THE REGULAR CHECKERBOARD ROUTINE	GROUP	CIRCUIT	LINE	VOLTAGE	EXCURSION APPLIED AT TIME OF FAILURE
		(APPLIED MARGINS AT TIME OF FAILURE)				

FIGURE 3-1. TYPICAL PRINTOUTS WITHOUT AND WITH MARGINS

UNCLASSIFIED

SECTION 4

TROUBLESHOOTING TECHNIQUES

4.1 TROUBLESHOOING SOLID MEMORY FAILURES

Logical troubleshooting requires that all information capable of detecting an error be analyzed on a systematic, step-by-step basis. The information presented in the subsequent steps is predicated on this concept, and must be performed in the order given to achieve maximum benefit in isolating solid memory failures. A summary of the pertinent troubleshooting procedures is shown in figure 4-1. Each block in the figure is numbered to correspond to the detailed procedural steps that follow:

1. Determine if a true memory parity exists. This can be ascertained by diagnosing the symptoms that differentiate between a false and true memory parity, as follows:

   a. It is a false memory parity if, at the time of computer halt on memory parity, the word in the memory buffer register is a good parity word. For this condition the trouble is not usually in memory but in the Central Computer parity count and assign circuitry.

   b. It is a true memory parity if, at the time of computer halt on memory parity, the word in the memory buffer register is:

      (1) All 0's, including the parity bit. This indicates trouble may be in either the memory buffer register, memory, or a missing start-memory pulse.

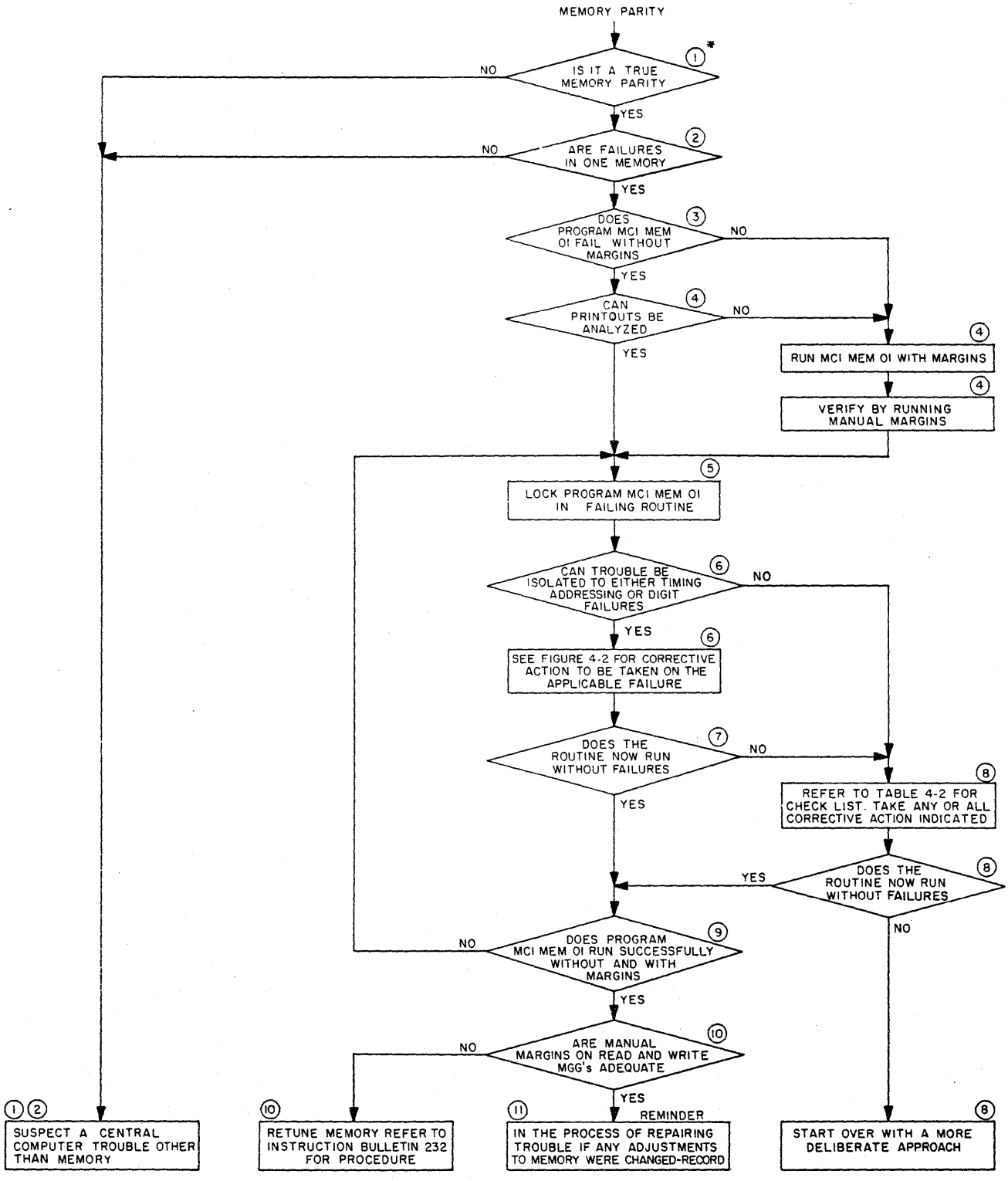
      (2) A bad parity word other than all 0's. This indicates trouble may be in either the memory buffer register, memory, or a missing inhibit-sample pulse.

   If a true memory parity exists, proceed with the next step:

2 Determine whether the failure is isolated to one memory or both memories. If the failure is common to both memories, it usually is not a memory trouble but rather a Central Computer trouble in any of the following areas: memory buffer register, a missing start-memory pulse, or a missing inhibit-sample pulse.

   If the failure occurs in only one memory, proceed with the next step:

3. Determine whether program MC-1 MEM 01 will fail without margins. For this check, it is recommended that the program



NOTE:
* REFER TO TEXT FOR DETAILED DESCRIPTION OF EACH NUMBERED BLOCK

FIGURE 4-1. TROUBLESHOOTING FLOW CHART FOR SOLID MEMORY FAILURES

be permitted to run completely through, providing a printout for every error. If the printouts are excessive, however, depress the L1 toggle switch of the A register to suppress X printouts.

Proceed with the next step:

4. Determine whether the printouts obtained in the previous step can be analyzed. Analyzation should be attempted only after at least one complete pass of the program. If analyzation is possible, proceed with step 5. If there are no printouts, or if the printouts are vague, or few in number, run the program MC-1 MEM 01 to prescribed. This may provide a larger number of printouts that are easier to analyze. If failures are obtained with margins, verify the margin by running the MC-1 MEM 01 program again while manually applying the excursion that caused the failure. Proceed with the next step.

5. Lock program MC-1 MEM 01 in a failing routine. This is accomplished with the A register toggle switches specified in the program writeup. Make certain that the selected routine will show the error when run separately. If it doesn't, try switching from the previous routine into the routine that caused the error. Proceed with the next step.

6. If the printout obtained in the previous step cannot be analyzed, proceed with step 8. If the printout can be analyzed, determine whether the error is a timing, addressing, or digit failure. If the error is in any of these three categories, follow the applicable procedure presented in the troubleshooting guide of figure 4-2, foldout. Since waveform observation provides an important aid in analyzing memory operation, the troubleshooting guide of figure 4-2 is supplemented by a complete set of waveforms (figs. 4-3 through 4-7) taken from a working memory. Figures 4-3 through 4-6 are designed specifically for use with the clock, memory driver panel and the sense amplifier, respectively. Figure 4-7, (foldout) is a composite illustration of the pertinent waveforms throughout memory depicted in their proper time perspective. With regard to addressing failures (B of fig. 4-2), it must be recognized that this type of failure is very difficult to diagnose. A defective memory driver panel causes misleading symptoms; therefore, if no failing address pattern other than isolation to all X or all Y lines is self-evident, proceed to check the four memory driver panels applicable to either X or Y addresses by any of the following methods:

   a. Replace all four memory driver panels with corresponding units from the other memory.

   b. Replace each of the four memory driver panels, one at a time, with a spare.

c. Remove each of the four memory driver panels, one at a time, and run the program MC-1 MEM 01. If a good panel is removed all 16_{10} addresses on that panel and all addresses that failed previously will printout. When the bad panel is removed, only the 16_{10} addresses of the removed panel will printout. Thus, the defective panel is isolated and corrective action may be taken.

For an addressing failure where all addresses in a group fail except one pair, reference data is provided in table 4-1 that identifies the defective DMD diodes under these conditions.

With regard to digit failures (C of fig. 4-2), if a failing bit(s) is traced to a DPD, the replacement DPD unit must be adjusted using an oscilloscope (refer to Instruction Bulletin 232 for the procedure).

7. Upon completion of whatever corrective action has been taken in the previous step, re-run the routine that had previously failed. If it still fails, refer again to the troubleshooting guide (fig. 4-2) and perform additional checks listed therein. Re-run the failing routine immediately following any corrective action taken. If all the checks in figure 4-2 are completed with no success, proceed with step 8. If success is achieved, proceed instead with step 9.

8. Refer to table 4-2 for a comprehensive list of things to check for in memory. Upon completion of any check which requires some definite corrective action, re-run the routine that had previously failed. If it still fails, refer again to the table and execute the remaining checks. Re-run the failing routine following any definite corrective action taken. Continued failure at the conclusion of all these checks indicates a need to start over again with a more deliberate approach.

   If success is achieved, proceed with step 9.

9. Run program MC-1 MEM 01 without and with margins, in that order. If an error occurs, repeat the foregoing procedural steps commencing with step 5. If the program runs successfully (without and with margins) proceed with step 10.

10. Run manual margins on the read and write MGG lines -300 B1, B2 (E1, E2). If these are less than ±25V and time permits, a retune should be initiated to establish these limits (refer to Instruction Bulletin 232 for tuning procedures). When adequate margins are available, the memory can be considered to be in good operating condition.

11. If, at any point during the troubleshooting procedures, the clock, or the inhibit, read, or write current adjustments are changed, the new readings must be recorded in the core memory record sheet or, if available, the preventive maintenance chart. (Refer to Instruction Bulletin 231.)

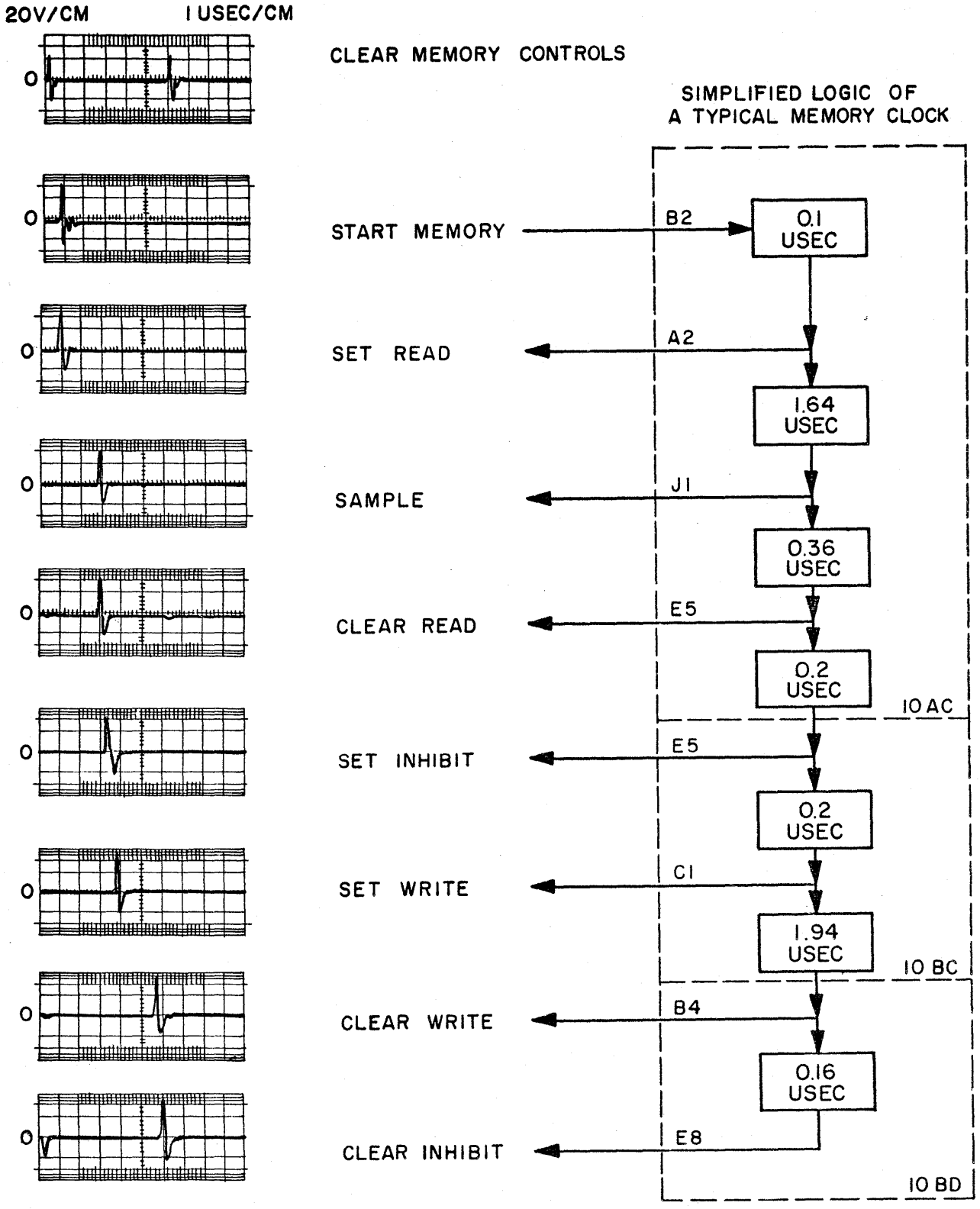


FIGURE 4-3. MEMORY PULSE DISTRIBUTOR, WAVEFORM ANALYSIS

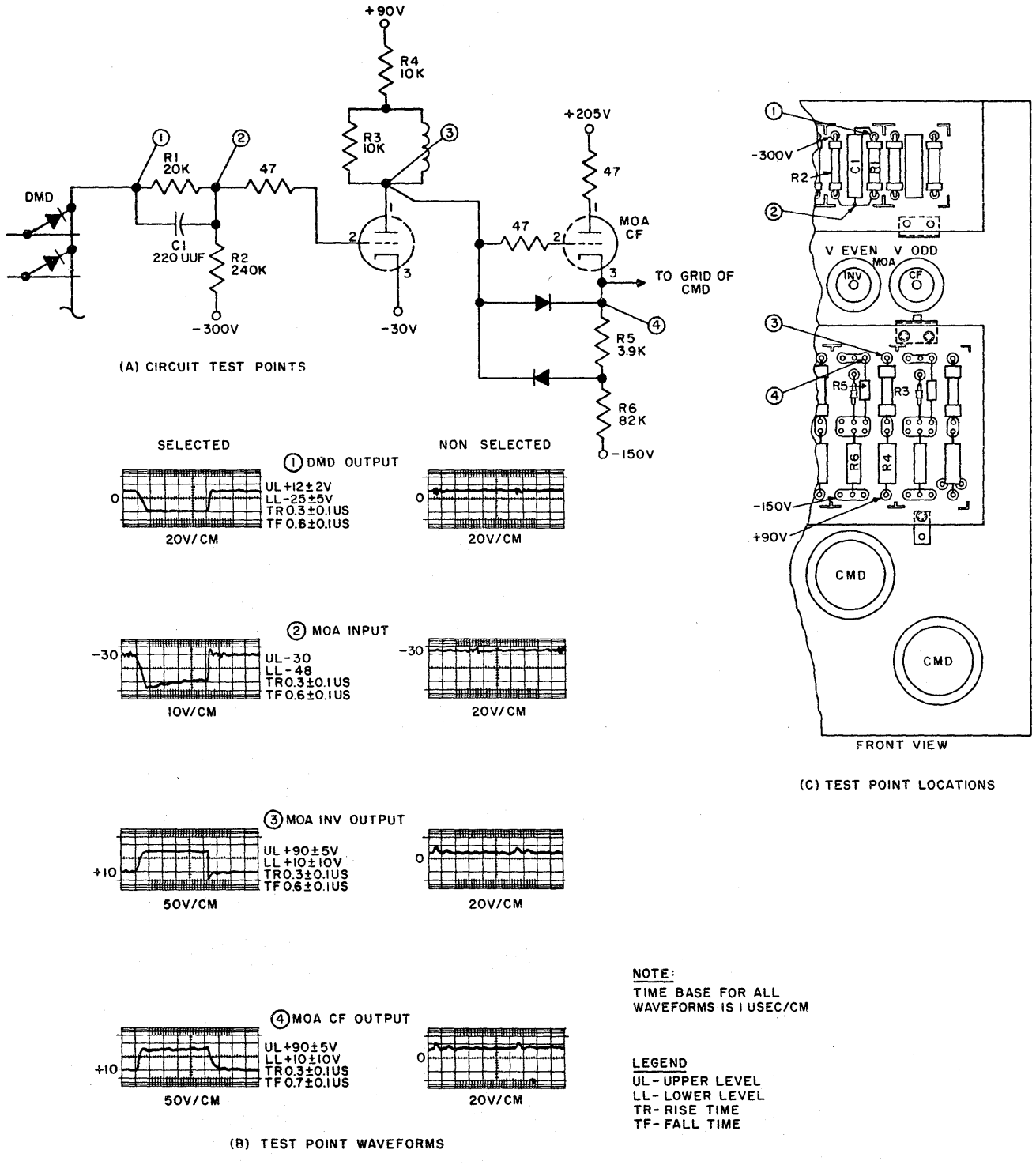
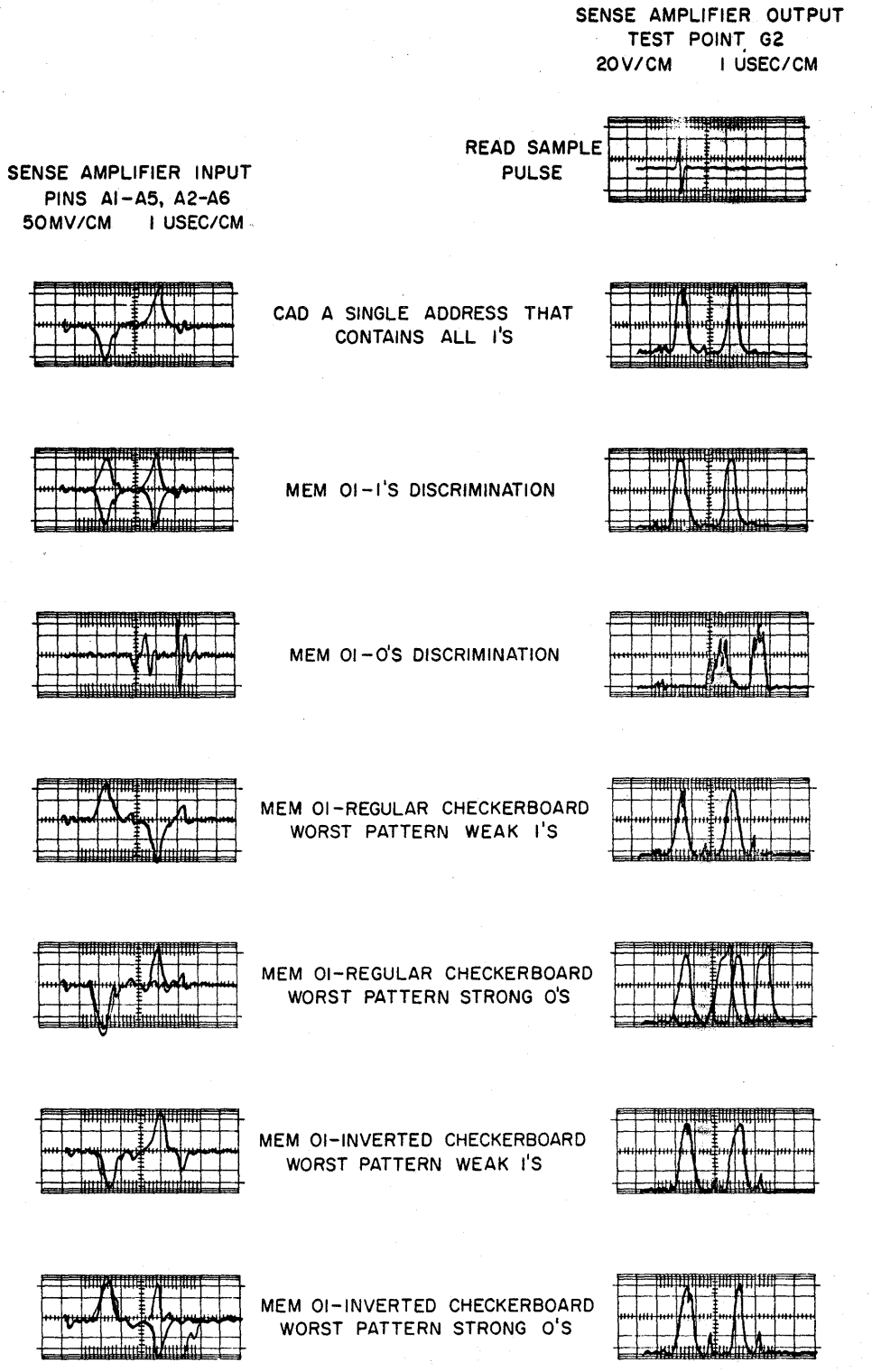
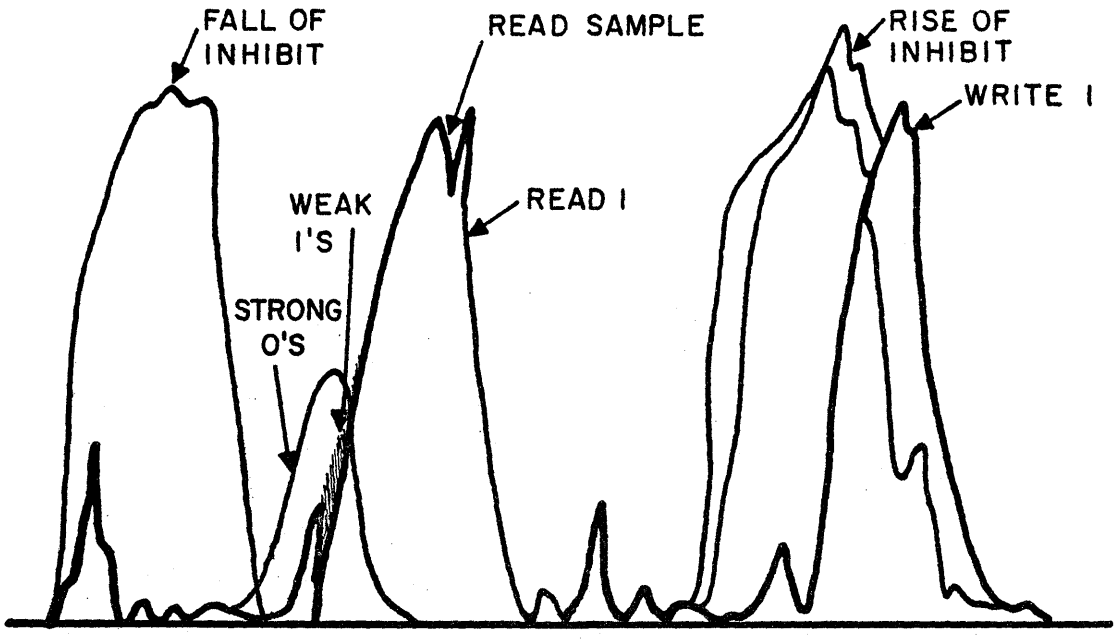


FIGURE 4-4. MEMORY DRIVER PANEL, WAVEFORM ANALYSIS



NOTES:
SA OUTPUT LOWER LIMIT IS -26V
FOR DETAILED ANALYSIS OF SA
OUTPUT WAVEFORMS SEE
FIGURE 4-6

FIGURE 4-5. SENSE AMPLIFIER, WAVEFORM ANALYSIS



NOTE: THE INDIVIDUAL WAVEFORMS OF FIGURE 4-5 ARE SHOWN COLLECTIVELY IN THIS ILLUSTRATION FOR IDENTIFICATION PURPOSES ONLY

FIGURE 4-6. SIGNAL IDENTIFICATION AT THE SA OUTPUT

TABLE 4-1. TEST CHART FOR DIODE MATRIX DECODER

Matrix Diodes	*Octal Address Groups
2^{1} or 2^{7}	0, 1, 4, 5, 10, 11, 14, 15, 20, 21, 24, 25, 30, 31, 34, 35, 40, 41, 44, 45, 50, 51, 54, 55, 60, 61, 64, 65, 70, 71, 74, 75.
2^{-1} or 2^{-7}	2, 3, 6, 7, 12, 13, 16, 17, 22, 23, 26, 27, 32, 33, 36, 37, 42, 43, 46, 47, 52, 53, 56, 57, 62, 63, 66, 67, 72, 73, 76, 77.
2^{2} or 2^{8}	0, 1, 2, 3, 10, 11, 12, 13, 20, 21, 22, 23, 30, 31, 32, 33, 40, 41, 42, 43, 50, 51, 52, 53, 60, 61, 62, 63, 70, 71, 72, 73.
2^{-2} or 2^{-8}	4, 5, 6, 7, 14, 15, 16, 17, 24, 25, 26, 27, 34, 35, 36, 37, 44, 45, 46, 47, 54, 55, 56, 57, 64, 65, 66, 67, 74, 75, 76, 77.
2^{3} or 2^{9}	0-7, 20-27, 40-47, 60-67.
2^{-3} or 2^{-9}	10-17, 30-37, 50-57, 70-77.
2^{4} or 2^{10}	0-17, 40-57.
2^{-4} or 2^{-10}	20-37, 60-77.
2^{5} or 2^{11}	0-37.
2^{-5} or 2^{-11}	40-77.

Note: *In the listed data, a diode is shorted if all the addresses in the group fail except two. The address pair that does not fail contains the defective diode.

TABLE 4-2. CHECK LIST OF MEMORY TROUBLE AREAS

Step	Procedure
1	Check the supply voltages at units 7, 8, and 9 (10, 11 and 12). This is to include the standard d-c and marginal check voltages (with and without excursion), filament voltages, and filament bias voltages. Compare these values with corresponding points on the other working memory.
2	Run margins to failure on the memory. This will expose any major problem areas. Record the results obtained since they are to be used again for comparison purposes in step 16.
3	Check the +90V decoupling circuitry in the memory driver panels; also the decoupling circuitry on the d-c distribution panel in unit 8 (11).
4	Remove all the memory driver panels and check that the grommets around the tubes are inserted correctly. Also check for bent pins on all pluggable units in units 7 and 9 (10 and 12), and ensure that each pluggable unit is correctly seated.
5	Check the waveshapes and timing relationships throughout the memory. This can best be accomplished as follows: by performing the preventive maintenance checks requiring scoping (refer to Instruction Bulletin 231); by photographing the read and write currents with a double exposure of the inhibit current to determine time relationships; by measuring the amplitude of the pip at the leading edge of the output of an even read MGG. If this latter pulse is too large it signifies that the set-memory and set-read pulses are too close together.
6	Check all control pulses and levels in the memory, and all signals fed to the memory for conformance to standard specifications.
7	Check the taper pin plugs on unit 8 (11) for a secure fit.
8	Perform all the preventive maintenance checks not requiring scoping (refer to Instruction Bulletin 231).
9	Visually inspect the memory for poorly soldered connections or incorrect wiring.
10	Check the -30V clamp diodes on the memory array.
11	Measure the resistance of: All inhibit windings for similar resistance All sense windings for similar resistance All drive lines through the array for similar resistance The ground side of each terminating resistor to ground
12	Measure the resistance of the grounding system throughout the array.
13	Adjust all DPD's for correct value (refer to Instruction Bulletin 232)
14	Ensure that the average read and write currents are the correct amplitude and that all inputs conform to specifications. Then check each individual read and write current against the standard average lines. Any discrepancies encountered should be thoroughly checked. (Refer to Instruction Bulletin 232.)

TABLE 4-2. CHECK LIST OF MEMORY TROUBLE AREAS (cont'd)

Step	Procedure
15	Run diagnostic programs to detect early peaking cores (refer to paragraph 5.4 in this Instruction Bulletin).
16	Upon the satisfactory completion of all the foregoing checks the memory is to be tuned (refer to Instruction Bulletin 232). Any of the memory pluggable units suspected of being bad should be replaced. An attempt should be made to obtain the highest possible margins.
17	Run margins to failure on the memory. Compare them against those taken in step 2.

4.2 TROUBLESHOOTING INTERMITTENT MEMORY PARITIES

4.2.1 Definition of Intermittent Memory Parities

An intermittent memory parity may be defined as a malfunction that occurs during the running of a program; however, it is non-recurrent when the same program is re-run or other programs are run to confirm the presence of the malfunction.

Since intermittent failures occur at random times, they are extremely difficult to analyze and correct. Any repair attempt is always shrouded in doubt regarding the benefit derived, because of the inability to duplicate the failure indication with the original equipment restored.

4.2.2 Recommended Action

A logical approach recommended for resolving intermittent memory parities is based on record keeping; that is, the recording of failure symptoms over an extended period of time. This procedure can provide a specific pattern which may be readily analyzed and corrective action instituted. For example, consider the analysis if, over a period of time, the recorded data on intermittents revealed the following failing addresses:

Y	X
33	42
36	26
43	24
52	76
77	60
42	34
07	16

A study of this data shows a consistent failure pattern in the X portion of the address in that they are all even numbers. This strongly suggests that the failures are intermittently caused by a defect in either the X- even MGG's, or the MAR bit 15 flip-flop.

To satisfactorily resolve intermittent conditions using record-keeping methods, pertinent data must be recorded on the incident report when a memory parity error is initially encountered. This must be done because when the error first occurs it is not immediately known whether the error is intermittent or solid. Specifically, the information to be provided on the incident report relative to a memory parity error is detailed in Field Technical Instruction (FTI) number 122. A summary of this FTI follows:

The important data required after a memory parity alarm has occurred consists of the bad parity word, the correct word, and the address in memory which failed, including the contents of memory at the failing address. This information may be obtained only when the program is in the specific option (there are three options available) determined by the settings of the following maintenance console switches:

MEMORY PARITY - ACTIVE switch in ACTIVE position

STOP - BRANCH switch in STOP position

With this option in effect, the program stops on a memory parity alarm and the aforementioned data requirements may be obtained as follows:

1. The bad parity word can be found in the memory buffer register.

2. The correct word is often difficult to determine. It sometimes may be found by analyzing the memory buffer register contents, or it may be necessary to refer to the program writeup of the program being run. When it is possible to determine the correct word, it should be recorded.

3. The address in memory which failed is the most important data required. If the computer stops before MAR is cleared, the required data is simply the contents of MAR. However, if MAR has been cleared, it is necessary to compare the contents of the left memory buffer register with the operations-index interval register. This comparison may yield any of the following conditions:

   a. If the left memory buffer register and the operations-index interval register are the same, and the branch flip-flop is clear, the failing address under these conditions is the program counter minus 1. Record this failing address and the contents of memory at this address.

   b. If the left memory buffer register and the operations-index interval register are the same and the branch flip-flop is set, the failing address under these conditions is the right A register minus 1. Record this failing address and the contents of memory at this address.

   c. If the left memory buffer register and the operations-index interval register are not the same, the failing address under

these conditions is either the address register, or the IO address counter minus 1. To determine which of these two registers is involved, it is necessary to know whether the memory cycle preceding the failure was a break cycle. If it was a break cycle, the contents of the IO address counter minus 1 designates the failing address. If it was not a break cycle, the contents of the address register designates the failing address. For either case, record the failing address and the contents of memory at this address. It is also possible for the condition to arise whereby the preceding cycle cannot be identified. Under these circumstances the only alternative is to record the contents of both the IO address counter and the address register, and the contents of both memory locations.

In practice, intermittent memory parities occurring over an extended period of time are recorded on many individual incident report forms. Evaluation of this data to establish a failure pattern is a time-consuming and ineffective process because of the large number of incident reports that must be screened to obtain the proper information. To facilitate meaningful record keeping of this data, it is recommended that the core memory log form (fig. 4-8, foldout) be used for this purpose. These forms (FED 204) are available at the sites and should be utilized to record the intermittent memory parity information directly from the incident reports on a continuing basis. In this manner, a handy reference is always available for detecting failure patterns.

SECTION 5

ANALYSIS OF SUBTLE ELECTRICAL CHARACTERISTICS IN MEMORY

5.1 SCOPE

This section analyzes certain memory characteristics that are not generally available or clearly defined in published form. They are of significant importance, however, in properly evaluating memory operation. These characteristics, each of which are discussed separately in the following paragraphs, cover the practical aspects of: component variations, program limitations, and circuit design on over-all equipment performance.

5.2 MAR $_C$PCF

This circuit consists of a single cathode follower stage which, in turn, feeds eight paralleled triodes that also function as cathode followers. The cathode return for the eight paralleled triodes is comprised of 18 resistors in parallel. Marginal-checking of this basic circuit has not porved to be too effective in the past in detecting aging tubes and/ or resistors. The result of component aging is deterioration of the rise and fall times of the MAR$_C$PCF signal, which may contribute intermittent memory failures.

Recognition of the foregoing facts will materially aid the Field Engineer in evaluating memory malfunctions, particularly of the intermittent type. In addition, a scheduled check for detecting MAR $_C$PCF circuit deficiencies has been incorporated into the preventive maintenance procedures for memory (refer to Instruction Bulletin 231). In these procedures, each of the MAR $_C$PCF circuits are scoped and the resultant waveforms are examined for conformance to specifications.

5.3 CHATHAM vs TUNG-SOL 5998 TUBES

Currently, 5998 tubes are supplied by two vendors: Chatham and Tung-Sol. It has been ascertained by an engineering study that the interelectrode capacitance is slightly higher in the Chatham tube. The immediate concern of field personnel is the effect of this difference on the interchangeability of the two vendors' tubes in the field.

Briefly, the use of a Chatham with its higher interelectrode capacitance will cause a slower rise time and consequently a narrower pulse width than a corresponding type Tung-Sol tube. The significant fact to consider is whether the decrease in width is of sufficient magnitude to prevent the inhibit current waveform from properly overlapping the write current waveform along the leading edge. (Refer to the preventive maintenance chart in Instruction Bulletin 231 for the specification.) If proper overlap is not maintained, the set-inhibit pulse must be moved to occur earlier, thus compensating for the

effect of the Chatham tube. Poor overlap will also be detected as poor margins on the -300 A1 (D1) line.

In practice, the substitution of Chatham for Tung-Sol tubes should not be construed as an automatic indication of an improper overlap condition. Instead, the following guide should be used to determine when the condition is most likely to occur:

a. If memories are factory-equipped with a combination of both vendors' tubes, the necessary compensation for the Chatham tube has been made prior to shipment and direct interchangeability is ensured.

b. If memories are factory-equipped with all Chatham tubes, the substitution of a Tung-Sol will result only in further improving (due to the wider response) the overlap. Hence, both vendors' tubes are directly interchangeable under these conditions.

c. If memories are factory equipped with all Tung-Sol tubes, it is possible that the substitution of a Chatham may adversely affect overlap, and necessitate the resetting of the set-inhibit pulse earlier in time. This condition will be invariably detected as poor margins on the -300A1 (D1) line.

5.4 PEAKING CORE CHARACTERISTICS

The cores in a memory plane, under identical operating conditions, do not all uniformly peak at the same time, nor with the same amplitudes. Core peaking may be classified into four general categories:

a. Normal

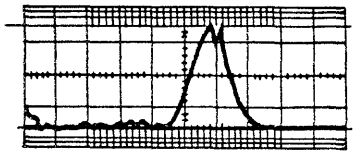
b. Early peaking

c. Late peaking

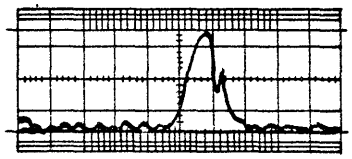
d. Low amplitude

Figure 5-1 illustrates examples of the four conditions as observed at the G2 test point of the sense amplifier. In each case, allied circuitry has been eliminated as a possible cause of the peaking conditions noted, so that the waveforms reflect the true characteristics of the core itself. Observation of the conditions shown do not necessarily imply defective cores. This is based on the fact that since core characteristics are known to vary, the criterion to be used to determine a core's acceptance is proper memory operation; that is, if margins are good, and reliable memory operation is present, the core is acceptable. Under these conditions, it is always considered good practice to record the location of the suspect core(s) for future failure analysis. This course of action is particularly important because it is conceivable that at some future date, under adequate margins, these cores will probably be the first to fail.

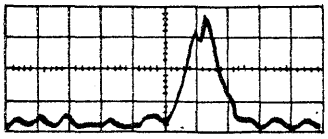
As a guide for field use, the following specific procedures are recommended whenever a core is suspected of causing unreliable memory operation:



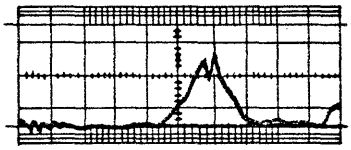
(A) NORMAL



(B) EARLY



(C) LATE



(D) LOW AMPLITUDE

FIGURE 5-1. CORE PEAKING CHARACTERISTICS

1. Eliminate all allied circuitry as a possible contributing cause to the core characteristic observed. In this regard, it is recommended that the core output signals be examined at the A1-A5 (A2-A6) input test points of the sense amplifier using a Tektronix 53/54G pre-amplifier with a Tektronix 545 oscilloscope.

2. Ascertain the average peaking characteristics by measuring a sufficient quantity of cores to establish this value.

3. Using the average value as a reference, measure the suspect core(s). If the peaking (early or late) exceeds ±0.1 usec of average, or if the core's amplitude is less than 80 percent of average, expedite the pertinent information, including photographs, to Field Technical Assistance, Department 912.

5.5 PRF CONDITIONS

Due to variations in circuit loading, the drive currents produced while reading and writing 0's differ from those obtained while reading and writing 1's. This occurs because, to read and write all 1's, the cores must be switched; whereas, to read and write all 0's, the cores remain at 0 and consequently are not switched. The resultant relationships appear in figure 5-2, and may be summed up as follows:

a. Read 0 is always greater than read 1

b. Write 0 is always greater than write 1

c. Read 0 = write 0
d. Read 1 = write 1
} if properly adjusted.

It can be appreciated, therefore, that during the running of various patterns dictated by program content, the amplitude of read and write currents will vary accordingly. This variation is slight for one memory cycle; however, when a pattern is programmed at a rapid PRF rate the CMD transformer causes a bias build-up that increases the read or write current above the nominal value. This characteristic is analagous to the results obtained while placing excursions on the -300 B1, B2 (E1,E2) MC lines. As a result, if the read and write margins are inadequate the current variations due to the program may exceed those current variations due to the margins, and failure will result.

The magnitude of current increase above the nominal value is dependent on the memory tune characteristics. To illustrate, if a memory is tuned for either reading 0's and writing 0's, or reading 1's and writing 1's, the areas under read and write (see shaded areas in fig. 5-2) are equal. Under these conditions, if a program is run that predominantly employs a pattern duplicating that used for the memory tune, the read and write currents will remain balanced and no CMD bias build-up will result. Conversely, if the program consists of a predominant read 1 write 0 pattern, the currents will be unbalanced and a bias build-up will occur in the direction of write, shown as line AB in figure 5-3. If the program utilizes a predominant read 0 write 1 pattern, the currents will be unbalanced and a bias build-up will occur in the direction of read, shown as line AC in figure 5-3. For either case, the memory tune pattern falls midway between the two possible unbalanced conditions.

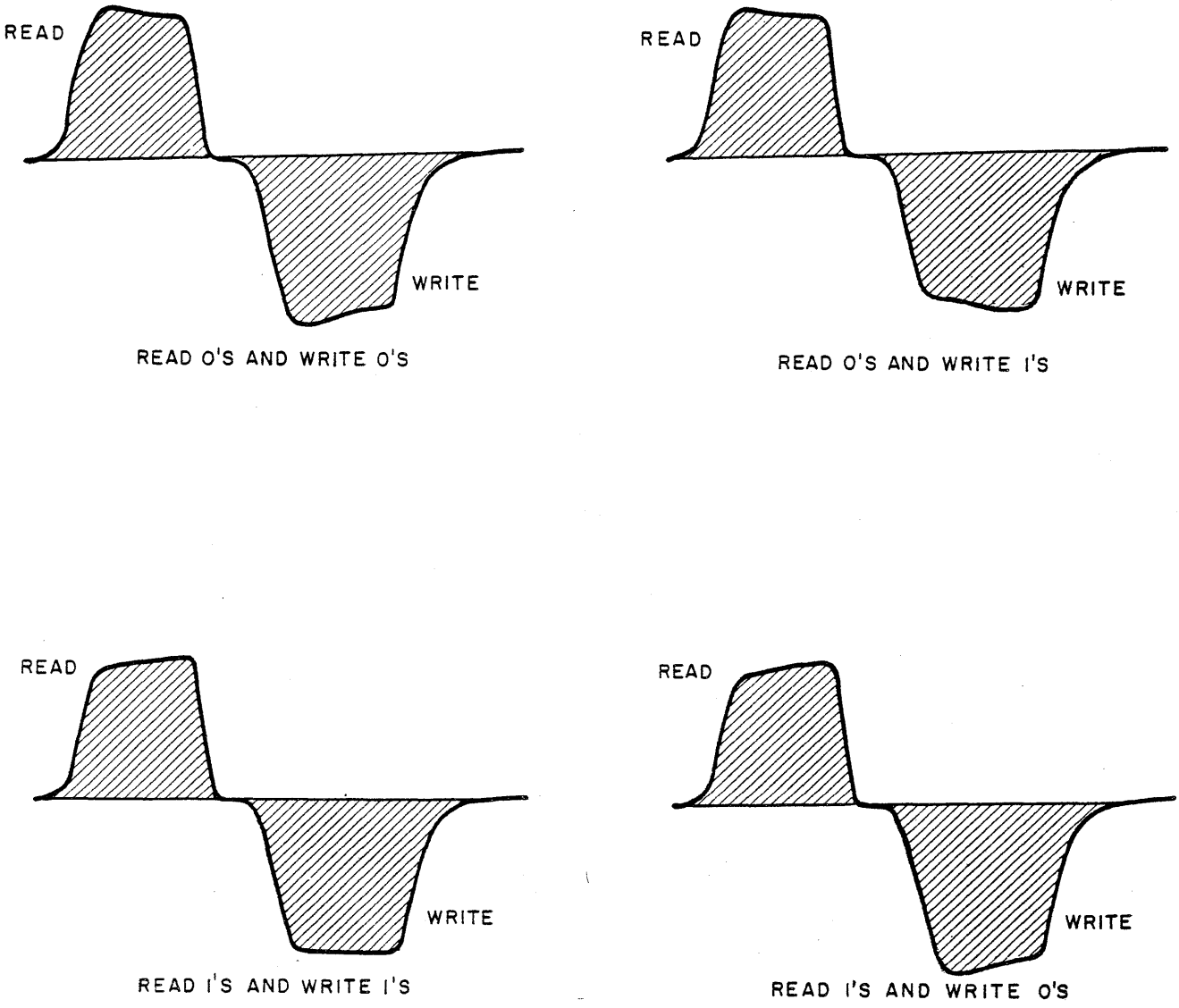


FIGURE 5-2. READ AND WRITE CURRENT VARIATIONS

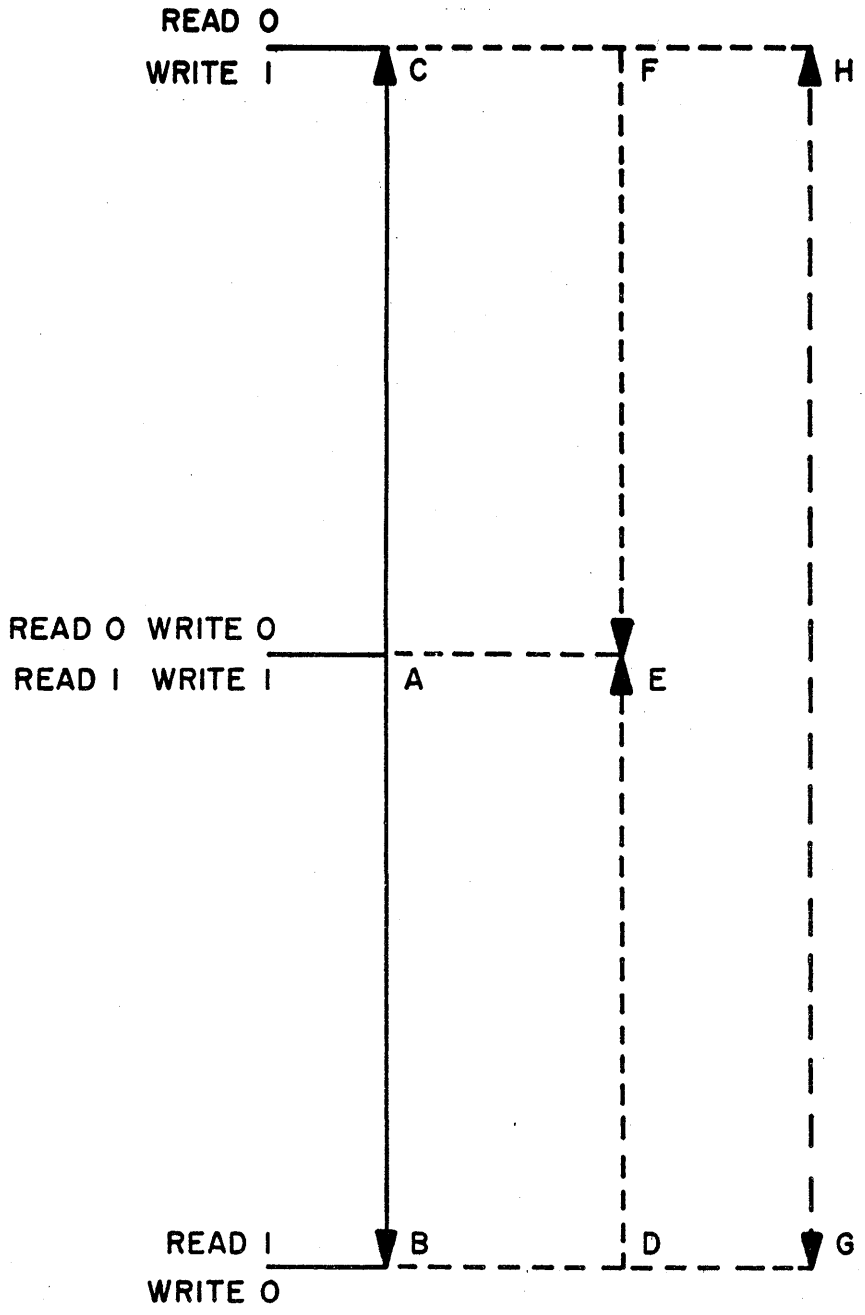


FIGURE 5-3. CURRENT UNBALANCE WITH PROGRAM CONTENT

If the memory was tuned instead to either read 1 write 0, or read 0 write 1, the degree of unbalance attained with respect to a program that consisted primarily of reading and writing 0's or 1's is approximately the same as before. (See lines DE and FE respectively in figure 5-3.) However, the unbalance would be considerable, shown as line GH in figure 5-3, if the memory is tuned to read 1 write 0 and the program content consists primarily of the pattern read 0 write 1. A similar unbalance would result, shown as line HG in figure 5-3, if the memory was tuned to read 0 write 1, and the program content was predominantly read 1 write 0. The latest tuning procedures (refer to Instruction Bulletin 232) have been planned and developed on the basis of the aforementioned theories.

5.6 ANALYSIS OF VARIOUS TIMING RELATIONSHIPS

5.6.1 General

The subject matter in the subsequent paragraphs is the type of information that may conceivably be overlooked during an investigation of memory malfunctions and is presented for the purpose of emphasizing the highly significant characteristics involved.

5.6.2 Differences in Sample Time for Left and Right Half-Words

This subject analysis will help explain why, in certain printouts with margins, only one half of the word seems to contain most of the errors.

The reason is based primarily on the different signal paths taken by the sample pulse for the respective half-words:

a. For the left half-word, the sample pulse path is from 10AC to 12CF to the pluggable units in Unit 12.

b. For the right half-word, the sample pulse path is from 10AC to 12CF to 10AF to the pluggable units in Unit 10.

Analysis of the signal paths reveals that the sample pulse for the right half-word traverses a greater distance due to the modular layout employed. As a result, the sample for the right half-word occurs slightly later than for the left half-word. This difference may be seen, if carefully observed with an oscilloscope, at the G2 test point of any sense amplifier.

The difference, under normal operating conditions, is negligible and should not impair memory operation. However, if sample is not adjusted properly, the effect may show predominantly in only one-half of the word.

5.6.3 Start-Memory Pulse

The start-memory pulse is available from three sources: during the PT cycle from the program counter, during the OT cycle from the address register, and during the BI or BO cycles from the IO address counter.

The signal path, for the respective start-memory pulses, is through a multitude of amplifiers, gates, and cables of varying lengths that connect different modules to the memory pulse distributor. The inevitable result is that the three start-memory pulses

may arrive at the memory pulse distributor with varying time delays. Since each start-memory pulse is used to initiate its respective cycle, one memory cycle may end later than usual and overlap the start of the following cycle. As an example, a condition may arise whereby the noise from the fall of inhibit will appear in the next cycle and contribute to PRF troubles.

To aid the Field Engineer in detecting such problems, a periodic timing check is specified for the three start-memory pulses in the preventive maintenance procedures for memory. (Refer to Instruction Bulletin 231.)

5.6.4 Read and Write Current Widths

To ensure the proper switching of cores, adequate read and write currents must be provided.

When improper core switching is indicated as the problem, the width of the read and write currents, as measured at the 90 percent points, must be examined for conformance to the following specifications: read must be a minimum of 1.3 usec, and write must be a minimum of 1.2 usec.

5.7 DPD DECOUPLING

5.7.1 Failure Symptoms

A problem which has the effect of producing spurious oscillations (noise) on the -150V or +150V lines is invariably due to a defect in the DPD decoupling circuitry located in the Z module (see fig. 2-11). The specific indications of faulty DPD decoupling are:

a. Memory operates erratically.

b. The +150 DPD DECOUPLER and -150 DPD DECOUPLER lights on the Z module are not lit, although the bulbs are good.

In order to properly evaluate troubles within this area, knowledge of circuit operation is important. This is presented in the following paragraph.

5.7.2 Circuit Description

The decoupling circuitry utlizes six relays which are connected to the -48V d-c source as shown in figure 5-4. These relays are of the instantaneous type except for K1 which is a 10-second thermal delay relay.

The composite circuitry including the decoupling capacitors C1 through C8 is depicted in simplified form in figure 5-5. Reference should be made to figures 5-4 and 5-5 for the circuit description that follows.

When d-c voltage is applied, -48V dc picks K3 and K4. This permits +150V to charge the decoupling capacitors C1, C2, C5, and C6, and -150V to charge the decoupling capacitors C3, C4, C7, and C8. The charging path is through the respective current-limiting resistors designated R1. These resistors prevent the charging current from exceeding the ratings of the circuit breakers 12Z3 -J13, -J19, -L1, and -L2. After 10

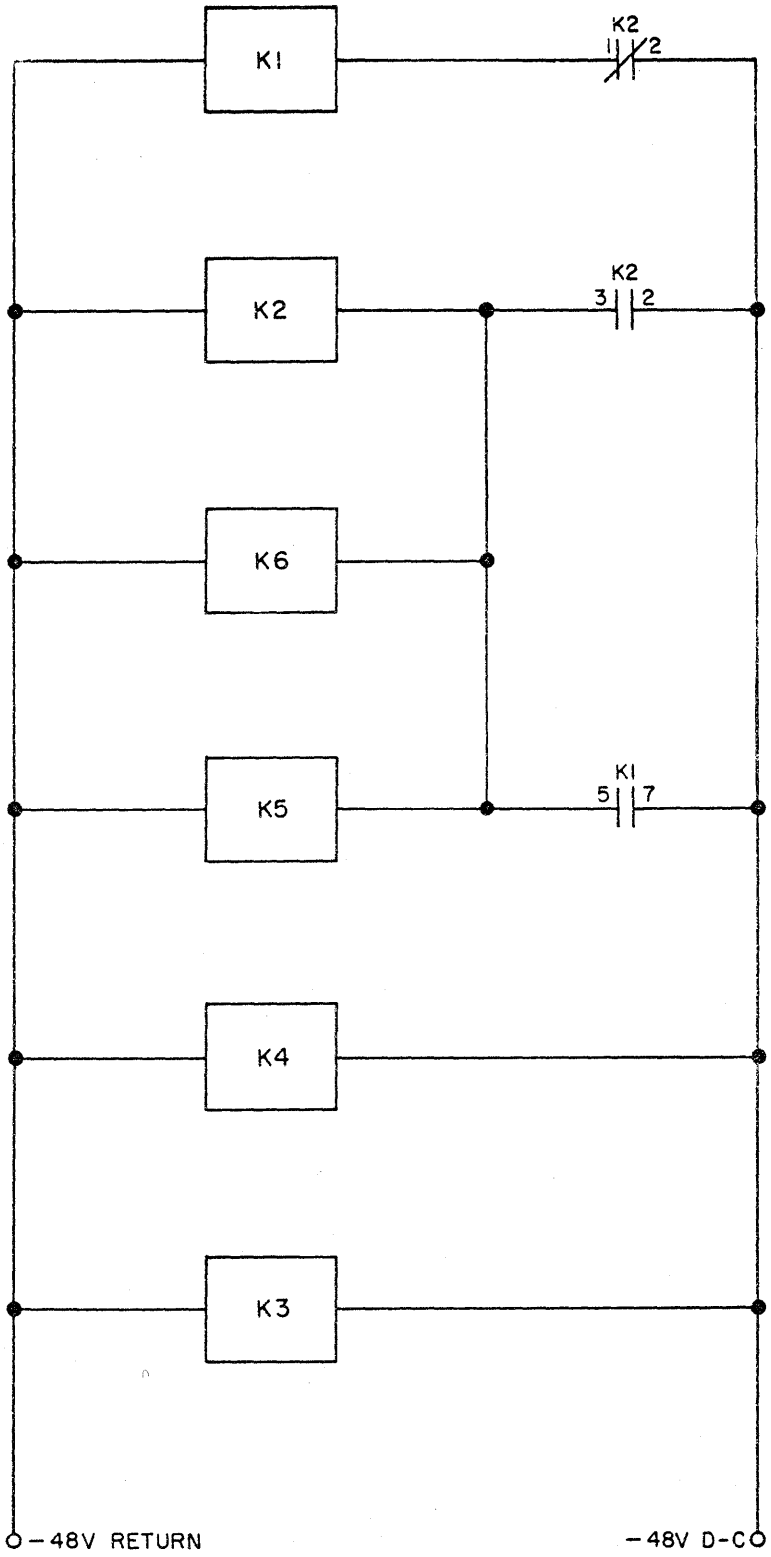


FIGURE 5-4. RELAY CONNECTIONS, DPD DECOUPLING

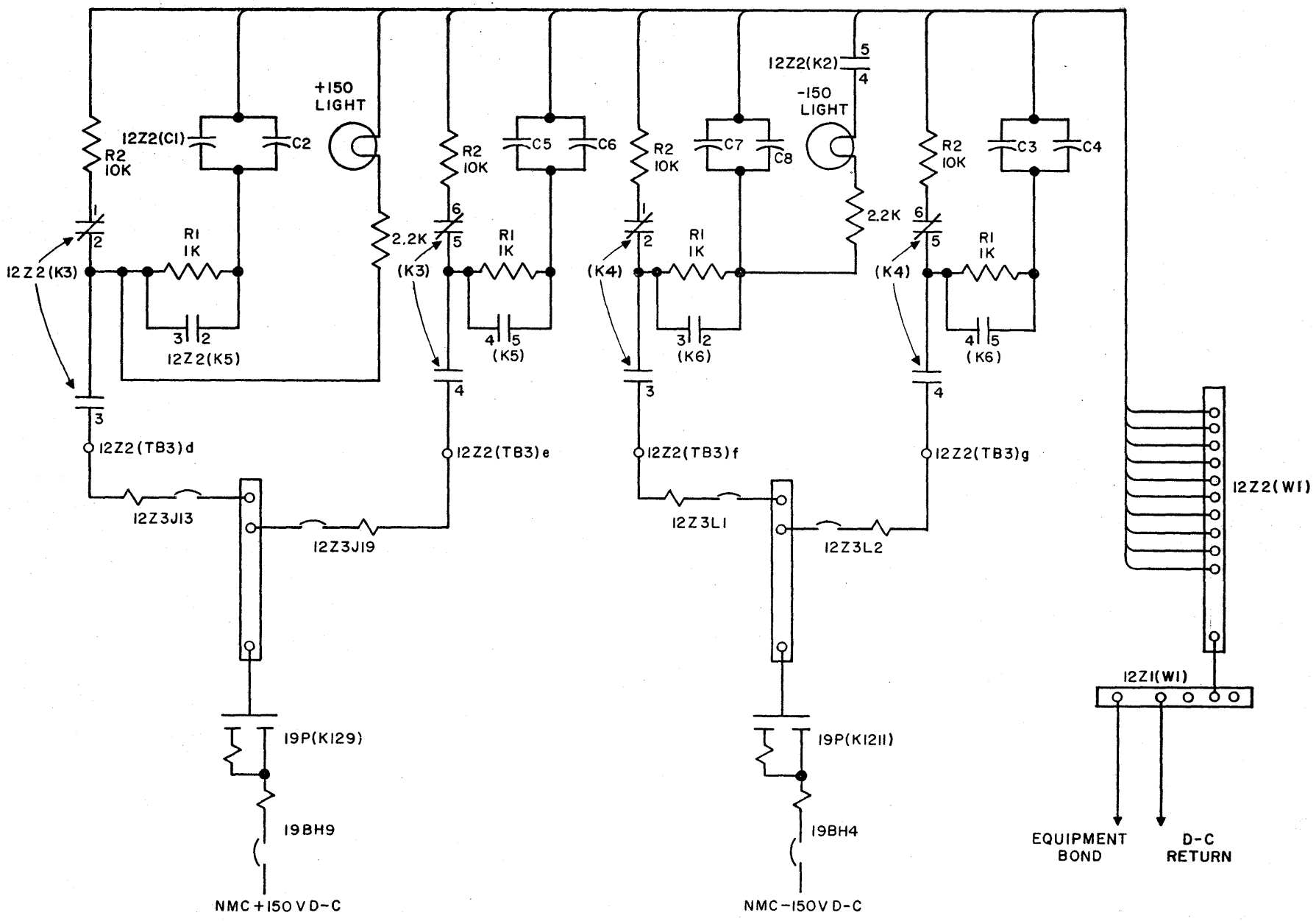


FIGURE 5-5. DPD DECOUPLING CIRCUITRY, SIMPLIFIED DIAGRAM

UNCLASSIFIED

seconds, relay K1 is energized and picks K2, K5, and K6. Relay K2 holds K5, K6, and K2,- and drops K1. Relay K2 also completes the -150V lamp circuit. Relays K5 and K6 short out their respective current-limiting resistors (R1) thus permitting the capacitors C1 through C8 to decouple any spurious information present on the -150V and +150V lines.

When the -48V dc is removed, the decoupling capacitors are discharged respectively through a path consisting of: the current-limiting resistors designated R2, the K3 and K4 relay points shown, and the current-limiting resistors designated R1.

5.8 MEMORY ARRAY FLOATING GROUND

The drive-line paralleled 10-ohm terminating resistors (effective load of 5 ohms) are not returned directly to ground (fig. 5-6) because it was found that such a connection introduced noise on the drive lines, resulting in lowered margins. Hence, an accidental ground such as may be introduced during troubleshooting (solder splash or other foreign matter) will adversely affect margins.

The inclusion of the ODD V circuit breaker (CB) was dictated by good design practice. Since the memory array operates better without a ground connection, a safety hazard condition arose based on the possibility of a short developing between the primary (250V) and secondary windings of the CMD transformer. Under these conditions, the memory array would be hot and maintenance personnel working on it would be endangered. Protection against this possibility is afforded by the CB. The 240-ohm resistor, in addition to limiting the current through the CB, further isolates the memory array from ground.

Summarizing: for best operation, the memory array must be maintained above ground. In addition, for safety reasons, the memory array must be returned to ground. Both conditions are satisfied by the use of the 240-ohm resistor and the CB (which has an inherent resistance of approximately 130 ohms) in a floating-ground arrangement.

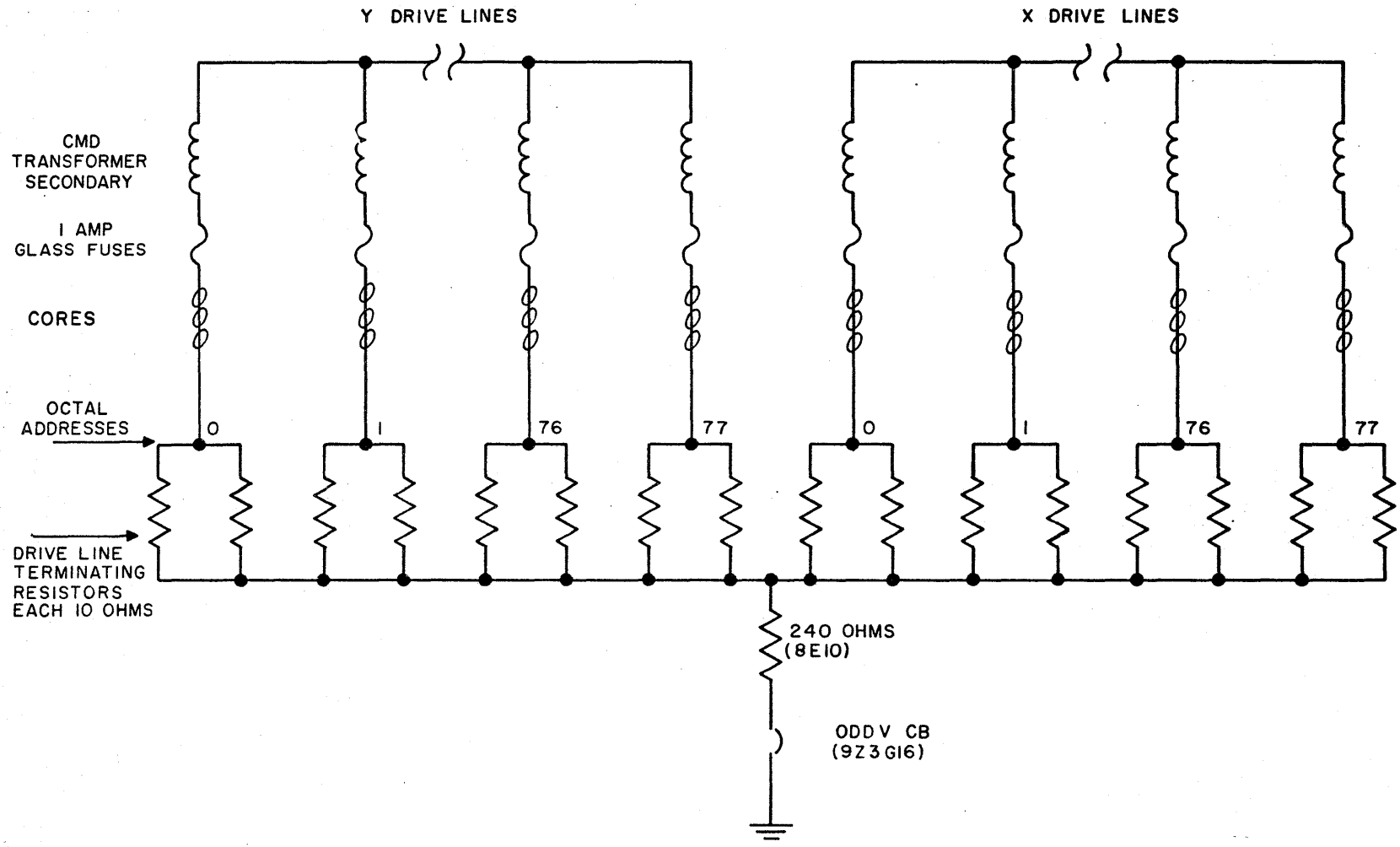


FIGURE 5-6. MEMORY ARRAY FLOATING GROUND

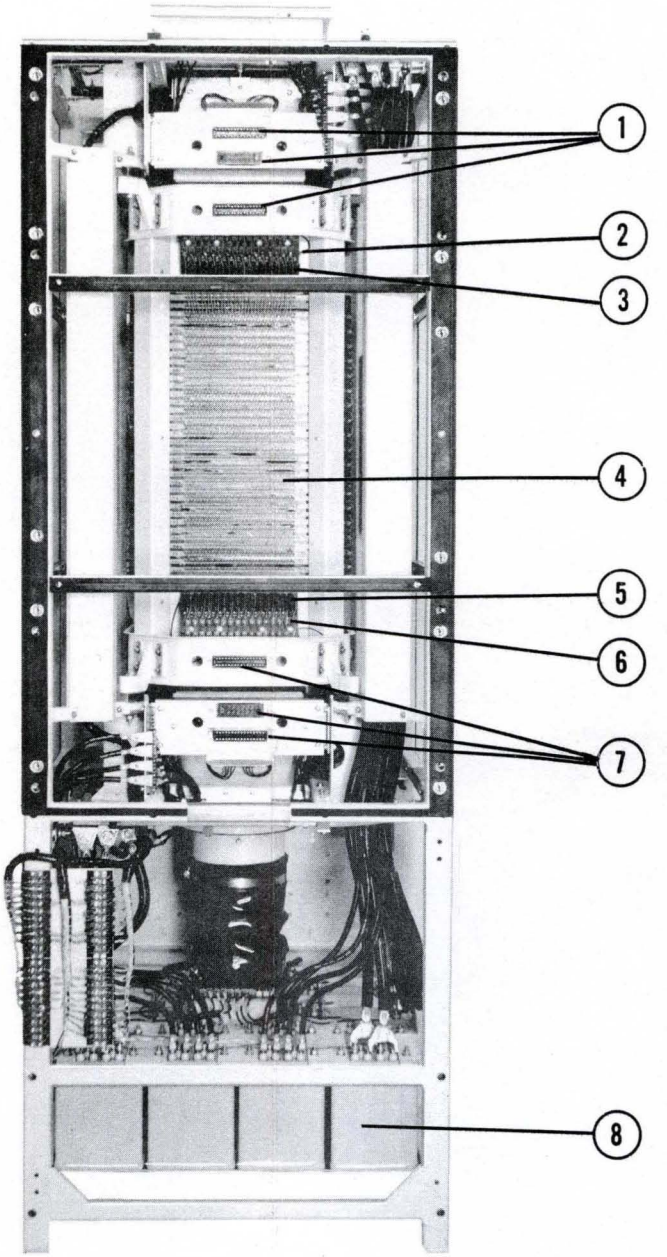


FIGURE 2-3. MEMORY ARRAY FRONT VIEW, COVERS REMOVED

Legend

1 – Connectors for driver panel XA
2 – Drive-line fuses for driver panel XA
} addresses 0-17

3 – Drive-line terminating resistors for driver panel XD (addresses 60-77)

4 – Array cage consisting of 36 core-memory planes in the following order, top to bottom:

Plane No.	Designation	Plane No.	Designation
1	Dummy	19	L7
2	Dummy	20	R8
3	L15	21	L6
4	R15	22	R7
5	L14	23	L5
6	R14	24	R6
7	L13	25	L4
8	R13	26	R5
9	L12	27	L3
10	R12	28	R4
11	L11	29	L2
12	R11	30	R3
13	L10	31	L1
14	R10	32	R2
15	L9	33	LS
16	R9	34	R1
17	L8	35	Parity
18	Spare	36	RS

5 – Drive-line terminating resistors for driver panel XA (addresses 0-17)

6 – Drive-line fuses for driver panel XD
7 – Connectors for driver panel XD
} addresses 60-77

8 – Filament transformers

Note: All address designations are in octal notation reading from left to right when facing the front side of the memory array.

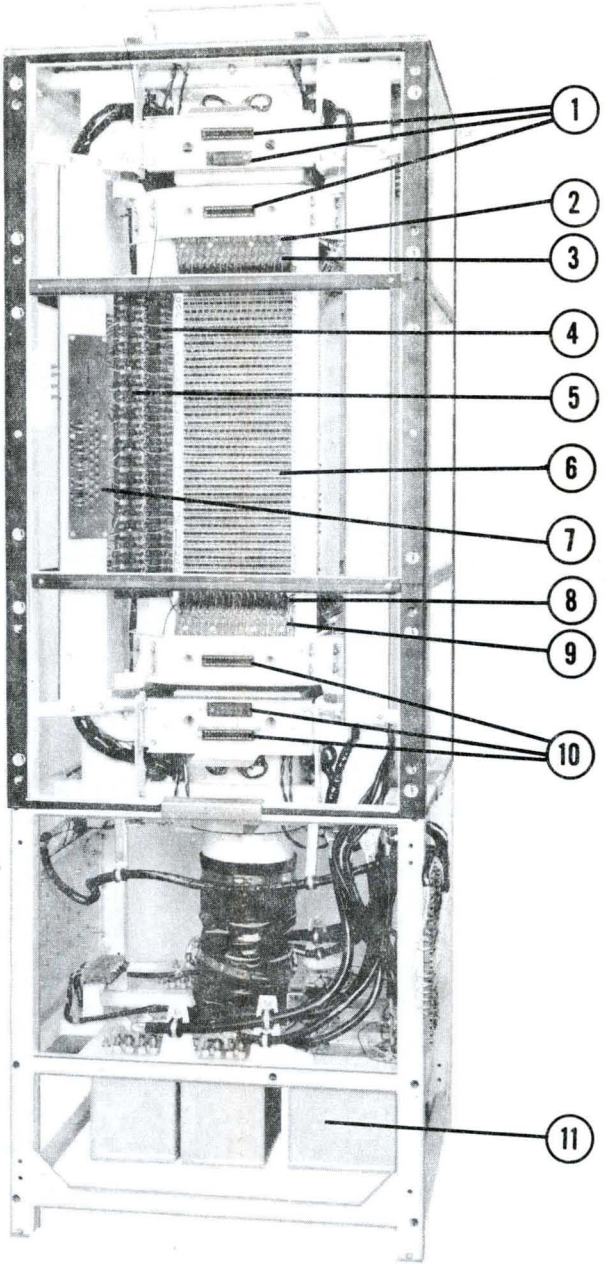


FIGURE 2-4. MEMORY ARRAY LEFT SIDE VIEW, COVERS REMOVED

Legend

1 – Connectors for driver panel YB
2 – Drive-line fuses for driver panel YB
} addresses 37-20

3 – Drive-line terminating resistors for driver panel YC (addresses 57-40)

4 – Inhibit-line terminating resistors for LHW
5 – Inhibit-line fuses for the LHW
} top to bottom: dummy, L15, L14, ... Parity

6 – Array cage consisting of 36 core-memory planes
See figure 2-3, foldout for designations

7 – Diode clamp board - the diodes mounted thereon are used to clamp the MOA inputs to -30V for the X addresses

8 – Drive-line terminating resistors for driver panel YB (addresses 37-20)

9 – Drive-line fuses for driver panel YC
10 – Connectors for driver panel YC
} Addresses 57-40

11 – Filament transformers

Note: All address designations are in octal notation reading from left to right when facing the left side of the memory array.

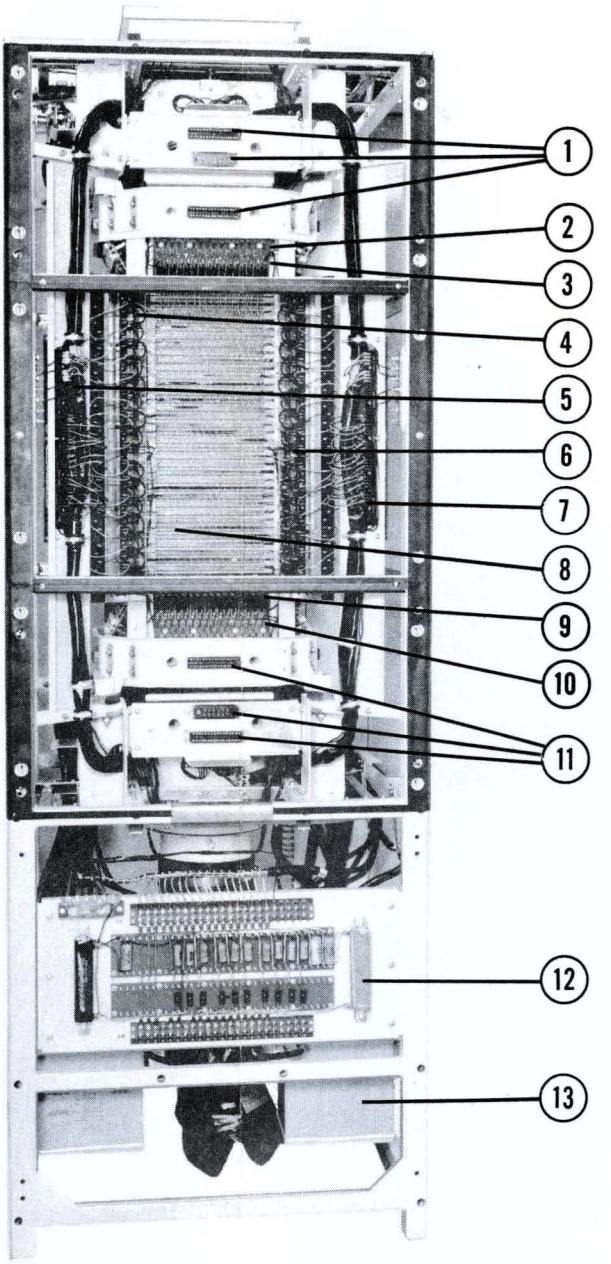


FIGURE 2-5. MEMORY ARRAY REAR VIEW, COVERS REMOVED

Legend

1 – Connectors for driver panel XB
2 – Drive-line fuses for driver panel XB
} addresses 37-20

3 – Drive-line terminating resistors for driver panel XC (addresses 57-40)

4 – Taper-pin terminal board for sense and inhibit winding connections, right half-word

5 – Taper-pin terminal board for the following Y-address connections: MAR to DMD, and MGG to CMD

6 – Taper-pin terminal board for sense and inhibit winding connections, left half-word

7 – Taper-pin terminal board for the following X-address connections: MAR to DMD, and MGG to CMD

8 – Array cage consisting of 36 core-memory planes. See figure 2-3, foldout, for designations

9 – Drive-line terminating resistors for driver panel XB (addresses 37-20)

10 – Drive-line fuses for driver panel XC
11 – Connectors for driver panel XC
} addresses 57-40

12 – D-C distribution panel assembly

13 – Filament transformers

Note: All address designations are in octal notation reading from left to right when facing the rear side of the memory array.

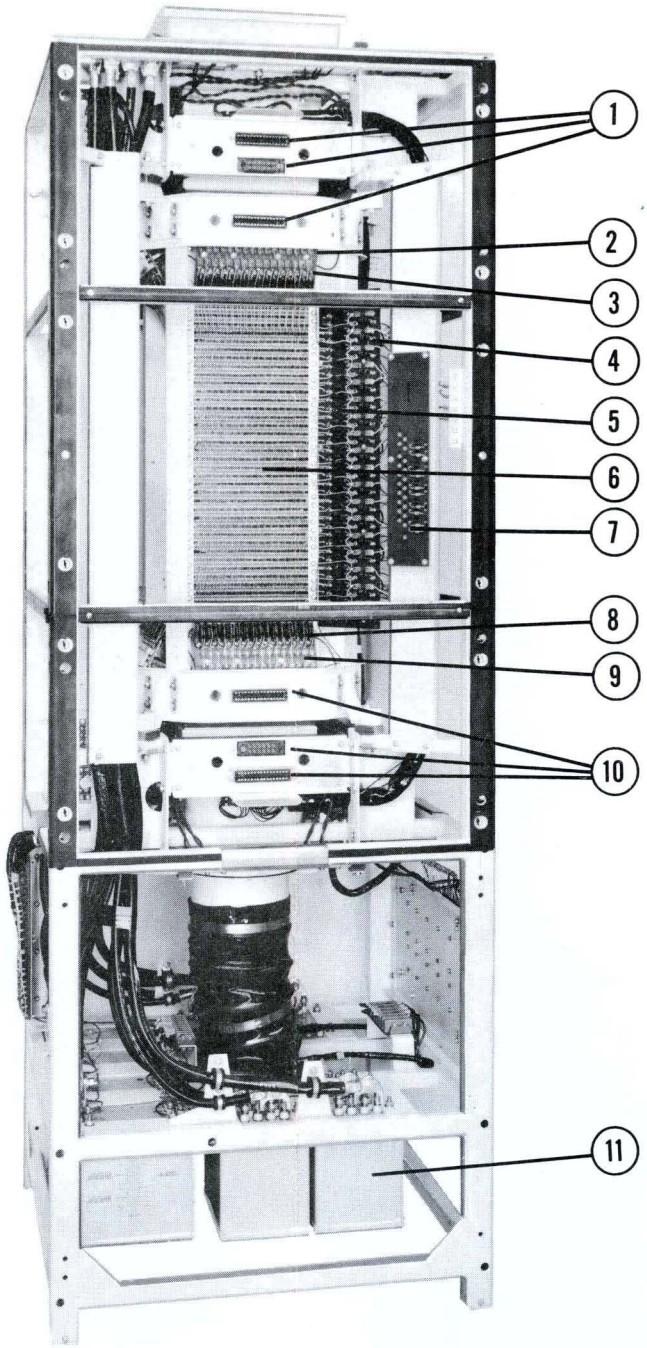


FIGURE 2-6. MEMORY ARRAY RIGHT SIDE VIEW, COVERS REMOVED

Legend

1 – Connectors for driver panel YA
2 – Drive-line fuses for driver panel YA
} addresses 00-17

3 – Drive-line terminating resistors for driver panel YD (addresses 60-77)

4 – Inhibit-line fuses for the RHW
5 – Inhibit-line terminating resistors for RHW
} top to bottom: dummy, R15 to R9, spare, and R8 to RS

6 – Array cage consisting of 36 core-memory planes. See figure 2-3, foldout, for designations

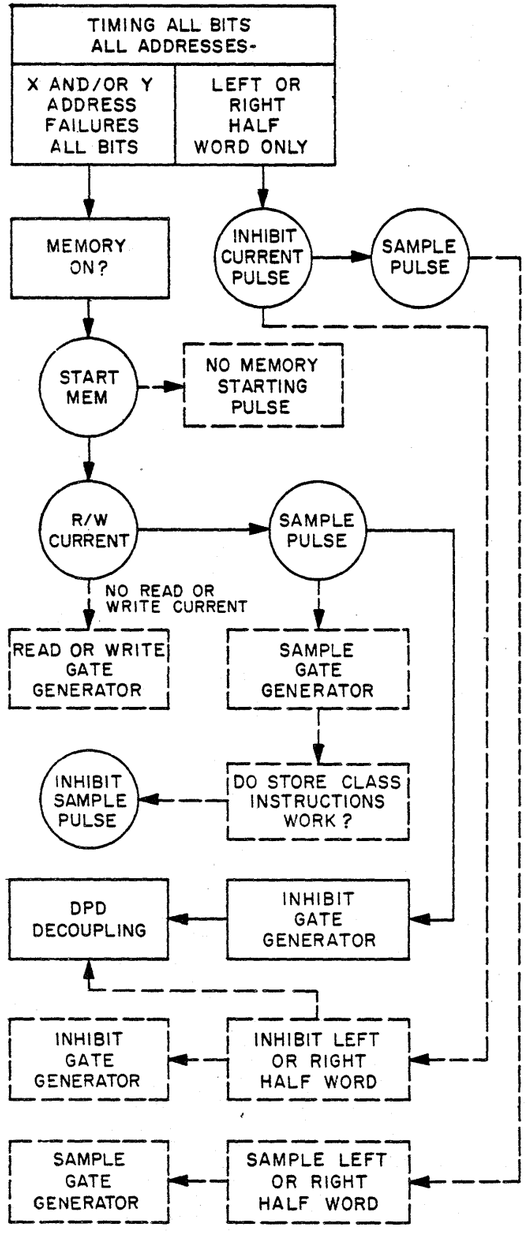
7 – Diode clamp board - the diodes mounted thereon are used to clamp the MOA inputs to -30V for the Y addresses.

8 – Drive-line terminating resistors for driver panel YA (addresses 00-17)

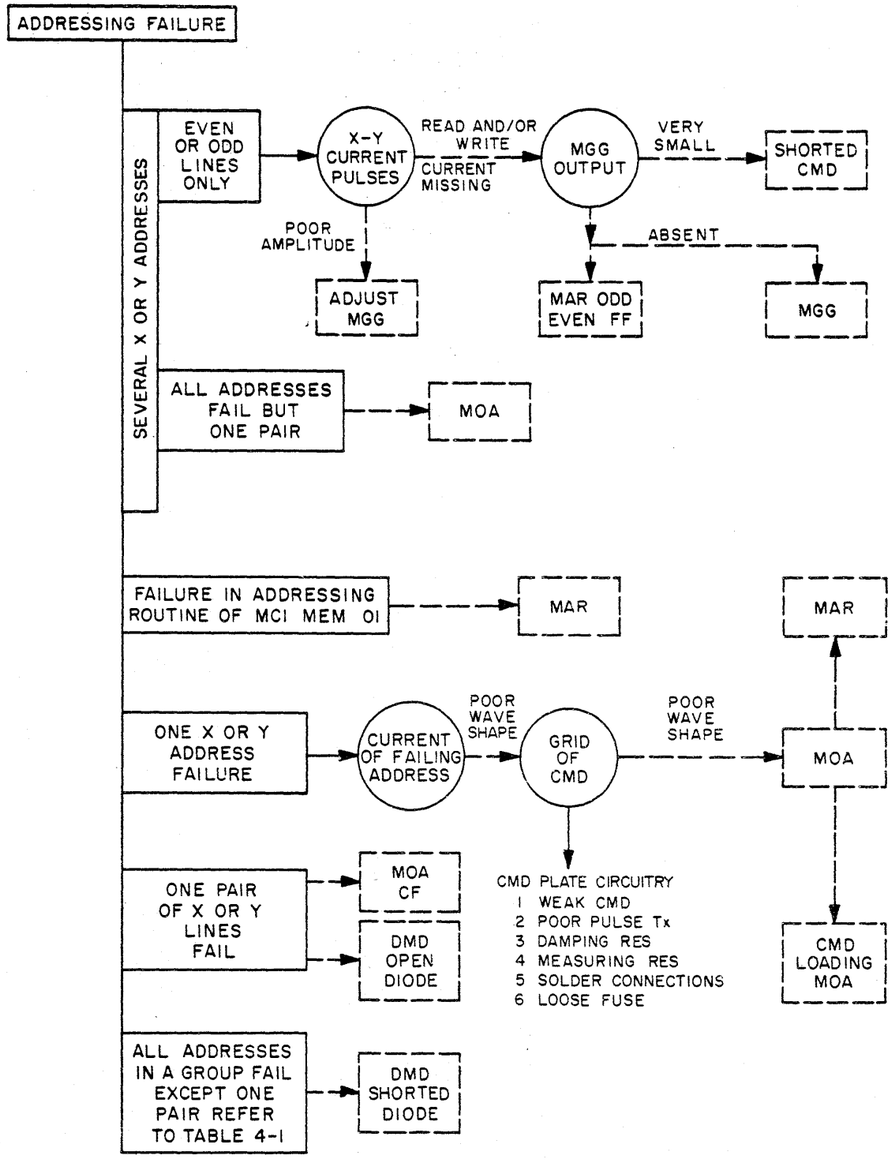
9 – Drive-line fuses for driver panel YD
10 – Connectors for driver panel YD
} addresses 60-77

11 – Filament transformers

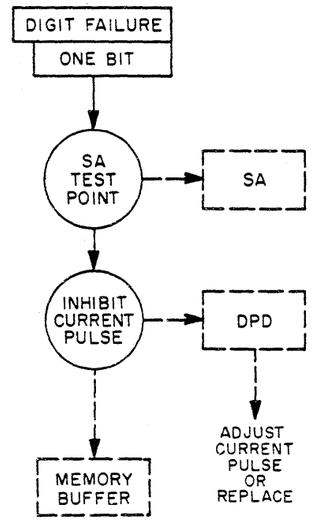
Note: All address designations are in octal notation reading from left to right when facing the right side of the memory array.



(A) TIMING FAILURES



(B) ADDRESSING FAILURES



(C) DIGIT FAILURES

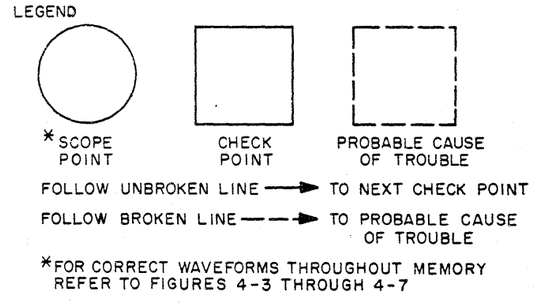


FIGURE 4-2. TROUBLESHOOTING GUIDE FOR TIMING, ADDRESSING, OR DIGIT FAILURES

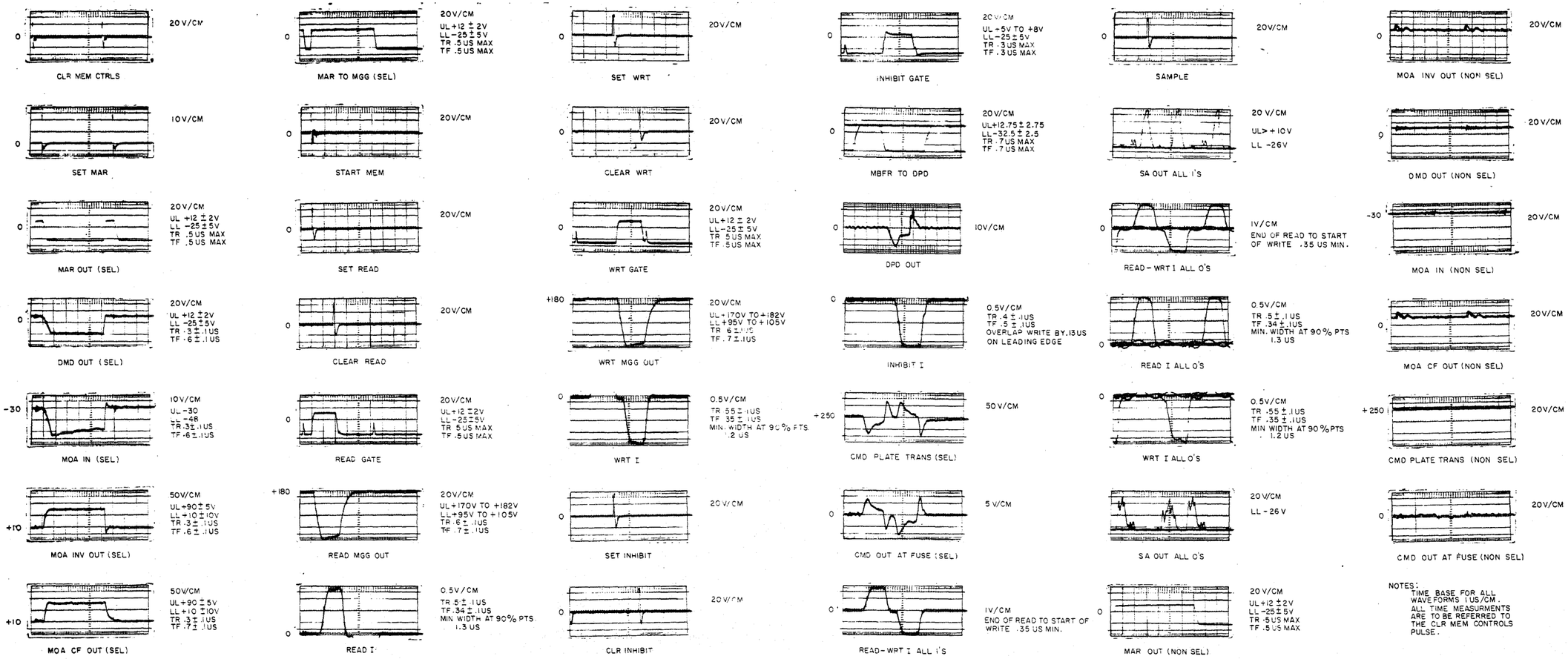


FIGURE 4-7. TYPICAL MEMORY WAVEFORMS

CORE MEMORY LOG

SITE NO. _____ COMPUTER _____ MEMORY _____ SHEET NO. _____

INCIDENT NO.	MEM.PAR.		MEM. BFR. CONTENTS			FAILING LOC. CONTENTS			BAD BITS	FAILING ADR.	FAILING PROG AND ROUTINE	M. C. DATA					FINAL CORRECTIVE ACTION AND COMMENTS
	YES	NO	P	LHW	RHW	P	LHW	RHW				G.P.	VOLT.	CKT.	LINE	EXC.	

FIGURE 4-8. FORM FOR LOGGING INTERMITTENT MEMORY PARITIES