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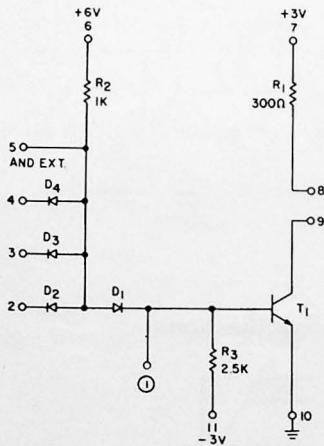
Functional Description

The AND Inverter, AI-1A module consists of three diode positive AND circuits followed by a saturating transistor inverter.

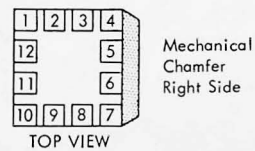
Pins 2, 3 and 4 are the AND inputs, connecting Pin 5 to the common anode diodes (FDD module) to extend the AND Fan In. This module is capable of higher fan-out than the AI-2A module and should be used in applications that require a power inverter.

The OR function can be accomplished by dotting collectors (parallel connected collectors) with other modules - only one collector resistor is required.

Schematic

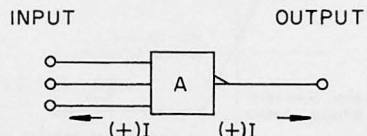


Terminal Configuration



Pins 1 and 12 Leave Open

Block Diagram



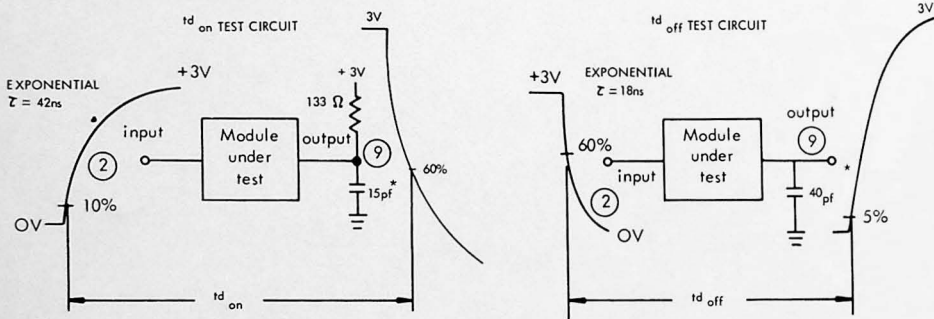
Maximum Ratings

Input Voltage = 13V
 Output Voltage = 6V
 $I_E = 40$ Milliamps

AI-1A Module Functional Tests

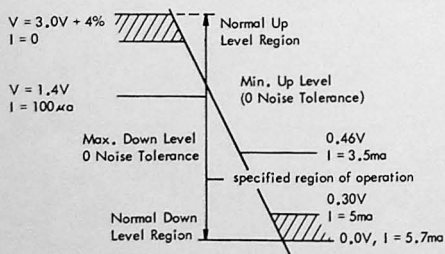
TESTS	TERMINAL CONDITIONS												o C	ADDITIONAL LOAD REQUIREMENTS	VARI-ABLE	LIMITS		UNITS
	1	2	3	4	5	6	7	8	9	10	11	12				MIN	MAX	
DC ON		+1.4V	+1.4V	+1.4V		+5.76V	+3.12V	V_0	V_0	GND	-3.12V	25 75	28 ma CURRENT INTO TERMINAL 8	V_0		0.3 0.31	V	
DC ON		+1.4V	+1.4V	+1.4V		+5.76V	+3.12V	V_0	V_0	GND	-3.12V	25		V_0		0.15	V	
DC OFF		+0.35V	+6.0V	+6.0V		+6.24V	+2.88V	V_0	V_0	GND	-2.88V	25		V_0	2.84		V	
DC OFF		+6.0V	+0.35V	+6.0V		+6.24V	+2.88V	V_0	V_0	GND	-2.88V	25		V_0	2.84		V	
DC OFF		+6.0V	+6.0V	+0.35V		+6.24V	+2.88V	V_0	V_0	GND	-2.88V	25		V_0	2.84		V	
DC NOISE					-1.13V		+2.88V	V_0	V_0	GND	-2.88V	75		V_0	1.8		V	
$t_{d_{on}}$	INPUT	+3.0V	+3.0V		+6.0V	+3.0V	15 pf CAP TO GND	OUTPUT	GND	-3.0V		25	133Ω RESISTOR TIED BETWEEN TERMINALS 7&8	$t_{d_{on}}$	5	20	ns	
$t_{d_{off}}$	INPUT	+3.0V	+3.0V		+6.0V	+3.0V	40 pf CAP TO GND	OUTPUT	GND	-3.0V		25 75		$t_{d_{off}}$	5	39 50	ns	

Test Waveforms

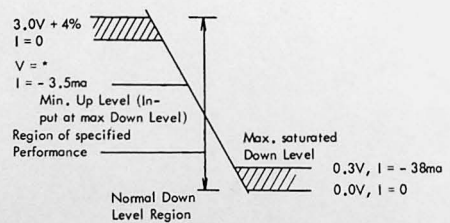


* Including Probe Capacitance

Input Requirements



Output Specifications



*Voltage as defined by collector load impedance

Fan In

Can be extended to a total of 15 inputs

Fan Out

Total available collector current = 38ma

$$38\text{ma} \geq I_{R_1} + N_1 K_1 + N_2 K_2 + \dots$$

I_{R_1} = Current through collector resistor

N_1 = Number of AI-2A loads being driven

N_2 = Number of AOI-2A loads being driven

K_1 = 2.3ma, AI - 2A loading constant

K_2 = 3.0ma, AOI - 2A loading constant

To double the Fan Out, the output collectors and inputs must be paralleled.

Maximum Power Supply Current Requirements (per module)

	<u>ON</u>	<u>OFF</u>
+6V	4.6ma	5.5ma
+3V	10.0ma	0
-3V	1.8ma	1.5ma

Maximum Power Dissipation (per module)

<u>ON</u>	<u>OFF</u>
73.0mw	38.0mw

$$\text{Average Normal Power Dissipation} = \frac{\text{NOMINAL ON} + \text{NOMINAL OFF}}{2} = 50.0\text{mw}$$

General Wiring Rules (For Printed Circuit Wire - 10 Mil Width Lines)

The input single line length should be less than 18 inches to prevent excessive reflections and noise coupling. The total net length at either input or output should be less than 60 inches unless longer delays can be tolerated.