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1.0 SCOPE

This practice outlines the procedures for preparation and Corporate release of Specifications and Circuit Flyers.

2.0 OBJECTIVES

The objectives of this practice are:

1. To make available to the entire Corporation the technical skills of all circuit designers, thereby eliminating duplication of design effort and providing the greatest number of standard circuits and circuit hardware possible.

2. To provide an input to computer programs permitting maximum design and manufacturing automation.

3.0 DEVIATIONS

3.1 Circuit design involves a wide variation in new circuits. Specific requirements to cover all variations are not possible. Questions arising that are not covered by this practice must be brought to the attention of the Corporate Circuit Flyer Group (Dept. 707, East Fishkill).

3.2 Deviation approval must be obtained from the Corporate Circuit Flyer Group (Dept. 707, East Fishkill).

4.0 TYPING REQUIREMENTS FOR FORMAL DOCUMENTATION

4.1 TYPING
Typing must be sans-serif upper case lettering that is a minimum of 0.090 inch high. (A IBM Manifold No. 12 or IBM Mid-Century No. 12 is recommended.)

4.2 RIBBON
Carbon ribbon (Ribbon No. 5122 is recommended) must be used. (A plastic backing is recommended for improved typing quality.) The typewriter impression should be set at 8 to 10.

4.3 NON-TYPED DATA
Non-typed data must be drawn with pencil. The lines must be sharp, dense, and in accordance with Corporate Drafting Standards. Line weights must be between 0.015 inch (minimum) and 0.025 inch (maximum).

4.4 FINAL MASTERS

4.4.1 The number one must not be underscored, and the zero and letter Z must not be slashed.

Examples:

1 - one	0 - zero	2 - digit 2
I - letter I	O - letter O	Z - letter Z

4.4.2 Where grid lines are used, the typing must not fall on these lines. Either erase that portion of the grid or type between the grids.

4.4.3 Changes must be neat and duplicate the original quality. Erasing must be clean.

4.4.4 A ball point pen or silk (cloth) typewriter ribbon must not be used.

4.4.5 Hand lettering must not be used, except for characters or symbols not on the typewriter.

5.0 WORK FLOW

Figure 1 shows the work flow involved to prepare and release Specifications and Circuit Flyers.

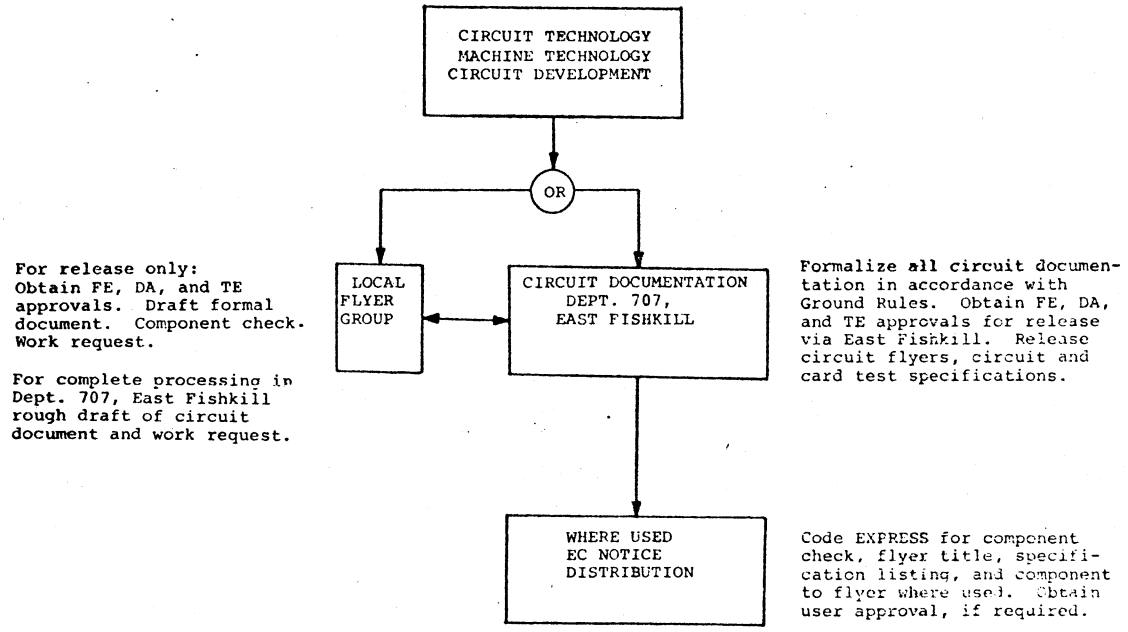


FIGURE 1 WORK FLOW

1.0 CIRCUIT SPECIFICATIONS

1.1 A Circuit Specification should consist of a full description of the performance capability of the circuit. This permits maximum utilization of the circuit. These Specifications must be released, if required, prior to release of the affected SLT cards. The Circuit Specification is used as a means of circuit selection and by Test Engineering for definition of circuit test parameters at the card level.

1.2 In cases where the Circuit Specification describes a circuit composed of more than one Circuit Flyer, the Circuit Specification should describe the entire circuit, regardless of the initial packaging intent. However, if the Circuit Flyers also have individual applications, or if the circuit will not always be packaged on the same card in the manner defined in the Circuit Specification, the individual Circuit Flyers must also have their I/O parameters defined.

2.0 CARD TEST SPECIFICATIONS

2.1 Card Test Specifications are specifications containing information pertinent to the electrical circuitry packaged on an SLT card. A Card Test Specification will be written in reference to card pins, components, and actual component locations on the card assembly. Card Test Specifications are required when the card meets one or more of the following criteria:

1. The circuitry on the card is but a portion of a larger circuit, the larger circuit being packaged on two or more cards.

2. There exists between unique circuits packaged on a card critical timing conditions, the nature of which is not covered in any of the individual circuit specifications.

2.2 Card Test Specifications are assigned a formal part number and released through the same channels as Circuit Specifications. Formal releasing, of Card Test Specifications, is a prerequisite to release of SLT cards which meet one or more of the preceding criteria. The part number must be referenced in the comment section of the SLD. (See DEP 2-6230, Suffix 1). Circuit Technology originates the Card Test Specification. Users of Card Test Specifications are:

1. Test Engineering. It provides them with necessary information concerning the circuitry on a particular SLT card thereby enabling an adequate card test program to be written.

2. Quality Engineering. It sets a standard for the referenced SLT card thereby giving Quality Engineering a basis for acceptance or rejection of the associated test program and subsequent card orders.

2.3 The format should be consistent with the Circuit Specification format; however, when "worst case" criteria would produce a specification of questionable value, cooperative effort between Circuit Technology and Test Engineering will establish the content. If Card Specifications of this type are of major proportions in a particular Circuit Technology area, a man may be sent to Test Engineering in Endicott to be educated as to the capabilities of Production Analog Circuit Test Equipment. A liaison between Circuit Technology and Test Engineering will be maintained in order to keep this man up-to-date as to advances in testing philosophy or new test capabilities.

1.0 CIRCUIT FLYER, SPECIFICATION AND ALD REFERENCING

Since Circuit Flyers and Circuit Specifications are released under separate release part numbers, appropriate cross-referencing must be made between the Card Automated Logic Diagram (ALD), the Circuit Flyer, and the Circuit Specification.

1.1 CIRCUIT FLYER TO SPECIFICATION

The Circuit Specification part number is the part number included in the Circuit Flyer as the Reference Circuit Specification Part Number. (See Section 25.) An indication must be made for the special case where no Circuit Specification is required.

1.2 SPECIFICATION TO CIRCUIT FLYER(S)

All Circuit Flyers that are covered by a given Specification will have their Block Identification numbers listed in the second section of the Specification.

1.3 ALD TO CIRCUIT SPECIFICATION

The Circuit Specification part number will be placed above the designated Circuit Flyer Logic Block Representation on the ALD. This Specification notation will be made for every different Circuit Flyer which appears on the ALD. When the Circuit Specification is not applicable, use the Circuit Flyer Part Number.

1.4 ALD TO CARD SPECIFICATIONS

The Card Test Specification part number will be referenced in the comment section of the ALD.

2.0 SPECIFICATIONS FOR COMBINED FLYERS

Combined flyers, whose function can be completely described by the basic specifications of the Unit Flyers which construct it, do not require a separate specification. However, it is conceivable that a Circuit Specification may be generated for combined flyers; that is, a combination of flyers connected such as to provide a new function. Examples might include a latch constructed from several logic functions or a single-shot fabricated from combinations of logic functions.

2.2 The Specification format should be followed to detail the collective functions provided by the assemblage of the individual circuits.

2.3 It will be the decision of the controlling Circuit Technology Group to determine which combined flyer should have its own specification.

3.0 CONTROL

Circuit Specifications will be under control of the circuit group generating the specification; this control may be transferred to another circuit group by mutual agreement of the two circuit groups concerned. (See Section 27).

4.0 CHANGE ACTIVITY

The controlling circuit group will initiate all changes. Other locations must make change requests through the controlling group. To do this, a change work request and marked brownline showing the change must be sent and approved by the Circuit Technology Group having technical control.

5.0 LISTINGS AVAILABLE

A cross reference list (for flyers to specifications) is distributed to all circuit groups. This listing is titled "Circuit Flyer, Title, and Specification Listing". It is controlled and distributed by the Corporate Flyer Group, Dept. 707, East Fishkill.

Prior to the release or pre-release of an Engineering Circuit or Card Specification, the following items must be made available by the circuit designer to the controlling Circuit Technology Group.

APPROVED MASTER DRAWINGS OF FORMAL RELEASED COMPONENTS (EXCLUSIVE OF SEMICONDUCTORS)

All circuits to be released must have approved components, or the status of non-approved components must be included.

It is necessary that the development master drawings be made available to the appropriate component approval groups so that these components may be released.

Semi-conductor devices must be released through the Components Division prior to release of the Specification.

To avoid delays the circuit designer should send an advance brownline copy of new components (exclusive of semi-conductors) to N. G. Jones, Dept. 307 Endicott.

LETTER OF WAIVER

A letter stating the intended usage of a restricted component and showing recognition of the exposure in using this component.

DESIGN EQUATIONS

The principle equations used in designing the circuit. A statement of design philosophy used and justify the deviations, if any, from standards. This should be legibly and coherently written on reproducible copy.

If the circuit will be used widely, statistical analysis may be performed on the circuit. Circuit Technology should be contacted as to the procedures to follow.

CIRCUIT PERFORMANCE DATA (STATEMENT OF LOAD CONDITIONS FOR CIRCUIT TEST AND A DESCRIPTION OF THE TEST ENVIRONMENT)

This data should be taken under conditions of temperature, humidity, voltages, loading, transistors, and other components, dictated by the design philosophy used. This should be legibly and coherently tabulated on a reproducible copy.

1.0 ENGINEERING SPECIFICATION SHEET (Figure 1)

Form No. 620-9035-0
MRO No. 780-522110

2.0 ENGINEERING SPECIFICATION GRAPH SHEET (Figure 2)

Form No. D-1675-0

3.0 HISTORY SHEET (Figure 3)

Form No. M30-2053-0

4.0 INSTRUCTIONS

1. When ordering, specify either linen or vellum.
2. Forms may be obtained from Circuit Documentation and Control, Dept. 707, East Fishkill.
3. All forms for processing must be reproducible copies.

ENGINEERING SPECIFICATION SHEET

IBM ENGINEERING SPECIFICATION	PART NO.
	CONTROL CODE
TITLE	PAGE NO.

PART NO.

MADE BY	ORIG. APP.	TECH. APP.	EC. LEVEL

FORM NO. 820-8035-0 MRO NO. 780522110

DRAFTING MEDIA GRAPHIC CONTROLS CORPORATION Buffalo, New York Printed in U.S.A. STOCK NO. N850T ANCDEF

FIGURE 1

ENGINEERING SPECIFICATION GRAPH SHEET

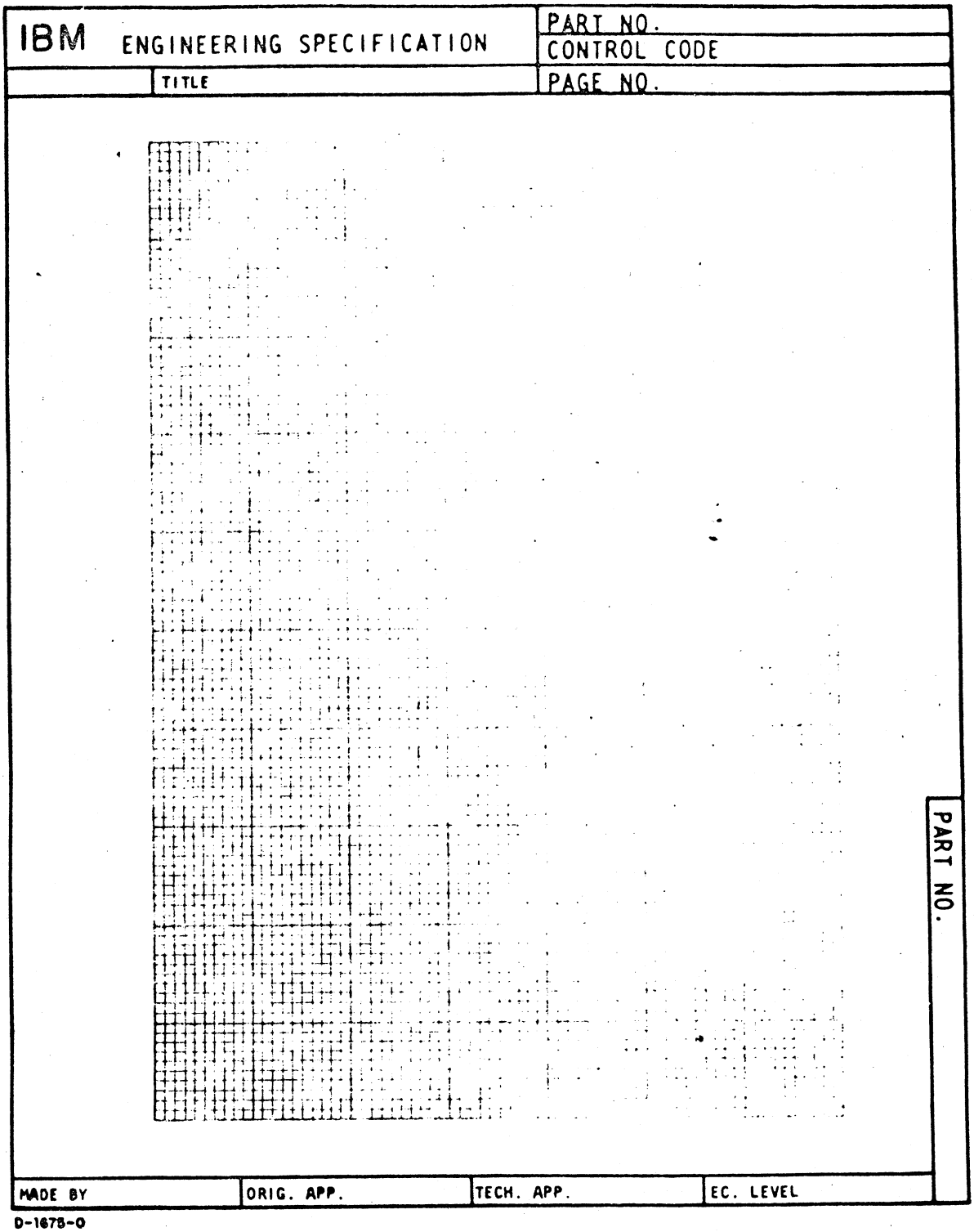


FIGURE 2

HISTORY SHEET

IBM **ENGINEERING HISTORY**

	PART NO.
	CONTROL CODE
TITLE	PAGE NO.

PAGE	DATE	EC. NO.	DESCRIPTION	APPR.

PART NO.

MADE BY	ORIG. APP.	TECH. APP.	EC. LEVEL

M30-2063-0

FIGURE 3

1.0 FAMILY

Enter in the box to the left of the "title" box one of the following:

SRETL - 5 - 12
SRETL - 30
SRETL - 700
SRETL - General
Analog

2.0 TITLE

This is an informative brief description of the circuit and should be closely allied with the circuit function.

3.0 PART NUMBER

1. Each Specification will have its own unique part number.

2. Blocks of part numbers are pre-assigned by Dept. 707, East Fishkill.

4.0 PAGE NUMBER

1. Pages will be numbered in ascending order starting at sheet 1 and finishing with the History Sheet.

2. Reference will be made to the total number of pages. Example: 1 of 35, 2 of 35, 3 of 35, . . . 35 of 35.

5.0 E.C.LEVEL

E.C. level should be indicated on the History Sheet and carried on each page of the specification.

6.0 CONTROLLED RELEASE

1. The change level for controlled release Specifications will be of the form nnnn (n-numeric).

2. Blocks of controlled numbers are obtained from Dept. 707 East Fishkill.

7.0 FORMAL RELEASE

A six digit numeric change level will be assigned at the time a Specification is to be formally released.

Blocks of formal release numbers are obtained from Dept. 707, East Fishkill.

8.0 APPROVAL SIGNATURES

1. Made By - Designer's signature.

2. Originator Approval - Designer's manager.

3. Technical Approval - Circuit Technology Manager or equivalent.

9.0 HISTORY SHEET

9.1 INITIAL RELEASE

Show the page numbers being released, date of release, the release E.C. number, statement of release under description, and engineering change approval (initials).

9.2 CHANGES

1. All pages that are affected must be listed.

2. The date, E.C. number, a brief description, and change approval must also be completed.

3. New history sheets are to be added to the specification when previous ones are filled. The E.C. level of the history sheets will be the last level listed.

1.0 INTRODUCTION

The circuit designer is responsible for writing an engineering specification that defines the performance required of the circuit in the system.

Nearly all IBM circuits are one of two types, switching circuits or non-switching (analog). The Engineering Specification format for each of these is described in paragraphs 2.0 and 3.0.

2.0 CONTENTS OF SWITCHING CIRCUITS

Engineering Specification Section numbers and contents are:

Section 1.0 Functional Description of the circuit in the system and a description of circuit operation. Include function of each component and system requirement. Component part numbers are not required.

Section 2.0 Schematic Diagram and Reference Circuit Flyer Block Identification Numbers.

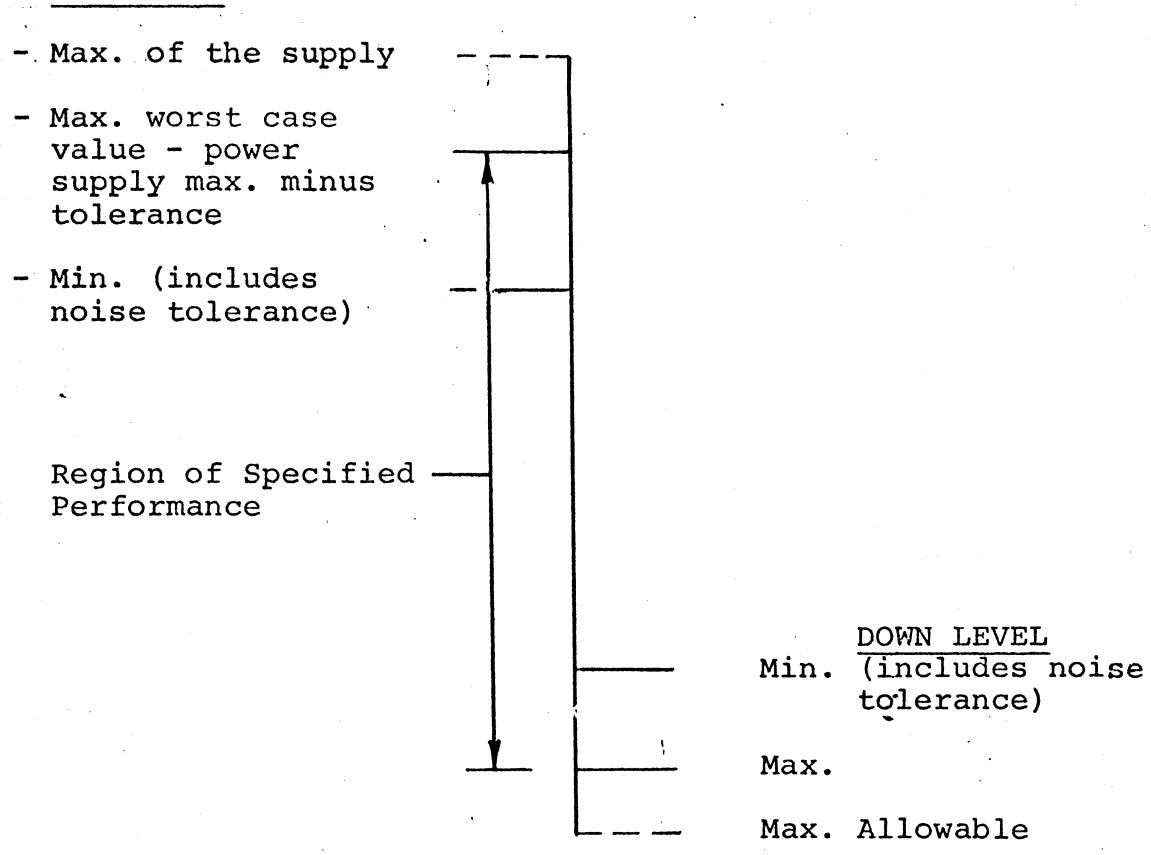
2.1 Referenced Circuit Flyer Block Identification and Part Number.

2.2 Block diagram of Circuit Flyer Connections if applicable.

2.3 Schematic diagram of circuit. When describing more than one Circuit Flyer, indicate boundaries of each flyer and associated Block Identification.

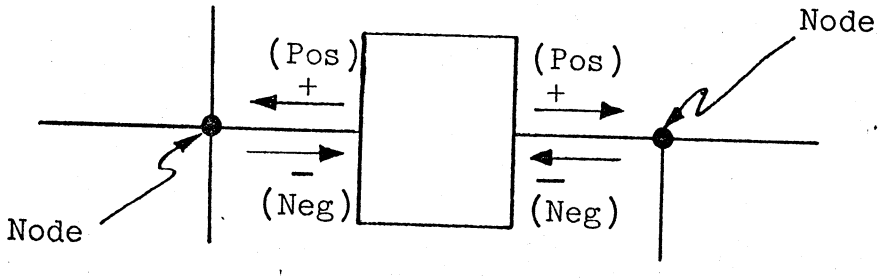
Section 3.0 Input Requirements

3.1 Voltage and Current Levels



3.2 Current Requirements (conventional current) - The IRE Standard is followed. It states that current flowing into a node is positive and away from a node is negative. Thus into a circuit is negative, out of a circuit is positive. Appropriate currents should also be indicated on the voltage curve (Section 3.1) along with associated voltages.

Example:



Current is to be shown in the form of an equation where each current component forms a term as shown below:

$$I_T = I_1 + I_2 + I_3 + I_4 - - - I_n$$

I_1 = Steady State DC current

I_2 = Displacement current $\left(C \frac{dv}{dt}\right)$

I_3 = Diode recovery current

I_4 = Overdrive current

$I_5 = I_n$ = Other appropriate consideration

Any current components considered not applicable should be so stated.

3.3 Equivalent Circuit Schematic - presented to drive (toleranced to give maximum loading on driving source).

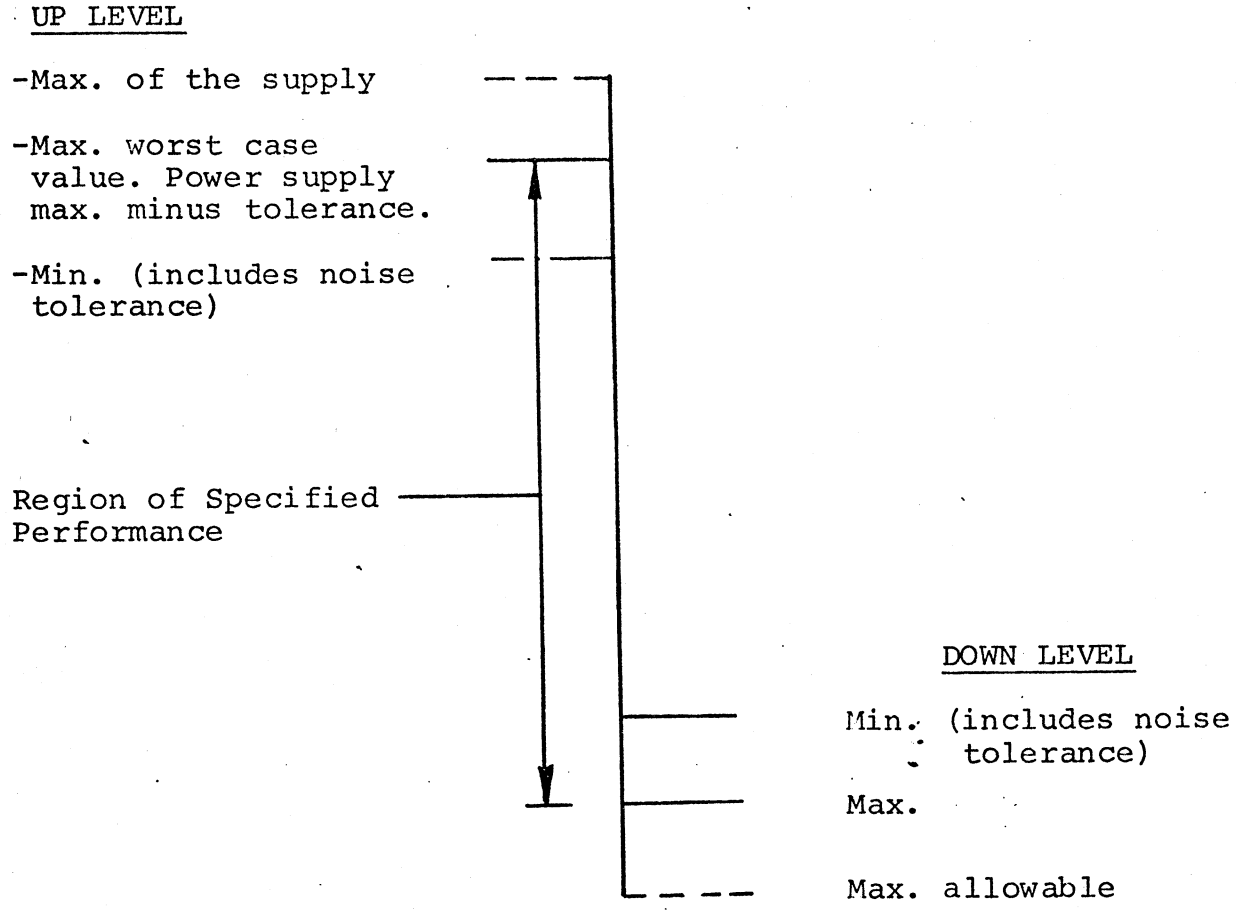
3.4 Pulse Width - Any limitations on input pulse such as maximum repetition rate, minimum pulse width, gate conditioning times, etc. (specify how measured, e.g., 10% to 10% etc.).

3.5 Input Slope Requirements In Transition Region - Specify voltage swing and how measured; e.g., 10% to 90%, etc.

3.6 Other limitations - Where applicable specify noise sensitivity (specify amplitude, pulse width, and slope of the input with respect to a reference level to cause a defined disturbance pulse in the output).

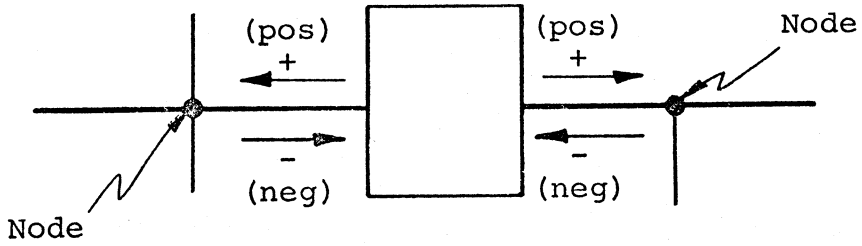
Section 4,0 Output Specifications

4.1 Voltage and Current Levels



4.2 Current Requirements (conventional current) - The IRE Standard is followed. It states that current flowing into a node is positive and away from a node is negative. Thus into a circuit is negative, out of a circuit is positive. The appropriate currents should also be indicated on the voltage curve (Section 4.1) along with associated voltages.

Example:



Current is to be shown in the form of an equation where each current component forms a term as shown below:

$I_T = I_1 + I_2 = I_3 - - - I_n$ where

I_1 = Steady State DC current

I_2 = Displacement current ($C \frac{dv}{dt}$)

$I_3 = I_n$ = Other applicable terms

4.3 Pulse width - Any limitations on output pulse such as maximum repetition rate, minimum pulse widths, etc., (specify how measured; e.g., 10% to 10%, etc.).

4.4 Output slope requirements in transition region - Specify voltage and/or current swing, and how measured, e.g., 10% to 90%, etc.

4.5 Other limitations

Section 5.0 Overall Performance

5.1 Phase shift - - Maximum, nominal and minimum.

5.2 Transient behavior - - How measured and under what conditions, such as:

5.2.1 Turn on - - Maximum, nominal, and minimum.

5.2.2 Turn off - - Maximum, nominal, and minimum.

5.2.3 Recovery time

5.3 Other

Section 6.0 Power Requirements

6.1 Power supply voltage - Tolerance at the circuit.

6.2 Power supply current requirements. Specify direction of current flow (e.g., + current taken from a power supply and - current into a power supply.). To calculate nominal current requirements, all circuit parameters are at their nominal value, and the input and output signals at their nominal value. If a nominal signal level is not specified, a mid-value between the minimum and maximum value may be taken.

6.2.1 Off condition - - maximum, nominal, and minimum currents per circuit.

6.2.2 On condition - - maximum, nominal, and minimum currents per circuit.

6.3 Component And Transistor Power Dissipation - Maximum on, Maximum off, and average transient power under worst case conditions. Specify rise and fall times.

6.4 Duty Cycle - of circuit.

6.5 Circuit Air Requirements - If dissipation is dependent on a minimum air flow: velocity, temperature and dynamic pressure.

6.6 Over-Voltage and Under-Voltage Limit - To prevent component damage (magnitude and time).

6.7 Supply Sequencing - If required, explain why.

Section 7.0 Marginal Check Specifications

7.1 Marginal Check Voltage Limits - Of the circuit are a 3 volt decrease toward ground with no catastrophic failures.

7.2 Other Applicable A.C. and D.C. information.

Section 8.0 Application Notes

3.0 CONTENTS OF NON-SWITCHING CIRCUITS (ANALOG)

Section 1.0 Functional Description - Of the circuit in the system and a description of the circuit operation.

Section 2.0 Circuit Diagram and reference circuit flyer block identification numbers.

2.1 Referenced Circuit Flyer Block Identification and Part Numbers.

2.2 Block diagram of Circuit Flyer connections, if applicable.

2.3 Schematic diagram of circuit. When describing more than one Circuit Flyer, indicate boundaries of each flyer and associated Block Identification.

Section 3.0 Input Signal Requirements

3.1 DC Voltage and Current Components - Maximum, nominal, minimum.

3.2 AC Signal Levels - maximum, nominal, minimum

3.3 Input Impedance - maximum, nominal, minimum

3.4 Signal To Noise Ratio - at input

Section 4.0 Output Specifications

4.1 DC Voltage and Current Component - maximum, nominal, minimum

4.2 AC Signal Levels - maximum, nominal, minimum

4.3 Output Impedance - maximum, nominal, minimum

4.4 Special Load Requirements - on output

4.5 Signal To Noise Ratio - on output

Section 5.0 Over-all Performance

5.1 Gain (current, voltage, power) - maximum, nominal, minimum at mid-band and other pertinent frequencies.

5.2 Bandwidth - maximum, nominal, minimum

5.3 Phase shift specifications corresponding to bandwidth conditions.

5.4 Transient behavior (describe how measured and under what conditions.

5.4.1 Turn-on - maximum, nominal, minimum

5.4.2 Turn-off - maximum, nominal, minimum

5.4.3 Recovery time

5.5 Stability - AC, DC, and temperature

5.6 Other

Section 6.0 Power Requirements

6.1 Power Supply Voltage - tolerance and back panel distribution and reference.

6.2 Power Supply Current Requirements - maximum, nominal, minimum.

6.3 Circuit Air Requirements - Velocity, temperature and dynamic pressure.

6.4 Over-Voltage and Under-Voltage Limits - (magnitude and time.)

6.5. Power Sequencing - if required and justification.

6.6 Component And Transistor Power Dissipation - maximum average, and minimum.

Section 7,0 Marginal Check Specifications

7.1 Marginal Check Voltage Limits - of the circuit are a 3 volt decrease toward ground with no catastrophic failures.

7.2 Marginal limits - of associated circuit family.

7.3 Dynamic Response - under marginal checking.

Section 8.0 Application Notes

8.1 How used

8.2 How tested

8.3 Special restrictions

1.0 INTRODUCTION

1.1 Circuit flyers are important communication documents providing a unique representation of circuits.

1.2 Each flyer is usually a collection of electronic components or elements connected in such a way as to perform a desired function.

1.3 The basic circuit flyer information consists of a standard symbol schematic of the circuit, a logic block representation, and complete load check data.

2.0 RULES

2.1 The representation of single components by unique circuit flyer block ID's should be avoided. All effort must be made to include these components in the basic associated circuit flyers. If this is not possible due to card packaging requirements, the single component flyer can be used. Load check data and reference specifications will be required for these circuits.

2.2 If a circuit flyer does not contain the information just stated in accordance with the ground rules set forth in this instruction, it will not be acceptable; and approval of the flyer cannot be given.

2.3 Furthermore, if a circuit flyer is used on a card in any manner resulting in a deviation in the flyer's schematic, logic representation, or load check data, it will be considered a misuse of the flyer; and the card will be placed on hold until the misuse is corrected.

1.0 INTRODUCTION

Circuit flyers are used to provide information in a standard form to the users specified in paragraphs 2.0 through 6.0.

2.0 CIRCUIT TECHNOLOGY

1. Standardization of circuits.
2. Reference document for determining card changes.

3.0 AS REFERENCE FOR SERVICEABILITY

1. Source document for part of the information supplied to Field Engineers.
2. Circuit logic function.
3. Voltage and delay listings.

4.0 DESIGN AUTOMATION

1. Basic requirement for full implementation of Circuit Card Design Automation (CCDA) and Solid Logic Design Automation (SLDA). See Suffix 1 and 4 of Card Ground Rules.
2. Logic block symbology used on systems ALD
3. Logic block symbology used on card ALD
4. Logic Test Data generation.
5. Logic function and delay parameters for logic simulation.
6. Electrical data for load check programs.
7. Hardware connections and options for automated packaging programs.

5.0 CARD LAYOUT

1. See Suffix 1 of Card Ground Rules.
2. Communications link between card logic diagram and card schematic.
3. Basic input to CCDA programs.
4. "B" factor for calculating amount of decoupling need on card.

6.0 TEST ENGINEERING

1. Test Engineering uses the circuit flyer as a primary source document.

2. It is required as input information to a set of computer programs designed to automatically generate test and analysis data for the SLT card.

3. The data is used in combination with a computer controlled SLT Card Final Tests System (SCFTS) for automated card testing and the locating of faulty components on a card.

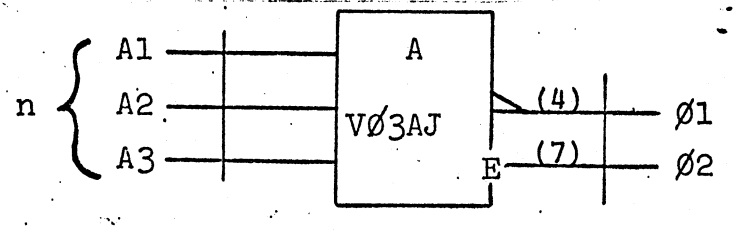
4. The test data is also distributed throughout the Corporation for card testing at other Plants. See Suffix 10 of Card Ground Rules.

1.0 UNIT FLYER

An electrical configuration of circuit elements which must always:

1. Perform the same unique function.
2. Exhibit definite input and output characteristics.
3. Be retained in its original logic block form if it has the capability of being used in more than one application.
4. Be an electrically connected unit without segmented elements.
5. Be represented as a single block in its logic block representation.

Example of a Unit Flyer for an And Invert:



n = 1 to 10 inputs
(See specified delays when n = 10)

FIGURE 1

NOTE: Decoupling capacitors which are used to decouple non-standard voltages or decoupling capacitors which are, at all times, required with a given circuit, must be defined alone as a unit circuit flyer and not included with the circuit.

2.0 COMBINED FLYER

1. A combination of unit flyers connected in a manner to provide a new unit circuit. (Not to be confused with grouping flyer.) The load check data is not required for combined flyers.
2. The logic block representation of a combined flyer is a single block.

3. Reference to the unit flyers which construct a combined flyer is indicated by showing the interconnection of the unit flyer's logic blocks on the schematic grid sheet.

4. The comb[illegible] schematic is optional.

Example of a combined flyer for a loaded And Invert:

Unit Flyer Combination:

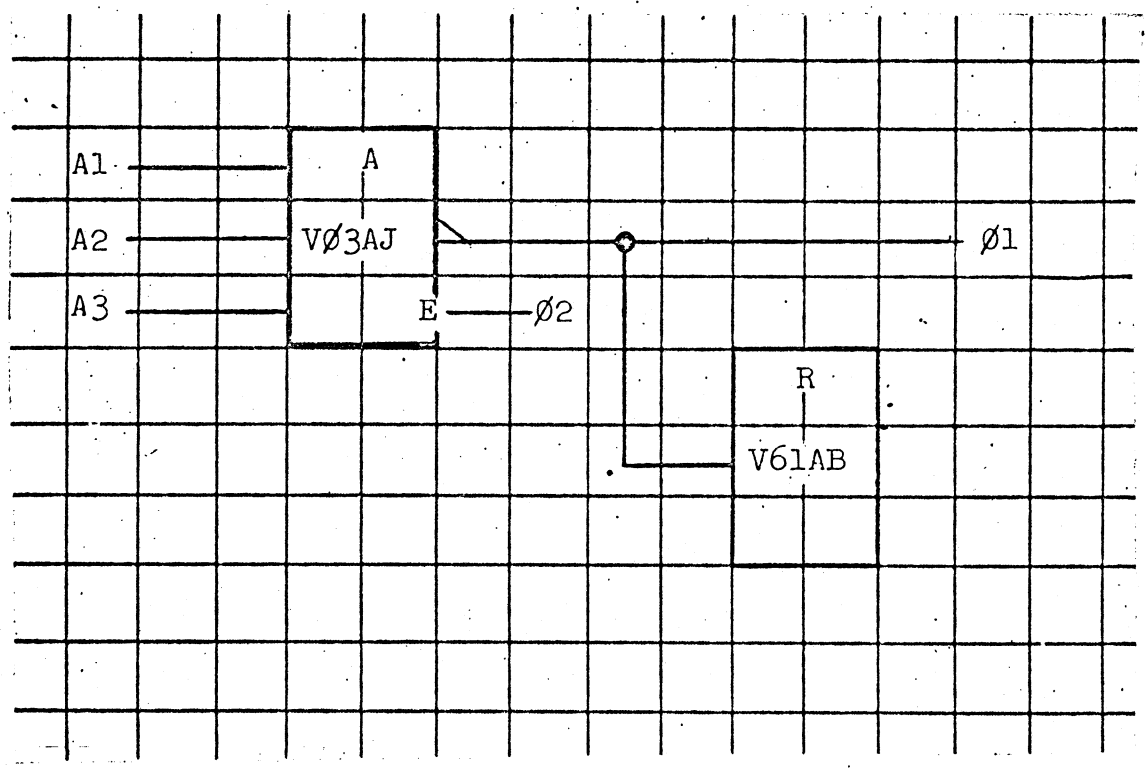
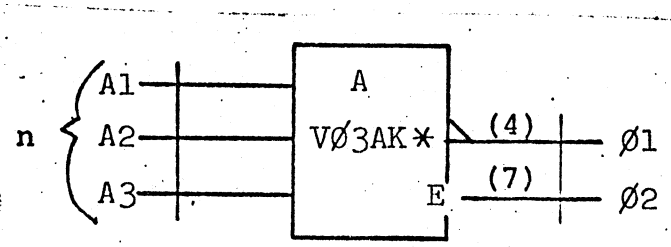


FIGURE 2

Combined Flyer Logic Block Representation:



n = 1 - 10 inputs

* (asterisk) following Block ID Code indicates a combined flyer when shown at card level.

FIGURE 3

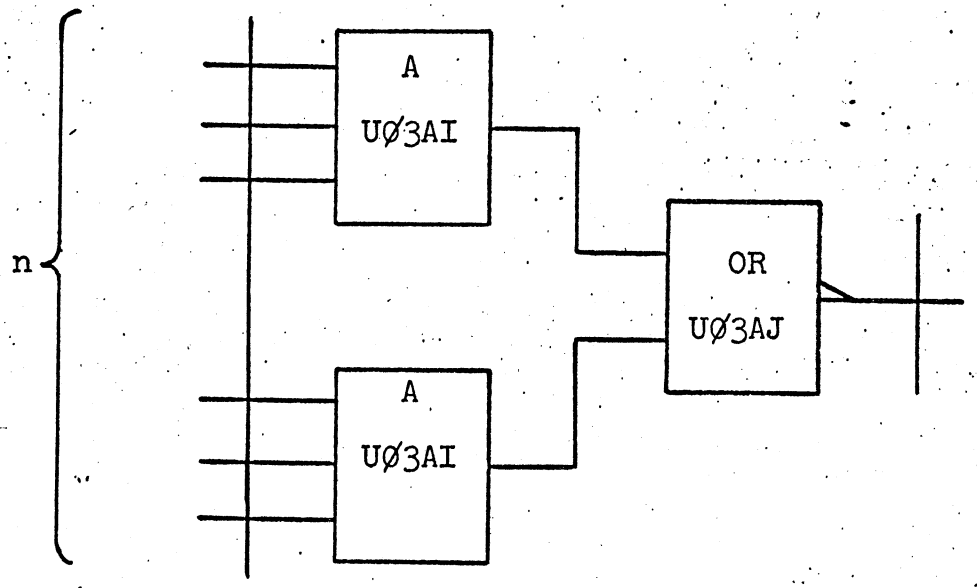
3.0 GROUPING FLYER

1. A flyer for Design Automation use only. One that consists of circuits represented on System Pages in more than one logic block, but which, without exception are always found on the same card.

2. Only two levels of logic are allowed. The grouping flyers logic block configuration will be found on the card logic page (ALD) but no reference will be made to the grouping flyer block identification. The block identifications of the individual unit flyers must be maintained on the ALD.

3. Circuits used on a grouping flyer may never be used alone or in other combinations other than in other grouping flyer combinations.

Example:



n = 1 to 6 (blocks)

FIGURE 4

4. The "OR" block is referred to as the object block of the group. The object block must have symmetrical inputs. Maximum number of inputs is 6.

5. The blocks feeding the object block must be the same identification number. The grouping circuit flyer will state "Design Automation use only, not for Logic Design or ALD usage."

6. The load checking data is not required for a grouping circuit flyer.

4.0 INTEGRATED FLYER

1. An integrated circuit flyer is the representation of a circuit by a collection of 2 or more logic functions, under one title, which has at least one single circuit element related to more than one unit logic function or is such that inputs or outputs can not be defined for unit level block symbology.

2. Its existence can only be justified when the circuit under consideration cannot be represented by any practical combination of unique circuit flyers each having a defined standard logic function and direct correlation to the hardware components contained in the overall schematic.

3. The integrated circuit is an entity and cannot be broken down in any form.

4. A unique circuit flyer for any of the logic block functions contained in the integrated flyer's logic block representation must not exist. Sequential block identification numbers will be assigned to each block of the logic block representation; however, only one circuit flyer schematic will be drawn.

5. An integrated flyer must be completely packaged on only one SLT card.

6. Design Automation and Test Engineering programs cannot automatically process integrated flyers; therefore, usage should be restricted.

Example of an integrated flyer:

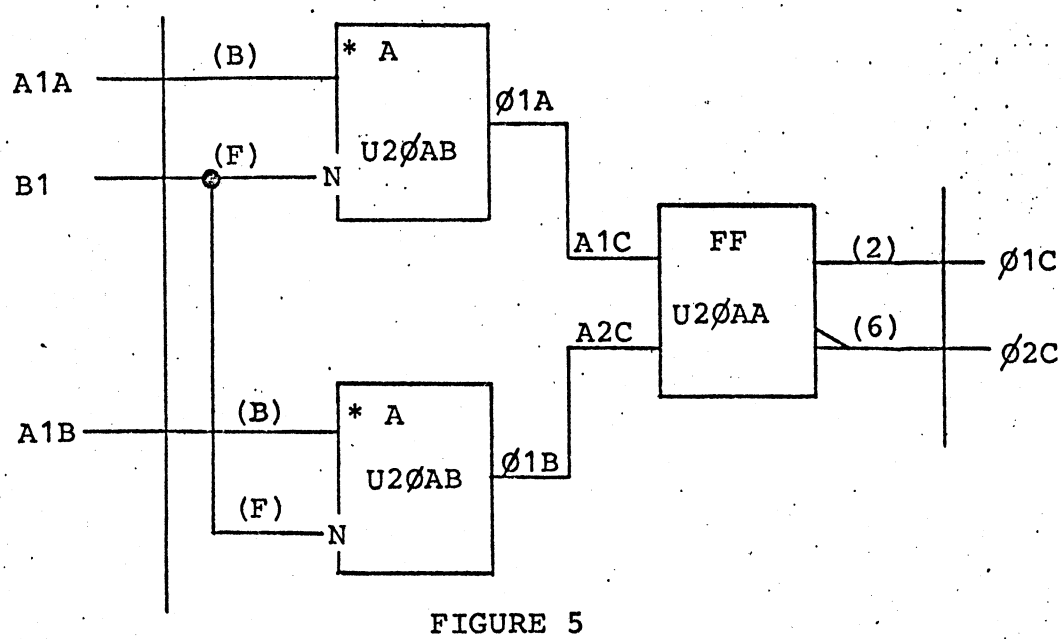


FIGURE 5

1.0 SINGLE PAGE SCHEMATIC SHEET (Figure 1)

Form Number:

M-30-1872-1

2.0 EXTENDED SCHEMATIC SHEET (Figure 2)

Form Number:

M-30-1873-1

3.0 LOAD CHECK SHEET (Figure 3)

Form Number:

D-1874-0

4.0 EXPANDED LOAD CHECK SHEET (Figure 4)

Form Number:

D-1534-1

5.0 HISTORY SHEET (Figure 5)

Form Number:

M-30-2053-0

6.0 INSTRUCTIONS

1. When ordering forms, specify either linen or vellum.
2. Forms can be obtained from Dept. 707, East Fishkill.
3. All forms for processing must be reproducible copies.

CIRCUIT FLYER FORMS

SINGLE PAGE SCHEMATIC SHEET

3-4-_____-_

IBM CIRCUIT FLYER -A

	PART NO.
	BLOCK ID.
TITLE	PAGE NO.

BLOCK CLASS _____ CONTROL CODE _____
*BLOCK STATUS _____ GROUPING _____
PACKAGING _____

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
A																			
B																			
C																			
D																			
E																			
F																			
G																			
H																			
J																			
K																			
L																			
M																			

PART NO.

DESIGN AUTOMATION BLOCK REPRESENTATION

REF. CKT. SPEC. P/N		E.C.	DATE	E.C.	DATE
MADE BY	ORIG. APP.				
TECH. APP.	R&S APP.				
D.A. APP.	T.E. APP.				

FIGURE 1.

EXTENDED PAGE SCHEMATIC SHEET

3-4-_ _ _ _-_

IBM CIRCUIT FLYER-B

	PART NO.
	BLOCK ID.
TITLE	PAGE NO.

BLOCK CLASS _____ CONTROL CODE _____

BLOCK STATUS _____ GROUPING _____

PACKAGING _____

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
A																			
B																			
C																			
D																			
E																			
F																			
G																			
H																			
J																			
K																			
L																			
M																			
N																			
P																			
Q																			
R																			
S																			

PART NO.

REF. CKT. SPEC. P/N.	E.C.	DATE

FIGURE 2

CIRCUIT FLYER FORMS

LOAD CHECK SHEET

3-4-_____-_

IBM CIRC... C

PART NO.	
BLOCK ID.	
TITLE	PAGE NO
	CONTROL CODE

LOGIC FUN / CKT NO.	LOGIC FUNCTIONS																		DOT FUNCTIONS		
	NAND	NOR	AND	OR	INV	RES	NONI	OTHER	EXTEND	EVENE	ODDE	EVENO	ODDO	OE	TH	THI	ORC	INVC	AND	OR	NONE

DELAY LIMITS

	DELAY USED BY SLDA	8" NET BC	8" NET WC	48" NET BC	48" NET WC
OUTPUT RISING					
OUTPUT FALLING					

"B" FACTOR _____

DELAY PARAMETERS ☐ DOES NOT APPLY

A REALISTIC ESTIMATE OF MACHINE CIRCUIT SPEEDS SHOULD BE OBTAINED FROM THE LOCAL MACHINE TECHNOLOGY GROUP

LOAD CHECKING DATA ☐ (DA USE ONLY) DOES NOT APPLY

SPI		CPL	CT	MAXIMUM VOLTAGE (VOLTS)	MINIMUM VOLTAGE (VOLTS)	AVAILABLE SOURCE CURRENT (MA)	MINIMUM SOURCE CURRENT (MA)	MAXIMUM LOAD CURRENT (MA)	MINIMUM LOAD CURRENT (MA)	DOT COUNT
	UP LEVEL									
	DOWN LEVEL									
	UP LEVEL									
	DOWN LEVEL									
	UP LEVEL									
	DOWN LEVEL									
	UP LEVEL									
	DOWN LEVEL									
	UP LEVEL									
	DOWN LEVEL									

PART NO.

SPECIAL DRIVING RULES: _____

REF. CKT. SPEC. P/N	E.C.	DATE

D- 1874-0

FIGURE 3

EXPANDED LOAD CHECK SHEET

3-4-_ _ _ _ - _

IBM CIRCUIT FLYER-C

PART NO.	
BLOCK ID.	
TITLE	
PAGE NO.	
CONTROL CODE	

	LOGIC FUNCTIONS																		DOT FUNCTIONS		
LOGIC FUN. / CKT NO.	NAND	NOR	AND	OR	INV	RES	NONI	OTHER	EXTEND	EVENE	ODDE	EVENO	ODDO	OE	TH	THI	ORC	INVC	AND	OR	NONE

	DELAY USED BY SLDA	DELAY LIMITS 8" NET BC	8" NET WC	48" NET BC	48" NET WC
OUTPUT RISING					
OUTPUT FALLING					

"B" FACTOR _____

DELAY PARAMETERS ☐ DOES NOT APPLY

A REALISTIC ESTIMATE OF MACHINE CIRCUIT SPEEDS SHOULD BE OBTAINED FROM THE LOCAL MACHINE TECHNOLOGY GROUP.

LOAD CHECKING DATA ☐ (DA USE ONLY) DOES NOT APPLY

SPECIAL DRIVING RULES: _____

PART NO.

REF. CKT. SPEC. P/N	E.C.	DATE

D-1334-1

FIGURE 4

HISTORY SHEET

IBM **ENGINEERING HISTORY**

PART NO.

CONTROL CODE

TITLE

PAGE NO.

PAGE	DATE	EC. NO.	DESCRIPTION	APPR.

PART NO.

MADE BY	ORIG. APP.	TECH. APP.	EC. LEVEL

M30-2053-0

FIGURE 5

1.0 BLOCK CLASS

The block class falls into one of the following categories:

1. Standard Circuit - Any technically approved circuit which is intended for use in more than one product type and/or possesses significant potential for multi-product usage.

2. Special Circuit - Any technically approved circuit which has usage in one product only and is not intended for multi-product use.

3. Experimental and/or Controlled - Any circuit which has not been completely reviewed and/or approved for Field shipment.

2.0 BLOCK STATUS

The block status falls into one of the following categories:

1. Active (Standard or Special) - Any circuit whose usage is encouraged.

2. Restricted (Standard or Special) - Any technically approved circuit whose usage is not encouraged due to one of the following reasons:

   (a) Restricted components.
   (b) Components with low availability.
   (c) Special component geometry causing manual assembly or other special mounting procedures.
   (d) Special component geometry causing special placement of a card (using the circuit flyer) in a machine not covered by the SLT Card Ground Rules.
   (e) Other characteristics with which indicate the circuits usage should be restricted.

3. Obsolete - Any circuit through engineering review that has been found to have no application in present or future products. Engineering documents are maintained at the obsolete level.

   An asterisk in Block Status is carried on all unreleased Circuit Flyers to fulfill an automation requirement for data in this field.

3.0 GROUPING

Prior to partitioning, certain circuit configurations must be associated together (See Grouping Flyer). The space labeled "Grouping" on a basic flyer must contain the block identification numbers of grouping flyers on which the basic flyer is used; otherwise, the work "none" will be written. This space on a grouping flyer will be left blank.

CONTROL CODES

AD	Mohansic
BR	Burlington, Vermont
BM	Burlington Memory
CO	Boulder, Colorado
CM	Boulder Memory
EC	Endicott Components Division
ED	Endicott Circuit Technology (SDD)
EM	Endicott Memory*
EP	Endicott Product Engineering (SDD)
EQ	Endicott Test Equipment
ES	Endicott Special Card Engineering
FD	France-Paris Military
FR	France - La Gaude
GL	German Lab - Boeblingen
HO	Uithoorn, Netherlands (Holland)
HV	Huntsville, Alabama
KM	Kingston Memory
KN	Kingston Circuit Technology
LX	Lexington*
MD	Gaithersburg, Maryland (FSD)
NL	Sweden (Nordic Lab)
OW	Owego, New York
PC	Components Division (E. Fishkill)
PD	Poughkeepsie Circuit Technology
PM	Poughkeepsie Memory
PP	Poughkeepsie C. E. Equipment
RA	Raleigh, North Carolina
RO	Rochester, Minnesota
SD	San Jose, California
SM	San Jose Memory*
TA	Austin, Texas
UK	United Kingdom (England)
ZD	Boca Raton
DD	Princeton, New Jersey

* Indicates shown for reference only. These codes are no longer being used.

4.0 BLOCK TITLE

This is an informative brief description of the circuit. The name should be closely related to the circuit function code. All flyers containing SLD Module Packaging should indicate SLD proceeding the title.

5.0 PART NUMBER

Each circuit flyer will have its own unique part number.

6.0 REFERENCE CIRCUIT SPECIFICATION PART NUMBER

6.1 Reference circuit specification part numbers must be specified for controlled and formal release circuit flyers. This part number will cross reference the flyer to the circuit specification and is the part number of the circuit specification.

6.2 Controlled and formal release circuit flyers must have a complete circuit specification released prior to the release of the affected SLT card(s).

6.3 With the exception of combined flyers, all circuit flyers pertaining to the same circuit design will have the same Reference Circuit Specification part number. Combined flyers will reference the unit flyers which it consists of, and in turn, the unit flyers will reference the circuit specification.

6.4 An exception to this may arise when a combined flyer provides a new function. Examples might include a latch constructed from several logic functions or a single-shot fabricated from combinations of logic functions.

7.0 BLOCK IDENTIFICATION NUMBER

7.1 The Block ID Number is five characters of the form "ANNAA" (A=alphabetic, N=numeric). The coding scheme follows the Data Classification System (DCS) Corporate Standard. The first character is alphabetic and designates circuit family.

Family	First Character	DCS Code
ANALOG	O	2600
SLD-100	R	2900
SRETL-General	S	4000
SRETL-30	T	4100
SRETL-5-12	U	4200
SRETL-700	V	4300
MONOLITHIC	W	4100

7.2 The second and third characters are numeric and designate the general type of circuit:

03 - Logic Circuits and Extenders
05 - Voltage Translate and Converter Circuits
06 - Transmission Line Drivers and Receivers
07 - Sense Amplifiers
10 - Inverting Drivers less than 50 ma
11 - Non-invert Driver less than 50 ma
15 - Power Driver more than 50 ma
16 - Magnetic Head and Core Driver
20 - Triggers, Flip Flops, Polarity Holds, Schmidt Trigger
21 - Single-Shots
22 - Oscillators
25 - Regulators, Clamps Clippers, and Limiters
29 - Analog Circuits - Reference Power Supplies
32 - Gates
40 - Special Circuits
45 - Delay Circuits
55 - Indicator Circuits
60 - Integrators and Filters
61, 62 - Components
63 - Reed Relays
65 - Functional Card
66 - Field Replacement Card

NOTE: For analog circuits, note the the distinction between 05, 62, and 63 in DCS 0-0106 under 2600 category.

7.3 The fourth and fifth characters are alphabetic and provide an individual identification within the general type of circuit. The fifth character is also used to identify sub-circuits in the case of integrated flyers.

7.4 A circuit with variable number of inputs will retain the same block ID number providing these inputs are symmetrical.

8.0 PAGE NUMBER

Pages are numbered in ascending order starting at 1. Reference will be made to the total number of pages.

Example: 1 of 3; 2 of 3; 3 of 3

9.0 DATA CLASSIFICATION SYSTEM (DCS) CODE

The description of the DCS coding system appears in the IBM Corporate Standards, Section 0-0-0106.

10.0 ENGINEERING CHANGE AND DATE

10.1 EXPERIMENTAL

The change level for Experimental flyers consists of the date of initiation followed by an alphabetic character. The date and alphabetic character is updated each time a given flyer undergoes a change.

Example: 1/12/65A is the initial level.
1/16/65B is the first change to the flyer after its origin.

10.2 CONTROLLED

The change levels for Controlled release circuit flyers will be of the form NNNNNN (N - numeric). The release or change date will accompany each engineering change number. Blocks of numbers are obtained from the Corporate Circuit Flyer Group, Dept. 707, East Fishkill.

10.3 FORMAL

A six digit numeric change level will be assigned at the time the flyer is to be formally released. Blocks of formal release numbers are obtained from the Corporate Circuit Flyer Group, Dept. 707, East Fishkill. The release or change date will accompany each release number.

11.0 APPROVAL SIGNATURES

All approvals are mandatory for the circuit flyer to be a valid document and must be completed before the circuit flyer is released by the Corporate Circuit Flyer Control Group in East Fishkill. The only exception to this is when the facilities are not available locally; in which case, the Corporate Circuit Flyer Group will furnish the facilities.

1. Made By - Designer's Signature.
2. Originator Approval - Design Manager's approval.
3. Technical Approval - Responsible manager in Circuit Technology.
4. Design Automation Approval - Approval by the local Design Automation Group indicates that the circuit flyer format is compatible with the SLDA and CCDA programs and/or that the flyer has been put on the Circuit Master Tape (CMT) and is available for use in SLDA and CCDA programs.
5. Test Engineering Approval - Made by the local Test Engineering representative. Approval indicates that the flyer is compatible with Test Engineering's requirements.

6. Field Engineering Approval - Approval by Field Engineering Representative indicates appropriate Logic Symbology has been assigned, and Circuit Flyer does not violate Corporate Logic Standards.

12.0 CIRCUIT FAMILY

12.1 Filled in the reserved space to the left of the "Title" box. The circuit family types are:

SLD - 100
SLD - 30
SLD - 700
SRETL - 5 - 12
SRETL - 30
SRETL - 700
SRETL - General
Monolithic
Analog

12.2 The circuit family SRETL (Screened Resistor Epitaxial Transistor Logic) will function with more than one circuit family or for circuits that cannot be purely classified in the existing specific families.

13.0 PACKAGING

13.1 This section is reserved for the SLT and R/C module part numbers relative to the "M" number identification given to them in the schematic section and module part numbers used for extending and alternate packaging.

13.2 Alternate Packaging will be allowed provided the following conditions are adhered to:

1. Components of the same nominal value but having more rigid tolerances can be used as alternates provided no circuit performance degradation occurs (i.e., a 1% Resistor can be used as an alternate for a 5% Resistor).

2. Components may be used as alternates when the nominal value is different, but yet falls within the tolerance of the original design values. The tolerance of the alternate in this case must keep the component within the original design parameters.

3. For alternate packaging of components with different tolerances (modular or discrete) the maximum tolerance range must be shown on the schematic.

4. Exact replacements can always be used as alternates.

13.3 There must not be packaging options between signular components and multiple component equivalents. That is to say, multiple component equivalents must not be used on an SLT card to implement components shown as singular components on the circuit flyer schematic. The only exception to this rule is when the equivalent can be obtained by using only one module, and only if external connections to the module are not required in obtaining the equivalent (that is, the equivalent circuit can be obtained by connecting to two pins only).

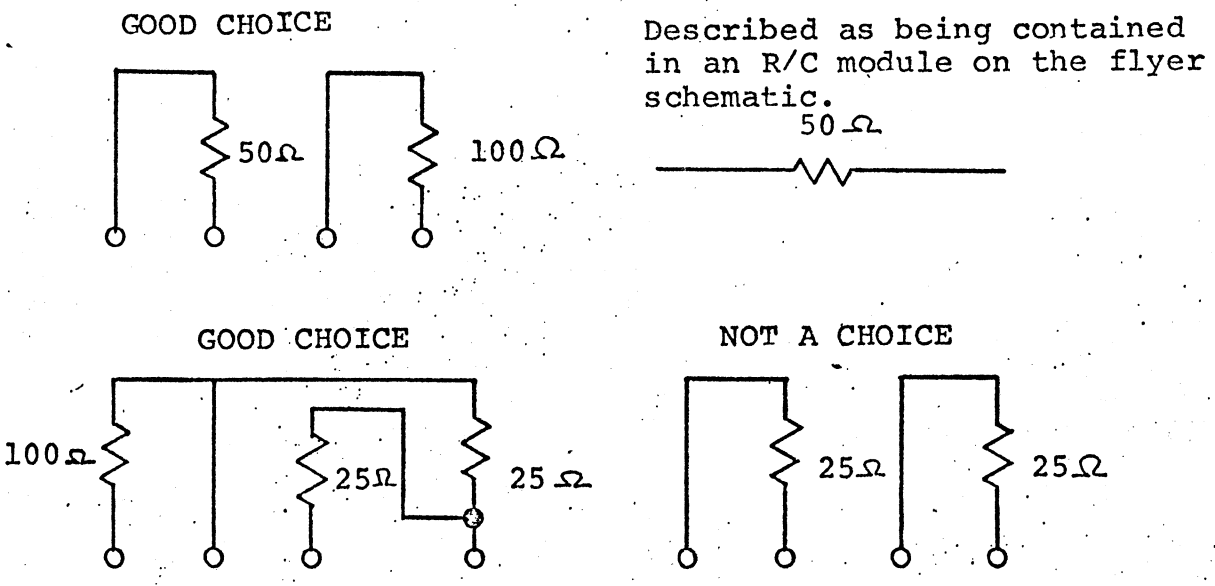
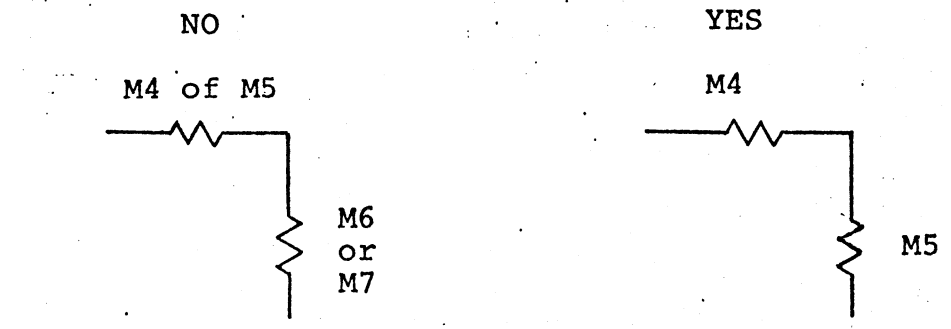


FIGURE 1

13.4 Alternate packaging will be indicated in the packaging section and not on the schematic.



M4 = 2390616
M5 = 2390630
M6 = 2390423
M7 = 2390420

M4 = 2390616 or 2390630
M5 = 2390423 or 2390420

FIGURE 2

13.5 The schematic must be drawn to show the maximum number of input diodes present as a group in any component which may be used to package the circuit. (Excluding extend diodes.) All choices of components will be listed in the Packaging Section.

14.0 SCHEMATIC USAGE

14.1 The schematic will be drawn on the grid format of the circuit flyer schematic sheet.

14.2 The single page schematic sheet (Form No. M-30-1872-1) should be used only when the entire circuit can be contained by one page. For any additional pages, use the extended schematic sheet, Form No. M-30-1873-1.

14.3 The expanded schematic sheet or extended schematic sheet should not be used until all efforts are made to draw the circuit on the single page schematic sheets.

14.4 The schematic should be limited to as few pages as possible.

14.5 Use of the Expanded - Schematic sheet must be limited to only cases where its use is mandatory for ease in reading the circuit. The present CCDA programs can not handle more than 9 circuit flyer schematic pages.

15.0 SCHEMATIC GRID RULES

15.1 For proper schematic symbols, refer to CES 0-1001-000, Section S (graphic symbols).

15.2 CIRCUIT LINES - Must be at right angles and terminate in a grid square.

15.3 NODES, COMPONENTS, AND ELEMENTS - Shall be contained within grid squares. Types of components that can be shown in one grid square must be shown in only one.

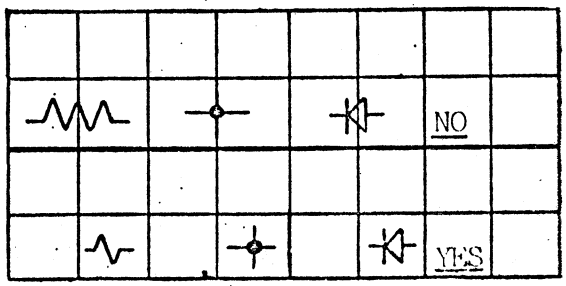


FIGURE 3

15.4 Only one node, component or element can be contained within a grid square.

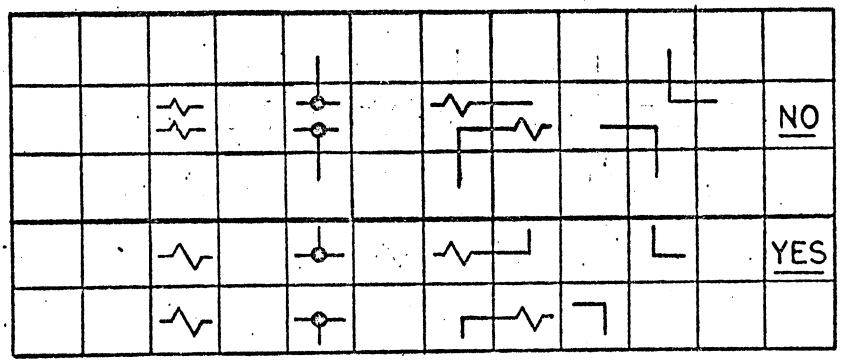


FIGURE 4

15.5 ELEMENTS THAT REQUIRE MORE THAN ONE GRID SQUARE FOR THEIR SYMBOL - Must be enclosed with solid lines. Components in this category are transformers, delay lines, tapped inductors and switches. (Transistors require more than one grid square but are excluded from this rule.) These solid lines must be drawn between the grid lines and must enclose a rectangular area. The solid lines will occupy grid squares; therefore, no other element may be drawn in its location. Any component pin identification required will be noted outside the solid boundary line and the pin number encircled. Solid lines are drawn such that no leads are drawn through corner grid squares. For example, a four-leaded transformer will be enclosed within a six-grid square solid line and will be properly numbered relative to connections.

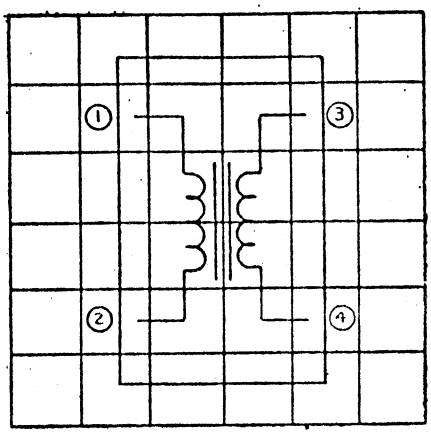
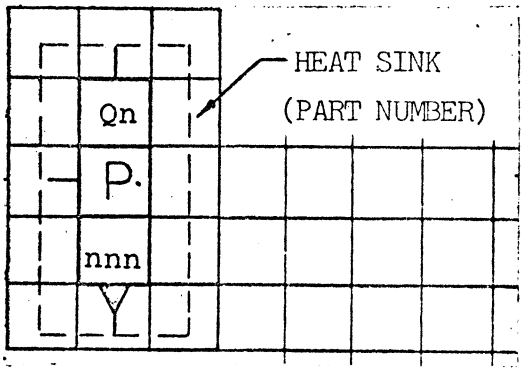


FIGURE 5
TRANSFORMER

15.6 HEAT SINKS - will be indicated by a dashed line drawn around the discrete transistor. This dashed line must be placed between grid lines and drawn such as to complete a rectangle. This dashed line will occupy grid squares; therefore, no other element may be drawn in its location. The part number will be referenced to the heat sink by writing the word "heat sink" with the part number directly below. An arrow will be drawn to point to the dashed line representing the heat sink.



Qn = Transistor Designation

nnn = Type Number

FIGURE 6

15.7 COMBINED FLYER LOGIC - is drawn on the schematic grid format as follows:

1. Logic blocks are drawn on grid lines and input/output and interconnection lines between grid lines.

2. The same rules as for the D/A block representation are used, excluding the line positioning and intersection of input/output line rules to identify the logic blocks.

3. A schematic showing actual elements that perform the function represented by the logic blocks is not required.

EXAMPLE:

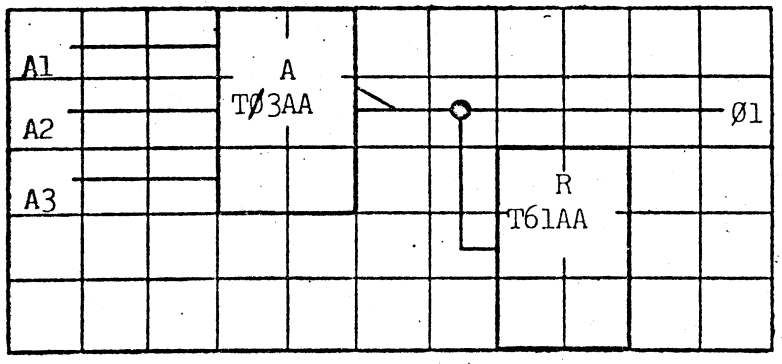


FIGURE 7

15.8 SPECIAL GRID RULES FOR THE EXPANDED SCHEMATIC SHEET - Elements such as resistors, diodes, capacitors, and fuses are allowed in grid rows 1 or 19 if drawn in their vertical position and in grid rows A or S if drawn in their horizontal position. (See Figure 8.)

1. A transistor can be placed in grid rows 1 or 19 only if the base lead is facing opposite the page divider. (See Figure 8)

2. Grid squares at the intersection of pages 2, 3, 4, and 5 may contain the intersection of two lines at right angles; interconnections between (only) adjacent pages, pin boxes and voltage ground pins. (See Figure 8)

Example of allowable conditions on the Expanded Schematic Sheet:

Qn = Transistor Designation

nnn = Type Number

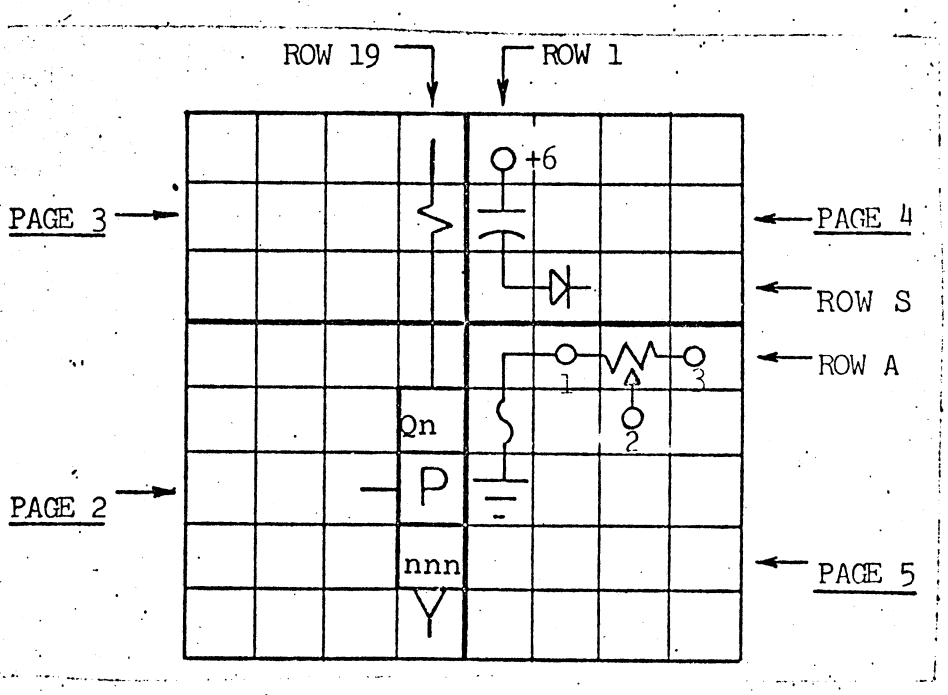


FIGURE 8

SCHEMATIC GRID RULES (continued)

15.9 PAGE CROSS REFERENCING

15.9.1 Cross Referencing is required to identify lines which are common but not drawn on the same schematic sheet or located on non-adjacent pages of the extended schematic sheet.

15.9.2 A continuation mark (——⟩) will be placed at the end of both the "TO' and "From" line. "Two systems of line referencing now exist. Either system will be acceptable at the discretion of the local flyer group."

15.9.3 System I - Reference will be made by placing the page and grid coordinates in the form NNNA(N - numeric, A - alphabetic) of the "to" line with the "from" line and vice versa. The first numeric is the page number. The second and third numeric is the X-coordinate of the grid square containing the continuation mark. The alphabetic character is the Y-coordinate of the grid square containing the continuation mark.

15.9.4 System II - Referencing may be accomplished by noting the same two digit grid coordinate above the end of both the "From" and the "To" line segments referenced - Use the grid coordinate of the nearest component in the "From" page net. To complete the referencing, indicate the referenced page number beneath the end of the line. (i.e. Page Two References to Page Three, and Page Three References Back to Page Two: The referenced grid coordinate is the same on both pages. This allows quick and easy reference without resorting to tracing out grid coordinates as in System I.) This rule does not apply to interconnections between adjacent pages of the Expanded Schematic Sheet.

Example of cross referencing between schematic sheets or between non-adjacent pages of the expanded schematic sheet:

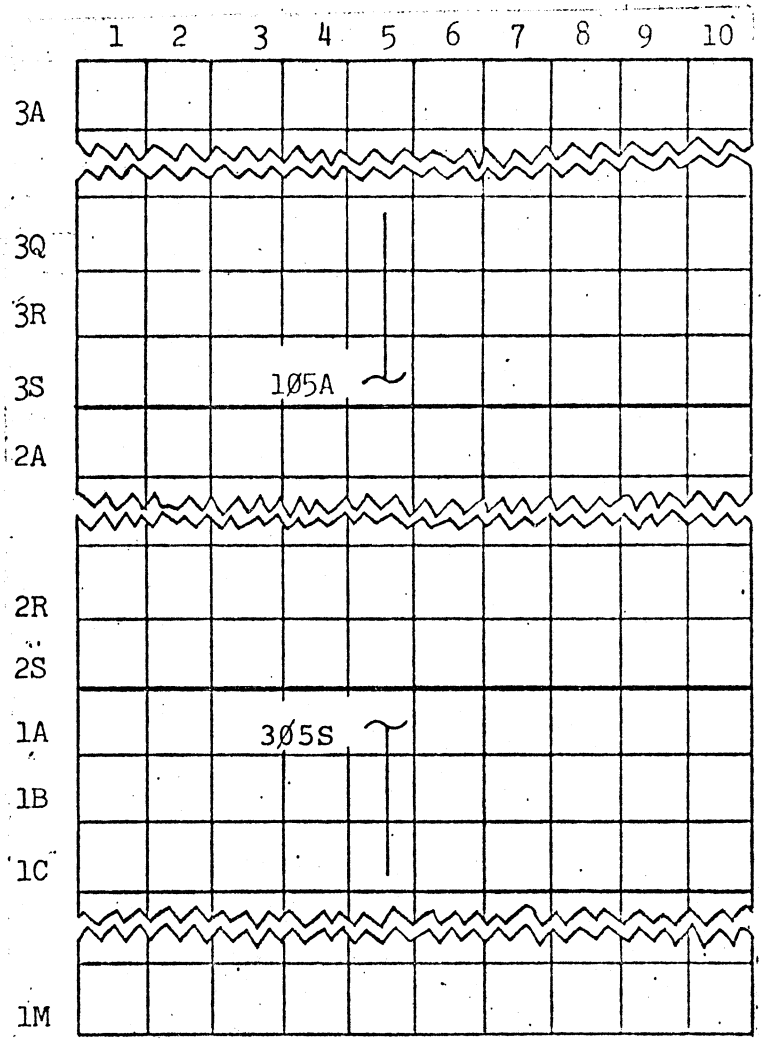


FIGURE 9

15.10 INTERCONNECTIONS BETWEEN ADJACENT PAGES OF THE EXPANDED SCHEMATIC SHEET - are made directly by continuing the line through the page divider to the desired location on that page. Restrictions to this method are that connections between two lines (nodes) must not be placed in the grid square adjacent to the page divider.

Examples of good and bad interconnections between adjacent pages of the expanded schematic sheet:

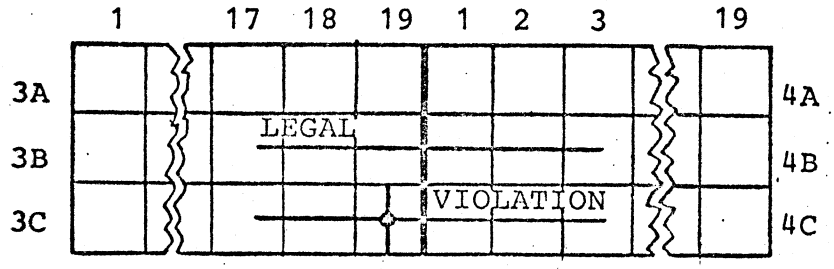


FIGURE 10

15.11 PIN BOXES

15.11.1 It has been established that pin boxes are not required when modules and module portions are identified by "M" numbers.

15.11.2 If there exists the possibility of extending a logic function, the "extend" module pin must be represented by a pin box. Extend diodes must not be shown (diodes that would be obtained from an additional component).

15.15.4 Unapproved components will be denoted by placing a (U) in parenthesis after the part number, restricted components by placing an (R) in parenthesis after the part number, and controlled or C-status components by placing a (C) in parenthesis after the part number.

15.16 DISCRETE COMPONENTS

15.16.1 Resistors - Show the power rating, ohmic tolerance, value, and IBM part number. If all or the majority of resistors have the same power rating and ohmic tolerance, it may be indicated by a note. All other resistors will be completely identified as indicated.

15.16.2 Capacitors - Show the capacitance value, tolerance, its IBM part number and polarity if polarized.

15.16.3 Transistors and Diodes - Show IBM type and part number.

15.16.4 All Other Components - Show proper identification for that type component and its IBM part number.

15.16.5 Component Identification - Will be implemented by placing the notations adjacent to the symbol. No strict rules need be followed other than the fact that the notation be easily associated with the element being identified.

Example:

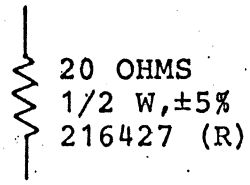


FIGURE 13

15.17 MODULAR COMPONENTS

15.17.1 The IBM part numbers for the module will be entered in the section entitled "Packaging."

15.17.2 Each module section (group of elements contained in a module) must have a unique "M" number assigned to it in the form MN (N - numeric).

Example:

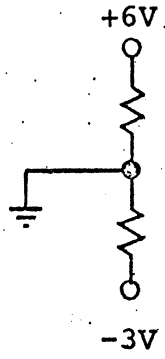


FIGURE 12

15.12.4 A separate voltage or ground pin must be shown for each module that is tied to a voltage or ground.

15.13 INPUTS AND OUTPUTS

15.13.1 Schematic inputs and outputs must be labeled to be compatible with those on the Design Automation Block Representation.

15.13.2 Inputs must be shown at the left and outputs at the right.

15.13.3 Input and output line terminations must have a small open circle.

15.14 TEST POINTS

Test points will be coded as outputs and must be labeled to be compatible with the corresponding test points on the Design Automation Block Representation.

15.15 GENERAL COMPONENT INFORMATION

15.15.1 All components on a controlled or formal release circuit flyer must bear a final part number. This is to insure that component and component hardware will be available when a card using these parts is ready for release to Manufacturing. (See Section 26, Paragraph 1.0).

15.15.2 Components with development part numbers may only be used on experimental circuit flyers.

15.15.3 Components with controlled (C-status) may be used on controlled or experimental flyers.

Example of typical circuit

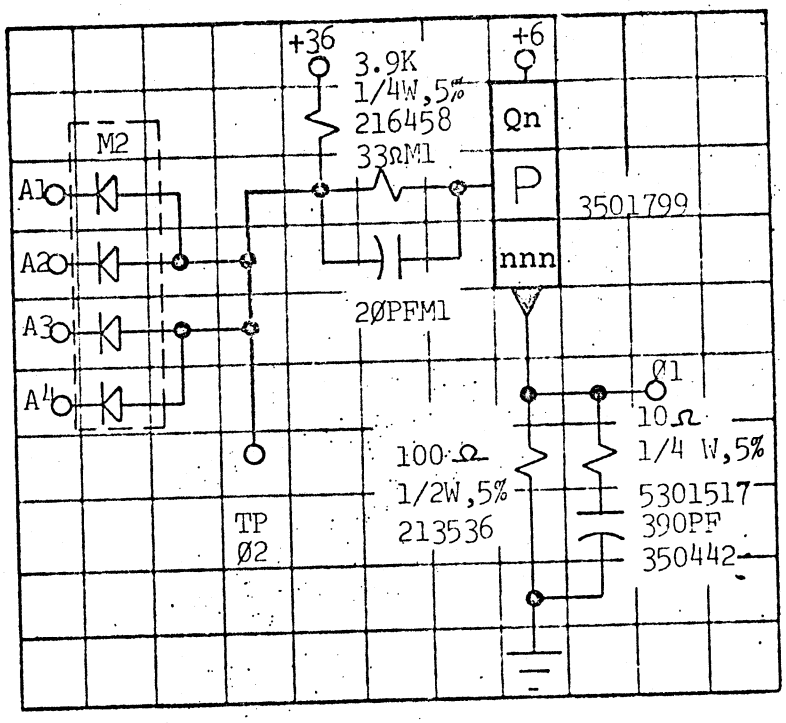


FIGURE 11

15.12 VOLTAGE AND GROUND PINS

15.12.1 Voltage Lines - Will be represented by placing a small open circle at the line termination with the voltage polarity and value easily associated with it (See Figure 11.)

15.12.2 Ground Lines - Will be represented by placing a ground symbol at the line termination (See Figure 11.)

15.12.3 For Reading Convenience - It is a good practice to have positive voltage on top and negative voltages and ground symbols shown on the bottom.

15.17.3 Reference will be made between the "M" number and the component part number in the Packaging Section. In the case where duplicate modules or module sections require individual "M" numbers, each individual "M" number will be referenced to the same module part number.

Example: (M1, [illegible] - SLT Module 361479)

15.17.4 SLT Modules - A portion of a circuit contained in an SLT module must be enclosed by dashed lines and identified by a "M" number. This dashed line will be drawn between grid lines; however, will not restrict a grid square. This is to say, an element, component, node, etc. may occupy the same grid square as this dashed line.

15.17.5 Resistor and capacitor values will be shown. For alternate packaging with different tolerances see paragraph 13.2.

15.17.6 For a complete circuit using one SLT module, see example in Figure 14. You will note that only passive components require component value identification. Since the semi-conductors are SLT chips, they need not be identified.

Example of a circuit contained in one SLT module:

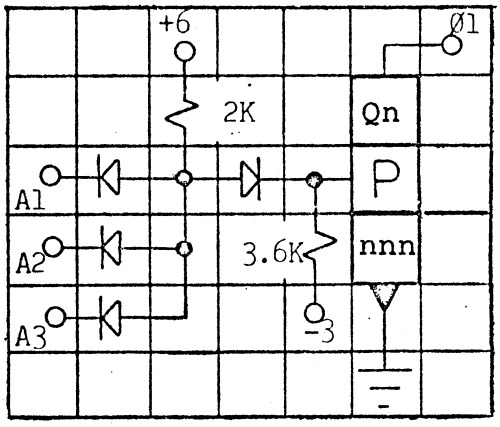


FIGURE 14

15.17.7 See example of a typical circuit (Figure 11) for a portion of a circuit contained in an SLT module. You will note the dashed lines drawn between the grid lines around the elements contained in that component. The "M" number must be placed inside the dashed lines to relate the elements to a specific module part number.

15.17.8 R/C Glazed Modules - Elements contained within a R/C module are not to be enclosed within dashed lines.

15.17.9 Each element of an R/C module is identified by a unique "M" number and value.

15.17.10 In the case where the circuitry is such that there is only one application for the modular elements, the whole module will be referenced by the same "M" number.

15.17.11 The representation of resistors and capacitors in this type of module is shown in the example of a typical circuit (Figure 11).

16.0 DESIGN AUTOMATION BLOCK REPRESENTATION

16.1 Logic representation of computer circuitry, designed for use within the limitations and subject to the requirements of the SLDA and CCDA programs as they exist at this time.

16.2 For ground rules on logic block symbols, use of the wedge to indicate polarity, and use of symbols to indicate positive and negative going shift through AC coupling, see Corporate Engineering Standard 0-1046-3, 0-1046-5, 0-1046-17, and/or SLT Card Logic Diagram, Suffix 1.

16.3 INPUT AND OUTPUT LINE NUMBERS

16.3.1 The block will be drawn with inputs on the left edge and outputs on the right edge.

16.3.2 Each block must have I/O numbers assigned. The outputs are numbered Ø1 through Ø9, and Ø. The maximum number of outputs is 10. Inputs are labeled A1, A2, B1, C1, C2, etc. - letters A through Z excluding I and O may be used. The maximum number of inputs is 24.

16.3.3 When Inputs Are Interchangeable - The first characters of the interchangeable inputs are identical; example, A1, A2, A3. The symmetrical inputs must be numbered consecutively and have their line positions adjacent to each other.

16.3.4 When Inputs Are Not Interchangeable - They must have a unique first character, example, A1, B1 C1.

16.3.5 Line Drawing Positions - Blocks which have non-interchangeable inputs must have an asterisk (*) in the first position of the block symbol and the input line drawing positions must be specified.

16.3.6 Output line drawing positions must always be shown when there are two or more outputs specified.

Example of non-interchangeable inputs and multiple outputs:

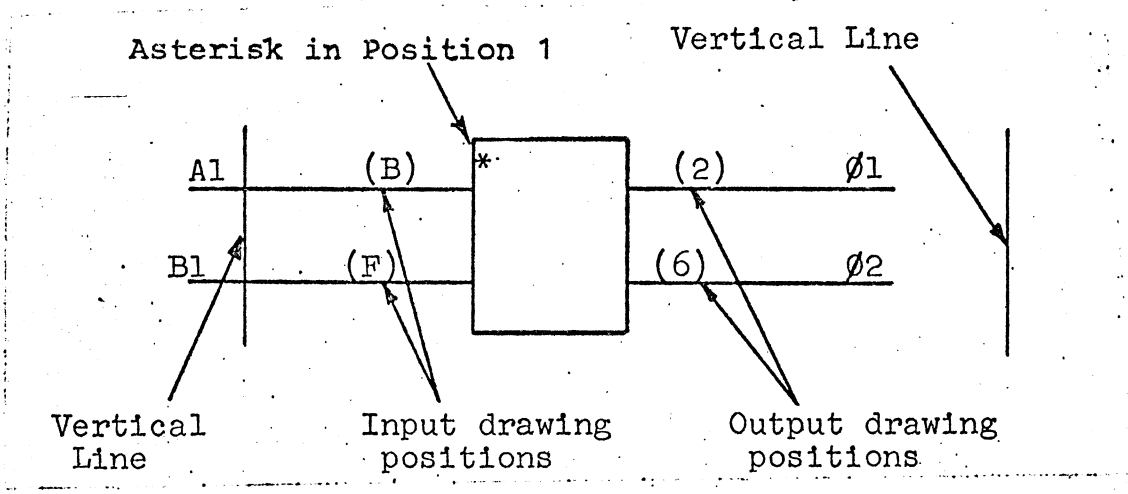


FIGURE 15

16.4 VERTICAL LINE INTERSECTION OR NON-INTERSECTION OF INPUTS AND OUTPUTS

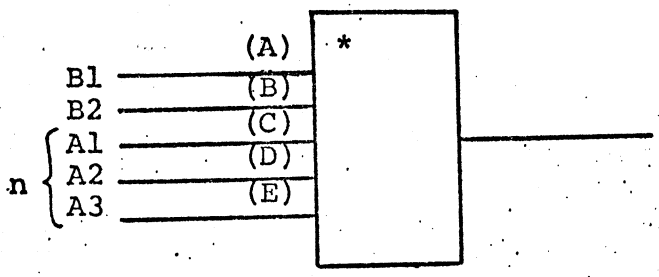
16.4.1 Intersect - If a vertical line intersects the I/O lines, the signal points may be brought out to a card pin.

16.4.2 Non-Intersect - If a vertical line does not intersect the I/O lines, the signals will never be brought out to card pins. An example of this is on grouping flyers.

16.4.3 Extendable Inputs

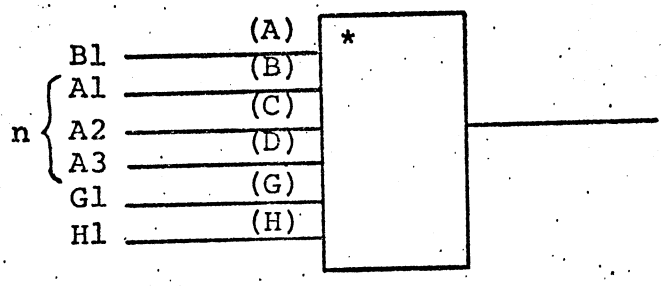
1. No circuit flyer may have more than one set of extendable input lines.
2. Extendable input lines must be grouped together.
3. The first such extendable block line must be line A1 which may occur in any line position.
4. Non-symmetrical block lines may precede or follow the set of extendable input lines, if any. (See Figure 16.)
5. For circuit flyers to be used in card ALD schematic applications an extend output should be used to indicate the extend capability of inputs which exceed the maximum number of inputs in the main module. (See Figure 16, Example C)

Example A:



n=1 to 22

Example B:



n=1 to 5

Example C:

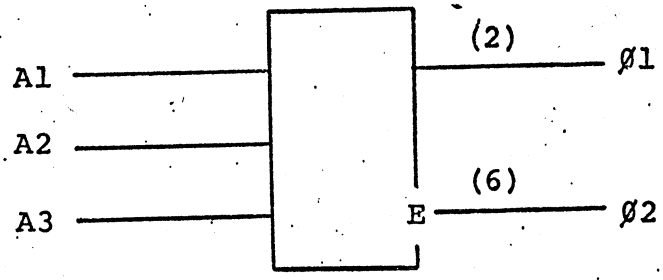


FIGURE 16

16.5. TEST POINTS

16.5.1 Test points will be indicated when they originate within a circuit. They should not be used by systems designers in their logic design. (Note: They will not be indicated when they originate between circuits.)

16.5.2 Test points will be treated only as outputs. The maximum number of test points is 9.

16.5.3 Indication will be made by placing the letter "T" in the right-hand edge line of the block, adjacent to the test point output line.

16.5.4 The test point line will be given a signal point identification number.

Example:

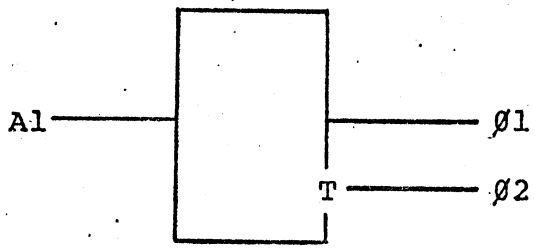


FIGURE 17

16.6 EDGE OF BLOCK CHARACTERS

See Corporate Engineering Standard 0-1046-3 for instructions on use of wedge (◺), non-logic connections (X), AC coupling (N or P), and extender (E). Also refer to suffix 1.

17.0 LOAD CHECK SHEET

Must be complete for each input and output (except test points) on all controlled and formal release circuit flyers.

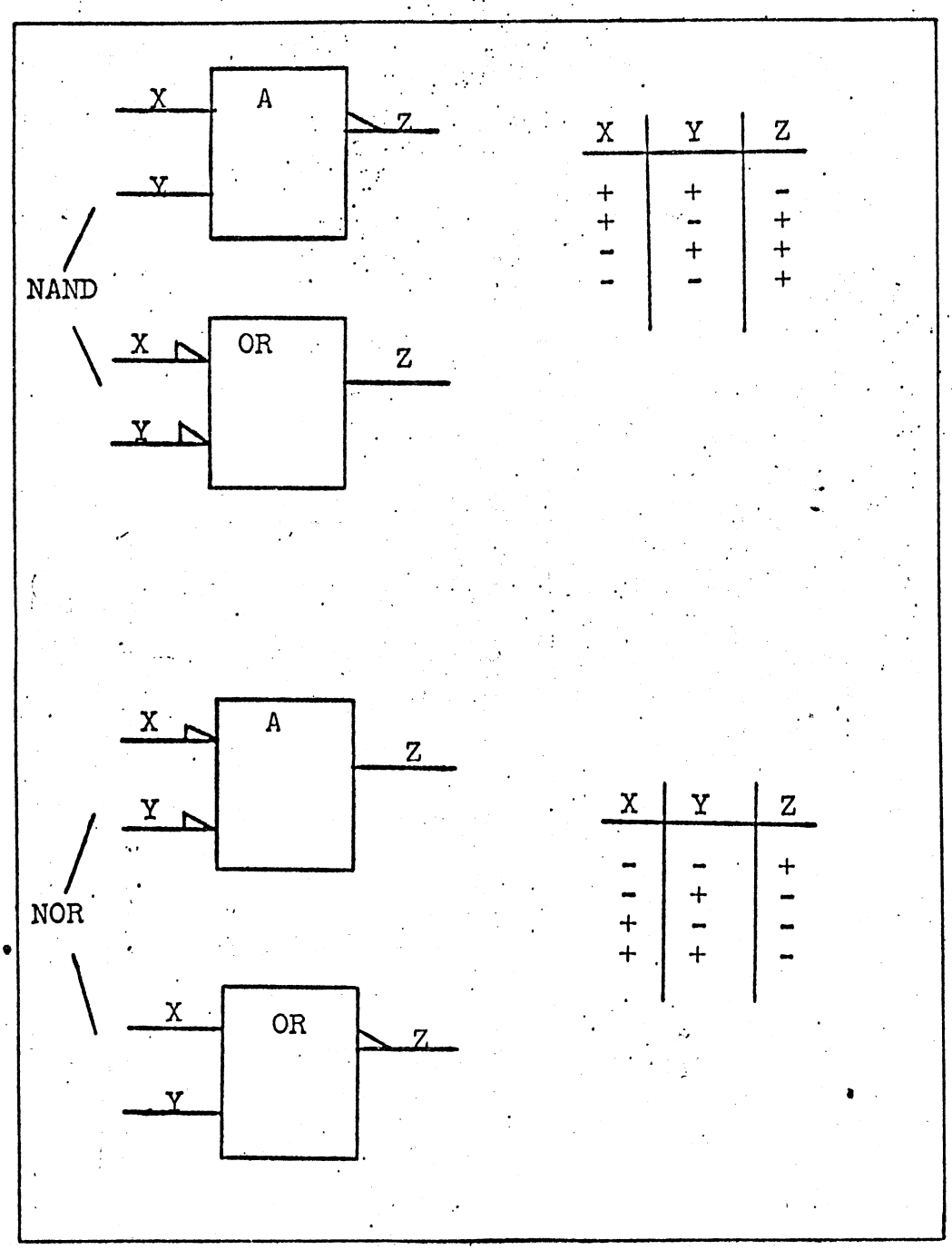
17.1 LOGIC FUNCTION

17.1.1 Information in this section of the logic check sheet is used by the Design Automation Block check and simulation programs.

NOTE: (wedge) = least positive logic level.

17.1.2 When a pure logic function is used, both representations must be shown under the DA Logic Representation section of the Circuit Flyer.

Standard Logic Blocks Having Symmetrical Inputs (See Figures 18-23).



X	Y	Z
+	+	-
+	-	+
-	+	+
-	-	+

X	Y	Z
-	-	+
-	+	-
+	-	-
+	+	-

FIGURE 18

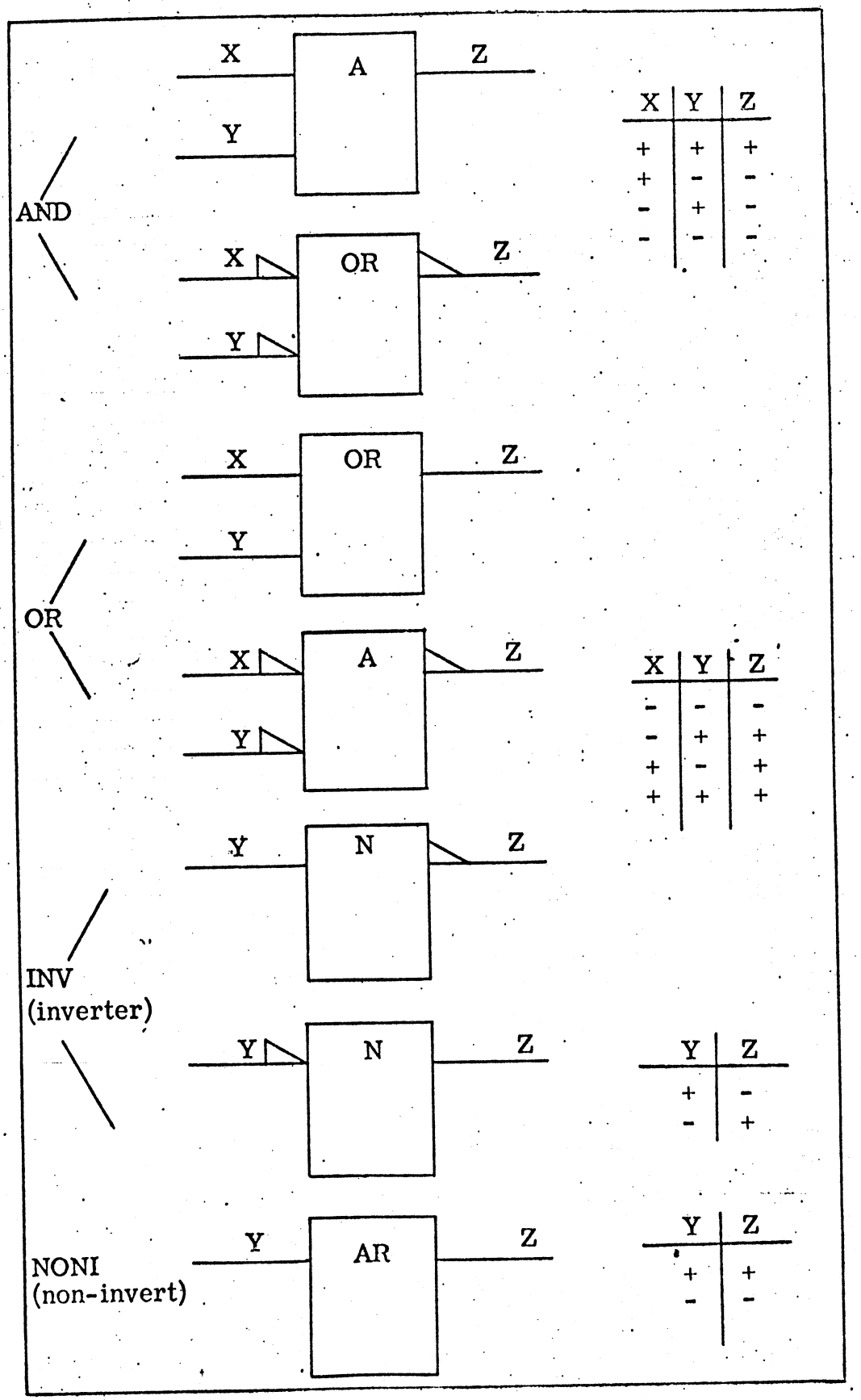

AND
X
Y
A
Z
X | Y | Z
+ + +
+ - -
- + -
- - -
OR
X
Y
OR
Z
X
Y
OR
Z
OR
X
Y
A
Z
X | Y | Z
- - -
- + +
+ - +
+ + +
INV
(inverter)
Y
N
Z
Y
N
Z
Y | Z
+ -
- +
NONI
(non-invert)
Y
AR
Z
Y | Z
+ +
- -

FIGURE 19

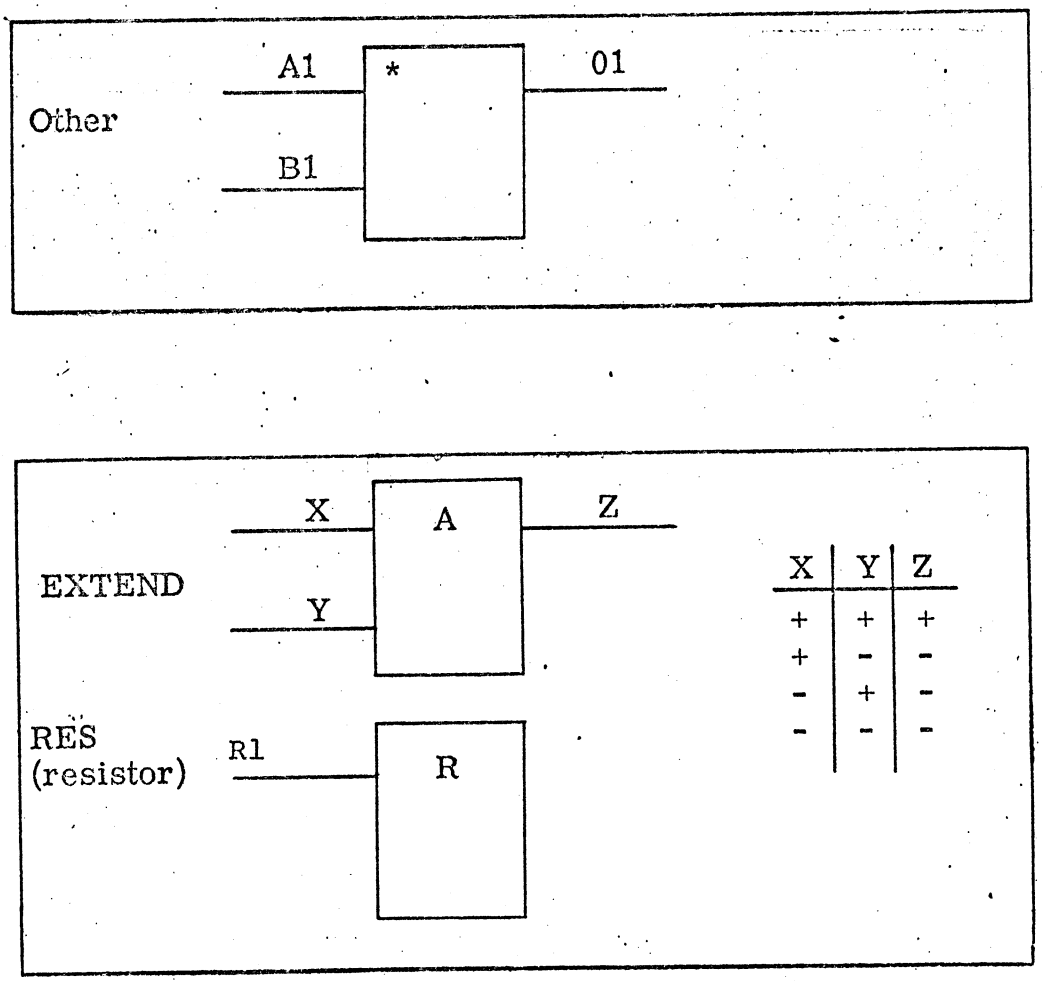
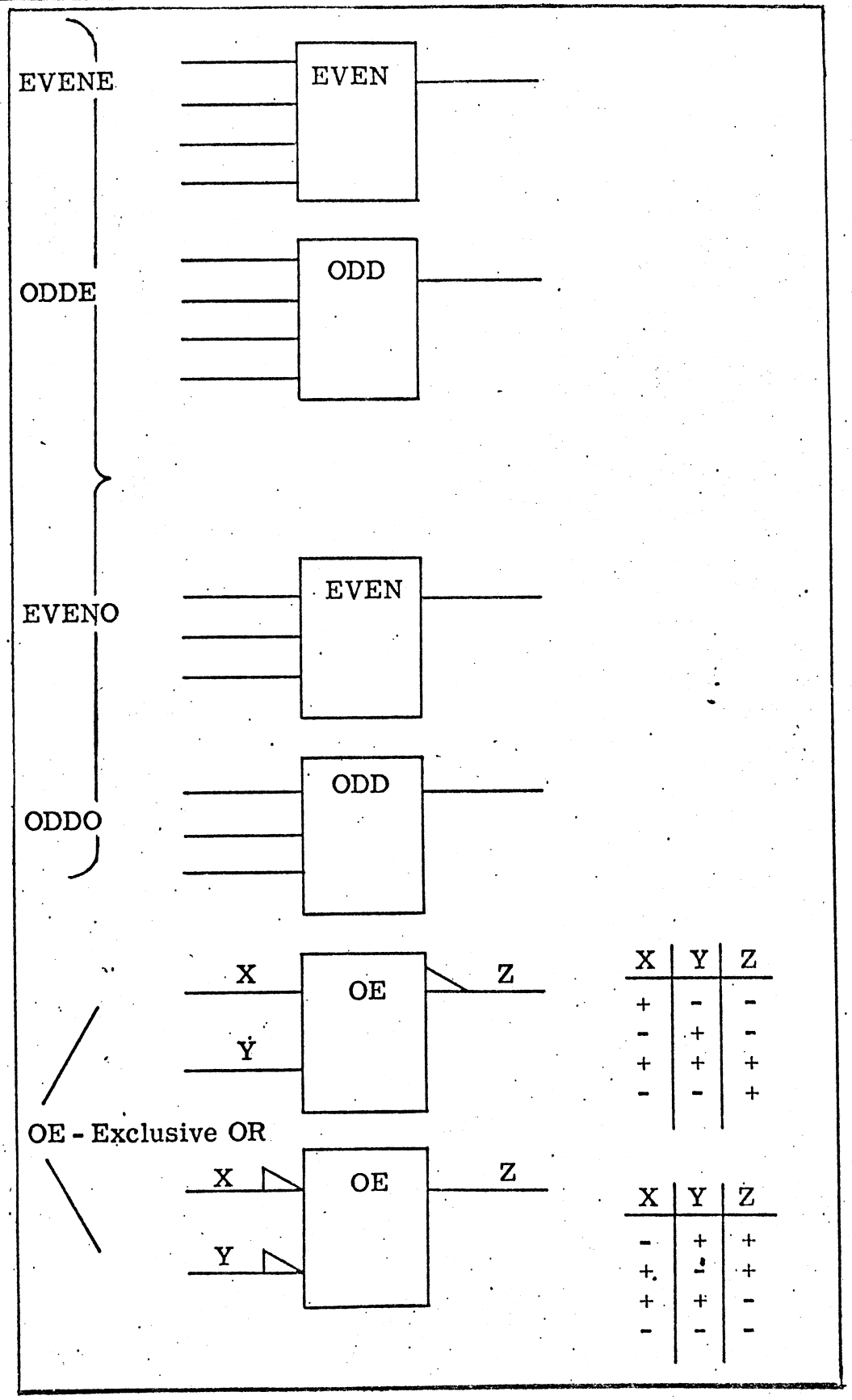


FIGURE 20



X	Y	Z
+	-	-
-	+	-
+	+	+
-	-	+

X	Y	Z
-	+	+
+	-	+
+	+	-
-	-	-

FIGURE 21

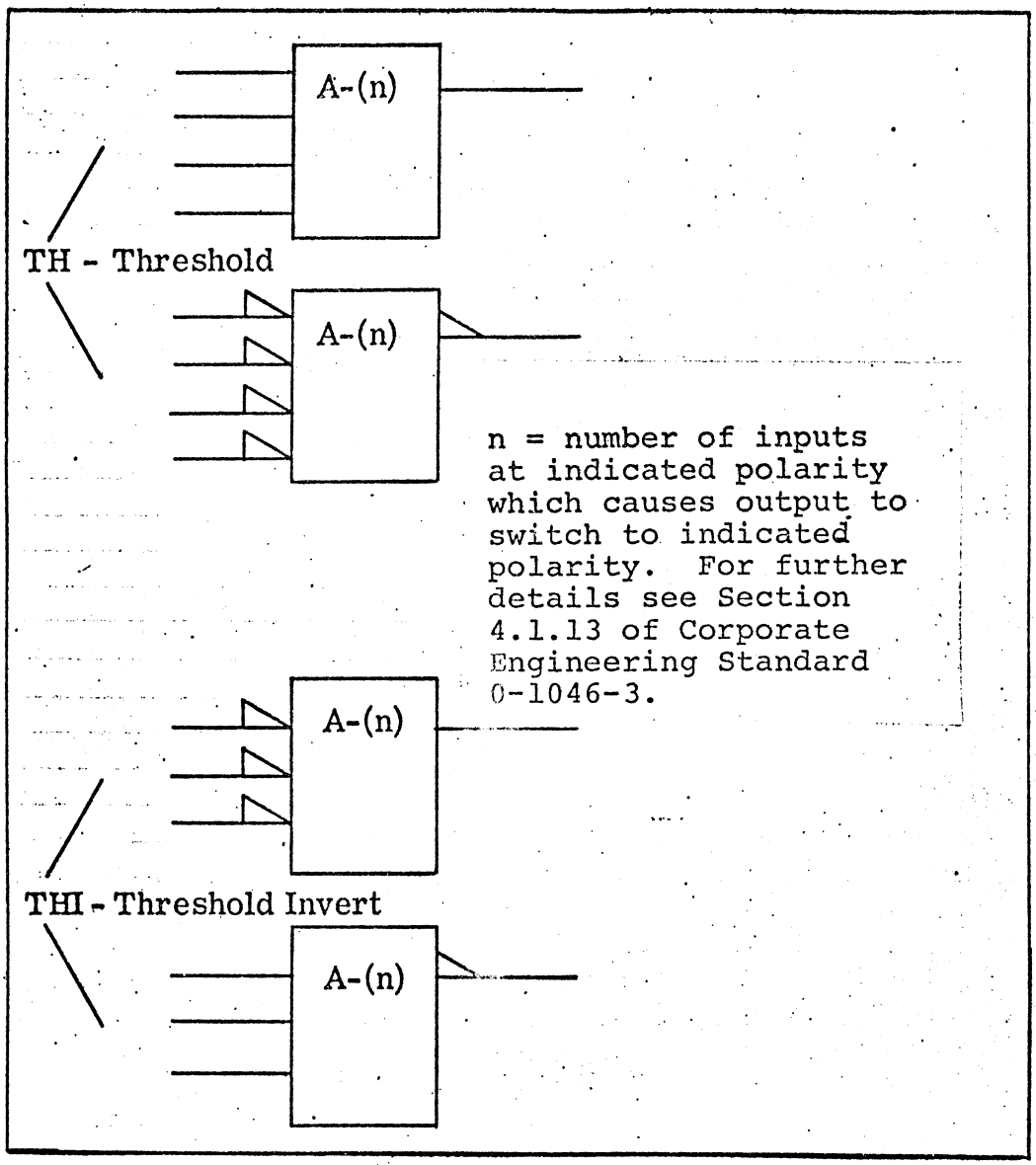
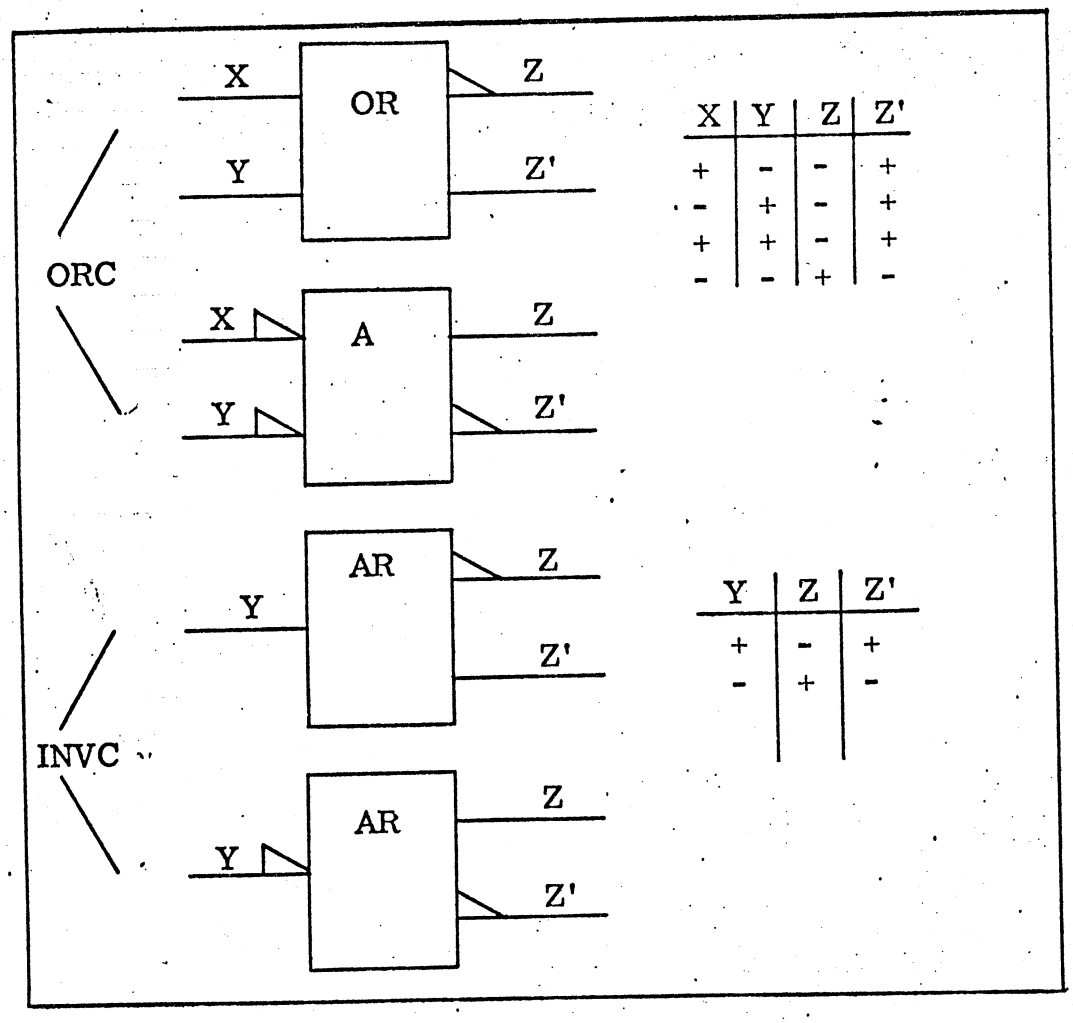

A-(n)
TH - Threshold
A-(n)
n = number of inputs at indicated polarity which causes output to switch to indicated polarity. For further details see Section 4.1.13 of Corporate Engineering Standard 0-1046-3.
A-(n)
THI - Threshold Invert
A-(n)

FIGURE. 22



X	Y	Z	Z'
+	-	-	+
-	+	-	+
+	+	-	+
-	-	+	-

Y	Z	Z'
+	-	+
-	+	-

FIGURE 23

17.2 DOT FUNCTION

One of the available boxes (AND, OR, None) is checked to describe the logical function performed when several blocks have collectors or emitters wired in common. Refer to Section 4.1.19 of Corporate Engineering Standard 0-1046-3 for a more detailed explanation.

17.2 DELAY PARAMETERS

17.2.1 This consists of the delay used by the SLDA logic simulation program. The formula for delay is:

Delay = 0.8 WC + 0.2 BC (for 8 inches net)
WC = worst case delay BC = best case delay

17.2.2 It is desirable to specify a delay figure for a circuit used in its average environment.

17.3 "B" FACTOR

A weight factor "B" is assigned to each circuit based on worst case loading and representative transition times for current changes.

$$B \approx \frac{\text{(maximum ground current change in m.a.)}}{\text{(current transition time in n.s.)}}$$

17.4 LOAD CHECK DATA

17.4.1 This data is used by Design Automation programs to perform over load and under load checks.

17.4.2 It is an aid for Test Equipment Engineering in generation of test data on special circuits.

17.4.3 Information from this section is extracted from the Circuit Master Tape (CMT) for the FUSED Program.

17.4.4 This load check data must always be complete even though the "Does Not Apply" block is checked. The "Does Not Apply" block is for Design Automation use only and indicates that no load checking rules have to be coded on the Design Automation Rules Tape (CMT).

17.5 CURRENT DIRECTION

The IRE Standard is followed. It states that current flowing into a node is positive and away from a node is negative. Thus into a block is negative. Out of a block is positive.

Example:

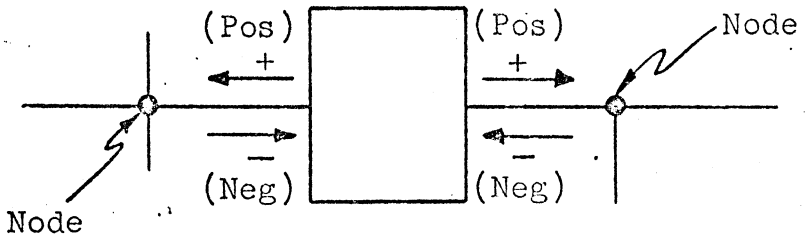


FIGURE 26

17.6 SPI - SIGNAL POINT IDENTIFICATION

SPI refers to specific input or output pins found on the Design Automation Block Representation.

Rule: Inputs alpha-numeric, Outputs numeric.

17.7 CPL - COUPLING INDICATOR

17.7.1 CPL is used to indicate if a given pin has a source current associated with the pin under consideration. The program checks that at least one coupled or non-check pin is in each net.

Either: C - Coupled
U - Uncoupled
N - Non-check

17.7.2 Examples of coupled:

When there is a direct path from the pin to a power supply voltage or ground via a resistive path.

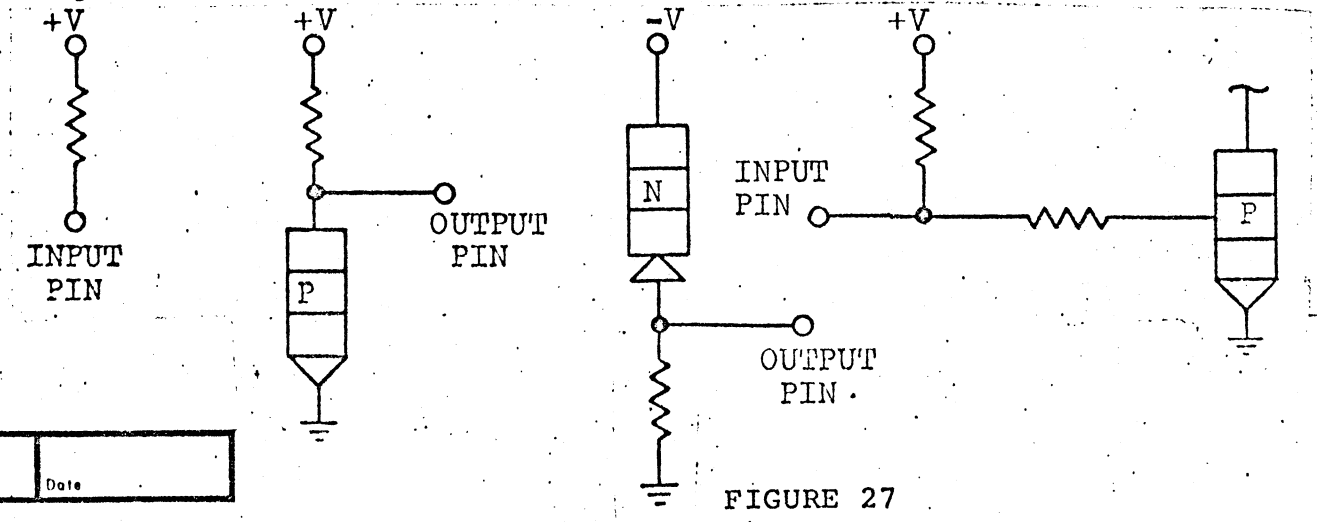


FIGURE 27

17.7.3 Example of uncoupled:

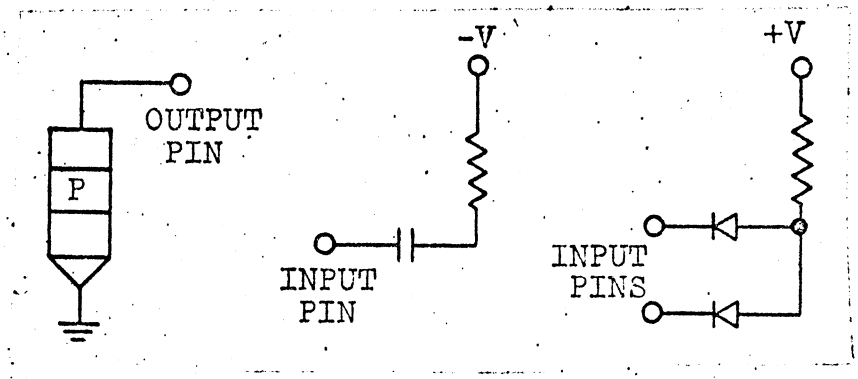


FIGURE 28

17.8 CT - CURRENT TYPE

17.8.1 This term defines the type of current making up the net and is defined at both the up and down voltage levels.

Enter: N - Non-check
L - Load Current
W - Weakest Source
A - Additive Source

1. N - This code is used when it is impossible to define currents and voltage or special driving rules for a given Circuit Signal Point Identifier (SPI). Do not use "N" with special driving rules.

NOTE: The Load Check program checks each net for rules. When non-checks are found, the program ignores that signal point and continues checking the remainder of the net. There is no indication or message given as to what nets contain the non-check condition. It is then the user's problem to locate and complete checking manually.

2. L - This code is used to indicate the signal point in question is absorbing current.

3. W - This code is used to identify a source that represents the worst case drive conditions in respect to other sources in a net.

4. A - This code is used to indicate that it is a source.

Even though it is worst case, it may be added to another source in a dot condition.

Family	Class	Up Level	Down Level
NPN	Output Input Resistor	L L A or W	A or W L L
PNP	Output Input Resistor	A or W L L	L L A or W

17.8.2 The terms W and A are used to determine the available and allowable current when the net contains more than one current source.

Example: +V

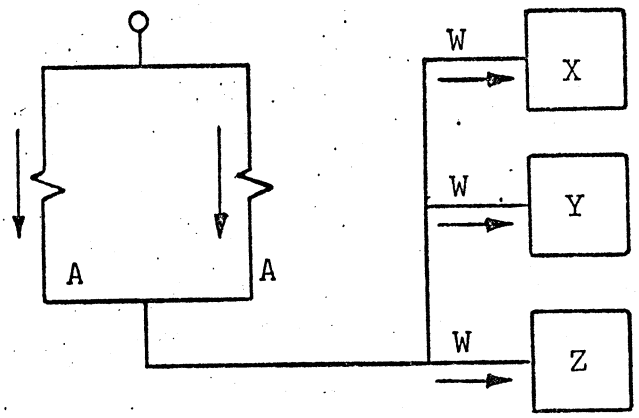
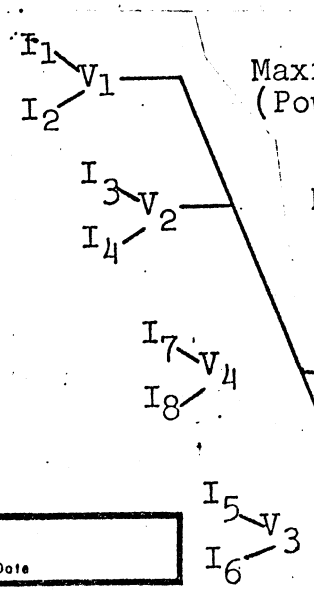


FIGURE 29

17.9 VOLTAGES AND CURRENTS



Maximum up level worst case value (Power supply maximum less tolerance).

Minimum up level - generally includes noise tolerance. (Minimum up level required to guarantee operation of the circuit.)

Minimum down level - generally includes noise tolerance (most positive or least negative down level voltage.)

Maximum down level (the most negative or least positive down level voltage).

1. At each level a minimum and maximum current can be calculated.

2. For each signal point, 4 voltage and 8 current terms must appear in the chart.

3. A blank does not substitute for a zero in the chart. See paragraphs 17.9.1 and 17.9.2 for example of the correct placement of voltage and current values.

17.9.1 Voltage Terms

V_1 - Maximum up level worst case value. Must be the power supply maximum less the tolerance.

V_2 - Minimum up level voltage.

V_3 - Maximum down level voltage (the most negative or least positive down level voltage).

V_4 - Minimum down level voltage (most positive or least negative).

17.9.1.1 All Voltages - are expressed in volts. They may be as accurate as is necessary - thus these fields are variable in length, and may have a variable number of decimal places. If the voltage is positive, the plus sign is optional. However, if negative, the minus sign must appear. In any case, the decimal point is necessary. (See Figures 30 - 34).

17.9.1.2 Analog Circuits - will require only a minimum up level voltage (V2) and a minimum down level voltage (V4) if no special driving rules are stated. In this case, the Signal Point Identifier (SPI) must be coded as "N".

17.9.2 Current Terms

I_1 - Available source current or the maximum load current at the maximum up level (worst case) voltage (V_1). If the current type (up level) is "I" (load current) I_1 is the maximum load current. Otherwise it is the available source current.

I_2 - Minimum source current or minimum load current at the maximum up level (worst case) voltage, depending again on current type.

I_3 - Available source current or maximum load current at the minimum up level voltage, depending again on current type.

I_4 - Minimum source current or the minimum load current at the minimum up level voltage, depending on current type.

I_5 - Available source current or maximum load current at the maximum down level voltage. depending on current type.

I_6 - Minimum source current or minimum load current at the maximum down level voltage, depending on current type.

I_7 - Available source current or the maximum load current at the minimum down level voltage. depending on current type.

I_8 - Minimum source current or the minimum load current at the minimum down level voltage, depending on current type.

17.9.2.1 All Currents - are expressed in milliamperes. A plus sign is optional; a minus sign is necessary for negative currents. Currents can be accurate to as many decimal places as necessary. The decimal point must always appear. (See Figures 30-34)

17.9.2.2 For Analog Circuits - it is not necessary to express currents due to the nature of analog pulses, but as many as possible would be helpful to both the user and simulation programs.

17.9.2.3 If no data is used for any portion of the chart leave the spaces blank. Do not use dashes.

17.10 SPECIAL DRIVING RULES

17.10.1 Special driving rules are used by Design Automation for branching and loading checks. This section must be complete in addition to the Load Check Data when special driving rules exist.

Example:

"Circuit X can only drive circuit Y, with no further branching of the drivers." Include all outputs and inputs of the driving and driven circuits.

17.10.2 It is acknowledged that some circuit inputs or outputs may not be compatible to the twelve statement requirement. One example of this is an I/O line upon which a non-standard, DC voltage appears. Circuits such as this can have no meaningful level statement. In these cases Special Driving Rules shall suffice if given properly.

CIRCUIT FLYER PREPARATION

Example of correct placement of voltage and current terms:

3-4-____-_

IBM CIRCUIT FLYER

PART NO.
BLOCK ID.
TITLE
PAGE NO.
CONTROL CODE

CKT NO. / LOGIC FUN.	LOGIC FUNCTIONS																		DOT FUNCTIONS		
	NAND	NOR	AND	OR	INV	RES	NONI	OTHER	EXTEND	EVENE	ODDE	EVENO	ODDO	OE	TH	THI	ORC	INVC	AND	R	NONE

DELAY LIMITS

	DELAY USED BY SLDA	8" NET BC	8" NET WC	48" NET BC	48" NET WC
OUTPUT RISING					
OUTPUT FALLING					

"B" FACTOR_____

DELAY PARAMETERS ☐ DOES NOT APPLY

A REALISTIC ESTIMATE OF MACHINE CIRCUIT SPEEDS SHOULD BE OBTAINED FROM THE LOCAL MACHINE TECHNOLOGY GROUP.

LOAD CHECKING DATA ☐ DOES NOT APPLY (DA USE ONLY)

SPI		CPL	CT	MAXIMUM VOLTAGE (VOLTS)	MINIMUM VOLTAGE (VOLTS)	AVAILABLE SOURCE CURRENT (MA)	MINIMUM SOURCE CURRENT (MA)	MAXIMUM LOAD CURRENT (MA)	MINIMUM LOAD CURRENT (MA)	DOT COUNT
	UP LEVEL			V1		I1	I2	I1	I2	
					V2	I3	I4	I3	I4	
	DOWN LEVEL				V4	I7	I8	I7	I8	
				V3		I5	I6	I5	I6	
	UP LEVEL									
	DOWN LEVEL									
	UP LEVEL									
	DOWN LEVEL									
	UP LEVEL									
	DOWN LEVEL									
	UP LEVEL									
	DOWN LEVEL									

PART NO.

SPECIAL DRIVING RULES:_____

REF. CKT. SPEC. P/N | E.C. | DATE

FIGURE 30

Sample flyer:

IBM CIRCUIT FLYER

PART NO.

BLOCK ID. ANNAA

TITLE (SAMPLE) AI-UNLOADED

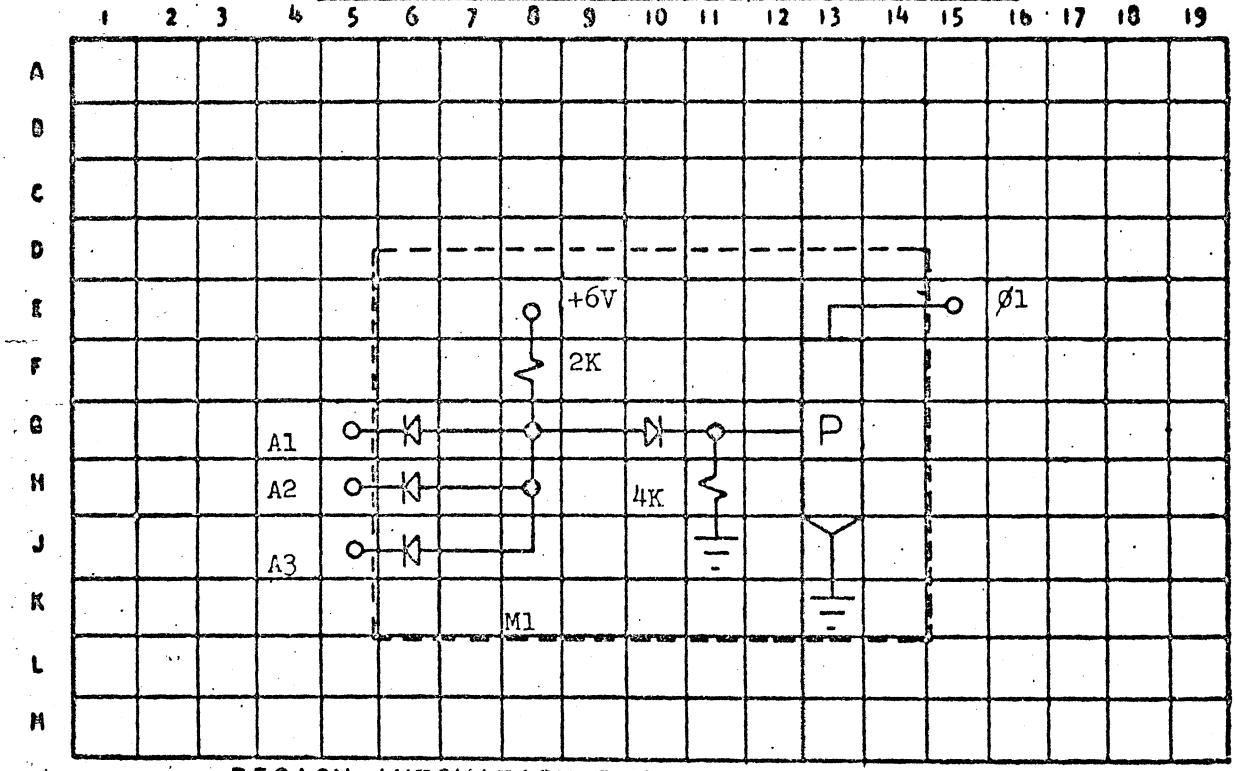
PAGE NO. 1 of 2

BLOCK CLASS Experimental CONTROL CODE ED

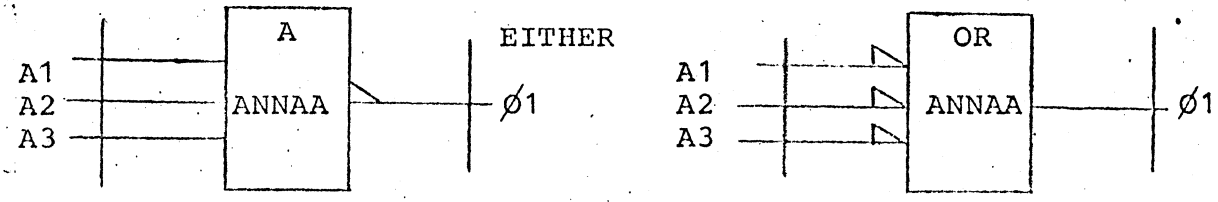
BLOCK STATUS * GROUPING NONE

PACKAGING M1 = SLT Module P/N 361451

SAMPLE FLYER



DESIGN AUTOMATION BLOCK REPRESENTATION



PART NO.

REF.CAT.SPEC.P/N		E.C.	DATE	E.C.	DATE
MADE BY	ORIG.APP.				
[illegible]	REL APP.				
D.A.APP.	T.E.APP.				

FIGURE 31

IBM CIRCUIT FLYER

PART NO.

BLOCK ID. ANNAA

SRETL-XXX | TITLE AI-UNLOADED

PAGE NO. 2 of 2

--------SAMPLE FLYER--------

CONTROL CODE ED

CKT NO. \ LOGIC FUN.	LOGIC FUNCTIONS																		DOT FUNCTIONS		
	NAND	NOR	AND	OR	INV	RES	NONT	OTHER	EXTEND	EVENE	ODDE	EVEN0	ODD0	OE	TH	THX	ORC	INVC	AND	OR	NONE
ANNAA																					

DELAY PARAMETERS ☐ DOES NOT APPLY

A REALISTIC ESTIMATE OF MACHINE CIRCUIT SPEEDS SHOULD BE OBTAINED FROM THE LOCAL MACHINE TECHNOLOGY GROUP.

	DELAY USED BY SLDA	DELAY LIMITS 8" NET BC	8" NET WC	48" NET BC	48" NET WC
OUTPUT RISING					
OUTPUT FALLING					

"B" FACTOR X

LOAD CHECKING DATA ☐ (DA USE ONLY) DOES NOT APPLY

SPI		CPL	CT	MAXIMUM VOLTAGE (VOLTS)	MINIMUM VOLTAGE (VOLTS)	AVAILABLE SOURCE CURRENT (MA)	MINIMUM SOURCE CURRENT (MA)	MAXIMUM LOAD CURRENT (MA)	MINIMUM LOAD CURRENT (MA)	DOT COUNT
A1	UP LEVEL	U	L	+12.48				2.Ø	Ø	5
					+1.3			2.5	Ø	
	DOWN LEVEL		L		+Ø.28			+2.33	+1.5	5
				+Ø.14				+2.4	+1.6	
A1	UP LEVEL	U	L	+12.48				2.Ø	Ø	5
					+Ø.29			3.Ø	Ø	
	DOWN LEVEL		W		+Ø.28	-19.Ø	Ø			5
				+Ø.14		Ø	Ø			
	UP LEVEL									
	DOWN LEVEL									
	UP LEVEL									
	DOWN LEVEL									
	UP LEVEL									
	DOWN LEVEL									

PART NO.

SPECIAL DRIVING RULES:

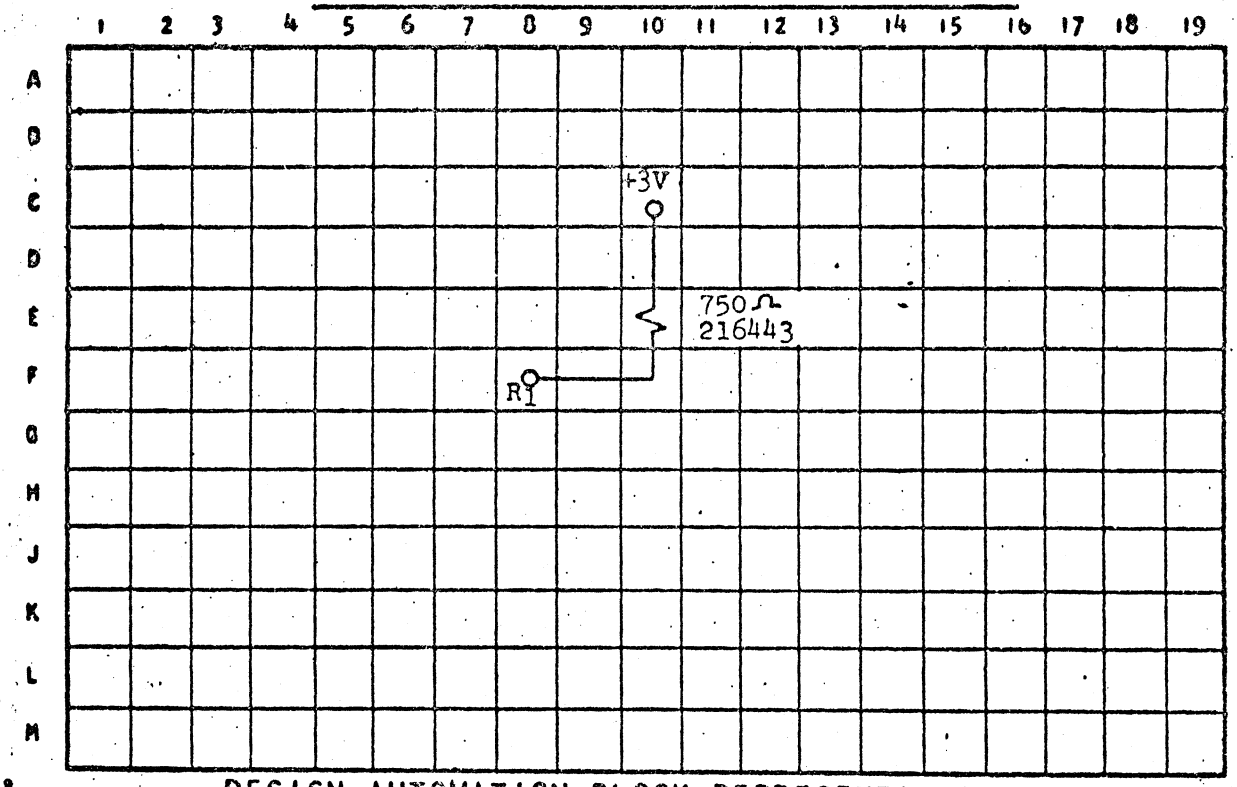
FSP. CIT. SPEC. P/N | E.C. | DATE

FIGURE 32

IBM CIRCUIT FLYER	PART NO.
	BLOCK ID. ANNAA
SRETL-XXX TITLE (SAMPLE) RESISTOR	PAGE NO. 1 of 2

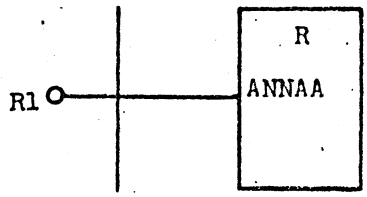
BLOCK CLASS EXPERIMENTAL CONTROL CODE ED
BLOCK STATUS * GROUPING NONE
PACKAGING

SAMPLE FLYER



PART NO.

DESIGN AUTOMATION BLOCK REPRESENTATION



REF.CAT.SPEC.P/N		E.C.	DATE	E.C.	DATE
MADE BY	ORIG.APP.				
ENGR.APP.	RES APP.				
DA.APP.	T.E.APP.				

FIGURE 33

IBM CIRCUIT FLYER

PART NO.
PACK NO. ANNAA

SRETL-XXX | TITLE RESISTOR | PAGE NO. 2 OF 2

----------SAMPLE FLYER---------- | CONTROL CODE ED

LOGIC FUN. / CKT NO.	LOGIC FUNCTIONS: NAND	NOR	AND	OR	INV	RES	NONT	OTHER	EXTEND	EVEN E	ODD E	EVEN O	ODD O	OE	YH	THT	ORE	XOVF	EXT FUNCTIONS: AND	OR	NONE
ANNAA																					

	DELAY USED BY SLDA	DELAY LIMITS 0" NET BC	0" NET WC	45" NET BC	45" NET WC
OUTPUT RISING					
OUTPUT FALLING					

"B" FACTOR X

DELAY PARAMETERS ☐ DOES NOT APPLY

A REALISTIC ESTIMATE OF MACHINE CIRCUIT SPEED SHOULD BE OBTAINED FROM THE LOCAL MACHINE TECHNOLOGY GROUP.

LOAD CHECKING DATA ☐ (DA USE ONLY) DOES NOT APPLY

SPI		CPL	CT	MAXIMUM VOLTAGE (VOLTS)	MINIMUM VOLTAGE (VOLTS)	AVAILABLE SOURCE CURRENT (MA)	MINIMUM SOURCE CURRENT (MA)	MAXIMUM LOAD CURRENT (MA)	MINIMUM LOAD CURRENT (MA)	USED
R	UP LEVEL	C	A	+3.12		0	0			
	DOWN LEVEL		L		+0.28	+3.3	+3.3			
				+0.14				+3.04	+3.3	
								+4.16	+3.46	
	UP LEVEL									
	DOWN LEVEL									
	UP LEVEL									
	DOWN LEVEL									
	UP LEVEL									
	DOWN LEVEL									
	UP LEVEL									
	DOWN LEVEL									

PART NO.

SPECIAL DRIVING RULES:

REF. CKT. SPEC. I/N | C.C. | DATE

FIGURE 34

1.0 GENERAL

1.1 Experimental, Controlled, and Formal release circuit flyers, will be approved, released, and distributed throughout the Corporation.

1.2 Where the necessary facilities (i.e. approvals, drafting) do not exist or are temporarily not established, the Corporate Flyer Group, Dept. 707, E. Fishkill, will provide the lacking services.

1.3 All controlled and formal release circuit flyers will be processed and distributed by Dept. 707, E. Fishkill.

1.4 A duplication check against existing circuitry should be made at all levels. This duplication check is the responsibility of the local areas and must be completed before release.

1.5 No circuit flyer may ever be assigned a higher classification or status than the lowest level component part number it carries. All component parts must be brought up to the requested flyer level before the circuit flyer will be processed or distributed.

2.0 EXPERIMENTAL RELEASE

Flyers in this category do not require a Circuit Specification.

3.0 CONTROLLED RELEASE

Flyers in this category require a "Reference Circuit Specification Part Number" and a complete Circuit Specification released prior to release of the affected cards.

4.0 FORMAL RELEASE

Same as applies to Controlled Release.

5.0 RESPONSIBILITIES

See Section 28.

1.0 GENERAL

1.1 Changes to Experimental, Controlled and Formal release circuit flyers will be approved and distributed throughout the Corporation.

1.2 Where the necessary facilities (i.e. approvals) do not exist or are temporarily not established, the Corporate Flyer Group, Dept. 707, E. Fishkill will provide the lacking services.

1.3 All controlled and formal release circuit flyers will be processed and distributed by Dept. 707, E. Fishkill.

1.4 A duplication check should be made against existing circuitry on all changes.

1.5 New users of existing circuit flyers must establish maintenance as users in order to be consulted for Engineering Change (EC) concurrance.

2.0 EXPERIMENTAL RELEASE

2.1 Early notification must be made to all users of Experimental flyers.

2.2 Originator of the flyer has control and all requests for change must be made through him.

3.0 CONTROLLED RELEASE

3.1 Early notification must be made to all users of Controlled Released flyers.

3.2 Changes must be made through the responsible circuit technology area.

4.0 FORMAL RELEASE

4.1 Concurrance must be obtained from all users of Formal Released flyers in released programs.

4.2 Early notification must be made to all users of flyers in this category in Development programs.

4.3 Changes must be made only through the area maintaining engineering control.

5.0 OBSOLETING FORMAL AND CONTROLLED RELEASED CIRCUIT FLYERS

5.1 Brownlines of all pages must be included and should show the change in EC number.

5.2 The Class and Status categories should be changed as follows:

5.3 Class - Remains the same.
Status - Remove this item and replace with "OBSOLETE".

5.4 The history sheet should indicate that the purpose of the change is to obsolete the document.

5.5 The word "OBSOLETE" must be indicated in minimum 1/4 inch letters on the upper grid of page 1.

6.0 TRANSFER OF CONTROL CODE OF CIRCUIT DOCUMENTS

6.1 FORMS REQUIRED

1. CD Engineering Work Request (DEP 2-6230-2, Section 28, Figure 1)
2. Brownline or Vellum of Circuit Document

6.2 INFORMATION REQUIRED

1. Control Code making transfer
2. Control Code receiving transfer
3. Individual making transfer
4. Individual receiving transfer
5. Date of transfer
6. List all part numbers and/or block ID's of circuit documents.

6.3 THE CONTROL CODE receiving the transfer must submit the work request and circuit documents affected with the above information.

6.4 In order to keep the documents and automated records up-to-date these changes should be made.

6.5 CIRCUIT DOCUMENTATION, DEPARTMENT 707 is responsible for the processing of these changes.

1.0 MACHINE TECHNOLOGY, SOLID STATE MEMORY CIRCUIT DEVELOPMENT, AND CIRCUIT ENGINEERING LOGIC DEVELOPMENT

1.1 Perform duplication check with existing circuitry when a new request is initiated for a new design or change.

1.2 Originate circuit designs and specifications.

1.3 Provide in appropriate format all data required for input to the Local Flyer Group or Corporate Flyer Group.

1.4 WHEN INPUT IS TO LOCAL FLYER GROUP - Location procedures prevail on determination of input format and type of information provided. However, output of the Flyer Group must conform to all requirements discussed in other sections of this instruction.

1.5 WHEN INPUT IS DIRECT TO CORPORATE FLYER GROUP

1.5.1 For Release Only Processing - by Dept. 707, E. Fishkill documentation must be completely in accordance with all ground rules described in this instruction for acceptance.

1.5.2 For Full Processing - by Dept. 707, E. Fishkill, new documents may be hand drawn using pencil. Hand drawn input must be submitted on reproducible copies of the proper form. No input will be accepted unless accompanied by an Engineering Work Request (Figure 1).

1.5.3 A component check must be made as to realistic validity and availability. (Refer to "Restricted Parts Listing" or EXPRESS published by Dept. 375, E. Fishkill).

1.5.4 All approvals must be obtained locally, unless the function is not available at the local level and will be provided by the Corporate Flyer Group.

2.0 LOCAL FLYER GROUP

2.1 Will provide a service to the local circuit design groups by furnishing all records functions, coordination, and finalized drafting of circuit flyers and circuit specifications.

2.2 Will assure that all Circuit Flyer Ground Rules contained in this instruction have been satisfied and that good quality documents are prepared.

2.3 Assure that all required local approvals are obtained, for example, D/A, Field Engineering, Test Engineering, etc.

2.4 Perform a components check as to realistic validity and availability. (Refer to EXPRESS or "Restricted Parts Listing" published by Dept. 375, E. Fishkill).

2.5 This Corporate Practice is not intended to dictate local procedures. The "Local Flyer Group" and its functions are only a suggested means of implementing the system.

3.0 FIELD ENGINEERING (RELIABILITY AND SERVICEABILITY)

3.1 Will provide any new requirements for function symbology.

3.2 Will approve all flyers for adherence to the established standard symbology.

4.0 DESIGN AUTOMATION

Will approve all flyers for format compatibility with Design Automation programs.

5.0 MANUFACTURING TEST ENGINEERING

5.1 Will approve all circuit flyers (see Section 25).

5.2 Will provide as Manufacturing documentation all flyer breakdown beyond Field Engineering symbology, required as input for the Test Engineering EDITOR program.

5.3 All local Flyer Groups will be provided with Test Engineering services on location. All other locations can obtain consultation services from the Test Engineer in the Corporate Flyer Group.

6.0 CORPORATE FLYER GROUP (Dept. 707, E. Fishkill)

6.1 Responsible for Corporate Flyer Ground Rules.

6.2 Final approval on all flyer activity where deviation from ground rules is involved.

6.3 Provide release and other assistance to locations not having the facilities.

6.4 Publish required listings on circuit flyers for Where Used and duplication checks.

IBM

COMPONENT ENGINEERING WORK REQUEST FOR CIRCUIT DOCUMENTATION

INVESTIGATED BY:	APPROVED BY:		DATE:		ACCOUNT NO.	IPT/ICA NO.	E.C. NO.
Thomas Jones	John Smith		June 20, 1970		1234-54321-213-123	654321	
TO: C. Reitano	DEPT. 707	DIV. CD	LOCATION East Fishkill		USER APPROVAL: OBTAINED: [X] NOT REQUIRED: [ ]	CIRCUIT FAMILY SRETL-Gen	MACHINE TYPE B150
FROM: John Block	DEPT. 123	DIV. SDD	PHONE 6543	LOCATION Kingston		MANAGER APPROVAL: John Geman	

REASON FOR CHANGE:

To change the part number of the capacitor to maintain a more stable oscillator

Circuit Flyer S22GG 873456

Circuit Spec. 875432

FOR DEPARTMENT 707 USE ONLY

BLOCK ID	PART NUMBER	DATE REC'D	WORK REQUEST	APPROVALS:	TO	FROM	COPY: CHECK
				TE			
		COMPONENT CHECK		FE			
				DRAFTING: DEPT. 707	TO	FROM	CHARGE CODE
		DA APPR. COMPLET. CK.		VIS			DISTRIBUTION:
EXPRESS INFO.	HOLD ON____ OFF____	TO ORIGINATOR FOR PROOF READ		REDRAFTING: DEPT. 707	TO	FROM	ADVANCE ____
				VIS			DECK 9 ____
							DECK 22 ____

REMARKS

M30-2605-0

COMPLETED EXAMPLE
WORK SHEET FOR CIRCUIT DOCUMENTATION

RESPONSIBILITIES

CARD GROUND RULES

SECTION 28 Cat. DEP 2-6230 Subject 2 Suffix

Date

Page 3 of 3

June 19, 1967
Endicott - Components Division

146
4376

Reed Relays on SLT Cards

Sent for information only as you have no cards that are affected.

W. Brodbeck
R. Burdett
T. A. Christenson
W. L. Clayton
L. I. Fowx
W. A. Klein
J. R. Krzyzewski
H. Lalo
W. H. Laman
J. D. Martin
P. E. McGuire
C. R. Nicoll
R. E. Paulsen
W. J. Richardson
P. H. Slater
C. Th. Steenstra
S. M. Symons
H. O. Wangberg

We have experienced several problems during the past in building SLT cards which contain reed relays. Requests to you for ECs against these cards have not been made previously as it was the intent to have only one EC combining all changes processed per card. To the best of our knowledge these problems are identified and the solutions now proven.

The problems are outlined below as well as the solutions.

Reed lead shorting during testing:

Since the reed lead was lengthened to solve a reed manufacturing problem a secondary operation has been required prior to card testing. This operation shortens the leads of the relays that are mounted on Y24 grid. A shorting condition or physical damage occurred with the tester handling mechanism. The tester could not be changed as the card clamp material thickness cannot be made thinner.

Attached is a print of each card requiring relayout (sent to controlling location)showing new relay locations. Other relays on these cards have been relocated to allow for possible future increase in coil bobbin size.

An update to the ground rules is in process and changes the grid location to Y26 as being the lower limit. The 1 high card is unsuitable for reed relays. There are only two (2) 1 high cards released, i.e., 5800744 which has no forecasted usage and 5801222 which cannot be changed.

Contact change:

The contact was changed to allow better relay retention and alignment for insertion in the card. These improvements require card changes for hole size, contact part number and spec. The following BA, BB and FN note codes action is required:

BA

Remove - "BA note - Drill .069 ± .001 at locations, etc."

Change to - Convert all of the X-Y locations in the BA note to "L" holes.

BB

Change to - "Drill .062 ± .002 after plating with location tolerance of ± .005 at locations, etc."

FN

Remove - "FN note - contacts 483316 to be inserted before liquid process per Eng. Spec. 892058, reed relay assembly to be hand mounted on contacts after liquid process."

Change to "FN note - Contacts 815198 to be inserted before liquid process per Eng. Spec. 871183, reed relay assembly to be hand mounted on contacts after liquid process."

Reed relay part number change:

A change was made to improve reed life and control was obtained by a part number change. The attached relay conversion listing is to be used for making the substitutions in the card B/Ms and the circuit flyers.

The actual conversion should be thoroughly validated in each case to assure technical compatibility.

For your respective locations you will find attached a listing of card assembly numbers with the relays used. Based on Endicott forecast and production records, we have identified on this listing those cards which have either no forecasted usage or very low usage. Please validate this information with your local system groups as ECs to these cards may not be justified. Submit a request to obsolete where applicable.

We have been maintaining production on an off-specification basis but this condition is not very good in an automated environment. I have no solution to the funding problem except that the group having technical control should support the EC. In processing the card ECs please include any other items which may be in suspense.

A schedule on when the ECs would be processed would be appreciated.

D. F. Cole, Manager
Packaging Release Eng.

DFC/my
Attachments
cc: N. G. Jones

CONVERSION LISTING
REED RELAY

Diffused Switch 765 Series Old	Race Switch 766 Series New	Tin-Nickel 766 Series New
765617 *	766035	766244
765619 ***	766036 *	766245
765623 *	766037 *	766246
765625 ***	766038 *	766247
765634 *	766039	766248
765654 ***	766040 *	766249
765655 ***	766041 *	766250
765664	766042	
765665 ***	766043 *	766252
765666 ***	766044 *	
765667	766045	
765668 ***	766046 *	
765669 *	766047 *	
765670 *	766048	
765671 ***	766049 *	
765672 *	766050	
765673 *	766051 *	
765683 *	766052	
765689 *	766053 *	
765690	766054	
765691	766055 *	
765692 *	766056 *	
765694 *	766057 *	
765859 *	766058 *	
765704 *	766059 *	
765706 ***	766060 *	
765733 **	766061	

Legend:

* -SMS
** -SLT
*** -SMS and SLT

CONVERSION LISTING
REED RELAY

765 Series Old	766 Series New
765743 *	766064
765719 *	766065
765696	766066
765702 *	766067
765717 *	766068 *
765718 *	766069 *
765698 *	766070
765700 ***	766071
765721 **	766072 *
765722 **	766073 *
765724	766074
765725	766075
765726	766076 *
765728	766077
765729	766078
765815	766079
765816 ***	766080
765818	766081
765819	766082
765820	766083
765821	766084
765822	766085
765825 *	766086
765832	766087 *
767036 *	766088
765901 **	
765973 ***	
765974 **	
766009	
767513	
767515	
766013	

Legend:

* - SMS
** - SLT
*** - SMS and SLT

NGJ/my
2/8/91 6/15/67

IBM Division
Engineering Practice

SUPPLEMENT OF STATUS

EFFECTIVE DATE: 4/24/69

SUBJECT: Card Layout Ground Rule Status; Suffix 3, Section 10.

This section has been updated to include the new SLT, SLD and MST module schematics.

Sections 10B, 10C, 10D and 10E are new sections.

SCOPE

This section includes the Module information as indicated below and defined in the following sub-sections.

Section	Section Title
10A	SLT/SLD/MST Modules - Ground Rules
10B	SLT, SLD and MST Module Schematic Index
10C	SLT Module Schematics
10D	SLD Module Schematics
10E	MST 1, 2 and 4 Module Schematics

IBM Division
Engineering Practice

Effective Date:

Subject: Card layout ground rule status suffix 3 section 10A.

This section has been updated to include the module requirements for SLD and MST. The schematic section that was previously included with this section will be updated at a later date under Suffix 3, Section 10B.

This update supersedes DEP 2-7047, Suffix 3, Section 10, dated 8/1/66 and book 03-10, DEP 2-6420-530, Pages 2 and 3 under circuits.

Package

The physical outlines for the MST Modules have been added. The lead codes for CMT coding have been added.

Requirements

CMT size code added. Hole size requirements defined for MST.

Limits

Expanded to include the five (5) MST card sizes.

Hand Assembly

Modules used on MST-4 card assemblies will be hand assembled.

Process Information

Updated to reflect the new high speed insertion equipment for 1 hi 6 card assemblies.

DESCRIPTION

SLT modules* have 12 or 16 leads. They are encased in an electricall flcating metal case with pinched standoffs on corner leads 1, 4, 7, and 10. Modules must be considered as being encased in an uninsulate metal case, except when next to another SLT module, and may contain a variety of electrical components. The leads are mechanically secured to the substrate and then potted during fabrication of the module itself.

Assembly drawing code is "Z for Modules or ZM for I/C Modules".

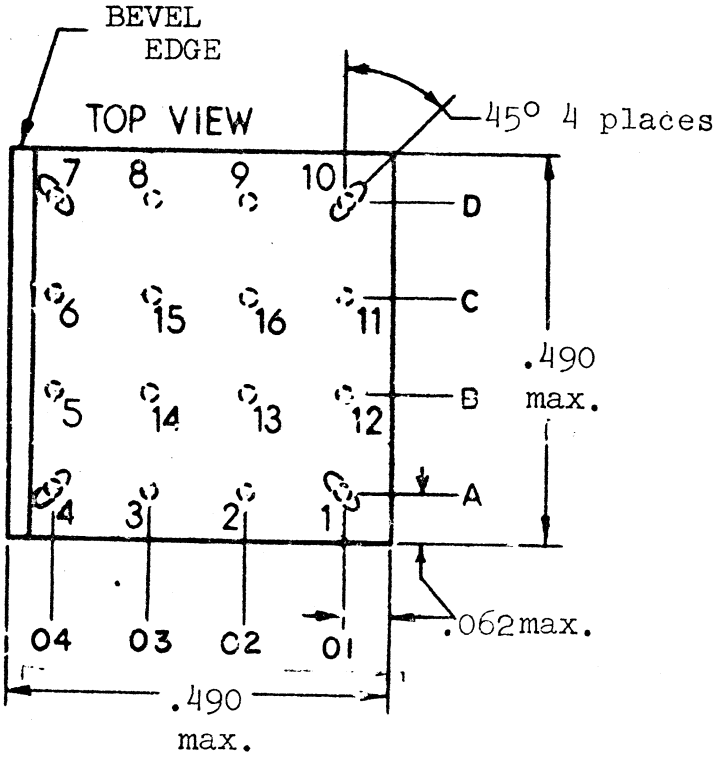
* The term SLT Module is used throughout this section to denote a physical form factor and not a module technology.

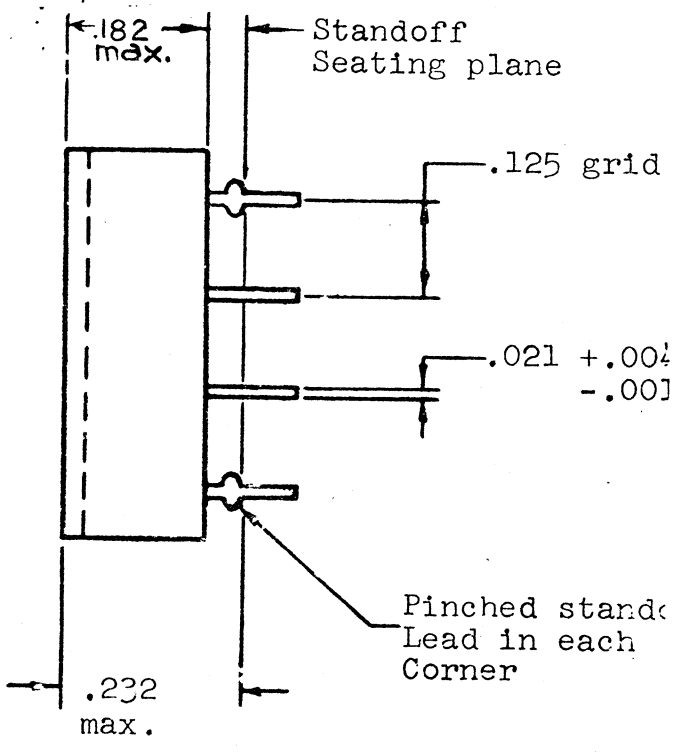
PACKAGE

The following physical outlines are machine insertable.

SLT,SLD	7M906C5 - 16 leads	MST-1	865707 - 16 leads
SLT	7M906B4 - 12 leads	MST-2	865707 - 16 leads
SLT	7M906H2 - 16 leads		

MST-4: Physical outline 873642 (s level) is not machine insertable.





PACKAGE (cont'd)

Lead number 1 or A01 will be identified by the figure "1" being printed on the top of the can directly over the top of that lead. For mechanical orientation a bevel is along the can edge by lead numbers 4, 5, 6, and 7. Views shown are for layout purposes only and the part drawing shall have precedence.

REQUIREMENTS

There are no note codes associated with this part.

Module leads must be mounted in:

"J (.040)" holes for SLT & SLD
".040" holes for MST 1 and 2
".031" holes for MST 4
"W (.031)" holes for the four corner leads for MST 4 modules mounted on SLT cards.

For CMT coding the size will be 4x4 and the leads will be coded for the "A" orientation as shown under package. The "A" orientation is the only allowable orientation for modules used on MST cards.

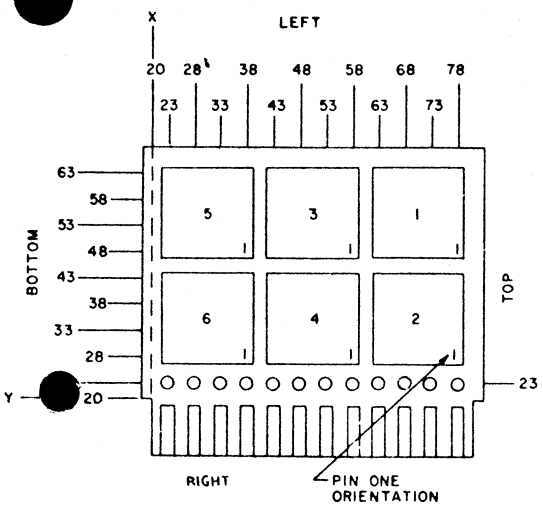
LIMITS

All SLT module leads must be on or within the following X and Y grid locati

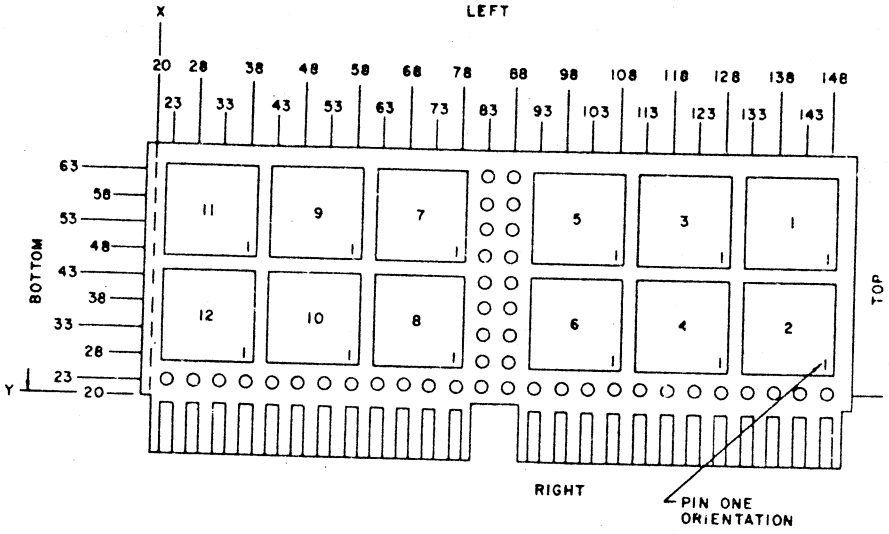
SLT, SLD:	1 Hi 6 - 12	X 23 - 78 - 148	Y 23 - 63
	2 Hi 6 - 12	X 23 - 78 - 148	Y 23 - 123
	3 Hi 12	X 23 - 148	Y 23 - 183
MST:	2 Hi 1,2&4 wide	X 01 - 12 - 26 - 54	Y C - W
	3 Hi 2&4 wide	X 01 - 26 - 54	Y C - 9

The preferred layout for modules on SLT cards is shown in the following illustrations. This is for the high speed inserter (SlCM) requiring modules to be located in this fixed position and fixed orientation.

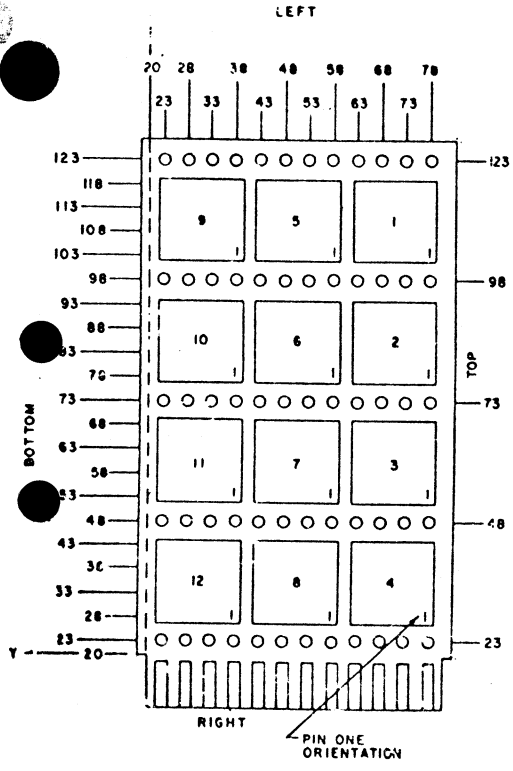
LIMITS (cont'd)



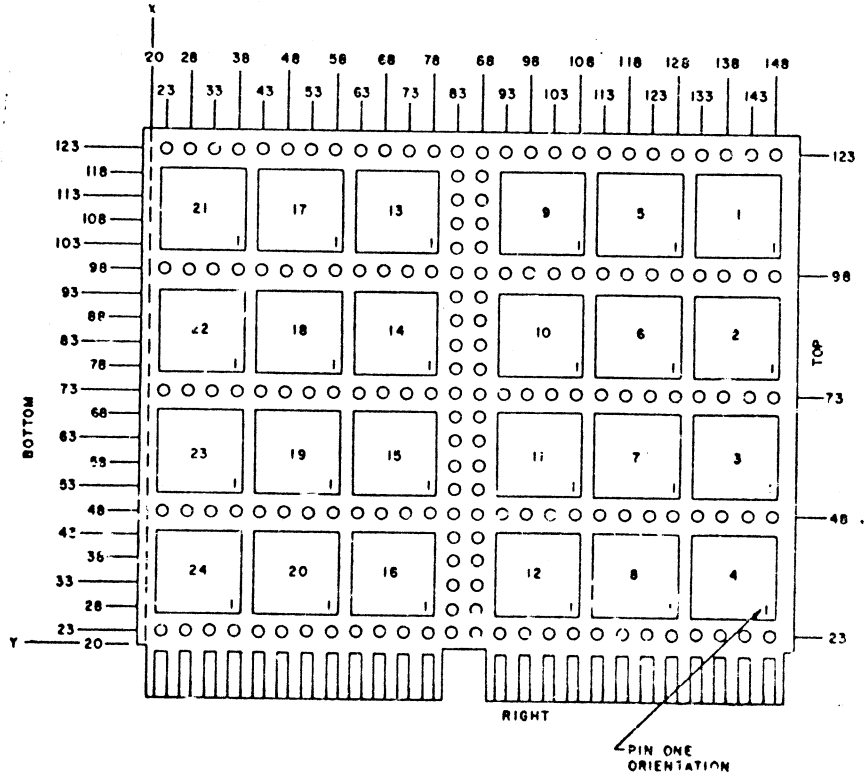
1 Hi 6



1 Hi 12



2 Hi 6



2 Hi 12

LIMITS (continued)

3 Hi 12 cards module placement is the same as the 2 Hi 12 except for the added module positions on Y grids 128 and 153.

Modules that are not on X - Y grid locations ending with digit 3 or 8 will be manually assembled.

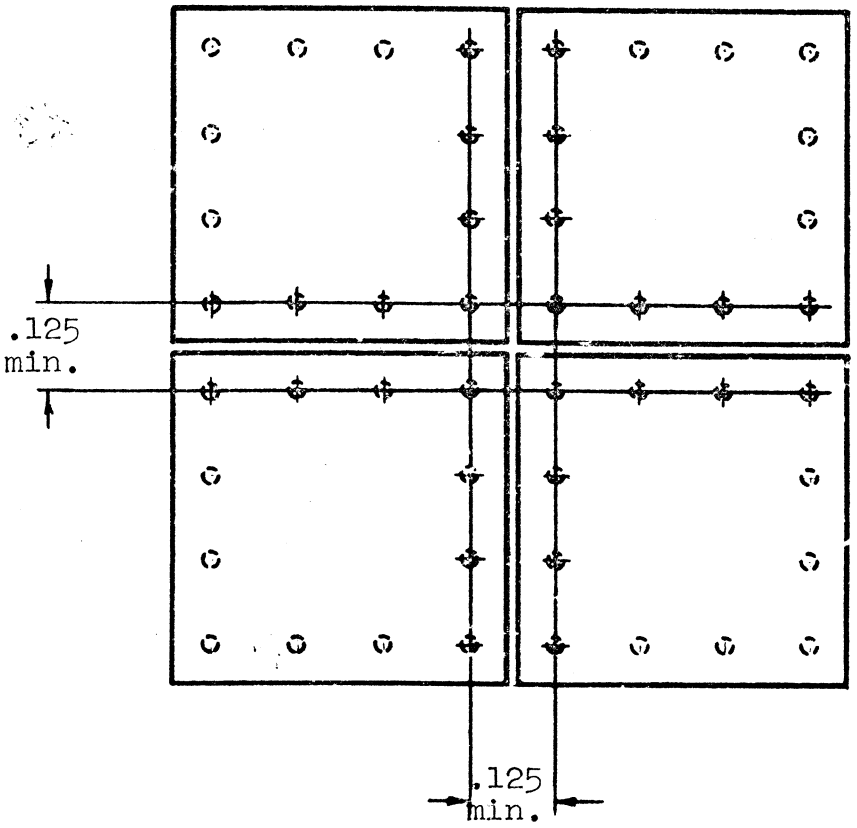
The preferred layouts for modules used on MST cards are defined in the following documents:

MST 1 - DEP 2-6420-540
MST 2 - DEP 2-6420-542
MST 4 - DEP 2-6420-544

RELATIONSHIP

The following illustration shows the physical minimum placement of the SLT modules.

TOP VIEW



ARTWORKS

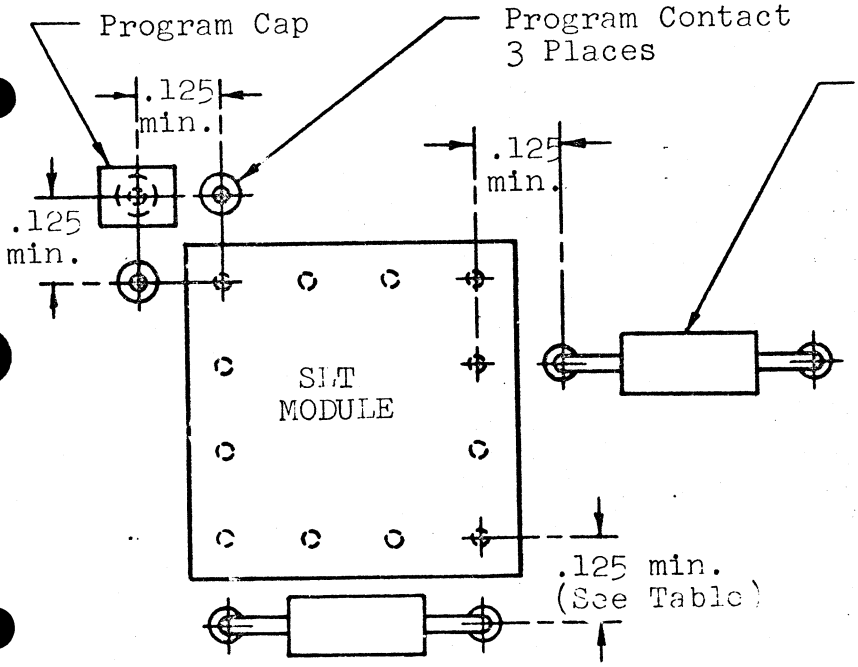
No restrictions apply to this component.

SEQUENCE EFFECT

The following illustration shows the physical relationship between SLT modules

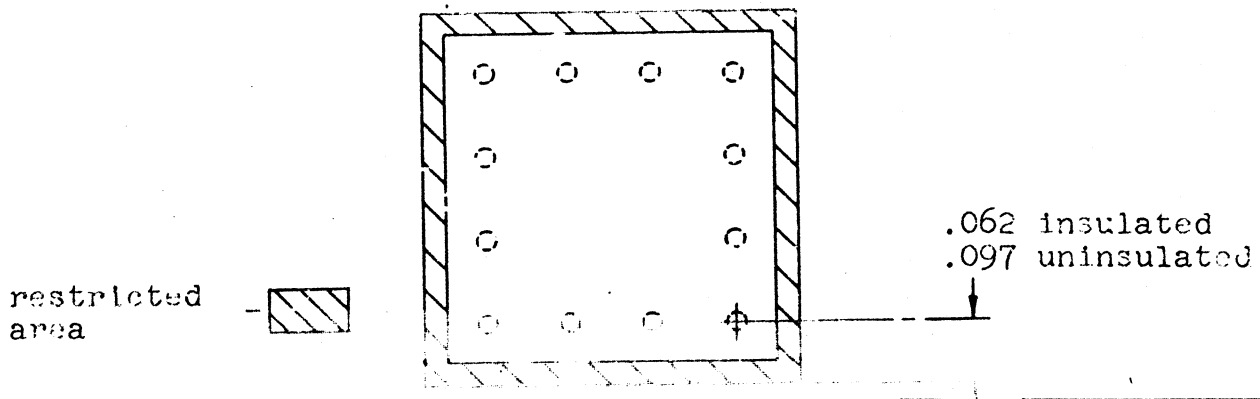
a. Tubular axial leaded components up to .230 DIA.
b. Program contact.
c. Other components up to .230 high.

TOP VIEW



Hole Spacing	Max. Body Diameter
.125	.125
.150	.175
.175	.225
.200	.230

The following illustration shows the physical relationship to all other components.



HAND ASSEMBLY

Layout will never reflect hand assembly of this part, but this part will be manually assembled if the leads are not on the standard .125 grid pattern.

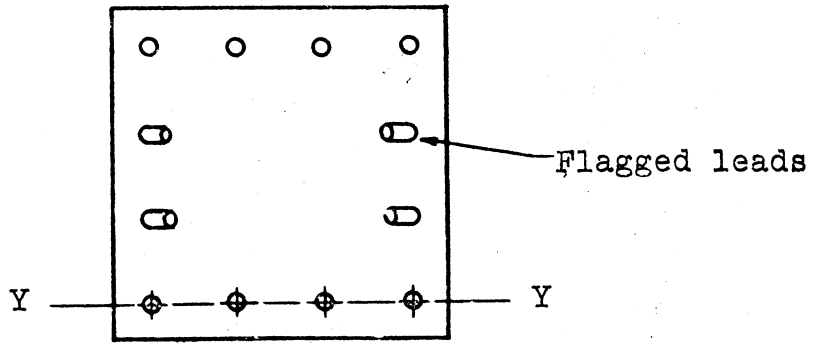
All modules are hand assembled on MST 4 card assemblies using double-sided tape and the leads are not flagged.

PROCESS INFORMATION

The SICM (Simultaneous Insertion Circuit Module) I and II machines are high speed insertion equipment using gravity feed and requiring fixed orientation of the 6 to 12 modules. The modules are inserted and clinched during one cycle. The SICM machines are capable of handling high volume modular 1 Hi 6 and 2 Hi 6 card assemblies.

Another type of assembly machine (gang clincher) only requires that module leads be on X - Y grid locations that end with digit 3 or 8 or its equivalent. Modules may be oriented in any four quadrants, but the preferred orientation is the same as the high speed inserter. The orientation of the modules should be the same on any one card assembly.

Two or more opposite leads will be flagged to secure the module to the card.



BOTTOM VIEW

PLANNING

Semi-automatic equipment for modules with leads not located on the .125 standard grid pattern is not contemplated.

IBM Division Engineering Practice

SLT, SLD AND MST
MODULE SCHEMATIC INDEX

Schematics in Sections 10C, 10D and 10E are for packaging layout purposes only and the module part schematic will have precedence.

MODULE PART NUMBER	FAMILY	SECTION	PAGE
361404	SLT 5NS	10C	5
361405	SLT 5NS	10C	5
361406	SLT 5NS	10C	5
361407	SLT 5NS	10C	5
361408	SLT 5NS	10C	5
361409	SLT 5NS	10C	5
361410	SLT 5NS	10C	5
361412	SLT 5NS	10C	9
361413	SLT 5NS	10C	9
361414	SLT 5NS	10C	1
361415	SLT 700NS	10C	8
361416	SLD 700NS	10D	10
361417	SLD 700NS	10D	10
361418	SLD 700NS	10D	10
361419	SLD 700NS	10D	10
361420	SLD 700NS	10D	8
361421	SLD 700NS	10D	8
361422	SLD 700NS	10D	8
361423	SLT SPECIAL	10C	3
361424	SLT SPECIAL	10C	3
361426	SLT SPECIAL	10C	3
361427	SLT 30NS	10C	6
361428	SLT SPECIAL	10C	2
361429	SLT 30NS	10C	6
361430	SLT SPECIAL	10C	3
361431	SLT 30NS	10C	6
361432	SLT SPECIAL	10C	3
361433	SLT 30NS	10C	6
361434	SLT SPECIAL	10C	3
361435	SLT 30NS	10C	6
361436	SLT 700NS	10C	8
361437	SLT 30NS	10C	6
361438	SLT 30NS	10C	6
361439	SLT SPECIAL	10C	3
361440	SLD 100NS	10D	11
361441	SLD 100NS	10D	11
361442	SLD 100NS	10D	11
361443	SLD 100NS	10D	11
361444	SLD 100NS	10D	9
361445	SLT 700NS	10C	8
361446	SLT 700NS	10C	8
361447	SLT 5NS	10C	1
361448	SLD 30NS	10D	7

SLT, SLD AND MST
MODULE SCHEMATIC INDEX

MODULE PART NUMBER	FAMILY	SECTION	PAGE
361449	SLD 30NS	10D	7
361450	SLD 30NS	10D	4
361451	SLT 30NS	10C	6
361452	SLD 100NS	10D	9
361453	SLT 30NS	10C	6
361454	SLT 30NS	10C	6
361455	SLT 30NS	10C	6
361456	SLT 30NS	10C	4
361457	SLT 30NS	10C	4
361458	SLD 100NS	10D	9
361459	SLT 30NS	10C	4
361468	SLT 5NS	10C	1
361469	SLT 5NS	10C	1
361472	SLT SPECIAL	10C	9
361473	SLT 30NS	10C	4
361475	SLT 30NS	10C	4
361476	SLT 30NS	10C	4
361477	SLT 30NS	10C	4
361479	SLT 30NS	10C	4
361480	SLT 5NS	10C	1
361481	SLT 30NS	10C	4
361482	SLT 5NS	10C	1
361485	SLT 30NS	10C	4
361486	SLT 30NS	10C	4
361487	SLT SPECIAL	10C	2
361488	SLT SPECIAL	10C	8
361489	SLT 700NS	10C	7
361490	SLD 700NS	10D	6
361491	SLT 700NS	10C	7
361492	SLT 700NS	10C	7
361493	SLT 700NS	10C	7
361494	SLT 700NS	10C	7
361495	SLT 700NS	10C	7
361496	SLT 700NS	10C	7
361497	SLT 700NS	10C	7
361499	SLT 700NS	10C	7
361594	SLD 30NS	10D	2
361595	SLD 30NS	10D	5
361596	SLD 30NS	10D	2
361597	SLD 30NS	10D	3
361598	SLD 30NS	10D	6
2391218	SLT SPECIAL	10C	2
2395053	SLT 30NS	10C	9
2395054	SLT 30NS	10C	9
2395055	SLT 30NS	10C	9
2395056	SLT 30NS	10C	9
2395057	SLT 30NS	10C	9
2395059	SLT 30NS	10C	9
2395079	SLT 30NS	10C	4
2395099	SLT 700NS	10C	10
2395112	SLD 30NS	10D	1

SLT, SLD AND MST
MODULE SCHEMATIC INDEX

CARD GROUND RULES	DEP	2-6230	3
SECTION 10B	Cat.	Subject	Suffix

MODULE PART NUMBER	FAMILY	SECTION	PAGE
2395113	SLD 30NS	10D	1
2395114	SLT SPECIAL	10C	2
2395124	SLT SPECIAL	10C	10
2395140	SLD 100NS	10D	3
2395144	SLT 30NS	10C	1
2395145	SLT 30NS	10C	1
2395147	SLT 700NS	10C	3
2395149	SLT 700NS	10C	2
2531620	MST 1	10E	16
2531622	MST 1	10E	13
2531627	MST 1	10E	8
2531629	MST 1	10E	8
2531631	MST 1	10E	12
2531634	MST 1	10E	17
2531647	MST 1	10E	13
2531670	MST 1	10E	18
2531671	MST 1	10E	1
2531672	MST 1	10E	12
2531673	MST 1	10E	11
2531674	MST 1	10E	7
2531698	MST SPECIAL	10E	7
2531699	MST SPECIAL	10E	15
2531701	MST 4	10E	19
2531706	MST 4	10E	4
2531708	MST 4	10E	17
2531716	MST 4	10E	17
2531726	MST 4	10E	17
2531728	MST 4	10E	9
2531830	MST 2	10E	18
2531832	MST 2	10E	5
2531837	MST 2	10E	2
2531840	MST 2	10E	14
2531843	MST 2	10E	10
2531847	MST 2	10E	20
2531849	MST 2	10E	11
2531851	MST 2	10E	11
2531855	MST 2	10E	13
2541621	MST 1	10E	11
2541623	MST 1	10E	14
2541625	MST 1	10E	16
2541630	MST 1	10E	20
2541632	MST 1	10E	19
2541646	MST 1	10E	20
2541649	MST 1	10E	19
2541702	MST 4	10E	19
2541704	MST 4	10E	4
2541709	MST 4	10E	8
2541711	MST 4	10E	1
2541712	MST 4	10E	14
2541714	MST 4	10E	1

SLT, SLD AND MST MODULE SCHEMATIC INDEX

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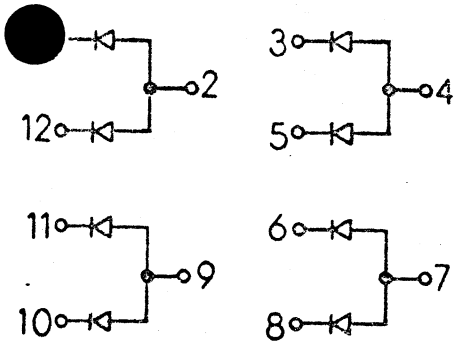

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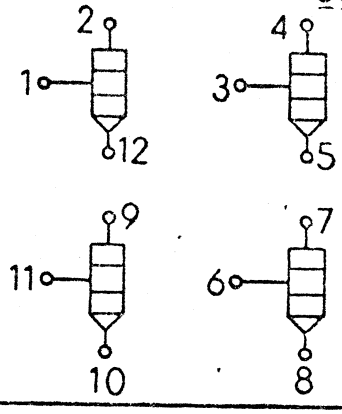

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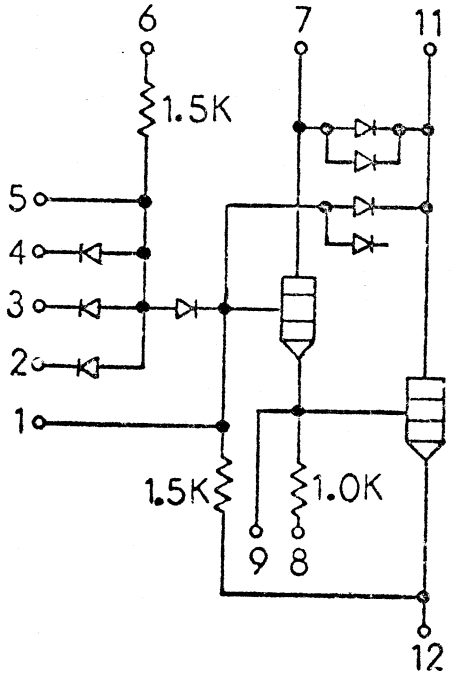

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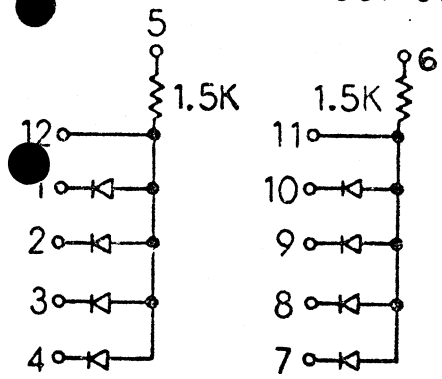

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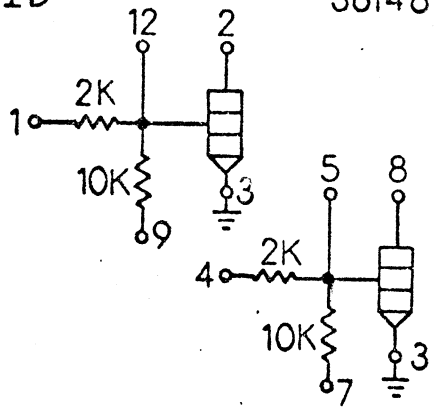

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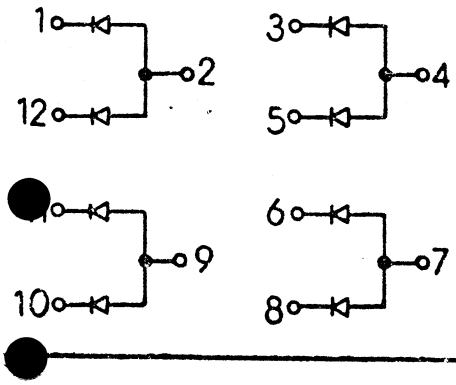

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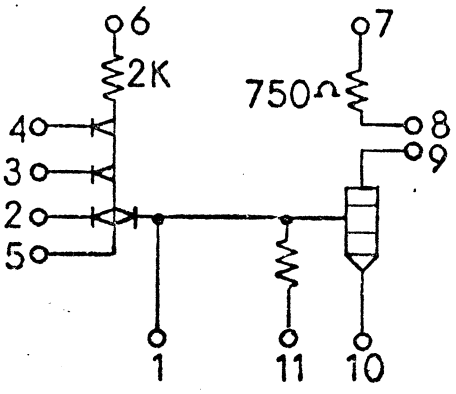

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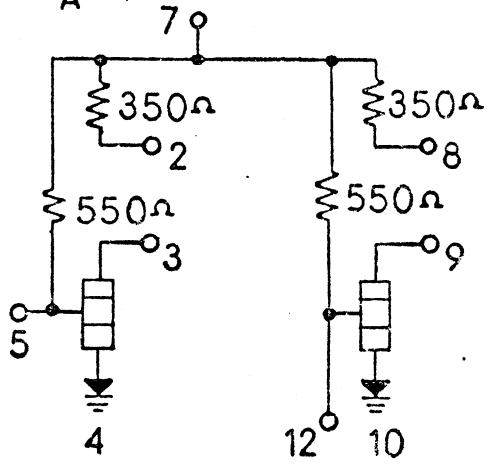
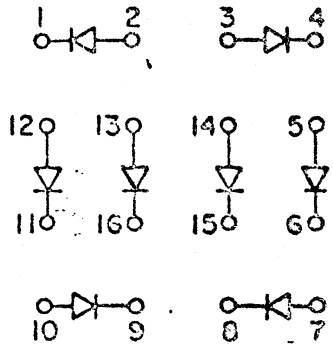
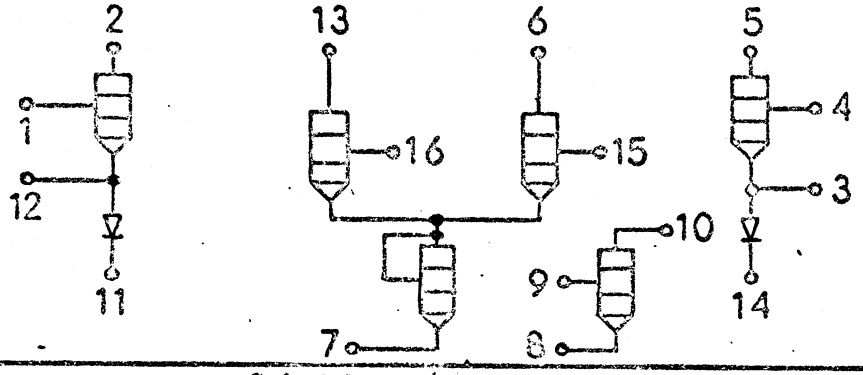


SLT MODULE SCHEMATICS

DIODE-SL 2391218



COMPARATOR 361487



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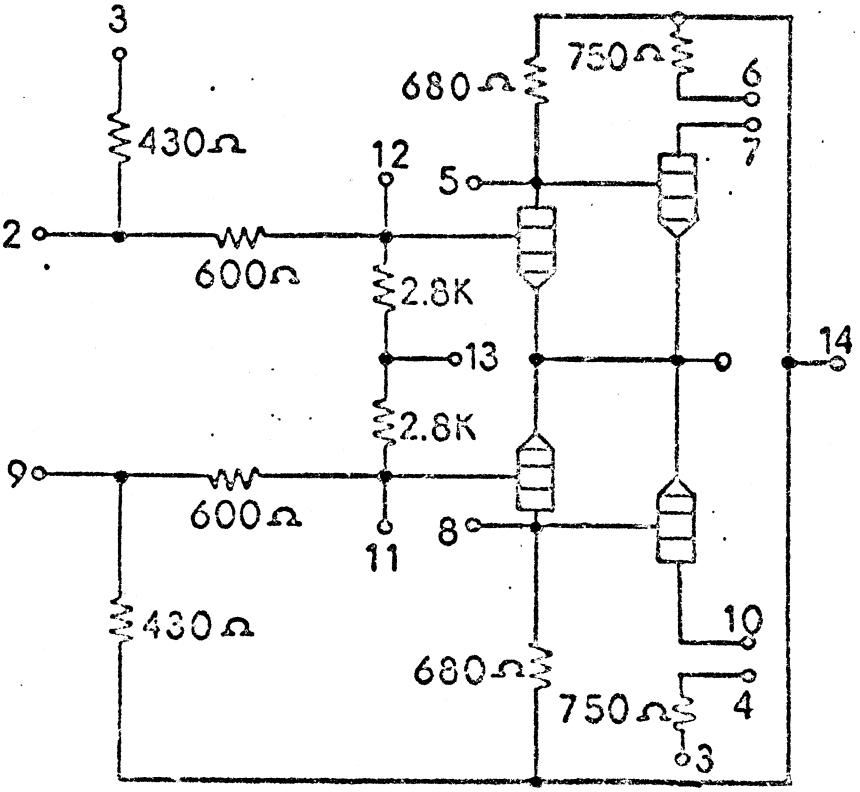

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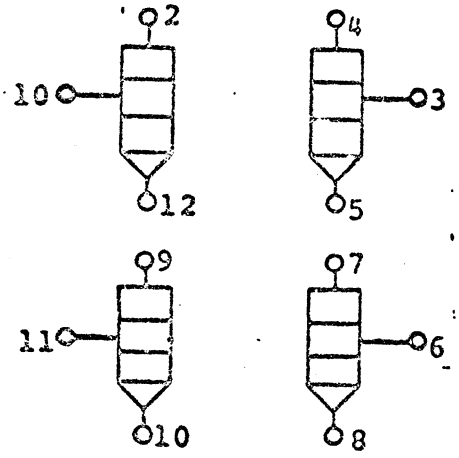

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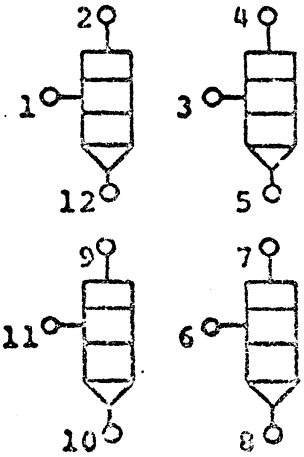
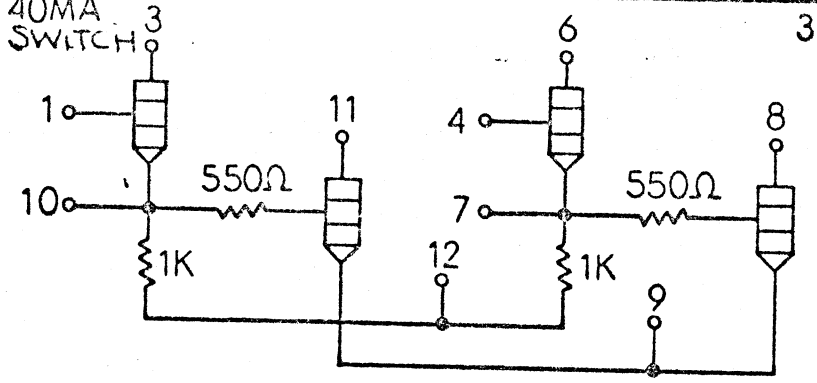


40MA SWITCH 361426



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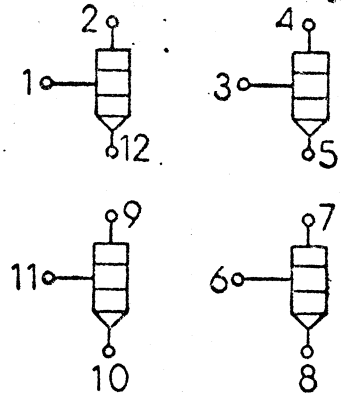
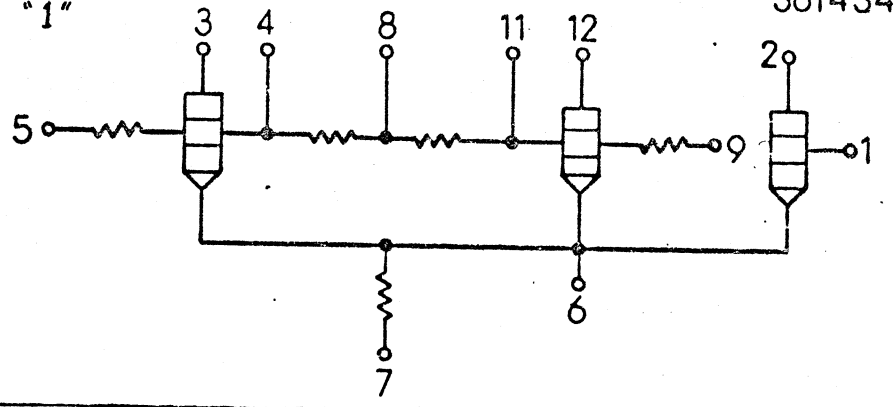


OBSOLETE
REPLACED BY
361432

SENSE AMPLIFIER "1" 361434



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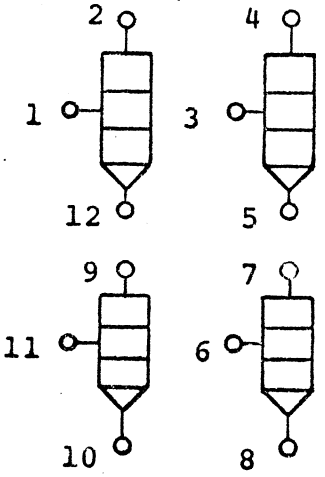

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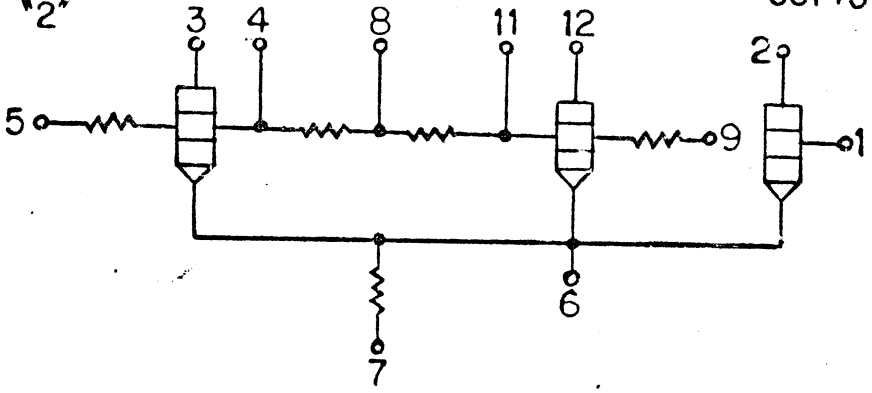

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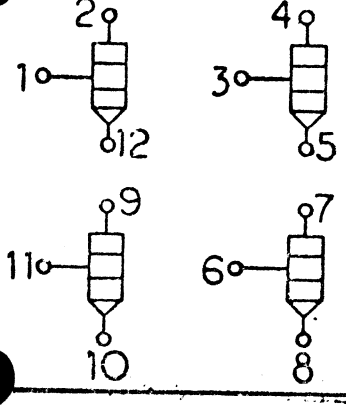

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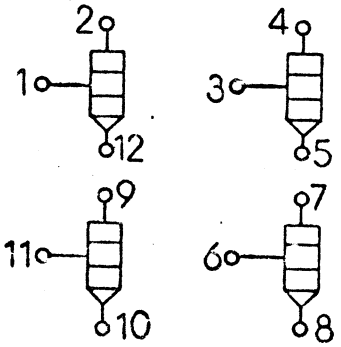

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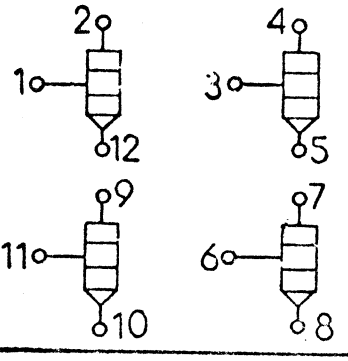

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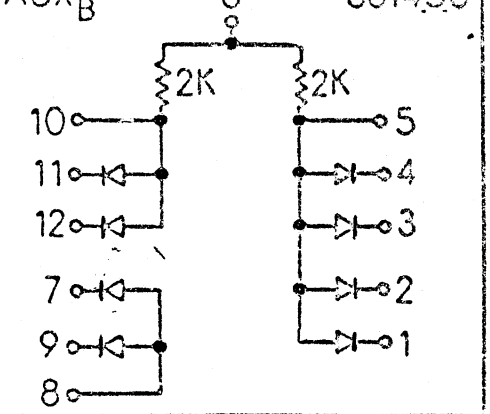

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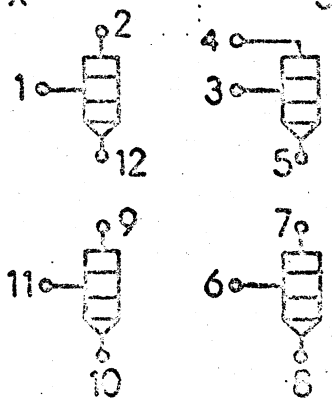

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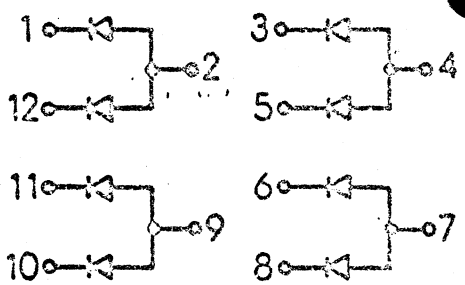

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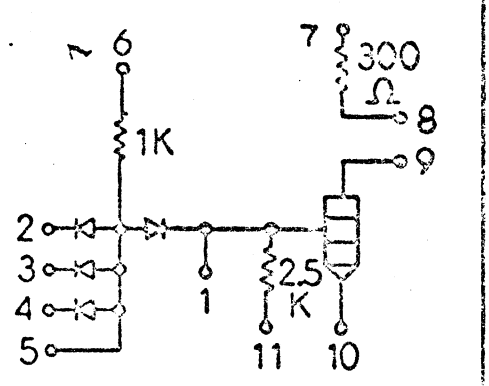
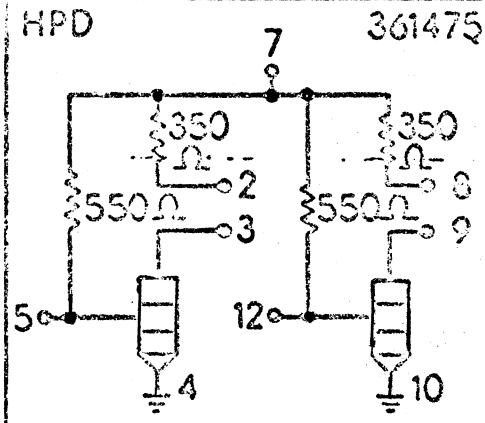


HPD 361475



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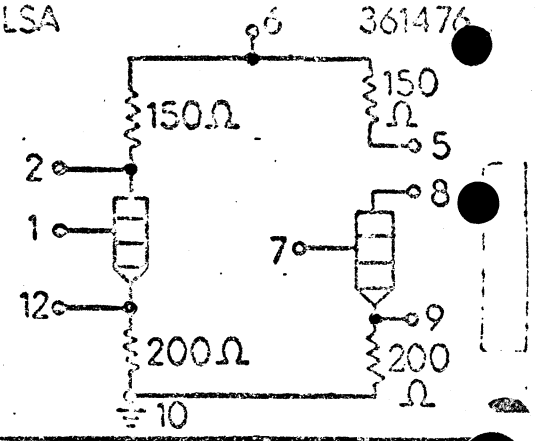
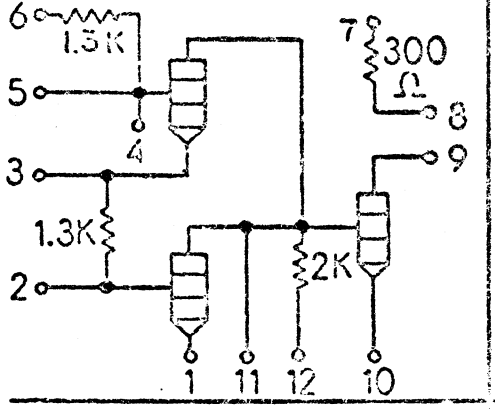
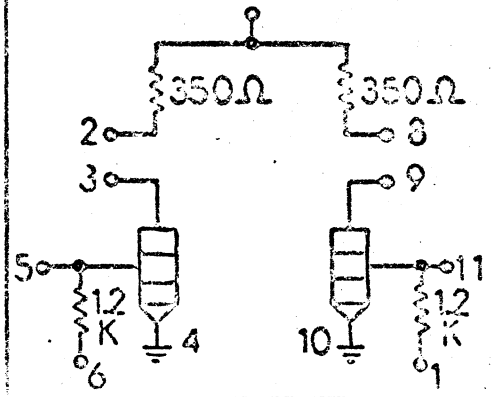


XOR 361477



II 361479



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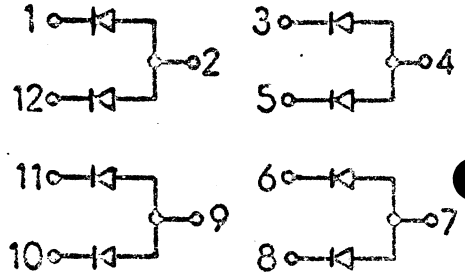

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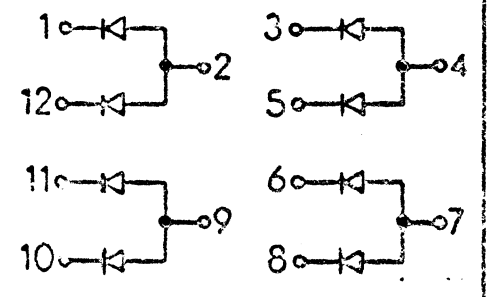

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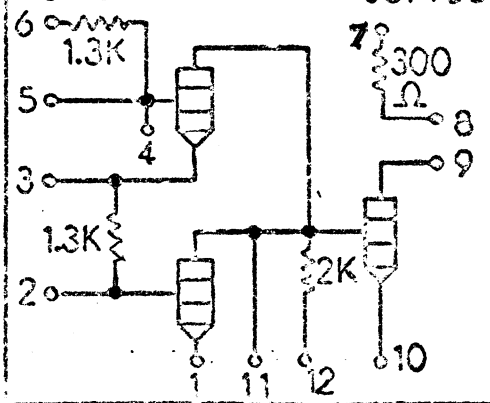

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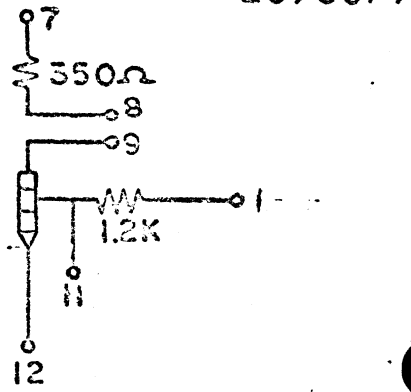

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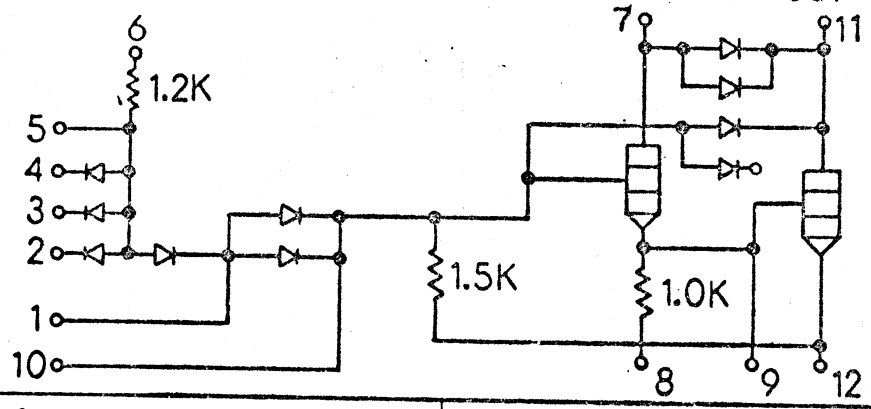

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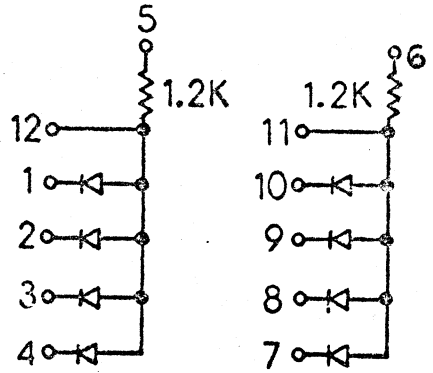

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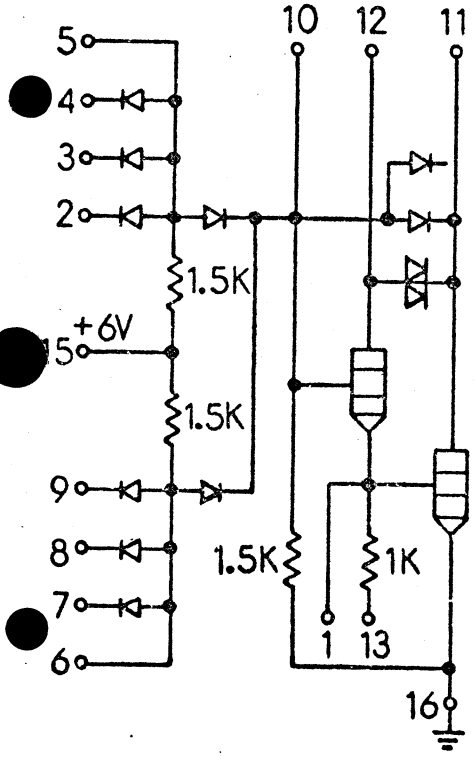

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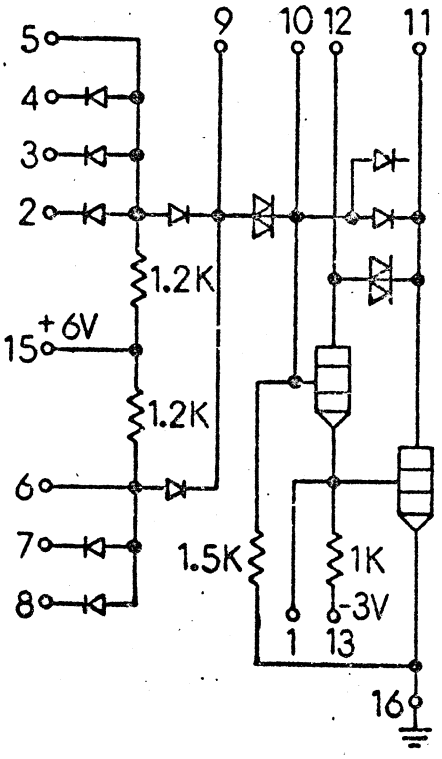
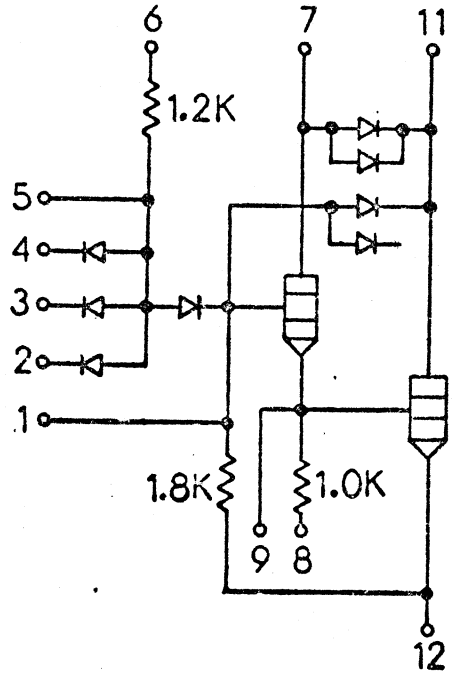
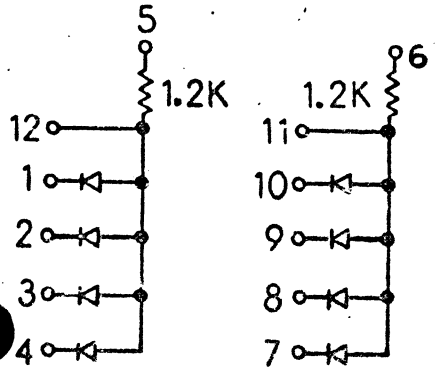


AOI$_{11}$ 361408



AOX-11 361409



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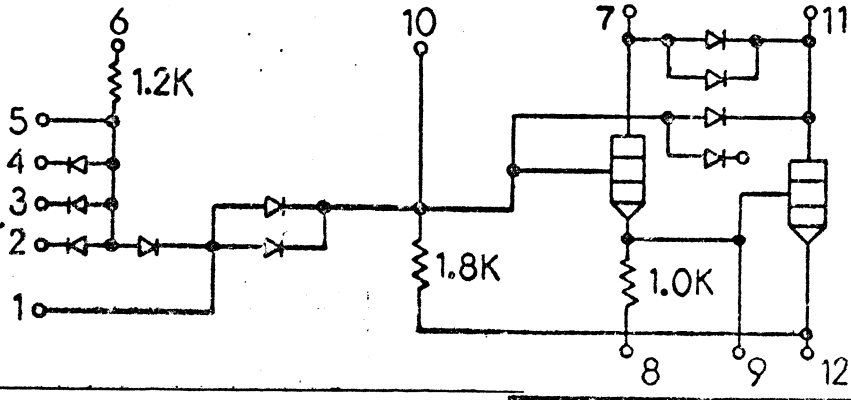

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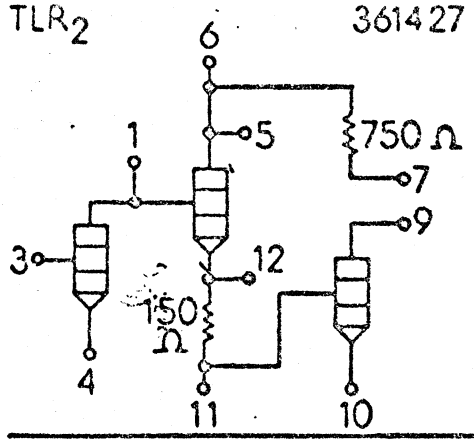

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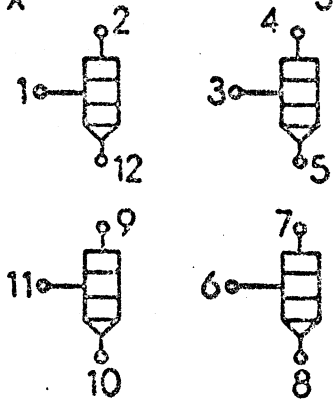

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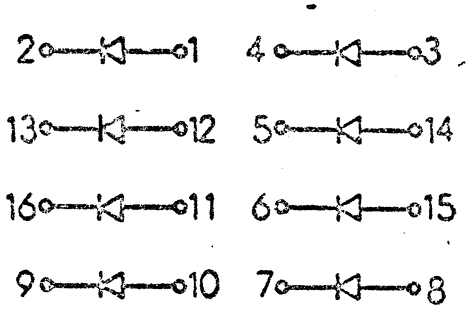

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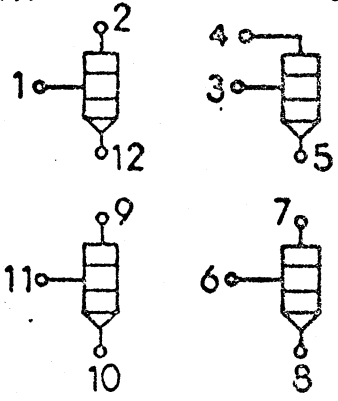

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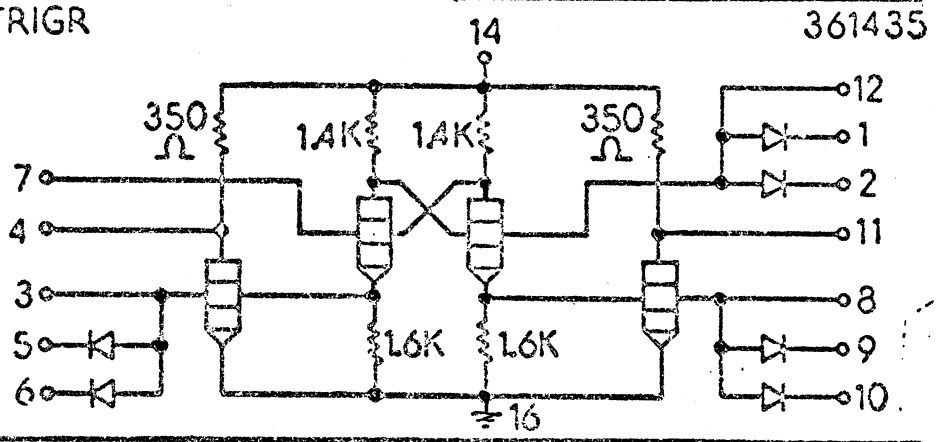

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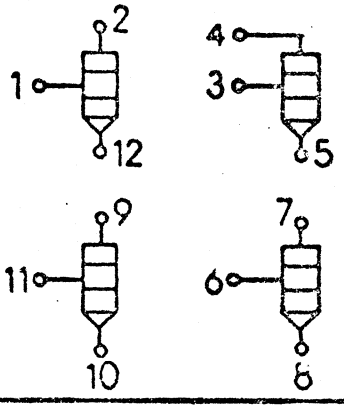

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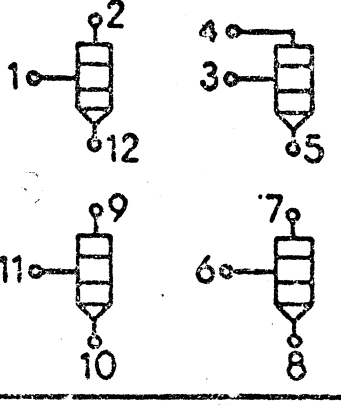

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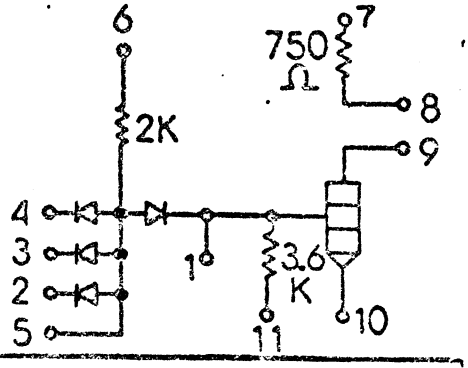

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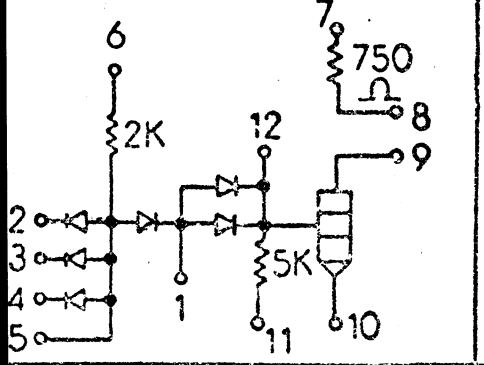
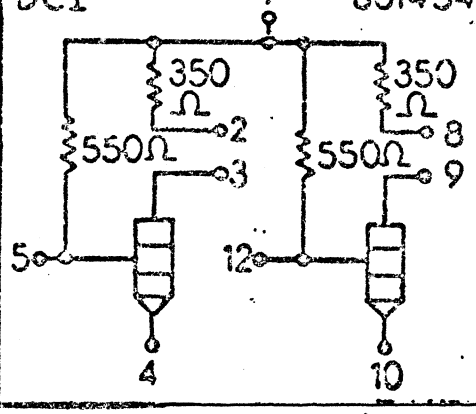


DCI 361454



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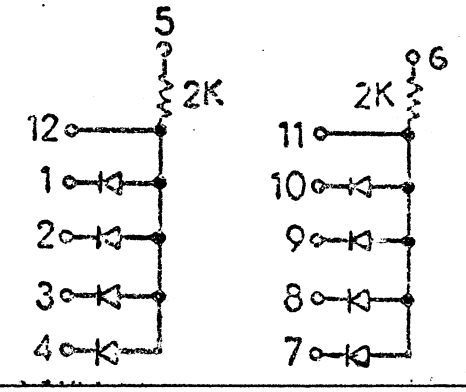

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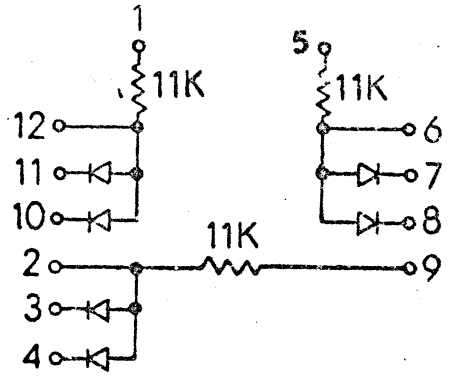

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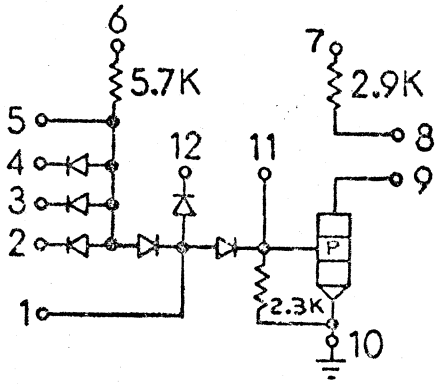

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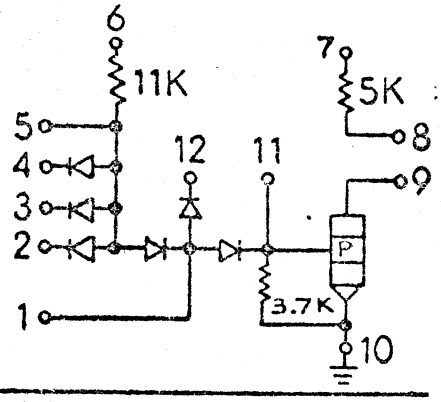

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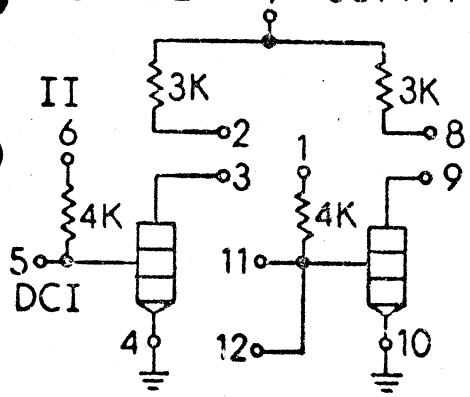

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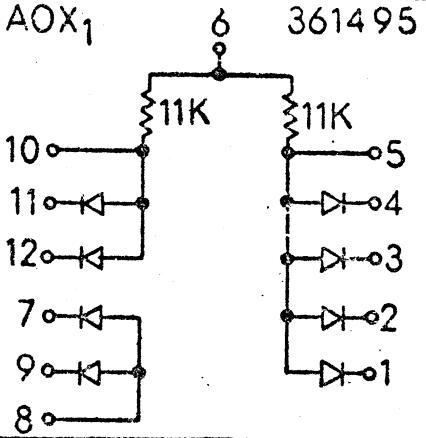

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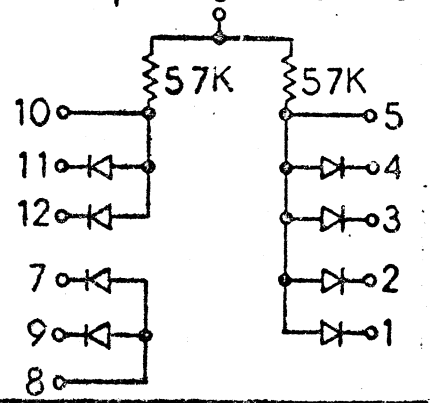

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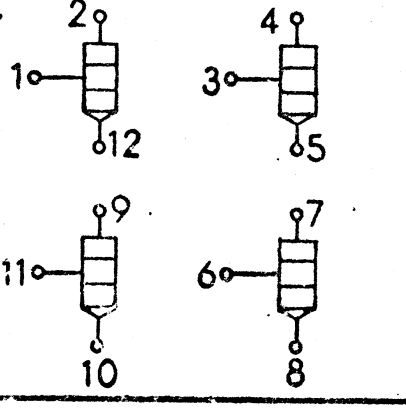

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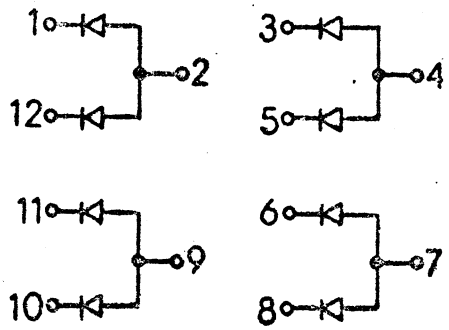

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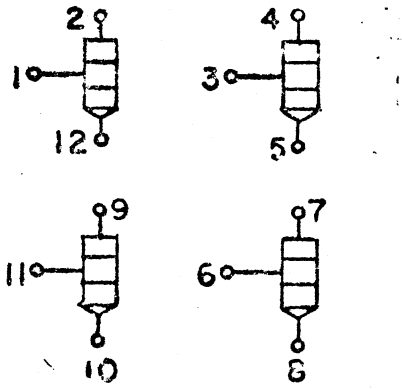
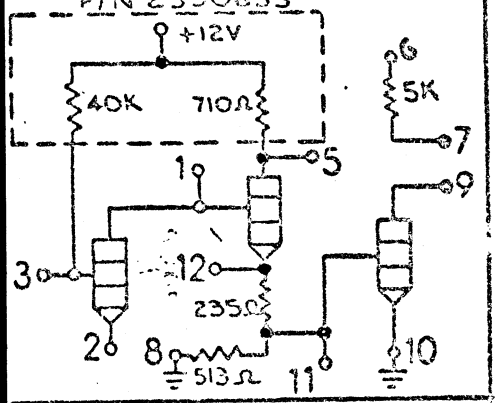
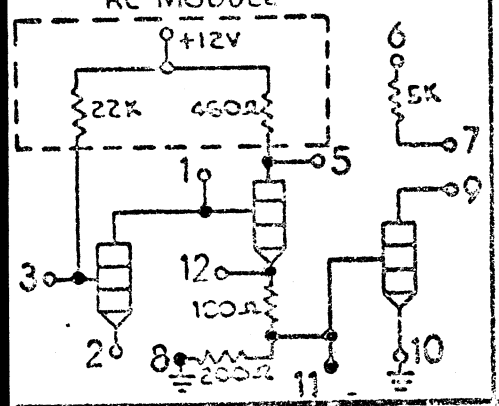


SLT MODULE SCHEMATICS

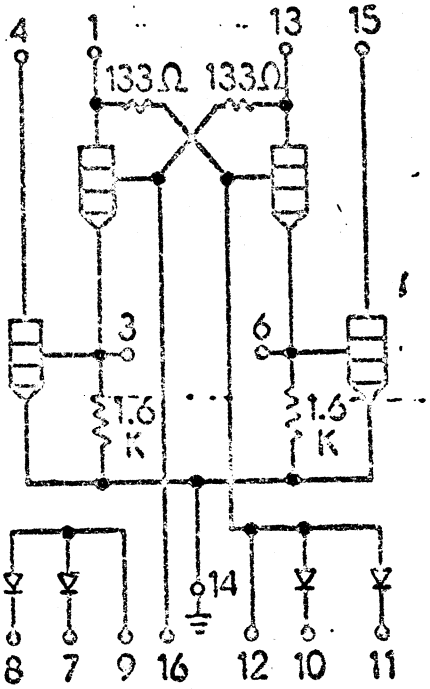
RC MODULE P/N 2390655 — 361415



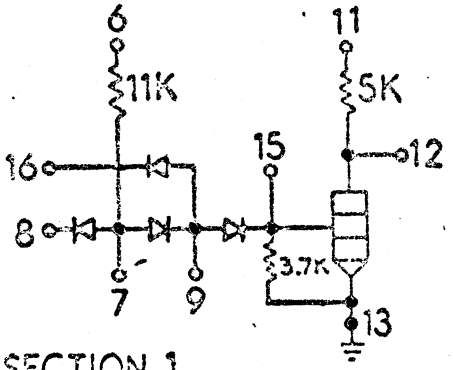
RC MODULE — 361446



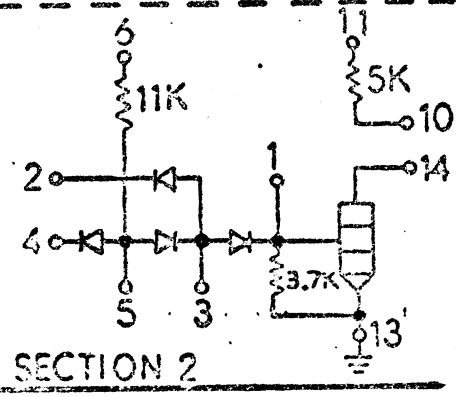
TRIGR — 361436



2-2 WAY AOI — 361445

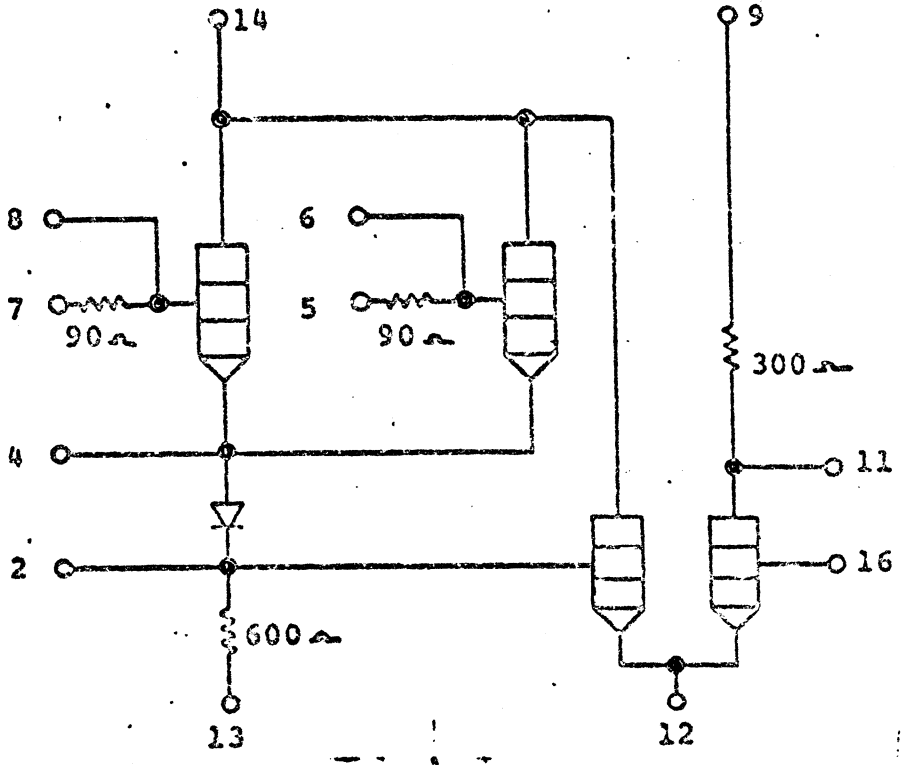


SECTION 1

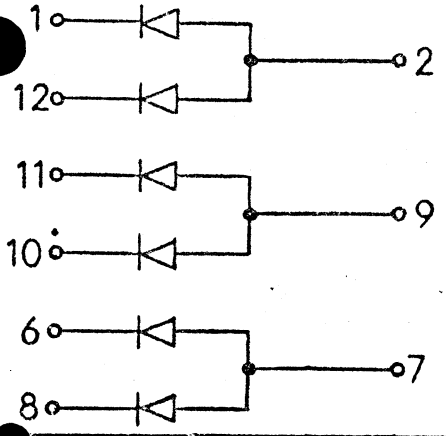


SECTION 2

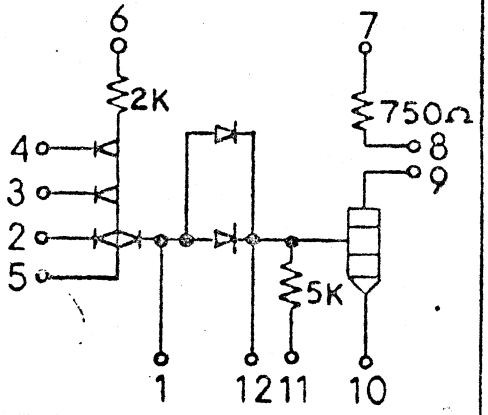
SLT COUPLER DRIVER — 361488



FDD #3 2395059



AOI #3 2395053



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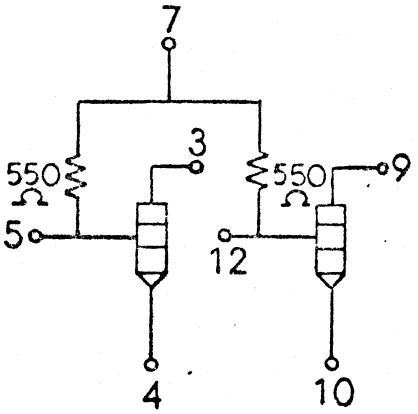

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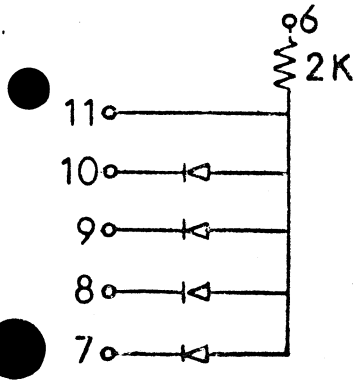

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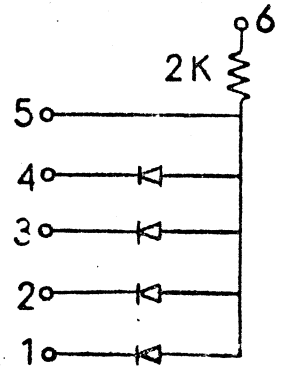

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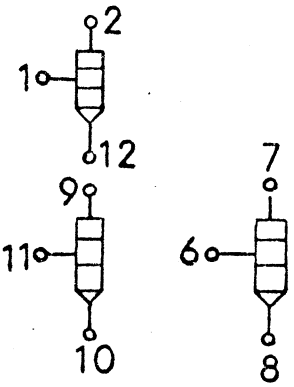

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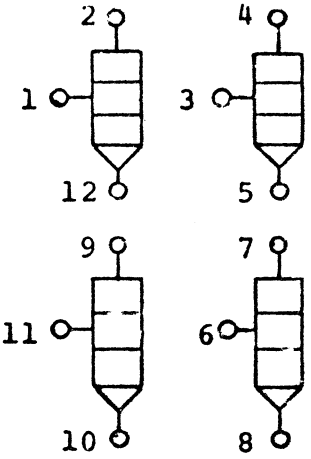

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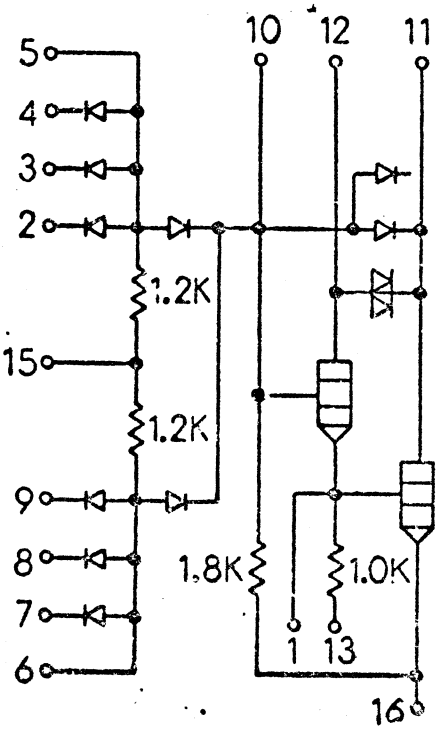
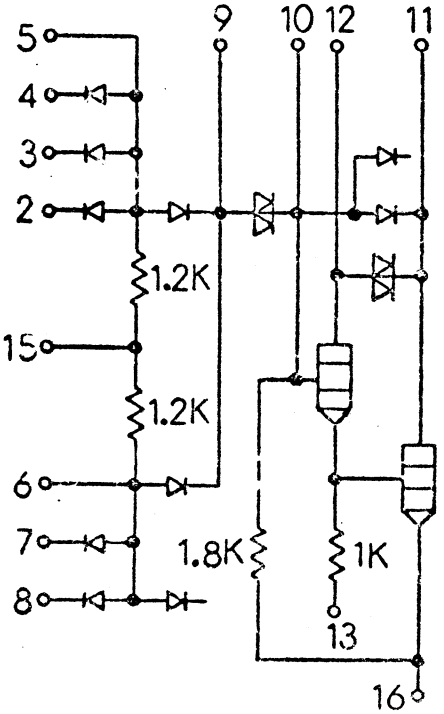


$AOI_{11}BT$ 361413



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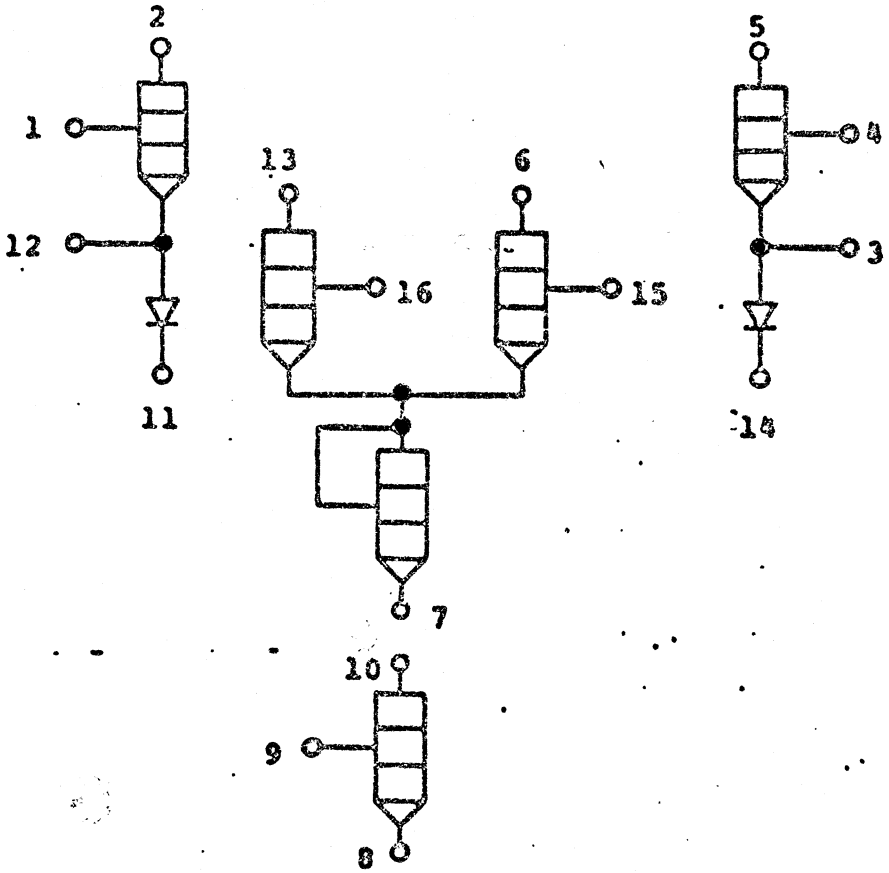
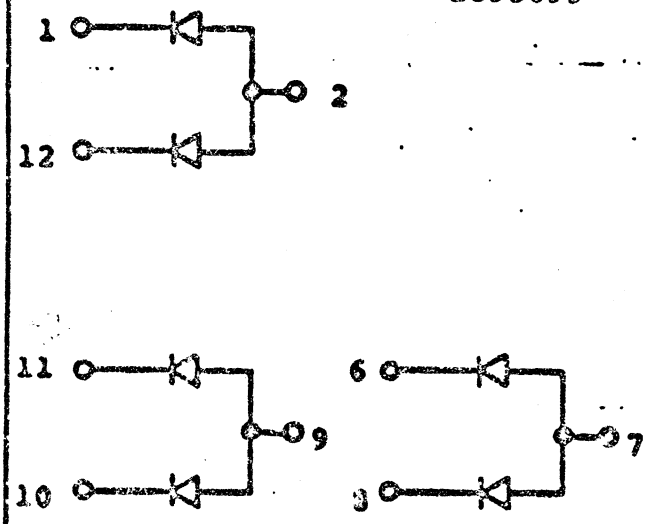
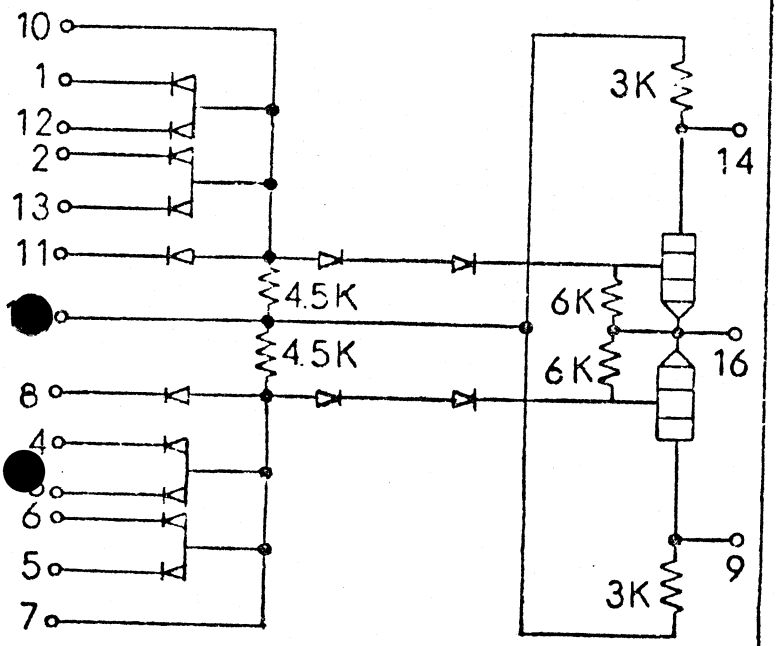


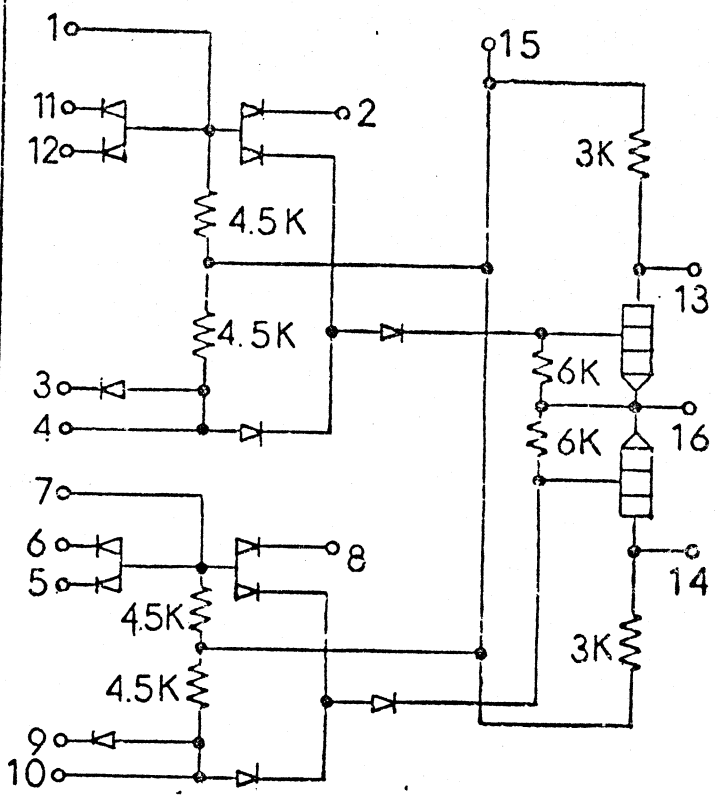
FDD03 2395099



2-5 WAY-AI 361440



2-3A/1A-2 OR INVERTER 361441



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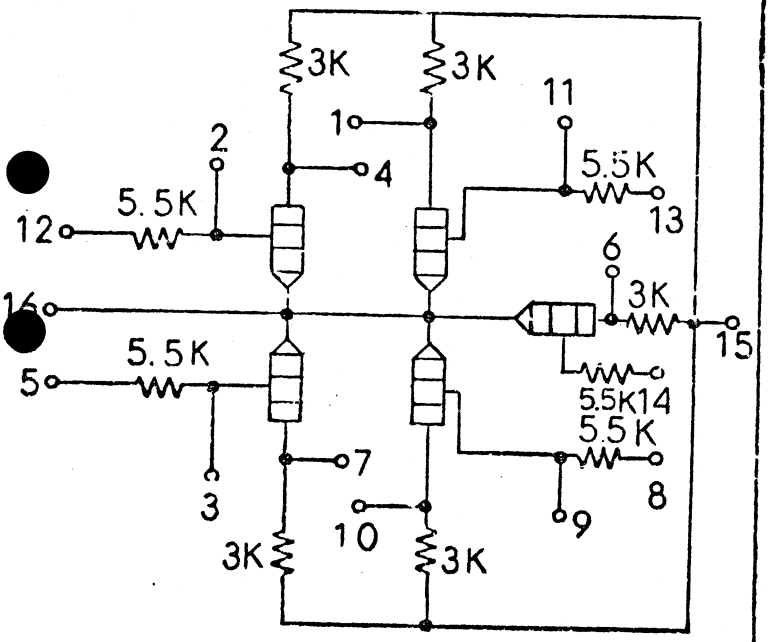

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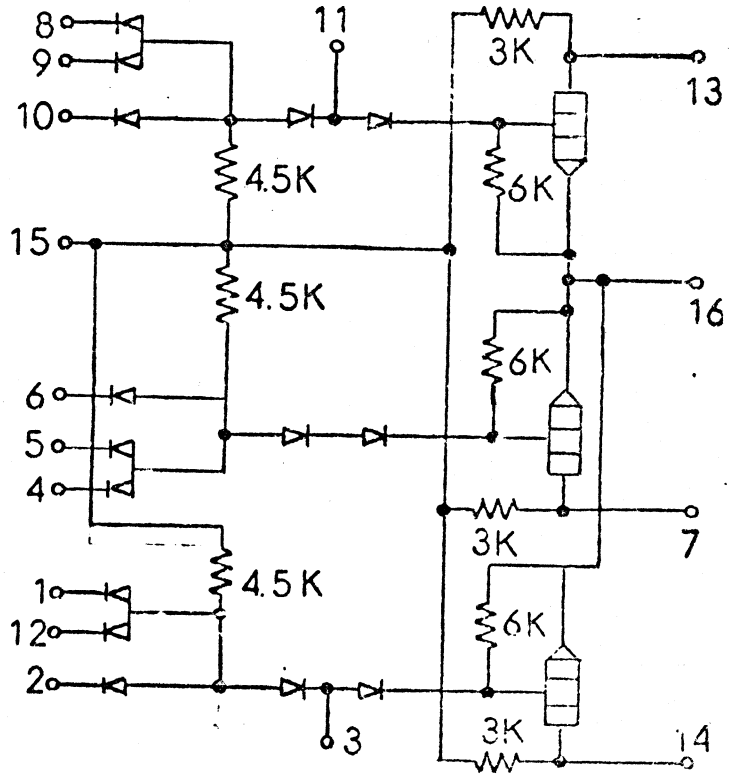
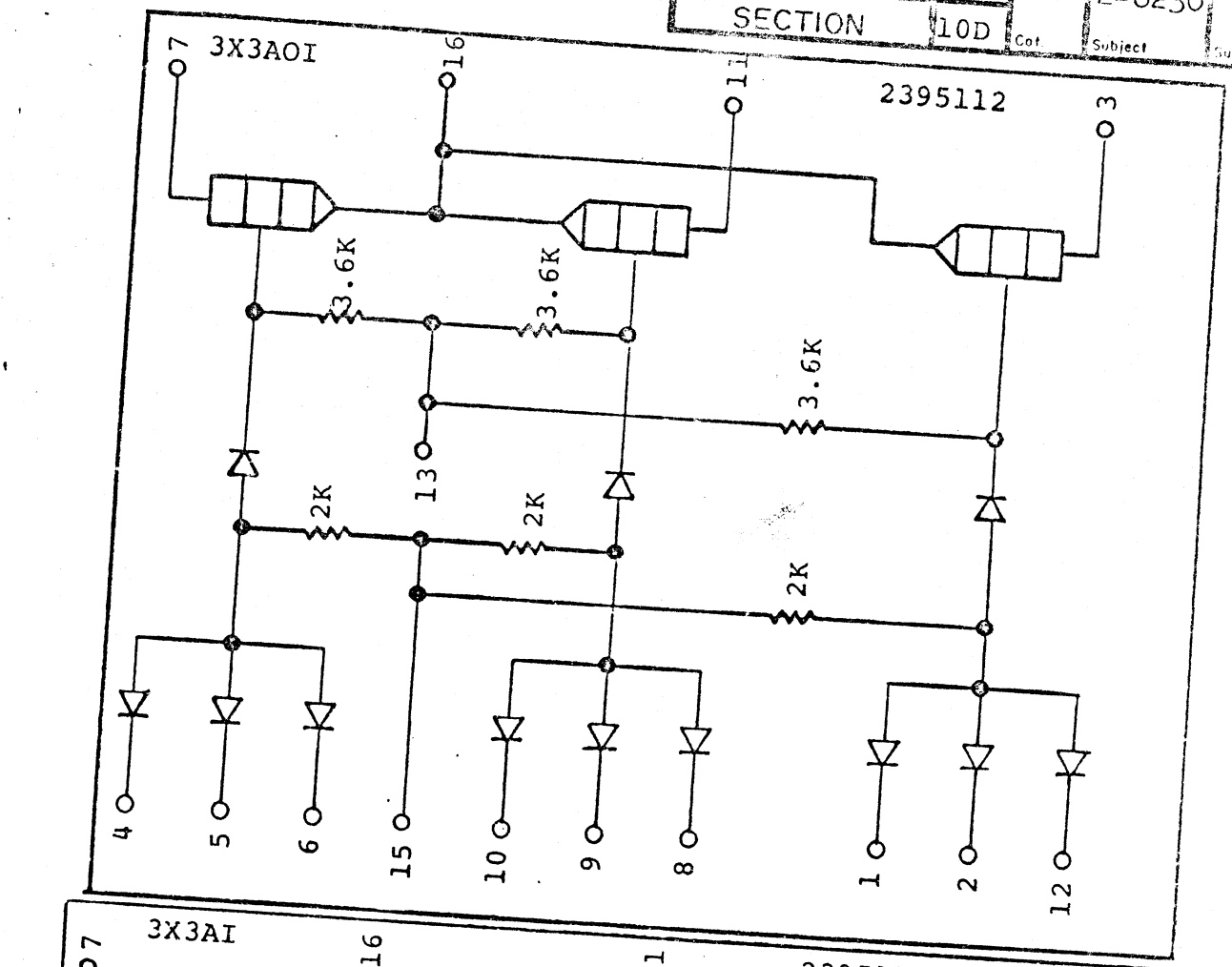
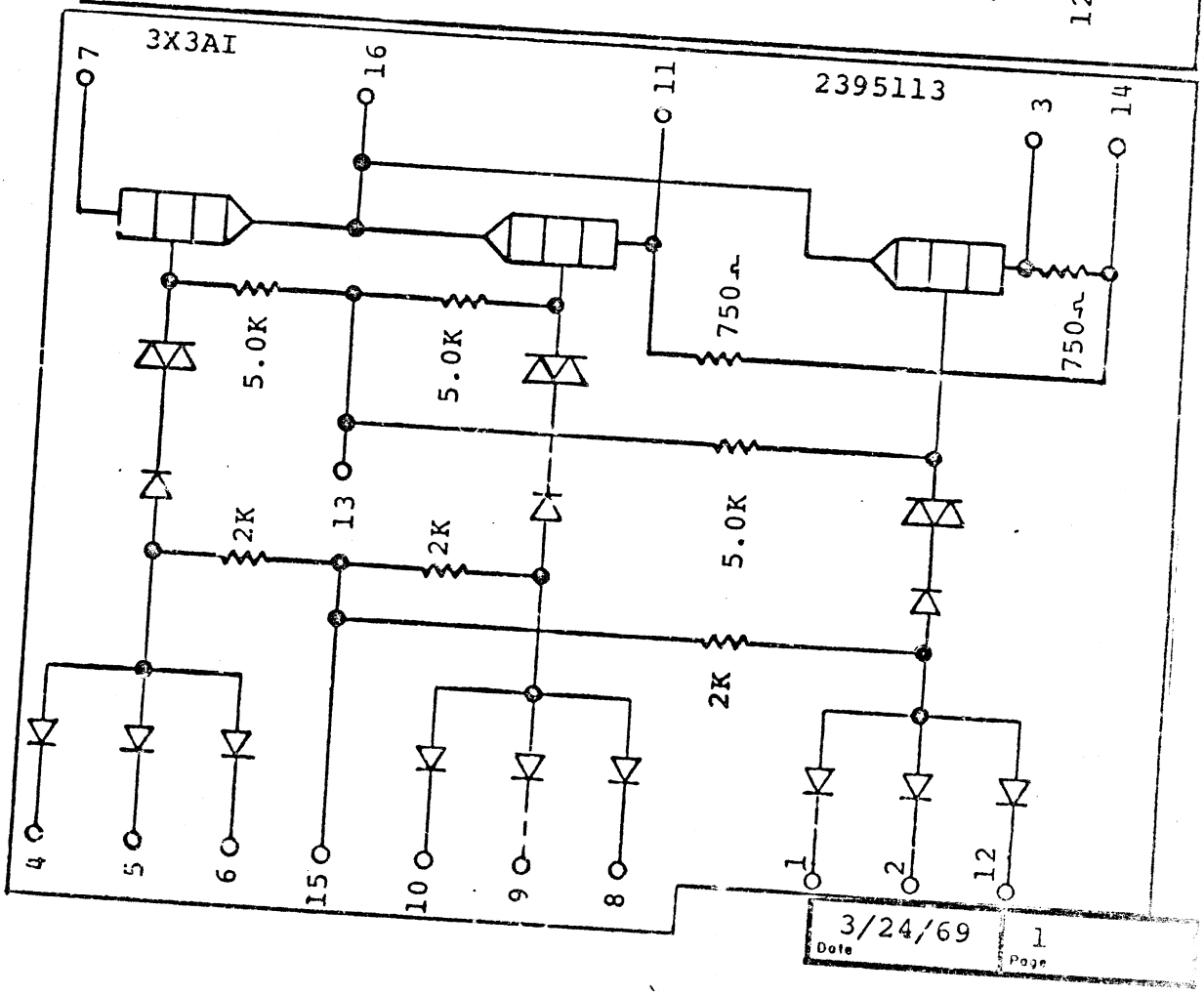


SLD MODULE SCHEMATICS

CARD GROUND RULES	DEP	2-6230	3
SECTION 10D	Cat	Subject	Suffix

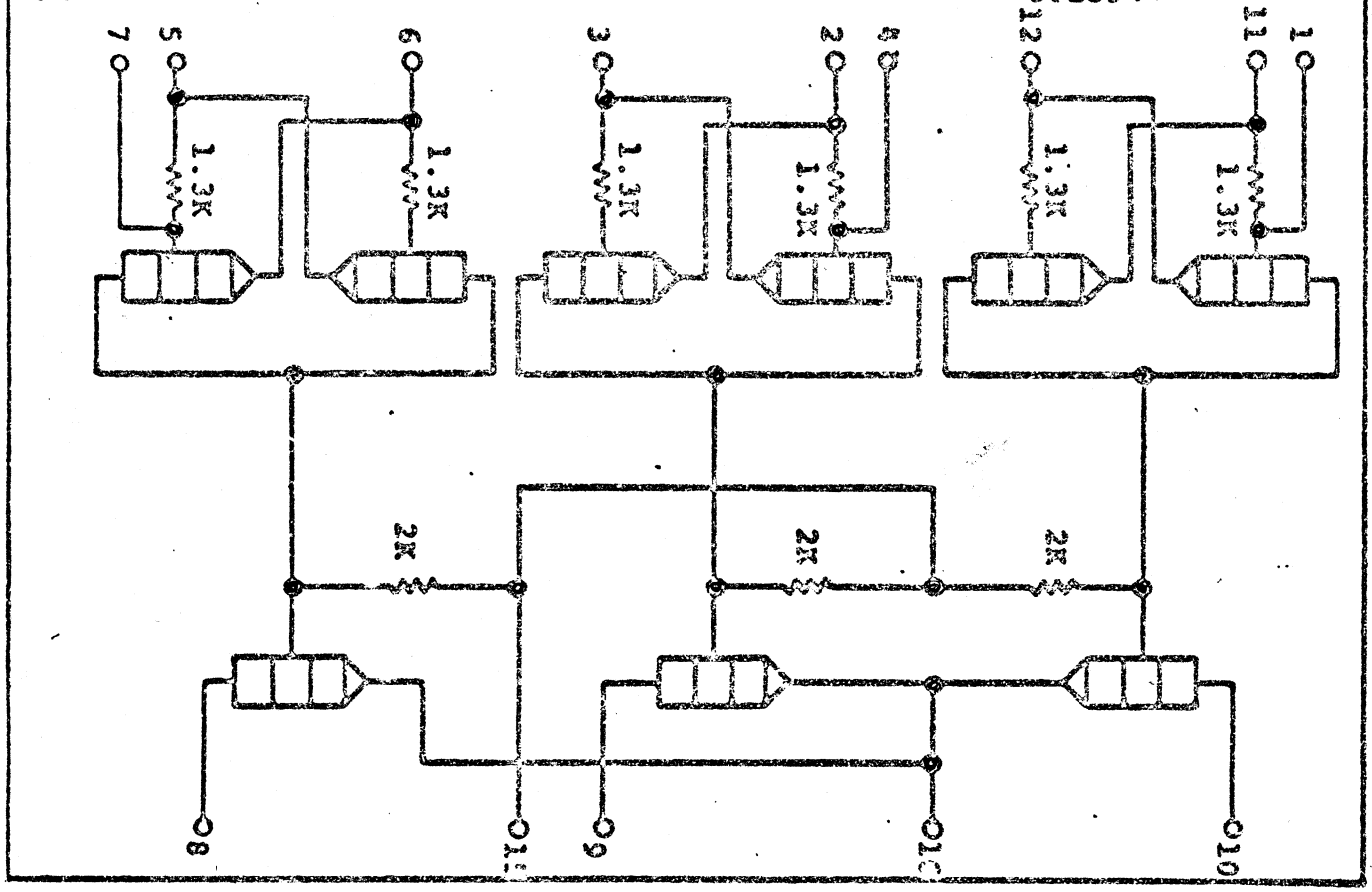




3/24/69	1
Date	Page

3X-XOR

361594



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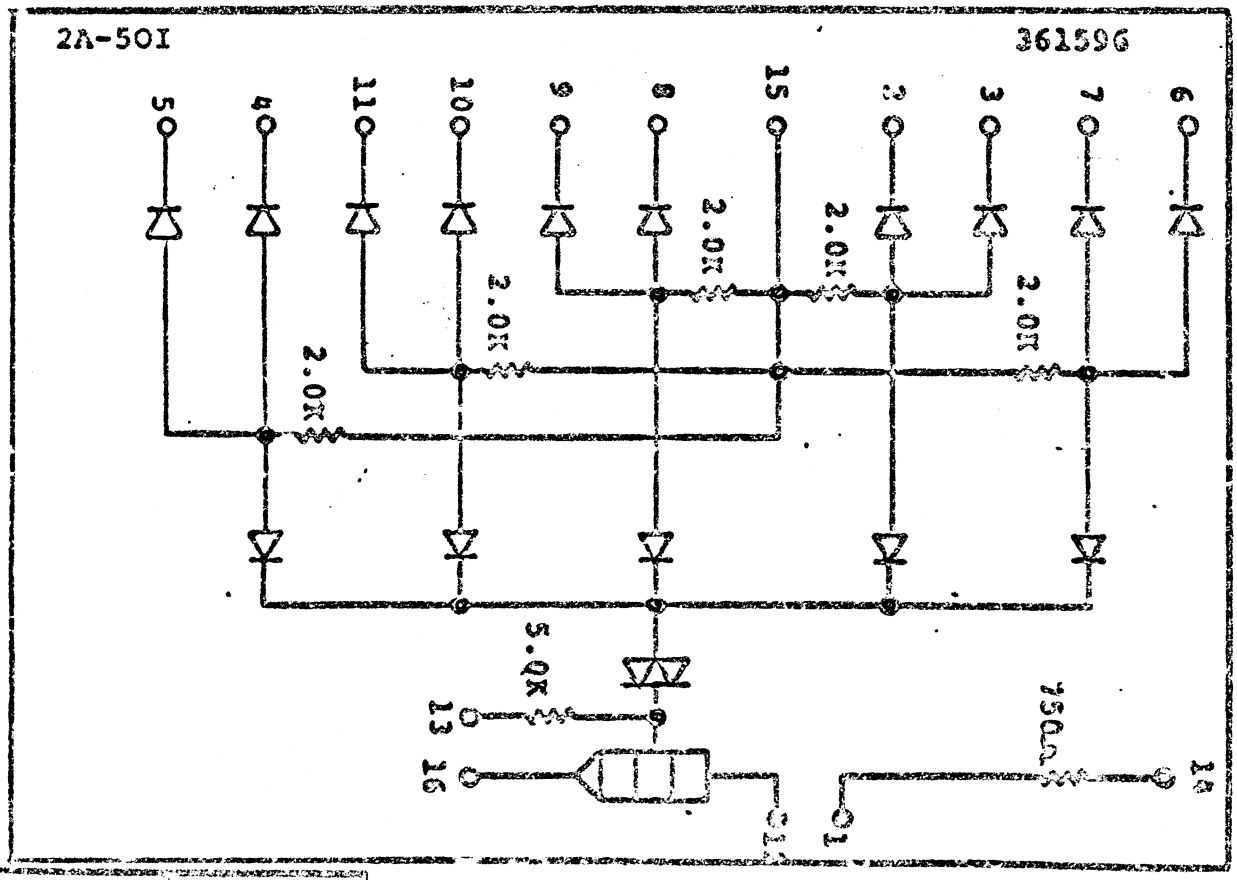

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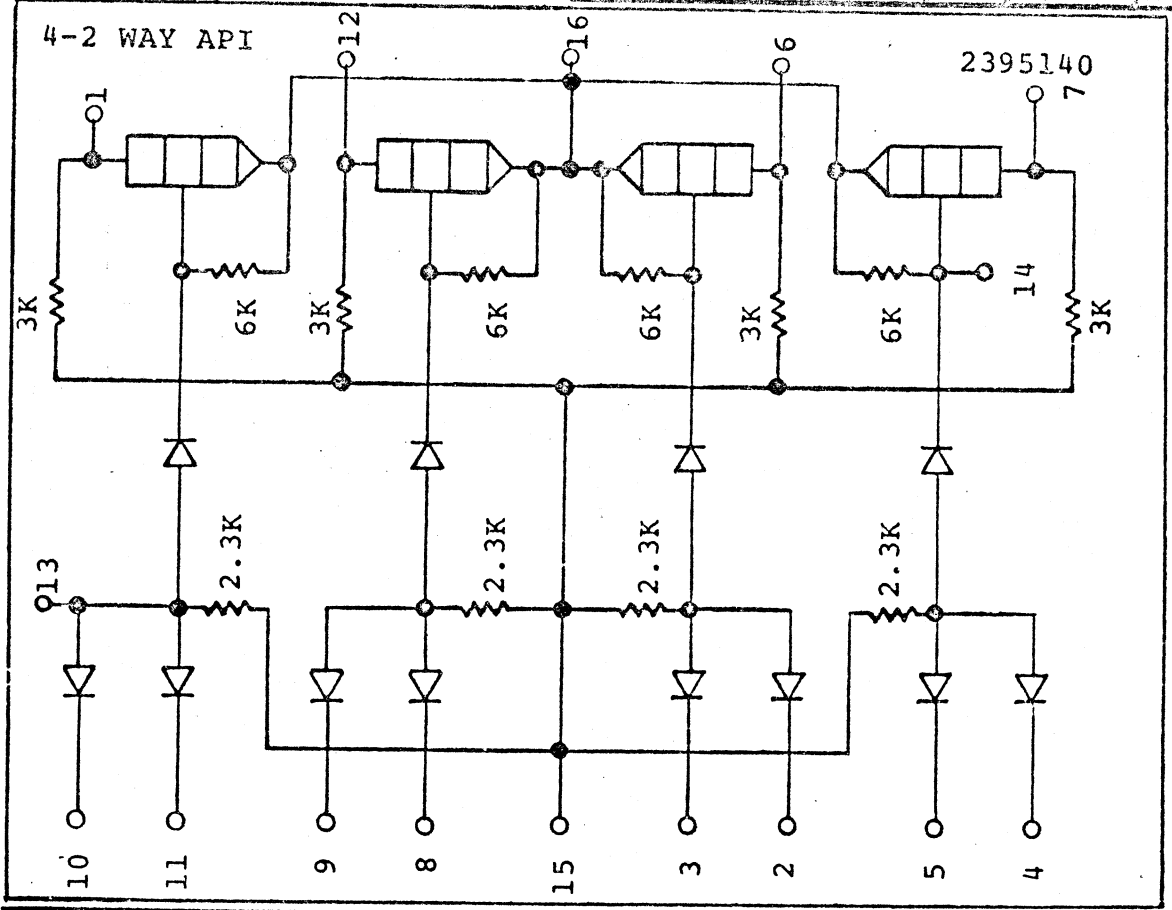
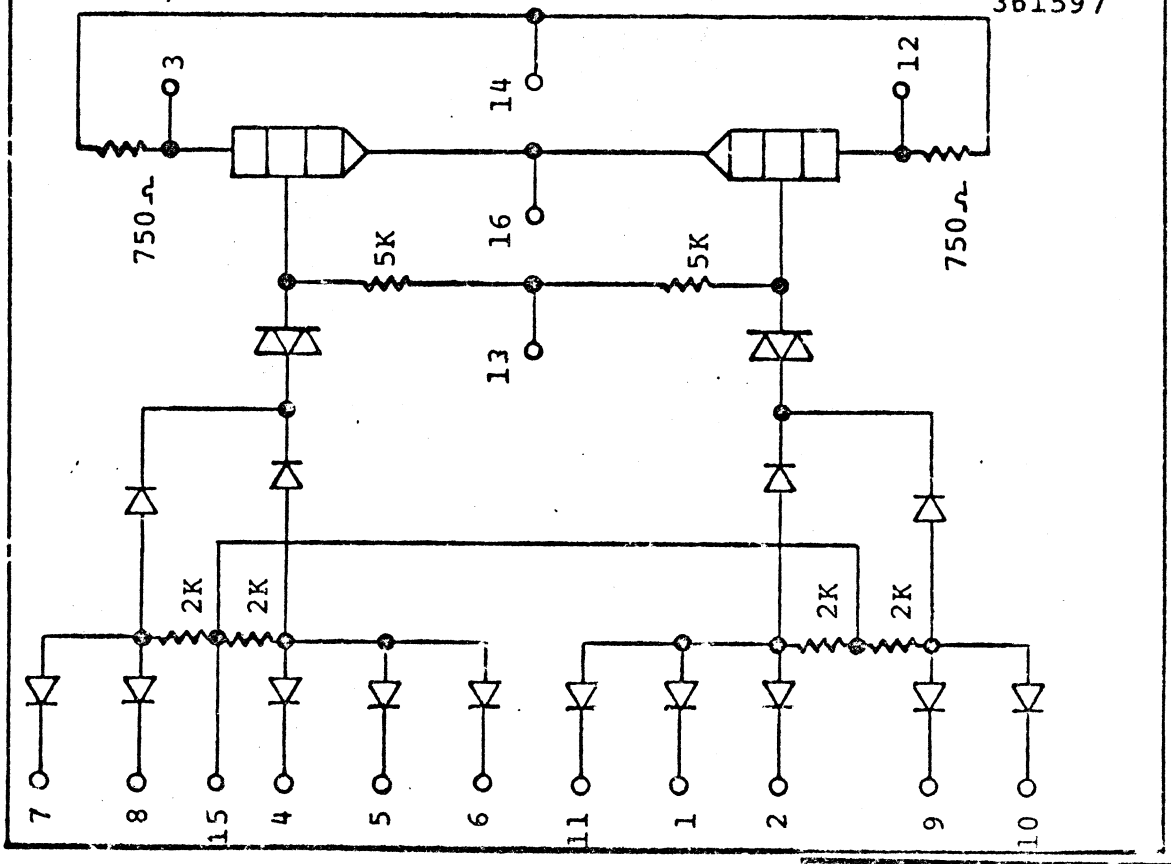
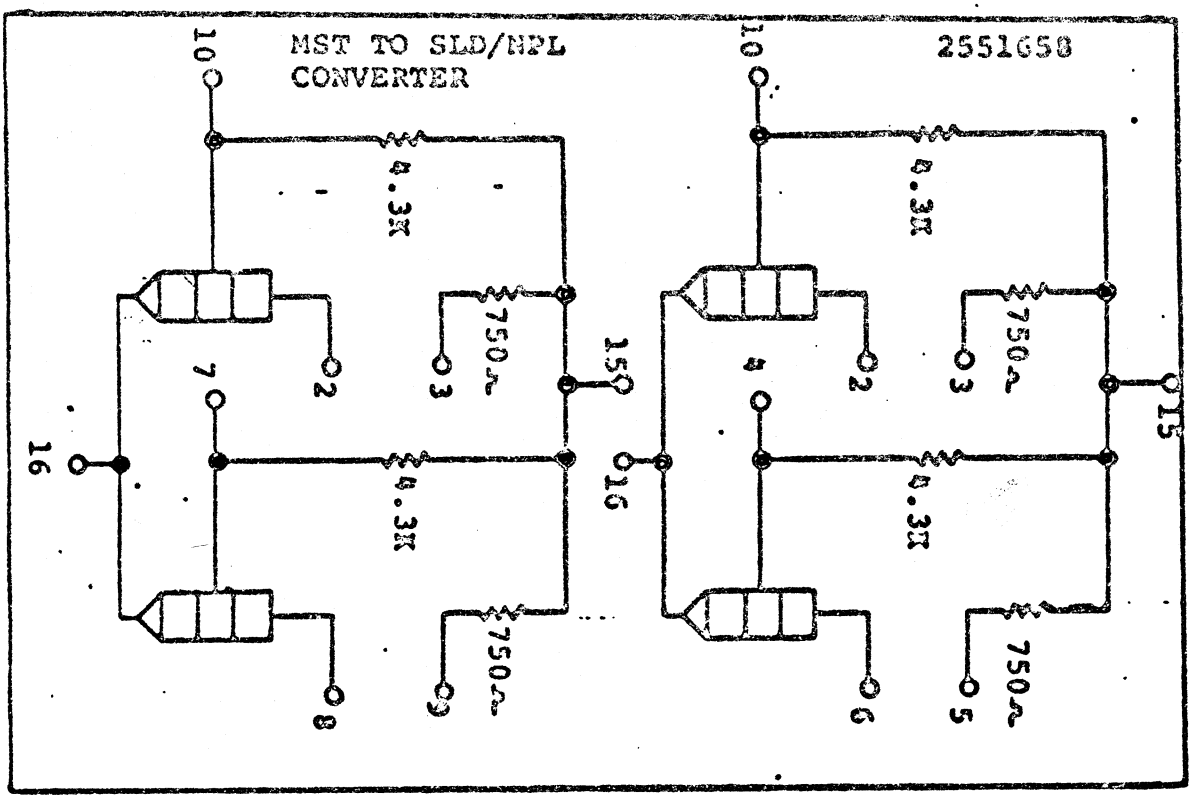


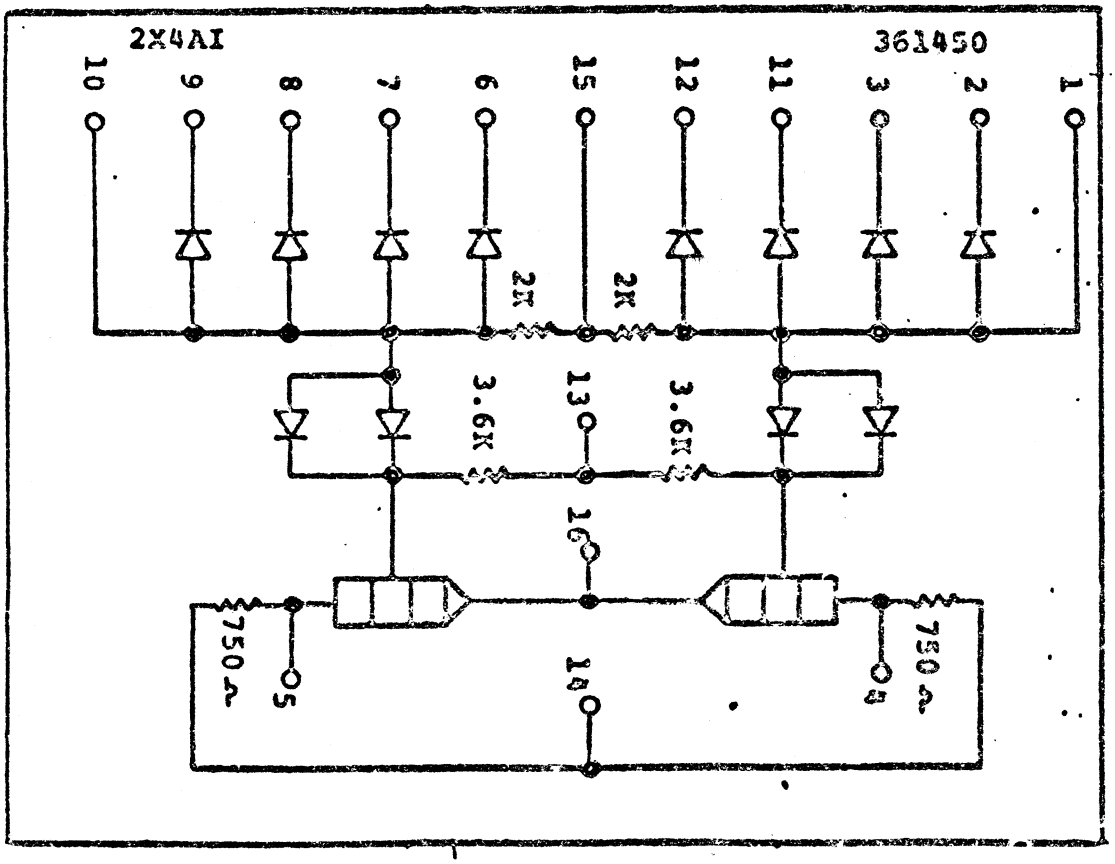
2X3A/2AOI

361597



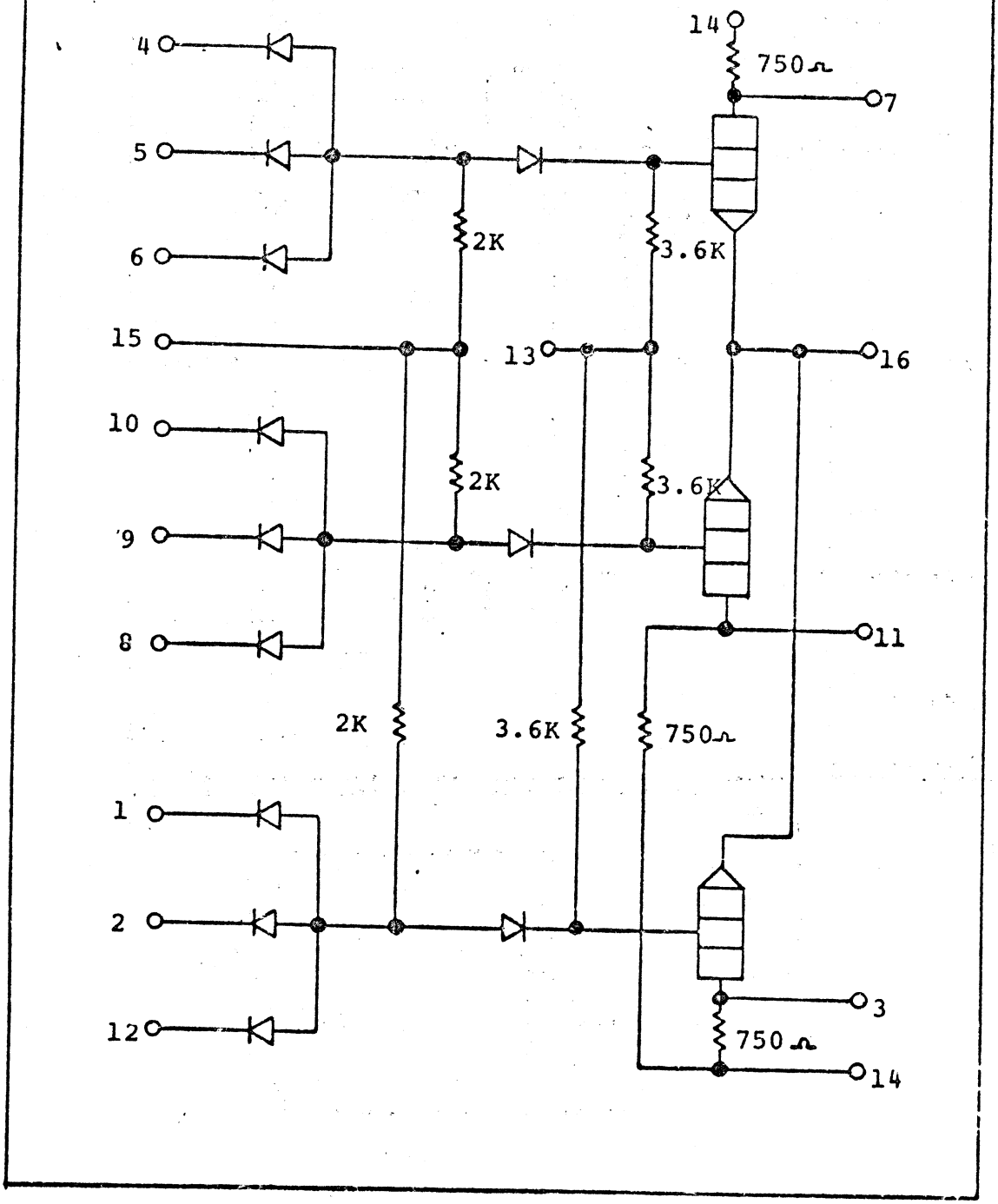
SLD MODULE SCHEMATICS





3-3AI

361595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3
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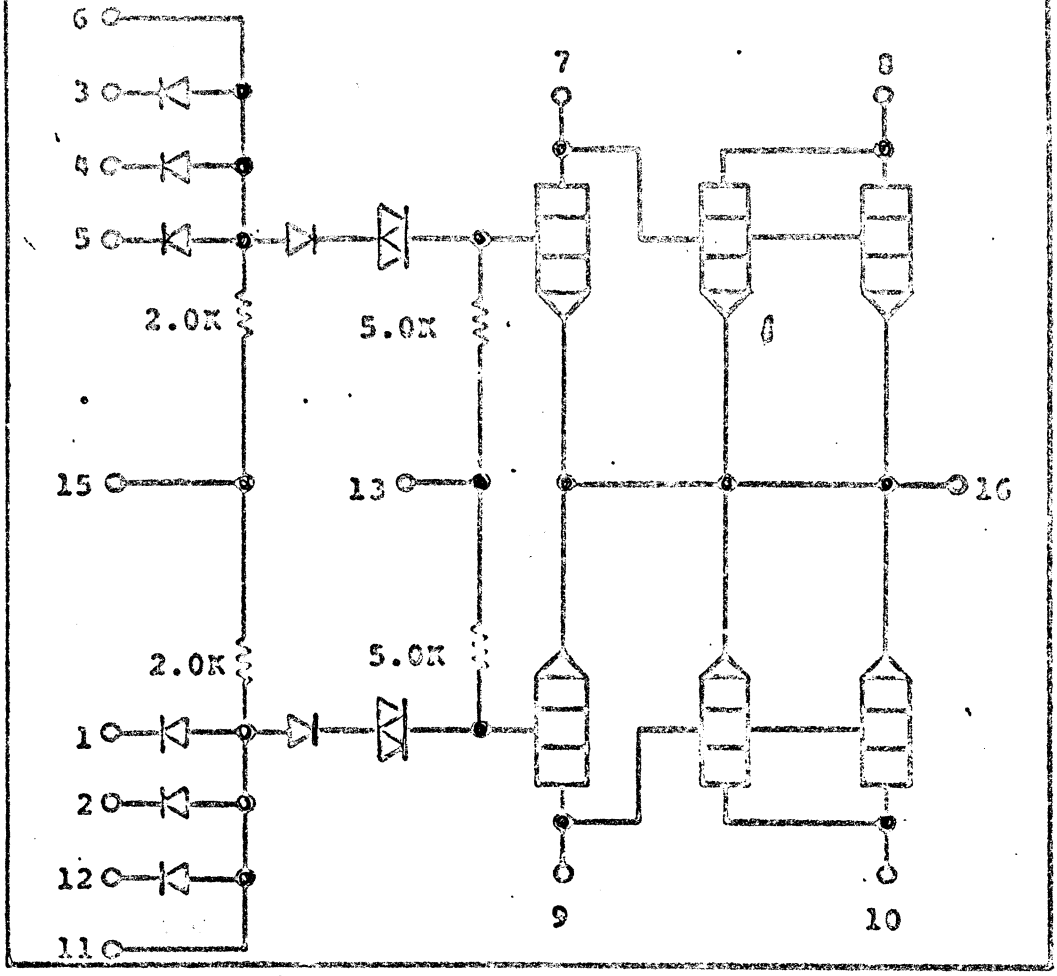
14

2KAOI-HPD 361598



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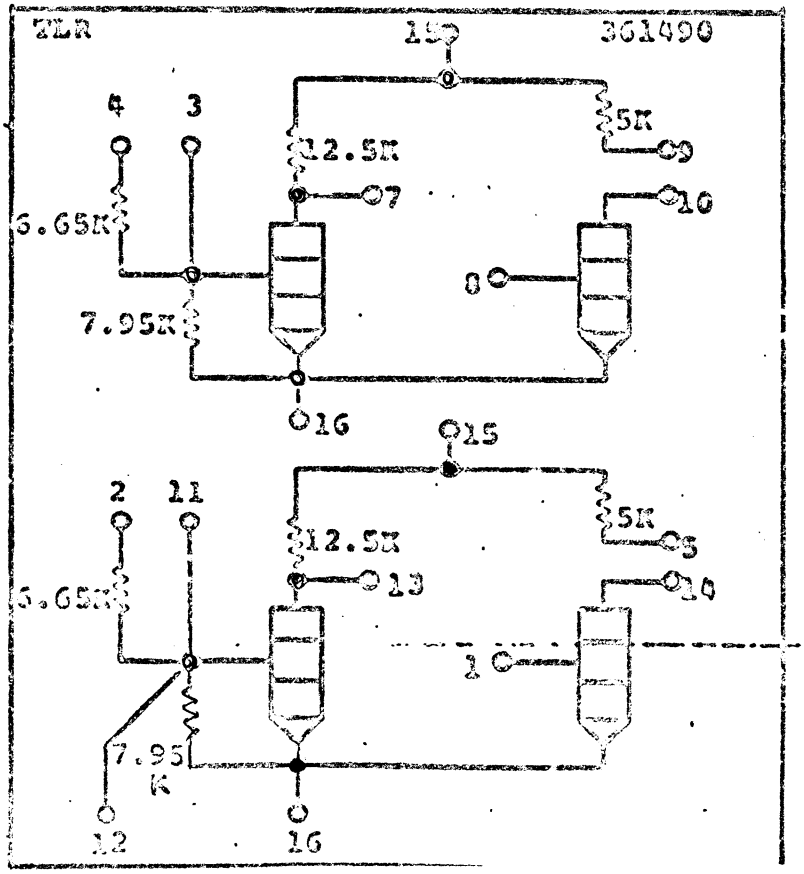

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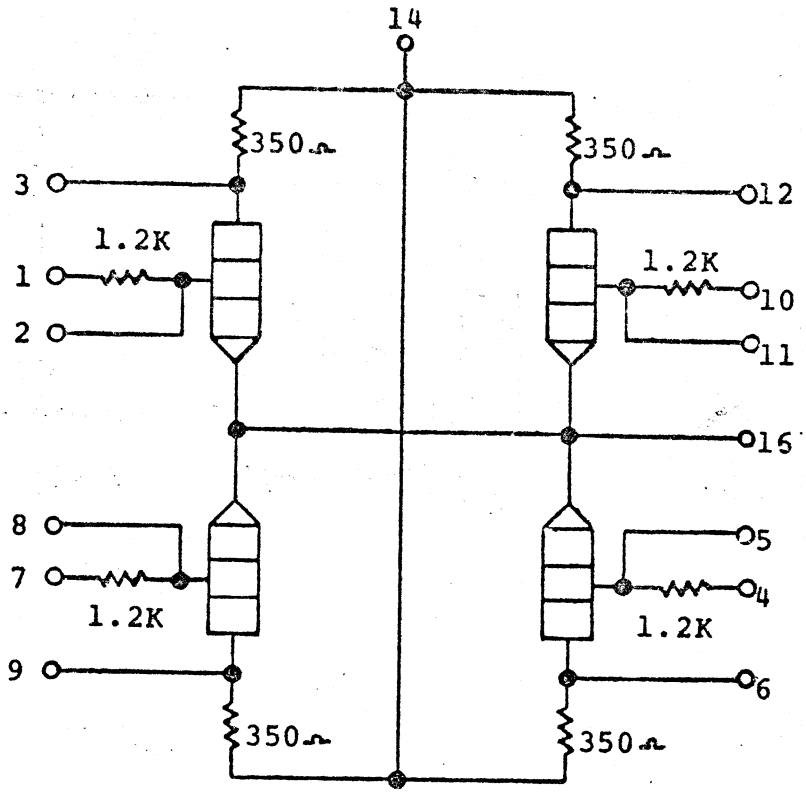

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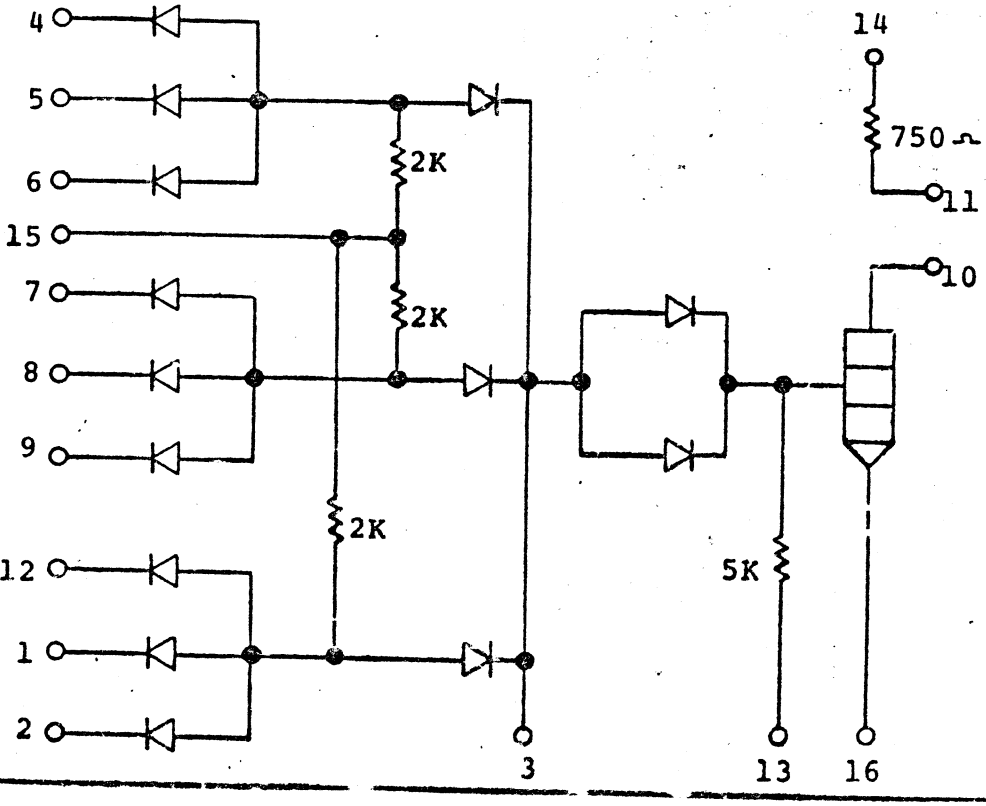

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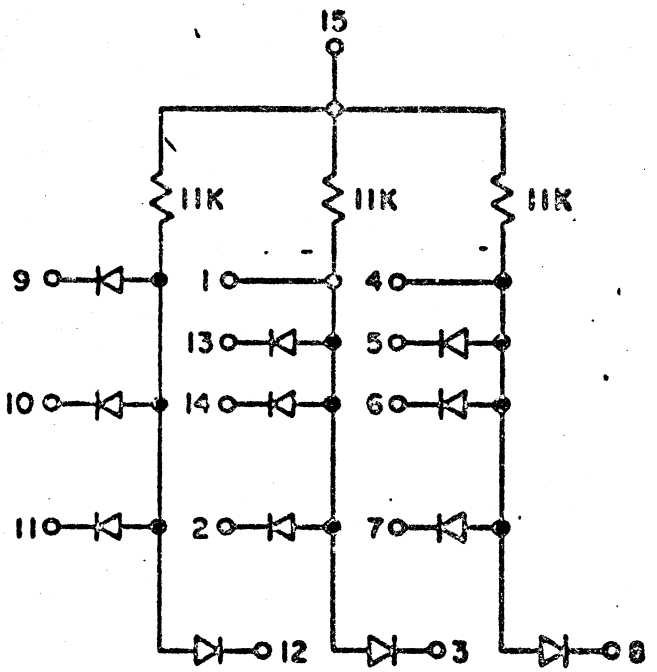

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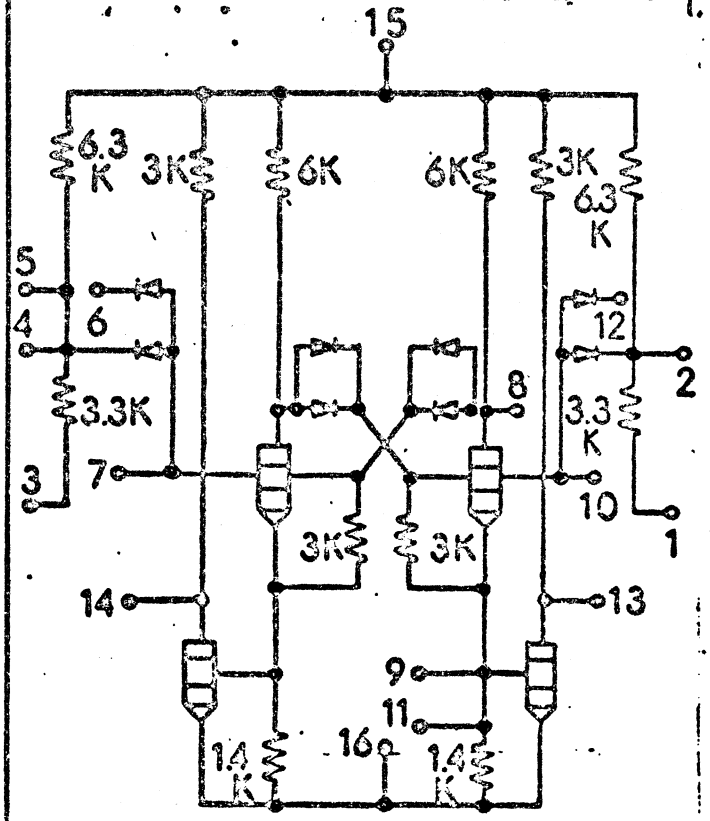
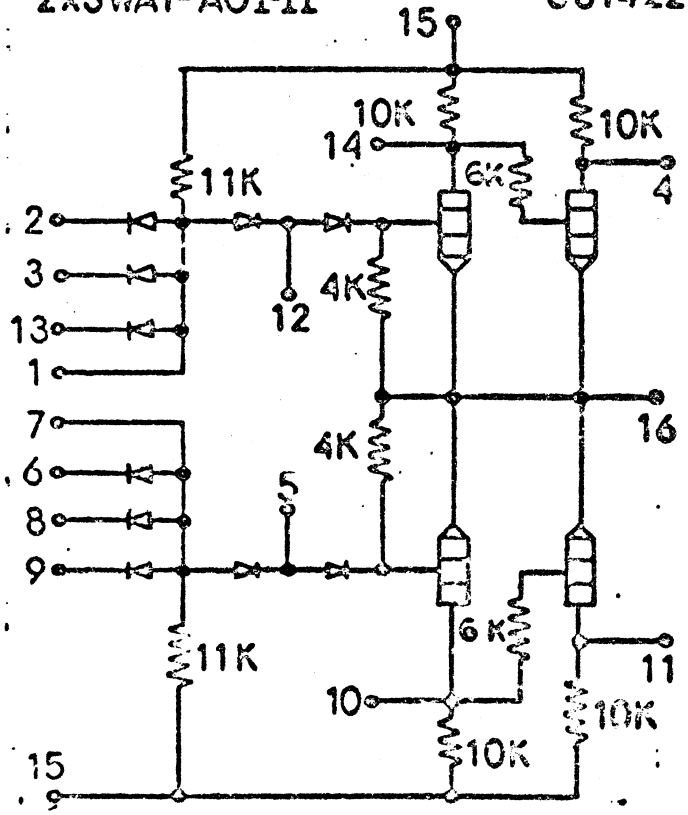


2x3WAY-AOI-II 361422



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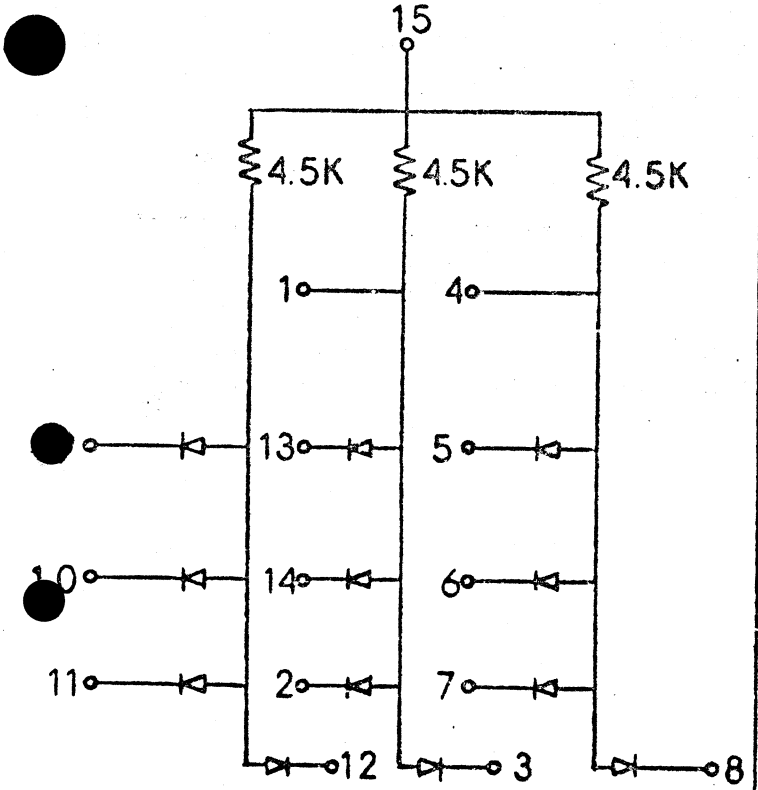

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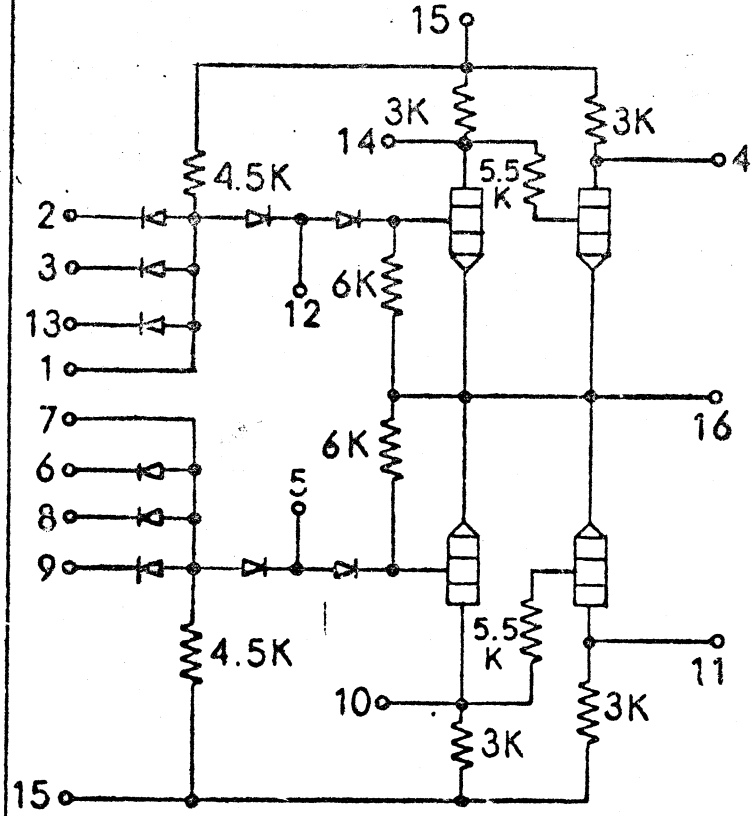

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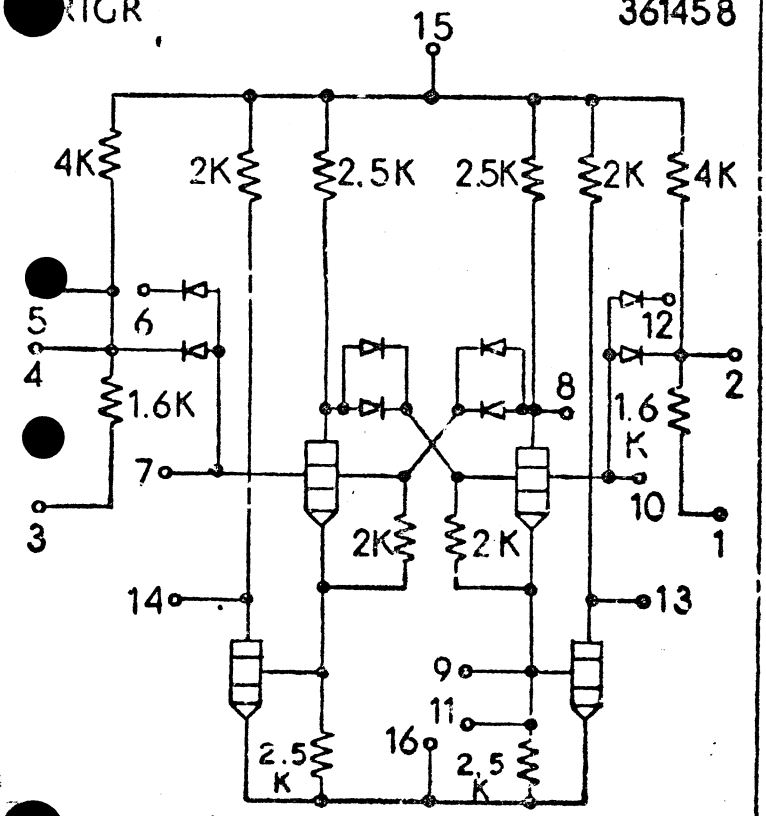
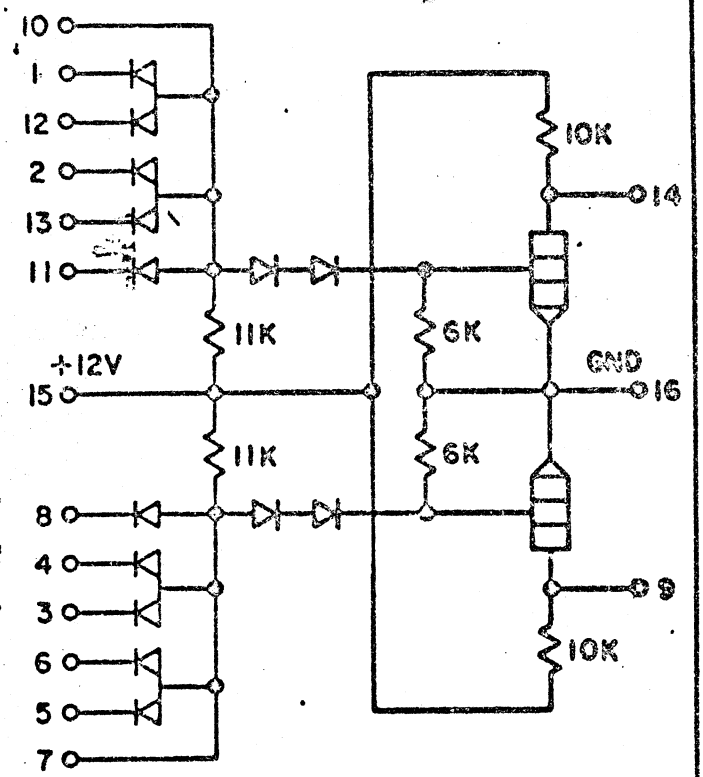
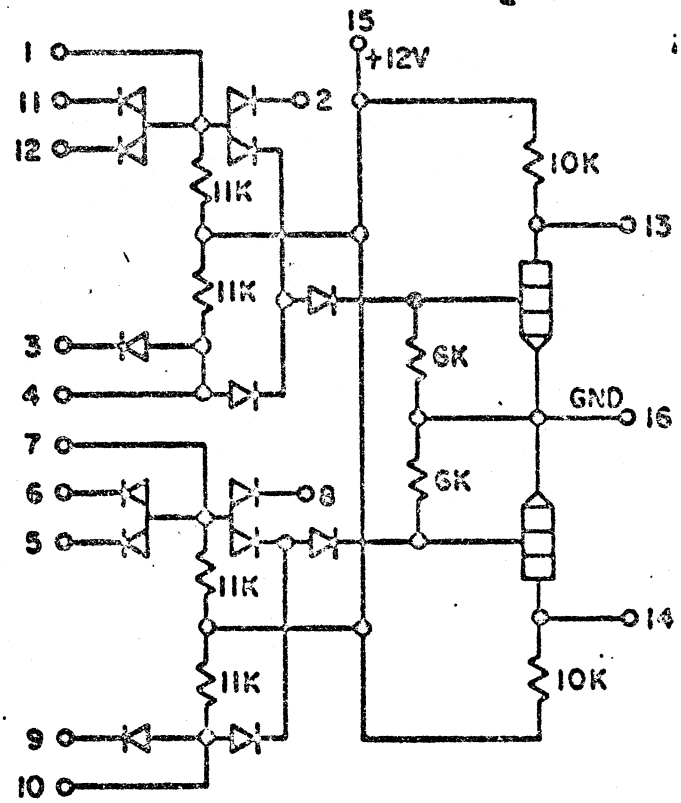


SLD MODULE SCHEMATICS

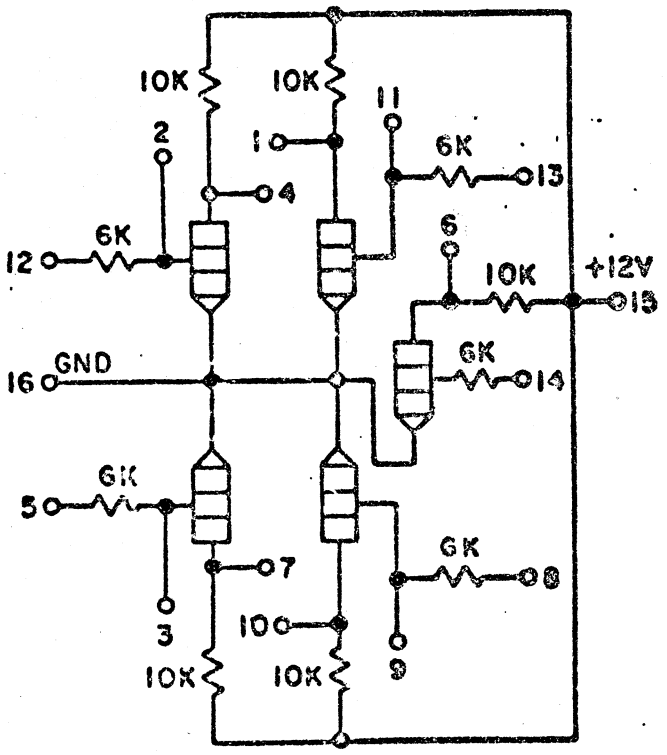
2-5 WAY AI — 361416



2-3A / 1A - 2 OR AI — 361417



4II / DCI - II — 361418



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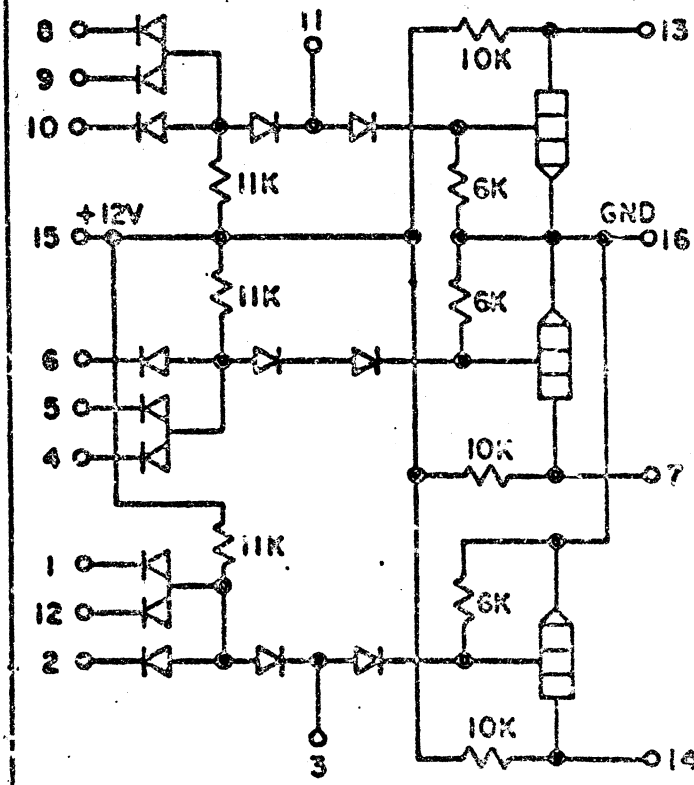
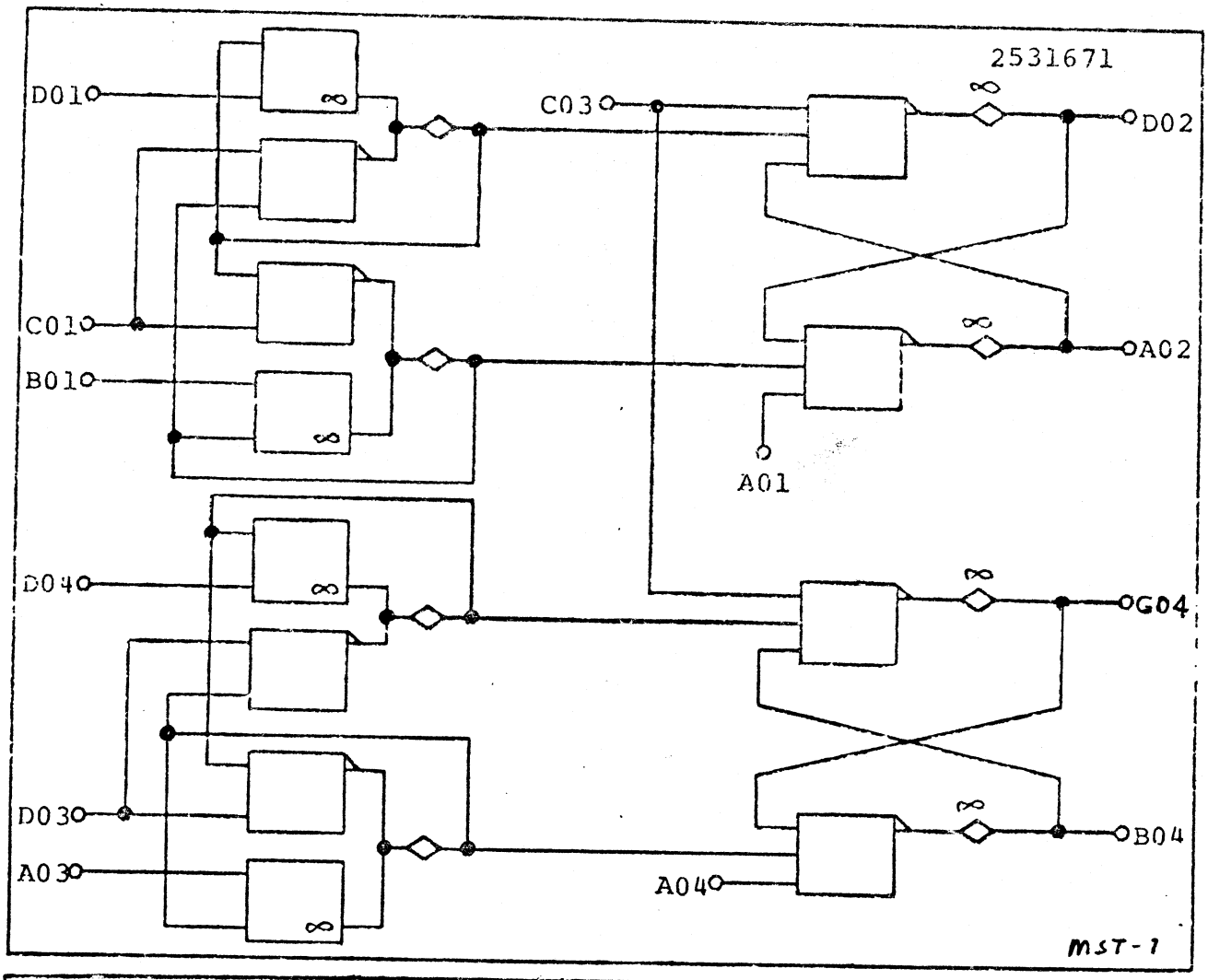
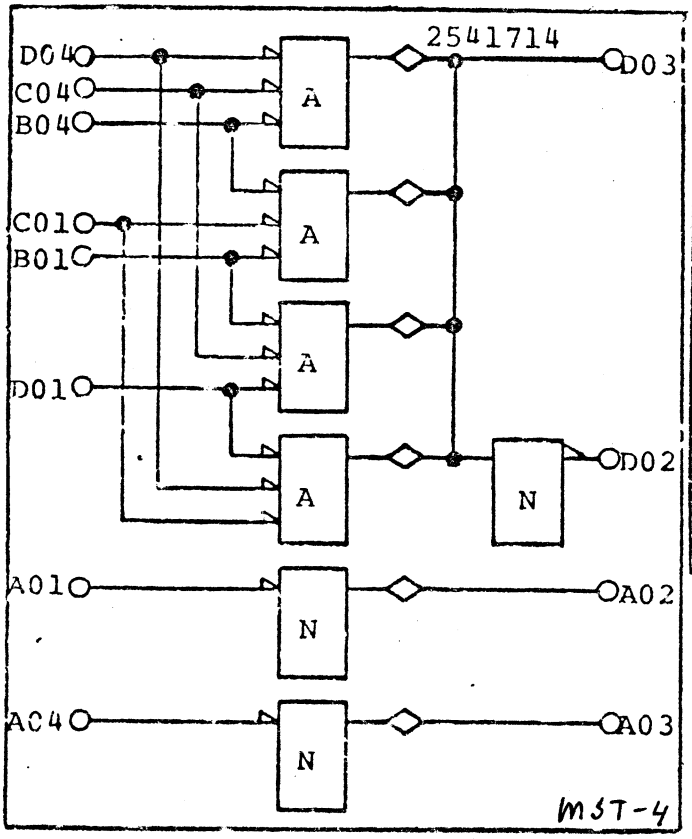
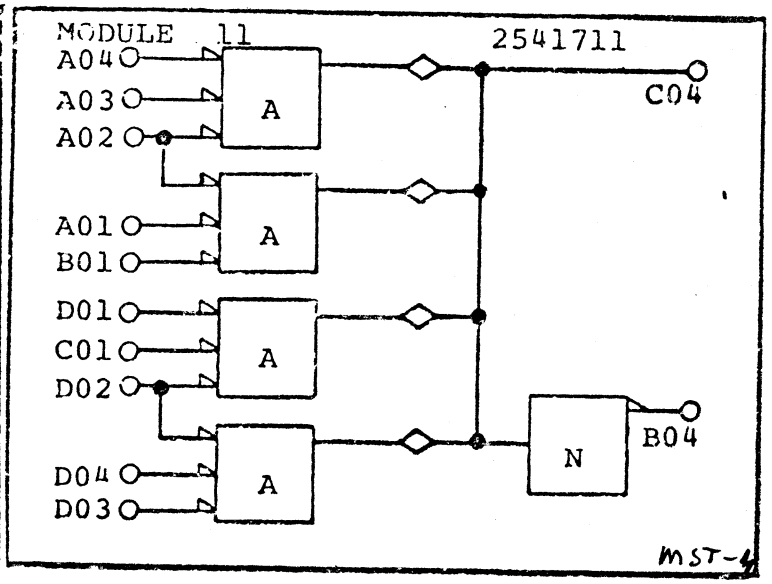


MST 1, 2 & 4 MODULE SCHEMATICS

CARD GROUND RULES	DEP	2-6230	3
SECTION 10E	Cat	Subject	Suffix







Date	Page
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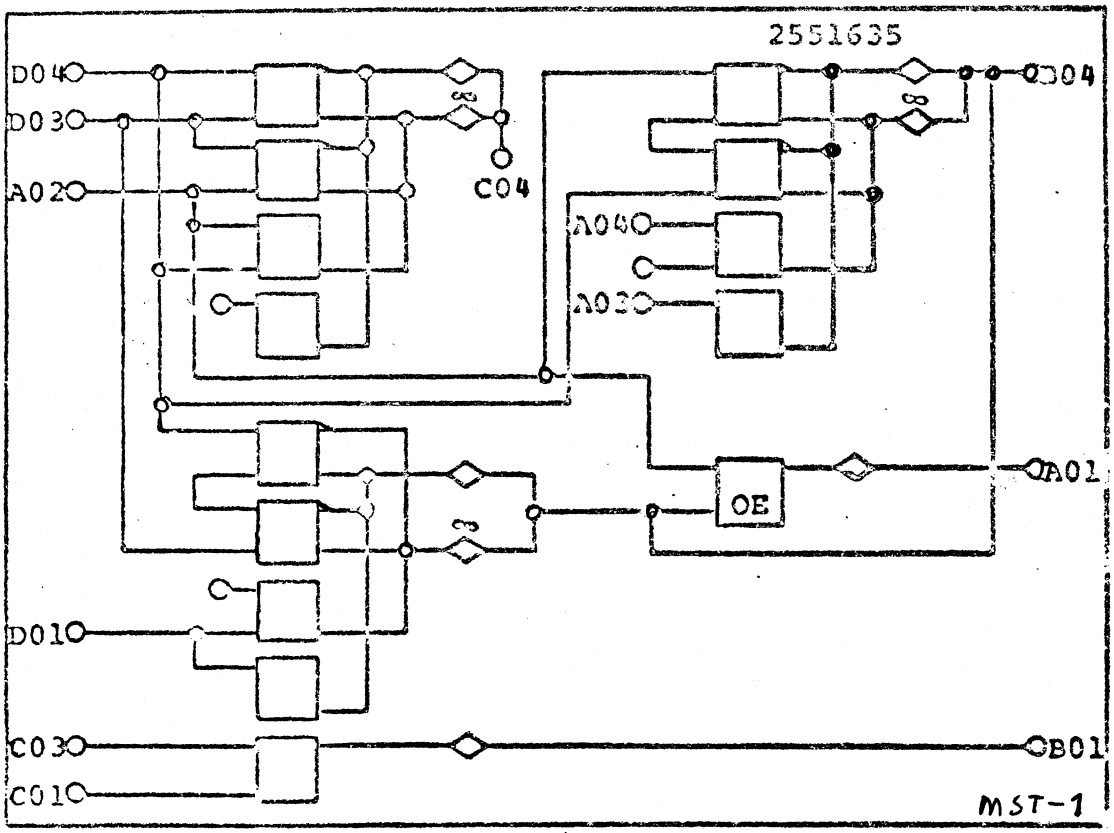
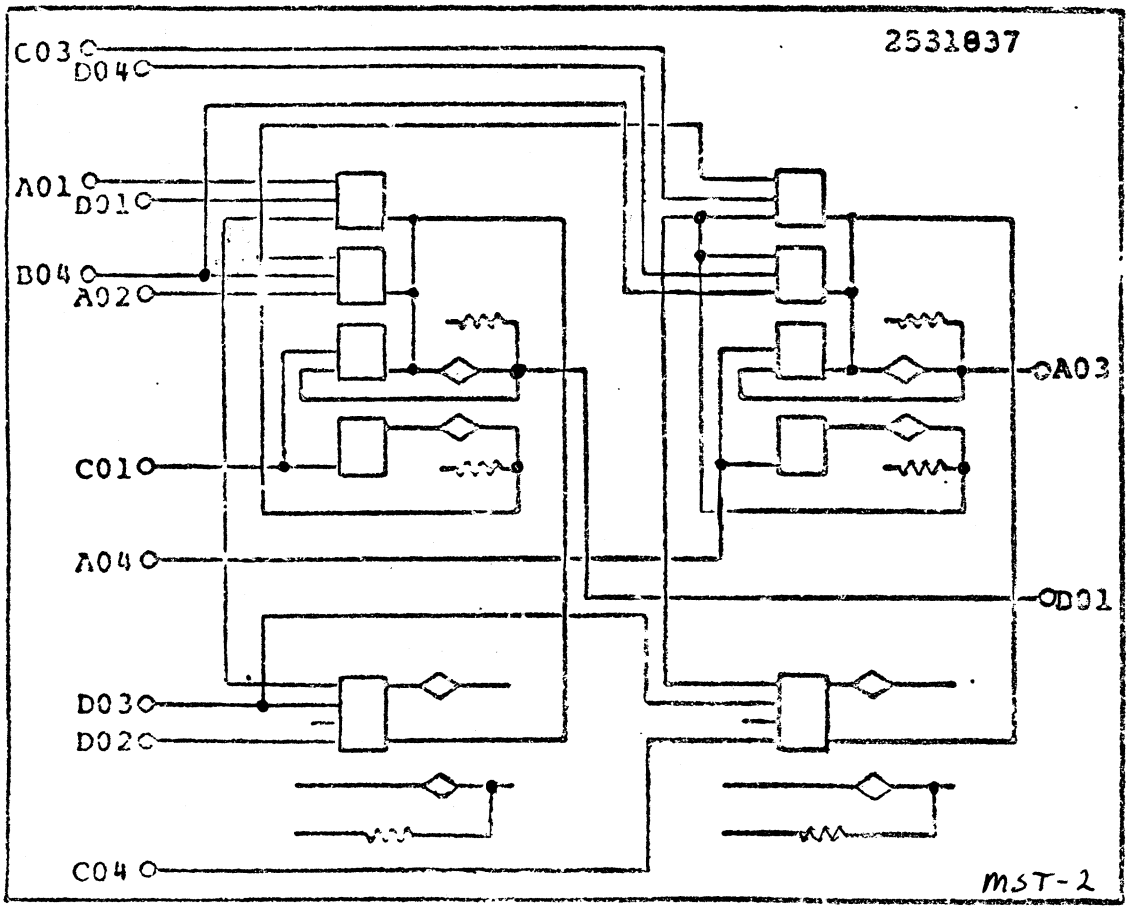
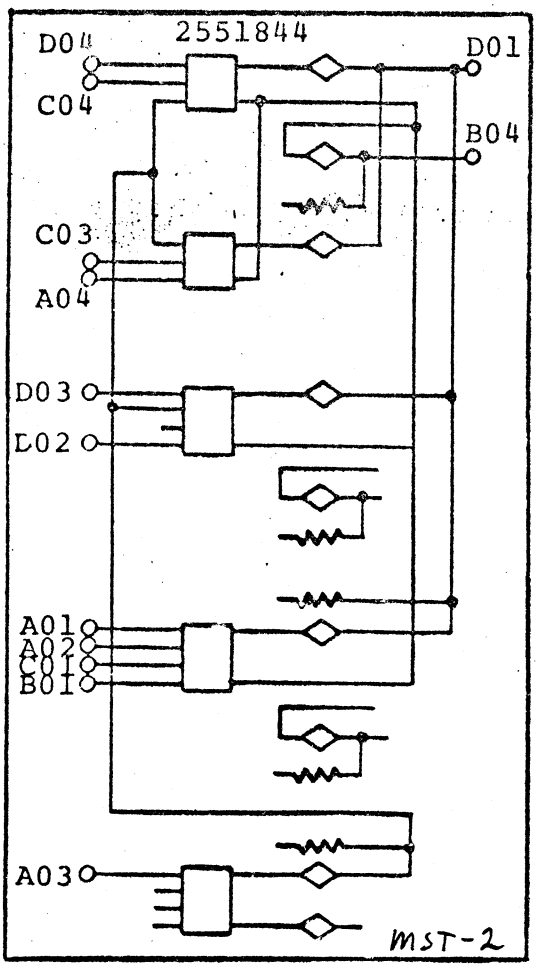
MST 1, 2 & 4 MODULE SCHEMATICS



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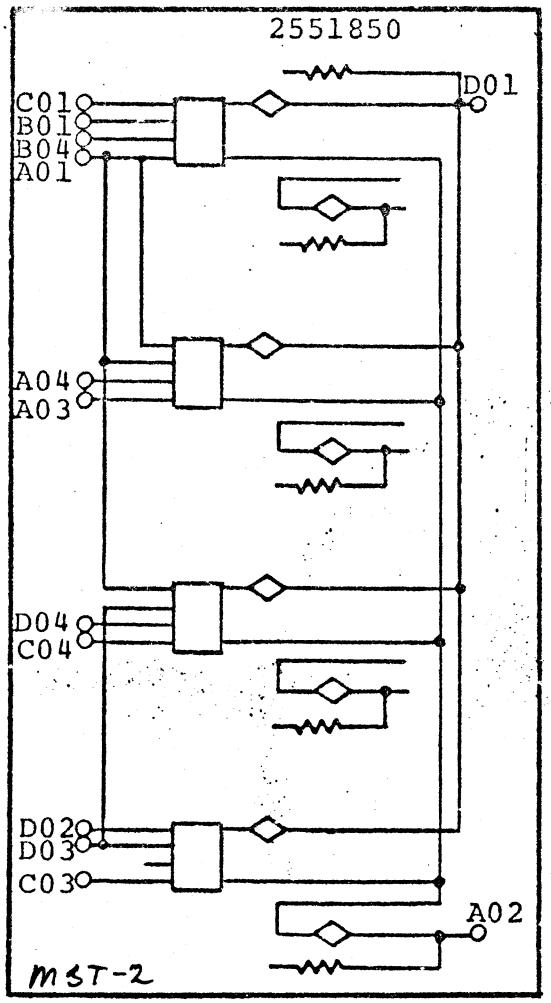
MST-2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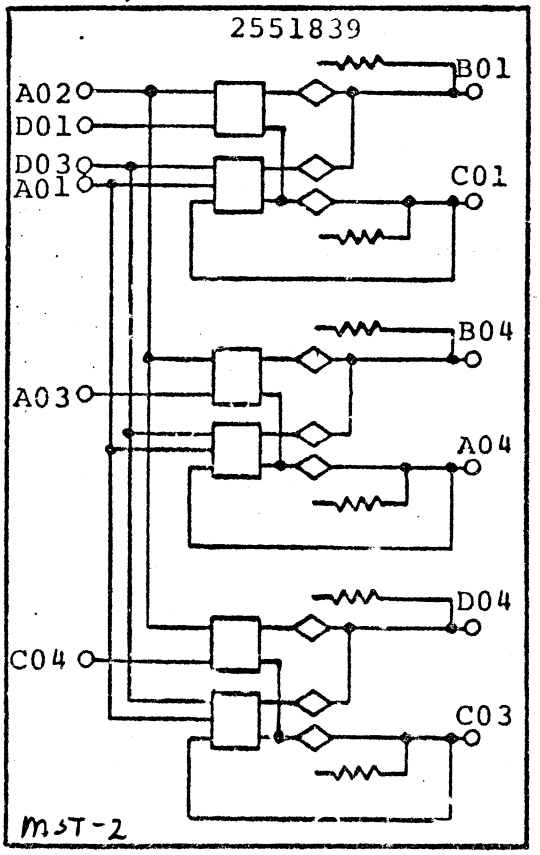
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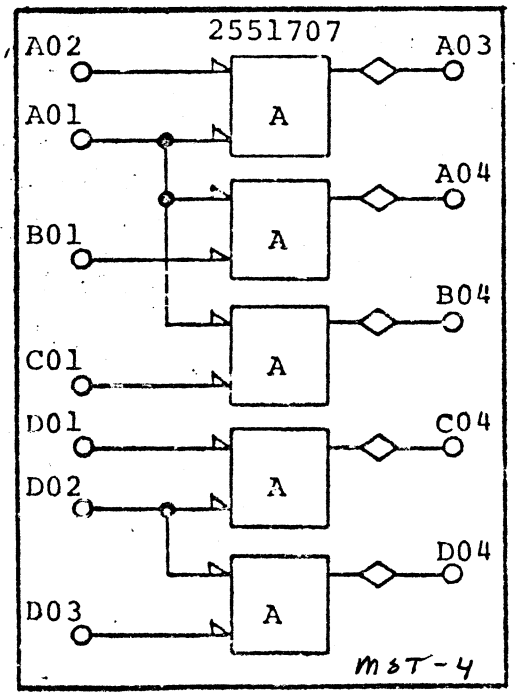
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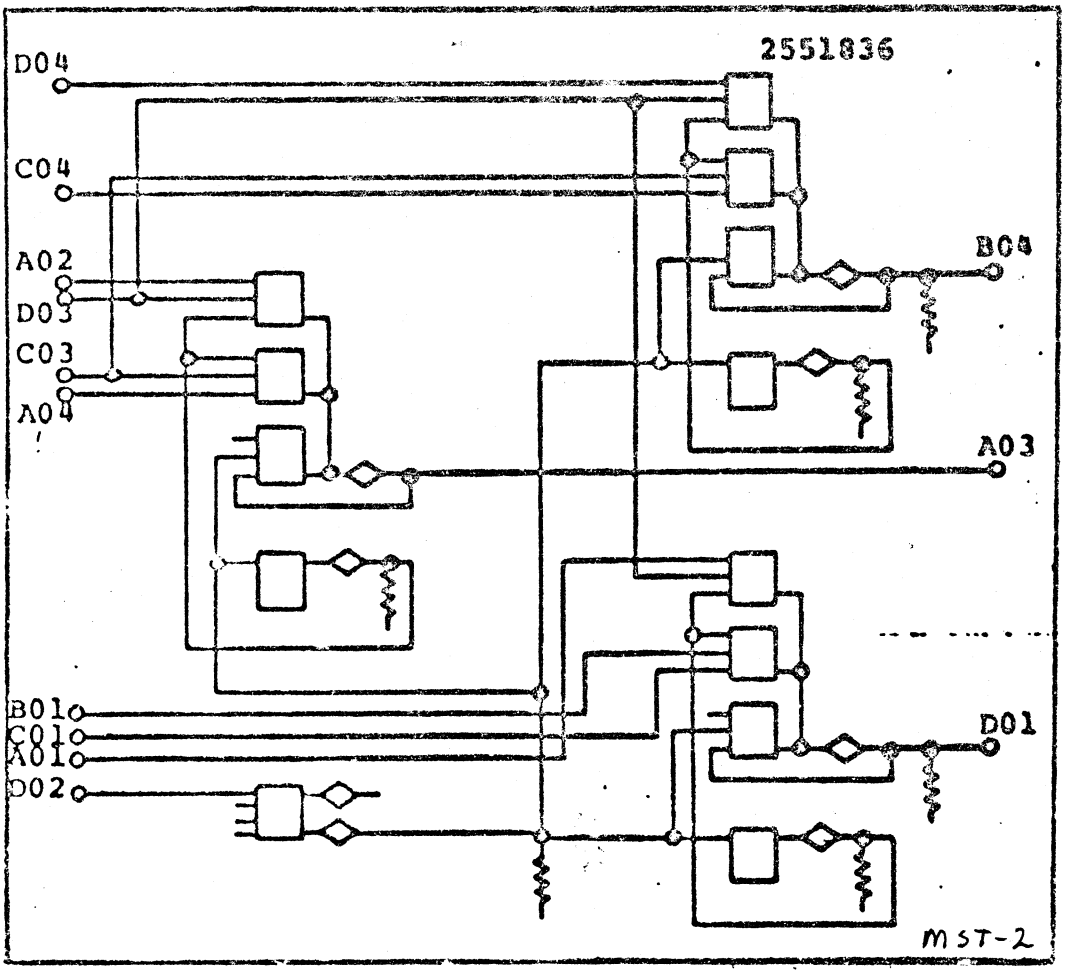
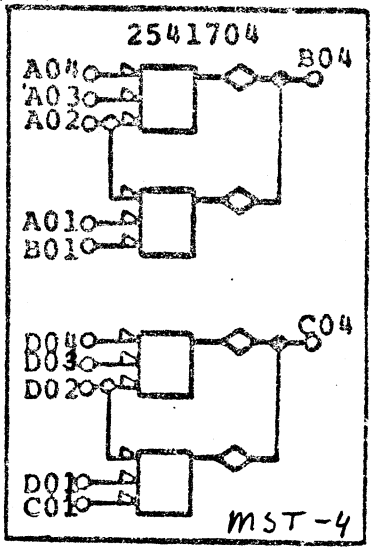
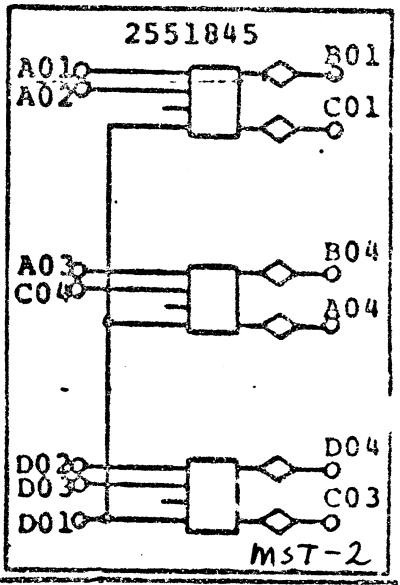
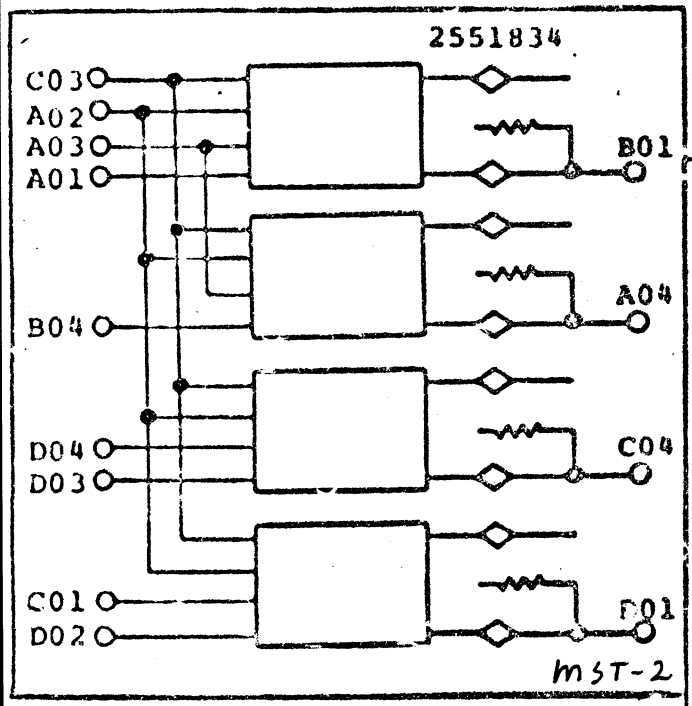
MST-4

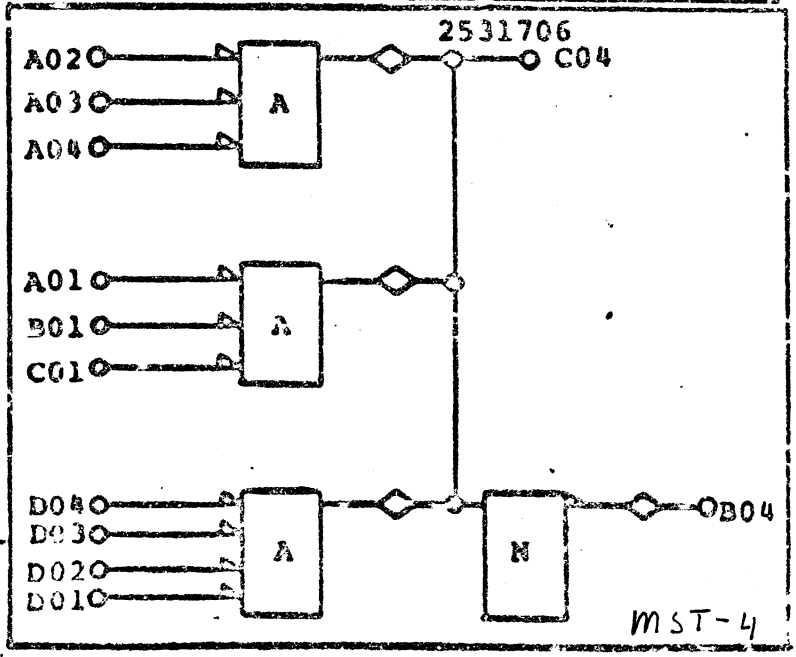
MST 1; 2 & 4 MODULE SCHEMATICS











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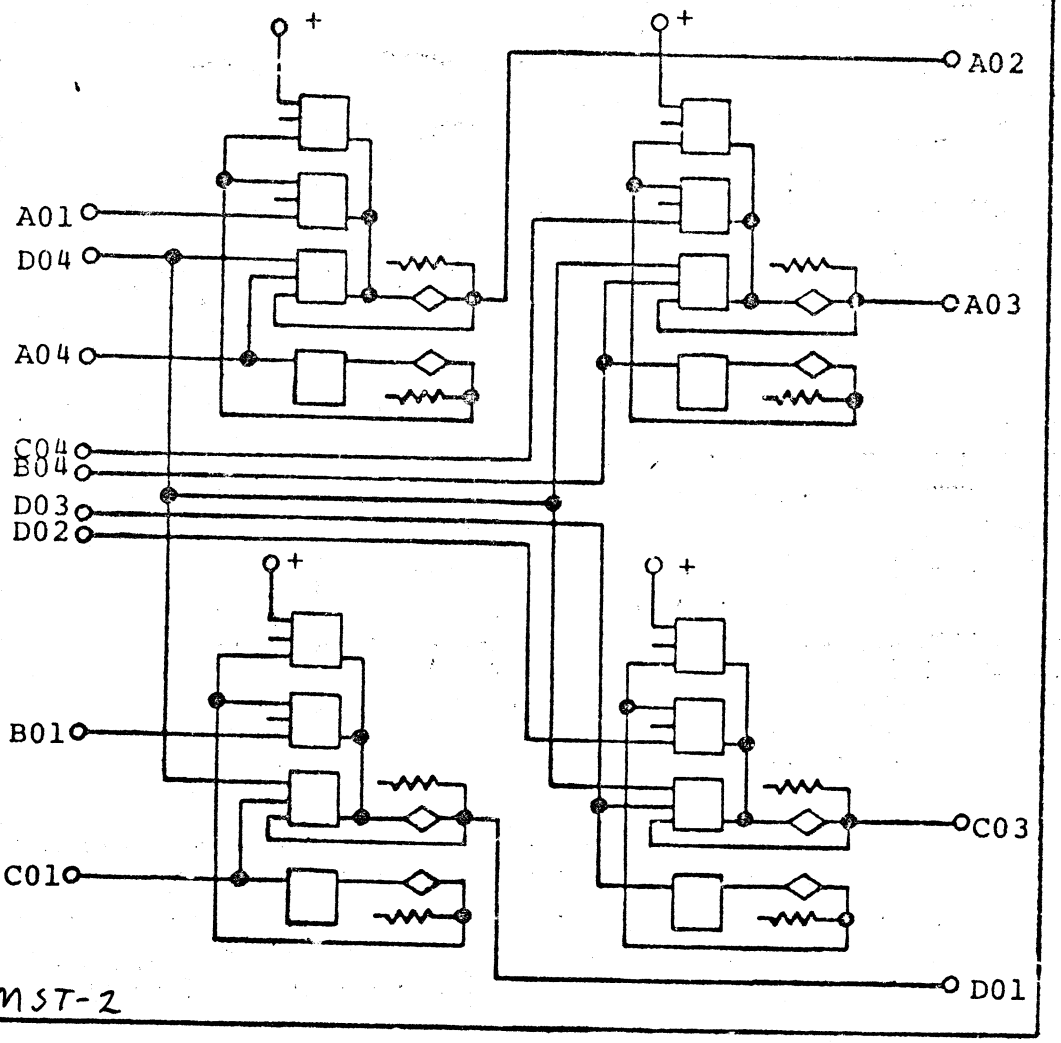

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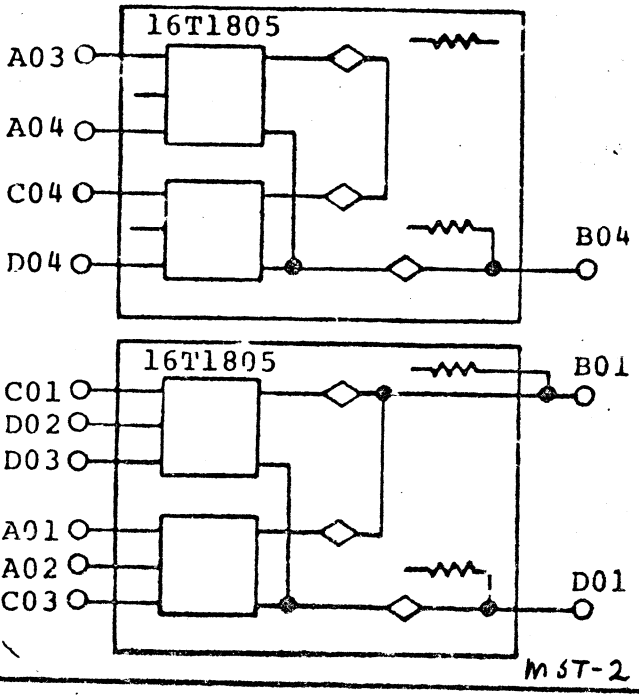

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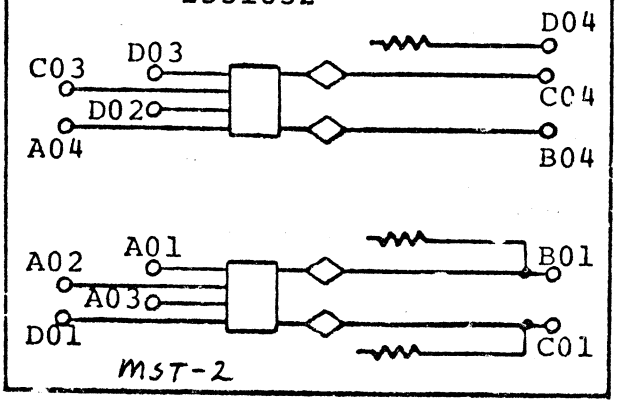
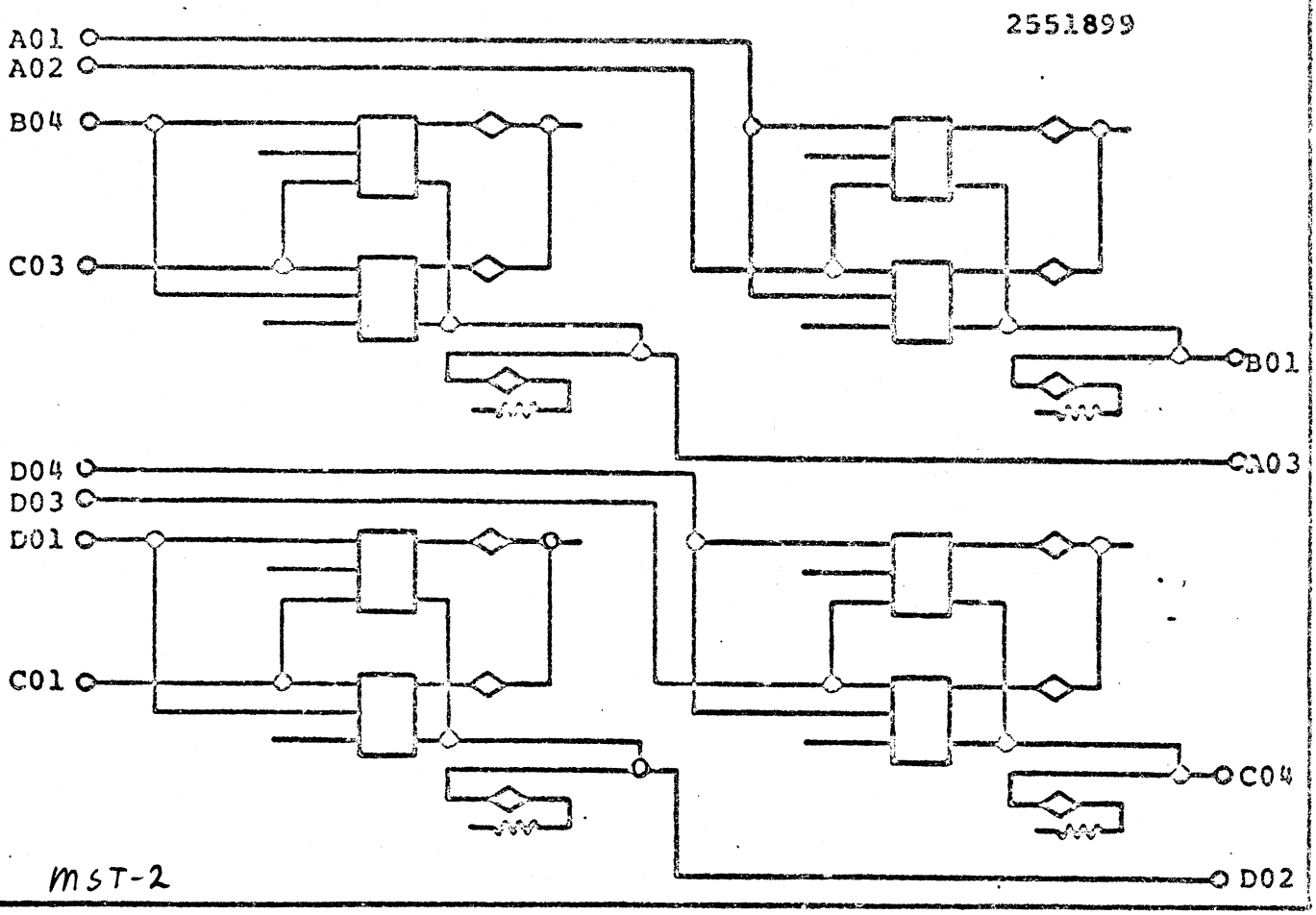


MST 1, 2 & 4 MODULE SCHEMATICS

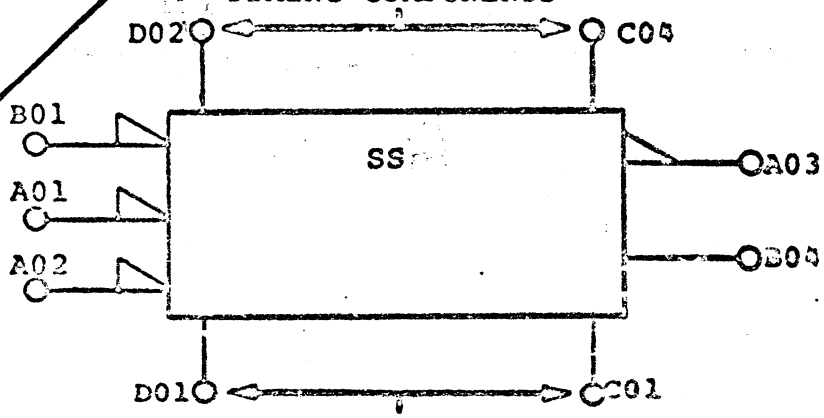
2551899



MST-2

2551652

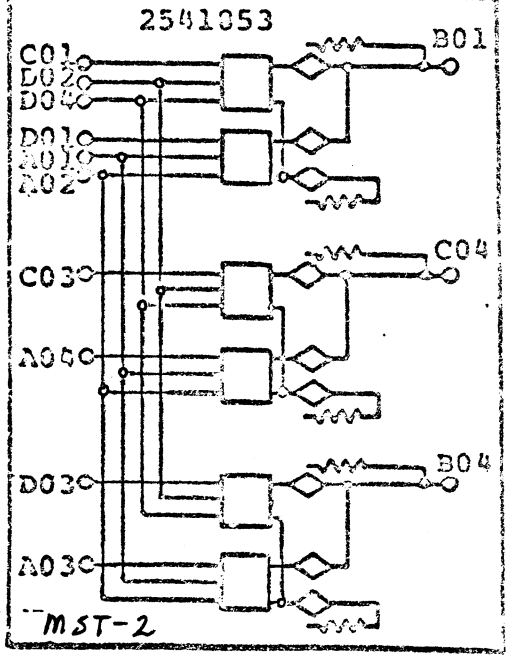
CONNECTION FOR EXTERNAL TIMING COMPONENTS



CONNECTION FOR OPTIONAL SPEED-UP FUNCTION

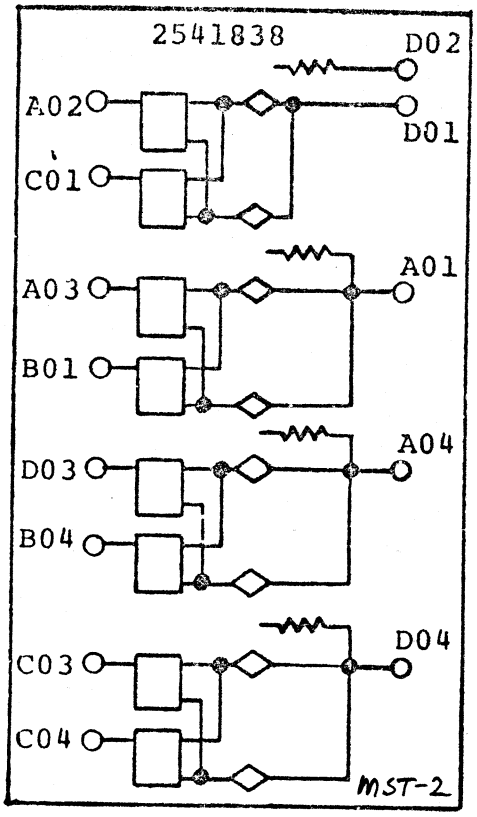
MST-1

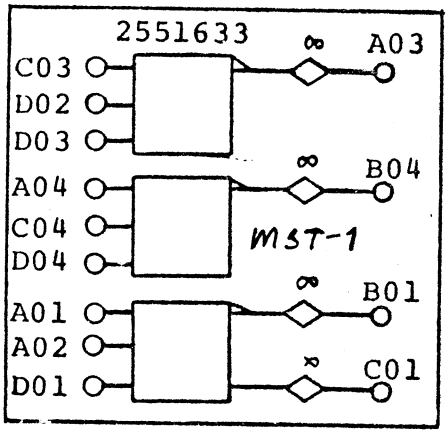
2541053

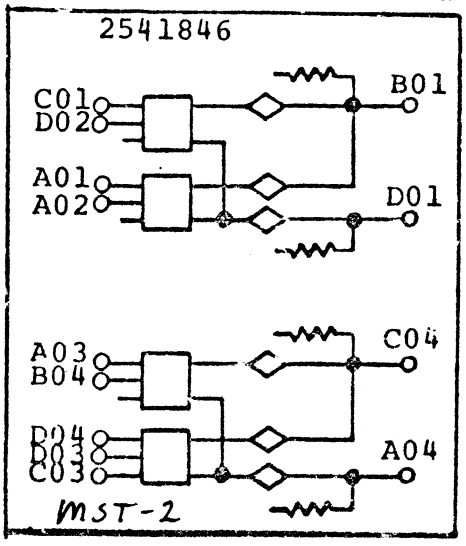


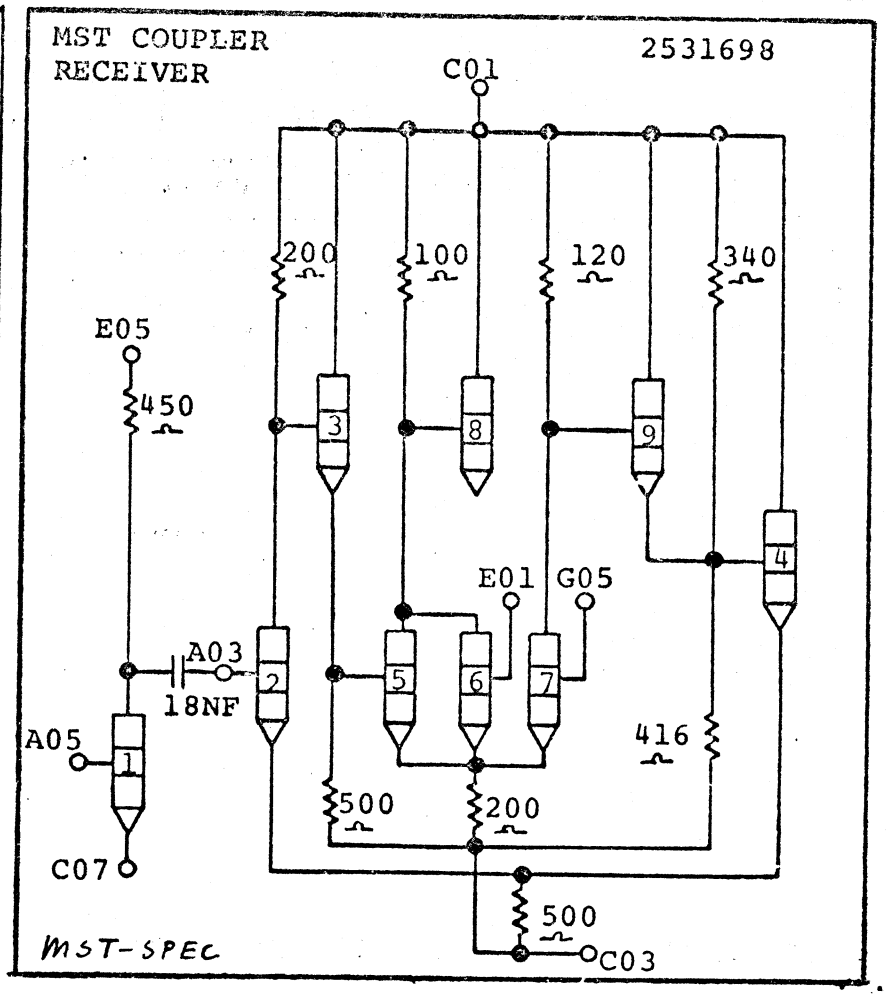
MST-2

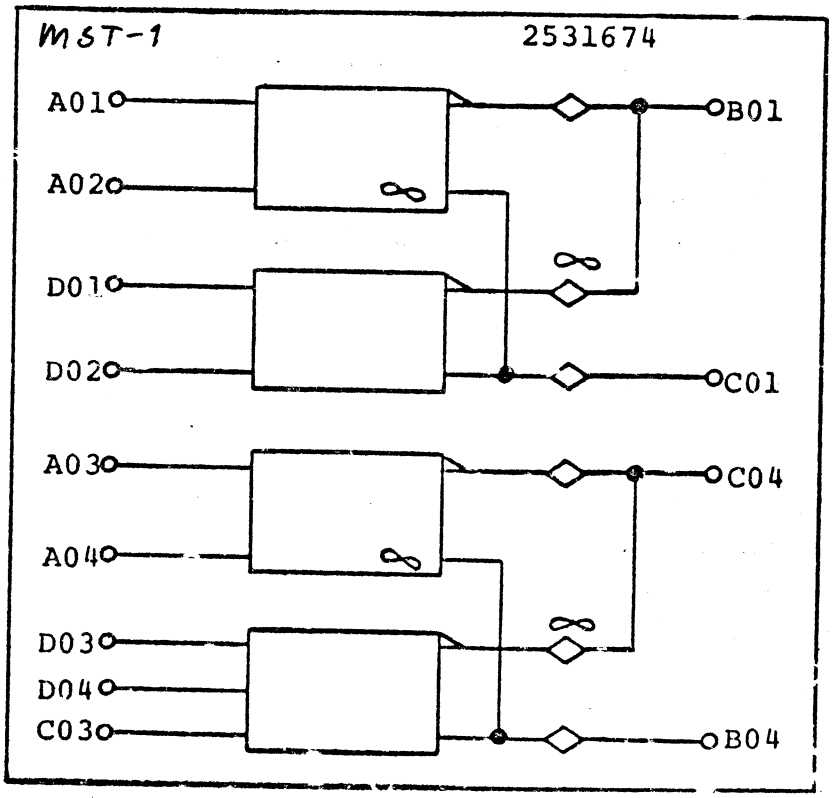
MST 1, 2 & 4 MODULE SCHEMATICS











MST 1, 2 & 4 MODULE SCHEMATICS

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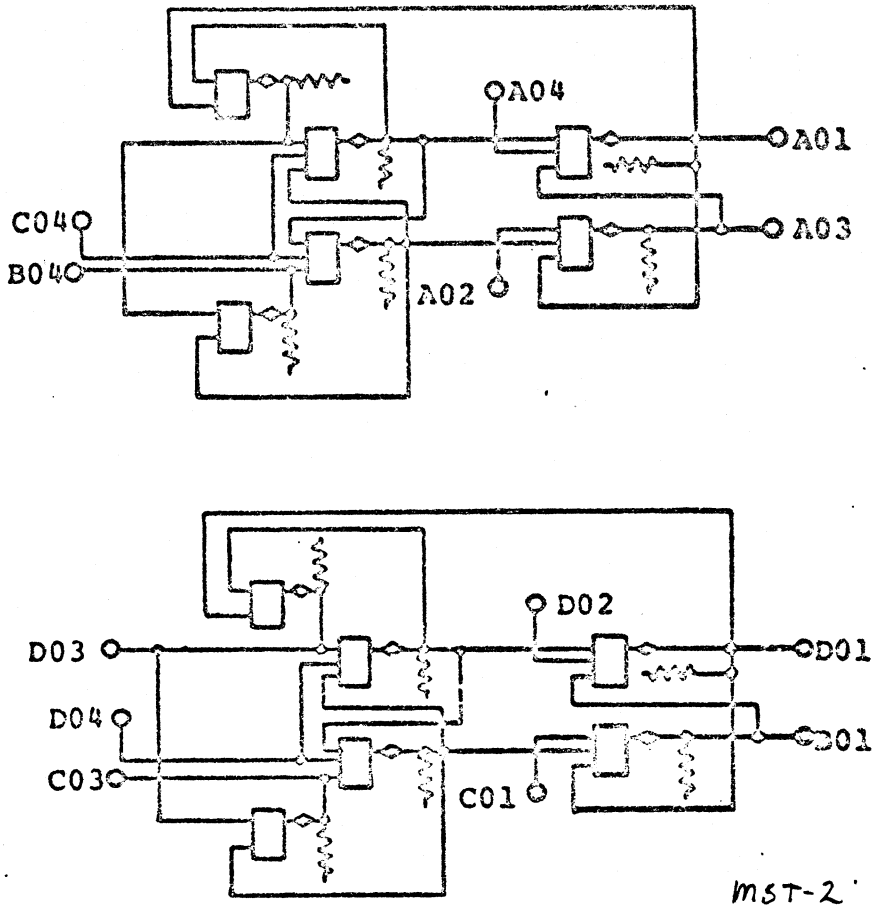

MST-2

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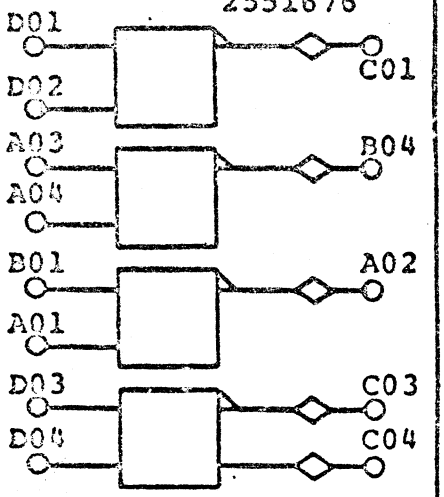

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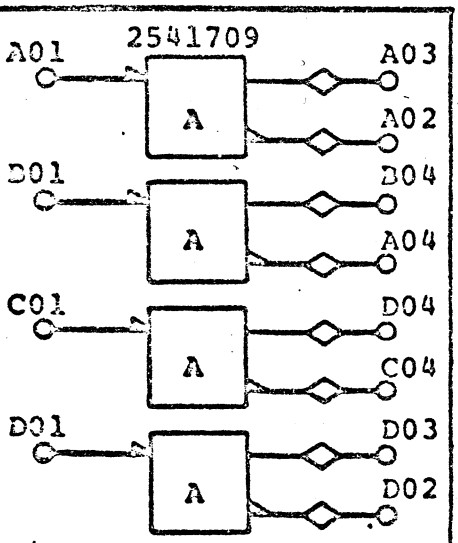

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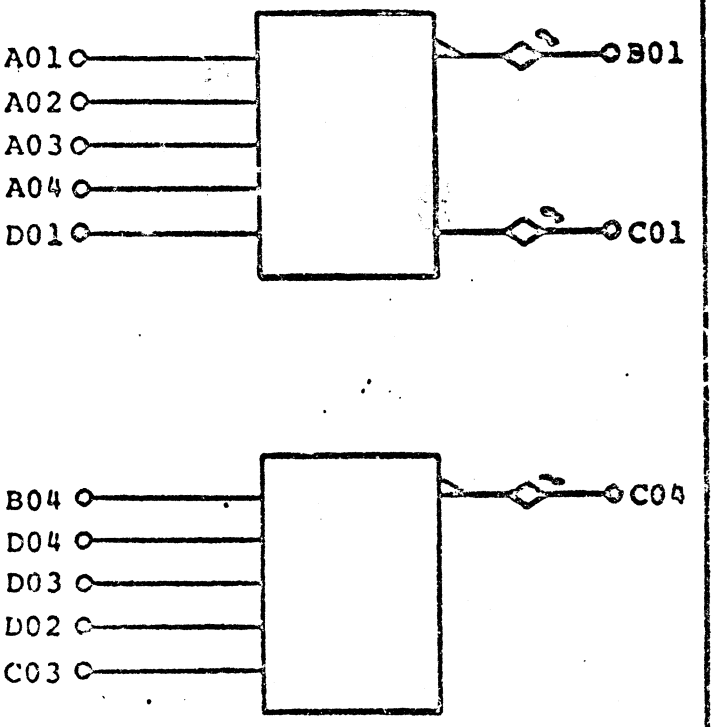

MST-1

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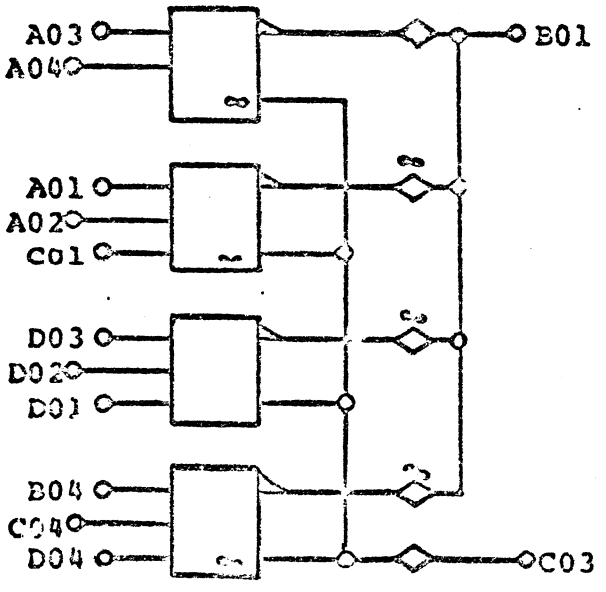
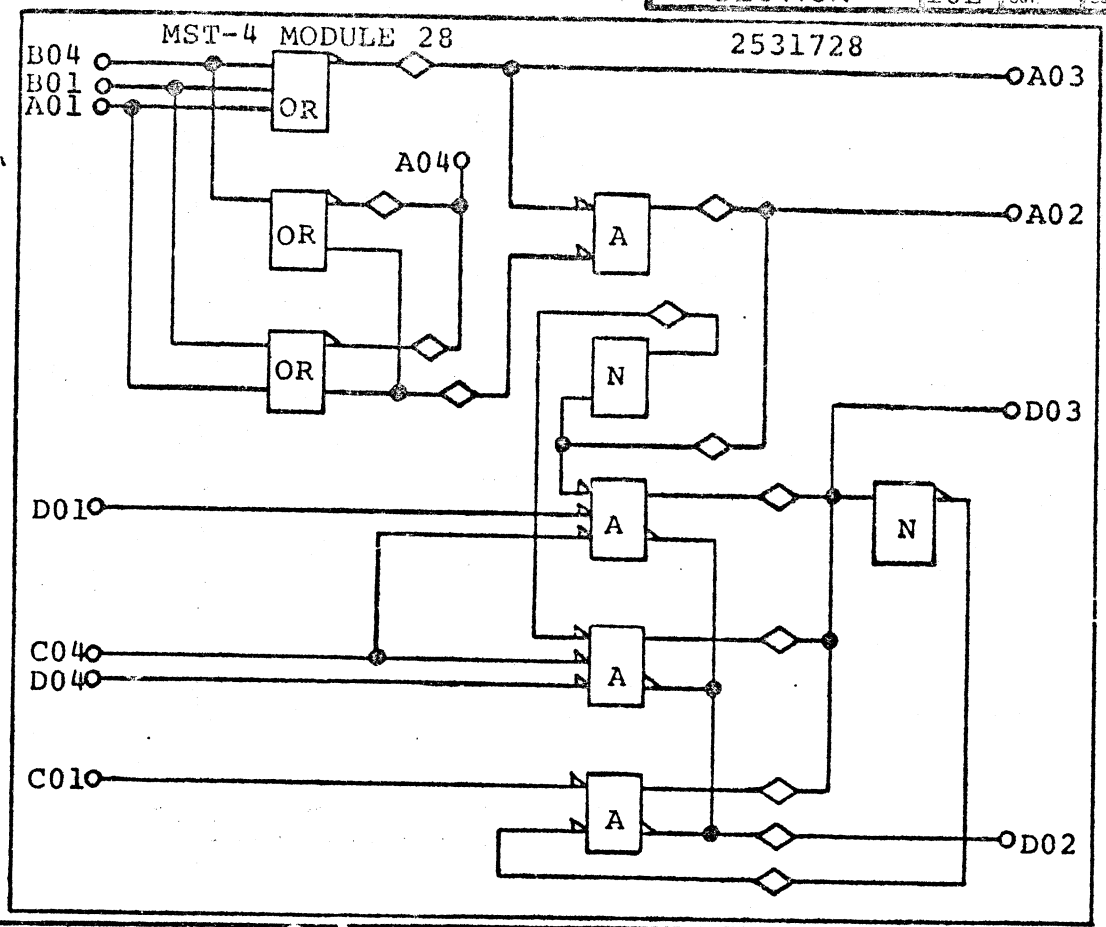
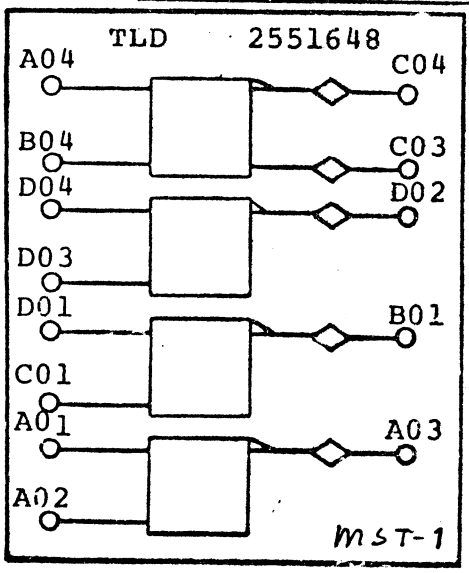


MST-1


MST-4 MODULE 28
2531728
B04
B01
A01
OR
OR
OR
A04
A
A
N
N
D01
C04
D04
C01
A03
A02
D03
D02


TLD
2551648
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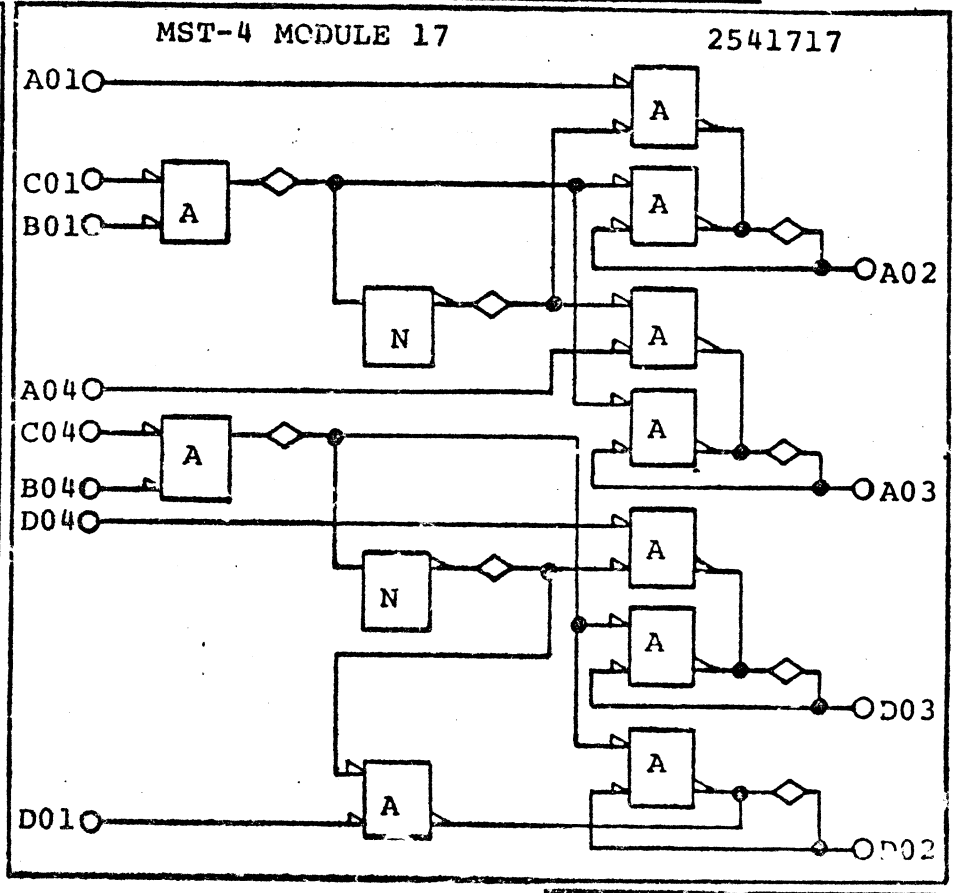
B04
D04
D03
D01
C01
A01
A02
C04
C03
D02
B01
A03
MST-1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C01
B01
A04
C04
B04
D04
D01
A
A
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A
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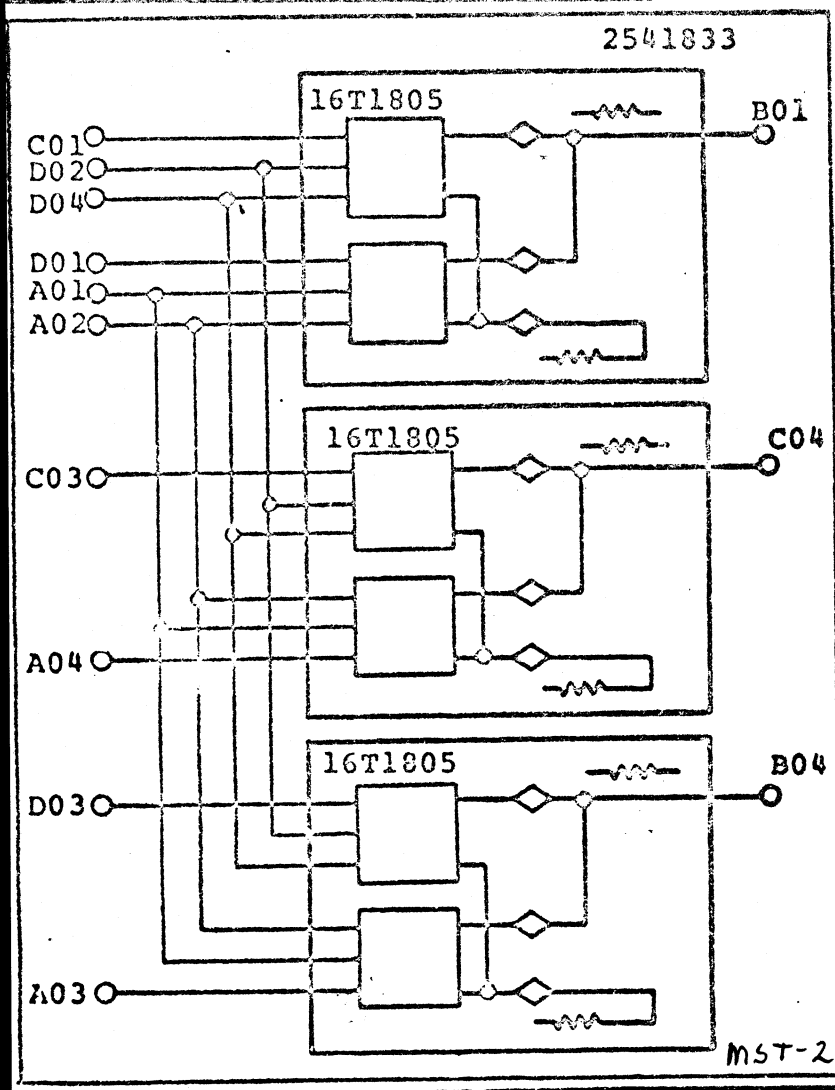
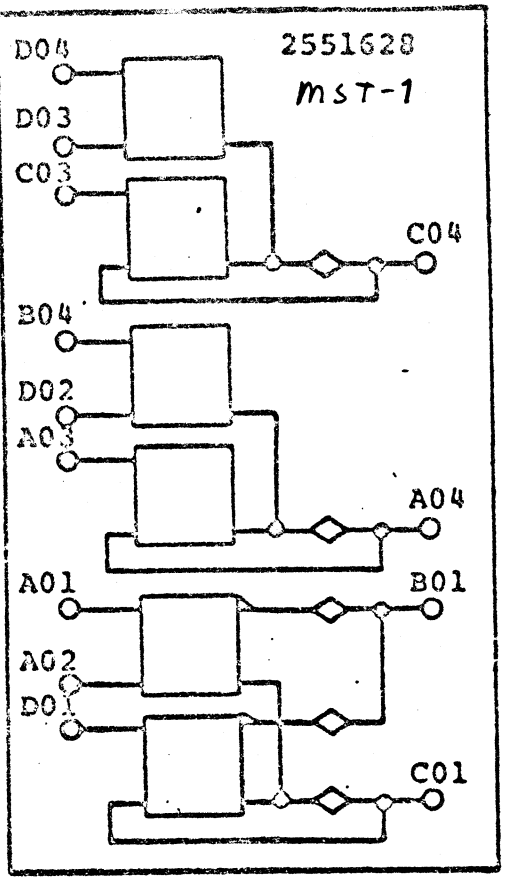
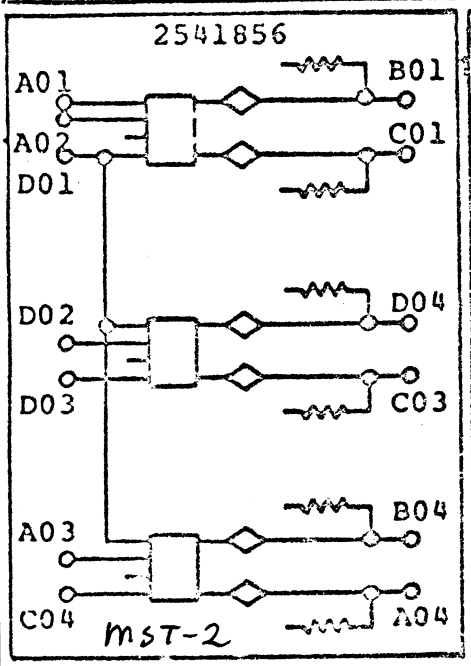
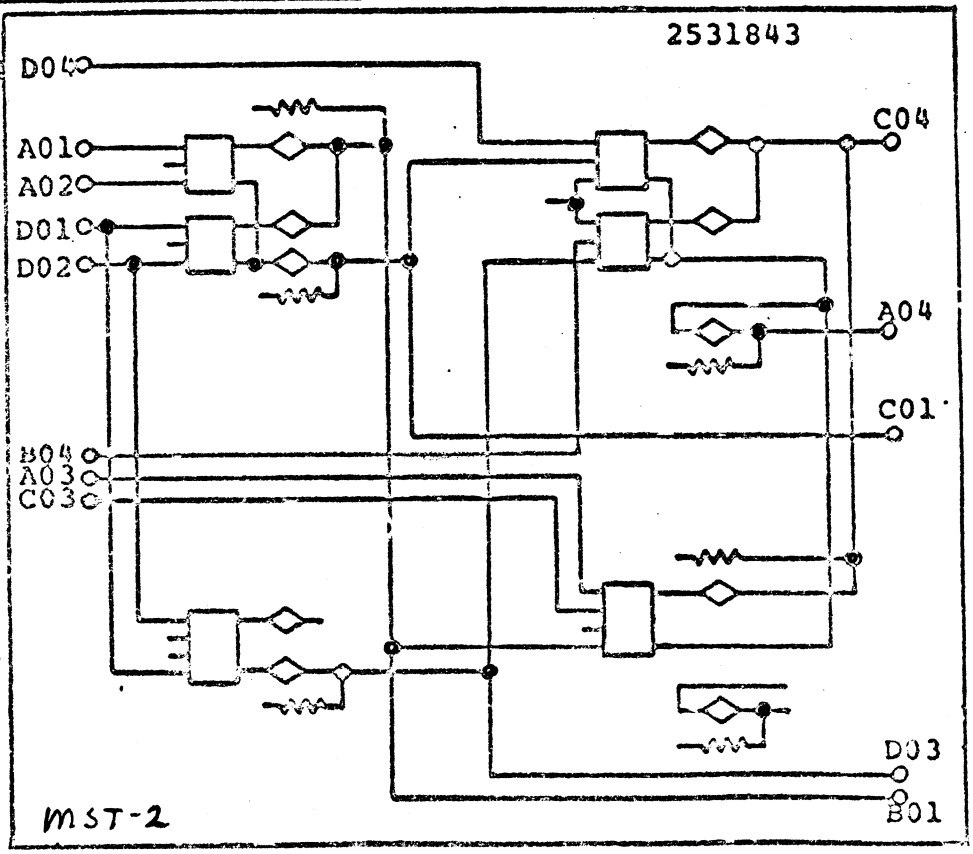
N
N
A02
A03
D03
D02

MST 1, 2 & 4 MODULE SCHEMATICS

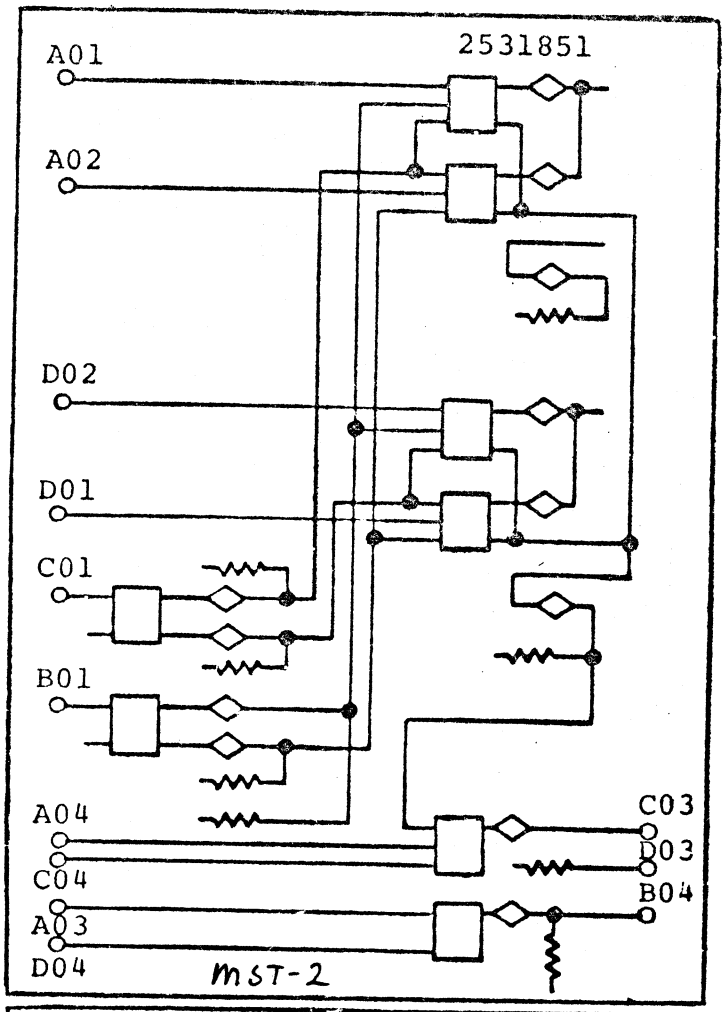


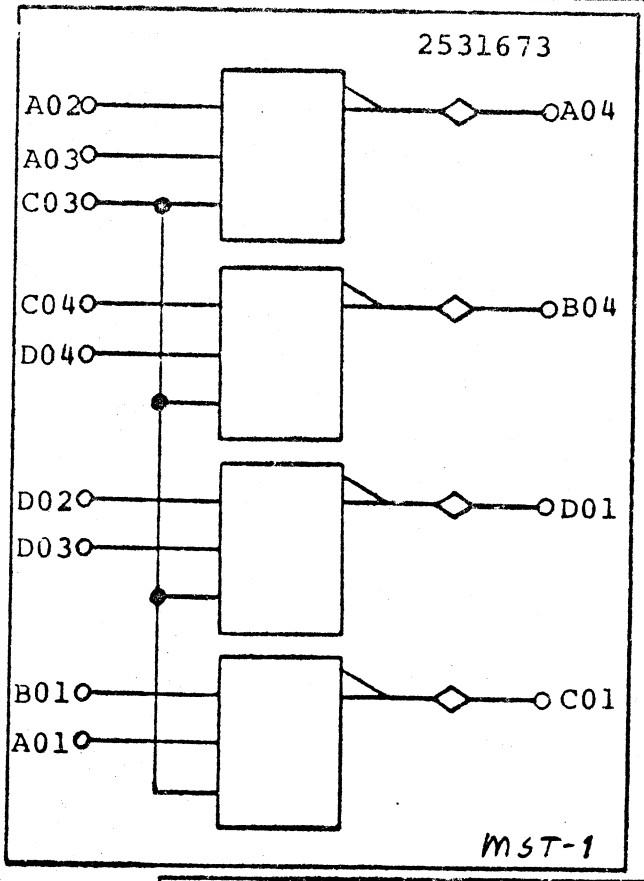


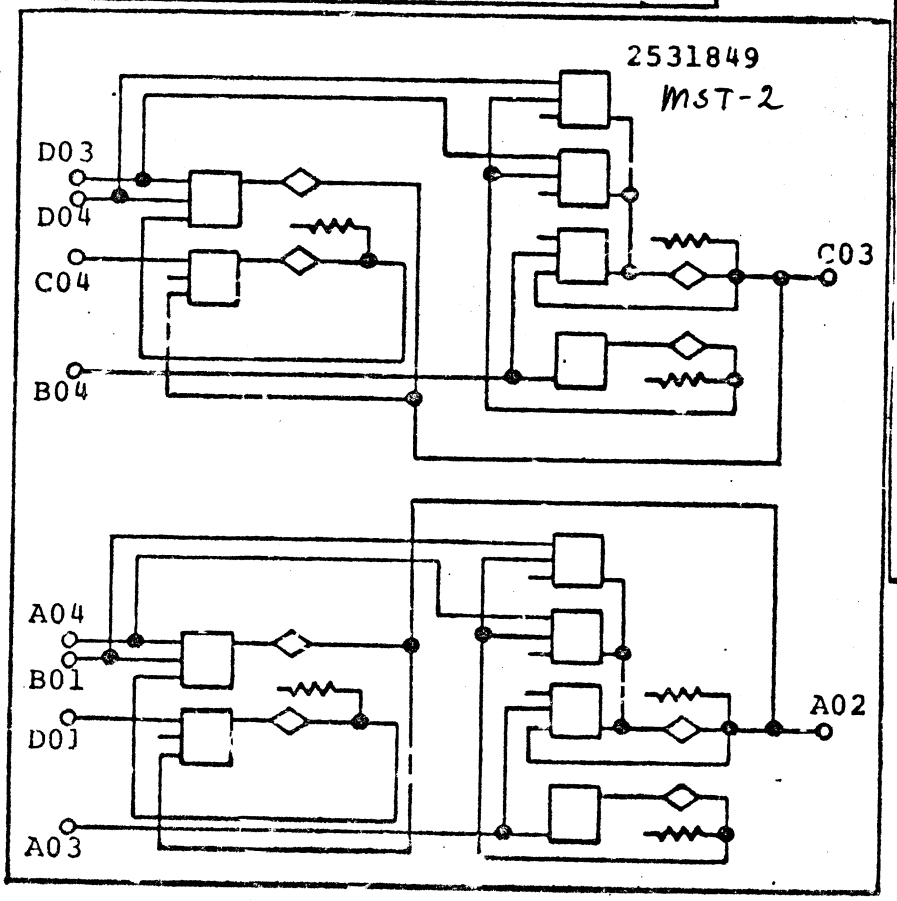


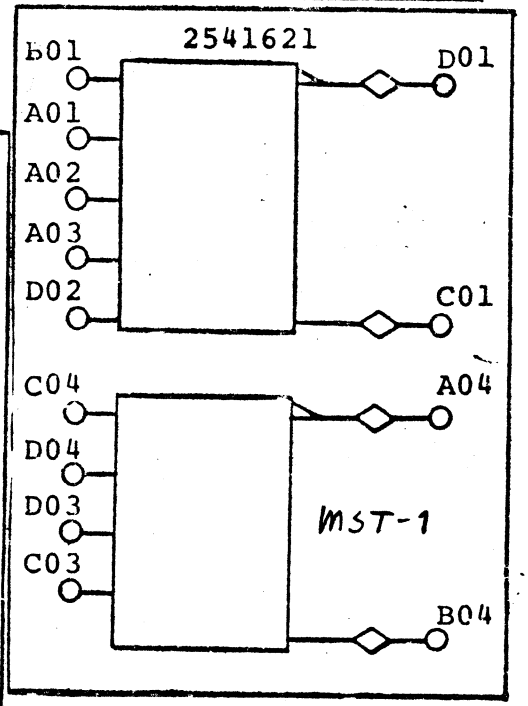


MST 1, 2 & 4 MODULE SCHEMATICS

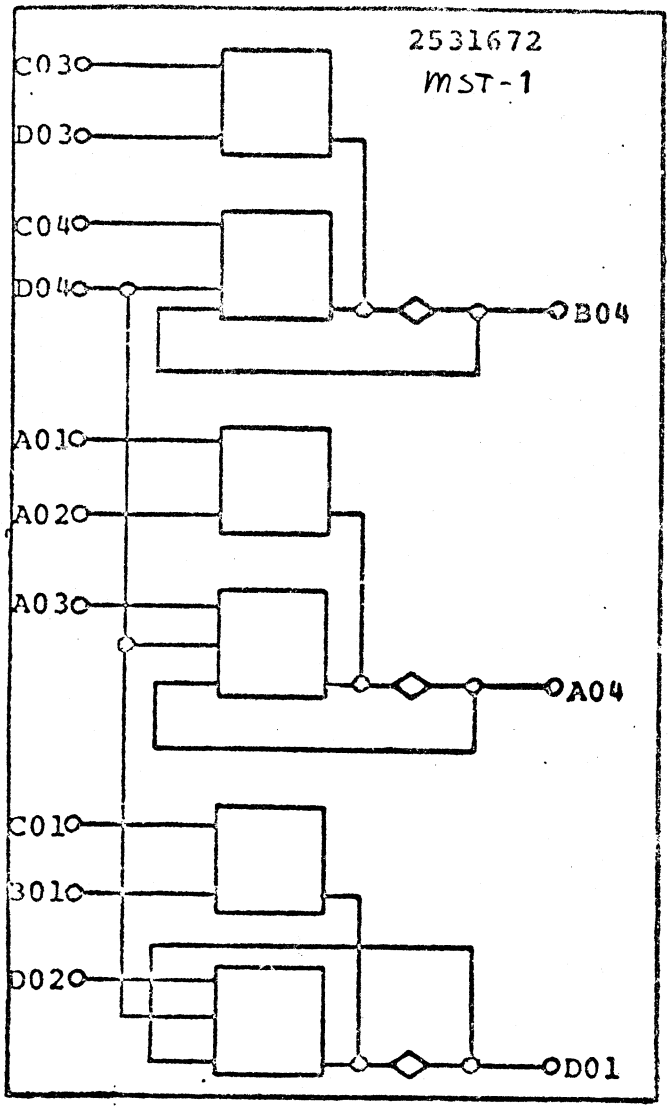


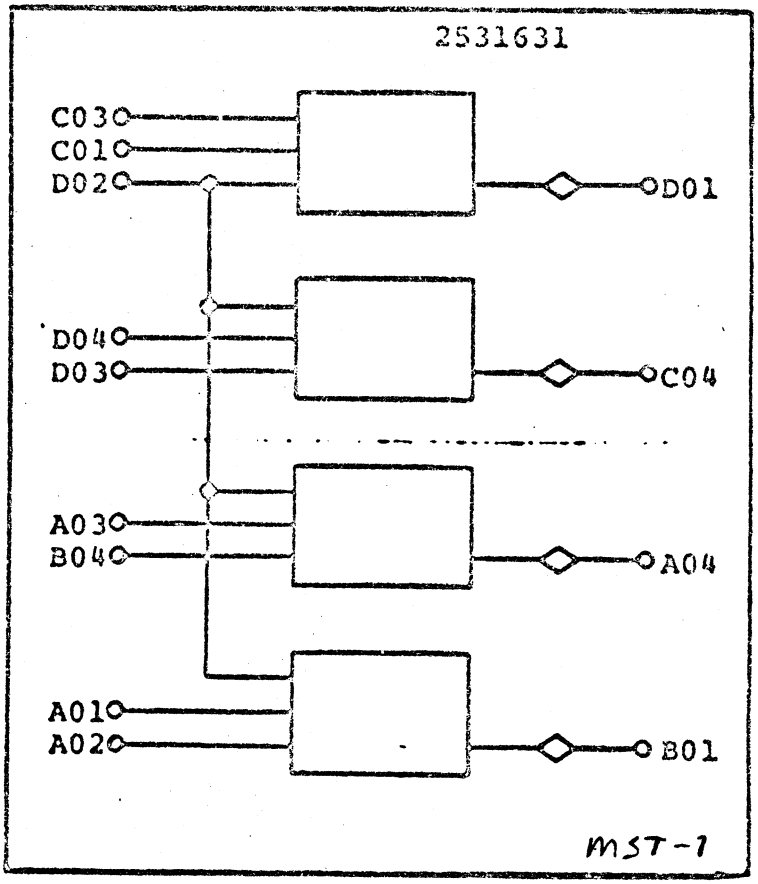


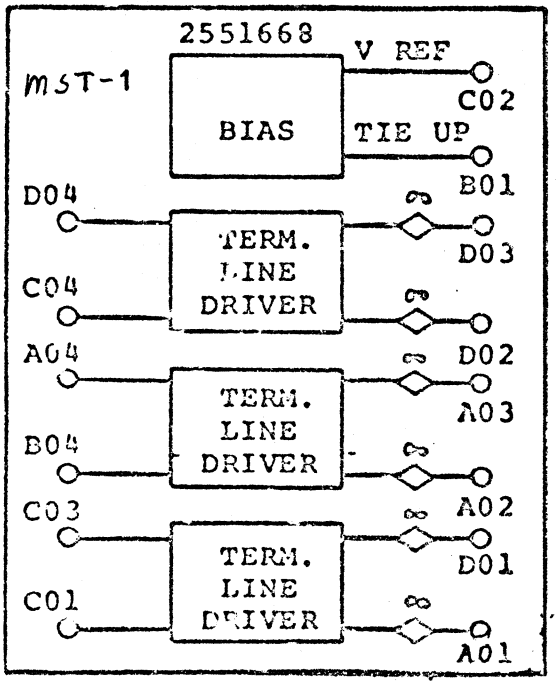


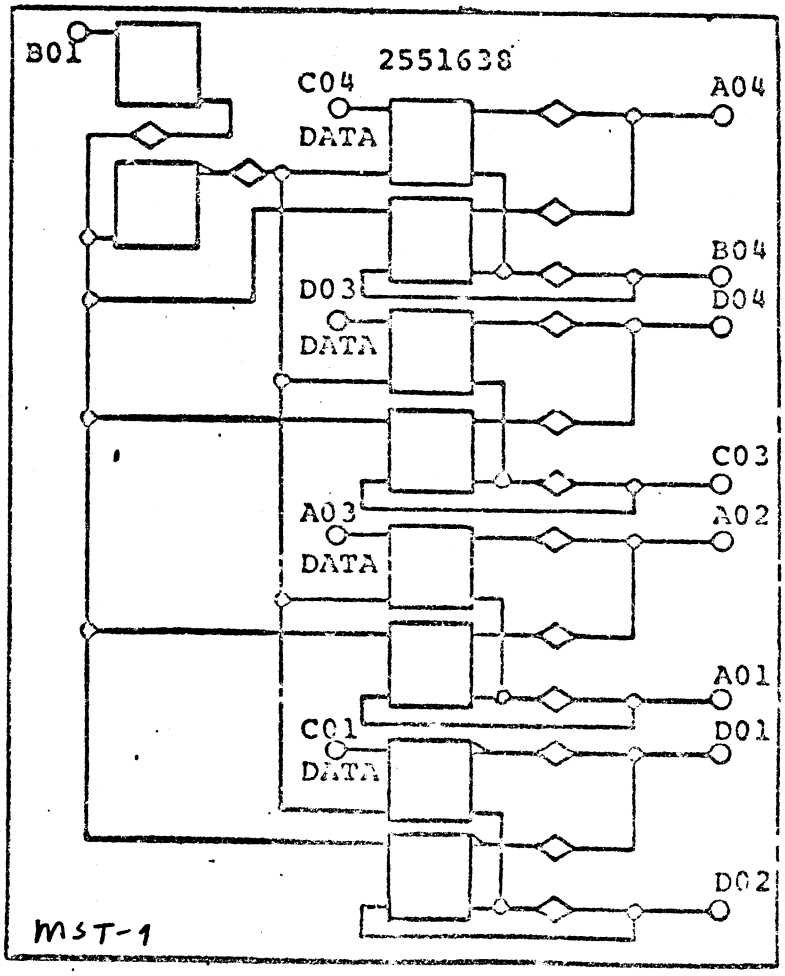


MST 1, 2 & 4 MODULE SCHEMATICS

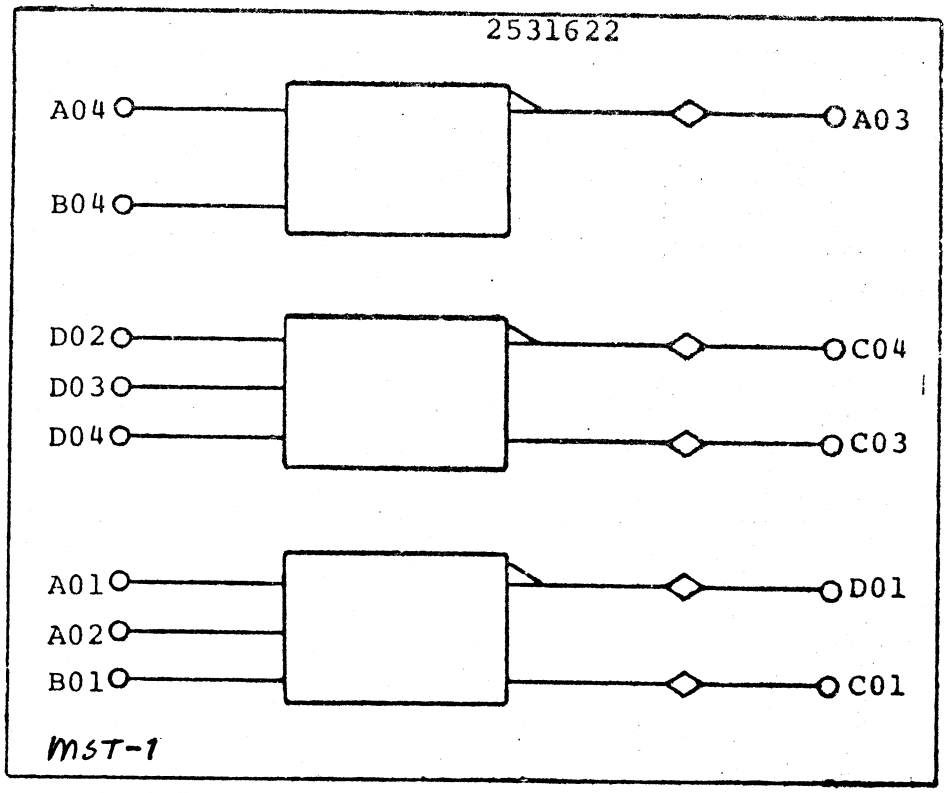


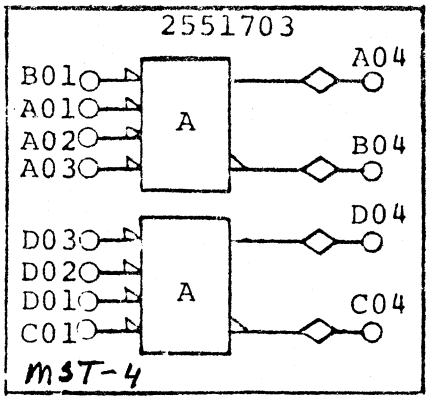


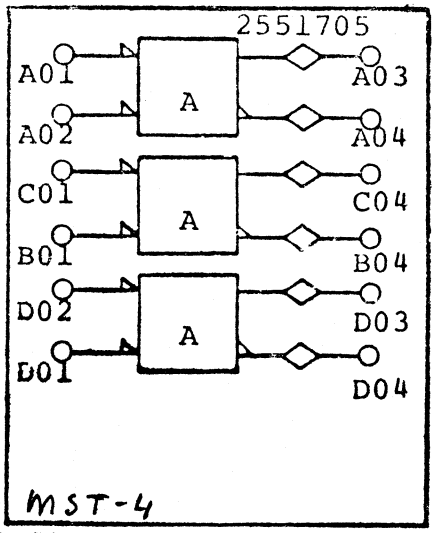


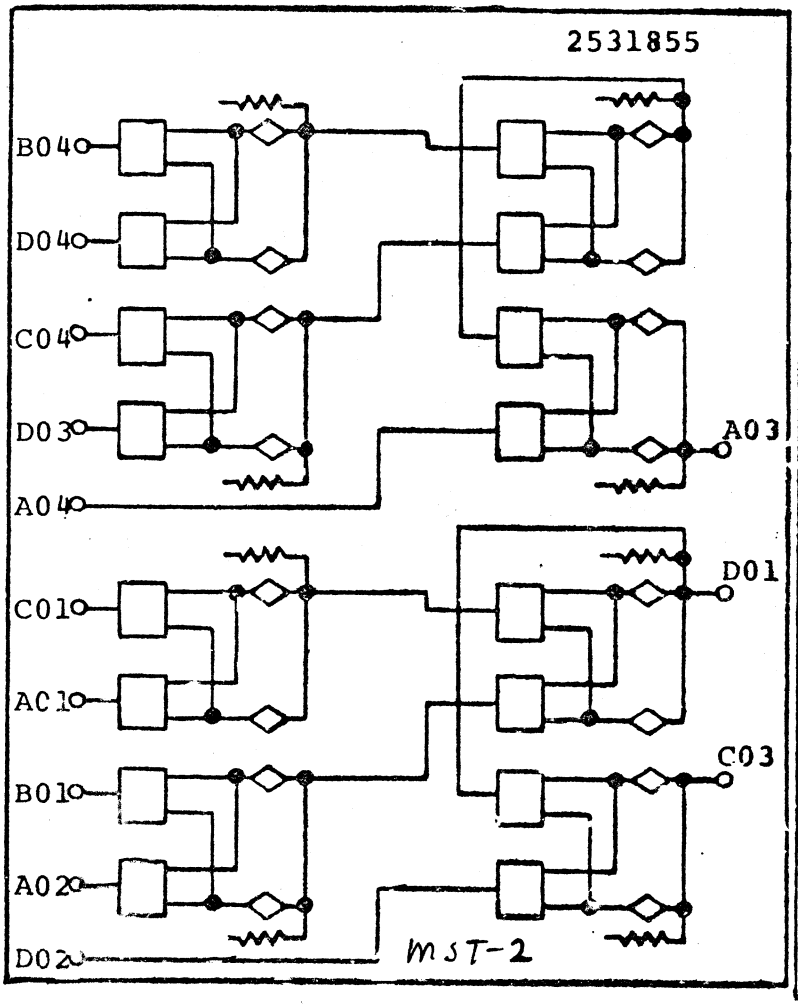


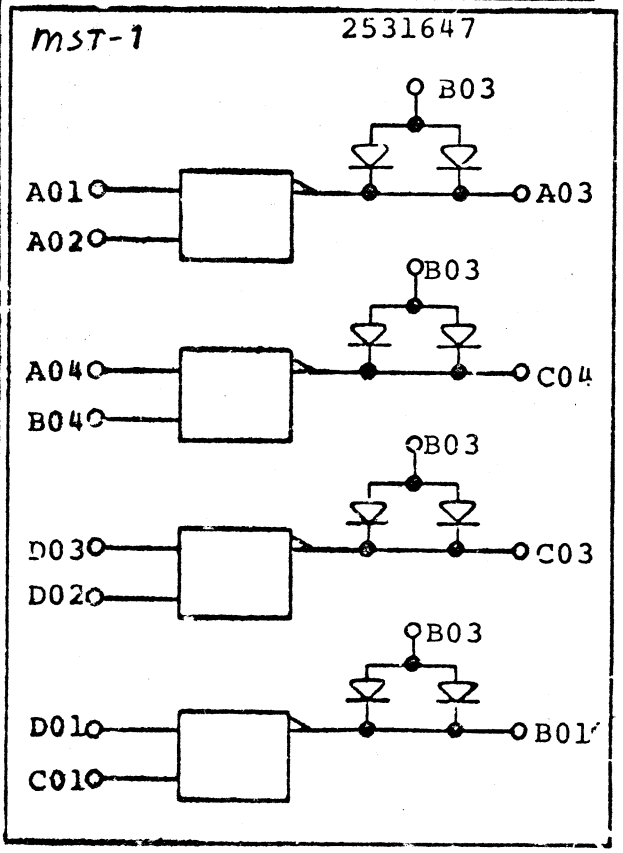
MST 1, 2 & 4 MODULE SCHEMATICS



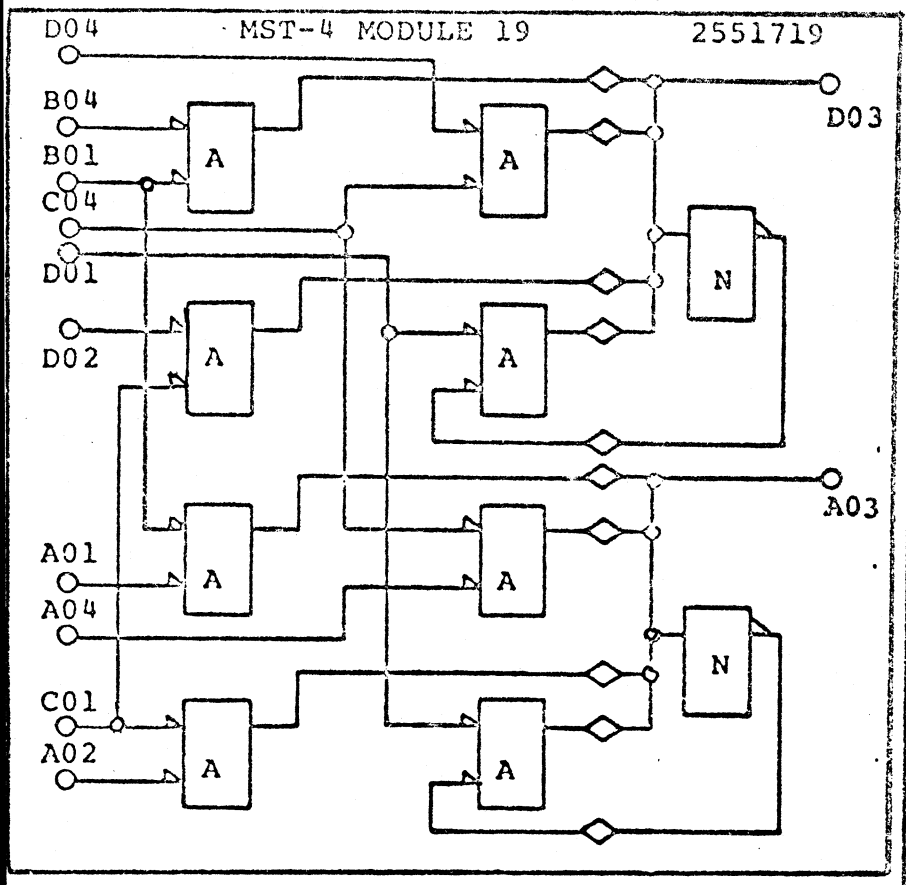


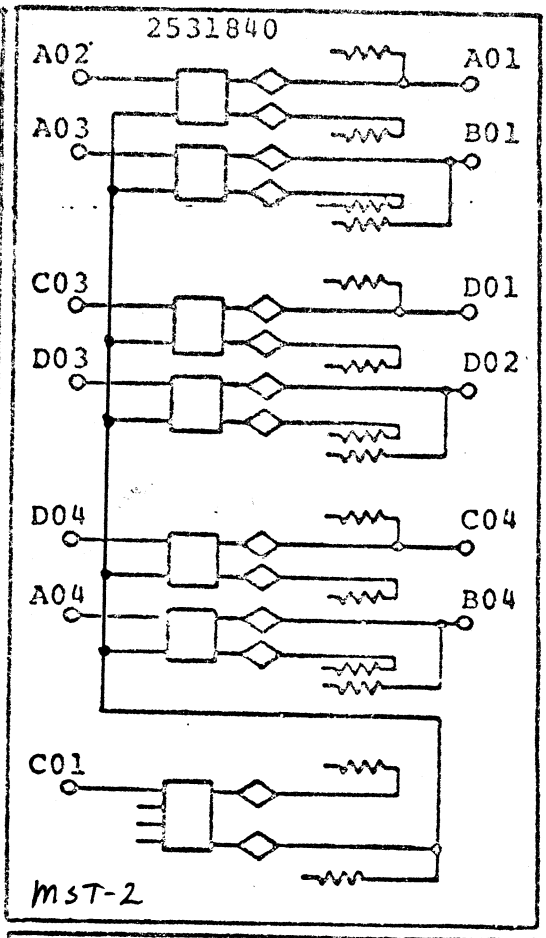


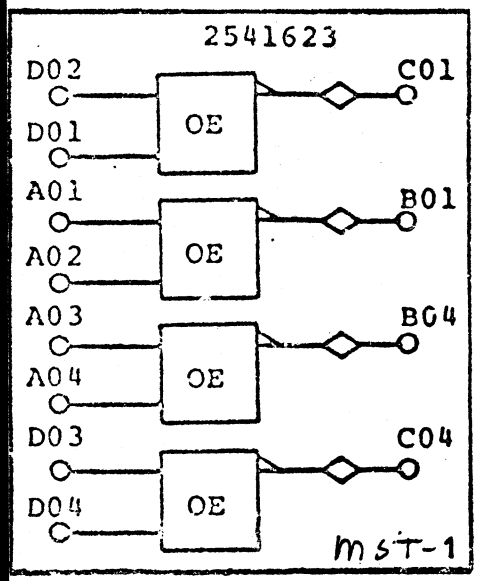


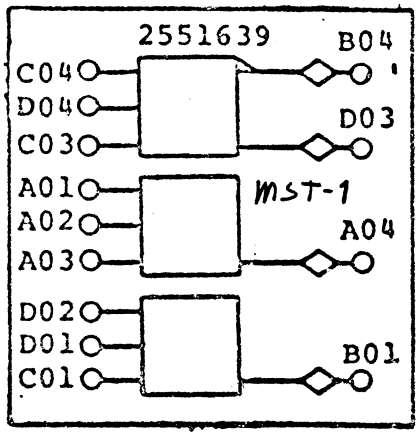


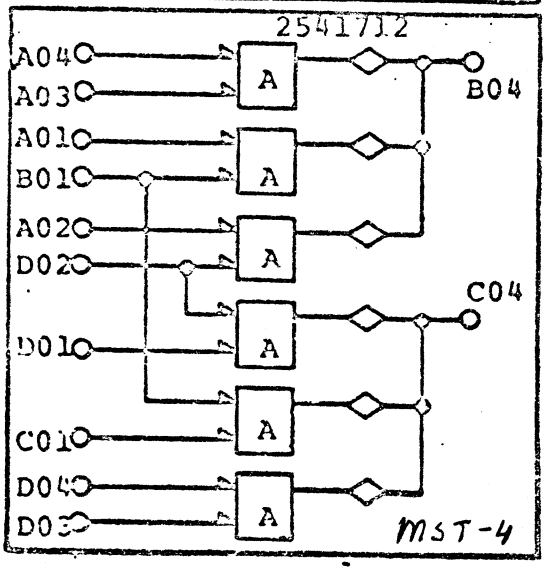
MST 1, 2 & 4 MODULE SCHEMATICS



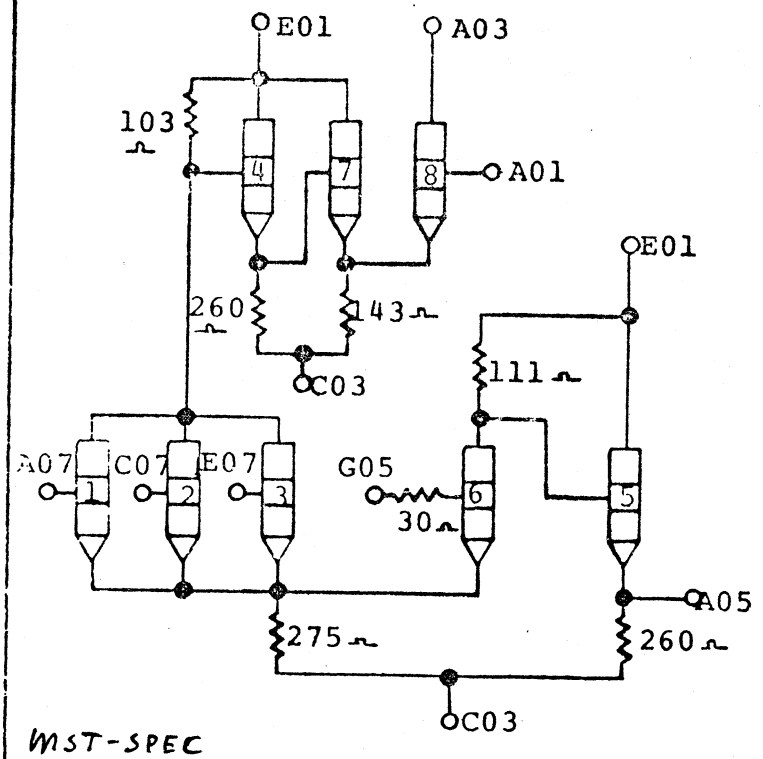






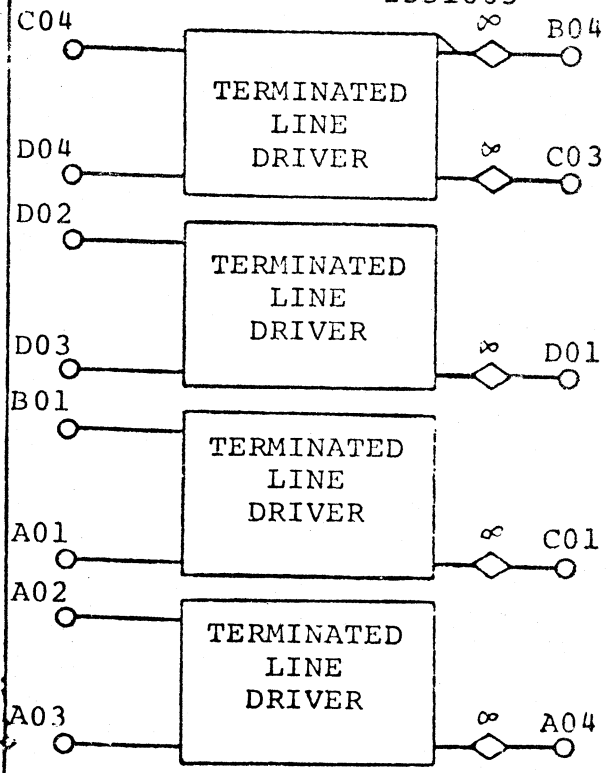


MST COUPLER DRIVER 2531699



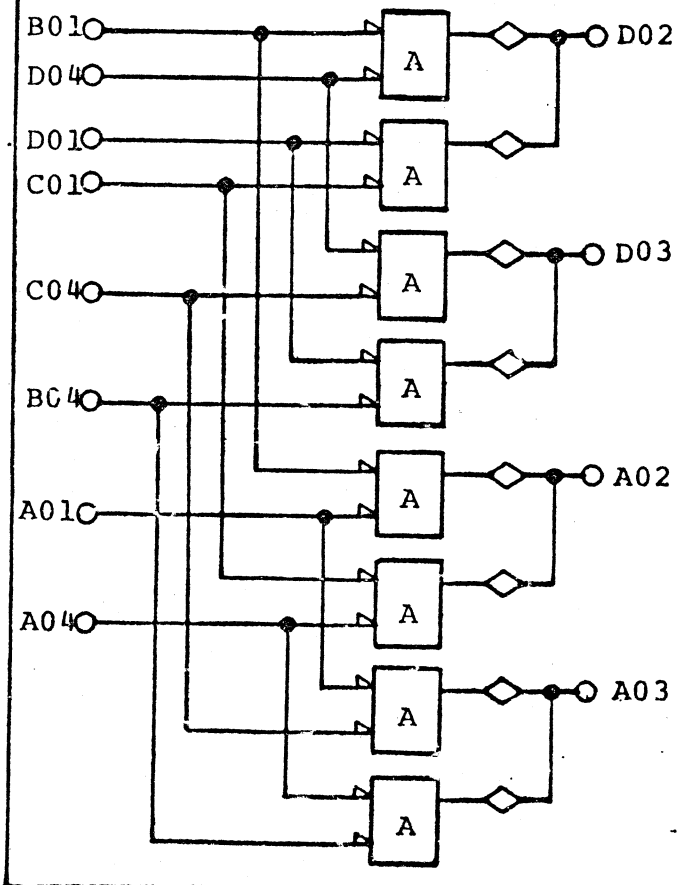
MST-SPEC

2551665

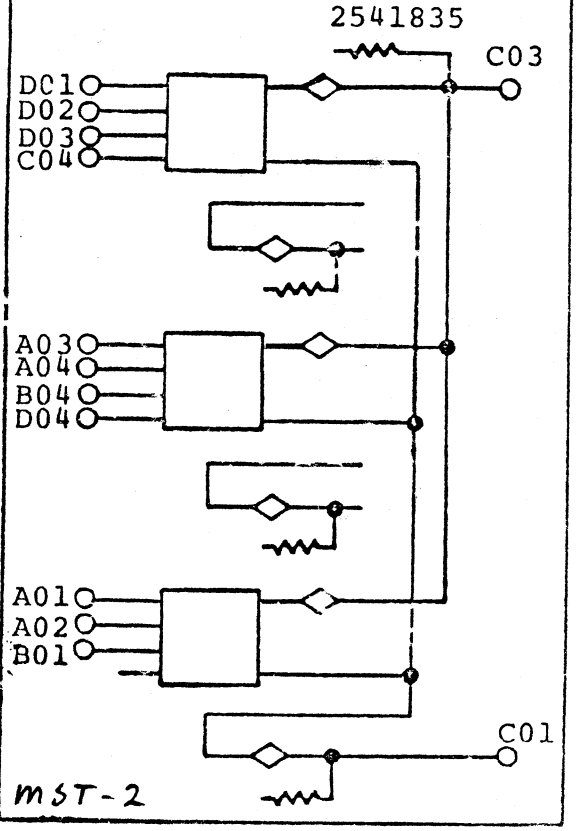


MST-1

MST-4 MODULE 23 2541723

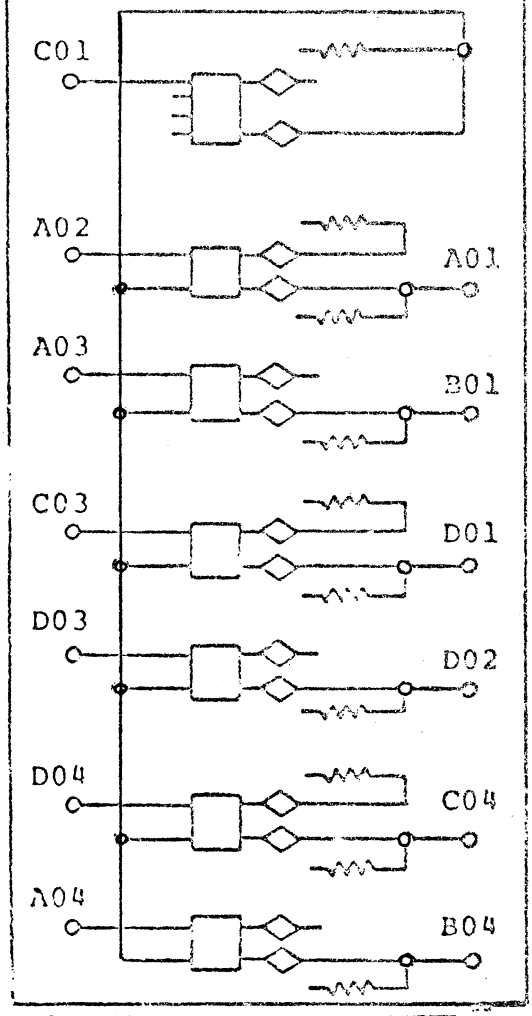


2541835

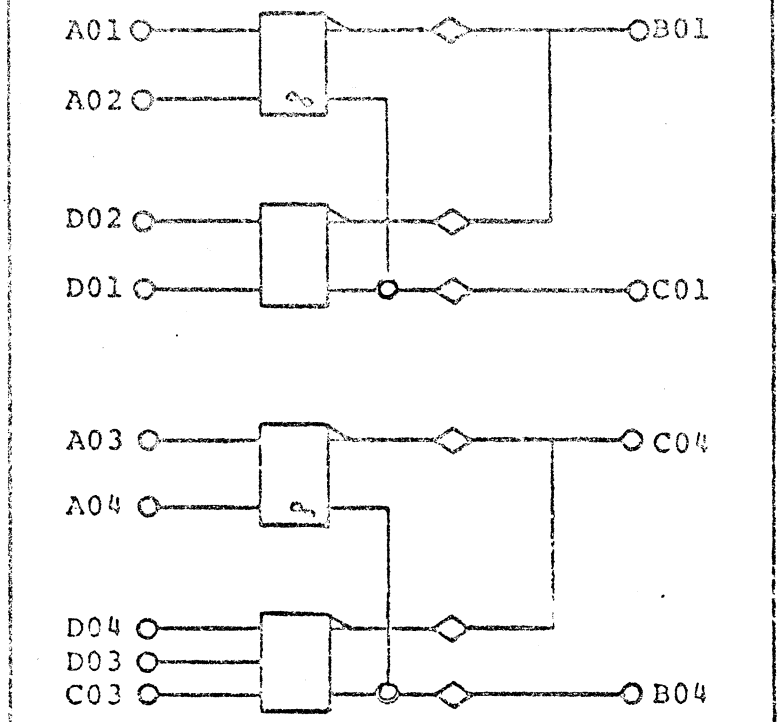


MST-2

MST-2 MODULE 2541648



2-2WAO, 1-2W, 1-3WAO 2531620



MST-1

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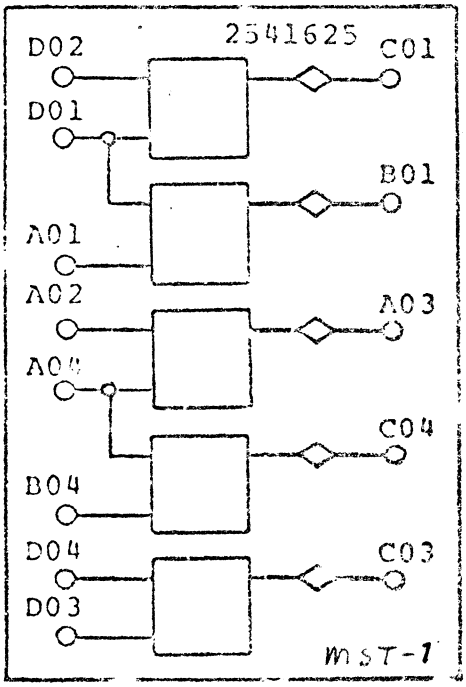
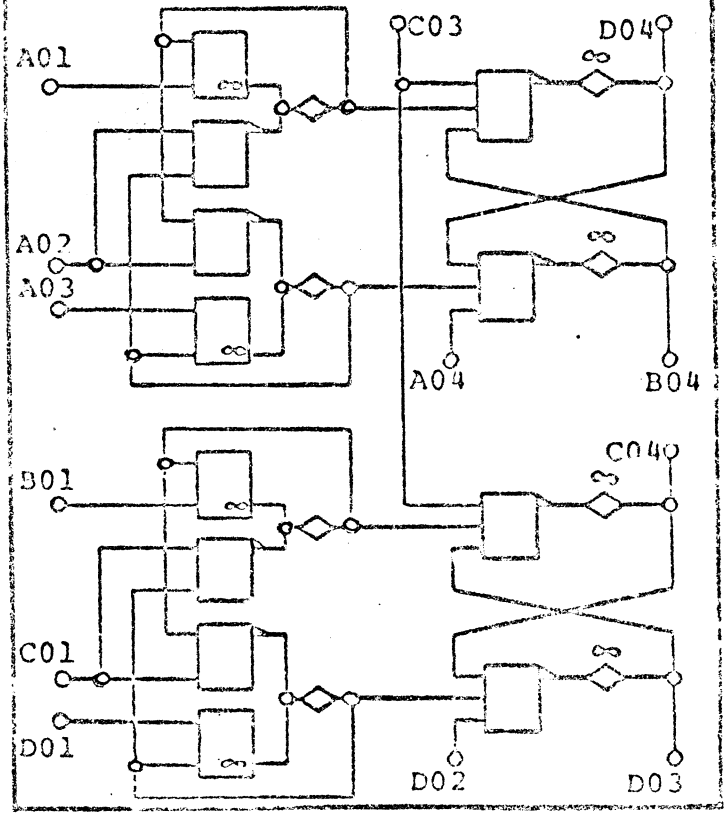
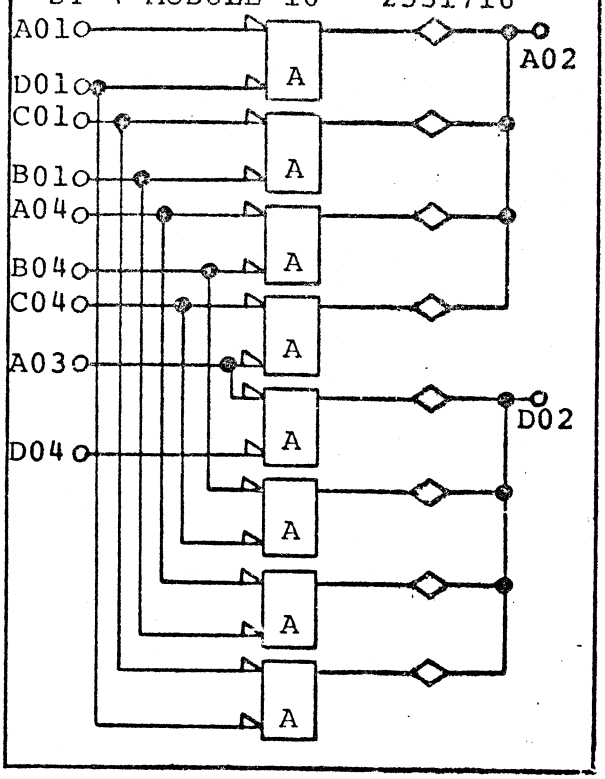


MST-1

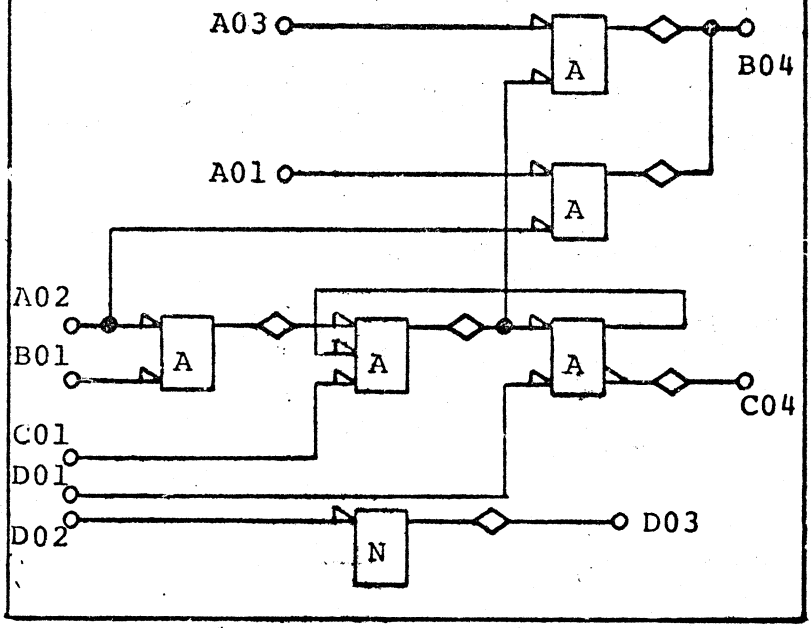
DC TRIGGER MST-1 2551624



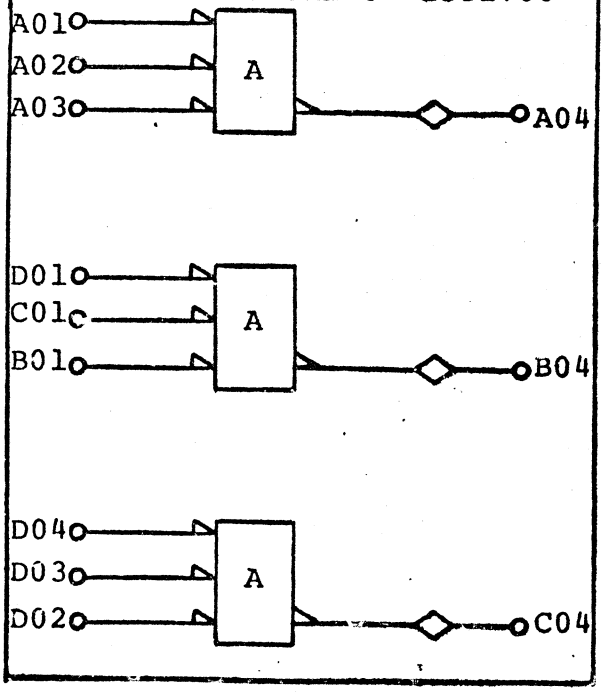
MST-4 MODULE 16 2531716



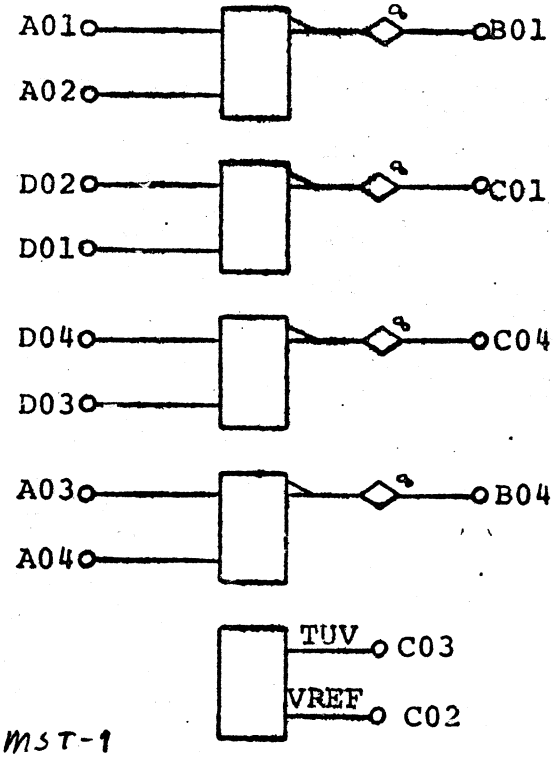
MST-4 MODULE 26 2531726



MST-4 MODULE 8 2531708

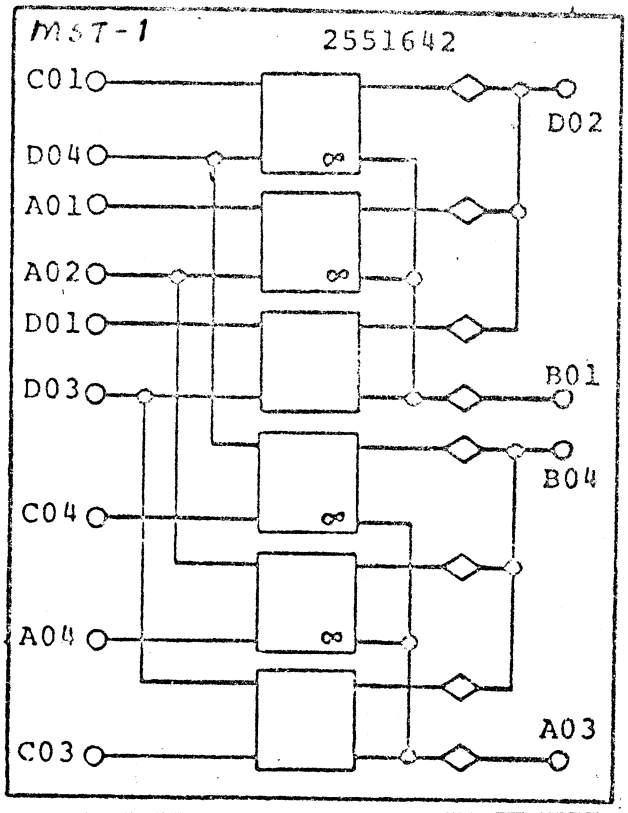


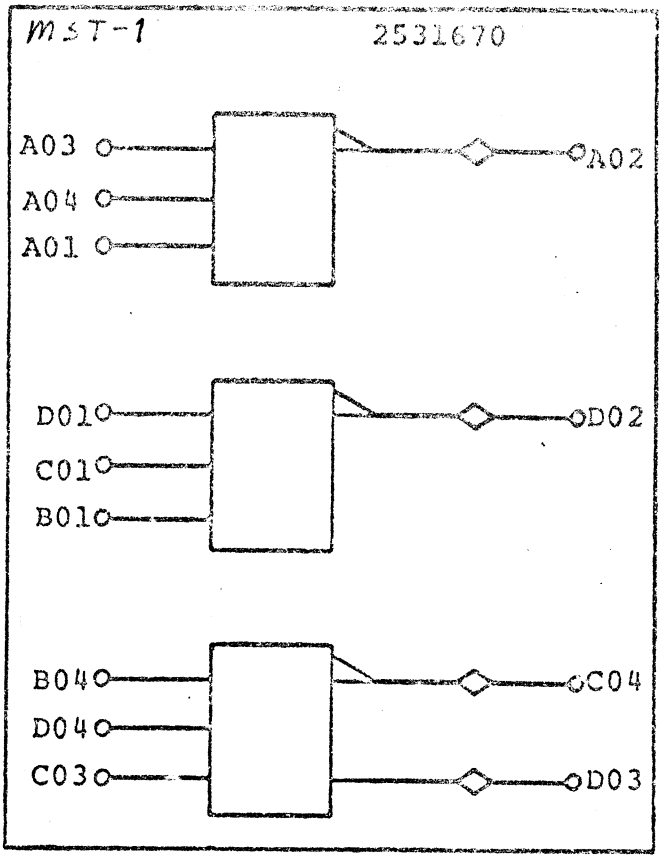
BIAS NETWORK 2531634

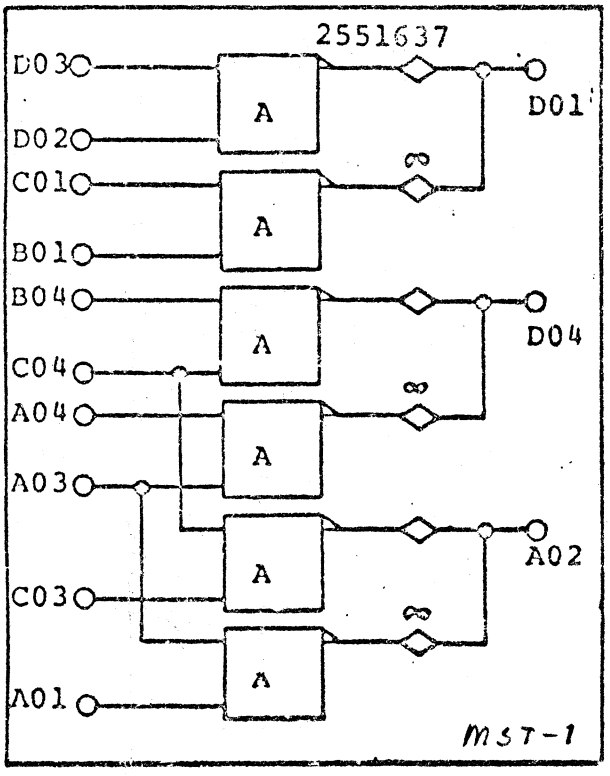


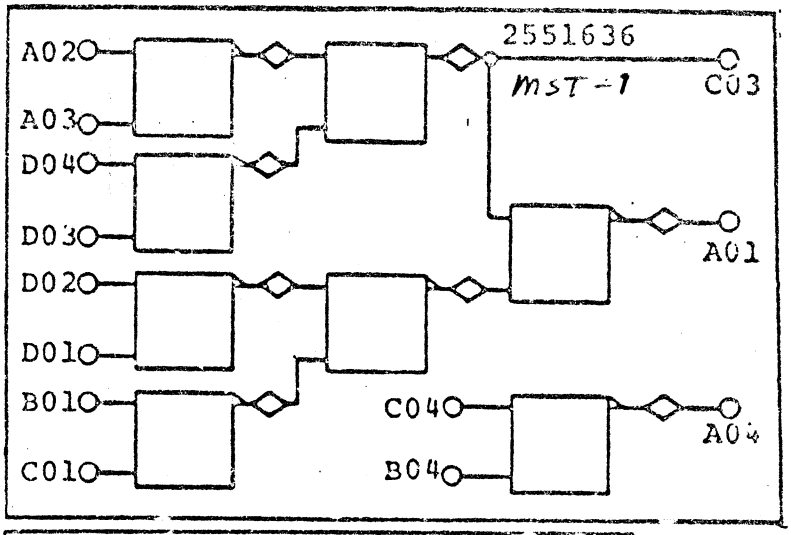
MST-1

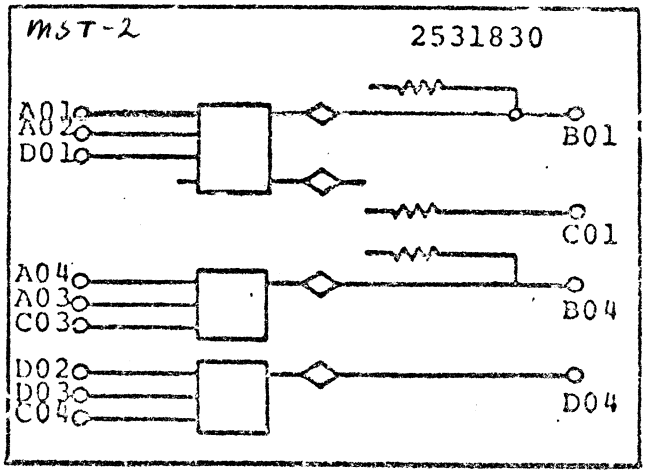
MST 1, 2 & 4 MODULE SCHEMATICS



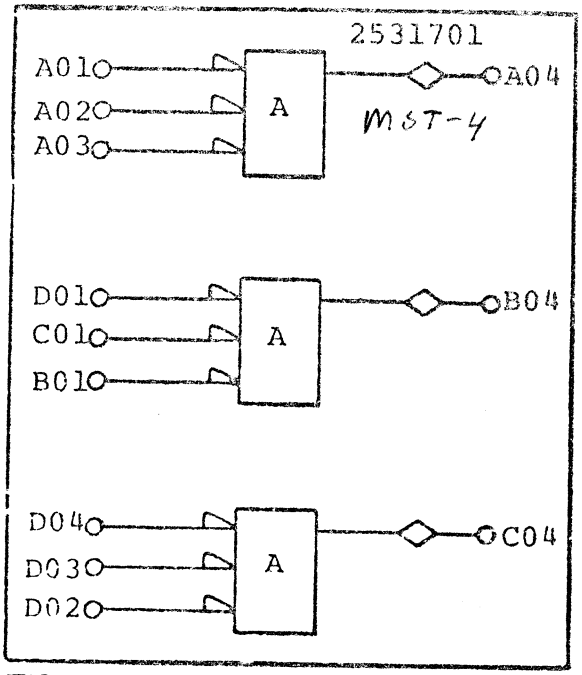


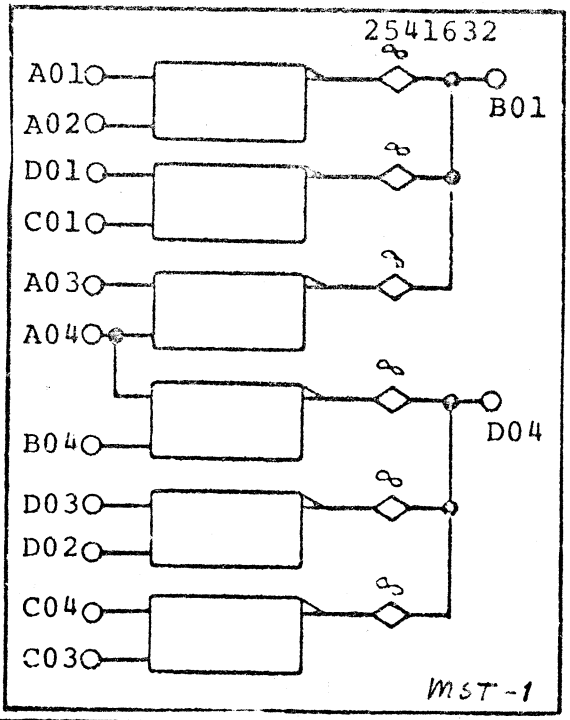


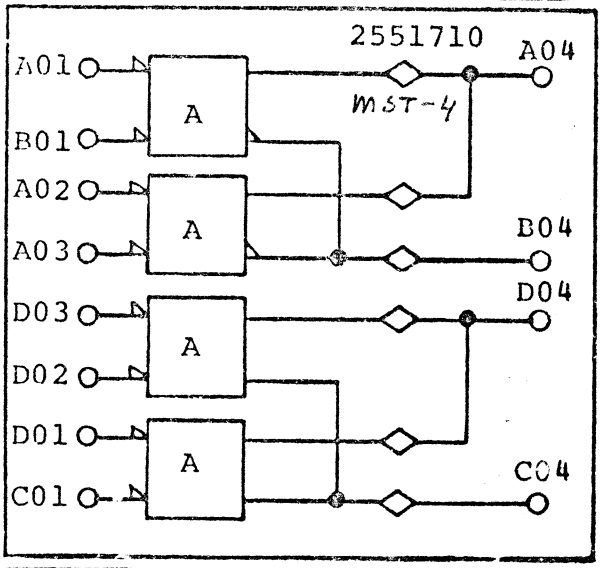


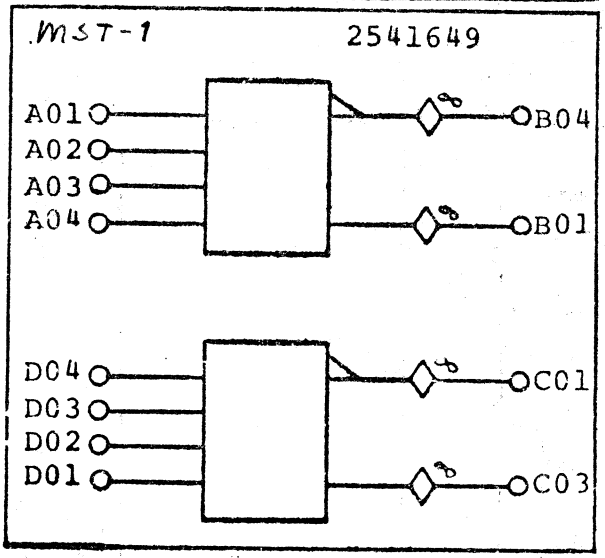


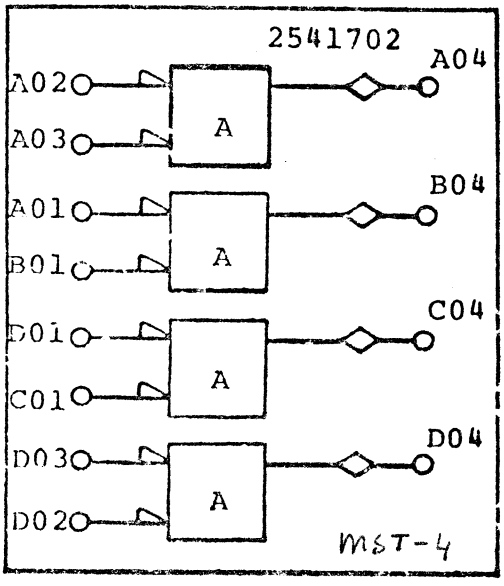
MST 1, 2 & 4 MODULE SCHEMATICS

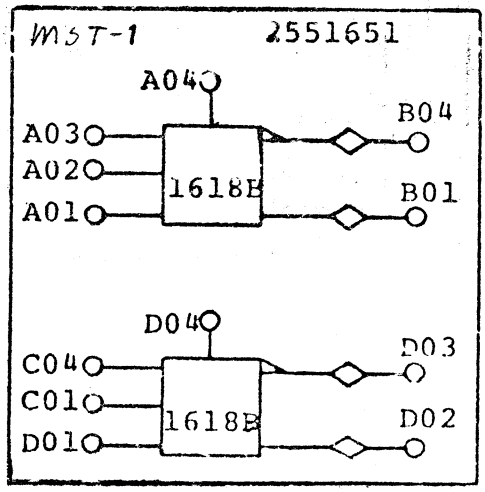




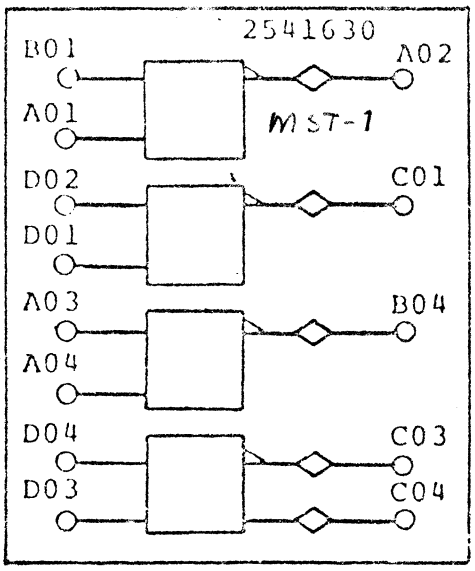


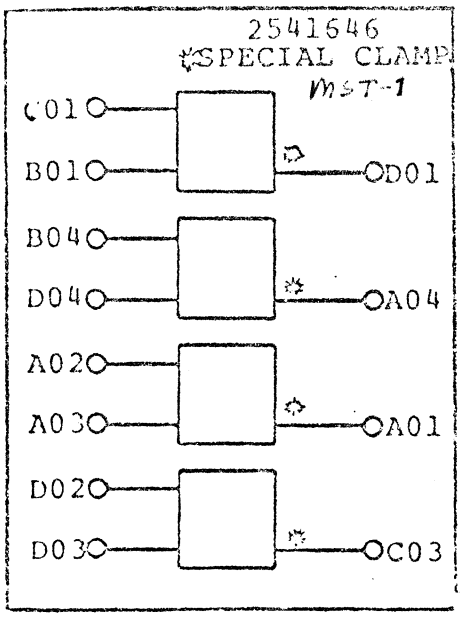


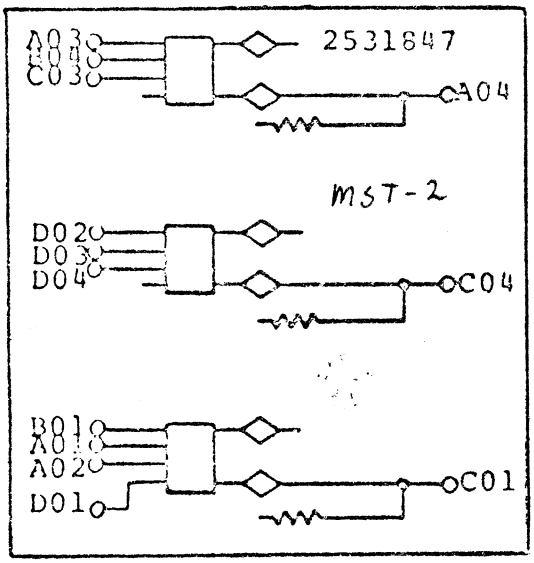


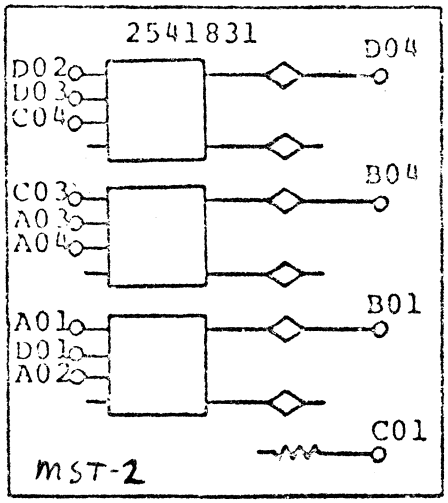


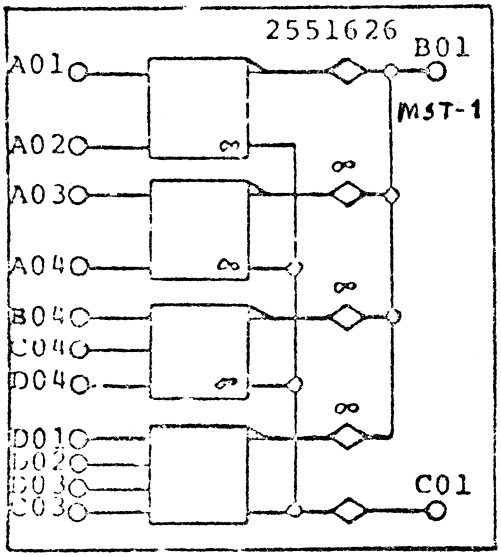
MST 1, 2 & 4 MODULE SCHEMATICS

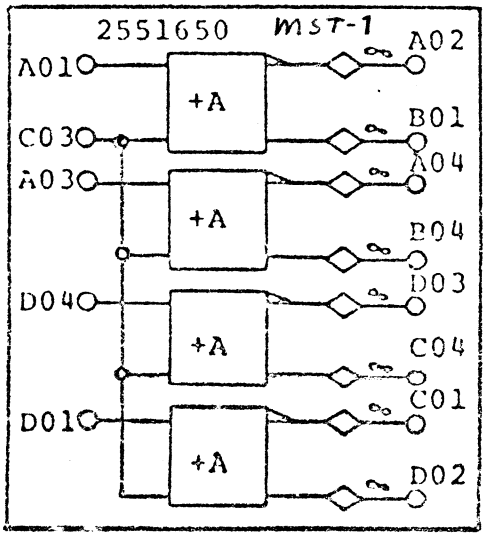












EFFECTIVE DATE: May 1, 1968

Subject: Card layout ground rule status Suffix 3 Section 11
R/C Modules

This section has been updated to include the R/C module layout requirements for SLD and MST.

PACKAGE

This section is updated to include the Circuit Master Tape (CMT) size codes for the four (4) R/C module packages. The four (4) new R/C module physical outline specifications have been added.

REQUIREMENTS

The CMT orientation and lead codes have been added. Hole size requirement for MST is defined.

LIMITS

Expanded to include the five (5) MST card sizes.

RELATIONSHIPS

R/C module placement on MST cards is defined. Placement of R/C modules under brick walled conditions is defined.

SEQUENCE EFFECT

Word "Automated" removed from spacing table because table shows body diameters which are both for hand assembled and machine inserted components.

HAND ASSEMBLY

Due to the MST hole size, R/C modules are hand assembled using double-sided tape.

PLANNING

Hand assembly of R/C modules for MST 1 and 2 will be eliminated if the planned hole size change is approved.

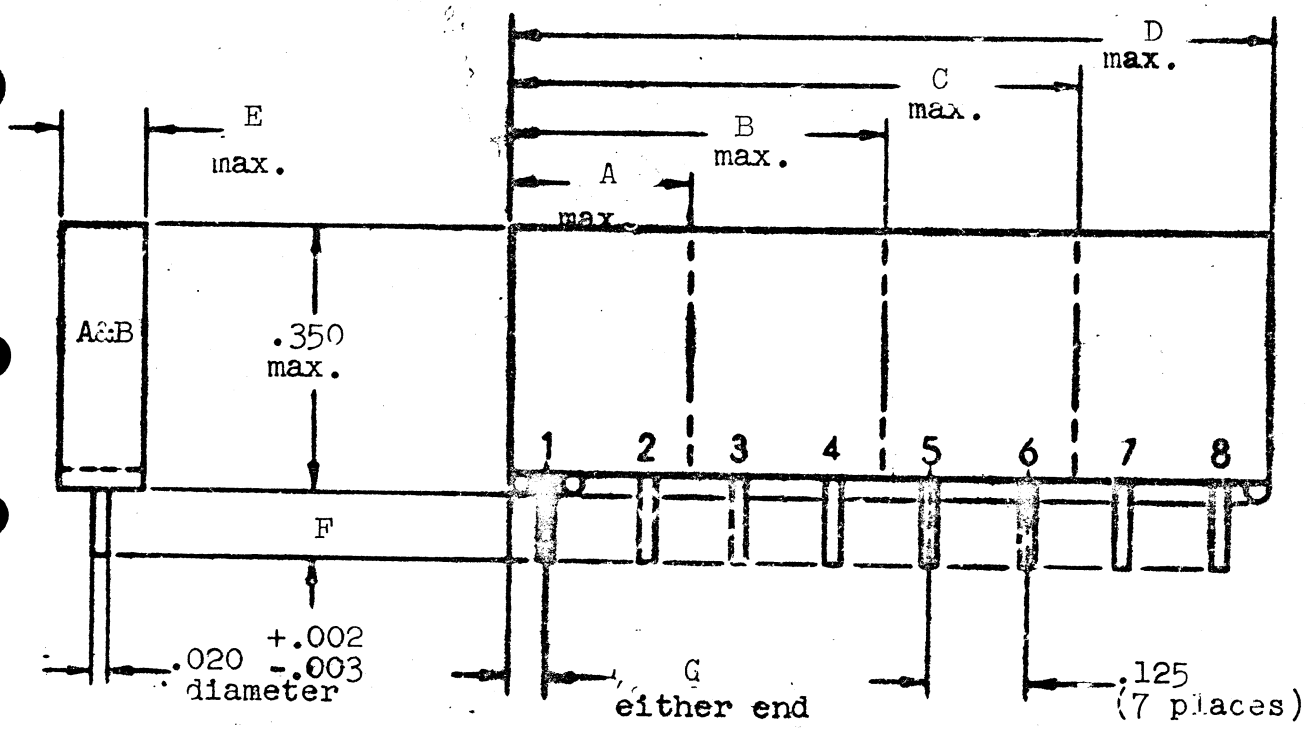
DESCRIPTION

R/C modules have 2, 4, 6 or 8 leads. They are insulated and any new designs must also be insulated. They may contain resistors and/or capacitors as well as a variety of other electrical components. Three basic packages are used:

a. Molded or painted substrate.
b. Shell molded(which is potted or cast).
c. Plastic dipped.

Assembly drawing code is "A" for R/C modules containing resistors and/or capacitors. All other components packaged in R/C modules will have their appropropriate code designated. Ex. inductors "L", diodes "CR", etc.

PACKAGE



Package Style

D-Dipped
M-Molded

PACKAGE (CONTINUED)

PHYSICAL OUTLINE	PACK. STYLE	No. of LEADS	A	B	C	D	E	F	G	CMT SIZE
865726	D	2	.240				.120	.090	.060	2 x 1
865727	D	4		.490			.120	.090	.060	4 x 1
865728	D	6			.740		.120	.090	.060	6 x 1
865729	D	8				.990	.120	.090	.060	8 x 1
873595	M	2	.234				.110	.090	.059	2 x 1
873596	M	4		.484			.110	.090	.059	4 x 1
873597	M	6			.734		.110	.090	.059	6 x 1
873600	M	8				.984	.110	.090	.059	8 x 1
2A801A4	M	4		.483			.110	.090	.059	4 x 1
2A801C4	M	6			.733		.110	.090	.059	6 x 1
2A801E4	M	8				.983	.110	.090	.059	8 x 1
2A801G4	M	2	.233				.110	.090	.059	2 x 1
4A803A	D	4		.500			.125	.095	.060	4 x 1
4A803B	D	6			.750		.125	.095	.060	6 x 1
4A803C	D	8				1.000	.125	.095	.060	8 x 1
4A803D	D	2	.250				.125	.095	.060	2 x 1

All lead numbers appear on the R/C module. Views shown are for layout purposes only and the part drawing has precedence.

Polarity will be indicated on the component where applicable by a "+" symbol for capacitors and an "X" symbol for diodes and will be reflected on the part drawing. "X" is the cathode end of a diode.

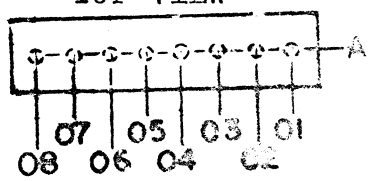
REQUIREMENTS

R/C module leads must always be mounted in:

1. "J" holes for SLT, SLD
2. .031 plated holes for MST

There are no note codes associated with this part. For CMT coding, the leads will be coded for "A" orientation as shown below. "A" and "C" orientation with leads parallel to the "Y-Y" axis (or card housing) are the only allowable orientations.

TOP VIEW



LIMITS

All R/C modules must have their leads on or within the following X and Y grid locations:

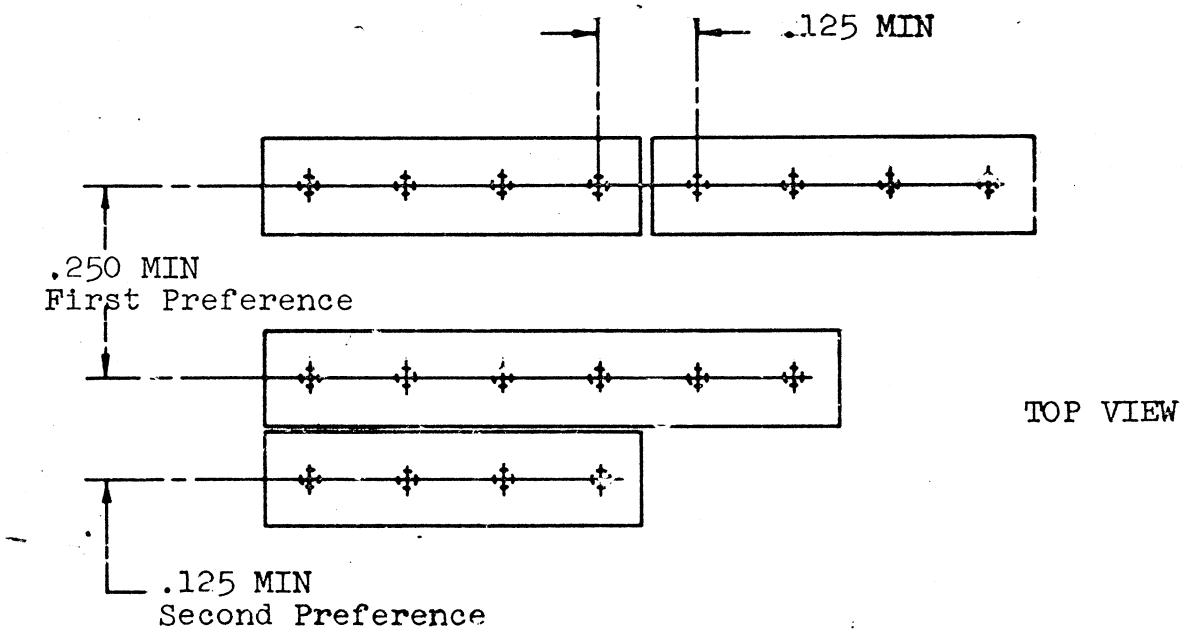
SLT/SLD	1 Hi 6 - 12	X 23 - 78 - 148	Y 23 - 63
	2 Hi 6 - 12	X 23 - 78 - 148	Y 23 - 123
	3 Hi 12	X 23 - 148	Y 23 - 183
MST	2 Hi x 1,2,&4 wide	X 01 - 12 - 26 - 54	Y C - W
	3 Hi x 2&4 wide	X 01 - 26 - 54	Y C - 9

R/C modules must be oriented in a vertical position in either of the two quadrants parallel to the YY grid coordinates (Parallel to the card housing).

RELATIONSHIPS

MST - R/C Module placement will be to the standard card description for each card size.

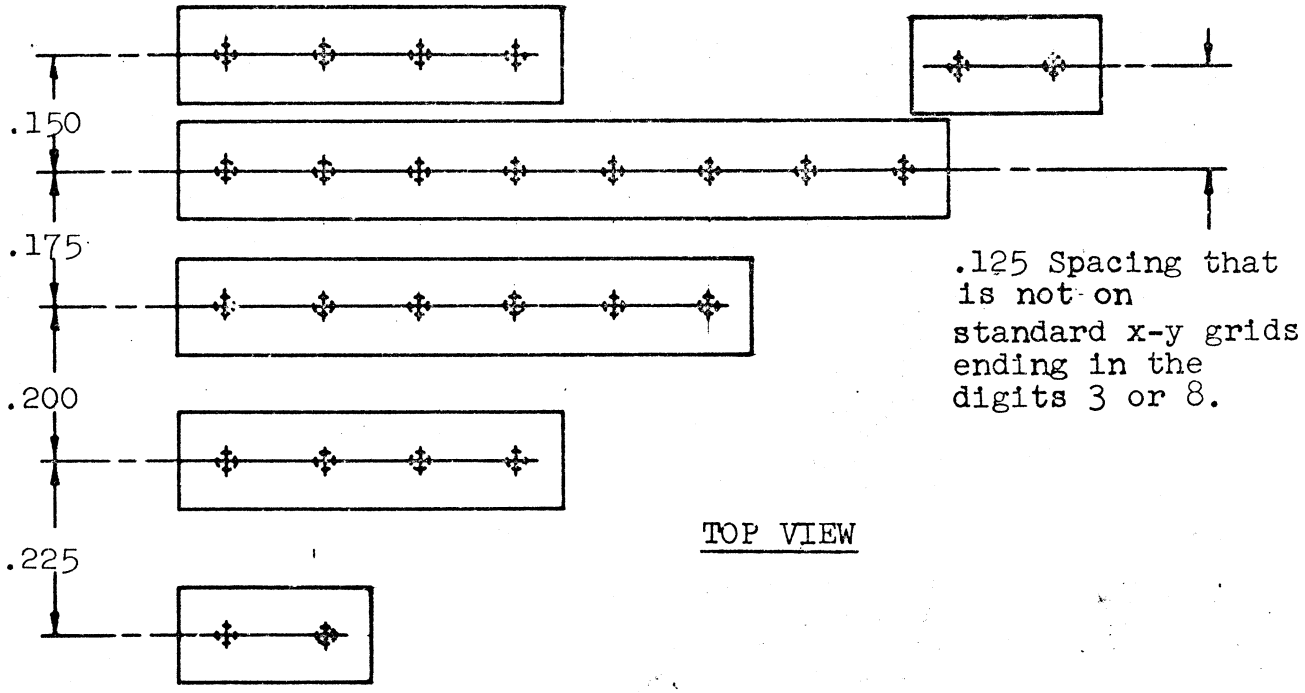
SLT/SLD The following illustration shows the physical minimum placement of R/C Modules:



NOTE: When brickwalled, the R/C Modules should be placed so that the element sides of the R/C modules (side numbered left to right starting with Lead 1) are not facing each other. This will facilitate cooling.

RELATIONSHIPS (CONT'D)

The following illustration shows the physical placement of R/C modules that are hand assembled. Placement of these modules is on random pattern and not on x-y grids ending in the digit 3 or 8.

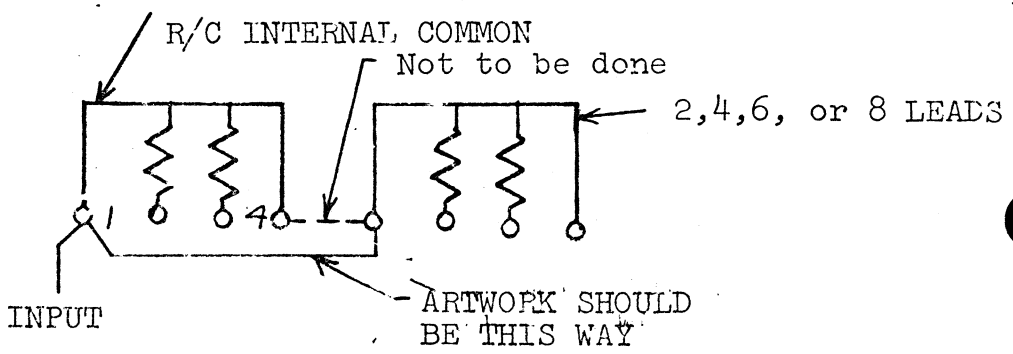


TOP VIEW

ARTWORK

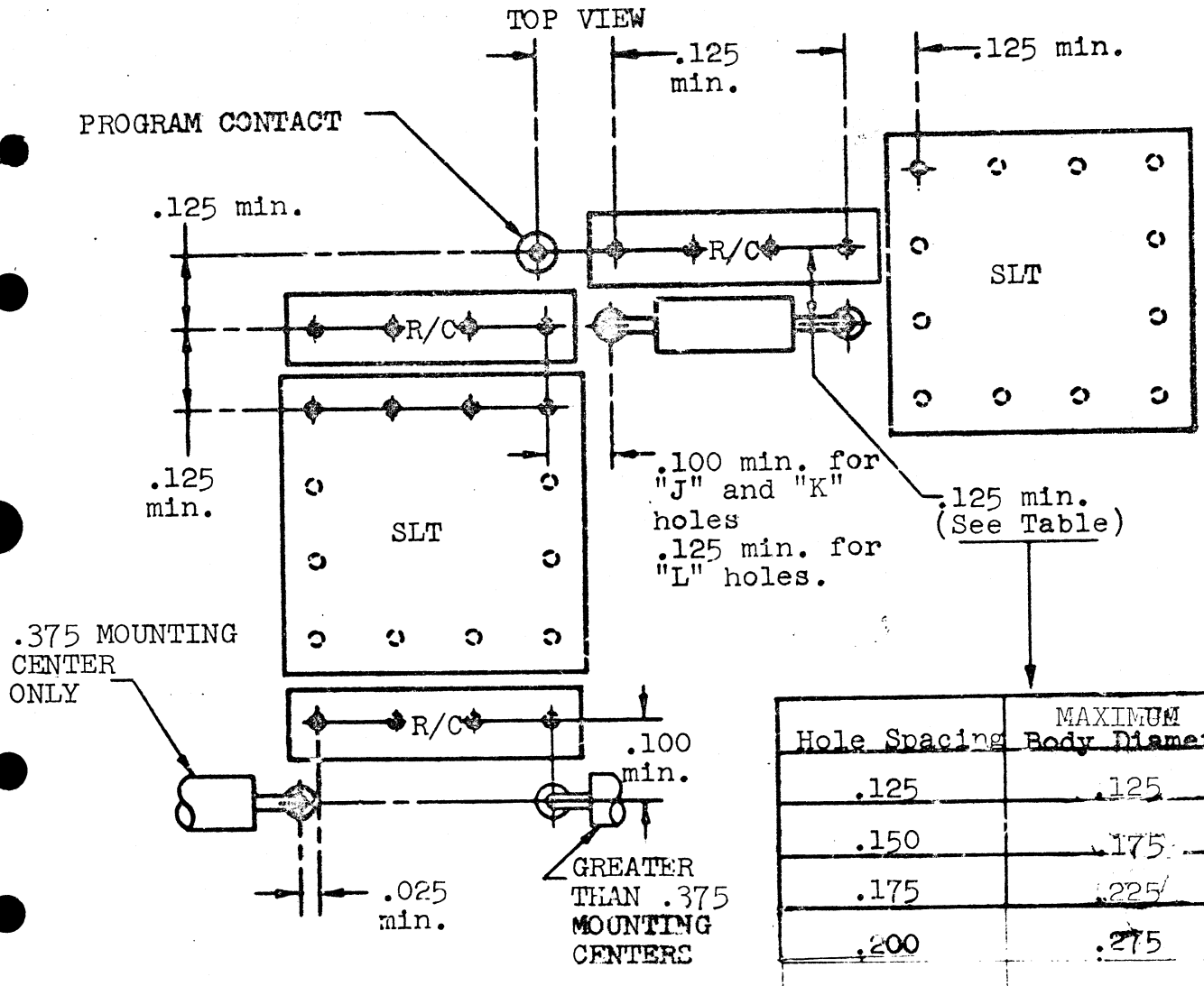
Any unused lead of an R/C module containing capacitors must not be connected to printed wiring by using its plated hole as a via or its lands as a pass through.

The following illustration shows a voltage line going to the common leads 1 to 4 through the R/C module and in series with the next R/C. This should not be done as there will be a voltage drop through the internal common in the R/C module due to its resistance.



SEQUENCE EFFECT

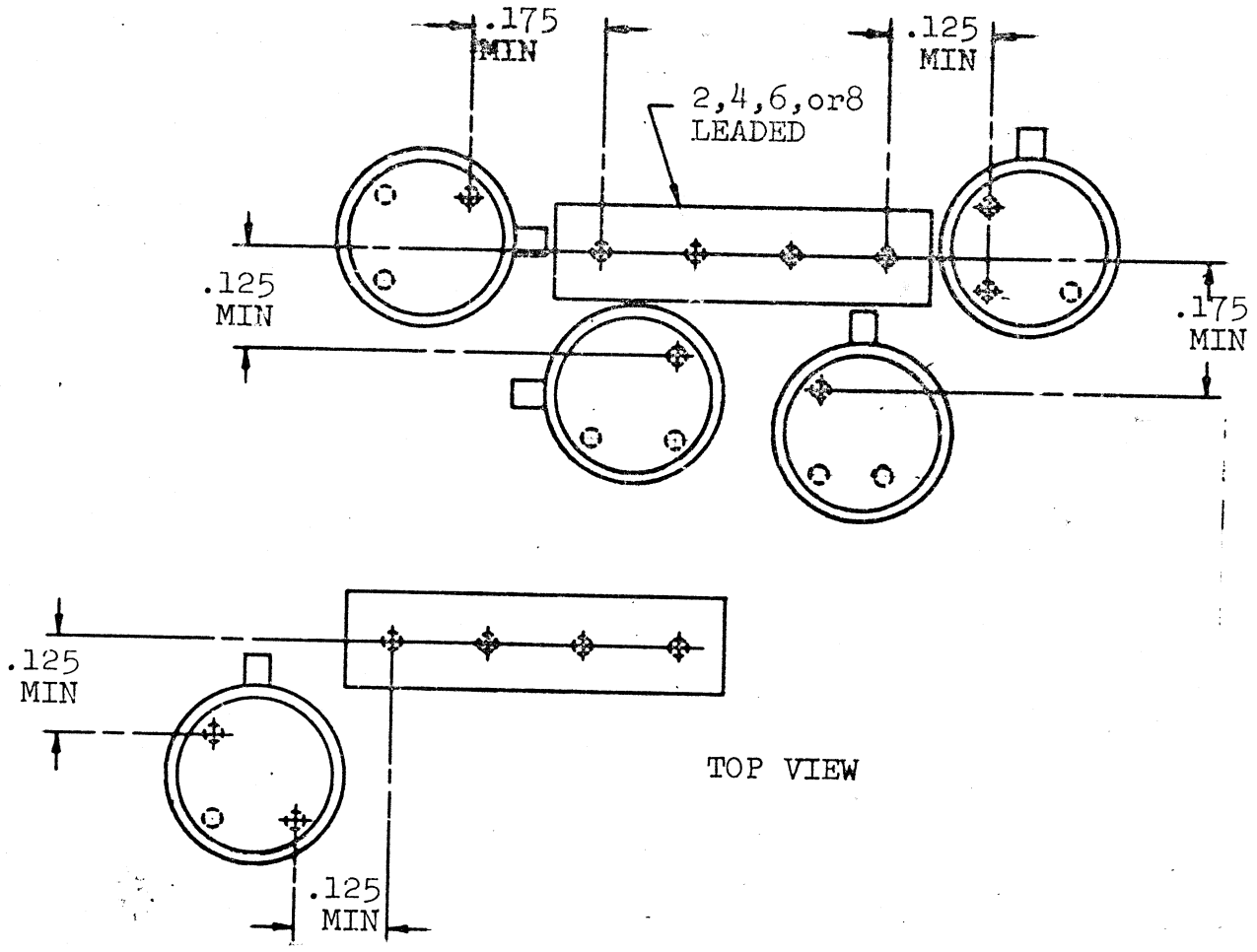
The following illustration shows the physical placement of R/C modules and those components that are assembled before R/C modules.



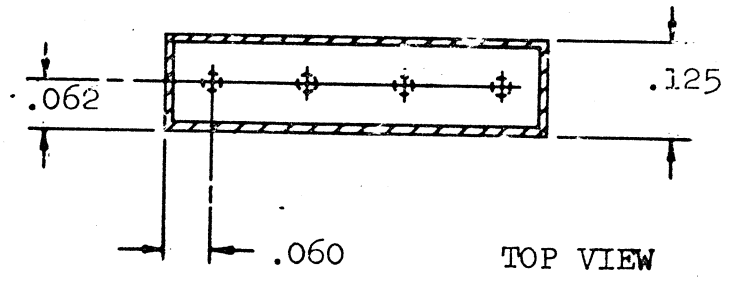
Hole Spacing	MAXIMUM Body Diameter
.125	.125
.150	.175
.175	.225
.200	.275
.225	.325
.250	.350

SEQUENCE EFFECT (continued)

The following illustration shows the minimum placement of R/C modules to TO-18 and TO-56 packages.



The following illustration shows the restricted area for insulated or uninsulated components next to R/C modules.

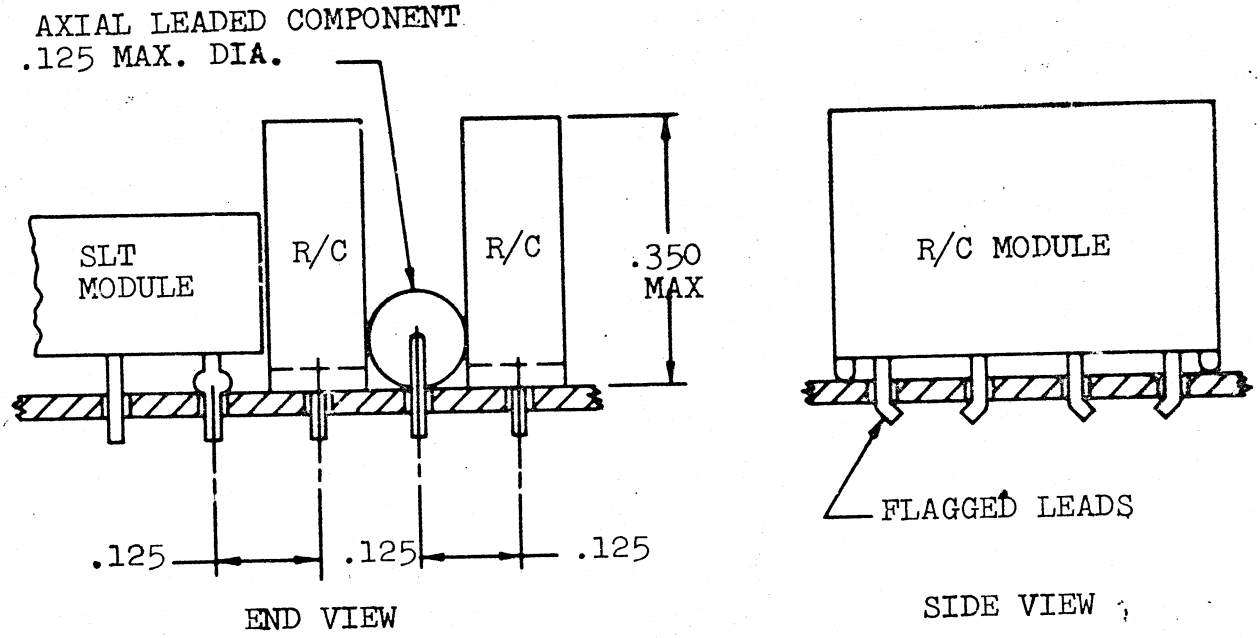


HAND ASSEMBLY

All R/C modules are hand assemblied if their leads are hand flagged and/or not on the standard x-y grid ending with digit 3 or 8.
All R/C modules are hand assembled on MST card assemblies using double sided tape and the leads are not flagged.

PROCESS INFORMATION

The Assembly Machines require the module leads to be on x-y grid locations that end with digit 3 or 8. Their leads will be gang clinched after all other components less than .350 high are assembled.



R/C Module leads will be flagged along the centerline of the module and in pairs toward each other.

PLANNING

Semi-automatic equipment for leads located off the standard grid pattern is not recommended due to high costs. Once the hole size change for MST 1 and 2 is approved R/C modules will then be semi-automatically assembled.

IBM Division Engineering Practice

CARD GROUND RULES

SUPPLEMENT OF STATUS
TRANSISTOR TO-18 AND TO-56
AND PRESS-ON HEAT SINKS

DEP Cat.	2-6230 Subject	3 Suffix
SECTION	12A	

EFFECTIVE DATE: November 28, 1968

SUBJECT: Card layout ground rules status, Suffix 3, Section 12A.

This update supersedes DEP 2-7047 Suffix 3, Section 12A dated 8-15-66 and Book 03-10, DEP 2-6420-530, Section 2, Page 5 under "Transistor in TO-18 or TO-56 Packages".

This Section has been updated to include the TO-18 and TO-56 transistor requirements for SLD and MST.

REQUIREMENTS

CMT size code defined. Plated hole size defined for MST. Heat sink 813169 has been removed. Due to the construction of this heat sink assembly, shorts were occurring between heat sinks. Heat sink 483454 has been added.

LIMITS

Updated to include the five (5) MST card sizes. Limits added for 483454.

RELATIONSHIPS

Updated to include heat sink 483454.

SEQUENCE EFFECT

Updated to include heat sink 483454.

HAND ASSEMBLY

Updated to reflect hand assembly of TO-18 and TO-56 transistors for MST-4.

PROCESS INFORMATION

Department 146 has been changed to Department 307 for release responsibility for new designs of spacers.

PLANNING

The gang-clinch machines have replaced the lead spinning machines.

DESCRIPTION

Devices in TO-18 and TO-56 packages have metal cans and headers and have 3 or 4 leads glassed in. The package is electrically hot and may contain a variety of components. Assembly drawing code is "Q" for transistors or "CR" for diodes depending on which device is in the package.

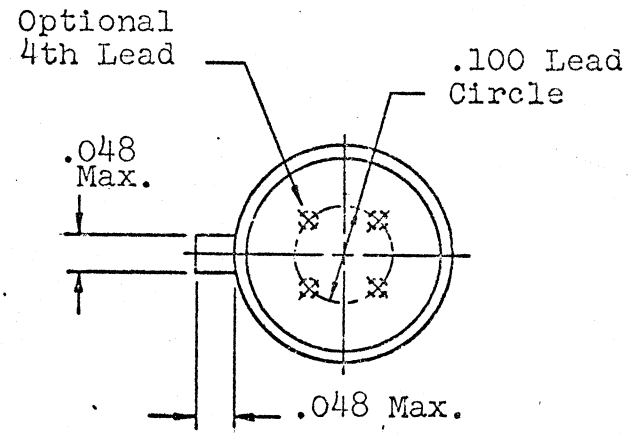
PACKAGE

All physical outlines of TO-18 and TO-56 packages are contained in the following coded list and are in the Component Library maintained by E.C. level of the component part number:

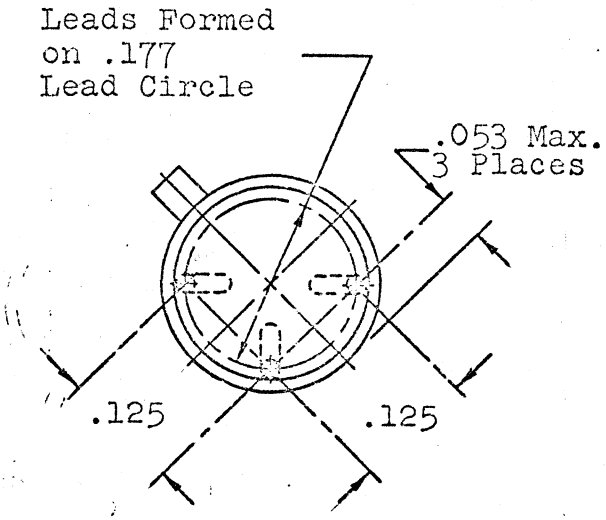
TO-56	TO-18	4 Leaded
16-T56A	1T-18A	1T-18D
16-T56B	1T-18B	20T-72B

The components are purchased with leads on a .100 diameter lead circle but prior to insertion, are formed and skewed to a .177 diameter lead circle to fit the .125 hole pattern.

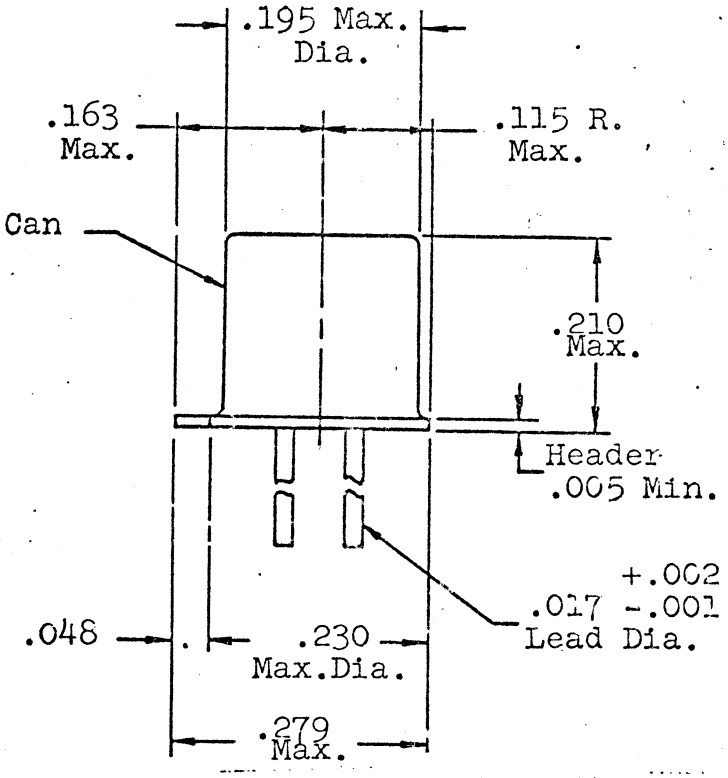
PACKAGE (CONTINUED)



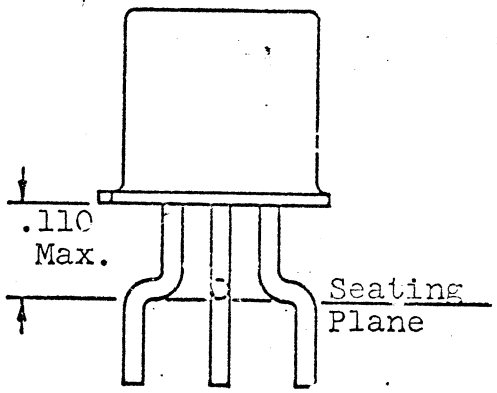
TOP VIEW



TOP VIEW



SIDE VIEW
Leads unformed on
.100 lead circle



SIDE VIEW
Leads formed on
.177 lead circle

Views shown are for packaging purposes only and part drawings have precedence.

TRANSISTORS TO-18 and TO-56

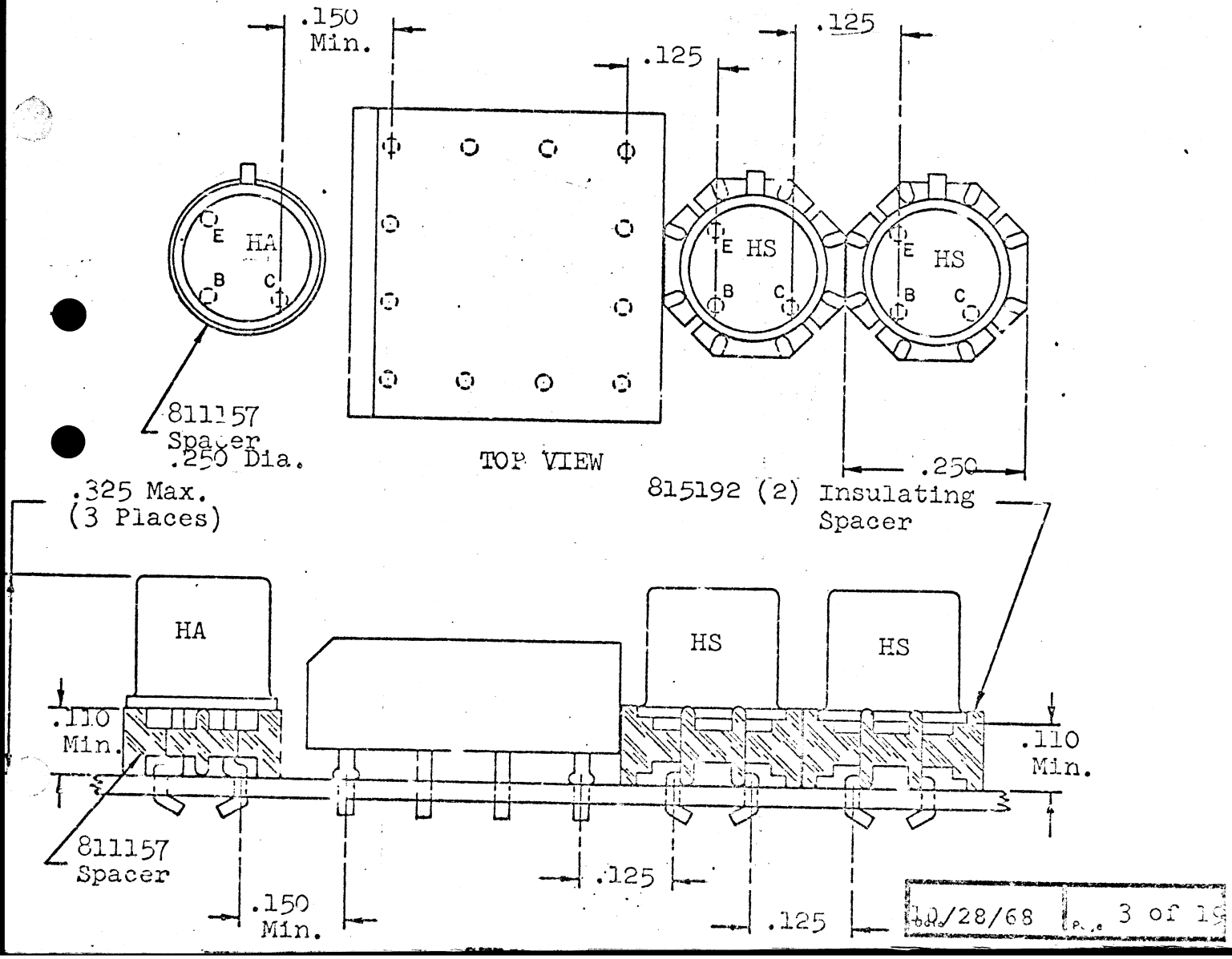
REQUIREMENTS

Leads of these components must be mounted in:
"J" .040 holes for SLT & SLD
.040 holes for MST 1 & 2
.031 holes for MST 4
Note codes must be used as follows:

HA - Note HA calling for the use of spacer part number 811157 normally must be used for all packages. The note code will appear on the package and in the note code field on the assembly drawing.

HS - This note code calls for the use of insulating spacer P/N 815192. Note HS must be used when the package lead is .125 from the lead of an SLT Module or another TO-18 or TO-56, as shown in the following illustration.

(When the AZ note code was used to describe the shorting condition between TO-56 and/or TO-18's and SLT Modules, then it must be replaced by note code "HS" when E.C. changes are made to the card assemblies.)



REQUIREMENTS (CONTINUED)

CMT CODING

TO-18 and TO-56 packages must be coded in the "A" direction with the emitter and base leads parallel to the "Y-Y" axis and the card housing. This orientation also places the tab parallel to the "Y-Y" axis.

811157 Spacer.
TO-18 and TO-56 transistors using this spacer must be coded as a 4 x 4 component with lead codes as follows:

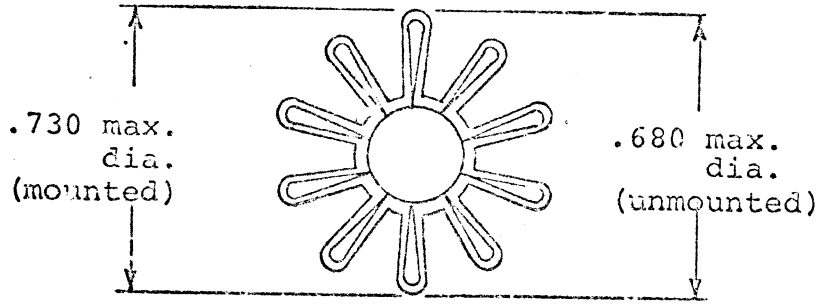
Emitter - BO3
Base - BO2
Collector - CO2

815192 Spacer.
TO-18 and TO-56 transistors using this spacer must be coded as a 2 x 2 component with lead codes as follows:

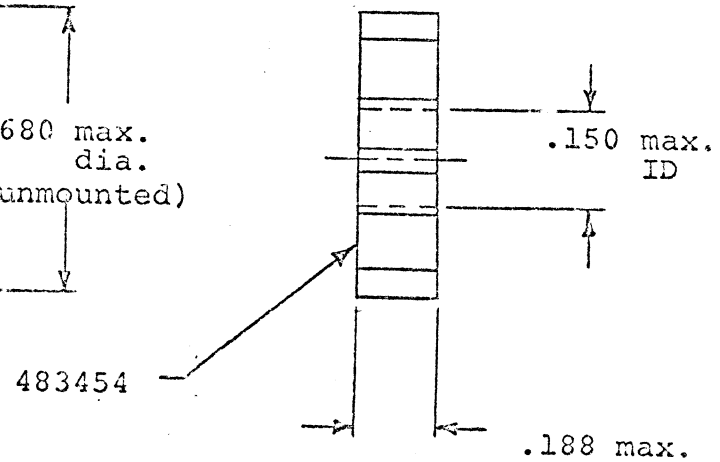
Emitter - AO2
Base - AO1
Collector - BO1

HEAT SINKS

483454 Heat Sink.
Heat Sink 483454 non-insulated can be used on all physical outlines. Si grease must not be used with this Heat Sink. CMT size code 6 x 6.



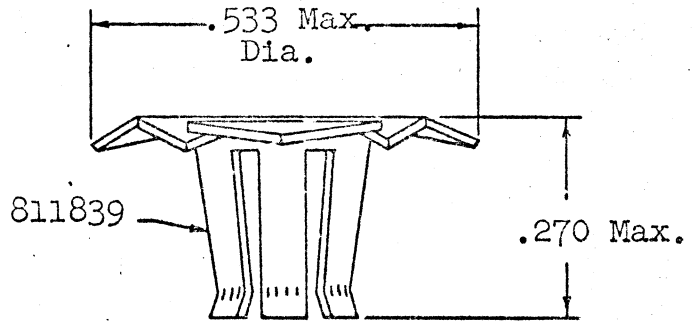
TOP VIEW



SIDE VIEW

811839 Heat Sink.

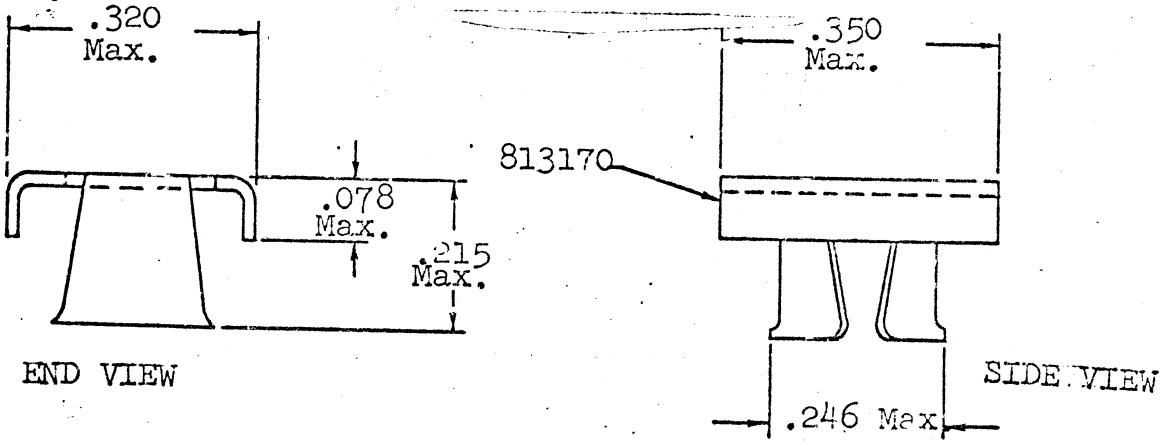
Heat Sink 811839 non-insulated can be used on 1T-18B, 16-T56A and 16-T56B physical outlines only. Si grease must not be used with this heat sink. CMT size code 6 x 6.



SIDE VIEW

813170 Heat Sink.

Heat Sink 813170, non-insulated, can be used on 1T-18B, 16-T56A and 16-T56B physical outlines only. CMT size code 4 x 4.



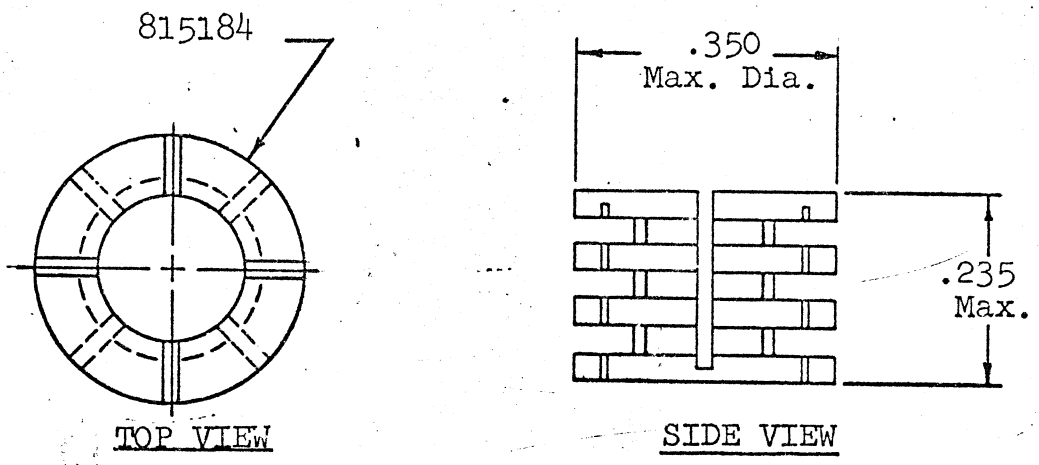
END VIEW

SIDE VIEW

REQUIREMENTS (CONTINUED)

HEAT SINKS

815184 Heat Sink.
Heat Sink 815184 non-insulated can be used on 16-T56A and 16-T56B physical outlines only. Si grease must not be used with this heat sink. Four slots staggered on each end of this heat sink create 8 spring surfaces over its entire height. CMT size code 4 x 4.



TOP VIEW SIDE VIEW

HEAT SINK NOTE CODES

Si grease cannot be used on Heat Sink 811839 and 815184. It is not recommended on 483454 and 813170 but when it is used note code FK must be on the heat sink and HA on the package. When Si grease is not used, the heat sinks are classified as wettable and no note code is required on the heat sink, but HA is required on the package.

LIMITS (PACKAGE ONLY)

To meet assembly requirements, leads must be on a .125 pattern within the following limits:

On a standard .125 pattern, TO-18 or TO-56 package leads will be placed on or within the following X and Y grids. Orientation tabs may be in any of the four quadrants.

SLT/SLD	1	Hi 6 and 12 X 28 - 73 - 143	Y 28 - 58
	2	Hi 6 and 12 X 28 - 73 - 143	Y 28 - 118
	3	Hi 12 X 28 - 143	Y 28 - 178

LIMITS (PACKAGE ONLY) (CONTINUED)

MST	2 Hi x 1,2 & 4 wide	X 02 - 11 - 25 - 53	Y C - V
	3 Hi x 2 & 4 wide	X 02 - 25 - 53	Y C - 8

Orientation tabs which do not project toward the card edge.

SLT/SLD	1 Hi 6 and 12	X 23 - 78 - 148	Y 23 - 58
	2 Hi 6 and 12	X 23 - 78 - 148	Y 23 - 118
	3 Hi 12	X 23 - 148	Y 23 - 178
MST	2 Hi x 1,2 & 4 wide	X 01 - 12 - 26 - 54	Y C - W
	3 Hi x 2 & 4 wide	X 01 - 26 - 54	Y C - 9

On a random pattern, TO-18 or TO-56 package leads will be placed on or within the following X and Y grids. Orientation tabs may be in any of the four quadrants.

SLT/SLD	1 Hi 6 and 12	X 25 - 76 - 146	Y 25 - 60
	2 Hi 6 and 12	X 25 - 76 - 146	Y 25 - 120
	3 Hi 12	X 25 - 146	Y 25 - 180

Orientation tabs which do not project toward the card edges.

SLT/SLD	1 Hi 6 and 12	X 23 - 78 - 148	Y 23 - 62
	2 Hi 6 and 12	X 23 - 78 - 148	Y 23 - 122
	3 Hi 12	X 23 - 148	Y 23 - 182

LIMITS (CONTINUED) HEAT SINKS

483454

Packages using Heat Sink 483454 must have their leads on or within the following X and Y grids. The heat sink may be parallel with X or Y axis.

SLT/SLD	1 Hi 6 and 12	X 32 - 54 - 113	Y 32 - 70
	2 Hi 6 and 12	X 32 - 54 - 113	Y 32 - 140
	3 Hi 12	X 32 - 113	Y 32 - 164
MST	2 Hi x 1,2 & 4 wide	X 03 - 10 - 24 - 52	Y E - U
	3 Hi x 2 & 4 wide	X 03 - 24 - 52	Y E - 7

LIMITS (CONTINUED) HEAT SINKS

811839

Packages using Heat Sink 811839 must have their leads on or within the following X and Y grids.

SLT/SLD	1 Hi 6 and 12	X 29 - 72 - 142	Y 29 - 56
	2 Hi 6 and 12	X 29 - 72 - 142	Y 29 - 116
	3 Hi 12	X 29 - 142	Y 29 - 176
MST	2 Hi x 1,2 & 4 wide	X 03 - 10 - 24 - 52	Y E - U
	3 Hi x 2 & 4 wide	X 03 - 24 - 52	Y E - 7

813170

Packages using Heat Sink 813170 must have their leads on or within the following X and Y grids. The heat sink must be parallel with X or Y axis.

SLT/SLD	1 Hi 6 and 12	X 25 - 76 - 146	Y 26 - 60
	2 Hi 6 and 12	X 25 - 76 - 146	Y 26 - 120
	3 Hi 12	X 25 - 146	Y 26 - 180
MST	2 Hi x 1,2 & 4 wide	X 02 - 11 - 25 - 53	Y D - V
	3 Hi x 2 & 4 wide	X 02 - 25 - 53	Y D - 8

815184

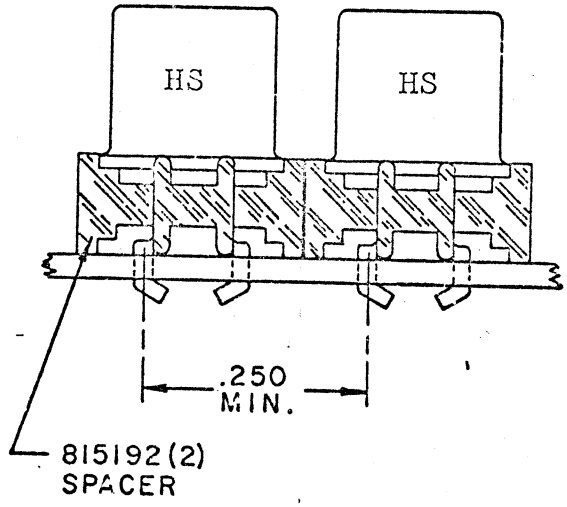
Packages using Heat Sink 815184 must have their leads on or within the following X and Y grids.

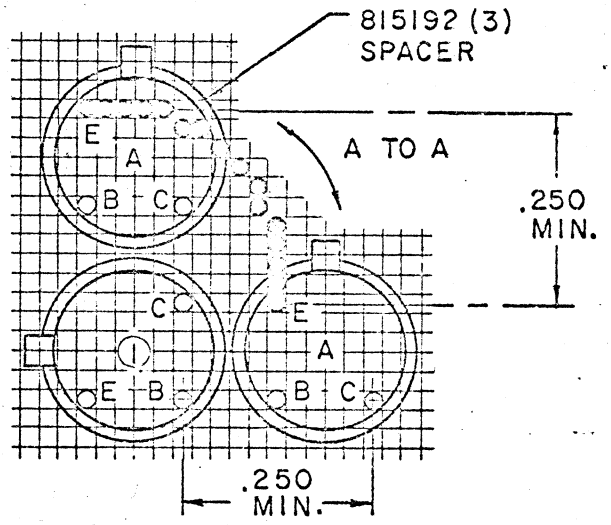
SLT/SLD	1 Hi 6 and 12	X 29 - 72 - 142	Y 29 - 56
	2 Hi 6 and 12	X 29 - 72 - 142	Y 29 - 116
	3 Hi 12	X 29 - 142	Y 29 - 176
MST	2 Hi x 1,2 & 4 wide	X 02 - 11 - 25 - 53	Y D - V
	3 Hi x 2 & 4 wide	X 02 - 25 - 53	Y D - 8

RELATIONSHIPS

The following illustration shows the physical minimum placement of TO-18 and TO-56 packages.

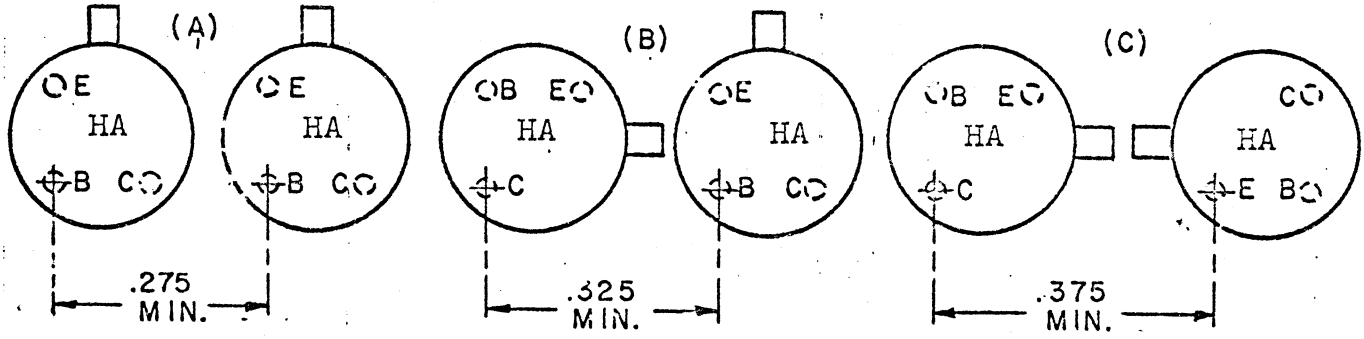
TO-18 and TO-56 packages with non-adjacent tabs may be mounted on .250" center to center distances. The insulating spacer 815192 (using Note Code HS) must be used with minimum mounting spacing as shown below.





To facilitate the use of these minimum mounting centers, A-.275, B-.325, C-.375 with TO-18 spacer (using Note Code HA).

TOP VIEWS

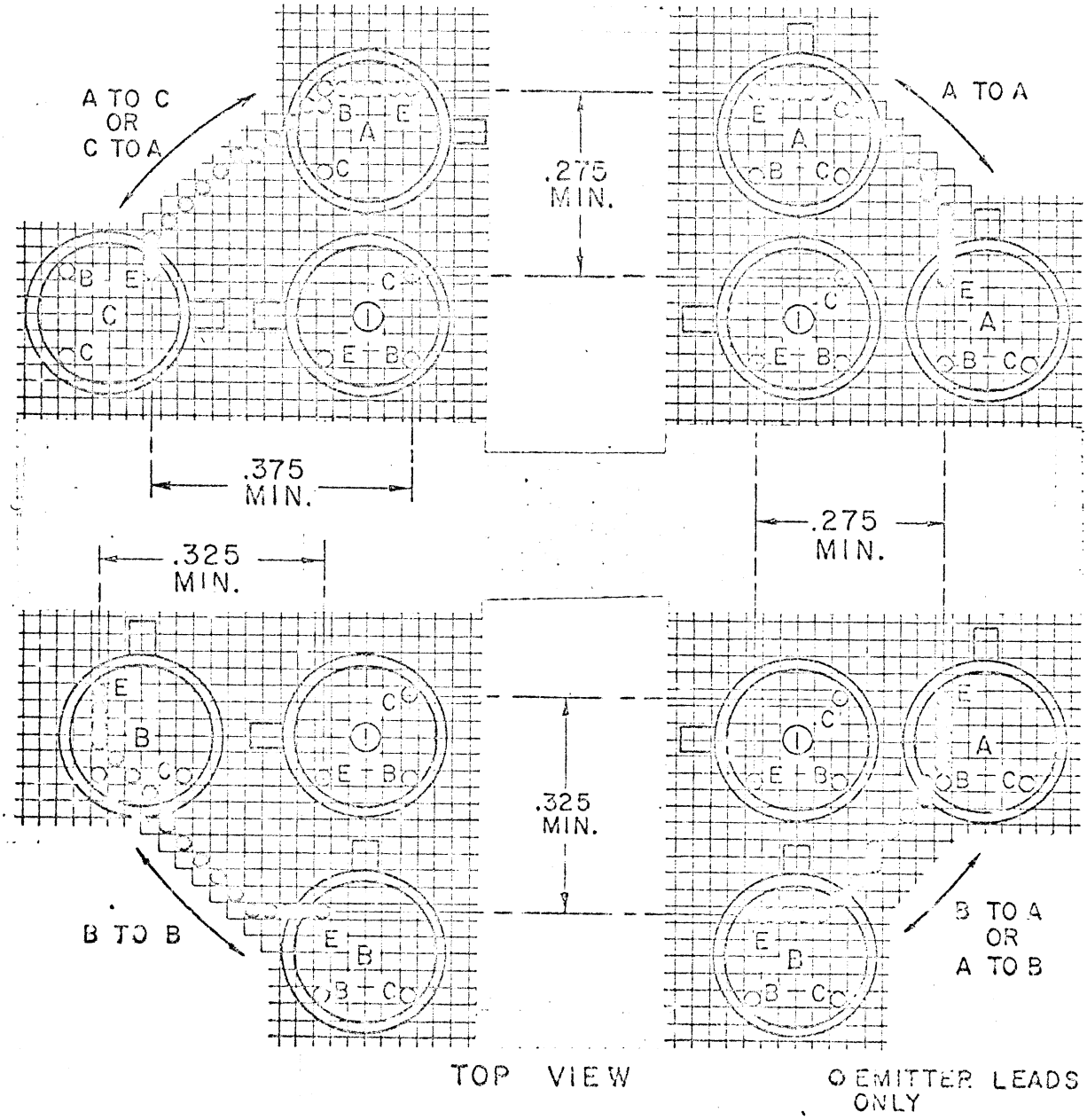


TO-18 and TO-56 packages must be mounted on the following minimum center to center distances.

(A)	Non-adjacent tabs	.275"
(B)	One adjacent tab	.325"
(C)	Two adjacent tabs	.375"

RELATIONSHIPS (CONTINUED)

The following illustration can be used to determine the actual minimum grid placement of the package leads when Note Code HA is used.



RELATIONSHIPS (CONTINUED)

In this illustration, package number (1) is fixed. The other package maintains the same orientation with respect to the card edges and moves about package number (1). Within each segment of this illustration there are portrayed only two packages. The moving package is shown twice, when it is positioned on the same X and Y grids as the fixed package. In these two positions, the moving package has either an A, B, or C on it. This letter indicates the condition existing between the moving and the fixed package. A indicates that a condition of non-adjacent tabs exists. B indicates that a condition of one-adjacent tab exists and C indicates that a condition of two-adjacent tabs exists. REMEMBER: The orientation of the moving package is always the same with respect to the card edges. The lead location for the moving package is given for one lead only. This is sufficient for specifying the minimum mounting of one package to the other. Although the relationship between both packages is shown for only a 90 degree swing of the moving package, the lead locations given must be extrapolated when working in the other 270 degrees around the fixed package.

The procedure to be followed for applying this illustration is outlined below:

a. Placement of TO-18 and TO-56 packages is not complex when both packages are located on the same X and/or same Y grid. Hence, this procedure should be used only when two packages are placed in a staggered manner.

b. Designate one of the transistors, which is on a multi-color or assembly drawing, as the fixed package as portrayed in the above illustration (1).

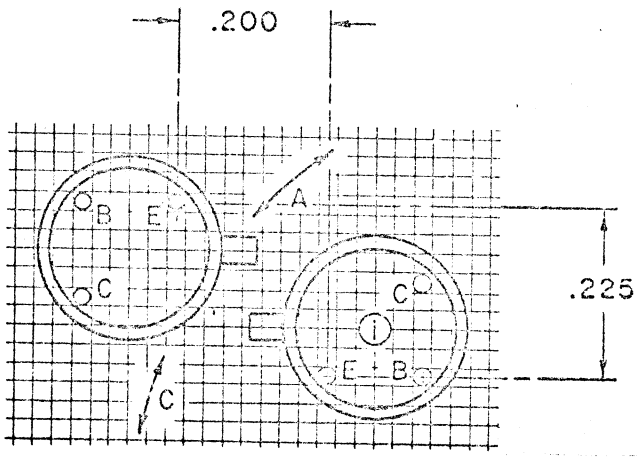
c. Translate the other package maintaining its orientation with respect to the card edges from its staggered position both ways until it is on the same X and same Y grid as the fixed package.

d. Label the translated package in both positions with an A, B, or C.

e. The combination of these two letters indicates which segment of the illustration above to refer to for the lead grid spacing which corresponds to the minimum spacing of the two packages.

RELATIONSHIPS (CONTINUED)

The following illustration is an example of how to use the previous illustration.

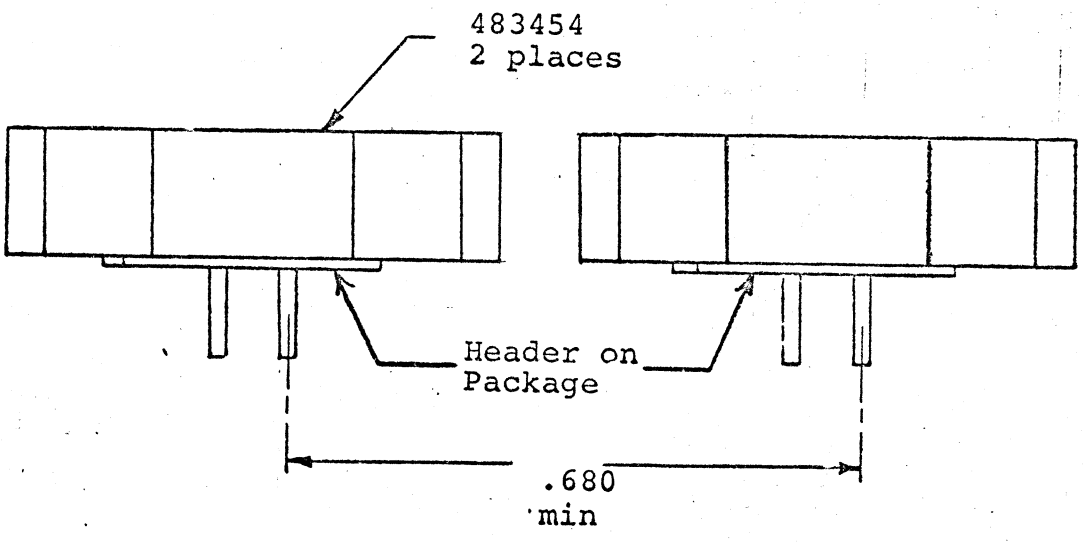


A TO C OR C TO A

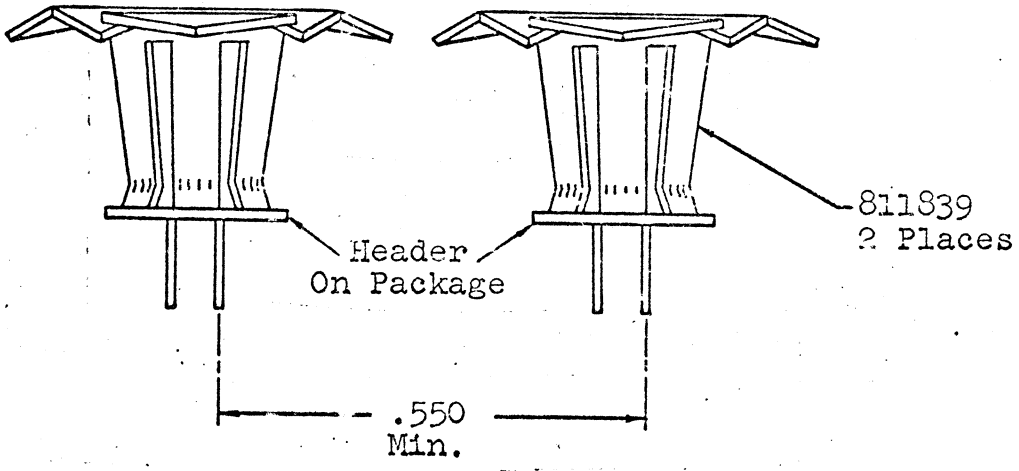
RELATIONSHIPS (CONTINUED) HEAT SINKS

The following illustrations show the physical minimum placement of TO-18 and TO-56 packages with like Heat Sinks.

483454

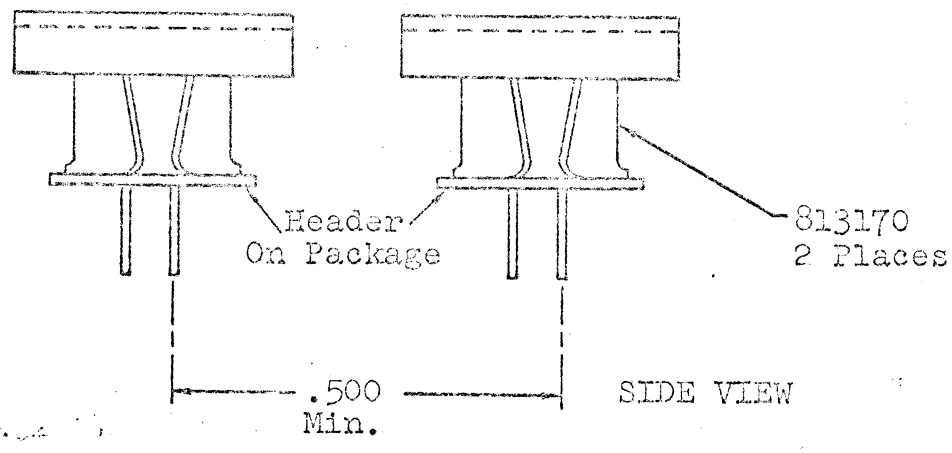


811839

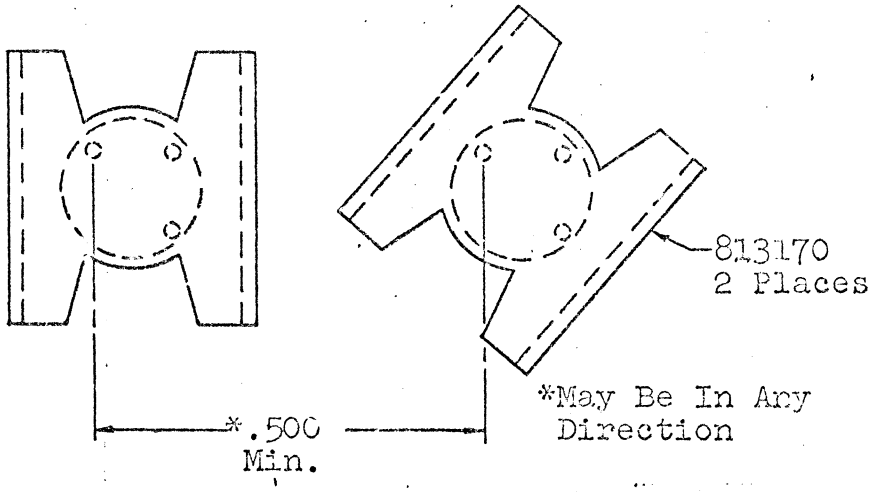


RELATIONSHIPS (CONTINUED) HEAT SINKS

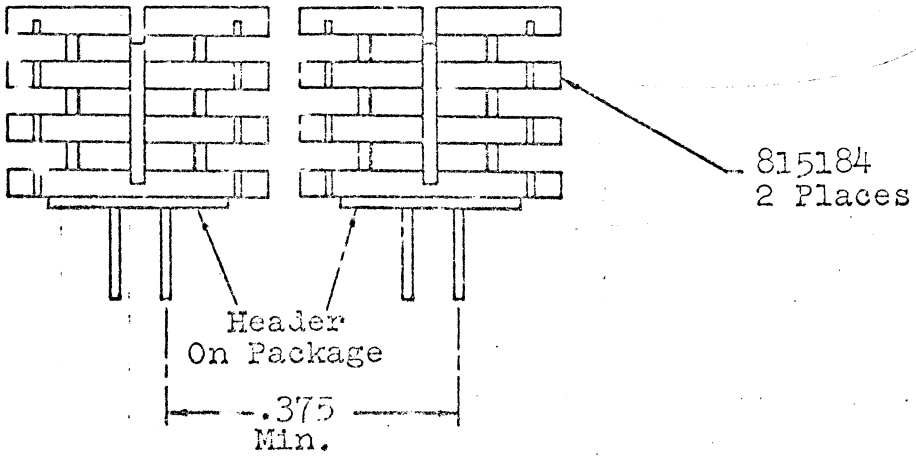
813170



TOP VIEW



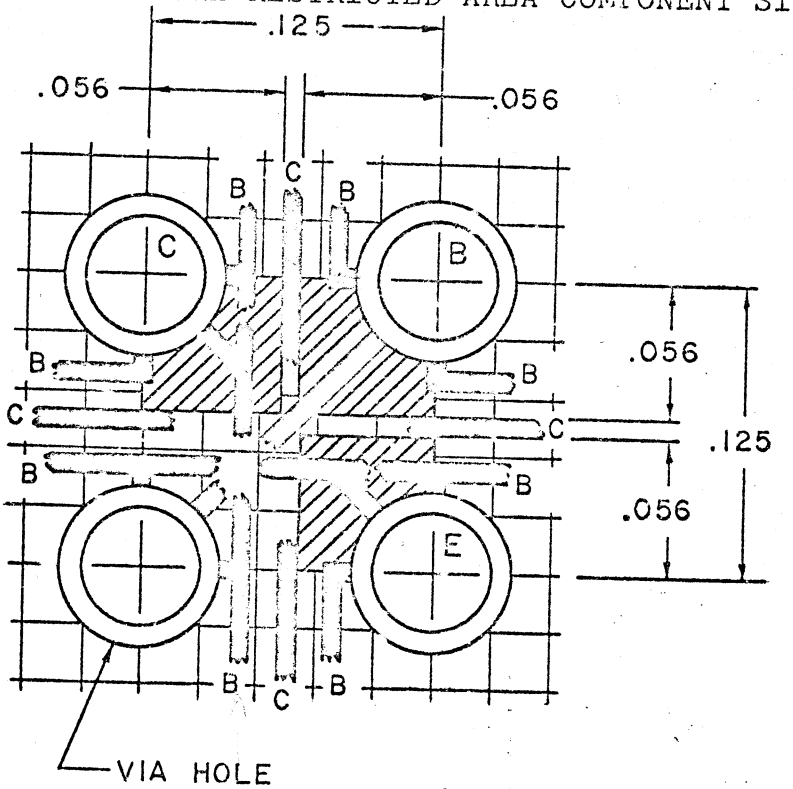
815184



ARTWORKS

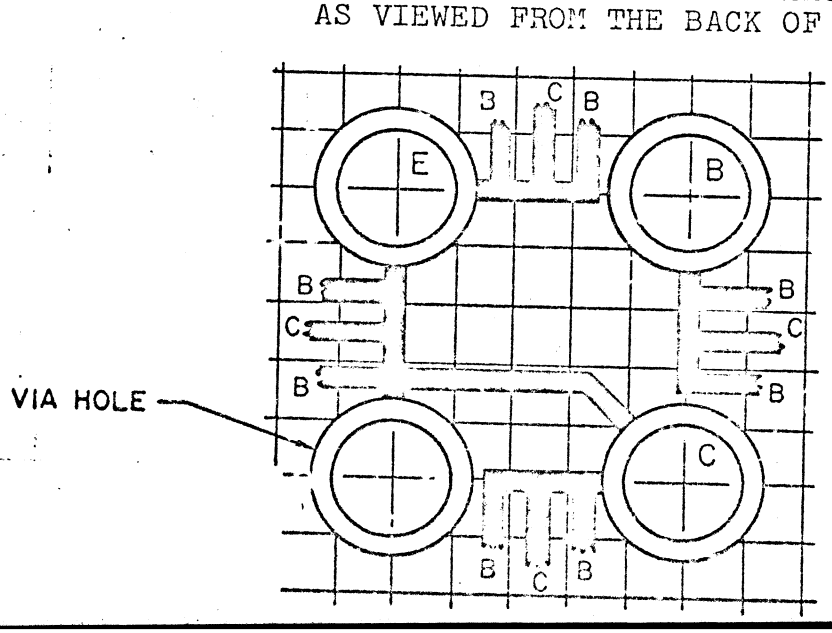
All three leaded TO-18 and TO-56 packages are subject to the following printed wire and artwork restrictions. A .013 "C" printed wire may pass under the transistor on FRONT artworks ONLY. A .013 "B" or "C" printed wire is allowed in the restricted area if common to land and/or lead.

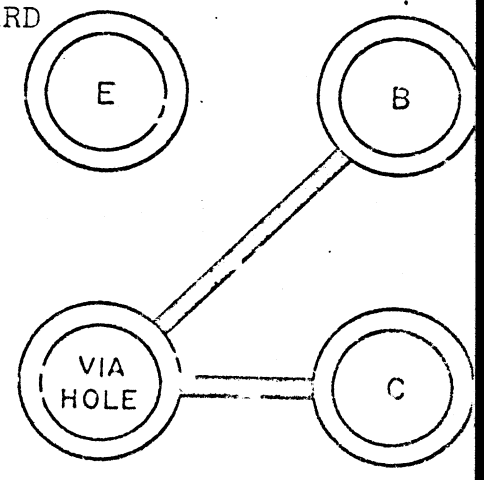
FRONT ARTWORK RESTRICTED AREA COMPONENT SIDE



Back artwork on the solder side of card can only have the following printed wiring placement due to spinning action of the lead clincher.

BACK ARTWORK WIRING PLACEMENT
AS VIEWED FROM THE BACK OF THE CARD

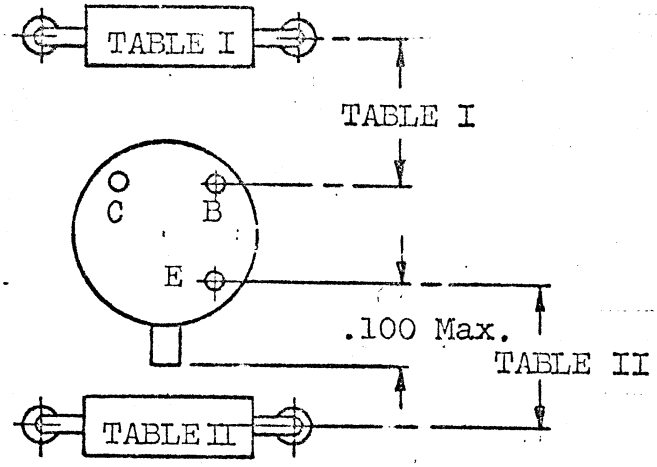


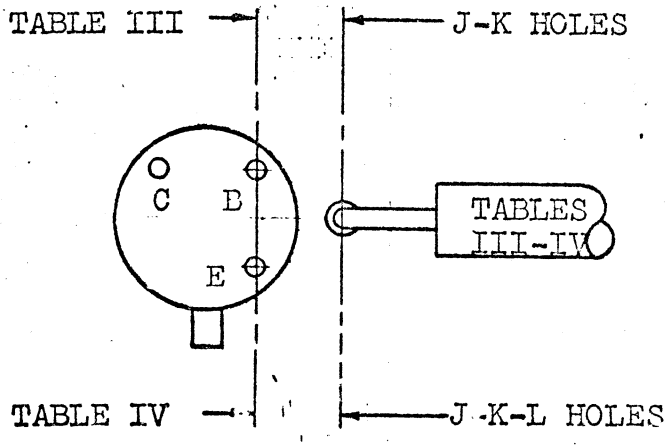


OPTIONS

SEQUENCE EFFECT

The following illustration shows TO-18 and TO-56 with tubular axial-leaded minimum mounting placement.





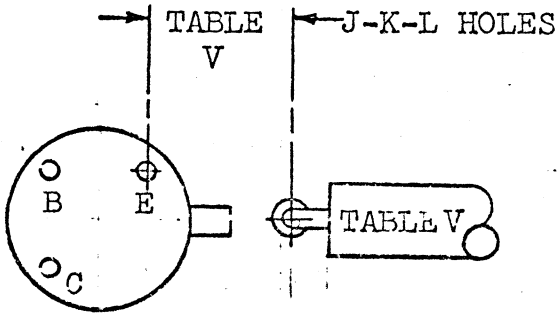


TABLE I	
HOLE SPACING MIN	MAX BODY DIAMETER
.125	.125
.150	.175
.175	.225
.200	.275
.225	.325

TABLE II	
HOLE SPACING MIN	MAX BODY DIAMETER
.150	.100
.175	.150
.200	.200
.225	.250
.250	.300
.275	.325

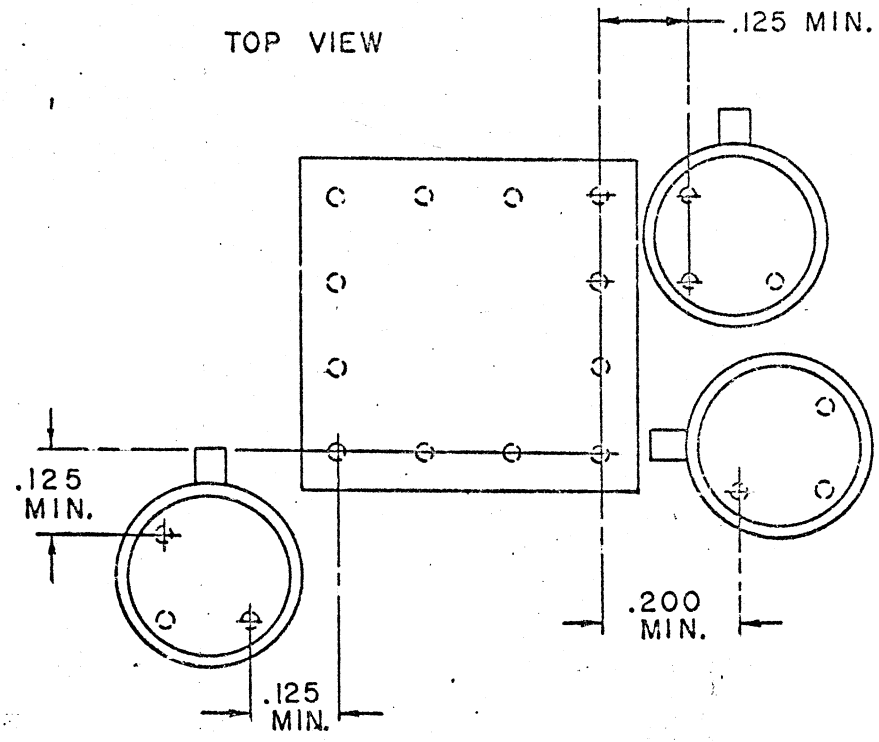
TABLE III	
HOLE SPACING MIN	MAX BODY DIAMETER
.100	.126

TABLE IV	
HOLE SPACING MIN	MAX BODY DIAMETER
.125	.325

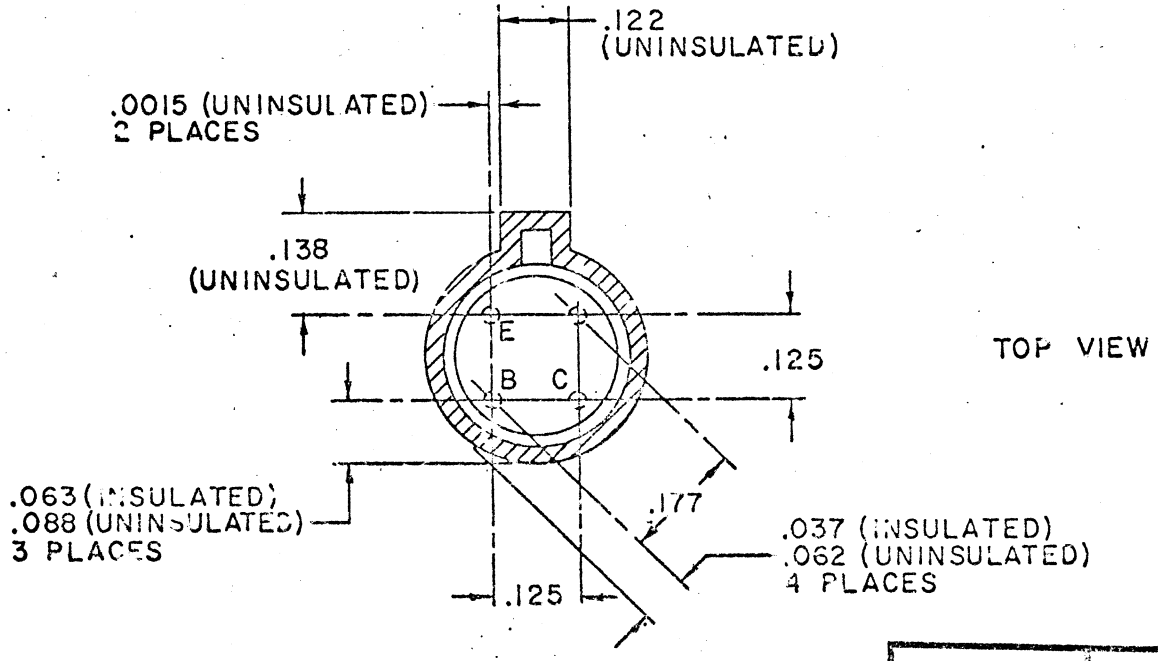
TABLE V	
HOLE SPACING MIN	MAX BODY DIAMETER
.125	.100
.150	.325

SEQUENCE EFFECT (CONTINUED)

The following illustration shows TO-18 and TO-56 packages and SLT module minimum placement.

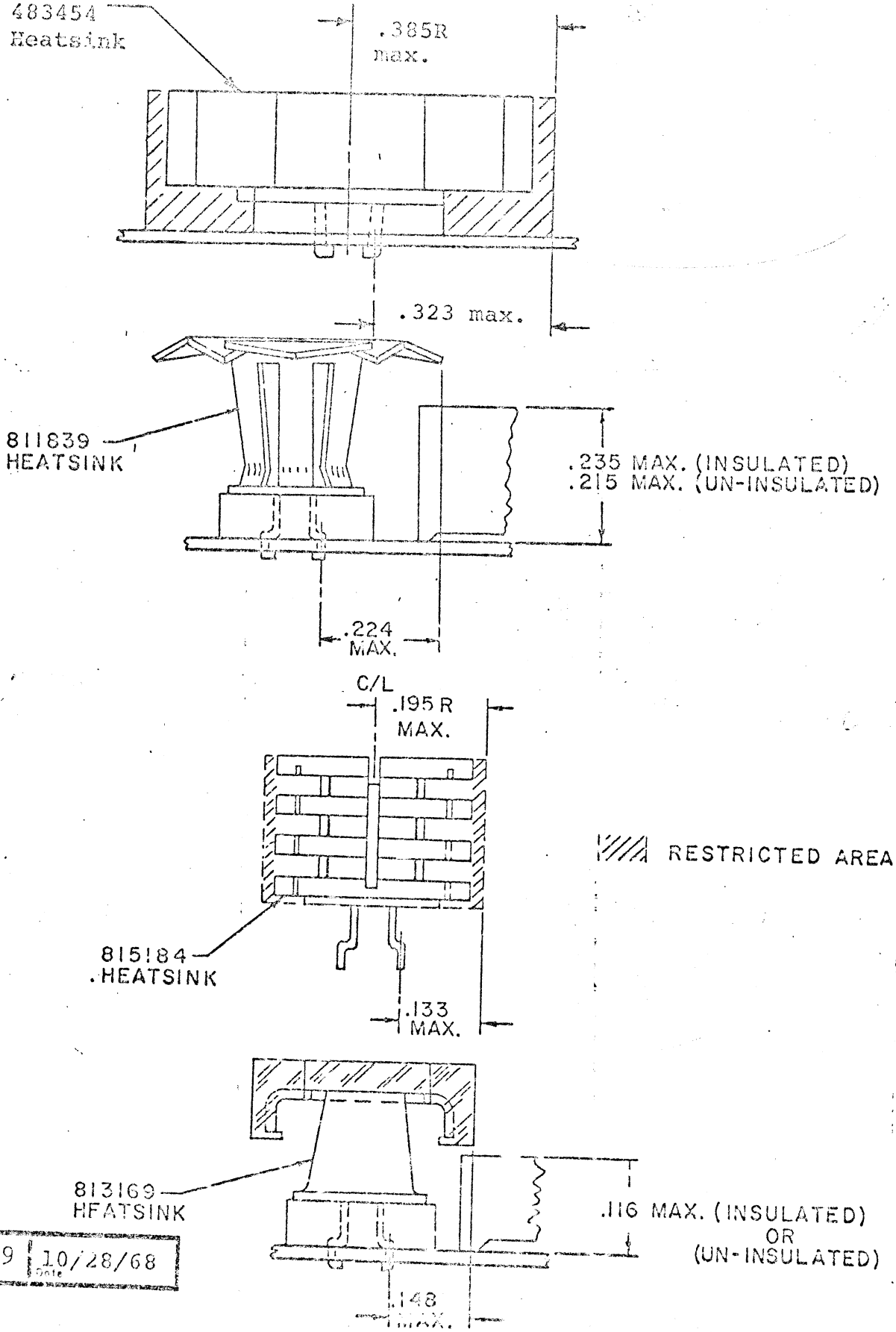


The following illustration shows the TO-18 and TO-56 restricted area required for all other adjacent components.



SEQUENCE EFFECT (CONTINUED)

The following illustration shows TO-18 and TO-56 packages with heat sinks and adjacent components.



HAND ASSEMBLY

All TO-18 and TO-56 packages will be hand assembled if their leads are not on the standard grids ending with digit 3 or 8. All TO-18 and TO-56 packages on MST-4 card assemblies will be hand assembled using double-sided tape.

PROCESS INFORMATION

The assembly machines require the TO-18 and TO-56 leads to be on the standard grid pattern that end with digit 3 or 8 or equivalent.

All packages will have their leads formed and cut prior to assembly.

The use of Si grease should be avoided whenever possible.

No package may have more than one spacer. Any new spacers must be released by Department 307.

All packages must have their leads mounted on a .125 hole pattern.

The leads will be gang-clinched to the card after all other components less than .325 high are assembled.

PLANNING

Semi-automatic equipment for leads not mounted on the standard pattern is not contemplated.

IBM Division Engineering Practice

TRANSISTORS TO-77 TO-78 AND "PRESS ON HEAT SINK"

Supplement of Status

Effective Date: February 16, 1969

Subject: Card Layout Ground Rule Status Suffix 3, Section 12B. This section has been updated to include TO-77 and TO-78 transistor requirements for SLD and MST.

This update supersedes DEP 2-7047, Suffix 3, Section 12B dated 6-15-66.

Requirements

CMT size code added. Hole size requirements defined for MST.

Limits

Expanded to include the five (5) MST card sizes.

DESCRIPTION

Devices in TO77-TO78 packages have metal cans and headers, and have 6 leads glassed in. The package is electrically hot. Assembly drawing code is "Q".

PACKAGE

A TO77 package is very similar in height to a TO 5 but the TO78 is much shorter. All physical outlines of TO77-TO78 packages are contained in the following coded list and are in the Component Library maintained by E. C. level of the component part number:

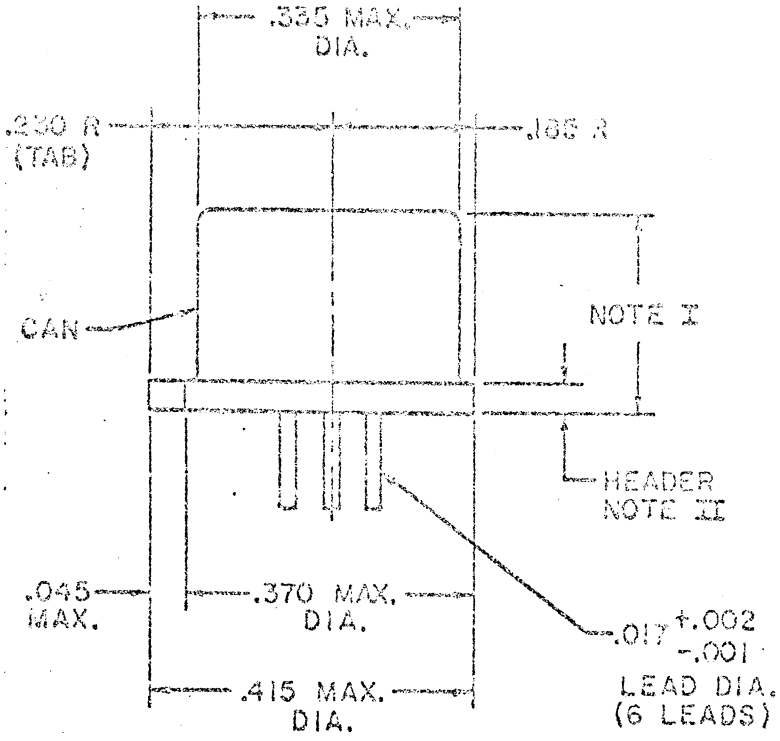
NON-AUTOMATED - 6 LEADS

3 TO 5E
23T78B, 21T77B

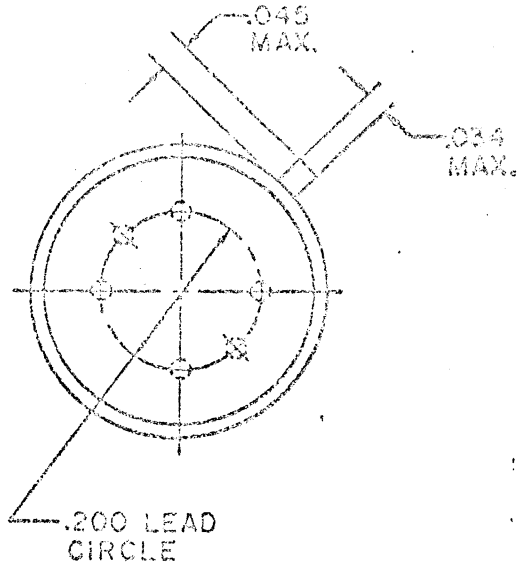
The components are purchased with leads on a .200 diameter lead circle and are later formed and skewed to fit a .250 x.250 hole pattern. Prior to manual insertion a spacer is assembled, this provides the package with support and standoffs.

The device industry (JETEC) had registered this package as R052 when originated. The R052 was to be changed to T052, but type T052 was used for designation of another transistor package. Therefore, R052 has been changed to T077 and T078.

PACKAGE (CONTINUED)



SIDE VIEW
6 LEADED UNFORMED



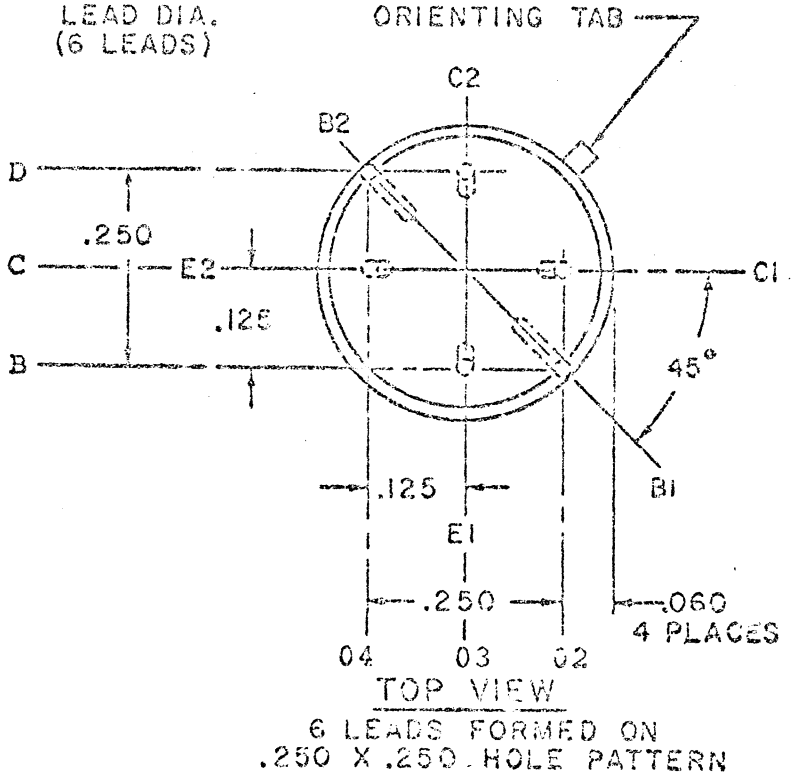
TOP VIEW
6 LEADED UNFORMED

NOTE I

.260 MAX. (3T05E, 21T77S)
.185 MAX. (23T78S)

NOTE II

.135 MAX. (3T05E)
.040 MAX. (23T78S, 21T77S)



TOP VIEW
6 LEADS FORMED ON .250 X .250 HOLE PATTERN

Views shown are for packaging purposes only and part drawing has precedence.

REQUIREMENTS

Leads of these components must be mounted in:

"J" .040 holes for SLT/SLD
.040 holes for MST 1 & 2
.031 holes for MST 4

Note codes must be used as follows:

Note code HE calling for the use of spacer part number 811660 must be used for all packages. The note code will appear on the package and in the note code field on the assembly drawing.

Heat sink 483376 non-insulated can be used on 21T77B physical outline only. Si grease 483151 must not be used with this heat sink. The package on the assembly drawing will reflect note code HE. Heat sink does not require any note code. The component part drawing shall take precedence over all views.

CMT Coding

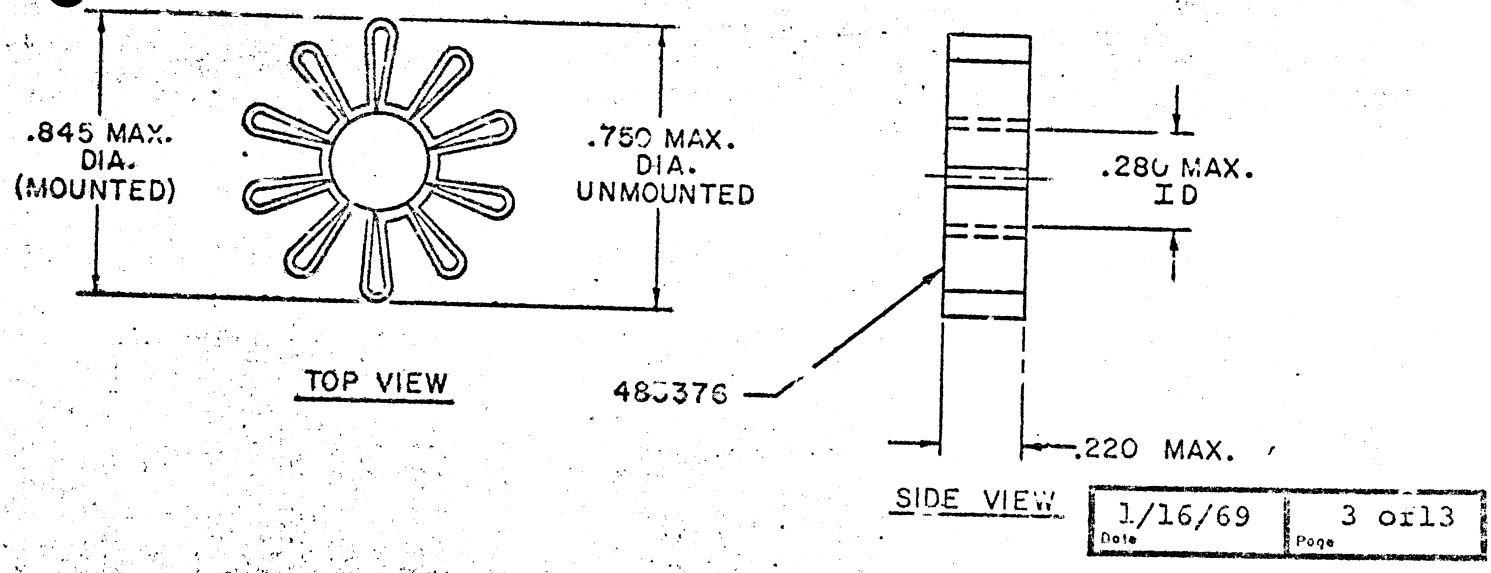
Transistors TO77 and TO78 with required spacer 811660 must be coded in the "A" direction with B1 and E1 in line parallel to the "X" - "X" axis. These packages must be coded as a 8x8 component with lead codes as follows:

E1 - B03	E2 - C04
B1 - B02	B2 - D04
C1 - C02	C2 - D03

HEAT SINKS

Heat sinks 492434, 492435, 813172, 813193, 814005, and 813168 cannot be used on these packages.

483376 Heat Sink



LIMITS

On a standard .125 pattern, package leads will be placed on or within the following X and Y grids. Orientation tabs may be in any of the four quadrants.

SLT/SLD

1-Hi 6 and 12	X 28 - 73 - 143	Y 28 - 58
2-Hi 6 and 12	X 28 - 73 - 143	Y 28 - 118
3-Hi 12	X 28 - 143	Y 28 - 178

MST

2-Hi 1,2,4 wide	X 02 - 11 - 25 - 53	YC - V
3-Hi 2,4 wide	X 02 - 25 - 53	YC - 8

On a random pattern, package leads will be placed on or within the following X and Y grids. Orientation tabs may be in any of the four quadrants.

SLT/SLD

1-Hi 6 and 12	X 24 - 77 - 147	Y 24 - 61
2-Hi 6 and 12	X 24 - 77 - 147	Y 24 - 121
3-Hi 12	X 24 - 147	Y 24 - 181

LIMITS HEAT SINK

T077 package using Heat Sink 483376 must have their leads on or within the following X and Y grids.

SLT/SLD

1-Hi 6 and 12	X 32 - 69 - 139	Y 33 - 53
2-Hi 6 and 12	X 32 - 69 - 139	Y 33 - 113
3-Hi 12	X 32 - 139	Y 33 - 173

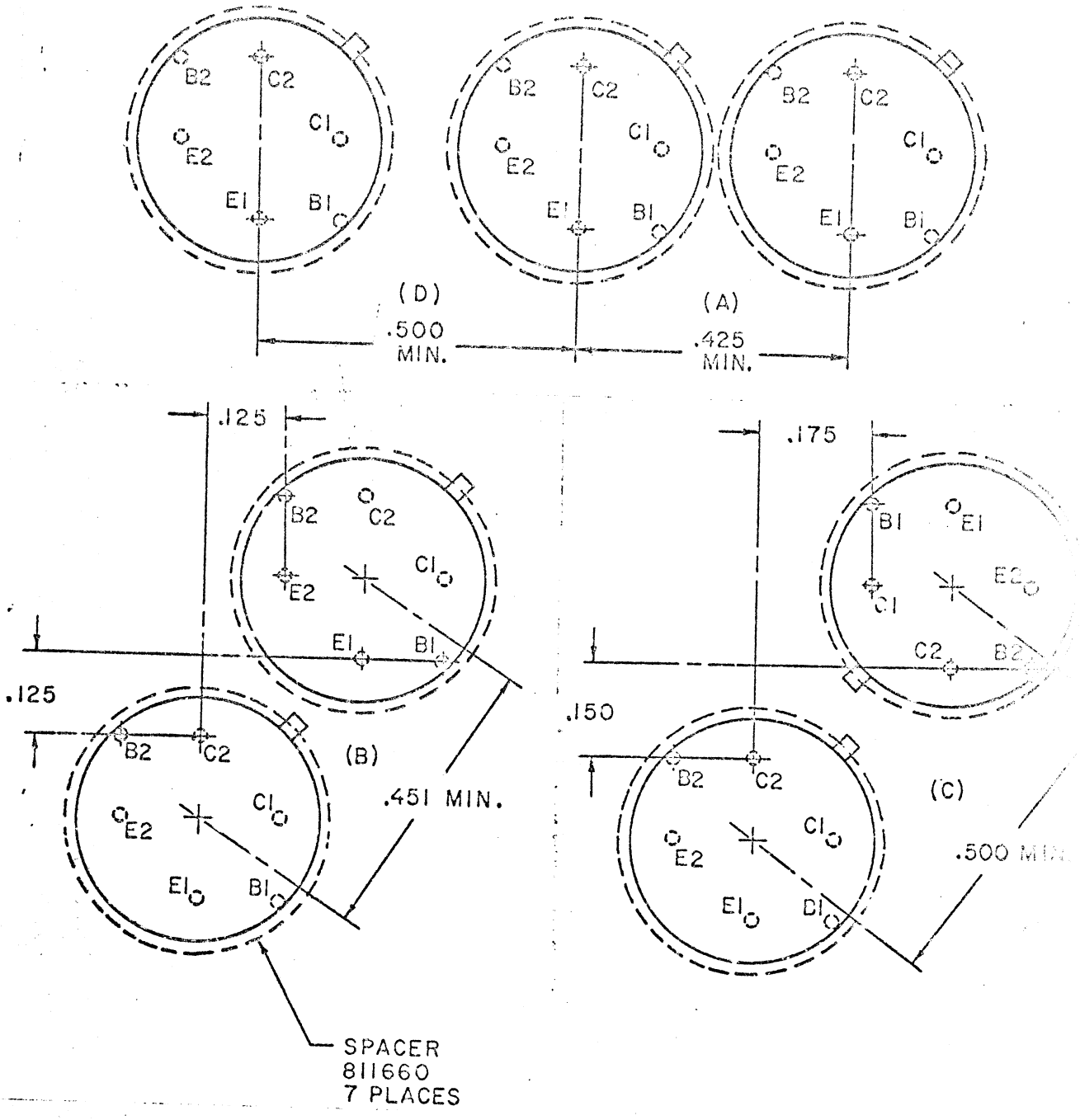
MST

2-Hi 1,2,4 wide	X 03 - 10 - 24 - 52	YC - U
3-Hi 2,4 wide	X 03 - 24 - 52	YC - 7

RELATIONSHIPS

The following illustration shows the physical minimum placement of all packages.

TOP VIEW

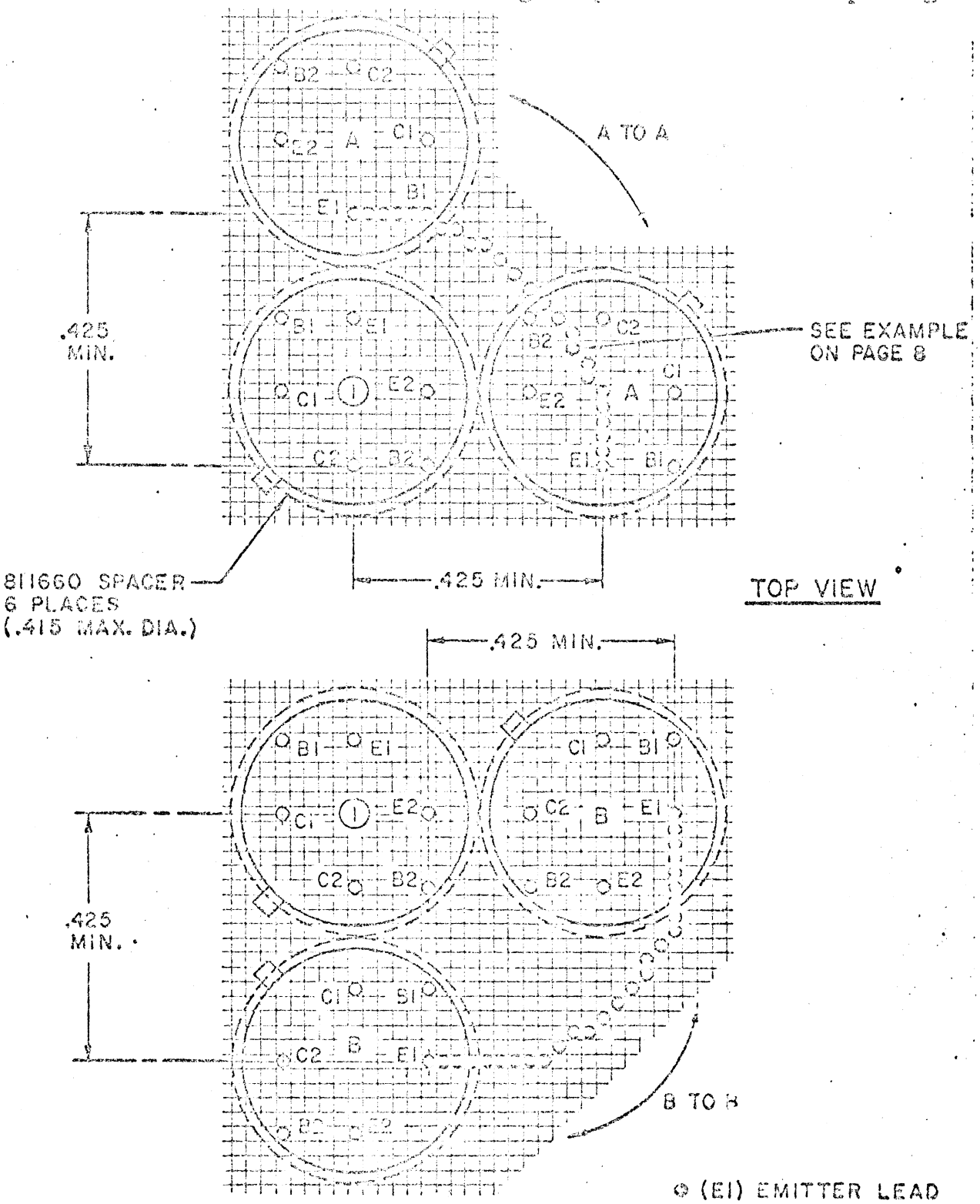


Packages must be mounted on the following minimum center to center distances.

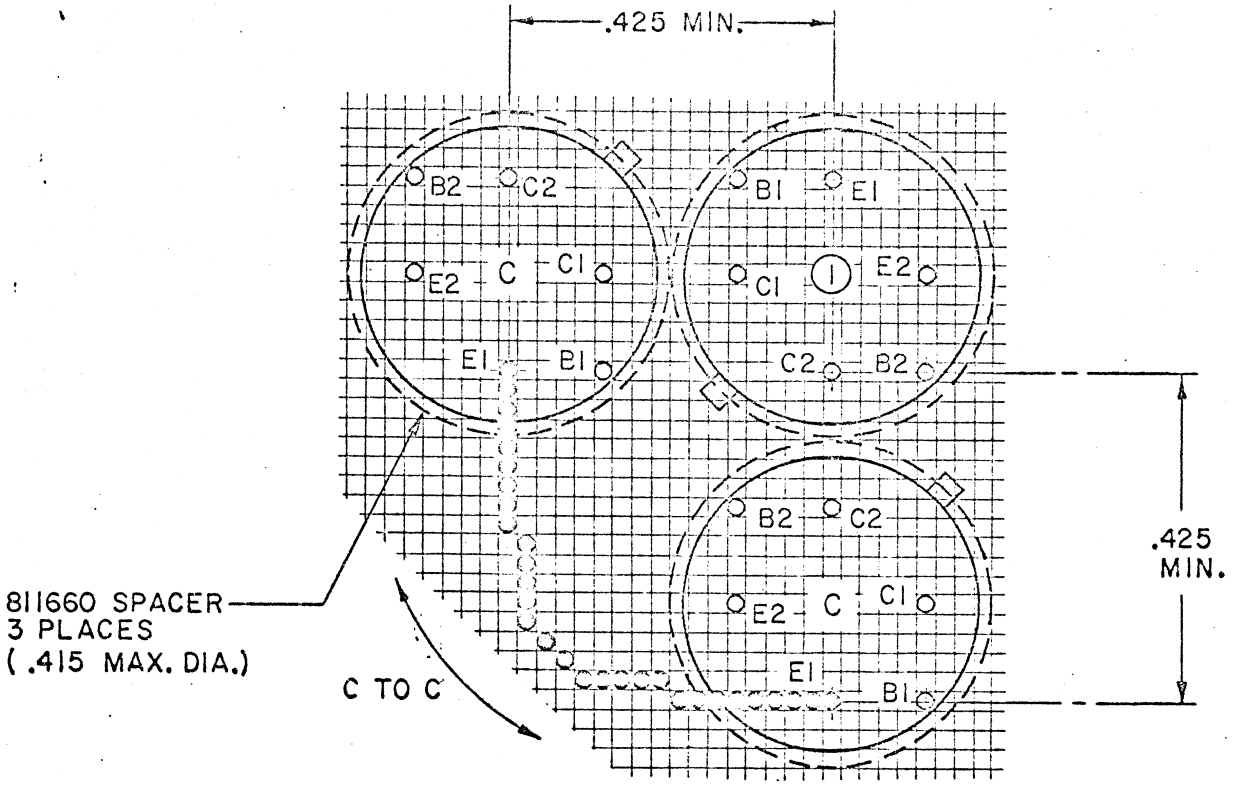
(A) Non-adjacent tabs .425 MIN
(B) One-adjacent tab .451 MIN
(C) Two-adjacent tabs .500 MIN
(D) Any orientation on a standard pattern .500 MIN

RELATIONSHIPS (CONTINUED)

To facilitate the use of these minimum mounting centers (.425, .451, .500, .500) the following illustration can be used to determine the actual minimum grid placement of the package leads.



RELATIONSHIPS (CONTINUED)



TOP VIEW

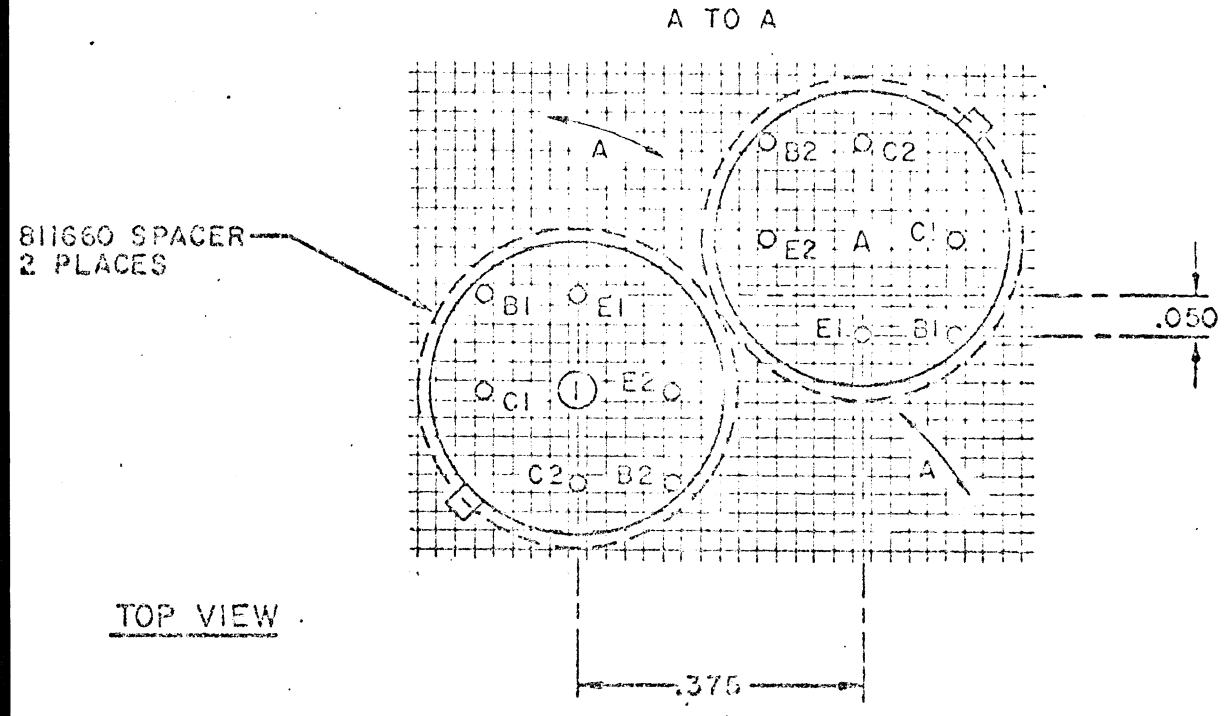
The previous three illustrations package number 1 is fixed. The other package maintains the same orientation with respect to the card edges and moves about package number 1. Within each segment of this illustration there are portrayed only two packages. The moving package is shown twice, when it is positioned on the same X and Y grids as the fixed package. In these two positions, the moving package has either an A, B, or C on it. This letter indicates the condition existing between the moving and the fixed package. A indicates that a condition of non-adjacent tabs exists. B indicates that condition of one-adjacent tab exists and C indicates that a condition of two-adjacent tab exists. REMEMBER: The orientation of the moving package is always the same with respect to the card edges. The lead location for the moving package is given for one lead only. This is sufficient for specifying the minimum mounting of one package to the other. Although the relationship between both packages is shown for only a 90 degree swing of the moving package, the lead locations given must be extrapolated when working in the other 270 degrees around the fixed package.

RELATIONSHIPS (CONTINUED)

The procedure to be followed for applying the three previous illustrations is outlined below:

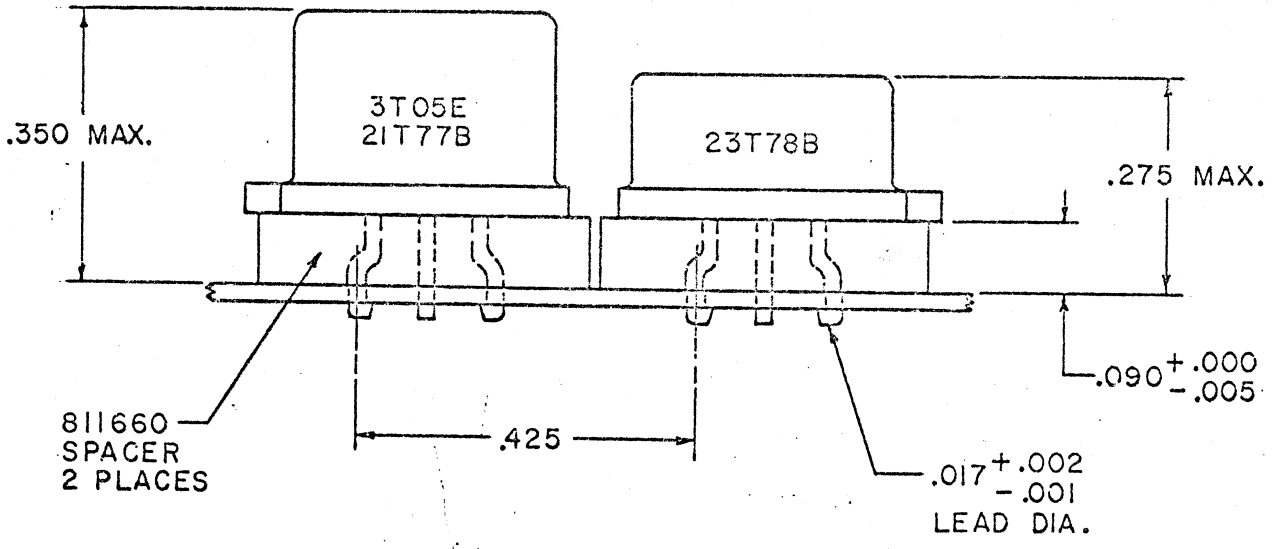
a. Placement of the packages is not complex when both packages are located on the same X and/or same Y grid. Hence, this procedure should be used only when two packages are placed in a staggered manner.
b. Designate one of the transistors, which is on a multi-color or assembly drawing, as the fixed package as portrayed in the previous illustrations as 1.
c. Translate the other package maintaining its orientation with respect to the card edges from its staggered position both ways until it is on the same X and same Y grid as the fixed package.
d. Label the translated package in both positions with an A, B, C, or combinations.
e. These letters indicate which segment of the illustration to refer to for the lead grid spacing which corresponds to the minimum spacing of the two packages.

The following illustration is an example of how to use the three previous illustrations.

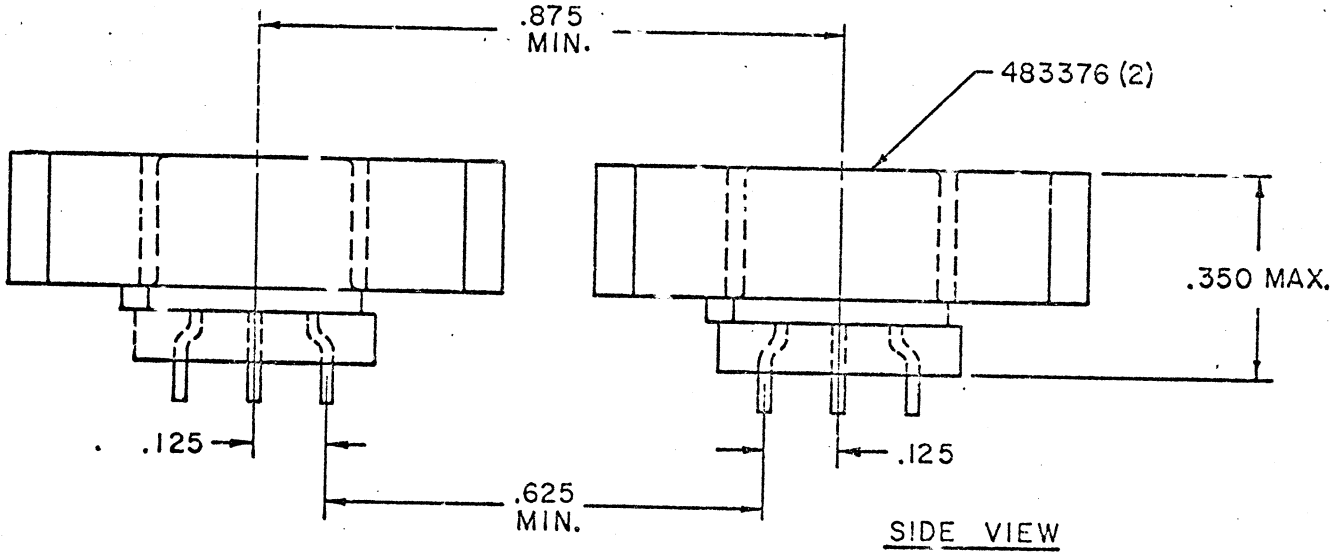


RELATIONSHIP (CONTINUED)

The following illustration shows the minimum placement of packages including their spacers.



The following illustration shows the minimum physical placement of T077 package using physical outline 21T77B and heat sink 483376.



ARTWORK

There are no artwork restrictions associated with the usage of this component package.

SEQUENCE EFFECT

The following illustration shows the packages and tubular axial mounting placement.

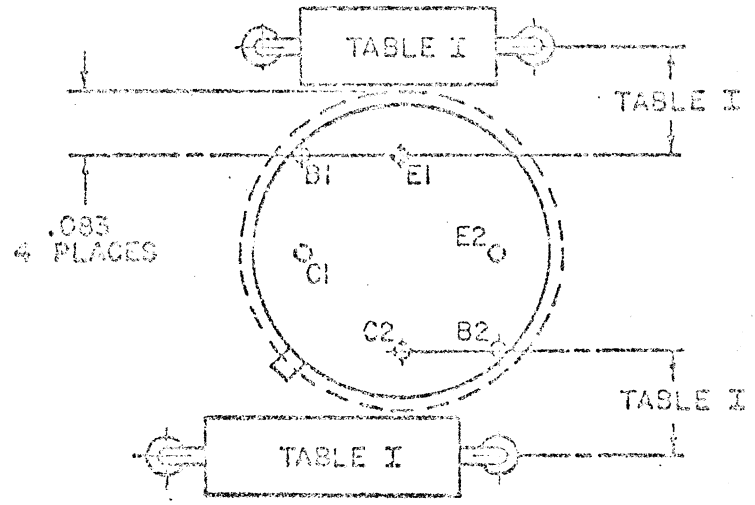
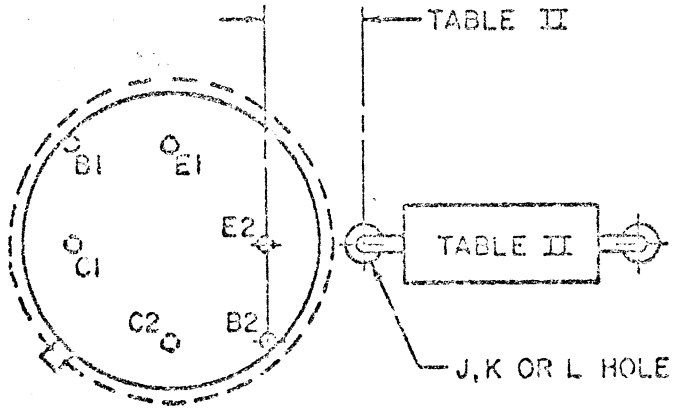
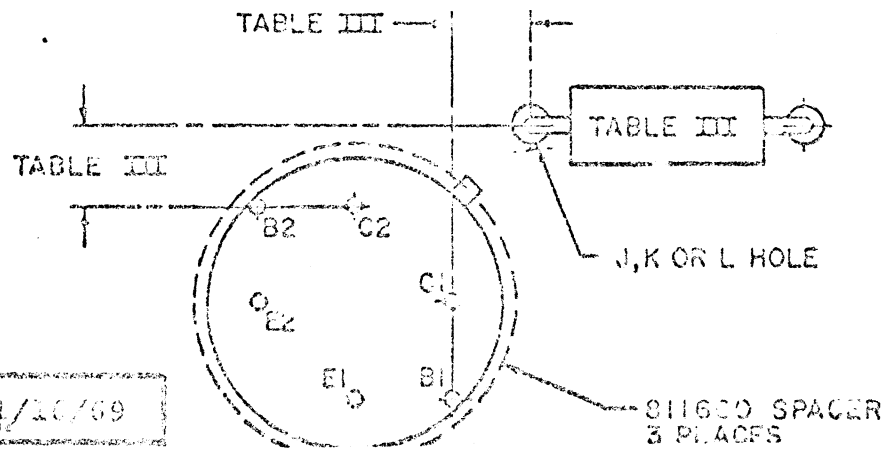


TABLE I	
HOLE SPACING MIN.	MAX. BODY DIAMETER
.125	.084
.150	.134
.175	.184
.200	.234
.225	.284
.250	.334
.275	.384
TABLE II	
HOLE SPACING MIN.	MAX. BODY DIAMETER
.125	.370
TABLE III	
HOLE SPACING MIN.	MAX. BODY DIAMETER
.100	.370

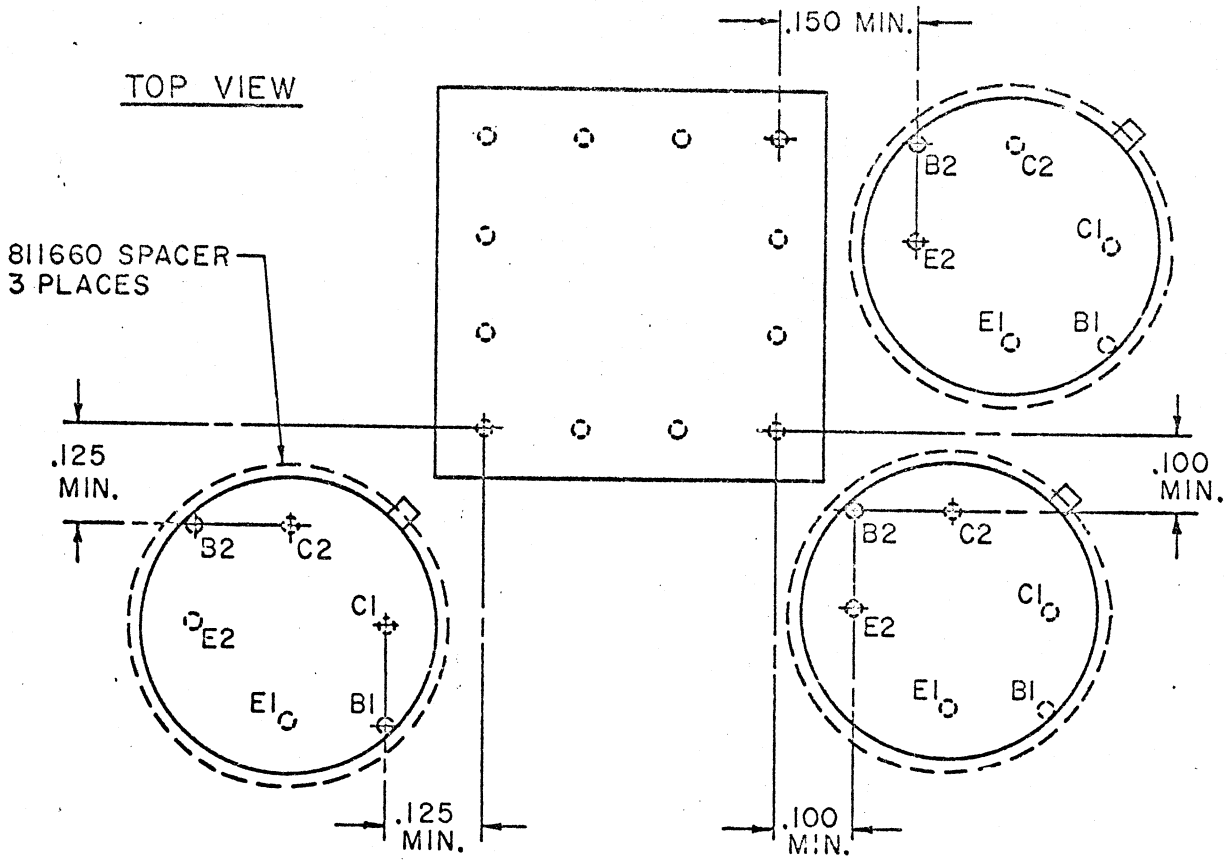


TOP VIEWS

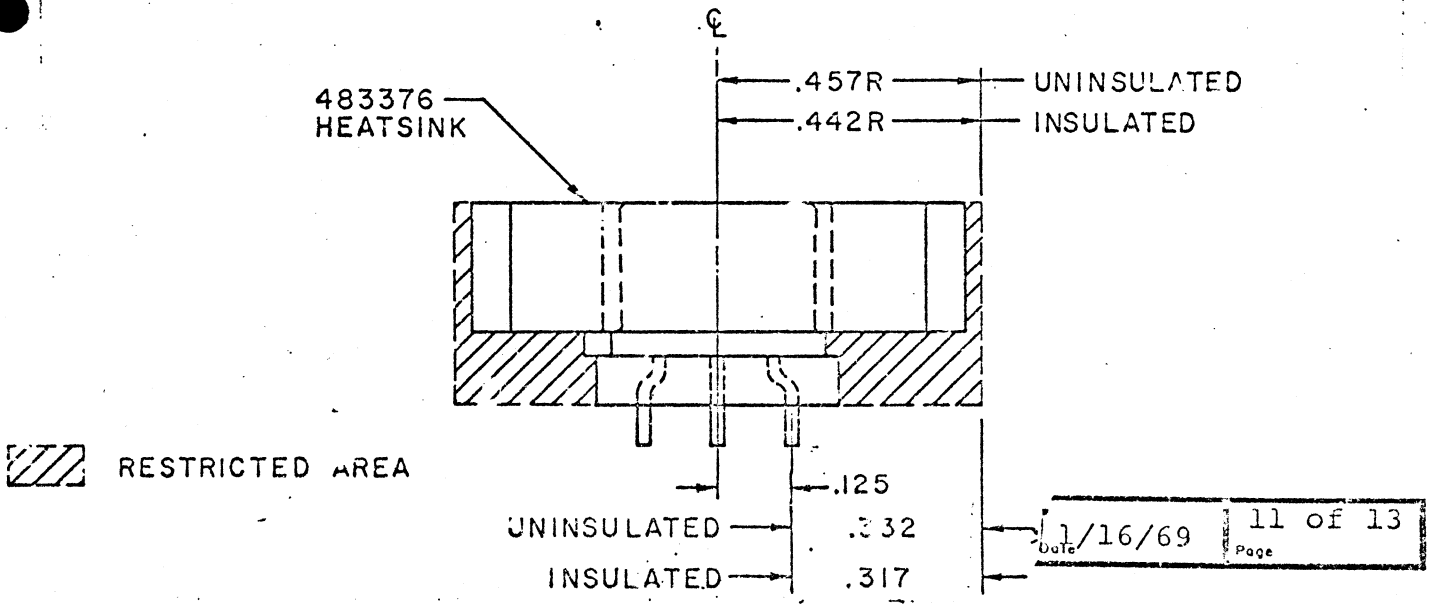


SEQUENCE EFFECT (CONTINUED)

The following illustration shows the packages and SLT module placement.

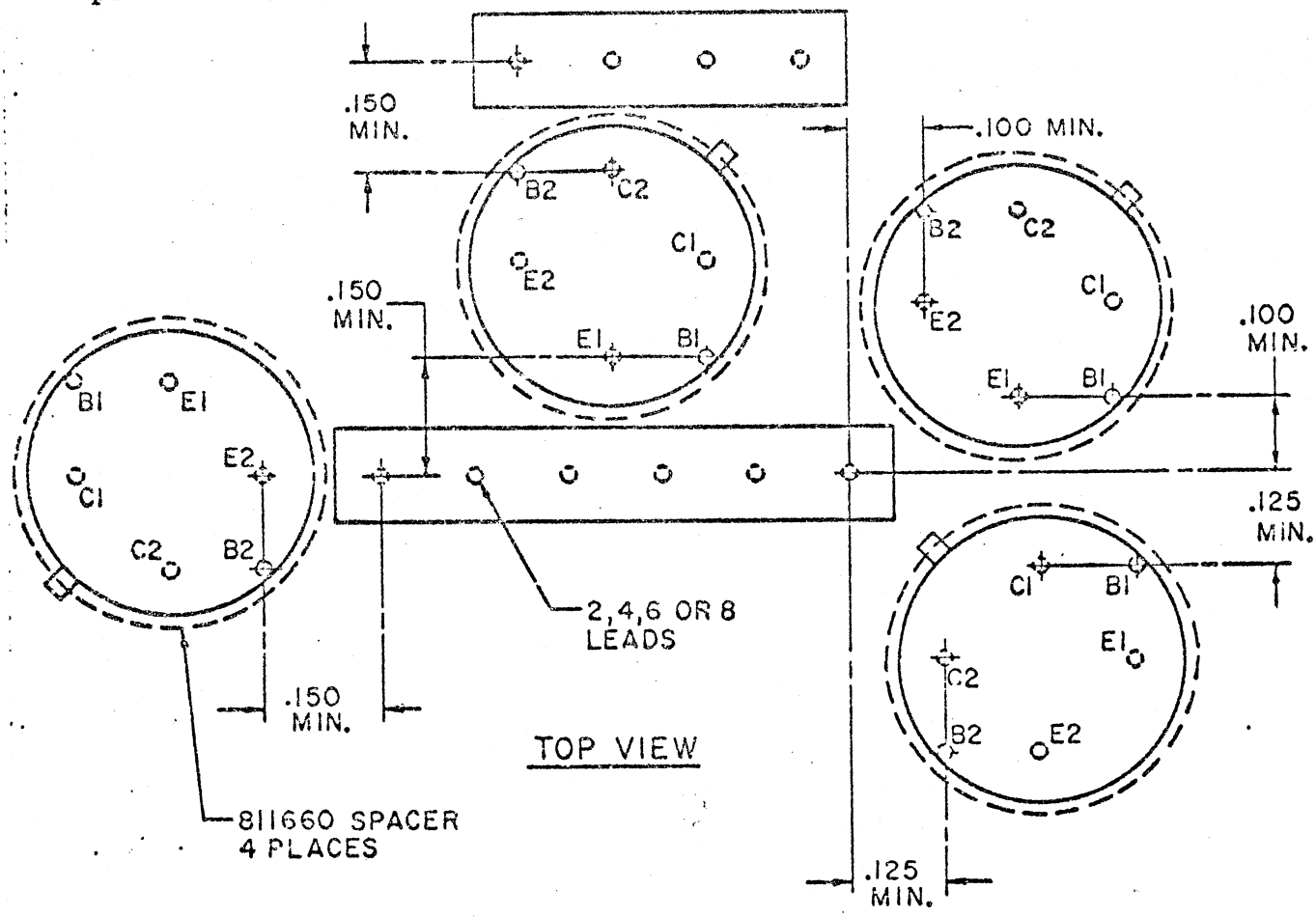


The following illustration shows the package with heat sink and the restricted area required. Clearance from other uninsulated or electrically hot components must be a minimum of .035". (.015" electrical clearance plus an additional .020" manufacturing tolerance) Clearance from insulated components must therefore be a minimum of .020".

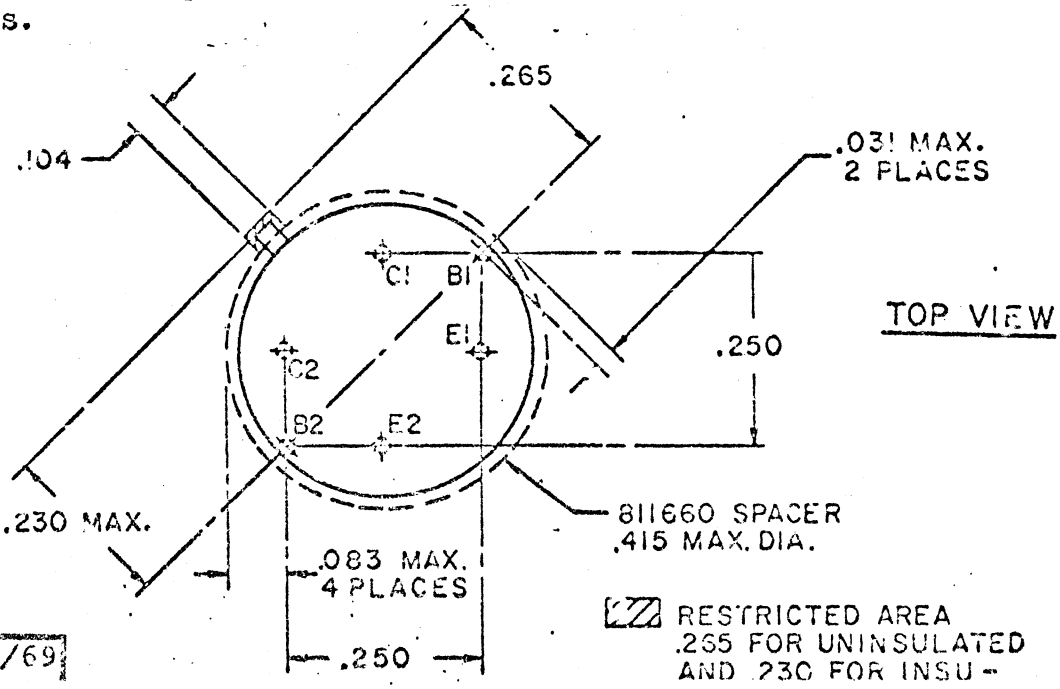


SEQUENCE EFFECT (CONTINUED)

The following illustration shows the packages and R/C module placement.



The following illustration shows the package and the restricted area required for the assembly of all other components.



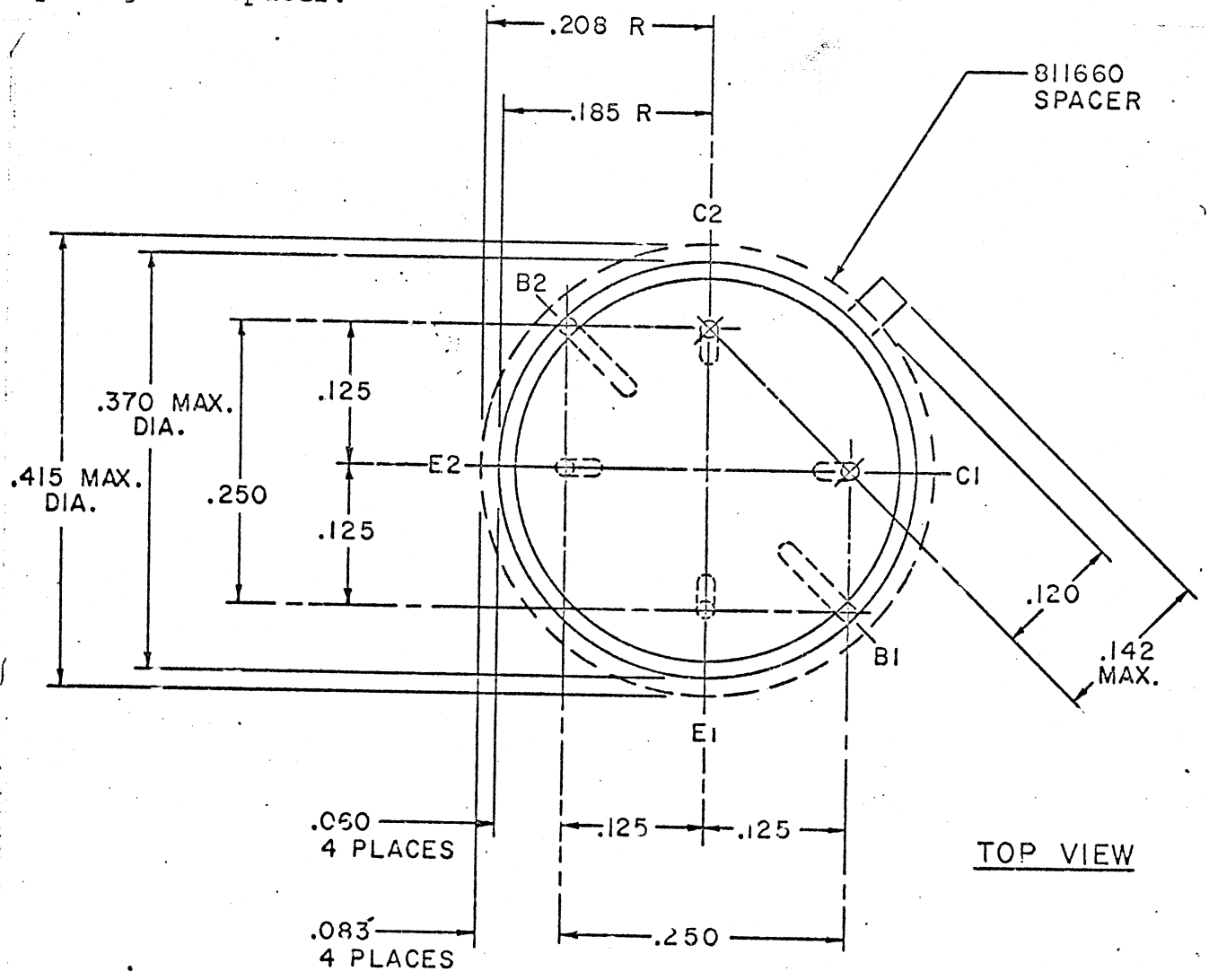
HAND ASSEMBLY

All packages are manually assembled with spacers if leads are not on the standard X-Y grids ending in 3 or 8, or equivalent.

PROCESS INFORMATION

All packages will have their leads formed and cut prior to assembly.

No package may have more than one spacer. The following illustration shows the formed leads and the dimensional relationship of them to the package or spacer.



Important consideration: It is preferred that all packages have their leads placed on X-Y grids ending in 3 or 8 or equivalent, in order to semi-automatically flag the leads.

PLANNING

Semi-automatic equipment for leads not mounted in standard pattern is not contemplated.

CARD LAYOUT GROUND RULES

IBM Division Engineering Practice

TRANSISTORS TO-5 and TO-55 AND "PRESS ON" HEAT SINKS

Supplement of Status

EFFECTIVE DATE: February 16, 1969

SUBJECT: Card Layout Ground Rule Status Suffix 3, Section 10A.

This section has been updated to include TO-5 and TO-55 Transistor requirements for SLD and MST.

This update supersedes DEP 2-7047, Suffix 3, Section 12C dated 9-1-66 and Book 03-10, DEP 2-6420-530, page 6 under Transistors in TO-5 or TO-55 Packages with Spacer 811399.

REQUIREMENTS

CMT size code added. Hole size requirements defined for MST.

LIMITS

Expanded to include the five (5) MST card sizes.

PROCESS INFORMATION

Changed Dept. 146 to Dept. 307.

PLANNING

Changed Dept. 146 to Dept. 307.

CARD LAYOUT GROUND RULES

IBM Division Engineering Practice

TRANSISTORS TO-5 and TO-55 AND "PRESS ON" HEAT SINKS

DESCRIPTION

Devices in TO-5 and TO-55 packages have metal cans and headers and have 3 leads glassed in. The package is electrically hot and may contain a variety of components. Assembly drawing code is "Q" for transistors.

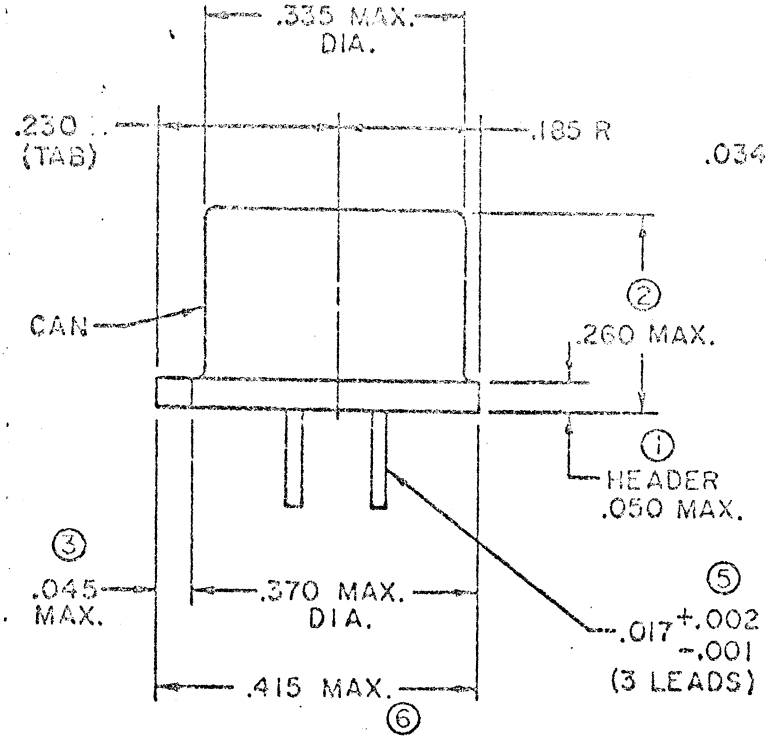
PACKAGE

All physical outlines of TO-5 and TO-55 packages are contained in the following coded list and are in the Component Library maintained by E.C. level of the component part number:

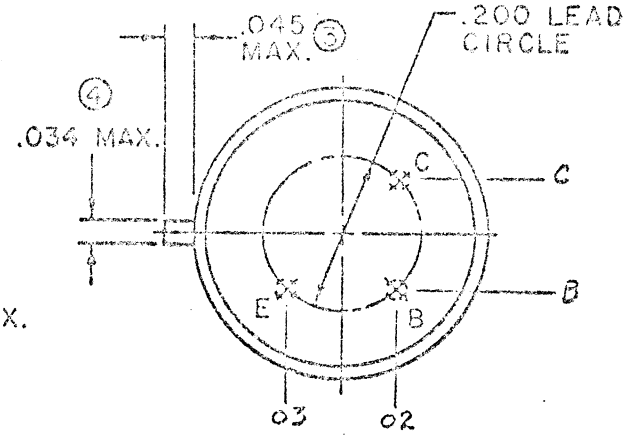
TO-5	TO-55	
3-TO-5A	15-T55A	15-T55D1
3-TO-5B2	15-T55B	15-T55E
3-TO-5B5	15-T55C	
3-TO-5C	15-T55C1	
3-TO-5D		

The components are purchased with leads on a .200 diameter lead circle but are assembled to a .177 diameter lead circle to fit the .125 hole pattern without forming. This is the result of the lead dia vs the hole diameter.

PACKAGE (Continued)



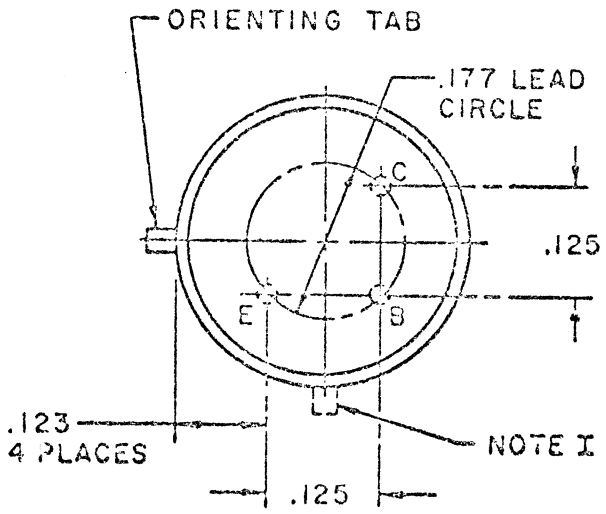
SIDE VIEW
3 LEADED AS RECEIVED



TOP VIEW
3 LEADED AS RECEIVED

① THRU ⑥ ARE THE DIFFERENCES AS INDICATED BY PHYSICAL OUTLINE DRAWINGS.	
15T55C1	⑤ .025 ± .003
15T55D	⑤ .025 ± .003
3T05A	① .135, ② .300, ⑤ .017 +.010 -.001
3T05C	① NO DIM., ③④⑥ NO TAB
3T05D	① .135, ② .300, ⑤ .017 +.010 -.001

NOTE
I. PHYSICAL OUTLINE 3T05D HAS DIFFERENT TAB POSITION AND THE NORMAL E-B-C IS B2-E-B1 FOR UNIJUNCTION TRANSISTOR ONLY.



TOP VIEW
3 LEADED ON CARD ASSEMBLY

REQUIREMENTS

Leads of these components must be mounted in:

"J" .040 holes for SLT/SLD
.040 holes for MST-1 and 2
.031 holes for MST-4

Transistors reflecting physical outlines 15T55C1 and 15T55D can not be mounted on MST-4 card assemblies because of their .028 maximum lead diameter.

Note codes must be used as follows:
HB - Note HB calling for the use of spacer part number 811399 must be used for all packages. The note code will appear on the package and in the note code field on the assembly drawing.

CMT CODING

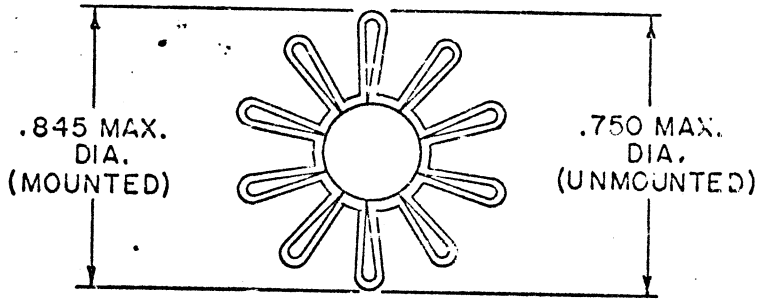
TO-5 and TO-55 packages with required spacer 811399 must be coded in the "A" direction with emitter and base in line parallel to the "Y-Y" axis and card housing. This orientation places the tab parallel to the "Y-Y" axis.

These packages must be coded as a 4 x 4 component with lead codes as follows:
Emitter - B03
Base - B02
Collector - C02

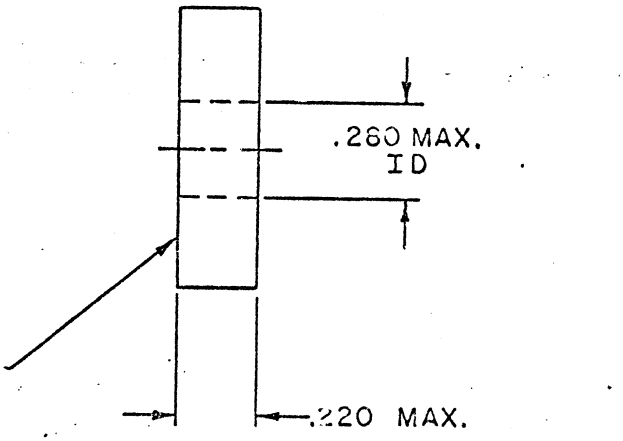
HEAT SINKS

483376 Heat Sink

Heat Sink 483376 non-insulated can be used on all physical outlines. Si grease must not be used with this Heat Sink. CMT size code is 8 x 8.



TOP VIEW



SIDE VIEW

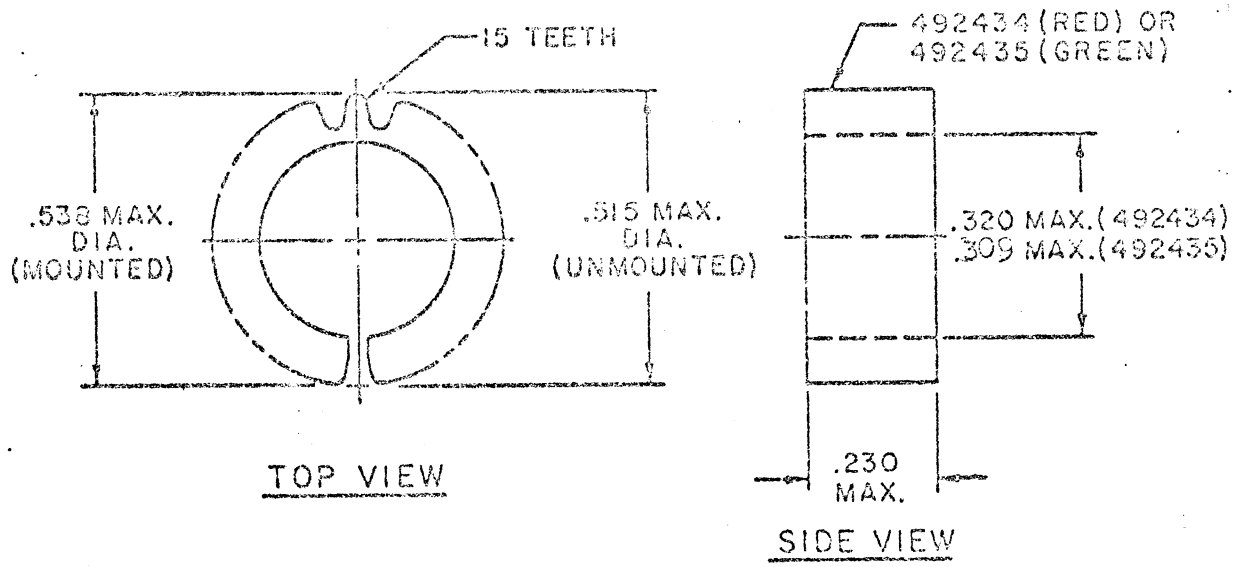
REQUIREMENTS (Continued)

HEAT SINKS

492434 and 492435 Heat Sink

These are non-insulated (gear type). Si grease cannot be used with these Heat Sinks. CMT size code is 6 x 6.

Note code FX must be used. It will appear on the Heat Sink view and in the note field on the assembly drawing. The component listing on the assembly drawing will have HS in the code column and will be placed with 492434 and its quantity. Heat Sink 492435 will have code FX and zero quantity. On the card assembly B/M both Heat Sinks will be listed in the PL column as J and CH column as D.

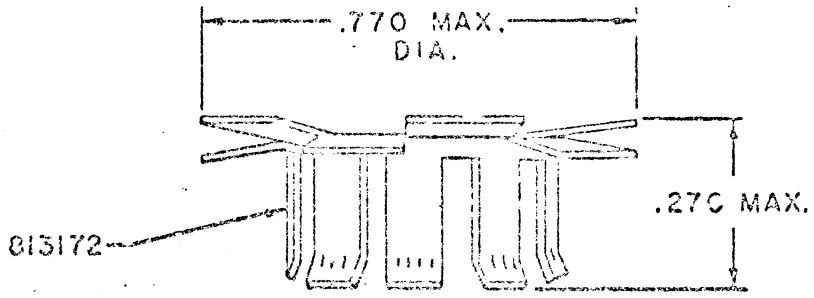


TOP VIEW

SIDE VIEW

813172 Heat Sink

Heat Sink 813172 non-insulated can be used on all physical outlines. Si grease must not be used with this Heat Sink. CMT size code is 8 x 8.



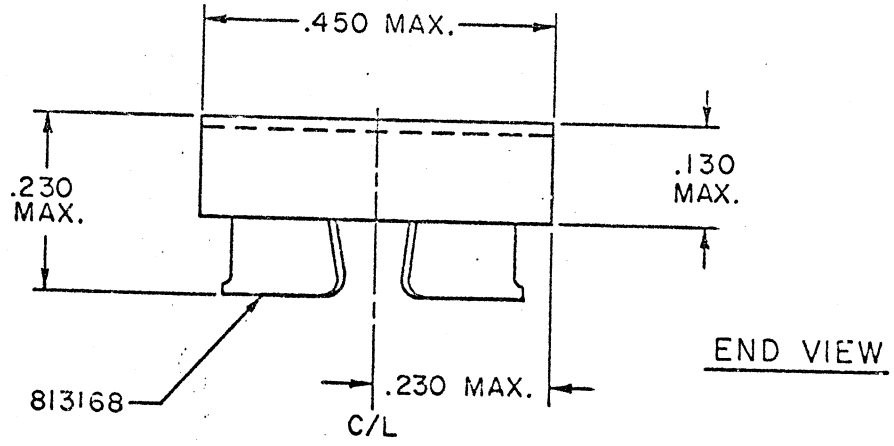
SIDE VIEW

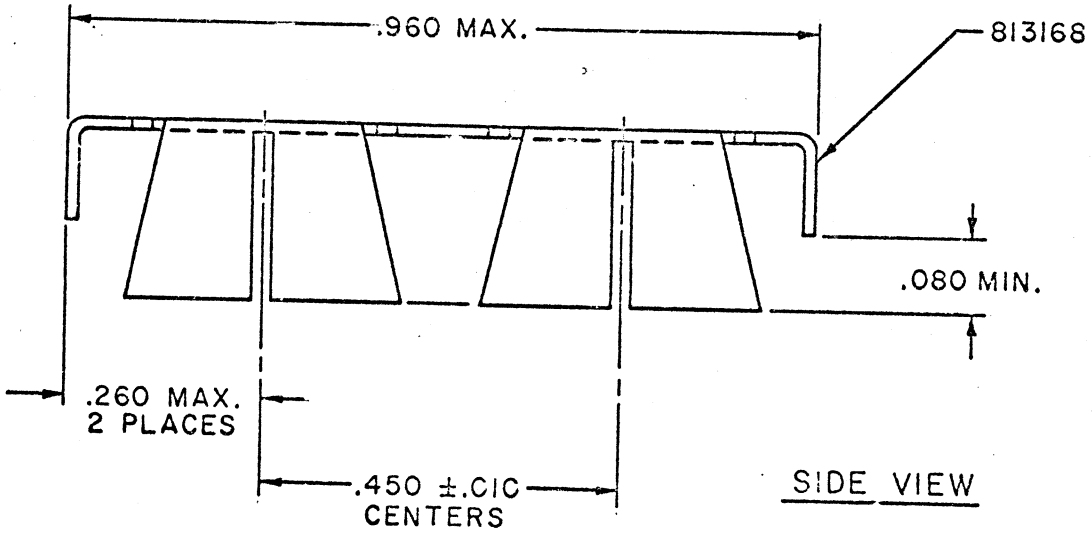
REQUIREMENTS (Continued)

HEAT SINKS

813168 Heat Sink

It is non-insulated and requires two transistors mounted on a random hole pattern.





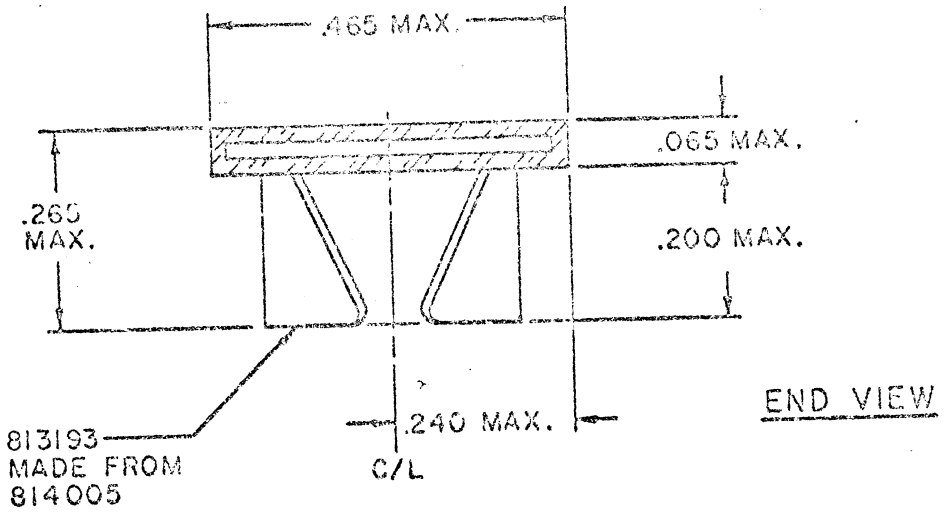
This Heat Sink can not be used on MST card assemblies because of the .450 center distance required for the mounting of the transistors.

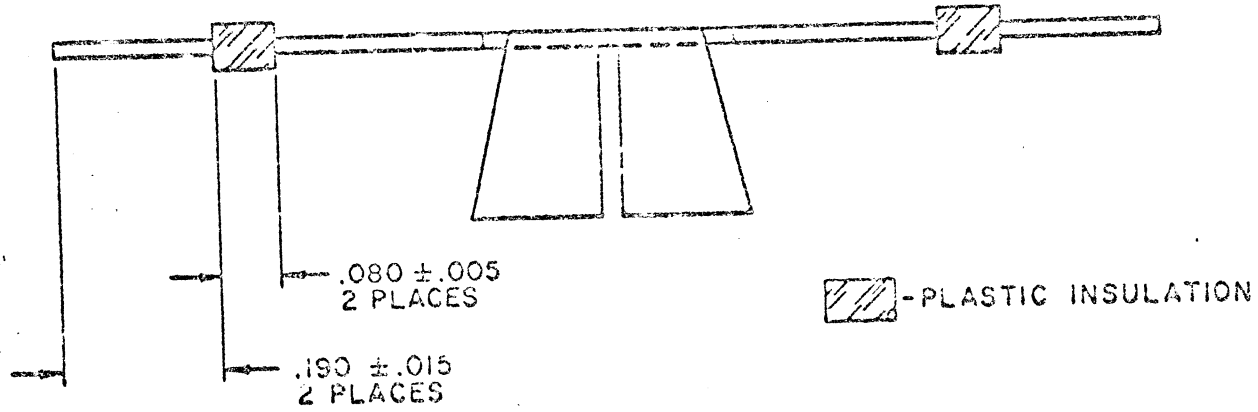
REQUIREMENTS (Continued)

HEAT SINKS

813193 Heat Sink

It is partially insulated so that its extending fins can be over non-insulated components. CMT size code is 12 x 4.



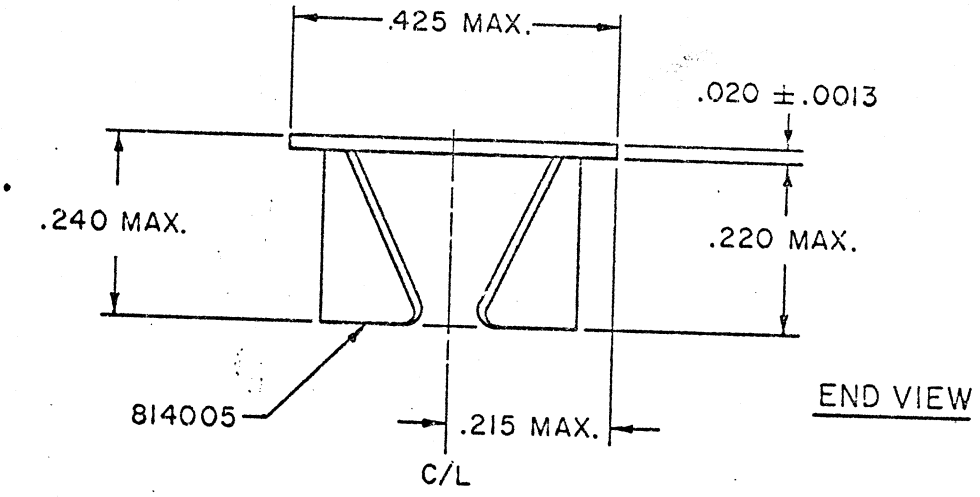


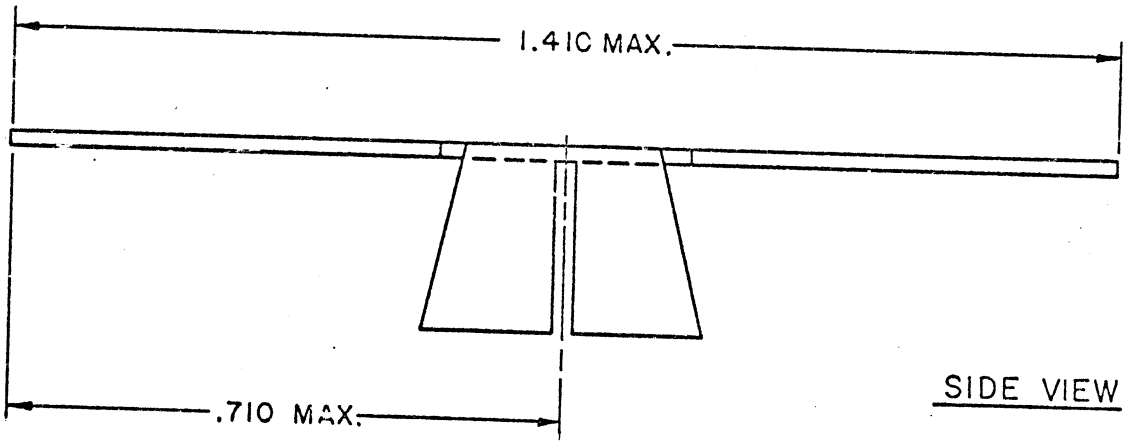
REQUIREMENTS (Continued)

HEAT SINKS

814005 Heat Sink

It is non-insulated with fins extending in opposite directions. CMT size code is 12 x 4.





HEAT SINK NOTE CODES

Si grease can not be used on Heat Sink 483376, 813172, 492434 and 492435. It is not recommended on 814005, 813193 and 813168 but when it is used, note code FK must be on the Heat Sink and HB on the package. When Si grease is not used, the Heat Sinks are classified as wettable and no note code is required on the Heat Sink (except FX on 492434 and 492435), but HB is required on the package.

LIMITS (PACKAGE ONLY)

To meet assembly requirements, leads must be on a .125 pattern within the following limits:

On a standard .125 pattern, TO-5 or TO-55 package leads will be placed on or within the following X and Y grids. Orientation tabs may be in any of the four quadrants.

SLT/SLD	1 Hi 6 and 12	X 28 - 73 - 143	Y 28 - 58
	2 Hi 6 and 12	X 28 - 73 - 143	Y 28 - 118
	3 Hi 12	X 28 - 143	Y 28 - 178
MST	2 Hi x 1,2 & 4 Wide	X 02 - 11 - 25 - 53	Y C - V
	3 Hi x 2 & 4 Wide	X 02 - 25 - 53	Y C - 8

Orientation tabs which do not project toward the card edge.

SLT/SLD	1 Hi 6 and 12	X 28 - 73 - 143	Y 28 - 58
	2 Hi 6 and 12	X 28 - 73 - 143	Y 28 - 118
	3 Hi 12	X 28 - 143	Y 28 - 178
MST	2 Hi x 1,2 & 4 Wide	X 02 - 11 - 25 - 53	Y C - V
	3 Hi x 2 & 4 Wide	X 02 - 25 - 53	Y C - 8

On a random pattern, TO-5 or TO-55 package leads will be placed on or within the following X and Y grids. Orientation tabs may be in any of the four quadrants.

SLT/SLD	1 Hi 6 and 12	X 27 - 74 - 144	Y 28 - 58
	2 Hi 6 and 12	X 27 - 74 - 144	Y 28 - 118
	3 Hi 12	X 27 - 144	Y 28 - 178

Orientation tabs which do not project toward the card edges.

SLT/SLD	1 Hi 6 and 12	X 25 - 77 - 147	Y 26 - 60
	2 Hi 6 and 12	X 25 - 77 - 147	Y 26 - 120
	3 Hi 12	X 25 - 147	Y 26 - 180

LIMITS (Continued)

HEAT SINKS

483376 Packages using Heat Sink 483376 must have their leads on or within the following X and Y grids.

SLT/SLD	1 Hi 6 and 12	X 34 - 67 - 137	Y 35 - 51
	2 Hi 6 and 12	X 34 - 67 - 137	Y 35 - 111
	3 Hi 12	X 34 - 137	Y 35 - 171
MST	2 Hi x 1,2 & 4 Wide	X 04 - 09 - 23 - 51	Y D - T
	3 Hi x 2 & 4 Wide	X 04 - 23 - 51	Y D - 6

813172 Packages using Heat Sink 813172 must have their leads on or within the following X and Y grids.

SLT/SLD	1 Hi 6 and 12	X 33 - 68 - 138	Y 33 - 52
	2 Hi 6 and 12	X 33 - 68 - 138	Y 33 - 112
	3 Hi 12	X 33 - 138	Y 33 - 172
MST	2 Hi x 1,2 & 4 Wide	X 03 - 10 - 24 - 52	Y C - U
	3 Hi x 2 & 4 Wide	X 03 - 24 - 52	Y C - 7

492434 and 492435
Packages using these Heat Sinks must have their leads on or within the following X and Y grids.

SLT/SLD	1 Hi 6 and 12	X 29 - 72 - 142	Y 29 - 56
	2 Hi 6 and 12	X 29 - 72 - 142	Y 29 - 116
	3 Hi 12	X 29 - 142	Y 29 - 176
MST	2 Hi x 1,2 & 4 Wide	X 03 - 10 - 24 - 52	Y C - U
	3 Hi x 2 & 4 Wide	X 03 - 24 - 52	Y C - 7

813168 Packages using Heat Sink 813168 must have their leads on or within the following X and Y grids. The Heat Sinks may be parallel with X or Y axis.

SLT/SLD	1 Hi 6 and 12	X 28 - 73 - 143	Y 28 - 57
	2 Hi 6 and 12	X 28 - 73 - 143	Y 28 - 117
	3 Hi 12	X 28 - 143	Y 28 - 177

LIMITS (Continued)

HEAT SINKS

814005 Packages using Heat Sink 814005 mounted parallel to the Y axis and card housing must have their leads on or within the following X and Y grids.

SLT/SLD	1 Hi 6 and 12	X 46 - 55 - 125	Y 27 - 59
	2 Hi 6 and 12	X 46 - 55 - 125	Y 27 - 119
	3 Hi 12	X 46 - 125	Y 27 - 179
MST	2 Hi x 1,2 & 4 Wide	X 06 - 07 - 21 - 49	Y C - V
	3 Hi x 2 & 4 Wide	X 06 - 21 - 49	Y C - 8

Packages using Heat Sink 814005 mounted parallel to the X axis must have their leads on or within the following X and Y grids.

SLT/SLD	1 Hi 6 and 12	X 26 - 75 - 145	Y 47 - 39
	2 Hi 6 and 12	X 26 - 75 - 145	Y 47 - 99
	3 Hi 12	X 26 - 145	Y 47 - 159
MST	2 Hi x 1,2 & 4 Wide	X 02 - 11 - 25 - 53	Y F - R
	3 Hi x 2 & 4 Wide	X 02 - 25 - 53	Y F - 4

813193 Packages using Heat Sink 813193 mounted parallel to the Y axis and card housing must have their leads on or within the following X and Y grids.

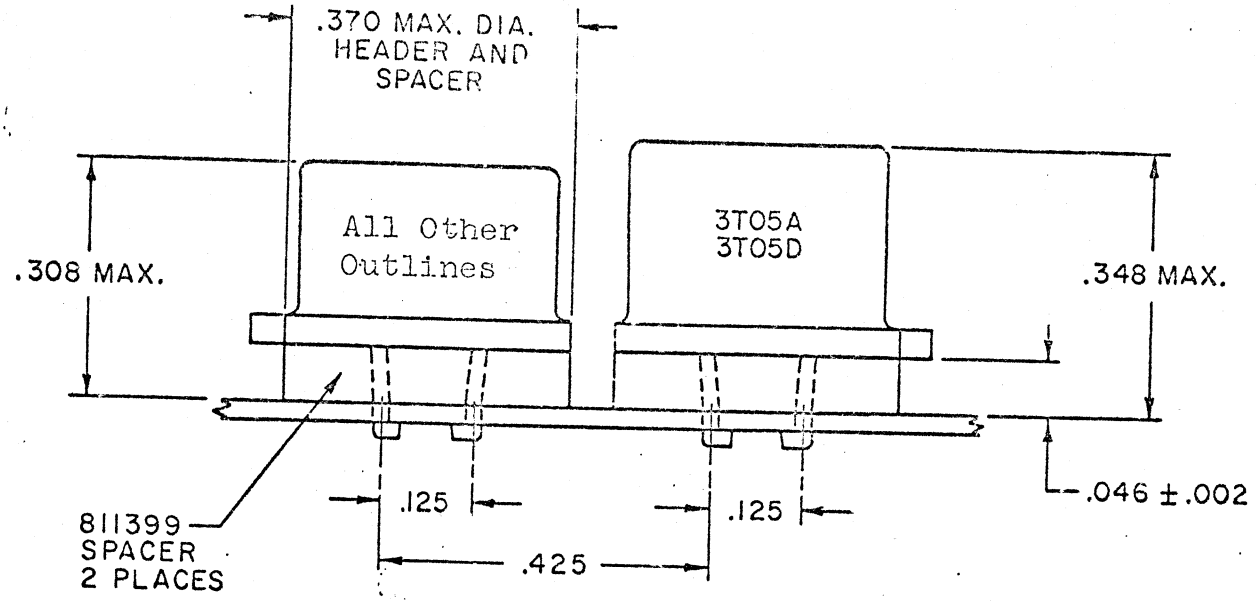
SLT/SLD	1 Hi 6 and 12	X 46 - 55 - 125	Y 28 - 58
	2 Hi 6 and 12	X 46 - 55 - 125	Y 28 - 118
	3 Hi 12	X 46 - 125	Y 28 - 178
MST	2 Hi x 1,2 & 4 Wide	X 06 - 07 - 21 - 49	Y C - V
	3 Hi x 2 & 4 Wide	X 06 - 21 - 49	Y C - 8

Packages using Heat Sink 813193 mounted parallel to the X axis must have their leads on or within the following X and Y grids.

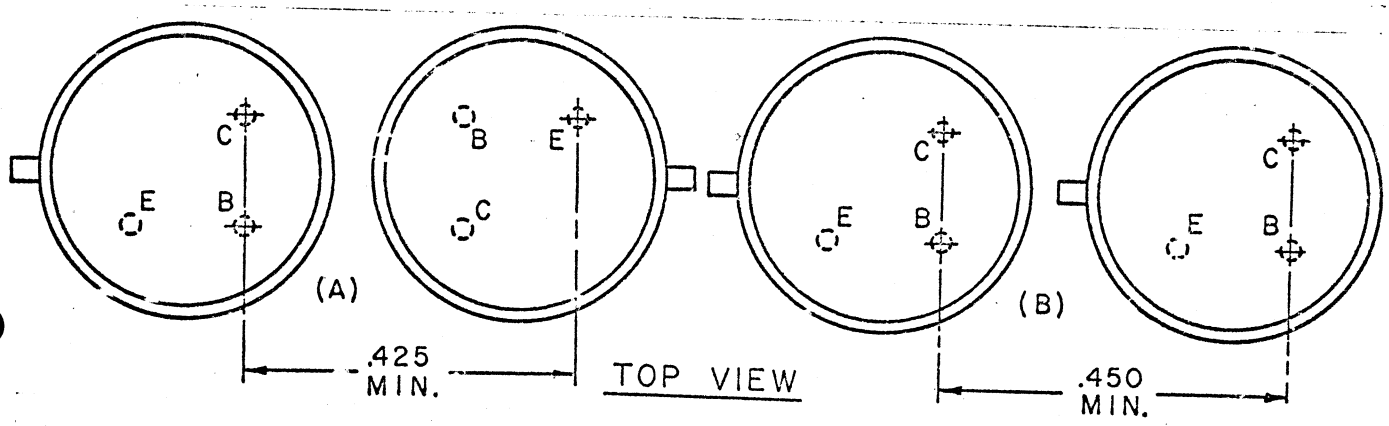
SLT/SLD	1 Hi 6 and 12	X 27 - 74 - 144	Y 47 - 39
	2 Hi 6 and 12	X 27 - 74 - 144	Y 47 - 99
	3 Hi 12	X 27 - 144	Y 47 - 159
MST	2 Hi x 1,2 & 4 Wide	X 02 - 11 - 25 - 53	Y F - R
	3 Hi x 2 & 4 Wide	X 02 - 25 - 53	Y F - 4

RELATIONSHIPS

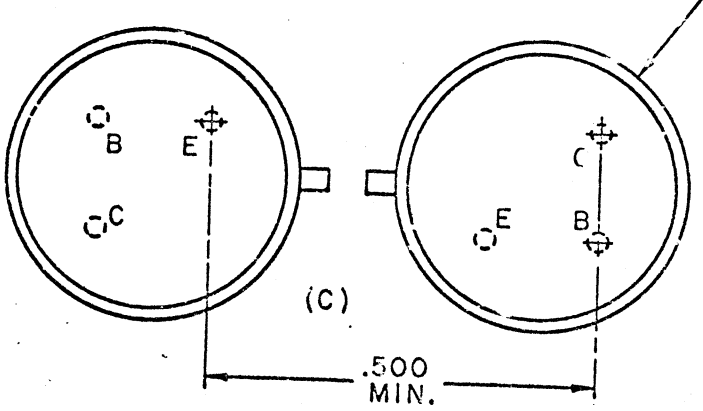
The following illustration shows the physical minimum placement of TO-5 and TO-55 packages as shown with their spacers.



SIDE VIEW



TOP VIEW



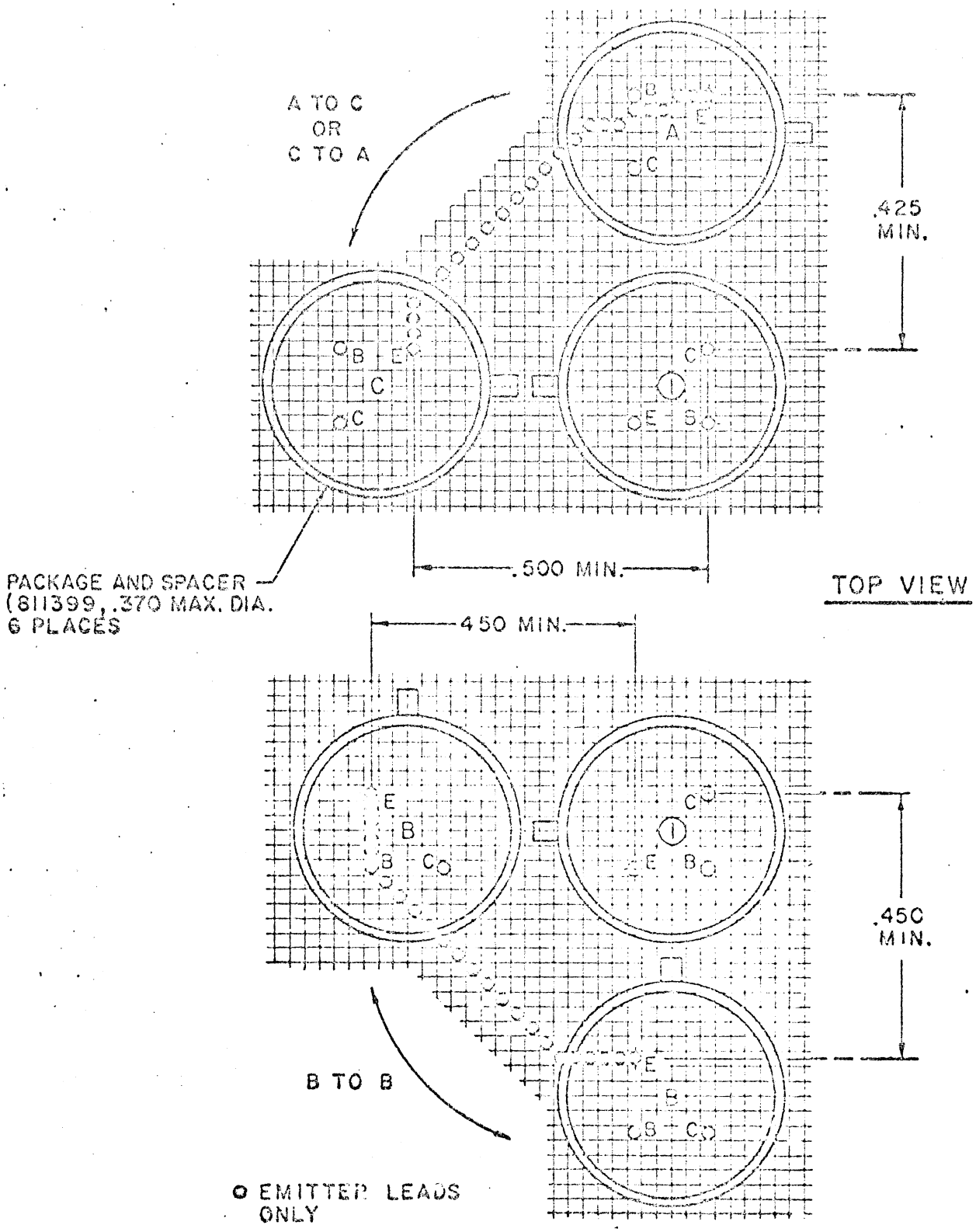
PACKAGE AND
SPACER (811399)
6 PLACES

TO-5 and TO-55 packages must be mounted on the following minimum center to center distances.

(A) Non-adjacent tabs .425
(B) One adjacent tab .450
(C) Two adjacent tabs .500

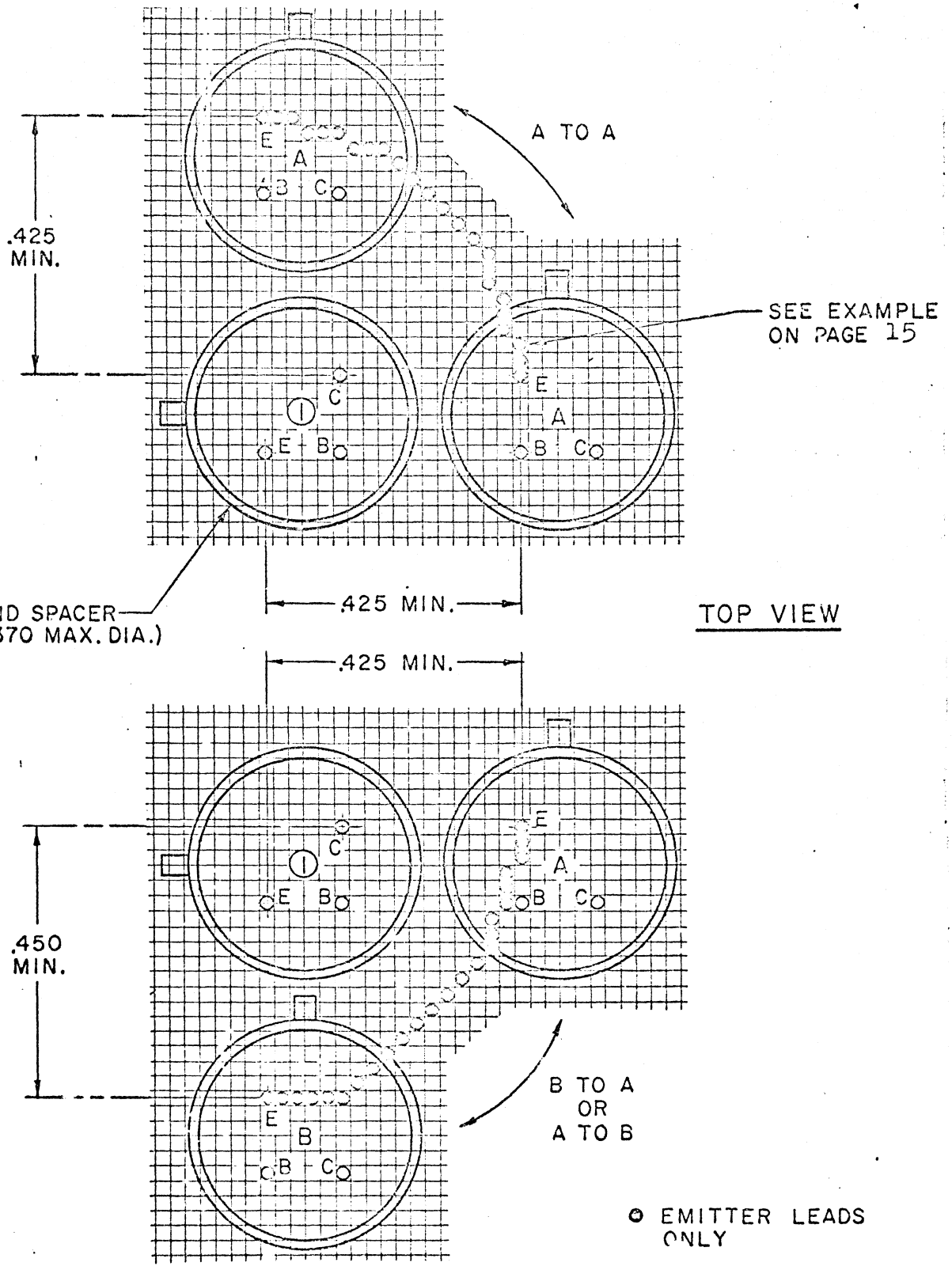
RELATIONSHIPS (CONTINUED)

The following illustrations can be used to determine the actual minimum grid placement of the package leads.



TRANSISTORS TO-5 and TO-55

RELATIONSHIPS (CONTINUED)



RELATIONSHIPS (CONTINUED)

In this illustration, package number (1) is fixed. The other package maintains the same orientation with respect to the card edges and moves about package number (1). Within each segment of this illustration there are portrayed only two packages. The moving package is shown twice, when it is positioned on the same X and Y grids as the fixed package. In these two positions, the moving package has either an A, B, or C on it. This letter indicates the condition existing between the moving and the fixed package. A indicates that a condition of non-adjacent tabs exists. B indicates that a condition of one-adjacent tab exists and C indicates that a condition of two-adjacent tabs exist. REMEMBER: The orientation of the moving package is always the same with respect to the card edges. The lead location for the moving package is given for one lead only. This is sufficient for specifying the minimum mounting of one package to the other. Although the relationship between both packages is shown for only a 90 degree swing of the moving package, the lead locations given must be extrapolated when working in the other 270 degrees around the fixed package.

The procedure to be followed for applying this illustration is outlined below:

a. Placement of TO-5 and TO-55 packages is not complex when both packages are located on the same X and/or same Y grid. Hence, this procedure should be used only when two packages are placed in a staggered manner.

b. Designate one of the transistors, which is on a multi-color or assembly drawing, as the fixed package as portrayed in the above illustration (1).

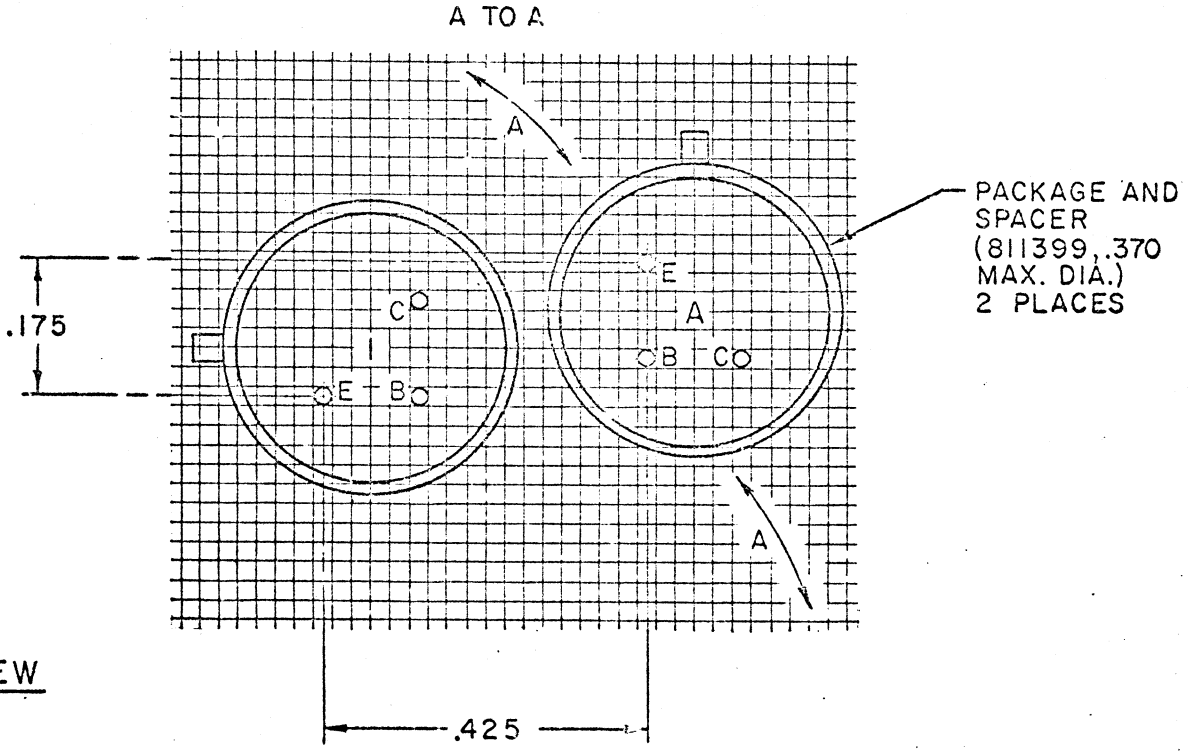
c. Translate the other package maintaining its orientation with respect to the card edges from its staggered position both ways until it is on the same X and same Y grid as the fixed package.

d. Label the translated package in both positions with an A, B, or C.

e. The combination of these two letters indicates which segment of the illustration above to refer to for the lead grid spacing which corresponds to the minimum spacing of the two packages.

RELATIONSHIPS (CONTINUED)

The following illustration is an example of how to use the previous illustration.



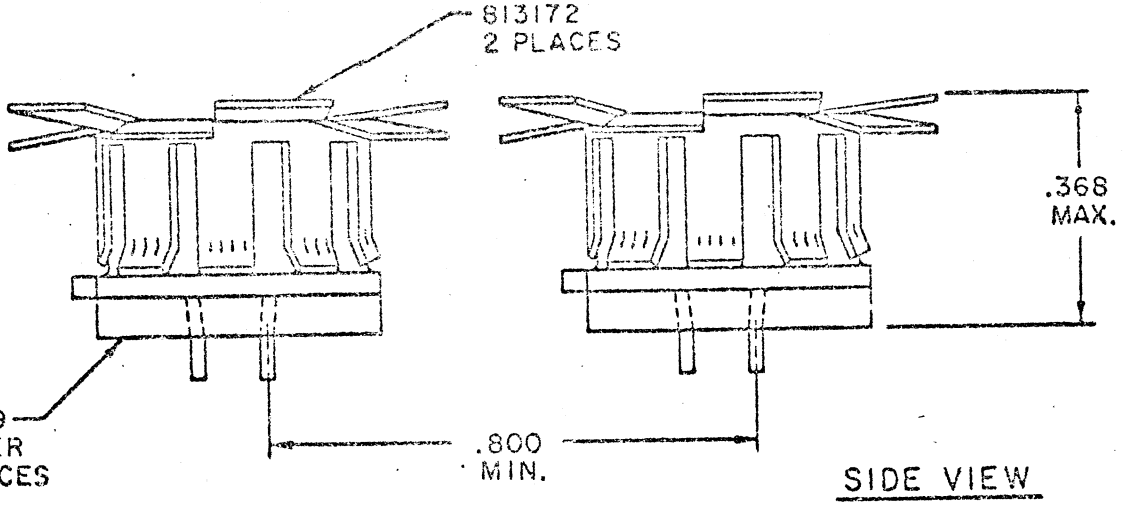
TOP VIEW

RELATIONSHIPS (CONTINUED)

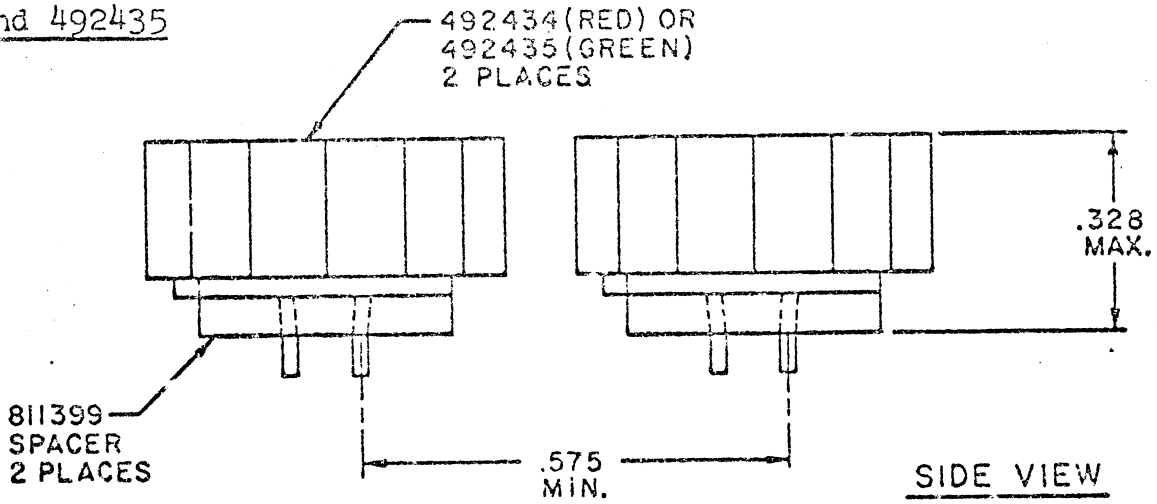
HEAT SINKS

The following illustrations show the physical minimum placement of TO-5 and TO-55 packages with like Heat Sinks.

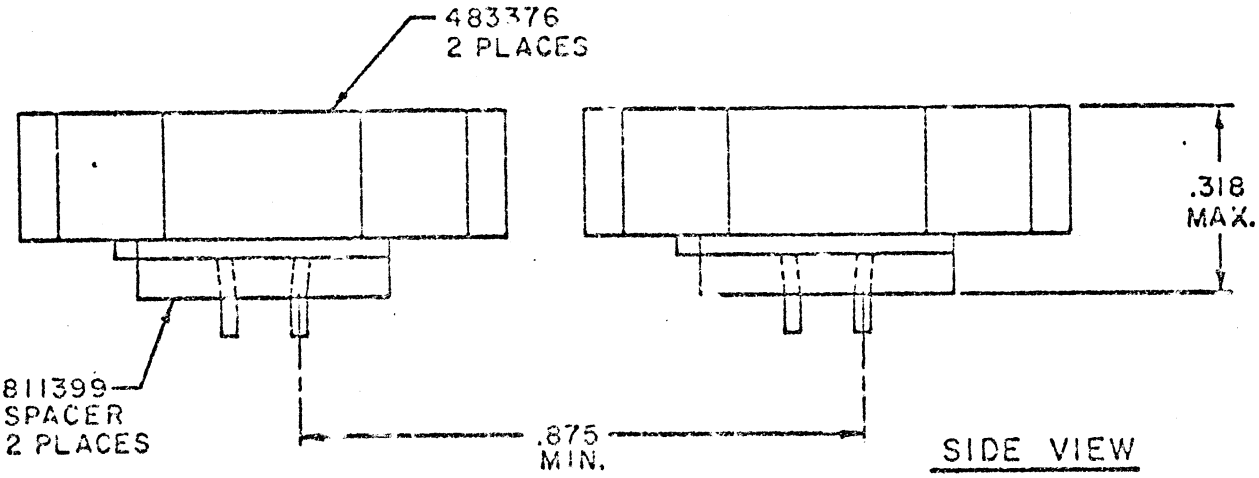
813172



492434 and 492435



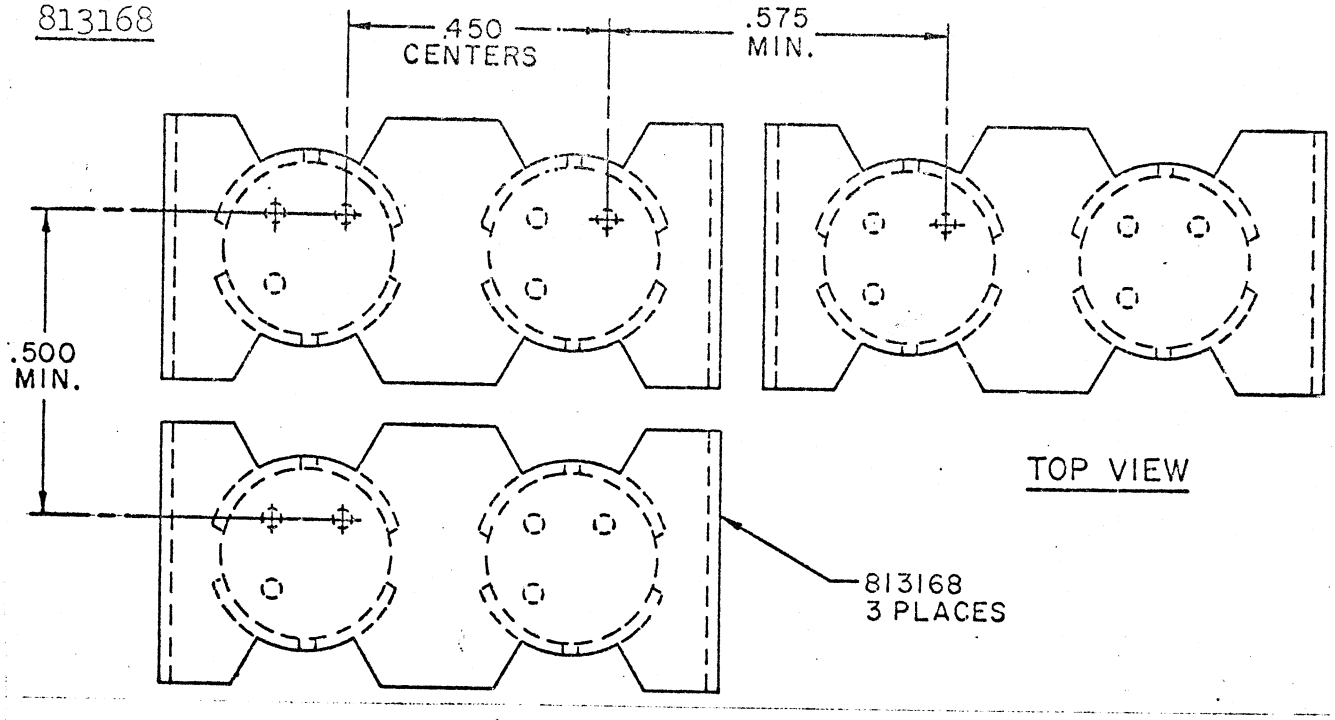
483376



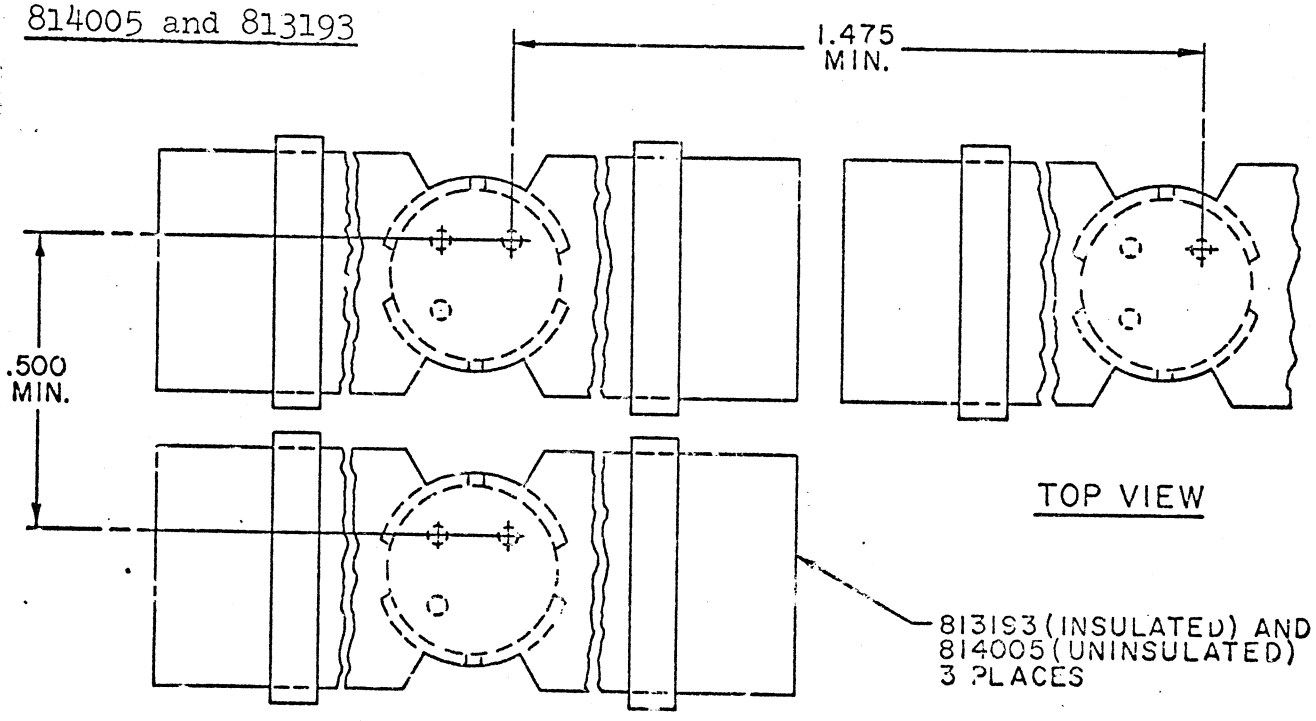
RELATIONSHIPS (CONTINUED)

HEAT SINKS

813168



814005 and 813193

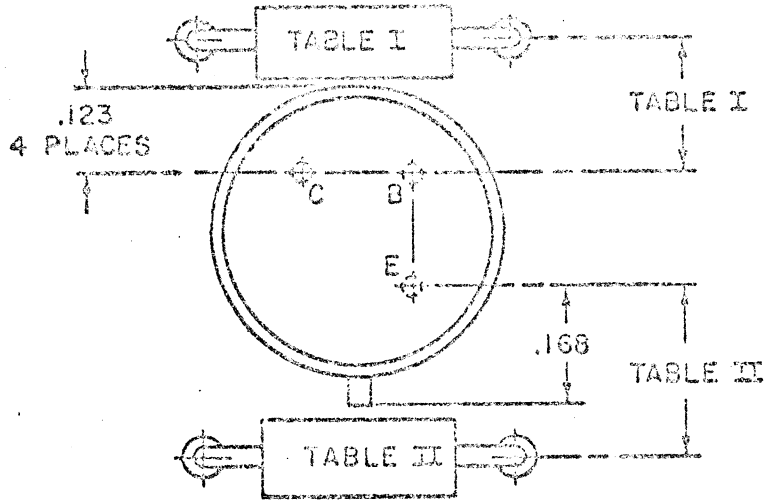


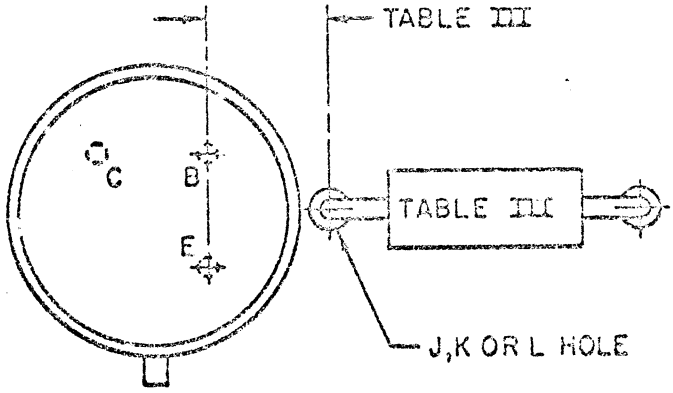
ARTWORKS

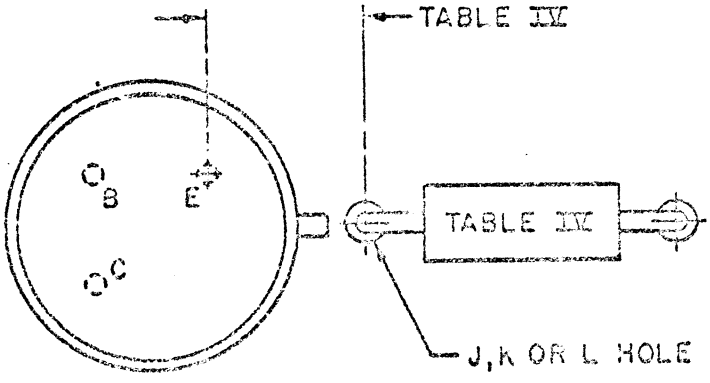
There are no artwork restrictions associated with the usage of this component package.

SEQUENCE EFFECT

The following illustration shows TO-5 and TO-55 with tubular axial-leaded minimum mounting placement.







TOP VIEW

TABLE I	
HOLE SPACING MIN.	MAX. BODY DIAMETER
.175	.100
.200	.150
.225	.200
.250	.250
.275	.300
.300	.350

TABLE II	
HOLE SPACING MIN.	MAX. BODY DIAMETER
.225	.110
.250	.160
.275	.210
.300	.260
.325	.310
.350	.360

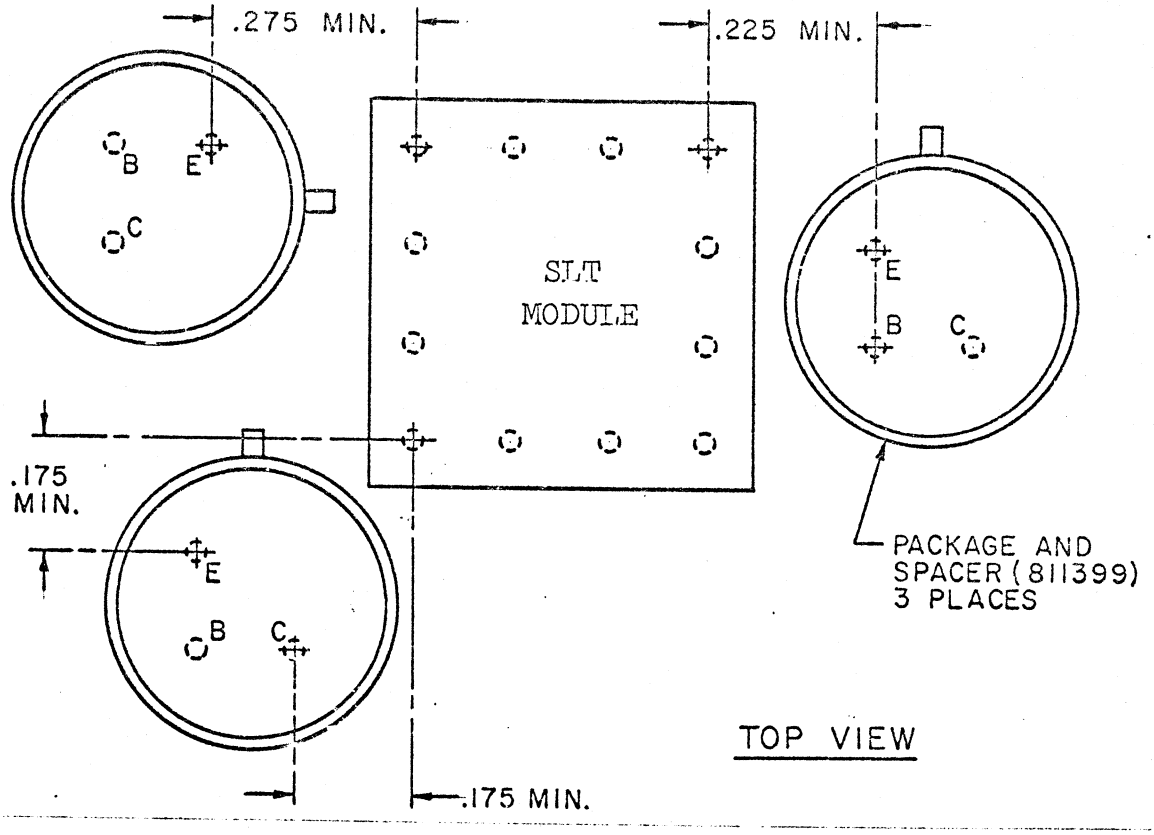
TABLE III	
HOLE SPACING MIN.	MAX. BODY DIAMETER
.175	.370

TABLE IV	
HOLE SPACING MIN.	MAX. BODY DIAMETER
.225	.370

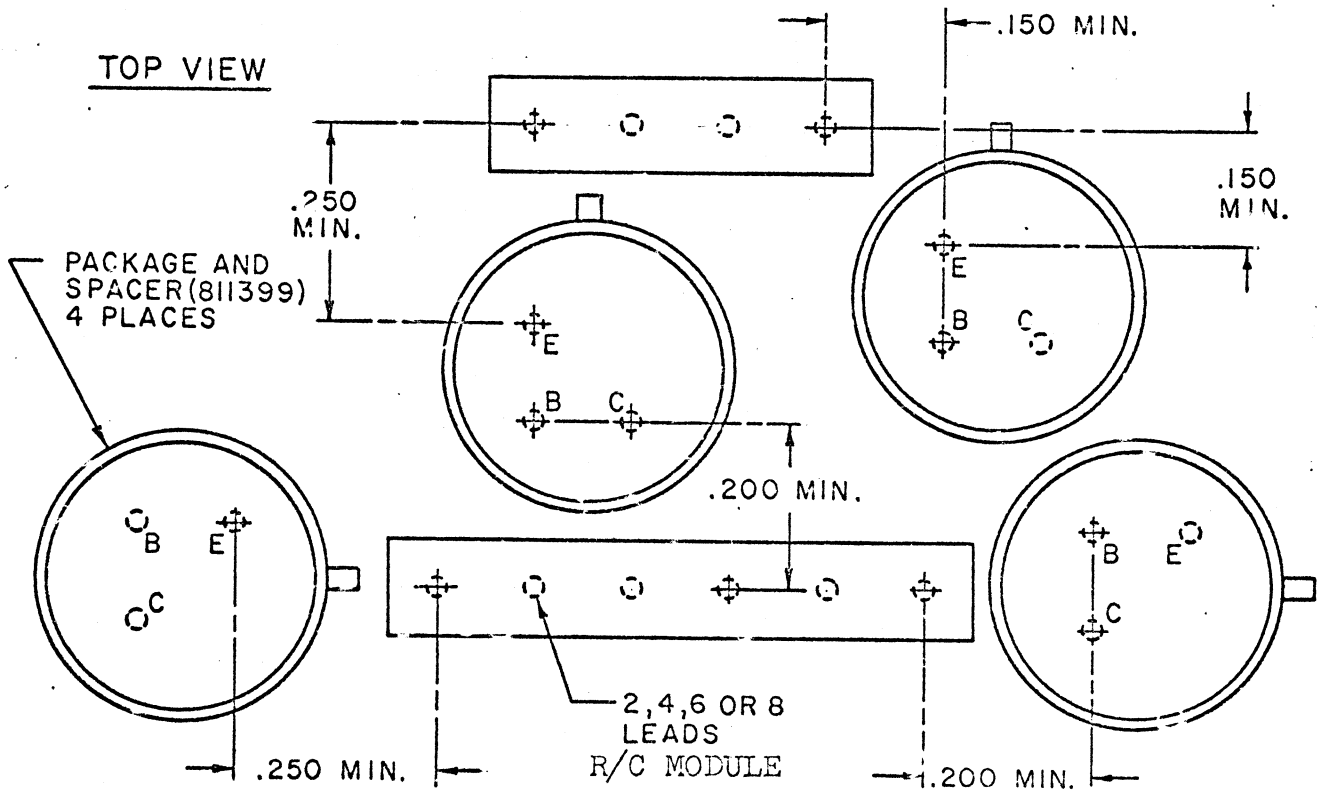
TRANSISTORS TO-5 and TO-55

SEQUENCE EFFECT (CONTINUED)

The following illustrations show TO-5 and TO-55 packages and SLT and R/C module minimum placement.

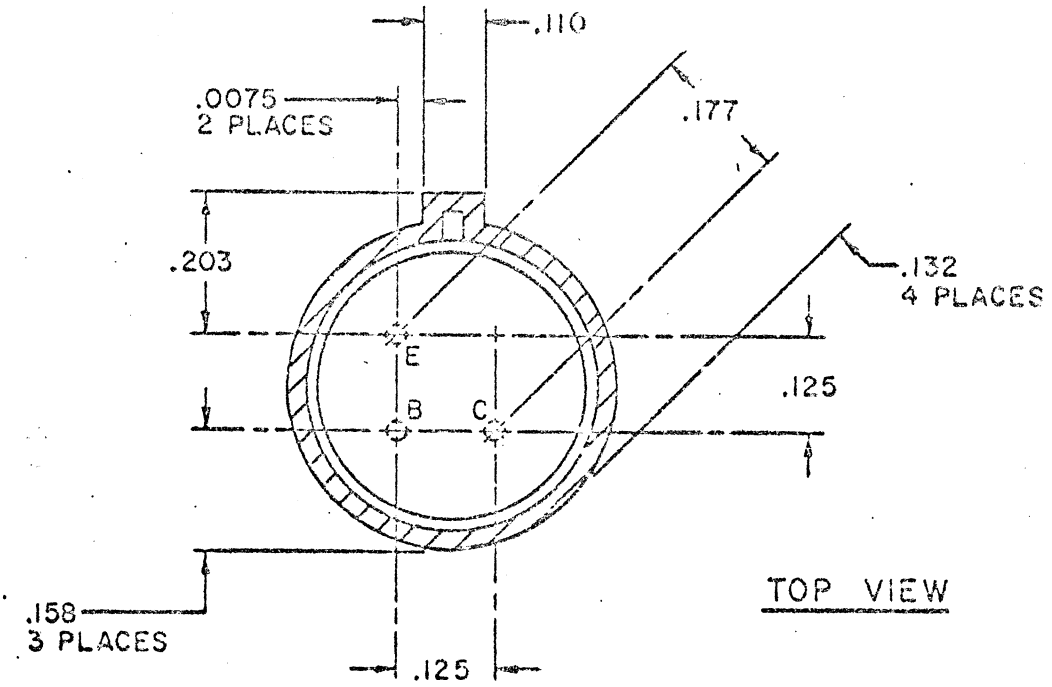


TOP VIEW



SEQUENCE EFFECT (CONTINUED)

The following illustration shows the TO-5 and TO-55 restricted area for all other adjacent components.



▨ – RESTRICTED AREA FOR UNINSULATED COMPONENTS.

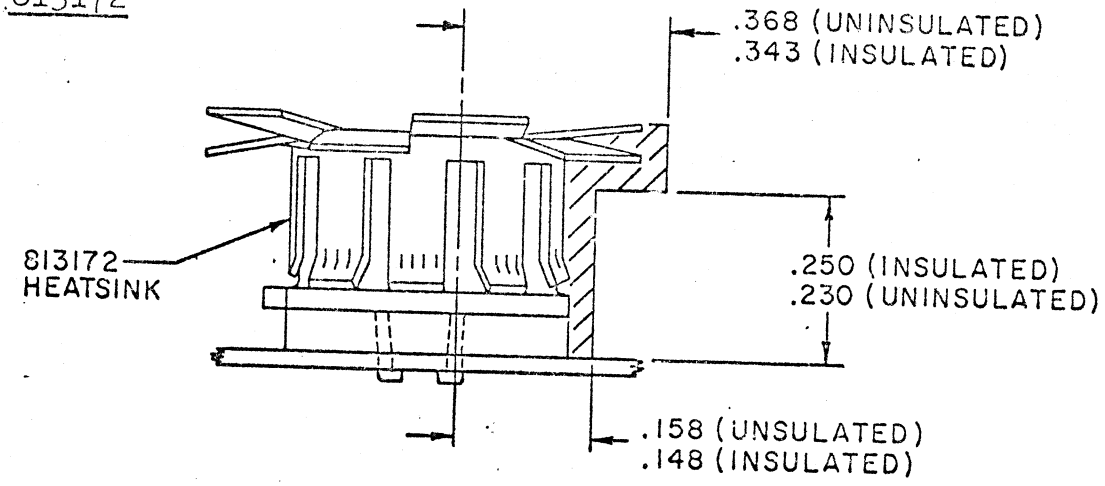
TRANSISTORS TO-5 and TO-55

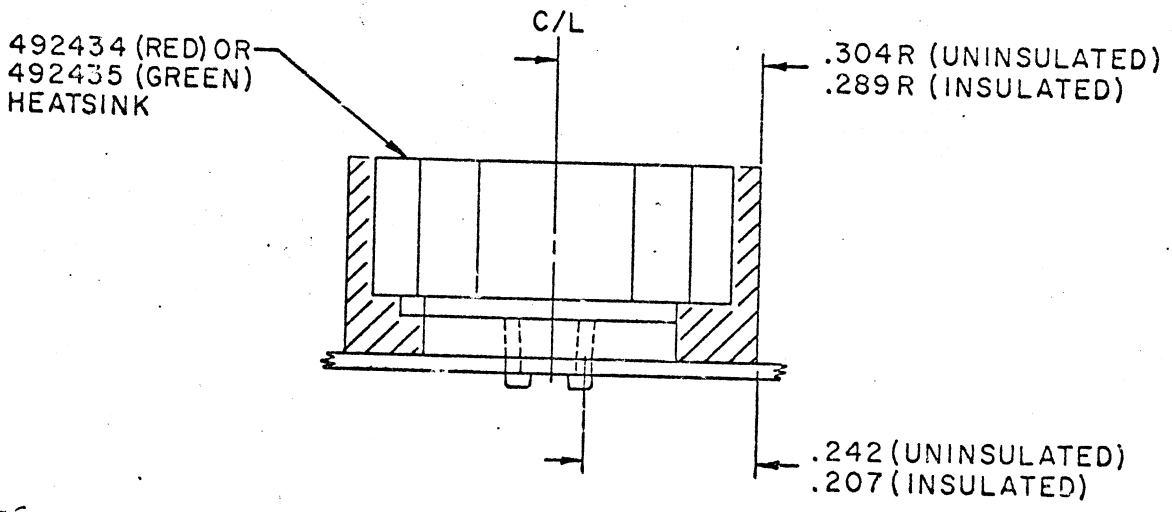
SEQUENCE EFFECT (CONTINUED)

HEAT SINKS

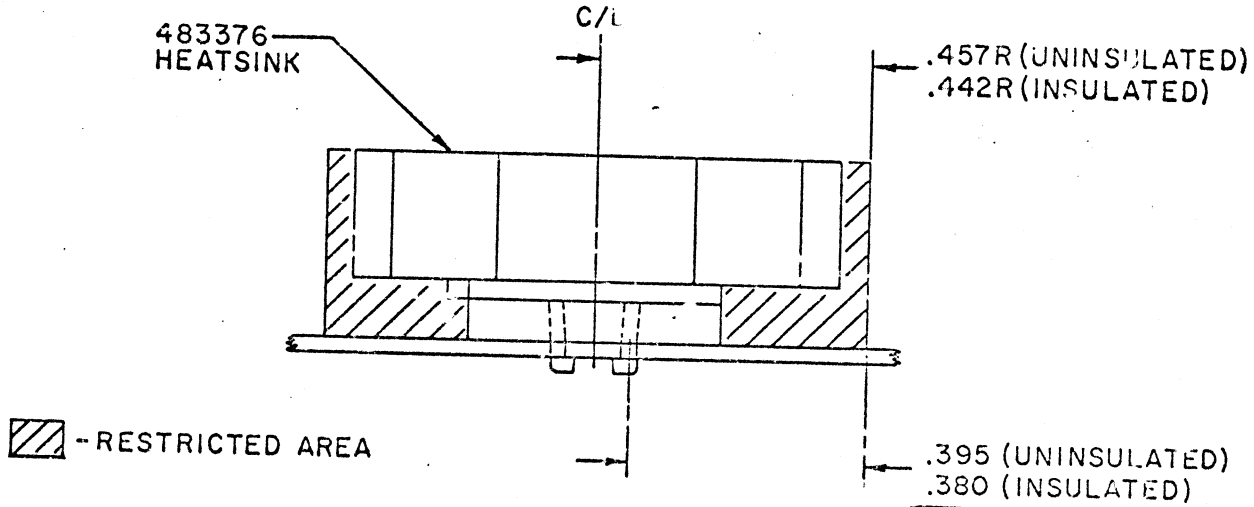
The following illustrations show TO-5 and TO-55 packages with Heat Sinks and adjacent components.

813172





483376

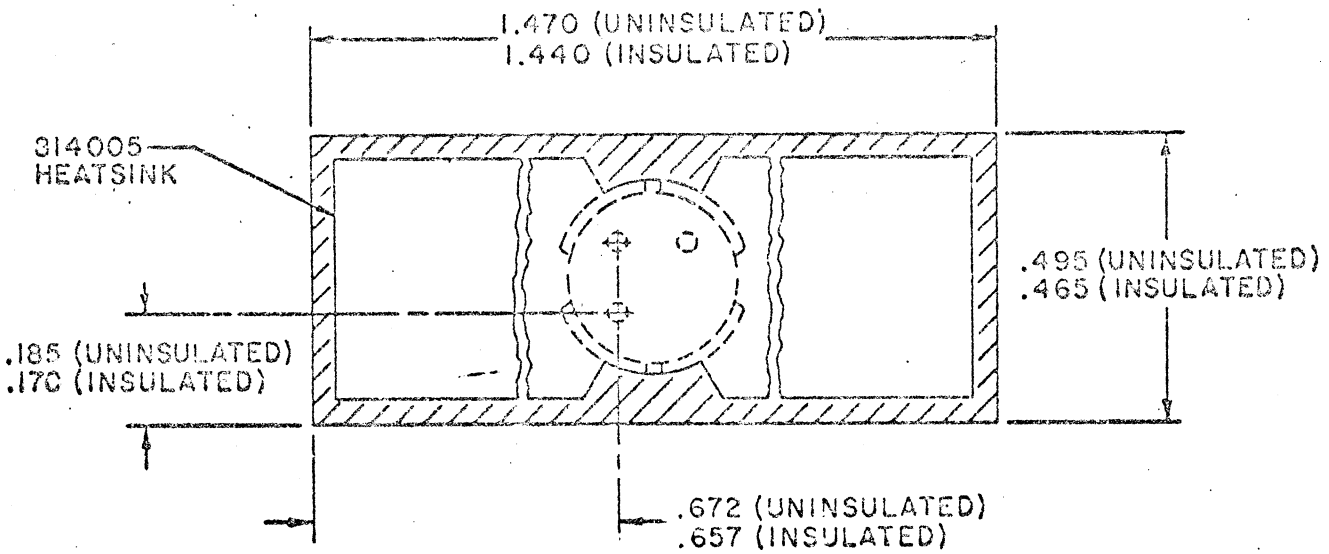


SIDE VIEWS

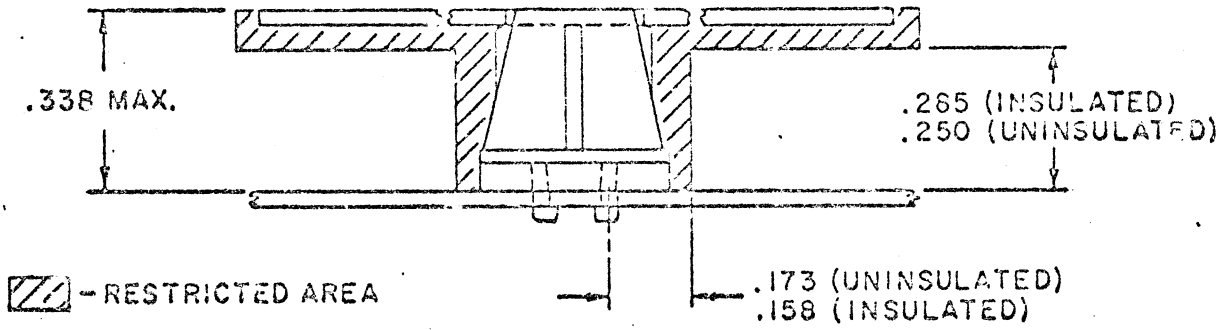
SEQUENCE EFFECT (CONTINUED)

HEAT SINK

814005



TOP VIEW

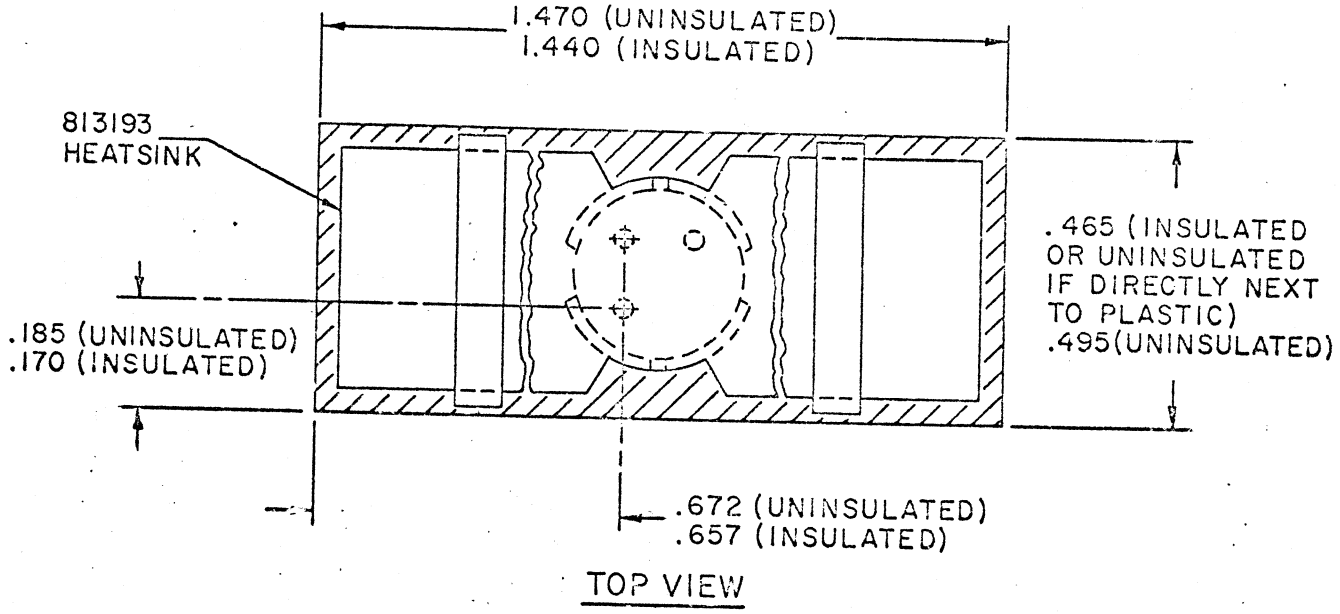


SIDE VIEW

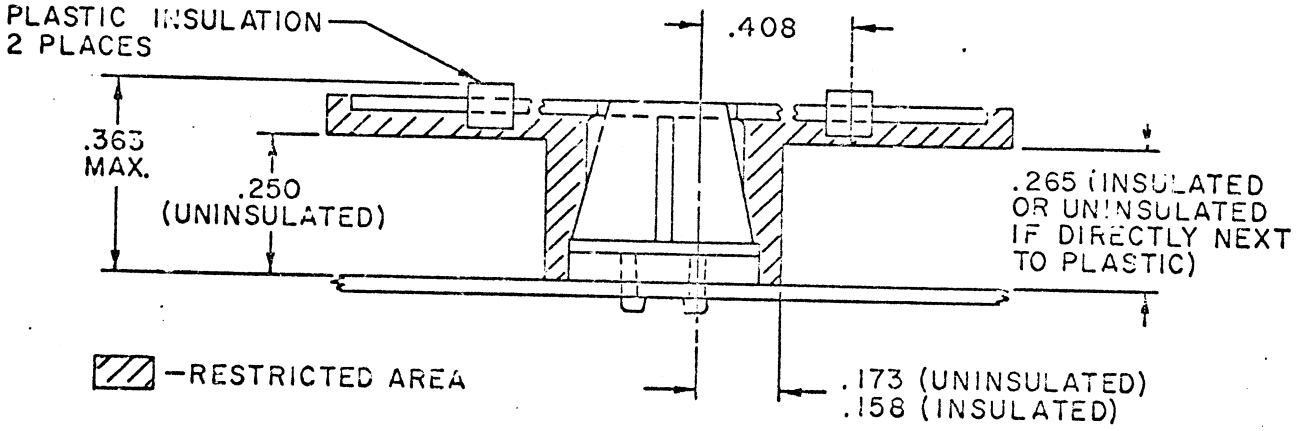
SEQUENCE EFFECT (CONTINUED)

HEAT SINKS

813193



TOP VIEW

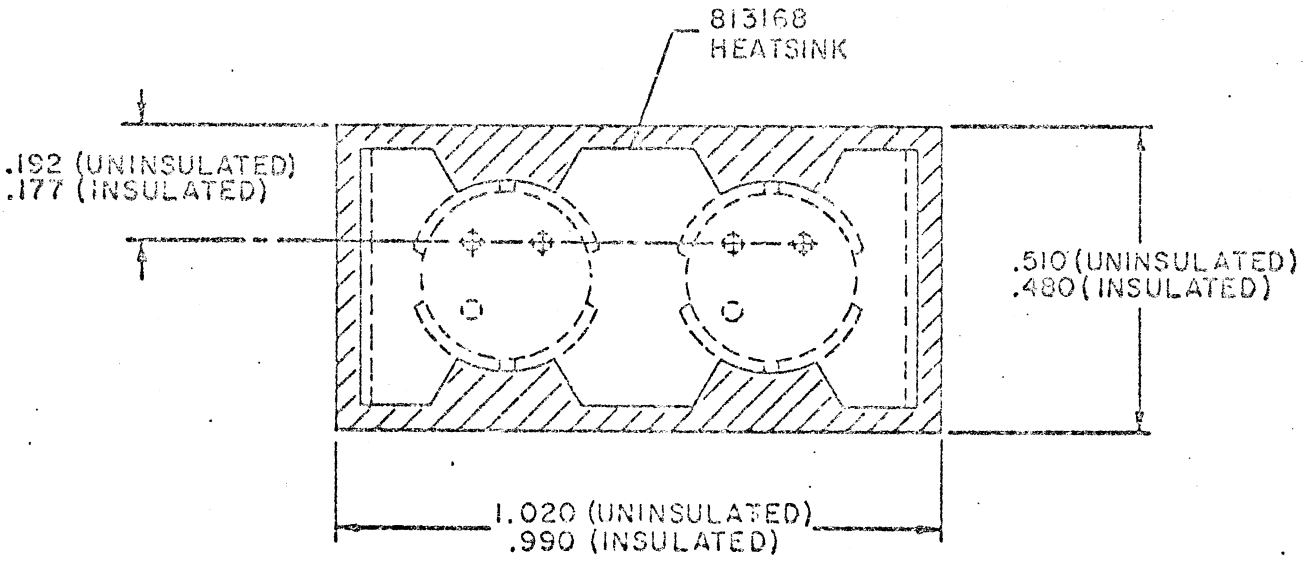


SIDE VIEW

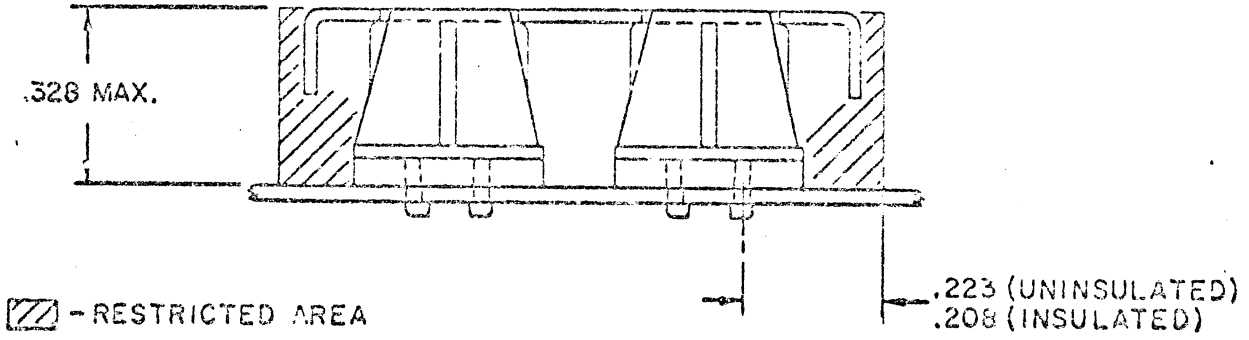
SEQUENCE EFFECT (CONTINUED)

HEAT SINKS

813168



TOP VIEW



SIDE VIEW

HAND ASSEMBLY

All TO-5 and TO-55 packages will be hand assembled if their leads are not on the standard grids ending with digit 3 or 8, or equivalent.

PROCESS INFORMATION

The assembly machines require the TO-5 and TO-55 leads to be on the standard grid pattern that end with digit 3 or 8, or equivalent.

All packages will have their leads cut prior to assembly.

The lead will be gang-clinched to the card after all other components less than .348 high are assembled.

The use of Si grease should be avoided whenever possible.

No package may have more than one spacer. Any new spacers must be released by Department 307.

PLANNING

Semi-automatic equipment for leads not mounted on the standard pattern is not contemplated.

A TO-5 and TO-55 Heat Sink that is similar to TO-56 Heat Sink 815184 can be released if desired. This type of Heat Sink has advantages over other TO-5 and TO-55 press-on designs. Contact Department 307, Endicott for release.

TO-5 - TO-55 TRANSISTOR HEATSINK ASSEMBLIES

DESCRIPTION

Listed below are the Heatsink Assemblies, and related reference drawings, for TO-5 - TO-55 Transistors recommended for SLT usage:

Number of Transistors	Heatsink	Reference Drawing
1	813166	816011
2	813173	816008
4	813160	816009
8	813163	816010

Assembly Drawing Code is "HS" for the Heatsinks and "Q" for the Transistors.

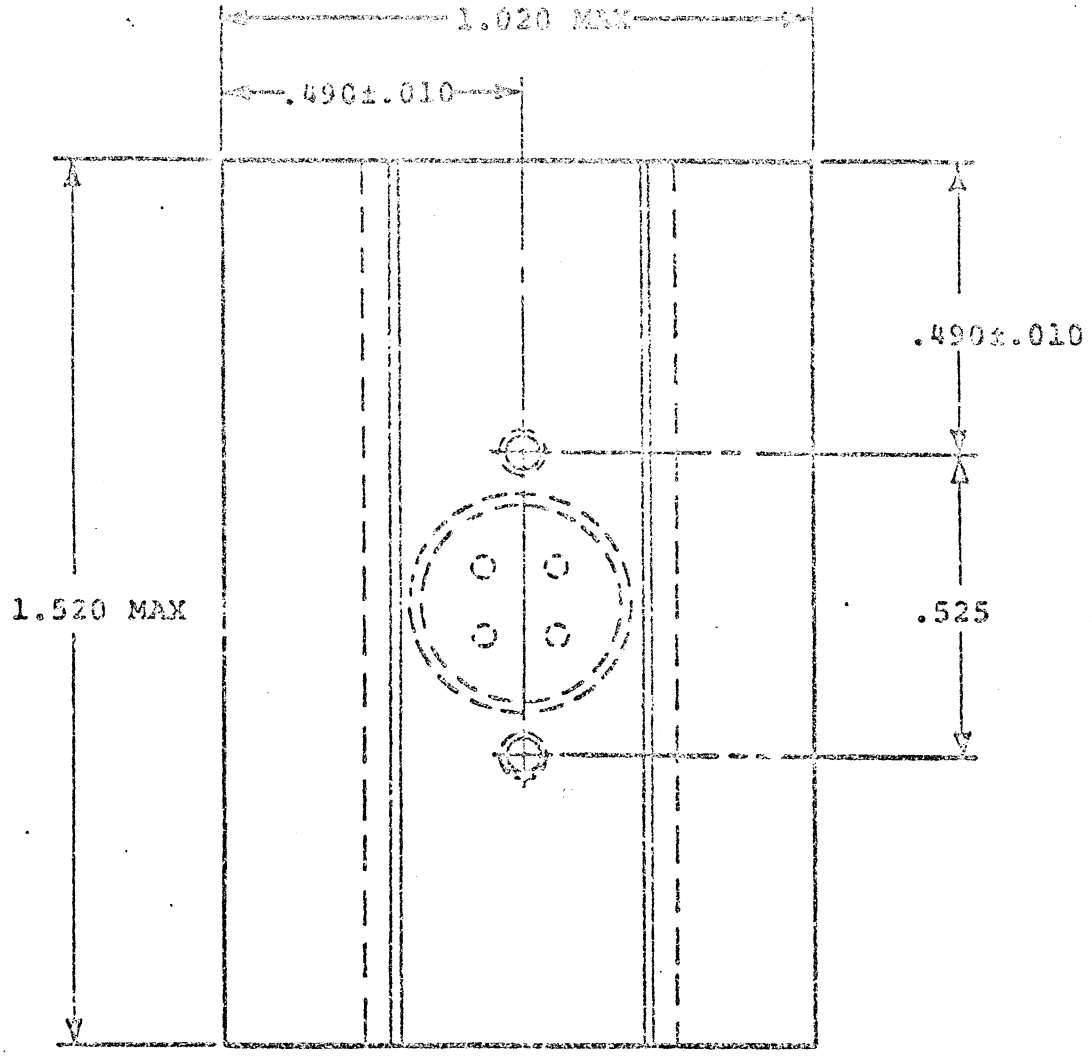
PACKAGE

The following illustrations show the TO-5 - TO-55 Heatsink Assemblies and related hardware.

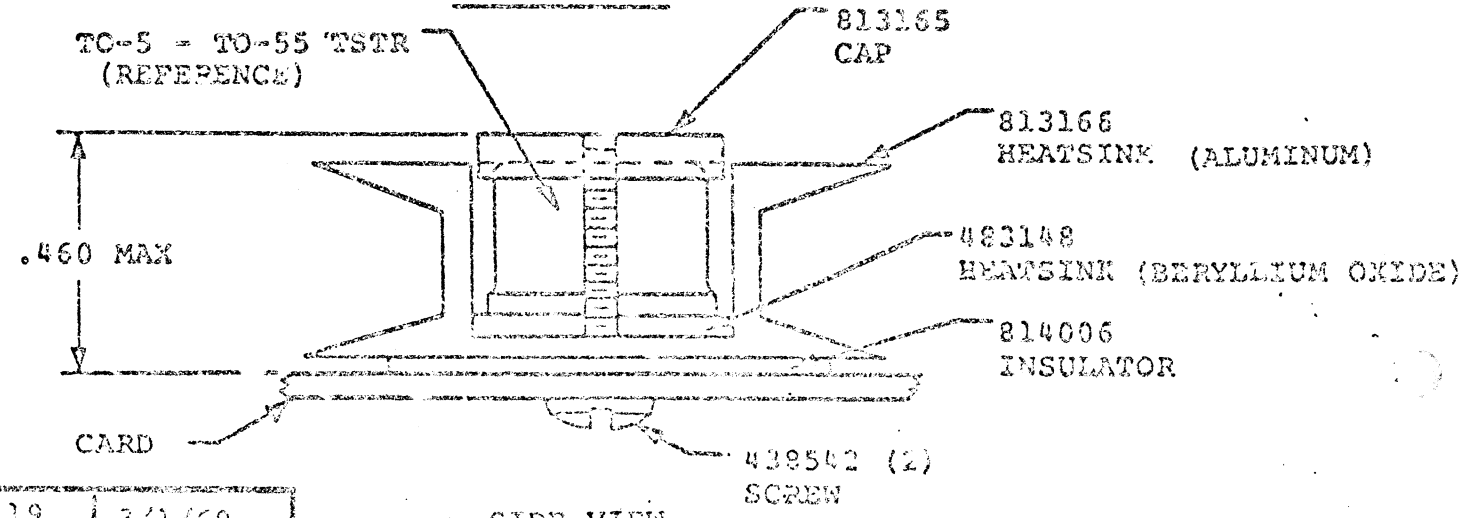
The views shown for the following Heatsink Assemblies are for layout purposes only, part drawings and reference drawings shall have precedence.

PACKAGE (Cont'd)

HEATSINK 813166 - for 1 TRANSISTOR



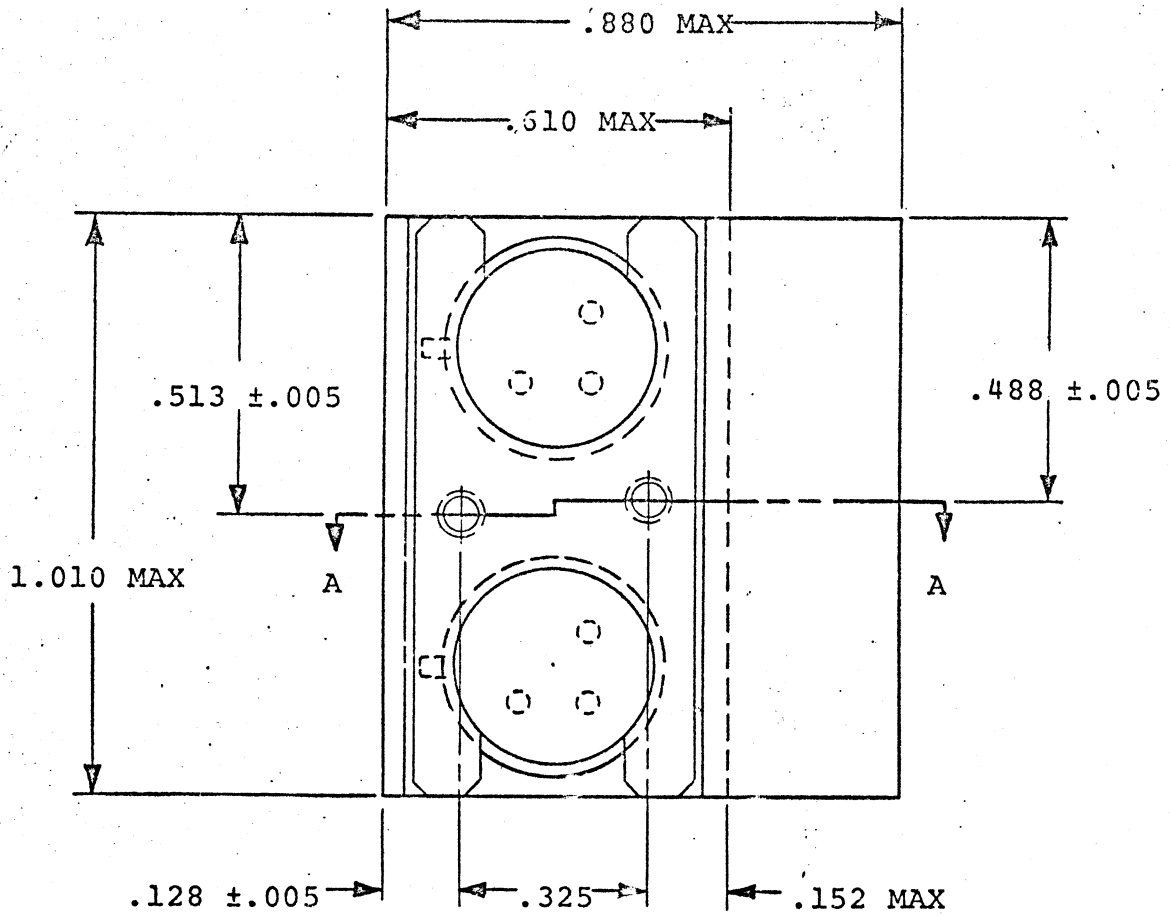
TOP VIEW



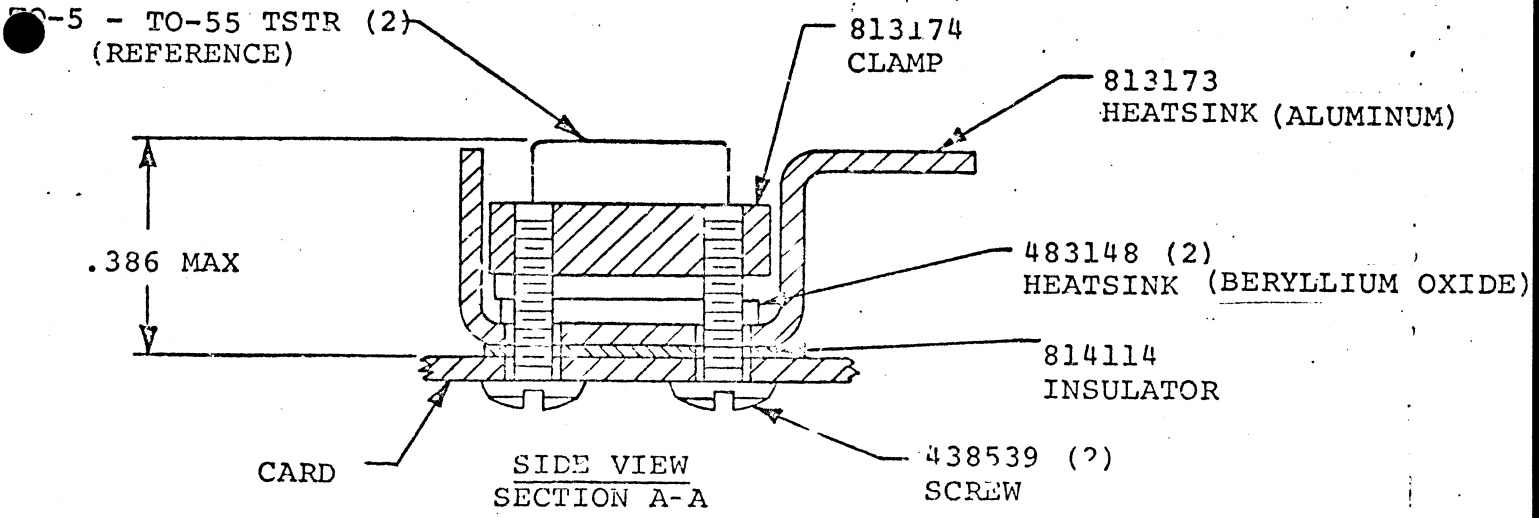
SIDE VIEW

PACKAGE (Cont'd)

HEATSINK 813173 - for 2 TRANSISTORS



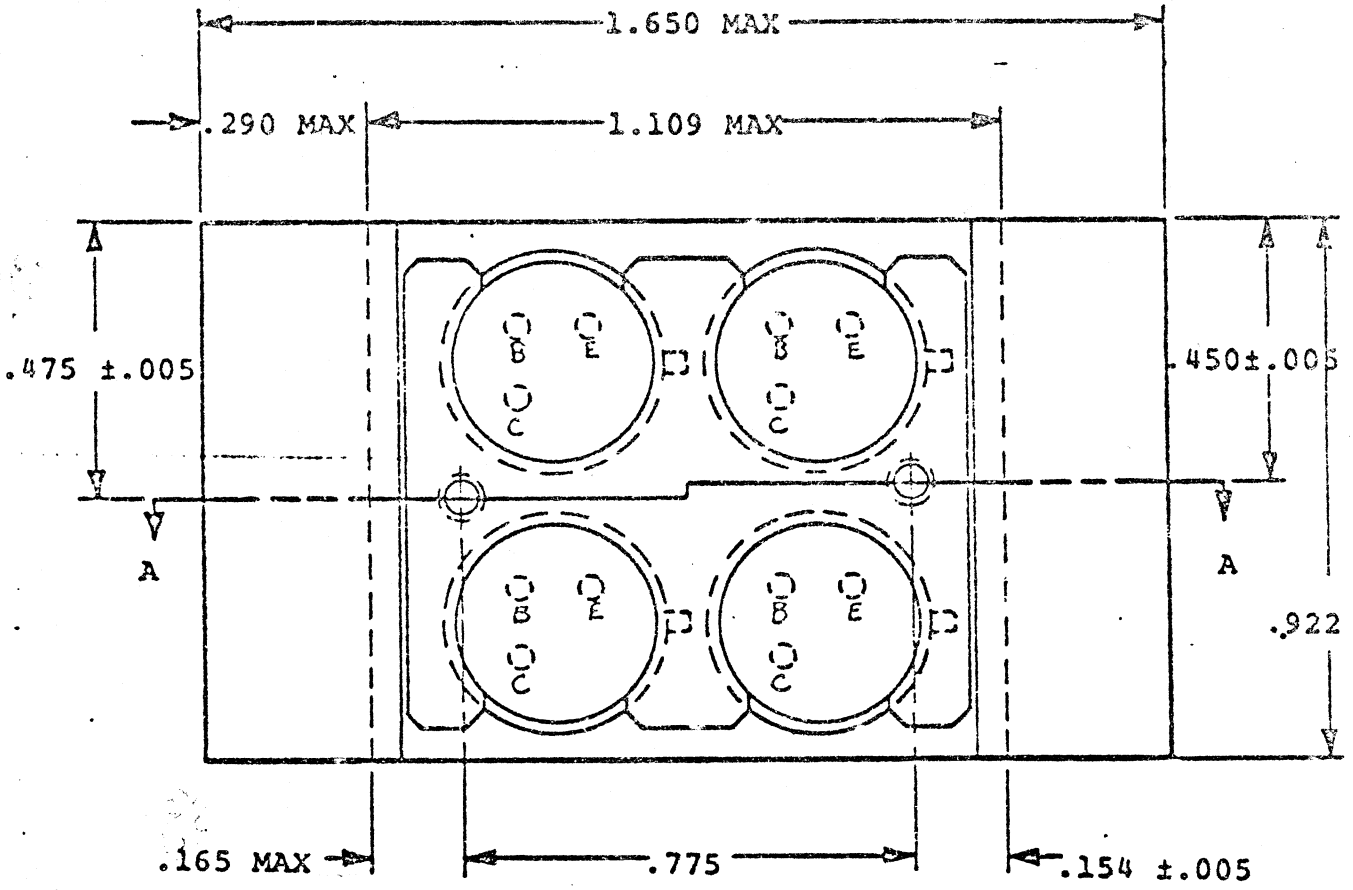
TOP VIEW



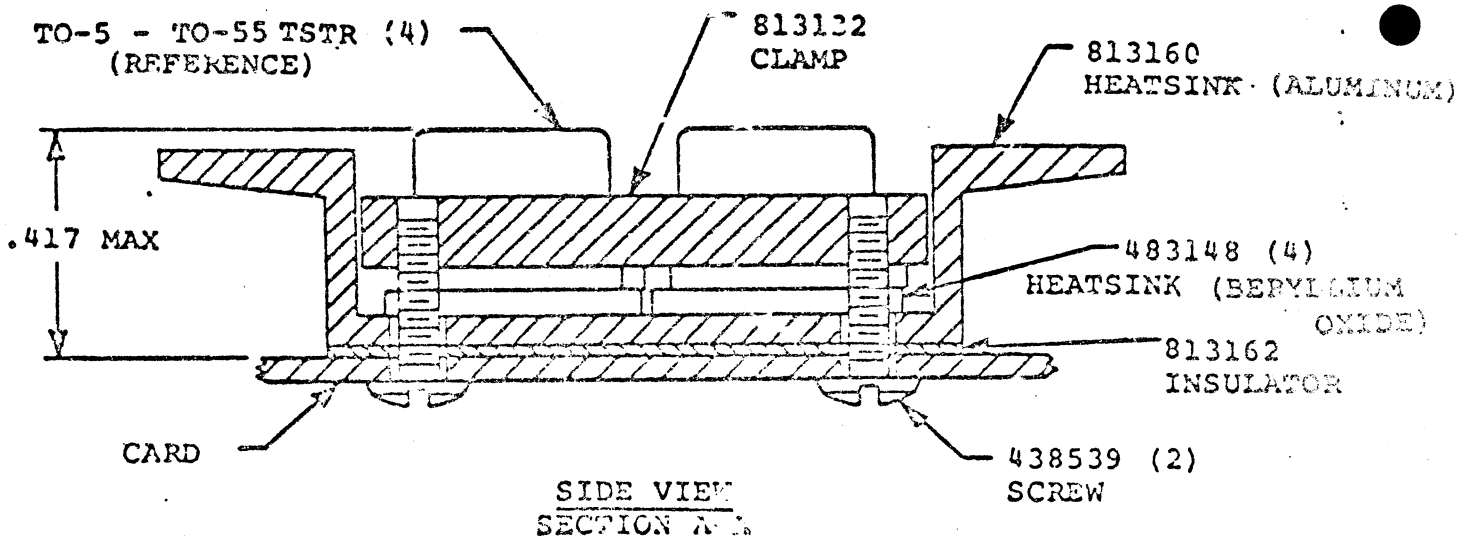
SIDE VIEW
SECTION A-A

PACKAGE (Cont'd)

HEATSINK 813160 - for 4 TRANSISTORS

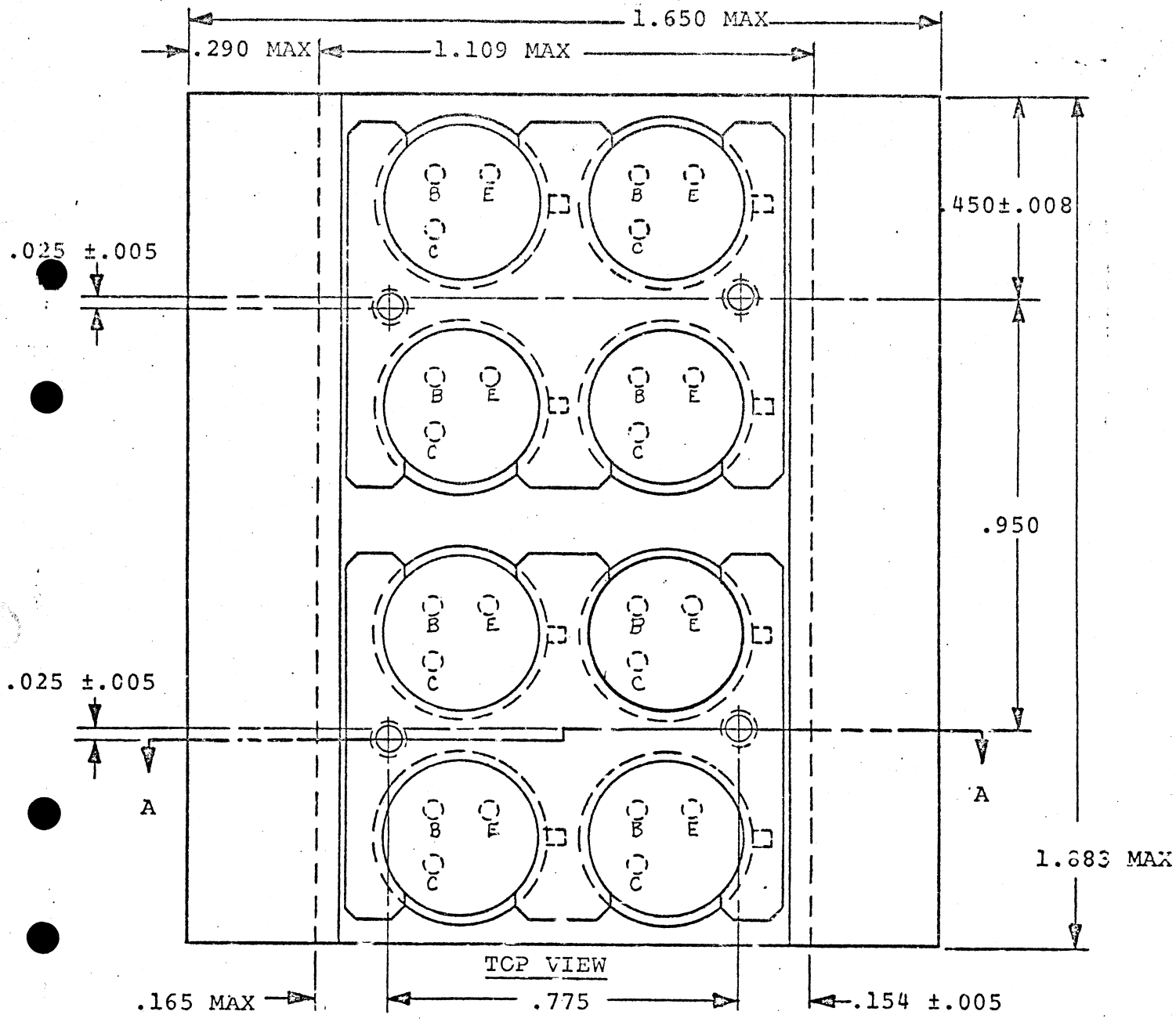


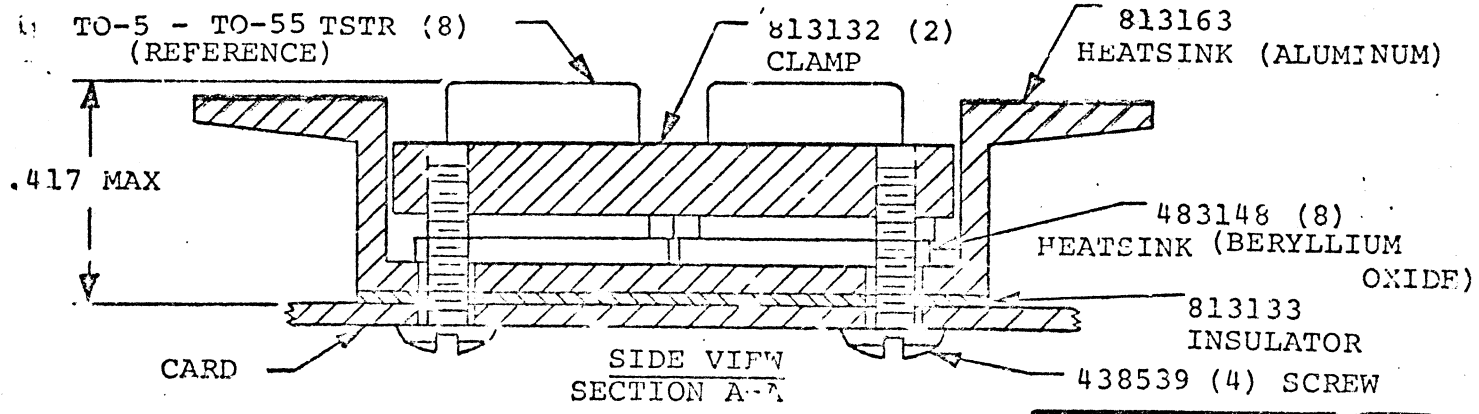
TOP VIEW



SIDE VIEW
SECTION A-A

PACKAGE (Cont'd) HEATSINK 813163 -for 8 TRANSISTORS





REQUIREMENTS

Mounting screws used to retain heatsink assemblies to the card require .096±.002 holes. The holes are to be drilled after plating in accordance with note code "BB".

Heatsink assemblies described in this section are not adaptable to MST card assemblies.

Note Code "AR" will be required for all heatsink assemblies described in this section. The note code will appear on the heatsink and transistor and in the note code field on the assembly drawing. The "AR" notes for these heatsink assemblies are listed in the note code section of the component library under the following note codes: OJ - OK - ON - OP - OS - OT - OW - OX - OY - OZ. The beryllium oxide heatsink is required between the heatsink and transistor, for insulation purposes, on all TO5 - TO55 heatsink assemblies. The use of silicon grease is optional, although not recommended. The wording of the "AR" notes listed in the component library reflect these options.

All parts listed in the "AR" note must appear, with their quantities, in the parts list on the assembly drawing and the Engineering Bill of Materials. The reference drawing part number must appear as the first special component when inputting the "AR" note.

Note Code "FH" must also appear in the note code field on the assembly drawing.

LIMITS

TO-5 - TO-55 Transistors, using heatsinks described in this section, must have their leads on or within the following "X" and "Y" grids:

Heatsink 813166

SLT/SLD	2 Hi-12	X 51 - 121	Y 71 - 108
	3 Hi-12	X 51 - 121	Y 71 - 168

Heatsink 813173

SLT/SLD	2 Hi-6-12	X 28 - 73 - 143	Y 63 - 115
	3 Hi-12	X 26 - 143	Y 63 - 175

LIMITS (Cont'd)

Heatsink 813160

SLT/SLD	2 Hi-6-12	X 28 - 73 - 143	Y 76 - 103
	3 Hi-12	X 28 - 143	Y 76 - 163

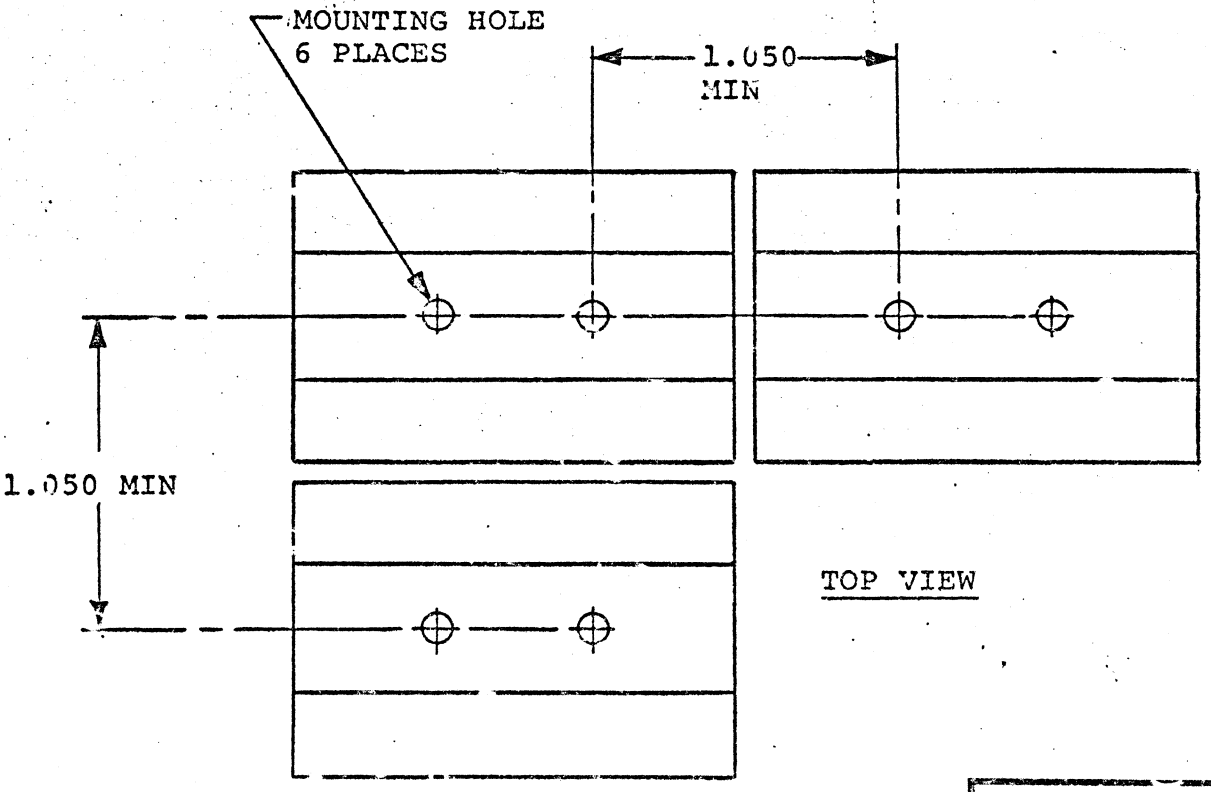
Heatsink 813160

SLT/SLD	2 Hi-12	X 28 - 143	Y 76 - 103
	3 Hi-12	X 28 - 143	Y 76 - 163

RELATIONSHIPS

The following illustrations show the minimum placement of adjacent heatsinks:

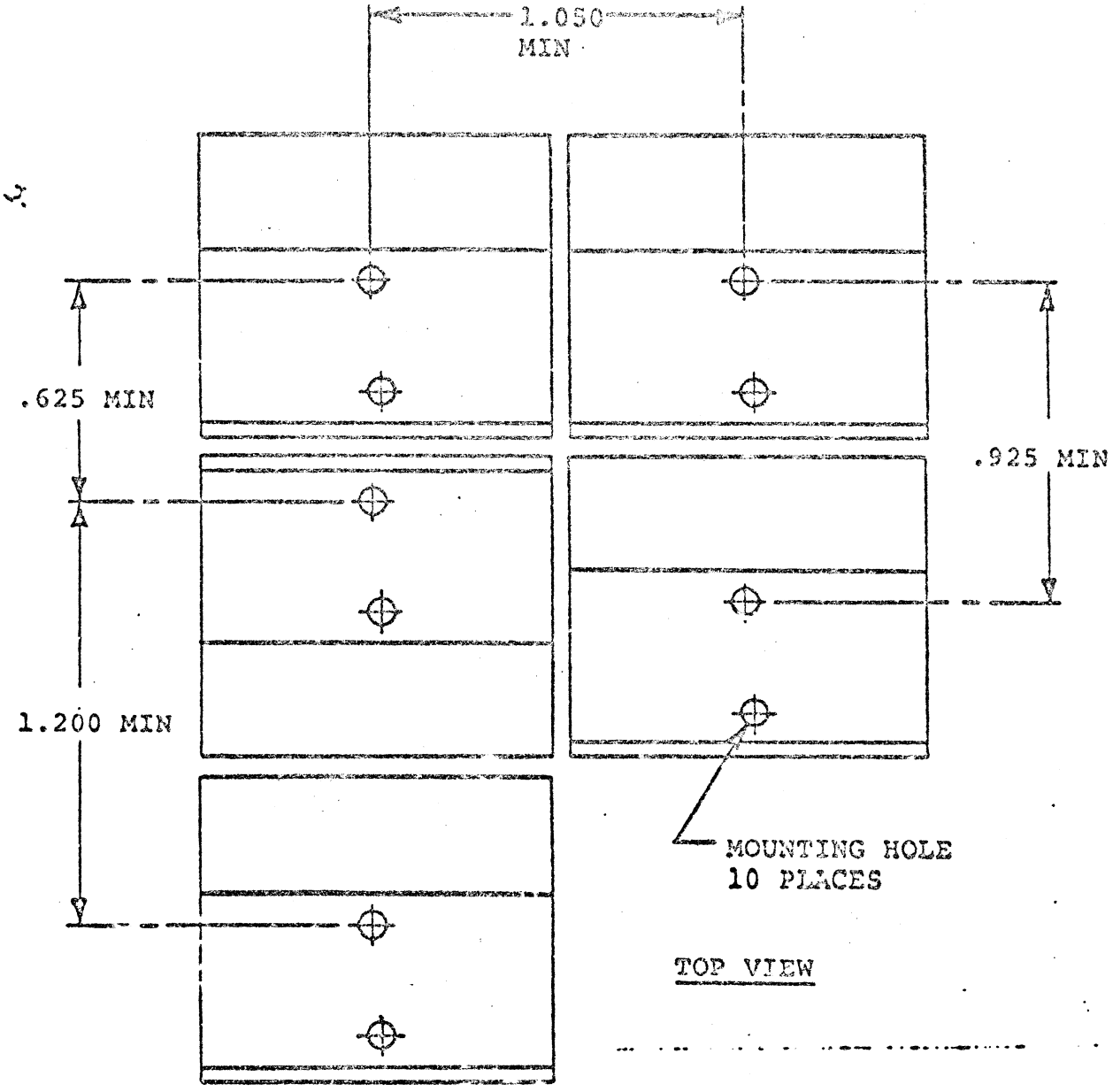
Heatsink 813166



TOP VIEW

RELATIONSHIPS (Cont'd)

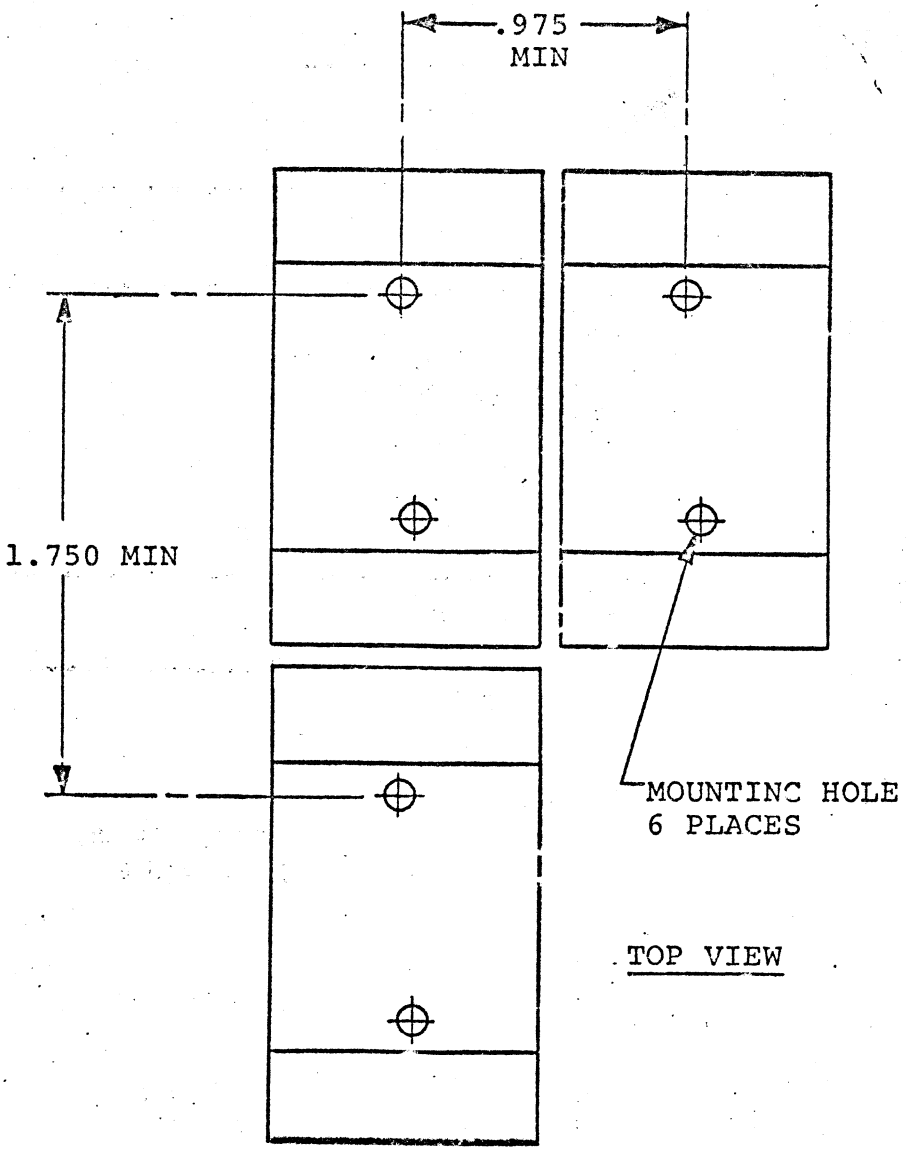
Heatsink 813173



TOP VIEW

RELATIONSHIPS (Cont'd)

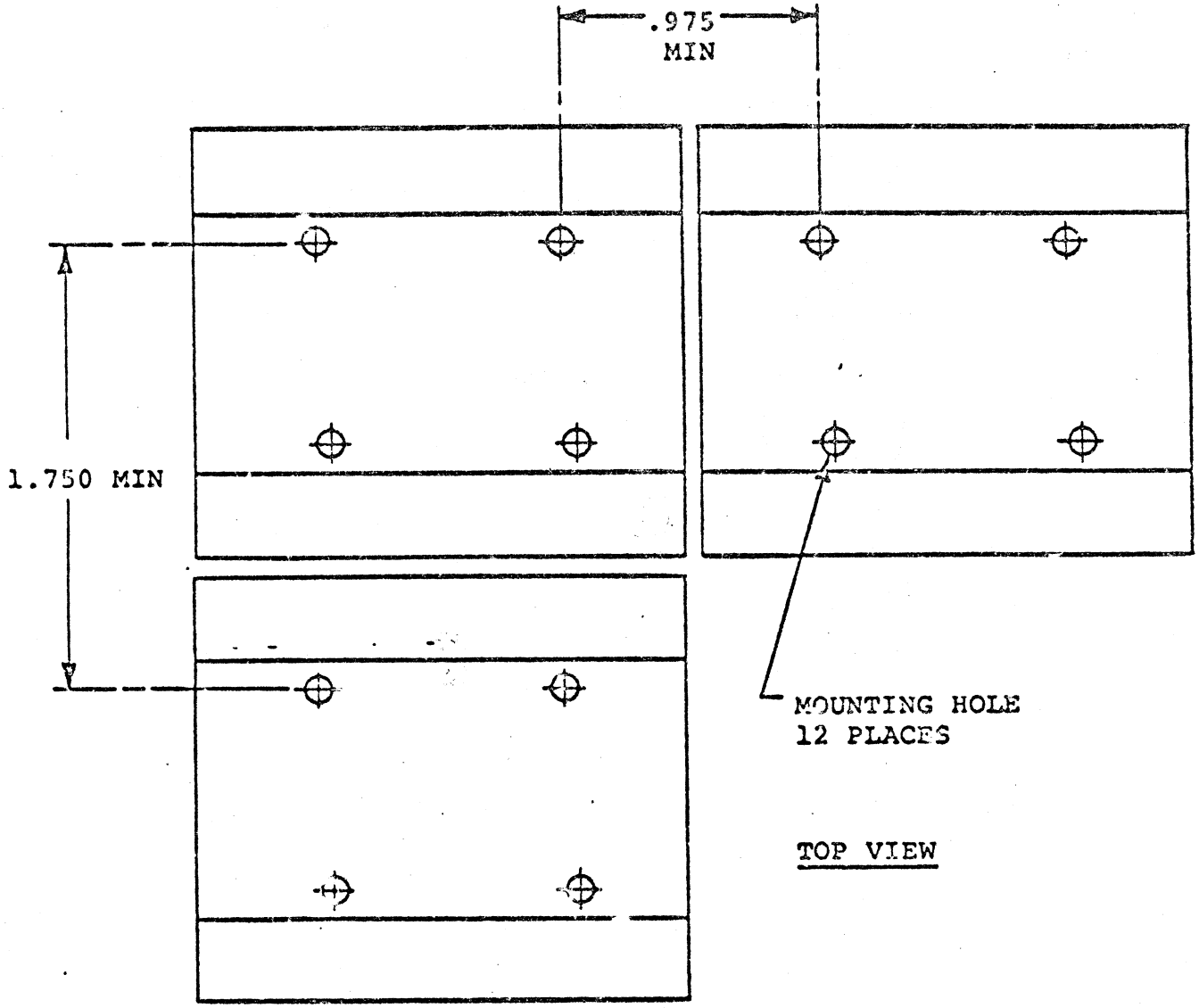
HEATSINK 813160



TOP VIEW

RELATIONSHIPS (Cont'd)

HEATSINK 813163



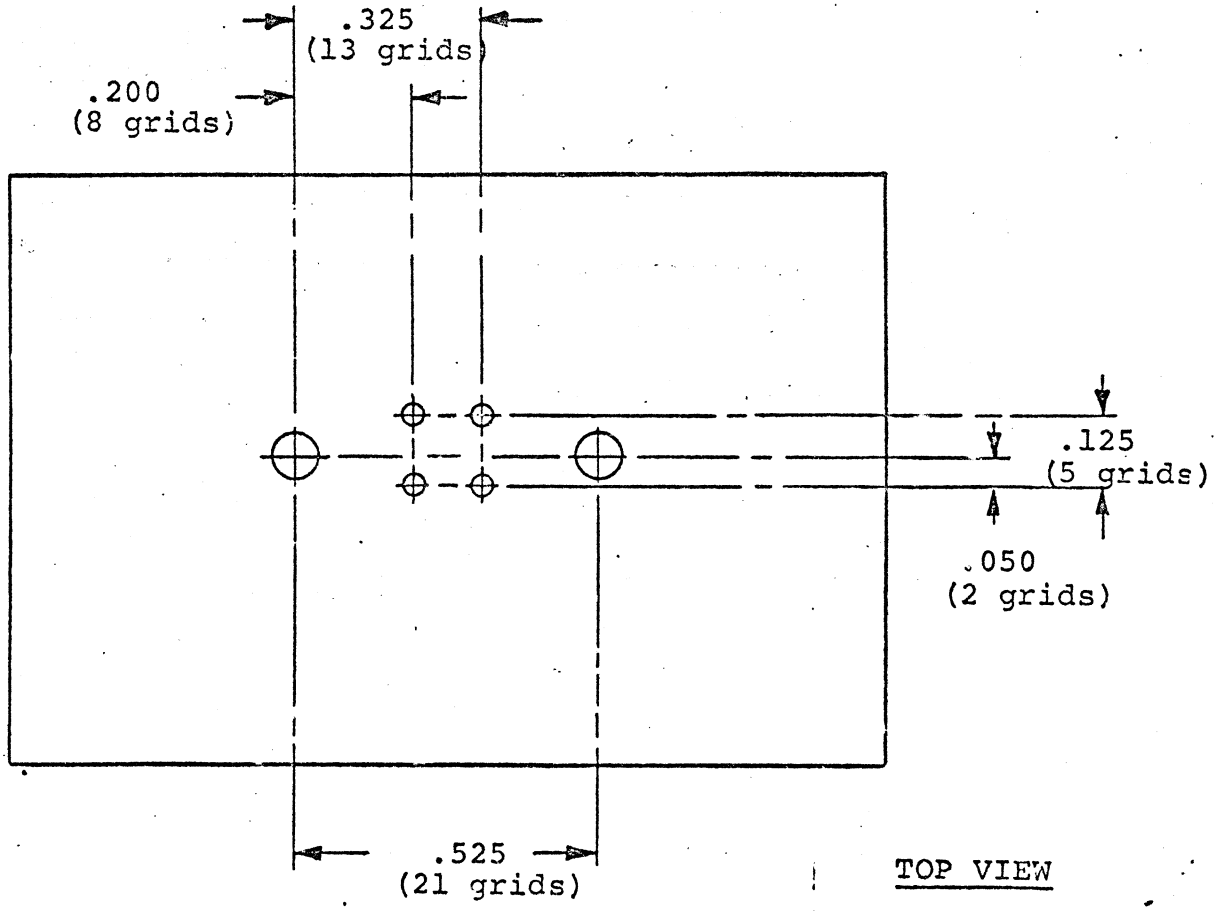
TOP VIEW

ARTWORKS

No circuit connections will be made to the transistors on the component side of the card.

The following drawings indicate the proper land and mounting hole placement.

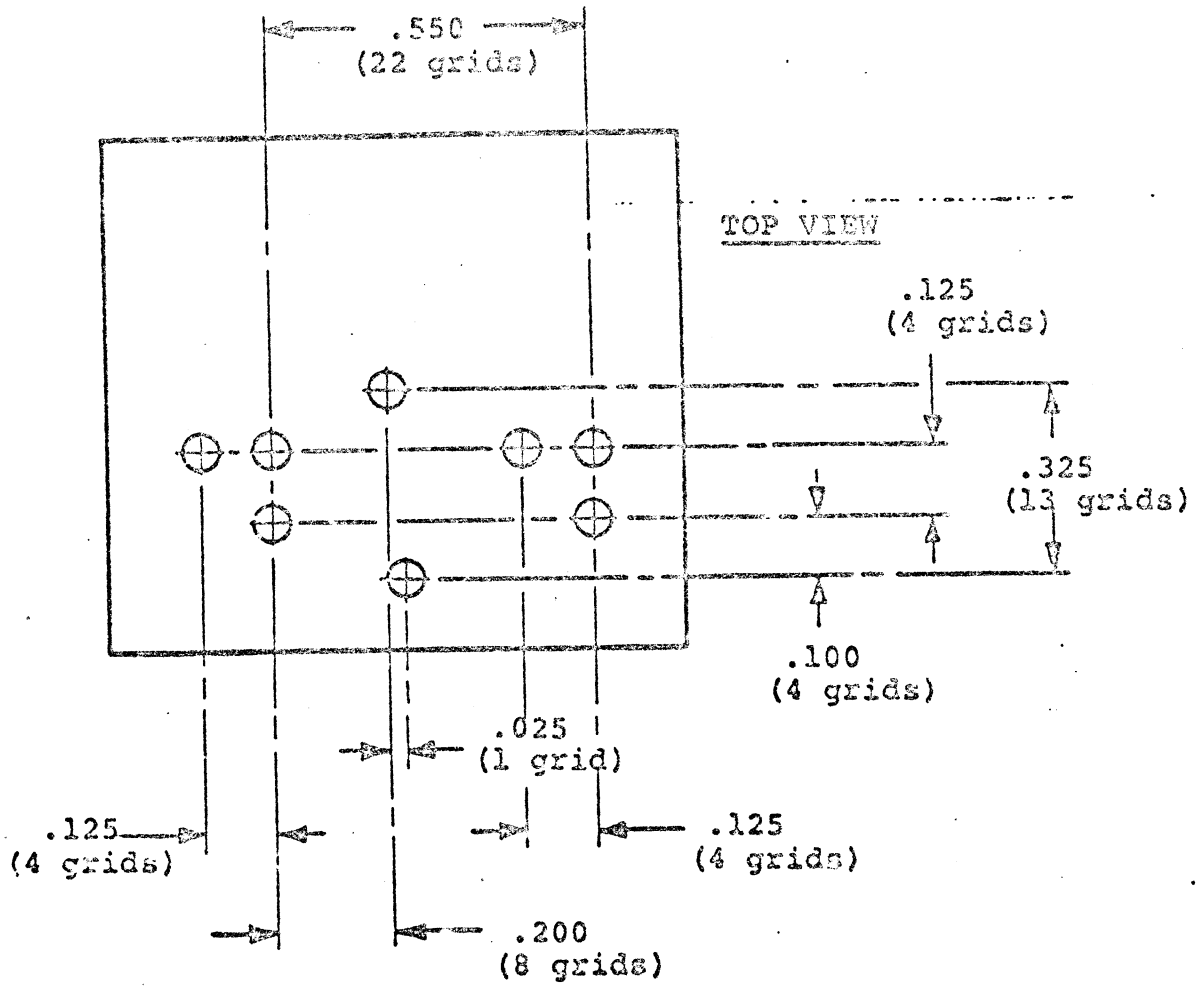
HEATSINK 813166



TOP VIEW

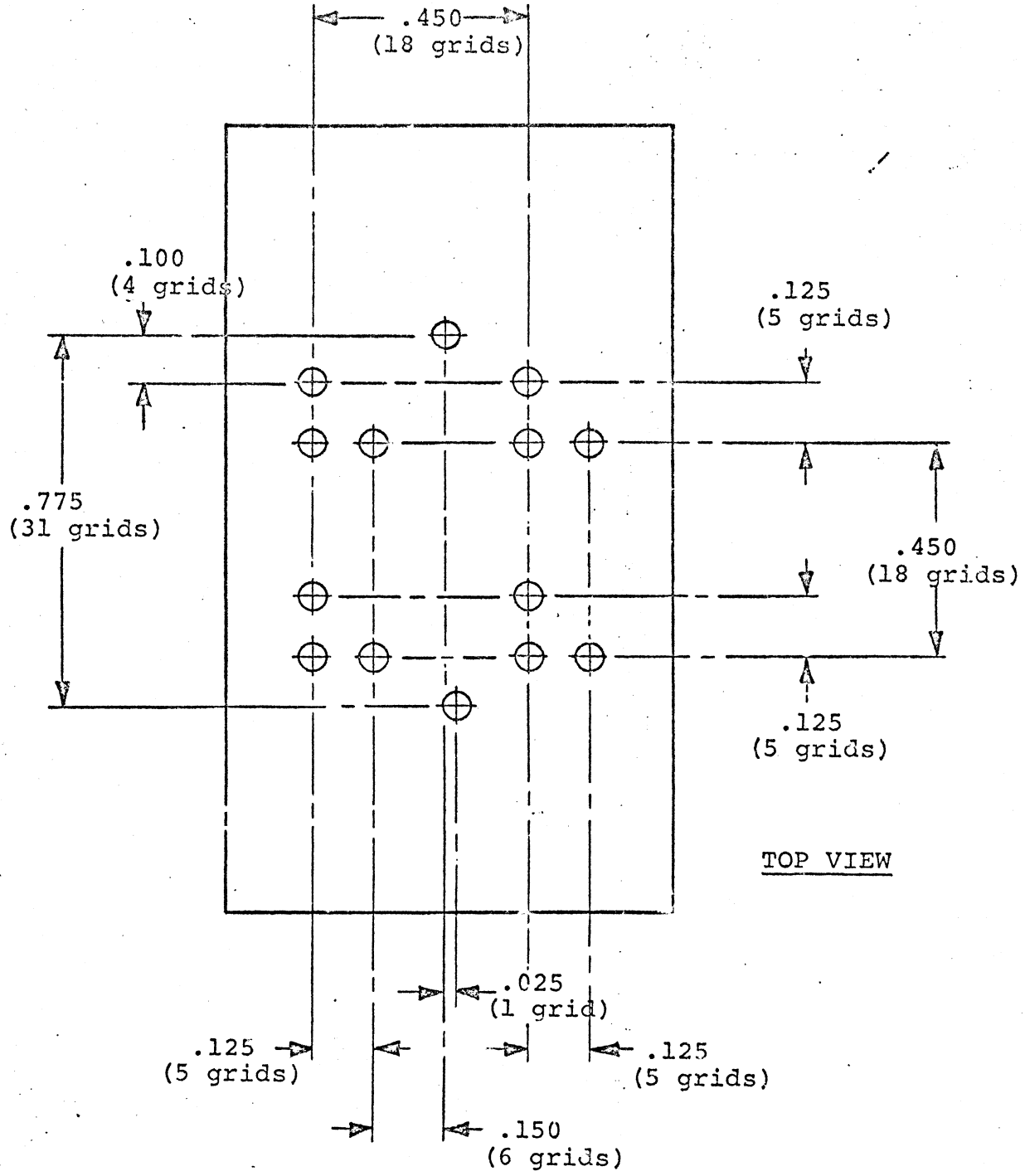
ARTWORKS (Cont'd)

HEATSINK 813173



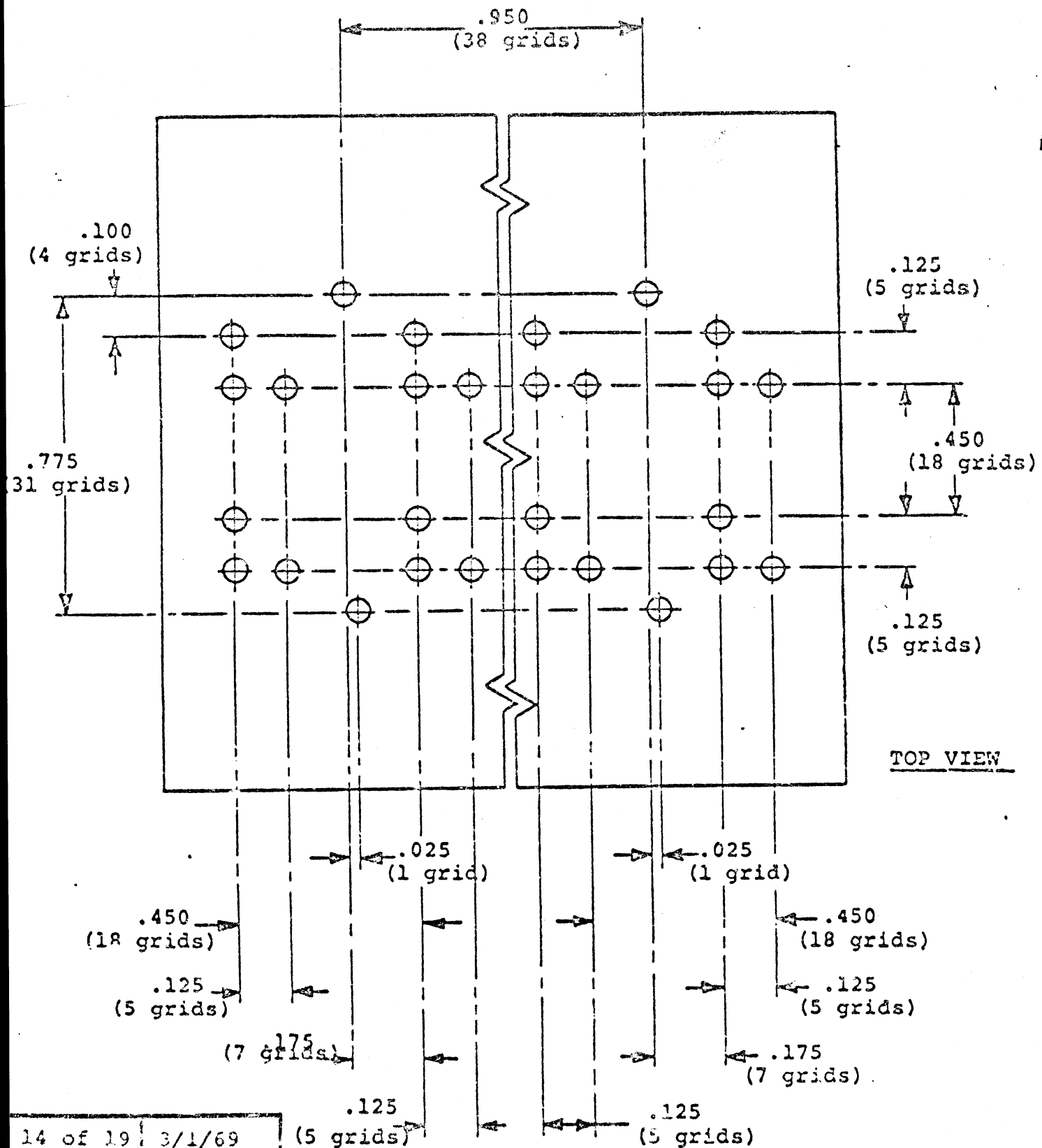
ARTWORK (Cont'd)

HEATSINK 813160



ARTWORKS (Cont'd)

HEATSINK 813163

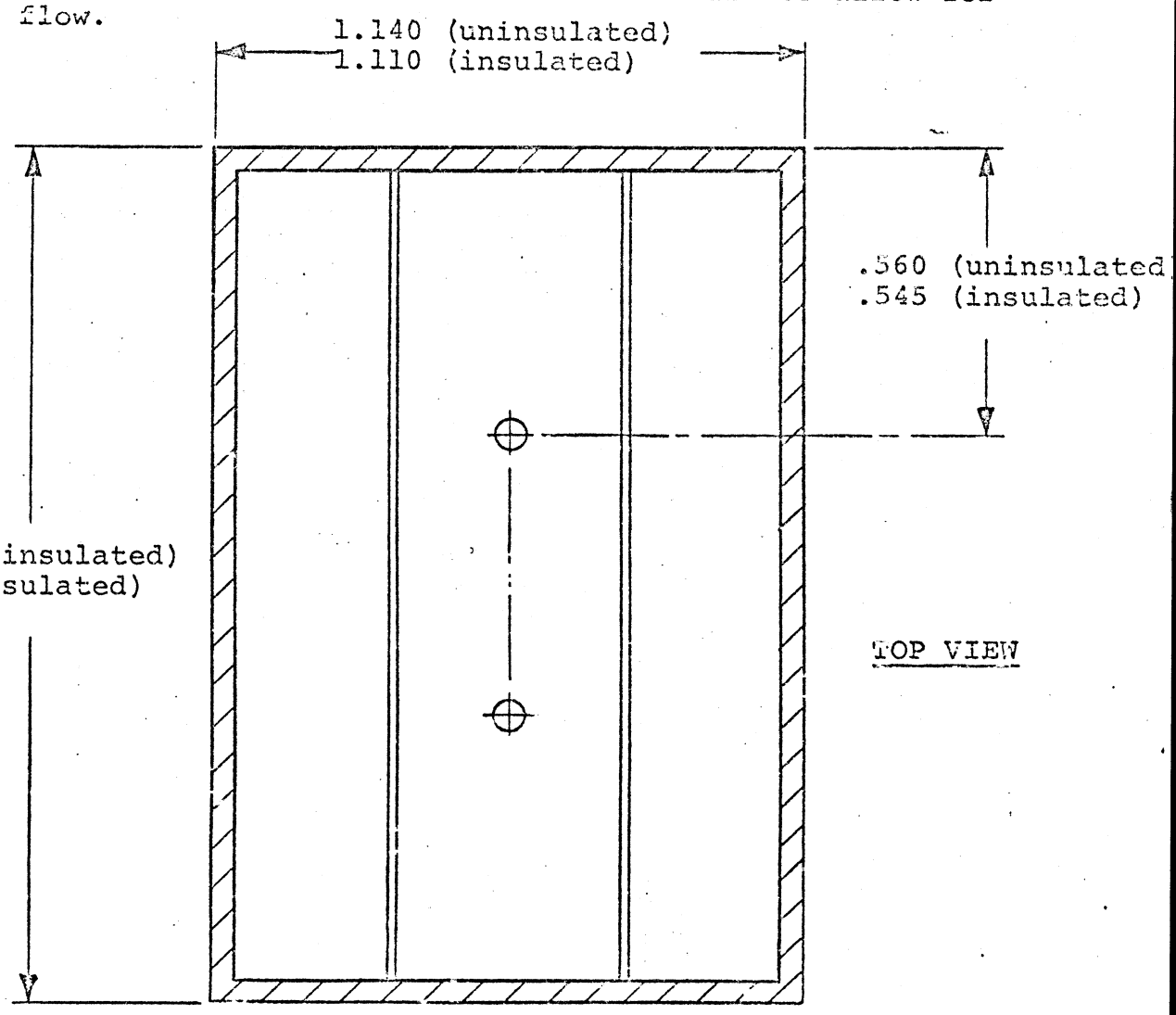


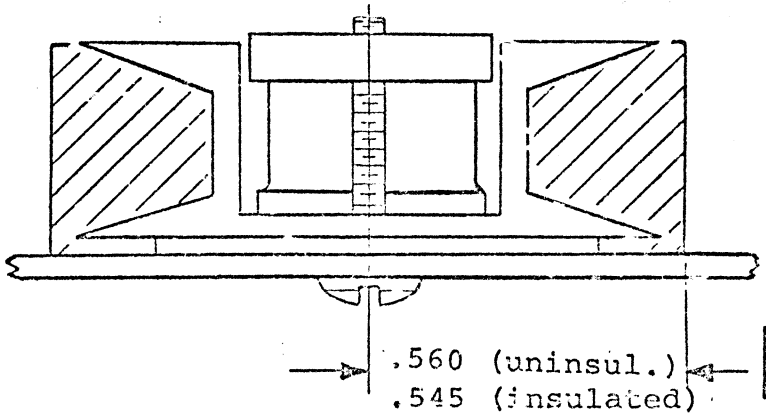
SEQUENCE EFFECT

The following illustrations show the TO-5 - TO-55 Heatsink restricted area for all other adjacent components.

HEATSINK 813166

This Heatsink must be placed on the card assembly so that the long axis of the Heatsink is parallel to the Y-Y axis of the card. Large components should not be mounted on the bottom side of the card to allow for proper air flow.

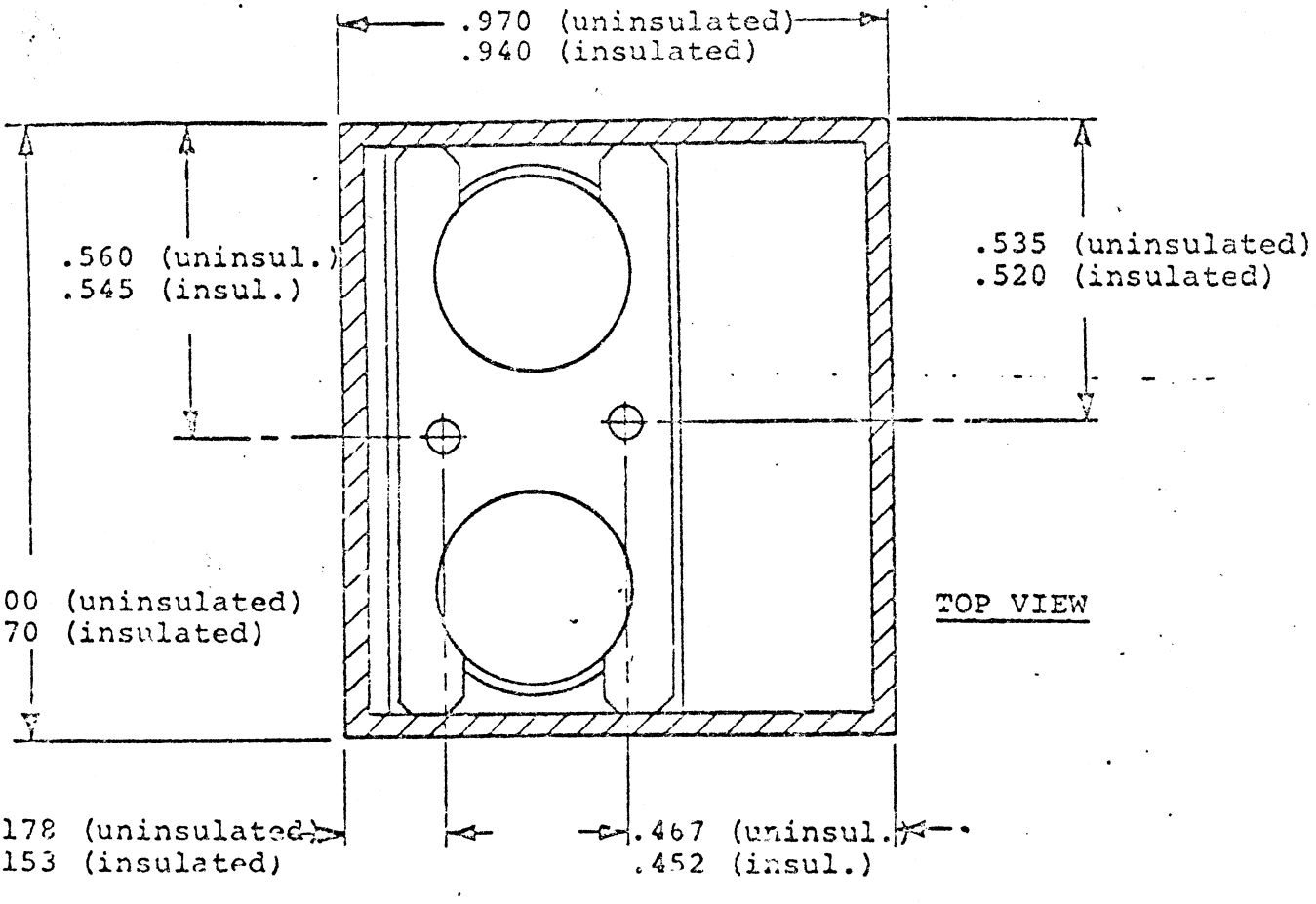


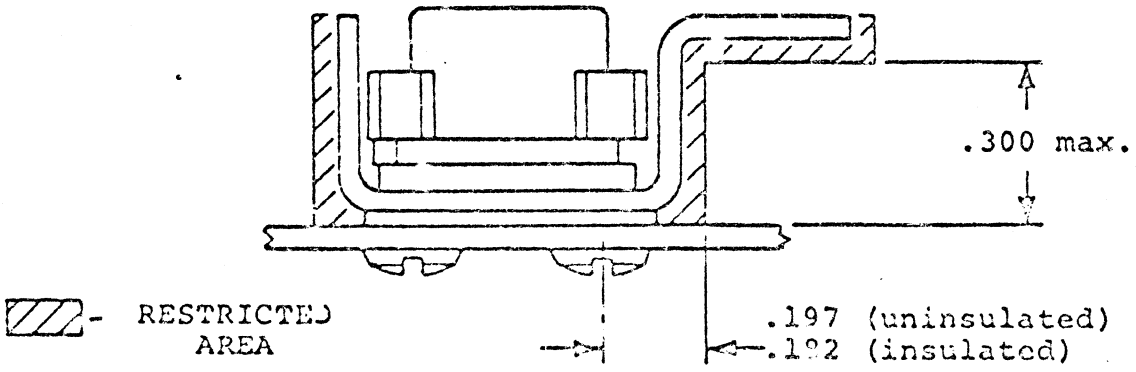


EQUENCE EFFECTS (Cont'd)

HEATSINK 813173

his Heatsink should be placed on the card so that the long axis is parallel o the air flow in a gate. Components not exceeding .300 in height may be laced under the fin that extends from the Heatsink.



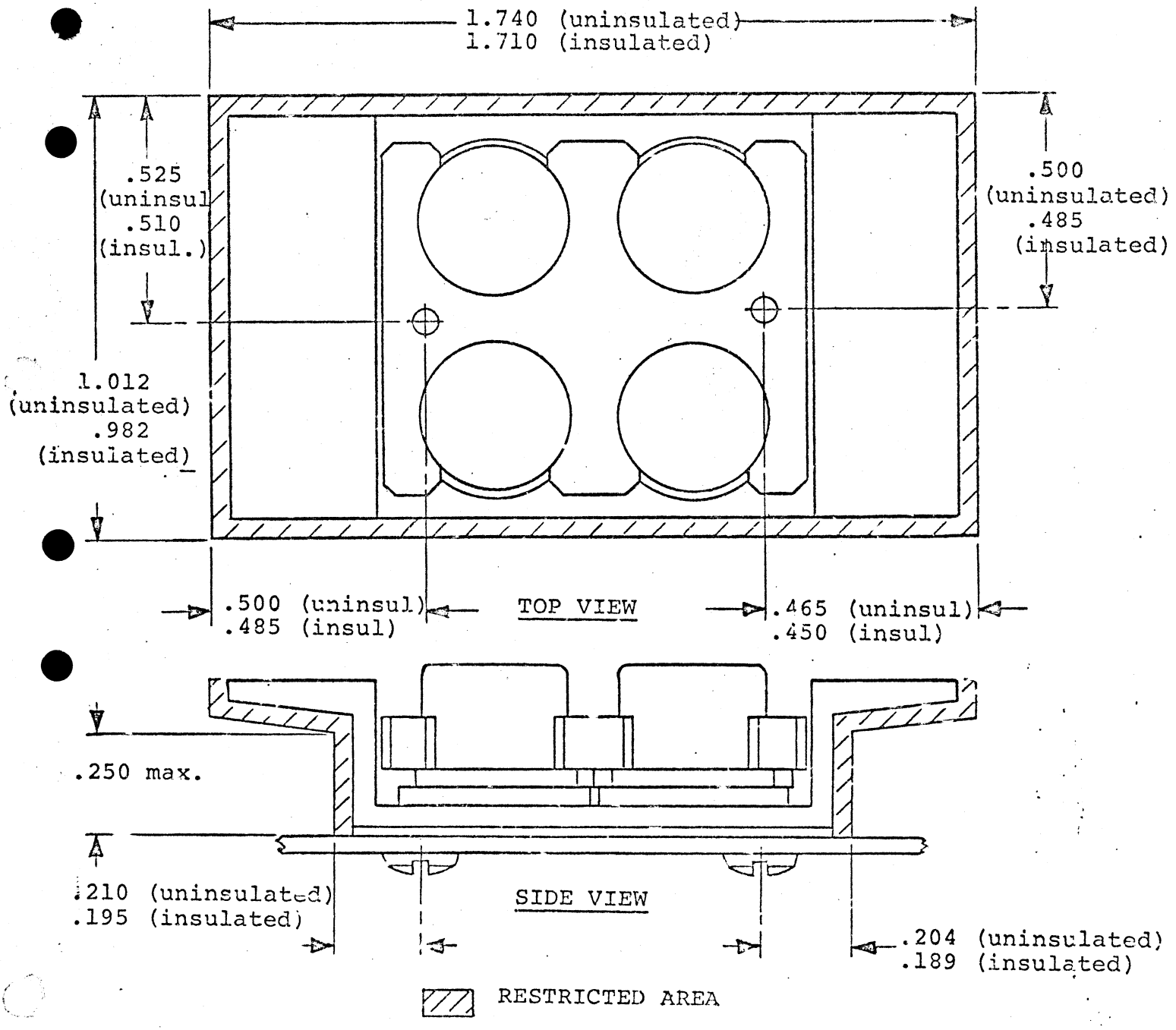


SIDE VIEW

SEQUENCE EFFECTS (Cont'd)

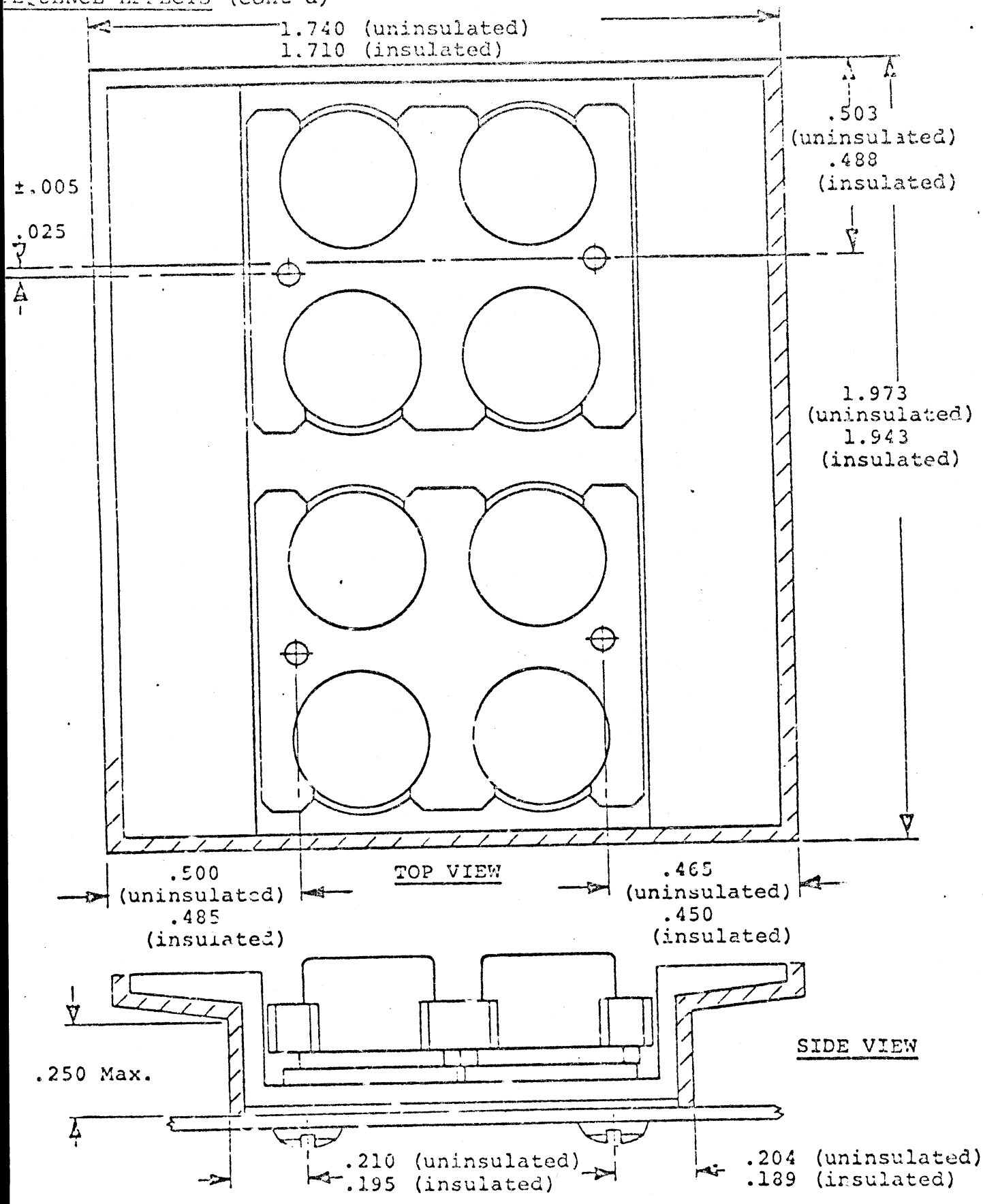
HEATSINK 813160

This Heatsink should be placed on the Card Assembly so that the Heatsink Fins are parallel to the air flow in a gate. Components not exceeding .250 height may be placed under the fins that extend from the Heatsink.



SEQUENCE EFFECTS (Cont'd)

HEATSINK 813163



SEQUENCE EFFECTS (Cont'd)

HEATSINK 816163 (Cont'd)

This Heatsink should be placed on the Card Assembly so that the fins on the Heatsink are parallel to the air flow in a gate. Components not exceeding .250 height may be placed under the fins that extend from the Heatsink.

HAND ASSEMBLY

These Heatsink Assemblies will be assembled manually during the "Manual assembly of non-wettables" operation.

PROCESS INFORMATION

TO-5 - TO-55 Transistors using these heatsink assemblies are not mechanically secured to the card by their leads. The transistors must have a lead length of greater than .200 inch.

PLANNING

No significant changes are being planned. No automatic or semi-automatic assembly equipment is contemplated.

IBM Division Engineering Practice

TO-3 TRANSISTORS

DESCRIPTION

Devices in TO-3 packages have metal cans and headers. These packages are 2, 3, or 4 leaded components. The package is electrically hot. The assembly drawing code is "Q".

PACKAGE

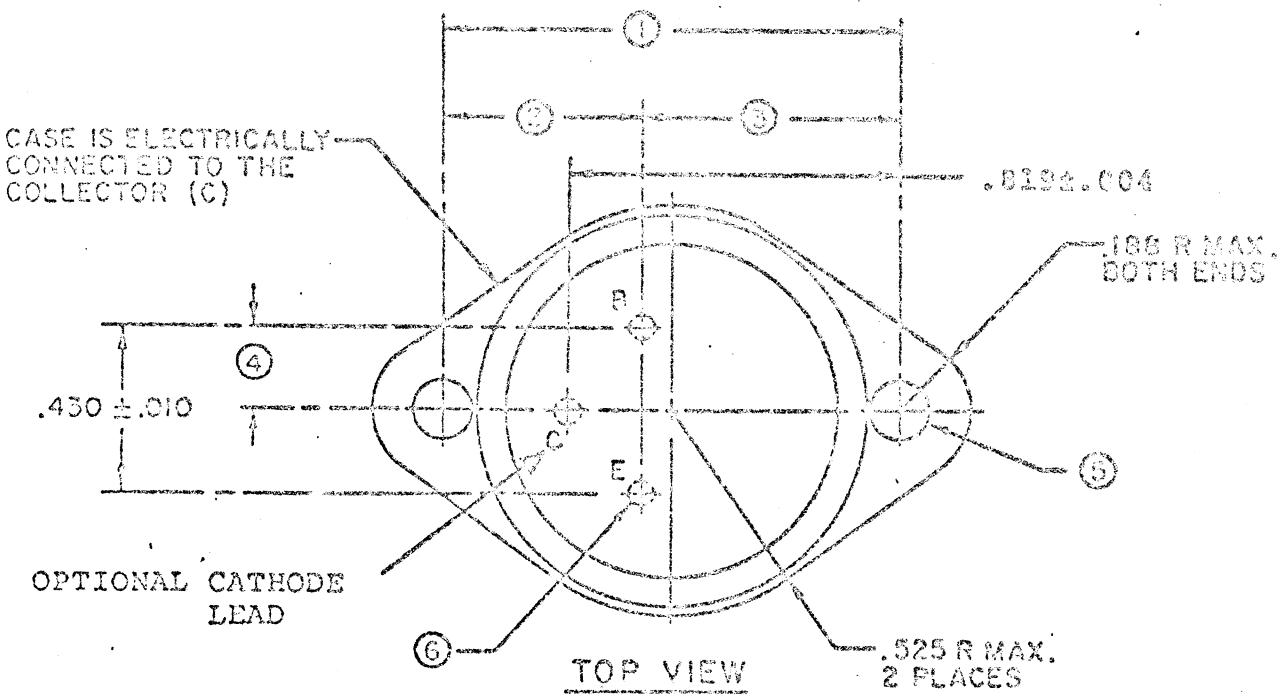
All physical outlines of TO-3 packages are contained in the following coded list, and are in the component library maintained by the EC level of the component part number.

2TO3A	2TO3C	2TO3D2	2TO3J
2TO3B	2TO3C1	2TO3E	2TO3K
2TO3B1	2TO3C2	2TO3F1*	
2TO3B2	2TO3D	2TO3G	
2TO3B3	2TO3D1	2TO3H	

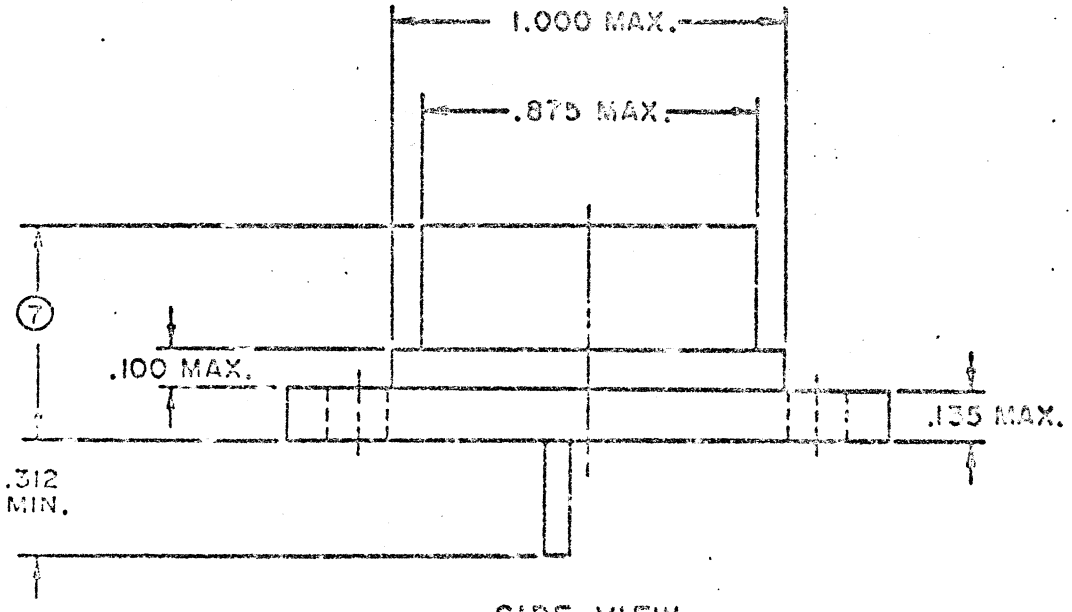
NOTE:

Physical outline 2TO3F1 provides for an optional cathode (C) lead (See following drawing). This optional lead will physically appear only on world trade transistors of this outline. Therefore, when using a transistor classified 2TO3F1, it is essential that an .081 plated through hole be provided for this optional lead. The circuitry to the cathode junction should be connected to this hole as well as the land to which the jumper assembly will be soldered. This process is necessary to facilitate the manufacturing of this card in domestic and world trade facilities.

PACKAGE (Cont'd)



TOP VIEW
2 LEADED AS RECEIVED

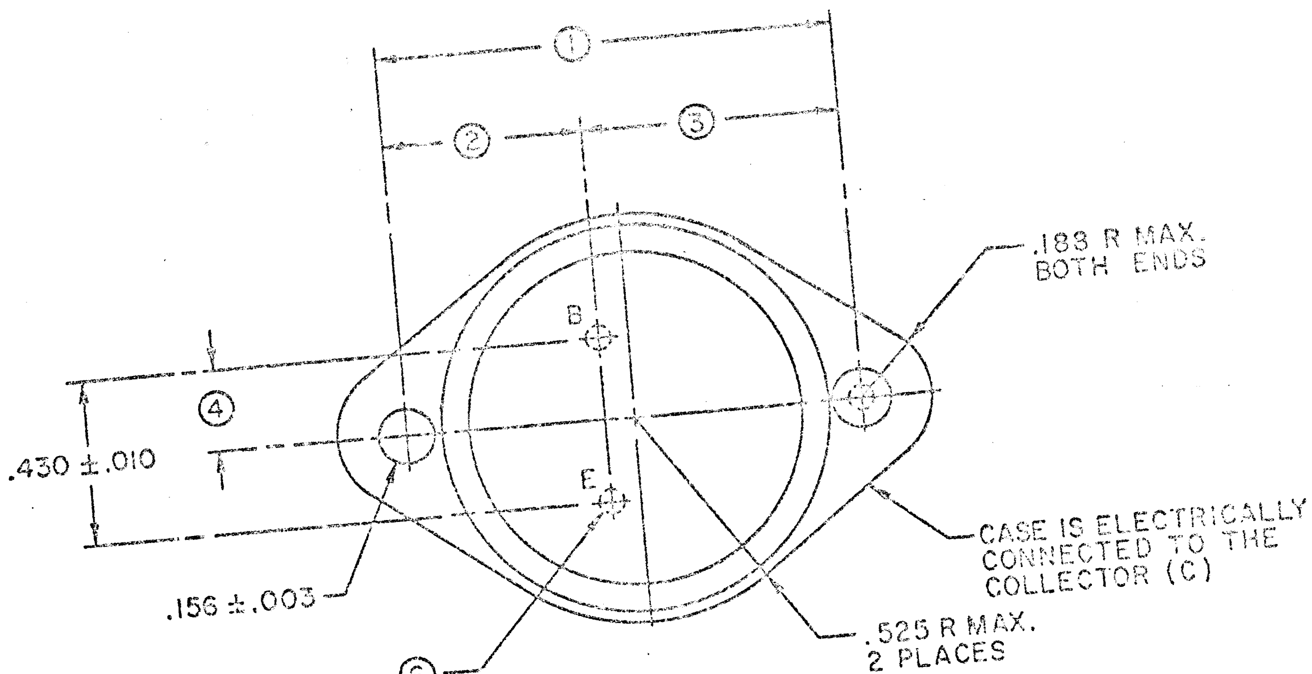


SIDE VIEW
2 LEADED AS RECEIVED

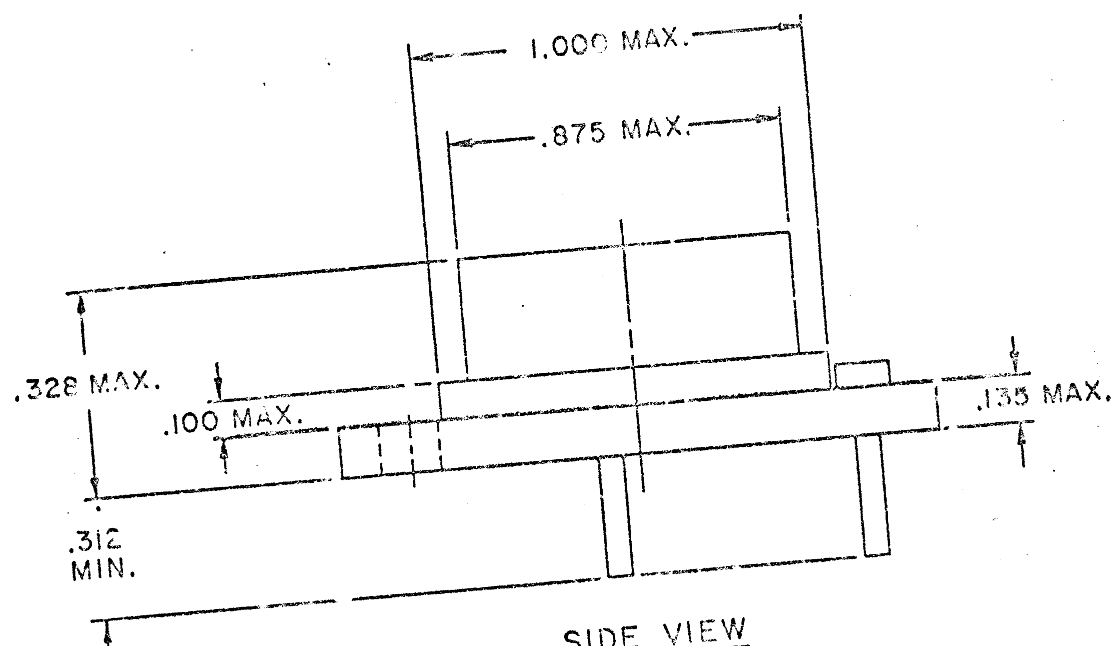
These views are for layout purposes only. Part drawings shall have precedence.

TO-3 TRANSISTORS

PACKAGE (Cont'd)

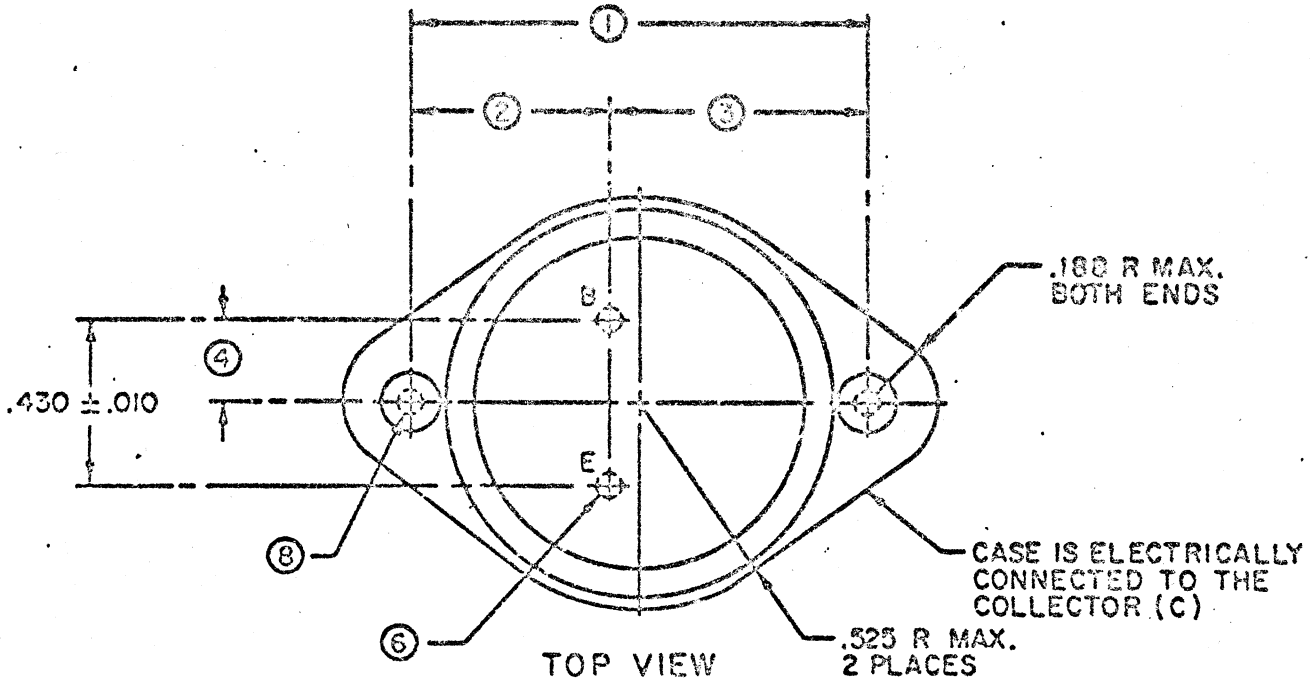


TOP VIEW
3 LEADED AS RECEIVED

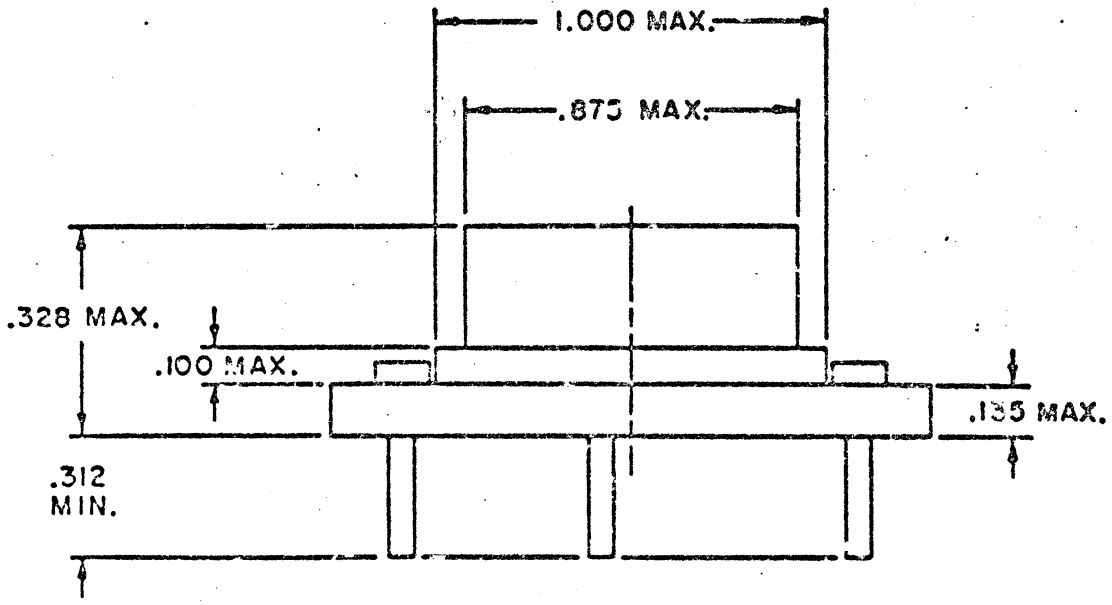


SIDE VIEW
3 LEADED AS RECEIVED

PACKAGE (Cont'd)



TOP VIEW
4 LEADED AS RECEIVED



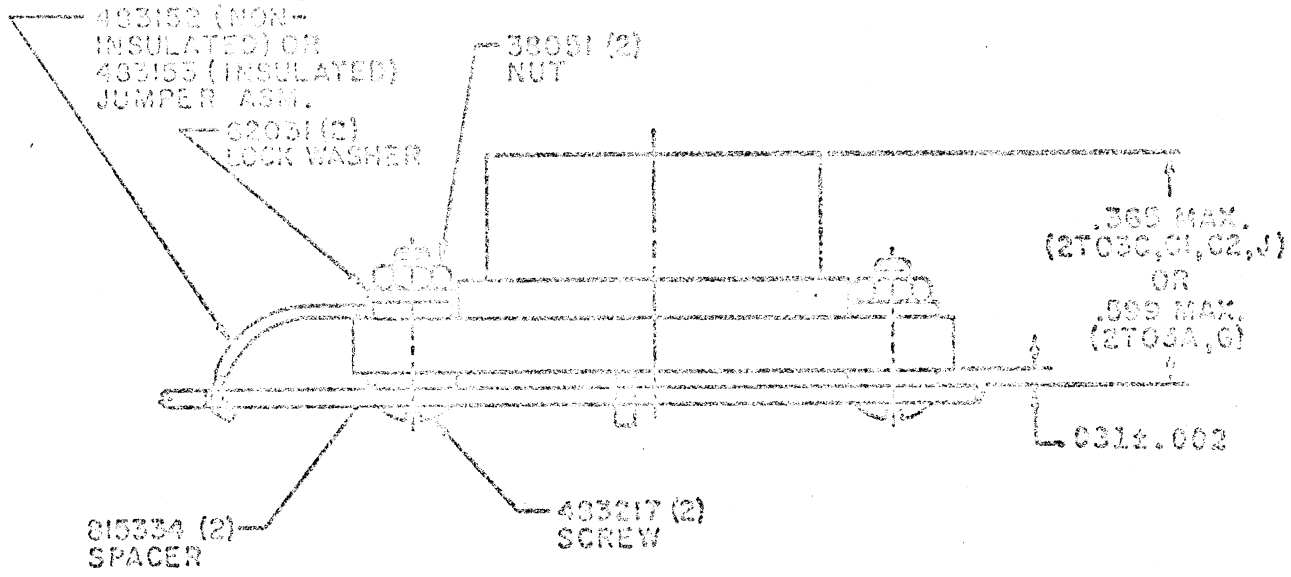
SIDE VIEW
4 LEADED AS RECEIVED

PACKAGE (Cont'd)

1 THRU 8 ARE THE DIFFERENCES AS INDICATED BY PHYSICAL OUTLINE DRAWINGS		
REF. NO.	PHYSICAL OUTLINE DRAWING	RELATED DIMENSIONS
1	2TO3A, B, B1, B2, B3, C, C1, C2, D, D1, D2, E, F1	SEE DIMENSIONS 2 AND 3
	2TO3G, H, J, K	1.187 ±.010
2	2TO3A, B, B1, B2, B3, C, C1, C2, D, D1, D2, E, F1	.521 ±.005
	2TO3G, H, J, K,	SEE DIMENSIONS 1 AND 3
3	2TO3A, B, B1, B2, B3, C, C1, C2, D, D1, D2, E, F1	.665 ±.005
	2TO3G, H, J, K	.665 ±.010
4	2TO3A, B, B1, B2, B3, C, C1, C2, D, D1, D2, E, F1, K	.215 ±.005
	2TO3G, H, J	.215 ±.010
5	2TO3A, E, G	.156 ±.003 DIA. 2 HOLES
	2TO3C, C1, C2, F1, J	.156 ±.005 DIA. 2 HOLES
	2TO3D, D1, D2, K	.156 ±.003 DIA. 1 HOLE
6	2TO3A, C, E, G	.040 $^{+.003}_{-.002}$ DIA. 2 LEADS
	2TO3D	.040 $^{+.003}_{-.002}$ DIA. 3 LEADS
	2TO3 B1, B3, C1, C2, H, J	.040 $^{+.013}_{-.002}$ DIA. 2 LEADS
	2TO3 D1, D2, K	.040 $^{+.013}_{-.002}$ DIA. 3 LEADS
	2TO3 F1	.060MAX/.038MIN LEAD DIA.
7	2TO3B, B1, B2, B3, C, C1, C2, D, D1, D2, F1, H, J, K	.328 MAX.
	2TO3A, E, G	.562 MAX.
8	2TO3 B1, B3, H	.040 $^{+.003}_{-.002}$ DIA.2(C)LEADS
	2TO3B, B2	.040 $^{+.003}_{-.002}$ DIA. 4 LEADS

REQUIREMENTS

The following illustrations show the proper assembly techniques and hardware required for mounting SC-3 Transistors:



SIDE VIEW
2 LEADED

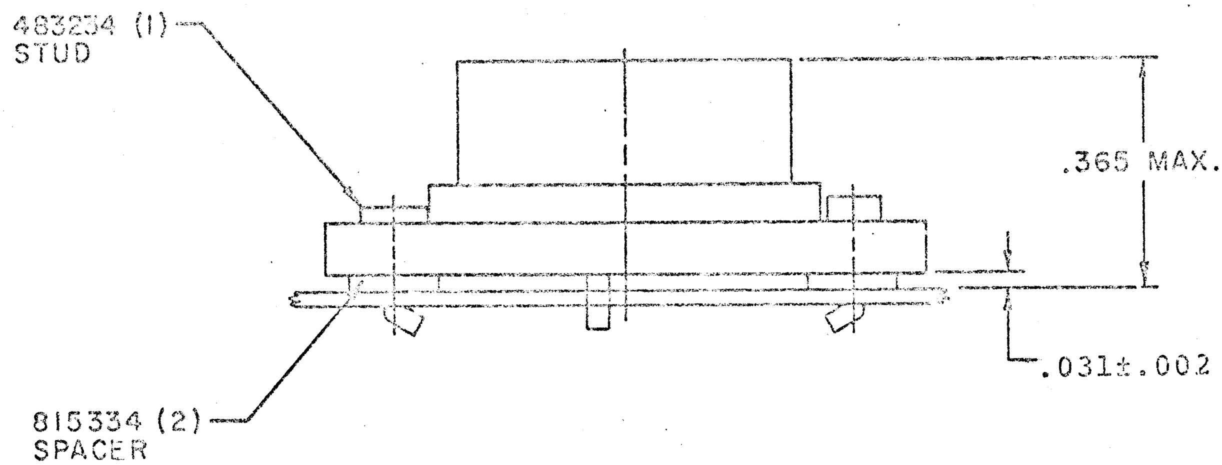
Note Code "AR" will be required for two leaded SC-3 Transistors. This note code will appear on the component view and in the note code field on the assembly drawing. For the proper wording of the "AR" note see note code 1C in the note code section of the component library. All hardware items shown above and on reference drawing 8160l4 must appear in the parts list on the assembly drawing and also in the Bill of Material. This assembly hardware should also be used for physical outline 2 TO3Y1.

The reference drawing part number must appear as the first special component when inputting the "AR" note.

Emitter and base leads must be mounted in .081 ± .002 diameter holes. These holes are to be drilled before plating (ref. note RR) with .103 square lands on both sides of the card. The mounting screws require .156 ± .002 diameter holes to be drilled after plating. (Ref. note BB)

When it is required an "FB" note code must appear in the note code field on the assembly drawing.

REQUIREMENTS (Cont'd)



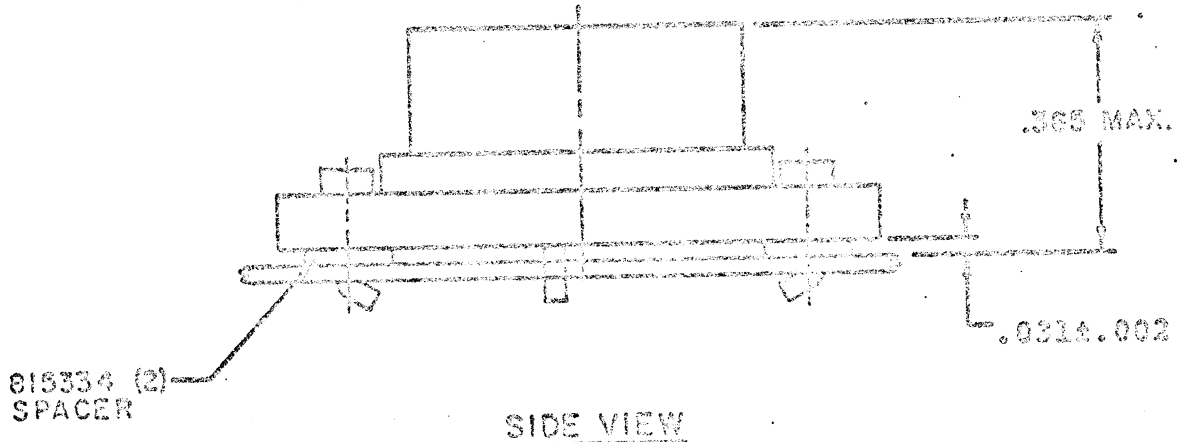
SIDE VIEW
3 LEADED

Note Code "AR" will be required for three-leaded TO-3 Transistors. This note code will appear on the component view and in the note code field on the assembly drawing. For proper wording of the "AR" note see note code 1E in the note code section of the component library. All hardware items shown above and on reference drawing 8:6015 must appear in the parts list on the assembly drawing and in the bill of material.

The reference drawing part number must appear as the first special component when inputting the "AR" note.

Leads must be mounted in .081±.002 diameter holes. These holes are to be drilled before plating (Ref. note BA) with .103 square lands on both sides of the card.

REQUIREMENTS (Cont'd)



SIDE VIEW
4 LEADED

Note Code "AZ" will be required for four-leaded TO-3 Transistors, this note code is worded as follows: "Transistor emitter and base leads are not to be bent in any way. Washer P/N 815334 is mounted on collector leads between the card and the bottom of the transistor. Crimp collector leads." Spacer 815334 is to be called out in the parts list on the assembly drawing and also in the bill of material.

Leads must be mounted in .0814.002 diameter holes. These holes are to be drilled before plating, (Ref. note code EX) with a location tolerance of ±.005 inch.

LIMITS

TO-3 Transistor packages 2, 3 or 4 leaded with the mounting holes or collector leads mounted on the "Y" axis and the emitter and base leads on the "X" axis, the leads must be on or within the following grid locations:

1 Hi-12	X28 - 143	Y33 - 53
2 Hi-12	X28 - 143	Y33 - 113
3 Hi-12	X28 - 143	Y33 - 173

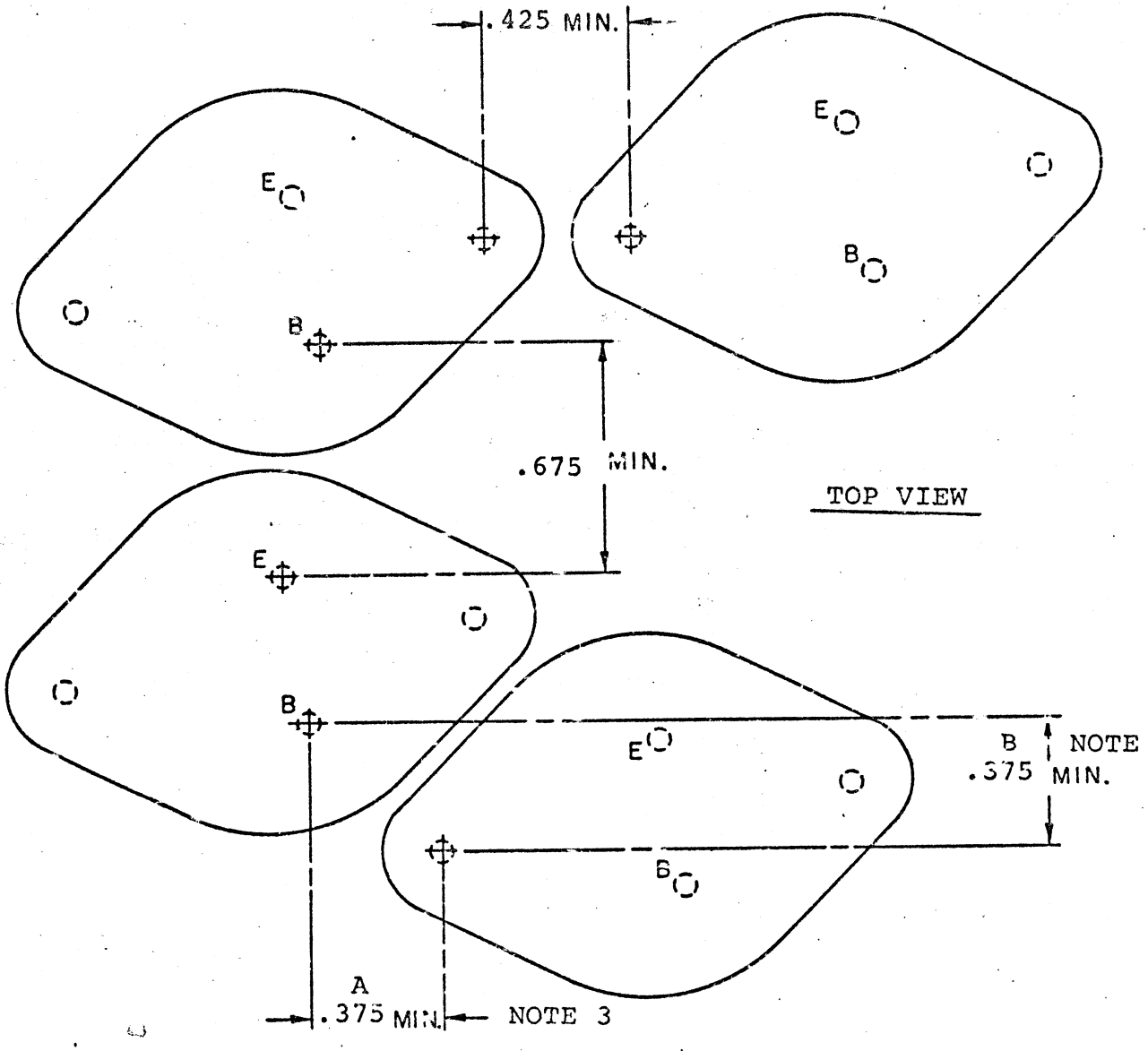
LIMITS (Cont'd)

TO-3 packages (2, 3 or 4 leaded) with the mounting holes or collector leads mounted on the "X" axis and the emitter and base leads on the "Y" axis, the leads must be on or within the following grid locations:

2 Hi-6-12	X32 - 69 - 139	Y28 - 118
3 Hi-12	X32 - 139	Y28 - 178

RELATIONSHIPS

The following illustration shows the physical minimum placement of TO-3 Transistors.



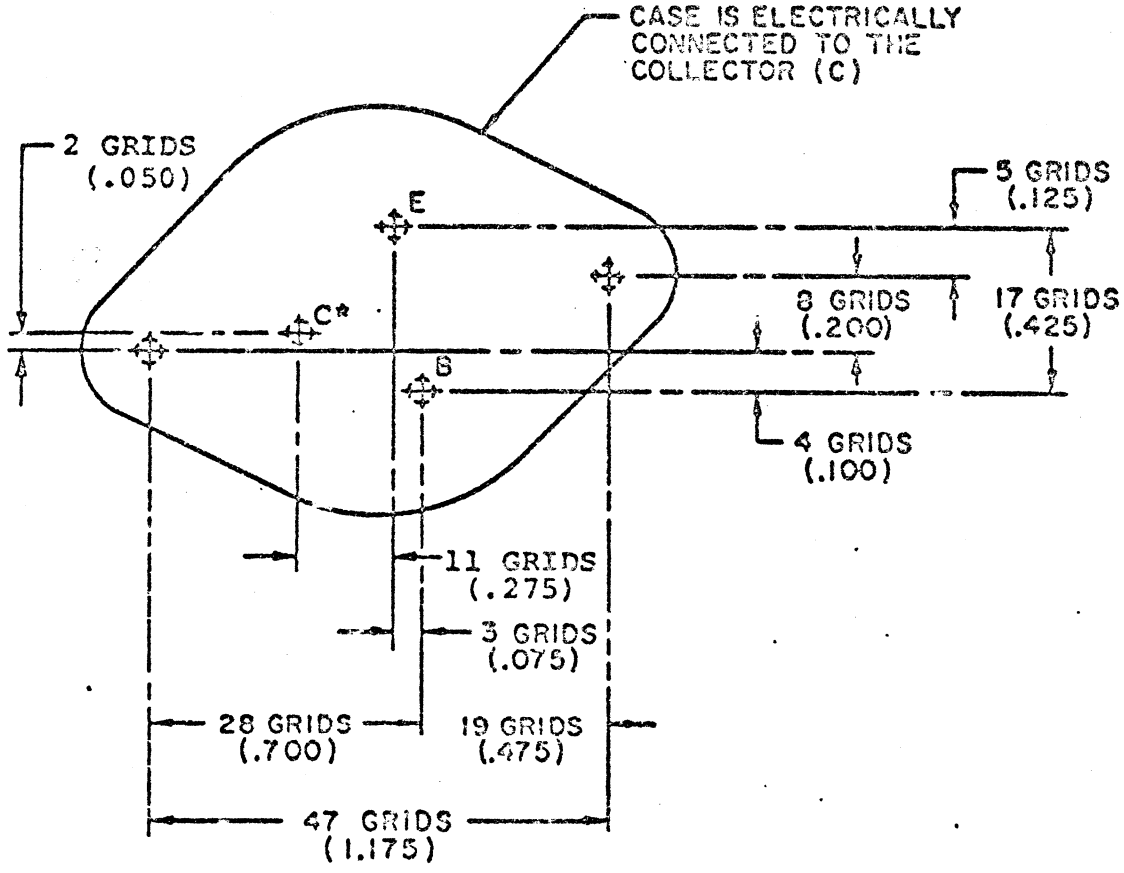
RELATIONSHIPS (Cont'd)

NOTE: Dimensions "A" and "B" as shown maintain a .375 relationship. These dimensions will be altered as the components are positioned higher or lower on the grid, while still maintaining the minimum physical placement. As dimension "B" is increased .025 dimension "A" will decrease .025, by increasing dimension "A" .025 dimension "B" will decrease .025.

ARTWORKS

All circuit connections will be made on the solder side of the card. No circuit lines or lands are allowed under the transistor on the component side of the card.

The following illustration shows the proper grid arrangement for the emitter, base and collector leads and mounting holes.

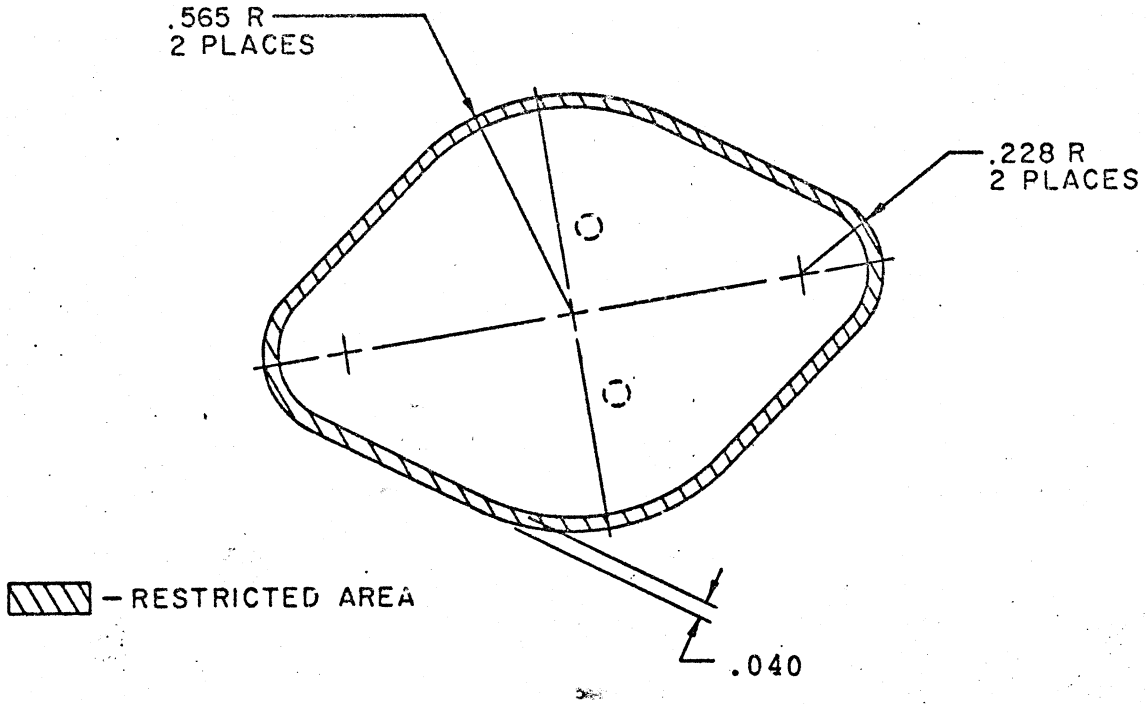


TOP VIEW

* Physical outlines 2T03F1 only.

SEQUENCE EFFECT

The following illustration shows the TO3 Transistor restricted area for all other adjacent components.



TOP VIEW

HAND ASSEMBLY

All TO-3 Transistors are hand assembled.

PROCESS INFORMATION

The TO-3 Transistor emitter and base leads are not to be bent in any way. The collector leads and stud of the 3 & 4 leaded packages will be clinched.

PLANNING

No semi-automatic insertion equipment is contemplated.

CARD LAYOUT GROUND RULES

IBM Division Engineering Practice

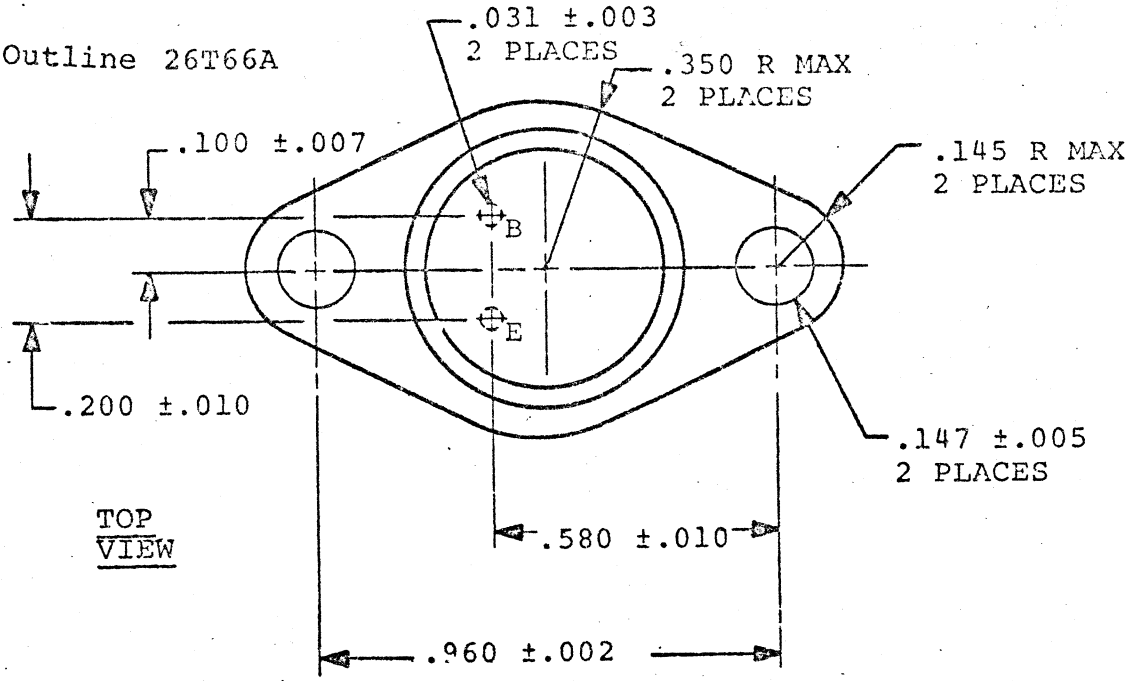
TO-66 TRANSISTORS

DESCRIPTION

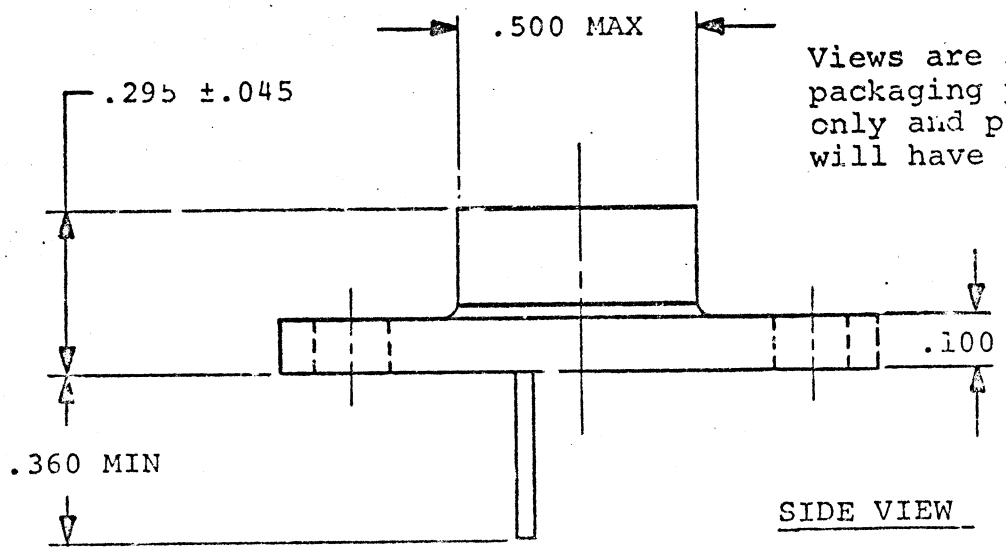
Devices within TO-66 packages have metal cans and headers. This package is a two leaded component. The package is electrically hot. The assembly drawing code is "Q".

PACKAGE

Physical Outline 26T66A



TOP VIEW

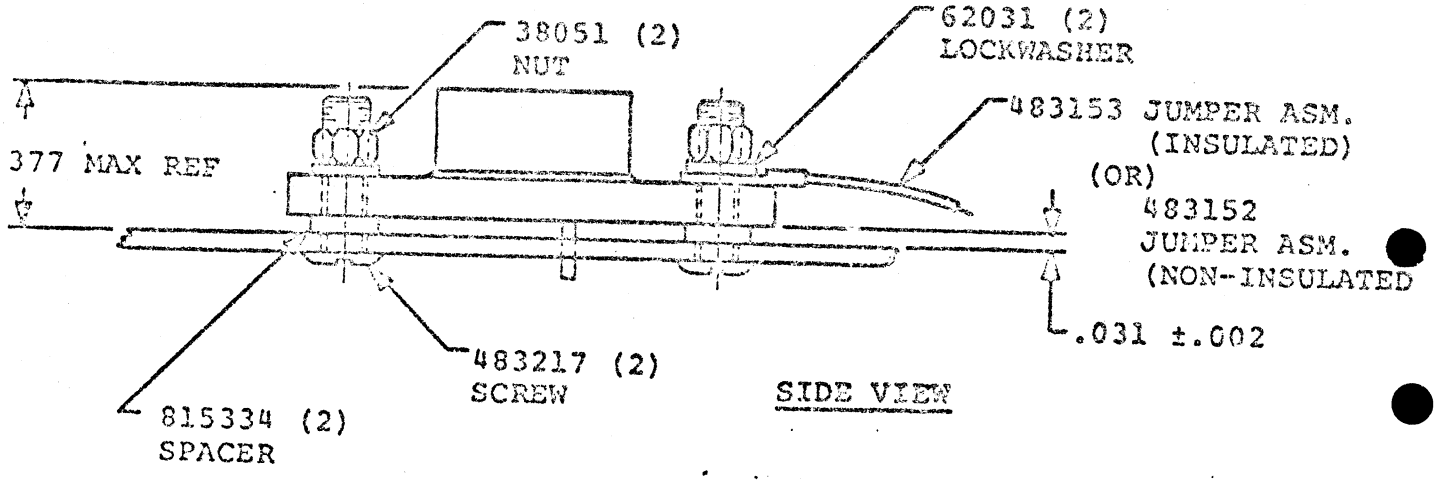


SIDE VIEW

Views are shown for packaging purposes only and part drawings will have precedence.

REQUIREMENTS

The following illustration shows the proper assembly technique and hardware required for mounting TO-66 Transistors.



Note Code "AR" will be required for TO-66 Transistors. This note code will appear on the component view and in the note code field on the assembly drawing. For the proper wording of the "AR" note see note code 1C in the note code section of the component library. All hardware items shown above and on reference drawing 816013 must appear in the parts list on the assembly drawing and also in the Bill of Material. The reference drawing part number must appear as the first special component when inputting the "AR" note.

Emitter and base leads are to be mounted in "L" holes, .062±.002. These holes are to be drilled before plating (Ref. Note BA) with .066 round lands on both sides of the card. The mounting screws require .156±.002 diameter holes to be drilled after plating. (Ref. Note BB)

Note code "FH" must appear in the note code field on the assembly drawing.

Due to the hole size requirements for the leads and mounting screws TO-66 transistors cannot be used on MST card assemblies.

LIMITS

TO-66 Transistor packages with the mounting holes mounted on the "Y" axis and emitter and base leads being parallel to the "X" axis, the mounting holes and leads must be on or within the following grid locations:

1 Hi-6 & 12	X28 - 73 - 143	Y35 - 51
2 Hi-6 & 12	X28 - 73 - 143	Y35 - 111
3 Hi-12	X28 - 143	Y35 - 171

LIMITS (Cont'd)

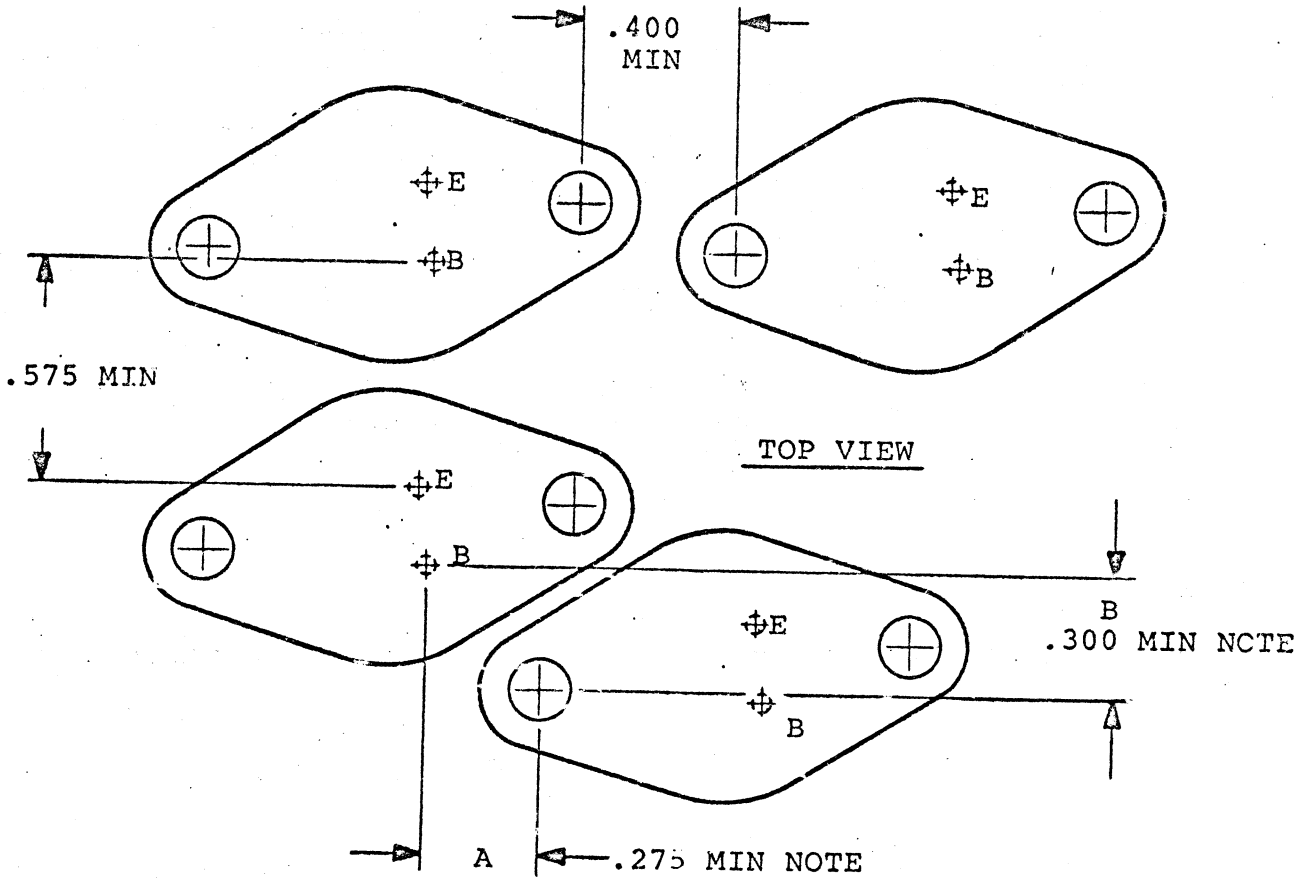
TO-66 Transistor packages with the mounting holes mounted on the "X" axis and the emitter and base leads parallel to the "Y" axis, the mounting holes and leads must be on or within the following grid locations:

1 Hi-6 & 12	X34 - 67 - 137	Y32 - 70
2 Hi-6 & 12	X34 - 67 - 137	Y32 - 117
3 Hi-12	X34 - 137	Y32 - 117

TO-66 Transistor lead size will not allow usage on MST card assemblies.

RELATIONSHIPS

The following illustration shows the physical minimum placement of TO-66 Transistors:



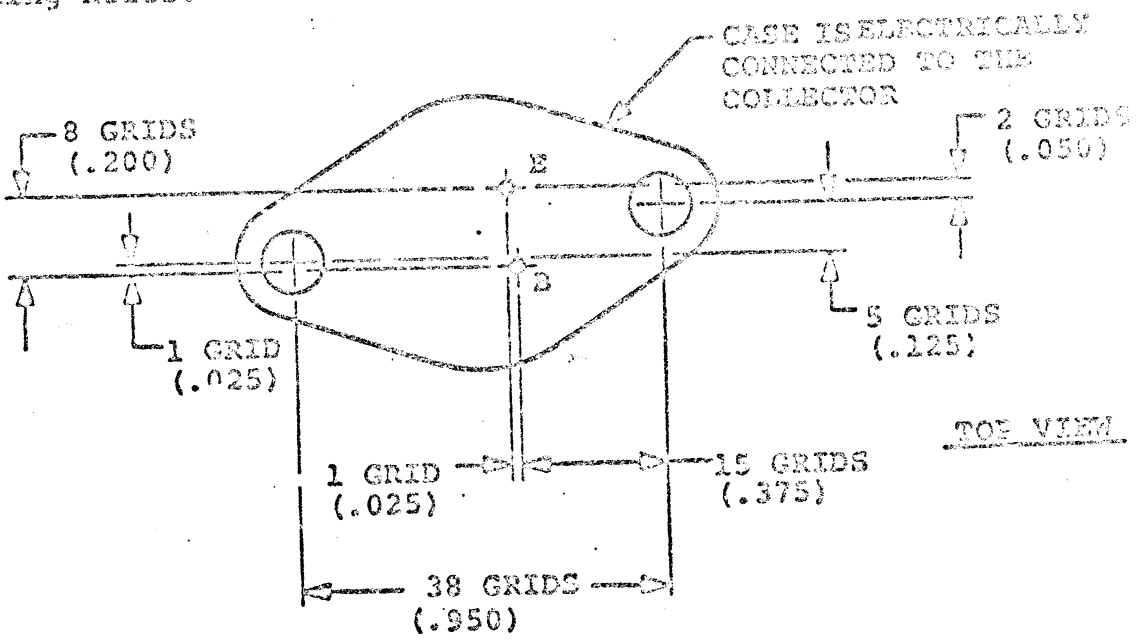
RELATIONSHIPS (Cont'd)

NOTE: Dimension "A", .275 and dimension "B", .300 will be altered as the components are positioned higher or lower on the grid, while still maintaining the minimum physical placement. As dimension "B" is increased by .025 dimension "A" will decrease by .025, by decreasing dimension "A" .025 dimension "B" will decrease .025.

ARTWORKS

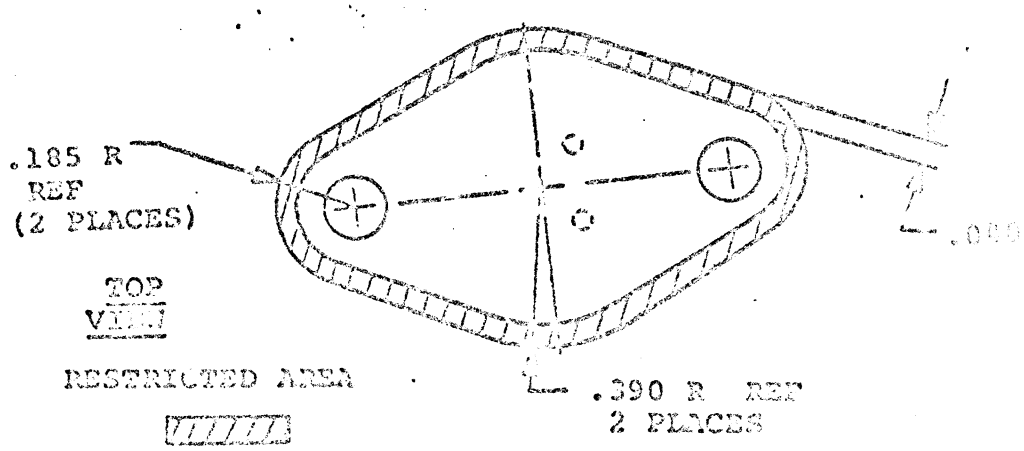
All circuit connections will be made on the solder side of the card. No circuit lines or lands are allowed under the transistor on the component side of the card.

The following illustration shows the proper grid arrangement for the emitter, base and mounting holes:



SEQUENCE EFFECT

The following illustration shows the TO-66 restricted area for all other adjacent components:



HAND ASSEMBLY

All TO-66 Transistors are hand assembled prior to wave soldering and after all other components less than .377 high.

PROCESS INFORMATION

The TO-66 Transistor emitter and base leads are not to be bent in any way.

PLANNING

No semi-automatic insertion equipment is contemplated.

IBM Division Engineering Practice

POTENTIOMETER .500 SQUARE

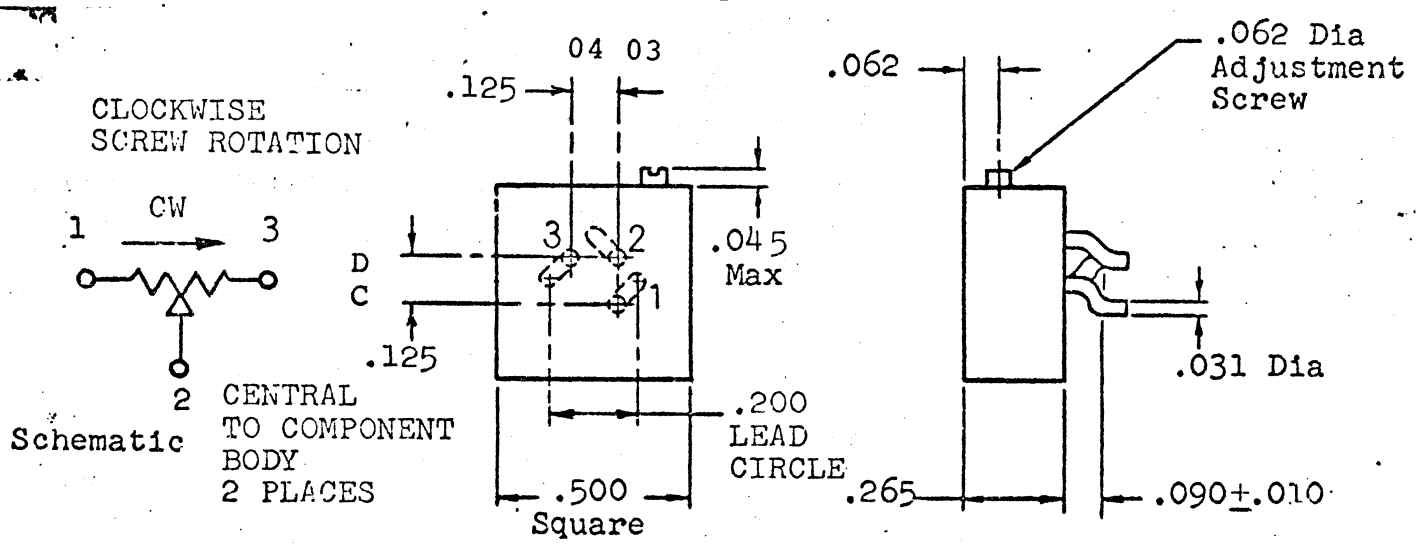
DESCRIPTION

.500 square potentiometers have three leads, are encased in an electrically floating case, and must be considered as uninsulated components. Trimming is achieved by means of an adjustment screw located along one edge of the component.

Assembly drawing code is "R".

PACKAGE

There is no physical outline code for this component. The leads as purchased are on a .200" lead circle diameter but they are formed and skewed to a .177" lead circle diameter before component insertion to fit the .125" hole pattern and to provide stand-off.



POTENTIOMETER .312 SQUARE

REQUIREMENTS

When it is desired to set the adjustment screw on the potentiometer at the final card test line, it should be called out in the card test specification. The epoxy to be used is IBM Material Code 1219 only. IBM Material Code 1219 is Moleom 21 - IBM part number 483002.

Leads of this component must be mounted in:

"J" .040 holes for SLT/SLD
.040 holes for MST 1 & 2
.031 holes for MST 4

Note codes to be as follows:

Note Code NA will be required with this component. This Note Code will appear on the component view and in the Note Code field on the assembly drawing. All potentiometer part numbers in the component library will reflect Note Code NA for library use and for manufacturing routings.

CMT CODING

Potentiometer .312 square must be coded in the "A" direction, with pins 1 and 2 parallel to the "X"-"X" axis and pins 2 and 3 parallel to the "Y"-"Y" axis. This orientation places the adjustment screw facing the left-hand edge of the board. This potentiometer must be coded as a 5x5 component with lead codes as follows:

Lead 1 - C03
2 - D03
3 - D04

LIMITS

On a standard .125" hole pattern, leads must be on or within the following X and Y grids:

Potentiometer Lead Numbers

	1	2	3
SLT/SLD	1 Hi 6 - 12 Y 38 - 58 X 28 - 73 - 143	Y 43 - 63 X 28 - 73 - 143	Y 43 - 63 X 23 - 68 - 138

LIMITS (Cont'd)

SLT/SLD	1	2	3
2-Hi 6 - 12			
	Y 098 - 108	Y 103 - 113	Y 103 - 113
	X 33 - 73 - 143	X 33 - 73 - 143	X 28 - 68 - 138
SLT/SLD			
3-Hi 12			
	Y 158 - 168	Y 163 - 173	Y 163 - 173
	X 33 - 143	X 33 - 143	X 28 - 138
MST			
2-Hi 1,2 & 4 wide			
	Y R - T	Y S - U	Y S - U
	X 02 - 10 - 24 - 52	X 03 - 10 - 24 - 52	X 03 - 11 - 25 - 53

On a Random hole pattern, leads must be on or within the following X and Y grids:

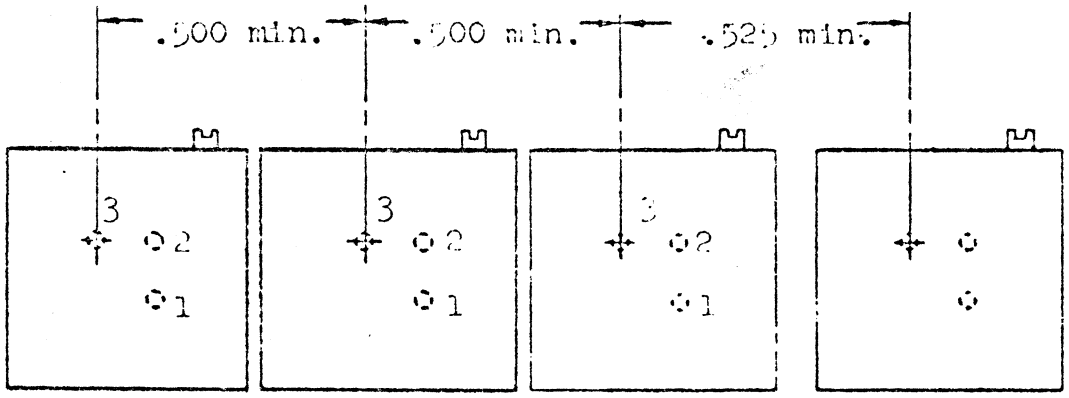
Potentiometer Lead Numbers

	1	2	3
SLT/SLD			
1-Hi 6 - 12			
	Y 38 - 50	Y 43 - 55	Y 43 - 55
	X 33 - 73 - 143	X 33 - 73 - 143	X 28 - 68 - 138
2-Hi 6 - 12			
	Y 098 - Y 110	Y 103 - 115	Y 103 - 115
	X 33 - 73 - 143	X 33 - 73 - 143	X 28 - 68 - 138
3-Hi 12			
	Y 158 - 170	Y 163 - 175	Y 163 - 175
	X 33 - 143	X 33 - 143	X 28 - 138

Potentiometers should be mounted as close to the left-hand edge of card as possible within the specified limits. Adjustment screw must face left-hand edge of card.

RELATIONSHIPS

Even though the maximum dimension of this component could theoretically be .515" square, manufacturing engineering will accept the following placement of three adjacent potentiometers based on practical experience.

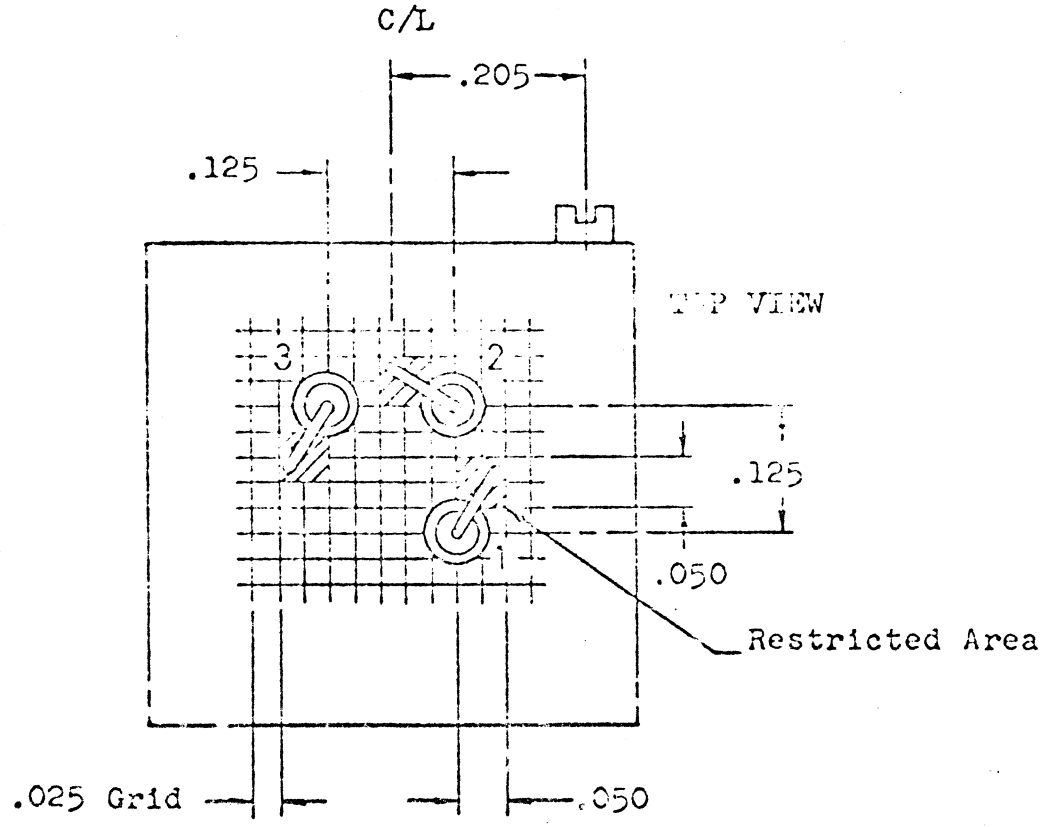


TOP VIEW

ARTWORKS

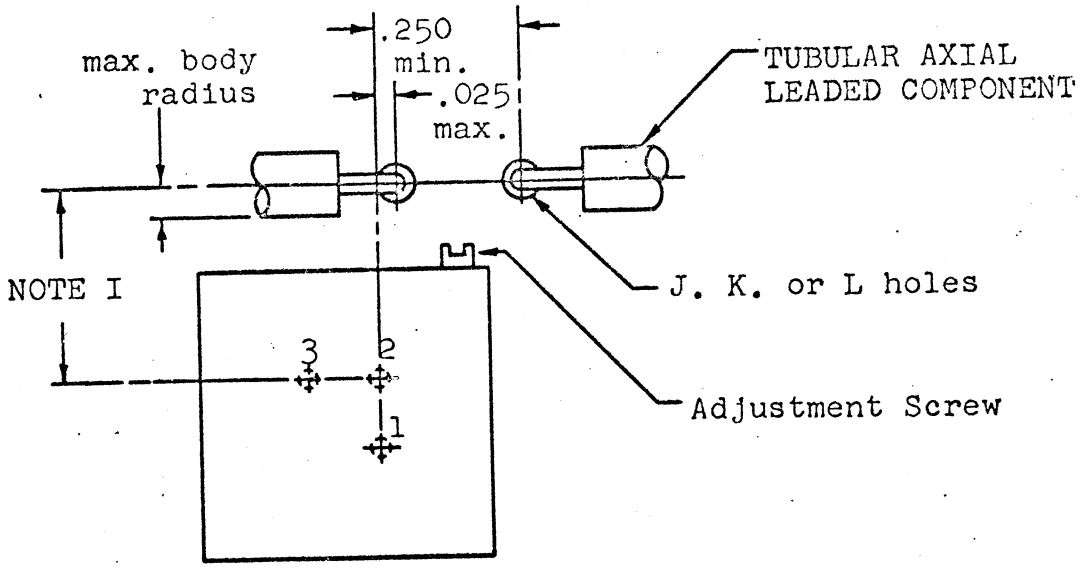
There are no restrictions on the back artworks.

The following view shows the restricted area which must apply to the front artwork unless the land and restricted area are electrically common.



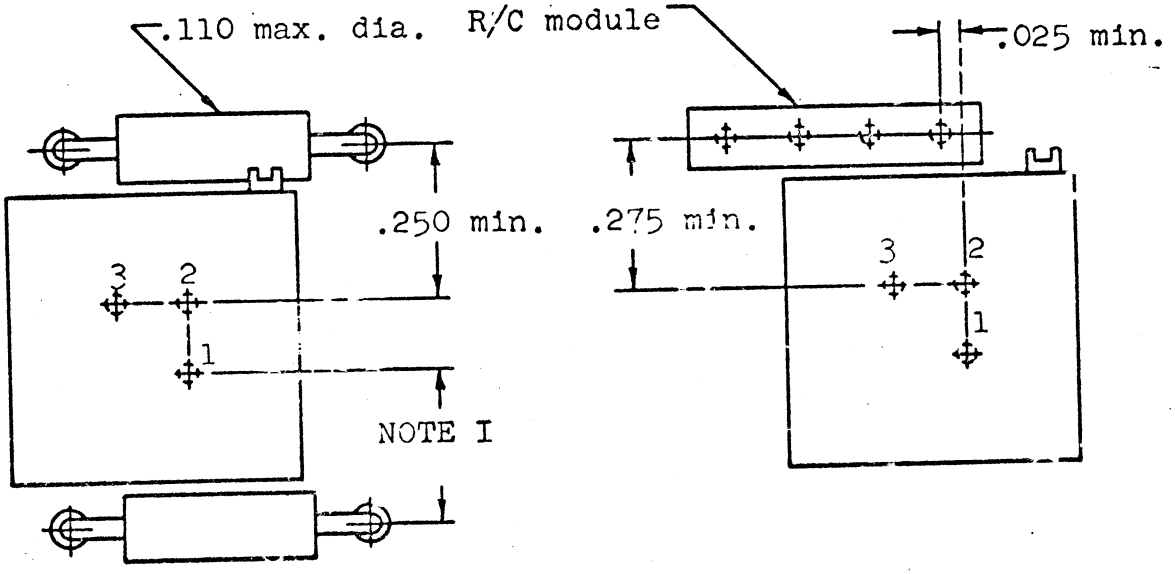
SEQUENCE EFFECT

If layout considerations require certain components to be mounted between the left-hand card edge and the potentiometer the following dimensions must be observed to permit access to the adjustment screw.



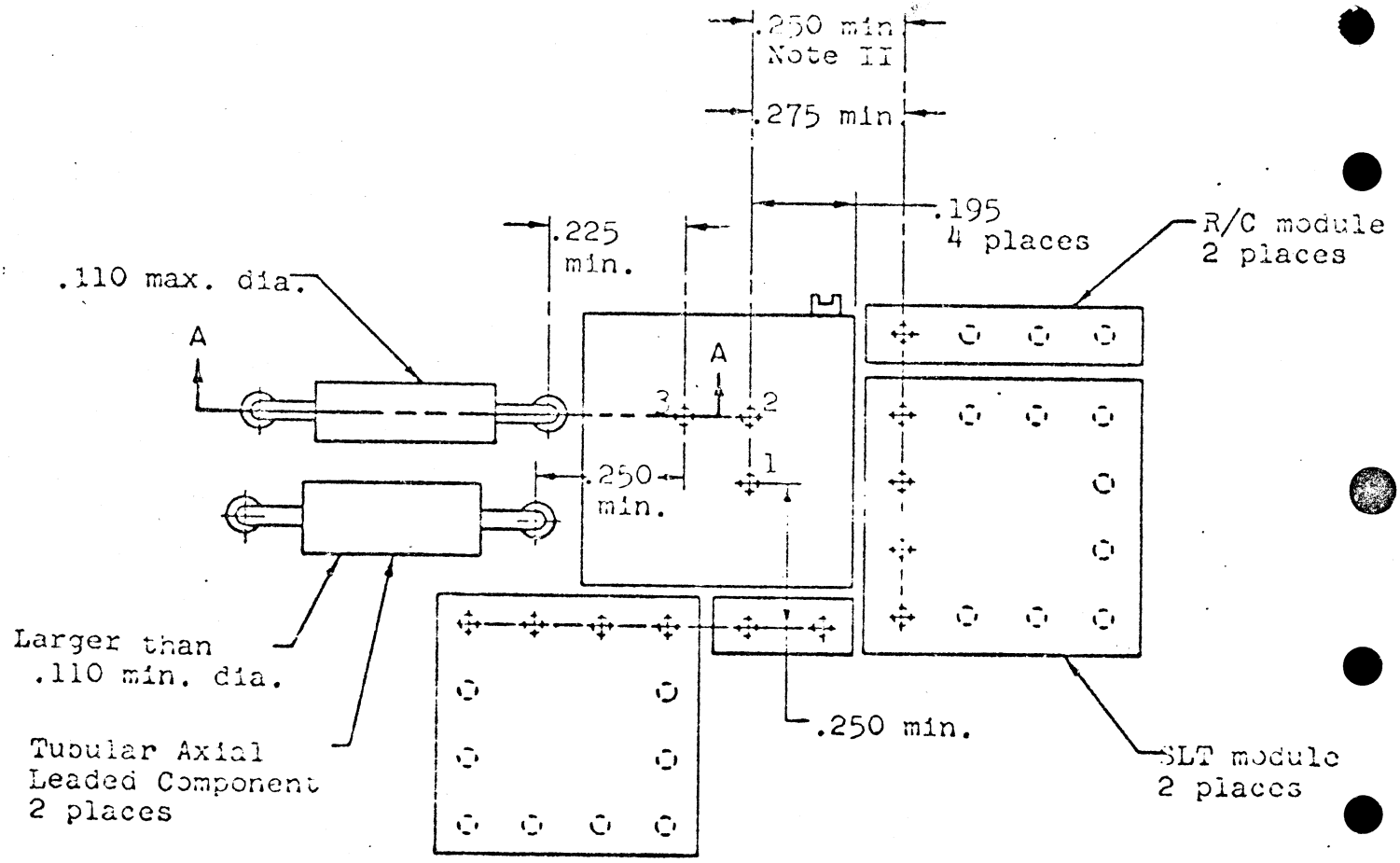
NOTE I
.195 min. plus the
max. body radius

TOP VIEWS



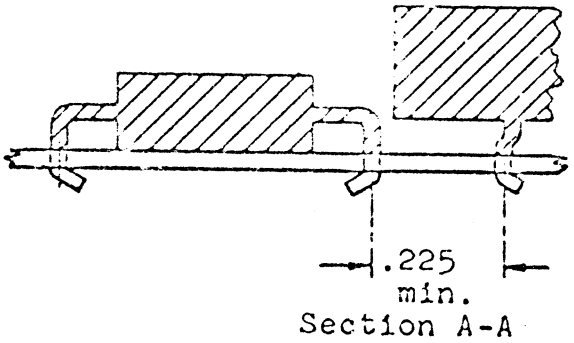
SEQUENCE EFFECTS (CONT'D)

Components mounted adjacent to square potentiometers must comply with the following minimum clearance. Clearance from all other uninsulated or electrically hot components must be a minimum of .035" (.015" electrical clearance plus an additional .020" manufacturing tolerance). Clearance from insulated components must therefore be a minimum of .020.



Top Views

NOTE II:
SLT and/or R/C modules cannot be mounted on the direct opposite sides of the potentiometer on the .250 min. dimension.



Section A-A

HAND ASSEMBLY

These components will be manually assembled during the "manual assembly of non-wettables" operation.

PROCESS INFORMATION

Components are not mechanically secured to the card by their leads.

Leads are hand soldered.
Tooling for lead forming will always be employed.

PLANNING

No automatic or semi-automatic insertion equipment is contemplated.

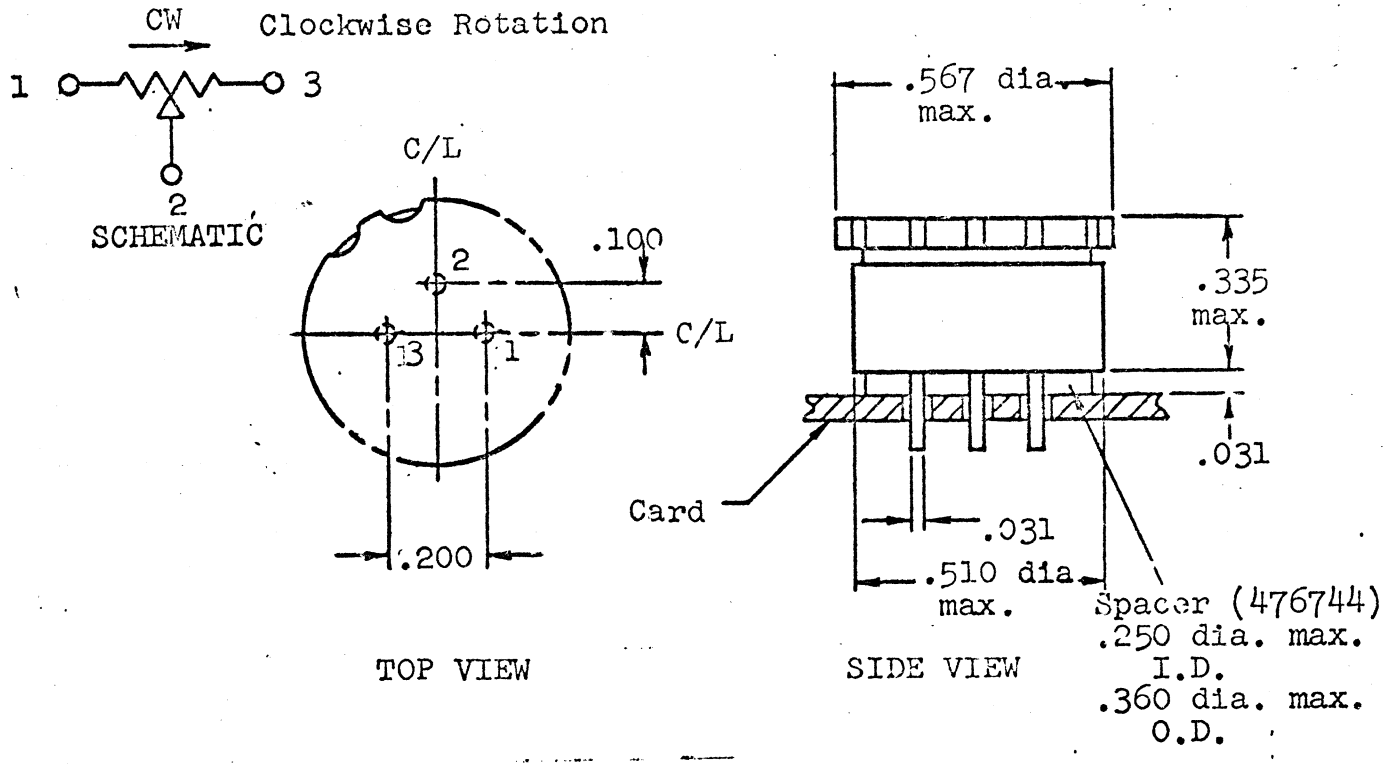
DESCRIPTION

.567" diameter potentiometers have 3 leads and are encased in an electrically insulated case. Trimming is achieved by means of a serrated disc located on top of the component.

Assembly drawing code is "R."

PACKAGE

There is no physical outline code for this component. The leads as purchased are on a .200" pin diameter circle and are not formed prior to assembly to card. They are assembled to the .125" grid pattern, as shown under SEQUENCE EFFECT.



Views shown are for layout purposes only and the part drawing shall have precedence.

REQUIREMENTS

When it is desired to set the adjustment disc on the Potentiometer at the Final Card Test Line, it should be called out in the Card Test Specification. The Epoxy to be used is IBM Material Code 1219 only. IBM Material Code 1219 is Moleom 21-IBM part number 483002.

Leads of this component must be mounted in:

"J" .040 holes for SLT/SLD
.040 holes for MST 1&2

This Potentiometer cannot be mounted on MST-4 assemblies because of its .031 maximum lead diameter.

Note codes must be as follows:

Note Code NB will be required with this component. This Note Code will appear on the component view and in the Note Code field on the assembly drawing. All potentiometers of this type will reflect Note Code NB in the component library and for use in manufacturing routing.

CMT CODING

This Potentiometer, with required Spacer 476744, must be coded in the "A" direction only with pins "2" and "3" parallel to the "Y" - "Y" axis and pin 1 toward the right-hand edge of the card. This Potentiometer must be coded as a 6x6 component with lead codes as follows:

Lead 1 - C03
2 - D03
3 - D04

LIMITS

On a standard .125" hole pattern, leads must be on or within the following X and Y grids.

SLT/SLD	1-Hi 6 - 12	X 33 - 68 - 138	Y 38 - Y 53
	2-Hi 6 - 12	X 33 - 68 - 138	Y 93 - Y 113
	3-Hi 12	X 33 - 138	Y 153 - Y 173
MST	2-Hi x 1,2 & 4 wide	X 03 - 10 - 24 - 52	Y Q - U

LIMITS (CONT'D)

On a Random hole pattern, leads must be on or within the following X and Y grids:

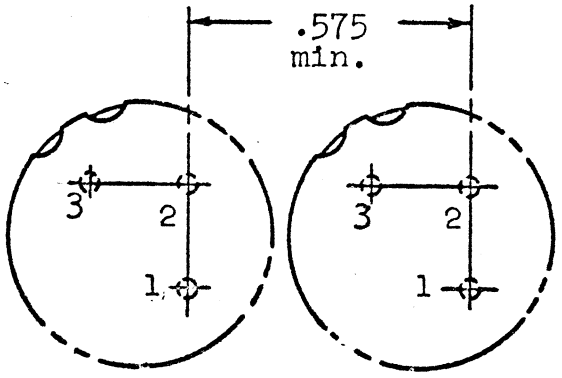
SLT/SLD

1-Hi 6 - 12	X 30 - 71 - 141	Y 38 - 56
2-Hi 6 - 12	X 30 - 71 - 141	Y 93 - 116
3-Hi 12	X 30 - 141	Y 153 - 176

Potentiometers should be mounted as close to the left-hand edge as possible within the specified limits, oriented in any one of the four quadrants.

RELATIONSHIPS

The following illustration shows the minimum placement of adjacent round potentiometers.



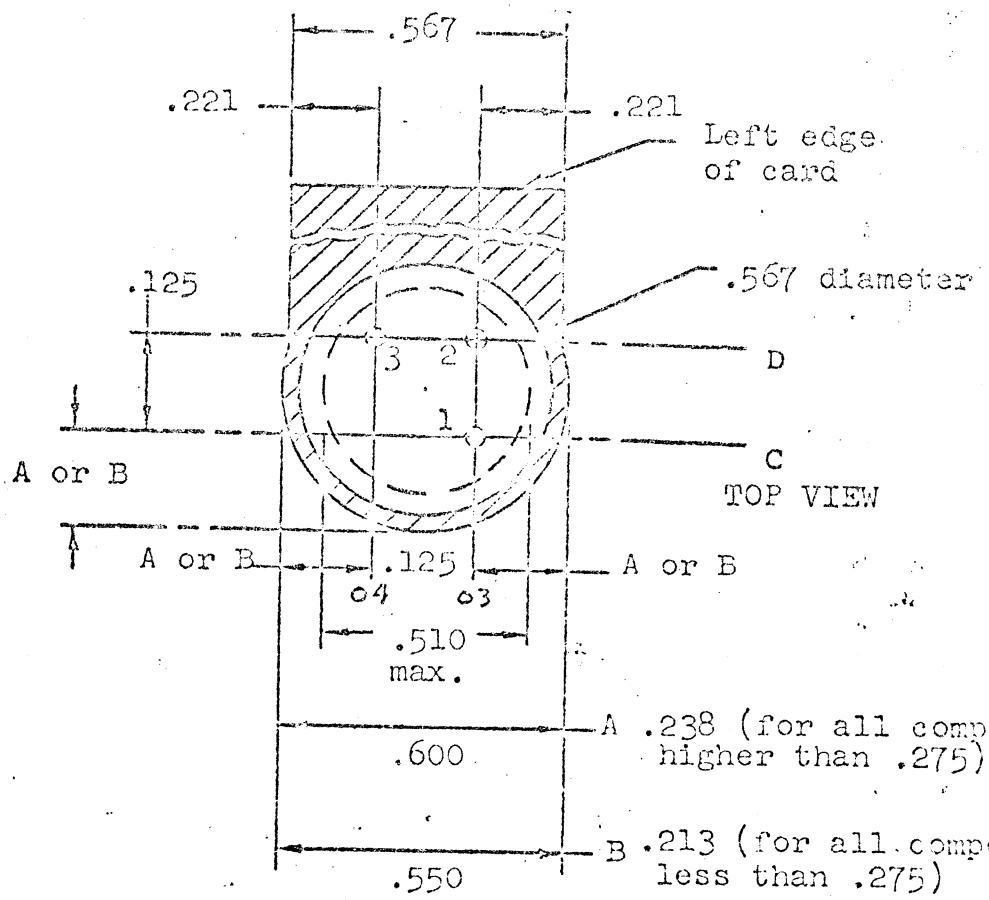
TOP VIEW

ARTWORK

There are no restrictions for front or back artwork.

SEQUENCE EFFECT

The shaded areas must be clear of all other components according to the dimensions shown. The exception is that a component .150" maximum height is permitted between the left card edge and the potentiometer.



HAND ASSEMBLY

These components will be manually assembled during the "manual assembly of non-wettables" operation.

PROCESS INFORMATION

Components are not mechanically secured to the card by their leads.

Leads are hand soldered and a spacer is used. No lead forming tools are used.

PLANNING

No automatic or semi-automatic insertion equipment is contemplated.

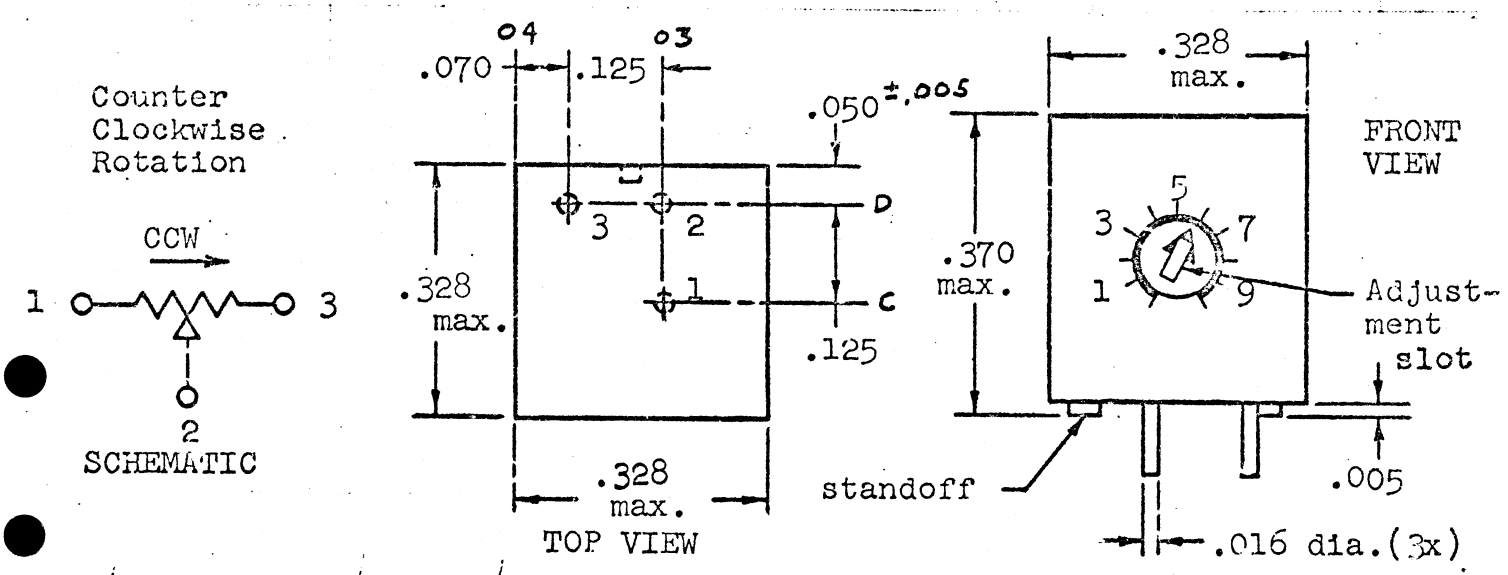
DESCRIPTION

.312 NDM square potentiometers have 3 leads and are encased in an electrically insulated case. Trimming is achieved by means of an adjustment slot situated on one face.

Assembly drawing code is "R."

PACKAGE

There is no physical outline code for this component. The leads as purchased are on .125 centers, and therefore, fit the .125 grid pattern.



Views shown are for layout purposes only and the part drawing shall have precedence.

REQUIREMENTS

When it is desired to set the adjustment screw on the potentiometer at the final card test line, it should be called out in the card test specification. The epoxy to be used is IBM Material code 1219 only. IBM Material code 1219 is Moleom 21 - IBM part number 483002.

Leads of this component must be mounted in:

"J" .040 holes for SLT/SLD
.040 holes for MST 1&2
.031 holes for MST 4

Note codes are to be as follows:

Note Code NA will be required with this component. This Note Code will appear on the component view and in the Note Code field on the assembly drawing. All potentiometer part numbers in the component library will reflect Note Code NA for library use and for manufacturing routings.

CMT CODING

This rectangular potentiometer must be coded in the "A" direction, with pins 1 and 3 parallel to the "X"-"X" axis. This orientation places the adjustment screw facing the left hand edge of the board. This potentiometer must be coded as a 3x2 component with lead codes as follows:

Lead 1 - C01
2 - B02
3 - A01

LIMITS

On a standard .125" hole pattern leads must be on or within the following X and Y grids:

Potentiometer Lead Numbers

	1	2	3
SLT/SLD 1-Hi	6 - 12		
	Y 48 - 58	Y 43 - 53	Y 38 - 48
	X 28 - 78 - 148	X 23 - 73 - 143	X 28 - 78 - 148

LIMITS (Cont'd)

Potentiometer Lead Numbers

	1	2	3
SLT/SLD 2-Hi 6 - 12	Y 98 - 118 X 28 - 73 - 143	Y 103 - 123 X 28 - 73 - 143	Y 103 - 123 X 23 - 68 - 138
SLT/SLD 3-Hi 12	Y 158 - 178 X 28 - 73	Y 163 - 183 X 28 - 73 - 143	Y 163 - 183 X 23 - 68 - 138
MST 2-Hi x 1,2&4 wide	Y R - V X 02 - 11 - 25 - 53	Y S - W X 02 - 11 - 25 - 53	Y S - W X 03 - 12 - 26 - 54
MST 3-Hi x 2&4 wide	Y 4 - 8 X 02 - 25 - 53	Y 5 - 9 X 02 - 25 - 53	Y 5 - 9 X 03 - 26 - 54

On a random hole pattern, leads must be on or within the following X and Y grids:

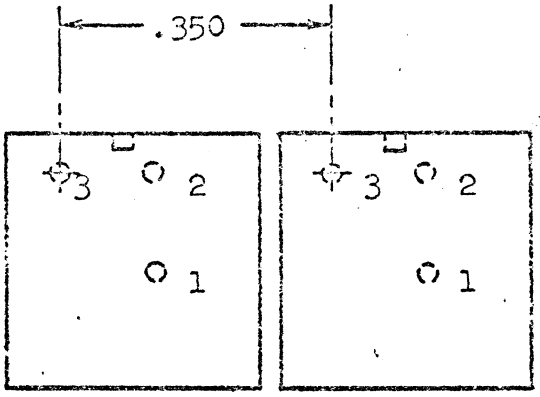
Potentiometer Lead Numbers

	1	2	3
SLT/SLD 1-Hi 6 - 12	Y 38 - 58 X 28 - 76 - 146	Y 43 - 63 X 28 - 76 - 146	Y 43 - 63 X 23 - 71 - 141
2-Hi 6 - 12	Y 98 - 118 X 28 - 76 - 146	Y 103 - 123 X 28 - 76 - 146	Y 103 - 123 X 23 - 71 - 141
3-Hi 12	Y 158 - 178 X 28 - 76 - 146	Y 163 - 183 X 28 - 76 - 146	Y 163 - 183 X 23 - 71 - 141

Potentiometers should be mounted as close to the left hand edge of card as possible within the specified limits. Adjustment slot must face the left hand edge of card.

RELATIONSHIPS

The following illustration shows the minimum placement of adjacent potentiometers.



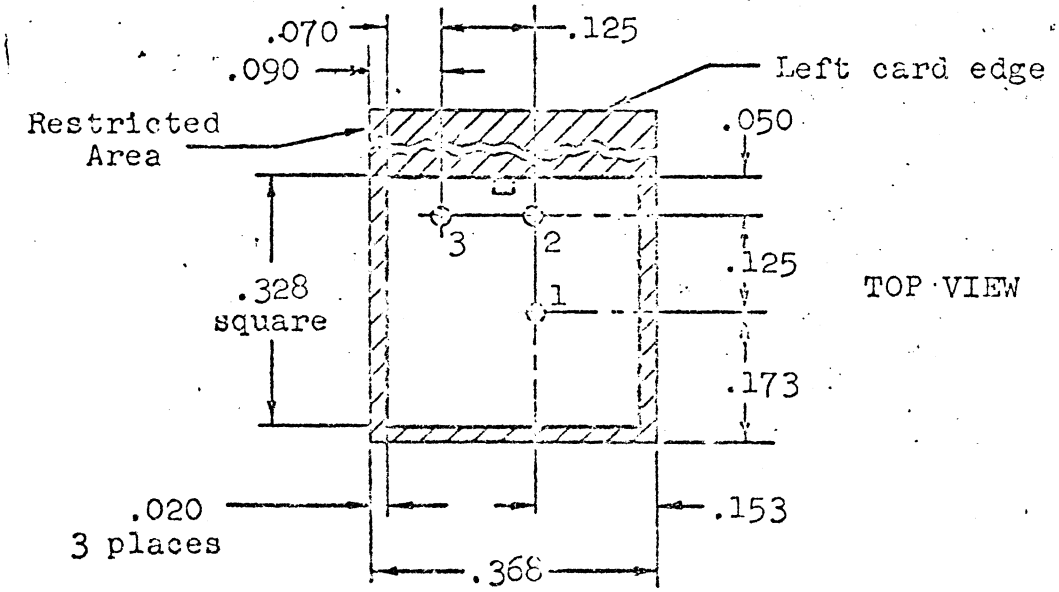
TOP VIEW

ARTWORKS

There are no artwork restrictions associated with the usage of this component.

SEQUENCE EFFECT

To allow for manufacturing requirements, the .020" restricted area must be clear of all other adjacent components. The exception is that a component .125 maximum height is permitted between the left card edge and the potentiometer.



TOP VIEW

HAND ASSEMBLY

These components will be manually assembled during the "manual assembly of non-wettables" operation.

PROCESS INFORMATION

Components are not mechanically secured to the card by their leads.

Leads are hand soldered.

Standoffs are for soldering purposes only.

PLANNING

This component type has been formally released.

No automatic or semi-automatic insertion equipment is contemplated.

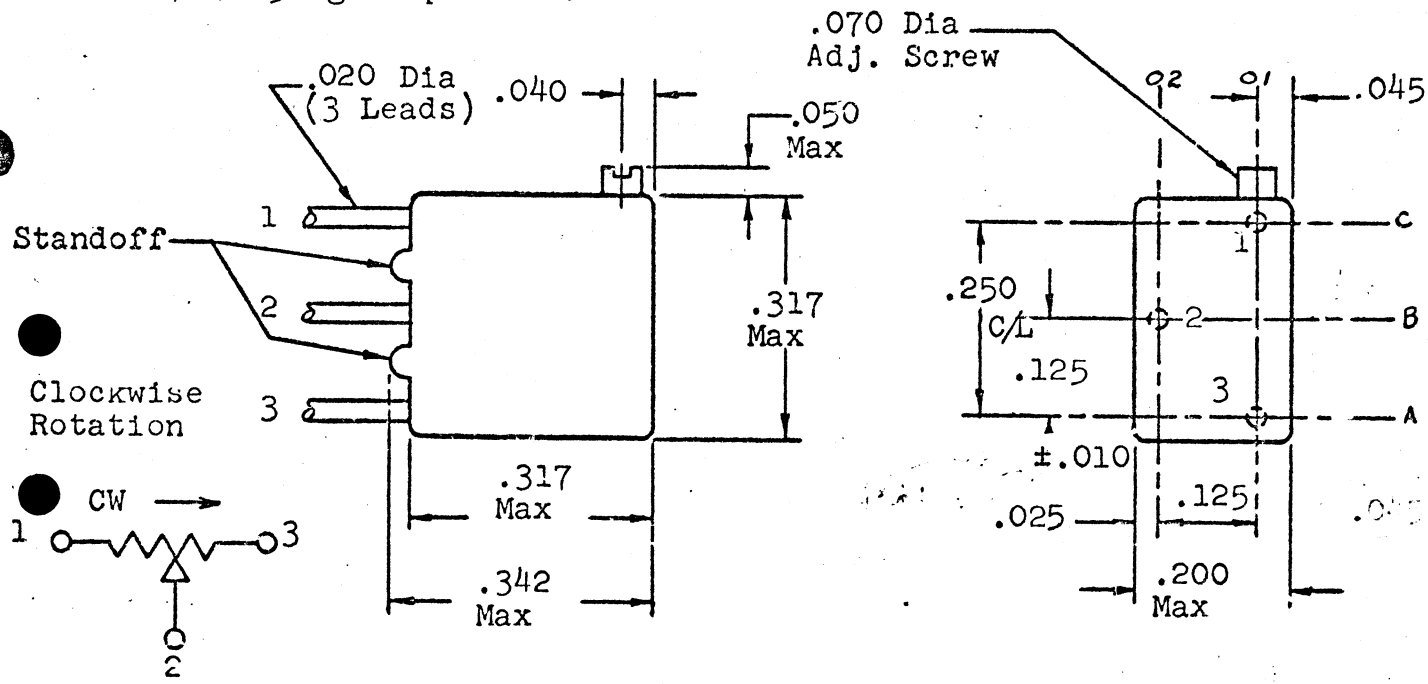
DESCRIPTION

.200 x .312 rectangular pots have 3 leads and are encased in an electrically insulated case. Trimming is achieved by means of an adjustment screw located along one edge of the component.

Assembly drawing code is "R."

PACKAGE

There is no physical outline code for this component. The leads as purchased are on .125 centers, and therefore, fit the standard .125" grid pattern.



Schematic

Side View

Top View

Views shown are for layout purposes only and the part drawing shall have precedence.

POTENTIOMETER .312 SQUARE

REQUIREMENTS

When it is desired to set the adjustment screw on the potentiometer at the final card test line, it should be called out in the card test specification. The epoxy to be used is IBM Material Code 1219 only. IBM Material Code 1219 is Moleom 21 - IBM part number 483002.

Leads of this component must be mounted in:

"J" .040 holes for SLT/SLD
.040 holes for MST 1 & 2
.031 holes for MST 4

Note codes to be as follows:

Note Code NA will be required with this component. This Note Code will appear on the component view and in the Note Code field on the assembly drawing. All potentiometer part numbers in the component library will reflect Note Code NA for library use and for manufacturing routings.

CMT CODING

Potentiometer .312 square must be coded in the "A" direction, with pins 1 and 2 parallel to the "X"-"X" axis and pins 2 and 3 parallel to the "Y"-"Y" axis. This orientation places the adjustment screw facing the left-hand edge of the board. This potentiometer must be coded as a 5x5 component with lead codes as follows:

Lead 1 - C03
2 - D03
3 - D04

LIMITS

On a standard .125" hole pattern, leads must be on or within the following X and Y grids:

Potentiometer Lead Numbers

	1	2	3
SLT/SLD	1 Hi 6 - 12		
	Y 38 - 58	Y 43 - 63	Y 43 - 63
	X 28 - 73 - 143	X 28 - 73 - 143	X 23 - 68 - 138

LIMITS (cont'd)

Potentiometer Lead Numbers

	1	2	3
2-Hi 6 - 12			
	Y 108 - 118	Y 103 - 113	Y 98 - 108
	X 28 - 78 - 148	X 23 - 73 - 143	X 28 - 78 - 148
3-Hi 12			
	Y 168 - 178	Y 163 - 173	Y 158 - 168
	X 28 - 148	X 23 - 143	X 28 - 148
MST 2 Hi x 1,2&4 wide			
	Y T - V	Y S - U	Y R - T
	X 01 - 11 - 25 - 53	X 02 - 12 - 26 - 54	X 01 - 11 - 25 - 53
MST 3 Hi x 2&4 wide			
	Y 6 - 8	Y 5 - 7	Y 4 - 6
	X 01 - 25 - 53	X 02 - 26 - 54	X 01 - 25 - 53

On a Random hole pattern, leads must be on or within the following X and Y grids:

Potentiometer Lead Numbers

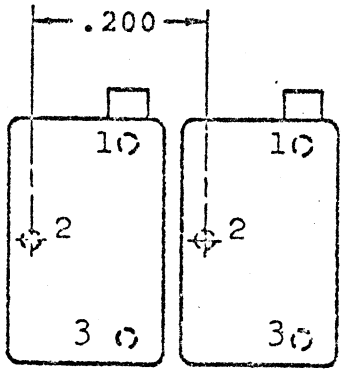
	1	2	3
SLT, SD 1-Hi 6 - 12			
	Y 48 - 61	Y 43 - 56	Y 38 - 51
	X 28 - 78 - 148	X 23 - 73 - 143	X 28 - 78 - 148
2-Hi 6 - 12			
	Y 108 - 121	Y 103 - 116	Y 98 - 111
	X 28 - 78 - 148	X 23 - 73 - 143	X 28 - 78 - 148
3-Hi 12			
	Y 168 - 181	Y 163 - 176	Y 158 - 171
	X 28 - 148	X 23 - 143	X 28 - 148

Potentiometers should be mounted as close to the left hand edge as possible within the specified limits. Adjustment screw must face the left hand edge of card.

POTENTIOMETER RECTANGULAR

RELATIONSHIP

The following illustration shows the minimum placement of adjacent rectangular potentiometers.



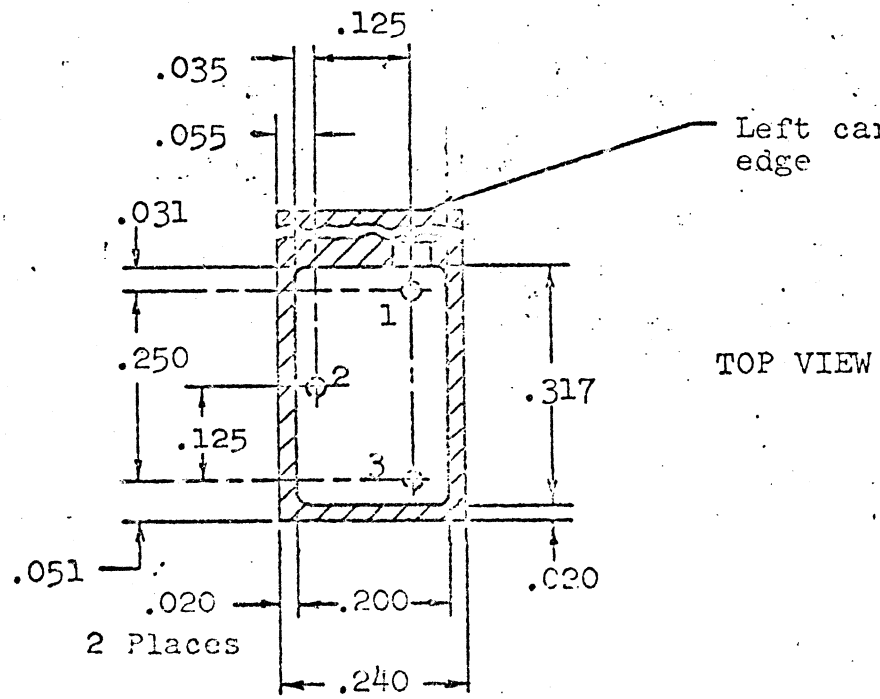
TOP VIEW

ARTWORK

There are no artwork restrictions associated with the usage of this part.

SEQUENCE EFFECT

To allow for manufacturing requirements, the .020" restricted area must be clear of all other adjacent components. The exception is that a component .200 maximum height is permitted between the left card edge and the potentiometer.



TOP VIEW

HAND ASSEMBLY

These components will be manually assembled during the "manual assembly of non-wettable" operation.

PROCESS INFORMATION

Components are not mechanically secured to the card by their leads. Leads are hand soldered. Standoffs are for soldering purposes only.

PLANNING

This component type has been formally released. No automatic or semi-automatic insertion equipment is contemplated.

IBM Division
Engineering Practice

CRYSTALS

SUPPLEMENT OF STATUS

EFFECTIVE DATE: 4/19/69

SUBJECT: Card Layout Ground Rule Status, Suffix 3, Section 14.

This section has been updated to include the crystal requirements for SLD and MST.

This update supersedes DEP 2-6230, Suffix 3, Section 14, dated 2/16/69.

REQUIREMENTS

CMT size code changed.

ARTWORKS

Restricted area defined for MST 1, 2 and 4.

DESCRIPTION

Crystals are two-leaded non-polarized devices. They are encased in an electrically floating metal case with metal standoffs and must be considered as uninsulated components. The leads are glassed in.

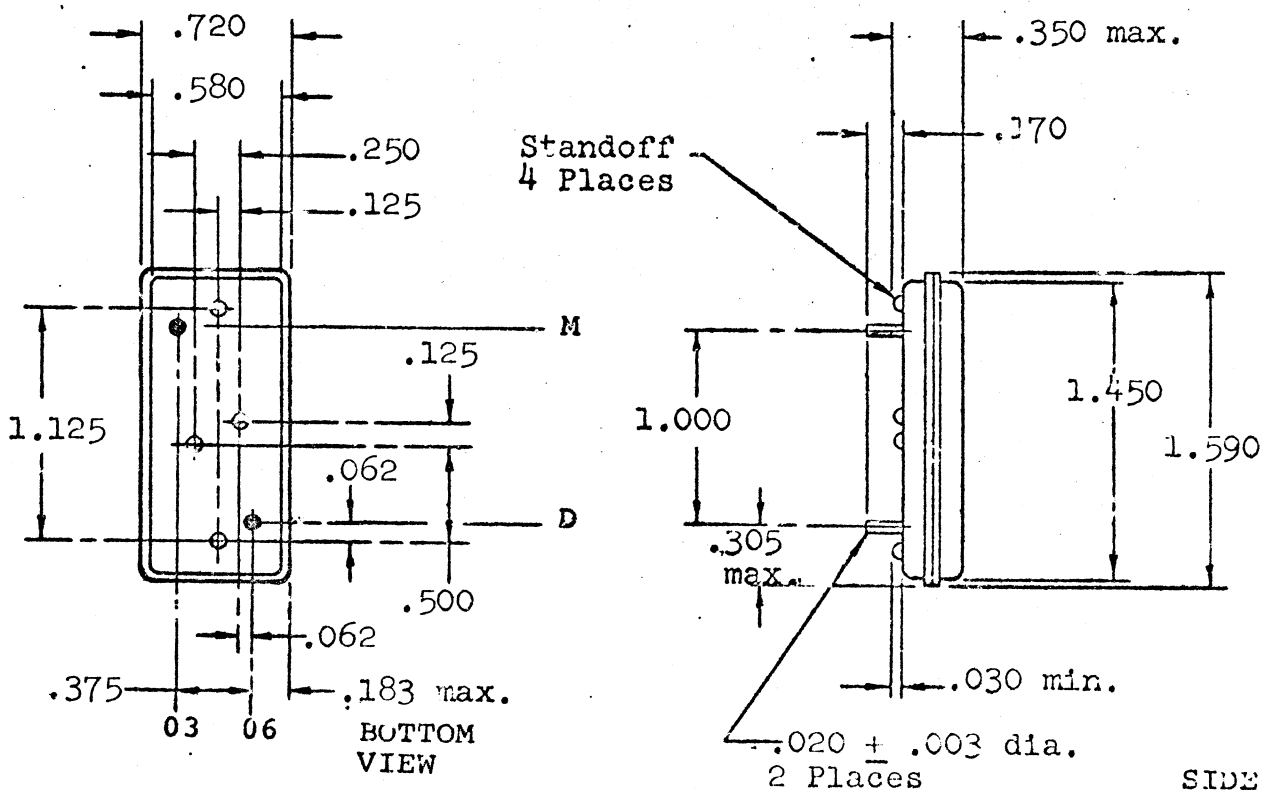
Assembly drawing code is "Y".

PACKAGE

There are 3 different package types. These are given in the following physical outline codes and are in the Component Library by physical type and are maintained by E.C. level.

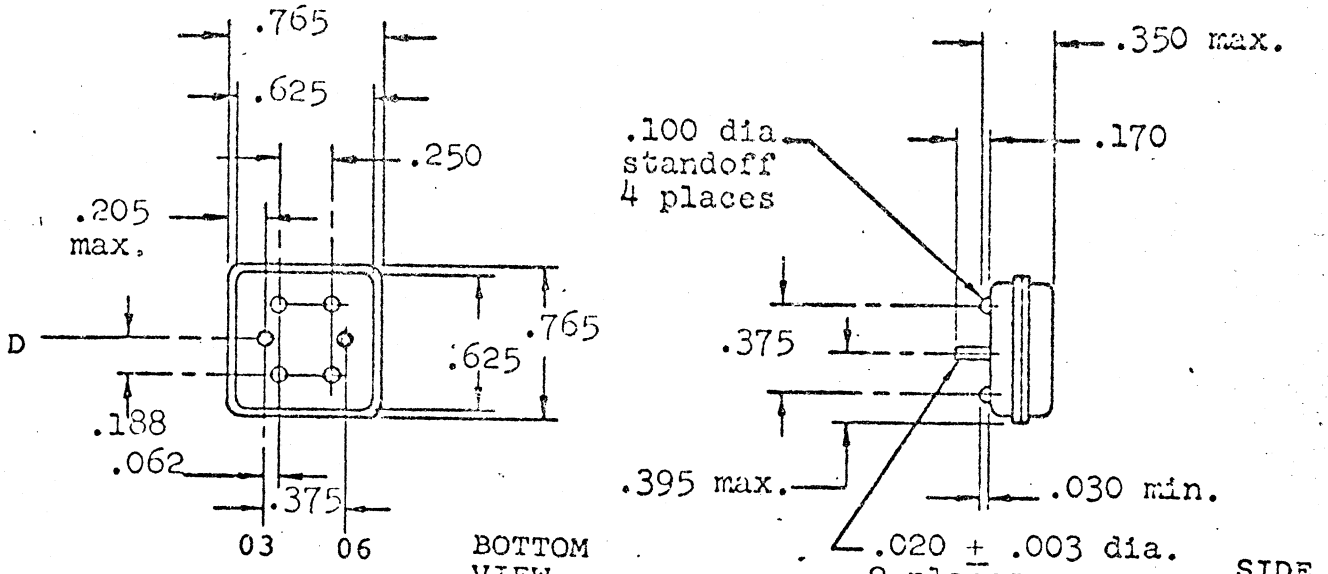
Type I - Outline code 2Y351A1
Type II - Outline code 1Y350A1
Type III - Outline code 3Y352A1

Views shown are for packaging purposes only and the part drawing shall have precedence.

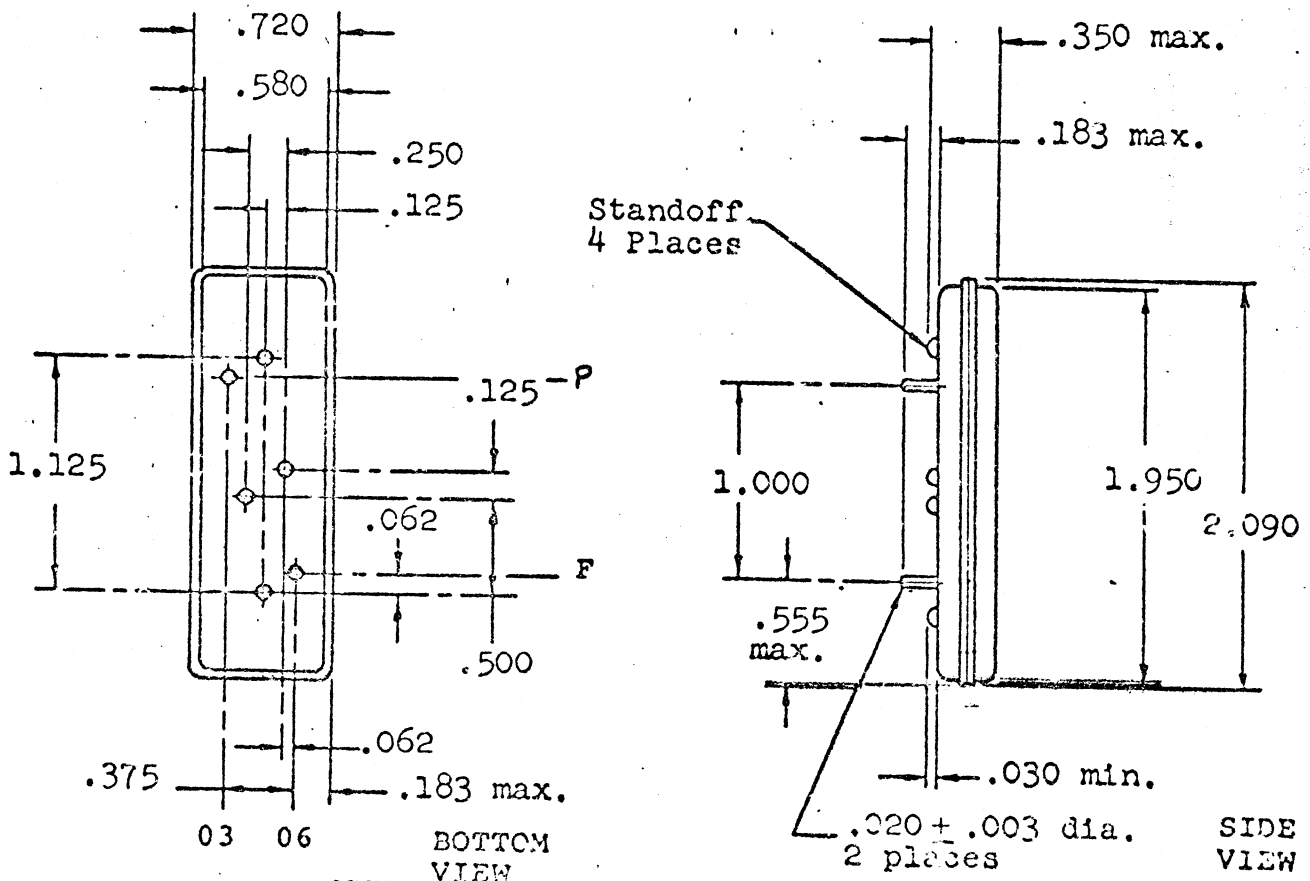


METAL PACKAGE TYPE I FOR QUARTZ CRYSTALS
(CONFORMS TO OUTLINE 2Y351A1)

PACKAGE (CONT'D)



METAL PACKAGE TYPE II FOR QUARTZ CRYSTALS
(CONFORMS TO OUTLINE 1Y350A1)



METAL PACKAGE TYPE III FOR QUARTZ CRYSTAL
(CONFORMS TO OUTLINE 3Y352A1)

REQUIREMENTS

Crystal leads must be mounted in:

"J" .040 holes for SLT/SLD
.040 holes for MST 1 & 2
.031 holes for MST 4

Normally no note code will be required with these components. Note code NC will be required for crystals with a frequency of 35-45 KHZ.

CMT CODING

Crystals type I, II, and III must be coded in the "A" direction. Leads for Type I and III will be perpendicular to the Y-Y axis, type II leads will be parallel to the Y-Y axis. Lead and size codes are as follows:

Type I - 8 x 15, D06 - M03
Type II - 8 x 7, D03 - D06
Type III - 8 x 19, F06 - P03

LIMITS

Crystal package type I placement must have one lead on and the other within or both within the following X and Y locations.

A. On a standard .125" hole pattern with the component length mounted parallel to the right edge (tabs).

SLT/SLD	1-Hi 12	X 33 - 138	Y 28 - 58
	2-Hi 12	X 33 - 138	Y 28 - 118
	3-Hi 12	X 33 - 138	Y 28 - 178
MST	2 Hi x 1,2,4 wide	X 03 - 10 - 24 - 52	Y C - V
	3 Hi x 2 & 4 wide	X 03 - 24 - 52	Y C - 8

B. On a random hole pattern with component length mounted parallel to the right edge (tabs).

SLT/SLD	1-Hi 12	X 32 - 139	Y 28 - 58
	2-Hi 12	X 32 - 139	Y 28 - 118
	3-Hi 12	X 32 - 139	Y 28 - 178

LIMITS (CONT'D)

C. Parallel to the top edge of card. .125" standard pattern.

SLT/SLD	2-Hi 6 - 12	X 28 - 73 - 143	Y 33 - 113
	3-Hi 12	X 28 - 143	Y 33 - 173
MST	2 Hi x 1,2&4 wide	X02 - 11 - 25 - 53	Y C - U
	3 Hi x 2&4 wide	X 02 - 25 - 53	Y C - 7

D. Parellel to the top edge of card. Random hole pattern.

SLT/SLD	2-Hi 6 - 12	X 27 - 74 - 144	Y 33 - 113
	3-Hi 12	X 27 - 144	Y 33 - 173

Crystal package type II placement must have one lead on and the other within or both within the following X and Y locations.

A. Both leads on the same X grid. .125" standard pattern.

SLT/SLD	1-Hi 6 - 12	X 38 - 63 - 133	Y 33 - 53
	2-Hi 6 - 12	X 38 - 63 - 133	Y 33 - 113
	3-Hi 12	X 38 - 133	Y 33 - 173
MST	2 Hi x 1,2&4 wide	X 04 - 09 - 23 - 51	Y C - U
	3 Hi 2&4 wide	X 04 - 23 - 51	Y C - 7

B. Both leads on the same X grid. Random hole pattern.

1-Hi 6 - 12	X 36 - 65 - 135	Y 29 - 57
2-Hi 6 - 12	X 36 - 65 - 135	Y 29 - 117
3-Hi 12	X 36 - 135	Y 29 - 177

C. Both leads on the same Y grid. .125" standard pattern.

SLT/SLD	1-Hi 6 - 12	X 28 - 73 - 143	Y 38 - 48
	2-Hi 6 - 12	X 28 - 73 - 143	Y 38 - 108
	3-Hi 12	X 28 - 143	Y 38 - 168
MST	2-Hi x 1,2&4 wide	X 02 - 11 - 25 - 53	Y D - T
	3-Hi x 2&4 wide	X 02 - 25 - 53	Y D - 6

LIMITS (Cont'd)

D. Both leads on the Y grid. Random hole pattern.

1-Hi 6 - 12	X 28 - 73 - 143	Y 36 - 49
2-Hi 6 - 12	X 28 - 73 - 143	Y 36 - 109
3-Hi 12	X 28 - 143	Y 36 - 169

Crystal package type III placement must have one lead on and the other within or both within the following X and Y locations.

A. Parallel to the right edge (tabs) of card. .125 standard pattern.

SLT/SLD	1-Hi 12	X 43 - 128	Y 28 - 58
	2-Hi 12	X 43 - 128	Y 28 - 118
	3-Hi 12	X 43 - 128	Y 28 - 178
MST	2 Hi x 1,2&4 wide	X 05 - 08 - 22 - 50	Y C - V
	3 Hi x 2,4 wide	X 05 - 22 - 50	Y C - 8

B. Parallel to the right edge (tabs) of card. Random hole pattern.

SLT/SLD	1-Hi 12	X 42 - 129	Y 28 - 58
	2-Hi 12	X 42 - 129	Y 28 - 118
	3-Hi 12	X 42 - 129	Y 28 - 178

C. Parallel to the top edge of card. .125" standard pattern.

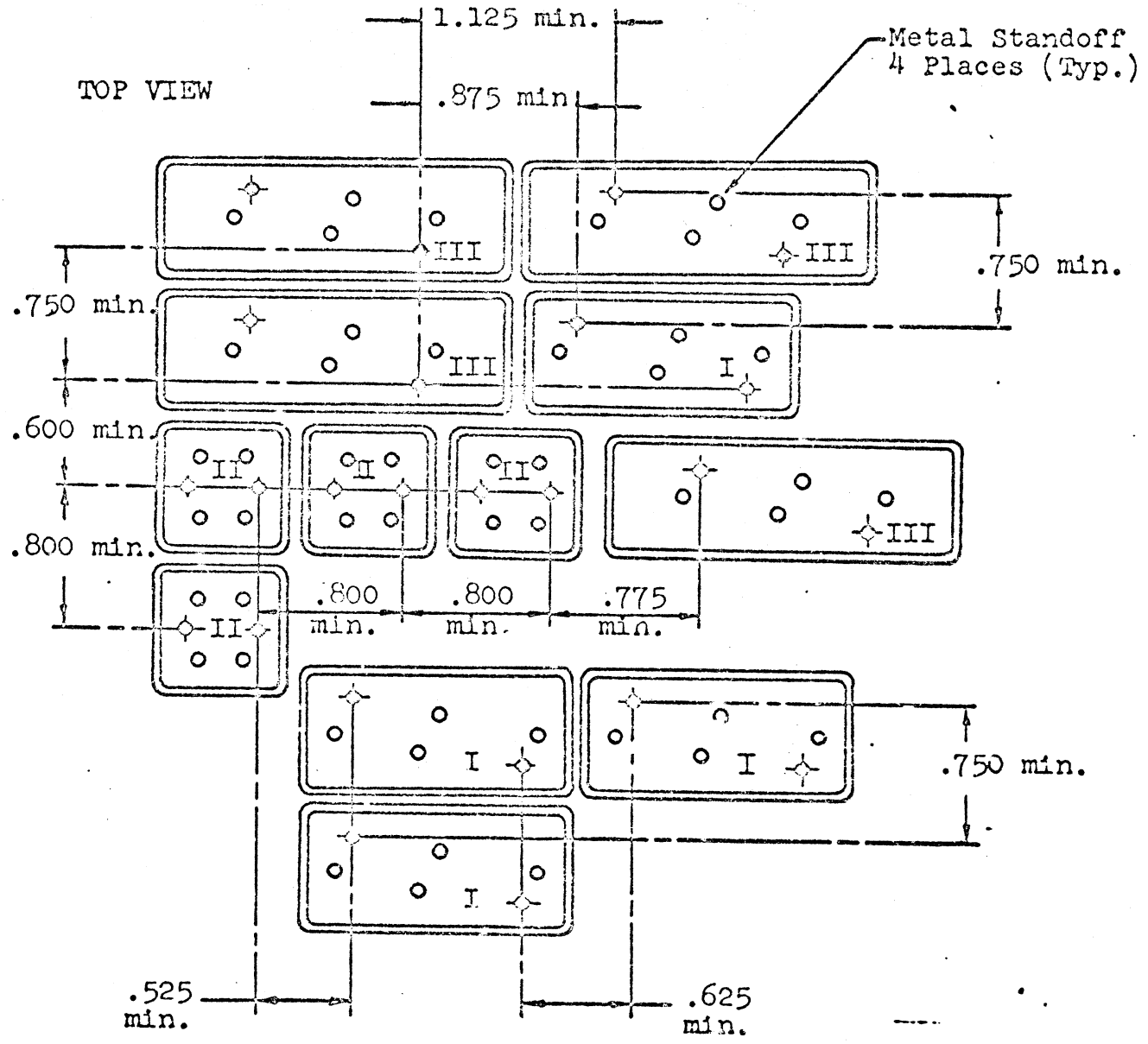
SLT/SLD	2-Hi 6 - 12	X 28 - 73 - 143	Y 43 - 103
	3-Hi 12	X 28 - 143	Y 43 - 163
MST	2 Hi x 1,2&4 wide	X 02 - 11 - 25 - 53	Y G - S
	3 Hi x 2&4 wide	X 02 - 25 - 53	Y G - 5

D. Parallel to the top edge of card. Random hole pattern.

SLT/SLD	2-Hi 12	X 27 - 74 - 144	Y 43 - 103
	3-Hi 12	X 27 - 144	Y 43 - 163

RELATIONSHIPS

The following illustration shows the intermix and normal relationship of all three types of crystal packages.



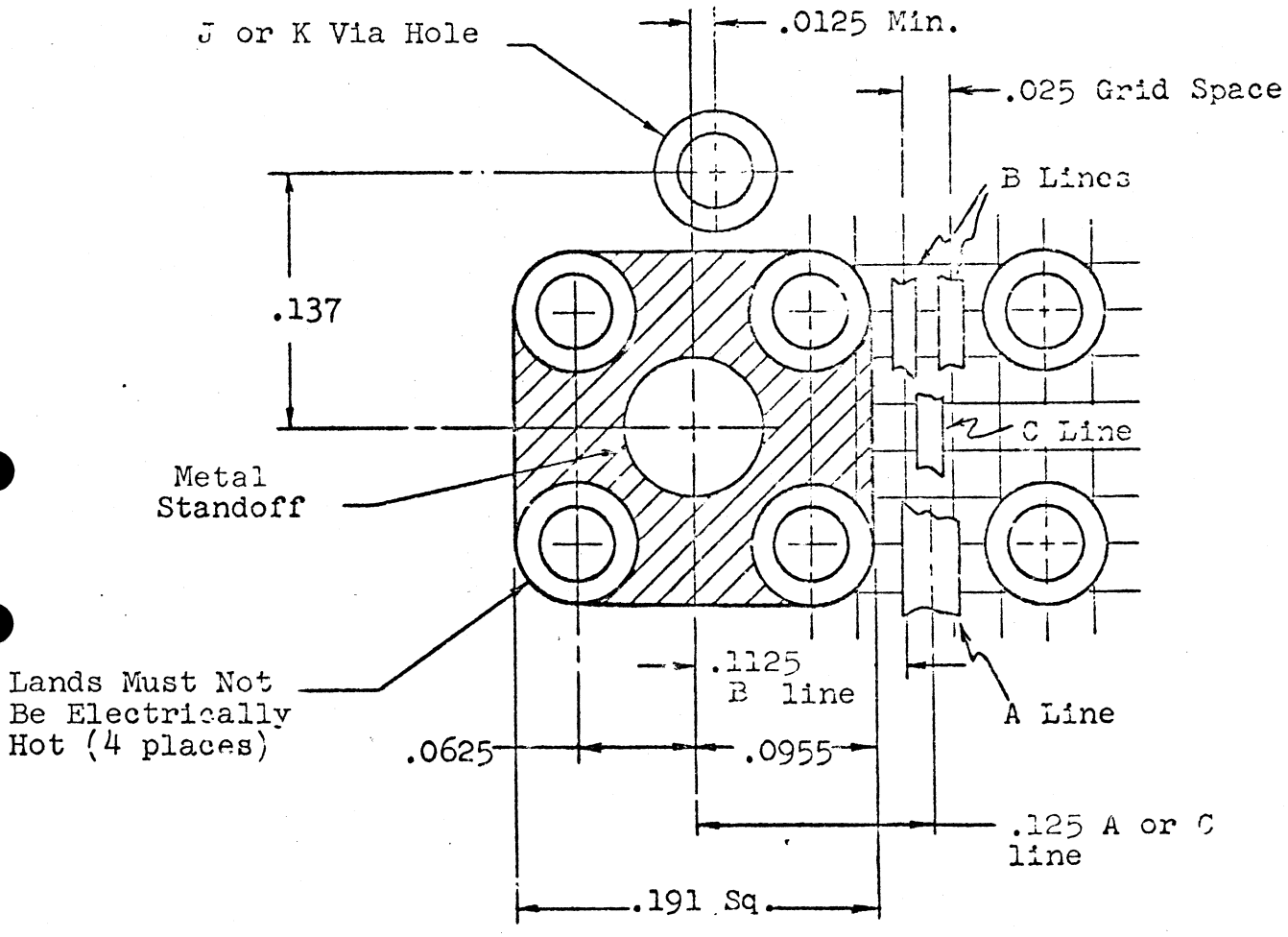
As viewed through components from component card side.

ARTWORKS

There must be no printed circuit lines through or connected to the lands on both sides of the card in the restricted area where a standoff is located.

SLT/SLD

The closest that the center of an "A" or "C" line may run to the center of a standoff location will be .125 inch (.1125 for "B" line) in either the X or Y direction. The closest the center of a via hole may be located to the center of a standoff location will be .137 inch in either the X or Y direction.



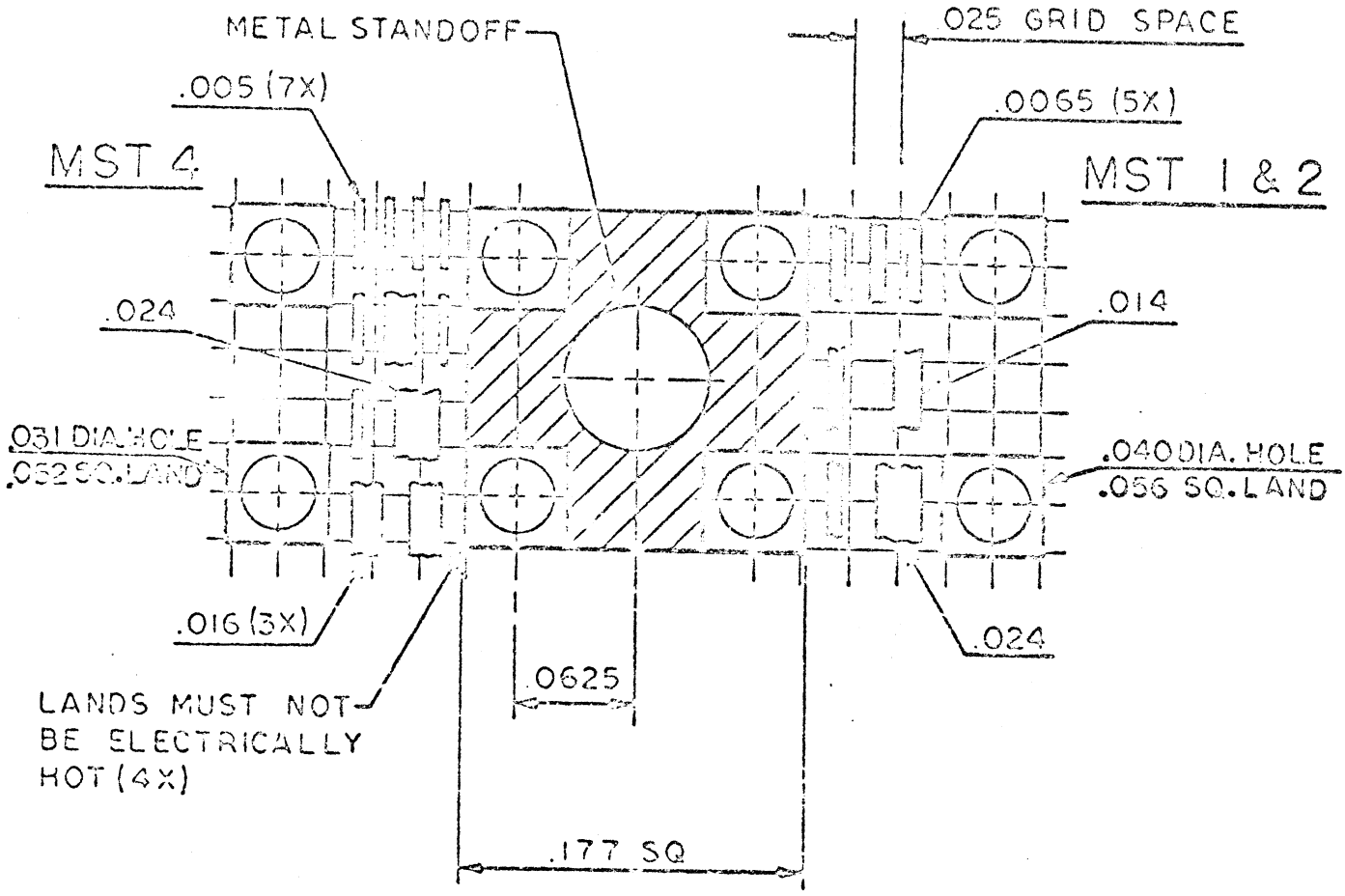
▨ — Indicates Restricted Area

SLT/SLD
FRONT ARTWORK RESTRICTED AREA FOR CRYSTALS

ARTWORKS (CONT'D)

MST 1, 2 and 4

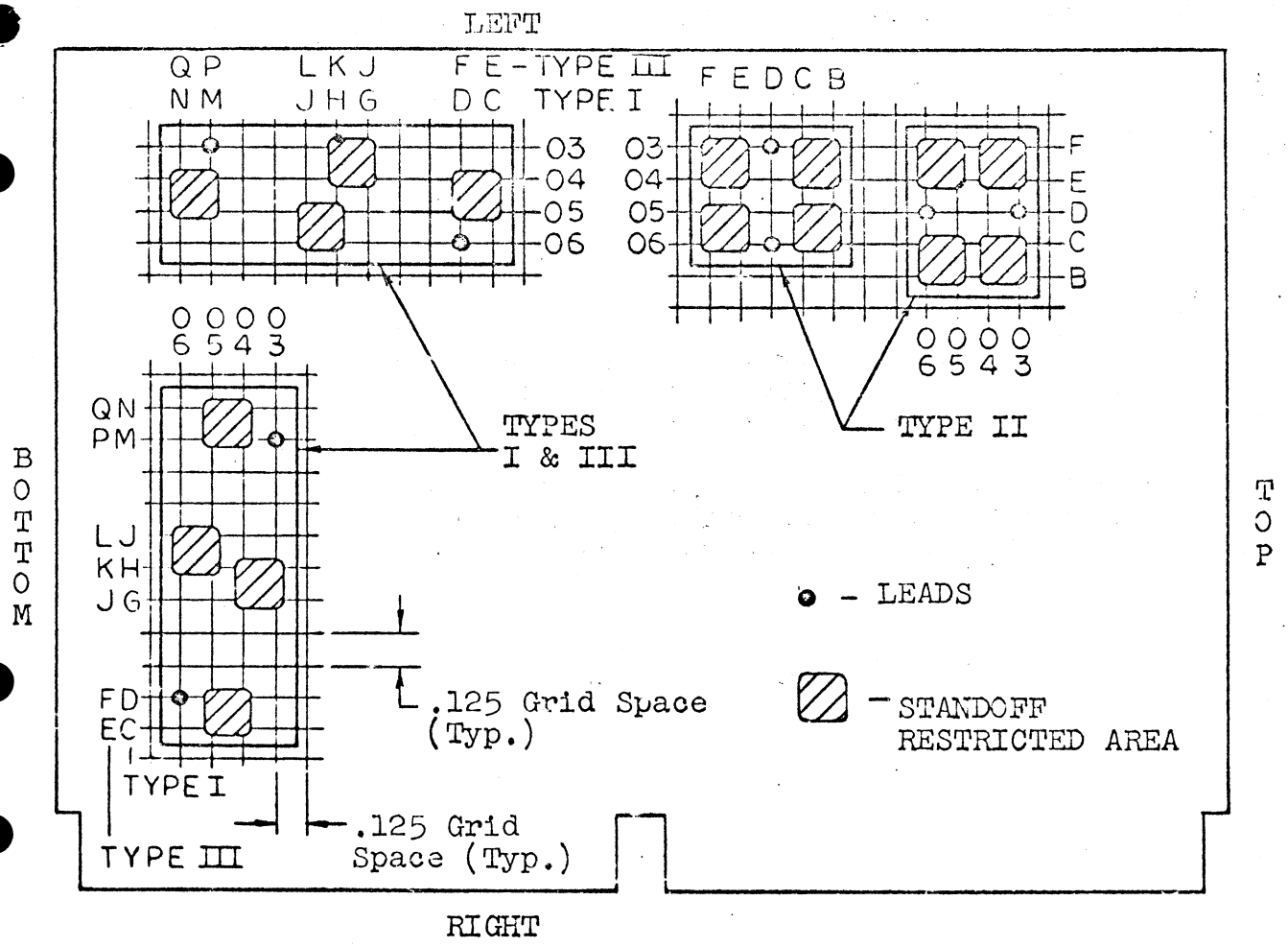
The MST/GPI programs do not consider artwork restrictions for crystals. Therefore, the holes enclosing the restricted areas around the metal standoffs must be reserved (as leads, they cannot be used as vias) to eliminate the automatic wiring in these areas. This may require manual routing for the wiring on all three crystal types.



MST 1, 2 AND 4
FRONT ARTWORK RESTRICTED
AREA FOR CRYSTALS

ARTWORKS (CONT'D)

The following sketches show the relationship between the restricted areas for standoffs and the component leads.



SEQUENCE EFFECT

All crystals will be assembled before the flux, solder and clean operation except for those rated at 35 - 45 KHZ. These will be assembled under the Manual Assembly of Non-Wettables Operation.

Clearance from other uninsulated or electrically hot components must be a minimum of .035". (.015" electrical clearance plus an additional .020" manufacturing tolerance).

HAND ASSEMBLY

All crystals are hand assembled if leads are not on the standard X-Y grids ending in 3 or 8, or equivalent.

PROCESS INFORMATION

Prepping is not required for crystals. Leads are flagged to retain the component to card. Crystals rated between 35-45 KHZ must not be subjected to ultrasonics.

Important consideration: It is preferred that all crystal leads be placed on X-Y grids ending in 3 or 8 or equivalent in order to semi-automatically flag the leads.

PLANNING

Semi-automatic equipment for leads not mounted in standard pattern is not contemplated.

CARD LAYOUT GROUND RULES

IBM Division
Engineering Practice

RELAYS-REED SWITCH

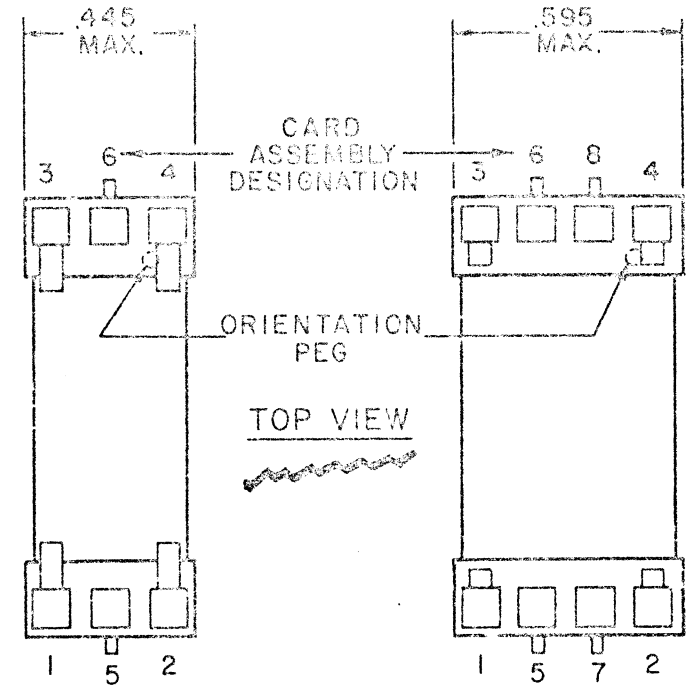
DESCRIPTION

Glass enclosed reed switches that are tubular axial leaded are inserted in a plastic bobbin that has had a coil of magnet wire wound on it. Plastic end plug(s) are inserted on the switch leads and pressed into the bobbin end(s) to retain the switch(s). The coil winding is terminated to metal tabs on the top corners of the bobbin and the coil winding is covered with plastic tape. This packaged assembly is pluggable on card assemblies and is considered insulated from the card artwork and along the length on both sides of the relay assembly. The ends of the bobbin have switch leads projecting which are electrically hot as well as the four corner tabs on the top of the bobbin. Assembly drawing code is "RR".

PACKAGE

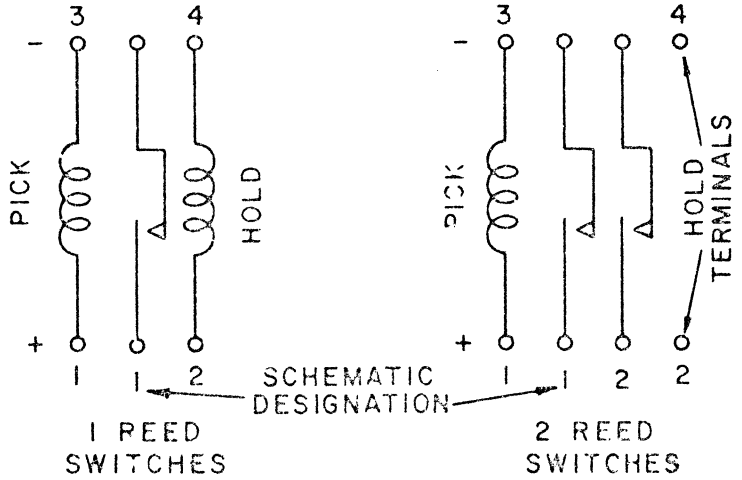
Reed Relay Assemblies may be either N/O (normally open) or N/C (normally closed). N/C reed switches are made N/O, but a permanent magnet is placed in the bobbin on the switches glass envelope to keep the contacts closed.

The package views and schematic diagrams are for packaging purposes. The part drawings have precedence. Reed Relay Assemblies are packaged in the sizes shown on the following pages.



1 POSITION
6 TERMINALS

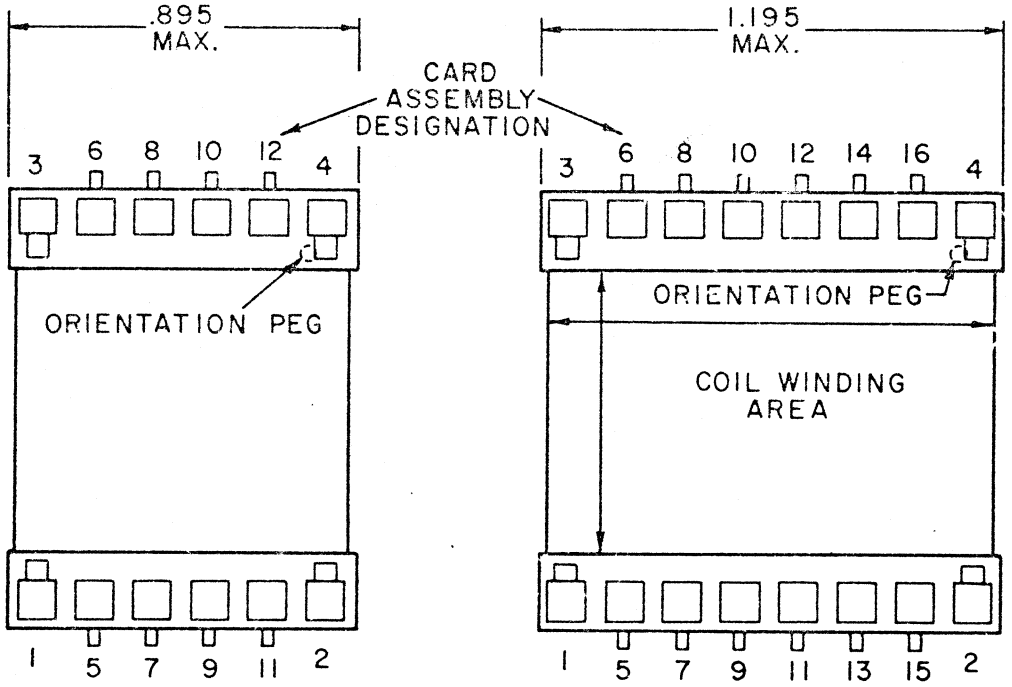
2 POSITION
8 TERMINALS



1 REED SWITCHES

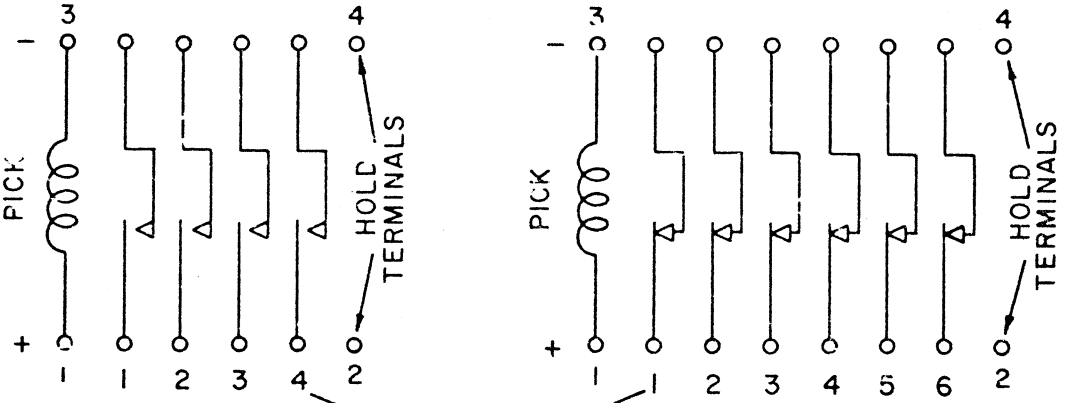
2 REED SWITCHES

TOP VIEW



4 POSITION
12 TERMINALS

6 POSITION
16 TERMINALS

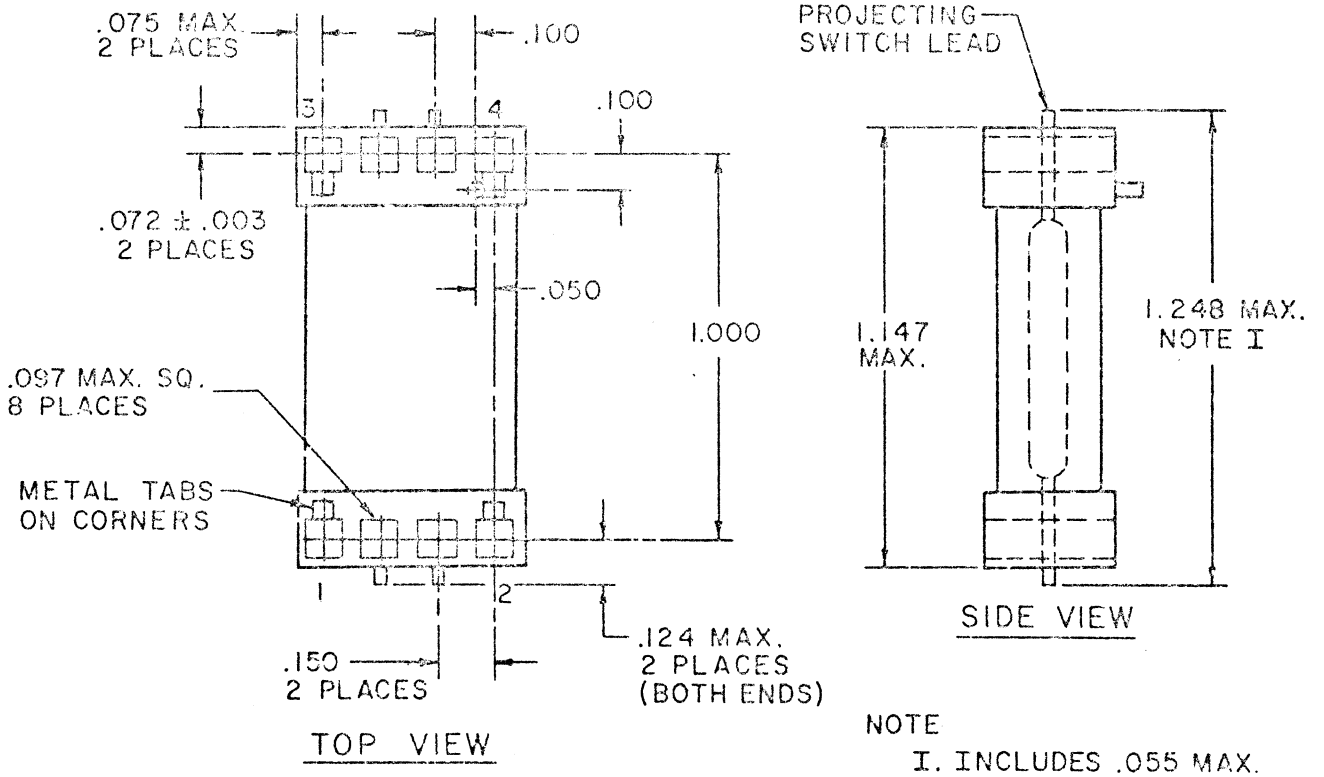


4 REED SWITCHES

6 REED SWITCHES

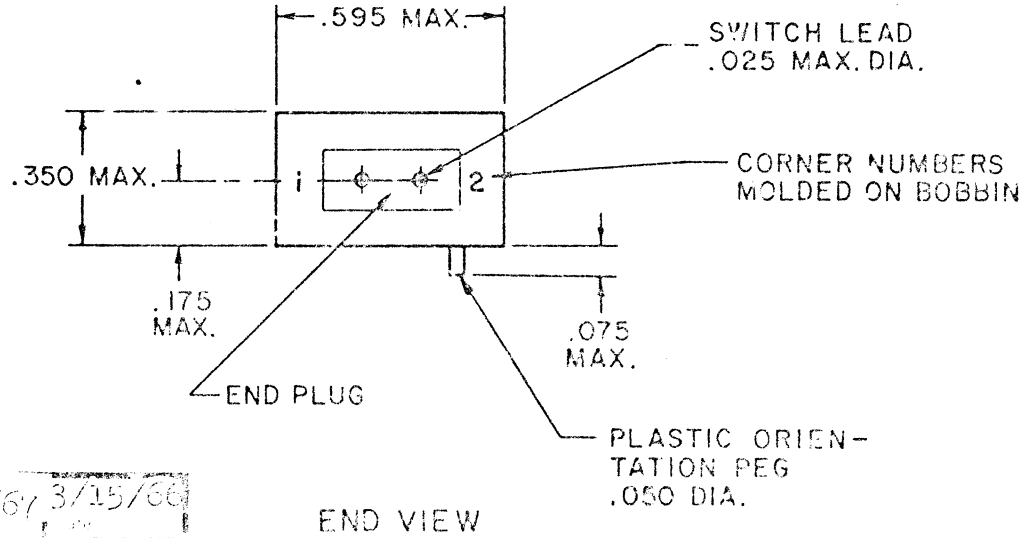
1.0 BASIS (CONTINUED)

The following view is a typical package for pluggable reed relay assemblies.



NOTE

I. INCLUDES .055 MAX. SWITCH LEAD PROJECTION ON EITHER END OR BOTH ENDS OF THE BOBBIN



REQUIREMENTS

All reed relay assemblies are pluggable onto pluggable contact terminals P/N 815198. This contact requires a "L" hole.

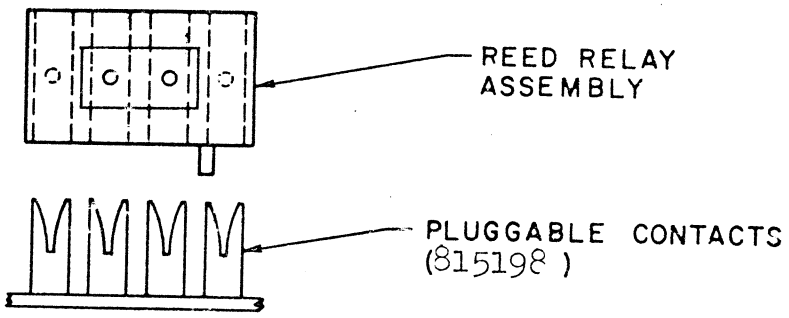
One orientation peg hole is needed for every reed relay assembly. This hole is .062± .002 (L) drill diameter and is called out in a BB note code as follows: "Drill .062 ± 002 after plating with location tolerance of ±.005 at locations, etc.

Note code FN is required for all reed relay assemblies, This note code will appear on the component view and in the note code field on the assembly drawing. All reed relay assembly part numbers in the Component Library will reflect note code FN for Library use and for manufacturing routings.

All reed relay assemblies must be mounted parallel to the X axis on all card assemblies and require a random (.025) hole pattern.

The following illustration shows reed relay assembly and pluggable contacts:

END VIEW



LIMITS

Reed Relay Assemblies cannot be used on 1 HI 6 or 12 card sizes. The pluggable contact terminals required for reed relay assemblies are used only on a random pattern (.025) and will be on or within the following X and Y grids.

2 HI 6-12 X 23-78-148 Y26-121

3 HI 12X23-148 Y26-181

From the following charts, one can determine the maximum combinations of Relay Types which can be assembled on the given card size.

NOTE: When using the charts, always begin with the largest relay required and work toward the smallest. Each alphabetic column represents the quantity of relay types that can be put on the given card size.

2-Hi 6

Relay Type	A	B	C	D	E	F	G	H	I	J	K	L	M
6 Position	2	1	1										
4 Position		1		2	2	1	1	1					
2 Position		1	1	2		3	2	1	4	3	2	1	
1 Position			1		2		1	3		1	2	4	6

RELAYS-REED SWITCH
Section 15

LIMITS (CONTINUED)

2-Hi 12

Relay Type	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V
6 Position	4	4	3	3	3	3	3	3	3	3	3	3	2	2	2	2	2	2	2	2	2	2
4 Position			2	2	1	1	1						4	3	3	2	2	2	1	1	1	1
2 Position	2		1		2	1		4	3	2	1			1		2	1		4	3	2	1
1 Position		2		1		2	3		1	3	4	5		1	2	2	3	4	1	2	4	5

Relay Type	AA	AB	AC	AD	AE	AF	AG	AH	AI	AJ	AK	AL	AM	AN	AO
6 Position	2	2	2	2	2	2	2	2	1	1	1	1	1	1	1
4 Position	1								5	4	4	4	3	3	3
2 Position		6	5	4	3	2	1			2	1		3	2	1
1 Position	6		1	2	4	6	7	8	1		1	3	1	2	3

Relay Type	AP	AQ	AR	AS	AT	AU	AV	AW	AX	AY	AZ	BA	BB	BC	BD
6 Position	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
4 Position	3	2	2	2	2	2	2	1	1	1	1	1	1	1	
2 Position		5	4	3	2	1		6	5	4	3	2	1		8
1 Position	5		1	2	4	5	7	1	2	3	4	5	7	8	

Relay Type	BE	BF	BG	BH	BI	BJ	BK	BL	BM	BN	BO	BP	BQ	BR
6 Position	1	1	1	1	1	1	1	1						
4 Position									6	5	5	5	4	4
2 Position	7	6	5	4	3	2	1			2	1		4	3
1 Position	1	2	4	5	6	8	9	10	2	1	2	4		2

2 Hi 12 (continued)

Relay Type	BS	BT	BU	BV	BW	BX	BY	BZ	CA	CB	CC	CD	CE	CF	CG	CH	CI
6 Position																	
4 Position	4	4	4	3	3	3	3	3	3	2	2	2	2	2	2	2	2
2 Position	2	1		5	4	3	2	1		7	6	5	4	3	2	1	
1 Position	3	4	5	1	2	3	5	6	7		1	3	4	5	6	8	9

Relay Type	CJ	CK	CL	CM	CN	CO	CP	CQ	CR	CS	CT	CU	CV	CW	CX	CY	CZ
6 Position																	
4 Position	1	1	1	1	1	1	1	1	1								
2 Position	8	7	6	5	4	3	2	1		10	9	8	7	6	5	4	3
1 Position	1	2	3	5	6	7	8	9	10		1	2	4	5	6	8	9

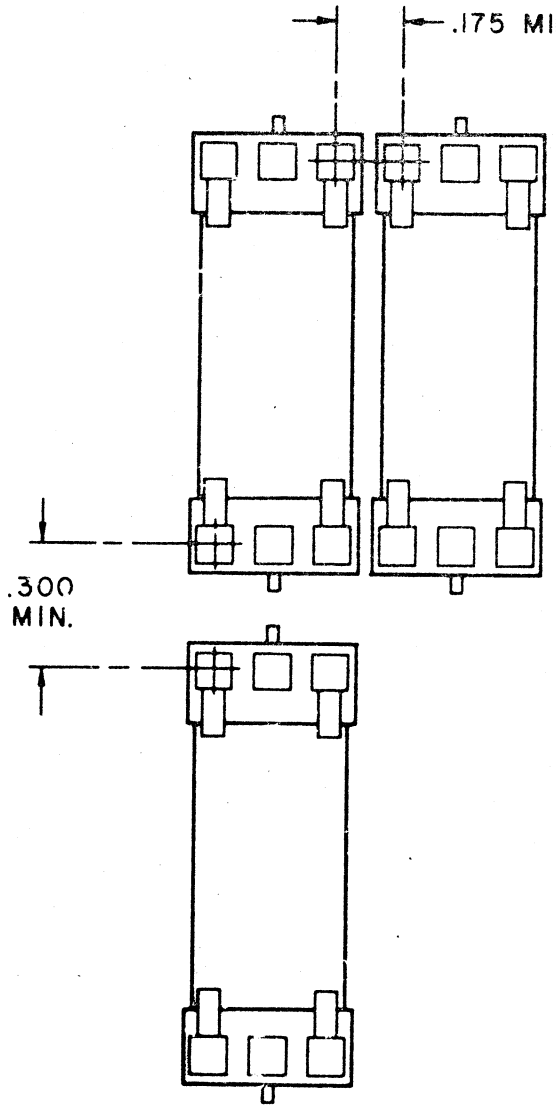
Relay Type	DA	DB	DC
6 Position			
4 Position			
2 Position	2	1	
1 Position	10	11	12

3-Hi 12 (use the above 2-Hi 12 plus the following table.)

Relay Type	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X
6 Position	2	2	2	1	1	1	1	1	1	1														
4 Position				2	1	1					3	2	2	2	1	1	1	1						
2 Position	2	1			1		3	2	1			2	1		3	2	1		5	4	3	2	1	
1 Position		1	2		1	2		1	3	4	1		1	3	1	2	3	4		1	2	3	5	6

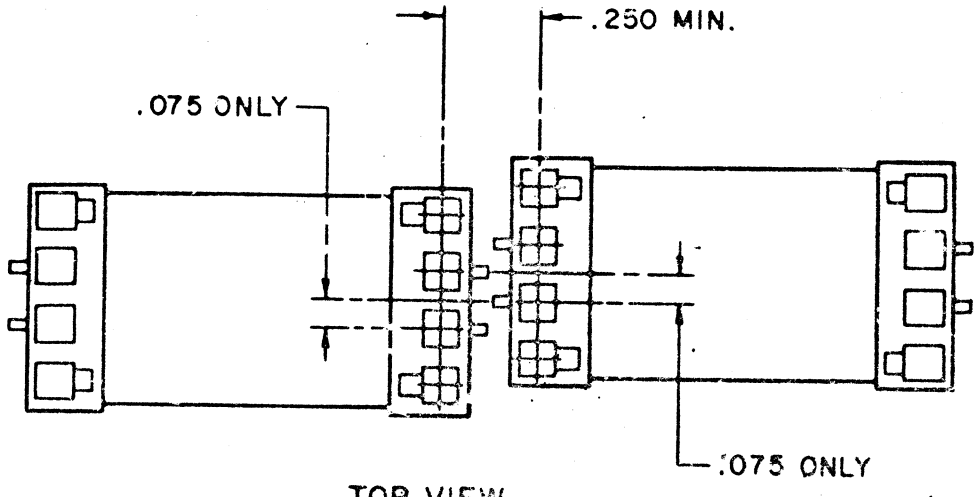
RELATIONSHIP

The following illustration shows the typical minimum physical placement of all reed relay assemblies.



TOP VIEW

The following illustration shows staggered placement.



TOP VIEW

SEQUENCE EFFECT

The following illustration shows reed relay assembly package and tubular axial lead mounting placement.

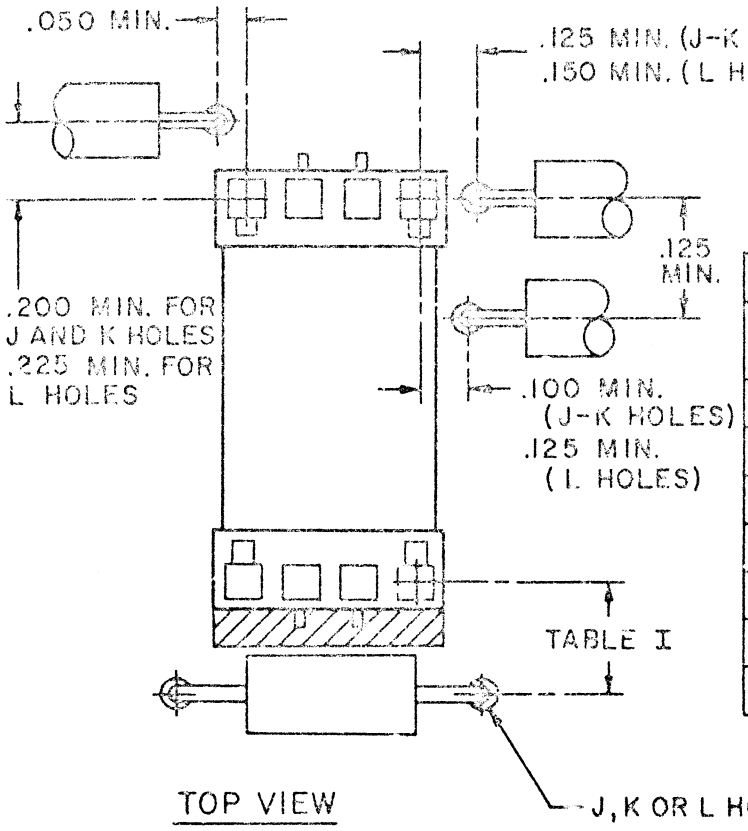
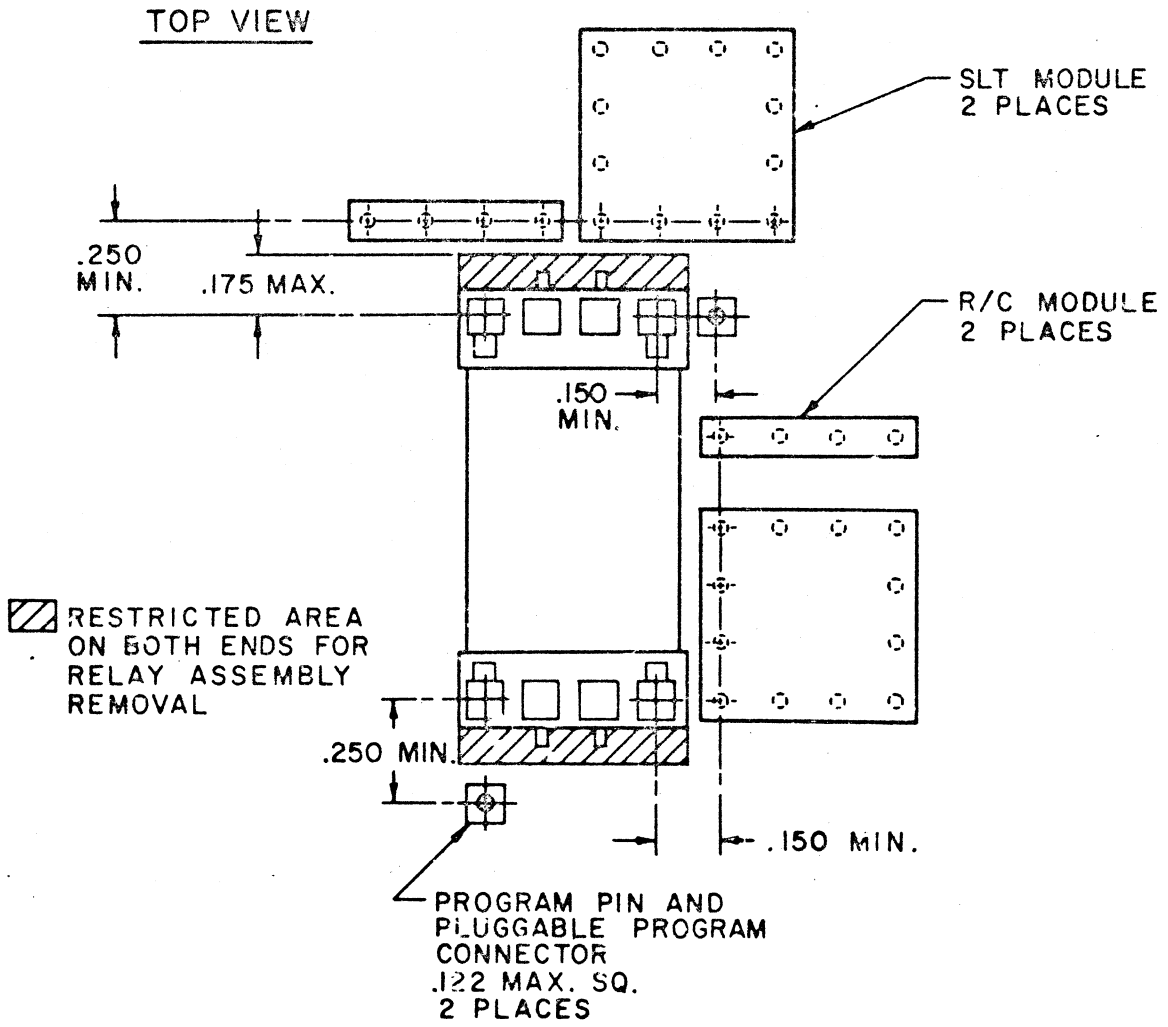


TABLE I		
HOLE SPACING MIN.	HOLE SIZE	MAX. BODY DIAMETER
.125	J-K	.100
.150-.250	J-K-L	.150
.275	J-K-L	.200
.300	J-K-L	.250
.325	J-K-L	.300
.350	J-K-L	.350
.375	J-K-L	.400

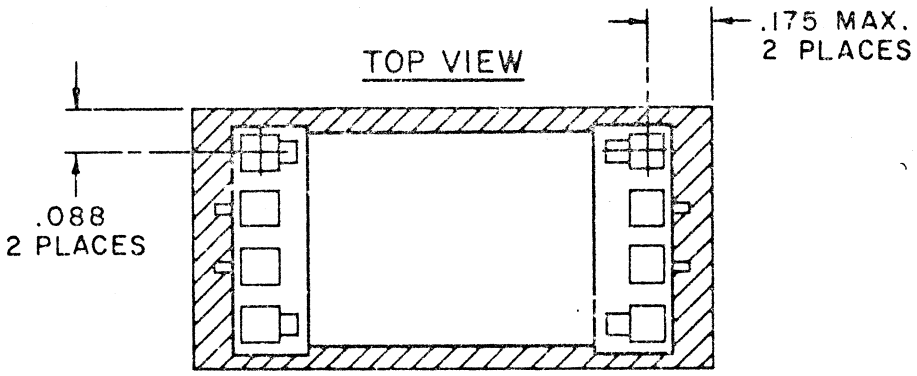
SEQUENCE EFFECT (continued)

The following illustration shows reed relay assembly package and R/C modules, SLT modules or pluggable program connectors mounting placement.

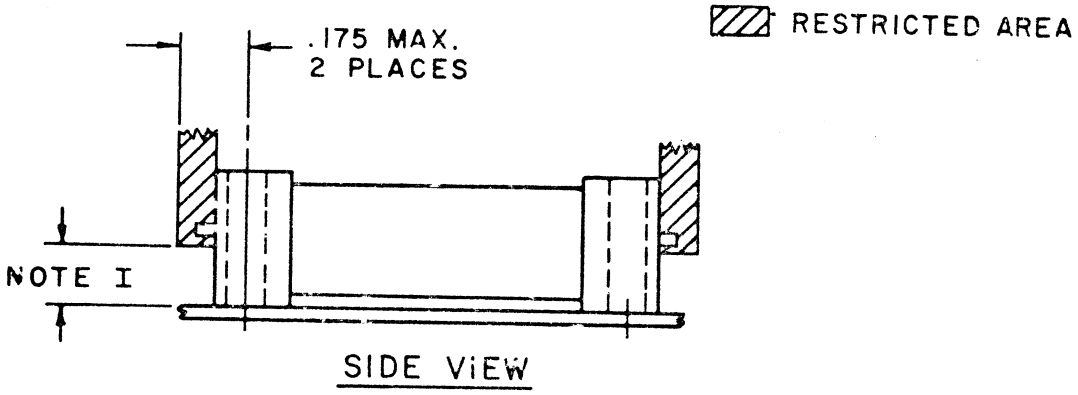


SEQUENCE EFFECT (continued)

The following illustration shows the restricted area required.



The following illustration shows the restricted area required by the CE relay removal tool.



NOTE
I .150 MAX. HEIGHT FOR INSULATED AND .135 MAX. HEIGHT FOR UNINSULATED COMPONENTS

ARTWORKS

Pluggable contacts used for plugging reed relay assemblies require the following.

The contacts plated hole cannot be used as a via hole nor be connected to an internal plane.

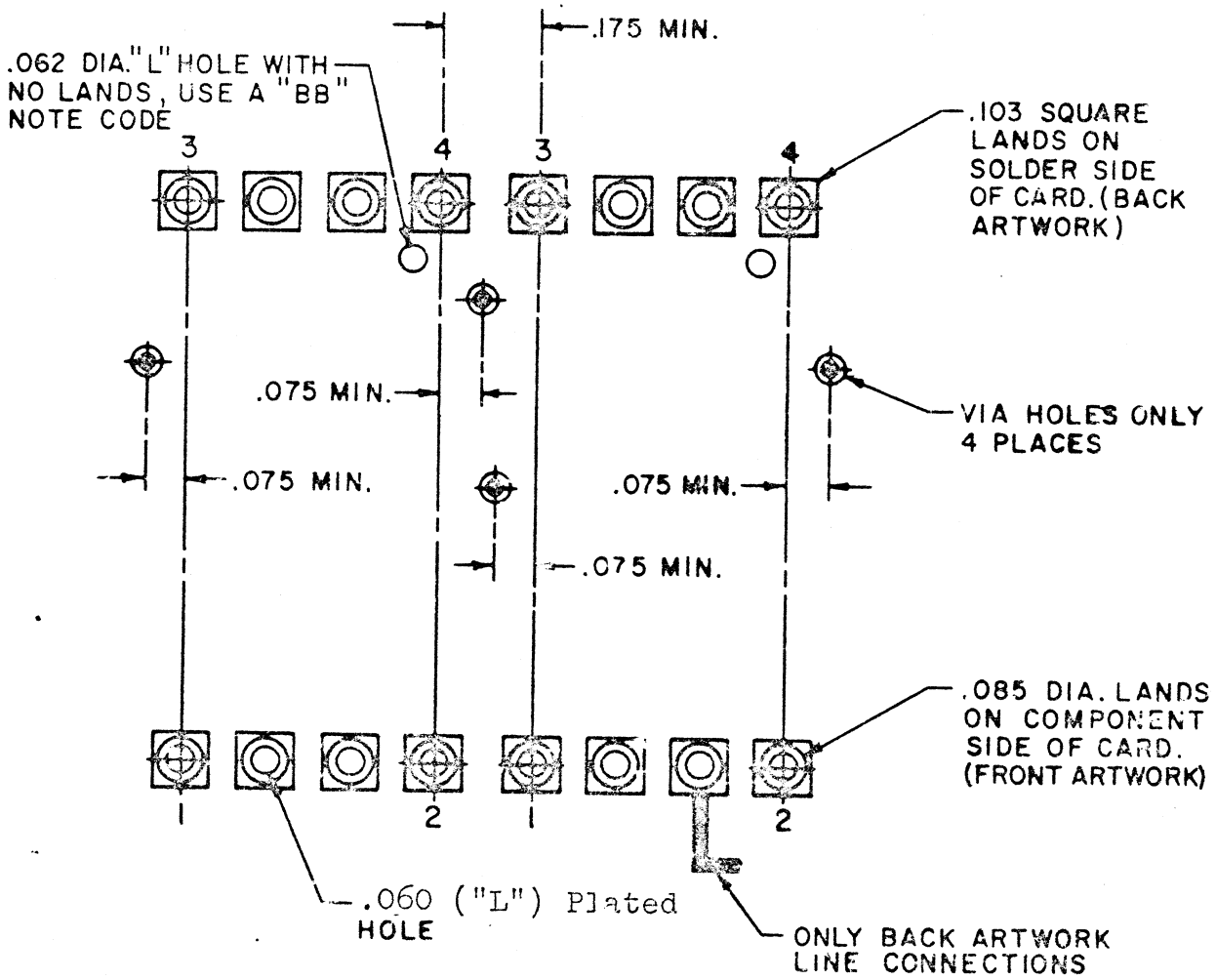
The front artwork lands (.085 diameter) for the contact cannot have printed wiring connected to them.

The back artwork land size is .103 square.

The orientation hole will not have lands and will be drilled after plating. (BB note code)

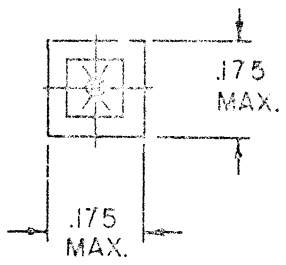
There will be no via holes under the area occupied by the reed relay assembly. They can be no closer than .075 minimum from the X grids that contact terminal positions 1, 3, or 2, 4 are on.

The following illustration represents the above context.

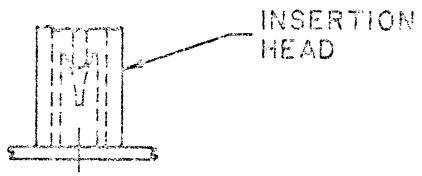


PROCESS INFORMATION

The pluggable contact terminal insertion head is shown in the sketch below.



TOP VIEW



SIDE VIEW

PLANNING

Burlington has been designing a longer and wider bobbin for various manufacturing reasons. If this comes into effect then most SLT and SMS cards will require relayout. Burlington's confidence level release is about 40%.

Burlington is reinvestigating the molded reed relay package with the final decision pending by the 3rd quarter 1967. If approved it would provide a major cost reduction to all users.

EFFECTIVE DATE: 12/29/68

SUBJECT: Card Layout Ground Rule Status Suffix 3 Section 17

This is the original publication of this section. This publication supersedes Book 03-10 DEP 2-6420-530, pages 6 and 7 under delay lines.

IBM Division
Engineering Practice

DESCRIPTION

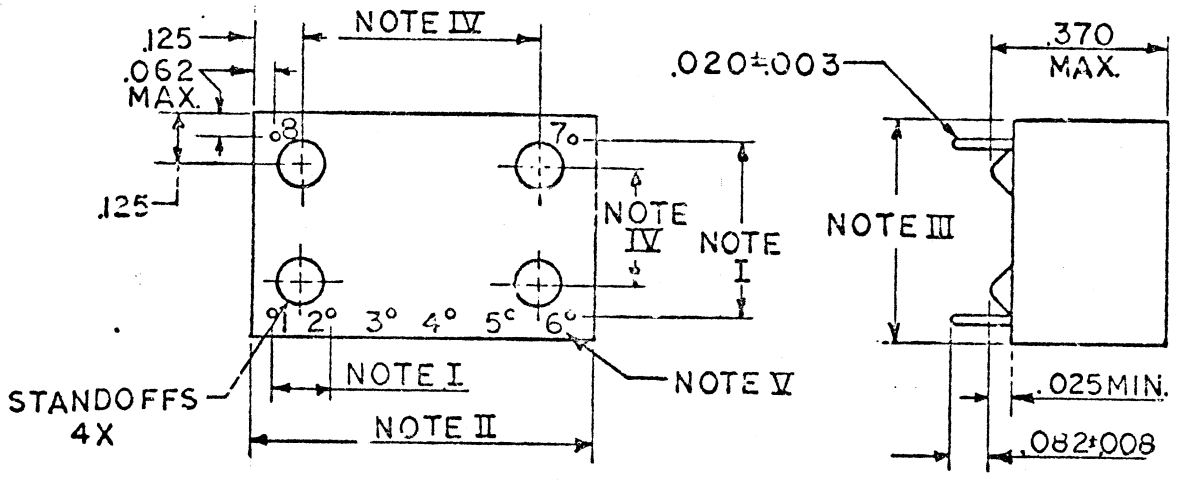
Delay lines are multi-leaded devices, designed to obtain a time lag. The delay line element is encased (molded or potted) in an electrically insulated case. Delay timing is achieved by the use of delay lines with fixed or multiple delays through the use of printed circuitry or the program pin/tuning fork system.

Assembly drawing code is "DL".

PACKAGE

There are no physical outline codes or specifications for these components.

The delay line elements that are available are so varied that standard delay line packages have not been established. The following theoretical delay line package should be used in developing new delay lines to help standardize delay line packages. The dimensions shown are from a card layout viewpoint and drafting standards shall have precedence.



PACKAGE (CONTINUED)

NOTES:

I. Leads must be spaced on a .125 multiple (ie. .125, .250, etc).

II. Body length should be a .125 multiple maximum minus .010" (i.e. .740 max, .990 max., etc.). The maximum length should not exceed 1.490 for use on one wide card assemblies.

III. Body width should be a .125 multiple maximum minus .010".

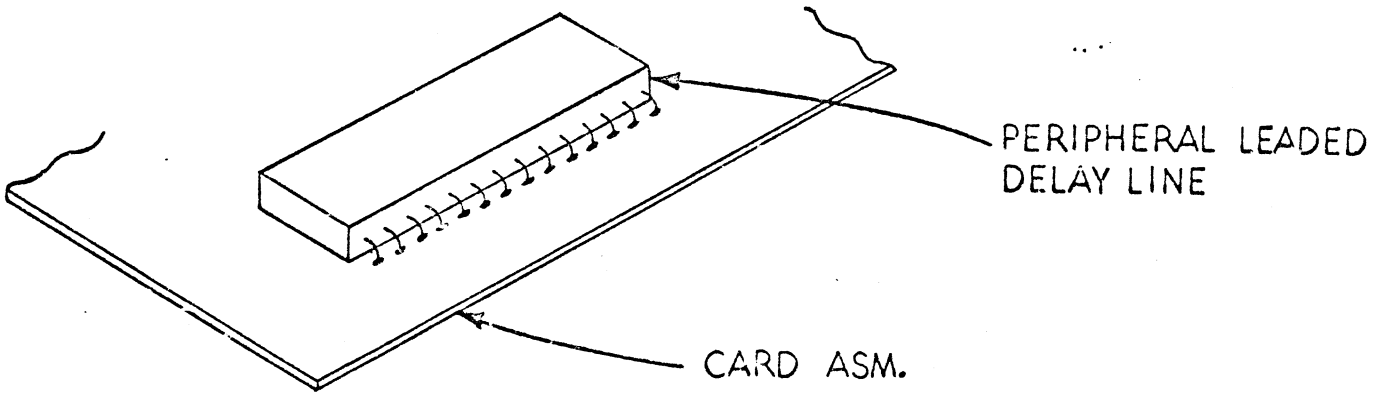
IV. Standoffs are required and should be placed no more than .750" apart.

V. The numbering system must be a counter-clockwise numerical spiral system decreasing toward the center of the body when viewing the bottom of the delay line. Lead number "1" will be identified by the figure "1" being printed on the top surface directly over lead "1".

VI. All dimensions must be dimensioned using the ± tolerance system.

REQUIREMENTS

Peripheral Leaded Delay Lines Are Not Acceptable



The delay line leads must project from the bottom of the delay line as shown under package.

There are no note codes associated with this part.

REQUIREMENTS (CONTINUED)

Delay line leads must be mounted in:

"J" (.040) plated holes for SLT and SLD
.040 plated holes for MST 1 and 2
.031 plated holes for MST 4

The CMT size code is dependent upon the lead configuration and its relationship to the delay line body. Body overhang with its maximum dimensional tolerances must be considered when coding delay lines.

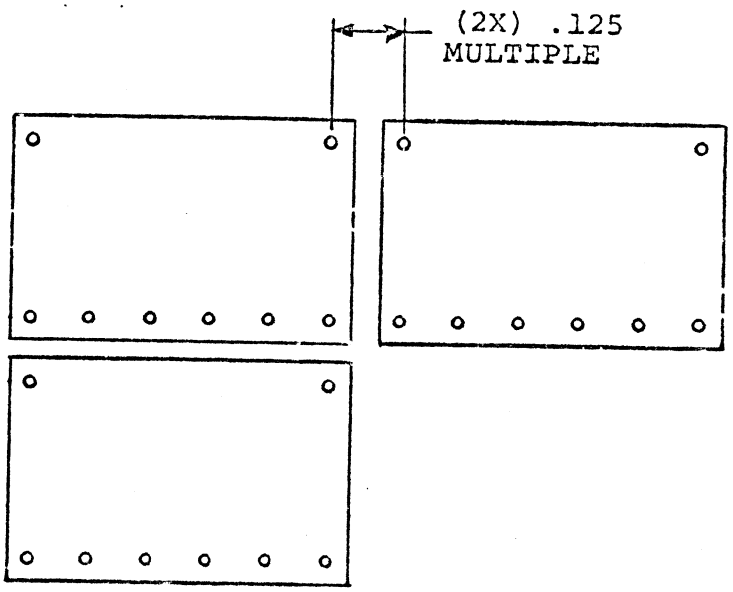
The only delay lines that are acceptable for use in MST/GPI documentation system are those that reflect the lead numbering system defined under package.

LIMITS

The maximum length and width dimensions of the delay line body must be .020 minimum from the restricted areas of the card assembly for the various card assembly sizes for SLT, SLD and MST as the delay line would normally sit on the card assembly.

RELATIONSHIPS

The following illustration shows the physical minimum placement for delay lines.



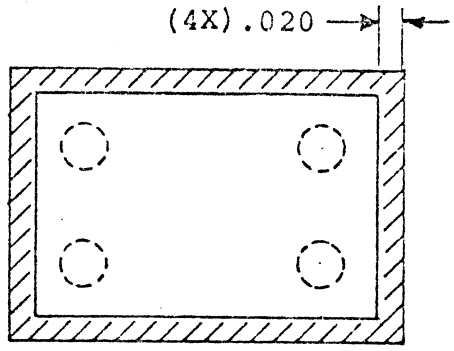
As viewed through components from the component side

ARTWORKS

There are no artwork restrictions associated with the usage of these components.

SEQUENCE EFFECT

To allow for manufacturing requirements, the .020 restricted area must be clear of all other adjacent components.



HAND ASSEMBLY

These components will be hand assembled if the leads are not on the standard X-Y grids ending in 3 of 8 or their equivalent.

PROCESS INFORMATION

The assembly machines require the delay line leads to be on X-Y grid locations ending in 3 or 8 or their equivalent.

Their leads will be gang clinched after all other components less than their maximum height are assembled.

PLANNING

Semi-automatic equipment for leads not mounted on the standard hole pattern is not contemplated.

The only delay lines that are acceptable for GPI use are:

2391190	2391325	2391715
2391191	2391708	
2391192	2391714	

CARD LAYOUT GROUND RULES

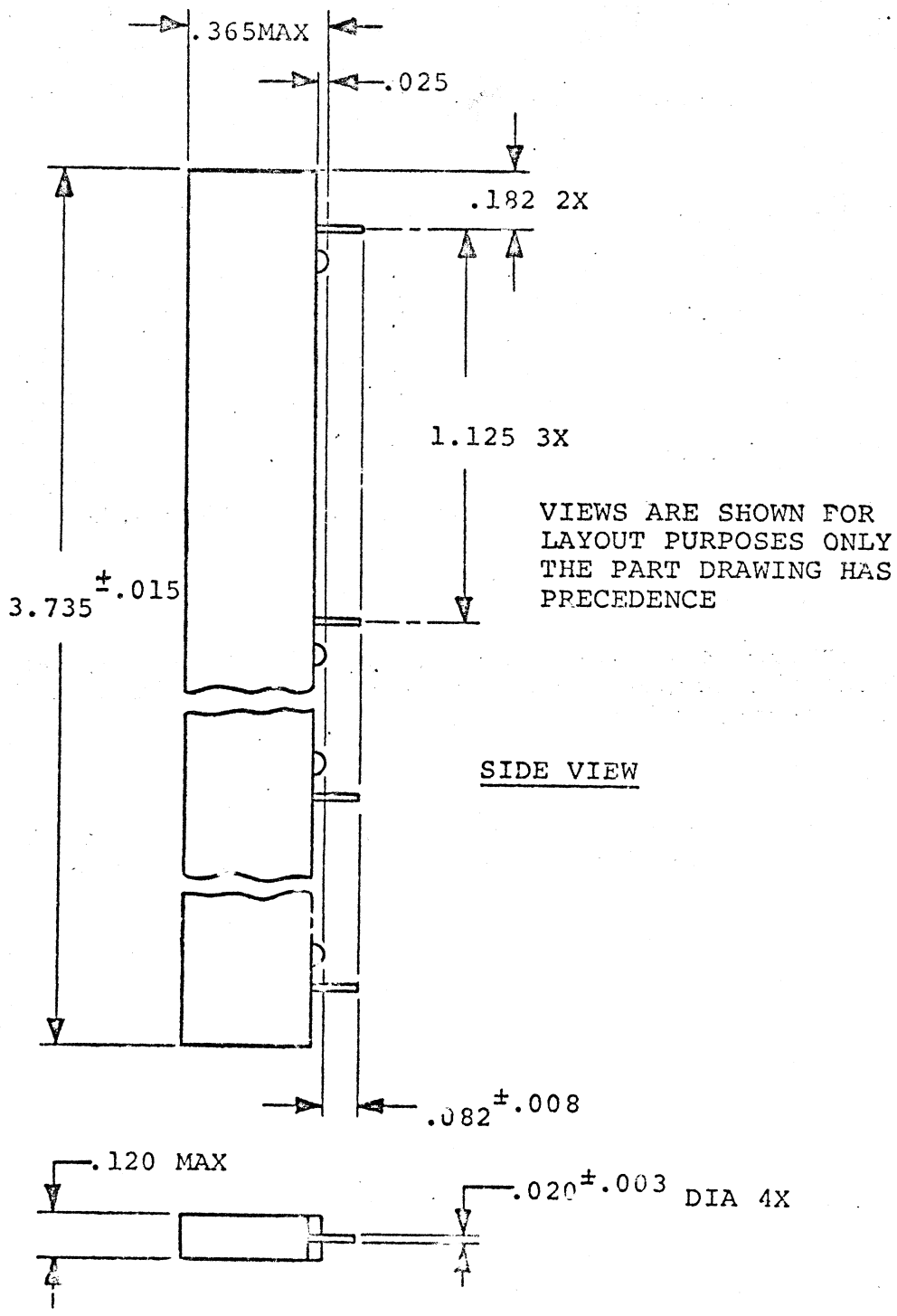
IBM Division Engineering Practice

TURBULATORS

DESCRIPTION: Turbulator 816858 is a 4 leaded insulated component; it has no electrical function. It is used as an air flow control only.

The assembly drawing code is "XX" for GPI and "HS" for EDT.

PACKAGE



REQUIREMENTS

Turbulator leads are to be mounted in:

"J" holes for SLT, SLD
.031 holes for MST 4

There are no note codes associated with this part. For CMT coding, the body of this part is to be coded in the "A" direction only with the leads parallel to the "X-X" axis. The lead and size codes are as follows:

Size Code - 1x30 Lead codes - B01, L01, V01, 501

LIMITS

Turbulators must have their leads on the following "X-Y" grid locations:

SLT	3 Hi-12	x 83 and 88	Y43-178
MST 4	3 Hi-2 wide — 2-20 pac	x 16	YE-8
MST 4	3 Hi-4 wide — 4-40 pac	x 16 and 33	YE-8
	4-50 pac	x 16 and 33	YE-8
	4-60 pac	x 14 and 32	YE-8

RELATIONSHIPS

Due to a fixed position requirement a turbulator is not mounted adjacent to another turbulator.

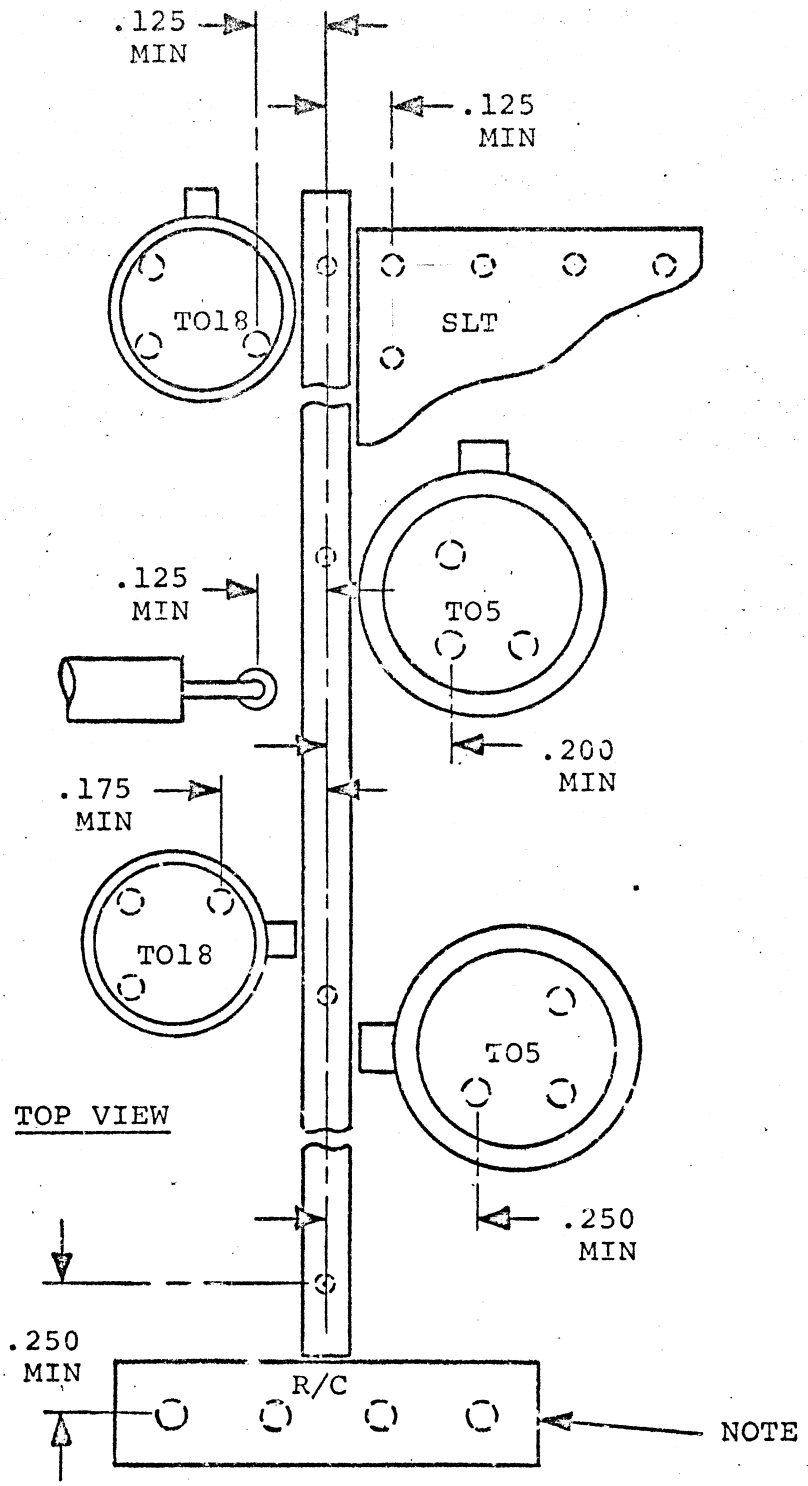
ARTWORK

There are no artwork restrictions for this component. The holes used to mount the turbulator may be used as via holes, as the turbulator leads are not electrically functional.

SEQUENCE EFFECT

The following illustration shows the physical minimum placement of the turbulators and those components assembled before turbulators.

SEQUENCE EFFECT (Cont'd)



NOTE: Turbulator axial leaded components mounted on a .375 maximum spacing may be mounted under the turbulator.

HAND ASSEMBLY

Turbulators are hand assembled on MST-4 card assemblies, leads are not clinched.

PROCESS INFORMATION

For SLT/SLD cards it is necessary to mount turbulators on "X-Y" grid locations that end in digits 3 or 8. Turbulators will be assembled and their leads gang clinched after all other components with a height of less than .360 are assembled.

PLANNING

Semi-automatic equipment for gang clinching turbulator leads on MST 4 cards is not contemplated.

For special application requirements the following two modified turbulators have been released:

2 leaded — 814319
3 leaded — 814318

IBM Division
Engineering Practice

BUMPER SPACER

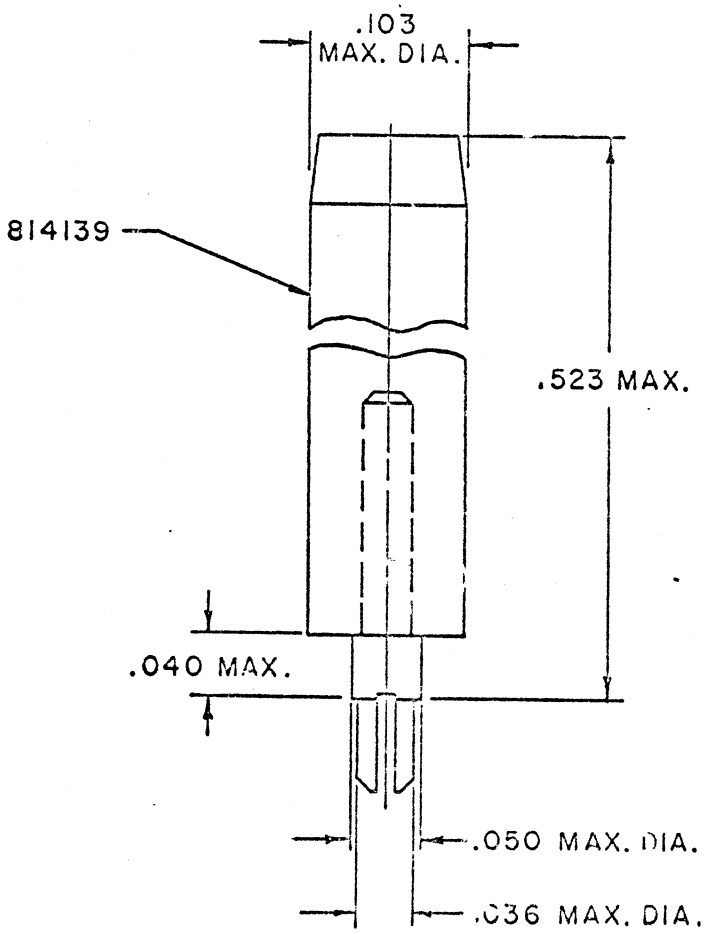
DESCRIPTION

Bumper spacer, P/N 814139, is a device used to prevent card assemblies, with heavy or high components, from touching each other when subjected to machine vibration. Without the use of bumper spacers heavy machine vibration will cause the cards to loosen from the board socket.

The spacer is made of nylon and is pressed on to program pins, P/N 814200 or 814201. This device is to be considered as an insulated component. The assembly drawing code is "U".

PACKAGE

The following illustration is for packaging purposes only, and the part drawing shall have precedence.



SIDE VIEW

BUMPER SPACER

REQUIREMENTS

Due to the card retention system for MST 2 & 4, bumper spacers are not required. For SLT/SLD and MST 1 card assemblies, if vibration tests at the machine level determines the need, bumper spacers are to be mounted within the boundries outlined in the limits section.

Bumper spacers are to be mounted in "J" holes (.040) holes.

This device requires an "AZ" note on the assembly drawing. This note shall read "Due to component height of .523 max. this card must be removed prior to removal of card adjacent to component side. Card left edge black mark required for 890913."

LIMITS

Bumper spacers are to be mounted on or within the following grid locations. The number of bumper spacers used will be determined by the allowable mounting space available on each card assembly.

A. For Card Left Edge Center Area - 1 Bumper Spacer required

2Hix1Wide		2Hix2Wide		3Hi-12	2Hix4Wide
SLT/SLD	MST 1	SLT/SLD	MST 1	SLT/SLD	MST 1
X38-58	X05-09	X73-93	X12-16	X73-93	X24-28
Y113-123	Y U-W	X113-123	Y U-W	Y173-183	Y U-W

B. For card left edge out of center area - 2 Bumper Spacers required, Distance between spacers to be at a maximum.

2Hix1Wide		2Hix2Wide		3Hi-12	2Hix4Wide
SLT/SLD	MST 1	SLT/SLD	MST 1	SLT/SLD	MST 1
X23-33	X10-12	X23-68	X17-26	X23-68	X45-54
X63-78	X01-04	X98-148	X01-11	X98-148	X01-11
Y113-123	Y U-W	Y113-123	Y U-W	Y173-183	Y U-W

RELATIONSHIP

A relationship does not occur as the limits prevent the bumper spacers from being placed next to each other.

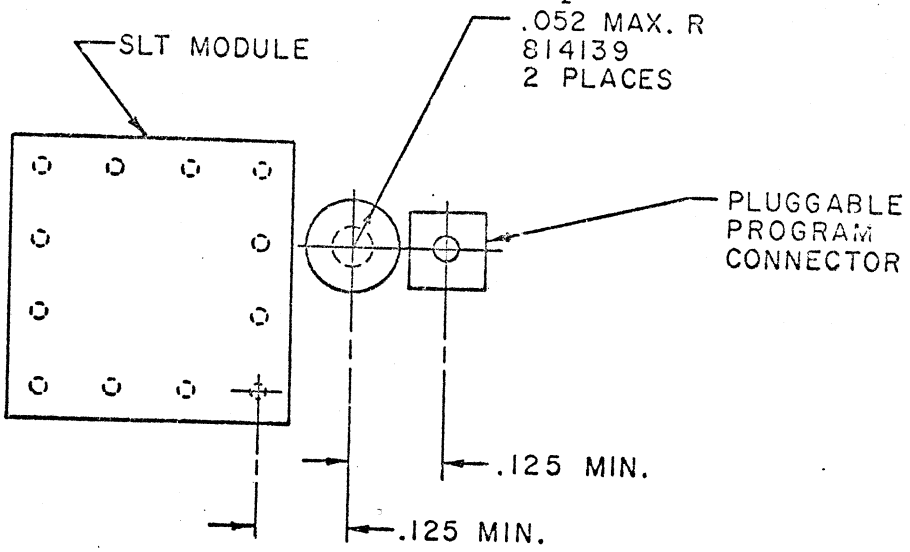
ARTWORKS

No artwork restrictions apply to this component.

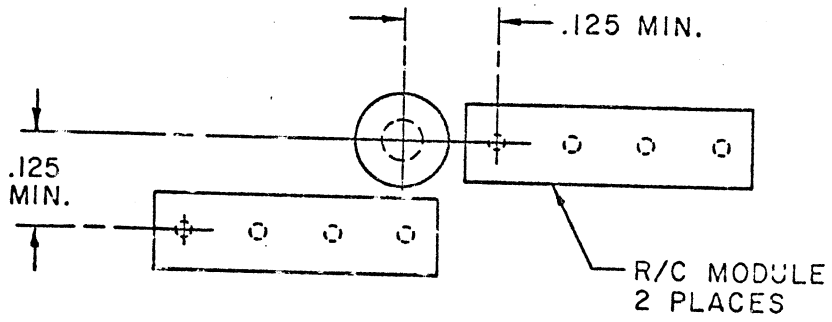
SEQUENCE EFFECT

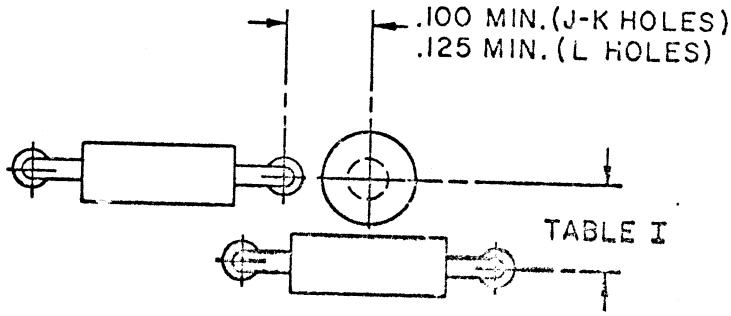
The following illustration shows the physical minimum placement between bumper spacers and:

A. Pluggable program connector
B. SLT Module
C. R/C Module
D. Tubular axial leaded components



TOP VIEW

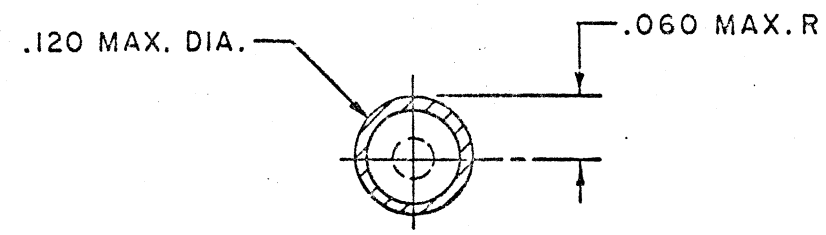




TOP VIEW

TABLE I	
HOLE SPACING MIN.	MAX. BODY DIAMETER
.125	.130
.150	.180
.175	.230
.200	.280
.225	.330
.250	.380

SEQUENCE EFFECT (CONT'D)



▨ RESTRICTED AREA

TOP VIEW

HAND ASSEMBLY

All bumper spacers are hand assembled.

PROCESS INFORMATION

Due to the height of bumper spacers they are to be assembled after final card testing has been made.

PLANNING

No semi-automatic insertion equipment is contemplated.

SUPPLEMENT OF STATUS

EFFECTIVE DATE: 4/17/69

SUBJECT: Card Layout Ground Rule Status, Suffix 3, Section 20

This section has been updated to include requirements for MST 1, 2 and 4.

This update supersedes DEP 2-7047, Suffix 3, Section 20, dated 12/31/65.

DECIMAL AND .025 GRIDS CORRELATION

This table may be used for layout and checking of card assemblies.

Once the number of grid spaces has been determined, refer to Line B for the number and Line A will give the decimal equivalent based on the .025 grid system.

A - Distance between grids consecutively totaled.
B - Number of grid spaces.

A	.025	.050	.075	.100	.125	.150	.175	.200	.225	.250
B	1	2	3	4	5	6	7	8	9	10
A	.275	.300	.325	.350	.375	.400	.425	.450	.475	.500
B	11	12	13	14	15	16	17	18	19	20
A	.525	.550	.575	.600	.625	.650	.675	.700	.725	.750
B	21	22	23	24	25	26	27	28	29	30
A	.775	.800	.825	.850	.875	.900	.925	.950	.975	1.000
B	31	32	33	34	35	36	37	38	39	40
A	1.025	1.050	1.075	1.100	1.125	1.150	1.175	1.200	1.225	1.250
B	41	42	43	44	45	46	47	48	49	50
A	1.275	1.300	1.325	1.350	1.375	1.400	1.425	1.450	1.475	1.500
B	51	52	53	54	55	56	57	58	59	60
A	1.525	1.550	1.575	1.600	1.625	1.650	1.675	1.700	1.725	1.750
B	61	62	63	64	65	66	67	68	69	70
A	1.775	1.800	1.825	1.850	1.875	1.900	1.925	1.950	1.975	2.000
B	71	72	73	74	75	76	77	78	79	80
A	2.025	2.050	2.075	2.100	2.125	2.150	2.175	2.200	2.225	2.250
B	81	82	83	84	85	86	87	88	89	90
A	2.275	2.300	2.325	2.350	2.375	2.400	2.425	2.450	2.475	2.500
B	91	92	93	94	95	96	97	98	99	100
A	2.525	2.550	2.575	2.600	2.625	2.650	2.675	2.700	2.725	2.750
B	101	102	103	104	105	106	107	108	109	110
A	2.775	2.800	2.825	2.850	2.875	2.900	2.925	2.950	2.975	3.000
B	111	112	113	114	115	116	117	118	119	120

DECIMAL AND .025 GRID CORRELATION (CONTINUED)

A	3.025	3.050	3.075	3.100	3.125	3.150	3.175	3.200	3.225	3.250
B	121	122	123	124	125	126	127	128	129	130
A	3.275	3.300	3.325	3.350	3.375	3.400	3.425	3.450	3.475	3.500
B	131	132	133	134	135	136	137	138	139	140
A	3.525	3.550	3.575	3.600	3.625	3.650	3.675	3.700	3.725	3.750
B	141	142	143	144	145	146	147	148	149	150
A	3.775	3.800	3.825	3.850	3.875	3.900	3.925	3.950	3.975	4.000
B	151	152	153	154	155	156	157	158	159	160
A	4.025	4.050	4.075	4.100	4.125	4.150	4.175	4.200	4.225	4.250
B	161	162	163	164	165	166	167	168	169	170

This Table may be used for determining the hypothenuse on triangles with sides of more than .025.

X and Y grids on a .025 increment and the resulting hypothenuse.

	.025	.050	.075	.100	.125	.150	.175	.200	.225	.250	.275	.300	.325	.350	.375	.400	.425	.450	.475	.500
.025	.035	.056	.079	.103	.128	.152	.177	.202	.226	.251	.276	.301	.326	.351	.376	.401	.426	.451	.476	.501
.050	-----	.071	.090	.112	.135	.158	.182	.206	.231	.255	.279	.304	.329	.354	.378	.403	.428	.453	.478	.502
.075	----------	.106	.125	.146	.168	.190	.214	.237	.261	.285	.309	.334	.358	.382	.407	.432	.456	.481	.506	
.100	----------	.141	.160	.180	.202	.224	.246	.269	.293	.316	.340	.364	.388	.412	.437	.461	.485	.510		
.125	----------	.177	.195	.215	.236	.257	.279	.302	.325	.348	.372	.395	.419	.443	.467	.491	.516			
.150	----------	.212	.230	.250	.270	.292	.313	.335	.358	.381	.404	.427	.451	.474	.498	.522				
.175	----------	.247	.266	.285	.305	.326	.347	.369	.391	.414	.437	.460	.483	.506	.530					
.200	----------	.283	.301	.320	.340	.361	.381	.403	.425	.447	.470	.492	.515	.539						
.225	----------	.318	.336	.355	.375	.395	.416	.437	.459	.481	.503	.526	.548							
.250	----------	.354	.372	.391	.410	.428	.451	.472	.493	.524	.537	.559								
.275	----------	.389	.407	.426	.445	.465	.485	.506	.527	.549	.571									
.300	----------	.424	.442	.461	.480	.500	.520	.541	.562	.583										
.325	----------	.460	.478	.496	.515	.535	.555	.576	.596											
.350	----------	.495	.513	.532	.551	.570	.590	.610												
.375	----------	.530	.548	.567	.586	.605	.625													
.400	----------	.566	.584	.602	.621	.640														
.425	----------	.601	.619	.637	.656															
.450	----------	.636	.654	.673																
.475	----------	.672	.690																	
.500	----------	.707																		

CARD GROUND RULES DEP 2-6230 3
SECTION 20 Cat. Subject Suffix

3/17/69 Date

3 of 9 Page

Date 3/17/69

This Table may be used for determining the hypothenuse on triangles with sides of less than .025.

	.001	.002	.003	.004	.005	.006	.007	.008	.009	.010	.011	.012	.013	.014	.015	.016	.017	.018	.019	.020	.021	.022	.023	.024	.025
.001	.0014	.0022	.0032	.0041	.0051	.0061	.0071	.0081	.0090	.0100	.0110	.0120	.0130	.0140	.0150	.0160	.0170	.0180	.0190	.0200	.0210	.0220	.0230	.0240	.0250
.002	-----	.0028	.0035	.0045	.0054	.0063	.0073	.0082	.0092	.0102	.0112	.0122	.0131	.0141	.0151	.0161	.0171	.0181	.0191	.0201	.0211	.0221	.0231	.0241	.0251
.003	-----	-----	.0042	.0050	.0058	.0067	.0076	.0085	.0095	.0104	.0114	.0124	.0133	.0143	.0153	.0163	.0173	.0182	.0192	.0202	.0212	.0222	.0232	.0242	.0252
.004	-----	-----	-----	.0056	.0064	.0072	.0080	.0089	.0098	.0108	.0117	.0126	.0136	.0146	.0155	.0165	.0175	.0184	.0194	.0204	.0214	.0224	.0233	.0243	.0253
.005	-----	-----	-----	-----	.0071	.0078	.0086	.0094	.0103	.0112	.0121	.0130	.0139	.0149	.0158	.0168	.0177	.0187	.0196	.0206	.0216	.0226	.0235	.0245	.0255
.006	-----	-----	-----	-----	-----	.0085	.0092	.0100	.0108	.0117	.0125	.0134	.0143	.0152	.0161	.0171	.0180	.0190	.0199	.0209	.0218	.0228	.0238	.0247	.0257
.007	-----	-----	-----	-----	-----	-----	.0099	.0106	.0114	.0122	.0130	.0139	.0148	.0156	.0165	.0175	.0184	.0193	.0202	.0212	.0221	.0231	.0240	.0250	.0260
.008	-----	-----	-----	-----	-----	-----	-----	.0113	.0120	.0128	.0136	.0144	.0153	.0161	.0170	.0179	.0188	.0197	.0206	.0215	.0225	.0234	.0243	.0253	.0262
.009	-----	-----	-----	-----	-----	-----	-----	-----	.0127	.0134	.0142	.0150	.0158	.0166	.0175	.0184	.0192	.0201	.0210	.0219	.0228	.0238	.0247	.0256	.0266
.010	-----	-----	-----	-----	-----	-----	-----	-----	-----	.0141	.0149	.0156	.0164	.0172	.0180	.0189	.0197	.0206	.0215	.0224	.0233	.0242	.0251	.0260	.0269
.011	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	.0155	.0163	.0170	.0178	.0186	.0194	.0202	.0211	.0219	.0228	.0237	.0246	.0255	.0264	.0273
.012	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	.0170	.0177	.0184	.0192	.0200	.0208	.0216	.0225	.0233	.0242	.0251	.0259	.0268	.0277
.013	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	.0184	.0191	.0198	.0206	.0214	.0222	.0230	.0238	.0247	.0255	.0264	.0273	.0282
.014	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	.0198	.0205	.0213	.0220	.0228	.0230	.0244	.0252	.0261	.0269	.0278	.0286
.015	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	.0212	.0219	.0227	.0234	.0242	.0250	.0258	.0266	.0275	.0283	.0291
.016	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	.0226	.0233	.0241	.0248	.0256	.0264	.0272	.0280	.0288	.0297
.017	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	.0240	.0248	.0255	.0262	.0270	.0278	.0286	.0294	.0302
.018	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	.0254	.0262	.0269	.0277	.0284	.0292	.0300	.0308
.019	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	.0269	.0276	.0283	.0291	.0298	.0306	.0314
.020	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	.0283	.0290	.0297	.0305	.0312	.0320
.021	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	.0297	.0304	.0311	.0319	.0326
.022	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	---	-----	-----	-----	-----	-----	-----	.0311	.0318	.0326	.0333
.023	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	.0325	.0332	.0340
.024	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	.0339	.0346
.025	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	.0353

X and Y grids on a .001 increment and the resulting hypothenuse.

DEP 2-6230 | 3 | CARD GROUND RULES | 20

Col. | Subject | Suffix | SECTION | TABLES

TABLES

SLT X grid distances by decimal and .025 increment. This Table may be used for checking and layout of card assemblies.

2.185	X64	1.110	2.160	X65	1.135			
2.210	X63	1.085	2.135	X66	1.160	.060	X149	3.235
2.235	X62	1.060	2.110	X67	1.185	.085	X148	3.210
2.260	X61	1.035	2.085	X68	1.210	.110	X147	3.185
2.285	X60	1.010	2.060	X69	1.235	.135	X146	3.160
2.310	X59	.985	2.035	X70	1.260	.160	X145	3.135
2.335	X58	.960	2.010	X71	1.285	.185	X144	3.110
2.360	X57	.935	1.985	X72	1.310	.210	X143	3.085
2.385	X56	.910	1.960	X73	1.335	.235	X142	3.060
2.410	X55	.885	1.935	X74	1.360	.260	X141	3.035
2.435	X54	.860	1.910	X75	1.385	.285	X140	3.010
2.460	X53	.835	1.885	X76	1.410	.310	X139	2.985
2.485	X52	.810	1.860	X77	1.435	.335	X138	2.960
2.510	X51	.785	1.835	X78	1.460	.360	X137	2.935
2.535	X50	.760	1.810	X79	1.485	.385	X136	2.910
2.560	X49	.735	1.785	X80	1.510	.410	X135	2.885
2.585	X48	.710	1.760	X81	1.535	.435	X134	2.860
2.610	X47	.685	1.735	X82	1.560	.460	X133	2.835
2.635	X46	.660	1.710	X83	1.585	.485	X132	2.810
2.660	X45	.635	1.685	X84	1.610	.510	X131	2.785
2.685	X44	.610	1.660	X85	1.635	.535	X130	2.760
2.710	X43	.585	1.635	X86	1.660	.560	X129	2.735
2.735	X42	.560	1.610	X87	1.685	.585	X128	2.710
2.760	X41	.535	1.585	X88	1.710	.610	X127	2.685
2.785	X40	.510	1.560	X89	1.735	.635	X126	2.660
2.810	X39	.485	1.535	X90	1.760	.660	X125	2.635
2.835	X38	.460	1.510	X91	1.785	.685	X124	2.610
2.860	X37	.435	1.485	X92	1.810	.710	X123	2.585
2.885	X36	.410	1.460	X93	1.835	.735	X122	2.560
2.910	X35	.385	1.435	X94	1.860	.760	X121	2.535
2.935	X34	.360	1.410	X95	1.885	.785	X120	2.510
2.960	X33	.335	1.385	X96	1.910	.810	X119	2.485
2.985	X32	.310	1.360	X97	1.935	.835	X118	2.460
3.010	X31	.285	1.335	X98	1.960	.860	X117	2.435
3.035	X30	.260	1.310	X99	1.985	.885	X116	2.410
3.060	X29	.235	1.285	X100	2.010	.910	X115	2.385
3.085	X28	.210	1.260	X101	2.035	.935	X114	2.360
3.110	X27	.185	1.235	X102	2.060	.960	X113	2.335
3.135	X26	.160	1.210	X103	2.085	.985	X112	2.310
3.160	X25	.135	1.185	X104	2.110	1.010	X111	2.285
3.185	X24	.110	1.160	X105	2.135	1.035	X110	2.260
3.210	X23	.085	1.135	X106	2.160	1.060	X109	2.235
3.235	X22	.060	1.110	X107	2.185	1.085	X108	2.210

BOTTOM EDGE OF CARD

TOP EDGE OF CARD

TABLES

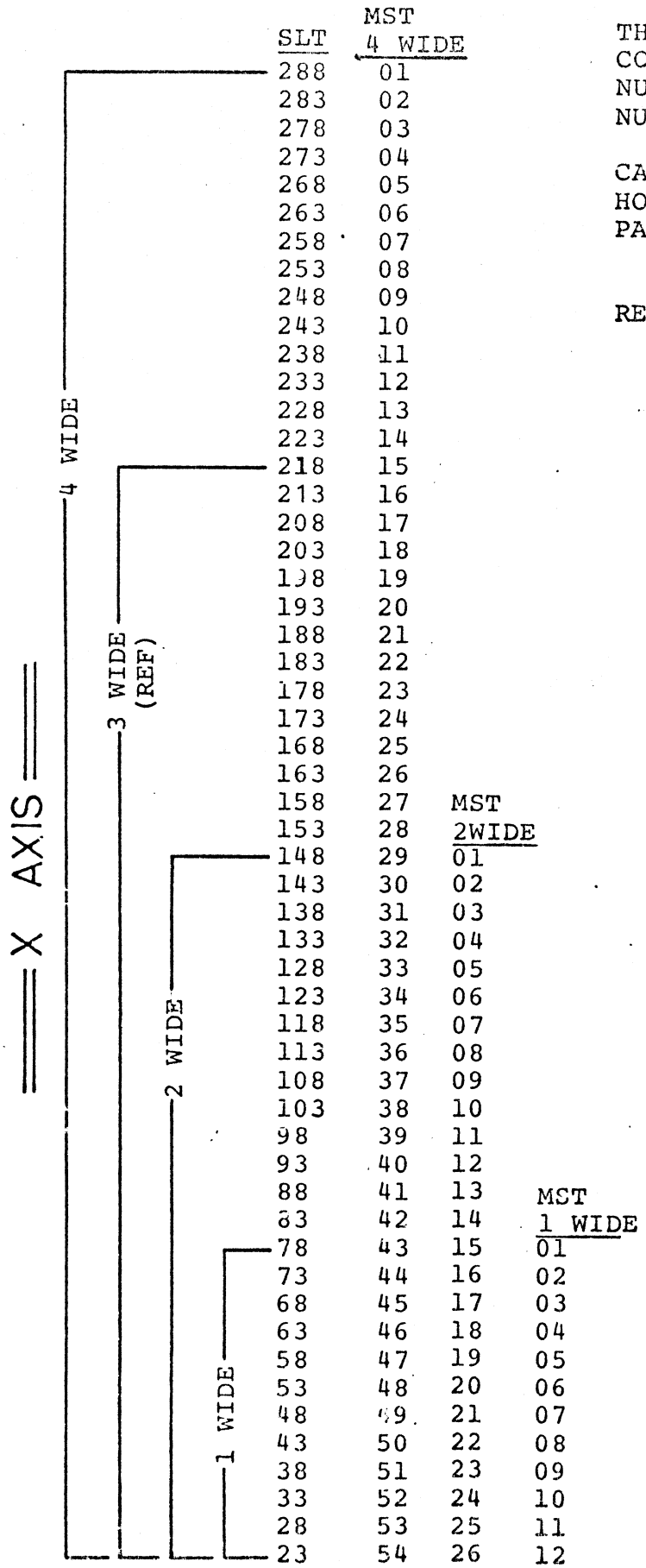
SLT Y grid distances by decimal and .025 increment. This Table may be used for checking and layout of card assemblies.

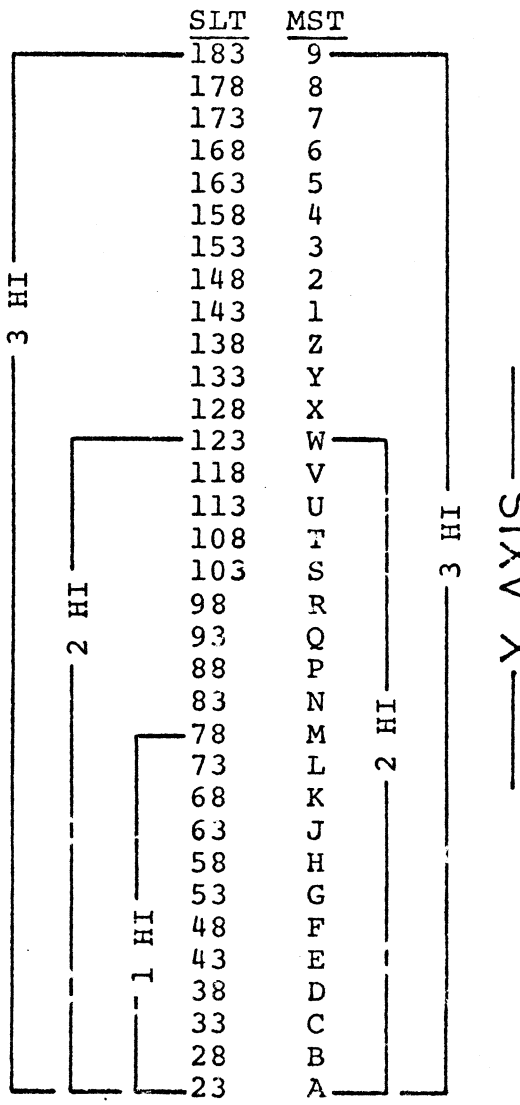
		RIGHT EDGE OF CARD						LEFT EDGE OF CARD		
2.763	Y75	1.375	2.738	Y76	1.400	.038	Y184	4.100
2.780	Y74	1.350	2.713	Y77	1.425	.063	Y183	4.075
2.813	Y73	1.325	2.688	Y78	1.450	.088	Y182	4.050
2.838	Y72	1.300	2.663	Y79	1.475	.113	Y181	4.025
2.863	Y71	1.275	2.638	Y80	1.500	.138	Y180	4.000
2.888	Y70	1.250	2.613	Y81	1.525	.163	Y179	3.975
2.913	Y69	1.225	2.588	Y82	1.550	.188	Y178	3.950
2.938	Y68	1.200	2.563	Y83	1.575	.213	Y177	3.925
2.963	Y67	1.175	2.538	Y84	1.600	.238	Y176	3.900
2.988	Y66	1.150	2.513	Y85	1.625	.263	Y175	3.875
3.013	Y65	1.125	2.488	Y86	1.650	.288	Y174	3.850
3.038	Y64	1.100	2.463	Y87	1.675	.313	Y173	3.825
3.063	Y63	1.075	2.438	Y88	1.700	.338	Y172	3.800
3.088	Y62	1.050	2.413	Y89	1.725	.363	Y171	3.775
3.113	Y61	1.025	2.388	Y90	1.750	.388	Y170	3.750
3.138	Y60	1.000	2.363	Y91	1.775	.413	Y169	3.725
3.163	Y59	.975	2.338	Y92	1.800	.438	Y168	3.700
3.188	Y58	.950	2.313	Y93	1.825	.463	Y167	3.675
3.213	Y57	.925	2.288	Y94	1.850	.488	Y166	3.650
3.238	Y56	.900	2.263	Y95	1.875	.513	Y165	3.625
3.263	Y55	.875	2.238	Y96	1.900	.538	Y164	3.600
3.288	Y54	.850	2.213	Y97	1.925	.563	Y163	3.575
3.313	Y53	.825	2.188	Y98	1.950	.588	Y162	3.550
3.330	Y52	.800	2.163	Y99	1.975	.613	Y161	3.525
3.363	Y51	.775	2.138	Y100	2.000	.638	Y160	3.500
3.388	Y50	.750	2.113	Y101	2.025	.663	Y159	3.475
3.413	Y49	.725	2.088	Y102	2.050	.688	Y158	3.450
3.438	Y48	.700	2.063	Y103	2.075	.713	Y157	3.425
3.463	Y47	.675	2.038	Y104	2.100	.738	Y156	3.400
3.488	Y46	.650	2.013	Y105	2.125	.763	Y155	3.375
3.513	Y45	.625	1.988	Y106	2.150	.788	Y154	3.350
3.538	Y44	.600	1.963	Y107	2.175	.813	Y153	3.325
3.563	Y43	.575	1.938	Y108	2.200	.838	Y152	3.300
3.588	Y42	.550	1.913	Y109	2.225	.863	Y151	3.275
3.613	Y41	.525	1.888	Y110	2.250	.888	Y150	3.250
3.638	Y40	.500	1.863	Y111	2.275	.913	Y149	3.225
3.663	Y39	.475	1.838	Y112	2.300	.938	Y148	3.200
3.688	Y38	.450	1.813	Y113	2.325	.963	Y147	3.175
3.713	Y37	.425	1.788	Y114	2.350	.988	Y146	3.150
3.738	Y36	.400	1.763	Y115	2.375	1.013	Y145	3.125
3.763	Y35	.375	1.738	Y116	2.400	1.038	Y144	3.100
3.788	Y34	.350	1.713	Y117	2.425	1.063	Y143	3.075
3.813	Y33	.325	1.688	Y118	2.450	1.088	Y142	3.050
3.838	Y32	.300	1.663	Y119	2.475	1.113	Y141	3.025
3.863	Y31	.275	1.638	Y120	2.500	1.138	Y140	3.000
3.888	Y30	.250	1.613	Y121	2.525	1.163	Y139	2.975
3.913	Y29	.225	1.588	Y122	2.550	1.188	Y138	2.950
3.938	Y28	.200	1.563	Y123	2.575	1.213	Y137	2.925
3.963	Y27	.175	1.538	Y124	2.600	1.238	Y136	2.900
3.988	Y26	.150	1.513	Y125	2.625	1.263	Y135	2.875
4.013	Y25	.125	1.488	Y126	2.650	1.288	Y134	2.850
4.038	Y24	.100	1.463	Y127	2.675	1.313	Y133	2.825
4.063	Y23	.075	1.438	Y128	2.700	1.338	Y132	2.800
4.088	Y22	.050	1.413	Y129	2.725	1.363	Y131	2.775
						1.388	Y130	2.750

THE FOLLOWING ILLUSTRATION IS FOR CORRELATION BETWEEN THE MST (ALPHA-NUMERIC) AND SLT (NUMERIC) GRID NUMBERING SYSTEMS.

CARD SIZES SHOWN ARE BASED ON CORNER HOLE LOCATIONS FOR STANDARD HOLE PATTERNS.

REF- INDICATES MANUAL SLT ASSEMBLY DRAWING ONLY





TABLES

DISTANCE FROM LEFT CARD EDGE		Y GRID DISTANCES BY DECIMAL AND .125 INCREMENTS	DISTANCE FROM RIGHT CARD EDGE
MST 2 HIGH	3 HIGH	GRID	MST 1, 2 AND 4 WIDE
2.575	4.075	A	.075
2.450	3.950	B	.200
2.325	3.825	C	.325
2.200	3.700	D	.450
2.075	3.575	E	.575
1.950	3.450	F	.700
1.825	3.325	G	.825
1.700	3.200	H	.950
1.575	3.075	J	1.075
1.450	2.950	K	1.200
1.325	2.825	L	1.325
1.200	2.700	M	1.450
1.075	2.575	N	1.575
.950	2.450	P	1.700
.825	2.325	Q	1.825
.700	2.200	R	1.950
.575	2.075	S	2.075
.450	1.950	T	2.200
.325	1.825	U	2.325
.200	1.700	V	2.450
.075	1.575	W	2.575
	1.450	X	2.700
	1.325	Y	2.825
	1.200	Z	2.950
	1.075	1	3.075
	.950	2	3.200
	.825	3	3.325
	.700	4	3.450
	.575	5	3.575
	.450	6	3.700
	.325	7	3.825
	.200	8	3.950
	.075	9	4.075

DISTANCE FROM TOP CARD EDGE MST 1, 2 AND 4 WIDE	X GRID DISTANCES BY DECIMAL AND .125 INCREMENTS GRID	4 WIDE	2 WIDE	DISTANCE FROM BOTTOM CARD EDGE 1 WIDE
.085	01	6.710	3.210	1.460
.210	02	6.585	3.085	1.335
.335	03	6.460	2.960	1.210
.460	04	6.335	2.835	1.085
.585	05	6.210	2.710	.960
.710	06	6.085	2.585	.835
.835	07	5.960	2.460	.710
.960	08	5.835	2.335	.585
1.085	09	5.710	2.210	.460
1.210	10	5.585	2.085	.335
1.335	11	5.460	1.960	.210
1.460	12	5.335	1.835	.085
1.585	13	5.210	1.710	
1.710	14	5.085	1.585	
1.835	15	4.960	1.460	
1.960	16	4.835	1.335	
2.085	17	4.710	1.210	
2.210	18	4.585	1.085	
2.335	19	4.460	.960	
2.460	20	4.335	.835	
2.585	21	4.210	.710	
2.710	22	4.085	.585	
2.835	23	3.960	.460	
2.960	24	3.835	.335	
3.085	25	3.710	.210	
3.210	26	3.585	.085	
3.335	27	3.460		
3.460	28	3.335		
3.585	29	3.210		
3.710	30	3.085		
3.835	31	2.960		
3.960	32	2.835		
4.085	33	2.710		
4.210	34	2.585		
4.335	35	2.460		
4.460	36	2.335		
4.585	37	2.210		
4.710	38	2.085		
4.835	39	1.960		
4.960	40	1.835		
5.085	41	1.710		
5.210	42	1.585		
5.335	43	1.460		
5.460	44	1.335		
5.585	45	1.210		
5.710	46	1.085		
5.835	47	.960		
5.960	48	.835		
6.085	49	.710		
6.210	50	.585		
6.335	51	.460		
6.460	52	.335		
6.585	53	.210		
6.710	54	.085		