

Application of cross-sectional transmission electron microscopy to thin-film-transistor failure analysis

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The locations of process-induced defects in hydrogenated amorphous silicon thin-film transistors (a-Si:H TFTs), which are used as elements of active-matrix liquid crystal displays, were investigated by combining focused ion beam (FIB) techniques with cross-sectional transmission electron microscopy (X-TEM). The FIB technique is applied to TFT failure-analysis problems which require very localized etching without inducing mechanical stress. We demonstrate how these techniques are used to characterize TFT defects such as thin layers formed from etching residue, microvoids in the multilayers, fragile aluminum whisker protrusions on the electrodes, or portions of the TFT multilayer damaged by mechanical stress.

Introduction

Hydrogenated amorphous silicon thin-film transistors (a-Si:H TFTs) are now widely used as elements in active-matrix liquid crystal displays (AMLCDs). As the

complexity of the TFT device structure has increased, the elimination of process-induced defects formed during TFT fabrication has become more critical to device performance, reliability, and manufacturing cost. If a part of a process in manufacturing is faulty and the cause of failure is not specifically identified, the entire process is usually investigated. To minimize this effort, it is important to determine how defects can be unintentionally introduced during TFT fabrication, and to identify the failure mechanisms. Usually only a few TFT defects occur on an array. In order to detect the defects, all pixels of a TFT/LCD array are electrically tested. A TFT array electrical test method [1-3] is used to characterize the array which detects, accurately locates, and identifies pixel faults in multilayered TFT structures.

When process-induced defects are located electrically in crystalline semiconductor devices, cross-sectional transmission electron microscopy (X-TEM) samples are often prepared for characterization of the defects [4]. The conventional method for preparing X-TEM samples consists of mounting a sample with, e.g., an epoxy resin at temperatures below 100°C onto a holder, mechanically

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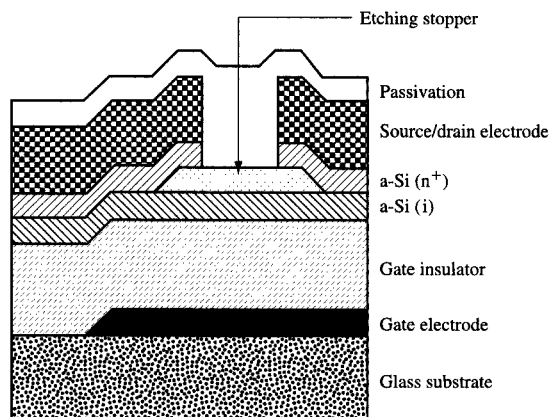


Figure 1

Schematic cross section of a TFT.

dicing the sample using a low-speed saw, thinning by mechanical polishing, dimpling, and low-angle ion milling at about 3 kV. For nanometer-scale failures located in a TFT multilayer, X-TEM samples must be prepared in which all the layers are viewed simultaneously. However, X-TEM is rarely used to study multilayer TFT nanostructures because formation of thin, fragile glass X-TEM samples is difficult and because the thermal and mechanical stresses imposed by this preparation method can degrade the multilayer structure. In structures with fragile components, such as a-Si:H TFT multilayers on glass, it is particularly important to distinguish device failures due to multilayer processing from artifacts such as ion/electron irradiation damage incurred during sample preparation. For these fragile structures, sample preparation and handling, rather than X-TEM characterization, can become the most important part of failure analysis.

An alternative approach to X-TEM sample preparation consists of using a focused ion beam (FIB) etching technique [5–16]. A FIB etches samples at high speeds and does not mechanically damage fragile samples [3, 5–16]. A FIB of sufficient power can etch a local area of a sample to create a thin wall without mechanical breakdown. One of the valuable features of using a FIB is that it eliminates the conventional gluing process from the procedure for X-TEM sample fabrication, thereby reducing the failure rate in sample preparation. Although FIB etching has recently been used for preparing fragile porous silicon X-TEM samples on silicon substrates [16], it has rarely been used for TFT structures on glass

substrates because of potential difficulties in sample preparation.

In this paper, we describe an extension of the application of FIB sample preparation and X-TEM characterization to TFT samples on a glass substrate. The samples are prepared by the FIB technique without inducing mechanical stress or damage at fragile failure locations.

The X-TEM studies illustrate how defective TFTs can include thin layers formed from etching residue and may have microvoid defects in their multilayers, fragile protrusions such as aluminum (Al) whiskers on the electrodes, and portions of the transistor multilayer damaged by mechanical stress.

TFT structure and failure analysis

A schematic cross section of an inverted staggered TFT is shown in **Figure 1**. The TFT is formed by depositing 10 or more nanometer-scale films of various materials, and fabricating it in a $10\text{--}20\text{-}\mu\text{m}^2$ area on a glass substrate. The individual layers in the TFT structure shown in Figure 1 may be composites formed from more than one film deposition. The morphology of an entire TFT is complex, and its total thickness ranges from 800 to 1500 nm. Typical layer thicknesses of the various metal and semiconductor layers range from 50 to 400 nm. The transistor fabrication process begins with the sputtering of gate metal (e.g., Al) onto the glass substrate. In the fabrication of TFTs, the gate insulator (silicon oxide or nitride), the active layer a-Si:H, and the etch stop are deposited consecutively in a plasma-enhanced chemical vapor deposition reactor. The source/drain electrodes (e.g., Al) and passivation layer (silicon nitride) are then fabricated, and a total of seven photolithographic masking processes are typically used. The total number of TFTs on a 12.1-in.-diagonal array is over two million for a color XGA (extended graphics array) resolution display ($1024 \times 768 \times 3$).

The TFT failure modes may be divided into two main groups: those associated with the fabrication process and those that arise during TFT usage. Many of the failures in the first group are catastrophic, and the anomalies are promptly detected during the manufacturing process, while most of the failures in the second group only become apparent after long periods of use in the field. The manufacturing yield of a TFT array that suffers from a processing-related problem can often be improved by isolating that stage of the manufacturing process in which the defects are introduced, and then detecting and correcting the faulty process.

FIB sample preparation for X-TEM

Each sample is cut into sections perpendicular to the layer, using a low-speed saw, and is reduced to a thickness

of 30 μm by precise mechanical polishing with a tripod-type polisher [15, 16] and a diamond-lapping film. The polished glass sample is mounted on a semicircular TEM grid. This shape allows both thinning from above and observation from a direction perpendicular to the wall.

In the Micrion 9000 FIB system, focused ions are produced using the system shown schematically in Figure 2. A gallium (Ga) liquid metal ion gun is capable of producing an ion-beam diameter with a resolution of 25 nm. The ion gun typically operates over a voltage range of 20 to 30 keV, but may be as high as 50 keV, depending upon the FIB instrument and application. An incident ion beam is focused on a small spot on a target specimen. To maintain performance and prevent contamination, the FIB requires a high vacuum (10^{-7} Torr).

The focused ions have sufficient energy to etch a small area of a specimen. The area to be etched is scanned with the incident ion beam. We can easily determine the area on the display, which shows the scanning ion or electron image of the sample surface, by drawing a rectangle on the screen image. The digital electronics automatically controls the focus, astigmatism, contrast, brightness, and other parameters that influence the quality of the image. The probe current is a critical parameter that governs the surface texture of the thin wall. Three main currents are typically used: 7.5 nA for the initial rough etching, 360 pA for the intermediate etching, and 60 pA for the final etching. The wall to be etched requires a taper angle correction because of the Gaussian beam profile. During FIB etching, the sample is tilted a few degrees toward the incident beam direction. Ion-beam-assisted deposition of an amorphous tungsten (a-W) film at the etching site prevents excessive etching. Electrical charging of a nonconducting specimen in a thin glass sample induced by the incident ion beam is reduced by sputter-coating the surface with a conducting metal such as gold (Au). It is also possible to electrically neutralize the FIB to prevent the sample from charging. A schematic illustration of a TEM sample etched by the FIB technique is shown in Figure 3.

Note that when the high-vacuum environment in the chamber is opened to atmospheric pressure, it is necessary to avoid fracture of the fragile sample. In most equipment, the pressure of the purge gas is too high for the fragile TEM specimen, which has a wall that is less than 50 nm thick. We have had some experience with fragile portions of the thin wall being blown out by the purge gas. To minimize the risk of breakdown of the sample, the pressure of the purge gas was manually reduced by using the control valve.

The total sample-preparation time, including the time for FIB etching, is only 1.5 hours under the worst conditions. This makes it possible to create five or more X-TEM samples per day. This is a considerably higher

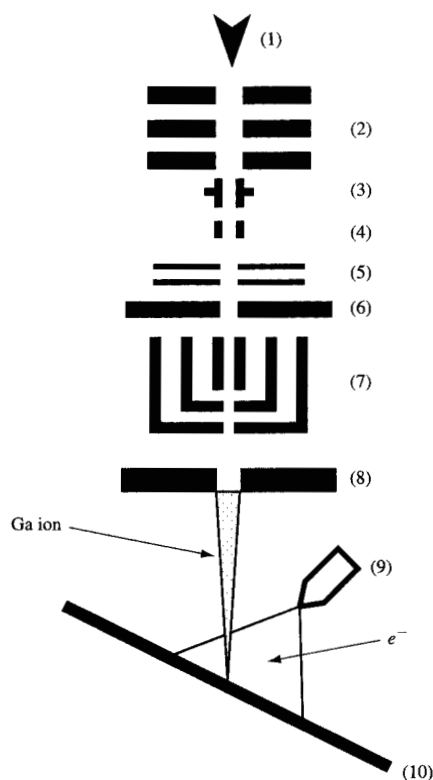


Figure 2

Beam paths in the FIB system: (1) Ga liquid metal ion source; (2) lens 1; (3) beam-limiting aperture; (4) blanking plates; (5) blanking aperture; (6) pre-lens deflectors; (7) lens 2; (8) microchannel plate; (9) charge neutralizer; (10) specimen surface.

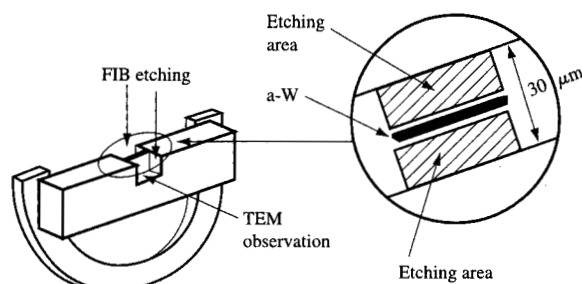


Figure 3

Schematic illustration of a sample prepared for cross-sectional transmission electron microscopy (X-TEM) observation.

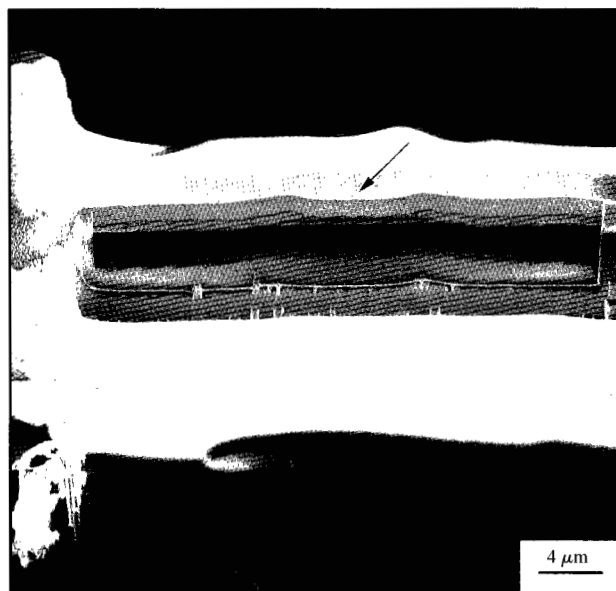


Figure 4

SEM image of a thin wall etched by FIB for X-TEM observation.

number of samples than with the conventional sample-preparation method.

Figure 4 shows a scanning electron microscope (SEM) image of a thin wall (center of figure) in a region of electron transparency just after FIB etching. TFT arrays are laser-marked in the vicinity of detected faulty TFTs, so that they become clearly visible as a result of a film color change caused by combustion. Structural analysis (X-TEM) was performed with a JEOL JEM-4000 FX electron microscope operated at 400 keV.

Results and discussion

Here we provide examples of how the FIB and X-TEM techniques have been effectively used to detect TFT defects and failure modes.

• Thin extra layer formed by etching residue

We first consider the case in which a thin extra layer exists as an etching residue in TFT multilayers. If the nanostructure of each individual metallization layer is not revealed in a cross-sectional image, each processing stage must be examined to determine the faulty stage of such a complex process.

Figures 5(a) and 5(b) show schematic illustrations of thin extra layers that can be caused by etching residues. In **Figure 5(a)**, there is an extra layer located under the a-Si (n^+) layer, and in **Figure 5(b)** there is one on top of the a-Si (n^+) layer. It is generally not possible to determine

the location of the extra layer by electrical measurement or by optical microscopy, since the overlying metal layer is not optically transparent. TEM analysis allows the morphology of even the very thin, difficult-to-detect contamination layers to be investigated. **Figures 6(a) and 6(b)** show cross-sectional bright-field TEM micrographs of TFT samples corresponding to the schematic diagrams shown in **Figures 5(a) and 5(b)**. In both examples in **Figure 6**, the thin extra layers are clearly visible: One lies under the a-Si (n^+) layer, as shown in **Figure 6(a)**, and the other lies on top of the a-Si (n^+) layer, as shown in **Figure 6(b)**. Both extra layers have a thickness of 10–30 nm. Ultrathin-window/energy-dispersive X-ray spectroscopy (UTW/EDX) used to identify the elements in the extra layer indicates that only silicon and oxygen peaks are

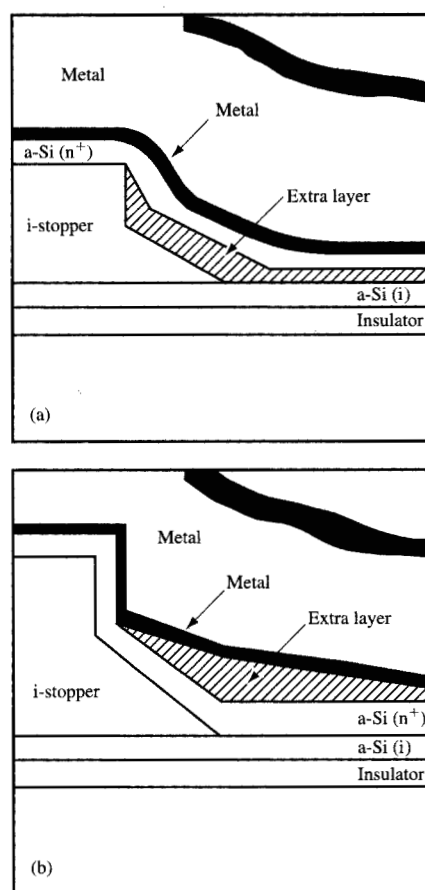


Figure 5

Schematic illustrations of the thin extra layers that can be caused by etching residues: (a) on an a-Si (i) layer; (b) on an a-Si (n^+) layer.

present in each layer; thus, we identify these extra layers as etching residues. These layers lead to contact failure. A comparison between X-TEM manufacturing sample micrographs and those shown in Figure 6 provides a mechanism to determine whether the manufacturing processes have been correctly carried out.

• *Microvoid formation by degassing*

During the manufacturing process, TFT arrays can occasionally form microvoids as a consequence of slightly malfunctioning processing equipment. It is difficult to trace such failures back to processing steps, because the TFTs usually fail as a result of gradual degradation mechanisms in the metallization or within the TFT material itself.

Figure 7(a) shows a bright-field X-TEM micrograph that includes microvoids in the silicon nitride layer (X) on the

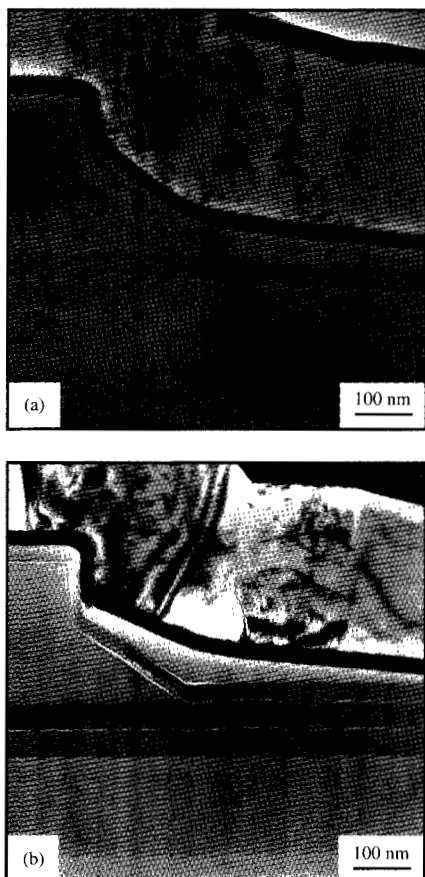


Figure 8

Bright-field X-TEM micrographs corresponding to the examples in Figures 5(a) and 5(b).

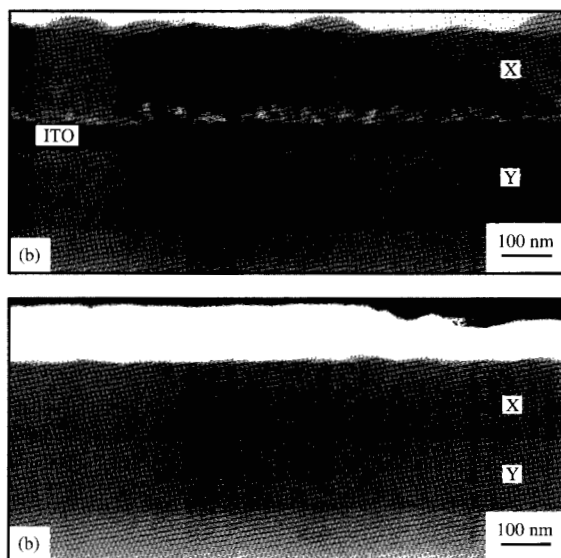


Figure 7

Bright-field X-TEM micrographs: (a) Those in which ITO exists between layers X and Y, and microvoids are clearly seen on the ITO layer; (b) those in which ITO is absent in the same sample.

indium-tin oxide (ITO) layer. These microvoids are not visible with an optical microscope. **Figure 7(b)** shows a bright-field X-TEM micrograph corresponding to the same sample in Figure 7(a), but in a region in which the ITO layer is absent. Here, we do not see an anomaly in the interface between layer X and the silicon nitride layer (Y). This is evidence that the microvoids were formed during the deposition of layer X. In addition, it can be clearly seen that these microvoids degrade the surface morphology of layer X. The microvoids were produced as a result of degassing from the ITO layer, and the ITO itself was imperfectly sputter-deposited during fabrication. This example shows how X-TEM identifies the internal structure of the TFT and provides a rapid means of detecting metallization defects.

• *Electrical leakage path created by etchant attack*

One advantage of FIB etching as a technique for TEM sample preparation is that it can produce a thin wall by controlling the etching parameters. In extreme cases of actual TFT failure analysis, we must reduce the thickness of the thin wall to the limit (i.e., to the point at which the sample breaks down). Direct observation of a nanoscale electrically conductive leak path generated during manufacturing processes is possible only with X-TEM

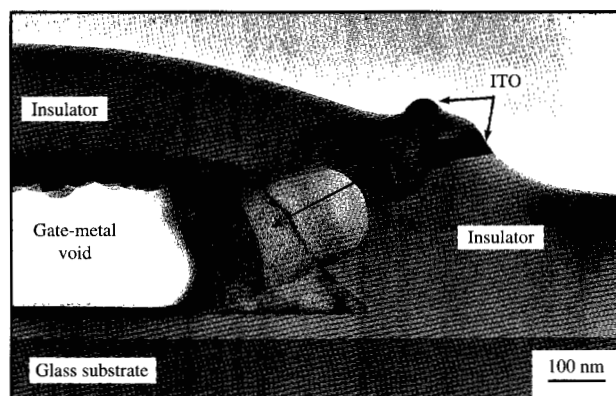


Figure 8

Bright-field X-TEM micrograph of an electrical leak path caused by etchant attack.

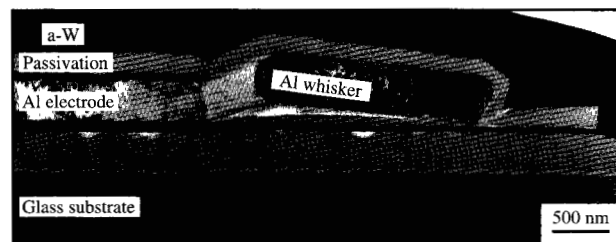
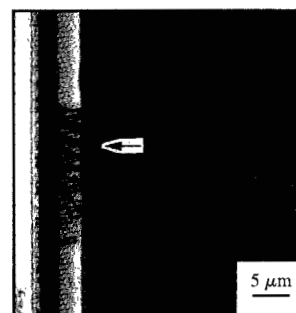


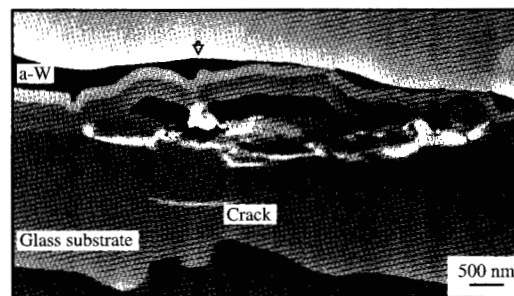
Figure 9

Bright-field X-TEM micrograph of an Al whisker produced by stress migration [17].

techniques. **Figure 8** shows an example of an X-TEM image in a short-circuit region of a TFT with the upper region of the sample removed by FIB etching during sample preparation. The fragile edges of the microvoid in the gate metal, which are produced by etchant attack, and the leak path through the gate insulator located between the residual MoTa gate metal and ITO (pixel-electrode) electrodes are clearly observable. The sample thickness is about 40 nm. The region of uneven contrast between the gate metal and the ITO electrode shows that the damage caused by the etchant attack must have caused dissolution in the insulator (center of the leak path indicated by an arrow in Figure 8). The spotted black contrast also indicates dissolved gate metal and ITO. This damaged region is revealed as the electrical leak path in such an X-TEM image. Despite its small size, the damaged structure, where the length of the leak path is as short as



(a)



(b)

Figure 10

(a) Optical micrograph of a faulty conductor track. (b) Bright-field X-TEM micrograph corresponding to the position indicated by the arrow in Figure 10 (a).

300 nm and the width is 200 nm, is detected because of the high TEM resolution.

● Aluminum whiskers caused by stress migration

We have detected defects caused by processing within TFT multilayers in X-TEM samples prepared using FIB. Using X-TEM, we next present an example in which Al migration occurs from an Al gate electrode during the manufacturing process and TFT device operation [17].

Figure 9 shows an example of a large Al whisker. This X-TEM micrograph illustrates that Al migration is a practical problem that can occur with TFT Al metallization and cause short circuits. The crystallographic relation between the whisker and the original thin film is revealed by X-TEM. In this case, the Al whisker is polycrystalline.

It is unlikely that electromigration causes the polycrystalline Al transport because of the relatively low current density in the TFT conductor layer. Instead, it is important to consider stress migration of Al in TFT applications, since large mechanical stresses exist in thin films deposited on an LCD-grade large glass substrate. Al whiskers produced by stress migration can easily produce a

short-circuit path between adjacent conductor tracks, which is an important mode of stress migration failure.

• *TFT multilayer damaged by mechanical stress*

Particularly interesting results have been obtained in protrusions created in a conductor track during the manufacturing process. **Figure 10(a)** shows an optical microscope image of protrusions on a conducting signal line from which an electrical open circuit is detected. **Figure 10(b)** shows a bright-field X-TEM micrograph of an example of FIB etching corresponding to the position indicated by the arrow in Figure 10(a). The internal TFT structure can be clearly seen with nanometer resolution. The damaged point and the propagation paths of the damage are indicated by the arrows in Figure 10(b). A semicircular microvoid is evidence of pinpoint mechanical damage. In this case, the glass substrate was intentionally damaged mechanically before deposition. These observations suggest that the observed damage in the X-TEM micrograph does not typically occur during sample preparation.

Concluding remarks

Several examples of TFT processing defects have been identified from X-TEM studies. To obtain the X-TEM samples for failure analysis of the TFTs on glass substrates, FIB etching was used to prepare the samples. Mechanical damage to the X-TEM specimens due to FIB etching was not detected in micrographs of the samples with processing defects. These X-TEM samples illustrate the formation of thin layers of etchant residue, microvoids inside multilayers of TFTs, fragile protrusions such as Al whiskers, and portions damaged by mechanical stress. The results have demonstrated the use of FIB etching for rapid X-TEM sample preparation for failure analysis in TFTs. X-TEM micrographs of an etched sample can precisely determine the stage of the manufacturing process in which a fault has occurred. The combination of FIB etching and X-TEM provides flexibility in the control of the sample preparation conditions, allowing rapid and precise failure analysis of TFTs.

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