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Response Time of Thyristors: Theoretical Study and Application to Electronic Switching Networks

Abstract: After restating the experimental definition of the response time of a low-power thyristor by assuming a well-defined dc triggering current, the authors show that the equivalent two-transistor representation of the thyristor leads to a theoretical interpretation of the triggering condition under certain simplifying assumptions. The accuracy of this theoretical model is shown to be satisfactory.

A practical definition of the response time of a thyristor is proposed, and the literal expression of the response time as a function of the parameters of both constituent transistors is given. Examples of application are then given in the design of the switching networks of the IBM 2750, where thousands of thyristors are used as crosspoints arranged in matrices and connected in series.

Symbols

β_1, β_2 = Common emitter current gain of the npn or pnp transistor
C_2 = Base-collector junction capacitance
D_p = Hole diffusion constant in the n_1 region
g = Gate current
g_0 = dc triggering current ($g_0 \simeq i_0$)
$G = \frac{g - i_0}{i_0}$ = normalized effective gate current [see Eq. (3-4)]
i_0 = Current in the shunting resistance R [see Eq. (1-1)]
i_1, i_2 = Collector current of the npn or pnp transistor
I_1, I_2 = Collector current of the npn or pnp transistor normalized by i_0
$\bar{i}$ = Laplace transform of the function $i(t)$
i_k = Cathode current
K = $\beta_1\beta_2 - 1$, overlatching factor
p = Laplace operator
p_1 = Positive root of the characteristic equation (3-8)
p_2 = Negative root of the characteristic equation (3-8)
q = Electron charge
R = Gate-cathode shunting resistor
t = Time
T_1, T_2 = Common emitter time constant of the npn or pnp transistor
θ = Duration of the gate pulse
$\tau = \frac{1}{p_1}$ = Response time of the thyristor [see Eqs. (1-2) and (3-13)]

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1. Introduction

The triggering sensitivity of a low-power, high-speed thyristor depends on two parameters: (1) the *response time* τ of the thyristor, and (2) the *gate-to-cathode resistance* R. The response time τ has been defined in a previous publication.[1] The thyristor is turned ON by a short current pulse applied to its gate. The direct current necessary to trigger the device is

$$g_0 \simeq i_0 = \frac{V_{GK}}{R}, \tag{1-1}$$

where V_{GK} is the gate-to-cathode voltage in the conducting state. When short pulse durations are considered, the triggering condition becomes, according to Fig. 1,

$$\theta \frac{g - i_0}{i_0} = \tau, \tag{1-2}$$

where *the response time τ is independent of i_0 and is thus a characteristic of the thyristor.*

The first purpose of this paper will be, under some simplifying assumptions,* to give a more general expression than that in Ref. 1 for the triggering condition and an expression for the response time τ as a function of the parameters of both constituent transistors, and to complete the theoretical work done by other authors on the turn-on process in the thyristor.[2-5]

*Particularly, the assumption of a well-defined threshold gate triggering current.

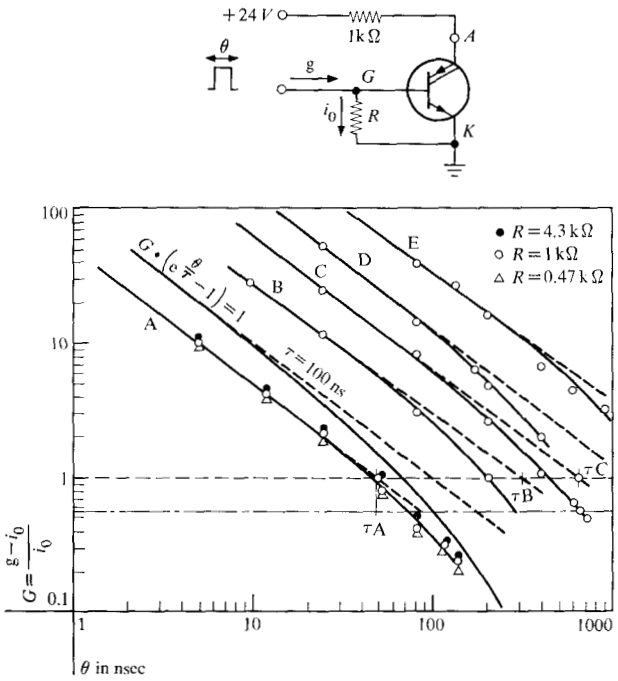


Figure 1 Triggering sensitivity of thyristors: $G(\theta)$ curves.

The second purpose is to show the usefulness of this notion of response time in the design of circuits where fast parasitic transients may exist and where the triggering condition must be tightly controlled. This situation is found particularly in an electronic switching network using thyristors as crosspoints.[6]

2. Discussion of the basic hypotheses

The theoretical approach to the problem will employ an idealized representation of the thyristor (Fig. 2), assuming some hypotheses which are discussed below.

A) The two-transistor representation[4] of the thyristor implies good geometrical homogeneity of the device; this assumption is realistic when small area junctions are considered, because in that case two-dimensional effects[4,5,7] either do not appear or can be ignored in the first approximation. For planar thyristors it must be noted that the equivalent circuit[8] contains a double structure: a lateral $p_1n_1p_2$ plus a vertical $n_2p_2n_1$ transistor and a p_1n_1 diode plus the $n_2p_2n_1$ transistor. Only the former structure exhibits the thyristor characteristics and is to be considered here.

B) Transistor gains

1) The presence of a resistor connected between gate and cathode, i.e., the case of the shorted or shunted emitter,[4] permits an interesting simplifying assumption concerning the variations in current gain of

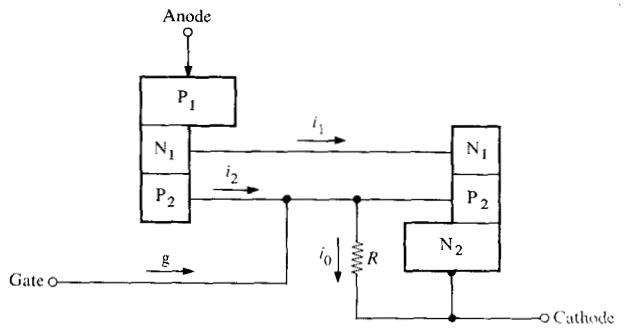


Figure 2 Two-transistor representation of a thyristor.

both complementary transistors. Indeed the resistance R is so chosen as to make the shunted current given by (1-1), $i_0 = V_{GK}/R$, much higher than the actual npn transistor base current for which the current gain reaches its constant value. This fact leads us to consider, contrary to what is supposed usually,[9] that *the dc common emitter current gains β are independent of the current* and have only discrete values:

For the npn transistor

$$\left.\begin{aligned} &\beta_1 = 0 \text{ for } g \leq i_0 \text{ or } i_k \leq i_0 \\ &\text{and} \\ &\beta_1 = \text{constant} = 0 \text{ for } g > i_0 \text{ or } i_k > i_0. \end{aligned}\right\} \quad (2\text{-}1)$$

For the pnp transistor

$$\beta_2 = \text{constant}.$$

This assumption is valid when moderate currents are considered; inasmuch as we are interested in the triggering condition, we limit our study to the period when triggering is not terminated and when collector currents are less than 20 mA.

2) Furthermore, we make the assumption that i_0 is a constant as soon as a current is flowing into the base of the npn transistor ($g > i_0$); in other words we assume that V_{GK} = constant = 0.6 V for silicon and neglect the dynamic impedance of the forward biased p_2n_2 junction.

3) Last, we shall also consider that current gains are independent of collector voltages. In fact, the anode-to-cathode voltage of the thyristor does not vary by more than 20% before the cumulative triggering process appears (Fig. 3).

C) After the beginning of the triggering process, the common base-collector junction J_2 is reverse-biased and the base-emitter junction is forward-biased: *the npn and pnp transistors operate Class A*. We can assume that both transistors operate Class A during the whole

period during which there is no certainty that the thyristor has been turned ON. When the junction J_2 becomes forward-biased, the switch has certainly been turned ON since this is the pnpn switch basic turn-on property.[4]

D) The triggering condition of the thyristor will be determined from the response of each of the two transistors. The response delays of the transistors themselves are being neglected. In general, the transfer function of a circuit containing a grounded-emitter transistor with a resistive load R_L has the form[10-12]

$$\beta^* = \frac{\beta}{(1 + pT_1')(1 + pT_2')}, \tag{2-2}$$

where p is the Laplace operator. However, in the particular cases of the $n_2p_2n_1$ and $p_1n_1p_2$ transistors, one time constant predominates and the responses of each of the transistors can be approximated by a single exponential of the form

$$i_c = \beta i_b(1 - e^{-t/T}). \tag{2-3}$$

The corresponding transfer function is

$$\beta^* = \frac{\beta}{1 + pT}. \tag{2-4}$$

Specifically, for the high-speed $n_1p_1n_2$ transistor $T = T_1$ is determined principally by the Miller-effect feedback capacitance C_2 from collector to base:

$$T_1 = (1 + \beta_1)R_LC_2. \tag{2-5}$$

For the low-speed and low-gain $p_1n_1p_2$ transistor, $T = T_2$ is essentially the lifetime of the holes in the n_1 region:

$$T_2 = \frac{1}{2\pi f_T} = \beta_2 \frac{W_{n1}^2}{2D_p}, \tag{2-6}$$

where W_{n1} is the base width and D_p the hole diffusion constant in the n_1 region.[13]

3. Triggering condition

3.1 *Equation of the triggering process.* During triggering, when the transistors are in the active region, from the two-transistor model (Fig. 2) we may write the following equations:[2,3]

$$\bar{i}_1 = \beta_1^* (\overline{g + i_2 - i_0}), \tag{3-1}$$

$$\bar{i}_2 = \beta_2^* \bar{i}_1, \tag{3-2}$$

where $\bar{i}_1$, $\bar{i}_2$ . . . .are the Laplace transforms of the collector currents and the index "1" indicates the npn transistor and "2" the pnp transistor.

After introduction of the collector currents normalized by the constant current i_0,

$$I = i/i_0, \tag{3-3}$$

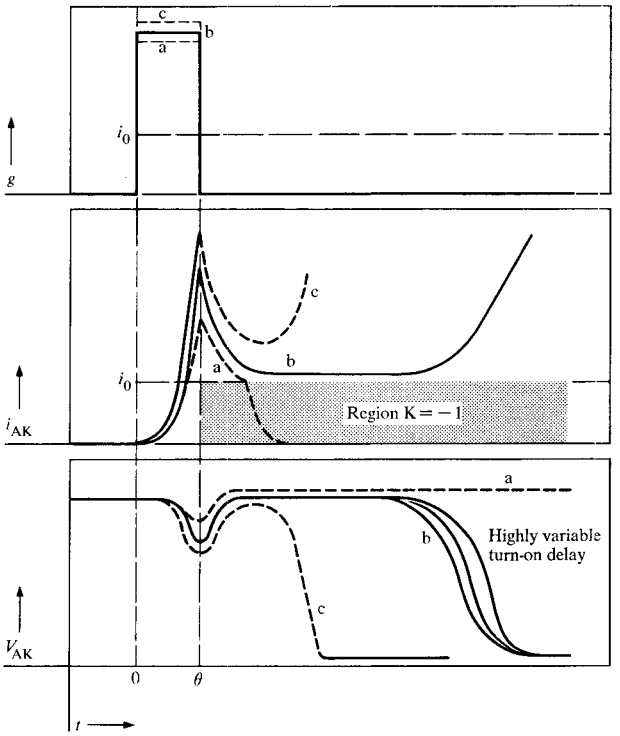


Figure 3 Voltage and current variations during triggering. (a) Below the limit of the triggering, (b) at the limit, and (c) above the limit.

and of the *normalized effective gate current*,

$$G = (g - i_0)/i_0, \tag{3-4}$$

we obtain the equation representative of the pnp collector current:

$$T_1T_2p^2\bar{I}_2 + (T_1 + T_2)p\bar{I}_2 - K\bar{I}_2 = \beta_1\beta_2\bar{G}, \tag{3-5}$$

where

$$K = \beta_1\beta_2 - 1 \quad \text{is the } \textit{overlatching factor}, \tag{3-6}$$

and $\bar{G}$ is the Laplace transform of the normalized effective gate pulse.

3.2. *Triggering a thyristor with a rectangular pulse of gate current.* Let G be the current amplitude and θ the pulse duration (Fig. 3):

$$\bar{G} = \frac{1}{p}[G - (G + 1)e^{-\theta p}]. \tag{3-7}$$

If the overlatching factor K is positive ($\beta_1\beta_2 > 1$) the characteristic equation of (3-5),

$$T_1T_2p^2 + (T_1 + T_2)p - K = 0, \tag{3-8}$$

has a *positive root* p_1 and a *negative root* p_2. Then Eqs. (3-5) and (3-7) yield the transfer current

$$\bar{I}_2 = \frac{\beta_1\beta_2}{T_1T_2}\left[\frac{G}{p(p-p_1)(p-p_2)} - \frac{(G+1)e^{-\theta p}}{p(p-p_1)(p-p_2)}\right] \tag{3-9}$$

and the current I_2 can then be written directly (inverse transform)

$$\frac{T_1T_2}{\beta_1\beta_2} I_2 = \frac{1}{p_1p_2}[G - \epsilon(G+1)] + \frac{e^{p_1t}}{p_1(p_1-p_2)}[G - \epsilon(G+1)e^{-p_1\theta}] + \frac{e^{p_2t}}{p_2(p_2-p_1)}[G - \epsilon(G+1)e^{-p_2\theta}], \tag{3-10}$$

where $\epsilon = 0$ for $t < \theta$

$\epsilon = 1$ for $t > \theta$.

The function I_2 is the sum of a constant term, an increasing exponential, and a decreasing exponential. The triggering of the thyristor can occur *only if the coefficient of the increasing term e^{p_1t} is positive after the end of the triggering pulse* ($t > \theta$). Thus the triggering condition takes the simple form:

$$G - (G+1)e^{-p_1\theta} > 0,$$

$$\boxed{G(e^{p_1\theta} - 1) > 1}\ . \tag{3-11}$$

If the pulse duration θ is small enough, the triggering condition corresponds to the relation (1-2): $G\theta > 1/p_1$.

We denote the response time of the thyristor by

$$\tau = \frac{1}{p_1}. \tag{3-12}$$

However, we have to verify that after the end of the gate pulse the minimum value of the normalized pnp collector current (or npn base current I_2) is greater than 1, in order to make sure that according to (2-1) the overlatching factor K remains positive (Fig. 3). The minimum of I_2 occurs at time $t = t_1$ given by

$$\frac{dI_2}{dt} = \frac{\beta_1\beta_2}{T_1T_2}\left[\frac{G - (G+1)e^{-p_1\theta}}{p_1 - p_2}e^{p_1t_1} + \frac{G - (G+1)e^{-p_2\theta}}{p_2 - p_1}e^{p_2t_1}\right] = 0$$

and is

$$I_{2\min} = \frac{\beta_1\beta_2}{K}\{1 + e^{p_1t_1}[G - (G+1)e^{-p_1\theta}]\}.$$

When the triggering condition is fulfilled, I_2 is the product of two numbers greater than 1. Thus relation (3-11) is the effective triggering condition.

3.3. *Response time.* From the expression for response time,

$$\tau = \frac{1}{p_1},$$

we have

$$\tau = \frac{1}{2K}[T_1 + T_2 + \sqrt{(T_1+T_2)^2 + 4KT_1T_2}]. \tag{3-13}$$

Figure 4 gives the values of τ/T_2 vs K, with the ratio $\alpha = T_1/T_2$ as a parameter.

In the particular case where $T_1 \ll T_2$,

$$\tau \simeq \frac{T_2}{K}, \tag{3-14}$$

and with the approximation ($1 \ll K \simeq \beta_1\beta_2$)

$$\tau \simeq \frac{T_2}{\beta_1\beta_2} \simeq \frac{W_{n1}^2}{2\,D_p}\cdot\frac{1}{\beta_1}, \tag{3-15}$$

where W_{n1} is the shortest base width of the $p_1n_1p_2$ transistor and D_p is the hole diffusion constant in the n_1 region.

This last relation can be found directly from some simple and intuitive considerations concerning the charge introduced in the base of the $p_1n_1p_2$ transistor.

3.4. *Physical interpretation of the response time.* The thyristor can be considered as turned ON when the charge injected in the base of the $p_1n_1p_2$ transistor is high enough that the collector current $i_2 \geq i_0$. In the limit, if (Fig. 5) $p_{n1}(0)$ is the hole concentration at the p_1n_1 junction and q the electron charge, the collector current is

$$i_2 = q\frac{P_{n1}(0)}{W_{n1}}D_p = i_0, \tag{3-16}$$

assuming that the diffusion length L_p of the holes in the base is much larger than the base width. The corresponding charge Q_{n1} stored in the pnp base is

$$Q_{n1} = \tfrac{1}{2}\,qp_{n1}(0)\cdot W_{n1}$$

or

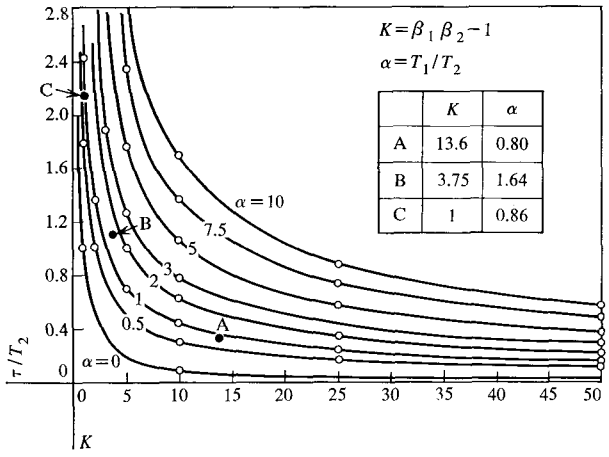
$$Q_{n1} = \frac{i_0T_2}{\beta_2}. \tag{3-17}$$

This charge Q_{n1} is provided by the collector current of the fast npn section of the thyristor. This collector current is due to the base current ($g - i_0$) applied during a period of time θ. We then have

$$Q_{n1} = \beta_1(g - i_0)\theta. \tag{3-18}$$

Comparing (3-17) and (3-18), we find from (3-4) and (2-6) the result (3-15):

$$G\theta = \frac{T_2}{\beta_1\beta_2} = \tau.$$



	K	α
A	13.6	0.80
B	3.75	1.64
C	1	0.86

Figure 4 τ/T_2 versus K curves, with $\alpha = T_1/T_2$ as parameter.

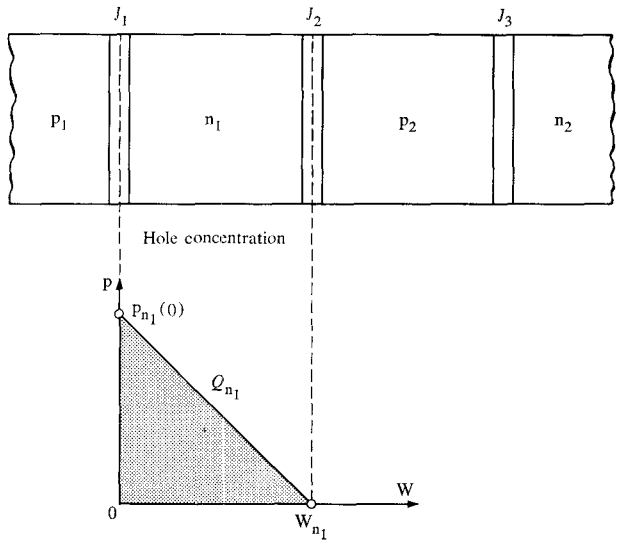


Figure 5 Minority carrier concentration in the base of the $p_1n_1p_2$ transistor.

4. Experimental verification

The validity of the foregoing calculations is demonstrated with some experimental results.

4.1. *Triggering condition.* Equation (3-11) can be verified for different types of thyristors. For comparison purposes we have plotted, in Fig. 1, the curve representing Eq. (3-11) for a value $\tau = 100$ ns, and the values of G versus θ measured for five types of thyristors from different manufacturers (A, B, C, D and E). The different curves can be deduced from each other by translation. According to (3-11), they have the same slope and the same shape, in good agreement with theory. The response time τ may be obtained in two ways:

1) The value of τ is obtained as the value of θ for which the asymptote of the curve $G(\theta)$ crosses the line $G = 1$.
2) The value of τ is the pulse duration needed to turn on the thyristor with a normalized gate current $G = 0.58$.

Table 1, deduced from Fig. 1, shows good agreement between the two values.

We can thus propose the following practical definition of the response time τ: *the response time τ is the minimum duration of a gate pulse necessary to turn* ON *the device with a gate current 1.6 times the dc triggering current.*

4.2. *Literal expression of τ.* The verification of the relation (3-13) has been made with the thyristors, A, B, C, which have four layers connected to external leads. Measuring current gain β and time constant T, the common emitter parameters in (2-2), under the same circuit conditions as used for the measurement of τ, we find that the agreement between calculated and measured values of τ is relatively good, indicating the validity of relation (3-13).

Table 1 Response time of various thyristors according to Fig. 1.

	Type of thyristor				
τ, ns	A	B	C	D	E
From asymptotic curve	46	300	620	1200	3200
From theoretical definition (G = 0.58)	66	280	620	800	3000

Table 2 Influence of device parameters on response time.

	Parameter					
Type	β_1	T_1 ns	β_2	T_2 ns	τ_{calc} ns	τ_{meas} ns
A	34	120	.43	150	48	46
B	25	410	.19	250	275	300
C	12.5	300	.16	350	750	620

This corroborates the results obtained by other authors[2-4] concerning the fact that the two-transistor analog representation of the thyristor gives a quantitative explanation of the dynamic behavior of low-power thyristors. Using this method with the particular assumption of

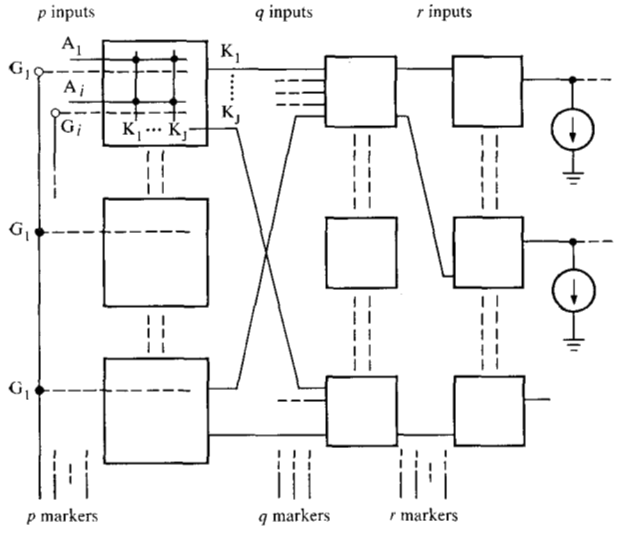
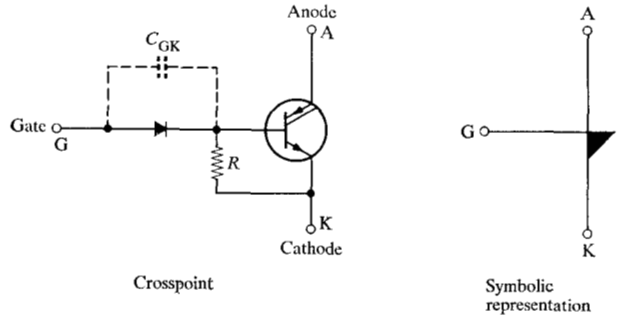


Figure 6 Switching network organization (three stages are represented).

Figure 7 Crosspoint and symbolic representation.



a well-defined threshold gate triggering current, we have obtained a very simple expression for the minimum gate triggering condition (3-11) and for the response time (3-13). In applications where false triggering is inadmissible, good control of the triggering sensitivity is the key necessity.

From the response time expression, the *device designer* is able to adjust the value of τ by modifying the parameters of the constituent transistors of the thyristor: 1) the overlatching factor $K = \beta_1\beta_2 - 1$, 2) the common-emitter time constant of the pnp transistor, 3) the common base-collector capacitance, ... and the *circuit designer* is able to avoid any unwanted triggering.

5. Applications

In the field of low-power thyristors, there is an important application of the notion of response time: the design of a space-division switching network using thyristors as crosspoints.[6] In order to fulfill the requirements of cross-talk attenuation, the thyristors are very small in size and have a correspondingly short response time (T_1 small). The results are a high triggering sensitivity of the crosspoint and also fast transients in the switching network because, according to (3-10), the rise time is related to the response time, as was pointed out by Bergman.[3]

Since the minimum value of the gate-cathode shunting resistance is defined by other conditions concerning the marking of a path in the switching network, *the only parameter which can be modified in order to decrease the triggering sensitivity of the crosspoint is its response time.* The importance of the role of the response time also becomes clear: if it is chosen too small 1) the triggering sensitivity of the crosspoint is high and 2) the rise times in the network are shorter. These two facts tend to increase the probability of unwanted parasitic triggerings.

5.1. *General description of a switching network.* Typically, a space-division switching network is composed of switching matrices connected in series (Fig. 6). Each switching matrix can establish an ac/dc connection between any one of the anode leads A_i and any one of the cathode leads K_J. It permits several simultaneous but independent connections to be established. Thus after one connection has been made, any remaining A_i terminals may be connected to any of the K_J terminals, and so on. The crosspoints are connected at each intersection of an anode lead A_i and a cathode lead K_J. In the same manner, the gates are connected together to the gate leads G_i.

A crosspoint is selected in the matrix by the choice of a cathode lead and of a gate lead. With the crosspoint[14] used in the IBM 2751 consisting of a thyristor, a resistor, and a diode (Fig. 7), the selection is done with a negative pulse on the cathode and a positive pulse on the gate thus providing a given gate current to the thyristor. Figure 8 shows how a typical path between A and B terminals is organized in a three-stage, one-wire network; the crosspoints (only one for each matrix has been represented) are connected in series between a voltage source V^+ and a current source J (feeder J). Connecting the two points A and B consists first in establishing the half ac/dc path A to feeder J_A and then B to feeder J_B and finally closing the ac path between A and B with the middle junctor J_M.

5.2. *Marking a half-path.* A half-path (A to J_A) is established by setting the chosen current source J_A (the voltage V_{K3} drops from the bias voltage V_B to the ground voltage) and by addressing the gate leads corresponding to the chosen path (marking voltage V_M lower than V_B): first the thyristor T_3 turns ON, then T_2, and when T_1 turns ON, the voltages at points A_2, A_3, K_3, rise to values close to V^+, and a current defined by J_A flows from V^+ to ground. At that time, the dc path is established, and the diode in series with the gate of each crosspoint isolates the A-J_A

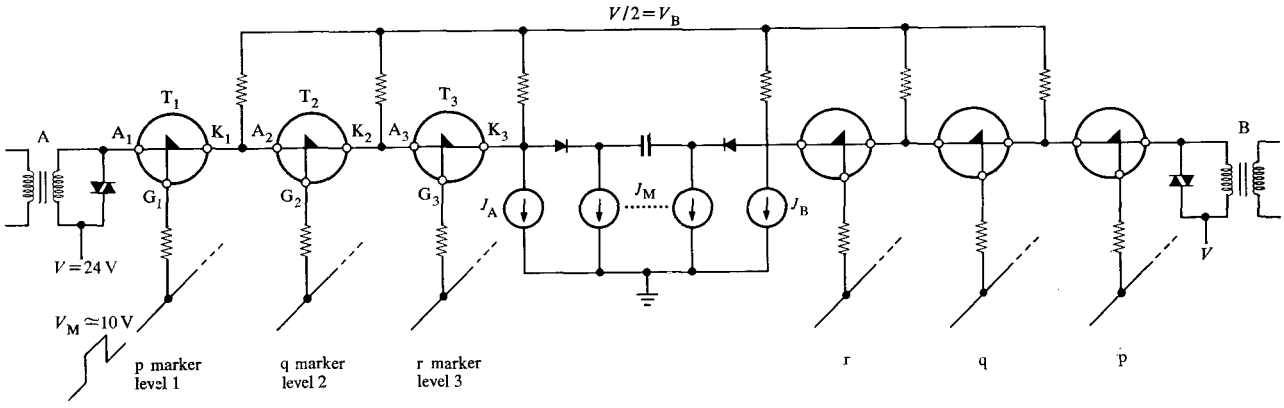


Figure 8 Complete path between subscribers A and B. The diagonal lines represent a common bus in series (OFF: $J(t) = 0$; ON: $J(t) = 15\text{mA}$).

path from the marking circuit. This path remains established as long as the current source J_A is ON; when J_A is turned OFF, the three thyristors connected in series turn OFF.

Numerous transients therefore appear in the switching network during connection or disconnection of a path. As we shall see now in more detail, if the thyristors are too sensitive, unwanted triggerings may occur, causing unacceptable "conferences" or transfers.

One type of transient is due to the connection or disconnection of the path; capacitive currents between anode and cathode or between gate and cathode are generated in some crosspoints. Another is due to the signals transmitted through the switching network, but this is often negligible (low amplitude or low frequency signals); their influence is only to increase (or decrease) the actual nominal dc voltages.

Let us consider the transients which appear during the marking of a path in a typical 3 × 3 matrix (Fig. 9) in which: 1) the path 0-0 has been established previously (crosspoint 00 is ON); 2) the path 1-1 has to be established (crosspoint 11 will be turned ON); 3) the path 2-2 remains idle.

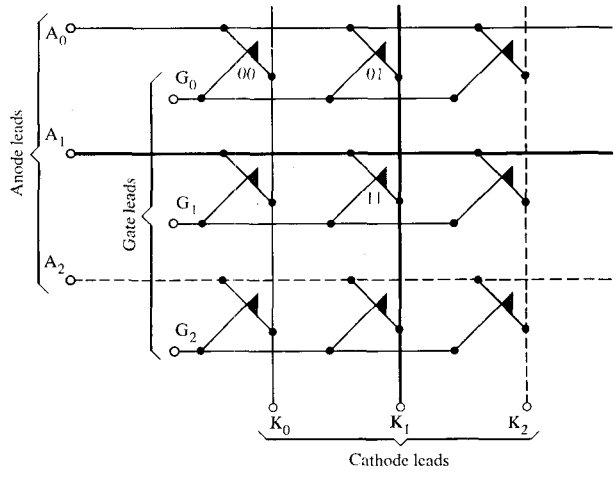
Tables 3 and 4 give the anode-to-cathode and gate-to-cathode voltages for each crosspoint of the matrix, at four different times:

t_0 = before selection of the current source J_A
t_1 = after selection of J_A
t_2 = during the triggering of the crosspoint 11
t_3 = once the half path has been established, but during the marking of the crosspoint 11.

The positions in bold face indicate a change from the preceding state.

5.2.1. *Transients applied between anode and cathode.* False triggering due to the so-called "rate effect" has to be avoided. The rate effect is the triggering of a thyristor when a fast-risetime positive voltage pulse is applied between anode and cathode, causing capacitive currents to flow. In Table 3 some crosspoints can be rate-effect triggered. The most critical is the crosspoint 01 (anode 0, cathode 1) at time t_1, because in its case false triggering means connection of J_1 to the established path 0-0 (transfer or conference).

Figure 9 3 × 3 matrix during triggering of crosspoint 11; crosspoint 00 is ON; the other crosspoints must remain OFF.



The classical expression of the rate effect is meaningless when the rate of rise is too high (0.2 V/ns or more). The rate-effect triggering is due to the capacitive current across the common base-collector junction, acting as a gate current. When extremely small rise times θ are considered, the capacitive pulse is very short. In that case, the triggering condition (1-2) becomes $\int_0^\theta g\,dt \geq i_0\tau$ and the thyristor will turn ON if the charge $\int_0^\theta g\,dt = Q_1$ supplied by the capacitive pulse is larger than $i_0\tau$ (= 60pC

Table 3 Anode-to-cathode voltages.

	t_0			t_1			t_2			t_3		
	K_0	K_1	K_2	K_0	K_1	K_2	K_0	K_1	K_2	K_0	K_1	K_2
A_0	ON	$\frac{+V}{2}$	$\frac{+V}{2}$	ON	V	$\frac{V}{2}$	ON	V	$\frac{V}{2}$	ON	+1	$\frac{V}{2}$
A_1	$\frac{-V}{2}$	0	0	$\frac{-V}{2}$	$\frac{V}{2}$	0	−V	ON	$\frac{-V}{2}$	+1	ON	$\frac{V}{2}$
A_2	$\frac{-V}{2}$	0	0	$\frac{-V}{2}$	$\frac{V}{2}$	0	$\frac{-V}{2}$	$\frac{V}{-2}$	0	$\frac{-V}{2}$	$\frac{-V}{2}$	0

Table 4 Gate-to-cathode voltages.

	t_0			t_1			t_2			t_3		
	K_0	K_1	K_2	K_0	K_1	K_2	K_0	K_1	K_2	K_0	K_1	K_2
G_0	$-V$	$\frac{-V}{2}$	$\frac{-V}{2}$	$-V$	0*	$\frac{-V}{2}$	$-V$	0*	$\frac{-V}{2}$	$-V$	−V	$\frac{-V}{2}$
G_1	$-V$	$\frac{-V}{2}$	$\frac{-V}{2}$	$-V$	0*	$\frac{-V}{2}$	$\frac{-V}{2}$*	+1.4	0*	$\frac{-V}{2}$	$\frac{-V}{2}$	0
G_2	$-V$	$\frac{-V}{2}$	$\frac{-V}{2}$	$-V$	0*	$\frac{-V}{2}$	$-V$	0*	$\frac{-V}{2}$	$-V$	−V	$\frac{-V}{2}$

* Approximate value.

with $\tau = 100\text{ns}$, $R = 1\text{k}\Omega$). In the limit

$$i_0\tau = Q_1 = \frac{C_{20}V'}{1-n}\left[\left(\frac{V'+V_0}{V_0}\right)^{1-n} - 1\right],$$

where

C_{20} is the junction capacitance at 0V bias,
$V_0 \simeq 0.6\text{V}$ for silicon,
V' = reverse voltage of the junction n_1p_2 and
$n = 1/3$ for a diffused junction.

As a function of the triggering sensitivity of the crosspoint, this equation defines the value of the pulse voltage V_{RE} below which it is impossible to trigger the thyristor, even with an infinite rate of rise. In fact, for a large enough response time, it is possible to design the thyristor with V_{RE} larger than the maximum voltage which appears in the switching network ($V_{RE} > V^+$).

For rise times $\Delta t > 10\tau$ the triggering condition (3-11) gives the classical relation $C_2\,\Delta V/\Delta t = i_0$.

5.2.2. *Transients applied between gate and cathode.* When a positive transient ΔV_{GK} appears between gate and cathode, a small capacitive current flows towards the gate if the cathode lead impedance is low. For example, in Table 4 this is the case for the crosspoints 01, 11, 21 at time t_1. Due to the fact that the gate diode remains reverse biased, the charge Q_2 supplied to the gate of the thyristor is $Q_2 = C_{GK}\,\Delta V_{GK}$. If this charge is larger than $i_0\tau$, the crosspoints 01, 11, 12, can be turned ON. The risks of false triggering have been suppressed by

1) biasing the network at $V_B = V^+/2$,
2) controlling the rise time of the gate marking pulses,
3) designing a very small gate diode ($C_{GK} \simeq 1\text{pF}$), and
4) controlling the triggering sensitivity of the crosspoints (i_0 and response time τ) in production.

Conclusion

We have given a theoretical interpretation of the triggering sensitivity of thyristors. An expression for the response-time as a function of the parameters of both constituent transistors of a thyristor has been obtained, showing how the thyristor functions as a charge-controlled device. We have found good agreement between the theory and ex-

perimental results for the case of low power, high speed thyristors. A practical definition of the response time has been proposed. A space-division switching network using more than 10,000 high speed thyristors as crosspoints has been built. A tight specification of the triggering sensitivity of the crosspoint permits taking advantage of the high speed and low triggering power of the device to obtain simple and reliable control of the switching network by a computer.

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