IBM Field Engineering Handbook

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System/360, Model 65

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IBM® Field Engineering Handbook

System/360, Model 65

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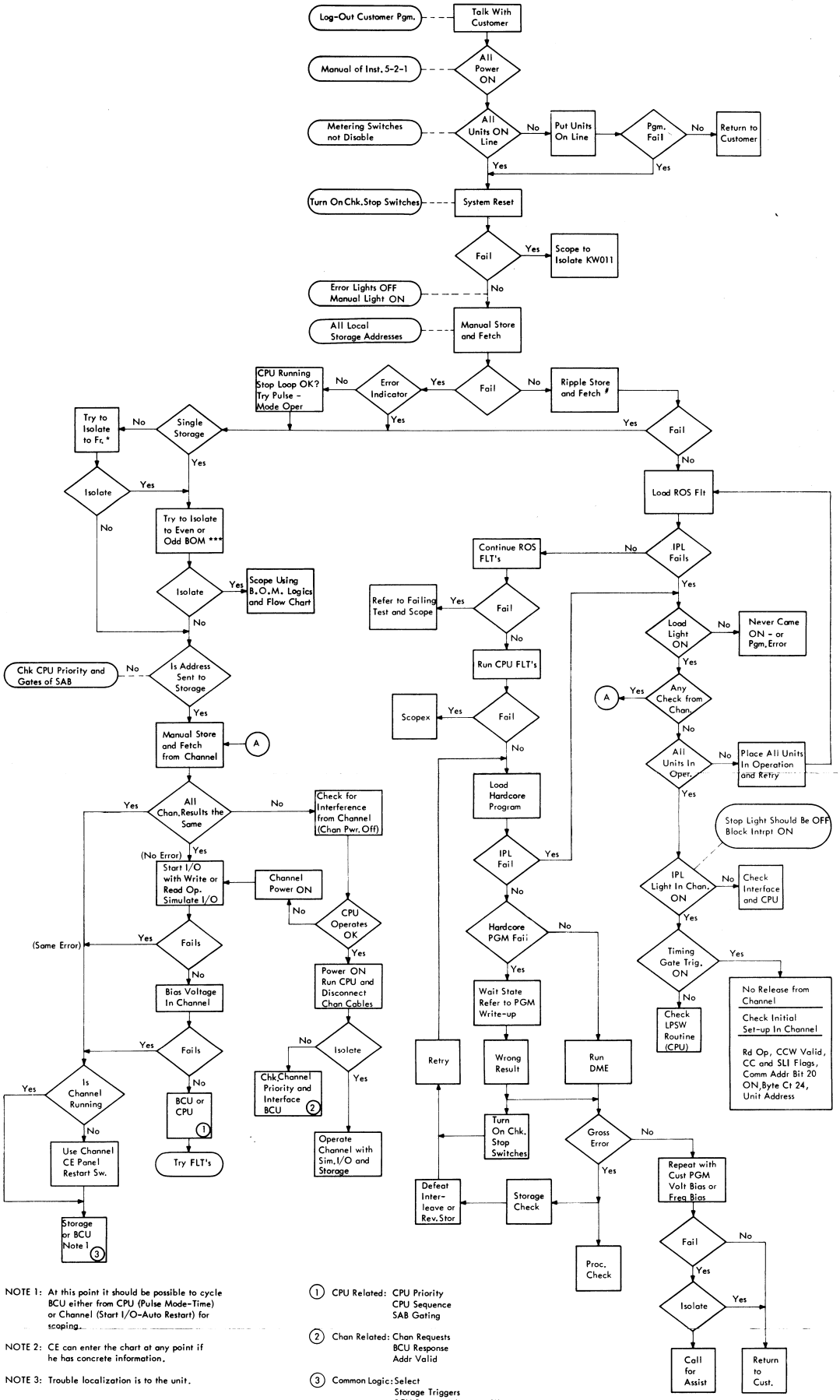
CONTENTS



NOTE 1: At this point it should be possible to cycle BCU either from CPU (Pulse Mode-Time) or Channel (Start I/O-Auto Restart) for scoping.

NOTE 2: CE can enter the chart at any point if he has concrete information.

NOTE 3: Trouble localization is to the unit.

(1) CPU Related: CPU Priority
CPU Sequence
SAB Gating

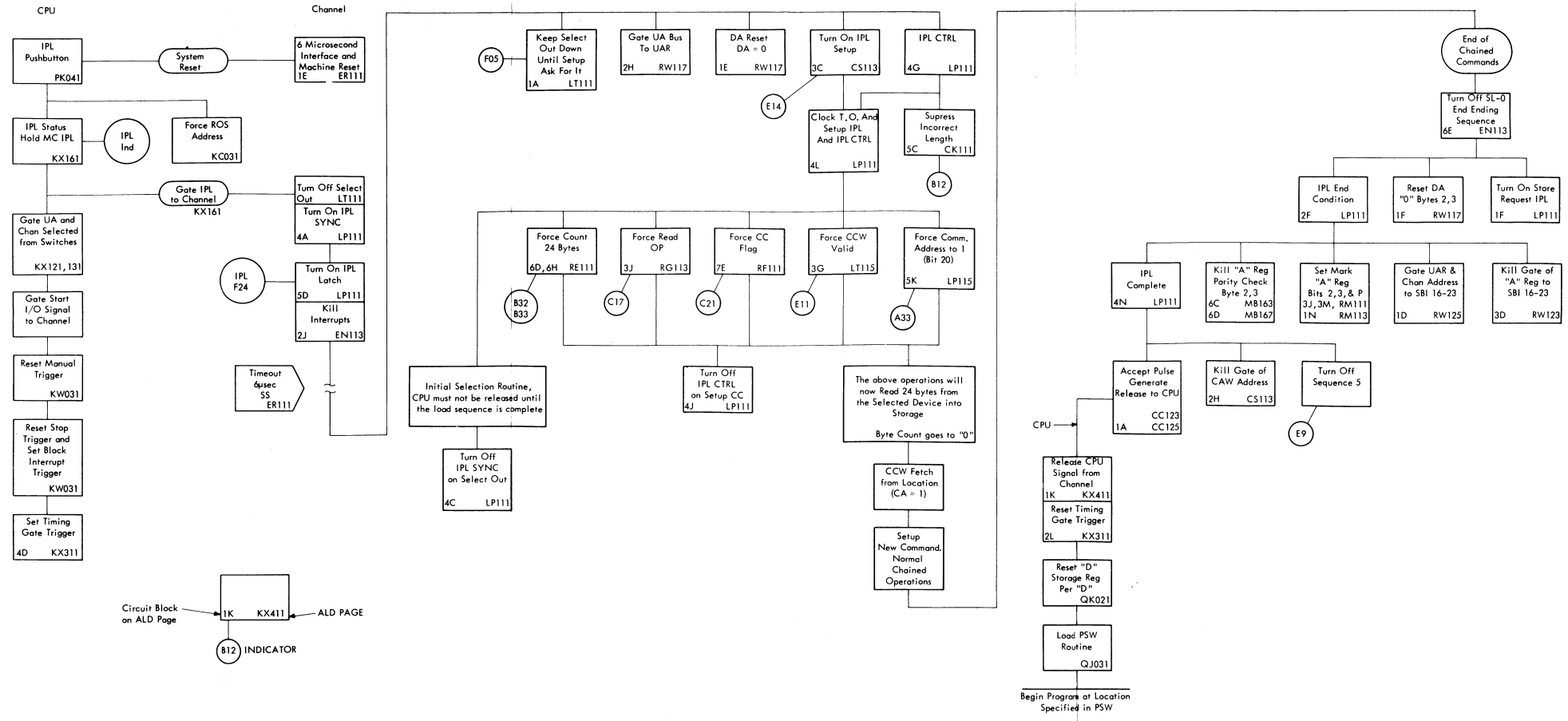
(2) Chan Related: Chan Requests
BCU Response
Addr Valid

(3) Common Logic: Select
Storage Triggers
BCU Busy and Advance Waiting

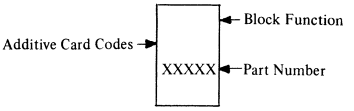
On Main or Local Store

Use Addressing:
Fr No 1 SAB 4 $\bar{5}$
Fr No 2 SAB $\bar{4}$ 5
Fr No 3 SAB 4 $\bar{5}$
Fr No 4 SAB 4 5

** SAB 20 = Odd
20 = Even
} High or Low Word


CPU
Channel
IPL Pushbutton PK041
System Reset
6 Microsecond Interface and Machine Reset 1E ER111
IPL Status Hold MC IPL KX161
IPL Ind
Force ROS Address KC031
Gate IPL to Channel KX161
Turn Off Select Out LT111
Turn On IPL SYNC 4A LP111
Gate UA and Chan Selected from Switches KX121, 131
IPL F24
Turn On IPL Latch 5D LP111
Kill Interrupts 2J EN113
Gate Start I/O Signal to Channel
Timeout 6usec SS ER111
Reset Manual Trigger KW031
Reset Stop Trigger and Set Block Interrupt Trigger KW031
Set Timing Gate Trigger 4D KX311
Circuit Block on ALD Page
1K KX411
ALD PAGE
B12 INDICATOR
F05
Keep Select Out Down Until Setup Ask For It 1A LT111
Gate UA Bus To UAR 2H RW117
DA Reset DA = 0 1E RW117
Turn On IPL Setup 3C CS113
IPL CTRL 4G LP111
E14
Clock T.O. And Setup IPL And IPL CTRL 4L LP111
Supress Incorrect Length 5C CK111
B12
Force Count 24 Bytes 6D, 6H RE111
Force Read OP 3J RG113
Force CC Flag 7E RF111
Force CCW Valid 3G LT115
Force Comm. Address to 1 (Bit 20) 5K LP115
B32 B33
C17
C21
E11
A33
Initial Selection Routine, CPU must not be released until the load sequence is complete
Turn Off IPL SYNC on Select Out 4C LP111
Turn Off IPL CTRL on Setup CC 4J LP111
The above operations will now Read 24 bytes from the Selected Device into Storage
Byte Count goes to "0"
CCW Fetch from Location (CA = 1)
Setup New Command. Normal Chained Operations
End of Chained Commands
Turn Off SL-0 End Ending Sequence 6E EN113
IPL End Condition 2F LP111
Reset DA "0" Bytes 2, 3 1F RW117
Turn On Store Request IPL 1F LP111
IPL Complete 4N LP111
Kill "A" Reg Parity Check Byte 2, 3 6C MB163 6D MB167
Set Mark "A" Reg Bits 2, 3, & P 3J, 3M, RM111 1N RM113
Gate UAR & Chan Address to SBI 16-23 1D RW125
Kill Gate of "A" Reg to SBI 16-23 3D RW123
Accept Pulse Generate Release to CPU CC123 1A CC125
Kill Gate of CAW Address 2H CS113
Turn Off Sequence 5
E9
CPU
Release CPU Signal from Channel 1K KX411
Reset Timing Gate Trigger 2L KX311
Reset "D" Storage Reg Per "D" QK021
Load PSW Routine QJ031
Begin Program at Location Specified in PSW

2065 CPU	Hardware Version	CAS Version
Basic Machine	000	000
Special Move Inst (7074) RPQ	001	001
LCS Attach and/or IH, J	004	---
Power Fail Logout - RPQ	010	010
Bank of America - RPQ	018	004
High Resolution Timer - RPQ	022	---
Edit, normalize and scale - RPQ	024	024
Shared Storage - RPQ	025	025
Non IBM Meter - RPQ	040	---
Remote OP Console (ROCP) - RPQ	047	---
Seven Bit Storage Protect - RPQ	048	---
Invalid Sign Decimal OP Supp.	---	050
Inverse Move - RPQ	051	051
7070/74 Emulator	074	074
7080 Emulator	080	080
7090 Emulator	090	090
Sense Indicator OPS - RPQ	091	091
1410 - 7010 Simul Assist	093	093
Special Inst (7080) - RPQ	---	180
High Resolution Timer (7090) - RPQ	A22	---
Shared Storage (7090) - RPQ	A25	A25
7080 Emulator Tape Parity - RPQ	A44	---
Power Fail Logout (7090) - RPQ	A91	A91
High Resolution Timer IH, J - RPQ	B22	---
Shared Storage IH, J - RPQ	B25	B25
2065/2930 Sync Pulse - RPQ	B36	---
Invalid Alpha (7074) - RPQ	B74	B74
High Resolution Timer (7080) RPQ	C22	---
Shared Storage (7074) - RPQ	C25	C25
High Resolution Timer (7074) - RPQ	D22	---
Shared Storage (7080) - RPQ	D25	D25
Shared Storage LCS - RPQ	E25	E25
Multiprocessor 2065	026	026
Multiprocessor 2065 (7074)	A76	---
Multiprocessor 2065 (7080)	A86	---
Multiprocessor 2065 (7090)	A96	---
Multiprocessor 2065 5–8 Storage	K69	---



ADDITIVE CARD CODES

1052 Adapter	ADA 2
7070/74 Emulator	CBS 5
7080 Emulator	CBS 6
7090 Emulator	CBS 7
2361 Attachment	LCSA
2870	CH 0
Selector Ch. 3	CH 3
Selector Ch. 4	CH 4
Selector Ch. 5	CH 5
Selector Ch. 6	CH 6
Additional Storage 3-4	M 34
Shared Processor Storage	SST
Indicators (Model J)	IND 4
Segmented Clock	SEGM
High Resolution Timer	HRT
Direct Control	DCT
Extended Direct Control	DCTE
Read Only Storage Extension	ROSE
Rounding	RND
List Processing	LP
Multi-system	MS
50 Cycle Oscillator	TIM
Dynamic Stg Relocation	DSR

Interpretation of Box Data

Left Edge Char	Print Positions 1	2	3	4	5	6	7	8	9	10	11	12	Right Edge Char	Meaning of Left Edge Character
A	PTV	PTV	PTV	PT	PU	PU	PU	PUQ	PUQ	PQ	PQ	Q		A Parallel Adder Inputs
A	P	→	AP	AP	AP	AP	,	E	,	C	C	C		A Parallel Adder Output Destination(s)
B	N	N	N	N	N	M	M	M	M	M	M	M		B Serial Adder Inputs
B		→	C	C	,	D	D			R	R	R		B Serial Adder Output Destination(s)
D	C	C	C	C	C	C	C	C	C	C	C	C		
D	E	E	E	E	E	E		G	G	G	G	G		D Misc. Ingating Controls
D	F	F	F	F	F	F	F	F	F	F				
D	A	A	A	A	A									
L	H	H	H	H	H	H	H	H	B	B	B	B		L Local Store Control
S	L	L	L	L	L	L	L	L	L	L	L	L		S Mark Setting and Storage Requests
C	F	F	F	F	F	F	F	F	F	F	F	F		
C	G	G	G	G	G	G	G	G	G	G	G	G		C Misc. Controls
C	E	E	E	E	E	E								
C	D	D	D	D	D	D	D	D	D	D				
R	JK	JK	JK	JK	JK	J	J	J	J	J	J	J		R Branching

Figure 1

```
100111————————0227
A Q1+0                 |
A→D                    |
B 1+0                  |
B→F                    |
D Q23→R                |
L RG*E2→S,T            |
S MS-REQ*D-3           |
C RESET                |
C 1→IC(21-22)          |
R E(02-07)→ROA         |
R EXCEP                |
                       |
Q6——000000——QF
```

Figure 2

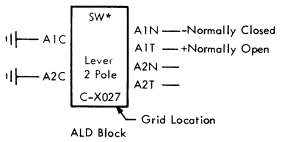
Use of Figure 1

Figure 1 is to be used to determine the actual mnemonics from the box data (Figure 2 is an example referred to in the following).

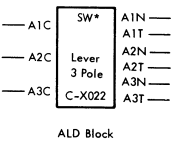
The two lines of edge character A completely define the action of the parallel adder during this cycle, and the two lines of edge character B define the serial adder. In each case, the first line defines the adder inputs. The second lines list the registers to which the adder latch output is to be gated during the next ingating time. In addition, the first character on the second A line may indicate a left or right shift at the adder latch input. Also, on the right side of the second B line, the choice of AB or F registers as serial adder input may be indicated.

The letters shown in the print position columns of Figure 1 indicate the ROS word field from which the given mnemonic comes. The number of print positions containing the same letter in a given line indicates the maximum size mnemonic which can be used in that position.

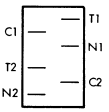
Toggle Switch Contact Numbering



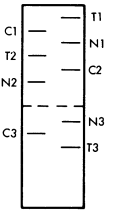
ALD Block



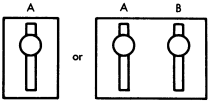
ALD Block



Contacts
As viewed from back panel

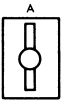


Contacts
As viewed from back panel



Switch
Front Panel View

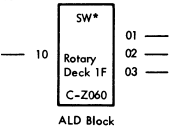
2-Position Double Pole Switch



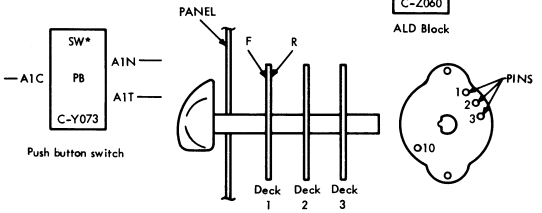
Switch
Front Panel

3-Position Triple Pole Switch

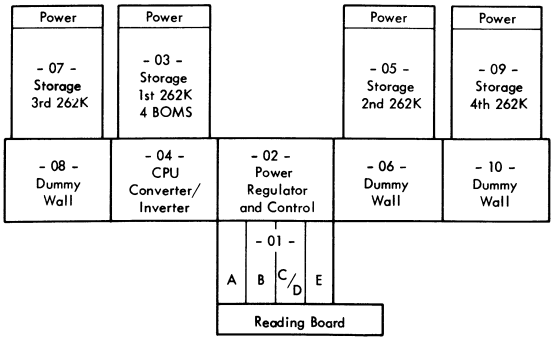
Rotary Deck Switch



ALD Block



Push button switch



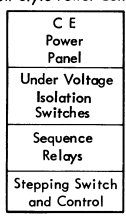
Model J65
Power Layout

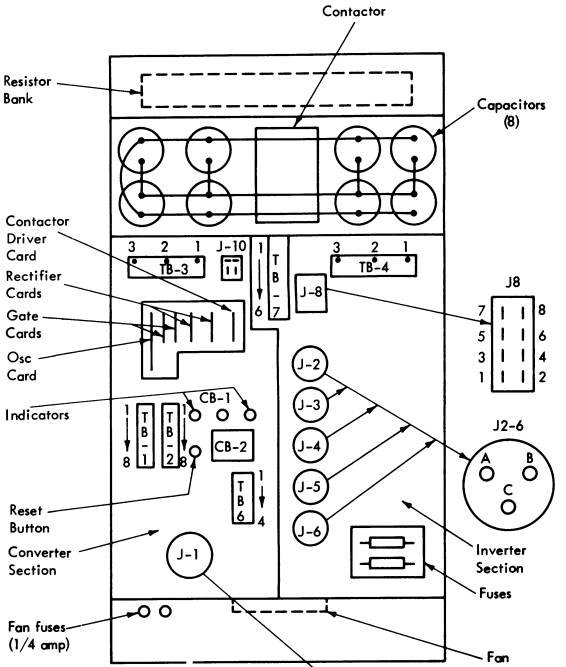
Old Style
Power Control

1 +6 C & D Upper	2 +3 B Lower	CE Power Panel	9 +48 1052	10 -3 A & B & E Upper & Lower
3 +3 E Lower	4 -3 C & D Upper & Lower	Under Voltage Isolation Switches / Stepping Relay and Switch	11 -18 C & D Upper	12 +3 A Lower
5 +3 E B - D1 & E1 Upper & 1052	6 +3 C & D Upper & Lower		13 +3 B Upper	14 +3 A Upper
7 +6M E Upper & Lower	8 +6M C & D Lower	Sequence Relays	15 +6M B Upper & Lower	16 +6M A Upper & Lower

- 02 -
DC Regulators

New Style Power Control





DANGER

Use extreme caution when working on the converter-inverter. High voltages are present throughout the converter-inverter tub assembly, including the heat sinks that are floating and the SMS cards.

2065 ALD VOLUMES

2065 ALD PAGES

See Data Flow on Page 32 for Logic Page Reference of Registers.

2065 ALD CONTENTS (Cont)

MANUAL CONTROLS

Add. Keys	PK 031
Add. SW - ROSAR	RX 301-302
Data Keys	PK 001-021
Indicators (Rollers)	PL 011-061
Indicator Scan Bus	KT 001-571
IPL	KX 161-411
Manual Control PB's	KW 011
Manual Control SW's	PK 041
Meter Logic	KC-051

INTERRUPTS

Channel Interrupts	KM 306-351
External (& time clk)	KM 221-251
Interrupt Controls	KM 121-191
Interrupt Priority (& Code to PSW)	KN 121-411
Specific & Except Condition	KM 421-861
Interrupt Resets	KM 281

STATUS TRIGGERS

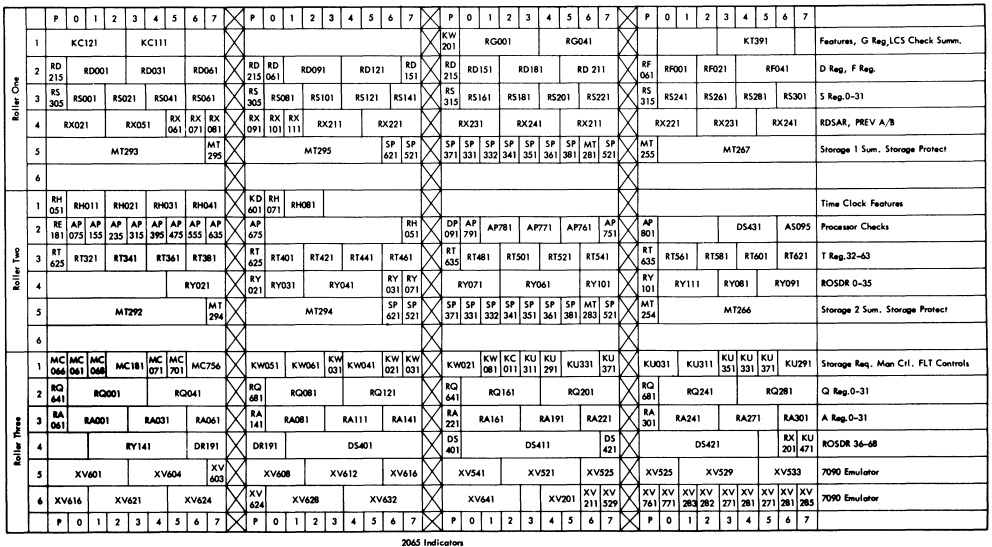
Status A - G	KS 021-141
Status H	AS 105

MISCELLANEOUS CONTROLS

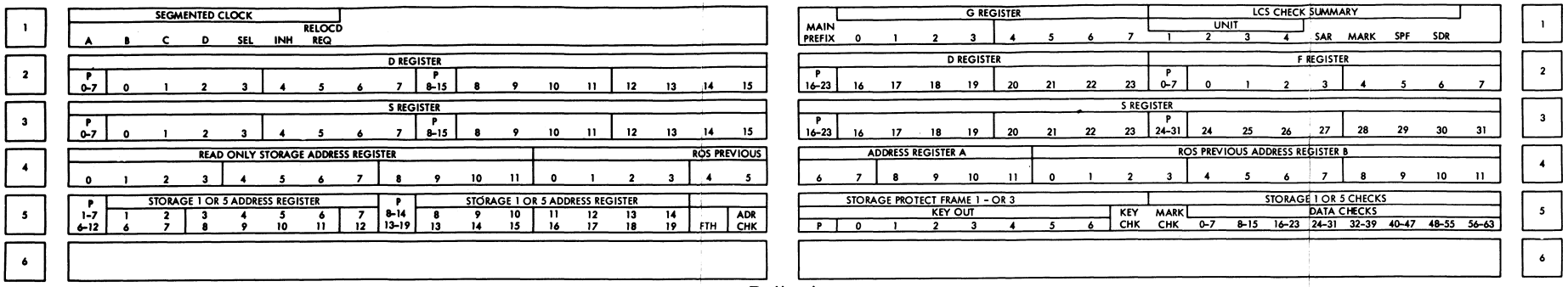
ABC	CW 011-051
Chan & UA	KC 011-151
Clock	KC 011-021
Clock Distrib	AS 201-MC391/RB 81
Clock for IC, Q-R, etc.	RQ 831
Clock Distrib for ROS & Parity	RY-011
Cond Code	RW 341-351
Direct Control	JA 121
Div Mult Select	RT 823
Edit	KZ 011-501
MPY RT BUS (S-SADD)	DP 011-012
Mult Decode & Sel	DP 031-071
PSW 0-33	RW 011-321
PSW 36-39	RW 361-381
S Reg Mpr Par Check	DP 091
ST Bytes 0-31	DP 021-022
ST-SIBB/STC	RT 751-757
STC	CS 011-061
OP Decoder	DN 001-101

STORAGE CONTROLS

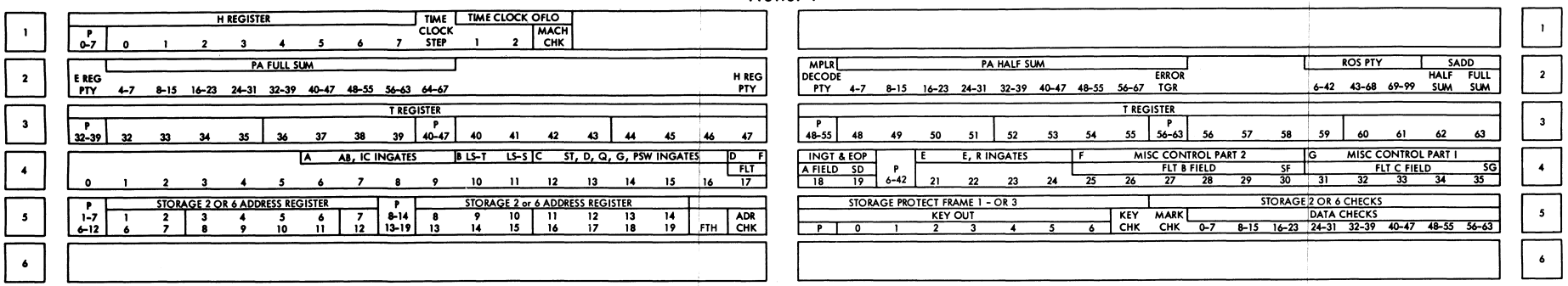
BCU Busy & CH 5 & 6 Prior	MC 321-331
CPU Req & Prior	MC 161-166
CPU Sequencers	MC 121-141
D 21-22 Decode	DR 061
D Requests	MC 061
D- -SAB	MA 291-293
Even/Odd & Inv Add. Dec	MC 461-467
Frame 1-4 Busy	MC 411-412
Gates to SAB	MC 062-065



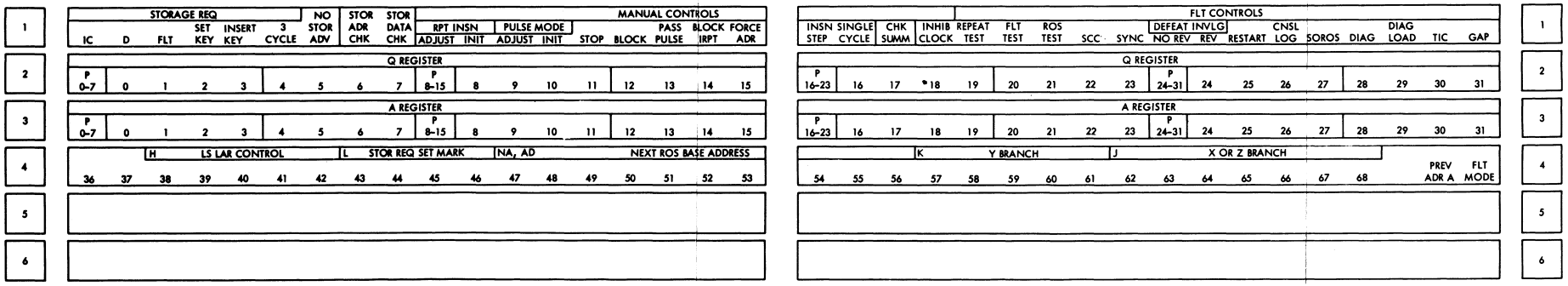
Note: Roller 1, Pos 5; Roller 2, Pos 5
SP – (Ind on MZ270)



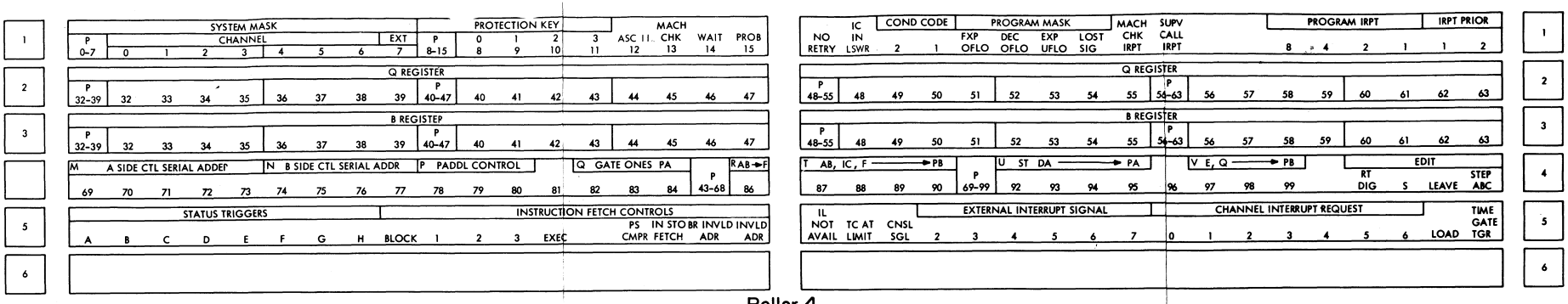
Roller 1

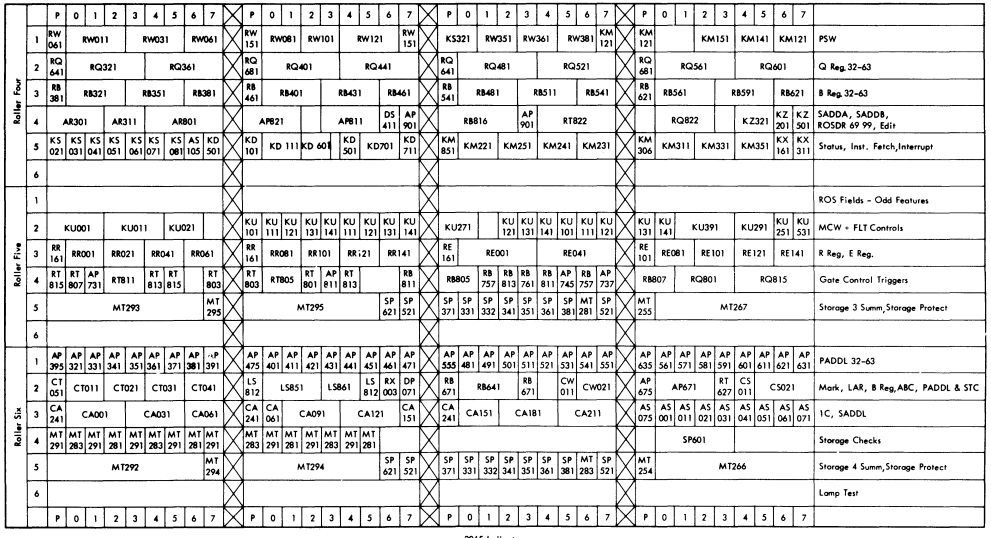


Roller 2

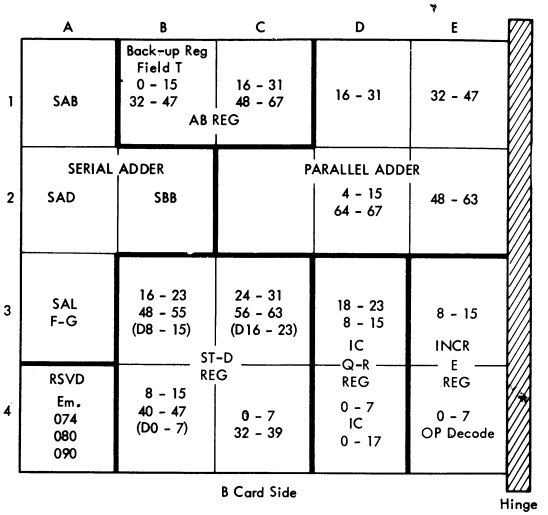


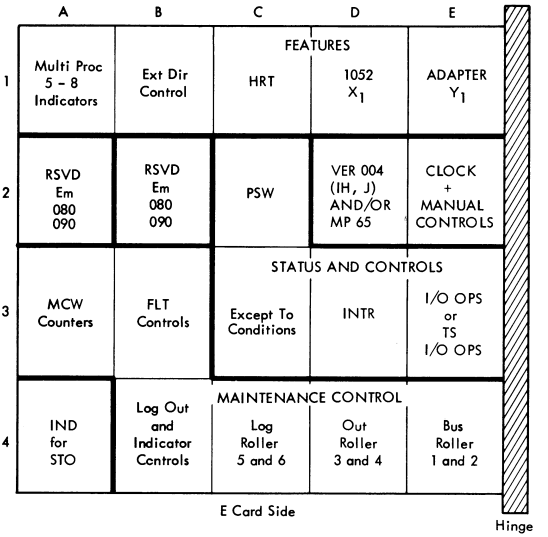
Roller 3

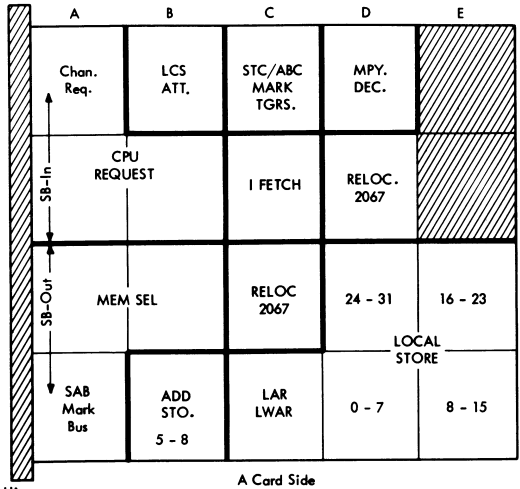

SYSTEM MASK
CHANNEL
EXT
PROTECTION KEY
MACH
ASC II CHK
WAIT
PROB
Q REGISTER
B REGISTER
M A SIDE CTL SERIAL ADDER
N B SIDE CTL SERIAL ADDR
P PADDL CONTROL
Q GATE ONES PA
RAB→F
STATUS TRIGGERS
INSTRUCTION FETCH CONTROLS
BLOCK
EXEC
PS CMPR
IN STO FETCH
BR INVLD ADR
INVLD ADR
IC
NO RETRY
IN LSWR
COND CODE
PROGRAM MASK
FXP OFLO
DEC OFLO
EXP UFLO
LOST SIG
MACH CHK IRPT
SUPV CALL IRPT
PROGRAM IRPT
IRPT PRIOR
T AB, IC, F → PB
U ST DA → PA
V E, Q → PB
EDIT
RT DIG
S
LEAVE
STEP ABC
IL NOT AVAIL
TC AT LIMIT
CNSL SGL
EXTERNAL INTERRUPT SIGNAL
CHANNEL INTERRUPT REQUEST
TIME GATE TGR
Roller 4
ROS FIELDS ODD
T U V
RSFSP
RMRKP RSARP RSARP LOGCT CHAN
CHANNEL SELECT
RDATP RBYCP SSDCK SEL
CPU TEST ADDRESS
LFTHF UNCT CONDT ERSLT
ADR SEQUENCE
FLT COUNTER
R REGISTER
S00-31 T32-63 T32-63 T32-47 T48-63 D00-23 D00-23 D00-23 ONES IC
32-63 32-63 31-62 43-63 08-31 07-30 40-63 61-63 PA PB 40-63
T C TLI CLI T C TLI CLI T C
STORAGE 3 OR 7 ADDRESS REGISTER
FTH
ADR CHK
FLT CHK
ROS TEST SEQ
CHECK COUNTER
BFR
PASS FAIL INTRM UDC CCC MMSC
E REGISTER
OPERATION CODE
A00-31 A04-07 A08-31 B32-63 B64-67 A06-31 B32-67 B64-67 EXCS-6 F08-07 HOT 1 E08-11 E12-15 F08-11 Q04-15 Q20-31 Q36-47 Q52-63
32-63 04-07 08-31 32-63 64-67 04-29 30-65 28-31 28-63 60-63 60 56-59 60-63 52-63 52-63
L2 L2
STORAGE PROTECT FRAME 2 - OR 4
KEY OUT
KEY CHK
MARK CHK
STORAGE 3 OR 7 CHECKS
DATA CHECKS
Roller 5
PADDL
CPU MARK
ST PAR 32-39
LS ADDRESS REG
LS WRITE
INHIB STORE WRITE
TX TGR
INSTRUCTION COUNTER
STORAGE CHECKS
FRAME 1
ADR 1 DATA 1
ADR 2 DATA 2
FRAME 2
ADR 3 DATA 3
ADR 4 DATA 4
FRAME 3
ADR 5 DATA 5
ADR 6 DATA 6
FRAME 4
ADR 7 DATA 7
ADR 8 DATA 8
STORAGE 4 OR 8 ADDRESS REGISTER
B REGISTER
ABC
PADDL
STC
LS SIGN
SADDL
STORAGE PROTECT CHECK
FRAME
STORAGE 4 OR 8 CHECKS
Roller 6

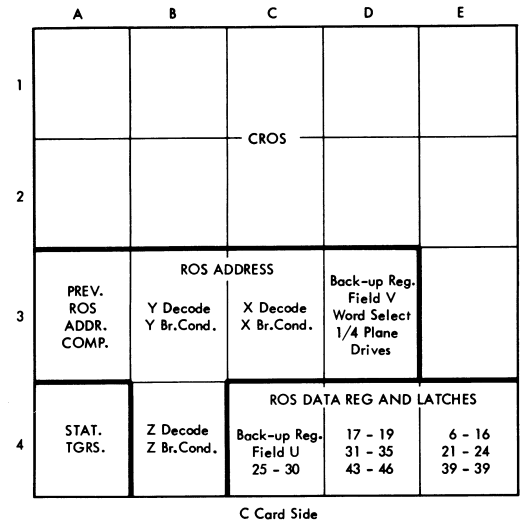


Note: Roller 5, Pos 5; Roller 6, Pos 5
SP - (Ind on MZ270)


A
B
C
D
E
1
SAB
Back-up Reg
Field T
0 - 15
32 - 47
16 - 31
48 - 67
AB REG
16 - 31
32 - 47
SERIAL ADDER
PARALLEL ADDER
2
SAD
SBB
4 - 15
64 - 67
48 - 63
3
SAL
F-G
16 - 23
48 - 55
(D8 - 15)
24 - 31
56 - 63
(D16 - 23)
ST-D
REG
18 - 23
8 - 15
IC
Q-R
REG
8 - 15
INCR
E
REG
4
RSVD
Em.
074
080
090
8 - 15
40 - 47
(D0 - 7)
0 - 7
32 - 39
0 - 7
IC
0 - 17
0 - 7
OP Decode
B Card Side
Hinge


A
B
C
D
E
FEATURES
1
Multi Proc
5 - 8
Indicators
Ext Dir
Control
HRT
1052
X_1
ADAPTER
Y_1
2
RSVD
Em
080
090
RSVD
Em
080
090
PSW
VER 004
(IH, J)
AND/OR
MP 65
CLOCK
+
MANUAL
CONTROLS
STATUS AND CONTROLS
3
MCW
Counters
FLT
Controls
Except To
Conditions
INTR
I/O OPS
or
TS
I/O OPS
MAINTENANCE CONTROL
4
IND
for
STO
Log Out
and
Indicator
Controls
Log
Roller
5 and 6
Out
Roller
3 and 4
Bus
Roller
1 and 2
E Card Side
Hinge


A
B
C
D
E
Chan. Req.
LCS ATT.
STC/ABC MARK TGRS.
MPY. DEC.
SB-In
CPU REQUEST
I FETCH
RELOC. 2067
SB-Out
MEM SEL
RELOC 2067
24 - 31
16 - 23
LOCAL STORE
SAB Mark Bus
ADD STO. 5 - 8
LAR LWAR
0 - 7
8 - 15
Hinge
A Card Side


A
B
C
D
E
1
CROS
2
ROS ADDRESS
3
PREV. ROS ADDR. COMP.
Y Decode Y Br.Cond.
X Decode X Br.Cond.
Back-up Reg. Field V Word Select 1/4 Plane Drives
ROS DATA REG AND LATCHES
4
STAT. TGRS.
Z Decode Z Br.Cond.
Back-up Reg. Field U 25 - 30
17 - 19 31 - 35 43 - 46
6 - 16 21 - 24 39 - 39
C Card Side

Gate B

Bits	Parallel Adder Input	Parallel Adder 1/2 Sum	Parallel Adder Latch	A	S	Q	D	E	R	F	G	Bits
0										A3L5		0
1				B1D3		D4E6		E4B3	D4G3		A3H6	1
2					C4C2		B4B5			A3K5		2
3				&					D4F3			3
4				B1E3		B4C4						4
5	D2K4		D2G4		C4C6				D4E4		A3G6	5
6		D2J4				D4C5		E4C3		A3H5		6
7				B1F3	C4D4		B4D3		D4D3			7
P0				&		D4H6		E4B4	D4H3	A3G5		P0
8									D3F2			8
9	D2E3		D2D4	B1E4	B4L4		B3E7	E3B7				9
10		D2C3				D3C3						10
11									D3G2			11
12				B1H3	B4K6		B3E4	E3B6				12
13	D2H3		D2D2	&					D3H2			13
14		D2F2				D3C4		E3C7				14
15				B1G4	B4K4		B3D4		D3K2			15
P1						D4H6	B3E4	E3D7	D3H7			P1
16							C3F2					16
17	D1H5		D1D6	C1C6	B3K6							17
18		D1F6				D4E7						18
19				&			C3H6					19
20				C1D6	B3J2							20
21	D1E5		D1D4				C3H5					21
22		D1C5				D4C6						22
23				C1E6			C3F2					23
P2				&	B3G2	D4H6	C3H5					P2
24					C3E4							24
25	D1K4		D1G4	C1F6		D3D3						25
26		D1J4			C3E6							26
27												27
28				C1G6								28
29	D1L5		D1M3	&	C3E4							29
30		D1M5				D3D4						30
31				C1H6	C3E2							31
P3						D4H6						P3

Gate B

Bits	Parallel Adder Input	1/2 Sum	Latch	B	T	Q	Bits
32							32
33		E1B5			C4D2		33
34	E1C5		E1B3			D4D5	34
35				B1L3			35
36					C4D6		36
37	E1D4		E1G4				37
38		E1E4				D4C7	38
39					C4E3		39
P4						D3E3	P 4
40				B1K3			40
41	E1J5		E1K4		B4K2		41
42		E1L5				D3C5	42
43							43
44					B4J6		44
45	E1F5		E1K6				45
46		E1H6		C1J3		D3C6	46
47					B4J4		47
P5						D3E3	P 5
48							48
49	E2F3		E2K2		B3J6		49
50		E2H2				D4D6	50
51				C1B6			51
52	E2J3				B3H2		52
53		E2L3				D4D7	53
54			E2K4				54
55					B3F2		55
P6						D3E3	P 6
56				C1J6	C3D4		56
57	E2D4		E2G4			D3D5	57
58		E2E4			C3D6		58
59							59
60					C3D4		60
61	E2C3		E2B5			D3D6	61
62		E2B3		C1K6			62
63					C3D2		63
P7						D3E3	P 7

Local Store Registers — Gate A

Bits	0-3	4	5-9	10-14	15-19	20-24	
0	K4	F3	H2	G2	G2	G2	
1	J4	F3	D2	H2	E2	H2	
2	L3	F3	D2	E2	D2	E2	
3	C3	F3	H5	J5	J5	J5	
4	F3	F3	F5	H5	G5	H5	Board D4
5	E4	F3	F5	G5	F5	G5	
6	D4	F3	D5	E5	E5	E5	
7	C4	F3	B5	D5	C5	D5	
P0	B4	F3	B5	C5	B5	C5	
8	M4	G6	L2	M2	M2	M2	
9	L4	G6	J2	L2	K2	L2	
10	J4	G6	G2	H2	H2	H2	
11	K4	G6	J2	K2	J2	K2	Board E4
12	D5	G6	H5	J5	J5	J5	
13	H4	G6	E2	G2	F2	G2	
14	G5	G6	E2	F2	E2	F2	
15	E4	G6	E5	H5	F5	H5	
P1	D4	G6	E5	F5	E5	F5	
16	M5	H4	J3	K3	K3	K3	
17	L5	H4	F3	J3	G3	J3	
18	K5	H4	F3	G3	F3	G3	
19	J5	H4	L6	M6	M6	M6	
20	L4	H4	J6	L6	K6	L6	Board E3
21	E4	H4	J6	K6	J6	K6	
22	F5	H4	G6	H6	H6	H6	
23	E5	H4	E6	G6	F6	G6	
P2	D5	H4	E6	F6	F6	F6	
24	J3	F2	H2	G2	G2	G2	
25	J4	F2	D2	H2	E2	H2	
26	H4	F2	D2	E2	D2	E2	
27	K3	F2	H5	J5	J5	J5	
28	F3	F2	F5	H5	G5	H5	Board D3
29	E4	F2	F5	G5	F5	G5	
30	D4	F2	D5	E5	E5	E5	
31	C4	F2	B5	D5	C5	D5	
P3	B4	F2	B5	C5	B5	C5	

A. Zero - Detect
SAL (0-7) ≠ 0
Edit Operations
PAL (7-63) or (32-63) = 0

B. Overflow
SAL (0-7) = 0
Decimal - Overflow
PAL (31) = 1
Fixed Pt. Overflow
Left Shift - Overflow
B(32) = 1

C. VFL Signs
SA (4-7) sign neg.
B (0) = 0 for sub. or compare 1 = add
Non - VFL, FP and S (0) = 1
SA (4-7) = positive during sub or compare
S (0) = 1 for add on FP
S (0) = 0 for sub or comp on FP

D. F. P. Mult/Div
SAL (0) = 1
Q-to-LAR = 0

E. Invalid Sign VFL
Edit Invalid Character

F. VFL Destination Operands Sign
VFL SB (4-7) sign negative
A (0) = 1 on FP

G. Miscellaneous Execution

H. Carry - Control
Serial Adder Carry

2065 CONDITIONS AT THE END OF I FETCH

RR FORMAT

Instruction in E Reg. (all instruction bits).
R1 Operand in A, B, & D Reg.
R2 Operand in S, T.

For Branch Instr. } STC = 4

R1 Operand in S, T Reg.
R2 Operand in A, B, & D Reg.

RX FORMAT

Instruction in E Reg. (first 16 bits of instruction).
R1 Operand in S, T.
Operand Address in D (C(B2) + C(X2) + D2).
Storage Req. for Operand given on last I Fetch Cycle.

RS, SI FORMAT

Instruction in E Reg. (first 16 bits of instruction).
R1 Operand (if applicable) in S, T.
Operand Address in D (C(B) + D).
Storage Req. for Operand given on last I Fetch Cycle.

SS FORMAT

Instruction in E Reg.
Destination Operand in S, T.
Destination Address in D Reg.

Logical Operand Address	=	C(B1) + D1
Divide Operand Address	=	C(B1) + D1
Dec. & Not Div. Operand Address	=	C(B1) + D1 + L1

Storage Req. for Source Operand given on last I Fetch Cycle.
Source Address in IC = (IC in local store working reg.)
Logical + Mult + Div Address = C(B2) + D2
Dec. ($\overline{\text{Mult + Div}}$) Address = C(B2) +D2 + L2
Program Store Compare (ASC) Has Been Made.

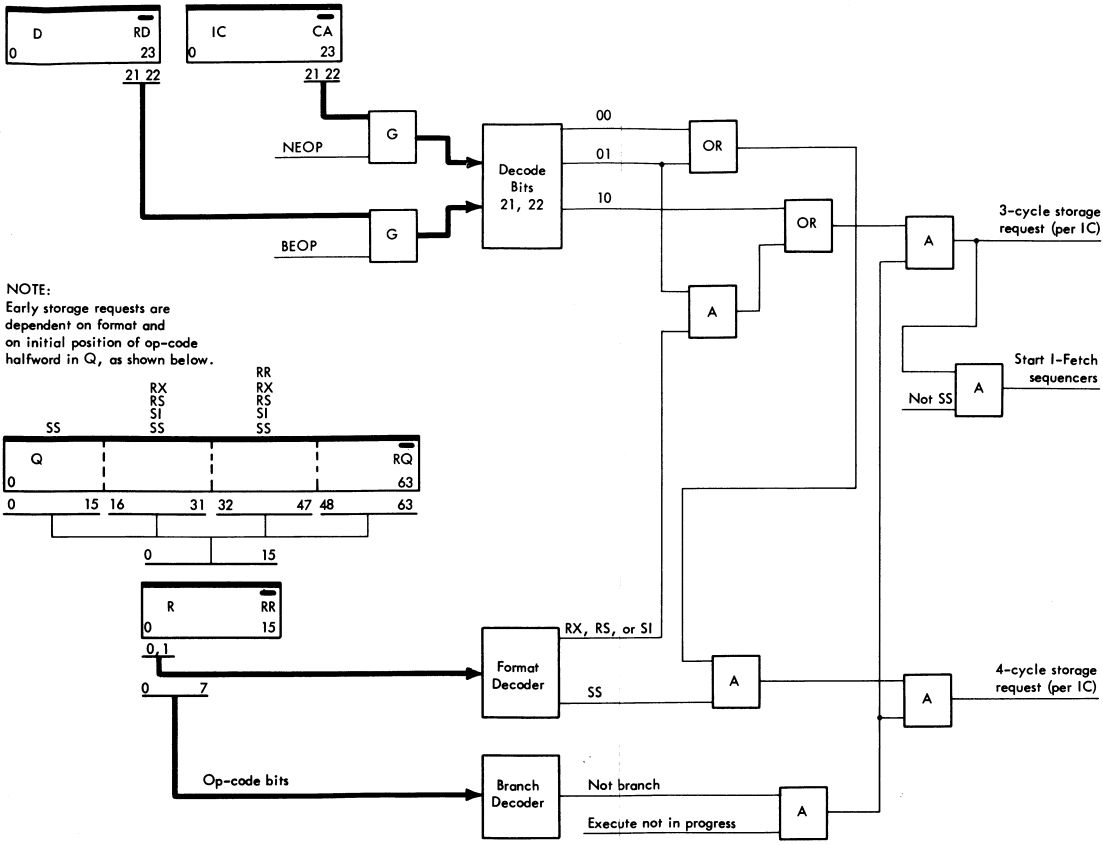
Condition	Forced Adr. D Reg.	Forced Adr. ROSAR	CLD Page	Block
1. Timer	80	014	QT041	A1
2. CPU Store in Progress	N/A	02E	QU001	Q7
3. Machine Check Int.	48	00C	QU001	A1
4. Program Int.	40	00A	QU001	N1
5. Supervisor Call Int.	32	008	QU001	J1
6. External Int.	24	006	QU001	G1
7. I/O Int.	56	00E	QU001	Q1
8. Stop Key, Storage Adr Compare Stop, Insn Step	N/A	026	QY041	C2
9. Manual Control Wait	N/A	02A	QY051	Q7
10. Repeat Insn - Multiple and Single	N/A	028	QY051	G1
11. Program Store Compare	N/A	004	QT041	N8
12. Invalid Instruction Adr.	N/A	002	QT041	Q4
13. Q Buffer Filling	N/A	7 entries	QT041	

Q BUFFER FILLING ENTRIES

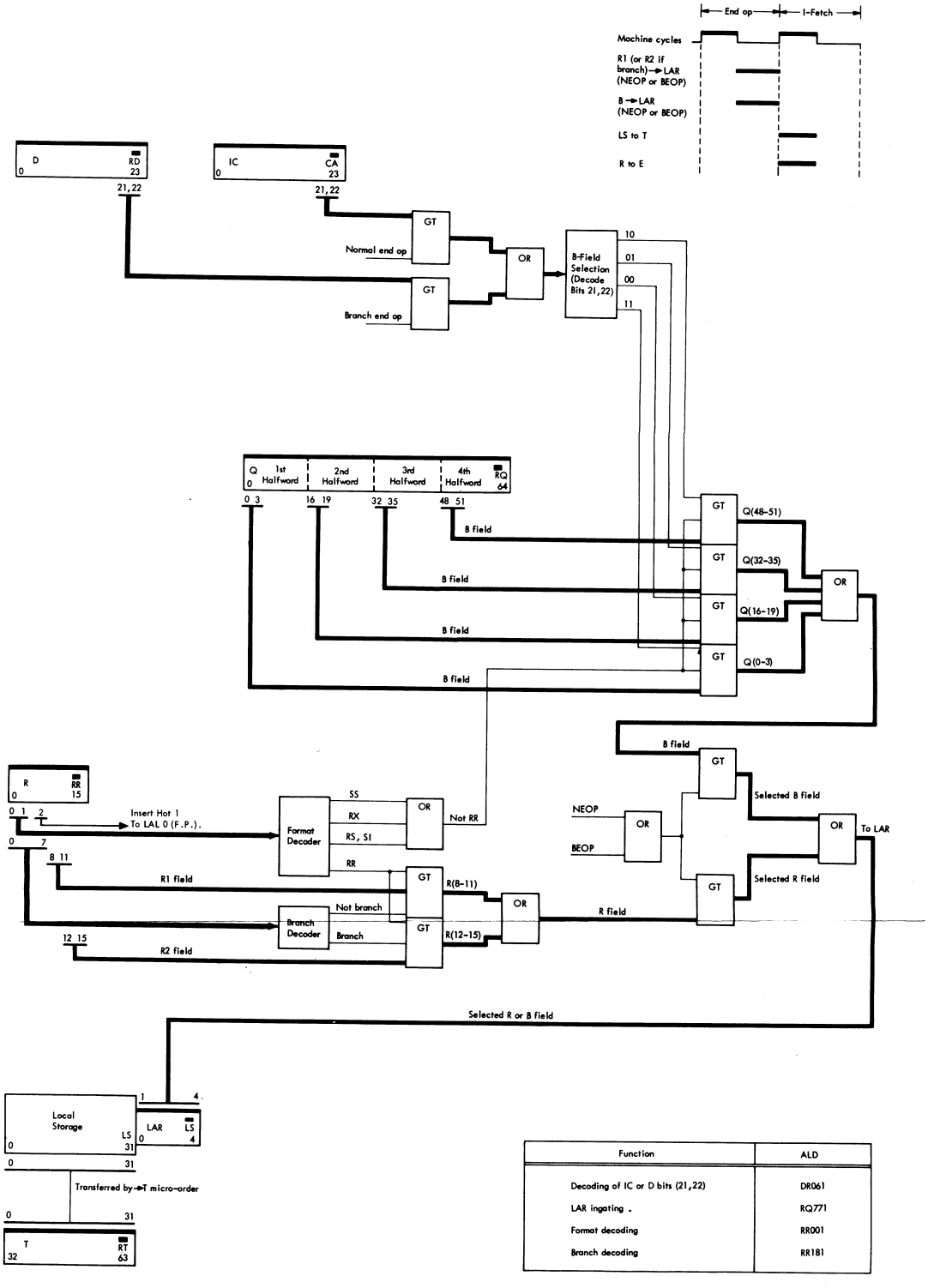
Format	End Op.	Cond.	Forced Adr. ROSAR	CLD Page	Block
a. RR	Normal	N/A	030	QT041	J6
RR	1 Cyc. Early	N/A	030	QT041	J6
b. RX	Normal	No Index	032	QT041	C2
RX	1 Cyc. Early	No Index	032	QT041	C2
c. RX	2 Cyc. Early	No Index	022	QT041	J4
d. RX	Normal	Index	03A	QT041	G2
RX	1 Cyc. Early	Index	03A	QT041	G2
e. RS, SI	Normal	No Shift	034	QT041	L2
RS, SI	1 Cyc. Early	No Shift	034	QT041	L2
f. RS, SI	2 Cyc. Early	No Shift	024	QT041	N3
g. RS, SI	All	Shift	020	QJ001	C1

Function	Forced Address	CLD Page	Block
All Zeros Test	000		N8
All Ones Test	801	QY051	N9
External Interrupt	006	QU001	G1
Force Padder Full Sum (Scan)	6B7	QJ031	N2
Invalid Ins'n Address	002	QT041	Q4
IPL	007	QK021	L1
I/O Interrupt	00E	QU001	Q1
Machine Check Interrupt	00C	QU001	A1
Manual Control Stop	026	QY041	C2
Power On Reset	00B	QY041	N1
Program Interrupt	00A	QU001	N1
Program Store Compare	004	QT041	N8
Pulse Mode Reset	005	QY051	E1
Q Refill RX Format	030	QT041	J6
Q Refill RX Format	032	QT041	C2
Q Refill RX Format	022	QT041	J4
Q Refill RX Format	03A	QT041	G2
Q Refill RS-SI Format	034	QT041	L2
Q Refill RS-SI Format	024	QT041	N3
Refill Shift Instruction	020	QJ001	C1
Repeat Instruction	028	QY051	G1
ROSAR Test	9BB	QY021	G7
SAP Interrupt Delay	02E	QU001	Q7
SCAN - Logout	019	QY001	A2
SCAN - SCNT	6B0	QY011	Q2
SCAN - MCW4	009	QY031	A1
SCAN - MASK	011	QY031	E1
Specification	010	QT041	E9
Storage Ripple	800	QY051	L1
SVC Interrupt	008	QU001	J1
System Reset	003	QY041	Q3
Time Clock Step	014	QT041	A1
Wait Exception	02A	QY051	Q7
Wait	784	QY051	Q8
IPL-Wait For Release	70E	QK021	L3
I/O Instruction Wait For Release	4B4	QK021	C6
I/O Interrupt Wait For Release	946	QU001	Q3
Diagnose - Keys to MCW Address +8	5B0	QY001	QD
BCU Scoping Loop	9CF	QY021	J7
Ripples IC and PADDL	5C7	QY051	A9
Ripples IC and PADDL 40-63	500	QS101	A8
Ripples Serial Adder and F Reg	83A	QY041	C9
Ripples D Reg	4C4	QY051	Q2
Ripples E Reg 8-15	839	QY041	N2
Ones to PADDL 32-63	7B2	QY041	N9
Ones to PADDL, D Reg	891	QY041	L5
Ones to D and T Regs	88F	QY041	A1
Ones to E Reg 8-15	00B	QY041	N1
Zeros to A, B Regs and AB CTR	545	QS001	E4
Set CPU Marks	9BF	QY051	J5
Logout (All Indicators Should Light)	02D	QY001	J7
Read LS per E 12-15	200	QT001	C3
Read LS per E 11-15	7CE	QY051	N6

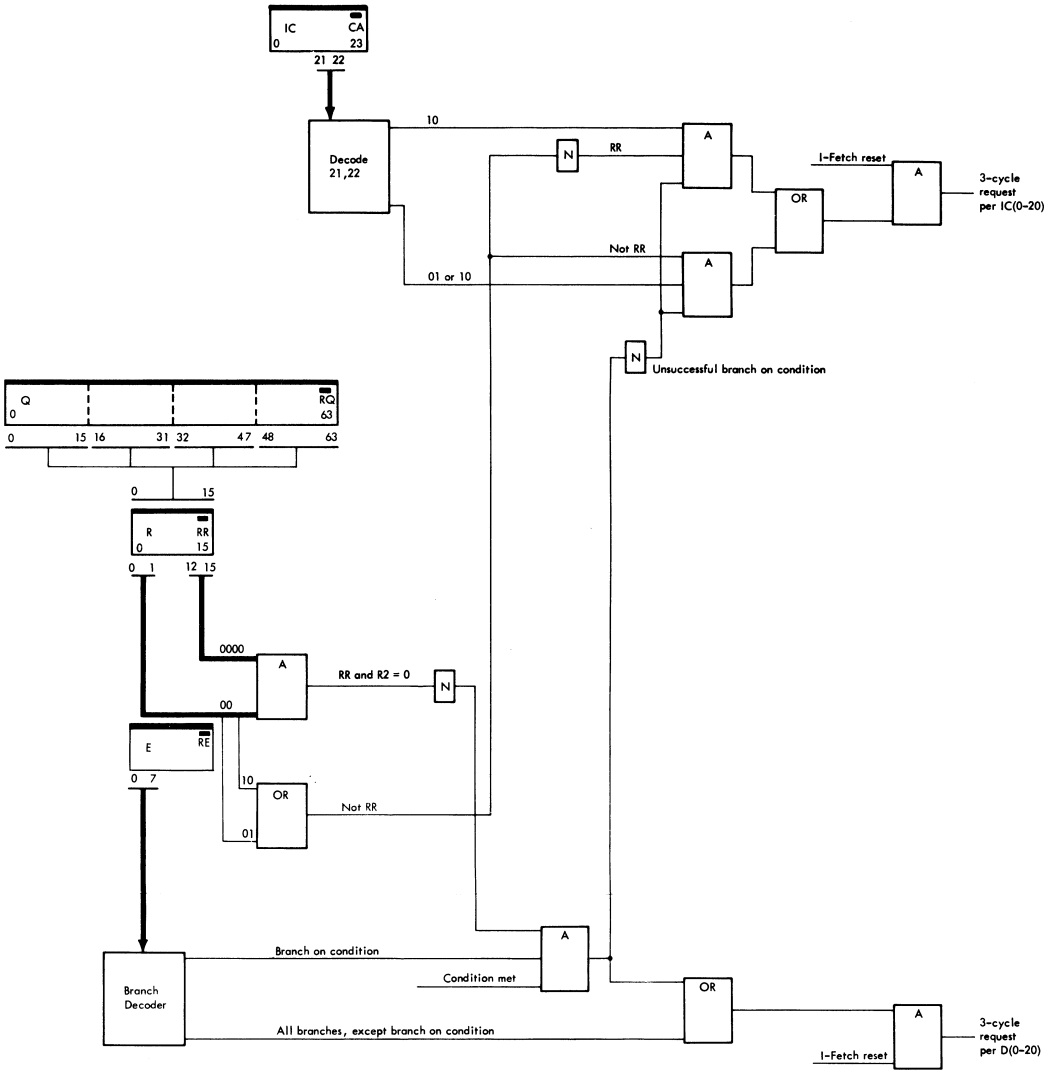
Function	Forced Address	CLD Page	Block
Write LS per E 11-15 Blank Cycle. No gates should be up and all errors on roller 2 position 2 should be able to be reset by the CHK RESET pushbutton.	7CF 5B2	QY051 QY041	L6 L9



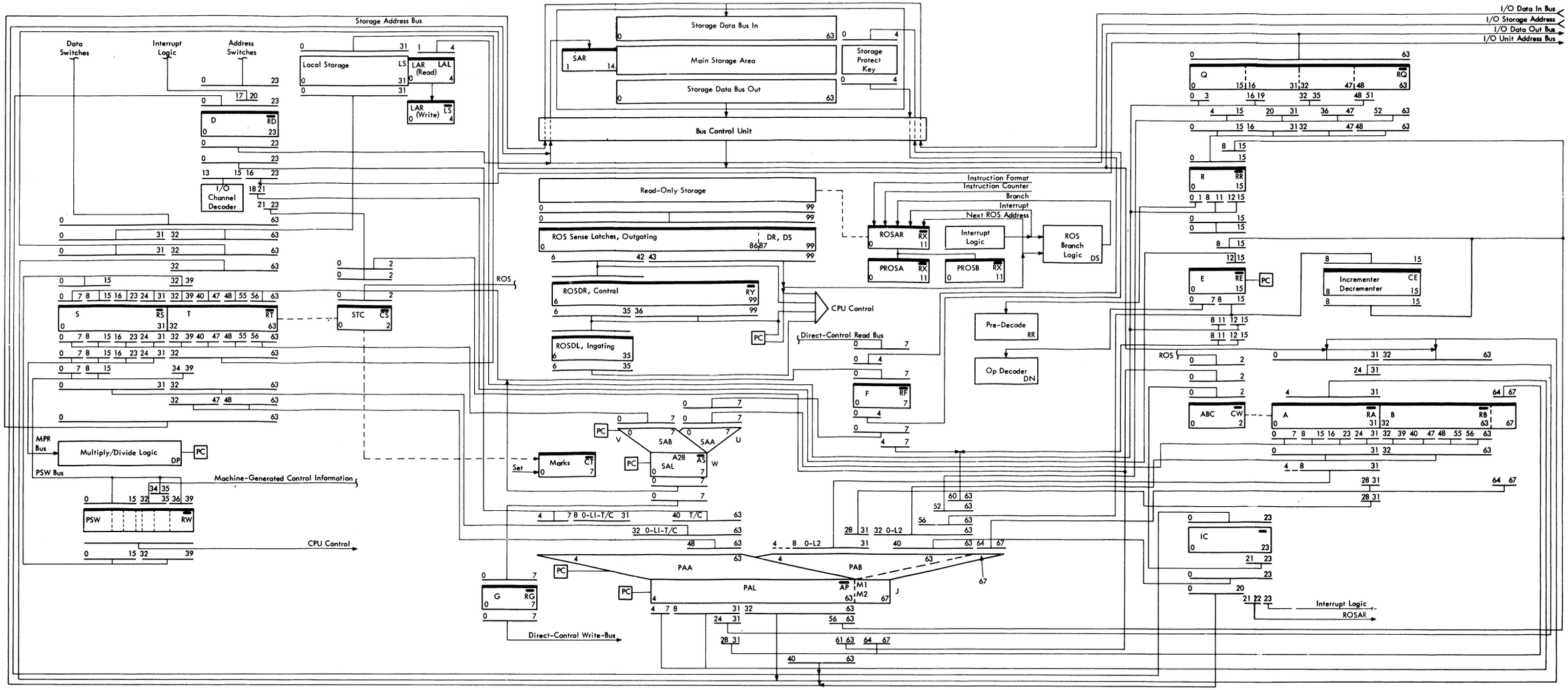
Function	ALD
Decoding of IC or D bits (21, 22)	DR061
Storage request logic	KD101, KD201
Format decoding	RR001
Branch decoding	RR181

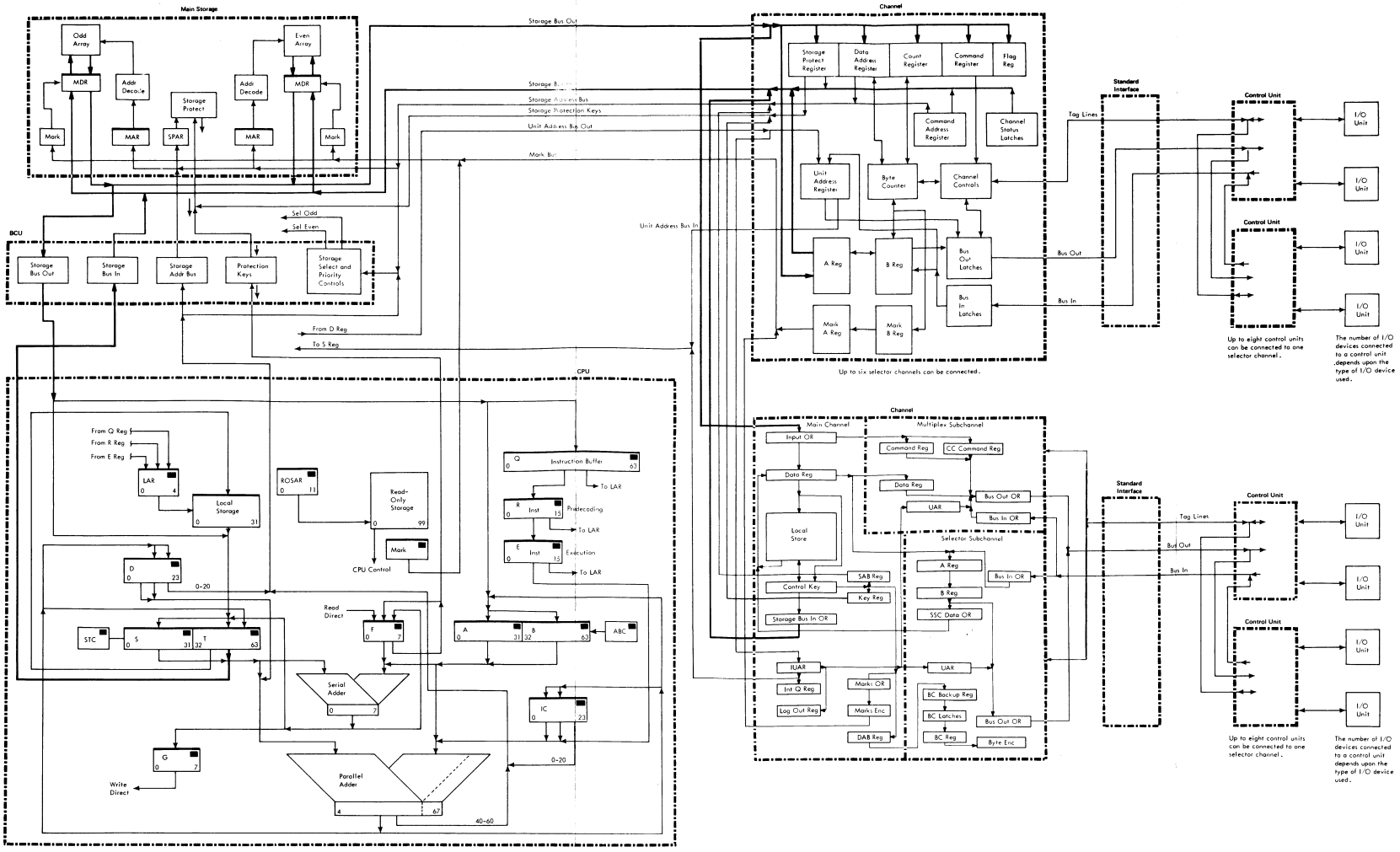


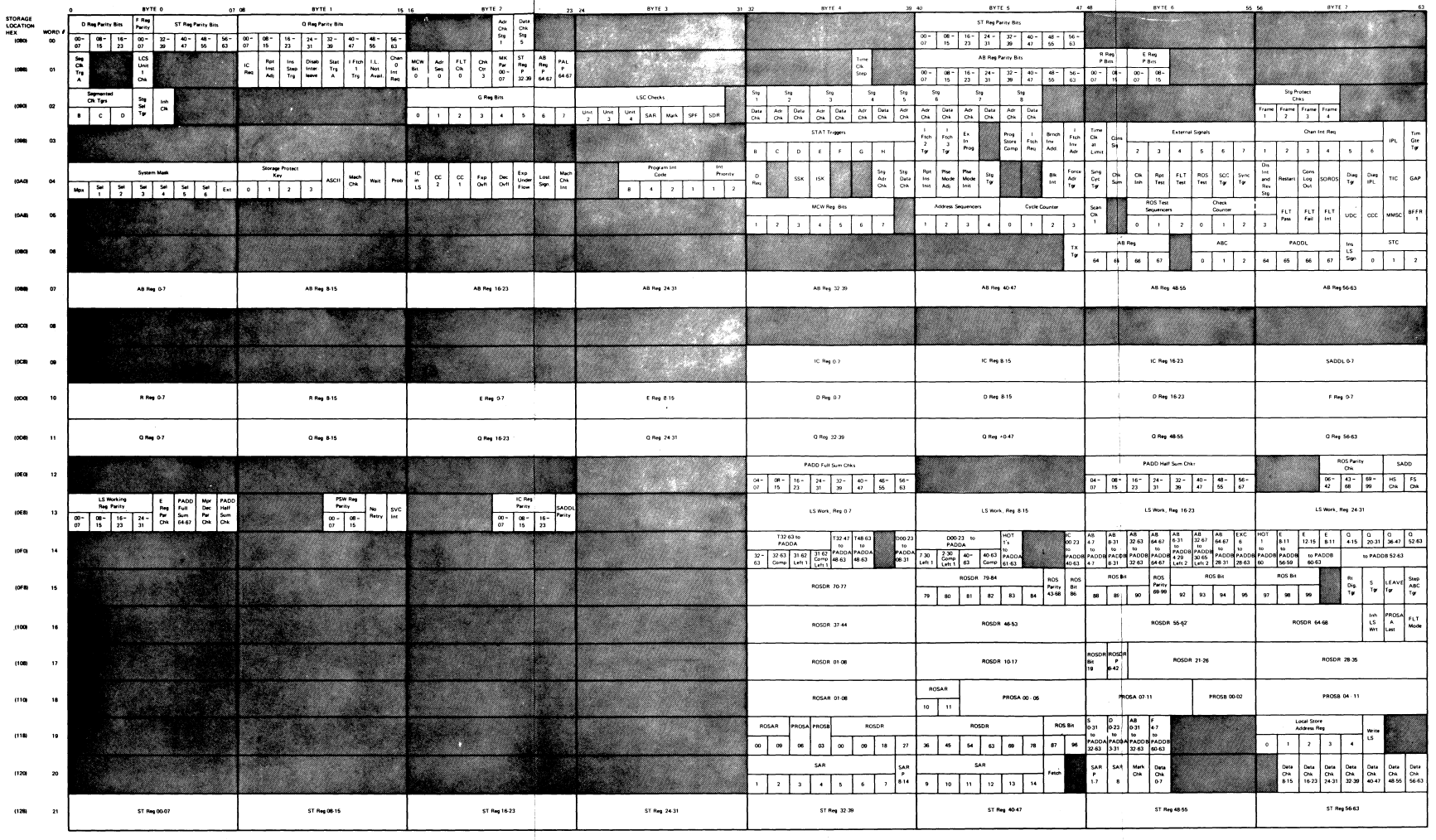
Function	ALD
Decoding of IC or D bits (21,22)	DR061
LAR ingating .	RQ771
Format decoding	RR001
Branch decoding	RR181



Function	ALD
Branch request logic	KD101, KD201
Format decoding	RR181
Branch decoding	RR001
Decoding of IC(21, 22)	DR061


Storage Address Bus
Data Switches
Interrupt Logic
Address Switches
Local Storage
LAR (Read)
LAR (Write)
I/O Channel Decoder
Storage Data Bus In
Main Storage Area
Storage Data Bus Out
SAR
Storage Protect Key
Bus Control Unit
I/O Data In Bus
I/O Storage Address
I/O Data Out Bus
I/O Unit Address Bus
Read-Only Storage
ROS Sense Latches, Outgating
ROSDR, Control
ROSDL, Ingating
ROSAR
PROSA
PROSB
Interrupt Logic
ROS Branch Logic
Instruction Format
Instruction Counter
Branch
Interrupt
Next ROS Address
CPU Control
Direct-Control Read Bus
Pre-Decode
Op Decoder
Multiply/Divide Logic
MPR Bus
PSW Bus
Machine-Generated Control Information
CPU Control
Marks
Set
SAB
SAA
SAL
PAA
PAB
PAL
Direct-Control Write-Bus
Incrementer Decrementer
Interrupt Logic
ROSAR


Main Storage
Odd Array
Even Array
MDR
Addr Decode
Storage Protect
MAR
SPAR
Mark
Storage Bus Out
Storage Bus In
Storage Address Bus
Storage Protection Keys
Unit Address Bus Out
Mark Bus
Unit Address Bus In
Set Odd
Set Even
BCU
Storage Bus Out
Storage Bus In
Storage Addr Bus
Protection Keys
Storage Select and Priority Controls
From D Reg
To S Reg
CPU
From Q Reg
From R Reg
From E Reg
LAR
Local Storage
ROSAR
Read-Only Storage
CPU Control
Q
Instruction Buffer
To LAR
R Inst
Predecoding
E Inst
Execution
D
0-20
STC
S
T
Read Direct
F
A
B
ABC
Serial Adder
IC
G
Write Direct
Parallel Adder
40-60
Channel
Storage Protect Register
Data Address Register
Count Register
Command Register
Flag Reg
Command Address Register
Channel Status Latches
Unit Address Register
Byte Counter
Channel Controls
A Reg
B Reg
Bus Out Latches
Bus In Latches
Mark A Reg
Mark B Reg
Up to six selector channels can be connected.
Standard Interface
Tag Lines
Bus Out
Bus In
Control Unit
I/O Unit
Up to eight control units can be connected to one selector channel.
The number of I/O devices connected to a control unit depends upon the type of I/O device used.
Channel
Main Channel
Multiplex Subchannel
Input OR
Command Reg
CC Command Reg
Data Reg
UAR
Bus Out OR
Bus In OR
Local Store
Selector Subchannel
Control Key
SAB Reg
Key Reg
Storage Bus In OR
A Reg
B Reg
SSC Data OR
IUAR
Int Q Reg
Log Out Reg
Marks OR
Marks Enc
DAB Reg
BC Backup Reg
BC Latches
BC Reg
Byte Enc

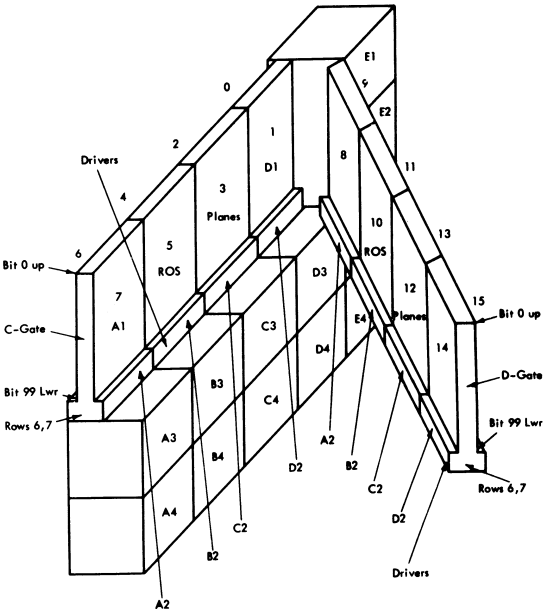


Note 1. Logout word #21 will have correct parity at completion of logout.

Note 2. Some bits are conditional on model of system and on features attached.

Note 3. LADS pages M3021 - M3061 contain logout information also.

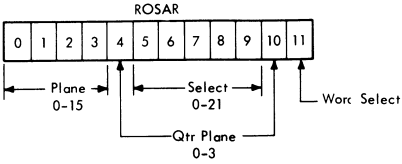
*If storage register has incorrect parity, the storage 1 data check will be turned on.



Read Only Storage

2816 - 100 Bit Words
Sense Amps E_1 and E_2
Sense Latch E_2 and E_3

Note: ROS Physical Layout Details in ED Pages.



Drive Location Chart

Qtr Plane	Select	Card Col	Qtr Plane	Select	Card Col
0	0-10	M6	2	0-10	F6
0	11-21	L6	2	11-21	E6
1	0-10	J6	3	0-10	C6
1	11-21	H6	3	11-21	B6

Select	Pin Col	Pin Col	Pin
0, 11	D	J	4
1, 12	D	J	2
2, 13	D	J	5
3, 14	D	J	6
4, 15	D	J	7
5, 16	B	G	8
6, 17	B	G	7
7, 18	B	G	5
8, 19	B	G	2
9, 20	B	G	3
10, 21	B	G	4

If Selected Plane is on Card Side

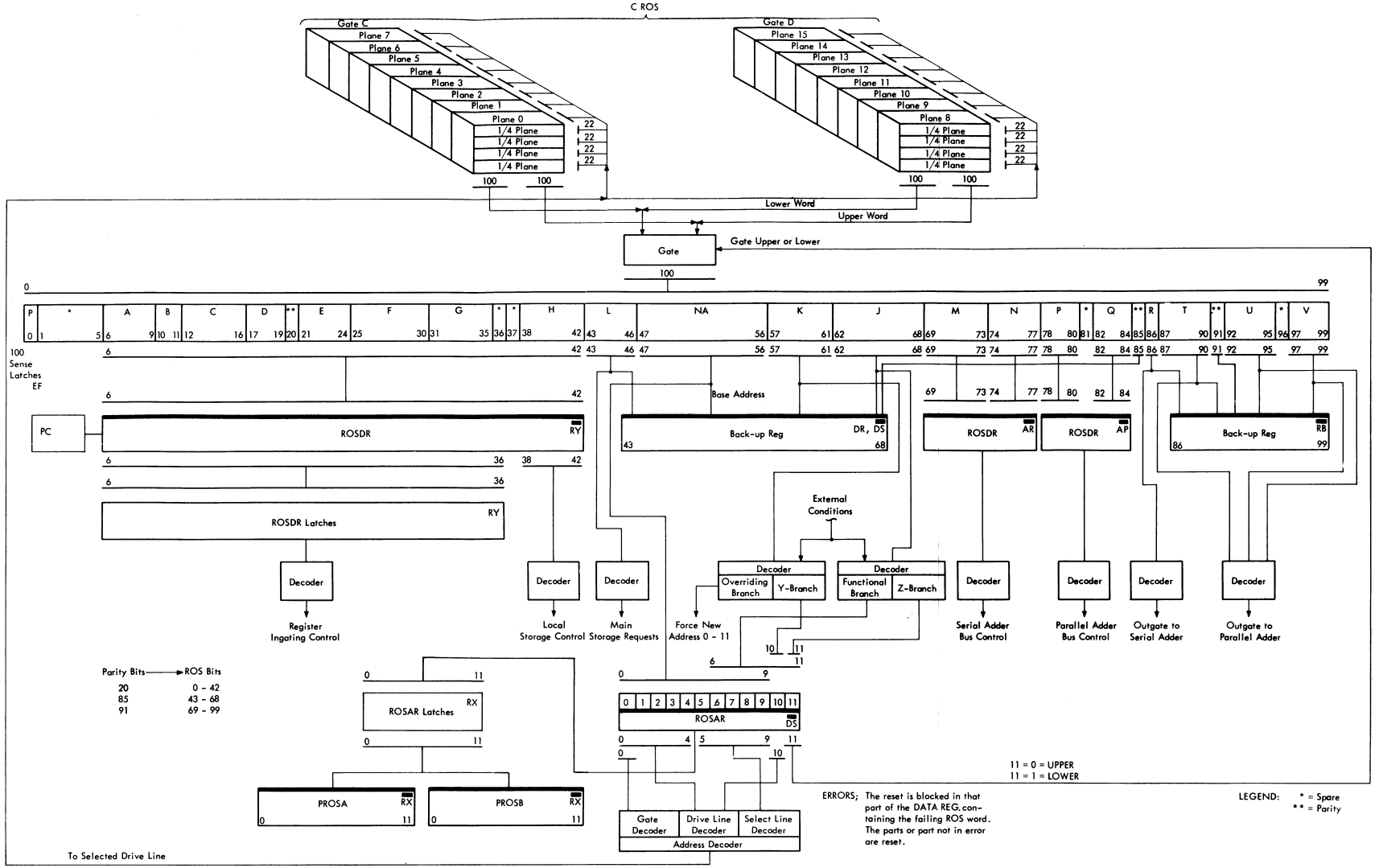
If Selected Plane is on Pin Side

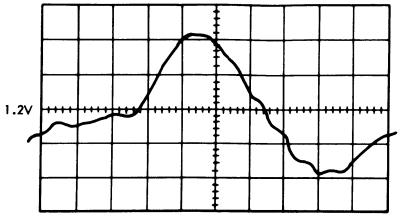
The output of the ROS is read by the sense amplifiers located in boards E1 and E2. Each bit of the 200-bit word is located as shown in Table below.

Bit	0	10	20	30	40	50	60	70	80	90
0u	E1B2G10	E1G2G10	E1B4G10	E1G4G10	E1B6G10	E1G6G10	E2B2G10	E2G2G10	E2B4G10	E2G4G10
01	J10	J10	J10	J10	J10	J10	J10	J10	J10	J10
1u	J12	J12	J12	J12	J12	J12	J12	J12	J12	J12
11	G12	G12	G12	G12	G12	G12	G12	G12	G12	G12
2u	E1C2G10	E1H2G10	E1C4G10	E1H4G10	E1C6G10	E1H6G10	E2C2G10	E2H2G10	E2C4G10	E2H4G10
21	J10	J10	J10	J10	J10	J10	J10	J10	J10	J10
3u	J12	J12	J12	J12	J12	J12	J12	J12	J12	J12
31	G12	G12	G12	G12	G12	G12	G12	G12	G12	G12
4u	E1D2G10	E1J2G10	E1D4G10	E1J4G10	E1D6G10	E1J6G10	E2D2G10	E2J2G10	E2D4G10	E2J4G10
41	J10	J10	J10	J10	J10	J10	J10	J10	J10	J10
5u	J12	J12	J12	J12	J12	J12	J12	J12	J12	J12
51	G12	G12	G12	G12	G12	G12	G12	G12	G12	G12
6u	E1E2G10	E1K2G10	E1E4G10	E1K4G10	E1E6G10	E1K6G10	E2E2G10	E2K2G10	E2E4G10	E2K4G10
61	J10	J10	J10	J10	J10	J10	J10	J10	J10	J10
7u	J12	J12	J12	J12	J12	J12	J12	J12	J12	J12
71	G12	G12	G12	G12	G12	G12	G12	G12	G12	G12
8u	E1F2G10	E1L2G10	E1F4G10	E1L4G10	E1F6G10	E1L6G10	E2F2G10	E2L2G10	E2F4G10	E2L4G10
81	J10	J10	J10	J10	J10	J10	J10	J10	J10	J10
9u	J12	J12	J12	J12	J12	J12	J12	J12	J12	J12
91	G12	G12	G12	G12	G12	G12	G12	G12	G12	G12

The 100-bit ROS control word is contained in the Sense latches located in boards E2 and E3. Each bit is located as shown in Table below.

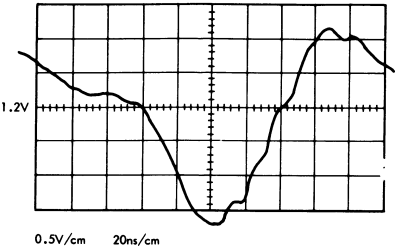
Bit	0	10	20	30	40	50	60	70	80	90
0	E3E2J13	E3H2J13	E3D4J13	E3H4J13	E3E6J13	E3J6J13	E2B6J10	E3H6J11	E2C6J12	E2H6J09
1	J10	J12	J10	J12	J10	J12	J12	J09	J09	J10
2	J11	J10	J11	J10	J11	J10	J09	J12	J10	J12
3	J12	J11	J12	J11	J12	J11	J11	J10	J11	J13
4	J09	J09	J09	J09	J09	J09	J13	J13	J13	J11
5	E3F2J10	E3J2J10	E3E4J10	E3J4J10	E3F6J10	E3K6J10	E3F4J12	E2L6J13	E2E6J13	E2K6J11
6	J09	J09	J09	J09	J09	J09	J09	J11	J10	J12
7	J13	J12	J13	J12	J13	J12	J13	J12	J09	J13
8	J12	J13	J12	J13	J12	J13	J11	J10	J12	J09
9	J11	J11	J11	J11	J11	J11	J10	J09	J13	J10


C ROS
Gate C
Plane 7
Plane 6
Plane 5
Plane 4
Plane 3
Plane 2
Plane 1
Plane 0
1/4 Plane
1/4 Plane
1/4 Plane
1/4 Plane
22
22
22
22
100
100
Gate D
Plane 15
Plane 14
Plane 13
Plane 12
Plane 11
Plane 10
Plane 9
Plane 8
1/4 Plane
1/4 Plane
1/4 Plane
1/4 Plane
22
22
22
22
100
100
Lower Word
Upper Word
Gate
Gate Upper or Lower
100
0
99
P
*
A
B
C
D
**
E
F
G
*
*
H
L
NA
K
J
M
N
P
*
Q
**
R
T
**
U
*
V
0 1 5 6 9 10 11 12 16 17 19 20 21 24 25 30 31 35 36 37 38 42 43 46 47 56 57 61 62 68 69 73 74 77 78 80 81 82 84 85 86 87 90 91 92 95 96 97 99
100 Sense Latches EF
6 42 43 46 47 56 57 61 62 68 69 73 74 77 78 80 82 84 85 86 87 90 91 92 95 97 99
6 42
Base Address
69 73 74 77 78 80 82 84
PC
ROSDR
RY
Back-up Reg
DR, DS
43 68
ROSDR
AR
ROSDR
AP
Back-up Reg
RB
86 99
6 36 38 42
6 36
ROSDR Latches
RY
External Conditions
Decoder
Overriding Branch
Y-Branch
Decoder
Functional Branch
Z-Branch
Decoder
Decoder
Decoder
Decoder
Register Ingating Control
Local Storage Control
Main Storage Requests
Force New Address 0 - 11
Serial Adder Bus Control
Parallel Adder Bus Control
Outgate to Serial Adder
Outgate to Parallel Adder
10 11
6 11
Parity Bits → ROS Bits
20 0 - 42
85 43 - 68
91 69 - 99
0 11
ROSAR Latches
RX
0 11
0 9
0 1 2 3 4 5 6 7 8 9 10 11
ROSAR
DS
0 4 5 9 11
0 10
11 = 0 = UPPER
11 = 1 = LOWER
PROSA
RX
0 11
PROSB
RX
0 11
Gate Decoder
Drive Line Decoder
Select Line Decoder
Address Decoder
To Selected Drive Line
ERRORS; The reset is blocked in that part of the DATA REG. containing the failing ROS word. The parts or part not in error are reset.
LEGEND: * = Spare
** = Parity



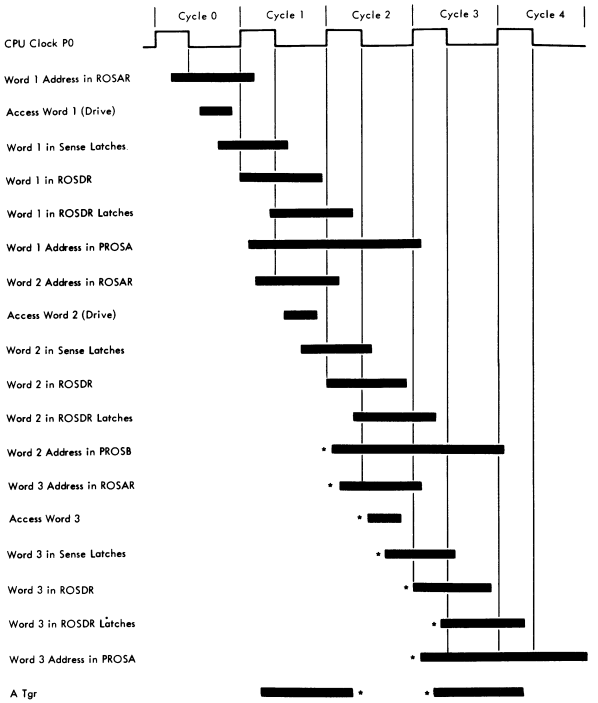
Bit "X"
Adr "YYY"

Normal Output of
1524 (C-13 Mod) "1" Bit



Bit "X"
Adr "YYW"

Normal Output of
1524 (C-13 Mod) "0" Bit



*If a ROS Parity error is detected in cycle 1, these steps will not be performed.

1. Main Storage Address Compare: ALD Page MA 311

   Gate: 01A-A4N3B6
   01B-D3N2D13
   01C-B3A5B12
   01E-E2N2D11

   E.C. 705168 brings these Sync signals to B.N.C. connectors on the front of Gate C. B.N.C. to Scope Probe adapter is P/N 453199

2. ROS Address Compare

   Gate: 01C-A3H5B10

   Stop On ROS Compare: Jumper 01C-A3H5B10 to 01E-E2M4D09

3. FLT SYNC Address = 150

4. I/O Operation Sync Points: ALD - DN 051

   a. Start I/O 01B-E4G7B03
   b. Test I/O 01B-E4G7D10
   c. Halt I/O 01B-E4G7B04
   d. Test Channel 01B-E4G6B03

5. Pulsing a Pushbutton at 16-ms Rate:

   a. Jumper 01A-C2D6D4 to 01E-E2F7B03
   b. Depress desired button

6. Degate Indicators During Logout:

   a. Jumper 01E-B4K4B02 to Ground
   b. Jumper 01E-B4K4D11 to Ground

7. 2365 Main Storage Address Compare: C-B3L2J6

STORAGE BUS TERMINATORS

A. Terminating cards (P/N 5800549) in following locations on all 2065's:

1. Models G, H, I, or IH

03C-C1L6
03C-C1L7

2. Model J

07C-C1L6
07C-C1L7

B. Terminating cards (P/N 5800549) in following locations on machines Without LCS Attachment:

1. For 2065 Model G or H

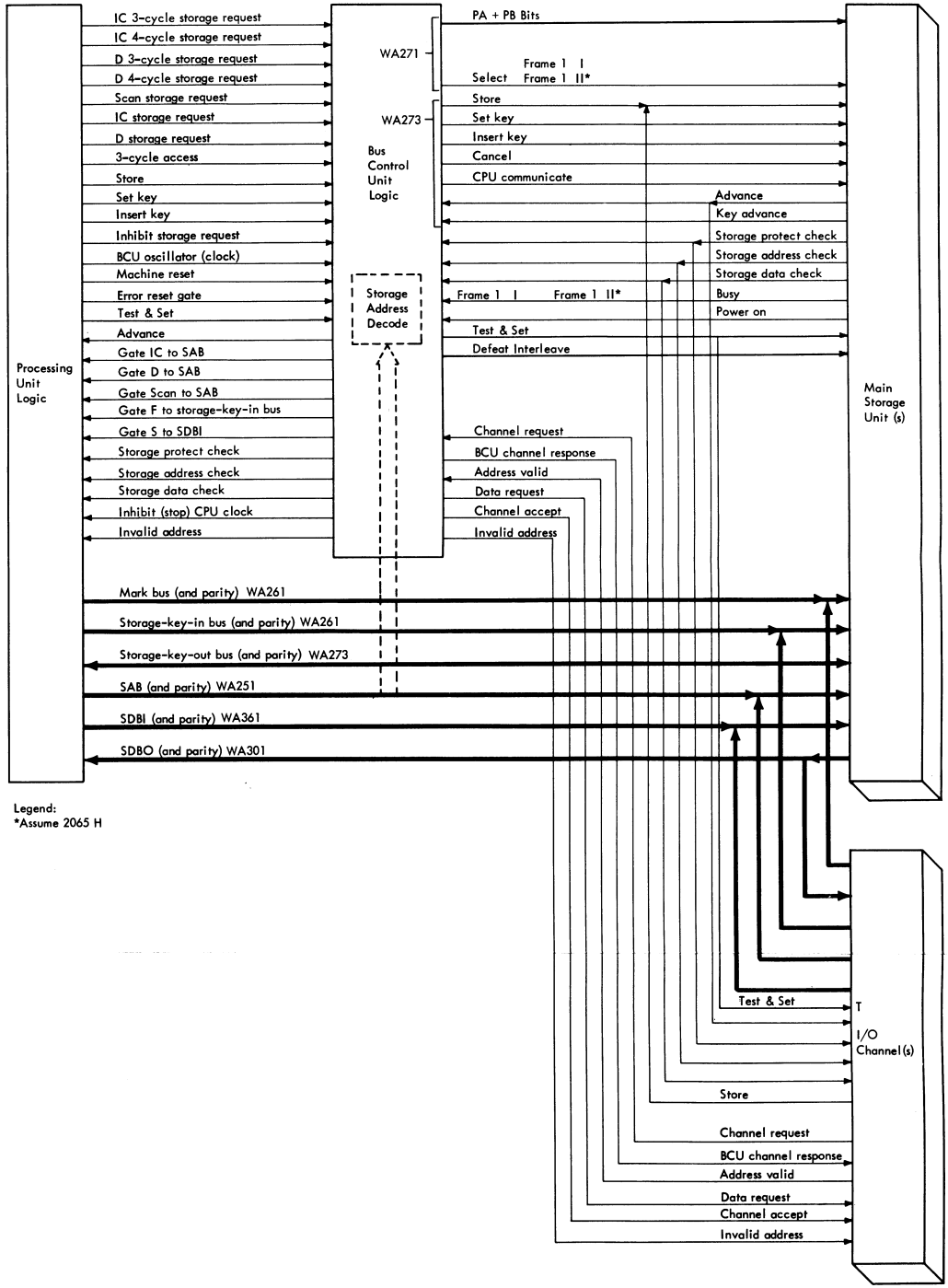
	01A-A1A6	01A-A3A4
01	01A-A1A7	01A-A3A5
	01A-A1B5	01A-A3A6
	01A-A2A3	01A-A4A3
	01A-A2A4	01A-A4A4
	01A-A2A5	01A-A4A5
	01A-A2A6	01A-A4A6
	01A-A2A7	01A-A4A7
	01A-A2C3	01A-A4C3
	01A-A2C5	01B-E4N3
	01A-A3A2	01B-E4N7
	01A-A3A3	

2. For 2065 Models I and IH

05C-C1M2	05C-C2N2
05C-C1N2	05C-C2M3
05C-C1M3	05C-C2N3
05C-C1N3	05C-C2M4
05C-C1M4	05C-C2N4
05C-C1N4	05C-C2M5
05C-C1M5	05C-C2N5
05C-C1N5	05C-C2M6
05C-C1M6	05C-C2N6
05C-C1N6	05C-C2M7
05C-C1N7	05C-C2N7
05C-C2M2	

3. For 2065 Model J

09C-C1M2	09C-C2N2
09C-C1N2	09C-C2M3
09C-C1M3	09C-C2N3
09C-C1N3	09C-C2M4
09C-C1M4	09C-C2N4
09C-C1N4	09C-C2M5
09C-C1M5	09C-C2N5
09C-C1N5	09C-C2M6
09C-C1M6	09C-C2N6
09C-C1N6	09C-C2M7
09C-C1N7	09C-C2N7
09C-C2M2	



Legend:
*Assume 2065 H

Operating Procedure

1. Mount ROS test supplied with system on appropriate I/O unit (tape reel, hypertape cartridge, disc pack, etc.).

2. Set load unit switches to address of I/O unit.

3. Set Test Mode key to ROS position. Set CPU Check key to Disable position.

4. Press system reset.

5. Set ST reg to all 1's by setting all data keys to 1 and pressing Store key. Address keys may be at any value.

6. Press Load key.
   Test should stop with the following indications:
   a. S reg=all 1's (roller 1 pos 3)
   b. T reg=all 0's (roller 2 pos 3)
   c. Pass tgr-on (roller 5 pos 2)
   d. Unct tgr-on (roller 5 pos 2)
   e. Erslt tgr-on (roller 5 pos 2)
   f. Bfr 1 tgr-on (roller 5 pos 2)

7. Press Restart FLT I/O key.
   Test should stop with the same indications as above.

8. Press Load key.
   Test should stop with the following indications:
   a. S reg=all D's (hex)
   b. T reg=FFFF0000 (hex)
   c. Fail tgr-on (roller 5 pos 2)
   d. Condt tgr-on (roller 5 pos 2)
   e. Unct tgr-on
   f. Erslt tgr-off
   g. Bfr 1 tgr-on

   If the above stops with their appropriate indications are not observed, there is a hardcore ROS test hardware failure. Refer to maintenance manual 226-2039-1 and M8006 (LADS) for error analysis.

9. Press Restart FLT I/O key.
   There are no further stops until the successful completion of the tests or until an ROS bit error is detected.

   Successful completion:
   Test should stop with the following indications:
   a. S reg=all 1's
   b. T reg=all 1's
   c. Pass tgr-on
   d. CPU test adr 0-3 on (roller 5 pos 2)
   e. Lfthf tgr-on (roller 5 pos 2)
   f. Unct tgr-on
   g. Condt tgr-on
   h. Erslt tgr-on

Error stop:
Errors are displayed as follows:

a. Plane–CPU test adr bits 0-3 (hex) - Roller 5, Pos 2*
b. Word–bits 0-7 (hex) of S reg
c. Bit–bits 8-15 (decimal) of S reg
} Roller 1, Pos 3**

There is no Scopex documentation for failing ROS tests. Refer to ALD's and use oscilloscope to isolate failure. Once the failing address is known, the 'repeat ROS address' facility may be used for scoping in lieu of repeating the failing test.

Certain errors may require a failure pattern for an effective diagnostic approach. Record failing address and bit, and proceed to step 11 to develop this pattern.

10. To continuously repeat a failing test:
    a. Depress Test Mode Repeat key.
    b. Press Start key.
    To stop repeating, raise Repeat key.

11. To continue testing after an error stop, press Restart FLT I/O (Repeat key must be up). Testing will continue until successful completion or another error.

Example:

** 3 E 25

* 4

- Failing ROS Address equals 43E.
- Failing Bit equals Bit 25.
- If ERSLT light is on, Bit 25 was dropped.
- If ERSLT light is off, Bit 25 was picked.

Note: It is normal operation for the PROC CHK light to be on while ROS tests are running.

Operating Procedure

1. Mount FLT's supplied with system on appropriate I/O unit (tape reel, hypertape cartridge, disc pack, etc.).

2. Set Load Unit switches to address of I/O unit.

3. Set Test Mode switch to FLT position. Set CPU Check key to Disable position.

4. Press system reset.

5. Set ST reg to all 1's by setting all data keys to 1 and pressing Store key. Address keys may be at any value.

6. Press Load key.
   Test should stop with the following indications:
   a. S reg=all 1's (roller 1 pos 3)
   b. T reg=all 0's (roller 2 pos 3)
   c. Pass tgr-on (roller 5 pos 2)
   d. Unct tgr-on (roller 5 pos 2)
   e. Erslt tgr-on (roller 5 pos 2)
   f. Bfr 1 tgr-on (roller 5 pos 2)

7. Press Restart FLT I/O key.
   Test should stop with the same indication as above.

8. Press Load key.
   Test should stop with the following indications:
   a. S reg=all D's (hex)
   b. T reg=FEFE0101 (hex)
   c. Fail tgr-on (roller 5 pos 2)
   d. Condt tgr-on (roller 5 pos 2)
   e. Unct tgr-on
   f. Erslt tgr-off
   g. Bfr 1 tgr-on

   If the above stops with their appropriate indications are not observed, there is a hardcore FLT hardware failure.
   Refer to maintenance manual 226-2039-1 for error analysis. Also M8006(LADS).

9. Press Restart FLT I/O key.
   There are no further stops until successful completion of the tests or until an error is detected.

   Successful completion:
   Test should stop with the following indications:
   a. S reg=all 1's
   b. T reg=all 1's
   c. Pass tgr-on
   d. Unct tgr-on

   Note: It is normal operation for the PROC CHK light to be on while FLT's are running.

Error stop:
Errors are displayed as follows:

a. Fail tgr-on
b. Pass and intermittent tgr may be on if the failure is intermittent
c. Condt tgr-on
d. Unct tgr-on
e. The failing test number is displayed in S reg 0-15 (hex). The first digit is the segment in which the failing test is located. If the first digit is zero, it is a zero cycle test. Refer to SI-SO Scopex.

10. To continuously repeat a failing test:
    a. Depress Test Mode Repeat key.
    b. Press Start key.
    To stop repeating, raise Repeat key.

11. To continue testing after an error stop, press Restart FLT I/O (Repeat key must be up). Testing will continue until successful completion or another error.

12. To search for a specific test:
    a. Follow FLT procedure up to and including step 8.
    b. Enter the desired test number in 48-63 of data keys.
    c. Enter the 1's complement of the desired test number in 32-47 of the data keys.
    d. Press Store key.
    e. Depress Test Mode Repeat key.
    f. Press Restart FLT I/O key.
    The tape will be searched until the desired test is located; it will then be repeated continuously.

Scope Setup

1. Repeat failing test (step 10 of FLT procedure).

2. Set ROS address keys to 150 (hex).

3. Sync scope on ROS address sync point at 01C-A3H1.

4. Place one probe on clock P2 01B-C1F7D10 (RB817AC4) or an equivalent point. Three clock pulses should be observed (except for segment B, which will have 2 clock pulses).

5. Use third probe to test the points called out in Scopex, starting with the first line of the test.

Note: Use ALD's in conjunction with Scopex when scoping through a failing test.

Scopex Definitions

1. Zero-cycle Scopex (SI-SO), (Segment 0) 2065 Service Aids, Section 2, Item A5.

Column heading–"NUMB"
This is the test number that will be displayed in S reg 0-15 when a test fails.

Column heading–"V"
A two-character field defining the state a tgr should assume for a given test and the voltage level that should be observed at the specified pin. R=reset, S=set, 1=+ Level, 0= - Level.
Columns headed pin, net, and description are self explanatory.

2. Segment Scopex
   Test number is shown as follows:

   2 1A

   B 32E

   First digit is segment number in hex. Last digits are test numbers within the segment in hex. Zeroes are not printed between the segment and test numbers.

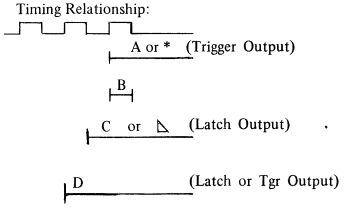
   G/F, G/FI
   Shown adjacent to those points appearing in a sensitive path for the first time in any test. These points should be scoped first, after it has been determined that the output point (first line of test) is incorrect.

NOTE: If there are four or less G/F, G/FI points (including cards listed at the end of the test), replace the specified cards one at a time and rerun the entire test for each card. If the failure is not cleared or there are more than four G/F, G/FI points, use scope to isolate the failure.

Column heading-"V"
A two-character field defining the timing relationship and voltage level that should be observed if the point is not failing.
Voltage level:
1=+ level
0=- level

A or * = During or After
B = During
C = Before or During
D = Before

Timing Relationship:



*More than one card is involved in the feedback loop of a tgr. If this is a failing point, refer to ALD's to determine all of the cards to be changed.

◺ More than one card is involved in the feedback loop of a latch. If this is a failing point, refer to ALD's to determine all of the cards to be changed.

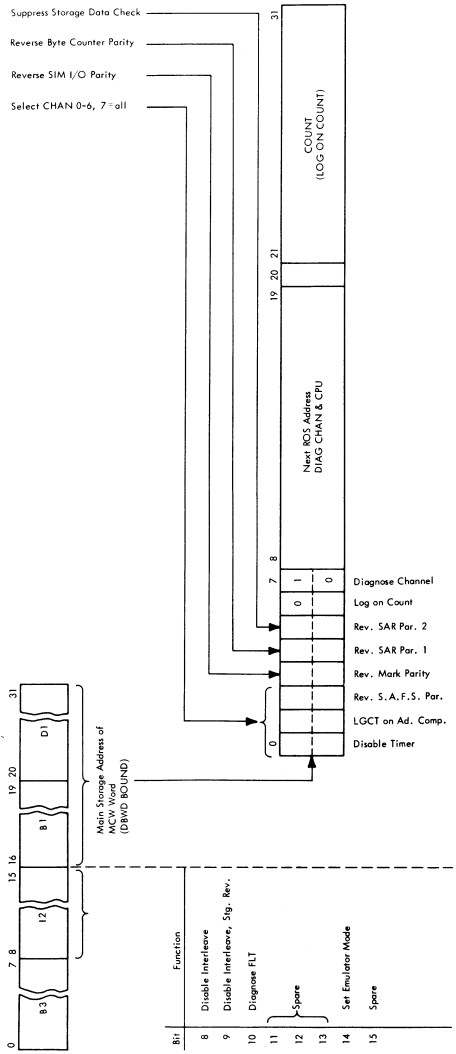
NOTE: The clock displayed above is a normal P2. Triggers that are set by a delayed clock (stat tgr's, 80EM character recognition tgr's, etc.) will have their timings displaced to the right by the amount of the delay. Refer to ALD.s to verify delayed clocks if timings are displaced.

The observed voltage level may be true at times other than specified by the timing information. For example: if Scopex calls out C1 for a particular point and a + DC is observed; this would be a correct indication because the voltage level is true at C time

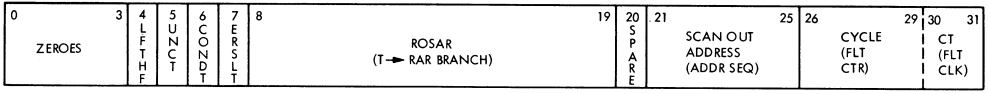
Columns headed "PIN" and "NET" are self-explanatory.

Column headed–"REF."
This reference uniquely identifies each line of print.

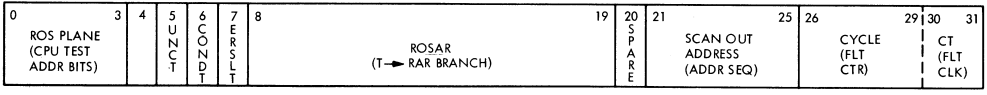
Column headed–"FED BY"
This point is fed by all the references appearing in the 'FED BY' column.
If a line has no 'FED BY', it means that the path has become insensitive past this point and more than one input would have to change to affect the referenced output.


Suppress Storage Data Check
Reverse Byte Counter Parity
Reverse SIM I/O Parity
Select CHAN 0-6, 7 = all
COUNT
(LOG ON COUNT)
Next ROS Address
DIAG CHAN & CPU
Diagnose Channel
Log on Count
Rev. SAR Par. 2
Rev. SAR Par. 1
Rev. Mark Parity
Rev. S.A.F.S. Par.
LGCT on Ad. Comp.
Disable Timer
Main Storage Address of
MCW Word
(DBWD BOUND)
B3
I2
B1
D1
Bit
Function
8 Disable Interleave
9 Disable Interleave, Stg. Rev.
10 Diagnose FLT
11 Spare
12 Spare
13 Spare
14 Set Emulator Mode
15 Spare

FLT MCW



ROS TEST MCW



2065 MAINTENANCE APPROACH

General

Analytical ability and troubleshooting proficiency are not easily taught or learned. Usually, experience is the best teacher in this area. Everyone has some method of troubleshooting. Some ideas are good; some are not. This section of the handbook may aid you in your own diagnostic approach to the Model 65. (Actually, many of the points given here apply to any unit or system.)

Some good general rules, when followed, will aid any troubleshooting approach:

1. Plan in advance - Ask yourself what you would do in the event of trouble in a given area. What would you try first? Is there a simple instruction loop or one-card program that can be used to exercise the failing area? Some mental exercises like this, especially in the areas most susceptible to failure, will pay off. Write down your approach and keep it handy.

2. Have a plan of attack - It can be implemented in a few moments after trouble occurs. Get in the habit of systematically eliminating as large an area as you can as a possible trouble source. Don't jump around and "shoot in the dark."

3. Don't limit yourself - Some people see a red-light machine check and jump right into ALD's. Look around first. There are over 1500 indicators on the system control panel. USE THEM! What instruction is in E-reg? Which register and adder gates are on? What is happening in core and channel at this time? Don't use a scope when the indicators can tell you as much.

4. Keep the diagnostic approach as simple as possible - Don't always use the first failing instruction you find to troubleshoot the problem. Why shoot a register gate trouble using a floating-point long multiply if you can get the trouble to show with an RR add? Don't write a complicated program loop if you can use FLT's.

Gathering Facts

Before starting to look for the trouble, gather up all the facts about it that you can.

Some of the basic 2065 error indications are:

1. Red light (machine check).
2. Wrong results.
3. Hang (or loop).
4. Power drops.

Some typical causes of trouble in the 2065 are:

1. Failing card (either making poor contact, has gunky pin, is loose, or has a defective component).
2. Failing cable.
3. Loss of voltage (lost in such a manner that system power stays up) such as a loose crossover connector.
4. Shorts (cold flow?).
5. Opens.
6. Timing problem.
7. Wiring error (most likely due to EC error).
8. Programming error.
9. Operator error.

Some points to keep in mind while gathering information for troubleshooting are:

1. Does the problem involve a broad area of the machine, or is it localized? Is the system really dead or getting multiple errors? (It could be a missing clock pulse or voltage.)

2. Always suspect the last thing that was done to the system (EC, program change, equipment change, etc.).

3. Don't trust indicator lamps. Many CE's have been misled by burned out indicators. LAMP TEST!

4. Is power up on all units?

Finding The Trouble

1. There are five general ways to shoot troubles in the Model 65.

   a. Ripple storage
   b. ROS test
   c. FLT'S (CPU troubles)
   d. Diagnostics
   e. "Brute force" (manual method)

If you have a red-light CPU error, run ROS and FLT first. For other errors, running FLT's first may still be the best way since it takes so little time to run them. Use your own judgment.

2. As you troubleshoot you will have your own "pilot" errors to contend with in addition to the original trouble. Some typical "pilot" errors at the system console are:

   a. Rate switch in wrong position. (Ever try to load FLT's with the rate switch in single cycle?)

   b. Specification error in the instruction you are trying to repeat or have in the data keys.

   c. Assuming good parity in GPR's and FPR's.

   d. The following sort of thing will happen to you at least once. Suppose you have just stored a small program in core that is supposed to loop on itself. You set IC to the beginning location, set Rate switch to Process, and activate Start. Instead of running your program, the machine does nothing. You left the wait bit on in the PSW. After clearing the wait bit and resetting the IC you again activate Start. Now instead of running your program the machine hangs up in a tight loop with the IC at 1 or 2. This time, your program has something wrong that caused an interrupt. The interrupt sequence stores the current PSW and pulls out a new PSW. Since you probably cleared core in the beginning, the new PSW is all zeros. This means that the machine will start executing instructions after the interrupt, starting at location zero (which also is cleared) and will cause a program interrupt (zero op code). It then goes hung up in a tight interrupt loop.

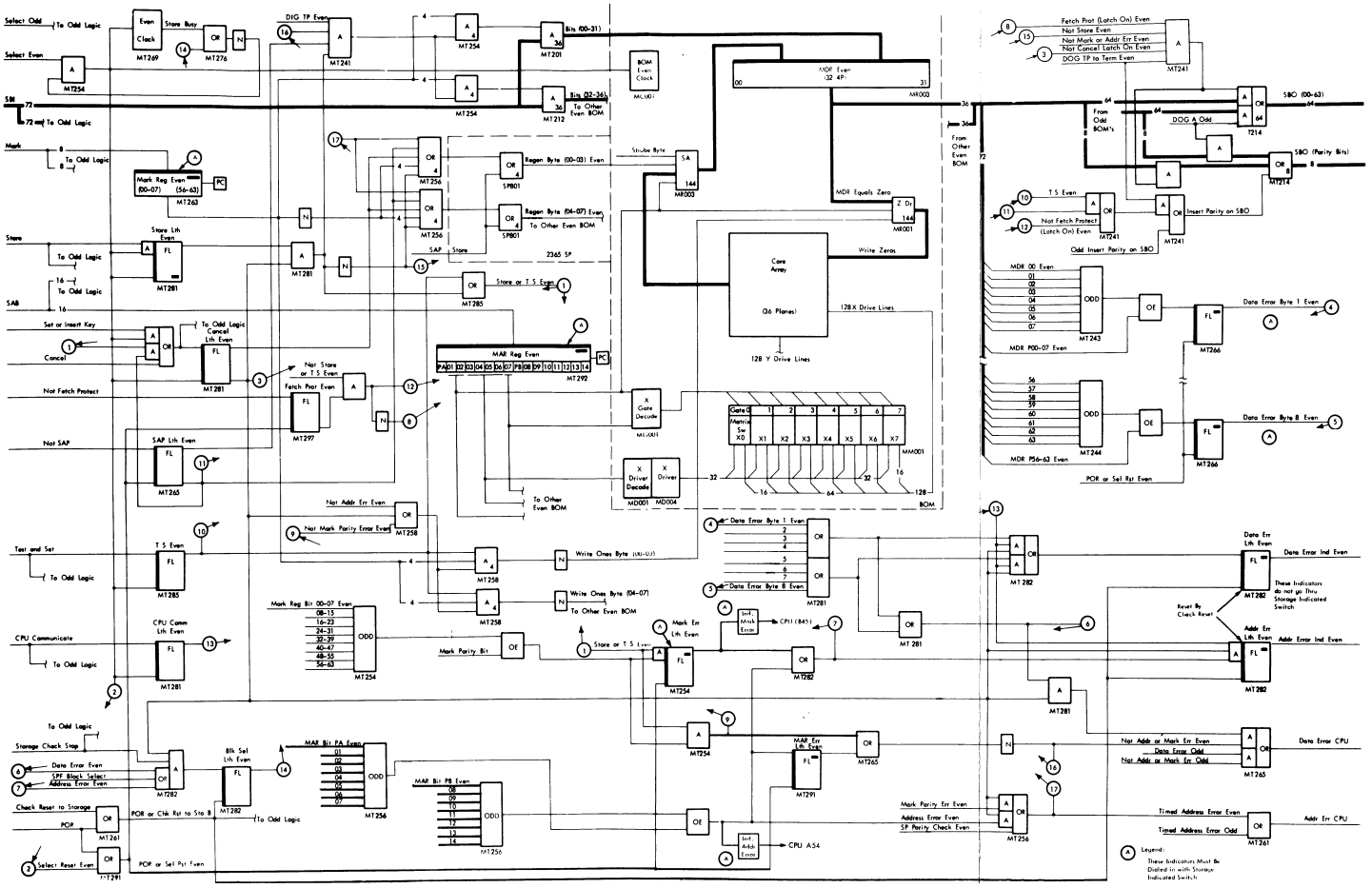
   e. If you try to do any store class of instruction (any one that puts something in storage - e.g., ST, STH, CVD, RDD, most SS, and others), it will bomb out if the PSW key is not zero (unless you are lucky enough to get a match).

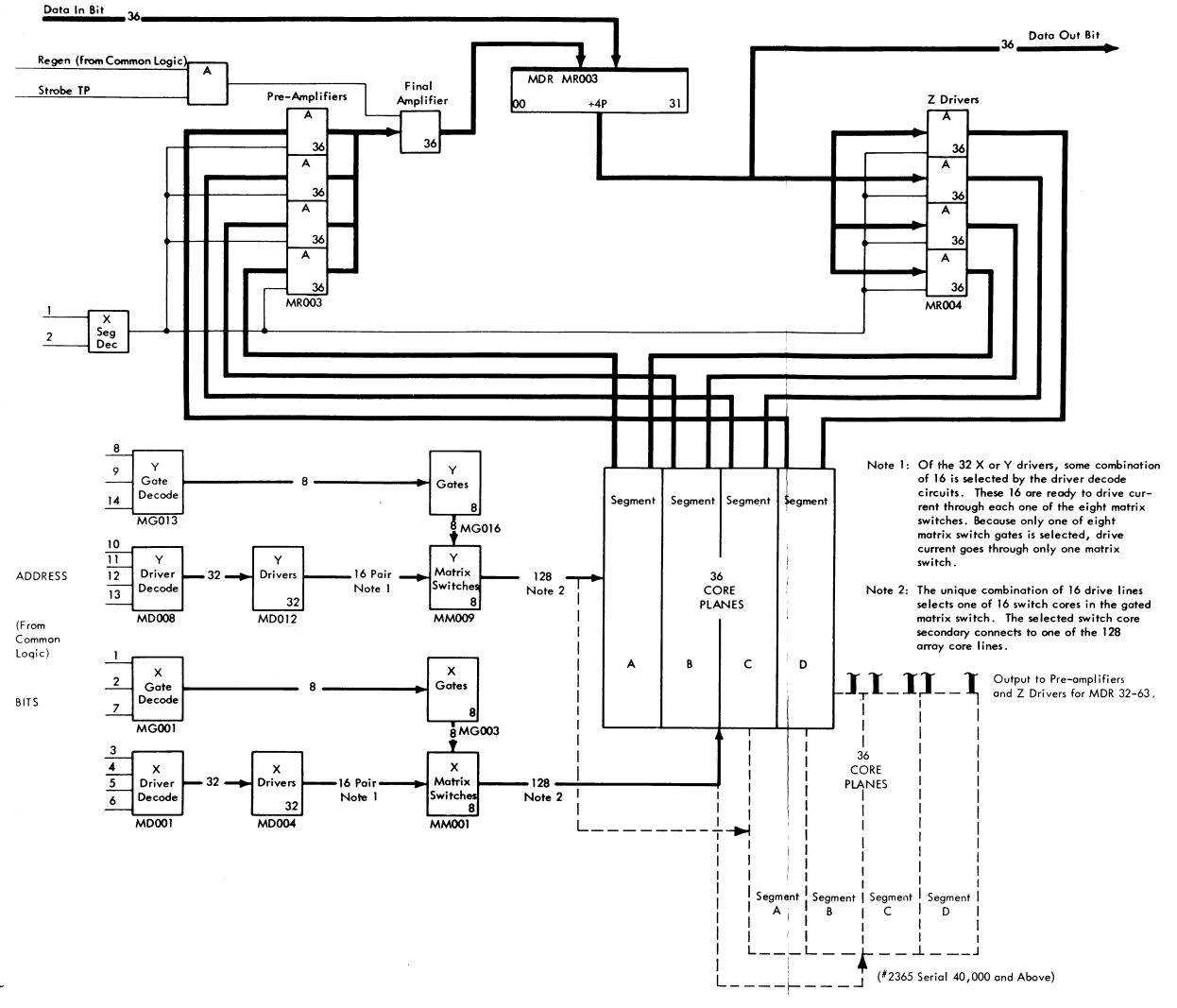
3. Try to isolate trouble by halving the amount of circuitry involved with each step. For example, if you start at a red-light indicator driver and scope backward through the ALD's a logic block at a time, you will reach the trouble (eventually). Rather, go back to some point in the middle that you know must be good or it will cause the indicated trouble. Scope it and go from there, forward or backward, but PLEASE, not a block at a time.

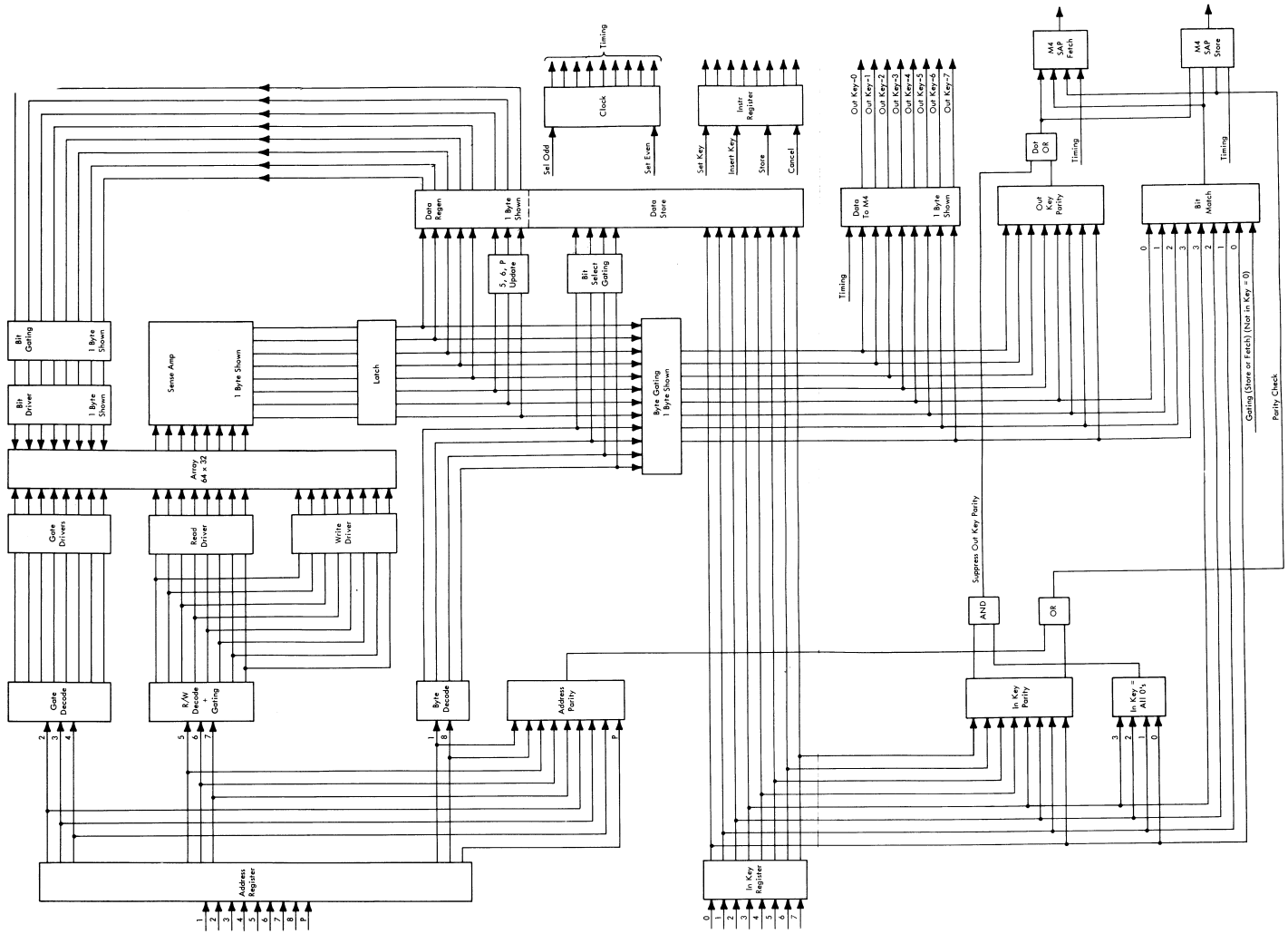
4. If you seem to be getting nowhere in troubleshooting a particular bug, go back and recheck that symptom you saw earlier (the one on which you have been basing all your efforts). It's easy to misread an indication.

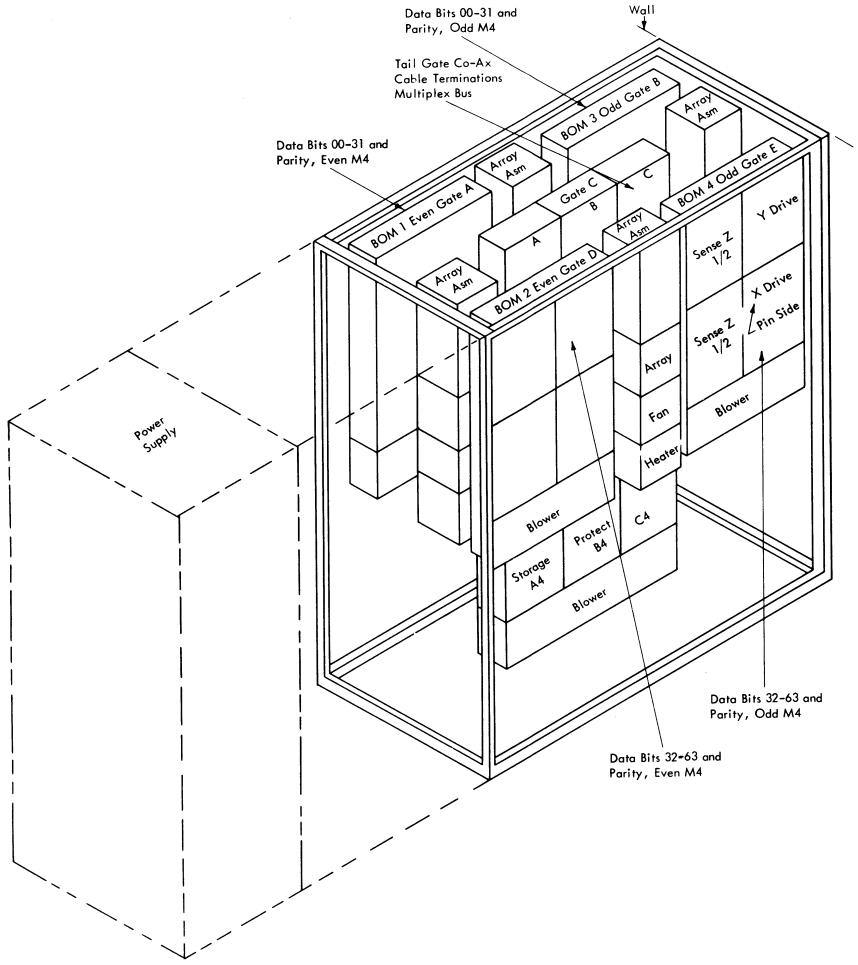
5. If you're still having trouble, look at the indicators.

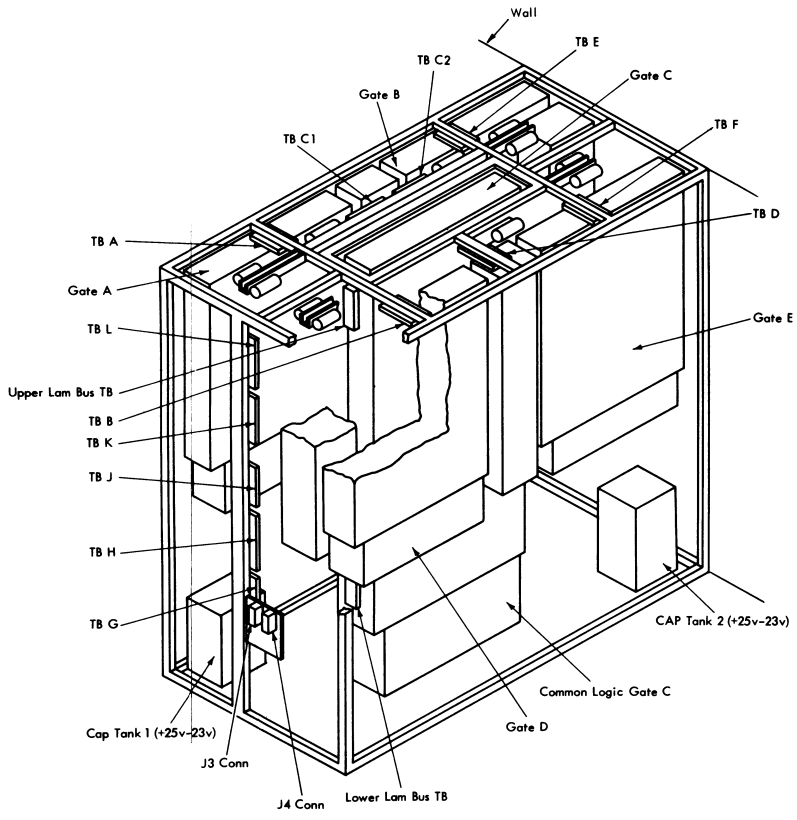
6. Do you have more than one trouble? (Not too likely, but it does happen.) Also, you may have only one trouble (one symptom) but several bad components. Perhaps a power surge or a short has wiped out more than one card of the same type and you've been swapping bad cards.

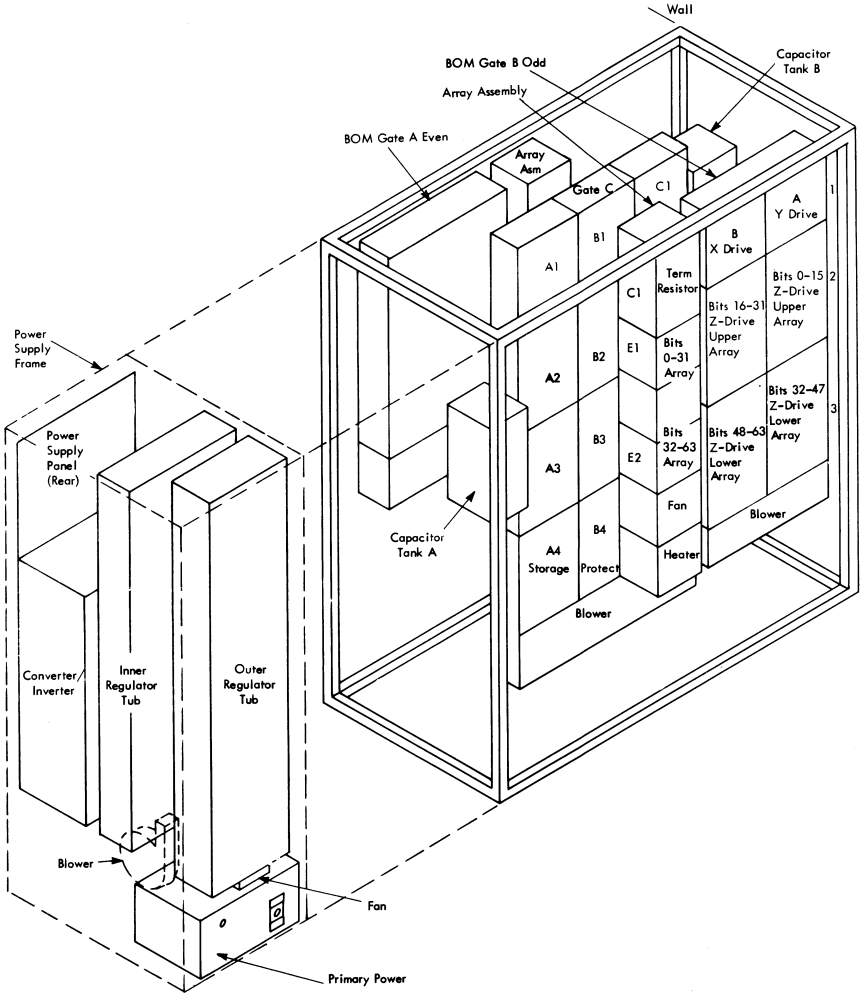

Select Odd
To Odd Logic
Select Even
SBI
To Odd Logic
Even Clock
Store Busy
MT269
MT276
DIG TP Even
MT241
MT254
Bits (00-31)
Bits (32-36)
To Other Even BOM
MT201
MT212
BOM Even Clock
MC001
MDR Even (32 BP)
MR003
Fetch Prot (Latch On) Even
Not Store Even
Not Mark or Addr Err Even
Not Cancel Latch On Even
DOG TP to Term Even
SBO (00-63)
SBO (Parity Bits)
From Odd BOM's
From Other Even BOM
DOG A Odd
MT214
Mark
Mark Reg Even (00-07) (56-63)
MT263
Regen Byte (00-03) Even
Regen Byte (04-07) Even
SP801
Strobe Byte
MR003
MDR Equals Zero
MR001
T S Even
Not Fetch Protect (Latch On) Even
Insert Parity on SBO
Odd Insert Parity on SBO
MT241
Store
Store Lth Even
MT281
SAP - Store
2365 SP
Store or T S Even
MT285
Core Array
(36 Planes)
128 X Drive Lines
128 Y Drive Lines
MDR 00 Even
MDR P00-07 Even
MDR 56-63 Even
MT243
MT244
MT266
Data Error Byte 1 Even
Data Error Byte 8 Even
SAB
Set or Insert Key
Cancel
To Odd Logic Cancel Lth Even
Not Fetch Protect
Not SAP
SAP Lth Even
MT265
Not Store or T S Even
Fetch Prot Even
MT297
MAR Reg Even
MT292
X Gate Decode
MC001
X Driver Decode
MD001
X Driver
MD004
Gate G Matrix Sw X0
MM001
To Other Even BOM
Not Addr Err Even
Not Mark Parity Error Even
MT258
Test and Set
T S Even
MT285
Write Ones Byte (00-03)
Write Ones Byte (04-07)
To Other Even BOM
Mark Reg Bit 00-07 Even
Mark Parity Bit
MT254
Mark Err Lth Even
Store or T S Even
Inst Mark Error
CPU (845)
MT282
MT281
CPU Communicate
CPU Comm Lth Even
Data Err Lth Even
Data Error Ind Even
Addr Err Lth Even
Addr Error Ind Even
Reset By Check Reset
These Indicators do not go Thru Storage Indicated Switch
Storage Check Stop
Data Error Even
SPF Block Select Address Error Even
Blk Set Lth Even
MAR Bit PA Even
MAR Bit PB Even
MT256
Not Addr or Mark Err Even
Data Error Odd
Not Addr or Mark Err Odd
Data Error CPU
Check Reset to Storage
POR
MT261
POR or Chk Rst to Sto B
To Odd Logic
Select Reset Even
MT291
POR or Sel Rst Even
MAR Err Lth Even
Mark Parity Err Even
Address Error Even
SP Parity Check Even
Inst Addr Error
CPU A54
Timed Address Error Even
Timed Address Error Odd
Addr Err CPU
Legend:
These Indicators Must Be Dialed In with Storage Indicated Switch

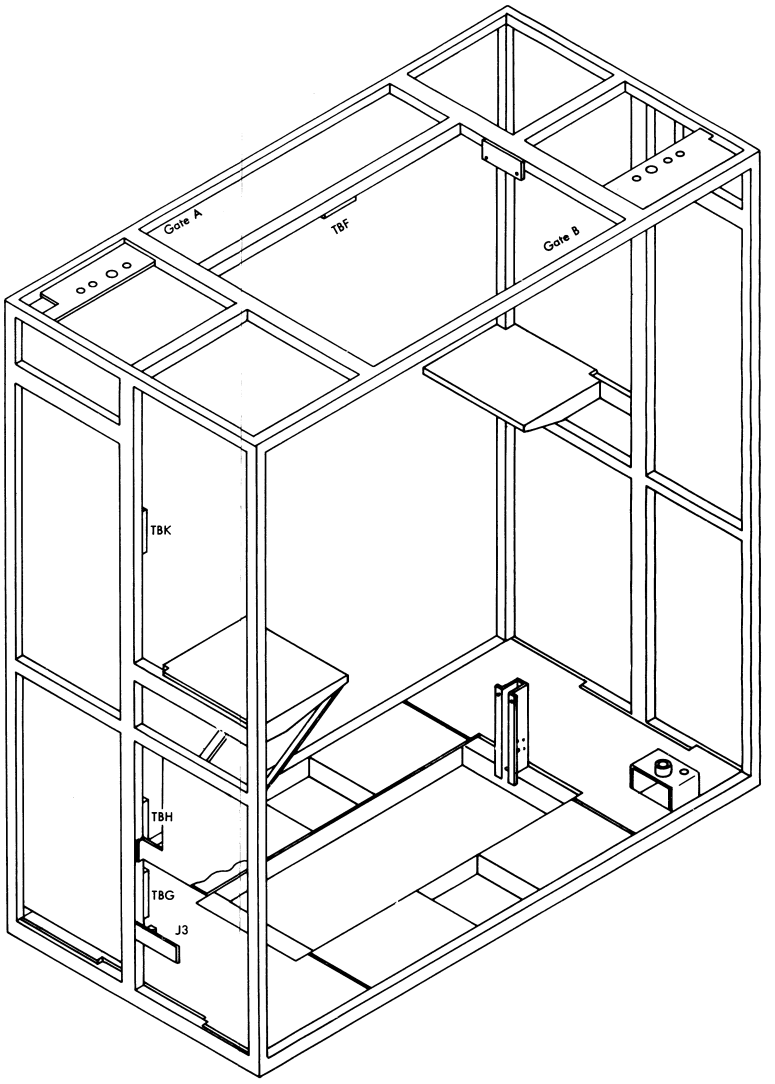

Data In Bit
36
Regen (from Common Logic)
Strobe TP
A
Pre-Amplifiers
Final Amplifier
MDR MR003
00
+4P
31
36
Data Out Bit
Z Drivers
MR003
MR004
1
2
X Seg Dec
8
9
14
Y Gate Decode
MG013
Y Gates
MG016
10
11
12
13
Y Driver Decode
MD008
32
Y Drivers
MD012
16 Pair Note 1
Y Matrix Switches
MM009
128 Note 2
ADDRESS
(From Common Logic)
BITS
1
2
7
X Gate Decode
MG001
X Gates
MG003
3
4
5
6
X Driver Decode
MD001
X Drivers
MD004
X Matrix Switches
MM001
Segment
A
B
C
D
36 CORE PLANES
Note 1: Of the 32 X or Y drivers, some combination of 16 is selected by the driver decode circuits. These 16 are ready to drive current through each one of the eight matrix switches. Because only one of eight matrix switch gates is selected, drive current goes through only one matrix switch.
Note 2: The unique combination of 16 drive lines selects one of 16 switch cores in the gated matrix switch. The selected switch core secondary connects to one of the 128 array core lines.
Output to Pre-amplifiers and Z Drivers for MDR 32-63.
(#2365 Serial 40,000 and Above)

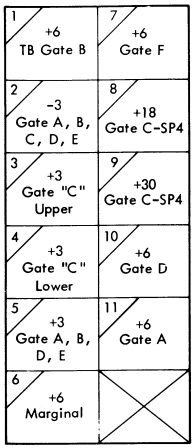

Timing
Clock
Sel Odd
Sel Even
Instr Register
Set Key
Insert Key
Store
Cancel
Out Key-0
Out Key-1
Out Key-2
Out Key-3
Out Key-4
Out Key-5
Out Key-6
Out Key-7
M4 SAP Fetch
M4 SAP Store
Dor OR
Timing
Data Regen
1 Byte Shown
Data Store
Data To M4
Out Key Parity
Bit Match
S, d, P Update
Bit Select Gating
Bit Gating
Bit Driver
Sense Amp
Latch
Byte Gating 1 Byte Shown
Array 64 x 32
Gate Drivers
Read Driver
Write Driver
Suppress Out Key Parity
AND
OR
Gate Decode
R/W Decode + Gating
Byte Decode
Address Parity
In Key Parity
In Key = All 0's
Address Register
In Key Register
Gating (Store or Fetch) (Not in Key = 0)
Parity Check


Data Bits 00-31 and Parity, Odd M4
Wall
Tail Gate Co-Ax Cable Terminations Multiplex Bus
Data Bits 00-31 and Parity, Even M4
BOM 3 Odd Gate B
Array Asm
BOM 1 Even Gate A
Array Asm
Gate C
C
B
A
Array Asm
BOM 4 Odd Gate E
Array Asm
BOM 2 Even Gate D
Sense Z 1/2
Y Drive
Sense Z 1/2
X Drive
Pin Side
Array
Fan
Heater
Blower
Power Supply
Blower
Protect B4
C4
Storage A4
Blower
Data Bits 32-63 and Parity, Odd M4
Data Bits 32-63 and Parity, Even M4

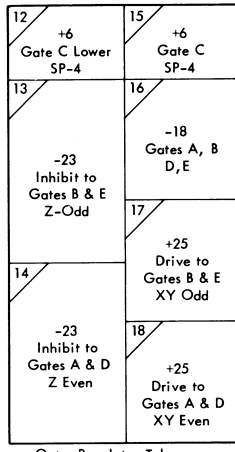

Wall
TB E
TB C2
Gate C
Gate B
TB F
TB C1
TB D
TB A
Gate A
Gate E
TB L
Upper Lam Bus TB
TB B
TB K
TB J
TB H
TB G
CAP Tank 2 (+25v-23v)
Common Logic Gate C
Gate D
Cap Tank 1 (+25v-23v)
J3 Conn
J4 Conn
Lower Lam Bus TB


Wall
BOM Gate B Odd
Capacitor Tank B
Array Assembly
BOM Gate A Even
Array Asm
Gate C
C1
A
Y Drive
B
X Drive
B1
A1
C1
Term Resistor
Bits 0-15 Z-Drive Upper Array
Bits 16-31 Z-Drive Upper Array
E1
Bits 0-31 Array
A2
B2
Bits 32-47 Z-Drive Lower Array
Bits 48-63 Z-Drive Lower Array
Bits 32-63 Array
E2
A3
B3
Fan
Blower
Heater
A4 Storage
Protect
B4
Blower
1
2
3
Power Supply Frame
Power Supply Panel (Rear)
Capacitor Tank A
Converter/ Inverter
Inner Regulator Tub
Outer Regulator Tub
Blower
Fan
Primary Power


Gate A
TBF
Gate B
TBK
TBH
TBG
J3

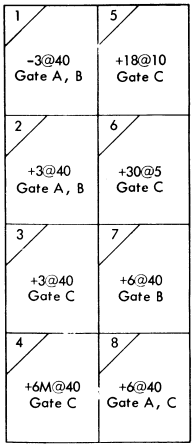


Inner Regulator Tub

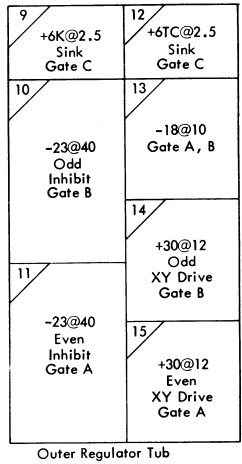


Outer Regulator Tub

ALD - YM Power Supply SN 30,000 - 2365

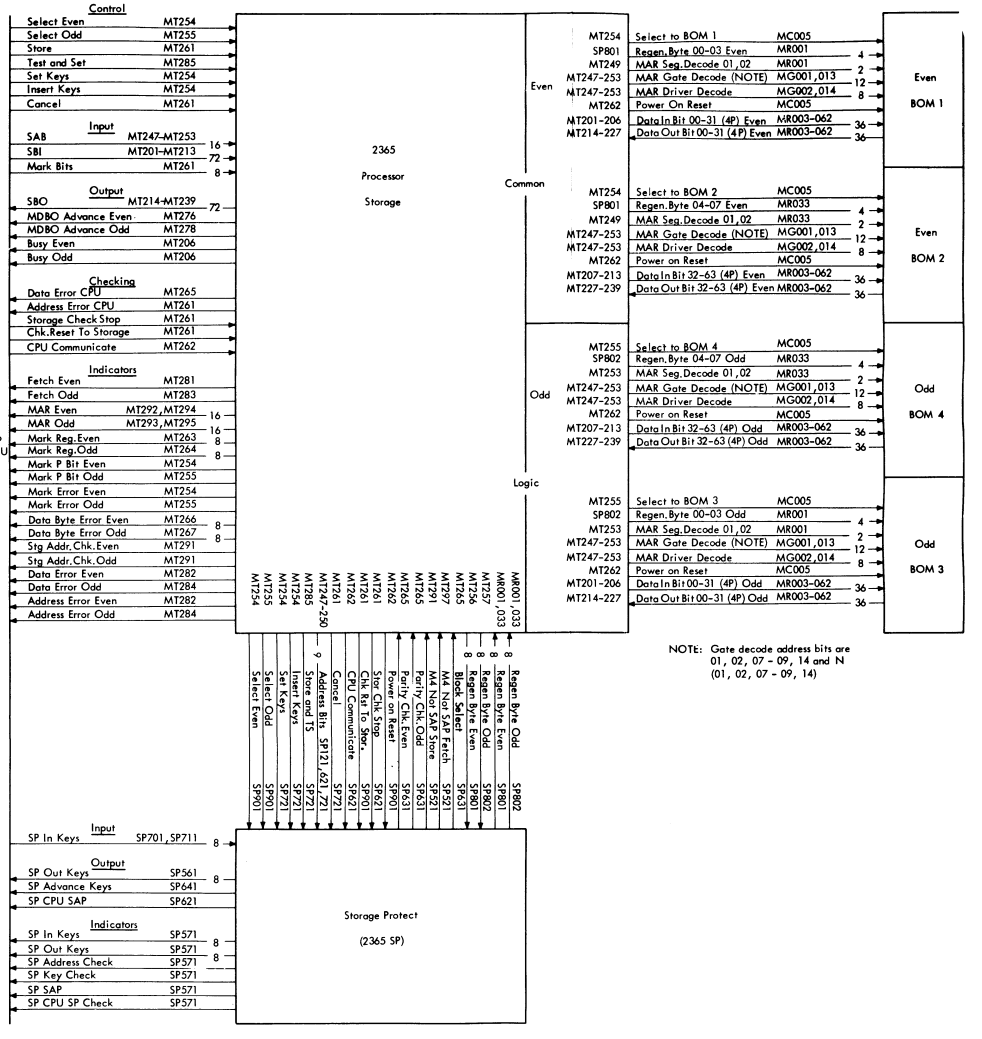


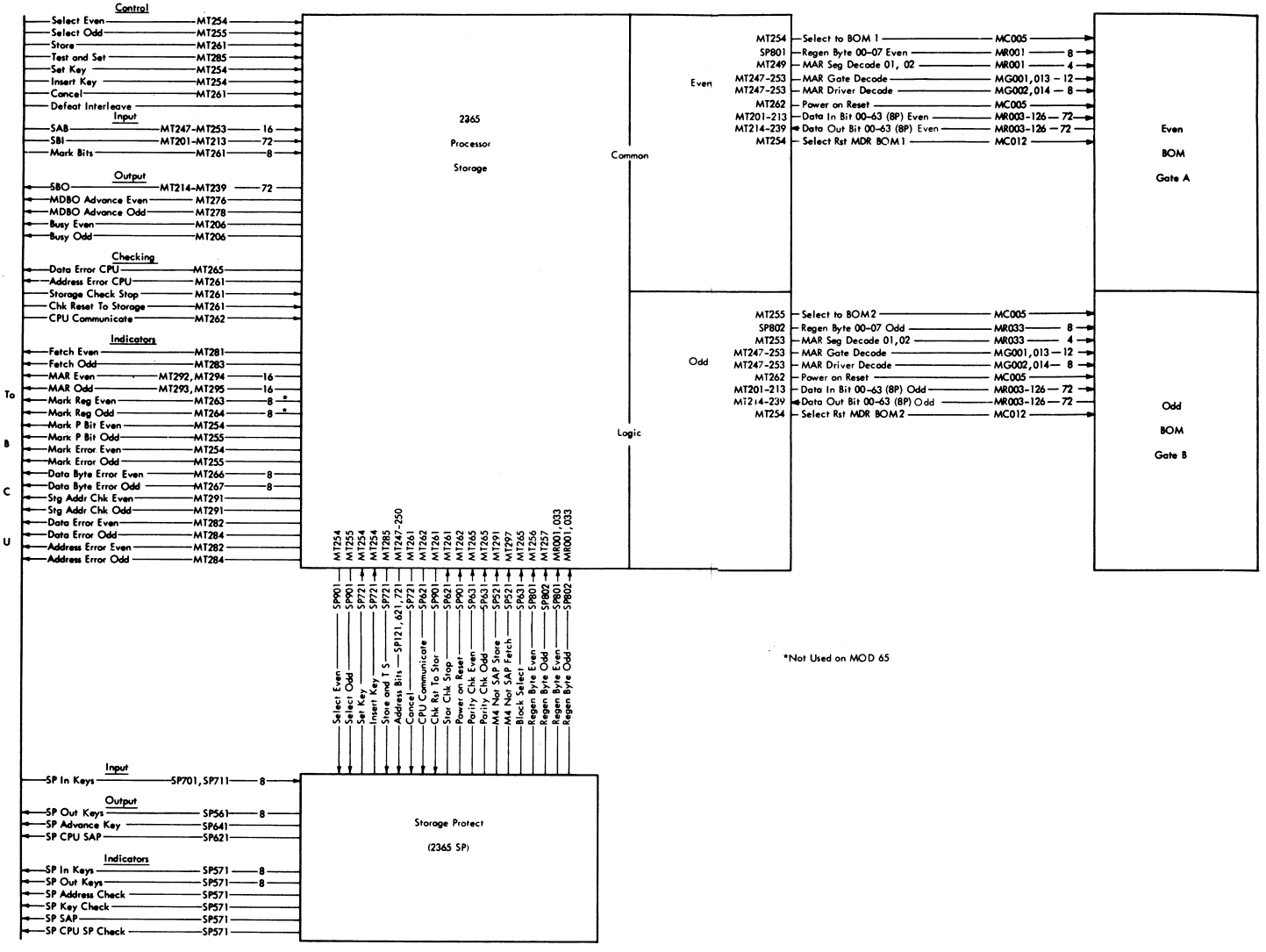
Inner Regulator Tub

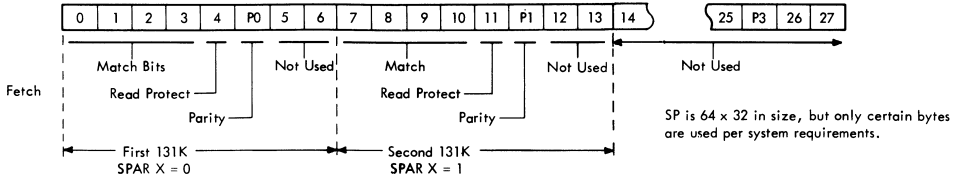


Outer Regulator Tub

SN 40,000 - 2365


Control
Select Even MT254
Select Odd MT255
Store MT261
Test and Set MT285
Set Keys MT254
Insert Keys MT254
Cancel MT261
Input
SAB MT247-MT253 16
SBI MT201-MT213 72
Mark Bits MT261 8
Output
SBO MT214-MT239 72
MDBO Advance Even MT276
MDBO Advance Odd MT278
Busy Even MT206
Busy Odd MT206
Checking
Data Error CPU MT265
Address Error CPU MT261
Storage Check Stop MT261
Chk.Reset To Storage MT261
CPU Communicate MT262
Indicators
Fetch Even MT281
Fetch Odd MT283
MAR Even MT292,MT294 16
MAR Odd MT293,MT295 16
To BCU
Mark Reg.Even MT263 8
Mark Reg.Odd MT264 8
Mark P Bit Even MT254
Mark P Bit Odd MT255
Mark Error Even MT254
Mark Error Odd MT255
Data Byte Error Even MT266 8
Data Byte Error Odd MT267 8
Stg Addr.Chk.Even MT291
Stg Addr.Chk.Odd MT291
Data Error Even MT282
Data Error Odd MT284
Address Error Even MT282
Address Error Odd MT284
2365
Processor
Storage
Common
Even
Odd
Logic
MT254 MT255 MT254 MT254 MT285 MT254 MT247-250 MT261 MT262 MT261 MT261 MT262 MT265 MT265 MT291 MT297 MT265 MT257 MT256 MR001,033 MR001,033
9
8 8 8 8
Select Even
Select Odd
Set Keys
Insert Keys
Store and TS
Address Bits SP121,621,721
Cancel
CPU Communicate
Chk.Rst To Stor.
Stor.Chk.Stop
Power on Reset
Parity Chk.Even
Parity Chk.Odd
M4 Not SAP Store
M4 Not SAP Fetch
Block Select
Regen Byte Even
Regen Byte Odd
Regen Byte Even
Regen Byte Odd
SP901 SP901 SP721 SP721 SP721 SP721 SP621 SP721 SP621 SP901 SP901 SP631 SP631 SP521 SP521 SP631 SP801 SP802 SP801 SP802
Input
SP In Keys SP701,SP711 8
Output
SP Out Keys SP561 8
SP Advance Keys SP641
SP CPU SAP SP621
Indicators
SP In Keys SP571
SP Out Keys SP571 8
SP Address Check SP571 8
SP Key Check SP571
SP SAP SP571
SP CPU SP Check SP571
Storage Protect
(2365 SP)
MT254 Select to BOM 1 MC005
SP801 Regen.Byte 00-03 Even MR001 4
MT249 MAR Seg.Decode 01,02 MR001 2
MT247-253 MAR Gate Decode (NOTE) MG001,013 12
MT247-253 MAR Driver Decode MG002,014 8
MT262 Power On Reset MC005
MT201-206 Data In Bit 00-31 (4P) Even MR003-062 36
MT214-227 Data Out Bit 00-31 (4P) Even MR003-062 36
Even BOM 1
MT254 Select to BOM 2 MC005
SP801 Regen.Byte 04-07 Even MR033 4
MT249 MAR Seg.Decode 01,02 MR033 2
MT247-253 MAR Gate Decode (NOTE) MG001,013 12
MT247-253 MAR Driver Decode MG002,014 8
MT262 Power on Reset MC005
MT207-213 Data In Bit 32-63 (4P) Even MR003-062 36
MT227-239 Data Out Bit 32-63 (4P) Even MR003-062 36
Even BOM 2
MT255 Select to BOM 4 MC005
SP802 Regen.Byte 04-07 Odd MR033 4
MT253 MAR Seg.Decode 01,02 MR033 2
MT247-253 MAR Gate Decode (NOTE) MG001,013 12
MT247-253 MAR Driver Decode MG002,014 8
MT262 Power on Reset MC005
MT207-213 Data In Bit 32-63 (4P) Odd MR003-062 36
MT227-239 Data Out Bit 32-63 (4P) Odd MR003-062 36
Odd BOM 4
MT255 Select to BOM 3 MC005
SP802 Regen.Byte 00-03 Odd MR001 4
MT253 MAR Seg.Decode 01,02 MR001 2
MT247-253 MAR Gate Decode (NOTE) MG001,013 12
MT247-253 MAR Driver Decode MG002,014 8
MT262 Power on Reset MC005
MT201-206 Data In Bit 00-31 (4P) Odd MR003-062 36
MT214-227 Data Out Bit 00-31 (4P) Odd MR003-062 36
Odd BOM 3
NOTE: Gate decode address bits are 01, 02, 07 - 09, 14 and N (01, 02, 07 - 09, 14)


Control
Select Even — MT254
Select Odd — MT255
Store — MT261
Test and Set — MT285
Set Key — MT254
Insert Key — MT254
Cancel — MT261
Defeat Interleave
Input
SAB — MT247-MT253 — 16
SBI — MT201-MT213 — 72
Mark Bits — MT261 — 8
Output
SBO — MT214-MT239 — 72
MDBO Advance Even — MT276
MDBO Advance Odd — MT278
Busy Even — MT206
Busy Odd — MT206
Checking
Data Error CPU — MT265
Address Error CPU — MT261
Storage Check Stop — MT261
Chk Reset To Storage — MT261
CPU Communicate — MT262
Indicators
Fetch Even — MT281
Fetch Odd — MT283
MAR Even — MT292, MT294 — 16
MAR Odd — MT293, MT295 — 16
Mark Reg Even — MT263 — 8 *
Mark Reg Odd — MT264 — 8 *
Mark P Bit Even — MT254
Mark P Bit Odd — MT255
Mark Error Even — MT254
Mark Error Odd — MT255
Data Byte Error Even — MT266 — 8
Data Byte Error Odd — MT267 — 8
Stg Addr Chk Even — MT291
Stg Addr Chk Odd — MT291
Data Error Even — MT282
Data Error Odd — MT284
Address Error Even — MT282
Address Error Odd — MT284
To B C U
2365 Processor Storage
Common
Even
MT254 Select to BOM 1 — MC005
SP801 Regen Byte 00-07 Even — MR001 — 8
MT249 MAR Seg Decode 01, 02 — MR001 — 4
MT247-253 MAR Gate Decode — MG001, 013 — 12
MT247-253 MAR Driver Decode — MG002, 014 — 8
MT262 Power on Reset — MC005
MT201-213 Data In Bit 00-63 (8P) Even — MR003-126 — 72
MT214-239 Data Out Bit 00-63 (8P) Even — MR003-126 — 72
MT254 Select Rst MDR BOM1 — MC012
Even BOM Gate A
Logic
Odd
MT255 Select to BOM2 — MC005
SP802 Regen Byte 00-07 Odd — MR033 — 8
MT253 MAR Seg Decode 01,02 — MR033 — 4
MT247-253 MAR Gate Decode — MG001, 013 — 12
MT247-253 MAR Driver Decode — MG002, 014 — 8
MT262 Power on Reset — MC005
MT201-213 Data In Bit 00-63 (8P) Odd — MR003-126 — 72
MT214-239 Data Out Bit 00-63 (8P) Odd — MR003-126 — 72
MT254 Select Rst MDR BOM2 — MC012
Odd BOM Gate B
MT254 MT255 MT254 MT254 MT285 MT1247-250 MT261 MT262 MT261 MT261 MT262 MT265 MT261 MT291 MT297 MT265 MT256 MT257 MR001, 033 MR001, 033
SP901 SP901 SP721 SP721 SP721 SP721 SP721 SP621 SP901 SP621 SP901 SP631 SP631 SP521 SP521 SP631 SP801 SP802 SP801 SP802
Select Even
Select Odd
Set Key
Insert Key
Store and T S
Address Bits — SP121, 621, 721
Cancel
CPU Communicate
Chk Rst To Stor
Stor Chk Stop
Power on Reset
Parity Chk Even
Parity Chk Odd
M4 Not SAP Store
M4 Not SAP Fetch
Block Select
Regen Byte Even
Regen Byte Odd
Regen Byte Even
Regen Byte Odd
*Not Used on MOD 65
Input
SP In Keys — SP701, SP711 — 8
Output
SP Out Keys — SP561 — 8
SP Advance Key — SP641
SP CPU SAP — SP621
Indicators
SP In Keys — SP571 — 8
SP Out Keys — SP571 — 8
SP Address Check — SP571
SP Key Check — SP571
SP SAP — SP571
SP CPU SP Check — SP571
Storage Protect
(2365 SP)


0
1
2
3
4
P0
5
6
7
8
9
10
11
P1
12
13
14
25
P3
26
27
Fetch
Match Bits
Read Protect
Parity
Not Used
Match
Read Protect
Parity
Not Used
Not Used
First 131K
SPAR X = 0
Second 131K
SPAR X = 1
SP is 64 x 32 in size, but only certain bytes
are used per system requirements.

2365	EVEN	
Lo		Hi
-BITS 0-31 GATE A-		BITS 32-63 GATE D
	ODD	
-BITS 0-31 GATE B		BITS 32-63 GATE E

2365A
Board A2 = Bits 0-15
Board B2 = Bits 16-31
Board A3 = Bits 32-47
Board B3 = Bits 48-63

Cards

BOARD B1			
Bit Number	Bit Number	Z Driver	S. A. & M. D. R.
0	32	K2	J2
2	34	G2	F2
4	36	D2	C2
6	38	L4	K4
PO-7	P32-39	F4	E4
9	41	C4	B4
11	43	L6	K6
13	45	H6	G6
15	47	E6	D6
1	33	H2	J2
3	35	E2	F2
5	37	B2	C2
7	39	J4	K4
8	40	D4	E4
10	42	A4	B4
12	44	J6	K6
14	46	F6	G6
P8-15	P40-47	C6	D6
A2	A3		

BOARD B2			
Bit Number	Bit Number	Z Driver	S. A. & M. D. R.
16	48	K2	J2
18	50	G2	F2
20	52	D2	C2
22	54	L4	K4
P16-23	P48-55	F4	E4
25	57	C4	B4
27	59	L6	K6
29	61	H6	G6
31	63	E6	D6
17	49	H2	J2
19	51	E2	F2
21	53	B2	C2
23	55	J4	K4
24	56	D4	E4
26	58	A4	B4
28	60	J6	K6
30	62	F6	G6
P24-31	P56-63	C6	D6
B2	B3		

Scoping Points

Seg.	Sense Amps Inputs		STROBE (SA and MDR Card)	M. D. R. Output Data Bus	M. D. R. Output To Z Driver
A	J09	J10	D13	D12	B02
B	J04	J05	D13	D12	B02
C	D09	D10	D13	D12	B02
D	D04	D05	D13	D12	B02
A	G09	G10	J02	J13	G02
B	G04	G05	J02	J13	G02
C	B09	B10	J02	J13	G02
D	B04	B05	J02	J13	G02

Z Driver

Input	Timing Pulse	Output
J02	J13	G08
J02	J05	G03
J02	D13	B08
J02	D04	B03

The following items provide a checklist for investigating 2365 problems.

1. Check the 18.0v power supply (PS 16). It must be set for 19.0v for proper sense amp response.

2. Check the array temperature for 95 ± 2°F. Use thermometer PN 5392366.

   NOTE: Some intermittents have been caused by this temperature cycling. This may be checked by making five or six readings at 3-minute intervals.

3. Check all power supply voltages at the test jacks (see installation manual for compensated test jack voltages). If the trouble persists after one pass through this list, testing the voltages on the back-panel pins is recommended.

4. Run a two point shmoo plot. With the Z-voltage setting at nominal, raise the XY drive voltage to failure, and lower it to failure. Compare these failures with the previous shmoo plot.

5. Scope the X and Y drivers and gates. The proper waveshapes are shown in the 2365 maintenance manual.

   Stop machine. Scope all driver outputs (X and Y) for down level. Maximum acceptable down level is less than 2vdc. MM-ALD reference pages may be used for scope points. If the down level of a driver output is +2v or greater, the driver card should be replaced. If the problem still exists, systematically remove the matrix switch cards one at a time. Check driver off level after each switch is removed. When level falls below 2v, that removed switch is defective. The 32 driver outputs can be observed on any matrix switch input.

6. Using the probe adapter tool and the 453 scope with a 220-ohm (approximate) buffer resistor (to slow down the preamplifier input and smooth out some of the noise), perform the following checks: (See Maintenance manual for setup.)

   a. Scope the suspected core signal. Compare it with other output signals.

   b. Check the output signal for proper relationship to the strobe pulse.

      NOTE: A late noise and a late strobe or an early noise and an early strobe can result in picked bits. Also, a late peaking core with a late strobe can result in dropping bits.

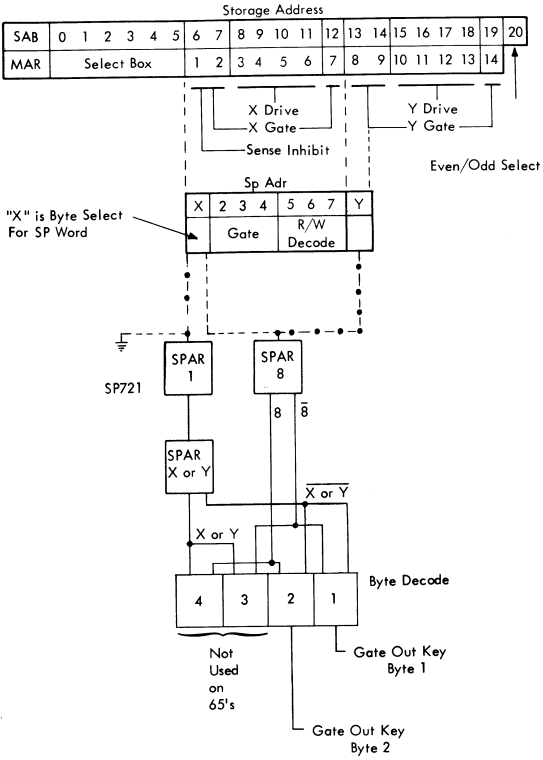
   c. Check for the following grouping of the strobe pulses:

      (1) Group 1 to 2: about 10ns.
      (2) Group 2 to 3: about 10ns to 15ns.
      (3) Group 3 to 4: about 10ns to 15ns.

7. Check for the matrix switch bias current:
   X bias to A2N6B2; then to A2L6B2.
   Y bias to A1N6B2; then to A1L6B2.

   NOTE: The slip-on connector has been found loose several times. A parallel-wire EC is in process.

8. With tweezers, gently pull the blue and white wire on the array at the suspected locations. The wire should come off if the weld is defective. Do not pull with the fingers; you may induce more failures than you find.

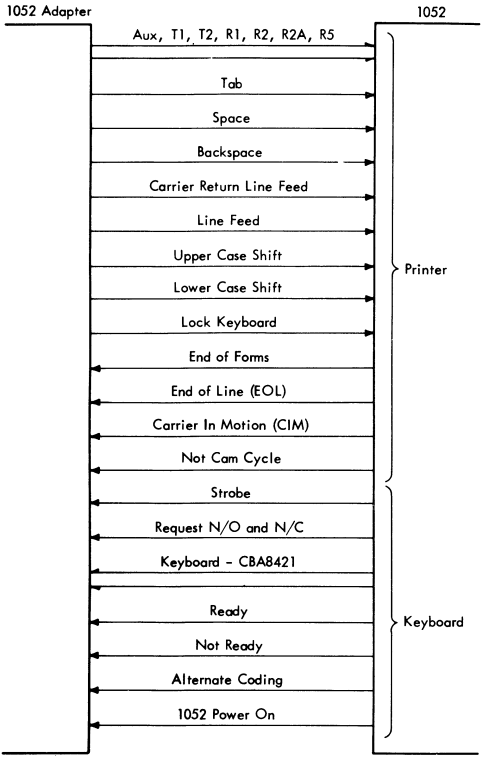


Legend —•— 75 Systems
——— 65 Systems

TO DISABLE S. P. -4

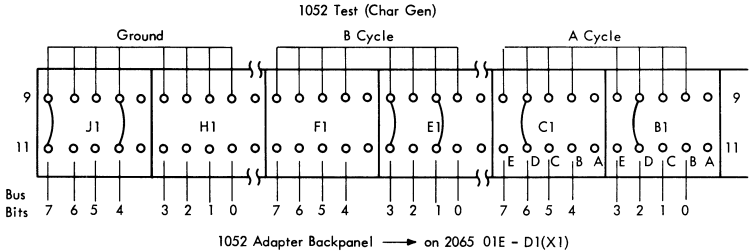
Ground the following pins:

SP	801C	B4	G2	B10	Regen Even
SP	802C	B4	H2	B10	Regen Odd
SP	601C	B4	H5	B10	SP Sel Even
SP	601C	B4	H5	D6	SP Sel Odd
SP	521C	B4	H4	B8	MH $\overline{\text{SAP}}$ Store
SP	521C	B4	H4	D2	M4 $\overline{\text{SAP}}$ Fetch
SP	631C	BM	M4	B3	+ Addr Par. Error



Adapter - Printer Keyboard Interface

2065 1052 Adapter ⟶ 1052 Interface



Layout desired characters in chart form as shown.
(In example "A" cycle will print W and "B" cycle will print M)

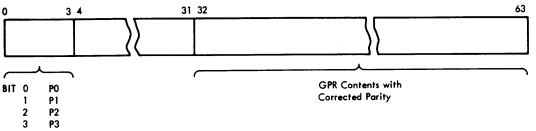
Bus	A Cycl	B Cycl
0	1	1
1	0	1
2	1	0
3	0	1
4	0	0
5	1	1
6	1	0
7	0	0
	"W"	"M"

Desired EBCDIC character and/or 1052 control function goes in this chart for layout purposes.

Then, from chart On Back Panel
If AB = 00 Jumper corresponding bus position to ground
If AB = 01 Jumper corresponding bus position to B Cycle
If AB = 10 Jumper corresponding bus position to A Cycle
If AB = 11 Leave Bus position open

Log Word	Bit		Logic	
Log Word 1 Location 88	02	Prefix enabled	KW	201
	38	CPU No 2		
	39	Storage frame 2 addr. 262K	PK	111
Log Word 2 Location 90	03	Select sent	MC	711
	04	Inhibit osc.	KC	111
Log Word 4 Location A0	25	Program interrupt bit 16	KM	411
Log Word 8 Location C0	08	M.S. timer 1 latch	MC	725
	09	M.S. timer 2 latch	MC	725
	10	System hang	MC	725
	12	Multisystem mode	KW	201
	13	Partition mode	KW	201
	16	CPU No 1		
	17	Storage frame 1 enabled		
	18	Storage frame 1 addr. 1048K	PK	111
	19	Storage frame 1 addr. 524K	PK	111
	20	Storage frame 1 addr. 262K	PK	111
	21	Storage frame 2 enabled		
	22	Storage frame 2 addr. 1048K	PK	111
	23	Storage frame 2 addr. 524K	PK	111
	24	Storage frame 3 enabled		
	25	Storage frame 3 addr. 1048K	PK	111
	26	Storage frame 3 addr. 524K	PK	111
	27	Storage frame 3 addr. 262K	PK	111
	28	Storage frame 4 enabled		
	29	Storage frame 4 addr. 1048K	PK	1111
	30	Storage frame 4 addr. 524K	PK	111
	31	Storage frame 4 addr. 262K	PK	111

GPR LOGOUT FORMAT

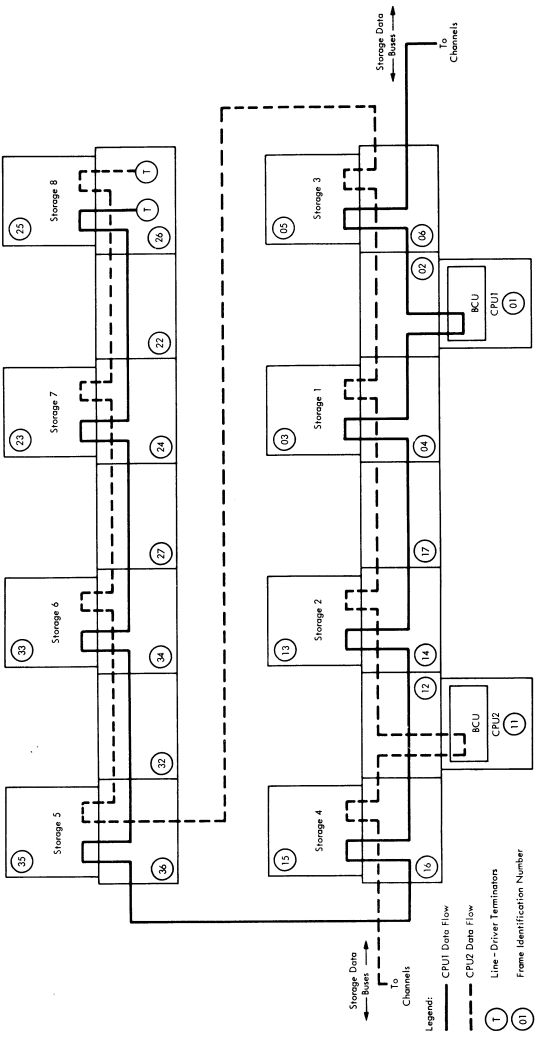


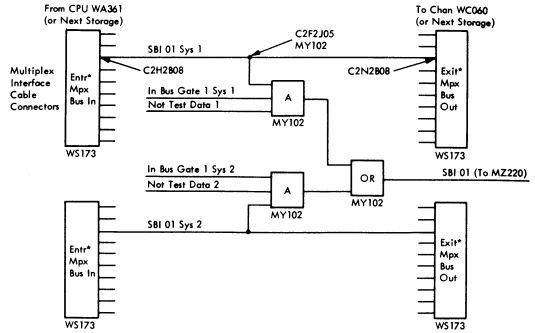
Address	GPR
1F8	15
1F0	14
1F8	13
1E0	12
1D8	11
1D0	10
1C8	09
1C0	08
1B8	07
1B0	06
1A8	05
1A0	04
198	03
190	02
188	01
180	00

Re Lads Page M3061

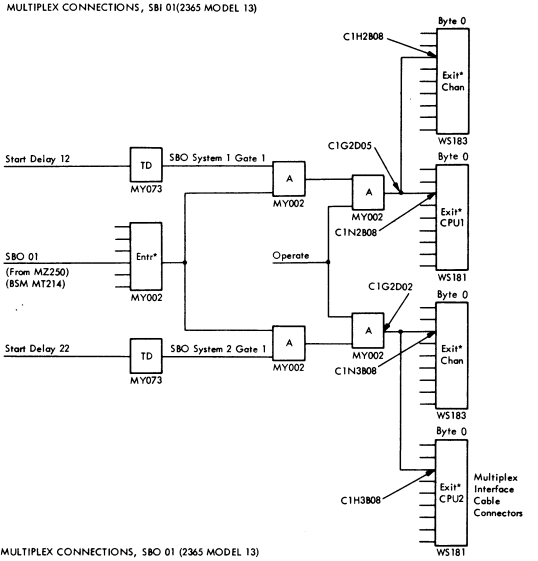
Sending CPU		Receiving CPU	
Action	I_2	Action	Interrupt Code
External Reset (D09)	40	System Reset (B02)	None
External Start (D10)	80	Load a PSW from Location Zero (B03)	None
Log IO Interrupt (D11)	C0	Allow IO interrupts to occur if pending (B04)	None
System Call (D12)	10	External Interrupt if enabled to do so (B05)	10
(D13) Machine Check (Malfunction) (Alert)	None	External Interrupt if enabled to do so (B06)	20

SCOPE POINTS
ON CARD LOCATION 01 E D2 N3
SEE SPECIFIC SIGNAL FOR PIN NO.

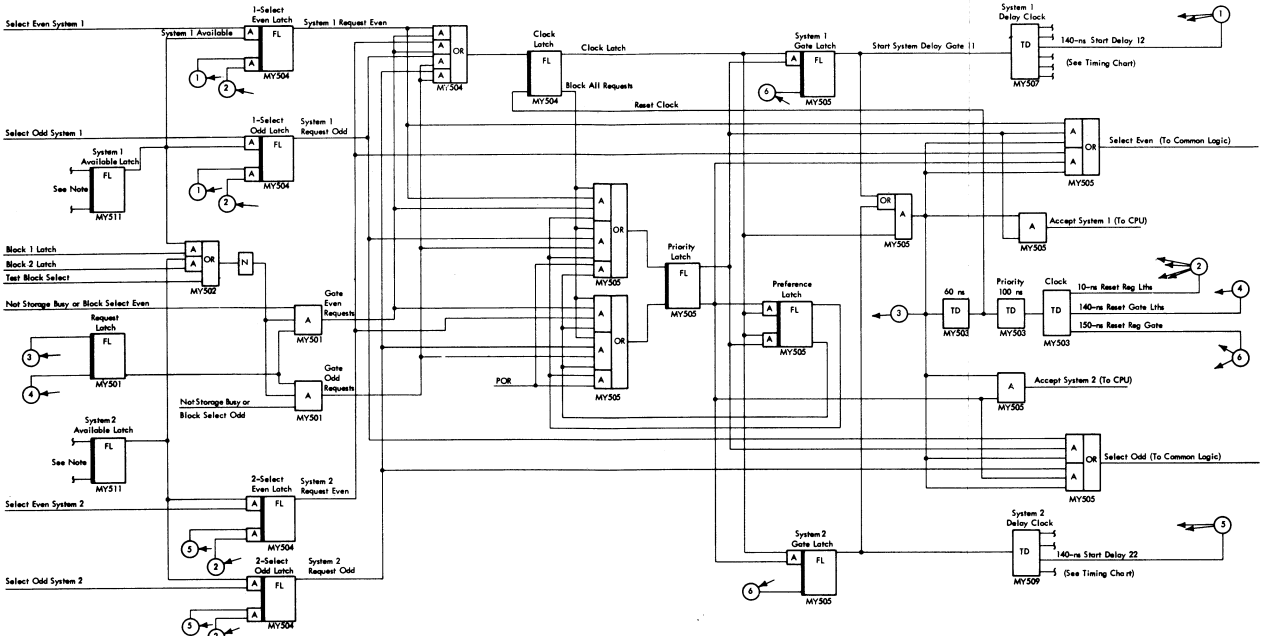

Storage Data Buses
To Channels
Storage 8
Storage 7
Storage 6
Storage 5
Storage 3
Storage 1
Storage 2
Storage 4
BCU
CPU1
BCU
CPU2
Storage Data Buses
To Channels
Legend:
CPU1 Data Flow
CPU2 Data Flow
Line - Driver Terminators
Frame Identification Number



MULTIPLEX CONNECTIONS, SBI 01(2365 MODEL 13)

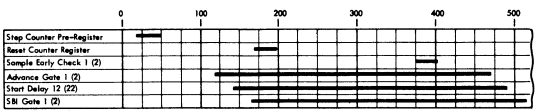


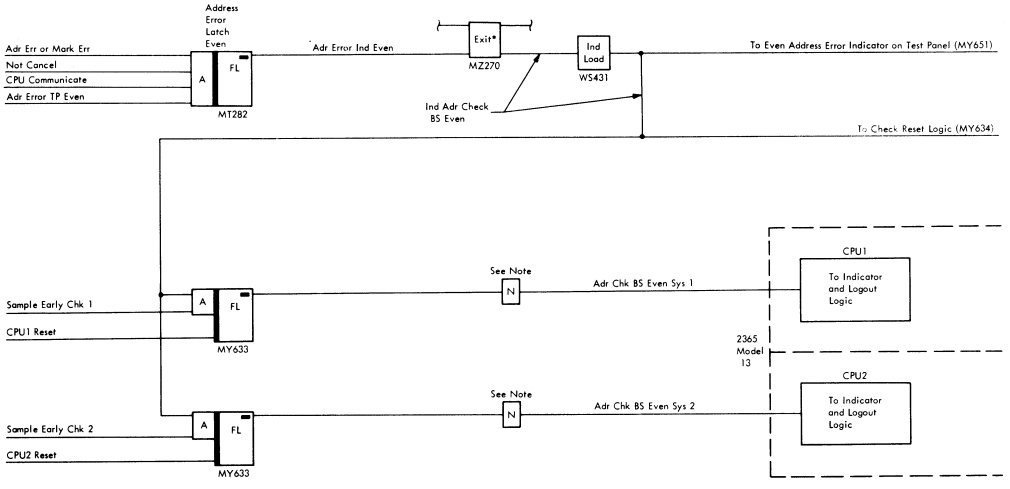
MULTIPLEX CONNECTIONS, SBO 01 (2365 MODEL 13)



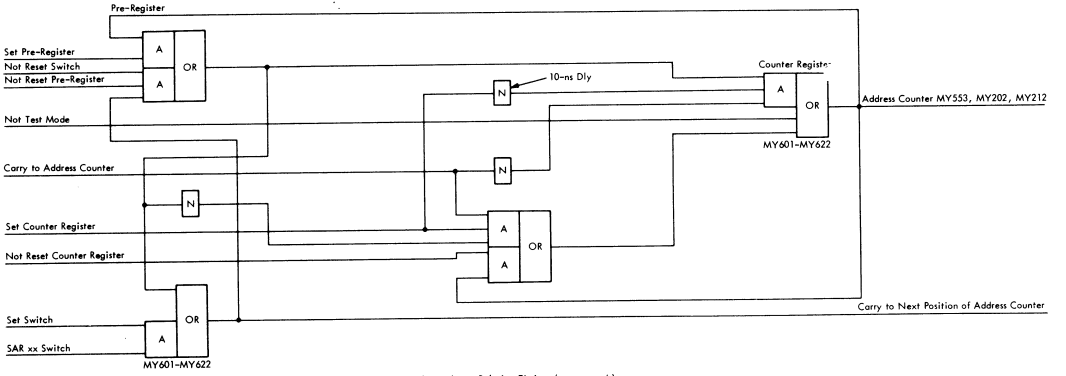
Note: The system available latch is on when system power is on, storage power is on, storage is in operate mode, and the enable-disable switch (on the system configuration control panel) is enabled.

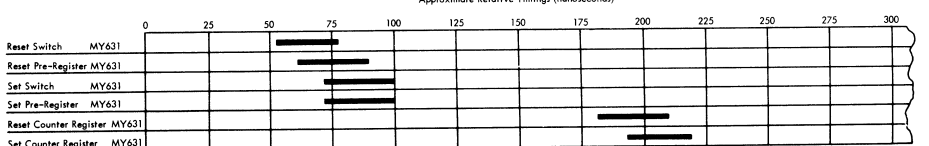
System Delay Clock Pulses (nanoseconds)





Note:
These drivers have +3 volts through isolation relay.


Pre-Register
Set Pre-Register
Not Reset Switch
Not Reset Pre-Register
A
A
OR
Not Test Mode
Carry to Address Counter
N
N
10-ns Dly
N
Set Counter Register
Not Reset Counter Register
A
A
OR
Counter Register
A
OR
MY601-MY622
Address Counter MY553, MY202, MY212
Carry to Next Position of Address Counter
Set Switch
SAR xx Switch
OR
A
MY601-MY622


Approximate Relative Timings (nanoseconds)
0
25
50
75
100
125
150
175
200
225
250
275
300
Reset Switch MY631
Reset Pre-Register MY631
Set Switch MY631
Set Pre-Register MY631
Reset Counter Register MY631
Set Counter Register MY631

CUT ALONG DOTTED LINE

IBM Field Engineering Handbook, System/360 Model 65, Form Y25-0501-2

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Circle one of the comments and explain in the space provided:

Suggested Addition (page _____) Suggested Deletion (page ____) Error (page ___)

Explanation:

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