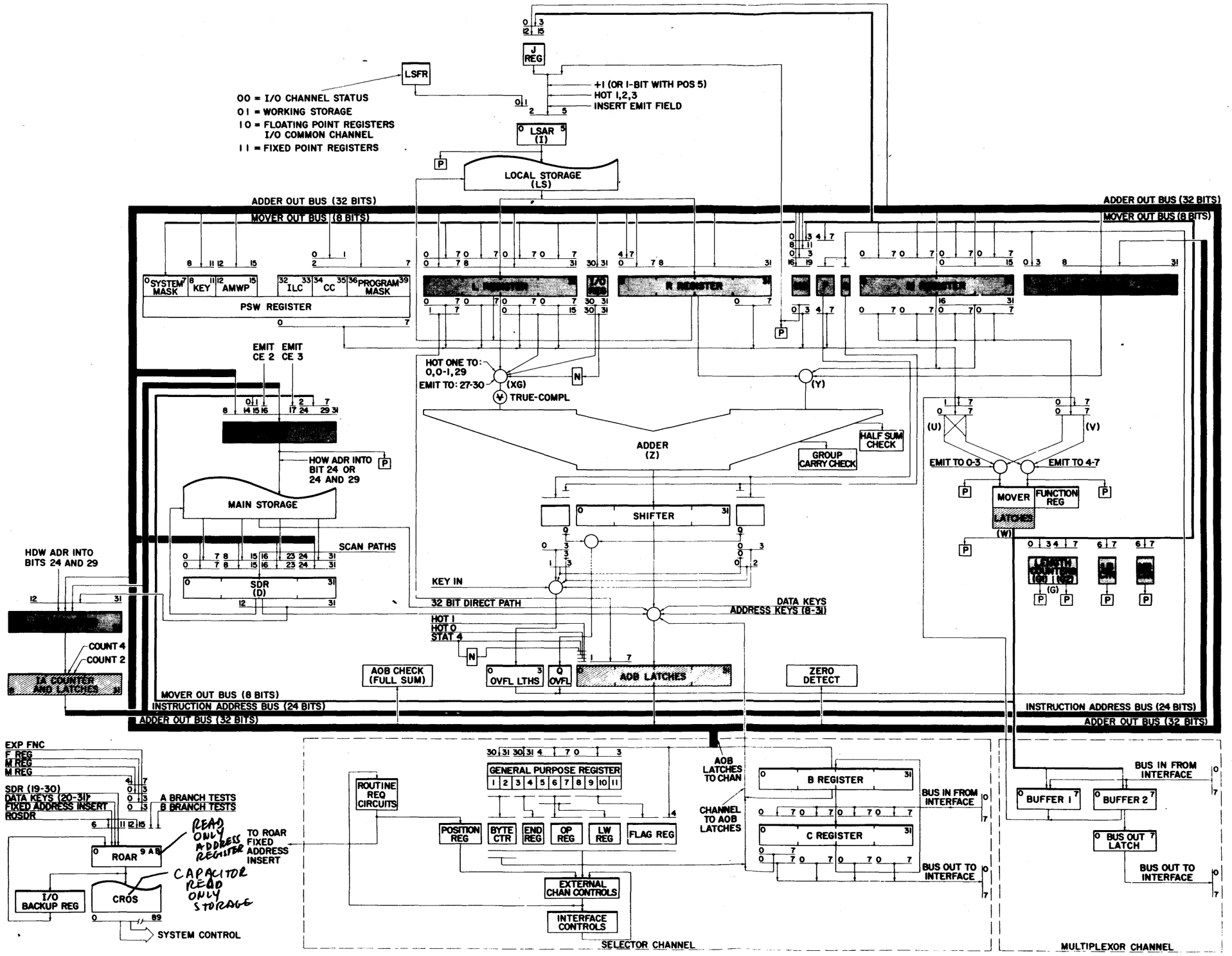
J REG
LSFR
00 = I/O CHANNEL STATUS
01 = WORKING STORAGE
10 = FLOATING POINT REGISTERS I/O COMMON CHANNEL
11 = FIXED POINT REGISTERS
+1 (OR 1-BIT WITH POS 5)
HOT 1,2,3
INSERT EMIT FIELD
LSAR (I)
LOCAL STORAGE (LS)
ADDER OUT BUS (32 BITS)
MOVER OUT BUS (8 BITS)
SYSTEM MASK
KEY
AMWP
ILC
CC
PROGRAM MASK
PSW REGISTER
L REGISTER
I/O
R REGISTER
T REGISTER
EMIT CE 2
EMIT CE 3
HOT ONE TO: 0,0-1,29
EMIT TO: 27-30
(XG)
TRUE-COMPL
(Y)
ADDER (Z)
HALF SUM CHECK
GROUP CARRY CHECK
(U)
(V)
EMIT TO 0-3
EMIT TO 4-7
MOVER FUNCTION REG
MOVER LATCHES
(W)
(G)
HOW ADR INTO BIT 24 OR 24 AND 29
MAIN STORAGE
SCAN PATHS
SDR (D)
HDW ADR INTO BITS 24 AND 29
IA COUNTER AND LATCHES
COUNT 4
COUNT 2
KEY IN
32 BIT DIRECT PATH
DATA KEYS ADDRESS KEYS (8-31)
HOT 1
HOT 0
STAT 4
SHIFTER
AOB CHECK (FULL SUM)
OVFL LTHS
Q OVFL
AOB LATCHES
ZERO DETECT
MOVER OUT BUS (8 BITS)
INSTRUCTION ADDRESS BUS (24 BITS)
ADDER OUT BUS (32 BITS)
EXP FNC
F REG
M REG
M REG
SDR (19-30)
DATA KEYS (20-31)
FIXED ADDRESS INSERT
ROSDR
A BRANCH TESTS
B BRANCH TESTS
ROAR
READ ONLY ADDRESS REGISTER
TO ROAR FIXED ADDRESS INSERT
I/O BACKUP REG
CROS
CAPACITOR READ ONLY STORAGE
SYSTEM CONTROL
ROUTINE REQ CIRCUITS
GENERAL PURPOSE REGISTER
POSITION REG
BYTE CTR
END REG
OP REG
LW REG
FLAG REG
AOB LATCHES TO CHAN
CHANNEL TO AOB LATCHES
B REGISTER
C REGISTER
BUS IN FROM INTERFACE
BUS OUT TO INTERFACE
EXTERNAL CHAN CONTROLS
INTERFACE CONTROLS
SELECTOR CHANNEL
BUFFER 1
BUFFER 2
BUS OUT LATCH
MULTIPLEXOR CHANNEL

LU FIELD ROSDR 1-3 MOVER INPUT - LEFT SIDE

EDGE CHAR	MNEMONIC	BITS	DEC ORDER	FUNCTION	ALD PAGE
		000	LU0	GATE ZEROS TO LEFT MOVER INPUT U.	DS001
B	MD•F→U	001	LU1	GATE MD REG TO LEFT MOVER INPUT U BITS 0-3. GATE F REG TO MOVER INPUT U BITS 4-7.	DS001
B	R3→U	010	LU2	GATE R REG BITS 24-31 TO LEFT MOVER INPUT U.	DS001
B	DCI→U	011	LU3	GATE DIRECT CONTROL DATA IN LINES TO LEFT MOVER INPUT U.	DS001
B	XTR→U	100	LU4	GATE EXTERNAL INTERRUPT REG TO LEFT MOVER INPUT U. RESET EXTERNAL INTERRUPT REG.	DS001
B	PSW4→U	101	LU5	GATE PSW BITS 32-39 (INSTRUCTION LENGTH•CONDITION REG•PROGRAM MASK) TO LEFT MOVER INPUT U.	DS001
B	LMB→U	110	LU6	GATE L REG TO LEFT MOVER INPUT U. BYTE SELECTION CONTROLLED BY M BYTE COUNTER.	DS001
B	LLB→U	111	LU7	GATE L REG TO LEFT MOVER INPUT U. BYTE SELECTION CONTROLLED BY L BYTE COUNTER.	DS001

MV FIELD ROSDR 4-5 MOVER INPUT - RIGHT SIDE

EDGE CHAR	MNEMONIC	BITS	DEC ORDER	FUNCTION	ALD PAGE
		00	MV0	GATE ZEROS TO RIGHT MOVER INPUT V.	DS021
B	MLB→V	01	MV1	GATE M REG TO RIGHT MOVER INPUT V. BYTE SELECTION CONTROLLED BY L BYTE COUNTER.	DS021
B	MMB→V	10	MV2	GATE M REG TO RIGHT MOVER INPUT V. BYTE SELECTION CONTROLLED BY M BYTE COUNTER.	DS021
		11	MV3	UNDEFINED	

ZP FIELD ROSDR 6-11 ROS ADDRESS BITS 0-5

THIS FIELD IS GATED DIRECTLY TO FORM BITS 0-5 OF THE NEXT ROS ADDRESS.

ZF FIELD ROSDR 12-15 FUNCTION BRANCH CONTROL OR ROS ADDRESS BITS 6-9

IF THE ZN FIELD IS NON-ZERO, THIS FIELD IS GATED DIRECTLY TO FORM BITS 6-9 OF THE NEXT ROS ADDRESS.
IF THE ZN FIELD IS ZERO, THIS FIELD IS DECODED AS SHOWN BELOW.

EDGE CHAR	MNEMONIC	BITS	DEC ORDER	FUNCTION	ALD PAGE
		0000	ZF0	UNDEFINED	
R	D→ROAR•SCAN	0010	ZF2	GATE STORAGE DATA REG BITS FOLLOWS: BITS 19-30 TO ROS ADDRESS BITS 1-3 TO SCAN CLOCK ADVANCE COUNTER BIT 4 TO SUPERVISORY ENABLE STORAGE STAT BIT 5 TO PROGRESSIVE SCAN STAT BIT 6 TO SUPERVISORY STAT BIT 7 TO I/O MODE STAT	KK002
		0100	ZF4	UNDEFINED	
R	M(03)→ROAR	0110	ZF6	GATE M REG BITS 0-3 TO NEXT ROS ADDRESS BITS 6-9.	KK002
R	M(47)→ROAR	1000	ZF8	GATE M REG BITS 4-7 TO NEXT ROS ADDRESS BITS 6-9.	KK002
R	F→ROAR	1010	ZF10	GATE F REG TO NEXT ROS ADDRESS BITS 6-9.	KK002
R	ED→ROAR	1100	ZF12	GATE EXPONENT DIFFERENCE REG TO NEXT ROS ADDRESS BITS 6-9.	KK002
R	RETURN→ROAR	1110	ZF14	GATE ROS ADDRESS BUFFER REG TO NEXT ROS ADDRESS. THIS REGISTER IS SET ON I/O BREAK-IN.	KK002

ZN FIELD ROSDR 16-18 ROS ADDRESS CONTROL (NULL VALUE: ZN4)

EDGE CHAR	MNEMONIC	BITS	DEC ORDER	FUNCTION	ALD PAGE
		000	ZN0	DECODE ZF FIELD	
S	SMIF	001	ZN1	SUPPRESS INITIATION OF MAIN STORAGE CYCLE BY DECIMAL ORDER IV7 IN THIS MICROINSTRUCTION IF REFETCH STAT IS OFF AND IAR BIT 30 IS 1. (NEXT INSTRUCTION IS OFF WORD BOUNDARY.)	KK003
R	AQ(B=0)→A	010	ZN2	FORCE A BIT TO 1 IF B BIT IS 0.	KK003
R	AQ(B=1)→A	011	ZN3	FORCE A BIT TO 1 IF B BIT IS 1.	KK003
		100	ZN4	NORMAL ROS ADDRESSING.	
R	FNTRAP	101	ZN5	FORCE ROS ADDRESS TO INVALID OP TRAP VALUE IF THIS MICROINSTRUCTION WAS REACHED BY A FUNCTION BRANCH.	KK003
R	BQ(A=0)→B	110	ZN6	FORCE B BIT TO 1 IF A BIT IS 0.	KK003
R	BQ(A=1)→B	111	ZN7	FORCE B BIT TO 1 IF A BIT IS 1.	KK003

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TEMPLATE FOR 'A' LINE STATEMENT: RRR↓LLL→TTTT

TEMPLATE FOR 'D' LINE STATEMENT: AAAA→TTTT

WHERE: R = RY FIELD L = LX FIELD T = TR FIELD
I = TC FIELD A = AL FIELD

TR FIELD ROSDR 19-23 ADDER LATCH DESTINATION

EDGE CHAR	MNEMONIC	BITS	DEC ORDER	FUNCTION	ALD PAGE
A	Z			DUMMY, USED IN 'A' LINE STATEMENT WHEN THERE IS ALSO A 'D' LINE STATEMENT.	
		00000	TR0	NO GATING FROM ADDER LATCH TO REGISTERS.	
A,D	T	00000	TR0	NO GATING FROM ADDER LATCH TO REGISTERS. USED WHEN OTHER TERMS OF STATEMENT ARE PRESENT.	
A,D	R	00001	TR1	GATE ADDER LATCH TO R REG.	DR121
A,D	RO	00010	TR2	GATE ADDER LATCH BITS 0-7 TO R REG BITS 0-7.	DR121
A,D	M	00011	TR3	GATE ADDER LATCH TO M REG.	DR121
A,D	D	00100	TR4	GATE ADDER LATCH TO SDR.	DR111
A,D	LO	00101	TR5	GATE ADDER LATCH BITS 0-7 TO L REG BITS 0-7.	DR111
A,D	R,A	00110	TR6	GATE ADDER LATCH TO R REG AND SAR. INITIATE STORAGE REQUEST.	DR111
A,D	L	00111	TR7	GATE ADDER LATCH TO L REG.	DR111
S	HA→A	01000	TR8	GATE HARDWARE-GENERATED ADDRESS TO SAR. INITIATE STORAGE REQUEST. DECODE EMIT FIELD TO DETERMINE STORAGE FUNCTION.	DR121

EMIT VALUE	FUNCTION
X000	WRITE IN MAIN STORAGE ADDRESS 80.
X001	READ FROM MAIN STORAGE ADDRESS 80.
X010	OR FROM MAIN STORAGE ADDRESS 80.
X011	UNDEFINED
X100	WRITE IN MAIN STORAGE ADDRESS 84, SET IAR TO 84.
X101	READ FROM MAIN STORAGE ADDRESS 84, SET IAR TO 84.
X110	UNDEFINED
X111	UNDEFINED

A,D	R,AN	01001	TR9	GATE ADDER LATCH TO R REG AND SAR. INITIATE STORAGE REQUEST. SUPPRESS INVALID ADDRESS TRAP, SET INVALID ADDRESS STAT INSTEAD.	DR121
A,D	R,AW	01010	TR10	GATE ADDER LATCH TO R REG AND SAR. INITIATE STORAGE REQUEST. TRAP IF ADDRESS NOT ON WORD BOUNDRY.	DR121
A,D	R,AD	01011	TR11	GATE ADDER LATCH TO R REG AND SAR. INITIATE STORAGE REQUEST TRAP IF ADDRESS NOT ON DOUBLE WORD BOUNDARY.	DR121
D*	D→IAR	01100	TR12	GATE SDR TO IAR. INTERLOCK WITH STORAGE TIMING RING.	DR121
D*	SCAN→D	01101	TR13	GATE SCAN BUS TO SDR IN FOLLOWING ARRANGEMENT: PARITY OF BYTE 0 TO BIT 0. BITS 0-7 TO BITS 1-8. PARITY OF BYTE 1 TO BIT 9. BITS 8-15 TO BITS 10-17. PARITY OF BYTE 2 TO BIT 18. BITS 16-23 TO BITS 19-26. PARITY OF BYTE 3 TO BIT 27. BITS 24-27 TO BITS 28-31. GOOD PARITY IS INSERTED IN SDR.	DR121
A,D	R13	01110	TR14	GATE ADDER LATCH BITS 8-31 TO R REG BITS 8-31.	DR121
A,D	A	01111	TR15	GATE ADDER LATCH BITS 8-31 TO SAR. INITIATE STORAGE REQUEST.	DR131
A,D	L,A	10000	TR16	GATE ADDER LATCH TO L REG AND SAR. INITIATE STORAGE REQUEST.	DR131
A,D	R,D	10001	TR17	GATE ADDER LATCH TO R REG AND SDR .	DR121
		10010	TR18	UNDEFINED	
A,D	R,IO	10011	TR19	GATE ADDER LATCH TO R REG. GATE ADDER LATCH BITS 30-31 TO I/O REG.	DR131

* NOT PART OF A STATEMENT

TR FIELD (CONTINUED)

EDGE CHAR	MNEMONIC	BITS	DEC ORDER	FUNCTION	ALD PAGE
A,D	H	10100	TR20	GATE ADDER LATCH TO H REG.	DR141
A,D	IA	10101	TR81	GATE ADDER LATCH BITS 8-31 TO IAR.	DR141
A,D	FOLD	10110	TR22	GATE SCAN BUS BITS 28-31 TO SDR BITS 28-31. GATE ZEROS TO SDR BITS 0-27. GOOD PARITY IS INSERTED IN SDR.	DR141
		10111	TR23	UNDEFINED	
A,D	L,M	11000	TR24	GATE ADDER LATCH TO L REG AND M REG.	DR111
A,D	ML,JK	11001	TR25	GATE ADDER LATCH TO L REG AND M REG. GATE LATCH BITS 12-15 TO J REG. GATE LATCH BITS 16-19 TO MD COUNTER. TURN OFF REFETCH STAT. IF LATCH BITS 12-15 ALL ZERO, TURN OFF STAT 0. OTHERWISE TURN OFF STAT 0. IF LATCH BITS 16-19 ALL ZERO, TURN ON STAT 1. OTHERWISE TURN OFF STAT 1. IF LATCH BITS 16-17 ALL ZERO, TURN ON ONE-SYLLABLE STAT. OTHERWISE TURN OFF ONE-SYLLABLE STAT. IF LATCH BITS 0-1 EQUAL 00, SET ILC TO 01. IF LATCH BITS 0-1 EQUAL 01 OR 10, SET ILC TO 10. IF LATCH BITS 0-1 EQUAL 11, SET ILC TO 11.	DR111
A,D	MH,L	11010	TR26	GATE ADDER LATCH TO L REG. GATE ADDER LATCH BITS 0-15 TO M REG BITS 16-31. GATE ADDER LATCH BITS 0-3 TO MD COUNTER.	DR111
A,D	MD	11011	TR27	GATE ADDER LATCH BITS 8-11 TO MD COUNTER.	DR111
A,D	M,SP	11100	TR28	GATE ADDER LATCH TO M REG. GATE ADDER LATCH BITS 8-11 TO STORAGE PROTECTION KEY (PSW BITS 8-11).	DR111
A,D	D*BS	11101	TR29	GATE ADDER LATCH TO SDR UNDER CONTROL OF CPU BYTE STATS.	DR111
A,D	L13	11110	TR30	GATE ADDER LATCH BITS 8-31 TO L REG BITS 8-31.	DR111
A,D	J	11111	TR31	GATE ADDER LATCH BITS 12-15 TO J REG.	DR111

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WS FIELD ROSDR 25-27 LOCAL STORAGE ADDRESSING (NULL VALUE: WS4)

EDGE CHAR	MNEMONIC	BITS	DEC ORDER	FUNCTION	ALD PAGE
		000	WS0	UNDEFINED	
L	WS1→LSA	001	WS1	SET LSAR TO 010001 TO ADDRESS WORD 1 OF WORKING STORAGE	KL0XX
L	WS2→LSA	010	WS2	SET LSAR TO 010010 TO ADDRESS WORD 2 OF WORKING STORAGE.	KL0XX
L	WS•E→LSA	011	WS3	SET LSAR BITS 0-1 TO 01, SET LSAR BITS 2-5 TO EMIT FIELD VALUE TO ADDRESS WORKING STORAGE PER THE EMIT FIELD.	KL0XX
L	FN•J→LSA	100	WS4	GATE LOCAL STORAGE FUNCTION REG TO LSAR BITS 0-1. GATE J REG TO LSAR BITS 2-5.	KL0XX
L	FN•JQ1→LSA	101	WS5	GATE LOCAL STORAGE FUNCTION REG TO LSAR BITS 0-1. GATE J REG TO LSAR BITS 2-5. OR A ONE INTO LSAR BIT 5.	KL031
L	FN•MD→LSA	110	WS6	GATE LOCAL STORAGE FUNCTION REG TO LSAR BITS 0-1. GATE MD REG TO LSAR BITS 2-5.	KL0XX
L	FN•MDQ1→LSA	111	WS7	GATE LOCAL STORAGE FUNCTION REG TO LSAR BITS 0-1. GATE MD REG TO LSAR BITS 2-5. OR A ONE INTO LSAR BIT 5.	KL031

SF FIELD ROSDR 28-30 LOCAL STORAGE FUNCTION (NULL VALUE: SF7)

EDGE CHAR	MNEMONIC	BITS	DEC ORDER	FUNCTION	ALD PAGE
L	R→LS	000	SF0	WRITE INTO LOCAL STORAGE FROM R REG.	KL0XX
L	LS→L•R→LS	001	SF1	READ LOCAL STORAGE INTO L REG, WRITE INTO LOCAL STORAGE FROM R REG.	KL0XX
L	LS→R→LS	010	SF2	READ LOCAL STORAGE INTO R REG, REGENERATE FROM R REG.	KL0XX
		011	SF3	UNDEFINED	
L	L→LS	100	SF4	WRITE INTO LOCAL STORAGE FROM L REG.	KL0XX
L	LS→R•L→LS	101	SF5	READ LOCAL STORAGE INTO R REG, WRITE INTO LOCAL STORAGE FROM L REG.	KL0XX
L	LS→L→LS	110	SF6	READ LOCAL STORAGE INTO L REG, REGENERATE FROM L REG.	KL0XX
		111	SF7	NO OPERATION.	

IV FIELD ROSDR 32-34 INVALID DIGIT TEST AND INSTRUCTION ADDRESS REG CONTROL

EDGE CHAR	MNEMONIC	BITS	DEC ORDER	FUNCTION	ALD PAGE
		000	IV0	NO OPERATION	
C	WL→IVD	001	IV1	TRAP IF VALUE OF MOVER OUTPUT BITS 0-3 IS GREATER THAN 9.	KP011
C	WR→IVD	010	IV2	TRAP IF VALUE OF MOVER OUTPUT BITS 4-7 IS GREATER THAN 9.	KP011
C	W→IVD	011	IV3	TRAP IF VALUE OF EITHER MOVER OUTPUT BITS 0-3 OR MOVER OUTPUT BITS 4-7 IS GREATER THAN 9.	KP011
S	IA+4→A,IA	100	IV4	INCREMENT IAR BY 4. GATE RESULT TO IAR AND SAR. INITIATE STORAGE REQUEST. INHIBIT INVALID ADDRESS TRAP, SET INVALID ADDRESS STAT INSTEAD.	KP012
C	IA+2/4	101	IV5	IF INSTRUCTION LENGTH CODE VALUE IS 0 OR 1, INCREMENT IAR BY 2. IF ILC VALUE IS 2 OR 3, INCREMENT IAR BY 4. GATE RESULT BACK TO IAR.	KP012
C	IA+2	110	IV6	INCREMENT IAR BY 2. GATE RESULT BACK TO IAR.	KP012
S	IA+0/2→A	111	IV7	GATE IAR TO SAR, INCREMENTED BY 2 IF REFETCH STAT IS OFF, NOT INCREMENTED IF REFETCH STAT IS ON. INITIATE STORAGE REQUEST. INHIBIT INVALID ADDRESS TRAP, SET INVALID ADDRESS STAT INSTEAD. IAR IS NOT ALTERED.	KP012

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TEMPLATE FOR 'D' LINE STATEMENT: AAAA→TTTT
WHERE: A = AL FIELD T = TR FIELD

'A' bits, at just field

AL FIELD ROSDR 35-39 SHIFT CONTROL AND GATING INTO ADDER LATCH

EDGE CHAR	MNEMONIC	BITS	DEC ORDER	FUNCTION	ALD PAGE
		00000	AL0	GATE ADDER OUTPUT TO LATCH, NO SHIFT.	
A	Q→SR1→F	00001	AL1	GATE ADDER OUTPUT TO LATCH, SHIFTED RIGHT 1, ENTERING Q. SPILL BIT ENTERS F, WHICH IS SHIFTED RIGHT.	DR071
A	LO,¬S4→	00010	AL2	GATE ADDER OUTPUT BITS 8-31 TO LATCH BITS 8-31. GATE L REG BITS 1-7 TO LATCH BITS 1-7. SET LATCH BIT 0 TO THE COMPLEMENT OF STAT 4.	DR061
A	+SGN→	00011	AL3	GATE ADDER OUTPUT BITS 1-31 TO LATCH BITS 1-31. SET LATCH BIT 0 TO ZERO.	DR061
A	−SGN→	00100	AL4	GATE ADDER OUTPUT BITS 1-31 TO LATCH BITS 1-31. SET LATCH BIT 0 TO ONE.	DR061
A	LO,S4→	00101	AL5	GATE ADDER OUTPUT BITS 8-31 TO LATCH BITS 8-31. GATE L REG BITS 1-7 TO LATCH BITS 1-7. GATE STAT 4 TO LATCH BIT 0.	DR061
D*	IA→H	00110	AL6	GATE ADDER OUTPUT TO LATCH, NO SHIFT. GATE IAR TO H REG BITS 8-31. H REG BITS 0-7 REMAIN UNCHANGED.	DR081
A	Q→SL→−F	00111	AL7	GATE ADDER OUTPUT TO LATCH, SHIFTED LEFT 1, ENTERING Q. COMPLEMENT OF SPILL BIT ENTERS F, WHICH IS SHIFTED LEFT.	DR081
A	Q→SL1→F	01000	AL8	GATE ADDER OUTPUT TO LATCH, SHIFTED LEFT 1, ENTERING Q. SPILL BIT ENTERS F, WHICH IS SHIFTED LEFT.	DR081
A	F→SL1→F	01001	AL9	GATE ADDER OUTPUT TO LATCH, SHIFTED LEFT 1, ENTERING BIT 0 OF F. SPILL BIT ENTERS F, WHICH IS SHIFTED LEFT.	DR081
A	SL1→Q	01010	AL10	GATE ADDER OUTPUT TO LATCH, SHIFTED LEFT 1, ENTERING ZERO. SPILL BIT ENTERS Q.	DR071
A	Q→SL1	01011	AL11	GATE ADDER OUTPUT TO LATCH, SHIFTED LEFT 1, ENTERING Q. SPILL BIT IS DISCARDED.	DR081
A	SR1→F	01100	AL12	GATE ADDER OUTPUT TO LATCH, SHIFTED RIGHT 1, ENTERING ZERO. SPILL BIT ENTERS F, WHICH IS SHIFTED RIGHT.	DR071
A	SR1→Q	01101	AL13	GATE ADDER OUTPUT TO LATCH, SHIFTED RIGHT 1, ENTERING ZERO. SPILL BIT ENTERS Q.	DR071
A	Q→SR1→Q	01110	AL14	GATE ADDER OUTPUT TO LATCH, SHIFTED RIGHT 1, ENTERING Q. SPILL BIT ENTERS Q.	DR071
A	F→SL1→Q	01111	AL15	GATE ADDER OUTPUT TO LATCH, SHIFTED LEFT 1, ENTERING BIT 0 OF F. SPILL BIT ENTERS Q. F IS SHIFTED LEFT 1, ENTERING ZERO.	DR051
A	SL4→F	10000	AL16	GATE ADDER OUTPUT TO LATCH, SHIFTED LEFT 4, ENTERING ZEROS. SPILL BITS ENTER F.	DROXX
A	F→SL4→F	10001	AL17	GATE ADDER OUTPUT TO LATCH, SHIFTED LEFT 4, ENTERING F. SPILL BITS ENTER F.	DR081
A	FPSL4	10010	AL18	GATE ADDER OUTPUT BITS 0-7 TO LATCH 0-7. GATE ADDER OUTPUT BITS 8-31 TO LATCH BITS 8-31, SHIFTED LEFT 4, ENTERING ZEROS. SPILL BITS FROM ADDER OUTPUT 8-11 ARE DISCARDED.	DR081
A	F→FPSL4	10011	AL19	GATE ADDER OUTPUT BITS 0-7 TO LATCH BITS 0-7. GATE ADDER OUTPUT BITS 8-31 TO LATCH BITS 8-31, SHIFTED LEFT 4, ENTERING F. SPILL BITS FROM ADDER OUTPUT 8-11 ARE DISCARDED.	DR081

AL FIELD (CONTINUED)

EDGE CHAR	MNEMONIC	BITS	DEC ORDER	FUNCTION	ALD PAGE
A	SR4→F	10100	AL20	GATE ADDER OUTPUT TO LATCH, SHIFTED RIGHT 4, ENTERING ZEROS. SPILL BITS ENTER F.	DROXX
A	F→SR4→F	10101	AL21	GATE ADDER OUTPUT TO LATCH, SHIFTED RIGHT 4, ENTERING F. SPILL BITS ENTER F.	DROXX
A	FPSR4→F	10110	AL22	GATE ADDER OUTPUT BITS 8-31 TO LATCH BITS 8-31, SHIFTED RIGHT 4, ENTERING ZEROS. GATE ZEROS TO LATCH BITS 0-7. SPILL BITS ENTER F.	DROXX
A	1→FPSR4→F	10111	AL23	GATE ADDER OUTPUT BITS 0-7 TO LATCH BITS 0-7. GATE ADDER OUTPUT BITS 8-31 TO LATCH BITS 8-31, SHIFTED RIGHT 4, ENTERING 0001. SPILL BITS ENTER F. A HOT CARRY IS FORCED INTO POSITION 7 OF THE ADDER. (THIS ORDER CAN BE USED ONLY WITH AN AD FIELD VALUE OF AD6.)	DR081
A	SR4→H	11000	AL24	GATE ADDER OUTPUT TO LATCH, SHIFTED RIGHT 4, ENTERING ZEROS. SPILL BITS ENTER H REG BITS 0-3. GATE LATCH BITS 4-7 TO R REG BITS 0-3. (THIS ORDER CAN BE USED ONLY WITH A TR FIELD VALUE OF TR1, AND LATCH BITS 4-7 MUST HAVE AN EVEN NUMBER OF ONES.)	DR052
A	F→SR4	11001	AL25	GATE ADDER OUTPUT TO LATCH, SHIFTED RIGHT 4, ENTERING F. SPILL BITS ARE DISCARDED. F IS NOT ALTERED.	DR052
A	E→FPSL4	11010	AL26	GATE ADDER OUTPUT BITS 0-7 TO LATCH BITS 0-7. GATE ADDER OUTPUT BITS 8-31 TO LATCH BITS 8-31, SHIFTED LEFT 4, ENTERING THE EMIT FIELD. SPILL BITS FROM ADDER OUTPUT 8-11 ARE DISCARDED.	DR041
A	F→SR1→Q	11011	AL27	GATE ADDER OUTPUT TO LATCH, SHIFTED RIGHT 1, ENTERING BIT 3 OF F. SPILL BIT ENTERS Q. F IS NOT CHANGED.	DR051
D	DKEY	11100	AL28	GATE DATA KEYS TO LATCH. GATE BITS 28-31 OF DATA KEYS TO F.	DR062
D	CH	11101	AL29	GATE BUS FROM SELECTOR CHANNELS TO LATCH.	DR061
D	D	11110	AL30	GATE STORAGE DATA REG TO LATCH. INTERLOCK WITH STORAGE TIMING RING TO CAUSE POSSIBLE STORAGE HOLDOFF.	DT041
D	AKEY	11111	AL31	GATE ADDRESS KEYS TO LATCH BITS 8-31. GATE ZEROS TO LATCH BITS 0-7.	DR062

* NOT PART OF A STATEMENT.

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WM FIELD ROSDR 40-43 MOVER OUTPUT DESTINATION

EDGE CHAR	MNEMONIC	BITS	DEC ORDER	FUNCTION	ALD PAGE
		0000	WM0	NO OPERATION	DS201
B	W→MMB	0001	WM1	GATE MOVER LATCHES TO BYTE OF M REG SPECIFIED BY M BYTE COUNTER.	DS201
B	W67→MB	0010	WM2	GATE MOVER LATCH BITS 6-7 TO M BYTE COUNTER.	DS201
B	W67→LB	0011	WM3	GATE MOVER LATCH BITS 6-7 TO L BYTE COUNTER.	DS201
B	W27→PSW4	0100	WM4	GATE MOVER LATCH BITS 2-7 TO PSW REGISTER BITS 34-39 (CONDITION CODE AND PROGRAM MASK).	DS201
B	W→PSW0	0101	WM5	GATE MOVER LATCH TO PSW REGISTER BITS 0-7 (SYSTEM MASK).	DS201
B	WL→J	0110	WM6	GATE MOVER LATCH BITS 0-3 TO J REG.	DS201
B	W→CHCTL	0111	WM7	GATE MOVER LATCH TO CHANNEL CONTROL.	DS201
B	W,E→A(BUMP)	1000	WM8	GATE MOVER LATCH BITS 0-1 TO SAR BITS 14-15. GATE MOVER LATCH BITS 2-7 TO SAR BITS 24-29. GATE EMIT FIELD BITS 2-3 TO SAR BITS 16-17. INITIATE BUMP STORAGE REQUEST.	DS201
B	WL→G1	1001	WM9	GATE MOVER LATCH BITS 0-3 TO LENGTH COUNTER G1. RESET G1 SIGN.	DS201
B	WR→G2	1010	WM10	GATE MOVER LATCH BITS 4-7 TO LENGTH COUNTER G2. RESET G2 SIGN.	DS201
B	W→G	1011	WM11	GATE MOVER LATCH TO COMBINED LENGTH COUNTER G. RESET G1,G2 SIGNS.	DS201
B	W→MMB(E?)	1100	WM12	GATE MOVER LATCH TO BYTE OF M REG SPECIFIED BY M BYTE COUNTER. IN CONJUNCTION WITH ORDERS ULO AND/OR URO AND VALUE OF 1 FOR BIT 12 OF PSW (ASCII BIT), THE EMIT FIELD IS MODIFIED IN THE MOVER AS FOLLOWS, WHERE 0,1,2,3 ARE EMIT FIELD BITS AND 0',1',2',3' ARE VALUES USED IN MOVER: 0' = ¬0 Λ ¬2 1' = 2 Λ ¬1 2' = ¬2 3' = 3	DS201
B	WL→MD	1101	WM13	GATE MOVER LATCH BITS 0-3 TO MD COUNTER.	DS201
B	WR→F	1110	WM14	GATE MOVER LATCH BITS 4-7 TO F REG.	DS201
B	W→MD,F	1111	WM15	GATE MOVER LATCH BITS 0-3 TO MD COUNTER. GATE MOVER LATCH BITS 4-7 TO F REG.	DS201

TEMPLATE FOR 'D' LINE STATEMENT: UPLB,MB,MD
OR: LB,MB,MDUP

WHERE: UP = UP FIELD MB = MB FIELD
LB = LB FIELD MD = MD FIELD
ANY COMBINATION OF LB,MB AND MD MAY BE PRESENT.

UP FIELD ROSDR 44-45 LB,MB,MD COUNTER FUNCTION CONTROL (NULL VALUE: UP2)

EDGE CHAR	MNEMONIC	BITS	DEC ORDER	FUNCTION	ALD PAGE
D	0→	00	UP0	SET SELECTED COUNTERS TO ZERO.	DS311
D	3→	01	UP1	SET SELECTED COUNTERS TO THREE.	DS311
D	−1	10	UP2	DECREMENT SELECTED COUNTERS BY ONE. IF UNDERFLOW, SET TO ALL ONES.	DS311
D	+1	11	UP3	INCREMENT SELECTED COUNTERS BY ONE. IF OVERFLOW, SET TO ALL ZEROS.	DS311

MD FIELD ROSDR 46 MD COUNTER CONTROL

EDGE CHAR	MNEMONIC	BITS	DEC ORDER	FUNCTION	ALD PAGE
		0	MD0	NO OPERATION	
D	MD	1	MD1	SELECT MD COUNTER FOR OPERATION SPECIFIED BY UP FIELD.	DS311

LB FIELD ROSDR 47 LB COUNTER CONTROL

EDGE CHAR	MNEMONIC	BITS	DEC ORDER	FUNCTION	ALD PAGE
		0	LB0	NO OPERATION	
D	LB	1	LB1	SELECT LB COUNTER FOR OPERATION SPECIFIED BY UP FIELD.	DS311

MB FIELD ROSDR 48 MB COUNTER CONTROL

EDGE CHAR	MNEMONIC	BITS	DEC ORDER	FUNCTION	ALD PAGE
		0	MB0	NO OPERATION	
D	MB	1	MB1	SELECT MB COUNTER FOR OPERATION SPECIFIED BY UP FIELD.	DS311

DG FIELD ROSDR 49-51 LENGTH COUNTER AND CARRY INSERTION CONTROL

EDGE CHAR	MNEMONIC	BITS	DEC ORDER	FUNCTION	ALD PAGE
		000	DG0	NO OPERATION	
D	CSTAT→ADDER	001	DG1	INSERT CARRY STAT INTO ADDER.	DS301
D	HOT1→ADDER	010	DG2	INSERT HOT CARRY INTO ADDER.	DS301
D	G1−1	011	DG3	DECREMENT LENGTH COUNTER G1 BY ONE. IF UNDERFLOW, SET G1 SIGN TO MINUS AND COUNTER TO ALL ONES.	DS302
D	HOT1,G−1	100	DG4	DECREMENT COUPLED LENGTH COUNTERS BY ONE. IF UNDERFLOW OCCURS IN BITS 4-7, SET G2 SIGN TO MINUS. IF ALL 8 BITS UNDERFLOW, SET G1 SIGN TO MINUS. INSERT HOT CARRY INTO ADDER.	DS301
D	G2−1	101	DG5	DECREMENT LENGTH COUNTER G2 BY ONE. IF UNDERFLOW, SET G2 SIGN TO MINUS AND COUNTER TO ALL ONES.	DS302
D	G−1	110	DG6	DECREMENT COUPLED LENGTH COUNTERS BY ONE. IF UNDERFLOW OCCURS IN BITS 4-7, SET G2 SIGN TO MINUS. IF ALL 8 BITS UNDERFLOW, SET G1 SIGN TO MUNUS.	DS302
D	G1,2−1	111	DG7	DECREMENT EACH LENGTH COUNTER BY ONE. IF A COUNTER UNDERFLOWS, SET ITS SIGN TO MINUS AND ITS VALUE TO ALL ONES.	DS302

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UL FIELD ROSDR 52-53 MOVER ACTION - LATCH BITS 0-3 (NULL VALUE: UL1)

EDGE CHAR	MNEMONIC	BITS	DEC ORDER	FUNCTION	ALD PAGE
B	E→WL	00	UL0	GATE EMIT FIELD TO MOVER LATCH BITS 0-3. (NOTE: EMIT FIELD IS RECODED IF ORDER WM12 IS USED AND ASCII BIT IS ON. SEE WM12.)	DS101
B	UL→WL	01	UL1	GATE LEFT INPUT (U) BITS 0-3 TO LATCH BITS 0-3.	DS101
B	VL→WL	10	UL2	GATE RIGHT INPUT (V) BITS 0-3 TO LATCH BITS 0-3.	DS101
B	?→WL	11	UL3	GATE TO LATCH BITS 0-3 ACCORDING TO CONTENTS OF MOVER FUNCTION REGISTER AS FOLLOWS:	DS101

FUNCTION REGISTER	ACTION
000	CROSS. GATE U BITS 4-7 TO LATCH BITS 0-3.
001	OR. GATE OR OF U BITS 0-3 AND V BITS 0-3 TO LATCH BITS 0-3.
010	AND. GATE AND OF U BITS 0-3 AND V BITS 0-3 TO LATCH BITS 0-3.
011	EXCLUSIVE OR. GATE EXCLUSIVE OR OF U BITS 0-3 AND V BITS 0-3 TO LATCH BITS 0-3.
100	STRAIGHT. GATE U BITS 0-3 TO LATCH BITS 0-3.
101	U LEFT,V RIGHT. GATE U BITS 0-3 TO LATCH BITS 0-3.
110	V LEFT,U RIGHT. GATE V BITS 0-3 TO LATCH BITS 0-3.
111	UNDEFINED

UR FIELD ROSDR 54-55 MOVER ACTION - LATCH BITS 4-7 (NULL VALUE: UR1)

EDGE CHAR	MNEMONIC	BITS	DEC ORDER	FUNCTION	ALD PAGE
B	E→WR	00	UR0	GATE EMIT FIELD TO MOVER LATCH BITS 4-7. (NOTE: EMIT FIELD IS RECODED IF ORDER WM12 IS USED AND ASCII BIT IS ON. SEE WM12.)	DS101
B	UR→WR	01	UR1	GATE LEFT INPUT (U) BITS 4-7 TO LATCH BITS 4-7.	DS101
B	VR→WR	10	UR2	GATE RIGHT INPUT (V) BITS 4-7 TO LATCH BITS 4-7.	DS101
B	?→WR	11	UR3	GATE TO LATCH BITS 4-7 ACCORDING TO CONTENTS OF MOVER FUNCTION REGISTER AS FOLLOWS:	DS101

FUNCTION REGISTER	ACTION
000	CROSS. GATE U BITS 0-3 TO LATCH BITS 4-7.
001	OR. GATE OR OF U BITS 4-7 AND V BITS 4-7 TO LATCH BITS 4-7.
010	AND. GATE AND OF U BITS 4-7 AND V BITS 4-7 TO LATCH BITS 4-7.
011	EXCLUSIVE OR. GATE EXCLUSIVE OR OF U BITS 4-7 AND V BITS 4-7 TO LATCH BITS 4-7.
100	STRAIGHT. GATE U BITS 4-7 TO LATCH BITS 4-7.
101	U LEFT,V RIGHT. GATE V BITS 4-7 TO LATCH BITS 4-7.
110	V LEFT,U RIGHT. GATE U BITS 4-7 TO LATCH BITS 4-7.
111	UNDEFINED

NOTE:- WHEN EQUAL DECIMAL ORDERS ARE USED IN UL AND UR FIELDS, THE FOLLOWING COMBINATION MNEMONICS ARE USED:

UL1 AND UR1: U→W

UL2 AND UR2: V→W

UL3 AND UR3: ?→W

CE FIELD ROSDR 57-60

THIS FIELD IS USED AS DATA BY MICRO ORDERS.

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TEMPLATE FOR 'A' LINE STATEMENT: RRR±LLL→TTTT

WHERE: R = RY FIELD L = LX FIELD
± = TC FIELD T = TR FIELD

LX FIELD ROSDR 61-63 LEFT INPUT TO ADDER (XG)

EDGE CHAR	MNEMONIC	BITS	DEC ORDER	FUNCTION	ALD PAGE
		000	LX0	NO OPERATION	DR011
A	1	000	LX0	NO OPERATION - USED WITH TC0 (COMPLEMENT) FOR -1.	DR011
A	L	001	LX1	GATE L REG TO XG.	DR011
A	SGN	010	LX2	GATE ONE TO XG BIT 0. GATE ZEROS TO OTHER BITS OF XG.	DR011
A	E	011	LX3	GATE EMIT FIELD TO XG BITS 27-30. GATE ZEROS TO OTHER BITS.	DR011
A	LRL	100	LX4	GATE L REG BITS 16-31 TO XG BITS 0-15. GATE ZEROS TO BITS 16-31.	DR011
A	LWA	101	LX5	GATE L REG TO XG. OR ONES INTO XG BITS 30-31 AND RIGHT INPUT (Y) BITS 30-31. THIS MICROINSTRUCTION MUST CONTAIN ORDER TC0 AND EITHER RY1 OR RY4. (USED TO COMPARE WORD ADDRESSES)	DR011
A	4	110	LX6	GATE ONE TO XG BIT 29 (HOT 4). GATE ZEROS TO OTHER BITS.	DR011
A	64C	111	LX7	GATE ONES TO XG BITS 0-1. GATE ZEROS TO OTHER BITS.	DR011

TC FIELD ROSDR 64 TRUE/COMPLEMENT GATING TO LEFT ADDER INPUT (NULL VALUE: TC1)

EDGE CHAR	MNEMONIC	BITS	DEC ORDER	FUNCTION	ALD PAGE
A	-	0	TC0	GATE COMPLEMENT OF XG TO LEFT ADDER INPUT.	DR021
A	+	1	TC1	GATE XG (TRUE) TO LEFT ADDER INPUT.	DR021

RY FIELD ROSDR 65-67 RIGHT INPUT TO ADDER (Y)

EDGE CHAR	MNEMONIC	BITS	DEC ORDER	FUNCTION	ALD PAGE
		000	RY0	NO OPERATION	DR021
A	R	001	RY1	GATE R REGISTER TO Y. (SEE NOTE BELOW)	DR021
A	M	010	RY2	GATE M REGISTER TO Y.	DR021
A	M23	011	RY3	GATE M REG BITS 16-31 TO Y BITS 16-31. GATE ZEROS TO BITS 0-15.	DR021
A	H	100	RY4	GATE H REGISTER TO Y. (SEE NOTE BELOW)	DR021
B	SEMT	101	RY5	OR THE FOUR SDR PARITY BITS INTO THE FOUR EMIT FIELD BITS.	DS021
		110	RY6	UNDEFINED	
		111	RY7	UNDEFINED	

NOTE: IF ORDER LX5 IS USED, ONES ARE ORED INTO Y BITS 30-31. SEE LX5.

AD FIELD ROSDR 68-71 ADDER FUNCTION (NULL VALUE: AD1)

EDGE CHAR	MNEMONIC	BITS	DEC ORDER	FUNCTION	ALD PAGE
		0000	AD0	UNDEFINED	
		0001	AD1	ADD. NO CARRIES ENTERED OR SAVED	
A	BCF0	0010	AD2	ADD. NO CARRY SAVED. IF F REG EQUALS ZERO, INSERT CARRY INTO POSITION 31.	DR031
		0011	AD3	UNDEFINED	
A	BC0	0100	AD4	ADD. SET CARRY STAT TO CARRY OUT OF POSITION 0.	DR032
A	BCVC	0101	AD5	ADD. SET CARRY STAT TO EXCLUSIVE OR OF CARRIES OUT OF POSITIONS 0 AND 1.	DR032
A	BC1B	0110	AD6	ADD. SET CARRY STAT TO CARRY OUT OF POSITION 1. BLOCK CARRY FROM POSITION 8 TO POSITION 7.	DR032
A	BC	0110	AD6	AS ABOVE. USED WITH ORDER AL23.	DR032
A	BC8	0111	AD7	ADD. SET CARRY STAT TO CARRY OUT OF POSITION 8.	DR032
A	DHL	1000	AD8	DECIMAL HALVE (LOW ORDER). BIT 2 OF EACH DIGIT OF THE SUM IS TESTED. IF THE BIT IS ONE, THE NEXT DIGIT POSITION TO THE RIGHT IN THE L REG IS SET TO 0110. IF THE BIT IS ZERO, THE DIGIT IN L REG IS SET TO 0000. THE LEFTMOST DIGIT IN THE L REG IS SET IN THE SAME WAY FROM THE AUXILIARY TRIGGER.	DR031
A	DC0	1001	AD9	DECIMAL ADD. SET STAT 1 TO CARRY OUT OF POSITION 0. INSERT PREVIOUS VALUE OF STAT 1 AS CARRY INTO POSITION 31. TEST CARRY OUT OF EACH DIGIT POSITION. IF CARRY, SET CORRESPONDING DIGIT POSITION IN L REG TO 0000. IF NO CARRY, SET DIGIT IN L REG TO 0110.	DR032
A	DDC0	1010	AD10	DECIMAL DOUBLE. SET STAT 1 TO CARRY OUT OF POSITION 0. INSERT PREVIOUS VALUE OF STAT 1 AS CARRY INTO POSITION 31. TEST EACH DIGIT OF SUM. IF 5 OR GREATER, SET CORRESPONDING DIGIT POSITION IN L REG TO 0110. IF LESS THAN 5, SET DIGIT IN L REG TO 0000.	DR032
A	DHH	1011	AD11	DECIMAL HALVE (HIGH ORDER). BIT 2 OF EACH DIGIT OF THE SUM IS TESTED. IF THE BIT IS ONE, THE NEXT DIGIT POSITION TO THE RIGHT IN THE L REG IS SET TO 0110. IF THE BIT IS ZERO, THE DIGIT IN L REG IS SET TO 0000. THE LEFTMOST DIGIT IN L REG IS SET TO 0000. THE AUXILIARY TRIGGER IS SET TO BIT 2 OF THE RIGHTMOST SUM DIGIT (SUM BIT 30).	DR032
A	DCBS	1100	AD12	DECIMAL ADD. SET STAT 1 TO CARRY OUT OF LEFTMOST BYTE POSITION FOR WHICH A BYTE STAT IS ON. INSERT PREVIOUS VALUE OF STAT 1 AS CARRY INTO POSITION 1. TEST CARRY OUT OF EACH DIGIT POSITION. IF CARRY, SET CORRESPONDING DIGIT POSITION IN L REG TO 0000. IF NO CARRY, SET DIGIT IN L REG TO 0110.	DR032
		1101	AD13	UNDEFINED	
		1110	AD14	UNDEFINED	
		1111	AD15	UNDEFINED	

NOTE: IN ALL CASES ADDITION IS BINARY. THE TERM 'DECIMAL ADD' USED ABOVE REFERS TO THE MANNER OF GENERATING THE CORRECTION FACTOR IN THE L REG.

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AB FIELD ROSDR 72-77 CONDITION BRANCH TEST A

EDGE CHAR	MNEMONIC	BITS	DEC ORDER	FUNCTION	ALD PAGE
R	0	000000	AB0	SET A BIT TO 0.	
R	1	000001	AB1	SET A BIT TO 1.	KK201
R	S0	000010	AB2	SET A BIT TO VALUE OF STAT 0.	KK201
R	S1	000011	AB3	SET A BIT TO VALUE OF STAT 1.	KK201
R	S2	000100	AB4	SET A BIT TO VALUE OF STAT 2.	KK201
R	S3	000101	AB5	SET A BIT TO VALUE OF STAT 3.	KK201
R	S4	000110	AB6	SET A BIT TO VALUE OF STAT 4.	KK201
R	S5	000111	AB7	SET A BIT TO VALUE OF STAT 5.	KK201
R	S6	001000	AB8	SET A BIT TO VALUE OF STAT 6.	KK201
R	S7	001001	AB9	SET A BIT TO VALUE OF STAT 7.	KK201
R	CSTAT	001010	AB10	SET A BIT TO VALUE OF CARRY STAT.	KK211
		001011	AB11	UNDEFINED	
R	1SYLS	001100	AB12	SET A BIT TO VALUE OF ONE SYLLABLE OP IN BUFFER STAT.	KK211
R	LSGNS	001101	AB13	SET A BIT TO VALUE OF L SIGN STAT.	KK211
R	∀SGNS	001110	AB14	SET A BIT TO EXCLUSIVE OR OF L SIGN STAT AND R SIGN STAT.	KK211
		001111	AB15	UNDEFINED	
R	CRMD	010000	AB16	PERFORM AND OF MD REG (MASK) AND DECODED CONDITION REG. IF RESULT IS NON-ZERO, SET A BIT TO ONE. IF RESULT IS ZERO, SET BIT A TO ZERO.	KK251
R	W=0	010001	AB17	IF MOVER LATCHES ARE ZERO, SET A BIT TO ONE. IF NON-ZERO, SET A BIT TO ZERO.	KK211
R	WL=0	010010	AB18	IF MOVER LATCH BITS 0-3 ARE ZERO, SET A BIT TO ONE. IF NON-ZERO, SET A BIT TO ZERO.	KK211
R	WR=0	010011	AB19	IF MOVER LATCH BITS 4-7 ARE ZERO, SET A BIT TO ONE. IF NON-ZERO, SET A BIT TO ZERO.	KK211
R	MD=FP	010100	AB20	IF BOTH BIT 0 AND BIT 3 OF MD REG ARE ZERO, SET A BIT TO ONE. OTHERWISE SET A BIT TO ZERO. (VALID FLOATING POINT REG)	KK221
R	MB=3	010101	AB21	IF MB COUNTER EQUALS 3, SET A BIT TO ONE. OTHERWISE SET A BIT TO ZERO.	KK221
R	MD3=0	010110	AB22	SET A BIT TO COMPLEMENT OF MD REG BIT 3.	KK221
R	G1=0	010111	AB23	IF LENGTH COUNTER G1 IS ZERO, SET A BIT TO ONE. OTHERWISE SET A BIT TO ZERO.	KK221
R	G1<0	011000	AB24	SET A BIT TO VALUE OF LENGTH COUNTER G1 SIGN.	KK221
R	G<4	011001	AB25	IF COUPLED LENGTH COUNTERS HAVE VALUE LESS THAN 4, SET A BIT TO ONE. OTHERWISE SET A BIT TO ZERO. SIGN OF G1 IS INCLUDED IN VALUE.	KK221

AB FIELD (CONTINUED)

EDGE CHAR	MNEMONIC	BITS	DEC ORDER	FUNCTION	ALD PAGE
R	G1MBZ	011010	AB26	IF EITHER LENGTH COUNTER G1 OR MB COUNTER IS ZERO, SET A BIT TO ONE. OTHERWISE SET A BIT TO ZERO.	KK221
R	IOS0	011011	AB27	SET A BIT TO VALUE OF MULTIPLEXOR CHANNEL STAT 0.	KK191
R	IOS2	011100	AB28	SET A BIT TO VALUE OF MULTIPLEXOR CHANNEL STAT 2.	KK191
R	R(31)	011101	AB29	SET A BIT TO VALUE OF R REG BIT 31.	KK221
R	F(2)	011110	AB30	SET A BIT TO VALUE OF F REG BIT 2.	KK231
R	L(0)	011111	AB31	SET A BIT TO VALUE OF L REG BIT 0.	KK231
R	F=0	100000	AB32	IF F REG IS ZERO, SET A BIT TO ONE. OTHERWISE SET A BIT TO ZERO.	KK231
R	UNORM	100001	AB33	IF STAT 0 IS OFF AND ADDER OUTPUT BITS 8-11 ARE ZERO, SET A BIT TO ONE. OTHERWISE SET A BIT TO ZERO.	KK231
R	TZ*BS	100010	AB34	IF ALL BYTES OF ADDER OUTPUT SPECIFIED BY BYTE STATS ARE ZERO, SET A BIT TO ONE. OTHERWISE SET A BIT TO ZERO.	KK231
R	EDITPAT	100011	AB35	SET A BIT TO VALUE OF EDIT STAT 1. SET B BIT TO VALUE OF EDIT STAT 2. (SEE NOTE 1)	KK231
R	PROB	100100	AB36	SET A BIT TO VALUE OF PSW BIT 15.	KK231
R	TIMUP	100101	AB37	SET A BIT TO VALUE OF TIMER UPDATE SIGNAL. RESET TIMER UPDATE SIGNAL.	KK231
		100110	AB38	UNDEFINED	
R	GZ/MB3	100111	AB39	IF EITHER THE VALUE OF THE COUPLED LENGTH COUNTER G IS ZERO OR THE VALUE OF THE MB COUNTER IS 3 SET A BIT TO ONE. OTHERWISE SET A BIT TO ZERO.	KK231
		101000	AB40	UNDEFINED	
R	LOG	101001	AB41	SET A BIT TO VALUE OF LOG/SCAN STAT.	KK291
R	STC=0	101010	AB42	IF SCAN TEST COUNTER IS ZERO, SET A BIT TO ONE. OTHERWISE SET A BIT TO ZERO.	KK291
R	G2<=LB	101011	AB43	IF LENGTH COUNTER G2 IS LESS THAN OR EQUAL TO LB COUNTER, SET A BIT TO ONE. OTHERWISE SET A BIT TO ZERO. SIGN OF LENGTH COUNTER IS IGNORED.	KK251
		101100	AB44	UNDEFINED	
R	D(7)	101101	AB45	SET A BIT TO VALUE OF SDR BIT 7.	KK221
R	SCPS	101110	AB46	SET A BIT TO VALUE OF SCAN PASS STAT.	KK291
R	SCFS	101111	AB47	SET A BIT TO VALUE OF SCAN FAIL STAT.	KK291
R	STORV	110000	AB48	SET A BIT TO VALUE OF I/O STORAGE VIOLATION TRIGGER.	KK291
R	W(67)→AB	110001	AB49	SET A BIT TO VALUE OF MOVER LATCH BIT 6. SET B BIT TO VALUE OF MOVER LATCH BIT 7. (SEE NOTE 1)	KK291

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AB FIELD (CONTINUED)

EDGE CHAR	MNEMONIC	BITS	DEC ORDER	FUNCTION	ALD PAGE
R	Z23≠0	110010	AB50	IF ADDER OUTPUT BITS 16-31 ARE NON-ZERO SET A BIT TO ONE. OTHERWISE SET A BIT TO ZERO.	KK211
R	CCW2OK	110011	AB51	IF SDR BITS 16-31 AND 5-7 ARE ALL ZERO SET A BIT TO ONE. OTHERWISE SET A BIT TO ZERO. (COUNT AND FLAG TEST)	KK291
R	MXBIO	110100	AB52	SET A BIT TO VALUE OF MULTIPLEXOR INPUT BUFFER BIT 0.	KK191
R	IBFULL	110101	AB53	SET A BIT TO VALUE OF INPUT BUFFER FULL STAT.	KK191
R	CANG	110110	AB54	IF ADDER OUTPUT BITS 29-31 ARE NON-ZERO OR INVALID ADDRESS TRIGGER IS ON. SET A BIT TO ONE. OTHERWISE SET A BIT TO ZERO.	KK291
R	CHLOG	110111	AB55	SET A BIT TO VALUE OF CHANNEL ERROR LOG REQUEST LINE.	KK191
R	I-FETCH	111000	AB56	FOUR-WAY BRANCH: (SEE NOTE 1) 0→A.0→B IAR BIT 30 IS ONE AND REFETCH STAT OFF 0→A.1→B IAR BIT 30 IS ONE AND REFETCH STAT ON 1→A.0→B IAR BIT 30 IS ZERO 1→A.1→B EXCEPTION TRIGGER ON	KK151
R	IA(30)	111001	AB57	SET A BIT TO VALUE OF IAR BIT 30.	KK211
R	EXT.CHIRPT	111010	AB58	IF EITHER A TIMER UPDATE REQUEST HAS OCCURRED. OR AN EXTERNAL INTERRUPT IS REQUESTED WITH MASK BIT ON. SET A BIT TO ONE. OTHERWISE SET A BIT TO ZERO. IF A CHANNEL INTERRUPT IS REQUESTED SET B BIT TO ONE. OTHERWISE SET B BIT TO ZERO. (SEE NOTE 1)	KK151
R	DCHOLD	111011	AB59	SET A BIT TO VALUE OF DIRECT CONTROL HOLD LINE.	KK191
R	PSS	111100	AB60	SET A BIT TO VALUE OF PROGRESSIVE SCAN STAT.	KK191
R	IOS4	111101	AB61	SET A BIT TO VALUE OF MULTIPLEXOR CHANNEL STAT 4.	KK191
		111110	AB62	UNDEFINED	
R	RX.SO	111111	AB63	IF STAT 0 IS ON AND M REG BITS 0-1 HAVE VALUE 01 SET A BIT TO ONE. OTHERWISE SET A BIT TO ZERO. (RX FORMAT AND INDEXING REQUIRED)	KK251

NOTE 1 IN BRANCHES WHERE BOTH A AND B BITS ARE SET. THE B BIT VALUE IS THE OR OF VALUES SPECIFIED BY AB AND BB FIELDS.

NOTE 2 A BIT AND B BIT VALUES MAY BE SUBSEQUENTLY ALTERED BY ZN FIELD ORDERS.

NOTE 3 ALL AB FIELD BRANCHES TEST CONDITIONS EXISTING AT THE END OF THE PREVIOUS CYCLE.

EXCEPTION TRIGGER SET WHEN WAIT BIT IS ON
PROBLSVC checked by AB56

EDIT STATS : MOVER (EVERY CYCLE)

I/O MODE TRIGGER CONTROLS DECODING.

EXCEP TRIG
SET BY
WAIT BIT
EXT INTRT PENDING
TIM INTRT "
CHAN INTRPT "
ADD COMPARE

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BB FIELD ROSDR 78-82 B CONDITION TEST

EDGE CHAR	MNEMONIC	BITS	DEC ORDER	FUNCTION	ALD PAGE
R	0	00000	BB0	SET B BIT TO 0.	
R	1	00001	BB1	SET B BIT TO 1.	KK141
R	S0	00010	BB2	SET B BIT TO VALUE OF STAT 0.	KK141
R	S1	00011	BB3	SET B BIT TO VALUE OF STAT 1.	KK141
R	S2	00100	BB4	SET B BIT TO VALUE OF STAT 2.	KK141
R	S3	00101	BB5	SET B BIT TO VALUE OF STAT 3.	KK141
R	S4	00110	BB6	SET B BIT TO VALUE OF STAT 4.	KK141
R	S5	00111	BB7	SET B BIT TO VALUE OF STAT 5.	KK141
R	S6	01000	BB8	SET B BIT TO VALUE OF STAT 6.	KK141
R	S7	01001	BB9	SET B BIT TO VALUE OF STAT 7.	KK141
R	RSGNS	01010	BB10	SET B BIT TO VALUE OF R SIGN STAT.	KK151
R	HSCH	01011	BB11	IF HIGH SPEED CHANNEL IS OPERATING OR 256 SUBCHANNEL OPTION IS INSTALLED, SET B BIT TO ONE. OTHERWISE SET B BIT TO ZERO.	KK141
R	EXC	01100	BB12	SET B BIT TO VALUE OF EXCEPTION TRIGGER.	KK151
R	WR=0	01101	BB13	IF MOVER LATCH BITS 4-7 ARE ZERO, SET B BIT TO ONE. OTHERWISE SET B BIT TO ZERO.	KK151
		01110	BB14	UNDEFINED	
R	T13=0	01111	BB15	IF ADDER OUTPUT BUS BITS 8-13 ARE ZERO, SET B BIT TO ONE. OTHERWISE SET B BIT TO ZERO.	KK151
R	T(0)	10000	BB16	SET B BIT TO VALUE OF ADDER OUTPUT BUS BIT 0.	KK151
R	T=0	10001	BB17	IF ADDER OUTPUT BUS IS ZERO, SET B BIT TO ONE. OTHERWISE SET B BIT TO ZERO.	KK151
R	TZ*BS	10010	BB18	IF THE BYTES OF THE ADDER OUTPUT BUS SPECIFIED BY THE BYTE STATS ARE ALL ZERO, SET B BIT TO ONE. OTHERWISE SET B BIT TO ZERO.	KK151
R	W=1	10011	BB19	IF THE MOVER LATCHES CONTAIN 0000 0001 SET B BIT TO ONE. OTHERWISE SET B BIT TO ZERO.	KK151
R	LB=0	10100	BB20	IF LB COUNTER IS ZERO SET B BIT TO ONE. OTHERWISE SET B BIT TO ZERO.	KK161
R	LB=3	10101	BB21	IF LB COUNTER EQUALS 3 SET B BIT TO ONE. OTHERWISE SET B BIT TO ZERO.	KK161
R	MD=0	10110	BB22	IF MD REG IS ZERO SET B BIT TO ONE. OTHERWISE SET B BIT TO ZERO.	KK161
R	G2=0	10111	BB23	IF LENGTH COUNTER G2 IS ZERO SET B BIT TO ONE. OTHERWISE SET B BIT TO ZERO.	KK161
R	G2<0	11000	BB24	SET B BIT TO VALUE OF LENGTH COUNTER G2 SIGN.	KK161
R	G2LBZ	11001	BB25	IF EITHER LENGTH COUNTER G2 OR LB COUNTER IS ZERO, SET B BIT TO ONE. OTHERWISE SET B BIT TO ZERO.	KK161

BB FIELD (CONTINUED)

EDGE CHAR	MNEMONIC	BITS	DEC ORDER	FUNCTION	ALD PAGE
R	IOS1	11010	BB26	SET B BIT TO VALUE OF MULTIPLEXOR CHANNEL STAT 1.	KK151
R	MD/JI	11011	BB27	IF EITHER BIT 1 OR BIT 3 OF EITHER MD REG OR J REG IS ONE, SET B BIT TO ONE (ILLEGAL FP REG). OTHERWISE SET B BIT TO ZERO.	KK161
R	IVA	11100	BB28	SET B BIT TO VALUE OF INVALID ADDRESS STAT.	KK161
R	IOS3	11101	BB29	SET B BIT TO VALUE OF MULTIPLEXOR CHANNEL STAT 3.	KK161
R	(CAR)	11110	BB30	SET B BIT TO VALUE OF CARRY LATCH AS SET THIS CYCLE.	KK171
R	(Z00)	11111	BB31	SET B BIT TO VALUE OF ADDER SUM BIT 0 (BEFORE SHIFT) THIS CYCLE.	KK171

NOTE WITH THE EXCEPTION OF ORDERS BB30 AND BB31, ALL TESTS ARE MADE ON THE STATUS OF THE CPU AT THE END OF THE PREVIOUS CYCLE.

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3 AUG 65 255449

CONTROL SIGNAL SPECIFICATION
CPU MODE
DATE 16 AUG 65 MACH. 2050
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CF110

SS FIELD ROSDR 84-89 STAT SETTING AND MISCELLANEOUS CONTROL

EDGE CHAR	MNEMONIC	BITS	DEC ORDER	FUNCTION	ALD PAGE
		000000	SS0	NO OPERATION	
		000001	SS1	UNDEFINED	
		000010	SS2	UNDEFINED	
C	D→CR*BS	000011	SS3	SET CONDITION REG FOR TEST AND SET INSTRUCTION. SET COND REG BIT 0 TO 0. SET BIT 1 OF COND REG TO ONE IF THE FIRST BIT IS ON IN ANY SDR BYTE SELECTED BY THE CPU BYTE STATS. WHEN USED WITH LARGE CAPACITY STORAGE, THIS ORDER INTERLOCKS THE SAME AS AN SDR TO LATCH TRANSFER.	RP251
C	E→SCANCTL	000100	SS4	CONTROL SCAN STATS PER EMIT FIELD AS FOLLOWS:	KS601

EMIT — FUNCTION

0000 IF SCAN TEST STAT IS OFF AND SDR IS ALL ONES SET SCAN TEST STAT ON. IF SCAN TEST STAT IS ON AND SDR IS ZERO LEAVE SCAN TEST STAT ON. OTHERWISE SET SCAN TEST STAT OFF.

0001 IF SCAN TEST STAT IS OFF TURN ON SCAN PASS STAT. IF SCAN TEST STAT IS ON TURN ON SCAN FAIL STAT. INCREMENT SCAN TEST COUNTER BY 1.

0010 TURN OFF SCAN TEST STAT.

0011 TURN OFF IGNORE I/O ERROR TRIGGER.

0100 TURN ON IGNORE I/O ERROR TRIGGER.

0101 TURN OFF SCAN PASS STAT AND SCAN FAIL STAT.

0110 TURN ON INVERT SAR BIT 13 TRIGGER.

0111 TURN OFF INVERT SAR BIT 13 TRIGGER.

1000 SET SUPERVISORY SCAN TRIGGER TO VALUE OF SDR BIT 6. SET PROGRESSIVE SCAN STAT TO VALUE OF SDR BIT 5. SET CLOCK ADVANCE COUNTER TO VALUE OF SDR BITS 0-2.

1001-1011 UNDEFINED

1100 TURN OFF LOG/SCAN STAT.

1101-1111 UNDEFINED

EDGE CHAR	MNEMONIC	BITS	DEC ORDER	FUNCTION	ALD PAGE
C	L•RSGNS	000101	SS5	IF LEFT MOVER INPUT U BITS 4-7 HAS VALUE LESS THAN 1010, FORCE INVALID DATA ROS TRAP. IF VALUE EQUALS 1011 OR 1101 (MINUS SIGN) TURN ON L SIGN STAT AND INVERT R SIGN STAT. OTHERWISE TURN OFF L SIGN STAT.	KS601
C	IVD/RSGNS	000110	SS6	IF LEFT MOVER INPUT U BITS 4-7 HAS VALUE LESS THAN 1010, FORCE INVALID DATA ROS TRAP. IF VALUE EQUALS 1011 OR 1101 (MINUS SIGN) INVERT R SIGN STAT.	KS601
C	EDITSGN	000111	SS7	IF MOVER LATCH BITS 4-7 HAS VALUE GREATER THAN 1001 (VALID SIGN) TURN ON R SIGN STAT. OTHERWISE TURN OFF R SIGN STAT. IF MOVER LATCH BITS 4-7 EQUAL TO 1010, 1100, 1110 OR 1111 (PLUS SIGN) TURN OFF L SIGN STAT.	KS601
C	E→S03	001000	SS8	GATE EMIT FIELD TO STATS 0-3.	KS611
C	S03ΩE•1→LSGN	001001	SS9	TURN ON STATS 0-3 PER EMIT FIELD. TURN ON L SIGN STAT.	KS611
C	S03ΩE	001010	SS10	TURN ON STATS 0-3 PER EMIT FIELD.	KS611
C	S03ΩE•0→BS	001011	SS11	TURN ON STATS 0-3 PER EMIT FIELD. TURN OFF CPU BYTE STATS.	KS611
C	X0•B0•1SYL	001100	SS12	IF ADDER LATCH BITS 12-15 ARE ZERO, SET STAT 0 TO ONE. (X=0) OTHERWISE SET STAT 0 TO ZERO. IF ADDER LATCH BITS 16-19 ARE ZERO, SET STAT 1 TO ONE. (B=0) OTHERWISE SET STAT 1 TO ZERO. IF ADDER LATCH BITS 16-17 ARE ZERO, SET ONE-SYLLABLE-OP-IN-BUFFER STAT TO ONE. OTHERWISE SET THIS STAT TO ZERO.	KS611
C	FPZERO	001101	SS13	IF ADDER LATCH BITS 8-31 ARE ZERO, F REG IS ZERO, AND STAT 3 IS ON, TURN ON STAT 0. OTHERWISE TURN OFF STAT 0.	KS611

SS FIELD (CONTINUED)

EDGE CHAR	MNEMONIC	BITS	DEC ORDER	FUNCTION	ALD PAGE
C	FPZERO•E→FN	001110	SS14	IF ADDER LATCH BITS 8-31 ARE ZERO, F REG IS ZERO, AND STAT 3 IS ON, TURN ON STAT 0. OTHERWISE TURN OFF STAT 0. GATE EMIT FIELD BITS 2-3 TO LOCAL STORAGE FUNCTION REG. (EFFECTIVE FOR LOCAL STORAGE ADDRESSING THIS CYCLE.)	KS611
C	B0•1SYL	001111	SS15	IF ADDER LATCH BITS 0-3 ARE ZERO, TURN ON STAT 1. (B=0) OTHERWISE TURN OFF STAT 1. IF ADDER LATCH BITS 16-17 ARE ZERO, TURN ON ONE-SYLLABLE-OP-IN-BUFFER STAT. OTHERWISE TURN THIS STAT OFF.	KS611
C	S03•¬E	010000	SS16	TURN OFF STATS 0-3 PER EMIT FIELD.	KS621
C	(T=0)→S3	010001	SS17	IF ADDER LATCH IS ZERO TURN ON STAT 3. OTHERWISE TURN OFF STAT 3.	KS621
C	E→BS•T30→S3	010010	SS18	GATE EMIT FIELD TO CPU BYTE STATS. SET STAT 3 TO VALUE OF ADDER LATCH BIT 30.	KS621
C	E→BS	010011	SS19	GATE EMIT FIELD TO CPU BYTE STATS.	KS621
C	1→BS*MB	010100	SS20	TURN ON BYTE STAT INDICATED BY VALUE OF MB COUNTER.	KS621
C	DIRCTL*E	010101	SS21	DIRECT CONTROL PER EMIT AS FOLLOWS:	KS631

EMIT BIT — FUNCTION IF BIT IS ON

0 GATE H REG BITS 24-31 TO DIRECT CONTROL DATA OUT REG.

1 INITIATE PULSE ON WRITE OUT LINE.

2 GATE H REG BITS 8-15 TO DIRECT CONTROL TIMING SIGNAL BUS OUT LINES IN PULSE FORM.

3 INITIATE PULSE ON READ OUT LINE. IF AT THE END OF THIS PULSE THE HOLD IN LINE IS NOT ON, LATCH THE DIRECT CONTROL BUS IN.

		010110	SS22	UNDEFINED	
C	MANUAL→STOP	010111	SS23	SET STOP TRIGGER TO VALUE OF MANUAL TRIGGER.	KS721
C	E→S47	011000	SS24	GATE EMIT FIELD TO STATS 4-7.	KS621
C	S47ΩE	011001	SS25	TURN ON STATS 4-7 PER EMIT FIELD.	KS621
C	S47•¬E	011010	SS26	TURN OFF STATS 4-7 PER EMIT FIELD.	KS621
C	S47•ED*FP	011011	SS27	SET STATS 4-7 AND EXPONENT DIFFERENCE REG FOR FLOATING POINT AS FOLLOWS:	KS621

STAT 4 TURNED ON IF:
STAT 0 OR STAT 1 IS ON AND RIGHT ADDER INPUT BIT 0 IS ONE AND THERE IS A CARRY OUT OF POSITION 1.
OR STAT 0 OR STAT 1 IS ON, THERE IS A CARRY OUT OF POSITION 1, AND EITHER LEFT ADDER INPUT BIT 0 IS ONE OR STAT 1 IS ON BUT NOT BOTH (ADD TYPE, RESULT MINUS)
OR BOTH STAT 0 AND STAT 1 ARE OFF AND LEFT ADDER INPUT BIT 0 IS NOT EQUAL TO RIGHT ADDER INPUT BIT 0 (MULTIPLY OR DIVIDE, SIGNS UNLIKE)

STAT 5 TURNED ON IF LEFT ADDER INPUT BIT 0, RIGHT ADDER INPUT BIT 0 AND STAT 1 CONTAIN AN EVEN NUMBER OF ONES. (TRUE ADD REQUIRED)

STAT 6 TURNED ON IF VALUE OF EXPONENT DIFFERENCE REG IS LESS THAN 16 (DEC) IN ABSOLUTE VALUE.

STAT 7 TURNED ON IF VALUE OF EXPONENT DIFFERENCE REG IS ZERO.

ABSENCE OF TURN ON CONDITION CAUSES STAT TO BE TURNED OFF.

EXPONENT DIFFERENCE REG SET AS FOLLOWS:
BIT 0 SET TO ONE IF CARRY FROM ADDER POS 1 AND SUM BITS 1-4 NON-ZERO, OR IF NO CARRY FROM POS 1 AND SUM BITS 1-4 EQUAL 1111.
BITS 1-3 SET EQUAL TO ADDER SUM BITS 5-7.

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CF111

SS FIELD (CONTINUED)

EDGE CHAR	MNEMONIC	BITS	DEC ORDER	FUNCTION	ALD PAGE
C	OPPANEL→S47	011100	SS28	SET STATS 4–7 PER MAINTENANCE CONSOLE SWITCHES AS FOLLOWS:	KS621

STATS	CONDITION
0000	NONE OF THOSE DESCRIBED BELOW.
0001	INSTRUCTION STEP, WAIT BIT NOT ON, START.
0010	SET INSTRUCTION COUNTER, MANUAL TRIGGER ON.
0011	REPEAT INSTRUCTION, MANUAL TRIGGER ON.
0100	IAR COMPARE (SYNC OR STOP), MANUAL TRIGGER AND WAIT BIT BOTH OFF.
0110	ENTER CHANNEL, MANUAL TRIGGER ON.
1XXY	DISPLAY OR STORE WITH MANUAL TRIGGER ON AS FOLLOWS:

XX – 00 MAIN STORAGE
01 PROTECTION TAG STORAGE
10 LOCAL STORAGE
11 MULTIPLEXOR BUMP STORAGE

Y – 0 DISPLAY
1 STORE

C	CAR,(T≠0)→CR	011101	SS29	SET LEFT BIT OF CONDITION REG (PSW BIT 34) TO VALUE OF CARRY OUT OF ADDER POSITION 0. SET RIGHT BIT (PSW 35) TO ONE IF ADDER LATCH IS NON-ZERO, TO ZERO IF LATCH IS ZERO.	KS621
C	KEY→F	011110	SS30	GATE FROM TAG STORAGE DATA LINES TO F REG. IF SAR ADDRESSES LCS, INITIATE SIGNAL TO STORAGE INDICATING READ STORAGE KEY OPERATION.	KS641
C	F→KEY	011111	SS31	GATE F REG TO TAG STORAGE DATA LINES. INITIATE WRITE STORAGE KEY OPERATION. (NOTE: THIS ORDER IS GIVEN ON W2 CYCLE OF STORAGE AND CAUSES HOLDOFF UNTIL NEXT W2 CYCLE.)	KS641
C	1→LSGNS	100000	SS32	TURN ON L SIGN STAT.	KS641
C	0→LSGNS	100001	SS33	TURN OFF L SIGN STAT.	KS641
C	1→RSGNS	100010	SS34	TURN ON R SIGN STAT.	KS641
C	0→RSGNS	100011	SS35	TURN OFF R SIGN STAT.	KS641
C	L(0)→LSGNS	100100	SS36	SET L SIGN STAT TO VALUE OF L REG BIT 0.	KS641
C	R(0)→RSGNS	100101	SS37	SET R SIGN STAT TO VALUE OF R REG BIT 0.	KS641
C	E(13)→WFN	100110	SS38	GATE EMIT FIELD BITS 1–3 TO MOVER FUNCTION REG.	KS641
C	E(23)→LSFN	100111	SS39	GATE EMIT FIELD BITS 2–3 TO LOCAL STORAGE FUNCTION REG. (EFFECTIVE FOR LOCAL STORAGE ADDRESSING THIS CYCLE.)	KS641
C	E(23)→CR	101000	SS40	GATE EMIT FIELD BITS 2–3 TO CONDITION REG (PSW BITS 34–35).	KS651
C	SETCRALG	101001	SS41	SET THE CONDITION REG ACCORDING TO ALGEBRAIC CONDITIONS AS FOLLOWS:	KS651

COND CODE	CONDITION
00	ADDER LATCH ZERO.
01	ADDER LATCH BIT 0 IS ONE. (MINUS)
10	ADDER LATCH BIT 0 IS ZERO, BITS 1–31 NON-ZERO. (PLUS)

SS FIELD (CONTINUED)

EDGE CHAR	MNEMONIC	BITS	DEC ORDER	FUNCTION	ALD PAGE
C	SETCRLOG	101010	SS42	SET THE CONDITION REG ACCORDING TO LOGICAL CONDITIONS AS FOLLOWS:	KS651

COND CODE	CONDITION
00	ADDER LATCH BYTES SELECTED BY BYTE STATS ARE ZERO.
01	ADDER LATCH BYTES SELECTED BY BYTE STATS ARE NOT ALL ZERO AND THERE IS NO CARRY OUT OF ADDER POSITION 0.
10	ADDER LATCH BYTES SELECTED BY BYTE STATS ARE NOT ALL ZERO AND THERE IS A CARRY OUT OF ADDER POSITION 0.

C	¬S4,S4→CR	101011	SS43	SET LEFT BIT OF CONDITION REG (PSW BIT 34) TO THE COMPLEMENT OF STAT 4. SET THE RIGHT BIT (PSW BIT 35) EQUAL TO STAT 4.	KS651
C	S4,¬S4→CR	101100	SS44	SET LEFT BIT OF CONDITION REG (PSW BIT 34) EQUAL TO STAT 4. SET THE RIGHT BIT (PSW 35) TO THE COMPLEMENT OF STAT 4.	KS651
C	1→REFETCH	101101	SS45	TURN ON THE REFETCH TRIGGER.	KS651
C	SYNC→OPPANEL	101110	SS46	SEND ADDRESS COMPARE SYNC/STOP PULSE TO CONSOLE.	KS651
C	SCAN≠E,10	101111	SS47	TURN ON SCAN CONTROL TRIGGER 1. IF THIS MICROINSTRUCTION CONTAINS TR22 ORDER, TURN ON SCAN CONTROL TRIGGER 0. OTHERWISE TURN IT OFF. GATE EMIT FIELD TO SCAN CONTROL TRIGGERS 2–5.	KS521
C	1→SUPOUT	110000	SS48	TURN ON MULTIPLEXOR CHANNEL SUPPRESS OUT LINE.	KS661
C	MPXSELRESET	110001	SS49	SELECTIVE RESET OF MULTIPLEXOR CHANNEL.	KS661
C	E(0)→IBFULL	110010	SS50	SET INTERRUPT BUFFER FULL STAT TO VALUE OF EMIT FIELD BIT 0.	KS661
		110011	SS51	UNDEFINED	
C	E→CH	110100	SS52	GATE THE EMIT FIELD TO THE COMMON CHANNEL.	KS661
		110101	SS53	UNDEFINED	
C	1→TIMERIRPT	110110	SS54	TURN ON THE TIMER BIT IN THE EXTERNAL INTERRUPT REG.	KS661
C	T→PSW,IPL→T	110111	SS55	GATE IPL UNIT ADDRESS BITS 0–7 TO L REG BITS 0–7. GATE CHANNEL ADDRESS TO L REG BITS 21–23. ORDER TR7 IS USED WITH THIS ORDER TO PROVIDE REGISTER PULSE FOR L, BUT T→L GATING IS INHIBITED.	KS661
C	T→PSW	111000	SS56	GATE ADDER LATCH BITS 12–15 TO PSW BITS 12–15 (MODE BITS).	KS671
C	SCAN≠E,00	111001	SS57	TURN OFF SCAN CONTROL TRIGGER 1. IF THIS MICROINSTRUCTION CONTAINS TR22 ORDER, TURN ON SCAN CONTROL TRIGGER 0. OTHERWISE TURN IT OFF. GATE EMIT FIELD TO SCAN CONTROL TRIGGERS 2–5.	KS521
C	1→IOMODE	111010	SS58	TURN ON I/O MODE STAT.	KS671
C	0→IOMODE	111011	SS59	TURN OFF I/O MODE STAT.	KS671
C	1→SELOUT	111100	SS60	TURN ON MULTIPLEXOR CHANNEL SELECT OUT LINE.	KS671
C	1→ADROUT	111101	SS61	TURN ON MULTIPLEXOR CHANNEL ADDRESS OUT LINE.	KS671
C	1→COMOUT	111110	SS62	TURN ON MULTIPLEXOR CHANNEL COMMAND OUT LINE.	KS671
C	1→SERVOUT	111111	SS63	TURN ON MULTIPLEXOR CHANNEL SERVICE OUT LINE.	KS671

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CF112

QG300•CFE
(1000XX)
FL PT LOAD

QA111•GBE
(0000XX)
(0001XX)
(0010XX)
(0011XX)
(1000XX)
SECOND LEVEL
I-FETCH

LNR

0001XX — 0284
A L→R
L FN•MD→LSA
L R→LS
C SETCRALG
R BΩ(A=0)→B
R L(0) 0
E1— ** —EA

IF T=0• 00→CR
IF T<0• 01→CR
IF 0<T• 10→CR

STORE•SET CR
ASSUMING NEG•
IF POS•DO
AGAIN NEXT CY

NEG

POS

01 — 0219
A —L→R
A BCVC
D HOT1→ADDER
L FN•MD→LSA
L R→LS
S IA+0/2→A
S SMIF
C SETCRALG
R I-FETCH
G3— ** —GC

SAVE CAR(0)
CAR(1)
SUPPRESS MEMORY
IF OFF BNDS
AND ¬REFETCH
IF T=0• 00→CR
IF T<0• 01→CR
IF 0<T• 10→CR
EXCPNΩIA(30)→A
EXCPNΩ(IA(30)•REF)→B

NO OFLO
POSSIBLE

COMPLEMENT•
STORE•SET CR
AGAIN•
OVLAP I-FETCH

LTR

0010XX — 0288
A L→T
L FN•MD→LSA
L L→LS
S IA+0/2→A
S SMIF
C SETCRALG
R I-FETCH
A7— ** —AG

SUPPRESS MEMORY
IF OFF BNDS
AND ¬REFETCH
IF T=0• 00→CR
IF T<0• 01→CR
IF 0<T• 10→CR
EXCPNΩIA(30)→A
EXCPNΩ(IA(30)•REF)→B

STORE• SET CR•
OVLAP I-FETCH•

LR

1000XX — 02A0
A L→T
L FN•MD→LSA
L L→LS
S IA+0/2→A
S SMIF
R I-FETCH
E7— ** —EG

STORE•OVLAP I-FETCH

01 — 021D
E 0010
C E(13)→WFN
G5— 11 —GE

SET WFN FOR
PGM MASK TEST

QB730 —EAE
(10)
I-FETCH

QB730 —GEE
(11)
TEST MASK FOR
OFLO TRAP

QT105 —GCD
(00•01•10•11)
I-FETCH

LCR

0011XX — 028C
E 1000
A —L→R
A BCVC
B E→WR
B W→MMB
D HOT1→ADDER
L FN•MD→LSA
L R→LS
C SETCRALG
R 0 (CAR)
L1— 0* —LA

SAVE CAR(0)
CAR(1)
IF T=0• 00→CR
IF T<0• 01→CR
IF 0<T• 10→CR

COMPLEMENT• SET
CR• STORE RESULT
OFLO ONLY FOR
MAX NEG NUMBER

RESULT OK
00 — 021C
E 1110
L WS•E→LSA
L LS→L→LS
S IA+0/2→A
C E→S47
R I-FETCH
L5— ** —LE

EXCPNΩIA(30)→A
EXCPNΩ(IA(30)•REF)→B
I-FETCH CY 1

QT110 —LEE
(00•01•10•11)
I-FETCH

LPR

0000XX — 0280
E 1000
A L→R
B E→WR
B W→MMB
L FN•MD→LSA
L R→LS
C SETCRALG
R L(0) 0
Q1— *0 —QA

IF T=0• 00→CR
IF T<0• 01→CR
IF 0<T• 10→CR

STORE•SET CR
ASSUMING POS•

POSITIVE•

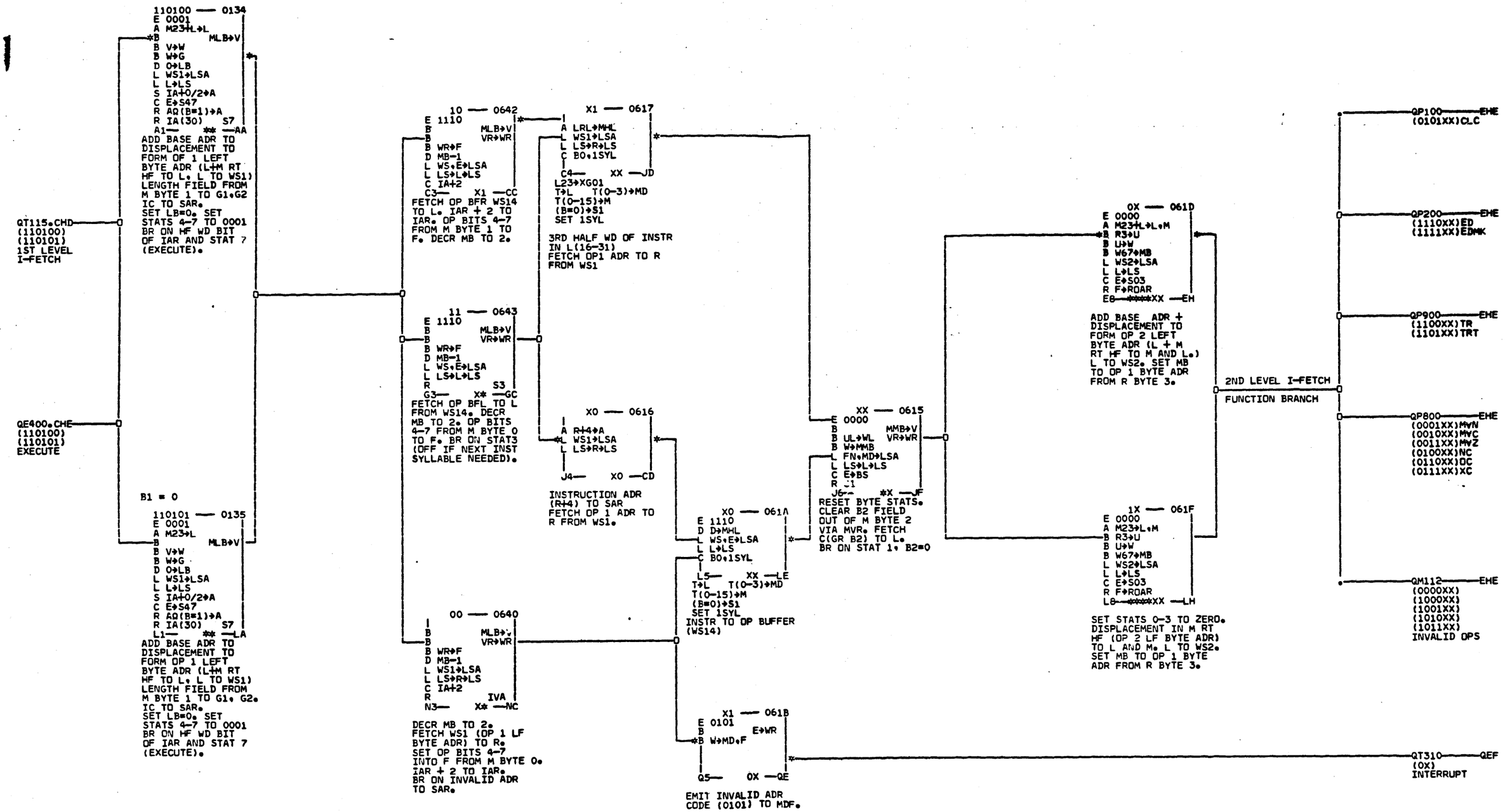
10 — 021E
A —L→R
A BCVC
D HOT1→ADDER
L FN•MD→LSA
L R→LS
C SETCRALG
R 0 (CAR)
Q5— 0* —QE

SAVE CAR(0) V
CAR(1)
IF T=0• 00→CR
IF T<0• 01→CR
IF 0<T• 10→CR

COMPLEMENT•
STORE•SET CR
AGAIN• TEST
OFLO•

QB100

254760	12/21/64	MACH	C2050	DATE 11/15/65	SHEET 1	QB100
255449	09/20/65	NAME		LOG 904	VERSION	
		MODE	MANUAL	FXD PT RR LOADS		
		P•N•	5364721	LPR LNR LTR LCR LR		
		IBM CORP•	SDD			



QP010

254760	12/21/64	MACH	C2050	DATE 11/15/65	SHEET 1 QP010
255449	09/20/65	NAME		LOG 904	VERSION
		MODE	MANUAL	2ND LEVEL I-FETCH FOR VFL CHARACTER OPS	
		P•N•	5364794		
		IBM CORP•	SDD		

REGISTERS—
L— OP2
R— OP2 ADR
H— OP1
H— OP1 ADR

XO — 063A
E 1000
D D→M
C S03→E
R S2 A4— 1 *1 —AD

NEXT OP1 WD TO M
TN ON S0 TO INDICATE
NON-ZERO BYTE STORED
BR ON OP2 FETCH
RQD (CASE 2)

NOT MOVE INSTR
FETCH NEXT OP1 WORD
10 — 060E
A H+4→A
R C2— TZ*BS X* —CB

NEXT OP1 ADR TO SAR
TEST FOR NON-ZERO
BYTE STORED IN
OP1 FIELD

GO TO END ROUTINE
11 — 0683
R G1<0 E3— LB=0 ** —EC

X1 — 063B
D D→M
R S2 E4— 1 *1 —ED

NEXT OP1 WD TO M
BR ON OP2 FETCH
RQD (CASE 2)

BRANCH ON
—ALL BYTES PROCESSED
—LAST BYTE IN L PROCESSED

QP830 — ECE
(00,01,10,11)
TO END ROUTINE

BRANCH ON MOVE (CHAR) INSTR

NOTE — OP1 FETCH NOT REQUIRED FOR MOVE INSTR

QP830.QDE
(01,10,11)
FROM END
ROUTINE

BRANCH ON
A—OP2 FETCH REQD
OR NOT MOVE
B—MOVE (CHAR)

01 — 060D
E 1000
A H+4→H
B LLB→U MMB→V
B ?→W
B W→MMB
D G-1
D LB,MB+1
C E→BS
R BQ(A=1)→B
R G<4 J2— LB=3 ** —JB

PROCESS A BYTE
OP1 ADR + 4 TO H
BRANCH ON
—LAST BYTE OF L,
—4 OR LESS BYTES
REMAINING IN
OP2 FIELD

00 — 0680
A R+4→R,A
B LLB→U MMB→V
B ?→W
B W→MMB
D G-1
D LB,MB+1
C 1→BS*MB
R AQ(B=1)→A
R 0 J3— LB=3 ** —JC

PROCESS A BYTE
NEXT OP2 ADR
TO SAR, R
BR ON LAST
BYTE OF L

00 — 0684
B LLB→U MMB→V
B ?→W
B W→MMB
D G-1
D LB,MB+1
C 1→BS*MB
R 1 J4— LB=3 1* —JD

PROCESS A BYTE
BR ON LAST
BYTE OF L

10 — 0686
B LLB→U MMB→V
B ?→W
B W→MMB
D D→L
D G-1
D LB,MB+1
C 1→BS*MB
J5— 11 —JE

PROCESS A BYTE
NEXT OP2 WORD
TO L

00 — 0688
B LLB→U MMB→V
B ?→W
B W→MMB
D G-1
D LB,MB+1
C 1→BS*MB
R MB=3 J6— 1 *1 —JF

PROCESS A BYTE
BR ON M FILLED

01 — 0689
A H→A
B LLB→U MMB→V
B ?→W
B W→MMB
D G-1
D LB,MB+1
C 1→BS*MB
R MB=3 J7— *X —JG

PROCESS A BYTE
OP1 ADR TO SAR
BR ON M FILLED

0X — 0635
B LLB→U MMB→V
B ?→W
B W→MMB
D G-1
D LB,MB+1
C 1→BS*MB
J8— 1X —JH

PROCESS A BYTE

FETCH NEXT OP2 WD
01 — 0681
A R+4→R,A
N3— 11 —NC

OP2 ADR + 4 TO SAR, R

11 — 0687
D D→L
R BQ(A=1)→B
R S1 N5— 0 ** —NE

NEXT OP2 WORD TO L
BRANCH ON CASE 1
(CASE 1 BR TAKEN
ON FIRST PASS IF
STORE REQD)

STORE OP1 BYTES
11 — 068B
A H→A
N7— 1X —NG

OP1 ADR TO SAR

1X — 0637
A M→D*BS
R AQ(B=0)→A
R 0 N9— MD=0 ** —NI

STORE COMPLETED
OP1 BYTES

CASE 2
FETCH NEXT OP2 WD
11 — 060F
E 0000
A H+4→H
C E→BS
Q2— 01 —QB

OP1 ADR + 4 TO H

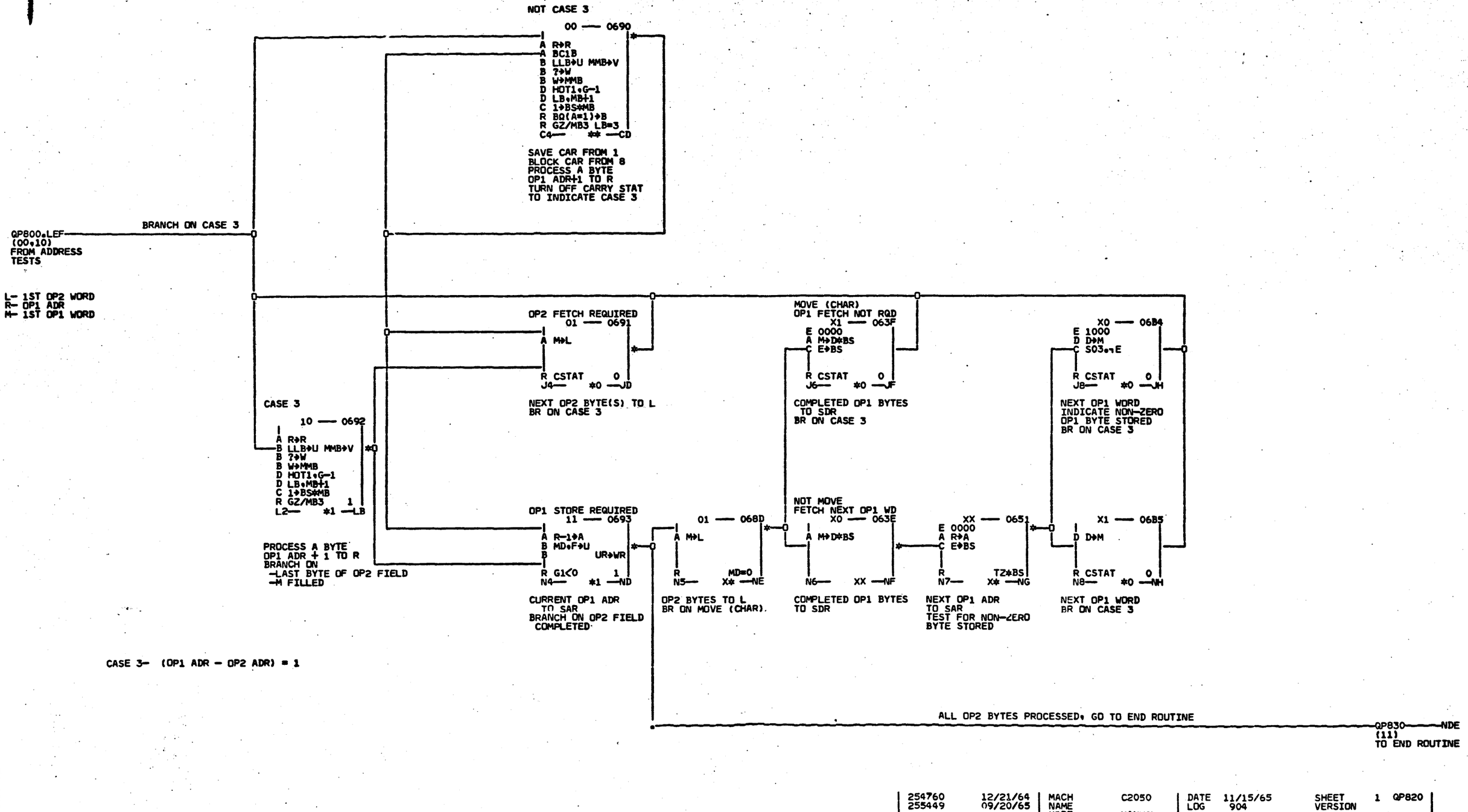
QP830 — QBE
(01)
TO END ROUTINE

QP800.LIE
(11)

QP800.GIE
(1X)

QP810

254760	12/21/64	MACH	C2050	DATE 11/15/65	SHEET 1 QP810
255449	09/20/65	NAME		LOG 904	VERSION
		MODE	MANUAL	LOGICAL AND MOVE INSTR (SS)	
		P.N.	5364803	MAIN LOOP	
		IBM CORP.	SDD		



CASE 3— (OP1 ADR — OP2 ADR) = 1

QP820

254760	12/21/64	MACH	C2050	DATE 11/15/65	SHEET 1 QP820
255449	09/20/65	NAME		LOG 904	VERSION
		MODE	MANUAL		
		P•N•	5364804	LOGICAL AND MOVE INSTR (SS)	
		IBM CORP•	SDD	OVERLAP ROUTINE	

REGISTERS—
L— OP2
R— OP2 ADR
M— OP1
H— OP1 ADR

1

QP800•LGF
(00•01•10•11)
FROM LENGTH
TEST

00 — 0694
B LLB→U MMB→V
B ?→W
B W→MMB
D G-1
D LB•MB+1
C 1→BS+MB
R GZ/MB3 LB=3
C2— ** —CB

PROCESS A BYTE
BRANCH ON—
—LAST BYTE OR
M FILLED
—LAST BYTE OF L

QP810•QBE
(01)
FROM MAIN LOOP
CASE 2

FETCH NEXT OP2 WORD
01 — 0695
A R+4→R•A
G2— XX —GB

OP2 ADR + 4 TO SAR• R

XX — 0682
D D→L
G4— 00 —GD

NEXT OP2 WORD

QP810•ECE
(00•01•10•11)
FROM MAIN LOOP

QP820•NDE
(11)
FROM OVERLAP
ROUTINE

STORE COMPLETED BYTES
10 — 0696
A H→A
B MD•F→U
B UR→WR
R BQ(A=1)→B
R G1<0 0
L2— ** —LB

OP1 ADR TO SAR
F TO MVR LTH TO
TEST FOR LOG INSTR
BRANCH OUT IF ALL
BYTES HAVE BEEN
PROCESSED

CASE 2
STORE COMPLETED BYTES
11 — 0697
E 0010
A H→A
B MD•F→U
B UR→WR
C S030E
R BQ(A=1)→B
R G1<0 0
Q2— ** —QB

OP1 ADR TO SAR
F TO MVR LTH TO
TEST FOR LOG INSTR
TN ON S2 FOR CASE 2
BRANCH OUT IF ALL
BYTES PROCESSED

FIELD COMPLETED
11 — 068F
A M→D*BS
R AQ(B=1)→A
R SO WR=0
L4— ** —LD

STORE COMPLETED BYTES
BRANCH ON
—NO ZERO BYTES STORED
PRIOR TO THIS STORE
—LOGICAL INSTR

FIELD NOT COMPLETED
00 — 068C
A M→D*BS
R AQ(B=0)→A
R S2 MD=0
Q4— ** —QD

COMPLETED OP1 BYTES
TO SDR

NOT LOGICAL INSTR
DONT CHANGE COND CODE
11 — 069B
C NOP
C6— 1X —CF

PREVIOUS OP1 BYTES
WERE ALL ZEROS
TEST BYTES NOW BEING STORED
10 — 069A
R 0 T2*BS
L6— 0* —LF

AT LEAST ONE NON-
ZERO BYTE STORED
IN OP1 FIELD
00 — 0698
E 0001
C E(23)→CR
G8— 1X —GH

01 TO PSW(34•35)

ALL ZEROS STORED
IN OP1 FIELD
01 — 0699
E 0000
C E(23)→CR
L8— 1X —LH

00 TO PSW(34•35)

QT100 —LHE
(1X)
TO I-FETCH

BRANCH ON—
—CASE 2
—MOVE INSTR

QP810 —QDE
(01•10•11)

254760	12/21/64	MAIN	C2050	DATE 11/18/65	SHEET 1 QP830
255449	09/20/65	NAME		LOG 904	VERSION
		MODE	MANUAL		
		PAT	5344605	LOGICAL AND MOVE INSTR (SS)	

QP830

QB500.SCD (1X)

QB750.CCE (1X)

QE555.CEE (1X)

QE802.JHE (1X)

QF100.AAE (1X)

QG409.JHE (1X)

QK222.QCE (1X)

QK300.JDE (1X)

QK555.QDE (1X)

QK666.AEE (1X)

QK702.LGE (1X)

QP102.AHE (1X)

QP206.JDD (1X)

QP830.LHE (1X)

QP900.GIE (1X)

QS120.NBE (1X)

QS120.NIE (1X)

QS500.SBE (1X)

QS601.ABF (1X)

QY140.QHE (1X)

1X — 0197

E 1110
L WS•E→LSA
*L LS→L→LS
S IA+0/2→A
C E→S47
R I-FETCH
J7— ** —JG
EXCPNQIA(30)→A
EXCPNQ(IA(30)•REF)→B

OP BUF TO L
IAR TO SAR
SET STATS 4-7

QT110 —JGE (00,01,10,11)
SECOND CYCLE
OF I-FETCH

2 - 7 closed at

QT100

254760	12/21/64	MACH	C2050	DATE 11/15/65	SHEET 1 QT100
255449	09/20/65	NAME		LOG 904	VERSION
		MODE	MANUAL	INSTRUCTION FETCH	
		P•N•	5364831	FIRST CYCLE	
		IBM CORP•	SDD		

4

QA500.QCE (00.01.10.11)

QB100.GCD (00.01.10.11)

QB400.LFE (00.01.10.11)

QB500.NCE (00.01.10.11)

QB801.LCE (00.01.10.11)

QB902.QGE (00.01.10.11)

QE100.AAE (00.01.10.11)

QE580.AFE (00.01.10.11)

QG100.NHE (00.01.10.11)

QG200.JCE (00.01.10.11)

QG408.AEE (00.01.10.11)

QG409.QCE (00.01.10.11)

QG503.JEE (00.01.10.11)

QG702.QED (00.01.10.11)

QG801.JCF (00.01.10.11)

QG804.NDE (00.01.10.11)

QG902.JGE (00.01.10.11)

QP900.LHD (00.01.10.11)

QS118.AID (00.01.10.11)

QS202.SGE (00.01.10.11)

ENTRIES TO THIS PAGE
HAVE DONE IAR TO SAR
BUT NOT OTHER FUNCTIONS
OF FIRST CYCLE
THIS FREE ENTRY SAVES
ONE CYCLE UNLESS
OFF BOUNDS

IAR TO SAR WAS INHIBITED
BY SMIF IF OFF BOUNDS

ON BOUNDS
10 — 0146
E 1111
B W→G
*C E(23)→LSFN
R 1 IVA
C7— 1* —CG
ZERO TO G
SET LS FN REG
TO GEN REG

QT115 —CGE
(10) CONTINUE
I-FETCH
(11) INVALID
ADDRESS

OFF BOUNDS
00 — 0144
E 1110
L WS→E→LSA
L LS→L→LS
S IA+0/2→A
C E→S47
R I-FETCH
G7— ** —GG
EXCPNΩIA(30)→A
EXCPNΩ(IA(30)•REF)→B

MUST BRING OP BUF
TO L, THEN READY
FOR SECOND CYCLE

QT110 —GGE
(00.01.10.11)
I-FETCH
SECOND CYCLE

REFETCH
01 — 0145
E 1111
B W67→LB
D 3→MB
C E(23)→LSFN
R AΩ(B=1)→A
R 0 IVA
L7— ** —LG
SET LS FN REG
TO GEN REG
SET LB=0,MB=3

QT115 —LGE
(00) REFETCH
(11) INVALID
ADDRESS

EXCEPTION
11 — XXX
GO TO
QT200.JBE

Q9— 11 —QI

254760	12/21/64	MACH	C2050	DATE 11/15/65	SHEET 1	QT105
255449	09/20/65	NAME		LOG 904	VERSION	
		MODE	MANUAL			
		P.N.	5364912	INSTRUCTION FETCH		
		IBM CORP.	SDD	FREE ENTRY		

QT100.JGE
(00.01.10.11)
FIRST CYCLE
OF I-FETCH

1

QA400.CCE
(00.01.10.11)

QA700.ADE
(00.01.10.11)

QA800.QIE
(00.01.10.11)

QB100.LEE
(00.01.10.11)

QB500.AEE
(00.01.10.11)

QB730.JEE
(00.01.10.11)

QB801.CCE
(00.01.10.11)

QB902.LGE
(00.01.10.11)

QG100.EME
(00.01.10.11)

QG300.QCE
(00.01.10.11)

QG406.LDE
(00.01.10.11)

QG408.LIE
(00.01.10.11)

QG409.ABE
(00.01.10.11)

QG416.GBD
(00.01.10.11)

QG503.AEE
(00.01.10.11)

QG702.ECE
(00.01.10.11)

QG804.JFE
(00.01.10.11)

QJ080.JGE
(00.01.10.11)

QJ090.EGE
(00.01.10.11)

QJ110.LHE
(00.01.10.11)

QJ130.NGE
(00.01.10.11)

QJ140.CHE
(00.01.10.11)

QJ600.AFE
(00.01.10.11)

QK555.AGE
(00.01.10.11)

QK701.CEE
(00.01.10.11)

QK702.AHE
(00.01.10.11)

QK705.JHD
(00.01.10.11)

QP100.EHE
(00.01.10.11)

QP102.GAE
(00.01.10.11)

QP206.EDD
(00.01.10.11)

QP900.QFD
(00.01.10.11)

QS120.EHE
(00.01.10.11)

QS202.NGE
(00.01.10.11)

QS308.NFE
(00.01.10.11)

QS406.EFD
(00.01.10.11)

QT105.GGE
(00.01.10.11)
FREE ENTRY
TO I-FETCH

QE901.ECF
(00.01.10.11)

QY110.QHE
(00.01.10.11)

10 — 014A
E 1111
B W→G
C E(23)→LSFN
R 1
C7—
IVA
1* —CG

QT115——CGE
(10) CONTINUE
I-FETCH
(11) INVALID
ADDRESS

00 — 0148
E 1111
A LRL→ML.JK
B W67→LB
D 3→MB
C E(23)→LSFN
R BQ(A=1)→B
R 1SYLS
IVA
G7—
** —GG

QT115——GGE
(00.01.11)
CONTINUE
I-FETCH

L23→XG01
T→L.M 0→REFETCH
T(12-15)→J
T(16-19)→MD
(X=0)→S0
(B=0)→S1
SET ILC.1SYL

01 — 0149
E 1111
B W67→LB
D 3→MB
C E(23)→LSFN
R AQ(B=1)→A
R 0
IVA
L7—
** —LG

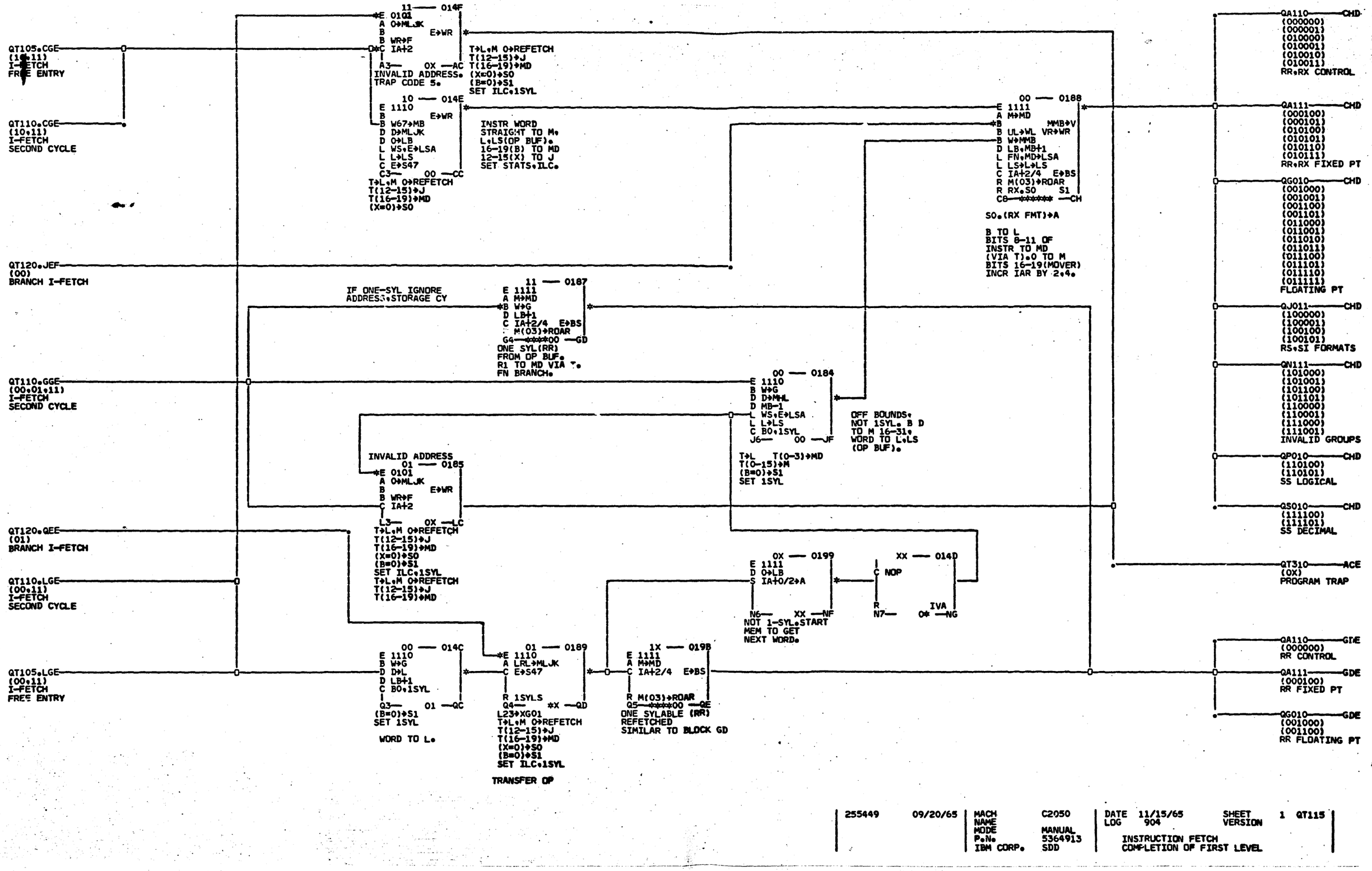
QT115——LGE
(00) REFETCH
(11) INVALID
ADDRESS

11 — XXX
GO TO
QT200.NBE

Q9—
11 —QI

[redacted] 254760 255449	[redacted] 12/21/65 9/20/65	MACH NAME MODE P.N. IBM CORP.	C2050 MANUAL 5364832 SDD	DATE 11/15/65 LOG 904	SHEET 1 QT110 VERSION

INSTRUCTION FETCH
SECOND CYCLE



255449	09/20/65	MACH	C2050	DATE	11/15/65	SHEET	1 QT115
		NAME		LOG	904	VERSION	
		MODE	MANUAL				
		P.N.	5364913				
		IBM CORP.	SDD				

INSTRUCTION FETCH
COMPLETION OF FIRST LEVEL

QT115