IBM

Field Engineering Maintenance Manual

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2025 Processing Unit

Y24-3528-1

Preface

This manual contains maintenance and service information for the IBM 2025 Processing Unit and integrated attachment circuitry.

The manual assumes knowledge of the System/360 as described in IBM System/360 Principles of Operation, Form A22-6821, and the following appropriate FE Theory of Operation Manuals:

Form No.	Subject
Y24-3527	CPU
Y24-3531	Channel Attachment
Y24-3532	2540 Attachment
Y24-3533	1403 Attachment
Y24-3534	2311 Attachment
Y24-3535	2560 Attachment
Y24-3536	Integrated Communications Attachment

Additional maintenance information can be found in the Symptom Index and Service Aids distributed by FE Technical Operations. Installation instructions, part 5870298, are included in the basic shipping group for each machine.

This manual contains references to diagrams in the Field Engineering Maintenance Diagrams Manual, 2025 Processing Unit, Form Y24-3529. These references use only the initials of the Maintenance Diagrams Manual followed by the diagram section and number; e.g., MDM X-XX.

Second Edition (July 1969)

This edition, Y24-3528-1, is a major revision of and obsoletes Y24-3528-0. It also obsoletes FE Supplements Y24-0096 and Y24-0100. This publication has been revised completely with additions, deletions, and reformatting of existing material. For this reason, the reader should review this edition in its entirety.

Significant changes or additions to the specifications contained in this publication are continually being made. Any such changes will be reported in subsequent revisions or FE Supplements.

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Contents

Abbreviations

A	AND (logic block)
ac	alternating current
acv	active
addr	address
ALD	automated logic diagram
alg	algebraic
ALS	arithmetic and logic section
AMWP	bits 12-15 of PSW 1
AND	AND circuit (logic)
arith	arithmetic
AS	auxiliary storage
ASCII	American Standard Code for Information Interchange
atn	attention
Aux	auxiliary
B	base address (field)
BCD	binary coded decimal
B-cycle	base address cycle
BSM	basic storage module
BTU	British Thermal Unit
CAR	channel address register
CAW	channel address word
CB	circuit breaker
CBA	channel background activity
C-bit	carry bit
CC	chain command; condition code compute clock
CCC	channel control check
CCW	channel command word
C-cycle	control cycle
CD	chain data
CDR	channel data register
CE	channel end; customer engineer
chan	channel
char	character
chk	check
chnl	channel
CI	command immediate
CLA	carry look-ahead
CLI	compare logical immediate
clk	clock
clr	clear
CLT	circuit level test
cmnd	command
cmpt	compute
COAR	command address register
com	common
comm	communications
comp	compare
compl	complement
cond	condition
corrn	correction
CP	main clock pulse
CPU	central processing unit
CSL	control storage load
CSU	core storage unit
ct	count
ctr	counter
CU	control unit
cyc	cycle
C0	carry zero
D	displacement (field)
DAC	disk attachment control
DAR	data address register
dbl	double
dc	direct current
DDC	direct data channel
DE	device end
dec	decimal
decond	deconditioned
decr	decrement
Diag	diagnostic
DIR	direct in register
div	divide
dly	delay, delayed
DM	diagnostic monitor
DOR	direct out register
Dply	display
DR	driver (logic block)
Dsply	display
dvd	dividend
dvr	divisor
EA	effective address
EA-cycle	effective address cycle
EBCDIC	extended binary coded decimal interchange code
EC	engineering change
ECAD	error check analysis diagram
ef	effective
End Ex	end execute
EOB	end of block
EPO	emergency power off
E-phase	execute phase
Eq	equal
EXOR	exclusive OR
excpn	exception
exec	execute
exp	exponent
ext	external
extn	extension
FEMDM	Field Engineering Maintenance Diagram Manual
FEMM	Field Engineering Maintenance Manual
FETOM	Field Engineering Theory of Operation Manual
FF	flip-flop (logic block)
FL	flip latch (logic block)
fltg	floating
FP	floating point
FPA	floating point arithmetic
FPR	floating point register
GPR	general purpose register
hex	hexadecimal
HI	high
hsmpx	high-speed multiplex channel

H/stop	hard stop
HW	hardware (funnel)
Hz	Hertz (cycles per second)
IB	interrupt buffer
IC	instruction counter
ICC	interface control check
I-cycle	instruction cycle
IF	interface
I-fetch	instruction fetch
IL	incorrect length
ILC	instruction length code
incr	increment
info	information
inh	inhibit
insn	instruction
int	interrupt
intch	interchange
intv	interval
intvn	intervention
inv	invert
I/O	input/output
IPL	initial program loading
IR	interrupt request
ISA	invalid storage address
I-time	instruction time
KB	keyboard
kva	kilovolt ampere
LCW	line control word
LO	low
log	logical
LS	local storage
lth	latch
LUA	load unit address (switches)
mA	milliamperes
Man	manual
MAP	maintenance analysis procedure
MAS	microprogram automation system
max	maximum
MC	machine check
MDM	Maintenance Diagrams Manual
MFCM	Multi-Function Card Machine
MHz	megacycle
min	minimum
MMSK	Trap (Mask) Priority Register
mped	multiplicand
mplr	multiplier
Mplx	multiplexer
mply	multiply
mpx	multiplexer
MS	main storage
ms	millisecond
N	inverter (logic block)
neg	negative
no	number
No-Op	no operation
norm	normalize
ns	nanosecond
OE	exclusive OR (logic block)
oflo	overflow
O/L	overload (console)
op	operation
opnd	operand
OR	OR circuit (logic)
OS	operating system
OSC	oscillator (logic)
P	parity bit
PC	parity check
Pch	punch
PCI	program controlled interrupt
PFR	punch feed read
PG	parity generation
PIW	priority interrupt wait
PLB	print line buffer
pos	positive
poss	possible
prgm	program
prgm chk	program check
pri	priority
priv	privileged
PR-KB	printer-keyboard
prot	protection
Prt	printer
PS	power supply (number)
PSA	protected storage address
PSW	program status word
pt	point
pty	parity
Pwr	power
PZR	possible zero remainder
QB	quotient bit
quot	quotient
RC	read clock
Rdr	reader
recomp	recomplement
reg	register
req	request
reqd	required
res	reset
rgen	regenerate
rmdr	remainder
rms	root mean square
RPQ	request for price quotation
RR	register-to-register operation
RS	register-to-storage operation
Rst	reset
rt	right
Rtn	return, routine
R-W	read-write
S	sign bit
SAR	storage address register
SC	shift counter
sc	scratch (register)
SCR	silicon controlled rectifier
SCT	system configuration table
SCh	subchannel
SDR	storage data register
SDSD	single disk storage drive
sel	select
seq	sequence
serv	service
sgnf	significance, significant
SI	storage immediate operation
SL	shift left
SLD	simplified logic diagram
SLI	suppress incorrect length indication

SLT	solid logic technology
SMS	standard modular system
spl	special
SR	shift right
SRETL	screened resistor etched transistor logic
SRP	serial reader punch
SS	storage-to-storage operation, singleshot
st	start
STP0	storage protect register
STP1	storage protect local storage
STP	storage protect
subt	subtract
svc	supervisor call
sw	switch
sys	system
TB	terminal board
T-cycle	timer cycle
TD	time delay (logic)
Temp	temperature
TH	thermal (console)
TIC	transfer in channel
tmr	timer
tgr	trigger
TP	test point
T/R	tilt/rotate
T/XC	true/criss-cross
UCW	unit control word
UDT	unit definition table
uflo	underflow
un	unnormalized
unobt	unobtainable
usec	microsecond
WC	write clock
wd	word
WLR	wrong length record
X	index (field)
X-cycle	index cycle

The following symbols are used with microword statements:

$ OR
- Minus
+ Add
*- Complement AND
¤ Exclusive OR.

Safety

CE SAFETY PRACTICES

All Customer Engineers are expected to take every safety precaution possible and observe the following safety practices while maintaining IBM equipment:

1. You should not work alone under hazardous conditions or around equipment with dangerous voltage. Always advise your manager if you MUST work alone.
2. Remove all power AC and DC when removing or assembling major components, working in immediate area of power supplies, performing mechanical inspection of power supplies and installing changes in machine circuitry.
3. Wall box power switch when turned off should be locked or tagged in off position. "Do not Operate" tags, form 229-1266, affixed when applicable. Pull power supply cord whenever possible.
4. When it is absolutely necessary to work on equipment having exposed operating mechanical parts or exposed live electrical circuitry anywhere in the machine, the following precautions must be followed:
   a. Another person familiar with power off controls must be in immediate vicinity.
   b. Rings, wrist watches, chains, bracelets, metal cuff links, shall not be worn.
   c. Only insulated pliers and screwdrivers shall be used.
   d. Keep one hand in pocket.
   e. When using test instruments be certain controls are set correctly and proper capacity, insulated probes are used.
   f. Avoid contacting ground potential (metal floor strips, machine frames, etc. — use suitable rubber mats purchased locally if necessary).
5. Safety Glasses must be worn when:
   a. Using a hammer to drive pins, riveting, staking, etc.
   b. Power hand drilling, reaming, grinding, etc.
   c. Using spring hooks, attaching springs.
   d. Soldering, wire cutting, removing steel bands.
   e. Parts cleaning, using solvents, sprays, cleaners, chemicals, etc.
   f. All other conditions that may be hazardous to your eyes. REMEMBER, THEY ARE **YOUR** EYES.
6. Special safety instructions such as handling Cathode Ray Tubes and extreme high voltages, must be followed as outlined in CEM's and Safety Section of the Maintenance Manuals.
7. Do not use solvents, chemicals, greases or oils that have not been approved by IBM.
8. Avoid using tools or test equipment that have not been approved by IBM.
9. Replace worn or broken tools and test equipment.
10. Lift by standing or pushing up with stronger leg muscles — this takes strain off back muscles. Do not lift any equipment or parts weighing over 60 pounds.
11. All safety devices such as guards, shields, signs, ground wires, etc. shall be restored after maintenance.
12. Each Customer Engineer is responsible to be certain that no action on his part renders product unsafe or exposes hazards to customer personnel.
13. Place removed machine covers in a safe out-of-the-way place where no one can trip over them.
14. All machine covers must be in place before machine is returned to customer.
15. Always place CE tool kit away from walk areas where no one can trip over it (i.e., under desk or table).
16. Avoid touching mechanical moving parts (i.e., when lubricating, checking for play, etc.).
17. When using stroboscope — do not touch ANYTHING — it may be moving.
18. Avoid wearing loose clothing that may be caught in machinery. Shirt sleeves must be left buttoned or rolled above the elbow.
19. Ties must be tucked in shirt or have a tie clasp (preferably nonconductive) approximately 3 inches from end. Tie chains are not recommended.
20. Before starting equipment, make certain fellow CE's and customer personnel are not in a hazardous position.
21. Maintain good housekeeping in area of machines while performing and after completing maintenance.

KNOWING SAFETY RULES IS NOT ENOUGH
AN UNSAFE ACT WILL INEVITABLY LEAD TO AN ACCIDENT
USE GOOD JUDGMENT — ELIMINATE UNSAFE ACTS

229-1264-1

Artificial Respiration

GENERAL CONSIDERATIONS

1. **Start Immediately, Seconds Count**
   Do not move victim unless absolutely necessary to remove from danger. Do not wait or look for help or stop to loosen clothing, warm the victim or apply stimulants.
2. **Check Mouth for Obstructions**
   Remove foreign objects — Pull tongue forward.
3. **Loosen Clothing — Keep Warm**
   Take care of these items after victim is breathing by himself or when help is available.
4. **Remain in Position**
   After victim revives, be ready to resume respiration if necessary.
5. **Call a Doctor**
   Have someone summon medical aid.
6. **Don't Give Up**
   Continue without interruption until victim is breathing without help or is certainly dead.

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Rescue Breathing for Adults
Victim on His Back Immediately

1. **Clear throat** of water, food, or foreign matter.
2. **Tilt head back** to open air passage.
3. **Lift jaw up** to keep tongue out of air passage.
4. **Pinch nostrils** to prevent air leakage when you blow.
5. **Blow** until you see chest rise.
6. **Remove your lips** and allow lungs to empty.
7. **Listen** for snoring and gurglings, signs of throat obstruction.
8. **Repeat mouth to mouth breathings** 10-20 times a minute.

Continue rescue breathing until he breathes for himself.


Thumb and finger positions


Final mouth to mouth position

Chapter 1. Reference Data and Diagnostic Techniques

Section 1. Reference Data

This section contains charts, listings, and diagrams giving general information for diagnosing system failures.

1.1 CORE STORAGE (FIGURES 1-1 THROUGH 1-17)

Hex Address	Decimal Address	Length	Purpose
0	0	Doubleword	Initial program-loading PSW
8	8	Doubleword	Initial program-loading CCW1
10	16	Doubleword	Initial program-loading CCW2
18	24	Doubleword	External old PSW
20	32	Doubleword	Supervisor-call old PSW
28	40	Doubleword	Program old PSW
30	48	Doubleword	Machine-check old PSW
38	56	Doubleword	Input/output old PSW
40	64	Doubleword	Channel-status word
48	72	Word	Channel-address word
4C	76	Word	Not used
50	80	Word	Timer
54	84	Word	Not used
58	88	Doubleword	External new PSW
60	96	Doubleword	Supervisor-call new PSW
68	104	Doubleword	Program new PSW
70	112	Doubleword	Machine-check new PSW
78	120	Doubleword	Input/output new PSW
80-9F	128-159	----------	Diagnostic scan-out area, beginning at address 128.

Figure 1-1. Permanent Storage Assignments

16K Systems

Addrs	Usage	Aux Stor	Array
7FFF 4000	Control Storage	2048 Bytes	32K
3FFF 0000	Program Storage	(see text)	

24K Systems

Addrs	Usage	Aux Stor	Array
BFFF 8000	Control Storage	2560 Bytes	16K
5FFF 0000	Program Storage	(see text)	24K

Note: Addresses 6000-7FFF are not available in the 24K M2-I storage array.

32K Systems

Addrs	Usage	Aux Stor	Array
BFFF 8000	Control Storage	3072 Bytes	16K
7FFF 0000	Program Storage	(see text)	32K

48K Systems

Addrs	Usage	Aux Stor	Array
FFFF C000	Control Storage	4096 Bytes	32K
BFFF 8000	Program Storage (High)	(see text)	
7FFF 4000	Program Storage (Mid)		32K
3FFF 0000	Program Storage (Low)		

Figure 1-2. Addressing Ranges for Program Storage, Control Storage, and Auxiliary Storage

System Size	Program Storage			Control Storage			Auxiliary Storage	
	Array Size	Bytes	Addrs Range (Decimal/Hex)	Array Size	Bytes	Addrs Range (Decimal/Hex)	Bytes	Addrs Range (Decimal/Hex)
16K	32K Low half	16,384	0-16, 383 0000 - 3FFF	32K High half	16,384	16,384 - 32,767 4000 - 7FFF	2,048	0x 00-7xFF
24K	24K All	24,576	0-24, 575 0000-5FFF	16K All	16,384	32,768 - 49,151 8000 - BFFF	2,560	0x00-5xFF and 8x00-BxFF
32K	32K All	32,768	0-32, 767 0000-7FFF	16K All	16,384	32,768-49,151 8000-BFFF	3,072	0x00-BxFF
48K	32K(1) All Plus 32K(2) Low half	49,152	0-49, 151 0000-BFFF	32K(2) High half	16,384	49,152-65,535 C000-FFFF	4,096	0x00-FxFF

Notes:
1. Program storage is always located in the low-order area of the composite core-storage array(s). For example, program storage for the 48K system is all of the low-order 32K unit plus the low-order 16K bytes of the high-order 32K unit.
2. Control storage is always the high-order 16K bytes of the composite core-storage array(s).
3. The notation 0x00-7xFF, etc. in the AUX STOR ADDRS RANGE column is defined in section 1.2.

Figure 1-3. Core-Storage Allocations and Addressing Scheme

1.1.1 TRAP ADDRESSES

When a microprogram trap occurs, the control-storage address of the routine is forced into the storage address assembler. The trap microprograms are located at the following fixed locations. The trap addresses given are relative to control-storage address 0000, and this location is 4000 for 16K systems, 8000 for 24K or 32K systems, or C000 for 48K systems.

Trap Address	Trap Routine
0010	CSL
0240	System reset or IPL
0220	Machine check
0280	FE trap
0210	Storage-wrap error, or storage protect violation
0170	Channel high priority
0140	File chaining
0180	Channel low priority
01B0	2540 reader
0110	2540 punch
01E0	Communications channel bit service
0120	Communications channel character service

1.1.1.1 Address Stop/Match

It is not possible to address stop at the first word of a trap because trap addresses are forced directly to the storage address lines, and the address match function refers to the contents of the M-register. To address match on a trap, make the match on the address of the second word of the trap. The address of the second word of a trap is normally the trap address +2. An exception is the storage-wrap and storage-protect violation trap, where the first word can be a direct branch. The appropriate MAS listing should be used, in this case, to determine the address to be matched.

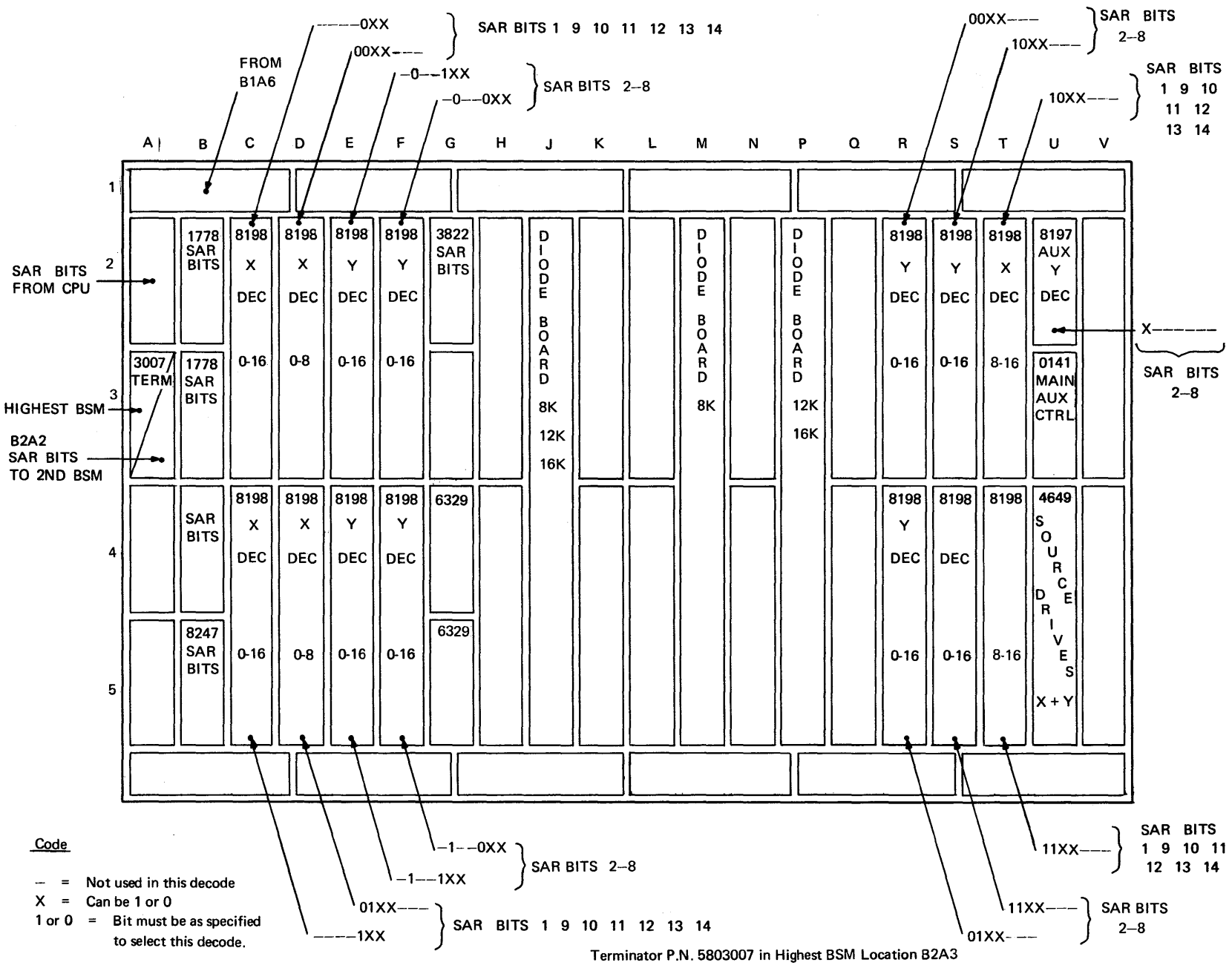


Figure 1-4. Core-Storage Plug Chart

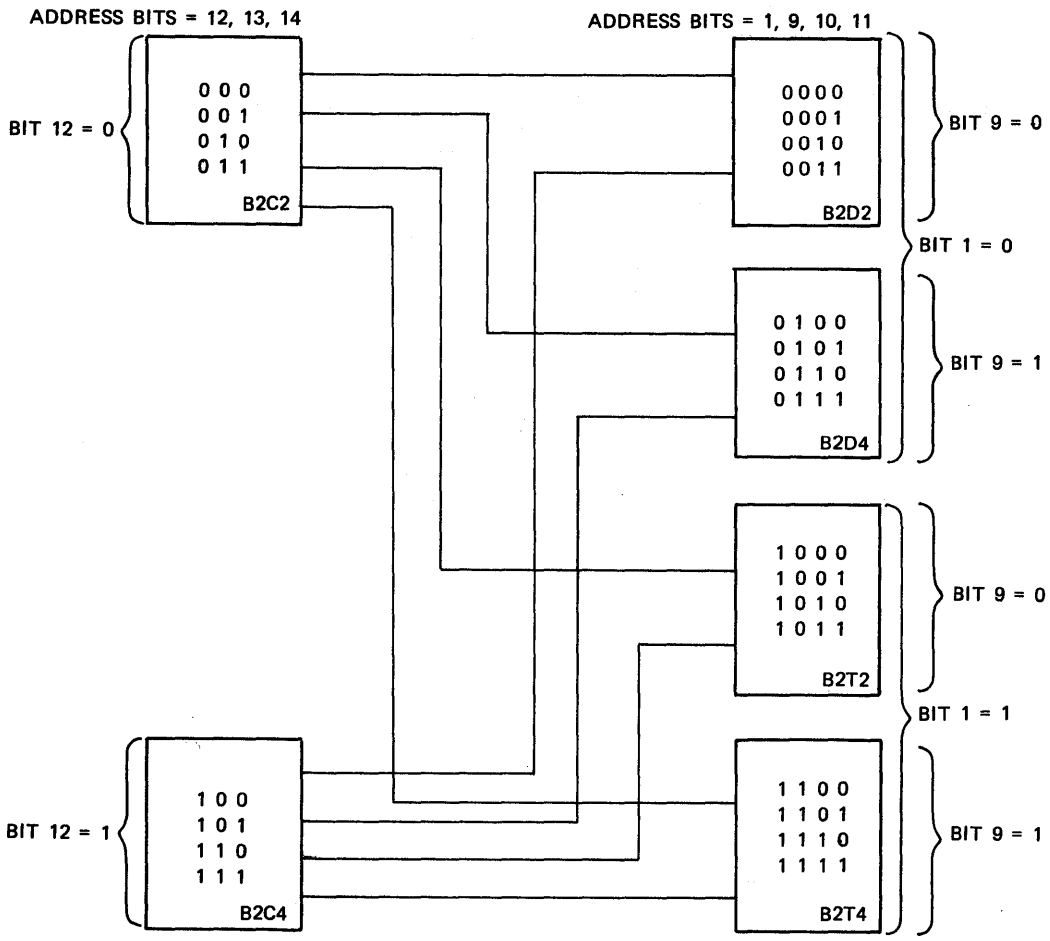


Figure 1-5. Core-Storage Y-Decodes

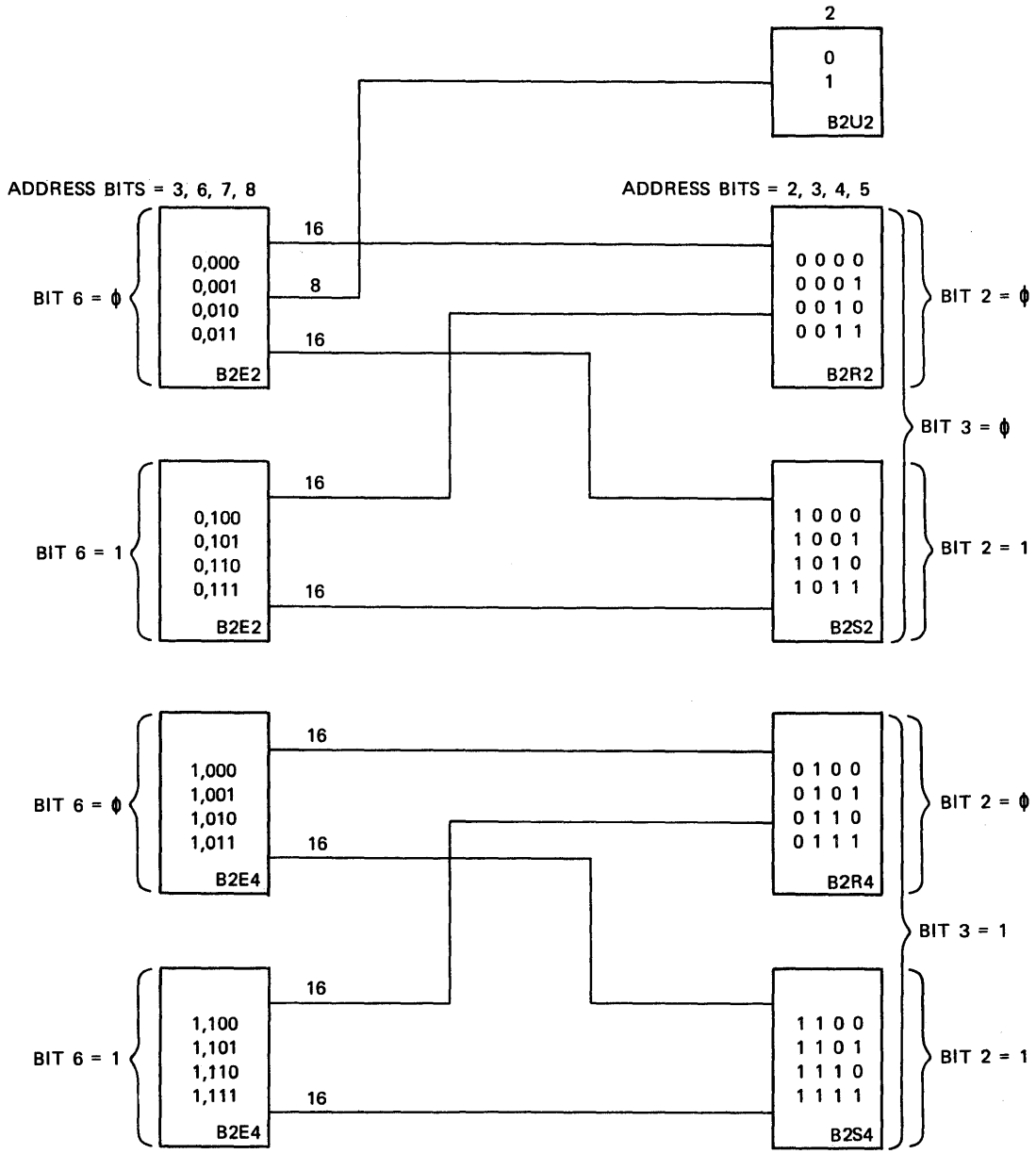


Figure 1-6. Core-Storage X-Decodes

1.2 AUXILIARY STORAGE MAPS (FIGURES 1-7 THROUGH 1-17)

Depending on the program-storage capacity of the system, there are from eight to sixteen 256-byte modules of auxiliary storage. Module 0 is used for CPU functions (general registers, etc.) and for storage of addresses and information relative to the integrated I/O attachment features. Module 2 is used for multiplexer-channel unit-control words. Modules 1 and 3-7 are used for operations involving the integrated attachment features. Modules 8-15 are reserved for special features. The 24K system (modules 6 and 7) is an exception (Figure 1-7).

Note: Three hexadecimal digits in the first, third and fourth positions of the storage address register are used to address auxiliary storage (the second hex character is not relevant).

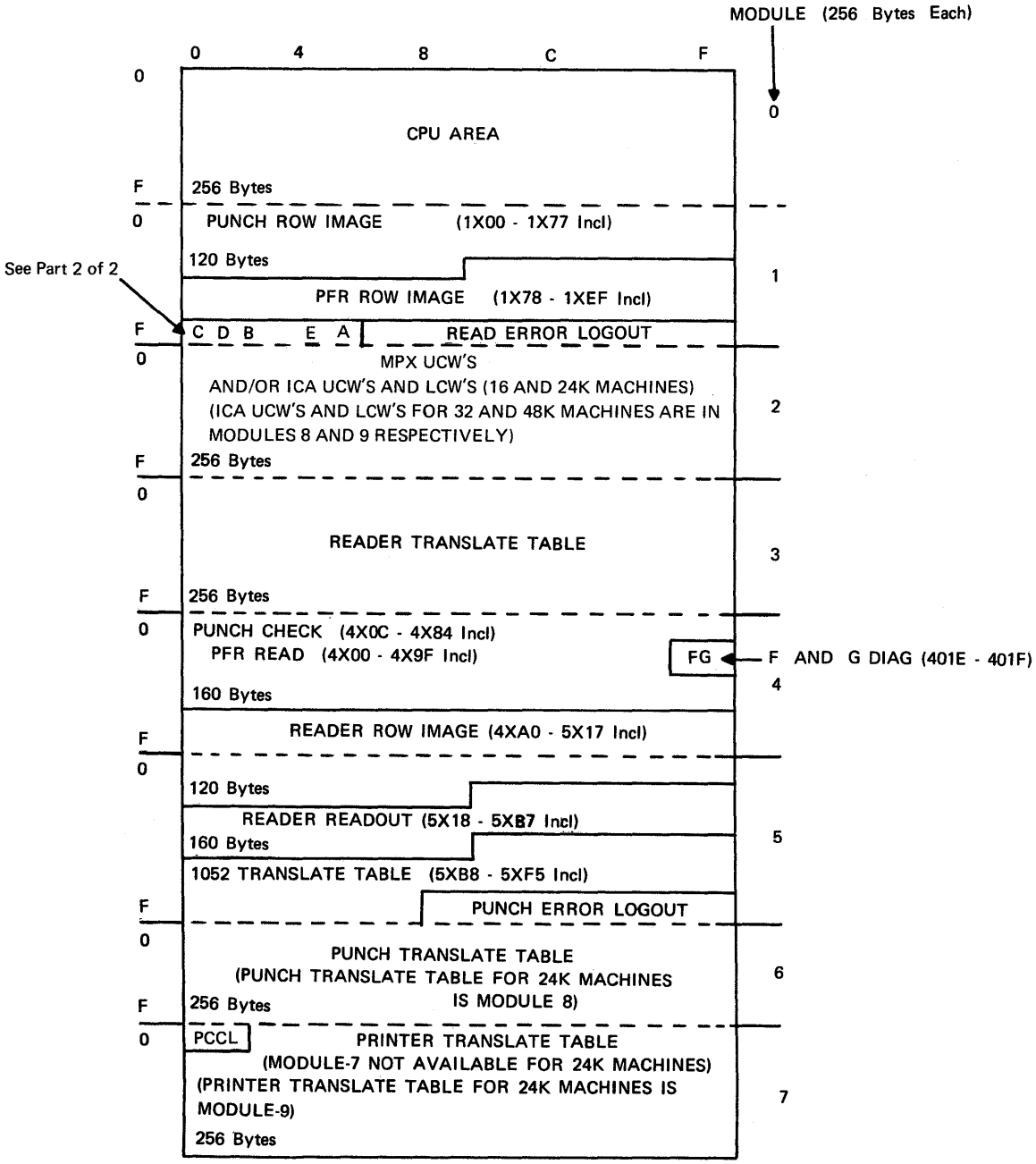
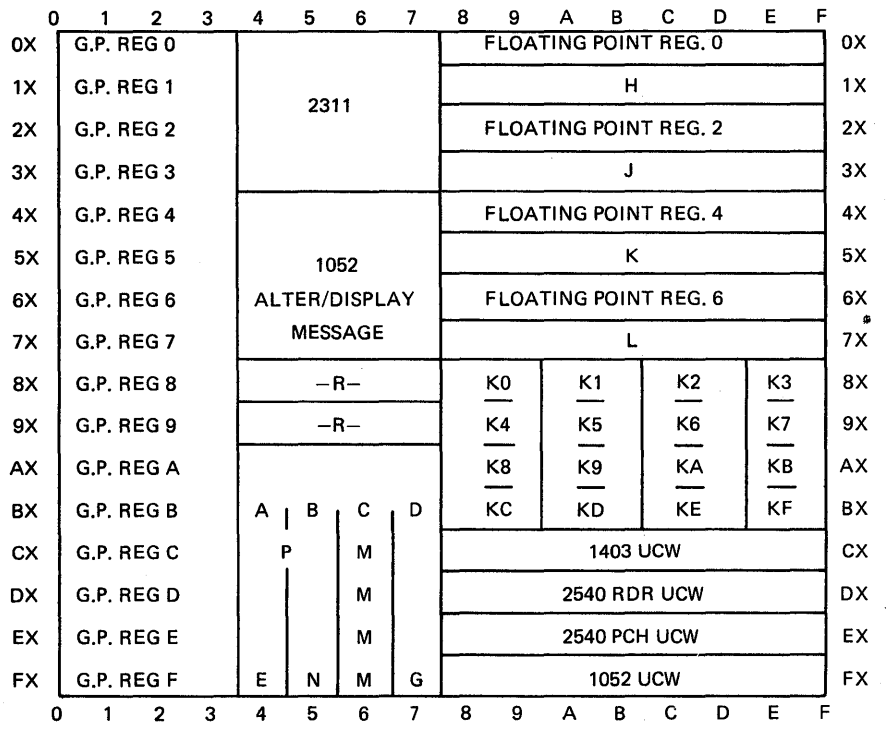


Figure 1-7. Auxiliary Storage Map (Part 1 of 2)

		BIT SIGNIFICANCE								
CODE	ROUTINES USING	0	1	2	3	4	5	6	7	USED FOR
A	ETRP-S	CMD REJ	NOT READY		EQUIP CHECK	VAL CHECK		UN-USUAL CMD		PUNCH SENSE
B	ETRP-S, ECOL-R		STACK SEL 1, 2, 3	STACK SEL 1, 2, 3						STACK SEL
C	EXFR-R	CDA	STACK SEL 1, 2, 3	STACK SEL 1, 2, 3		READ	CT STOR	FEED	WLR	READER INDICATOR
D	EXFR-R	CMD REJ	NOT READY		EQUIP CHECK	VAL CHECK		UN-USUAL CMD		READER SENSE
E	EPCH-R	CDA	STACK SEL 1, 2, 3	STACK SEL 1, 2, 3		PFR READ	CT STOR	PFR COUNT	WLR	PUNCH INDICATOR

Note: PCCL byte for 1403 translate table is kept in auxiliary storage 7x00 (9x00 for 24K machines).

Figure 1-7. Auxiliary Storage Map (Part 2 of 2)



A–––––1403 UNIT ADDRESS
B–––––READER UNIT ADDRESS
C–––––PUNCH UNIT ADDRESS
D–––––1052 UNIT ADDRESS
E–––––H1 SAVE
G–––––1052 SENSE
N–––––2311 ADDRESS

H–––––MULT/DVD TABLE (X1) AND ALT/DIS REGS BACKUP
J–––––MULT/DVD TABLE (X4) AND ALT/DIS BACKUP + FLPT SAVE
K–––––MULT/DVD TABLE (X16)
L––––– MULT/DVD TABLE (X64), FLPT SAVE
M––––– NATIVE KEY KKKK0000
P––––– COMMU. Q–EXIT POINTER
R–––––BURST CHANNEL BUFFERED DEVICE ADDRESSES.

K-ADDRESSABLE AREA

K0-88- CHANNEL 1 INTERRUPT BUFFER
KI-8A- STANDARD INTERFACE, NEXT CCW ADDRESS
K2-8C- CHANNEL UNIT ADDRESS BUFFER
K3-8E- STATUS/ACTIVE BYTE FOR 2311 OR CHANNEL 1
K4-98- 2311 NEXT CCW ADDRESS
K5-9A- 2311 SENSE OR PREVIOUS OP AND MASK
K6-9C- 2311 SENSE OR FILE ADDRESS
K7-9E DIAGNOSTICS, ALTER/DISPLAY BAL BACKUP
K8-A8- SYSTEM MASK -A9- CPU KEY AND AMWP
K9-AA- EXECUTE INSTRUCTION COUNTER––––– I REGISTER BACKUP
KA-AC- U REGISTER BACKUP Q FLPT SAVE DURING INSTRUCTIONS
KB-AE- G REGISTER BACKUP
KC-B8- P REGISTER BACKUP
KD-BA- CHANNEL 0 INTERRUPT BUFFER
KE-BC- ADDRESS OF STRAIGHT MULT/DVD, FLPT SAVE 2540 REGS BACKUP
KF-BE- ADDRESS OF SKEWED MULT/DVD, FLPT SAVE OR CAW KEY 2540 REGS BACKUP

Figure 1-8. Auxiliary Storage Module 0 (Part 1 of 2)

STANDARD DEVICE ADDRESSES

INTEGRATED	LOC	BURST CHANNEL	LOC
1403 ----------0E	B4	1443 or 1445 ----------0B	84
2540 RDR----------0C	B5	2540 RDR ----------0C	85
2540 PCH ----------0D	B6	2540 PCH ----------0D	86
1052 ----------1F	B7	1403 ----------0E	87
2311 ----------9X	F5	1404 or 2ND 1403 --------0F	94
Note:		2520 ----------15	95

The text preceding the –BCPL– Routine contains information on punching cards to reconfigurate the system to other than the standard assignments.

Figure 1-8. Auxiliary Storage Module 0 (Part 2 of 2)

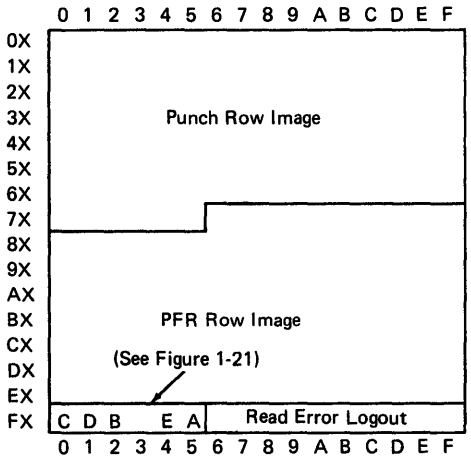


Figure 1-9. Auxiliary Storage Module 1

	x0	x2	x4	x6	x8	xA	xC	xE
0x	UCW	0, Addrs 000 or 080*			UCW 16, Addrs 010			
1x	UCW	1, Addrs 001 or 090*			UCW 17, Addrs 011			
2x	UCW	2, Addrs 002 or 0A0*			UCW 18, Addrs 012			
3x	UCW	3, Addrs 003 or 0B0*			UCW 19, Addrs 013			
4x	UCW	4, Addrs 004 or 0C0*			UCW 20, Addrs 014			
5x	UCW	5, Addrs 005 or 0D0*			UCW 21, Addrs 015			
6x	UCW	6, Addrs 006 or 0E0*			UCW 22, Addrs 016			
7x	UCW	7, Addrs 007 or 0F0*			UCW 23, Addrs 017			
8x	UCW	8, Addrs 008			UCW 24, Addrs 018			
9x	UCW	9, Addrs 009			UCW 25, Addrs 019			
Ax	UCW	10, Addrs 00A			UCW 26, Addrs 01A			
Bx	UCW	11, Addrs 00B			UCW 27, Addrs 01B			
Cx	UCW	12, Addrs 00C			UCW 28, Addrs 01C			
Dx	UCW	13, Addrs 00D			UCW 29, Addrs 01D			
Ex	UCW	14, Addrs 00E			UCW 30, Addrs 01E			
Fx	UCW	15, Addrs 00F			UCW 31, Addrs 01F			

Example: Unit control word 27 is located at position B8 in auxiliary-storage module 2. The unit address is 01B.

* These eight MPX UCW's may be used for single-address subchannels or shared subchannels.

Figure 1-10. Auxiliary Storage Module 2

READER TRANSLATE TABLE (Address 30xx)

TENS	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0X	40	F1	F2	F3	F4	F5	F6	F7	F0	61	E2	E3	E4	E5	E6	E7	0X
1X	60	D1	D2	D3	D4	D5	D6	D7	D0	A1	A2	A3	A4	A5	A6	A7	1X
2X	50	C1	C2	C3	C4	C5	C6	C7	C0	81	82	83	84	85	86	87	2X
3X	6A	91	92	93	94	95	96	97	70	B1	B2	B3	B4	B5	B6	B7	3X
4X	F9	31	32	33	34	35	36	37	E9	21	22	23	24	25	26	27	4X
5X	D9	11	12	13	14	15	16	17	A9	E1	62	63	64	65	66	67	5X
6X	C9	01	02	03	04	05	06	07	89	41	42	43	44	45	46	47	6X
7X	99	51	52	53	54	55	56	57	B9	71	72	73	74	75	76	77	7X
8X	F8	79	7A	7B	7C	7D	7E	7F	E8	69	E0	6B	6C	6D	6E	6F	8X
9X	D8	59	5A	5B	5C	5D	5E	5F	A8	A0	AA	AB	AC	AD	AE	AF	9X
AX	C8	49	4A	4B	4C	4D	4E	4F	88	80	8A	8B	8C	8D	8E	8F	AX
BX	98	90	9A	9B	9C	9D	9E	9F	B8	B0	BA	BB	BC	BD	BE	BF	BX
CX	38	39	3A	3B	3C	3D	3E	3F	28	29	2A	2B	2C	2D	2E	2F	CX
DX	18	19	1A	1B	1C	1D	1E	1F	68	20	EA	EB	EC	ED	EE	EF	DX
EX	08	09	0A	0B	0C	0D	0E	0F	48	00	CA	CB	CC	CD	CE	CF	EX
FX	58	10	DA	DB	DC	DD	DE	DF	78	30	FA	FB	FC	FD	FE	FF	FX
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	

UNITS

Figure 1-11. Auxiliary Storage Module 3

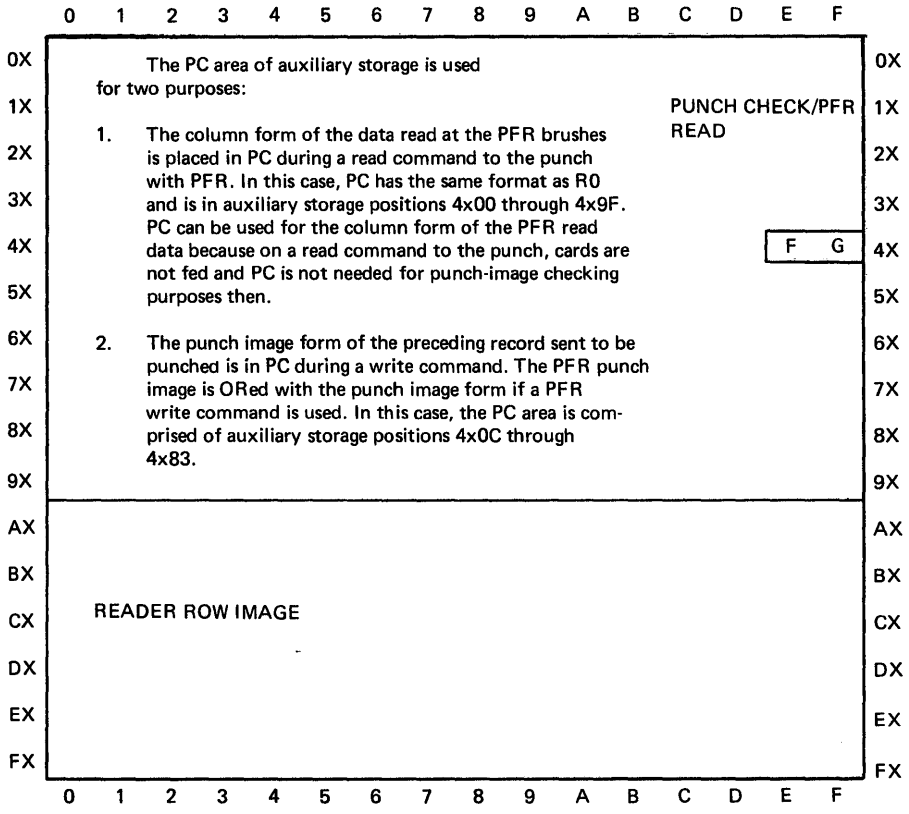


Figure 1-12. Auxiliary Storage Module 4

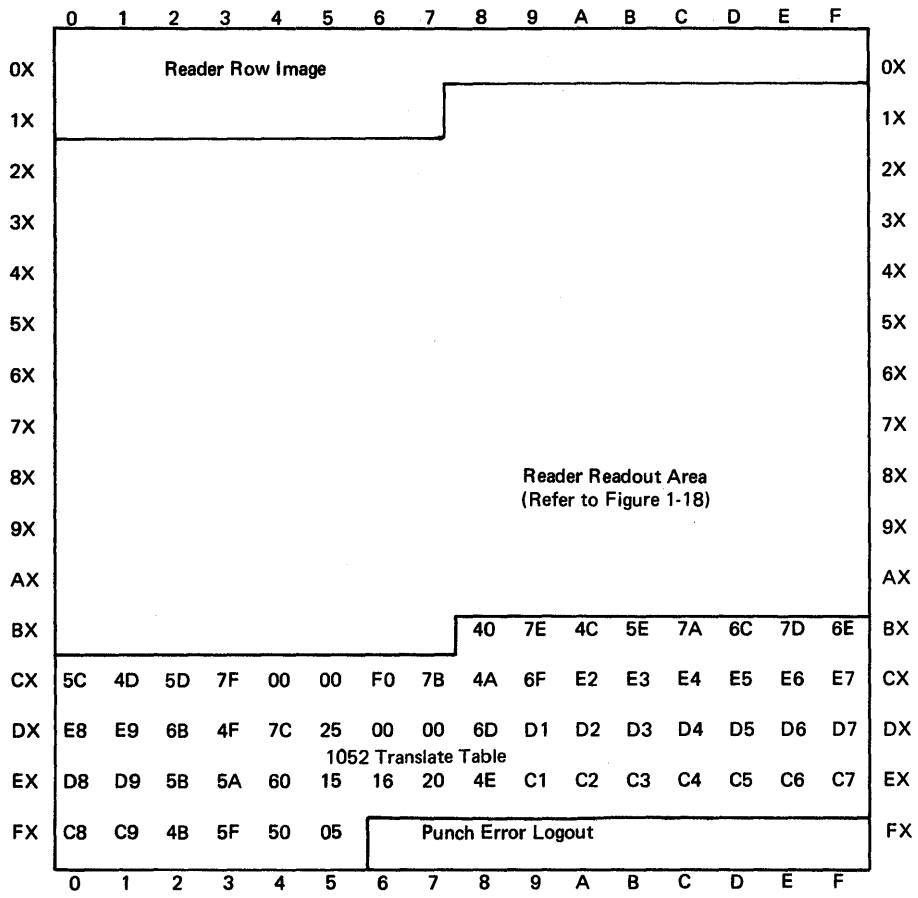


Figure 1-13. Auxiliary Storage Module 5

PUNCH TRANSLATE TABLE

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0X	B9	89	8A	8B	8C	8D	8E	8F	98	99	9A	9B	9C	9D	9E	9F	0X
1X	D9	49	4A	4B	4C	4D	4E	4F	58	59	5A	5B	5C	5D	5E	5F	1X
2X	79	29	2A	2B	2C	2D	2E	2F	38	39	3A	3B	3C	3D	3E	3F	2X
3X	F9	09	0A	0B	0C	0D	0E	0F	18	19	1A	1B	1C	1D	1E	1F	3X
4X	00	A9	AA	AB	AC	AD	AE	AF	B8	91	92	93	94	95	96	97	4X
5X	80	C9	CA	CB	CC	CD	CE	CF	D8	51	52	53	54	55	56	57	5X
6X	40	21	6A	6B	6C	6D	6E	6F	78	31	C0	33	34	35	36	37	6X
7X	E0	E9	EA	EB	EC	ED	EE	EF	F8	11	12	13	14	15	16	17	7X
8X	B1	A1	A2	A3	A4	A5	A6	A7	B0	A8	B2	B3	B4	B5	B6	B7	8X
9X	D1	C1	C2	C3	C4	C5	C6	C7	D0	C8	D2	D3	D4	D5	D6	D7	9X
AX	71	61	62	63	64	65	66	67	70	68	72	73	74	75	76	77	AX
BX	F1	E1	E2	E3	E4	E5	E6	E7	F0	E8	F2	F3	F4	F5	F6	F7	BX
CX	A0	81	82	83	84	85	86	87	90	88	BA	BB	BC	BD	BE	BF	CX
DX	60	41	42	43	44	45	46	47	50	48	DA	DB	DC	DD	DE	DF	DX
EX	32	69	22	23	24	25	26	27	30	28	7A	7B	7C	7D	7E	7F	EX
FX	20	01	02	03	04	05	06	07	10	08	FA	FB	FC	FD	FE	FF	FX
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	

Figure 1-14. Auxiliary Storage Module 6

PRINTER TRANSLATE TABLE (FOLDED, DUALED, BLOCK DATA CHECK)
NON MCS CSL LOAD (REFER TO SECTION 1.14)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0X	04	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30	18	2E	00	0X
1X	16	19	1A	1B	1C	1D	1E	1F	20	21	22	23	24	30	00	00	1X
2X	22	0D	CE	0F	10	11	12	13	14	15	16	17	18	00	17	00	2X
3X	0A	01	02	03	04	05	06	07	08	09	0A	0B	0C	0C	0B	00	3X
4X	00	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30	18	2E	00	4X
5X	16	19	1A	1B	1C	1D	1E	1F	20	21	22	23	24	30	00	00	5X
6X	22	0D	0E	0F	10	11	12	13	14	15	16	17	18	00	17	00	6X
7X	0A	01	02	03	04	05	06	07	08	09	0A	0B	0C	0C	0B	00	7X
8X	16	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30	18	2E	00	8X
9X	22	19	1A	1B	1C	1D	1E	1F	20	21	22	23	24	30	00	00	9X
AX	00	0D	0E	0F	10	11	12	13	14	15	16	17	18	00	17	00	AX
BX	0A	01	02	03	04	05	06	07	08	09	0A	0B	0C	0C	0B	00	BX
CX	16	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30	18	2E	00	CX
DX	22	19	1A	1B	1C	1D	1E	1F	20	21	22	23	24	30	00	00	DX
EX	00	0D	0E	0F	10	11	12	13	14	15	16	17	18	00	17	00	EX
	0A	01	02	03	04	05	06	07	08	09	0A	0B	0C	0C	0B	00	FX
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	

AN CHAIN — 1234567890#@/STUVWXYZ&,%JKLMNOPQR—$*ABCDEFGHI+.□

POSITION #— 00000000000 0 0 00 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 2 2 2 2 2 2 2 2 2 2 2 2 2 3
123456789ABCD EF01 2345 6789ABC DEF01 234 56789ABCDE F 0

Figure 1-15. Auxiliary Storage Module 7

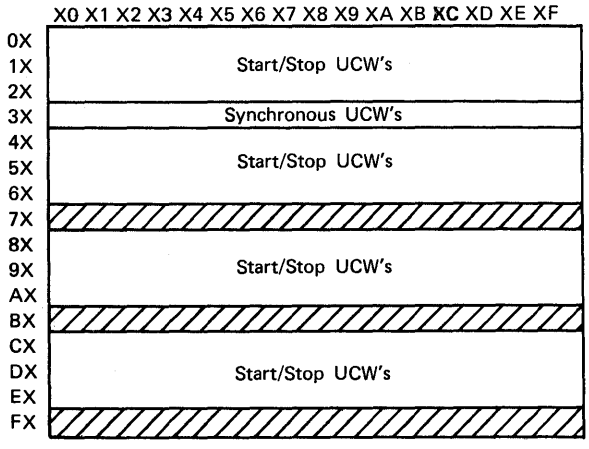


Figure 1-16. Auxiliary Storage Module 8

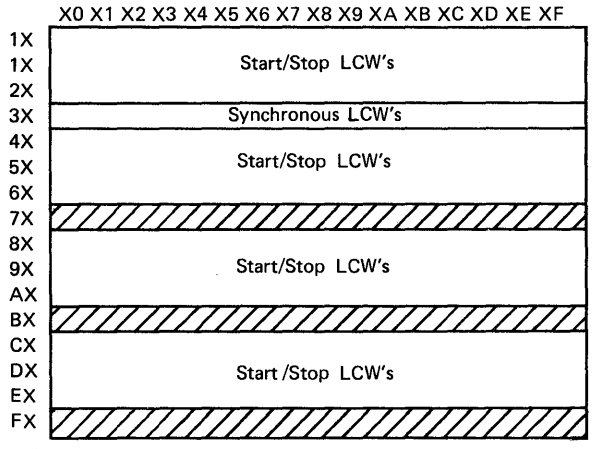


Figure 1-17. Auxiliary Storage Module 9

1.3 2540 READER/PUNCH (FIGURES 1-18 THROUGH 1-23)

BYTE	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
5 x 10									1U	1L	2U	2L	3U	3L	4U	4L
	5U	5L	etc												12U	12L
	13U	13L													20U	20L
	21U	21L													28U	28L
	29U	29L													36U	36L
	37U	37L													44U	44L
	45U	45L													52U	52L
	53U	53L													60U	60L
	61U	61L													68U	68L
	69U														76U	76L
5 x B0	77U	77L	78U	78L	79U	79L	80U	80L								

ADDRESS

U = Upper half of a card column.
L = Lower half of a card column.
1U corresponds to data-record byte 1; 80L corresponds to data-record byte 160.

Hole patterns in a column:	Upper --	12	11	0	1	2	3
	Lower --	4	5	6	7	8	9
Correspond to bit patterns in R0:	0	1	2	3	4	5	6	7

0 0 for either upper or lower.

Figure 1-18. 2540 Readout Area of Aux. Storage (160 Bytes of Column Form)

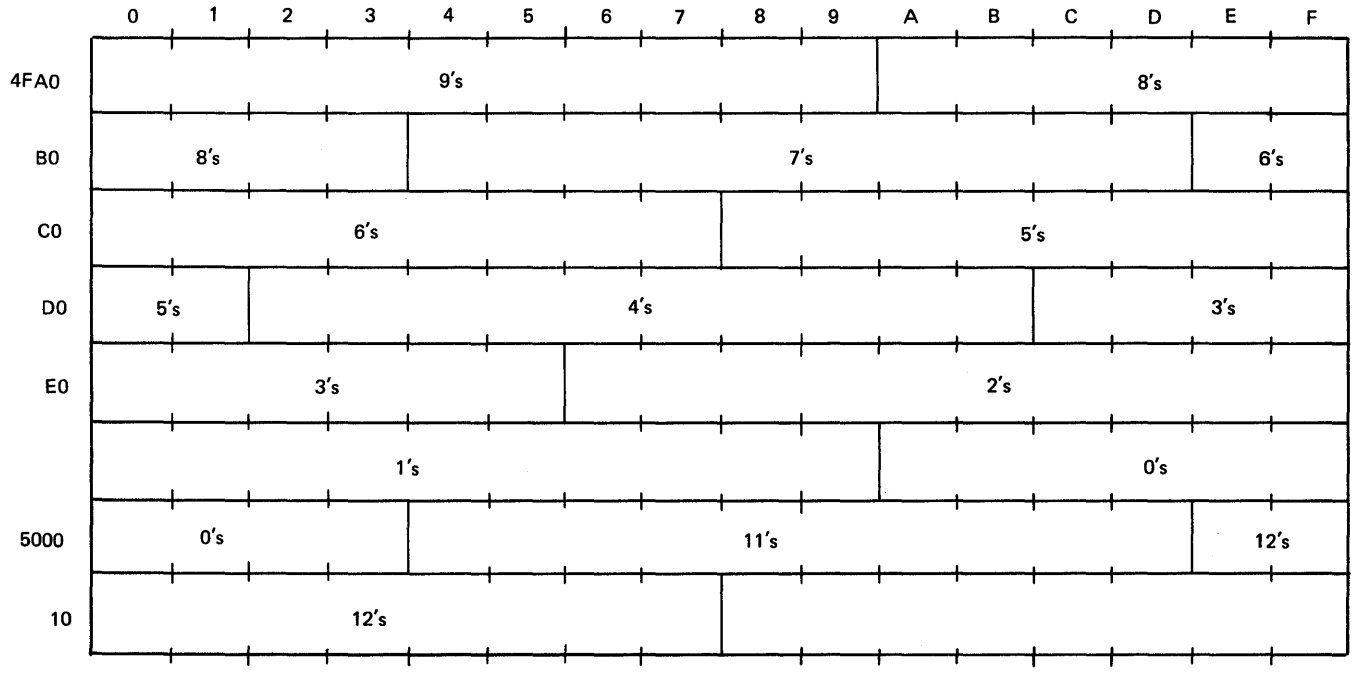
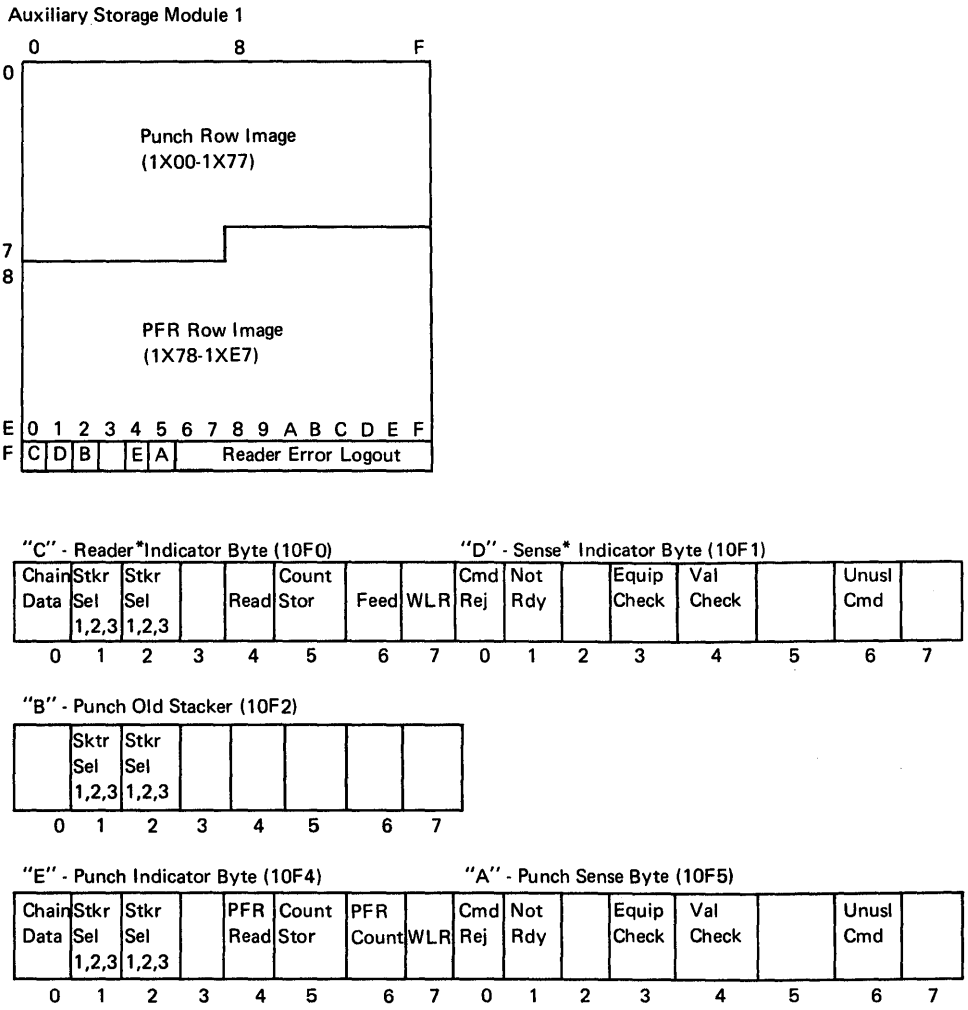


Figure 1-19. 2540 Reader Row Image, Auxiliary Storage

TENS \ UNITS	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	40	F1	F2	F3	F4	F5	F6	F7	F0	61	E2	E3	E4	E5	E6	E7
1	60	D1	D2	D3	D4	D5	D6	D7	D0	A1	A2	A3	A4	A5	A6	A7
2	50	C1	C2	C3	C4	C5	C6	C7	C0	81	82	83	84	85	86	87
3	6A	91	92	93	94	95	96	97	70	B1	B2	B3	B4	B5	B6	B7
4	F9	31	32	33	34	35	36	37	E9	21	22	23	24	25	26	27
5	D9	11	12	13	14	15	16	17	A9	E1	62	63	64	65	66	67
6	C9	01	02	03	04	05	06	07	89	41	42	43	44	45	46	47
7	99	51	52	53	54	55	56	57	B9	71	72	73	74	75	76	77
8	F8	79	7A	7B	7C	7D	7E	7F	E8	69	E0	6B	6C	6D	6E	6F
9	D8	59	5A	5B	5C	5D	5E	5F	A8	A0	AA	AB	AC	AD	AE	AF
A	C8	49	4A	4B	4C	4D	4E	4F	88	80	8A	8B	8C	8D	8E	8F
B	98	90	9A	9B	9C	9D	9E	9F	B8	B0	BA	BB	BC	BD	BE	BF
C	38	39	3A	3B	3C	3D	3E	3F	28	29	2A	2B	2C	2D	2E	2F
D	18	19	1A	1B	1C	1D	1E	1F	68	20	EA	EB	EC	ED	EE	EF
E	08	09	0A	0B	0C	0D	0E	0F	48	00	CA	CB	CC	CD	CE	CF
F	58	10	DA	DB	DC	DD	DE	DF	78	30	FA	FB	FC	FD	FE	FF

Figure 1-20. 2540 Reader Translate Table, Auxiliary Storage--30xx



* Reader and sense indicators reset on SIO decode (error).

Figure 1-21. 2540 Sense Indicator Bytes

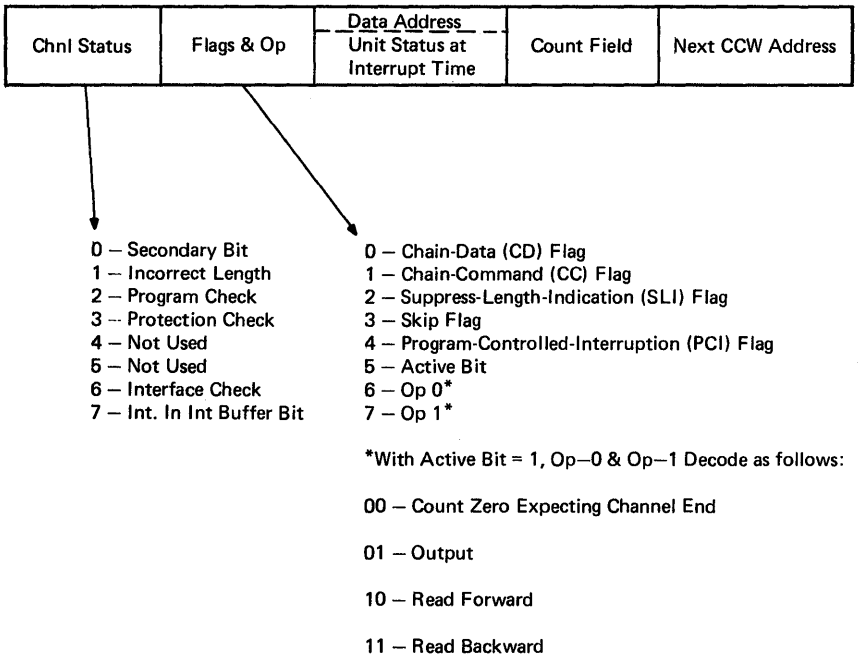


Figure 1-22. 2540 Reader-UCW Format

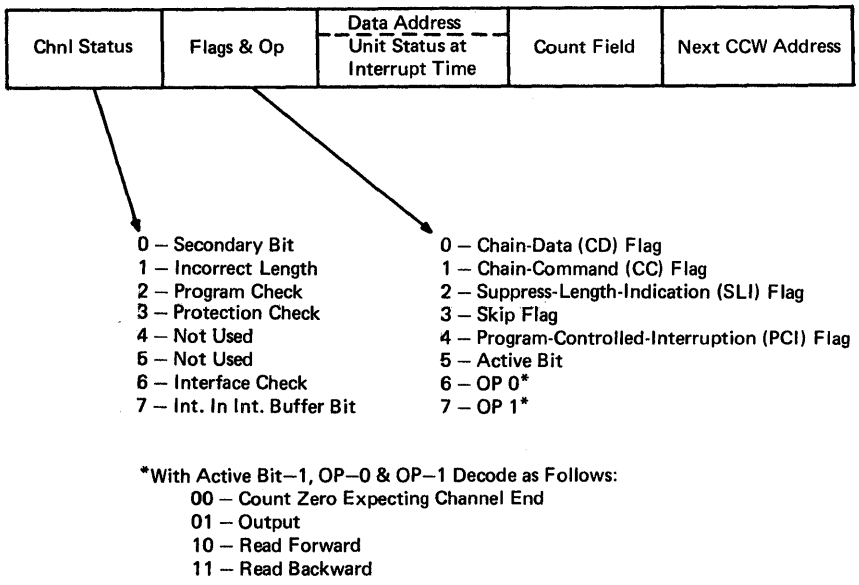


Figure 1-23. 2540 Punch-UCW Format

1.4 STORAGE PRCTECTION FEATURES (FIGURES 1-24 THROUGH 1-26)

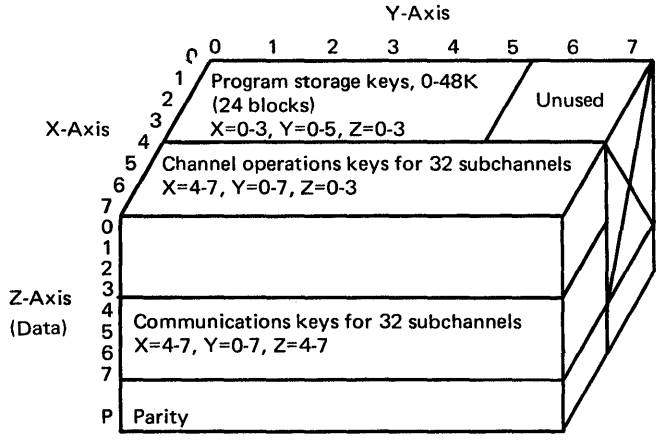


Figure 1-24. STP1 Allocations Map

X-Axis \ Y-Axis**	0	1	2	3	4	5	6*	7*
0	0000-07FF 0-2K	2000-27FF 8-10K	4000-47FF 16-18K	6000-67FF 24-26K	8000-87FF 32-34K	A000-A7FF 40-42K	C000-C7FF 48-50K	E000-E7FF 56-58K
1	0800-0FFF 2-4K	2800-2FFF 10-12K	4800-4FFF 18-20K	6800-6FFF 26-28K	8800-8FFF 34-36K	A800-AFFF 42-44K	C800-CFFF 50-52K	E800-EFFF 58-60K
2	1000-17FF 4-6K	3000-37FF 12-14K	5000-57FF 20-22K	7000-77FF 28-30K	9000-97FF 36-38K	B000-B7FF 44-46K	D000-D7FF 52-54K	F000-F7FF 60-62K
3	1800-1FFF 6-8K	3800-3FFF 14-16K	5800-5FFF 22-24K	7800-7FFF 30-32K	9800-9FFF 38-40K	B800-BFFF 46-48K	D800-DFFF 54-56K	F800-FFFF 62-64K

* These columns are shown for reference only. The storage locations represented are never used for program storage, and thus are not subject to the storage protection feature.

** For systems with less than 48K bytes of program storage, the locations above the installed program storage are not protected.

Figure 1-25. STP1 Allocations for Program Storage

X-Axis \ Y-Axis	0	1	2	3	4	5	6	7
4	00-07 (1)	20-27 (5)	40-47 (9)	60-67 (13)	80-87 (17)	A0-A7 (21)	C0-C7 (25)	E0-E7 (29)
5	08-0F (2)	28-2F (6)	48-47 (10)	68-67 (14)	88-8F (18)	A8-AF (22)	C8-CF (26)	E8-EF (30)
6	10-17 (3)	30-37 (7)	50-57 (11)	70-77 (15)	90-97 (19)	B0-B7 (23)	D0-D7 (27)	F0-F7 (31)
7	18-1F (4)	38-3F (8)	58-5F (12)	78-7F (16)	98-9F (20)	B8-BF (24)	D8-DF (28)	F8-FF (32)

Note: For channel operations, bits 0-3 (Z-axis) are used for a maximum of 32 keys (shown in parentheses).

For communications channel operations, bits 4-7 are used for a maximum of 32 keys.

Figure 1-26. STP1 Allocations for Channel and Communications Channel Operation

1.5 1400 COMPATIBILITY FEATURE (FIGURES 1-27 THROUGH 1-33)

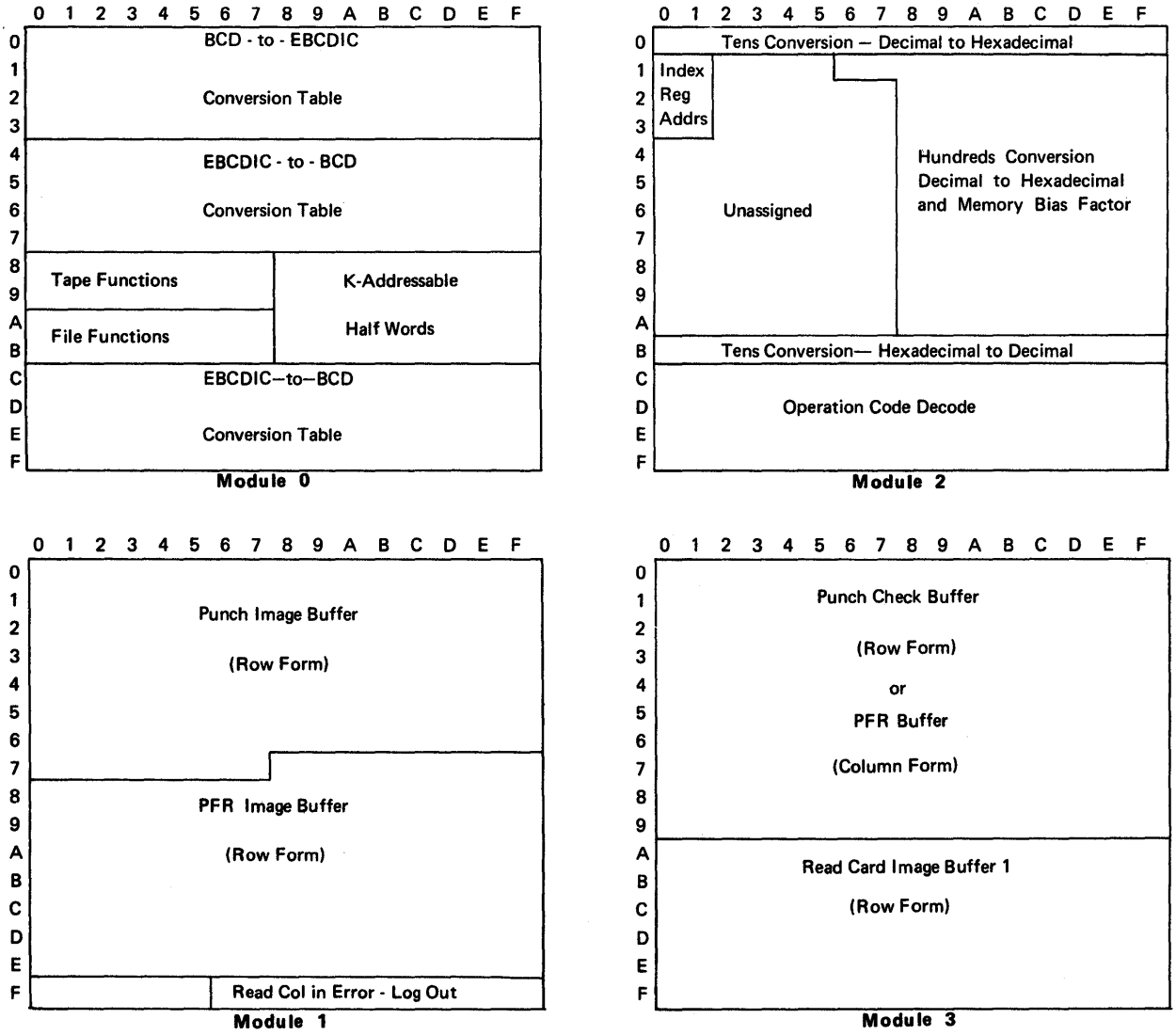


Figure 1-27. 1401/1460 Compatibility Features Aux. Storage Map (Part 1 of 2)

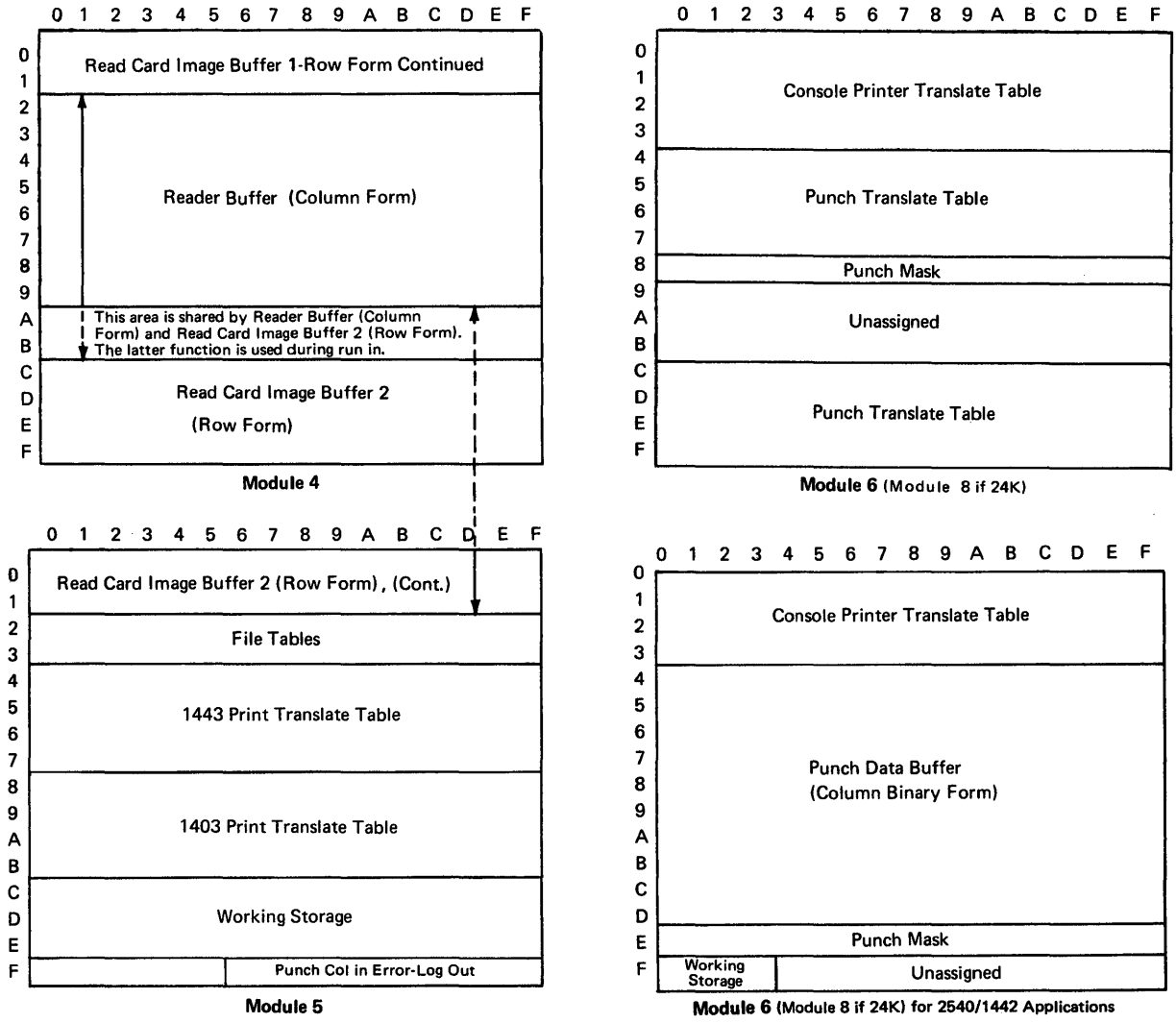


Figure 1-27. 1401/1460 Compatibility Features Aux. Storage Map (Part 2 of 2)

1.5.1 AUXILIARY STORAGE MODULE 0 (1400 COMPATIBILITY)

Rows 0-3; BCD to EBCDIC Conversion Table: These 4 rows provide the constants for translating the 64 possible BCD configurations to the appropriate EBCDIC bytes.

Rows 4-7 and C-F; EBCDIC to BCD Conversion Table: These 8 rows provide a 128 character table that contains a BCD code corresponding to each EBCDIC character. EBCDIC to BCD translation is required during the execution of instructions such as Bit Tests, Move Zone and Move Numeric.

Rows 8 and 9, Bytes 0 through 7; Tape Assignments: The utilization of the tape control and initial load bytes in auxiliary storage module 0 is as follows.

Byte	Bit	Use
	0	Last Command Write or WTM
80	1-3	Last 1400 tape unit addressed (initialized to 000).
	4-7	Tape Control Unit Address
81	0-1	Tape density for 1400-mode tape drive 1: 00=200 bpi on 7-track tape drive 01=556 bpi on 7-track tape drive 10=800 bpi on 7-track tape drive 11=9-track tape drive
	2	If on, a backspace was the last operation performed on 1400-mode tape drive 1 (initialized to 0).
	3	If on, an end-of-file condition is outstanding on 1400-mode tape drive 1(initialized to 0).
	4	Used internally
	5-7	System/360 unit address assigned to be 1400-mode tape drive 1.
82-86		Same as byte 81, for 1400-mode tape drives 2 through 6.
87		Last status byte received from tape-control unit (initialized to 40).
88-8F		Refer to K-addressable halfwords.
90		Tape sense byte 0
91		Tape sense byte 1
92		Tape sense byte 2 (tape track in error)
93		Tape sense byte 3
94-95		Tape O-STAR backup location
96	0	Temporary command information
	1	1400 tape drive 1 EOF-block bit
	2	1400 tape drive 2 EOF-block bit
	3	1400 tape drive 3 EOF-block bit
	4	1400 tape drive 4 EOF-block bit
	5	1400 tape drive 5 EOF-block bit
	6	1400 tape drive 6 EOF-block bit
	7	Temporary command information
97		MCS control; Print Character Counter Length (PCCL) Bit significance
	0	Unassigned
	1	240 character
	2	120 character
	3	80 character
	4	60 character
	5	48 character
	6	40 character
	7	16 character

Rows A and B, bytes 0 through 7 are used for disk file functions:

Byte	Bit	Compatibility Mode Use
A0-A1		1400 Drive-0 Assignment
A0	0-3	Must be set to 0000
	4-7	Modular addresses 0 to 19,999=0000 Modular addresses 20K to 39,999=0010 Modular addresses 40K to 59,999=0100 Modular addresses 60K to 79,999=0110 Modular addresses 80K to 99,999=1000
A1	0-3	System/360 File Select Addresses: File 0=1000 File 1=0100 File 2=0010 File 3=0001
	4-5	Not used
	6	Compare Disable. 6=0; compare disable is inactive. A successful address compare on a 1400-series indelible address (I/A) must occur before an I/A read or write can be executed. 6=1; compare disable is active. Read or write with I/A is executed without first doing an address compare on the 1400-series indelible address. This bit should be set to 1 only when initializing a disk pack in 1400 mode.
	7	Module overflow detection. 7=0; module overflow detection is active. The 1400-program

module value, within each disk-control field, is compared against a module value that is present in auxiliary storage. If the module values disagree, a coded stop occurs with 60 displayed. In addition, Unequal Address Compare is set. Correct module values must be set in auxiliary storage 0 locations A0, A2, etc.
7=1; module-overflow detection is inactive. (Most user applications set bit 7 to 1.)

A2-A3, A4-A5, A6-A7 and B6-B7 represent 1400 drives 2, 4, 6, and 8 respectively. Assignments follow the same structure format as A0-A1. Compare disable and module-overflow detection need only be set in the A1 byte.

B0-B5 Disk Error information for diagnostic use.

Rows 8 through B, Bytes 8 through F, K-addressable Halfwords: The 16 K-addressable halfwords of auxiliary storage module 0 are used as follows for 1401/1460 and 1440 compatibility mode.

K-Adr	Byte	Bit	Use
K0	88-89		Bias constant. Refer to Figure 1-30 for correct value.
K1	8A-8B		Working storage
K2	8C-8D		B-STAR backup for local storage V0,V1
K3	8E-8F		A-STAR backup for local storage U0,U1
K4	98-99		Working storage
K5	9A-9B		Working storage
K6	9C (Integrated Attachment Printer)	0	132 print position 1403
		1	Channel 9
		2	Channel 12
		3	Invalid channel
		4	Secondary bit
		5	Device end
		6	Print wordmark operation
		7	Printer error
K6	9C (Channel Attached Printer)	0	132-position 1403; or greater than 120 positions if 1443.
		1	Channel 9
		2	Channel 12
		3-7	Device address
	9D		Forms command
		0	1403 Printer (Integrated Attachment Only)
		1	On Channel (Integrated Attachment Only)
		2	
		3	
		4	Go to Set Up after Rmt/Rst (Integrated Attachment Only)
		5	From General Stop Loop (Integrated Attachment Only)
		6	Last CMD Skip or Spc Sup.
		7	Forms After Cmd
K7	9E		Reader-1 address
	9F		Reader-2 address
K8	A8	0	Sense switch A (last card)
		1	Sense switch B
		2	Sense switch C
		3	Sense switch D
		4	Sense switch E
		5	Sense switch F
		6	Sense switch G
		7	Sense switch A for second serial reader punch
	A9	0	High-compare result (U)
		1	Unequal-compare result (/)
		2	Low-compare result (T)
		3	Equal-compare result (S)
		4	Inquiry clear indicator(*)
		5	Overflow indicator (Z)
		6	Inquiry request indicator (Q)
		7	Not used
K9	AA	0	Not move or load instruction (PR-KB)
		1	H-Typehead installed (PR-KB)
		2	Secondary bit (PR-KB)
		3	Load mode (PR-KB)
		4	Stop message being performed (PR-KB)
		5	Reader error
		6	Punch error
		7	Printer error
	AB		Unassigned
KA	AC	0	48K*
		1	24K, 32K*
		2	16K, 32K, or 48K*
		3-7	Initialized to 1*
			*High-order byte of highest storage address initialized to 3F,5F,7F, or BF.
	AD		1442/1443 Status
		0	Skip GMWM check
		1	Channel end only
		2	Last card on
		3	Column binary mode
		4	Print operation
		5	Output command
		6-7	00=R/W, 01=Test I/O, 10=Sense, 11=Control

KB	AE	0-7	Previous file operation
	AF	0	Read back check interlock
		1	Recalibrate sequence bit
		2	Unequal-address compare (X)
		3	Access busy (\)
		4	Wrong-length record (W)
		5	Any disk err condition (Y)
		6	Disk error (V)
		7	Not ready (N)
KC	B8	0	I/O check-stop switch
		1	Not used
		2	Expanded print-edit feature
		3	Period-comma inversion (World Trade only)
		4	Column binary feature
		5	No punch buffer
		6	Model-G emulation
		7	51-column cards
		Usage of bits 5, 6, and 7 when using 2540 as 1442:	
		5	Simulate read and punch in same card
		6	Select read-error card to pocket R2
		7	Use 2540 as 1442
	B9	0	Alternate read mode
		1	120-print position printer
		2	Tape erase (initialized off)
		3	Alternate 9-track tape
		4	Temporary Status
		5	Channel printer
		6-7	Sterling feature (World Trade only)
KD	BA	0	System/360 tape drive 0 is a 9-track unit
		1	System/360 tape drive 1 is a 9-track unit
		2	System/360 tape drive 2 is a 9-track unit
		3	System/360 tape drive 3 is a 9-track unit
		4	System/360 tape drive 4 is a 9-track unit
		5	System/360 tape drive 5 is a 9-track unit
		6	System/360 tape drive 6 is a 9-track unit
		7	System/360 tape drive 7 is a 9-track unit
KD	BB	0	0=0 tape drive 0=800 bpi density 0=1--1600 bpi
		1	1=0 tape drive 1=800 bpi density 1=1--1600 bpi
		2	2=0 tape drive 2=800 bpi density 2=1--1600 bpi
		3	3=0 tape drive 3=800 bpi density 3=1--1600 bpi
		4	4=0 tape drive 4=800 bpi density 4=1--1600 bpi
		5	5=0 tape 5=800 bpi density 5=1--1600 bpi
		6	6=0 tape drive 6=800 bpi density 6=1--1600 bpi
		7	7=0 tape drive 7=800 bpi density 7=1--1600 bpi

KE-KF BC-BF Working Storage

1.5.2 AUXILIARY STORAGE MODULE 1 (1400 COMPATIBILITY)

Rows 0-7(7): Punch Image Buffer, (row form)
Rows 7(8)-E: PFR Image Buffer, (row form)
Row F: (F6-FF) Logout area for card read errors.

1.5.3 AUXILIARY STORAGE MODULE 2 (1400 COMPATIBILITY)

Row 0; Tens Conversion Constants: This row provides tens conversion for translating BCD to EBCDIC. 0A through 0F contain invalid digit values.

Rows 1, 2, and 3; Bytes 0 and 1; Index Register Addresses: These three halfwords give the addresses for the index registers for the tens character zones A, B, and AB respectively.

Rows 1-A, Bytes 8-F; Hundreds, Thousands and Bias Conversion Table: The values in this table are determined by the sizes of the 1401/1460 or 1440 being emulated and the size of the 2025 program storage area. Entry into the table is according to hundreds and hundreds zones (thousands). Thus, the result from the table solves hundreds, thousands, and bias translation simultaneously. The halfword at 16 is an extension of the table and is used to translate the / character.

Row B; Hexadecimal-to-Decimal Conversion Table: This row gives the decimal equivalent of the second order hex digit value.

Rows C through F; Operation Code Decode Table: These four rows provide the translation of 1401/1460 and 1440 operation codes to a bit significant form that is usable by the 2025. In the chart (Figure 1-28), the 1400-series op-code is shown in

parentheses. Code 34 is used to indicate an invalid 1400-series op-code. Code 06 is used to indicate a No-op.

1.5.4 AUXILIARY STORAGE MODULE 3 (1400 COMPATIBILITY)

Rows 0-9: Punch Check Buffer (row form) or PFR Buffer (column form).
Rows A-F: Read Image Buffer 1 (row form). Partial; remainder of buffer area is in module 4, rows 0 and 1.

1.5.5 AUXILIARY STORAGE MODULE 4 (1400 COMPATIBILITY)

Rows 0-1: Read Image Buffer 1 (row form) continued from module 3.
Rows 2-B: Reader Buffer (column form).
Rows A-F: Read Image Buffer 2 (row form). Partial; remainder of buffer is in module 5, rows 0 and 1. Rows A and B are shared with the column form buffer.

1.5.6 AUXILIARY STORAGE MODULE 5 (1400 COMPATIBILITY)

Rows 0 and 1: Read Image Buffer 2 (row form). Continued from module 4.
Rows 2 and 3: Disk File Tables, conversion tables for cylinder and head decode, file op-code conversion, etc.
Rows 4-7: 1443 Translate Table
Rows 8-B: 1403 Translate Table
Rows C-E: Working Storage
Row F: (F6-FF) Logout area for card punch errors.

1.5.7 AUXILIARY STORAGE MODULE 6 (8 IN 24K SYSTEMS--1400 COMPATIBILITY)

Rows 0-3: Console Printer Translate Table
Rows 4-7: Punch Translate Table
Row 8: Punch Mask
Rows 9-B: Unassigned
Rows C-F: Punch Translate Table.

Differences for 2540/1442 applications:
Rows 4-D: Punch Data Buffer (column binary form)
Row E: Punch Mask
Row F: Working Storage and Unassigned.

1.5.8 LOCAL STORAGE (1400 COMPATIBILITY)

The 64-byte local storage is divided into six zones that are used in the same general manner in the 1400 mode as in System/360 mode.

Zone 0, CPU Mode; 16 bytes
Zone 1, 2311 Mode; 8 bytes
Zone 4, Backup area; 16 bytes
Zone 5, Undefined; 8 bytes
Zone 6, 2540 Mode; 8 bytes
Zone 7, Channel Mode; 8 bytes

Local storage is used when operating in 1401/1460 or 1440 compatibility mode for intermediate storage for factors unique to this mode of operation. Example: I-STAR, A-STAR, B-STAR, Op-register and A-register. In addition, local storage is used for problem-program factors and microprogram factors, Also, data stored in local storage is used by control words to perform some problem-program functions.

1.5.8.1 Zone 0 (1400 Compatibility)

Zone 0 is addressed when the Model 25 is operating in CPU mode. There are 16 bytes within the zone-0 area addressed by X-lines 0-7 and Y-lines 0 and 1. Not all bytes have assigned functions.

AS/BS Decode	Sym	X	Y	Assigned Function
0	U0	0	0	A-Address Register
1	U1	1	0	A-Address Register
2	V0	2	0	B-Address Register
3	V1	3	0	B-Address Register
4	G0	4	0	Working Register
5	G1	5	0	Op-Register
6	D0	6	0	Status Indicators
7	D1	7	0	A-Register
8	I0	0	1	I-Address Register
9	I1	1	1	I-Address Register
A	T0	2	1	Working Register
B	T1	3	1	Working Register
C	P0	4	1	Working Register
D	P1	5	1	Working Register
E	H0	6	1	Working Register
F	H1	7	1	Working Register

1.5.8.2 Zone 1 (1400 Compatibility)

Zone 1 is addressed when the Model 25 is operated in 2311 mode. There are 8 bytes within the zone-1 area addressed by X-lines 0-7 and Y-line 2, as follows.

AS/BS Decode	Sym	X	Y	Assigned Function
8	I0	0	2	Count Register
9	I1	1	2	Count Register
A	T0	2	2	Data Address Register
B	T1	3	2	Data Address Register
C	P0	4	2	
D	P1	5	2	
E	H0	6	2	
F	H1	7	2	

1.5.8.3 Zone 4 (1400 Compatibility)

Zone 4 is used as the backup area for all modes of operation except 2311 mode. There are 16 bytes within the zone-4 area

addressed by X-lines 0-7 and Y-lines 3 and 4.

For the CPU mode operation the backup area can be addressed by setting mode register bits 5, 6, and 7 to 1,0,0. For operation in 2540 or channel mode (MMSK bits 0, 2, 3, or 4 on), the low-order 8 bytes of zone 4 can be addressed. None of the bytes of the backup area can be addressed when operating in 2311 mode (MMSK bit 1 on).

All 16 bytes of the backup area can be addressed manually by console switches C and D. Assignments are as follows.

AS/BS Decode	Sym	X	Y	Assigned Function
0	U0	0	4	High-order Level-1 Backup addr
1	U1	1	4	Low-order Level-1 Backup addr
2	V0	2	4	High-order Level-2 Backup addr
3	V1	3	4	Low-order Level-2 Backup addr
4	G0	4	4	High-order Level-3 Backup addr
5	G1	5	4	Low-order Level-3 Backup addr
6	D0	6	4	High-order Machine-Check Backup Addr
7	D1	7	4	Low-order Machine-Check Backup Addr
8	I0	0	3	High-order CPU Branch and link Backup Address
9	I1	1	3	Low-order CPU Branch and link Backup address
A	T0	2	3	Spare
B	T1	3	3	Spare
C	P0	4	3	Workarea
D	P1	5	3	Workarea
E	H0	6	3	Workarea
F	H1	7	3	Workarea

1.5.8.4 Zone 6 (1400 Compatibility)

Zone 6 is addressed when operating in 2540 mode (MMSK bits 3 or 4 on). There are eight bytes in the zone-6 area addressed by X-lines 0-7 and y-line 6. Also, zone 6 can be addressed when in CPU mode by setting the mode register bits 5, 6, 7 to 1, 1, 0 respectively.

AS/BS Decode	Sym	X	Y	Assigned Function
0	U0	0	6	Reader Image Buffer Address
1	U1	1	6	Reader Image Buffer Address
2	V0	2	6	Punch Image Buffer Address
3	V1	3	6	Punch Image Buffer Address
4	G0	4	6	Reader/Punch Status
5	G1	5	6	Stacker-Select Information
6	D0	6	6	Punch Count
7	D1	7	6	Read Count

1.5.8.5 Zone 7 (1400 Compatibility)

Zone 7 is address when operating in channel mode (MMSK bits 0 or 2 on). There are 8 bytes in the zone-7 area addressed by X-lines 0-7 and Y-line 7. The functional assignments for these bytes are:

AS/BS Decode	Sym	X	Y	Assigned Function
0	U0	0	7	
1	U1	1	7	
2	V0	2	7	Data Address Register
3	V1	3	7	Data Address Register
4	G0	4	7	
5	G1	5	7	Data Register
6	D0	6	7	Status Register
7	D1	7	7	Word Separator

Sequence of Operation for Combination Operations Is Print, Read, and Punch	
1400 Operation	
Read (1)	Starts as 21, and during read ending routine (LRDR) is changed to 20. In case of error (and the I/O Stop switch is on,) the code remains 21 and display stop occurs.
Print (2)	Starts as 22 and is reset to 00 at the end of the normal print routine (MPRT) before return to LOPD and ICYC.
Print, Read (3)	Starts as 23 and is changed to 21 at end of the print routine. Routine branches back to ICYC VALADR 0, is decoded as a 1 Op and executed.
Punch (4) Punch Col Bin (4C)	Starts as 24 and is changed to 20 during punch ending routine (LPCH). In case of error, code remains 24 and a display stop occurs.
Read, Punch (5)	Starts as 25 and is changed to 24 at read ending (LRDR). In case of error (with I/O Stop switch on) code remains 25 and display stop occurs. No error routine branches back to LOPD, performs punch op and is changed to 20.
Print, Punch (6)	Starts as 26 and is changed to 24 at end of Print routine. Routine branches back to ICYC VALADR 0 and is decoded as a punch op. Operation is then the same as a 4 op and is changed to 20 at the ending.
Print, Read, Punch (7)	Statts as 27, changes to 25 at end of print operation. 25 causes a read op, at end of read op code changes to 24 and causes a punch op. At end of punch op, code changes to 20. All error limitations for the various operations apply.
Punch Feed Read (4R)	Starts as 24. The d-modifier causes the op code to change to A4, then a normal punch routine is started. At the end of the punch routine the code is changed to 28 and a punch feed read operation is performed. At end op code changes to 20.
Read Column Binary (1C)	Starts as 21. Changes to 20 during read ending routine (RDREND). Error handling same as for Read op. (Validity not checked.)

Figure 1-28. Op-Code Information (1400 Compatibility)

	WITH WORDMARK				NO WORDMARK				WITH WORDMARK				NO WORDMARK			
4567 ↓ / 0123 →	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	Blank	&	-		Blank	&	--		?	I	‡	0	?	I	‡	0
0001			/				/		A	J		1	A	J		1
0010									B	K	S	2	B	K	S	2
0011									C	L	T	3	C	L	T	3
0100									D	M	U	4	D	M	U	4
0101									E	N	V	5	E	N	V	5
0110									F	O	W	6	F	O	W	6
0111									G	P	X	7	G	P	X	7
1000									H	Q	Y	8	H	Q	Y	8
1001									I	R	Z	9	I	R	Z	9
1010				ъ				ъ								
1011	.	$	'	#	.	$	'	#								
1100	¤	*	%	@	¤	*	%	@								
1101	⌊	⌋	v	:	⌊	⌋	v	:								
1110	<	;	\	>	<	;	\	>								
1111	‡	△	⧻	√‾	‡	△	⧻	√‾								

Figure 1-29. 1400 Defined Characters

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
C	(?) 1C	(A) 18	(B) 0B	(C) 1F	(D) 12	(E) 16	(F) 2A	34	(H) B1	34	34	(·) 02	(¤) 15	34	34	34
D	(!) 1D	34	(K) 29	(L) 90	(M) 80	(N) 06	34	(P) 1E	(Q) F1	34	34	34	34	34	34	34
E	34	(/) 05	(S) 19	34	(U) 20	(V) 0E	(W) 0F	34	(Y) 13	(Z) 17	34	(,) 04	(%) 1B	34	34	34
F	34	(1) 21	(2) 22	(3) 23	(4) 24	(5) 25	(6) 26	(7) 27	(8) 06	(9) 06	34	(≠) 14	(@) 1A	34	34	34

Notes:

1. The 1400-series operation code is shown in parentheses.
2. The code 34 is used to indicate an invalid 1400-series operation code.
3. The code 06 is used to indicate a No Op (no operation).
4. Notice that several 1400-series special features, such as Branch if Bit Equal (W op code), Divide (% op code), etc. are standard with the compatibility feature. These 1400-series operations can be made invalid by inserting the invalid code (34) in the corresponding table location, if desired.

Figure 1-30. 1400 Operation-Code Decode Table

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
4	00	40	40	40	40	40	40	40	40	40	40	3B	3C	3D	3E	3F
5	30	40	40	40	40	40	40	40	40	40	40	2B	2C	2D	2E	2F
6	20	11	40	40	40	40	40	40	40	40	40	1B	1C	1D	1E	1F
7	40	40	40	40	40	40	40	40	40	40	10	0B	0C	0D	0E	0F
C	3A	31	32	33	34	35	36	37	38	39	40	40	40	48	45	5C
D	2A	21	22	23	24	25	26	27	28	29	40	40	40	40	46	5D
E	1A	40	12	13	14	15	16	17	18	19	40	40	40	49	4F	56
F	0A	01	02	03	04	05	06	07	08	09	40	40	40	40	44	5F

Figure 1-31. EBCDIC-to-BCD Translate Table (1400)

25 / 1400	16,384		24,576		32,768		49,152	
	Bias Constant	File Table	Bias Constant	File Table	Bias Constant	File Table	Bias Constant	File Table
16K	0180	0000	2180	2000	4180	4000	8180	8000
12K	1120	1000	3120	3000	5120	5000	9120	9000
8K	20C0	1F00	40C0	3F00	60C0	5F00	A0C0	9F00
4K	3060	2F00	5060	4F00	7060	6F00	B060	AF00
2K	3830	3700	5830	5700	7830	7700	B830	B700
1.4K	3A88	3900	5A88	5900	7A88	7900	BA88	B900

Bias Constant: Located in byte 88-89, (K0) in Module 0.

File Table Address: Developed from bias constant during file routine.

Figure 1-32. Storage Bias Constant Values and File Table Addresses (1400 Compatibility)

AUXILIARY STORAGE MODULE 2

	6 7	8 9	A B	C D	E F
1X	B+044C	B+0BB8	B+07D0	B+03E8	B+0000
2X		B+0C1C	B+0834	B+044C	B+0064
3X		B+0C80	B+0898	B+04B0	B+00C8
4X		B+0CE4	B+08FC	B+0514	B+012C
5X		B+0D48	B+0960	B+0578	B+0190
6X		B+0DAC	B+09C4	B+05DC	B+01F4
7X		B+0E10	B+0A28	B+0640	B+0258
8X		B+0E74	B+0A8C	B+06A4	B+02BC
9X		B+0ED8	B+0AF0	B+0708	B+0320
AX		B+0F3C	B+0B54	B+076C	B+0384

Note: B=Halfword bias constant in K0 (Module 0; 88-89)
See previous figure for value.

Hundreds/Thousands/Bias Conversion

AUXILIARY STORAGE MODULE 2

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0X	00	0A	14	1E	28	32	3C	46	50	5A	01	01	01	01	01	01

Tens Conversion

Figure 1-33. Decimal-to-Hex Conversion Tables (1400 Compatibility)

1.6 PR-KB (PRINTER-KEYBOARD) FIGURES 1-34 THROUGH 1-38

BCD Bits		A	B	BA		A	B	BA
	Space	@	-	&	Space	Ç	—	+
1	1	/	j	a	=	?	J	A
2	2	s	k	b	⟨	S	K	B
2 1	3	t	l	c	;	T	L	C
4	4	u	m	d	:	U	M	D
4 1	EOB 5 Note 2	v	n	e	%	V	N	E
4 2	6	w	o	f	'	W	O	F
4 2 1	7	x	p	g	⟩	X	P	G
8	8	y	q	h	*	Y	Q	H
8 1	9	z	r	i	(	Z	R	I
8 2	Cancel 0 Note 2				)			
8 2 1	#	'	$	.	"	|	!	¬
8 4								
8 4 1			NEW LINE				NEW LINE	
8 4 2	UPPER CASE SHIFT			LOWER CASE SHIFT	UPPER CASE SHIFT			LOWER CASE SHIFT
8 4 2 1								

LOWER CASE UPPER CASE

Note 2: Alternate coding key must be pressed for EOB and Cancel

The keyboard code characters are sent to the CPU in 8-bit form as follows.

Bus-In Bits	KB Bits	
0	x	See Note 1
1	x	
2	B	
3	A	
4	8	
5	4	
6	2	
7	1	

Note 1:

x = 1, x = 1 — Uppercase

x = 0, x = 0 — Lowercase

Figure 1-34. Input Code from Keyboard (PR-KB)

EBCDIC Bits 0123:

Bits 4567:	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	sp	&	–	–	sp	&	–	–	@	&	–	0	%	>	?	0
0001	sp	n	/	8	sp	n	/	8	a	j	/	1	A	J	_	1
0010	sp	o	b	,	sp	o	b	,	b	k	s	2	B	K	S	2
0011	sp	o	s	#	sp	o	s	#	c	l	t	3	C	L	T	3
0100	sp	2	@	@	sp	2	@	@	d	m	u	4	D	M	U	4
0101	sp	NL	/	8	sp	5	/	8	e	n	v	5	E	N	V	5
0110	sp	6	k	#	sp	6	k	#	f	o	w	6	F	O	W	6
0111	sp	6	s	#	sp	6	s	#	g	p	x	7	G	P	X	7
1000	h	q	y	y	H	Q	Y	Y	h	q	y	8	H	Q	Y	8
1001	i	r	z	9	i	r	z	9	i	r	z	9	I	R	Z	9
1010	.	$	.	,	Ç	!	Ç	:	@	$	–	0	%	>	?	0
1011	.	$	,	#	.	$	,	#	.	$	,	#	Ç	!	:	#
1100	3	7	@	@	<	*	%	@	e	n	u	4	E	N	U	4
1101	1	5	/	8	(	)	_	'	e	n	v	5	E	N	V	5
1110	2	6	&	#	+	;	>	=	e	p	u	6	E	P	U	6
1111	0	4	–	9	|	¬	?	"	e	n	v	5	E	N	V	5

Note: Blocked areas show normal decoded Characters using 1052 keyboard Input

Figure 1-35. EBCDIC Output with Resulting PR-KB Graphics

Figure 1-36. Tilt/Rotate Code (PR-KB)

TILT/ROTATE CODE

Char	EBCDIC Hex	T1	T2	R5	R2A	R2	R1	Upper Case
¢	4A	0	0	0	0	0	0	1
.	4B	0	0	0	0	0	0	0
<	4C	1	1	1	1	1	0	1
(	4D	1	1	1	1	1	1	1
+	4E	1	1	0	1	1	0	1
|	4F	1	1	0	1	1	1	1
&	50	1	0	0	1	1	1	0
!	5A	1	0	0	0	0	0	1
$	5B	1	0	0	0	0	0	0
*	5C	1	1	1	1	0	0	1
)	5D	1	1	1	1	0	1	1
;	5E	1	1	0	1	0	0	1
¬	5F	1	1	0	1	0	1	1
-	60	0	1	0	1	1	1	0
/	61	0	1	1	1	1	1	0
,	6B	0	1	0	0	0	0	0
%	6C	0	0	0	1	1	1	1
_	6D	0	1	1	1	1	1	1
>	6E	1	0	0	1	1	1	1
?	6F	0	1	0	1	1	1	1
:	7A	0	1	0	0	0	0	1
#	7B	1	1	0	0	0	0	0
@	7C	0	0	0	1	1	1	0
▼	7D	1	1	1	0	0	1	1
=	7E	1	1	0	0	0	0	1
"	7F	1	1	0	0	0	1	1
a	81	0	0	1	1	1	1	0
b	82	0	0	0	1	1	0	0
c	83	0	0	1	1	1	0	0
d	84	0	0	0	1	0	1	0
e	85	0	0	1	1	0	1	0

Char	EBCDIC Hex	T1	T2	R5	R2A	R2	R1	Upper Case
f	86	0	0	0	1	0	0	0
g	87	0	0	1	1	0	0	0
h	88	0	0	1	0	0	1	0
i	89	0	0	0	0	0	1	0
j	91	1	0	1	1	1	1	1
k	92	1	0	0	1	1	0	0
l	93	1	0	1	1	1	0	0
m	94	1	0	0	1	0	1	0
n	95	1	0	1	1	0	1	0
o	96	1	0	0	1	0	0	0
p	97	1	0	1	1	0	0	0
q	98	1	0	1	0	0	1	0
r	99	1	0	0	0	0	1	0
s	A2	0	1	0	1	1	0	0
t	A3	0	1	1	1	1	0	0
u	A4	0	1	0	1	0	1	0
v	A5	0	1	1	1	0	1	0
w	A6	0	1	0	1	0	0	0
x	A7	0	1	1	1	0	0	0
y	A8	0	1	1	0	0	1	0
z	A9	0	1	0	0	0	1	0
0	F0	1	1	0	1	1	1	0
1	F1	1	1	1	1	1	1	0
2	F2	1	1	0	1	1	0	0
3	F3	1	1	1	1	1	0	0
4	F4	1	1	0	1	0	1	0
5	F5	1	1	1	1	0	1	0
6	F6	1	1	0	1	0	0	0
7	F7	1	1	1	1	0	0	0
8	F8	1	1	1	0	0	1	0
9	F9	1	1	0	0	0	1	0

Note: For alphabetic characters, only the lowercase is shown. The tilt/rotate code for an uppercase alphabetic character is the same as the corresponding lowercase character.

Table Addr	Char	EBCDIC Hex	Table Addr	Char	EBCDIC Hex
50B8	Space	40	D8	—	6D
B9	=	7E	D9	J	D1
BA	<	4C	DA	K	D2
BB	;	5E	DB	L	D3
BC	:	7A	DC	M	D4
BD	%	6C	DD	N	D5
BE	'	7D	DE	O	D6
BF	>	6E	DF	P	D7
CO	*	5C	E0	Q	D8
C1	(	4D	E1	R	D9
C2	)	5D	E2	$	5B
C3	"	7F	E3	!	5A
C4	Space	00	E4	—	60
C5	Space	00	E5	New Line	15
C6	0	F0	E6	BKSP (Not used)	16
C7	#	7B	E7	Space	00
C8	¢	4A	E8	+	4E
C9	?	6F	E9	A	C1
CA	S	E2	EA	B	C2
CB	T	E3	EB	C	C3
CC	U	E4	EC	D	C4
CD	V	E5	ED	E	C5
CE	W	E6	EE	F	C6
CF	X	E7	EF	G	C7
D0	Y	E8	F0	H	C8
D1	Z	E9	F1	I	C9
D2	,	6B	F2	.	4B
D3	|	4F	F3	¬	5F
D4	@	7C	F4	&	50
D5	LF (not used)	25	F5	H. Tab (not used)	05
D6	Space	00			
D7	Space	00			

Figure 1-37. PR-KB Translate Table (Keyboard Code to EBCDIC)

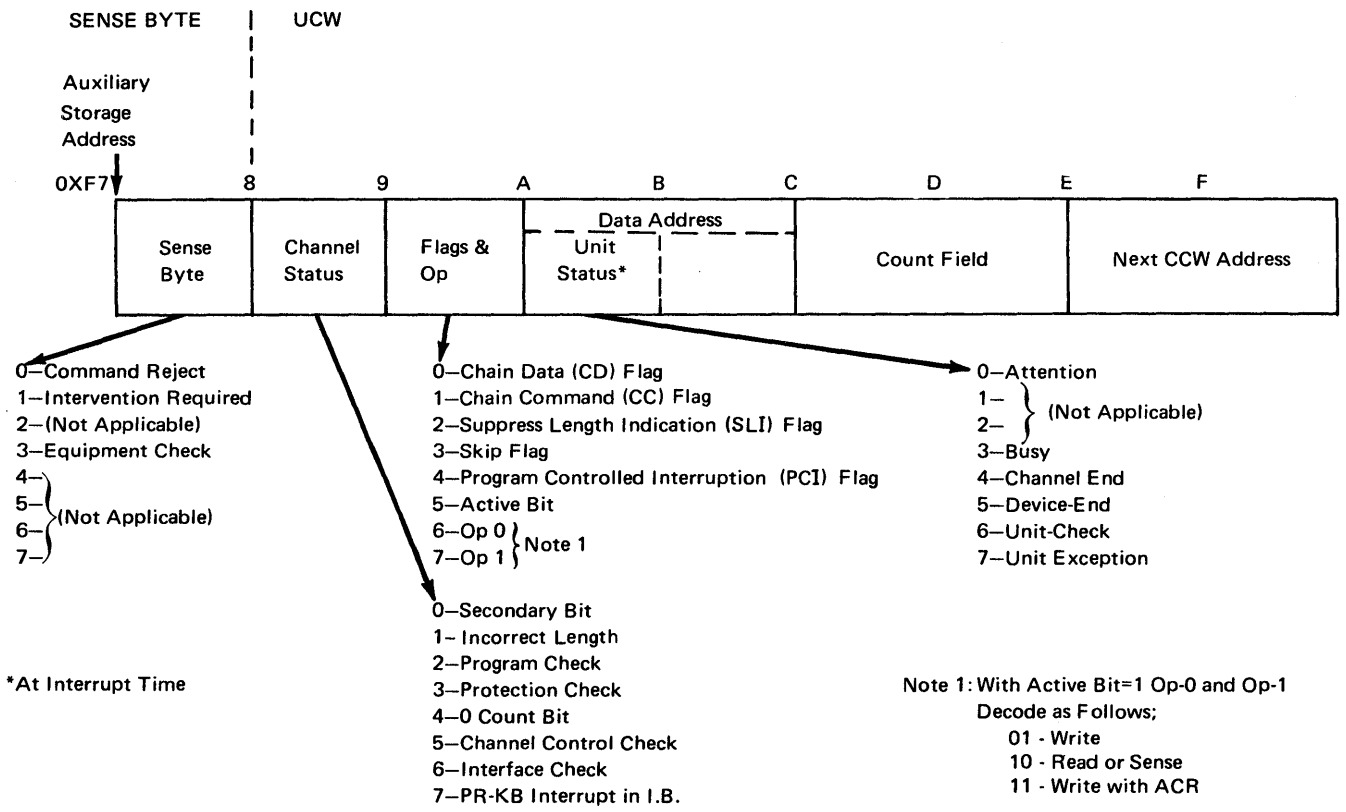


Figure 1-38. PR-KB Sense Byte and Unit Control Word -- UCW Format

1.7 CONTROL WORDS (MICRO) FIGURES 1-39 THROUGH 1-46

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Set/Reset	0	0	Reset/Set	K High 0	CS-Field 0	1	2	3	K-Low 0	1	2	3	K-High 1	2	3	0
Arithmetic/ Constant	0	0	CD-Fld 0	1	AS-Field 0	1	2	3	K-Field 0	1	2	3	CC-Field 0	1	2	1
Storage	0	1	RCS RAS SCS SAS		AS-Field 0	1	2	Byte Select 3	BS-Field 0	1	2	Main Stor	MC-Field 0	1	2	0
Move/ Arithmetic	0	1	CD-Fld 0	1	AS-Field 0	1	2	3	BS-Field 0	1	2	3	CC-Field 0	1	2	1
Branch Unconditional	1	0	RP0 2	3	4	5	6	7	RP1 0	1	2	3	4	5	6	0
Branch on Mask	1	0	Mask 0	1	AS-Field 0		ST/X	2	3	LS/Ext	RP1 1	2	0	RP0 5	6	7	1
Branch on Condition	1	1	BC-Fld 0	1	AS-Field 0		ST/X	2	3	LS/Ext	RP1 1	2	3	4	5	6	Test

Figure 1-39. Control-Word Alignment

WORD TYPE			K HIGH	SET/RST SOURCE FIELD				B SOURCE OR K LOW FIELD				K HIGH FIELD			
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0 = RST 1 = SET	K HIGH 0 BIT	0000 = S REGISTER 0010 = MMSK REGISTER 0100 = MODE REGISTER 0110 = BC FACILITY 1000 = DR REGISTER			ALL MODES ALL MODES ALL MODES ALL MODES ALL MODES	WHEN MMSK ADDRESSED FOR A LINK OR RETURN FUNCTION, THE B SOURCE DECODES ARE FOR LOCAL STORAGE 0000 = U REGISTER 0010 = V REGISTER 0100 = G REGISTER 0110 = D REGISTER 1000 = I REGISTER 1010 = T REGISTER 1100 = P REGISTER 1110 = H REGISTER WHEN USED AS THE K FIELD BIT 8 = K LOW BIT 0 BIT 9 = K LOW BIT 1 BIT 10 = K LOW BIT 2 BIT 11 = K LOW BIT 3				1 BIT	2 BIT	3 BIT	0
				1001 = RPD 1011 = DIAB 1011 = R 1011 = GA 1100 = DIAC 1101 = PRA 1101 = FIA 1101 = RP 1101 = CSETF 1101 = GB 1110 = FIB 1111 = CPF 1111 = PRB 1111 = TA 1111 = FIC 1111 = P 1111 = CCTRL 1111 = GC	FACILITY 2540 MODE FACILITY 2311 MODE FACILITY 2540 MODE FACILITY CHNL MODE FACILITY 2311 MODE FACILITY 1403 MODE FACILITY 2311 MODE FACILITY 2540 MODE FACILITY COMM MODE FACILITY CHNL MODE FACILITY 2311 MODE FACILITY CPU MODE FACILITY 1403 MODE FACILITY 1052 MODE FACILITY 2311 MODE FACILITY 2540 MODE FACILITY COMM MODE FACILITY CHNL MODE										

WHEN THE MMSK REGISTER IS ADDRESSED BY THE SET/RST SOURCE FIELD, CONTROL WORD BIT 11 = 0 INDICATES A LINK OR RETURN FUNCTION. BIT 11 = 1 INDICATES NO LINK OR RETURN FUNCTION.

Figure 1-40. Set/Reset Word (Word Type 0)

WORD TYPE		FUNCTION DECODE		A-SOURCE FIELD		FIELD		FUNCTION DECODE		WORD TYPE
0	1	2	3	4 5 6 7		8 9 10 11		12 13 14		15
0	0	0	0	0000 = U0		0000		000 - Z = A + KL	ADD	1
		0	0	0001 = U1		0001		001 - Z = A*-KL		
		0	0	0010 = V0		0010		010 - Z = A*-KH		
		0	0	0011 = V1		0011		011 - Z = A*-KK		
		0	0	0100 = G0		0100		100 - Z = A + KH		
		0	0	0101 = G1		0101		101 - Z = A ¤ KL		
		0	0	0110 = D0		0110		110 - Z = A ¤ KH		
		0	0	0111 = D1		0111		111 - Z = A ¤ KK	XOR	
				1000 = I0		1000				
		0	1	1001 = I1		1001		000 - A = 0 + KL		
		0	1	1010 = T0		1010		001 - A = A*-KL		
		0	1	1011 = T1		1011		010 - A = A*-KH		
		0	1	1100 = P0		1100		011 - A = A*-KK		
		0	1	1101 = P1		1101		100 - A = 0 + KH		
		0	1	1110 = H0		1110		101 - A = A ¤ KL		
		0	1	1111 = H1		1111		110 - A = A ¤ KH		
		0	1					111 - A = A ¤ KK		
		1	0					000 - A = 0 - KL		
		1	0					001 - A = 0$KL		
		1	0					010 - A = 0$KH		
		1	0					011 - A = 0$KK		
		1	0					100 - A = A - KH		
		1	0					101 - A = A + KL		
		1	0					110 - A = A + KH		
		1	0					111 - A = A + KK		
		1	1					000 - A = 0 - KL		
		1	1					001 - A = 0$KL		
		1	1					010 - A = 0$KH		
		1	1					011 - A = 0$KK		
		1	1					100 - A = 0 - KH		
		1	1					101 - A = A - KL		
		1	1					110 - A = A - KH		
		1	1					111 - A = A - KK		

THE FUNCTION DECODE IS A COMBINATION OF CONTROL WORD BITS 2, 3, 12, 13, AND 14.

THE -A- SYMBOL IN THE FORMULAS UNDER COLUMNS 12, 13, AND 14 CAN BE ANY OF THE LOCAL STORAGE BYTE SOURCES LISTED UNDER THE A-SOURCE FIELD.

THE SYMBOL ¤ IN THE FORMULAS UNDER COLUMNS 12, 13, AND 14 INDICATES AN EXCLUSIVE -OR0 FUNCTION.

THE $ SYMBOL IN THE FORMULAS UNDER COLUMNS 12, 13, AND 14 INDICATE S AN OR FUNCTION.

THE *-SYMBOL IN THE FORMULAS UNDER COLUMNS 12, 13, AND 14 INDICATES A COMPLEMENT AND FUNCTION.

Figure 1-41. Arithmetic Constant Word (Word Type 1)

Figure 1-42. Storage Word (Word Type 2)

WORD TYPE		STORAGE CONTROL		DATA REGISTER ADDRESS				ADDRESS REGISTER OR K FIELD				MODIFIER CONTROL			WORD TYPE
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
0	1	00 = READ CONTROL 01 = READ AUX OR PROGRAM 10 = STORE CNTL 11 = STORE AUX OR PROGRAM		THIS FIELD MAY ADDRESS LOCAL STORAGE FOR A BYTE OR HALFWORD. BYTE SELECTION OF LOCAL STORAGE IS LIMITED TO THE ODD ADDRESSES. HALFWORD SELECTION IS LIMITED TO EVEN ADDRESS EXTERNAL FACILITY ADDRESSING IS ALWAYS DONE IN BYTE MODE. THEREFORE ONLY THE EXTERNALS WITH ODD ADDRESSES CAN BE ACCESSED.				FOR INDIRECT ADDRESSING THE ADDRESS REGISTER SELECTED BY THIS FIELD IS A HALFWORD LOCAL STORAGE REGISTER BIT 11 DOES NOT ENTER INTO THE ADDRESSING OF THE LOCAL STORAGE REGISTER. BUT DOES INDICATE THE FOLLOWING			000 - NO UPDATE 001 - DIRECT ADDRESSING 010 - NO ACCESS, PLUS UPDATE. 011 - NO ACCESS, MINUS UPDATE. 100 - LOCAL STORAGE DATE REG, ACCESS, PLUS UPDATE 101 - LOCAL STORAGE DATE REG, ACCESS, MINUS UPDATE 110 - EXTERNAL DATA REG. ACCESS, PLUS UPDATE 111 - EXTERNAL DATA REG, ACCESS, MINUS UPDATE		0
								BIT 11 / BITS 2,3 / MEANING 0 / 01 / READ AUXILIARY 1 / 01 / READ PROGRAM 0 / 11 / STORE AUXILIARY 1 / 11 / STORE PROGRAM							
		BIT 11 DETERMINES IF THE AUXILIARY STORAGE AREA OR THE PROGRAM STORAGE AREA IS ACCESSED FOR BIT 2, 3 DECODES OF 01 and 11. THIS IS ONLY TRUE WHEN INDIRECTLY ADDRESSING.		LOCAL STORAGE DECODES 0000 - U0 0001 - U1 0010 - V0 0011 - V1 0100 - G0 0101 - G1 0110 - D0 0111 - D1 1000 - I0 1001 - I1 1010 - T0 1011 - T1 1100 - P0 1101 - P1 1110 - H0 1111 - H1				FOR DIRECT ADDRESSING THIS FIELD CONTAINS BIT CODES THAT FORCE THE ADDRESS REGISTER M1 TO SPECIFIC VALUES THESE VALUES ARE –			FOR K ADDRESSABLE AUX M0 = 00000000 CTRL M0 = XX00011 DEPENDENT ON STORAGE SIZE		
		WHEN NO ACCESS TO STORAGE IS DESIGNATED BY THE MODIFIER CONTROL FIELD. BITS 2 and 3 INDICATE THE UPDATE VALUE. BITS 2,3 / VALUE 00 / 0 01 / +OR - 1 10 / +OR - 2 11 / +OR - 2		ALL EVEN ADDRESSES CAN BE USED AS ADDRESS REGISTERS IN THE FIELD DESIGNATED BY CONTROL WORD BITS 8, 9, 10, and 11.				BITS 8,9,10,11 / FORCED M1 VALUES 0000 88 0001 8A 0010 8C 0011 8E 0100 98 0101 9A 0110 9C 0111 9E 1000 A8 1001 AA 1010 AC 1011 AE 1100 B8 1101 BA 1110 BC 1111 BE					

WORD TYPE		FUNCTION DECODE		A SOURCE FIELD		B SOURCE FIELD		FUNCTION DECODE		WORD TYPE
0	1	2	3	4 5 6 7		8 9 10 11		12	13 14	15
0	1	0	0	0000 = U0		0000 = U0		000 -	B = AX ¤ B	1
		0	0	0001 = U1		0001 = U1		001 -	B = AXH + BL	
		0	0	0010 = V0		0010 = V0		010 -	B = AXL $ BH	
		0	0	0011 = V1		0011 = V1		011 -		
		0	0	0100 = G0		0100 = G0		100 -	B = A + B	
		0	0	0101 = G1		0101 = G1		101 -	B = AH + BL	
		0	0	0110 = D0		0110 = D0		110 -	B = AL + BH	
		0	0	0111 = D1		0111 = D1		111 -	EXT = B	
				1000 = I0		1000 = I0				
		0	1	1001 = I1		1001 = I1		000 -	B = AX	
		0	1	1010 = T0		1010 = T0		001 -	B = AXH	
		0	1	1011 = T1		1011 = T1		010 -	B = AXL	
		0	1	1100 = P0		1100 = P0		011 -	B = 0 (STOP)	
		0	1	1101 = P1		1101 = P1		100 -	B = A	
		0	1	1110 = H0		1110 = H0		101 -	B = AH	
		0	1	1111 = H1		1111 = H1		110 -	B = AL	
		0	1					111 -	B = EXT	
		1	0	THE FUNCTION DECODE IS A COMBINATION OF				000 -	A = A ¤ B	
		1	0	CONTROL WORD BITS 2, 3, 12, 13, AND 14-				001 -	A = A + B	
		1	0					010 -	A = A $ B	
		1	0	IF THE FUNCTION DECODE IS EQUAL TO 00111,				011 -	A = A * B	
		1	0	THE A-SOURCE FIELD ADDRESSES AN EXTERNAL				100 -	AC = A + B + 1	
		1	0	FACILITY.				101 -	AC = A + B	
		1	0	IF THE FUNCTION DECODE IS EQUAL TO 01111, THE				110 -	AC = A + B + C	
		1	0	B-SOURCE FIELD ADDRESSES AN EXTERNAL FACILITY.				111 -	AC = AL + B + C	
		1	1	THE SYMBOL -A- USED IN THE FUNCTION DECODE				000 -	A = A - B + 1	
				FORMULAS, REFERS TO ANY OF THE LOCAL STORAGE						
		1	1	SYMBOLS UNDER THE A-SOURCE FIELD.				001 -	A = A - B	
		1	1	THE SYMBOL -B- USED IN THE FUNCTION DECODE				010 -		
				FORMULAS, REFERS TO ANY OF THE LOCAL STORAGE						
		1	1	SYMBOLS UNDER THE B-SOURCE FIELD.				011 -		
		1	1	THE SYMBOL -C- REFERS TO THE ADDER CARRY				100 -	AC = A - B + C	
				(S3) LATCH						
		1	1					101 -	AC = 0 - B + C	
		1	1	THE SYMBOL ¤ INDICATES AN EXCLUSIVE-OR				110 -	AC = A ± B + C	
				FUNCTION.						
		1	1	THE SYMBOL -$- INDICATES AN OR FUNCTION.				111 -	AC = A @ B + C	
				THE SYMBOL -*- INDICATES AN AND FUNCTION.						
				THE SYMBOL -@- INDICATES AN ADD/SUBTRACT						
				DECIMAL FUNCTION.						

Figure 1-43. Move/Arthmetic (Word Type 3)

Figure 1-44. Branch Unconditional Word (Word Type 4)

WORD TYPE		REPLACEMENT BITS FOR THE M0-REGISTER						REPLACEMENT BITS FOR THE M1-REGISTER							WORD TYPE
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	0	BITS 2 THRU 7 OF THIS CONTROL WORD CONTAIN THE VALUES THAT ARE GATED TO BITS 2 THRU 7 OF THE M0-REGISTER WHEN THIS WORD IS EXECUTED WHEN THIS WORD IS GATED INTO THE CONTROL REGISTER, BIT 5 OF THE CONTROL REGISTER IS FORCED TO A 1. THE REPLACEMENT VALUE FOR THE M0-REGISTER BIT 5 POSITION IS GATED FROM THE STORAGE DATA BUS BIT 5 POSITION.						BITS 8 THRU 14 CONTAIN THE VALUES THAT ARE GATED TO BITS 0 THRU 6 OF THE M1-REGISTER WHEN THIS WORD IS EXECUTED							0
		WHEN THIS WORD IS EXECUTED, THE ADDRESS OF THE NEXT SEQUENTIAL CONTROL WORD IS STORED IN THE I-REGISTER OF LOCAL STORAGE ZONE 4.													

WORD TYPE	BRANCH CONTROL	A SOURCE FIELD	REPLACEMENT BITS FOR M1-REGISTER	REPLACEMENT BITS FOR M0-REGISTER	WORD TYPE
0 1	2 3	4 5 6 7	8 9 10 11	12 13 14	15
1 0	C0 = 4 WAY BR- 01 = 8 WAY BR 10 = 2 WAY BR (A SOURCE NOT ZERO) 11 = 16 WAY BR	BIT 5 = 0 MEANS STRAIGHT A-REG GATING. BIT 5 = 1 MEANS CROSS A-REG OUTPUT --- WHEN THIS CONTROL WORD IS READ INTO THE CONTROL REGISTER. BIT 5 IS FORCED TO 1. THIS RESTRICTS THE FACILITIES THAT CAN BE ADDRESSED BY THE A-SOURCE FIELD TO THOSE THAT HAVE AT LEAST BIT 5 = 1 IN THEIR A-SOURCE DECODES. BECAUSE BIT 5 IS FORCED IN THE CONTROL REGISTER, THE TRUE STATUS OF BIT 5 IS TAKEN FROM THE STORAGE DATA BUS OUT, FOR A-REG GATING. EITHER DECODE IN CONTROL STORAGE. — LOCAL STORAGE REGISTER 0000 OR 0100 — G0 0001 OR 0101 — G1 0010 OR 0110 — D0 0011 OR 0111 — D1 1000 OR 1100 — P0 1001 OR 1101 — P1 1010 OR 1110 — H0 1011 OR 1111 — H1 EXTERNAL FACILITIES HAVE THE SAME ADDRESSING RESTRICTIONS.	0 = LS 1 = EXT BIT 9 CONTAINS THE REPLACEMENT VALUE FOR BIT 1 of the M1-REGISTER. BIT 10 CONTAINS THE REPLACEMENT VALUE FOR BIT 2 OF THE M1 REGISTER. BIT 11 CONTAINS THE REPLACEMENT VALUE FOR BIT 0 OF THE M1 REGISTER	BITS 12, 13, AND 14 CONTAIN THE REPLACEMENT VALUES FOR BITS 5, 6, AND 7 OF THE M0 REG.	1

Figure 1-45. Branch on Mask Word (Word Type 5)

Figure 1-46. Branch on Condition Code (Word Type 6 or 7)

WORD TYPE		BIT CONTROL		A SOURCE FIELD					REPLACEMENT BITS FOR THE M1 REGISTER						WORD TYPE
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	1	0C = BIT 0 OR 4 01 = BIT 1 OR 5 10 = BIT 2 OR 6 11 = BIT 3 OR 7		BIT 5 = 0 MEANS STRAIGHT A-REG GATING. BIT 5 = 1 MEANS CROSS A-REG OUTPUT. --- WHEN THIS CONTROL WORD IS READ INTO THE CONTROL REGISTER, BIT 5 IS FORCED TO 1. THIS RESTRICTS THE FACILITIES THAT CAN BE ADDRESSED BY THE A-SOURCE FIELD TO THOSE THAT HAVE AT LEAST BIT 5 = 1 IN THEIR A-SOURCE DECODES. BECAUSE BIT 5 IS FORCED IN THE CONTROL REGISTER, THE TRUE STATUS OF BIT 5 IS TAKEN FROM THE STORAGE DATA BUS OUT, FOR A-REG GATING. EITHER DECODE IN CONTROL STORAGE — LOCAL STORAGE REGISTER 0000 OR 0100 — G0 0001 OR 0101 — G1 0010 OR 0110 — D0 0011 OR 0111 — D1 1000 OR 1100 — P0 1001 OR 1101 — P1 1010 OR 1110 — H0 1011 OR 1111 — H1 EXTERNAL FACILITIES HAVE THE SAME ADDRESSING RESTRICTIONS.		0 = LS 1=Ext	BITS 9--14 CONTAIN THE REPLACEMENT VALUES FOR BITS 1--6 OF THE M1-REGISTER						0= TEST FOR 0 --- 1= TEST FOR 1

1.8 EXTERNAL DECODES, MNEMONICS, AND ADDRESSING (FIGURE 1-47)

This section summarizes the detailed bit definitions of external facilities. AS-decodes followed by asterisk (*) can be tested with the Branch on Condition or Branch on Mask words.

CPU Mode

AS-Field Decode	Ext to CPU	CPU to Ext
0000	SWAB	---
0001	SWCD	---
0010	STP0	STP0
0011	STP1	STP1
0100*	DYN	SM
0101*	S	---
0110*	MMSK	---
0111*	BA	JO
1000	JI	---
1001	XINT	JA
1010	TIM	---
1011	---	---
1100*	DR	---
1101*	---	---
1110*	MC	---
1111*	BB	MW

2311 Disk Mode

AS-Field Decode	Ext to CPU	CPU to Ext
0000	TGRI	---
0001	EBI	---
0010	STP0	STP0
0011	FOB	FEBO
0100*	DYN	---
0101*	DASI	---
0110*	MMSK	---
0111*	BA	---
1000	CHI	---
1001	CLI	MS
1010	TC	---
1011	SDI	TGRO
1100*	FGA	---
1101*	FFI	FFC
1110*	DS	FBO
1111*	FOP	FCP

2540 Punch Mode

AS-Field Decode	Ext to CPU	CPU to Ext
0000	---	---
0001	---	---
0010	STP0	STP0
0011	STP1	STP1
0100*	DYN	---
0101*	S	---
0110*	MMSK	---
0111*	BA	---
1000	RPD1	---
1001	RPD2	---
1010	RP2	---
1011	RP1	---
1100*	---	---
1101*	RS	---
1110*	RPS	---
1111*	PS	PO

1403 Mode

AS-Field Decode	Ext to CPU	CPU to Ext
0000	---	---
0001	---	---
0010	STP0	STP0
0011	STP1	STP1
0100*	DYN	---
0101*	S	---
0110*	MMSK	---
0111*	BA	---
1000	---	---
1001	---	PCCL
1010	PRT	---
1011	PRI	PRO
1100*	---	---
1101*	---	PRC
1110*	PRS	---
1111*	PRD	PR

1052 (PRKB) Mode

AS-Field Decode	Ext to CPU	CPU to Ext
0000	---	---
0001	---	---
0010	STP0	STP0
0011	STP1	STP1
0100*	DYN	---
0101*	S	---
0110*	MMSK	---
0111*	BA	---
1000	---	---
1001	---	---
1010	TI	---
1011	TR	---
1100*	---	---
1101*	TD	---
1110*	TT	---
1111*	TU	TE

Communications Mode

AS-Field Decode	Ext to CPU	CPU to Ext
0000	---	---
0001	---	---
0010	STP0	STP0
0011	STP1	STP1
0100*	DYN	---
0101*	S	CADR
0110*	MMSK	---
0111*	BA	PARCK
1000	---	---
1001	---	LADR
1010	DAIN	---
1011	LAIN	DAOUT
1100*	IACCN	---
1101*	LASTAT	DILOUT
1110*	DIIIN	---
1111*	GSTAT	LAOUT

2540 Reader Mode

AS-Field Decode	Ext to CPU	CPU to Ext
0000	---	---
0001	---	---
0010	STP0	STP0
0011	STP1	STP1
0100*	DYN	---
0101*	S	---
0110*	MMSK	---
0111*	BA	---
1000	RPD1	---
1001	RPD2	---
1010	RP2	---
1011	RP1	---
1100*	---	---
1101*	RS	---
1110*	PRS	---
1111*	PS	PO

Channel Mode

AS-Field Decode	Ext to CPU	CPU to Ext
0000	---	---
0001	---	---
0010	STP0	STP0
0011	STP1	STP1
0100*	DYN	---
0101*	S	---
0110*	MMSK	---
0111*	BA	---
1000	---	---
1001	---	---
1010	---	---
1011	---	---
1100*	GS	---
1101*	GT	---
1110*	GD	---
1111*	GB/IN	GB/OUT

Note: The GA and GB external facilities cannot be displayed directly, but can be displayed in GP, GS, or GT external facilities. GB/IN and GB/OUT have the same external decode.

2560 MFCM Mode

AS-Field Decode	Ext to CPU	CPU to Ext
0000	MFD3(MFD3)**	---
0001	MFD1	MFSS
0010	MFD4(STP0)**	---
0011	MFD2(STP1)**	MFPU
0100*	DYN	---
0101*	S	MFHS
0110*	MMSK	---
0111*	BA	MFPR1
1000	MFR1	---
1001	MFD5	MFPR2
1010	MFR2	---
1011	MFD6	MFPR3
1100*	MFS	---
1101	MFD7	MFPR4
1110*	MFT	---
1111	MFD8	MFPR5

* These fields may be tested with Branch on Condition or Branch on Mask control words.
**Fields in parentheses apply to 2540 Emulate operation.

External Field Definitions, CPU Mode (EXT to CPU)

Console Address Switch 0 (SWAB)
MDM 4-35

0000	0	Switch A bit 0
	1	Switch A bit 1
	2	Switch A bit 2
	3	Switch A bit 3
	4	Switch B bit 0
	5	Switch B bit 1
	6	Switch B bit 2
	7	Switch B bit 3

Console Address Switch 1 (SWCD)
MDM 4-35

0001	0	Switch C bit 0
	1	Switch C bit 1
	2	Switch C bit 2
	3	Switch C bit 3
	4	Switch D bit 0
	5	Switch D bit 1
	6	Switch D bit 2
	7	Switch D bit 3

Storage Protect 0 (STP0)
MDM 4-41

0010	0	STP0 bit 0 (Q0)
	1	STP0 bit 1 (Q1)
	2	STP0 bit 2 (Q2)
	3	STP0 bit 3 (Q3)
	4	STP0 bit 4 (Q4)
	5	STP0 bit 5 (Q5)
	6	STP0 bit 6 (Q6)
	7	STP0 bit 7 (Q7)

Storage Protect 1, Manual Only (STP1)
MDM 4-41

0011	0	STP1 bit 0
	1	STP1 bit 1
	2	STP1 bit 2
	3	STP1 bit 3
	4	STP1 bit 4
	5	STP1 bit 5
	6	STP1 bit 6
	7	STP1 bit 7

Dynamic Condition Register (DYN)
MDM 4-40

0100*	0	Z=0 (DC Bit 0)
	1	Storage wrap latch
	2	OVFL (overflow) (DC Bit 2)
	3	Adder carry (DC Bit 3)
	4	Not hold in (Dir Ctl feat)
	5	Check disable switch
	6	DYN Reg bit 6 (HZ=0) (DC Bit 6)
	7	DYN Reg bit 7 (LZ=0) (DC Bit 7)

Status Register (S)
MDM 4-16

0101*	0	S0 True/Compl latch
	1	S1 Z=nonzero (all arith ops)
	2	S2 Z=nonzero (log, dec, & binary ops)
	3	S3 ALU 0-bit carry
	4	S4 Invalid decimal digit
	5	S5 (general purpose)
	6	S6 Not execute (MDM 4-40)
	7	S7 Not exceptional condition (MDM 4-40)

MMSK Register, Bits 0-7 (MMSK)
MDM 4-15

0110*	0	MMSK0 Channel high trap
	1	MMSK1 2311 disk control trap
	2	MMSK2 Channel low trap
	3	MMSK3 2540 reader trap
	4	MMSK4 2540 punch trap
	5	MMSK5 Comm chnl bit service
	6	MMSK6 Comm chl char service
	7	MMSK7 level 1 priority hold

Branch Conditions (BA)
MDM 4-40

0111*	0	Chnl 0 interruption latch
	1	Mode bit 0
	2	Mode bit 1
	3	Mode bit 2
	4	IPL latch
	5	LS zone bit 0
	6	LS zone bit 1
	7	LS zone bit 2

Direct Control In (JI) **
MDM 4-41

1000	0	Dir In bit 0
	1	Dir In bit 1
	2	Dir In bit 2
	3	Dir In bit 3
	4	Dir In bit 4
	5	Dir In bit 5
	6	Dir In bit 6
	7	Dir In bit 7

External Interruption (XINT) or Dir Ctl **
MDM 4-41

1001	0	Timer interruption (Int Timer feature)
	1	Console interruption
	2	Ext Int or Dir Ctl sig-in, bit 2
	3	Ext Int or Dir Ctl sig-in, bit 3
	4	Ext Int or Dir Ctl sig-in, bit 4
	5	Ext Int or Dir Ctl sig-in, bit 5
	6	Ext Int or Dir Ctl sig-in, bit 6
	7	Ext Int or Dir Ctl sig-in, bit 7

Timer Count (TIM) **
MDM 4-41

1010	0	0
	1	0
	2	0
	3	0
	4	Timer count bit 4
	5	Timer count bit 5
	6	Timer count bit 6
	7	Timer count bit 7

1011 Unassigned

Diagnostic Register (DR)
MDM 4-13

1100*	0	Disable stop on error
	1	Force all A-Reg ALU entries on
	2	Force stor-data parity bits on
	3	Block actual, gen. pseudo I/O trap requests
	4	0
	5	Force external entry to A/B-Regs
	6	PSW Restart Latch
	7	Turn on diag-branch latch

1011* Unassigned

Error Register (MC)
MDM 4-10

1110*	0	File control check
	2	Storage address check
	3	Control word parity latch
	4	Storage data parity latch
	5	ALU error latch
	6	A-Reg parity latch
	7	B-Reg parity latch

Soft-Stop Branch Conditions (BB)
MDM 4-40

1111* 0 Not soft stop
1 Integrated I/O request
2 Not chnl 0 Int (masked)
3 Not Ext Int (masked)
4 Set IC latch
5 Instruction step latch
6 Not chnl 1 Int (masked)
7 Not comm chnl Int (masked)

* These eight fields tested with Branch on Condition or Branch on Mask control words.

** The active level is minus.

External Field Definitions, CPU Mode (CPU to EXT)

0000 Unassigned

0001 Unassigned

Storage Protect 0 (STP0)
MDM 4-41

0010 0 STP0 bit 0 (Q0)
1 STP0 bit 1 (Q1)
2 STP0 bit 2 (Q2)
3 STP0 bit 3 (Q3)
4 STP0 bit 4 (Q4)
5 STP0 bit 5 (Q5)
6 STP0 bit 6 (Q6)
7 STP0 bit 7 (Q7)

Storage Protect 1 (STP1)
MDM 4-41

0011 0 STP1 bit 0
1 STP1 bit 1
2 STP1 bit 2
3 STP1 bit 3
4 STP1 bit 4
5 STP1 bit 5
6 STP1 bit 6
7 STP1 bit 7

System Mask (SM)
MDM 4-50

0100 0 Chnl 0 mask
1 Chnl 1 mask
2 Chnl 2 mask
3 Ignored
4 Ignored
5 Ignored
6 Ignored
7 Ext Int mask

0101 Unassigned

0110 Unassigned

Direct Control -1 (JO)
MDM 4-92

0111 0 Dir Bus Out bit 0
1 Dir Bus Out bit 1
2 Dir Bus Out bit 2
3 Dir Bus Out bit 3
4 Dir Bus Out bit 4
5 Dir Bus Out bit 5
6 Dir Bus Out bit 6
7 Dir Bus Out bit 7

1000 Unassigned

Direct Control -2, Timing (JA)
MDM 4-92

1001 0 0
1 0
2 Sig Out bit 2
3 Sig Out bit 3
4 Sig Out bit 4
5 Sig Out bit 5
6 Sig Out bit 6
7 Sig Out bit 7

1010 Unassigned

1011 Unassigned

1100 Unassigned

1101 Unassigned

1110 Unassigned

MW Bits (2) of AMWP Bits (MW)
MDM 4-50

1111 0 0
1 0
2 0
3 0
4 0
5 Machine check mask
6 Wait state latch
7 0

External Field Definitions, 2311 Disk Mode (EXT to CPU)

Tag Register In (TGRI)
MDM 4-46

0000 0 Set difference
1 Set Cylinder
2 Set head
3 Control
4 Not 2311 trap latch
5 Machine check
6 Storage protect check
7 Storage wrap check

File Bus In (FBI)
MDM 4-46

0001	0	Cyl addrs 128
	1	Cyl addrs 64
	2	Cyl addrs 32
	3	Cyl addrs 16
	4	Cyl addrs 8
	5	Cyl addrs 4
	6	Cyl addrs 2
	7	Cyl addrs 1

2311 Storage Protect Key (STP0)
MDM 4-41

0010	0	STP0 bit 3 (FQ0)
	1	STP0 bit 1 (FQ1)
	2	STP0 bit 2 (FQ2)
	3	STP0 bit 3 (FQ3)
	4	STP0 bit 4 (Q4)
	5	STP0 bit 5 (Q5)
	6	STP0 bit 6 (Q6)
	7	STP0 bit 7 (Q7)

File Out Bus (FCB) - Diagnostic

		Ccntrol	Cyl	Set Hd/Dir	Set Difference
0011	0	Write gate	128	Frwd 1	Not 128
	1	Read gate	64	x	Not 64
	2	Seek start	32	x	Not 32
	3	Restr hd reg	16	x	Not 16
	4	Erase gate	8	Head 8	Not 8
	5	Select head	4	Head 4	Not 4
	6	Return 000	2	Head 2	Not 2
	7	Head adv	1	Head 1	Not 1

Note: Bit 2 can also be Clock Thrcugh K and D.

Dynamic Ccndition Register (DYN)
MDM 4-40

0100*	0	Z=0
	1	Storage wrap latch
	2	OVFL (overflow)
	3	Adder carry
	4	Not hold in (Dir Ctl feat)
	5	Check disable switch
	6	DYN Reg bit 6 (HZ=0)
	7	DYN Reg bit 7 (LZ=0)

Disk Attachment Status In (DASI)
MDM 4-46

0101	0	Compare home address
	1	Skip
	2	Selected or any gated attention
	3	Erase gate
	4	Unusual condition
	5	Status modifier not short search
	6	Control unit end
	7	Control unit busy

MMSK Register, Bits 0-7 (MMSK)
MDM 4-15

0110*	0	MMSK0 Channel high trap
	1	MMSK1 2311 disk control trap
	2	MMSK2 Channel low trap
	3	MMSK3 2540 reader trap
	4	MMSK4 2540 punch trap
	5	MMSK5 Comm chnl bit service
	6	MMSK6 Comm chnl char service
	7	MMSK7 Level 1 priority hold

Branch Conditions (BA)
MDM 4-40

0111*	0	Chnl 0 interruption latch
	1	Mode bit 0
	2	Mode bit 1
	3	Mode bit 2
	4	IPL latch
	5	LS zone bit 0
	6	LS zone bit 1
	7	LS zone bit 2

Counter 1 High in (CHI) - Diagnostic
MDM 4-46

1000	0	Counter position 32,768
	1	Counter position 16,384
	2	Counter position 8,192
	3	Counter position 4,096
	4	Counter position 2,048
	5	Counter positicn 1,024
	6	Counter position 512
	7	Counter position 256

Counter 1 Low In (CLI) - Diagnostic
MDM 4-46

1001	0	Counter position 128
	1	Counter position 64
	2	Counter position 32
	3	Counter position 16
	4	Counter position 8
	5	Counter position 4
	6	Counter position 2
	7	Counter position 1

Terminating Conditions (TC)
MDM 4-46

1010	0	Data check in count **
	1	Track overrun **
	2	No record found **
	3	Missing address mark **
	4	Data check **
	5	Overrun **
	6	Track condition **
	7	0

Serializer/Deserializer In (SDI) - Diag.
MDM 4-46

1011 0 Read buffer position 128
1 Read buffer position 64
2 Read buffer position 32
3 Read buffer position 16
4 Read buffer position 8
5 Read buffer position 4
6 Read buffer position 2
7 Read buffer position 1

File Gated Attention (FGA)
MDM 4-46

1100* 0 Module 0 ***
1 Module 1 ***
2 Module 2 ***
3 Module 3 ***
4 Wrong length record
5 Unit Exception **
6 Flag Bit 6
7 Selected index hold

File Flags In (FFI)
MDM 4-46

1101* 0 Chain data (CD)
1 Command chain (CC)
2 CC or CD and not unusual condition
3 Status modifier
4 Program-controlled interruption (PCI)
5 Interruption latch
6 Interrupt condition
7 Suppress length indicator (SLI)

Disk Status (DS) -- This register is multiplexed for diagnostic uses (MDM 4-345).

Nondiagnostic
1110* 0 Ready **
1 On line **
2 Unsafe **
3 0
4 Trap gate latch **
5 End of cylinder **
6 Low compare
7 Seek incomplete **

Diag Addr 0
0 Write buffer 128
1 Write buffer 64
2 Write buffer 32
3 Write buffer 16
4 Write buffer 8
5 Write buffer 4
6 Write buffer 2
7 Write buffer 1

Diag Addr 1
0 Test unit exception
1 Read Op
2 Erase Op
3 Scan Op
4 Space count Op
5 Home address Op
6 Home address or R0 Op
7 Count Op

Diag Addr 2
0 Key Op
1 Data Op
2 R0 Op
3 Count, key, or data Op
4 Count or key Op
5 Write check Op
6 Standard index
7 Bit ring inhibit

Diag Addr 3
0 CYC code position 1
1 CYC code position 16
2 CYC code position 17
3 CYC code error latch
4 Unequal compare
5 Bit ring 7
6 Write clock bit
7 Write data bit

Diag Addr 4
0 Zone A
1 Zone B
2 Zone 1
3 Zone 2
4 Zone 3
5 Zone 4
6 HA field
7 Count field

Diag Addr 5
0 Key field
1 Data field
2 Flag bit 0
3 Flag bit 6
4 Flag bit 7
5 Counter decode 0
6 Counter decode 1
7 Counter decode 2

Diag Addr 6
0 Counter decode 3
1 Counter decode 4
2 Counter decode 5
3 Counter decode 6
4 Counter decode 7
5 Counter decode 8
6 Counter decode 9
7 Count = 000

File Op Register (FOP)
MDM 4-46

1111* 0 Search high
1 Multiple/track
2 Search high or equal
3 Count
4 Key
5 Data
6 Read
7 Write

* These eight fields tested with Branch on Condition or Branch on Mask control words.

** Any of these bits turn on DASI bit 4.

*** Any of these bits turn on DASI bit 2.

External Field Definitions, 2311 Disk Mode (CPU to EXT)

0000 Unassigned

0001 Unassigned

2311 Storage Protect (key (STP0)

0010 0 STP0 bit 3 (FQ0)
1 STP0 bit 1 (FQ1)
2 STP0 bit 2 (FQ2)
3 STP0 bit 3 (FQ3)
4 STP0 bit 4
5 STP0 bit 5
6 STP0 bit 6
7 STP0 bit 7

File 1400 Emulator Bus Out (FEBO)

0011 0 FEBO bit 0
1 FEBO bit 1
2 FEBO bit 2
3 FEBO bit 3
4 FEBO bit 4
5 FEBO bit 5
6 FEBO bit 6
7 FEBO bit 7

0100 Unassigned

0101 Unassigned

0110 Unassigned

0111 Unassigned

1000 Unassigned

Module Select Register (MS)

1001 0 Module select 0
1 Module select 1
2 Module select 2
3 Module select 3
4 0
5 0
6 0
7 0

1010 Unassigned

Tag Register Out (TGRO)
MDM 4-349

1011 0 Set difference
1 Set cylinder
2 Set head and direction
3 Control
4 0
5 0
6 Trap gate
7 Control single shot

1100 Unassigned

File Flags Out (FFO)

1101 0 Chain data (CD)
1 Command chain (CC)
2 Suppress length indicator (SLI)
3 Skip
4 Program-controlled int (PCI)
5 0
6 0
7 0

File Bus Out (FBO)
MDM 4-349

		Control	Cyl	Set Hd/Dir	Set Difference
1110	0	Write gate	128	Frwd 1	Not 128
	1	Read gate	64	x	Not 64
	**2	Seek start	32	x	Not 32
	3	Rstr hd reg	16	x	Not 16
	4	Erase gate	8	Head 8	Not 8
	5	Select head	4	Head 4	Not 4
	**6	Return 000	2	Head 2	Not 2
	**7	Head adv	1	Head 1	Not 1

** Timed Operations

File Op Register (FOP)

1111 0 Multiple/track
1 Search high
2 Search equal
3 Count
4 Key
5 Data
6 Read
7 Write

External Field Definitions, 2540 Punch Mode (EXT to CPU)

0000 Unassigned

0001 Unassigned

Storage Protect 0 (STP0)
MDM 4-41

0010 0 STP0 bit 0 (Q0)
1 STP0 bit 1 (Q1)
2 STP0 bit 2 (Q2)
3 STP0 bit 3 (Q3)
4 STP0 bit 4 (Q4)
5 STP0 bit 5 (Q5)
6 STP0 bit 6 (Q6)
7 STP0 bit 7 (Q7)

Storage Protect 1 (STP1)
MDM 4-41

0011 0 STP1 bit 0
1 STP1 bit 1
2 STP1 bit 2
3 STP1 bit 3
4 STP1 bit 4
5 STP1 bit 5
6 STP1 bit 6
7 STP1 bit 7

Dynamic Condition Register (DYN)
MDM 4-40

0100* 0 X=0
1 Storage wrap latch
2 OVFL (overflow)
3 Adder carry
4 Not hold in (Dir Ctl feat)
5 Check disable switch
6 DYN Reg bit 6 (HZQ=0)
7 dyn Reg bit 7 (LZ=0)

Status Register (S)
MDM 4-16

0101* 0 S0 True/Compl latch
1 S1 Z=nonzero (all arith ops)
2 S2 Z=nonzero (log, dec, & bin ops)
3 S3 ALU 0-bit carry
4 S4 Invalid decimal digit
5 S5 (general purpose)
6 S6 Not execute
7 S7 Not exceptional condition

MMSK Register, Bits 0-7 (MMSK)
MDM 4-15

0110* 0 MMSK0 Channel high trap
1 MMSK1 2311 disk control trap
2 MMSK2 Channel low trap
3 MMSK3 2540 reader trap
4 MMSK4 2540 punch trap
5 MMSK5 Comm chnl bit service
6 MMSK6 Comm chnl char service
7 MMSK7 Level 1 priority hold

Branch Conditions (BA)
MDM 4-40

0111* 0 Chnl 0 interruption latch
1 Mode bit 0
2 Mode bit 1
3 Mode bit 2
4 IPL latch
5 LS zone bit 0
6 LS zone bit 1
7 LS zone bit 2

Diagnostic R/P Conditions 1 (RPD1)
MDM 4-43

1000 0 R/P tens AR A
1 R/P tens AR B
2 R/P tens AR C
3 R/P tens AR D
4 R/P tens AR E
5 Punch address check
6 Punch overrun latch
7 Punch sync check latch

Diagnostic R/P Conditions 2 (RPD2)
MDM 4-43

1001 0 R/P units AR A
1 R/P units AR B
2 R/P units AR C
3 R/P units AR D
4 R/P units AR E
5 Reader address check
6 Reader overrun latch
7 Reader sync check latch

Reader/Punch Data In 2 (RP2)
MDM 4-110

1010 0 Col 1 RD2 punch check, data in
1 Col 2 RD2 punch check, data in
2 Col 3 RD2 punch check, data in
3 Col 4 RD2 punch check, data in
4 Col 5 RD2 punch check, data in
5 Col 6 RD2 punch check, data in
6 Col 7 RD2 punch check, data in
7 Col 8 RD2 punch check, data in

Reader/Punch Data In 1 (RP1)
MDM 4-110

1011 0 Ccl 1 RD1 PFR data in
1 Col 2 RD1 PFR data in
2 Col 3 RD1 PFR data in
3 Col 4 RD1 PFR data in
4 Col 5 RD1 PFR data in
5 Col 6 RD1 PFR data in
6 Col 7 RD1 PFR data in
7 Col 8 RD1 PFR data in

1100* Unassigned

Reader Branch Ccnditicns (RS)
MDM 4-43

1101* 0 Not gate read complete 2540
1 Not rdr intervention (rdr ready)
2 Unit exception gate reader
3 Reader check
4 Reader validity check
5 Reader device-end (hardware)
6 Reader status request
7 Not 1400 unit exception

Reader/Punch Branch Conditions (RPS)
MDM 4-43

1110* 0 Reader punch on-line
1 2540 rdr trap req (data avail, CSL)
2 Nct 1400 time cut
3 2540 Pch Trap Req/Diag Stacker
4 Punch brush CI
5 Punch decode
6 Reader select latch
7 Punch select latch

Punch Branch Ccnditions (PS)
MDM 4-43

1111* 0 Not punch intervention (pch ready)
1 Not 4-bit mod pull-on
2 PFR unit exception gate
3 Punch equipment check
4 Punch PFR validity
5 Punch device-end (hardware)
6 Punch status request
7 0

* These eight fields tested with Branch on Condition or Branch on Mask ccntrcl words.

External Field Definitions, 2540 Punch Mode (CPU to EXT)

0000 Unassigned

0000 Unassigned

Storage Protect 0 (STP0)

0010 0 STP0 bit 3 (Q0)
1 STP0 bit 1 (Q1)
2 STP0 bit 2 (Q2)
3 STP0 bit 3 (Q3)
4 STP0 bit 4 (Q4)
5 STP0 bit 5 (Q5)
6 STP0 bit 6 (Q6)
7 STP0 bit 7 (Q7)

Storage Protect 1 (STP1)

0011 0 STP1 bit 0
1 STP1 bit 1
2 STP1 bit 2
3 STP1 bit 3
4 STP1 bit 4
5 STP1 bit 5
6 STP1 bit 6
7 STP1 bit 7

0100 Unassigned

0101 Unassigned

0110 Unassigned

0111 Unassigned

1000 Unassigned

1001 Unassigned

1010 Unassigned

1011 Unassigned

1100 Unassigned

1101 Unassigned

1110 Unassigned

Punch Data Out (PO)

1111 0 Pch data cols 1, 9, 17, etc.
1 Pch data cols 2, 10, 18, etc.
2 Pch data cols 3, 11, 19, etc.
3 Pch data cols 4, 12, 20, etc.
4 Pch data cols 5, 13, 21, etc.
5 Pch data cols 6, 14, 22, etc.
6 Pch data cols 7, 15, 23, etc.
7 Pch data cols 8, 16, 24, etc.

External Field Definitions, 1403 Mode (EXT to CPU)

0000 Unassigned
0001 Unassigned

Storage Protect 0 (STP0)
MDM 4-41

0010 0 STP0 bit 0 (Q0)
1 STP0 bit 1 (Q1)
2 STP0 bit 2 (Q2)
3 STP0 bit 3 (Q3)
4 STP0 bit 4 (Q4)
5 STP0 bit 5 (Q5)
6 STP0 bit 6 (Q6)
7 STP0 bit 7 (Q7)

Storage Protect 1 (STP1)
MDM 4-41

0011 0 STP1 bit 0
1 STP1 bit 1
2 STP1 bit 2
3 STP1 bit 3
4 STP1 bit 4
5 STP1 bit 5
6 STP1 bit 6
7 STP1 bit 7

Dynamic Condition Register (DYN)
MDM 4-40

0100* 0 X=0
1 Storage wrap latch
2 OVFL (overflow)
3 Adder carry
4 Not hold in (Dir Ctl feat)
5 Check disable switch
6 DYN Reg bit 6 (HZ=0)
7 DYN Reg bit 7 (LZ=0)

Status Register (S)
MDM 4-16

0101* 0 S0 True/Compl latch
1 S1 Z=nonzero (all arith ops)
2 S2 Z=nonzero (log, dec, & bin ops)
3 S3 ALU 0-bit carry
4 S4 Invalid decimal digit
5 S5 (general purpose)
6 S6 Not execute
7 S7 exceptional condition

MMSK Register, Bits 0-7 (MMSK)
MDM 4-15

0110* 0 MMSK0 Channel high trap
1 MMSK1 2311 disk control trap
2 MMSK2 Channel low trap
3 MMSK3 2540 reader trap
4 MMSK4 2540 punch trap
5 MMSK5 Comm chan bit service
6 MMSK6 Comm chan char service
7 MMSK7 Level 1 priority hold

Branch Conditions (BA)
MDM 4-40

0111* 0 Chnl 0 interruption latch
1 Mode bit 0
2 Mode bit 1
3 Mode bit 2
4 IPL latch
5 LS zone bit 0
6 LS zone bit 1
7 LS zone bit 2

1000 Unassigned

1001 Unassigned

1403 PLBAR Data In (PRT)
MDM 4-207

1010 0 PLBAR 128
1 PLBAR 64
2 PLBAR 32
3 PLBAR 16
4 PLBAR 8
5 PLBAR 4
6 PLBAR 2
7 PLBAR 1

1403 PLB Data In (PRI)
MDM 4-208

1011 0 PLB 128
1 PLB 64
2 PIB 32
3 PLB 16
4 PLB 8
5 PLB 4
6 PLB 2
7 PLB 1

1100* Unassigned

1101* Unassigned

Sense/Status Conditions (PRS)
MDM 4-44

1110* 0 Device-end
1 Print ready
2 Channel 9
3 Channel 12
4 Initial ready
5 Hammer check
6 Parity check
7 Print request

1403 Diagnostic Conditions (PRD) 1

MDM 4-202
1111* Diagnostic Decode 1
0 PCC TR 128
1 PCC TR 64
2 PCC TR 32
3 PCC TR 16
4 PCC TR 8
5 PCC TR 4
6 PCC TR 2
7 PCC TR 1

Diagnostic Decode 2
0 Print Control
1 Print Scan
2 PSS Gate
3 Home Gate
4 SS3 TR
5 Print Compare
6 Last Scan
7 Sync Check Latch

Diagnostic Decode 3
0 Carriage Busy
1 Space Drive
2 Skip Drive
3 Carriage Settling
4 Carriage Brush Reg 8
5 Carriage Brush Reg 4
6 Carriage Brush Reg 2
7 Carriage Brush Reg 1

Diagnostic Decode 4
0 PLC
1 PIB C1
2 PLB C2
3 PIB C3
4 MCS Mode
5 Addr Hd Off
6 E1 Emitter
7 Channel 1 Latch

* These eight fields tested with Branch on Condition or Branch on Mask control words.

External Field Definitions, 1403 Mode (CPU to EXT)

0000 Unassigned

0001 Unassigned

Storage Protect 0 (STP0)

0010 0 STP0 bit 0 (Q0)
1 STP0 bit 1 (Q1)
2 STP0 bit 2 (Q2)
3 STP0 bit 3 (Q3)
4 STP0 bit 4 (Q4)
5 STP0 bit 5 (Q5)
6 STP0 bit 6 (Q6)
7 STP0 bit 7 (Q7)

Storage Protect 1 (STP1)

0011 0 STP1 bit 0
1 STP1 bit 1
2 STP1 bit 2
3 STP1 bit 3
4 STP1 bit 4
5 STP1 bit 5
6 STP1 bit 6
7 STP1 bit 7

0100 Unassigned

0101 Unassigned

0110 Unassigned

0111 Unassigned

1000 Unassigned

Print Character Counter Length (PCCL)

1001 0 Spare
1 Spare
2 PCCL 120
3 PCCL 80
4 PCCL 60
5 PCCL 48
6 PCCL 40
7 PCCL 16

Note: If 00, 40, or 80 is specified by the PCCL=AS Move/Arithmetic word, a graphic-set length of 240 is set. A count of 48 applies to all printers without MCS.

1010 Unassigned

1403 PLB Data Out (PRO)

1011 0 PLB data out 128
1 PLB data out 64
2 PLB data out 32
3 PLB data out 16
4 PLB data out 8
5 PLB data out 4
6 PLB data out 2
7 PLB data out 1

1100 Unassigned

1403 Carriage Data Out (PRC)

1101 0 Skip
1 Carriage control 8
2 Carriage control 4
3 Carriage control 2
4 Carriage control 1
5 0
6 Set carr-busy if 6-7 bcth cn
7 Set carr-busy if 6-7 both on

1110 Unassigned

1403 PLBAR Data Out (PR)

1111 0 PLB AR data out 128
1 PLB AR data out 64
2 PLB AR data out 32
3 PLB AR data out 16
4 PLB AR data out 8
5 PLB AR data out 4
6 PLB AR data out 2
7 PLB AR data out 1

External Field Definitions, Console Printer-Keyboard Mode (EXT to CPU)

0000 Unassigned

0001 Unassigned

Storage Protect 0 (STP0)
MDM 4-41

0010 0 STP0 bit 0 (Q0)
1 STP0 bit 1 (Q1)
2 STP0 bit 2 (Q2)
3 STP0 bit 3 (Q3)
4 STP0 bit 4 (Q4)
5 STP0 bit 5 (Q5)
6 STP0 bit 6 (Q6)
7 STP0 bit 7 (Q7)

Storage Protect 1 (STP1)
MDM 4-41

0011 0 STP1 bit 0
1 STP1 bit 1
2 STP1 bit 2
3 STP1 bit 3
4 STP1 bit 4
5 STP1 bit 5
6 STP1 bit 6
7 STP1 bit 7

Dynamic Condition Register (DYN)
MDM 4-40

0100* 0 Z=0
1 Storage wrap latch
2 OVFL (overflow)
3 Adder carry
4 Not hold in (Dir Ctl Feat)
5 Check disable switch
6 DYN Reg bit 6 (HZ=0)
7 DYN Reg bit 7 (LZ=0)

Status Register (S)
MDM 4-16

0101* 0 S0 True/compl latch
1 S1 Z=nonzero (all arith ops)
2 S2 Z=nonzero (log, dec, & bin ops)
3 S3 ALU 0-bit carry
4 S4 Invalid decimal digit
5 S5 (general purpose)
6 S6 Not execute
7 S7 Not exceptional condition

MMSK Register, Bits 0-7 (MMSK)
MDM 4-15

0110* 0 MMSK0 Channel high trap
1 MMSK1 2311 disk control trap
2 MMSK2 Channel low trap
3 MMSK3 2540 reader trap
4 MMSK4 2540 punch trap
5 MMSK5 Comm chnl bit service
6 MMSK6 Comm chnl char service
7 MMSK7 Level 1 priority hold

Branch Conditions (BA)
MDM 4-40

0111* 0 Chnl 0 interruption latch
1 Mode bit 0
2 Mode bit 1
3 Mode bit 2
4 IPL latch
5 LS zone 0
6 LS zone 1
7 LS zone 2

1000 Unassigned

1001 Unassigned

1052 Data In (TI)
MDM 4-73

1010 0 Uppercase store latch (bits 0-1)
1 Uppercase store latch (bits 0-1)
2 KB bit B
3 KB bit A
4 KB bit 8
5 KB bit 4
6 KB bit 2
7 KB bit 1
P KB bit C

1052 Tilt/Rotate Register (TR)
MDM 4-74

1011	0	Tilt bit 1
	1	Tilt bit 2
	2	Rotate bit 5
	3	Rotate bit 2A
	4	Rotate bit 2
	5	Rotate bit 1
	6	Uppercase character
	7	Function cycle

1100* Unassigned

PRKB Diagnostic Branch Conditions (TD)
MDM 4-75

1101*	0	0
	1	0
	2	Read/write share latch
	3	New line latch
	4	Key switch (On), CE mode
	5	Shift cycle latch
	6	Lowercase decode
	7	Uppercase decode

PRKB Branch Conditions (TT)
MDM 4-71

1110*	0	Attn Request key
	1	Not-ready to ready
	2	Intervention required
	3	Alter/display
	4	Keyboard check
	5	Alternate coding key
	6	PRKB request
	7	Logout latch

PRKB Branch Conditions (TU)
MDM 4-71

1111*	0	Read latch
	1	Write latch
	2	Microforce (Int Stkd)
	3	Alter/display active
	4	Cycle interlock latch
	5	Data ready latch
	6	Initialize printer
	7	Printer busy

* These eight fields tested with Branch on condition or Branch on Mask control words.

External Field Definitions, Console Printer-Keyboard Mode (CPU TO EXT)

0C00 Unassigned

0001 Unassigned

Storage Protect 0 (STP0)

0010	0	STP0 bit 0 (Q0)
	1	STP0 bit 1 (Q1)
	2	STP0 bit 2 (Q2)
	3	STP0 bit 3 (Q3)
	4	STP0 bit 4 (Q4)
	5	STP0 bit 5 (Q5)
	6	STP0 bit 6 (Q6)
	7	STP0 bit 7 (Q7)

Storage Protect 1 (STP1)

0011	0	STP1 bit 0
	1	STP1 bit 1
	2	STP1 bit 2
	3	STP1 bit 3
	4	STP1 bit 4
	5	STP1 bit 5
	6	STP1 bit 6
	7	STP1 bit 7

0100 Unassigned

0101 Unassigned

0110 Unassigned

0111 Unassigned

1000 Unassigned

1001 Unassigned

1010 Unassigned

1011 Unassigned

1100 Unassigned

1101 Unassigned

1110 Unassigned

PRKB Data Out (TE)

1111	0	TE bit 0
	1	TE bit 1
	2	TE bit 2
	3	TE bit 3
	4	TE bit 4
	5	TE bit 5
	6	TE bit 6
	7	TE bit 7

External Field Definitions, Communication Mode (EXT TO CPU)

0000 Unassigned

0001 Unassigned

Storage Protect 0 (STP0)
MDM 4-90

0010	0	STP0 bit 0 (HQ0)
	1	STP0 bit 1 (HQ1)
	2	STP0 bit 2 (HQ2)
	3	STP0 bit 3 (HQ3)
	4	STP0 bit 4 (Q4)
	5	STP0 bit 5 (Q5)
	6	STP0 bit 6 (Q6)
	7	STP0 bit 7 (Q7)

Storage 1 (STP1)
MDM 4-41

0011	0	STP1 bit 0
	1	STP1 bit 1
	2	STP1 bit 2
	3	STP1 bit 3
	4	STP1 bit 4
	5	STP1 bit 5
	6	STP1 bit 6
	7	STP1 bit 7

Dynamic Condition Register (DYN)
MDM 4-40

0100*	0	Z=0
	1	Storage wrap latch
	2	CVFI (overflow)
	3	Adder carry
	4	Not hold in (Dir Ctl Feat)
	5	Check disable switch
	6	DYN reg bit 6 (HZ=0)
	7	DYN Reg bit 7 (LZ=0)

Status Register (S)
MDM 4-16

0101*	0	S0 True/compl latch
	1	S1 Z=nonzero (all arith ops)
	2	S2 Z=nonzero (log, dec, & bin ops)
	3	S3 ALU 0-bit carry
	4	S4 Invalid decimal digit
	5	S5 (general purpose)
	6	S6 Not execute
	7	S7 Not exceptional conditicn

MMSK Register, Bits 0-7 (MMSK)
MDM 4-15

0110*	0	MMSK0 Channel high trap
	1	MMSK1 2311 disk control trap
	2	MMSK2 Channel low trap
	3	MMSK3 2540 reader trap
	4	MMSK4 2540 punch trap
	5	MMSK5 Comm chnl bit serv
	6	MMSK6 Comm chnl char serv
	7	MMSK7 level 1 priority hold

Branch Conditions (BA)
MDM 4-40

0111*	0	Chnl 0 interruption latch
	1	Mode bit 0
	2	Mode bit 1
	3	Mode bit 2
	4	IPL latch
	5	LS zone bit 0
	6	LS zone bit 1
	7	LS zone bit 2

1000		Unassigned
1001		Unassigned

Data In (DAIN)
MDM 4-47

1010	0	Sync data in bit 0
	1	Sync data in bit 1
	2	Sync data in bit 2
	3	Sync data in bit 3
	4	Sync data in bit 4
	5	Sync data in bit 5
	6	Sync data in bit 6
	7	Sync data in bit 7

Line Address In (LAIN)
MDM 4-47

1011	0	Comm line address in bit 0
	1	Comm line address in bit 1
	2	Comm line address in bit 2
	3	Comm line address in bit 3
	4	Comm line address in bit 4
	5	0
	6	0
	7	0

Line Adapter Conditions (LACON)
MDM 4-47

		Sync	Start/Stop
1100*	0	IA Enable latch	LA Enable latch
	1	Sync Clock Ind.	
	2	Even/odd parity	Even/odd parity
	3	Leased/switched	L'S'D/SW'D NETWORK
	4	Interface A/B	Bit overflow
	5	Test Mode latch	Recv bit buffer
	6	Transmit latch	
	7	Req to send lat	

Line Adapter Status (LASTAT)
MDM 4-47

		Sync	Start/Stop
1101*	0	Clr to send off	Clear to send off
	1	Data set rdy on	Data set ready on
	2	Sync Char trap	TC type II/I
	3	Char overflow	Type TTY/IBM
	4	Char phase	Transmit latch
	5	1-sec timeout trap	Transmit line trigger (mrk/sp)
	6	3-sec timeout trap	Line quiet; recv line (mark/space)
	7	Sync chain trap	Telegr line adptr

Dial In (DILIN)
MDM 4-47

1110*	0	Not Pwr Indicator on (PWI)
	1	Not Abandon Call and Retry (ACR)
	2	Not Present Next Digit (PND)
	3	Not Digit Present (DPR)
	4	Not Call Reqst (CRQ); or Not Diag NBRB (if DPR on)
	5	Not Dial NBR4 (diag)
	6	Not Diag NBR2 (diag)
	7	Valid address; dial NBR1 (if DPR on)

General Status (GSTAT)
MDM 4-47

1111*	0	Sync trap
	1	Start/stop chain trap
	2	Start/stop Data set ready trap
	3	Dial trap
	4	Start/stop char trap
	5	Timeout update trap
	6	
	7	Timeout remember

* These eight fields tested with Branch on Condition or Branch on Mask control words.

External Field Definitions, Communication Mode (CPU TO EXT)

0C00 Unassigned

0001 Unassigned

Storage Protect 0 (STP0)

0010	0	STP0 bit 0 (Q0)
	1	STP0 bit 1 (Q1)
	2	STP0 bit 2 (Q2)
	3	STP0 bit 3 (Q3)
	4	STP0 bit 4 (Q4)
	5	STP0 bit 5 (Q5)
	6	STP0 bit 6 (Q6)
	7	STP0 bit 7 (Q7)

Storage Protect 1 (STP1)

0011	0	STP1 bit 0 (Q0)
	1	STP1 bit 1 (Q1)
	2	STP1 bit 2 (Q2)
	3	STP1 bit 3 (Q3)
	4	STP1 bit 4 (Q4)
	5	STP1 bit 5 (Q5)
	6	STP1 bit 6 (Q6)
	7	STP1 bit 7 (Q7)

0100 Unassigned

Communications Adptr Diag Register (CADR)

0101	0	Bit trap check
	1	General trap
	2	First priority-check trap
	3	
	4	
	5	
	6	
	7	

0110 Unassigned

Communications Parity Check (PARCK)

0111	0	Data bit 0
	1	Data bit 1
	2	Data bit 2
	3	Data bit 3
	4	Data bit 4
	5	Data bit 5
	6	Data bit 6
	7	Data bit 7

1000 Unassigned

Line Adapter Diag Register (LADR)

		Sync	Start/Stop
1001	0	Sync Diag ctls	Adpt Grp Test Ocs
	1	Gate A-Reg DAIN	Adpt Grp Test Ocs
	2	Gate B-Reg DAIN	
	3	Gate TRCR to DAIN	
	4	Gate Diag Stat-DAIN	
	5	Recv data mark diag	
	6	Select diag clock	
	7	Diag clock	

1010 Unassigned

Data Out (DAOUT)

1011	0	Data out bit 0 (sync)
	1	Data out bit 1 (sync)
	2	Data out bit 2 (sync)
	3	Data out bit 3 (sync)
	4	Data out bit 4 (sync)
	5	Data out bit 5 (sync)
	6	Data out bit 6 (sync)
	7	Data out bit 7 (sync)

1100 Unassigned

Dial Out (DILOUT)

1101 0 Diag 1
1 Diag 2
2 Direct present (DPR)
3 Call request (CRQ)
4 Dial digit NBR8
5 Dial digit NBR4
6 Dial digit NBR2
7 Dial digit NBR1

1110 Unassigned

Line Address Out (LAOUT)

1111 0 LAOUT bit 0
1 IAOUT bit 1
2 IAOUT bit 2
3 LAOUT bit 3
4 IAOUT bit 4
5
6
7

External Field Definitions, 2540 Reader Mode (EXT TO CPU)

0000 Unassigned

0001 Unassigned

Storage Protect 0 (STP0)

0010 0 STP0 bit 0 (Q0)
1 STP0 bit 1 (Q1)
2 STP0 bit 2 (Q2)
3 STP0 bit 3 (Q3)
4 STP0 bit 4 (Q4)
5 STP0 bit 5 (Q5)
6 STP0 bit 6 (Q6)
7 STP0 bit 7 (Q7)

Storage Protect 1 (STP1)

0011 0 STP1 bit 0
1 STP1 bit 1
2 STP1 bit 2
3 STP1 bit 3
4 STP1 bit 4
5 STP1 bit 5
6 STP1 bit 6
7 STP1 bit 7

Dynamic Condition Register (DYN)

0100* 0 Z=0
1 Storage wrap latch
2 CVFL (overflow)
3 Adder carry
4 Not hold in (Dir Ctl Feat)
5 Check disable switch
6 DYN Reg bit 6 (HZ=0)
7 DYN Reg bit 7 (LZ=0)

Status Register (S)

0101* 0 S0 True/compl latch
1 S1 Z=nonzero (all arith ops)
2 S2 Z=nonzero (log, dec, & bin ops)
3 S3 ALU 0-bit carry
4 S4 Invalid decimal digit
5 S5 (general purpose)
6 S6 Not execute
7 S7 Not exceptional condition

MMSK Register, Bits 0-7 (MMSK)

0110* 0 MMSK0 Channel high trap
1 MMSK1 2311 disk control trap
2 MMSK2 Channel low trap
3 MMSK3 2540 reader trap
4 MMSK4 2540 punch trap
5 MMSK5 Comm chnl bit service
6 MMSK6 Comm chnl char service
7 MMSK7 Level 1 priority hold

Branch Conditions (BA)

0111* 0 Chnl 0 interruption latch
1 Mode bit 0
2 Mode bit 1
3 Mode bit 2
4 IPL latch
5 LS zone bit 0
6 LS zone bit 1
7 LS zone bit 2

Diagnostic R/P Conditions 1 (RPD1)
MDM 4-43

1000 0 R/P tens AR A
1 R/P tens AR B
2 R/P tens AR C
3 R/P tens AR D
4 R/P tens AR E
5 Punch address check
6 Punch overrun latch
7 Punch sync check latch

Diagnostic R/P Conditions 2 (RPD2)
MDM 4-43

1001	0	R/P units AR A
	1	R/P units AR B
	2	R/P units AR C
	3	R/P units AR D
	4	R/P units AR E
	5	Reader address check
	6	Reader overrun latch
	7	Reader sync check latch

Reader/Punch Data in 2 (RP2)
MDM 4-110

1010	0	Col 1 RD2 punch check data in
	1	Col 2 RD2 punch check data in
	2	Col 3 RD2 punch check data in
	3	Col 4 RD2 punch check data in
	4	Col 5 RD2 punch check data in
	5	Col 6 RD2 punch check data in
	6	Col 7 RD2 punch check data in
	7	Col 8 RD2 punch check data in

Reader/Punch Data In 1 (RP1)
MDM 4-110

1011	0	Col 1 RD1 PFR dat in
	1	Col 2 RD1 PFR data in
	2	Col 3 RD1 PFR data in
	3	Col 4 RD1 PFR data in
	4	Col 5 RD1 PFR data in
	5	Col 6 RD1 PFR data in
	6	Col 7 RD1 PFR data in
	7	Col 8 RD1 PFR data in

1100* Unassigned

Reader Branch Conditions (RS)
MDM 4-43

1101*	0	Not gate read complete 2540
	1	Not reader intervention (rdr ready)
	2	Unit exception gate reader
	3	Reader check
	4	Reader validity check
	5	Reader device end (hardware)
	6	Reader status request
	7	Not 1400 unit exception

Reader/Punch Branch Conditions (RPS)
MDM 4-43

1110*	0	Reader punch on-line
	1	2540 rdr trap req (data avail, CSL)
	2	Not 1400 timeout
	3	0
	4	Punch brush CI
	5	Punch decode
	6	Reader select latch
	7	Punch select latch

Punch Branch Conditions (PS)
MDM 4-43

1111*	0	Not pch intervention (pch ready)
	1	Not 4-bit mod pull-on
	2	PFR unit exception gate
	3	Punch equipment check
	4	Punch PFR validity
	5	Punch device end (hardware)
	6	Punch status request
	7	0

* These eight fields tested with Branch on Condition or Branch on Mask control words.

External Field Definitions, 2540 Reader Mode (CPU TO EXT)

0000 Unassigned

0001 Unassigned

Storage Protect 0 (STP0)

0010	0	STP0 bit 0 (Q0)
	1	STP0 bit 1 (Q1)
	2	STP0 bit 2 (Q2)
	3	STP0 bit 3 (Q3)
	4	STP0 bit 4 (Q4)
	5	STP0 bit 5 (Q5)
	6	STP0 bit 6 (Q6)
	7	STP0 bit 7 (Q7)

Storage Protect 1 (STP1)

0011	0	STP1 bit 0
	1	STP1 bit 1
	2	STP1 bit 2
	3	STP1 bit 3
	4	STP1 bit 4
	5	STP1 bit 5
	6	STP1 bit 6
	7	STP1 bit 7

0100 Unassigned

0101 Unassigned

0110 Unassigned

0111 Unassigned

1000 Unassigned

1001 Unassigned

1010 Unassigned

1011 Unassigned

1100 Unassigned

1101 Unassigned

1110 Unassigned

Punch Data Out (PO)

1111 0 PO bit 0
1 PO bit 1
2 PO bit 2
3 PO bit 3
4 PO bit 4
5 PO bit 5
6 PO bit 6
7 PO bit 7

External Field Definitions, Channel Mode (EXT TO CPU)

0000 Unassigned

0001 Unassigned

Storage Protect 0 (STP0)
MDM 4-90

0010 0 STP0 bit 0 (GQ0)
1 STP0 bit 1 (GQ1)
2 STP0 bit 2 (GQ2)
3 STP0 bit 3 (GQ3)
4 STP0 bit 4 (Q4)
5 STP0 bit 5 (Q5)
6 STP0 bit 6 (Q6)
7 STP0 bit 7 (Q7)

Storage Protect 1 (STP1)
MDM 4-41

0011 0 STP1 bit 0
1 STP1 bit 1
2 STP1 bit 2
3 STP1 bit 3
4 STP1 bit 4
5 STP1 bit 5
6 STP1 bit 6
7 STP1 bit 7

Dynamic Condition Register (DYN)
MDM 4-40

0100* 0 Z=0
1 Storage wrap latch
2 CVFL (overflow)
3 Adder carry
4 Not hold in (Dir Ctl Feat)
5 Check disable switch
6 DYN Req bit 6 (HZ=0)
7 DYN Req bit 7 (LZ=0)

Status Register (S)
MDM 4-16

0101* 0 S0 True/compl latch
1 S1 X=nonzero (all arith ops)
2 S2 Z=nonzero (log, dec, & bin ops)
3 S3 ALU 0-bit carry
4 S4 Invalid decimal digit
5 S5 (general purpose)
6 S6 Not execute
7 S7 Not excepticnal condition

MMSK Register, Bits 0-7 (MMSK)
MDM 4-15

0110* 0 MMSK0 Channel high trap
2 MMSK2 Channel low trap
3 MMSK3 2540 reader trap
4 MMSK4 2540 punch trap
5 MMSK5 Comm chnl bit service
6 MMSK6 Comm chnl char service
7 MMSK7 Level 1 priority hold

Branch Conditions (BA)
MDM 4-40

0111* 0 Chnl 0 interruption latch
1 Mode bit 0
2 Mode bit 1
3 Mode bit 2
4 IPL latch
5 LS zone bit 0
6 LS zcne bit 1
7 LS zone bit 2

1000 Unassigned

1001 Unassigned

1010 Unassigned

1011 Unassigned

Channel Branch Conditions (GS)
MDM 4-45

1100* 0 Data chain request latch
1 Buffered device latch
2 Burst latch
3 Channel parity-error latch
4 Initial select latch
5 Channel 1 interrupt buffer latch
6 Spare
7 Suppress control latch

Channel Branch Conditions (GT)
MDM 4-409

1101* 0 Address in
1 Not select in
2 Service in
3 Status in
4 Operational in
5 Not request in
6 Channel identification latch
7 Channel diagnostic latch

Channel Diagnostic Register (GD)
MDM 4-411

1110* 0 Operational out
1 Service out
2 Address out
3 Command out
4 0
5 Select out
6 0
7 Suppress out

Channel Bus In (GB/IN)
MDM 4-405

1111* 0 Channel bus in bit 0
1 Channel bus in bit 1
2 Channel bus in bit 2
3 Channel bus in bit 3
4 Channel bus in bit 4
5 Channel bus in bit 5
6 Channel bus in bit 6
7 Channel bus in bit 7

* These eight fields tested with Branch on Condition or Branch on Mask control words.

External Field Definitions, Channel Mode (CPU TO EXT)

0C00 Unassigned

0001 Unassigned

Storage Protect 0 (STP0)

0010 0 STP0 bit 3 (Q0)
1 STP0 bit 1 (Q1)
2 STP0 bit 2 (Q2)
3 STP0 bit 3 (Q3)
4 STP0 bit 4 (Q4)
5 STP0 bit 5 (Q5)
6 STP0 bit 6 (Q6)
7 STP0 bit 7 (Q7)

Storage Protect 1 (STP1)

0011 0 STP1 bit 0 (Q0)
1 STP1 bit 1 (Q1)
2 STP1 bit 2 (Q2)
3 STP1 bit 3 (Q3)
4 STP1 bit 4 (Q4)
5 STP1 bit 5 (Q5)
6 STP1 bit 6 (Q6)
7 STP1 bit 7 (Q7)

0100 Unassigned

0101 Unassigned

0110 Unassigned

0111 Unassigned

1000 Unassigned

1001 Unassigned

1010 Unassigned

1011 Unassigned

1100 Unassigned

1101 Unassigned

1110 Unassigned

Channel Bus Out (GB/OUT)

1111 0 Channel bus out bit 0
1 Channel bus out bit 1
2 Channel bus out bit 2
3 Channel bus out bit 3
4 Channel bus out bit 4
5 Channel bus out bit 5
6 Channel bus out bit 6
7 Channel bus out bit 7

External Field Definitions, 2560 Mode (EXT to CPU)

2560 External 3 (MFD3) (20 Mode Operation)

0000 0 + SEC first PCH EJSEL
1 - FCB4 to FCB5 FL
2 + SEC PRE PCH REG SEL
3 - FCB3 to FCB6
4 + SEC read inject SEL
5 - Card PRT MAG strobe
6 + Secondary hopper SEL
7 + 100 micro SEC LW POT

2560 External 3 (MFD3) (2540 Emulator Operation)

```
0000**0  + PRI hopper empty
     1   + SEC hopper empty
     2   + Punch check light FL
     3   Spare
     4   + Punch status request
     5   + Read check
     6   Spare
     7   Spare
```

2560 External 1 (MFD1)

```
0001  0  + Feed CB6
      1  + Feed CB5
      2  + Feed CB4
      3  - Feed CB3
      4  + Feed CB2
      5  Spare
      6  + Feed Clutch select
      7  - Motor ready
```

2560 External 4 (MFD4) (20 Mode Operation)

```
0010  0  + Corn kick SC9 EXP
      1  + AFT PRT SC8 EXP
      2  + PRE PRT SC7 EXP
      3  + PRE PCH PRI SC5 EXP
      4  - Read cell 3 exposed
      5  - Cell 3 dark FL
      6  + Input station SC1 EXP
      7  + Feed CB1
```

Storage Protect 0 (STP0) (2540 Emulator Operation)

```
0010**0  + STP0 bit 0 (Q0)
     1   + STP0 bit 1 (Q1)
     2   + STP0 bit 2 (Q2)
     3   + STP0 bit 3 (Q3)
     4   + STP0 bit 4 (Q4)
     5   + STP0 bit 5 (Q5)
     6   + STP0 bit 6 (Q6)
     7   + STP0 bit 7 (Q7)
```

2560 External 2 (MFD2) (20 Mode Operation)

```
0011  0  + PRI first PCH EJ SEL
      1  - Allow COL emitter FL
      2  + PRI PRE PCH REG SEL
      3  - FCB1 to FCB2 FL
      4  + PRI read inject SEL
      5  + Read cell -4-9 EXP
      6  + Primary hopper SEL
      7  + Any punch DR
```

Storage Protect 1 (STP1) (2540 Emulator Operation)

```
0011**0  + STP1 bit 0
     1   + STP1 bit 1
     2   + STP1 bit 2
     3   + STP1 bit 3   See Note 5
     4   + STP1 bit 4   AAAD Routine
     5   + STP1 bit 5   *E60 Listing
     6   + STP1 bit 6
     7   + STP1 bit 7
```

```
0100* Same as in CPU Mode
0101* Same as in CPU Mode
0110* Same as in CPU Mode
0111* Same as in CPU Mode
```

2560 Read Rows 4-9 (MFR1)

```
1000  0  - PRE RD SEC SC2 EXP
      1  + 2540 RDR device end
      2  + Card code FL4
      3  + Card code FL5
      4  + Card code FL6
      5  + Card code FL7
      6  + Card code FL8
      7  + Card code FL9
```

2560 External 5 (MFD5)

```
1001  0  - Cell 1 dark FL
      1  - Cell 4 dark FL
      2  - Cell 5 dark FL
      3  - Punch CB1
      4  - Punch CB2
      5  - PCH INCR DR CBE
      6  + PCH push clutch SEL
      7  + Cell 8 dark FL
```

2560 Read Rows 12-3 (MFR2)

```
1010  0  + Diag feed check
      1  + 2540 PCH device end
      2  + Card code FL12
      3  + Card code FL11
      4  + Card code FL0
      5  + Card code FL1
      6  + Card code FL2
      7  + Card code FL3
```

2560 External 6 (MFD6)

```
1011  0  + PRT gate SEL/TRAN RL
      1  - Cell 7 dark FL
      2  - COL emitter test FL
      3  + 2560 stacker SEL REQ
      4  + Corner kick MAG SEL
      5  - Pass print FL
      6  - Pass punch FL
      7  + PRE RD PRI SC3 EXP
```

2560 Conditions 1 (MFS)

1100*	0	+ Cycle run
	1	+ 2560 primary
	2	+ Card in PRE PUNCH
	3	- SC7 DRK FI-CD in PRT
	4	+ 2560 punch execute
	5	+ 2560 read execute
	6	+ 2560 card in PRE RD
	7	+ Any feed CB

2560 External 7 (MFD7)

1101	0	- Punch push CB1
	1	- Punch push FI1
	2	+ SEC punch push SEL
	3	+ PRE PCH SEC SC4 EXP
	4	+ PRI punch push SEL
	5	+ PRE PCH PRI SC5 EXP
	6	- Cell 2 dark FL
	7	+ Mechan cycle

2560 Conditions 2 (MFT)

1110*	0	+ Feed check
	1	- 2560 card print REQ
	2	+ 2560 punch REQ
	3	+ Print execute FL
	4	- 2560 read REQ FL
	5	- Run out REQ
	6	- 2540 RDR status REQ
	7	+ PCH INCR DR CBA

2560 External 8 (MFD8)

1111	0	+ Read or punch check
	1	+ Print busy
	2	- 2560 ready
	3	- Hopper check
	4	- COL EM FL
	5	- RD strobe INIK FL
	6	+ Read cell 12-3 EXP
	7	+ Read COI EM

* These fields may be tested with Branch on Condition or Branch on Mask control words.
**These field definitions apply when 2540 Emulate latch is on.

<u>External Field Definitions, 2560 Mode (CPU to EXT)</u>

0C00 Unassigned

2560 Stacker Select (MFSS)

0001	0	
	1	
	2	
	3	See Note 1
	4	
	5	Set STS latch 4
	6	Set STS latch 2
	7	Set STS latch 1

2560 Punch Date (MFPU) (20 Mode Operation)

0011	0	Set data BFR LCH12
	1	Set data BFR LCH11
	2	Set data BFR LCH0
	3	Set data BFR LCH8
	4	Set data BFR LCH9
	7	Set data BFR LCH1 See Note 2
	6	Set data BFR LCH2
	6&7	Set data BFR LCH3
	5	Set data BFR LCH4
	5&7	Set data BFR LCH5
	5&6	Set data BFR LCH6
	5,6&7	Set data BFR LCH7

0100 Unassigned

2560 PRT Head Select (MFHS)

0101	0	Set head SEL latch 4
	1	Set head SEL latch 2
	2	Set head SEL latch 1
	3	
	4	
	5	
	6	
	7	

0110 Unassigned

2560 Print Latches 1-8 (MFPR1)

0111	0	Set print latch 1
	1	Set print latch 2
	2	Set print latch 3
	3	Set print latch 4
	4	Set print latch 5
	5	Set print latch 6
	6	Set print latch 7
	7	Set print latch 8

1000 Unassigned

2560 Print Latches 9-16 (MFPR2)

1001	0	Set print latch 9
	1	Set print latch 10
	2	Set print latch 11
	3	Set print latch 12
	4	Set print latch 13
	5	Set print latch 14
	6	Set print latch 15
	7	Set print latch 16

1010 Unassigned

2560 Print Latches 17-24 (MFPR3)

1011	0	Set print latch 17
	1	Set print latch 18
	2	Set print latch 19
	3	Set print latch 20
	4	Set print latch 21
	5	Set print latch 22
	6	Set print latch 23
	7	Set print latch 24

1100 Unassigned

2560 Print Latches 25-32 (MFPR4)

1101	0	Set print latch 25
	1	Set print latch 26
	2	Set print latch 27
	3	Set print latch 28
	4	Set print latch 29
	5	Set print latch 30
	6	Set print latch 31
	7	Set print latch 32

1110 Unassigned

2560 Print Latches 33-S5 (MFPR5)

1111	0	Set print latch 33
	1	Set print latch 34
	2	Set print latch 35
	3	Set print latch S1 See Note 3
	4	Set print latch S2
	5	Set print latch S3
	6	Set print latch S4
	7	Set print latch S5

Notes:

1. MFSS--Decode sets stacker SEL interlock latch automatically as data is loaded into stacker select registers.
2. MFPU--If punch time FL is on, data is XFERED to data BFR reg. If punch time FL is off, data is compared to data BFR reg.
3. MFPR5--Sets print latches 33 thru S5 and turns on PRT REQ INIK.

EXTERNAL MNEMONIC	DEFINITION			DISPLAYABLE FACILITY	SWITCH C	SWITCH D	ACCESSED BY SET/RESET WORD ONLY
BA	BRANCH CONDITIONS	ALL MODES	EXT TO CPU	YES	--	7	
BB	SOFT STOP BRANCH CONDITIONS	CPU MODE	EXT TO CPU	YES	CPU	F	
BC	EXTERNAL FACILITY	ALL MODES		--	--	-	YES
CADR	COMM ADAPTER DIAGNOSTIC REG	COMM MODE	CPU TO EXT	--	--	-	
CCTRL	START-STOP CONTROL	COMM MODE		--	--	-	YES
CHI	COUNTER 1 HIGH IN--DIAGNOSTIC	2311 MODE	EXT TO CPU	YES	2311	8	
CLI	COUNTER 1 LOW IN--DIAGNOSTIC	2311 MODE	EXT TO CPU	YES	2311	9	
CPF	READ DIRECT ENABLE	CPU MODE		--	--	-	YES
CSFTF	START STOP/SYNC	COMM MODE		--	--	-	YES
DAIN	DATA IN	COMM MODE	EXT TO CPU	YES	COMM	A	
DAOUT	DATA OUT	COMM MODE	CPU TO EXT	--	--	-	
DASI	DISK ATTACHMENT STATUS IN	2311 MODE	EXT TO CPU	YES	2311	5	
DIAB	DIAGNOSTIC REG	2311 MODE		--	--	-	YES
DIAC	DIAGNOSTIC REG	2311 MODE		--	--	-	YES
DILIN	DIAL IN	COMM MODE	EXT TO CPU	YES	COMM	E	
DILOUT	DIAL OUT	COMM MODE	CPU TO EXT	--	--	-	
DR	DIAGNOSTIC REGISTER	ALL MODES		YES	CPU	C	NOTE 1
DS	DISK STATUS	2311 MODE	EXT TO CPU	YES	2311	E	
DYN	DYNAMIC CONDITION REGISTER	ALL MODES		YES	--	4	
FBI	FILE BUS IN	2311 MODE	EXT TO CPU	YES	2311	1	
FBO	FILE BUS OUT	2311 MODE	CPU TO EXT	--	--	-	
FEBO	FILE 1400 EMULATOR BUS OUT	2311 MODE	CPU TO EXT	--	--	-	
FFI	FILE FLAGS IN	2311 MODE	EXT TO CPU	YES	2311	D	
FFO	FILE FLAGS OUT	2311 MODE	CPU TO EXT	--	--	-	
FGA	FILE GATED ATTENTION	2311 MODE	EXT TO CPU	YES	2311	C	
FIA	FILE INFORMATION	2311 MODE		--	--	-	YES
FIB	FILE INFORMATION	2311 MODE		--	--	-	YES
FIC	FILE INFORMATION	2311 MODE		--	--	-	YES
FOB	FILE OUT BUS--DIAGNOSTIC	2311 MODE	EXT TO CPU	YES	2311	3	
FOP	FILE OP REGISTER	2311 MODE		YES	2311	F	
GA	CHANNEL SIGNALS	CHAN MODE		--	--	-	YES
GB	CHANNEL SIGNALS	CHAN MODE		--	--	-	YES
GB/IN	CHANNEL BUS IN	CHAN MODE	EXT TO CPU	YES	CHNL	F	
GB/OUT	CHANNEL BUS OUT	CHAN MODE	CPU TO EXT	--	--	-	
GC	CHANNEL SIGNALS	CHAN MODE		--	--	-	YES
GD	CHANNEL DIAGNOSTIC REGISTER	CHAN MODE	EXT TO CPU	YES	CHNL	E	
GS	CHANNEL BRANCH CONDITIONS	CHAN MODE	EXT TO CPU	YES	CHNL	C	
GSTAT	GENERAL STATUS	COMM MODE	EXT TO CPU	YES	COMM	F	
GT	CHANNEL BRANCH CONDITIONS	CHAN MODE	EXT TO CPU	YES	CHNL	D	
JA	DIRECT CONTROL--2 TIMING	CPU MODE	CPU TO EXT	--	--	-	
JI	DIRECT CONTROL IN	CPU MODE	EXT TO CPU	YES	CPU	8	
JO	DIRECT CONTROL--1	CPU MODE	CPU TO EXT	--	--	-	
LACON	LINE ADAPTER CONDITIONS	COMM MODE	EXT TO CPU	YES	COMM	C	
LADR	LINE ADAPTER DIAG REGISTER	COMM MODE	CPU TO EXT	--	--	-	
LAIN	LINE ADDRESS IN	COMM MODE	EXT TO CPU	YES	COMM	B	
LAOUT	LINE ADDRESS OUT	COMM MODE	CPU TO EXT	--	--	-	
LASTAT	LINE ADAPTER STATUS	COMM MODE	EXT TO CPU	YES	COMM	D	
MC	ERROR REGISTER	CPU MODE	EXT TO CPU	YES	CPU	E	
MMSK	MICROPROGRAM MASK REGISTER	ALL MODES		YES (0 - 7)	--	6	NOTE 2
MODE	MODE REG (LS AND EXT ADDR CTRL)	ALL MODES		--	--	-	NOTE 3
MS	MODULE SELECT REGISTER	2311 MODE	CPU TO EXT	--	--	-	
MW	MACH CHK. WAIT STATE LATCHES	CPU MODE	CPU TO EXT	--	--	-	
P	PUNCH SIGNALS	2540 MODE		--	--	-	YES
PARCK	COMMUNICATIONS PARITY CHECK	COMM MODE	CPU TO EXT	--	--	-	
PCCL	PRINT CHAR COUNTER LENGTH	1403 MODE	CPU TO EXT	--	--	-	
PO	PUNCH DATA OUT (READER)	2540 MODE	CPU TO EXT	--	--	-	
PR	1403 PLBAR DATA OUT	1403 MODE	CPU TO EXT	--	--	-	
PRA	PRINTER SIGNALS	1403 MODE		--	--	-	YES

Figure 1-47. External Mnemonics and Addressing (Part 1 of 2)

EXTERNAL MNEMONIC	DEFINITION			DISPLAYABLE FACILITY	SWITCH C	SWITCH D	ACCESSED BY SET/RESET WORD ONLY
PRB	PRINTER SIGNALS	1403 MODE		—	—	—	YES
PRC	1403 CARRIAGE DATA OUT	1403 MODE	CPU TO EXT	—	—	—	
PRD	1403 DIAGNOSTIC CONDITIONS	1403 MODE	EXT TO CPU	YES	1403	F	
PRI	1403 PLB DATA IN	1403 MODE	EXT TO CPU	YES	1403	B	
PRO	1403 PLB DATA OUT	1403 MODE	CPU TO EXT	—	—	—	
PRS	SENSE/STATUS CONDITIONS	1403 MODE	EXT TO CPU	YES	1403	E	
PRT	PLBAR DATA IN	1403 MODE	EXT TO CPU	YES	1403	A	
PS	PUNCH BRANCH CONDITIONS	2540 MODE	EXT TO CPU	YES	2540	F	
R	READER SIGNALS	2540 MODE		—	—	—	YES
RP	2540 SIGNALS	2540 MODE		—	—	—	YES
RP1	READER/PUNCH DATA IN 1	2540 MODE	EXT TO CPU	YES	2540	B	
RP2	READER/PUNCH DATA IN 2	2540 MODE	EXT TO CPU	YES	2540	A	
RPD	2540 SIGNALS DIAG	2540 MODE		—	—	—	YES
RPD1	DIAGNOSTIC R/P CONDITIONS 1	2540 MODE	EXT TO CPU	YES	2540	8	
RPD2	DIAGNOSTIC R/P CONDITIONS 2	2540 MODE	EXT TO CPU	YES	2540	9	
RPS	READER/PUNCH BR CONDITIONS	2540 MODE	EXT TO CPU	YES	2540	E	
RS	READER BRANCH CONDITIONS	2540 MODE	EXT TO CPU	YES	2540	D	
S	STATUS REGISTER	ALL MODES		YES	NOT 2311	5	NOTE 4
SDI	SERIALIZER/DESERIALIZER IN DIAG	2311 MODE	EXT TO CPU	YES	2311	B	
SM	SYSTEM MASK	CPU MODE	CPU TO EXT	—	—	—	
STPO	STORAGE PROTECT KEY	ALL MODES		YES	NOTE 5	NOTE 5	
STP1	STORAGE PROTECT STACK	ALL MODES	(NOT 2311)	YES	NOTE 5	NOTE 5	
SWAB	CONSOLE ADDRESS SWITCHES A–B	CPU MODE	EXT TO CPU	—	—	—	
SWCD	CONSOLE ADDRESS SWITCHES C–D	CPU MODE	EXT TO CPU	—	—	—	
TA	1052 SIGNALS	1052 MODE		—	—	—	YES
TC	TERMINATING CONDITIONS	2311 MODE	EXT TO CPU	YES	2311	A	
TD	PRKB DIAGNOSTIC REGISTER	1052 MODE	EXT TO CPU	YES	PRKB	D	
TF	PRKB DATA OUT	1052 MODE	CPU TO EXT	—	—	—	
TGRI	TAG REGISTER IN	2311 MODE	EXT TO CPU	YES	2311	O	
TGRO	TAG REGISTER OUT	2311 MODE	CPU TO EXT	—	—	—	
TI	1052 DATA IN	1052 MODE	EXT TO CPU	YES	PRKB	A	
TIM	TIMER COUNT	CPU MODE	EXT TO CPU	YES	CPU	A	
TR	1052 TIIT/ROTATE REGISTER	1052 MODE	EXT TO CPU	YES	PRKB	B	
TT	PRKB BRANCH CONDITIONS	1052 MODE	EXT TO CPU	YES	PRKB	E	
TU	PRKB BRANCH CONDITIONS	1052 MODE	EXT TO CPU	YES	PRKB	F	
XINT	EXTERNAL INTERRUPT	CPU MODE	EXT TO CPU	YES	CPU	9	

NOTE 1 THE DR REGISTER IS SET BY THE SET/RESET WORD. EXECUTION OF A BRANCH WORD OR A RETURN WORD WITH BIT-7 OF DR ON SETS THE DIAGNOSTIC BRANCH LATCH.

NOTE 2 THE MMSK REGISTER 0-9 IS SET OR RESET BY THE SET/RESET WORD. FOR OTHER WORD ACCESSES AND DISPLAY, ONLY BITS 0-7 CAN BE ADDRESSED.

NOTE 3 THE MODE REGISTER IS SET BY THE SET/RESET WORD. THE ACTUAL BIT STRUCTURE OF THE MODE REGISTER IS NOT ALWAYS WHAT IS DISPLAYED IN THE CONSOLE INDICATORS LABELED MODE/ZONE REG. THE MODE BIT DECODE IS DISPLAYED IN BITS 2, 3, 4, AND THE LS ZONE BIT DECODE IS DISPLAYED IN BITS 5, 6, AND 7. THESE COULD BE THE FORCED DECODES CAUSED BY AN MMSK BIT BEING SET.

NOTE 4 THE S-REGISTER IS SET OR RESET BY THE SET/RESET WORD. IT CAN ALSO BE ACCESSED BY A BRANCH WORD.
BITS 0-6 CAN BE DISPLAYED DIRECTLY BUT BIT 7 OF THE DISPLAY INDICATES THE STATUS OF THE S7 BRANCH CONDITION LINE. TO DISPLAY THE ACTUAL CONDITION OF THE S7 LATCH, THE BA FACILITY MUST BE DISPLAYED AND BIT 0 WILL INDICATE THE S7 LATCH STATUS.

NOTE 5 REFER TO ROUTINE AAAD IN THE MICROPROGRAM LISTINGS FOR STP DISPLAY DETAILS.

Figure 1-47. External Mnemonics and Addressing (Part 2 of 2)

1.9 LOCAL-STORAGE LOCATION DECODE

Figures 1-48 through 1-53 give the local storage locations designated by the AS- or BS-field decodes for the various operation modes specified by the mode register or the microprogram mask (MMSK) register. The mode register is used for normal operations. The MMSK register is used during microprogram trap routines.

AS/BS Field Decode	Code	Zone					
		0	1	4	5	6	7
0000	U0	CPU	-----	Backups	Comm Chnl	2540	Chnl
0001	U1						
0010	V0						
0011	V1						
0010	G0						
0101	G1						
0110	D0						
0111	D1						
1000	I0	CPU	2311	CPU Bal Backup			
1001	I1			CPU Bal Backup			
1010	T0			Comm. Chnl Backup			
1011	T1			Comm. Chnl Backup			
1100	P0			Lv 1 work area for local-storage zones 4, 5, 6, and 7.			
1101	P1						
1110	H0						
1111	H1						

Note: The local storage areas are defined in the associated Figures.

Figure 1-48. Local-Storage Zones for System/360 Operation

Local-Storage Allocations, Zone 0		
AS or BS Field Decode	LS Area Code	Local-Storage Area
0000	U0	First operand address, high-order byte
0001	U1	First operand address, low-order byte
0010	V0	Second operand address, high-order byte
0011	V1	Second operand address, low-order byte
0100	G0	Operation code, byte 0
0101	G1	Operation code, byte 1
0110	D0	Data
0111	D1	High-order 8 bits, 24-bit 2nd operand address
1000	I0	Instruction counter, high-order byte
1001	I1	Instruction counter, low-order byte
1010	T0	Working area (0 at start of I-cycles)
1011	T1	Gen Register Addr (B, X, R)
1100	P0	Condition code
1101	P1	Program mask and AMWP bits*
1110	H0	Data
1111	H1	High-order 8 bits, 24-bit instruction counter, or first operand address

Note 1: *USASCII, machine check, wait state, and problem state bits.

Note 2: Zone 0 is also used for integrated 2540 status and chaining, and console attachment functions between execution of CPU instructions.

Figure 1-49. Local-Storage Decodes when Mode Register Bits 5-7 are 000: CPU Functions

Local-Storage Allocations, Zone 1		
AS or BS Field Decode	LS Area Code	Local-Storage Area
1000	I0	Integrated file attachment CCW count field, high-order byte
1001	I1	Integrated file attachment CCW count field, low-order byte
1010	T0	Integrated file attachment data address, high-order byte
1011	T1	Integrated file attachment data address, low-order byte
1100	P0	Working area (Flags)
1101	P1	Working area (Command)
1110	H0	Integrated file attachment next CCW address, high-order byte
1111	H1	Integrated file attachment next CCW address, low-order byte

Figure 1-50. Local-Storage Decodes when Mode Register Bits 5-7 are 001: 2311 Disk Locations

Local-Storage Allocations, Zone 4		
AS or BS Field Decode	LS Area Code	Local-Storage Area
0000	U0	Level-1 backup, high-order byte
0001	U1	Level-1 backup, low-order byte
0010	V0	Level-2 backup, high-order byte
0011	V1	Level-2 backup, low-order byte
0100	G0	Level-3 backup, high-order byte
0101	G1	Level-3 backup, low-order byte
0110	D0	Machine-check backup, high-order byte
0111	D1	Machine-check backup, low-order byte
The following locations are shared between zones 4, 5, 6, and 7.		
1000	I0	CPU branch and link backup, high-order byte
1001	I1	CPU branch and link backup, low-order byte
1010	T0	Spare
1011	T1	Spare
1100	P0	Level-1 working area
1101	P1	Level-1 working area
1110	H0	Level-1 working area
1111	H1	Level-1 working area

Figure 1-51. Local-Storage Decodes when Mode Register Bits 5-7 are 100: Address Backup Locations

Local-Storage Allocations, Zone 5		
AS or BS Field Decode	LS Area Code	Local-Storage Area
0000	U0	Line control word (LCW) address, high-order btye
0001	U1	Line control word (LCW) address, low-order byte
0010	V0	Character service pointer, high-order byte
0011	V1	Character service pointer, low-order byte
0100	G0	Line control word (LCW)
0101	G1	Line control word (LCW) +1
0110	D0	Line control word (LCW) +2
0111	D1	Line control word (LCW) +3
The following locations are shared between zones 4, 5, 6, and 7.		
1000	I0	CPU branch and link backup, high-order byte
1001	I1	CPU branch and link backup, low-order byte
1010	T0	Comm chnl branch and link function, high-order byte
1011	T1	Comm chnl branch and link function, low-order byte
1100	P0	Level-1 working area
1101	P1	Level-1 working area
1110	H0	Level-1 working area
1111	H1	Level-1 working area

Figure 1-52. Local-Storage Deccdes when Mode Register Bits 5-7 are 101: Communications Channel

Local-Storage Allocations, Zone 6		
AS or BS Field Decode	LS Area Code	Local-Storage Area
0000	U0	Reader image buffer address, high-order byte
0001	U1	Reader image buffer address, low-order byte
0010	V0	Punch image card-image address, high-order byte
0011	V1	Punch image card-image address, low-order byte
0100	G0	Punch trap count, high-order byte
0101	G1	Not used
0110	D0	Indicators
0111	D1	Reader trap count
The following locations are shared between zones 4, 5, 6, and 7.		
1000	I0	CPU branch and link backup, high-order byte
1001	I1	CPU branch and link backup, low-order byte
1010	T0	Spare
1011	T1	Spare
1100	P0	Level-1 working area
1101	P1	Level-1 working area
1110	H0	Level-1 working area
1111	H1	Level-1 working area

Figure 1-53. Local-Storage Decodes when Mode Register Bits 5-7 are 110: 2540 Reader Punch

1.10 CODE CONVERSIONS (FIGURES 1-54 THROUGH 1-60)

Hex	Card Code	Hex	Card Code	Hex	Card Code	Hex	Card Code	Hex	Card Code
00	12-0-1-8-9	34	4-9	67	11-0-7-9	9A	12-11-2-8	CD	12-0-5-8-9
01	12-1-9	35	5-9	68	11-0-8-9	9B	12-11-3-8	CE	12-0-6-8-9
02	12-2-9	36	6-9	69	0-1-8	9C	12-11-4-8	CF	12-0-7-8-9
03	12-3-9	37	7-9	6A	12-11	9D	12-11-5-8	D0	11-0
04	12-4-9	38	8-9	6B	0-3-8	9E	12-11-6-8	D1	11-1
05	12-5-9	39	1-8-9	6C	0-4-8	9F	12-11-7-8	D2	11-2
06	12-6-9	3A	2-8-9	6D	0-5-8	A0	11-0-1-8	D3	11-3
07	12-7-9	3B	3-8-9	6E	0-6-8	A1	11-0-1	D4	11-4
08	12-8-9	3C	4-8-9	6F	0-7-8	A2	11-0-2	D5	11-5
09	12-1-8-9	3D	5-8-9	70	12-11-0	A3	11-0-3	D6	11-6
0A	12-2-8-9	3E	6-8-9	71	12-11-0-1-9	A4	11-0-4	D7	11-7
0B	12-3-8-9	3F	7-8-9	72	12-11-0-2-9	A5	11-0-5	D8	11-8
0C	12-4-8-9	40	No Punches	73	12-11-0-3-9	A6	11-0-6	D9	11-9
0D	12-5-8-9	41	12-0-1-9	74	12-11-0-4-9	A7	11-0-7	DA	12-11-2-8-9
0E	12-6-8-9	42	12-0-2-9	75	12-11-0-5-9	A8	11-0-8	DB	12-11-3-8-9
0F	12-7-8-9	43	12-0-3-9	76	12-11-0-6-9	A9	11-0-9	DC	12-11-4-8-9
10	12-11-1-8-9	44	12-0-4-9	77	12-11-0-7-9	AA	11-0-2-8	DD	12-11-5-8-9
11	11-1-9	45	12-0-5-9	78	12-11-0-8-9	AB	11-0-3-8	DE	12-11-6-8-9
12	11-2-9	46	12-0-6-9	79	1-8	AC	11-0-4-8	DF	12-11-7-8-9
13	11-3-9	47	12-0-7-9	7A	2-8	AD	11-0-5-8	E0	0-2-8
14	11-4-9	48	12-0-8-9	7B	3-8	AE	11-0-6-8	E1	11-0-1-9
15	11-5-9	49	12-1-8	7C	4-8	AF	11-0-7-8	E2	0-2
16	11-6-9	4A	12-2-8	7D	5-8	B0	12-11-0-1-8	E3	0-3
17	11-7-9	4B	12-3-8	7E	6-8	B1	12-11-0-1	E4	0-4
18	11-8-9	4C	12-4-8	7F	7-8	B2	12-11-0-2	E5	0-5
19	11-1-8-9	4D	12-5-8	80	12-0-1-8	B3	12-11-0-3	E6	0-6
1A	11-2-8-9	4E	12-6-8	81	12-0-1	B4	12-11-0-4	E7	0-7
1B	11-3-8-9	4F	12-7-8	82	12-0-2	B5	12-11-0-5	E8	0-8
1C	11-4-8-9	50	12	83	12-0-3	B6	12-11-0-6	E9	0-9
1D	11-5-8-9	51	12-11-1-9	84	12-0-4	B7	12-11-0-7	EA	11-0-2-8-9
1E	11-6-8-9	52	12-11-2-9	85	12-0-5	B8	12-11-0-8	EB	11-0-3-8-9
1F	11-7-8-9	53	12-11-3-9	86	12-0-6	B9	12-11-0-9	EC	11-0-4-8-9
20	11-0-1-8-9	54	12-11-4-9	87	12-0-7	BA	12-11-0-2-8	ED	11-0-5-8-9
21	0-1-9	55	12-11-5-9	88	12-0-8	BB	12-11-0-3-8	EE	11-0-6-8-9
22	0-2-9	56	12-11-6-9	89	12-0-9	BC	12-11-0-4-8	EF	11-0-7-8-9
23	0-3-9	57	12-11-7-9	8A	12-0-2-8	BD	12-11-0-5-8	F0	0
24	0-4-9	58	12-11-8-9	8B	12-0-3-8	BE	12-11-0-6-8	F1	1
25	0-5-9	59	11-1-8	8C	12-0-4-8	BF	12-11-0-7-8	F2	2
26	0-6-9	5A	11-2-8	8D	12-0-5-8	C0	12-0	F3	3
27	0-7-9	5B	11-3-8	8E	12-0-6-8	C1	12-1	F4	4
28	0-8-9	5C	11-4-8	8F	12-0-7-8	C2	12-2	F5	5
29	0-1-8-9	5D	11-5-8	90	12-11-1-8	C3	12-3	F6	6
2A	0-2-8-9	5E	11-6-8	91	12-11-1	C4	12-4	F7	7
2B	0-3-8-9	5F	11-7-8	92	12-11-2	C5	12-5	F8	8
2C	0-4-8-9	60	11	93	12-11-3	C6	12-6	F9	9
2D	0-5-8-9	61	0-1	94	12-11-4	C7	12-7	FA	12-11-0-2-8-9
2E	0-6-8-9	62	11-0-2-9	95	12-11-5	C8	12-8	FB	12-11-0-3-8-9
2F	0-7-8-9	63	11-0-3-9	96	12-11-6	C9	12-9	FC	12-11-0-4-8-9
30	12-11-0-1-8-9	64	11-0-4-9	97	12-11-7	CA	12-0-2-8-9	FD	12-11-0-5-8-9
31	1-9	65	11-0-5-9	98	12-11-8	CB	12-0-3-8-9	FE	12-11-0-6-8-9
32	2-9	66	11-0-6-9	99	12-11-9	CC	12-0-4-8-9	FF	12-11-0-7-8-9
33	3-9								

Figure 1-54. Hexadecimal/Punched-Card Translate Table

Digits	Zones and 9															
Twelve (T) Eleven (E) Zero (0)					T 0	T E	E 0	T E 0	T 0	T E	E 0	T E 0	T	E	0	Blank
	9	9	9	9	9	9	9	9								
Blank	C9	D9	E9	F9	89	99	A9	B9	C0	6A	D0	70	50	60	F0	40
1	01	11	21	31	41	51	E1	71	81	91	A1	B1	C1	D1	61	F1
2	02	12	22	32	42	52	62	72	82	92	A2	B2	C2	D2	E2	F2
3	03	13	23	33	43	53	63	73	83	93	A3	B3	C3	D3	E3	F3
4	04	14	24	34	44	54	64	74	84	94	A4	B4	C4	D4	E4	F4
5	05	15	25	35	45	55	65	75	85	95	A5	B5	C5	D5	E5	F5
6	06	16	26	36	46	56	66	76	86	96	A6	B6	C6	D6	E6	F6
7	07	17	27	37	47	57	67	77	87	97	A7	B7	C7	D7	E7	F7
8	08	18	28	38	48	58	68	78	88	98	A8	B8	C8	D8	E8	F8
18	09	19	29	39	00	10	20	30	80	90	A0	B0	49	59	69	79
28	0A	1A	2A	3A	CA	DA	EA	FA	8A	9A	AA	BA	4A	5A	E0	7A
38	0B	1B	2B	3B	CB	DB	EB	FB	8B	9B	AB	BB	4B	5B	6B	7B
48	0C	1C	2C	3C	CC	DC	EC	FC	8C	9C	AC	BC	4C	5C	6C	7C
58	0D	1D	2D	3D	CD	DD	ED	FD	8D	9D	AD	BD	4D	5D	6D	7D
68	0E	1E	2E	3E	CE	DE	EE	FE	8E	9E	AE	BE	4E	5E	6E	7E
78	0F	1F	2F	3F	CF	DF	EF	FF	8F	9F	AF	BF	4F	5F	6F	7F

Note: Exceptions to sequence are underlined

Figure 1-55. New Program Card Code to Hexadecimal

Extended Binary-Coded-Decimal Interchange Code (EBCDIC)

Bit Positions → 01 / 23 / 4567	00	01	10	11	00	01	10	11	00	01	10	11	00	01	10	11
0000	NULL				b blank	&	-						>	<	‡	0
0001							/		a	j			A	J		1
0010									b	k	s		B	K	S	2
0011									c	l	t		C	L	T	3
0100	PF	RES	BYP	PN					d	m	u		D	M	U	4
0101	HT	NL	LF	RS					e	n	v		E	N	V	5
0110	LC	BS	EOB	UC					f	o	w		F	O	W	6
0111	DEL	IDL	PRE	EOT					g	p	x		G	P	X	7
1000									h	q	y		H	Q	Y	8
1001					•		,	"	i	r	z		I	R	Z	9
1010					?	!		:								
1011					.	$	,	#								
1100					←	*	%	@								
1101					(	)	⌒	'								
1110					+	;	_	=								
1111					‡	¢	±	✓								

Figure 1-56. EBCDIC Chart

American Standard Code for Information Interchange (ASCII)
Extended to Eight Bits

Bit Positions → 76 / X5 / 4321	00	01	10	11	00	01	10	11	00	01	10	11	00	01	10	11
0000	NULL	DC_0			b blank	0					@	P				P
0001	SOM	DC_1			!	1					A	Q			a	q
0010	EOA	DC_2			"	2					B	R			b	r
0011	EOM	DC_3			#	3					C	S			c	s
0100	EOT	DC_4 STOP			$	4					D	T			d	t
0101	WRU	ERR			%	5					E	U			e	u
0110	RU	SYNC			&	6					F	V			f	v
0111	BELL	LEM			'	7					G	W			g	w
1000	BKSP	S_0			(	8					H	X			h	x
1001	HT	S_1			)	9					I	Y			i	y
1010	LF	S_2			*	:					J	Z			j	z
1011	VT	S_3			+	;					K	[			k	
1100	FF	S_4			,	<					L	\			l	
1101	CR	S_5			-	=					M	]			m	
1110	SO	S_6			.	>					N	↑			n	ESC
1111	SI	S_7			/	?					O	←			o	DEL

Figure 1-57. ASCII-8 Chart

DEF CHAR	CARD CODE	BCD	CM6	CM6 WM
Blank		C	40	00
.	12-3-8	BA8 21	48	0B
¤	12-4-8	BA84	4C	0C
[	12-5-8	BA84 1	4D	0D
<	12-6-8	BA842	4E	0E
≠	12-7-8	BA8421	4F	0F
&	12	BA	50	10
$	11-3-8	B 8 21	5B	1B
*	11-4-8	B 84	5C	1C
]	11-5-8	B 84 1	5D	1D
;	11-6-8	B 842	5E	1E
Δ	11-7-8	B 8421	5F	1F
-	11	B	60	20
/	0-1	A 1	61	21
,	0-3-8	A8 21	68	2B
%	0-4-8	A84	6C	2C
∨	0-5-8	A84 1	6D	2D
\	0-6-8	A842	6E	2E
≠	0-7-8	A8421	6F	2F
ъ	2-8	A	7A	3A
#	3-8	8 21	7B	3B
@	4-8	84	7C	3C
:	5-8	84 1	7D	3D
>	6-8	842	7E	3E
√‾	7-8	8421	7F	3F
?	12-0	BA8 2	C0	80
A	12-1	BA 1	C1	81
B	12-2	BA 2	C2	82
C	12-3	BA 21	C3	83
D	12-4	BA 4	C4	84
E	12-5	BA 4 1	C5	85
F	12-6	BA 42	C6	86
G	12-7	BA 421	C7	87
H	12-8	BA8	C8	88
I	12-9	BA8 1	C9	89
!	11-0	B 8 2	D0	90
J	11-1	B 1	D1	91
K	11-2	B 2	D2	92
L	11-3	B 21	D3	93
M	11-4	B 4	D4	94
N	11-5	B 4 1	D5	95
O	11-6	B 42	D6	96
P	11-7	B 421	D7	97
Q	11-8	B 8	D8	98
R	11-9	B 8 1	D9	99
≠	0-2-8	A8 2	E0	A0
S	0-2	A 2	E2	A2
T	0-3	A 21	E3	A3
U	0-4	A 4	E4	A4
V	0-5	A 4 1	E5	A5
W	0-6	A 42	E6	A6
X	0-7	A 421	E7	A7
Y	0-8	A8	E8	A8
Z	0-9	A8 1	E9	A9
0	0	8 2	F0	B0
1	1	1	F1	B1
2	2	2	F2	B2
3	3	21	F3	B3
4	4	4	F4	B4
5	5	4 1	F5	B5
6	6	42	F6	B6
7	7	421	F7	B7
8	8	8	F8	B8
9	9	8 1	F9	B9

Figure 1-58. BCD-to-CM6 Conversion

Collating Sequence	Graphics 8 Bit	Graphics BCD	8 Bit Code 0	1	2	3	4	5	6	7	BCD B	A	8	4	2	1
00	blank	blank	0	1	0	0	0	0	0	0	0	0	0	0	0	0
01	.	.	0	1	0	0	1	0	1	1	1	1	1	0	1	1
02	←	X)	0	1	0	0	1	1	0	0	1	1	1	1	0	0
03	(	⊏	0	1	0	0	1	1	0	1	1	1	1	1	0	1
04	+	<	0	1	0	0	1	1	1	0	1	1	1	1	1	0
05	GM	GM	0	1	0	0	1	1	1	1	1	1	1	1	1	1
06	&	& +	0	1	0	1	0	0	0	0	1	1	0	0	0	0
07	S	S	0	1	0	1	1	0	1	1	1	0	1	0	1	1
08	*	*	0	1	0	1	1	1	0	0	1	0	1	1	0	0
09	)	⊐	0	1	0	1	1	1	0	1	1	0	1	1	0	1
10	;	;	0	1	0	1	1	1	1	0	1	0	1	1	1	0
11	MC	MC	0	1	0	1	1	1	1	1	1	0	1	1	1	1
12	-	-	0	1	1	0	0	0	0	0	1	0	0	0	0	0
13	/	/	0	1	1	0	0	0	0	1	0	1	0	0	0	1
14	,	,	0	1	1	0	1	0	1	1	0	1	1	0	1	1
15	%	% (	0	1	1	0	1	1	0	0	0	1	1	1	0	0
16	WS	WS	0	1	1	0	1	1	0	1	0	1	1	1	0	1
17	↑	\	0	1	1	0	1	1	1	0	0	1	1	1	1	0
18	SM	SM	0	1	1	0	1	1	1	1	0	1	1	1	1	1
19	ъ	ъ	0	1	1	1	1	0	1	0	0	1	0	0	0	0
20	"	"=	0	1	1	1	1	0	1	1	0	0	1	0	1	1
21	@	@′	0	1	1	1	1	1	0	0	0	0	1	1	0	0
22	▽	:	0	1	1	1	1	1	0	1	0	0	1	1	0	1
23	=	>	0	1	1	1	1	1	1	0	0	0	1	1	1	0
24	TM	TM	0	1	1	1	1	1	1	1	0	0	1	1	1	1
25	ŏ	ŏ	1	1	0	0	0	0	0	0	1	1	1	0	1	0
26	A	A	1	1	0	0	0	0	0	1	1	1	0	0	0	1
27	B	B	1	1	0	0	0	0	1	0	1	1	0	0	1	0
28	C	C	1	1	0	0	0	0	1	1	1	1	0	0	1	1
29	D	D	1	1	0	0	0	1	0	0	1	1	0	1	0	0
30	E	E	1	1	0	0	0	1	0	1	1	1	0	1	0	1
31	F	F	1	1	0	0	0	1	1	0	1	1	0	1	1	0
32	G	G	1	1	0	0	0	1	1	1	1	1	0	1	1	1
33	H	H	1	1	0	0	1	0	0	0	1	1	1	0	0	0
34	I	I	1	1	0	0	1	0	0	1	1	1	1	0	0	1
35	ō	ō	1	1	0	1	0	0	0	0	1	0	1	0	1	0
36	J	J	1	1	0	1	0	0	0	1	1	0	0	0	0	1
37	K	K	1	1	0	1	0	0	1	0	1	0	0	0	1	0
38	L	L	1	1	0	1	0	0	1	1	1	0	0	0	1	1
39	M	M	1	1	0	1	0	1	0	0	1	0	0	1	0	0
40	N	N	1	1	0	1	0	1	0	1	1	0	0	1	0	1
41	O	O	1	1	0	1	0	1	1	0	1	0	0	1	1	0
42	P	P	1	1	0	1	0	1	1	1	1	0	0	1	1	1
43	Q	Q	1	1	0	1	1	0	0	0	1	0	1	0	0	0
44	R	R	1	1	0	1	1	0	0	1	1	0	1	0	0	1
45	RM	RM	1	1	1	0	0	0	0	0	0	1	1	0	1	0
46	S	S	1	1	1	0	0	0	1	0	0	1	0	0	1	0
47	T	T	1	1	1	0	0	0	1	1	0	1	0	0	1	1
48	U	U	1	1	1	0	0	1	0	0	0	1	0	1	0	0
49	V	V	1	1	1	0	0	1	0	1	0	1	0	1	0	1
50	W	W	1	1	1	0	0	1	1	0	0	‡	0	1	1	0
51	X	X	1	1	1	0	0	1	1	1	0	1	0	1	1	1
52	Y	Y	1	1	1	0	1	0	0	0	0	1	1	0	0	0
53	Z	Z	1	1	1	0	1	0	0	1	0	1	1	0	0	1
54	0	0	1	1	1	1	0	0	0	0	0	0	1	0	1	0
55	1	1	1	1	1	1	0	0	0	1	0	0	0	0	0	1
56	2	2	1	1	1	1	0	0	1	0	0	0	0	0	1	0
57	3	3	1	1	1	1	0	0	1	1	0	0	0	0	1	1
58	4	4	1	1	1	1	0	1	0	0	0	0	0	1	0	0
59	5	5	1	1	1	1	0	1	0	1	0	0	0	1	0	1
60	6	6	1	1	1	1	0	1	1	0	0	0	0	1	1	0
61	7	7	1	1	1	1	0	1	1	1	0	0	0	1	1	1
62	8	8	1	1	1	1	1	0	0	0	0	0	1	0	0	0
63	9	9	1	1	1	1	1	0	0	1	0	0	1	0	0	1

*BCD code for blank is:
C bit for odd parity
C and A bits for even parity

Figure 1-59. 8-Bit Code--BCD Relations (7- and 9-Track Tape)

CHARACTER IN STORAGE	CHARACTER TO 1443	CHARACTER IN STORAGE	CHARACTER TO1443
&	&	Q	Y
-	-	9	8
1	0	≠	I
/	A ①	I	R
A	J	R	≠
J	/ ②	0	9
2	1	‡	>
S	B	?	<
B	K	:	‡
K	S	#	:
3	2	,	.
T	C	.	$
C	L	$	,
L	T	@	#
4	3	%	←
U	D	¤	*
D	M	*	%
M	U	:	@
5	4	∨	(
V	E	(	)
E	N	)	¬
N	V	>	∀
6	5	\	+
W	F	<	;
F	O	;	-
O	W	¬	=
7	6	+++	≠
X	G	≠	≠
G	P	Δ	±
P	X	Blank	√
8	7	Blank	Blank
Y	H	∦	Blank
H	Q		

① Sent As 01000001
② Sent As 11100001

Figure 1-60. 52- and 63-Character Typebar Decode (1400 Compatibility)

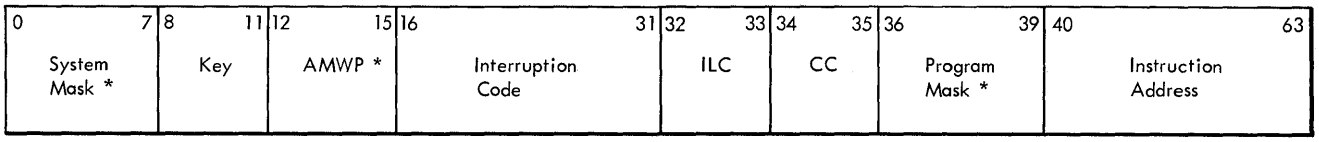
1.11 PROGRAM CCDES AND PSW (FIGURES 1-60 THROUGH 1-63)

Condition Code	0	1	2	3
Mask bit position	8	4	2	1
Floating-Point Arithmetic				
Add Normalized S/L	Zero	< Zero	>Zero	Overflow
Add Unnormalized S/L	Zero	< Zero	>Zero	Overflow
Compare S/L (A:B)	Equal	A Low	A High	—
Load and Test S/L	Zero	< Zero	>Zero	—
Load Complement S/L	Zero	< Zero	>Zero	—
Load Negative S/L	Zero	< Zero	—	—
Load Positive S/L	Zero	—	>Zero	—
Subtract Normalized S/L	Zero	<Zero	>Zero	Overflow
Subtract Unnormalized S/L	Zero	<Zero	>Zero	Overflow
Fixed-Point Arithmetic				
Add H/F	Zero	<Zero	>Zero	Overflow
Add Logical	Zero	Not Zero,	Zero,	Not Zero,
	No Carry	No Carry	Carry	Carry
Compare H/F (A:B)	Equal	A Low	A High	—
Load and Test	Zero	<Zero	>Zero	—
Load Complement	Zero	<Zero	>Zero	Overflow
Load Negative	Zero	<Zero	—	—
Load Positive	Zero	—	Zero	Overflow
Shift Left Double	Zero	<Zero	>Zero	Overflow
Shift Left Single	Zero	<Zero	>Zero	Overflow
Shift Right Double	Zero	<Zero	>Zero	—
Shift Right Single	Zero	<Zero	>Zero	—
Subtract H/F	Zero	<Zero	>Zero	Overflow
Subtract Logical	—	Not Zero	Zero,	Not Zero,
	—	No Carry	Carry	Carry
Decimal Arithmetic				
Add Decimal	Zero	<Zero	>Zero	Overflow
Compare Decimal (A:B)	Equal	A Low	A High	—
Subtract Decimal	Zero	<Zero	>Zero	Overflow
Zero and Add	Zero	<Zero	>Zero	Overflow
Logical Operations				
AND	Zero	Not Zero	—	—
Compare Logical (A:B)	Equal	A Low	A High	—
Edit	Zero	<Zero	>Zero	—
Edit and Mark	Zero	<Zero	>Zero	—
Exclusive OR	Zero	Not Zero	—	—
OR	Zero	Not Zero	—	—
Test Under Mask	Zero	Mixed	—	One
Translate and Test	Zero	Incomplete	Complete	—
Input/Output Operations				
Halt I/O	Int. Pending	CSW Stored	Stopped	Not Oper
Start I/O	Available	CSW Stored	Busy	Not Oper
Test Channel	Not Working	CSW Ready	Working	Not Oper
Test I/O	Available	CSW Stored	Working	Not Oper

Figure 1-61. Condition-Code Settings

Interruption Code			Program Interruption Cause
Dec	Hex	Binary	
1	01	0000 0001	Operation
2	02	0000 0010	Privileged operation
3	03	0000 0011	Execute
4	04	0000 0100	Protection
5	05	0000 0101	Addressing
6	06	0000 0110	Specification
7	07	0000 0111	Data
8	08	0000 1000	Fixed-point overflow
9	09	0000 1001	Fixed-point divide
10	0A	0000 1010	Decimal overflow
11	0B	0000 1011	Decimal divide
12	0C	0000 1100	Exponent overflow
13	0D	0000 1101	Exponent underflow
14	0E	0000 1110	Significance
15	0F	0000 1111	Floating-point divide

Figure 1-62. Program Interruption Codes



0 Multiplexer channel mask
1 Selector channel 1 mask
2 Selector channel 2 mask
3 Selector channel 3 mask
4 Selector channel 4 mask
5 Selector channel 5 mask
6 Selector channel 6 mask
7 External mask
12 ASCII mode (A)
13 Machine check mask (M)
14 Wait state (W)
15 Problem state (P)
32-33 Instruction Length code (ILC)
34-35 Condition code (CC)
36 Fixed-point overflow mask
37 Decimal overflow mask
38 Exponent underflow mask
39 Significance mask

* A one-bit equals on, and permits an interrupt

Figure 1-63. Program Status Word (PSW)

1.12 CHANNEL COMMAND AND ADDRESS FORMATS (FIGURES 1-64 THROUGH 1-68)

	Command for CCW	8-Bit Code 0	1	2	3	4	5	6	7	Hex	Dec
1052	Read Inquiry BCD	0	0	0	0	1	0	1	0	0A	10
	Read Reader 2 BCD	0	0	0	0	0	0	1	0	02	02
	Write BCD, Auto Carriage Return	0	0	0	0	1	0	0	1	09	09
	Write BCD, No Auto Carriage Return	0	0	0	0	0	0	0	1	01	01
	No Op	0	0	0	0	0	0	1	1	03	03
	Sense	0	0	0	0	0	1	0	0	04	04
	Alarm	0	0	0	0	1	0	1	1	0B	11
2540	Read, Feed, Select Stacker SS — Type AA	S	S	D	0	0	0	1	0		
	Read — Type AB	1	1	D	0	0	0	1	0		
	Read, Feed (1440 compatibility mode only)	1	1	D	1	0	0	1	0		
	Feed, Select Stacker SS — Type BA	S	S	1	0	0	0	1	1		
	PFR Punch, Feed Select Stacker SS — Type BA	S	S	D	0	1	0	0	1		
	Punch, Feed, Select Stacker SS — Type BB	S	S	D	0	0	0	0	1		
1442 N1	Read	M	M	M	0	0	0	1	0		
	Write	M	M	M	0	0	0	0	1		
	Control	M	M	0	0	0	0	1	1		
	No Op	0	0	0	0	0	0	1	1		
	Sense	0	0	M	M	0	1	0	0		
1403 or 1443	Write, No Space	0	0	0	0	0	0	0	1	01	01
	Write, Space 1 After Print	0	0	0	0	1	0	0	1	09	09
	Write, Space 2 After Print	0	0	0	1	0	0	0	1	11	17
	Write, Space 3 After Print	0	0	0	1	1	0	0	1	19	25
	Write, Skip to Channel N After Print	1	C	H	A	N	0	0	1		
	Diagnostic Read	0	0	0	0	0	0	1	0	02	02
	Test I/O	0	0	0	0	0	0	0	0	00	00
	Sense	0	0	0	0	0	1	0	0	04	04
Carriage Control	Space 1 Line Immediately	0	0	0	0	1	0	1	1	0B	11
	Space 2 Line Immediately	0	0	0	1	0	0	1	1	13	19
	Space 3 Line Immediately	0	0	0	1	1	0	1	1	1B	27
	Skip to Channel N Immediately	1	C	H	A	N	0	0	1		
	No Op	0	0	0	0	0	0	1	0	03	03
2400 Tape*	Transfer in Channel	0	0	0	0	1	0	0	0	08	08
	Sense	0	0	0	0	0	1	0	0	04	04
	Read Backward**	0	0	0	0	1	1	0	0	0C	12
	Write	0	0	0	0	0	0	0	1	01	01
	Read	0	0	0	0	0	0	1	0	02	02
	Control	0	0	C	C	C	1	1	1		
	Mode Set	D	D	M	M	M	0	1	1		

1442 N1 — M M M M

Read	0	0	X		Eject and SS1
Read	1	0	X		Eject and SS1
Read	0	1	X		Eject and SS2
Read	1	1	X		Eject and SS2
Write	0	0	X		SS1
Write	1	0	X		Eject and SS1
Write	0	1	X		SS2
Write	1	1	X		Eject and SS2
Control	1	0			Eject and SS1
Control	0	1			SS2
Control	1	1			Eject and SS2
Sense			1	1	Punch Diagnostic
Sense			0	1	Read Diagnostic

X-0 means EBCDIC mode
X=1 means Column Binary Mode

2540 Stacker

SS	Stacker
00	R1
01	R2
10	RP3

2540 Data Mode

D	Data Mode
0	EBCDIC
1	Column Binary

Carriage Control Channel

C	H	A	N	Channel
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	1	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12

*9 track op. forces 800 BPI and odd parity; also, it overrides
7 track but does not reset 7 track. Load/Sys Reset forces
7 track to 800 BPI, odd parity, data converter on, translator off.

C	C	C	Control Codes	Hex	Dec
0	0	0	REW	7	7
0	0	1		0F	15
0	1	0		17	23
0	1	1		1F	31
1	0	0		27	39
1	0	1		2F	47
1	1	0		37	55
1	1	1		3F	63

**Overrides Data Converter On

D	D	7 Track Density
0	0	200
0	1	556
1	0	800
1	1	800

M	M	M	(Mode Modifiers)	Set Density	Set Odd Parity	Set Even Parity	Data Converter On	Data Converter Off	Translator On	Translator Off	Request TIE (Track In Error)
0	0	0	No Op								
0	0	1	Not Used								
0	1	0	Reset Condition	X	X			X		X	
0	1	1	Nine-track only			X					X
1	0	0				X		X		X	
1	0	1		X		X		X	X		
1	1	0	Reset Condition	X	X			X		X	
1	1	1		X	X			X	X		

Figure 1-64. Channel Command Codes

Command Code	Data Address	Flags	000	Ignored	Count
(8)	00000000 (24)	(5)	(3)	(8)	(16)

Command Code

0 1 2 3 4 5 6 7	
* * * * 0 0 0 0	Invalid
m m m m 0 1 0 0	Sense
* * * * 1 0 0 0	TIC
m m m m 1 1 0 0	Read Backward
m m m m m m 0 1	Write
m m m m m m 1 0	Read
m m m m m m 1 1	Control

*-Bit Ignored
m-Modifier Bit

Flags

0-CD	Bit 32, causes the address portion of the next CCW to be used.
1-CC	Bit 33, causes the command code and data address in the next CCW to be used.
2-SLI	Bit 34, causes a possible incorrect length indication to be suppressed.
3-SKIP	Bit 35, suppresses the transfer of information to main storage.
4-PCI	Bit 36, causes an interruption as Program Control Interrupt.

Figure 1-65. Channel Command Word (CCW)

CHANNEL ADDRESS WORD

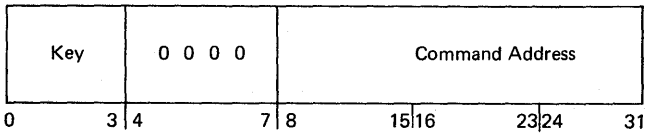
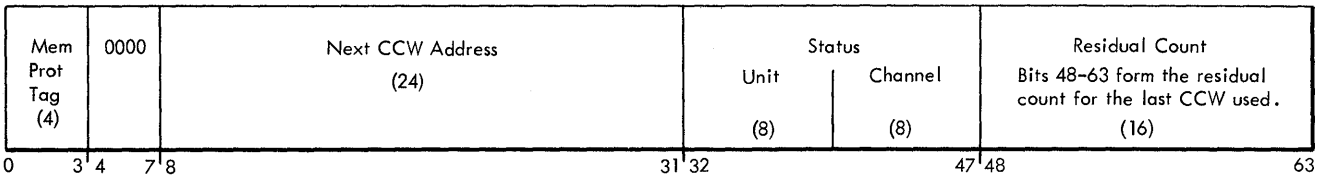
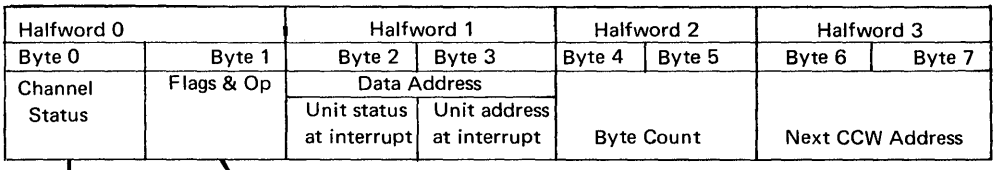


Figure 1-66. Channel Address Word (CAW)



Unit Status	Channel Status
0-Attention	0-PCI
1-Status Modifier	1-Incorrect Length
2-Control Unit End	2-Program Check
3-Busy	3-Protection Check
4-Channel End	4-Channel Data Check
5-Device End	5-Channel Control Check
6-Unit Check	6-Interface Control Check
7-Unit Exception	7-Chaining Check

Figure 1-67. Channel Status Word (CSW)



Byte 1 (Flags and Op)

Bit	Significance
0	CDA (Data Chain in progress)
1	Chain Command (Chain Command in progress)
2	SLI (Suppress Length Indication)
3	Skip
4	PCI (Program Controlled Interrupt)
5	Active (On from time operation initiated at device associated with UCW until channel end has been stored in the CSW).
6	Op 0 (See note)
7	Op 1 (See note)

** With active bits on, bits 6 and 7 decode as follows:

00 = Count zero, expect channel end (after initial selection; Test I/O or Interrupt (during initial selection). If latter, bit 3=0 means Test I/O; bit 3=1 means interrupt.
01 = Output
10 = Read Forward
11 = Read Backward

Byte 0 (Channel Status)

Bit	Significance
0	Secondary*
1	Incorrect Length
2	Program Check
3	Protection Check
4	Channel Data Check**
5	Channel Control Check
6	Interface Control Check
7	Interrupt in Interrupt Buffer*

*Bits 0 and 7 indicate the following:

00 = Handling data, expecting data
01 = Handling data, expecting status
10 = Status queued at I/O device
11 = Status in Interrupt Buffer

** Channel Data Check can be set on only during input operations. The parity check is detected in the CPU A-Register, and no machine check occurs.

Figure 1-68. Channel-UCW Format

1.13 INTEGRATED COMMUNICATIONS ADAPTER (FIGURES 1-69 AND 1-72)

Name	Mnemonic	Code Assignment			
		EBCDIC	Hex	USASCII	Hex
Start of Heading	SOH	SOH	01	SOH	01
Start of Text	STX	STX	02	STX	02
End of Transmission Block	ETB	ETB	26	ETB	17
End of Text	ETX	ETX	03	ETX	03
End of Transmission	EOT	EOT	37	EOT	04
Enquiry	ENQ	ENQ	2D	ENQ	05
Negative Acknowledge	NAK	NAK	3D	NAK	15
Synchronous Idle	SYN	SYN	32	SYN	16
Data Link Escape	DLE	DLE	10	DLE	10
Intermediate Block Character	ITB	IUS	1F	US	1F
Even Acknowledge	ACK0	DLE(70)*	1070	DLE0	1030
Odd Acknowledge	ACK1	DLE/	1061	DLE1	1031
Wait Before Transmit	WABT	DLE(7F)*	107F	DLE?	103F
Mandatory Disconnect	DISC	DLE EOT	1037	DLE EOT	1004
Stop Acknowledge	SAK	DLE,	106B	DLE;	103B
Reverse Interrupt	RVI	DLE@	107C	DLE<	103C
Temporary Text Delay	TTD	STX ENQ	022D	STX ENQ	0205
Transparent Start of Text	XSTX	DLE STX	1002	DLE STX	1002
Transparent Intermediate Block	XITB	DLE IUS	101F	DLE US	101F
Transparent End of Text	XETX	DLE ETX	1003	DLE ETX	1003
Transparent End of Trans. Block	XETB	DLE ETB	1026	DLE ETB	1017
Transparent Synchronous Idle	XSYN	DLE SYN	1032	DLE SYN	1016
Transparent Block Cancel	XENQ	DLE ENQ	102D	DLE ENQ	1005

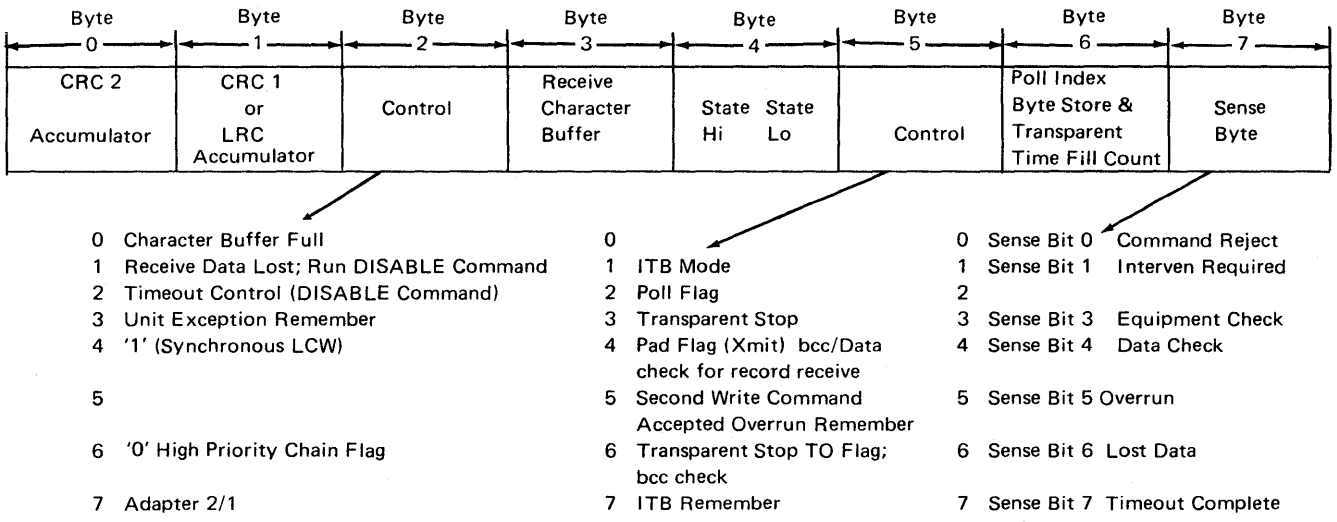
* Hexadecimal representation (no control or graphic assignment)

Figure 1-69. Bisynchronous Control Character Chart

0	1	2	3	4	5	6	7
Channel Status	**Flags and Ops**	**Data Address** / **Unit Status**		**Count**		**Next CCW Address**	

Byte 0	Bit 0	- PCI CHK CHNL STATUS: also before channel status is presented acts to indicate that a pending interrupt is for a PCI interrupt only and not a Channel End-Device End interrupt.
	Bit 1	- Incorrect length record check (ILC).
	Bit 2	- Program check.
	Bit 3	- Protection check.
	Bit 4	- Not used.
	Bit 5	- Not used.
	Bit 6	- Indicates whether the address of the UCW is in the interrupt Q table.
	Bit 7	- Interrupt pending bit.
Byte 1	Bit 0	- Chain Data flag (CD).
	Bit 1	- Chain Command flag (CC).
	Bit 2	- Suppress Length Indication (SLI).
	Bit 3	- SKIP flag.
	Bit 4	- Programmed Controlled Interrupt flag (PCI).
	Bit 5	- Active Bit; on when commands are being executed or when interrupt pends in interrupt Q table.
	Bits 6 and 7	- Decoded as follows.
	0 0	- Count has gone to zero in count field and UCW is waiting for another data transfer request to respond with channel stop and set up to set ILC in CHNL. Status in GEND.
	0 1	- Write type command being executed.
	1 0	- Read type command being executed.
	1 1	- Set when a channel stop is given and will indicate to GEND to signal a possible ILC.
Bytes 2 and 3		- Data Address during command execution
Byte 2		- Device Status at Command End.
	Bit 0	- Not set by ICA
	Bit 1	- Status Modifier
	Bit 2	- Not set by ICA
	Bit 3	- Not set by ICA -- Busy set by CC to SIO, TIO
	Bit 4	- Channel End } Always presented together in ICA
	Bit 5	- Device End } Always presented together in ICA
	Bit 6	- Unit Check
	Bit 7	- Unit Exception
Bytes 4 and 5		- Count Field
Bytes 6 and 7		- Next CCW Address
Byte 7	Bit 7	- On when ICA UCW is not operational (tested in DCLA)

Figure 1-70. ICA UCW Format



LCW Byte 4

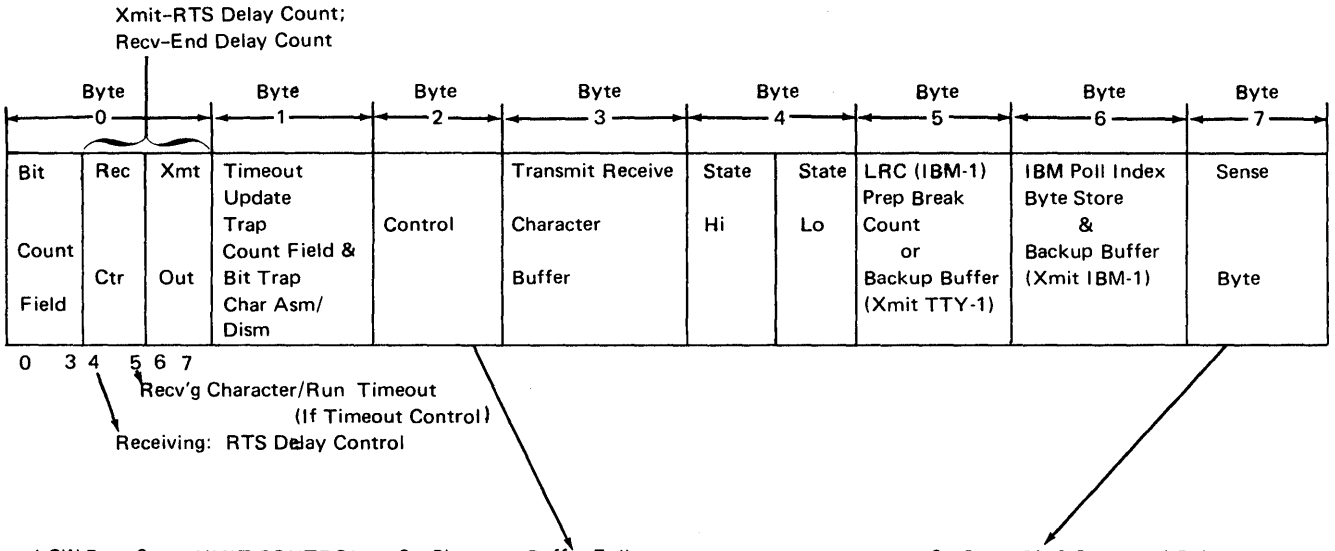
STATE HI DECODE

BIT	0	1	2	3			
HEX					TRANSMITTING	RECEIVING	CONTROL STATE
0	0	0	0	0	Monitor For Clear to Send	Monitor For First Non-SYN	DISABLE
1	0	0	0	1	DLE Decoded, Not In Text Mode	DLE Decoded, Not in Text Mode	
2	0	0	1	0	End (WRITE); Turnaround (POLL)	Monitor For First Non-SYN, Poll Read	ENABLE
3	0	0	1	1	Not In Text Mode	Receive First Non-SYN Not in Text Mode	DIAL
4	0	1	0	0	Transmit CRC-2	Expect CRC-2	PREPARE
5	0	1	0	1	Transmit Pad Character	Invalid Decode	
6	0	1	1	0	Xmit SYN Time Fill, Transparent Stop	Invalid Decode	
7	0	1	1	1	Xmit DLE Time Fill, Transparent Stop	Invalid Decode	
8	1	0	0	0	Transmit CRC-1 (or LRC)	Expect CRC-1 (or LRC)	
9	1	0	0	1	DLE Decoded in Text Mode	DLE Decoded, In Text Mode	
A	1	0	1	0	Xmit, SYN Time Fill In Text Mode	SYN Decoded, In Text Mode	
B	1	0	1	1	Text Mode	Text Mode	
C	1	1	0	0	ENQ Decoded, in Poll Transmit	Text Mode	
D	1	1	0	1	DLE Decoded Transparent Mode or Transparent Stop	DLE Decoded, In Transparent Mode	
E	1	1	1	0	Xmit SYN Time Fill, Transparent Mode	DLE SYN Decoded, In Transparent Mode	
F	1	1	1	1	Transparent Mode or Transparent Stop	Transparent Mode	

STATE LO DECODE

BIT	4	5	6	7	
HEX					
0	0	0	0	0	Control State; DIAL Step 1
1	0	0	0	1	WRITE
2	0	0	1	0	Receive Monitor
3	0	0	1	1	READ
4	0	1	0	0	DIAL Step 2
5	0	1	0	1	POLL Write
6	0	1	1	0	Invalid Decode
7	0	1	1	1	POLL Read
8	1	0	0	0	DIAL Step 3
9	1	0	0	1	Invalid Decode
A	1	0	1	0	ADPREP Monitor
B	1	0	1	1	Invalid Decode
C	1	1	0	1	Invalid Decode
D	1	1	0	1	Invalid Decode
E	1	1	1	0	ADPREP Control
F	1	1	1	1	Invalid Decode

Figure 1-71. Synchronous LCW Format



LCW Byte 0 BIT	6	7	XMIT CONTROL DECODE
HEX			
0	0	0	
1	0	1	Transmit Normal
2	1	0	Transmit Break (TTY)
3	1	1	Transmit End

0	Character Buffer Full
1	Recv. Data Lost (Recv); Pad Control (Write)
2	T.O. Control
3	Poll Flag (IBM)
4	'0' (Start/stop LCW)
5	Telegraph Adapter Echo check or TTY II Break Detected (Xmit)
6	TTY II Space Remem (Xmit) Stop Bit Error (Recv)
7	Data Bit Transfer Check (Xmit)

0	Sense Bit 0 Command Reject
1	Sense Bit 1 Intervention Required
2	Unit Exception Status Remember
3	Sense Bit 3 Equipment Check
4	Sense Bit 4 Data Check
5	Sense Bit 5 Overrun
6	Sense Bit 6 Lost Data
7	Sense Bit 7 Timeout Complete

LCW BYTE 0 — BIT COUNT FIELD DECODE

BIT HEX	0	1	2	3	RECEIVING	TTY II	IBM I	IBM II	TTY I	TRANSMITTING	TTY II	IBM I	IBM II	TTY I
0	0	0	0	0						Pad Start Bit				
1	0	0	0	1	Normal Data Bit					First Data Bit	1	B	B	1
2	0	0	1	0	Normal Data Bit	2				Normal Data Bit	2			
3	0	0	1	1	Normal Data Bit	3	A	A		Normal Data Bit	3	A	A	
4	0	1	0	0	Normal Data Bit	4	8	8		Normal Data Bit	4	8	8	
5	0	1	0	1	Normal Data Bit	5	4	4	2	Normal Data Bit	5	4	4	2
6	0	1	1	0	Normal Data Bit	6	2	2	3	Normal Data Bit	6	2	2	3
7	0	1	1	1	Normal Data Bit	7	1	1	4	Normal Data Bit	7	1	1	4
8	1	0	0	0	Last Data Bit	8	C	C	5	Normal Data Bit	8	C	C	5
9	1	0	0	1	Stop Bit					Stop 1 Bit (IBM-II, TTY-II)	S		S	
A	1	0	1	0	Xmit RTS Delay					Xmit CTS Test				
B	1	0	1	1	Enable Dial DCD Test					Normal Start Bit				
C	1	1	0	0	Recv. End Delay					Transmit End 1				
D	1	1	0	1										
E	1	1	1	0	First Data Bit	1	B	B	1	Transmit End 2				
F	1	1	1	1						Final Stop Bit				

Figure 1-72. Start/Stop LCW Format (Part 1 of 2)

LCW Byte 4

STATE HI DECODE

BIT HEX	0	1	2	3	IBM XMIT/RECV	TTY XMIT/RECV	CONTROL STATE
0	0	0	0	0	Receive Monitor	Receive Monitor	Receive Monitor (DISABLE)
1	0	0	0	1	Invalid Decode	Read Data, TTY-I	PREPARE Break
2	0	0	1	0			ENABLE (Switched Network)
3	0	0	1	1	Read Data	Read Data, TTY-II	DIAL (IBM-I, TTY-II)
4	0	1	0	0	Read LRC, IBM-I	Invalid Decode	PREPARE
5	0	1	0	1	Read End IBM	Read End TTY	
6	0	1	1	0	Invalid Decode	Read FIGS H Remember, TTY-I	
7	0	1	1	1	Poll Read	Read First Non LTRS, TTY-I	
8	1	0	0	0	Write Data	Write Data, TTY-II	
9	1	0	0	1	Write Stop	Write Stop	
A	1	0	1	0	Write LRC, IBM-I	Break Data	
B	1	0	1	1	Write Prepend	Write Shift Remember, TTY-I	
C	1	1	0	0	Write Shift Remember, IBM-I	Write Data, TTY-I	
D	1	1	0	1	Poll Initial		
E	1	1	1	0	Poll Write	Break Initial	
F	1	1	1	1	Write End	Write End	

STATE LO DECODE

BIT HEX	4	5	6	7	
0	0	0	0	0	Control State; DIAL Step 1
1	0	0	0	1	IBM Text in Downshift Mode: IBM POLL Write Step 3
2	0	0	1	0	TTY Downshift Mode
3	0	0	1	1	IBM Control, (Downshift) Mode
4	0	1	0	0	DIAL Step 2
5	0	1	0	1	IBM Text Out. Downshift Mode: POLL Write Step 2
6	0	1	1	0	Invalid
7	0	1	1	1	IBM, Control, Downshift Mode: POLL Write Step 1
8	1	0	0	0	DIAL Step 3
9	1	0	0	1	IBM-I Text In, Upshift Mode
A	1	0	1	0	TTY-I Upshift Mode
B	1	0	1	1	IBM-I Control, (Upshift Mode)
C	1	1	0	0	Invalid
D	1	1	0	1	IBM-I Text Out, Upshift Mode; IBM POLL Write Step 0
E	1	1	1	0	Invalid
F	1	1	1	1	IBM-I Control, (Upshift Mode)

Figure 1-72. Start/Stop LCW Format (Part 2 of 2)

1.14 1403 PRINTER (FIGURES 1-73 THROUGH 1-95)

Figure 1-73 shows the possible Start I/O command byte configurations for the 1403. The legend for this figure is as follows.

Char in Column	Printer Command
b	Sense
c	Write with valid carriage-control
d	No-Op
e	Carriage control with valid carriage-control modifier
f	Load multiple character set (MCS) and fold
g	Load multiple character set (MCS) and no fold
h	Gate load
j	Block data check
k	Allow data check.

BITS 0123 ↓	BITS 4567															
	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000		c		d	b					c		e				
0001		c		e						c		e				
0010																
0011																
0100																
0101																
0110																
0111				j								k				
1000										c		e				
1001		c		e						c		e				
1010		c		e						c		e				
1011		c		e						c		e				
1100		c		e						c		e				
1101		c		e						c		e				
1110		c		e								h				
1111				f								g				

Figure 1-73. 1403 Command Byte Description

"PCS-AN" (3 LEVEL SET-48 "A" GRAPHICS)

Note I

12	34	56	78	90	,-	PQ	R#	$@	/S	TU	VW	XY	Z⌑	.*	12	34	56	78	90	,-	JK	LM	NO	AB	CD	EF	GH	I+	.*
							R&	$%																					

"PCS-HN" (3 LEVEL SET-48 "H" GRAPHICS)

Note I

12	34	56	78	90	,-	PQ	R=	$'	/S	TU	VW	XY	Z)	.*	12	34	56	78	90	,-	JK	LM	NO	AB	CD	EF	GH	I+	.*
							R&	$(																					

"AN"

Note III

12	34	56	78	90	#@	/S	TU	VW	XY	Z&	,%	JK	LM	NO	PQ	R-	$*	AB	CD	EF	GH	I+	.⌑

"HN"

Note III

12	34	56	78	90	='	/S	TU	VW	XY	Z&	,(	JK	LM	NO	PQ	R-	$*	AB	CD	EF	GH	I+	.)

"PN" PL/I (60 GRAPHICS)

Note II

12	34	56	78	90	XY	/S	TU	VW	|:	_"	,=	JK	LM	NO	PQ	R-	Z(	AB	CD	EF	GH	I+	.)	%$	*#	&@	<;	¬'	?>

"QN" PL/I (60 GRAPHICS-45 PREFERRED)

12	34	56	78	90	XY	/S	TU	VW	_"	$*	,=	JK	LM	NO	PQ	R-	Z(	AB	CD	EF	GH	I+	.)
									<;	#*													
									?>	@*													
									¬'	&*													
									|:	%*													

Note I Two full sets per cartridge arrangement
Note II Four full sets per cartridge arrangement
Note III Five full sets per cartridge arrangement
Note IV Six full sets per cartridge arrangement

"RN" FORTRAN COBOL COMMERCIAL (52 GRAPHICS-47 PREFERRED)

12	34	56	78	90	XY	/S	TU	VW	'@	$*	,=	JK	LM	NO	PQ	R-	Z(	AB	CD	EF	GH	I+	.)
									%@														
									#@														
									⌑@														
									&@														

"SN" TEXT PRINTING (84 GRAPHICS-78 PREFERRED)

12	34	56	78	90	&.	/S	TU	VW	XY	Z,	$*	JK	LM	NO	PQ	R-	":	AB	CD	EF	GH	I+	ab	cd	ef	gh	ij	kl	mn	op	qr	st	uv	wx	yz	@'	()	-|			
																																							?!	;¢	%⌑

"TN" TEXT PRINTING (120 GRAPHICS)

Note I

12	34	56	78	90	=.	/S	TU	VW	XY	Z,	#&	JK	LM	NO	PQ	R-	":	AB	CD	EF	GH	I+	ab	cd	ef	gh	ij	kl	mn
op	qr	st	uv	wx	yz	@'	?;	±!	$*	%⌑	12	34	56	78	90	-+	()	°¬	( )	≠+	><	≤≥	¢•	[ ]	} {	└ ┘	┌ ┐	•_	-|

"XN" HIGH SPEED ALPHANUMERIC (40 GRAPHICS)

Note IV

12	34	56	78	90	,.	AB	CD	EF	GH	IZ	JK	LM	NO	PQ	R*	$S	TU	VW	XY

ODA - FIRST ARRAY

Note III

12	34	56	78	90	#@	/S	TU	VW	XY	Z&	,%	JK	LM	NO	PQ	R-	$*	AB	CD	EF	GH	I+	.⌑

ONA - FIRST ARRAY

Note III

12	34	56	78	90	#@	/S	TU	VW	XY	Z&	,H	JK	LM	NO	PQ	R-	$*	AB	CD	EF	GH	IY	.♪

OAA - FIRST ARRAY

Note III

12	34	56	78	90	#@	/S	TU	VW	XY	Z&	¬%	JK	LM	NO	PQ	R-	$*	AB	CD	EF	GH	I+	.<

ONB - FIRST ARRAY (WTC Only)

Note III

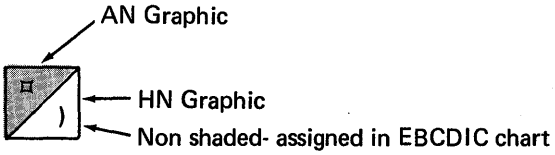
12	34	56	78	90	='	/S	TU	VW	XY	Z&	,>	JK	LM	NO	PQ	R-	$*	AB	CD	EF	GH	I+	.<

Figure 1-74. Chain Arrangements for System/360 (Printout Representation)

Note I Two full sets per cartridge arrangement
Note II Four full sets per cartridge arrangement
Note III Five full sets per cartridge arrangement

Figure 1-75. Train Arrangements for System/360 (Printout Representation)

	0X	1X	2X	3X	4X	5X	6X	7X	8X	9X	AX	BX	CX	DX	EX	FX
X0		&	–	0		&	–	0	&	–		0	&	–		0
X1	A	J	/	1	A	J	/	1	A	J	/	1	A	J	/	1
X2	B	K	S	2	B	K	S	2	B	K	S	2	B	K	S	2
X3	C	L	T	3	C	L	T	3	C	L	T	3	C	L	T	3
X4	D	M	U	4	D	M	U	4	D	M	U	4	D	M	U	4
X5	E	N	V	5	E	N	V	5	E	N	V	5	E	N	V	5
X6	F	O	W	6	F	O	W	6	F	O	W	6	F	O	W	6
X7	G	P	X	7	G	P	X	7	G	P	X	7	G	P	X	7
X8	H	Q	Y	8	H	Q	Y	8	H	Q	Y	8	H	Q	Y	8
X9	I	R	Z	9	I	R	Z	9	I	R	Z	9	I	R	Z	9
XA	+	–	&	0	+	–	&	0	+	–	&	0	+	–	&	0
XB	.	$	,	# / =	.	$	,	# / =	.	$	,	# / =	.	$	,	# / =
XC	¤ /)	*	% / (	@ / '	¤ /)	*	% / (	@ / '	¤ /)	*	% / (	@ / '	¤ /)	*	% / (	@ / '
XD	% / (	¤ /)		@ / '	% / (	¤ /)		@ / '	% / (	¤ /)		@ / '	% / (	¤ /)		@ / '
XE	+		,	# / =	+		,	# / =	+		,	# / =	+		,	# / =
XF																



Characters printed are basic integrated 1403.
Non-shaded graphics indicate the defined codes
in the EBCD interchange code chart.

Figure 1-76. AN and HN Graphics for Basic 1403 Attachment

Command Byte 0 1 2 3	4 5 6 7	Function
0 0 0 0	0 0 0 1	Write and No Space After Print
0 0 0 0	1 0 0 1	Write and Space 1 Line After Print
0 0 0 1	0 0 0 1	Write and Space 2 Lines After Print
0 0 0 1	1 0 0 1	Write and Space 3 Lines After Print
1 0 0 0	1 0 0 1	Write and Skip to Channel 1 After Print
1 0 0 1	0 0 0 1	Write and Skip to Channel 2 After Print
1 0 0 1	1 0 0 1	Write and Skip to Channel 3 After Print
1 0 1 0	0 0 0 1	Write and Skip to Channel 4 After Print
1 0 1 0	1 0 0 1	Write and Skip to Channel 5 After Print
1 0 1 1	0 0 0 1	Write and Skip to Channel 6 After Print
1 0 1 1	1 0 0 1	Write and Skip to Channel 7 After Print
1 1 0 0	0 0 0 1	Write and Skip to Channel 8 After Print
1 1 0 0	1 0 0 1	Write and Skip to Channel 9 After Print
1 1 0 1	0 0 0 1	Write and Skip to Channel 10 After Print
1 1 0 1	1 0 0 1	Write and Skip to Channel 11 After Print
1 1 1 0	0 0 0 1	Write and Skip to Channel 12 After Print

Figure 1-77. 1403 Commands (Write Operation with Various Carriage Functions)

Command Bytes 0 1 2 3	4 5 6 7	Function
0 0 0 0	1 0 1 1	Space 1 Line Immediately
0 0 0 1	0 0 1 1	Space 2 Lines Immediately
0 0 0 1	1 0 1 1	Space 3 Lines Immediately
1 0 0 0	1 0 1 1	Skip to Channel 1 Immediately
1 0 0 1	0 0 1 1	Skip to Channel 2 Immediately
1 0 0 1	1 0 1 1	Skip to Channel 3 Immediately
1 0 1 0	0 0 1 1	Skip to Channel 4 Immediately
1 0 1 0	1 0 1 1	Skip to Channel 5 Immediately
1 0 1 1	0 0 1 1	Skip to Channel 6 Immediately
1 0 1 1	1 0 1 1	Skip to Channel 7 Immediately
1 1 0 0	0 0 1 1	Skip to Channel 8 Immediately
1 1 0 0	1 0 1 1	Skip to Channel 9 Immediately
1 1 0 1	0 0 1 1	Skip to Channel 10 Immediately
1 1 0 1	1 0 1 1	Skip to Channel 11 Immediately
1 1 1 0	0 0 1 1	Skip to Channel 12 Immediately

Figure 1-78. 1403 Commands (Independent Carriage Operations)

Command Byte 0 1 2 3	4 5 6 7	Function
0 0 0 0	0 0 1 1	No-Op
0 1 1 1	0 0 1 1	Block Data Check
0 1 1 1	1 0 1 1	Allow Data Check
1 1 1 0	1 0 1 1	Gate Load
1 1 1 1	0 0 1 1	Load MCS and Fold
1 1 1 1	1 0 1 1	Load MCS and No Fold
0 0 0 0	0 1 0 0	Sense

Figure 1-79. 1403 Commands (No Printing or Carriage Motion)

7X00 or 9X00		Set Length (Decimal)
Not Block Data Check	Block Data Check	
01	81	16
02	82	40
04	84	48
08	88	60
10	90	80
20	A0	120
40	C0	240
00	80	240

Figure 1-80. PCCL Code for Different Character Set Lengths

Figure 1-81 shows the contents of the translate table for the basic attachment. The table is loaded for dualed and folded AN or HN chains or trains. The table causes the same translation as the non-UCS translator in the 2821 control unit. The table is loaded in the preceding manner when the control storage is reloaded with a System/360 load. When control storage is loaded with a System/360 load with MCS, the translate table is unaffected.

PCCL byte is shown with block data check not set.

da 7000

0425 2627 2829 2A2B 2C2D 2E2F 3018 2E00
1619 1A1B 1C1D 1E1F 2021 2223 2430 0000

220D 0E0F 1011 1213 1415 1617 1800 1700
0A01 0203 0405 0607 0809 0A0B 0C0C 0B00

0025 2627 2829 2A2B 2C2D 2E2F 3018 2E00
1619 1A1B 1C1D 1E1F 2021 2223 2430 0000

220D 0E0F 1011 1213 1415 1617 1800 1700
0A01 0203 0405 0607 0809 0A0B 0C0C 0B00

0025 2627 2829 2A2B 2C2D 2E2F 3018 2E00
1619 1A1B 1C1D 1E1F 2021 2223 2430 0000

220D 0E0F 1011 1213 1415 1617 1800 1700
0A01 0203 0405 0607 0309 0A0B 0C0C 0B00

0025 2627 2829 2A2B 2C2D 2E2F 3018 2E00
1619 1A1B 1C1D 1E1F 2021 2223 2430 0000

220D 0E0F 1011 1213 1415 1617 1800 1700
0A01 0203 0405 0607 0809 0A0B 0C0C 0B00

Note:
Graphics are folded and dualed aswith the IBM 2821 non-UCS translator.

Graphic

Graphic Position Code

	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18
AN	1	2	3	4	5	6	7	8	9	0	#	@	/	S	T	U	V	W	X	Y	Z	&	,	%
HN																								(
	19	1A	1B	1C	1D	1E	1F	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30
AN	J	K	L	M	N	O	P	Q	R	–	$	*	A	B	C	D	E	F	G	H	I	+	.	¤
HN																								)

Figure 1-81. Printer Translate Table (Basic Attachment)

Figures 1-82 through 1-94 show several different versions of the translate table for different MCS chain or train arrangements.

When preferred-character arrangements with MCS are used, only the last character set of the arrangement and unique characters in the other sets are printable positions. These positions are indicated by the heavy bar in the graphic position code charts.

PCCL byte is shown with block data check not set.

```
da 7000
01FF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF

FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF

00FF FFFF FFFF FFFF FFFF FF0F 10FF FFFF
FFFF FFFF FFFF FFFF FFFF FF0D 0E10 FFFF

0CFF FFFF FFFF FFFF FFFF FF0B FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF

FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF

FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF

FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF

FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
0A01 0203 0405 0607 0800 FFFF FFFF FFFF
```

(Not Folded)

```
da 7000
01FF FFFF FFFF FFFF FFFF FF0F 10FF FFFF
FFFF FFFF FFFF FFFF FFFF FF0D 0E10 FFFF

0CFF FFFF FFFF FFFF FFFF FF0B FFFF FFFF
0A01 0203 0405 0607 0809 FFFF FFFF FFFF

00FF FFFF FFFF FFFF FFFF FF0F 10FF FFFF
FFFF FFFF FFFF FFFF FFFF FF0D 0E10 FFFF

0CFF FFFF FFFF FFFF FFFF FF0B FFFF FFFF
0A01 0203 0405 0607 0809 FFFF FFFF FFFF

00FF FFFF FFFF FFFF FFFF FF0F 10FF FFFF
FFFF FFFF FFFF FFFF FFFF FF0D 0E10 FFFF

0CFF FFFF FFFF FFFF FFFF FF0B FFFF FFFF
0A01 0203 0405 0607 0809 FFFF FFFF FFFF

00FF FFFF FFFF FFFF FFFF FF0F 10FF FFFF
FFFF FFFF FFFF FFFF FFFF FF0D 0E10 FFFF

0CFF FFFF FFFF FFFF FFFF FF0B FFFF FFFF
0A01 0203 0405 0607 0809 FFFF FFFF FFFF
```

(Folded)

Graphic Position Code	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18
Graphic	1	2	3	4	5	6	7	8	9	0	,	–	$	*	.	¤								

Figure 1-82. Printer Translate Table for MCS: Numeric Arrangement; Count Length 10 (Hex)

```
da 7000
04FF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
00FF FFFF FFFF FFFF FFFF FF2F 3018 2EFF
16FF FFFF FFFF FFFF FFFF FF23 2430 FFFF
220D FFFF FFFF FFFF FFFF FF17 18FF FFFF
FFFF FFFF FFFF FFFF FFFF FF0B 0C0C 0BFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FF25 2627 2829 2A2B FFFF FFFF FFFF FFFF
FF19 1A1B 1C1D 1E1F 2021 FFFF FFFF FFFF
FFFF 0E0F 1011 1213 1415 FFFF FFFF FFFF
0A01 0203 0405 0607 0809 FFFF FFFF FFFF
```

AN (Not Folded)

```
da 7000
04FF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
00FF FFFF FFFF FFFF FFFF FF2F 3018 2EFF
16FF FFFF FFFF FFFF FFFF FF23 2430 FFFF
220D FFFF FFFF FFFF FFFF FF17 18FF FFFF
FFFF FFFF FFFF FFFF FFFF FF0B 0C0C 0BFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FF25 2627 2829 2A2B 2C2D FFFF FFFF FFFF
FF19 1A1B 1C1D 1E1F 2021 FFFF FFFF FFFF
FFFF 0E0F 1011 1213 1415 FFFF FFFF FFFF
0A01 0203 0405 0607 0809 FFFF FFFF FFFF
```

HN (Not Folded)

Graphic

Graphic Position Code

	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18
AN	1	2	3	4	5	6	7	8	9	0	#	@	/	S	T	U	V	W	X	Y	Z	&	,	%
HN											=	,												(

	19	1A	1B	1C	1D	1E	1F	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30
AN	J	K	L	M	N	O	P	Q	R	–	$	*	A	B	C	D	E	F	G	H	I	+	.	¤
HN																								)

Figure 1-83. Printer Translate Table for MCS: AN-HN Arrangement; Count Length 30 (Hex)

```
da 7000
0425 2627 2829 2A2B 2C2D FF2F 3018 2EFF
1619 1A1B 1C1D 1E1F 2021 FF23 2430 FFFF
220D 0E0F 1011 1213 1415 FF17 18FF FFFF
0A01 0203 0405 0607 0809 FF0B 0C0C 0BFF
0025 2627 2829 2A2B 2C2D FF2F 3018 2EFF
1619 1A1B 1C1D 1E1F 2021 FF23 2430 FFFF
220D 0E0F 1011 1213 1415 FF17 18FF FFFF
0A01 0203 0405 0607 0809 FF0B 0C0C 0BFF
0025 2627 2829 2A2B 2C2D FF2F 3018 2EFF
1619 1A1B 1C1D 1E1F 2021 FF23 2430 FFFF
220D 0E0F 1011 1213 1415 FF17 18FF FFFF
0A01 0203 0405 0607 0809 FF0B 0C0C 0BFF
0025 2627 2829 2A2B 2C2D FF2F 3018 2EFF
1619 1A1B 1C1D 1E1F 2021 FF23 2430 FFFF
220D 0E0F 1011 1213 1415 FF17 18FF FFFF
0A01 0203 0405 0607 0809 FF0B 0C0C 0BFF
```

AN (Folded)

```
da 7000
0425 2627 2829 2A2B 2C2D FF2F 3018 2EFF
1619 1A1B 1C1D 1E1F 2021 FF23 2430 FFFF
220D 0E0F 1011 1213 1415 FF17 18FF FFFF
0A01 0203 0405 0607 0809 FF0B 0C0C 0BFF
0025 2627 2829 2A2B 2C2D FF2F 3018 2EFF
1619 1A1B 1C1D 1E1F 2021 FF23 2430 FFFF
220D 0E0F 1011 1213 1415 FF17 18FF FFFF
0A01 0203 0405 0607 0809 FF0B 0C0C 0BFF
0025 2627 2829 2A2B 2C2D FF2F 3018 2EFF
1619 1A1B 1C1D 1E1F 2021 FF23 2430 FFFF
220D 0E0F 1011 1213 1415 FF17 18FF FFFF
0A01 0203 0405 0607 0809 FF0B 0C0C 0BFF
0025 2627 2829 2A2B 2C2D FF2F 3018 2EFF
1619 1A1B 1C1D 1E1F 2021 FF23 2430 FFFF
220D 0E0F 1011 1213 1415 FF17 18FF FFFF
0A01 0203 0405 0607 0809 FF0B 0C0C 0BFF
```

HN (Folded)

Graphic

Graphic Position Code

01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18
1	2	3	4	5	6	7	8	9	0	#	@	/	S	T	U	V	W	X	Y	Z	&	.	% (

19	1A	1B	1C	1D	1E	1F	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30
J	K	L	M	N	O	P	Q	R	–	$	*	A	B	C	D	E	F	G	H	I	+	.	¤)

Figure 1-84. Printer Translate Table for MCS: AN-HN Folded; Count Length 30 (Hex)

```
da 7000
08FF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
00FF FFFF FFFF FFFF FFFF FF2F 3724 2E13
35FF FFFF FFFF FFFF FFFF FF32 3330 3839
220D FFFF FFFF FFFF FFFF FF17 3115 3C3B
FFFF FFFF FFFF FFFF FFFF 1434 363A 1816
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FF25 2627 2829 2A2B 2C2D FFFF FFFF FFFF
FF19 1A1B 1C1D 1E1F 2021 FFFF FFFF FFFF
FFFF 0E0F 1011 120B 0C23 FFFF FFFF FFFF
0A01 0203 0405 0607 0809 FFFF FFFF FFFF
```

(Not Folded)

```
da 7000
0825 2627 2829 2A2B 2C2D FF2F 3724 2E13
3519 1A1B 1C1D 1E1F 2021 FF32 3330 3839
220D 0E0F 1011 120B 0C23 FF17 3115 3C3B
0A01 0203 0405 0607 0809 1434 363A 1816
0025 2627 2829 2A2B 2C2D FF2F 3724 2E13
3519 1A1B 1C1D 1E1F 2021 FF32 3330 3839
220D 0E0F 1011 120B 0C23 FF17 3115 3C3B
0A01 0203 0405 0607 0809 1434 363A 1816
0025 2627 2829 2A2B 2C2D FF2F 3724 2E13
3519 1A1B 1C1D 1E1F 2021 FF32 3330 3839
220D 0E0F 1011 120B 0C23 FF17 3115 3C3B
0A01 0203 0405 0607 0809 1434 363A 1816
0025 2627 2829 2A2B 2C2D FF2F 3724 2E13
3519 1A1B 1C1D 1E1F 2021 FF32 3330 3839
220D 0E0F 1011 120B 0C23 FF17 3115 3C3B
0A01 0203 0405 0607 0809 1434 363A 1816
```

(Folded)

Graphic

Graphic Position Code

01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18
1	2	3	4	5	6	7	8	9	0	X	Y	/	S	T	U	V	W	|	:	_	"	,	=

19	1A	1B	1C	1D	1E	1F	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30
J	K	L	M	N	O	P	Q	R	–	Z	(	A	B	C	D	E	F	G	H	I	+	.	)

31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F	40	41	42	43	44	45	46	47	48
%	$	*	#	&	@	<	;	¬	'	?	>												

Figure 1-85. Printer Translate Table for MCS: PN Arrangement; Count Length 3C (Hex)

```
da 7000
20FF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
00FF FFFF FFFF FFFF FFFF FF77 58FF 76FF
4CFF FFFF FFFF FFFF FFFF FF4D 78FF FFFF
664F FFFF FFFF FFFF FFFF FF65 4EFF FFFF
FFFF FFFF FFFF FFFF FFFF FF10 12FF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FF6D 6E6F 7071 7273 7475 FFFF FFFF FFFF
FF67 6869 6A6B 6C49 4A4B FFFF FFFF FFFF
FFFF 5051 5253 5455 5657 FFFF FFFF FFFF
6458 5C5D 5E5F 6061 6263 FFFF FFFF FFFF
```

(Not Folded)

```
da 7000
206D 6E6F 7071 7273 7475 FF77 58FF 76FF
4C67 6869 6A6B 6C49 4A4B FF4D 78FF FFFF
664F 5051 5253 5455 5657 FF65 4EFF FFFF
645B 5C5D 5E5F 6061 6263 FF10 12FF FFFF
006D 6E6F 7071 7273 7475 FF77 58FF 78FF
4C67 6869 6A6B 6C49 4A4B FF4D 78FF FFFF
664F 5051 5255 5455 5657 FF65 4EFF FFFF
645B 5C5D 5E5F 6061 6263 FF10 12FF FFFF
006D 6E6F 7071 7273 7475 FF77 58FF 76FF
4C67 6869 6A6B 6C49 4A4B FF4D 78FF FFFF
664F 5051 5253 5455 5657 FF65 4EFF FFFF
645B 5C5D 5E5F 6061 6263 FF10 12FF FFFF
006D 6E6F 7071 7273 7475 FF77 58FF 76FF
4C67 6866 6A6B 6C49 4A4B FF4D 78FF FFFF
664F 5051 5253 5455 5657 FF65 4EFF FFFF
645B 5C5D 5E5F 6061 6263 FF10 12FF FFFF
```

(Folded)

Graphic

Graphic Position Code

01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18
															#		@						

19	1A	1B	1C	1D	1E	1F	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30

31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F	40	41	42	43	44	45	46	47	48

49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F	60
P	Q	R	&	$	%	/	S	T	U	V	W	X	Y	Z	¤			1	2	3	4	5	6

61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F	70	71	72	73	74	75	76	77	78
7	8	9	0	,	–	J	K	L	M	N	O	A	B	C	D	E	F	G	H	I	+	.	*

Figure 1-86. Printer Translate Table for MCS: PCS-AN Arrangement; Count Length 78 (Hex)

da 7000

```
20FF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
00FF FFFF FFFF FFFF FFFF FF77 FF4E 76FF
4CFF FFFF FFFF FFFF FFFF FF4D 7858 FFFF
664F FFFF FFFF FFFF FFFF FF65 FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FF12 10FF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FF6D 6E6F 7071 7273 7475 FFFE FFFF FFFF
FF67 6869 6A6B 6C49 4A4B FFFF FFFF FFFF
FFFF 5051 5253 5455 5657 FFFF FFFF FFFF
6458 5C5D 5E5F 6061 6263 FFFF FFFF FFFF
```

(Not Folded)

da 7000

```
206D 6E6F 7071 7273 7475 FF77 FF4E 76FF
4C67 6869 6A6B 6C49 4A4B FF4D 7858 FFFF
664F 5051 5253 5455 5657 FF65 FFFF FFFF
645B 5C5D 5E5F 6061 6263 FFFF FF12 10FF
006D 6E6F 7071 7273 7475 FF77 FF4E 76FF
4C67 6869 6A6B 6C49 4A4B FF4D 7858 FFFF
664F 5051 5253 5455 5657 FF65 FFFF FFFF
645B 5C5D 5E5F 6061 6263 FFFF FF12 10FF
006D 6E6F 7071 7273 7475 FF77 FF4E 76FF
4C67 6869 6A6B 6C49 4A4B FF4D 7858 FFFF
664F 5051 5253 5455 5657 FF65 FFFF FFFF
645B 5C5D 5E5F 6061 6263 FFFF FF12 10FF
006D 6E6F 7071 7273 7475 FF77 FF4E 76FF
4C67 6869 6A6B 6C49 4A4B FF4D 7858 FFFF
664F 5051 5253 5455 5657 FF65 FFFF FFFF
645B 5C5D 5E5F 6061 6263 FFFF FF12 10FF
```

(Folded)

Graphic

Graphic Position Code

Graphic Position Code	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18
Graphic																=		'						

Graphic Position Code	19	1A	1B	1C	1D	1E	1F	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30
Graphic																								

Graphic Position Code	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F	40	41	42	43	44	45	46	47	48
Graphic																								

Graphic Position Code	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F	60
Graphic	P	Q	R	&	$	(	/	S	T	U	V	W	X	Y	Z	)			1	2	3	4	5	6

Graphic Position Code	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F	70	71	72	73	74	75	76	77	78
Graphic	7	8	9	0	,	–	J	K	L	M	N	O	A	B	C	D	E	F	G	H	I	+	.	*

Figure 1-87. Printer Translate Table for MCS: PCS-HN Arrangement; Count Length 78 (Hex)

```
da 7000
40FF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
00FF FFFF FFFF FFFF FFFF FFEF 43E4 EED3
A5FF FFFF FFFF FFFF FFFF FF15 D6F0 44A3
E2CD FFFF FFFF FFFF FFFF FFD7 D513 7473
FFFF FFFF FFFF FFFF FFFF D445 75A4 D814
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFE5 E6E7 E8E9 EAEB ECED FFFF FFFF FFFF
FFD9 DADB DCDD DEDF E0E1 FFFF FFFF FFFF
FFFF CECF D0D1 D2CB CCE3 FFFF FFFF FFFF
CAC1 C2C3 C4C5 C6C7 C8C9 FFFF FFFF FFFF
```

(Not Folded)

```
da 7000
40E5 E6E7 E8E9 EAEB ECED FFEF 43E4 EED3
A5D9 DADB DCDD DEDF E0E1 FF15 D6F0 44A3
E2CD CECF D0D1 D2CB CCE3 FFD7 D513 7473
CAC1 C2C3 C4C5 C6C7 C8C9 D445 75A4 D814
00E5 E6E7 E8E9 EAEB ECED FFEF 43E4 EED3
A5D9 DADB DCDD DEDF E0E1 FF15 D6F0 44A3
E2CD CECF D0D1 D2CB CCE3 FFD7 D513 7473
CAC1 C2C3 C4C5 C6C7 C8C9 D445 75A4 D814
00E5 E6E7 E8E9 EAEB ECED FFEF 43E4 EED3
A5D9 DADB DCDD DEDF E0E1 FF15 D6F0 44A3
E2CD CECF D0D1 D2CB CCE3 FFD7 D513 7473
CAC1 C2C3 C4C5 C6C7 C8C9 D445 75A4 D814
00E5 E6E7 E8E9 EAEB ECED FFEF 43E4 EED3
A5D9 DADB DCDD DEDF E0E1 FF15 D6F0 44A3
E2CD CECF D0D1 D2CE CCE3 FFD7 D513 7473
CAC1 C2C3 C4C5 C6C7 C8C9 D445 75A4 D814
```

(Folded)

Graphic

Graphic Position Code

Graphic Position Code	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18
Graphic																			_	"	$			

Graphic Position Code	19	1A	1B	1C	1D	1E	1F	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30
Graphic																								

Graphic Position Code	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F	40	41	42	43	44	45	46	47	48
Graphic																			<	;	#			

Graphic Position Code	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F	60
Graphic																								

Graphic Position Code	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F	70	71	72	73	74	75	76	77	78
Graphic																			?	>	@			

Graphic Position Code	79	7A	7B	7C	7D	7E	7F	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F	90
Graphic																								

Graphic Position Code	91	92	93	94	95	96	97	98	99	9A	9B	9C	9D	9E	9F	A0	A1	A2	A3	A4	A5	A6	A7	A8
Graphic																			¬	'	&			

Graphic Position Code	A9	AA	AB	AC	AD	AE	AF	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	BA	BB	BC	BD	BE	BF	C0
Graphic																								

Graphic Position Code	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF	D0	D1	D2	D3	D4	D5	D6	D7	D8
Graphic	1	2	3	4	5	6	7	8	9	0	X	Y	/	S	T	U	V	W	I	:	%	*	,	=

Graphic Position Code	D9	DA	DB	DC	DD	DE	DF	E0	E1	E2	E3	E4	E5	E6	E7	E8	E9	EA	EB	EC	ED	EE	EF	F0
Graphic	J	K	L	M	N	O	P	Q	R	–	Z	(	A	B	C	D	E	F	G	H	I	+	.	)

Figure 1-88. Printer Translate Table for MCS: QN Arrangement; Count Length F0 (Hex)

da 7000

```
40FF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
00FF FFFF FFFF FFFF FFFF FFD7 8EF0 FF5E
D6FF FFFF FFFF FFFF FFFF FFE3 E4EE 8F90
E2CD FFFF FFFF FFFF FFFF FF2F D860 C0BF
FFFF FFFF FFFF FFFF FFFF 5FCB CCBE 302E
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFE5 E6E7 E8E9 EAEB ECED FFFF FFFF FFFF
FFD9 DADB DCDD DEDF E0E1 FFFF FFFF FFFF
FFFF CECF D0D1 D2D3 D4D5 FFFF FFFF FFFF
CAC1 C2C3 C4C5 C6C7 C8C9 FFFF FFFF FFFF
```

(Not Folded)

da 7000

```
40E5 E6E7 E8E9 EAEB ECED FFD7 8EF0 EF5E
D6D9 DADB DCDD DEDF E0E1 FFE3 E4EE 8F90
E2CD CECF D0D1 D2D3 D4D5 FF2F D860 C0BF
CAC1 C2C3 C4C5 C6C7 C8C9 5FCB CCBE 302E
00E5 E6E7 E8E9 EAEB ECED FFD7 8EF0 EF5E
D6D9 DADB DCDD DEDF E0E1 FFE3 E4EE 8F90
E2CD CECF D0D1 D2D3 D4D5 FF2F D860 C0BF
CAC1 C2C3 C4C5 C6C7 C8C9 5FCB CCBE 302E
00E5 E6E7 E8E9 EAEB ECED FFD7 8EF0 EF5E
D6D9 DADB DCDD DEDF E0E1 FFE3 E4EE 8F90
E2CD CECF D0D1 D2D3 D4D5 FF2F D860 C0BF
CAC1 C2C3 C4C5 C6C7 C8C9 5FCB CCBE 302E
00E5 E6E7 E8E9 EAEB ECED FFD7 8EF0 EF5E
D6D9 DADB DCDD DEDF E0E1 FFE3 E4EE 8F90
E2CD CECF D0D1 D2D3 D4D5 FF2F D860 C0BF
CAC1 C2C3 C4C5 C6C7 C8C9 5FCB CCBE 302E
```

(Folded)

Graphic

Graphic Position Code

01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12
13	14	15	16	17	18												

19	1A	1B	1C	1D	1E	1F	20	21	22	23	24	25	26	27	28	29	2A
2B	2C	2D	2E	2F	30												
			"	,	=												

31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F	40	41	42
43	44	45	46	47	48												

49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	59	5A
5B	5C	5D	5E	5F	60												
			|	:	_												

61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F	70	71	72
73	74	75	76	77	78												

79	7A	7B	7C	7D	7E	7F	80	81	82	83	84	85	86	87	88	89	8A
8B	8C	8D	8E	8F	90												
			<	;	¬												

91	92	93	94	95	96	97	98	99	9A	9B	9C	9D	9E	9F	A0	A1	A2
A3	A4	A5	A6	A7	A8												

A9	AA	AB	AC	AD	AE	AF	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	BA
BB	BC	BD	BE	BF	C0												
			'	?	>												

C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF	D0	D1	D2
1	2	3	4	5	6	7	8	9	0	#	@	/	S	T	U	V	W
D3	D4	D5	D6	D7	D8												
X	Y	Z	&	.	%												

D9	DA	DB	DC	DD	DE	DF	E0	E1	E2	E3	E4	E5	E6	E7	E8	E9	EA
J	K	L	M	N	O	P	Q	R	–	$	*	A	B	C	D	E	F
EB	EC	ED	EE	EF	F0												
G	H	I	)	+	(												

Figure 1-89. Printer Translate Table for MCS: QNC Arrangement; Count Length F0 (Hex)

```
da 7000
40FF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
00FF FFFF FFFF FFFF FFFF FFEF A3E4 EEFF
D3FF FFFF FFFF FFFF FFFF FFD5 D6F0 FFFF
E2CD FFFF FFFF FFFF FFFF FFD7 43FF FFFF
FFFF FFFF FFFF FFFF FFFF FF73 D413 D8FF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFE5 E6E7 E8E9 EAEB ECED FFFF FFFF FFFF
FFD9 DADB DCDD E0E1 FFFF FFFF FFFF FFFF
FFFF CECF D0D1 D2CB CCE3 FFFF FFFF FFFF
CAC1 C2C3 C4C5 C6C7 C8C9 FFFF FFFF FFFF
```

(Not Folded)

```
da 7000
40E5 E6E7 E8E9 EAEB ECED FFEF A3E4 EEFF
D3D9 DADB DCDD DEDF E0E1 FFD5 D6F0 FFFF
E2CD CECF D0D1 D2CB CCE3 FFD7 43FF FFFF
CAC1 C2C3 C4C5 C6C7 C8C9 FF73 D413 D8FF
00E5 E6E7 E8E9 EAEB ECED FFEF A3E4 EEFF
D3D9 DADB DCDD DEDF E0E1 FFD5 D6F0 FFFF
E2CD CECF D0D1 D2CB CCE3 FFD7 43FF FFFF
CAC1 C2C3 C4C5 C6C7 C8C9 FF73 D413 D8FF
00E5 E6E7 E8E9 EAEB ECED FFEF A3E4 EEFF
D3D9 DADB DCDD DEDF E0E1 FFD5 D6F0 FFFF
E2CD CECF D0D1 D2CB CCE3 FFD7 43FF FFFF
CAC1 C2C3 C4C5 C6C7 C8C9 FF73 D413 D8FF
00E5 E6E7 E8E9 EAEB ECED FFEF A3E4 EEFF
D3D9 DADB DCDD DEDF E0E1 FFD5 D6F0 FFFF
E2CD CECF D0D1 D2CB CCE3 FFD7 43FF FFFF
CAC1 C2C3 C4C5 C6C7 C8C9 FF73 D413 D8FF
```

(Folded)

Graphic

Grpahic Position Code

01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18

19	1A	1B	1C	1D	1E	1F	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30

31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F	40	41	42	43	44	45	46	47	48
																		%					

49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F	60

61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F	70	71	72	73	74	75	76	77	78
																		#					

79	7A	7B	7C	7D	7E	7F	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F	90

91	92	93	94	95	96	97	98	99	9A	9B	9C	9D	9E	9F	A0	A1	A2	A3	A4	A5	A6	A7	A8
																		¤					

A9	AA	AB	AC	AD	AE	AF	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	BA	BB	BC	BD	BE	BF	C0

C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF	D0	D1	D2	D3	D4	D5	D6	D7	D8
1	2	3	4	5	6	7	8	9	0	X	Y	/	S	T	U	V	W	&	@	$	*	,	=

D9	DA	DB	DC	DD	DE	DF	E0	E1	E2	E3	E4	E5	E6	E7	E8	E9	EA	EB	EC	ED	EE	EF	F0
J	K	L	M	N	O	P	Q	R	–	Z	(	A	B	C	D	E	F	G	H	I	+	.	)

Figure 1-90. Printer Translate Table for MCS: RN Arrangement; Count Length F0 (Hex)

```
da 7000
40FF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
00FF FFFF FFFF FFFF FFFF EEA8 F0E7 CAEA
A7FF FFFF FFFF FFFF FFFF ECB3 B4E8 EDFF
BEA9 FFFF FFFF FFFF FFFF FFB2 EFFF FFEB
FFFF FFFF FFFF FFFF FFFF C0FF E5E6 FFBF
FFCB CCCD CECF D0D1 D2D3 FFFF FFFF FFFF
FFD4 D5D6 D7D8 D9DA DBDC FFFF FFFF FFFF
FFFF DDDE DEF0 E1E2 E3E4 FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFE9
FFC1 C2C3 C4C5 C6C7 C8C9 FFFF FFFF FFFF
FFB5 B6B7 B8B9 BABB BCBD FFFF FFFF FFFF
FFFF AAAB ACAD AEAF B0B1 FFFF FFFF FFFF
A69D 9E9F A0A1 A2A3 A4A5 FFFF FFFF FFFF
```

Graphic

Graphic Position Code

01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18

19	1A	1B	1C	1D	1E	1F	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30

31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F	40	41	42	43	44	45	46	47	48

49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F	60

61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F	70	71	72	73	74	75	76	77	78

79	7A	7B	7C	7D	7E	7F	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F	90

91	92	93	94	95	96	97	98	991	9A	9B	9C	9D	9E	9F	A0	A1	A2	A3	A4	A5	A6	A7	A8
												1	2	3	4	5	6	7	8	9	0	&	.

A9	AA	AB	AC	AD	AE	AF	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	BA	BB	BC	BD	BE	BF	C0
/	S	T	U	V	W	X	Y	Z	,	$	*	J	K	L	M	N	O	P	Q	R	–	″	:

C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF	D0	D1	D2	D3	D4	D5	D6	D7	D8
A	B	C	D	D	F	G	H	I	+	a	b	c	d	e	f	g	h	i	j	k	l	m	n

D9	DA	DB	DC	DD	DE	DF	E0	E1	E2	E3	E4	E5	E6	E7	E8	E9	EA	EB	EC	ED	EE	EF	F0
o	p	q	r	s	t	u	v	w	x	y	z	@	'	(	)	–	!	?	!	;	¢	%	¤

Figure 1-91. Printer Translate Table for MCS: SN Arrangement; Count Length F0 (Hex)

```
da 7000
20FF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
00FF FFFF FFFF FFFF FFFF 6B0C 6863 2E78
18FF FFFF FFFF FFFF FFFF 4E4F 5064 4C62
220D FFFF FFFF FFFF FFFF FF16 5176 674B
FFFF FFFF FFFF FFFF FFFF 2417 494A 0B23
FF2F 3031 3233 3435 3637 FF70 695F 5E66
FF38 393A 3B3C 3D3E 3F40 FF6F 5260 4D6C
5D61 4142 4344 4546 4748 FF71 736D 6A75
5C53 5455 5657 5859 5A5B FF72 746E 6577
FF25 2627 2829 2A2B 2C2D FFFF FFFF FFFF
FF19 1A1B 1C1D 1E1F 2021 FFFF FFFF FFFF
FFFF 0E0F 1011 1213 1415 FFFF FFFF FFFF
0A01 0203 0405 0607 0809 FFFF FFFF FFFF
```

Graphic

Graphic Position Code

01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18
1	2	3	4	5	6	7	8	9	0	=	.	/	S	T	U	V	W	X	Y	Z	,	#	&

19	1A	1B	1C	1D	1E	1F	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30
J	K	L	M	N	O	P	Q	R	–	″	:	A	B	C	D	E	F	G	H	I	+	a	b

31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F	40	41	42	43	44	45	46	47	48
c	d	e	f	g	h	i	j	k	l	m	n	o	p	q	r	s	t	u	v	w	x	y	z

49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F	60
@	'	?	;	±	!	$	*	%	¤	1	2	3	4	5	6	7	8	9	0	–	+	(	)

61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F	70	71	72	73	74	75	76	77	78
°	¬	(	)	≠	+	>	<	≤	≥	¢	■	[	]	}	{	└	┘	┌	┐	•	_	–	|

Figure 1-92. Printer Translate Table for MCS: TN Arrangement; Count Length 78 (Hex)

```
da 7000
02FF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
00FF FFFF FFFF FFFF FFFF FF0C FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FF21 20FF FFFF
FFFF FFFF FFFF FFFF FFFF FF0B FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FF0D 0E0F 1011 1213 1415 FFFF FFFF FFFF
FF17 1819 1A1B 1C1D 1E1F FFFF FFFF FFFF
FFFF 2223 2425 2627 2816 FFFF FFFF FFFF
0A01 0203 0405 0607 0809 FFFF FFFF FFFF
```

(Not Folded)

```
da 7000
020D 0E0F 1011 1213 1415 FF0C FFFF FFFF
FF17 1819 1A1B 1C1D 1E1F FF21 20FF FFFF
FFFF 2223 2425 2627 2816 FF0B FFFF FFFF
0A01 0203 0405 0607 0809 FFFF FFFF FFFF
000D 0E0F 1011 1213 1415 FF0C FFFF FFFF
FF17 1819 1A1B 1C1D 1E1F FF21 20FF FFFF
FFFF 2223 2425 2627 2816 FF0B FFFF FFFF
0A01 0203 0405 0607 0809 FFFF FFFF FFFF
000D 0E0F 1011 1213 1415 FF0C FFFF FFFF
FF17 1819 1A1B 1C1D 1E1F FF21 20FF FFFF
FFFF 2223 2425 2627 2816 FF0B FFFF FFFF
0A01 0203 0405 0607 0809 FFFF FFFF FFFF
000D 0E0F 1011 1213 1415 FF0C FFFF FFFF
FF17 1819 1A1B 1C1D 1E1F FF21 20FF FFFF
FFFF 2223 2425 2627 2816 FF0B FFFF FFFF
0A01 0203 0405 0607 0809 FFFF FFFF FFFF
```

(Folded)

Graphic Position Code	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18
Graphic	1	2	3	4	5	6	7	8	9	0	,	.	A	B	C	D	E	F	G	H	I	Z	K	K

Graphic Position Code	19	1A	1B	1C	1D	1E	1F	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30
Graphic	L	M	N	O	P	Q	R	*	$	S	T	U	V	W	X	Y								

Figure 1-93. Printer Translate Table for MCS: XN Arrangement; Count Length 28 (Hex)

```
da 7000
20FF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
00FF FFFF FFFF FFFF FFFF FF78 FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FF51 76FF FFFF
50FF FFFF FFFF FFFF FFFF FF77 FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FF4F FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FF5E 5F60 6162 6364 6566 FFFF FFFF FFFF
FF67 6869 6A6B 6C6D 6E6F FFFF FFFF FFFF
FFFF 5C5D 7071 7273 7475 FFFF FFFF FFFF
5B52 5354 5556 5758 595A FFFF FFFF FFFF
```

(Not Folded)

```
da 7000
205E 5F60 6162 6364 6566 FF78 FFFF FFFF
FF67 6869 6A6B 6C6D 6E6F FF51 76FF FFFF
50FF 5C5D 7071 7273 7475 FF77 FFFF FFFF
5B52 5354 5556 5758 595A FF4F FFFF FFFF
005E 5F60 6162 6364 6566 FF78 FFFF FFFF
FF67 6869 6A6B 6C6D 6E6F FF51 76FF FFFF
50FF 5C5D 7071 7273 7475 FF77 FFFF FFFF
5B52 5354 5556 5758 595A FF4F FFFF FFFF
005E 5F60 6162 6364 6566 FF78 FFFF FFFF
FF67 6869 6A6B 6C6D 6E6F FF51 76FF FFFF
50FF 5C5D 7071 7273 7475 FF77 FFFF FFFF
5B52 5354 5556 5758 595A FF4F FFFF FFFF
005E 5F60 6162 6364 6566 FF78 FFFF FFFF
FF67 6869 6A6B 6C6D 6E6F FF51 76FF FFFF
50FF 5C5D 7071 7273 7475 FF77 FFFF FFFF
5B52 5354 5556 5758 595A FF4F FFFF FFFF
```

(Folded)

Graphic

Graphic Position Code

01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18

19	1A	1B	1C	1D	1E	1F	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30

31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F	40	41	42	43	44	45	46	47	48

49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F	60
						#	—	$	1	2	3	4	5	6	7	8	9	0	S	T	A	B	C

61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F	70	71	72	73	74	75	76	77	78
D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	U	V	W	X	Y	Z	*	,	.

Figure 1-94. Printer Translate Table for MCS: YN Arrangement; Count Length 78 (Hex)

Chnl Status	Flags & OP	Unit Status	Unit Sense	Residual Count		Next CCW Address	
C8	C9	CA	CB	CC	CD	CE	CF

Chnl Status (C8):
0 – Secondary Bit
1 – Incorrect Length
2 – Program Check
3 – Protection Check
4 – Channel Data Check
5 – Channel Control Check
6 – Interface Check
7 – Int. In Int Buffer Bit

Flags & OP (C9):
0 – Chain-Data (CD) Flag
1 – Chain-Command (CC) Flag
2 – Suppress-Length-Indication (SLI) Flag
3 – Skip Flag
4 – Program-controlled-Interruption (PCI) Flag
5 – Active Bit
6 – Input
7 – Output

Unit Status (CA):
0 –
1 – } Not Used
2 –
3 – Busy
4 – Channel End
5 – Device End
6 – Unit Check
7 – Unit Exception (Channel 12)

Unit Sense (CB):
0 – Command Reject
1 – Intervention Required
2 – Not Used
3 – Equipment Check
4 – Data Check
5 – Block Data Check } **
6 – Gate Load } **
7 – Channel-9

** Not Sense Bits - these are stored here but stripped before a sense byte is presented to the channel.

Figure 1-95. 1403 UCW Format

1.15 2311/DAC (FIGURES 1-96 THROUGH 1-118)

	COMMAND	HEX VALUE	M/T ON	GO	OP REGISTER LATCHES SET FOR EACH COMMAND: M/T	SEARCH HI	SEARCH EQ	COUNT	KEY	DATA	READ	WRITE
					CMD BYTE POSITION							
					0	1	2	3	4	5	6	7
CONTROL	SEEK	07			T					X	X	X
	CYL SEEK	0B			U				X		X	X
	HEAD SEEK	1B			R			X	X		X	X
	RECALIBRATE	13			N			X			X	X
	NO OP	03			E						X	X
	SET FILE MASK	1F			D			X	X	X	X	X
	SPACE COUNT	0F		**					X	X	X	X
	RESTORE (NO-OP)	17			O			X		X	X	X
	TEST I/O	00			N							
	SENSE I/O	04								X		
READ	RD DATA	06	86	X	F O					X	X	
	RD KEY-DATA	0E	8E	X	R				X	X	X	
	RD C-K-D	1E	9E	X				X	X	X	X	
	RD HA	1A	9A	X	M/T			X	X		X	
	RD R0	16	96	X				X		X	X	
	RD COUNT	12	92	X				X			X	
	RD (IPL)	02	82	X	R						X	
WRITE	WR DATA	05		X	E					X		X
	WR KEY = DATA	0D		X	A				X	X		X
	WR C-K-D	1D		X	D			X	X	X		X
	WR HA	19		X				X	X			X
	WR R0	15		X	O			X		X		X
	ERASE	11		X	R			X				X
SEARCH	SCH ID EQ	31	B1	X	S		X	X				X
	SCH ID HI	51	D1	X	E	X		X				X
	SCH ID EQ OR HI	71	F1	X	A	X	X	X				X
	SCH KEY EQ	29	A9	X	R		X		X			X
	SCH KEY HI	49	C9	X	C	X			X			X
	SCH KEY EQ OR HI	69	E9	X	H	X	X		X			X
	SCH HA EQ	39	B9	X	C		X	X	X			X
	*SCH K-D EQ	2D	AD	X	M		X		X	X		X
	*SCH K-D HI	4D	CD	X	D	X			X	X		X
	*SCH K-D EQ OR HI	6D	ED	X	S.	X	X		X	X		X

* File Scan Commands

** Go Issued unless Space Count is the First Command of a Chain

Go Issued to DAC for Indicated Cmds.

Figure 1-96. Integrated File Commands

TIC Command Code		
Decimal	Hexadecimal	Binary
X8	X8	XXXX1000
Positions Marked "X" are Ignored		

Figure 1-97. 2311/DAC Operation Code for TIC Command

No-Operation Command Code		
Decimal	Hexadecimal	Binary
03	03	00000011

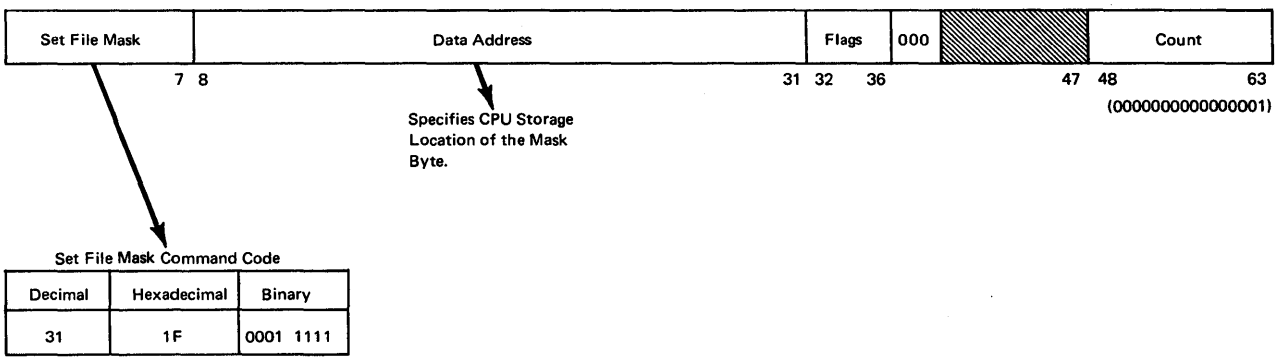
Figure 1-98. 2311/DAC Operation Code for No-Op Command

Recalibrate Command Code		
Decimal	Hexadecimal	Binary
19	13	00010011

Figure 1-99. 2311/DAC Operation Code for Recalibrate Command

Read IPL Command Code		
Decimal	Hexadecimal	Binary
02	02	0000 0010

Figure 1-100. 2311/DAC Read IPL Command Code



Set File Mask Command Code

Decimal	Hexadecimal	Binary
31	1F	0001 1111

B_0	B_1	Permit Write Commands
0	0	All Except Write Home Address and Write Record R_0
0	1	None
1	0	Write Data or Write Key & Data
1	1	All

B_3	B_4	Permit Seek Commands
0	0	All
0	1	Seek Cylinder or Seek Head
1	0	Seek Head
1	1	None

For the 2311, bits 2,5,6 and 7 of the mask must be zero. If these bits are not zero, the mask is considered to be invalid and a unit check signal is generated. A subsequent sense command indicates command reject.

Figure 1-101. 2311/DAC Set File Mask Command

Command	Seek Command Code		
	Decimal	Hexadecimal	Binary
Seek	07	07	00000111
Seek Cylinder	11	0B	00001011
Seek Head	27	1B	00011011

Figure 1-102. 2311/DAC Operation Codes for Seek Commands

	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5
Binary	00000000	00000000	00000000	00000000 to 11001010	00000000	00000000 to 00001001
Hexadecimal Equivalent	00	00	00	00 to CA	00	00 to 09

Figure 1-103. 2311/DAC 6-Byte Seek Commands

Space Count Command Code

Decimal	Hexadecimal	Binary
15	OF	00001111

Figure 1-104. 2311/DAC Operation Code for Space Count Command

Sense I/O Command Code

Decimal	Hexadecimal	Binary
04	04	00000100

Figure 1-105. 2311/DAC Operation Code for Sense Command

Read R0 Command Code		
Decimal	Hexadecimal	Binary
22	16	00010110

Read R0 Command Code Multiple-Track		
Decimal	Hexadecimal	Binary
150	96	10010110

Figure 1-106. 2311/DAC Read Track Descriptor Record (R0) Command Codes

Read HA Command Code		
Decimal	Hexadecimal	Binary
26	1A	00011010

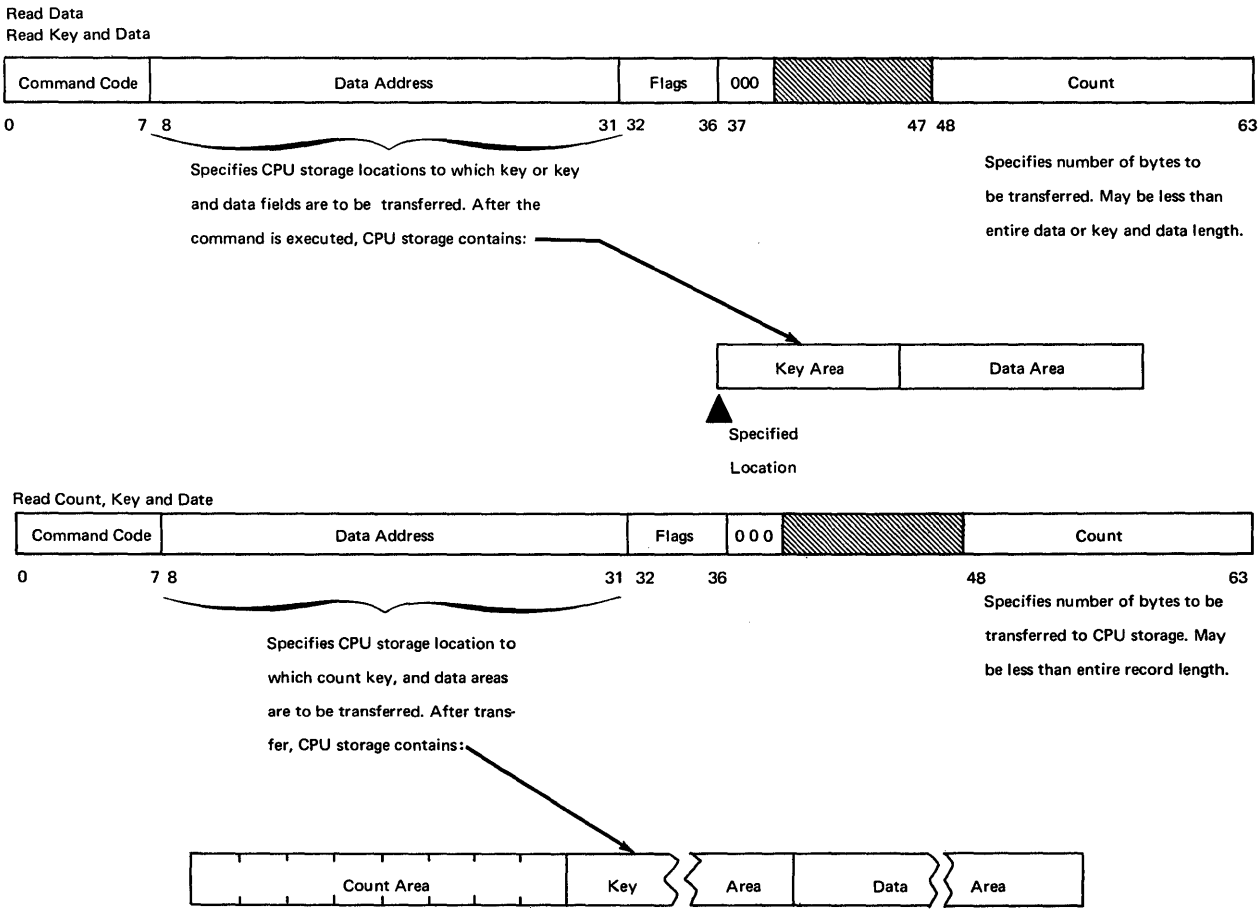
Read HA Command Code Multiple-Track		
Decimal	Hexadecimal	Binary
154	9A	10011010

Figure 1-107. 2311/DAC Read Home Address Command Codes

Read Count Command Code		
Decimal	Hexadecimal	Binary
18	12	00010010

Read Count Command Code, Multiple-Track		
Decimal	Hexadecimal	Binary
146	92	10010010

Figure 1-108. 2311/DAC Read Count Command Codes



Read Data Command Codes

	Decimal	Hexadecimal	Binary
Read Data	06	06	00000110
Read Key & Data	14	0E	00001110
Read Count, Key & Data	30	1E	00011110

Read Data Command Codes, Multiple Track

	Decimal	Hexadecimal	Binary
Read Data	134	86	10000110
Read Key & Date	142	8E	10001110
Read Count, Key & Data	158	9E	10011110

Figure 1-109. 2311-DAC Read Data, Read Key Data, and Read Count Key Data Command Codes

Write Data Command Codes			
	Decimal	Hexadecimal	Binary
Write Data	05	05	00000101
Write Key & Data	13	0D	00001101

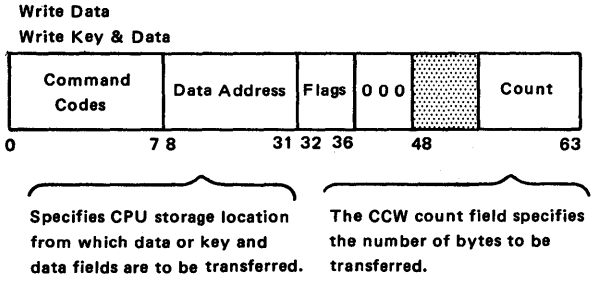
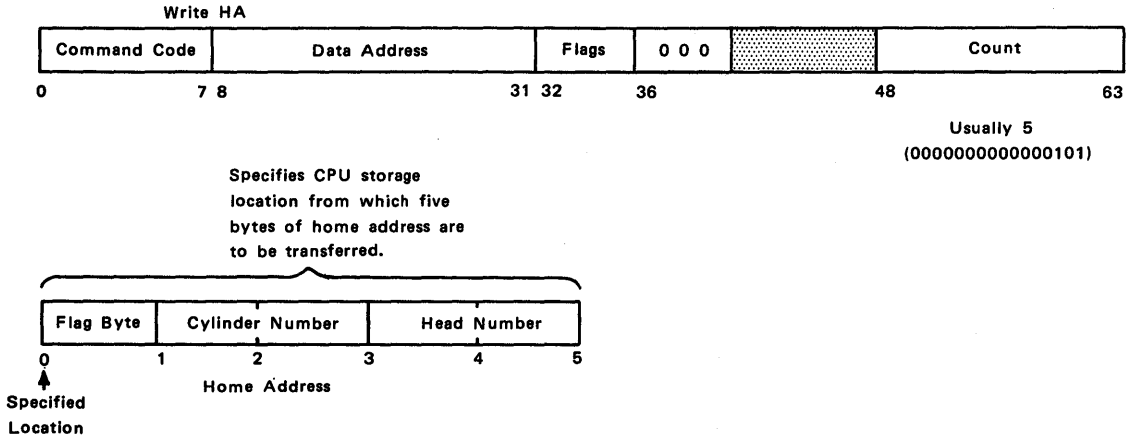


Figure 1-110. 2311/DAC Write Data and Write Key and Data Command Codes



Write Home Address Command		
Decimal	Hexadecimal	Binary
25	19	0001 1001

Figure 1-111. 2311/DAC Write Home Address Command Code

	Sense Byte 0	Sense Byte 1	Sense Byte 2	Sense Byte 3
Bit 0	Command Reject	Data Check in Count Field	Unsafe	Ready
Bit 1	Intervention Required	Track Overrun		On Line
Bit 2		End-of-Cylinder		Unsafe
Bit 3	Equipment Check	Invalid Sequence	Selected Status	
Bit 4	Data Check	No Record Found	Cyclic-Code Check	On Line
Bit 5	Overrun	File Protected	Unselected File Status	End of Cylinder
Bit 6	Track-Condition Check	Missing Address Marker		
Bit 7	Seek Check			Seek Incomplete

Figure 1-112. 2311/DAC Sense Byte Summary

	Search Home Address Equal Command Code		
	Decimal	Hexadecimal	Binary
MT Bit Off	57	39	0011 1001
MT Bit On	185	B9	1011 1001

Figure 1-113. 2311/DAC Operation Codes for Search Home Address Equal Command

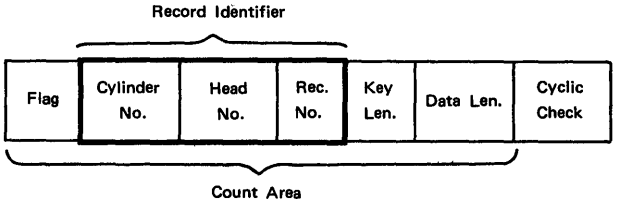


Figure 1-115. 2311/DAC Identifier (ID)

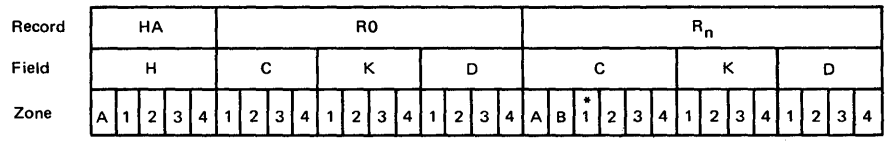
Command	Search ID Command Code		
	Decimal	Hexadecimal	Binary
Search ID Equal	49	31	00110001
Search ID High	81	51	01010001
Search ID Equal or High	113	71	01110001

Command	Search ID Multipule Track Command Code		
	Decimal	Hexadecimal	Binary
Search ID Equal	177	B1	10110001
Search ID High	209	D1	11010001
Search ID Equal or High	241	F1	11110001

Figure 1-114. 2311/DAC Search ID Command Codes

Command	Command Sequence	Initial Field and Zone State	Field and Zone State at End of Command
Read Count, Key and Data	None	C1	D4
Read Key and Data	None	C1	D4
	After Search ID	C4	D4
Read Data	None	C1	D4
	After Search ID	C4	D4
	After Search Key	K4	D4
Write Count, Key and Data	Search Equal ID	C4	D4
	Search Equal Key	K4	D4
	Write R0	D4	D4
	Write Count, Key and Data	D4	D4
Write Key and Data	Search Equal ID	C4	D4
Write Data	Search Equal ID	C4	D4
	Search Equal Key	K4	D4
Search ID	None	C1	C4
Search Key	None	C1	K4
	After Read or Search ID	C4	K4
Search Key and Data	None	C1	D4
	After Read or Search ID	C4	D4
Search Home Address	None	HA	H4
Read R0	None	HA	D4
	After Read or Search Home Address	H4	D4
Write R0	Write Home Address	H4	D4
	Search Equal Home Address	H4	D4
Read Home Address	None	HA	H4
Write Home Address	None	HA	H4
Read Initial Program Load	None	C1	D4
Read Count	None	C1	C4
Erase	Search Equal ID	C4	D4
	Search Equal Key	K4	D4
	Write R0	D4	D4
	Write Count, Key and Data	D4	D4
No Operation	None	Reset Condition	

Figure 1-116. 2311/DAC Track Orientation Field and Zone State Summary

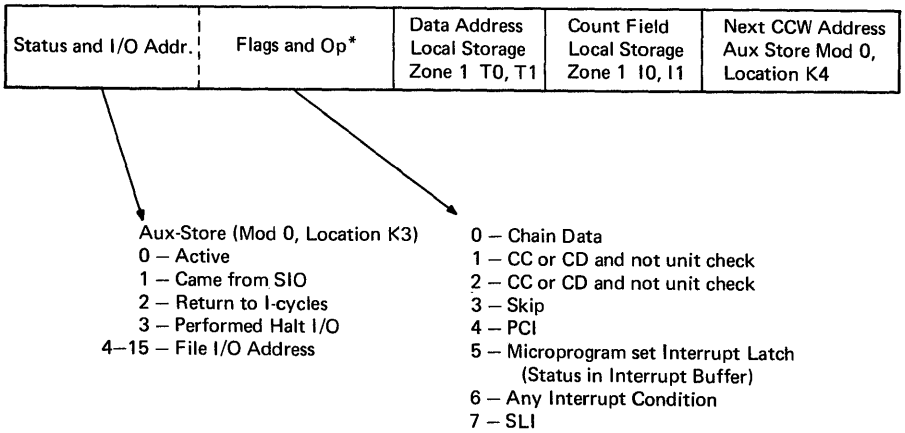


Field	Definition
H	Home-address area (including gaps)
C	Count area (including gaps)
K	Key area (including gaps)
D	Data area (including gaps)

Zone	Definition
1	Pre-record gap (including address marker)
2	Record
3	Cyclic code
4	Post-record gap
A	Constant gap of 12-ones bytes in the count field, or 28 all-zeros bytes in the home-address field.
B	The 4.9% variable gap between records.

Notes: The index point immediately precedes the home-address area.
* Location of the address marker.

Figure 1-117. 2311/DAC Track Orientation



* Flags - - In file external register D (FFI)
Op - - In file external register F (FOP)

Note: Unlike UCW's for other I/O attachments, the 2311 UCW is stored in Local Storage, External Registers, and Auxiliary Storage.

Figure 1-118. 2311 UCW Format

Section 2. Diagnostic Techniques

This section of the manual describes maintenance concepts, system failure and handling procedures, and maintenance program definitions. The Model 25 Field Engineering Maintenance Diagrams Manual (MDM), Y24-3529, contains detailed analysis routines and should be referred to on other than obvious failures requiring minimal diagnosis.

1.16 MAINTENANCE CONCEPTS

Microdiagnostic programs are designed to reduce CE diagnostic time by taking advantage of the CPU speed and capability for self-diagnosis through the reloadable control storage feature. The programs are intended for use:

1. During unscheduled maintenance
2. During scheduled or deferred maintenance
3. At installation
4. Before and after EC installation.

There are two general types of microdiagnostic programs:

a. Resident
b. Nonresident.

The primary repair strategy for both types of programs is to replace an SLT card or cards shown on a fault list or logged out on the Console Printer-Keyboard (PR-KB).

In addition, looping capabilities are designed into the programs for scoping and other diagnostic procedures.

The entire strategy has been condensed into diagnostic technique flow diagrams for easy use by the CE and is included in the Model 25 Maintenance Diagram Manual. On other than obvious failures requiring minimal diagnosis, the CE should refer to the diagrams and execute the appropriate section or sections of these programs.

Where the cause of failure cannot be located by microdiagnostic programs (such as in a channel attached I/O device) DMA4 and the associated diagnostic programs already in existence will be used by the CE. The Model 25 macrodiagnostic package is as follows.

3020 DMA4 Diagnostic Monitor
310A Message Editor
E108 DMA4 Expansion Section
338F Meter Test
34E1 Direct Control
FFF0 Disk Initializer
3FE1 SEREP
F0FE Disk Utility
3FCZ Syt-25/30
F061 FRIEND
C675-C67A File Function
C678- File Scan
C67C,C67D 2311 Diagnostic Text

All other monitor-controlled macrodiagnostics presently released for I/O devices that can be attached to the Model 25 standard interface channel will be functional on the Model 25. These decks and documentation will be shipped from the plant of control for the I/O control unit for device.

Failures not detected by either the micro or macrodiagnostic programs must be located by use of the system environment program SYS-M30-B or possibly the customer problem program.

1.16.1 MALFUNCTION INDICATIONS

a. Customer Problem Program
Malfunctions during execution of the customer problem program are indicated by console lights (see 3.0 System Failure Detection and Handling) and printed logout on the 1052 (see section 1.17.1.2).
Malfunctions detected during execution of resident microdiagnostics cause a stop word or stop loop. These programs are executed automatically during system reset, CSL and IPL.
b. Nonresident Micro/Macro Diagnostic Programs
Malfunctions are indicated as follows.
1. Nonresident/nonmonitor-controlled microprograms cause a stop word or stop loop.
2. Nonresident/monitor-controlled programs provide fault-locating information on the console printer-keyboard.
3. Macroprograms under DMA4 Monitor. Error messages are determined by system configuration and memory size. These messages can be printed on the output printer defined by CE option (1052, 1403, or 1443).
4. System environment (SYS-M30-B) Error message printout is the same as DMA4 monitor.

A successful reset is indicated by:

a. No console check lights.
b. Manual light turns off then on.
c. System light turns on then off.

1.16.2 UNIT IDENTIFICATION

Standard SLT nomenclature applies to the 2025 CPU.

1.16.3 MALFUNCTION ISOLATION

The aim of the Model 25 Diagnostic Program Package (DPP) is to achieve a minimum DUI by high-resolution fault location of an easily replaceable component. The package provides effective malfunction isolation to the two general types of exposure:

A. Logic - malfunction in the basic CPU, integrated I/O attachments, channel, and CPU features.
   Resolution capabilities within the integrated devices are as follows.

2540
1. Hole-count test, read and punch (brush failures),
2. Manual operations, including card transport paths,
3. Stacker select,
4. PFR.

Chnl
1. Check Sel-out wraparound to Sel-in,
2. Test address response,
3. Test I/O; complete initial selection of all possible device addresses, section 1.19.7).
4. Single-cycle routine; command to a particular address and loop.

1403
1. Print coil checking
2. Drum pulse response
3. Hydraulic speed
4. Carriage brushes/emitter/ mechanics
5. Hammer fire,
6. Print quality.

1052
1. Manual intervention section: Function of all keys, End-of-forms contact, Capability of repeatedly printing any key.
2. Dynamic section: Ability to print characters for all tilt/rotate combinations,

   End-of-forms contact.

B. 2311 - Resolution is provided by macrodiagnostics.

   Hard Core - for malfunctions that would prevent basic CPU functions necessary for execution of resident diagnostics, the following strategy will be used.
   1. Power, clock, etc.
      Normal CE repair procedures will be applied using console capabilities, power diagnostic techniques diagram in the maintenance diagram manual, etc.
   2. Memory
      A memory diagnostic techniques diagram for diagnosis and repair is provided in the maintenance diagram manual. The capabilities designed into the Model 25 such as SCAN STOR, TEST PATTERN, etc. are used in this strategy.
         A nonresident memory microdiagnostic is also provided for CPU with two memory modules.

The recommended sequence for executing the DPP as outlined in the Maintenance Diagrams Manual provides for a building block approach to locating the failure. Each program basically builds on the successful execution of the previous lower level program.

1.16.4 REPAIR

Repair will generally consist of replacing the failing component (usually an SLT card) from on site or branch office stock.

1.16.5 REPAIR VERIFICATION

The micro- or macro-program where the failure was diagnosed should be reexecuted after the repair. Successful execution will be considered a justification for returning to the customer problem-program.

1.16.6 INTERMITTENT MALFUNCTION

Intermittent failures as seen by the customer can take one of two forms:
1. The failure is actually a solid hardware defect, but appears intermittent because that area of the logic is called on only to function occasionally.
   Microdiagnostic programs will be effective to a high degree on this type of failure because by design, they are capable of checking the majority of CPU and integrated I/O attachment logic.
2. The failure is intermittent due to a degraded or marginal component.
   The looping capabilities designed into the microdiagnostic programs will

attack this type of failure effectively by exercising the logic until a pattern can be established.

Other diagnostic capabilities that will also impact intermittent failures are CE Trap (See section 1.18.7) and 1052 Logout (See section 1.17.1.3).

1.16.7 PROTECTION OF CONTROL STORAGE, CSL

Module 0 (first 128 control words) will be protected by the resident CSL routine on all core loads.

Alter control storage from the 1052 will not be operative unless the CE key is on.

The enable control-storage store key on the CPU will not be operative unless the CE key is on.

1.17 SYSTEM FAILURE DETECTION AND HANDLING

The objectives of failure detection and handling procedures for the Model 25 are to provide:

a. Assurance to the customer that the system is functionally operational.
b. Sufficient indication and information to enable the CE to locate the failure rapidly and accurately.

A version of the SEREP program is also provided.

1.17.1 ERROR HANDLING

The Model 25 will come to a hard stop on second error, a second malfunction which occurs before the first malfunction has caused a machine-check interrupt to be taken (Figure 1-119).

There are no special provisions on the Model 25 for continued operation in the presence of a solid malfunction.

Error restart capabilities for such intermittent I/O failures as data checks, punch checks, etc. are provided by the operating system used by the customer.

Nonhardware-caused troubles (jams, failures, etc.) are normally not expected to result in a customer-reported call. The Model 25 Functional Characteristics Manual, Form A24-3510, provides restart procedures for these situations; also consult the index in this manual for the specific area of interest.

1.17.1.1 Machine-Check and Channel Control Check

Any of the following machine-check conditions (if the M-bit of the PSW is on), will cause the corresponding bit to be set in the error register (MC) and initiate the machine-check trap routine:

0 File Control Check
1 Storage Protect Check
2 Storage Address Check
3 Control Word Parity Check
4 Storage Data Parity Check
5 ALU Error Latch
6 A-Reg Parity Check
7 B-Reg Parity Check

The machine-check trap routine stores the following information into program storage starting at hex location 80.

80 - Trap priority register (MMSK)
81 - Branch condition register (BA)
82 - Machine-check register (MC)
83 - Error count*
84-85 - Backup address (address of the microword)
86-87 - Unused

*Bits 1-2 of byte 83 contain the logout code: 00 for machine check or channel control check; or 11 for interface control check.

If none of the 0 through 6 bits of the MMSK register is on (indication that an I/O trap is not in process), the logout area above is printed on the console printer. The machine-check interrupt will then take place.

If an I/O trap is in process (any of the 0 through 6 bits of MMSK register on) when a machine-check trap occurs, the I/O operation involved will be terminated and then the I/O interrupt will take place. The logout area will be printed on the console printer-keyboard before any CPU instructions are executed.

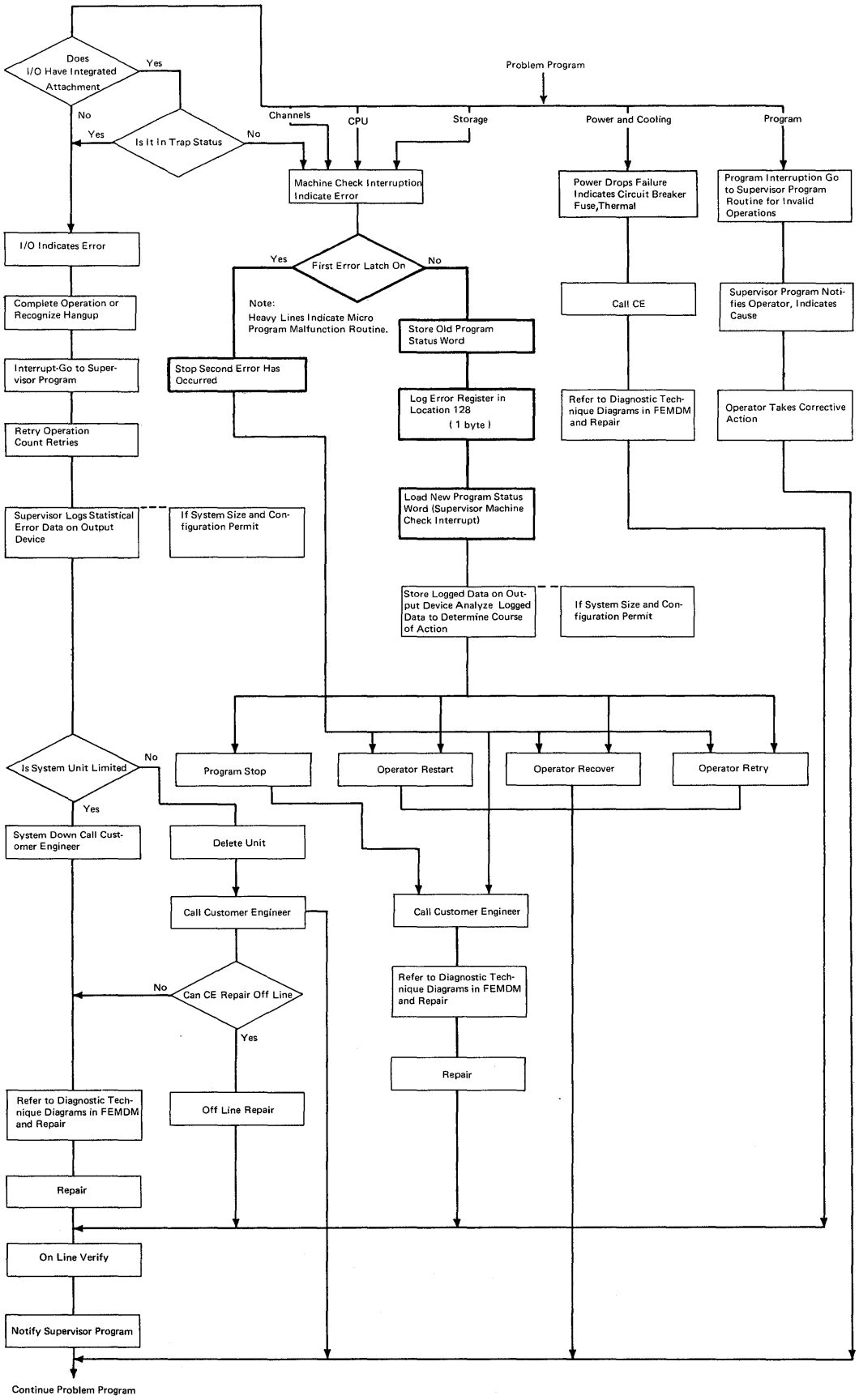


Figure 1-119. Maintenance Approach

1.17.1.2 Interface Control Check

When an interface control check is detected on either the multiplexer or selector channel, the following information is stored in program-storage locations 80-87 (hex).

80 Trap priority register (MMSK)
81 Branch conditions register (BA)
82 Channel branch conditions register (GS)
83 Error count*
84 Channel branch conditions register (GT)
85 Channel diagnostic register (GD)
86 Code byte

Burst Channel
01XYYYYZ
X=1 if time out
Z=1 if status trap or chained to CCW.
YYYYY=time out counter bits

Byte Channel
001XMMMZ
X&Z=same as burst channel
M=Misc. use

87 Device address

*Bits 1-2 of byte 83 contain the logout code: 00 for machine check or channel control check, or 11 for interface control check.

1.17.1.3 1052 Logout

The 1052 logout is a microprogram-supported function that prints out information contained in the diagnostic logout area of program storage, (locations 80-87, hexadecimal). Existing problem programs are not affected by this logout provided they do not use this area. The format and contents of the diagnostic logout area are machine dependent. A version of SEREP that acts on this information is available for use on the Model 25.

In general, the function of such macroprograms is provided by the 1052 logout microprogram. Subsequent to execution of the 1052 logout microprogram, a System/360 machine-check or I/O interrupt is initiated. Existing restart procedures and problem programs that do not act directly on the diagnostic logout area (such as BPS, DOS, OBR/SDR, etc.) are applicable to the Model 25 within the limits of storage size.

The program-storage byte locations and contents of the diagnostic scanout area are given in section 1.17.1.1.

1.17.2 CPU HARDWARE CHECKS

The setting of the check control switch determines the action taken when a CPU hardware check occurs (see section 1.18).

Checking is provided at the following points; an indicator for the conditions is located on the system control panel:

1. A-Register Parity Check
   B-Register Parity Check
   These checks are not always activated because some external registers are set and reset by bit and do not carry parity. In the case of a byte gated to A or B without parity, the check is disabled. Local-storage data is always checked.

2. Storage Address Parity Check
   A parity check is made on all addresses used to access main storage except on the address after a Branch on Mask word.

3. Storage Data Bus-Out Parity Check

   This check is made on all data requested from storage. A control-word check occurs on all machine cycles except during the second cycle of a storage word. A storage data check may occur during the second cycle of a storage control word.

4. ALU Check
   Parallel logic is used in the ALU to detect an error between the A and B parity checks and the ALU output.
   Each bit position of ALU (including +6 circuit, complementor and decimal corrector) has two outputs. One output goes to the local store assembler and the system mask register; this output is displayed by the indicators. The other output goes to the Z=0 test. Both outputs go to the parity generator and the ALU check (2-wire check) circuit.

5. Storage Protect Check
   This is a parity check on the data out of the storage-protect buffer (STP1).

1.17.3 CPU MICROPROGRAM CHECKS

There are some cases during machine operation when a hardware failure that is not detected by hardware checks could occur. In these cases, the microprogram can reach a state from which it must not continue: the microprogram branches to a stop word. The listings will describe the reason for reaching the stop word.

Stop words in Model 25 mode are limited to the system reset diagnostic (BDIA), IPL

routines, and unused control-storage locations.

1.17.4 CPU ATTACHMENT CHECKS

This section describes some capabilities for handling check conditions occurring within the integrated I/O attachment devices. For further information, consult the index in this manual for the specific area of interest.

1.17.4.1 2540 Attachment Checks

1. Overrun--This check occurs when all ten traps that must be completed during each row have not occurred by the time the next row is ready to be read. Priority circuitry ensures that overrun will not occur unless there is a hardware failure.
2. Sync Check--This check ensures that the shift registers receiving data from the 1540 are in synchronism with each other.
3. Address Check--This check is on the address sent to the 2540 for each bit. It checks for a 2/5 code, and for an address greater than or equal to 90.

Each of these checks will give a unit check to the status byte, with equipment check in the sense information. Hardware checks in the 2540 unit will give the same status and sense information to the program as the 2821. The microprogram interrogates the attachment hardware checks; the 2540 unit checks combines this with the information it may detect itself and places the result in the proper sense bits. The microprogram forms the status and sense information.

1.17.4.2 1403 Attachment Checks

1. Hammer Check--Equipment check sense bit. This check is made to determine if each hammer driver that was requested to operate, did operate.
2. Sync Check--Intervention-required sense bit. This check indicates that the chain or train and the printer controls are out of synchronism.
3. Print Buffer Parity Check--Equipment check sense bit. This check is for correct parity on data read from the print buffer while printing a line or when receiving data from the CPU.

The 1403 microprogram interrogates the hardware check information and sets the proper sense and status information. The microprogram also checks information for printability when loading the buffer, and signals data check for unprintable characters. This depends on the information loaded at CSL time into the module of auxiliary storage used as the print translator, or loaded by the UCS utility program UT048. The 1052 (PR-KB) printouts of the printer area of auxiliary storage are shown in Section 1.14.

1.17.4.3 1052 Attachment Checks

The 1052 hardware checks the keyboard data for proper parity. The microprogram detection of a parity error would cause unit-check status and the equipment check sense bit to be set.

1.17.4.4 2311 Attachment Checks

1. Data check--unit-check status--data check sense. This check occurs when data read from the file does not generate the proper check character.
2. Overrun--unit-check status--overrun sense. This check occurs when the attachment requires service from the CPU and does not receive it soon enough to keep from losing data or causing improper operation.

The 2311 attachment microprogram checks the hardware signals from the 2311 for errors detected in the unit, interrogates the attachment checks and sets the appropriate status and sense information.

1.17.4.5 Channel Checks

1. Incorrect Length Check--occurs when the number of bytes contained in the storage areas assigned for the I/O operation is not equal to the number of bytes requested or offered by the I/O device.
2. Program Check--occurs when programming errors are detected by the channel.
3. Protection Check--occurs when the channel attempts to place data in a portion of main storage that is protected for the current operation on the subchannel; or, the protection key associated with the I/O operation does not match the key of the addressed main-storage location, and the protection key is not zero.
4. Channel Data Check--indicates that the channel has detected a parity error in the information transferred to or from main storage during an I/O operation.
5. Channel Control Check--caused by any machine malfunction affecting channel controls. This includes parity errors on CCW and data addresses and parity errors on the contents of the CCW. (Logout is initiated.)
6. Interface Control Check--caused by an invalid signal on the I/O interface. The condition is detected by the channel and usually indicates malfunctioning of an I/O device. (Logout is initiated.)

The channel microprogram is the path through which all status bytes are set in the CSW. Accesses for sense information are through the same path as for a read operation to the desired unit.

1.17.5 SYSTEM CHECKS

1.17.5.1 Power Check

If any of the dc supplies (except +24V control voltage) falls below its sensed output level, if a circuit breaker trips, or if a thermal trip occurs, the machine sequences down to its normal power-off status and the power-check light turns on.

A power-on sequence cannot occur until the power-check light is reset by pressing the power-off key, and by correcting and resetting the condition that caused the power-off sequence.

1.17.5.2 Low Temperature

This light turns on when a temperature below 96±5 degrees is detected at the main storage array. When power is turned on initially, this light comes on and remains on until the array is at proper operating temperature (about two minutes.).

1.17.6 STATUS BYTES

Because the integrated attachments present the same status information as did the corresponding System/360 control units, the Model 25 does not introduce any new status byte definitions. The only exception is chaining check (bit 47) which is not used on the Model 25.

1.17.7 EXTERNAL BRANCH CONDITIONS

The following sections define the external facility bytes for the Model 25 diagnostic microprograms.

1.17.7.1 Integrated Disk Attachment

CHI--COUNTER HIGH IN (for diagnostic analysis)

0	Ctr	Pos	32,768
1	Ctr	Pos	16,384
2	Ctr	Pos	8,192
3	Ctr	Pos	4,096
4	Ctr	Pos	2,048
5	Ctr	Pos	1,024
6	Ctr	Pos	512
7	Ctr	Pos	256

CLI--COUNTER LOW IN (for diagnostic analysis)

0	Ctr	Pos	128
1	Ctr	Pos	64
2	Ctr	Pos	32
3	Ctr	Pos	16
4	Ctr	Pos	8
5	Ctr	Pos	4
6	Ctr	Pos	2
7	Ctr	Pos	1

SDI--SERIALIZER/DESERIALIZER IN (for diagnostic analysis and comparing of home address by Model 25 microprogram)

0	Read Buffer	128
1	Read Buffer	128
2	Read Buffer	64
3	Read Buffer	32
4	Read Buffer	16
4	Read Buffer	8
5	Read Buffer	4
6	Read Buffer	2
7	Read Buffer	1

FOB--FILE-OUT BUS (for diagnostic analysis)

	Ctrl Tag	Set Cyl Tag	Set Head Tag	Set Diff Tag
0	Write Gate	128	Forward	Not 128
1	Read Gate	64	Not Used	Not 64
2	Seek Start	32	Not Used	Not 32
3	Reset Head	16	Not Used	Not 16
4	Erase Gate	8	Head 8	Not 8
5	Select Head	4	Head 4	Not 4
6	Return to 000	2	Head 1	Not 2
7	Head Advance	1	Head 1	Not 1

DS--Disk Status When Gated with Diagnostic Controls

	Gate Diag Addr0
0	WR BUF 128
1	WR BUF 64
2	WR BUF 32
3	WR BUF 16
4	WR BUF 8
5	WR BUF 4
6	WR BUF 2
7	WR BUF 1

	Gate Diag Addr1
0	Test Unit Exec
1	RD Op
2	Erase Op
3	Scan Op
4	Space Count Op
5	HA Op
6	HA or R0 Op
7	Count Op

Gate Diag Addr2
0 Key Op
1 Data Op
2 R0 Op
3 Count or Key or Data Op
4 Count or Key Op
5 WR CKD Op
6 Standard Index
7 Bit Ring Inhibit

Gate Diag Addr3
0 Cyc Code Pos 1
1 Cyc Code Pos 16
2 Cyc Code Pos 17
3 CC Error
4 Unequal Compare
5 Bit Ring 7
6 Write Clock Bit
7 Write Data Bit

Gate Diag Addr4
0 Zone A
1 Zone B
2 Zone 1
3 Zone 2
4 Zone 3
5 Zone 4
6 HA Field
7 Count Field

Gate Diag Addr5
0 Key Field
1 Data Field
2 Flag Bit 0
3 Flag Bit 6
4 Flag Bit 7
5 Counter Decode 0
6 Counter Decode 1
7 Counter Decode 2

Gate Diag Addr6
0 Counter Decode 3
1 Counter Decode 4
2 Counter Decode 5
3 Counter Decode 6
4 Counter Decode 7
5 Counter Decode 8
6 Counter Decode 9
7 Counter = 000

1.17.7.2 Integrated 2540 Attachment

RPD=K (CS Decode)
0 R/P Diagnostic Latch
1 R/P Diagnostic Singleshot
2 R/P Diagnostic Single Cycle
3 R/P Reset Shift Register
4 R/P Diagnostic Attachment Reset
5 Unused
6 Unused
7 Unused

RPD1--R/P Diag. Cond 1
0-4 R/P Tens AR A-E
5 Punch Addr Check
6 Punch Overrun Latch
7 Punch Sync Check Latch

RPD2--R/P Diag. Cond. 2
0-4 R/P Units AR A-E
5 Reader Address Check
6 Reader Overrun Latch
7 Reader Sync Check Latch

1.17.7.3 Integrated 1403 Attachment

PRD--Diagnostic Conditions
Diagnostic Decode 1
0 PCC TR 128
1 PCC TR 64
2 PCC TR 32
3 PCC TR 16
4 PCC TR 8
5 PCC TR 4
6 PCC TR 2
7 PCC TR 1

Diagnostic Decode 2
0 Print Control
1 Print Scan
2 PSS Gate
3 Home Gate
4 SS3 TR
5 Print Compare
6 Last Scan
7 Sync Check Latch

Diagnostic Decode 3
0 Carriage Busy
1 Space Drive
2 Skip Drive
3 Carriage Settling
4 Carriage Brush Reg 8
5 Carriage Brush Reg 4
6 Carriage Brush Reg 2
7 Carriage Brush Reg 1

Diagnostic Decode 4
0 PIC
1 PLB C1
2 PIB C2
3 PLB C3
4 MCS Mode
5 Addr HD off
6 E1 Emitter
7 Channel 1 Latch

1.17.7.4 Multiplexer or Selector Channel

GA--Channel Conditions Register
0 Selective Reset
1 Selective Out
2 Address Out
3 Command Out
4 Initial Selection
5 Select Out
6 Channel Reset (diagnostic)
7 Spare

GB--Channel Conditions Register
0 Data Chain Latch
1 Channel Identification Latch
2 Burst Latch
3 Set Buffered Device Latch or Reset Channel Parity-Error Latch
4 Channel Diagnostic Latch
5 Channel-1 Interruption Latch
6 Spare
7 Suppress Cut Control Latch

GD--Channel Diagnostic Register
0 Operational Cut
1 Service Cut
2 Address Cut
3 Command Out
4 0
5 Select Out
6 0
7 Suppress Out

GS--Channel Branch Conditions
0 Data Chain Request Latch
1 Buffered Device Latch
2 Burst Latch
3 Channel Parity-Error Latch
4 Initial Select Latch
5 Channel 1 Interrupt Buffer Latch
6 Spare
7 Suppress Control Latch

GT--Channel Branch Conditions
0 Address In
1 Not Select In
2 Service In
3 Status In
4 Operational In
5 Not Request In
6 Channel Identification Latch
7 Channel Diagnostic Latch

Bits 0-5 of Sense Byte 1: These bits are common to all devices and are described in the System/360 Principles of Operation, Form A22-6821.

1.18 SYSTEM CONTROL PANEL

This section describes the controls and indicators on the system control panel that are unique to the Model 25 and/or fundamental to maintenance strategy (Figures 1-120 and 1-121). Other controls and functions are explained in the IBM System/360 Model 25 FETOM, Form Y24-3527.

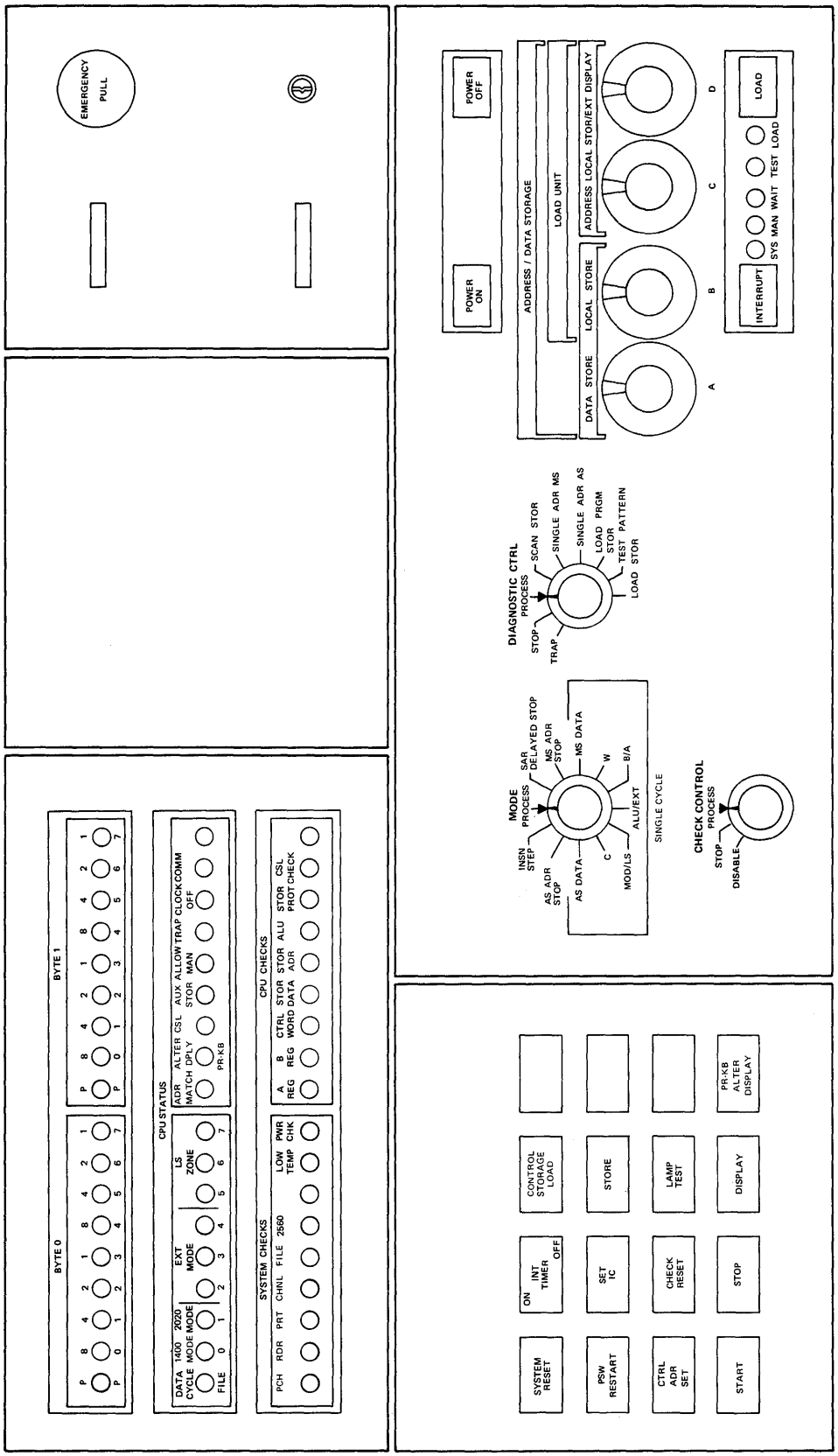
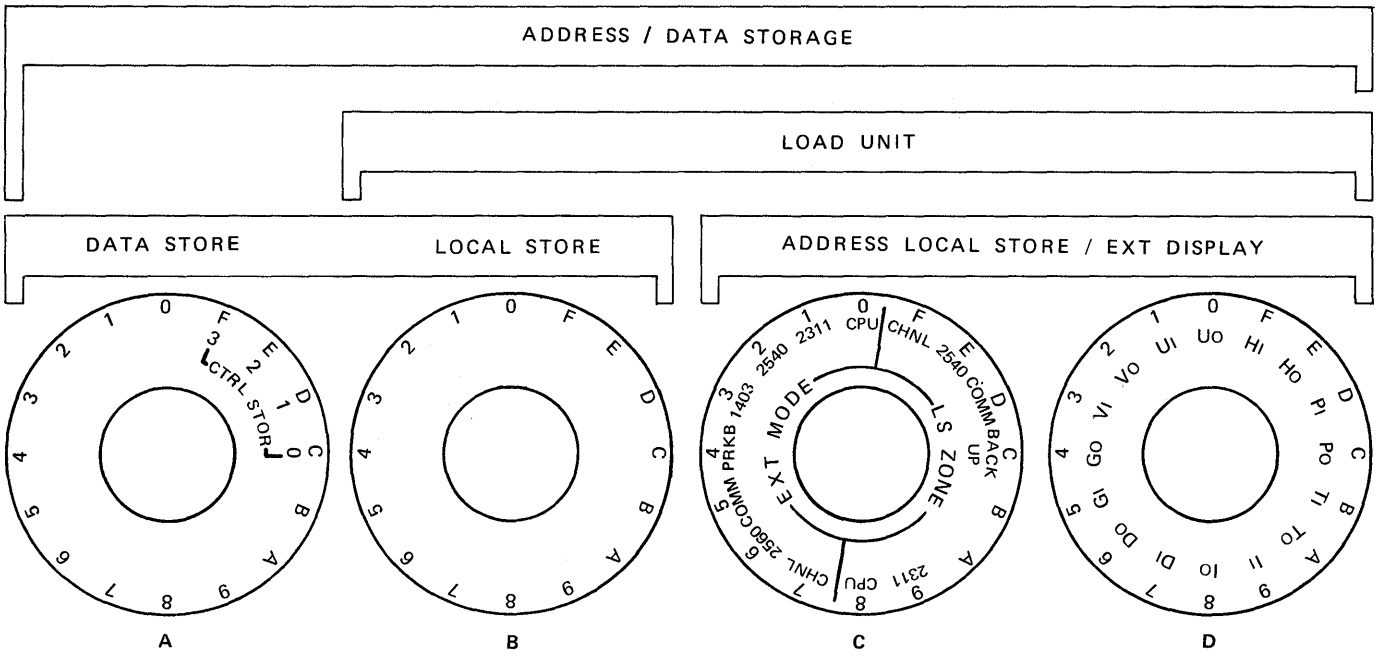
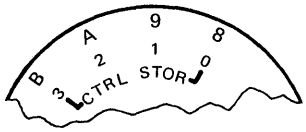


Figure 1-120. System Control Panel



Switch A For 16K Systems



Switch A for 24K and 32K Systems

Note:
The full view of Switch A shows control storage positions for 48K systems, the partial views of Switch A are used for 16K, 24K, and 32K systems.

Figure 1-121. Control Panel Switches A, B, C, and D

1.18.1 CPU STATUS INDICATORS

1.18.1.1 Address Match

The address match indicator is turned on by:

a. Address Match Latch - when the mode switch is in AS ADR STOP or MS ADR STOP. The CPU clock stops when the address match latch comes on. It is reset at T1 time.
b. SAR Delayed Stop Match Latch - when the mode switch is in SAR DLY STOP. The instruction in progress is completed and the CPU enters a soft-stop state; the indicator is reset when the start key is pressed (clock start pulse).

1.18.1.2 Alter/Display PR-KB

Pressing the PR-KB alter display key turns this light on to indicate that the alter/display microprogram is waiting for an operator response on the 1052 printer-keyboard. This light is turned off by pressing the start key, or after the operator has completed the required keyboard entry.

Control storage cannot be altered from the 1052 unless the CE key is on.

1.18.1.3 CSL

Pressing the control storage load key turns on this light and starts the CSL

microprogram. The indicator is reset when the CSL routine is completed.

1.18.1.4 Allow Manual

The ALLOW MAN light being on indicates that storage can be manually displayed or altered from the CPU control panel.

The MODE SW must be in the AS DATA or MS DATA positions and the CPU is not stopped after the first cycle of a storage word.

1.18.1.5 Trap

When any TRAP is allowed to occur the trap light is turned on.

1.18.1.6 Clock Off

The CLOCK OFF light is turned on when the CPU clock is not running.

1.18.2 SYSTEM CHECKS

1.18.2.1 Low Temperature

The LOW TEMP light indicates that the system is not yet up to minimum core-storage array operating temperature (96F±5F). When system power is turned on, this indicator lights and stays on until the specified operating range is reached (approximately 2 minutes, depending upon room temperature).

1.18.2.2 Power Check

The PWR CHK light turns on if any dc supply falls below its sensed output level (and/or circuit breaker or thermal sensor trip). The machine sequences down to its normal power-off status.

Power restart cannot be activated until the power-check light is reset by pressing the power-off switch and/or resetting the tripped circuit breaker or manually operating the thermal-reset switch. This must be done by a customer engineer.

If no circuit breaker is tripped or no thermal indicator is set in the power tower, the reason for the power failure is a sensed low output from any of the dc supplies (except the 24V dc control voltage).

The power check light also turns on if any of the fuses F30 through F35 are open. These fuses are in the 1403 attachment. The machine will not power-off under this condition. The light will go off when the open fuse is replaced.

1.18.2.3 PCH (Punch)

The PCH indicator is turned on for the following error conditions.

- Hole-count check
- Address check
- Shift register sync check
- Overrun
- PFR validity
- Punch not ready at start I/O of a command other than sense or No-Op.

1.18.2.4 RDR (Reader)

The RDR indicator is turned on for the following error conditions.

- Hole-count check
- Address check
- Shift register sync check
- Overrun
- Validity check
- Reader not ready at start I/O of a command other than sense or No-Op.

1.18.2.5 PRT (Printer)

The PRT indicator is turned on for the following error conditions.

- Print hammer check
- PIB parity check
- Printer not ready at start I/O of a command other than sense or No-Op.
- Coil-protect check bypass switch in 1403 CE area is on.

1.18.2.6 CHNL (Channel)

The CHNL indicator is turned on for a parity check on bus in or a microprogram-detected channel error.

1.18.2.7 File

The FILE indicator is turned on for a machine-check trap or a parity error detected during file operation.

1.18.3 CPU CHECKS

1.18.3.1 Control Word

The CTRL WORD light indicates that the control word currently in the C-register has bad parity when read from the storage data register.

1.18.3.2 Storage Data

The STOR DATA light indicates that the information contained in the storage data register contains bad parity.

1.18.3.3 CSL Check

This light is an indication that the checksum microroutine has detected a

difference between the checksum control word and the contents of control storage.

1.18.4 OPERATOR'S CONTROL PANEL (OCP) INDICATORS

1.18.4.1 Power On Key

This key is backlighted in white to indicate that the system power-on sequence is completed. If the key glows pink, the power-on or power-off sequence cannot be completed because of a malfunction in a power supply or an I/O unit.

1.18.4.2 Pluggable Indicators

Refer to IBM System/360 Model 25 External Field Definitions, Form Z29-2176.

1.18.5 KEYS

Only those keys that have special significance in the maintenance strategy are discussed here. Refer to the Model 25 FETOM, Form Y24-3527 for a complete description of the console keys.

1.18.5.1 Control Storage Load

This key is used to initialize the system when:

1. Operating modes are to be changed (as from Model 25 mode to 1400 mode),
2. The contents of control storage have been affected by a system failure, or
3. The system is being returned to the customer after extensive service (such as engineering change activity.)

1.18.5.2 PSW Restart

This key is used to restart an application using the IPL PSW, rather than the current PSW used when the system-reset key is pressed.

1.18.5.3 Control Address Set

This key must be pressed to allow the CE to restart the microprogram at an address other than that specified by the normal control-storage addressing means. The CTRL ADR SET key is operational only when the CPU clock is off.

1.18.5.4 Enable Control Storage Store

This switch must be pressed and held during a store into the control storage area of core storage so that the control-storage store circuitry remains activated. The storage operation is successful when the new information is displayed in the byte-0 and byte-1 indicators.

This key is effective only when the use-meter key switch is in the CE position.

1.18.5.5 Printer-Keyboard Alter/Display

Although this key is available for customer use, it is used in maintenance strategy to control certain phases on the 1052 diagnostics.

1.18.6 MODE SWITCH

Only switch positions that are unique to the Model 25 maintenance strategy are described here. Refer to the Model 25 FETOM, Form Y24-3527 for complete information.

1.18.6.1 Main Storage Address Stop

With the switch in MS ADR STOP position, the machine stops at the completion of the microword in progress when the address in switches A, B, C, and D matches the address of the core-storage location being accessed. The address-match indicator turns on. Byte-0 and byte-1 indicators display the address of the position of memory that was just accessed. The match occurs for addresses that specify either program or control storage.

1.18.7 DIAGNOSTIC CONTROL SWITCH

1.18.7.1 Stop

When the switch is in this position and no hubs are wired on the CE back panel, the system stops every cycle. When a circuitry line is wired to the COND IN hub on the CE back panel, the system stops every cycle in which the line goes positive.

1.18.7.2 Trap

This position forces a trap to the CE trap area of control storage. With the diagnostic control switch in the trap position and either (1) no wiring to the CE panel. or (2) a positive pulse to the IN hub of the CE panel, the machine-check latch is set and a trap is taken to 0280. If priority is not established in the trap routine, the trap to 0280 is repeated every other cycle. The CE trap routine can be used to log information on the printer-keyboard.

1.18.7.3 Scan Storage

With the switch in this position, all core storage positions are read and regenerated. When the check control switch is in the stop position, a parity error on storage data or a storage address causes a hard stop.

This switch position is also useful in displaying sequential storage locations when used with the mode switch in either the MS DATA or AS DATA position. With the mode switch in one of these positions, byte-0 and byte 1 indicators display the addressed location each time the start key is pressed.

1.18.7.4 Single Address MS

This position permits the CE to scan a single storage address set in switches A, B, C, and D by pressing the control address set key and then the start key.

1.18.7.5 Single Address AS

This position permits the CE to repeatedly access a single auxiliary-storage location set in switches A, B, C, and D by pressing the control address set key and then the start key.

1.18.7.6 Test Pattern

This switch position is used to exercise core storage with data set in switches A, B, C, and D. Switches A and B should contain the complement of switches C and D; i.e., ABCD = FF00, 00FF, 01FE, or FE01.

The system must be placed in CE mode by the CE key for the test pattern position of the diagnostic control switch to be effective.

Each storage address is accessed four times before a +2 address update occurs. During these four accesses a readout, store, readout, and store sequence is performed as follows (ABCD = FF00).

Addr	Cycle	Operation	Data
0000	1	Readout	Unknown (1st time)
	2	Store (AB)	FFFF
	3	Readout	FFFF
	4	Store (CD)	0000
0002	Same as address 0000.		
0004	1	Readout	Unknown (1st time)
	2	Store (CD)	0000
	3	Readout	0000
	4	Store (AB)	FFFF
0006	Same as address 0004.		

This pattern continues for the first 256 bytes of storage and reverses every 256 bytes.

Addr	Cycle	Operation	Data
0100	1	Readout	Unknown (1st time)
	2	Store (CD)	0000
	3	Readout	0000
	4	Store (AB)	FFFF
0102	Same as address 0100.		
0104	1	Readout	Unknown (1st time)
	2	Store (AB)	FFFF
	3	Readout	FFFF
	4	Store (CD)	0000
0106	Same as address 0104.		

This process continues for each program, control, and auxiliary storage location. The resident CSL area of control storage is read out and regenerated only.

1.18.7.7 Load Program Storage

When the switch is in this position, the data in switches A, B, C, and D is loaded into every halfword of program storage. When the control storage area of memory is reached, the locations are accessed in sequence, but the store lines are not activated. A storage scan should follow the load program storage to determine if the data is stored properly.

1.18.7.8 Load Storage

This function is similar to the load program storage operation except that all core-storage locations (program, control, and auxiliary, except the resident CSI area) are loaded with the data set from switches A, B, C, and D.

The system must be put in CE mode with the CE key for the load storage position of the diagnostic control switch to be effective.

To store into the CSL area, set the mode switch to MS DATA. The data switches can then be stored into the CSL area in single cycle.

1.19 MAINTENANCE PROGRAMS

The maintenance program package is designed to validate system and unit operation rapidly with a minimum of human intervention. The package is designed to progress from basic CPU-assurance microdiagnostics up through a system environment macrodiagnostic designed to exercise and test a majority of the system in a total system environment. The package provides failing-card locating information of high resolution for rapid repair. Refer to 2025 FEMDM, Form Y24-3529, page 1-1.

1.19.1 MACHINE LEVEL CONTROL (MLC) AND ENGINEERING CHANGES (EC'S)

Reloadable control storage is the unique Model 25 concept which requires definition under this objective. All IBM-supported Model 25 microprograms are provided with microprogram listings and punched-card decks. The listings and decks are generated by MAS (Microprogram Automated System). MAS has the capability of producing customized listings and decks on machine-feature sensitive microprograms.

1.19.1.1 FIELD MICROPROGRAM CHANGES

Field microprogram changes are released by Field B/M's and utilize existing Field B/M control procedures. These changes are accomplished with replacement core loads (in card form) and lists. The foregoing applies to all IBM-supported emulator and microdiagnostic microprograms.

1.19.2 FIELD CHANGE EXCEPTIONS

The following exceptions exist relative to field changes to any machine-feature sensitive microprogram core load.

1. MLC determines field machine requirement for changed microprograms (core load decks and lists).
2. MLC requires field machine-feature history information to achieve (1) above.
3. Field B/M's of microprogram emulators cannot be prepackaged.

1.19.3 UNIQUE CONSIDERATIONS

Unique FE responsibilities for field installation of a 2025 microprogram change are:

1. Changes to microdiagnostic programs are applied to FE tapes or disks when the M25 diagnostic program package is maintained in either form in addition to card decks. Tape and file utility programs, FOFF and FOFE, are used for such updates.
2. Changes to emulator microprograms are installed by replacement of the IBM-maintained customer emulator core load decks. The customer will be notified that affected customer duplicated emulator core loads should be updated.
3. On emulator microprogram changes the CE loads appropriate EC level identification into a CSL protected area of control storage. This enables checking for emulation EC level and machine EC level compatibility on CSL.

Check all microprogramming temporary fixes (MPTF) to ensure that they are incorporated in the current EC. Any missing MPTF must be added to the core load deck and recorded on the list before the customer is given the new deck. It is also necessary to alter the checksum in control storage for the emulator affected.

1.20 MULTISYSTEM CONFIGURATION

The Model 25 cannot be the host processor, but can be a supplement in a configuration controlled by a larger system having the channel-to-channel adapter feature. The direct control and external interruption features are provided on the Model 25 for the necessary intersystem data and control lines.

No unique maintenance features are provided or required on the Model 25 when it is operated in a multisystem environment.

1.21 1401/1460 AND 1440 COMPATIBILITY FEATURES

These special features are implemented almost entirely by microprogramming. The maintainability plan for this mode of operation assumes that the CPU, circuitry for integrated I/O attachments, and the standard I/O interface will be tested by the Model 25 diagnostic routines (resident and nonresident microdiagnostics, and the System/360 macrodiagnostic tests). No special 1400 compatibility diagnostic or function tests are provided for these features, and no special tools or test equipment are required.

The 1401/1460 and 1440 compatibility microprograms incorporate the following maintenance features.

- Resident CPU microdiagnostic (BDIA) and checksum tests,
- FE trap (64 bytes beginning at control-storage address 0280),
- Resident card-reader microdiagnostic (when the card reader is the only input device),
- Machine-check trap and 1052 logout, and
- 1052 alter/display.

The minor additional circuitry required for 1400-mode operation of 2311 and 2540 devices is tested using the microdiagnostics for these attachment features. The 1400-mode test in the CPU nonresident diagnostic must be initiated by a control address to the starting address of routine S14H in the diagnostic.

1.22 MODEL 20 MODE FEATURE

The Model 20 mode feature is implemented almost entirely by microprograms. It uses the normal Model 25 CPU hardware and I/O devices, except for the 2560 MFCM attachment feature that can be added specifically for Model 20 mode operations when required.

The maintainability plan for this mode assumes that the CPU and all I/O devices (except the 2560) are tested by the Model 25 diagnostics (resident and nonresident microdiagnostics, and the System/360 macrodiagnostic tests). The 2560 attachment is tested by nonresident microdiagnostics, and the 2560 is tested by Impulse Check Routines (ICRs) and Model 20 Machine Function Tests (MFTs). Refer to 2025 MDM, Form Y24-3529, page 1-1.

The Model 20 Mode feature microprograms incorporate the following maintenance features.

- Resident CPU microdiagnostic (BDIA) and checksum tests,
- FE trap (64 bytes beginning at control-storage address 0280),
- Resident card-reader microdiagnostic (when the card reader is the only input device),
- Machine-check trap and 1052 logout, and
- 1052 alter/display.

Operation of these maintenance features under Model 20 Mode is the same as for the basic 2025 except for machine check trap, which is described in the following section.

1.22.1 MACHINE-CHECK TRAP AND 1052 LOGOUT

With the check control switch set to PROCESS, detection of machine check will cause a machine-check trap to be taken. This microprogram stores status information in a part of the protected first 144 bytes of program storage. This logout area is also printed out on the 1052 printer-keyboard. The format of the logout is identical to that presented for Model 25 mode operation, and operation is similar except that after the logout, the machine stops instead of initiating an interrupt. (See Sections 1.17.1.1 and 1.17.1.2.)

1.22.2 DIAGNOSE INSTRUCTION

The Diagnose instruction (Op-code 83) is provided for use with the ICR and machine function tests. This instruction can perform several functions as specified by the D1 field of the instruction. For example, it is used to store the contents of the six diagnose op switches (auxiliary storage locations 00FC through 00FE) into program storage at locations 00FC through 00FE.

The diagnose instruction permits a diagnostic program to use special diagnostic microprogram routines in conjunction with normal machine instructions. A complete description of diagnose actions is given in the 2560 test descriptions, ID001 in Vol. 44.

1.22.3 CE TRAP

With the diagnostic control switch in the trap position, and any desired signal wired into the CE test panel, a microprogram trap is entered when the chosen signal goes positive. This function is the same for Model 20 mode as it is for Model 25 mode.

1.22.4 CE TEST PANEL HUBS

The function of the CE test-panel hubs (sync, switching, and match) is the same for Model 20 and Model 25 modes (see Section 1.23).

1.22.5 CE DISPLAY CABLE

This pluggable service aid provides similar information on the Model 25 operating in Model 20 mode as is provided on the Model 20 system. The 2560 attachment feature pluggable display charts are included in the publication, Model 25 External Field Definitions, Form 229-2176, available with the CPU.

1.22.6 PROGRAMMING ERRORS

Programming errors, such as invalid op-code, addressing error, specification error, etc., are detected by microprogramming during execution of the instruction. On the Model 20, such errors are indicated by stopping the system and displaying an error code in the I-register. However, when in Model 20 mode on the Model 25, the error code is printed on the 1052 to provide a corresponding identification of the error. See MDM 5-604 for a summary of error codes.

1.22.7 LOCAL STORAGE ZONE AND EXTERNAL MODE FOR 2560

In 2020 mode (mode register bit 1 on), 2311 data operations cannot overlap other operations. Therefore, local storage zone 1 is shared by the 2311 and 2560. External

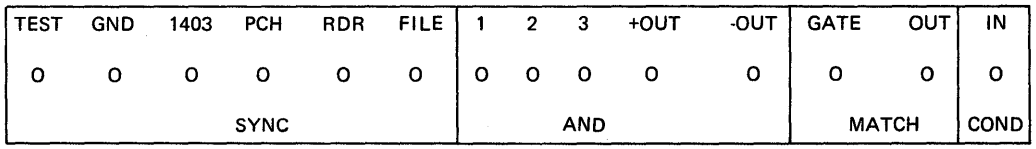


Figure 1-122. CE Panel

mode 6 and local storage zone 1 are assigned for use with the 2560.

For local storage zone 1 to be altered or displayed when it is being used for a 2560 operation, switch C must be set at the label 2311. External mode for 2560 can be altered or displayed by setting switch C to the label 2560.

1.23 CE PANEL

The CE test panel (Figure 1-122) is located on the A-gate back panel between boards C1 and C2.

Some of the uses of the the panel are to provide:

1. Sync points for scoping.
2. An AND function for various diagnostic purposes (scope sync, monitor, etc.).
3. Capability to stop the system under CE-selected conditions.
3. Capability to stop the system under CE-selected conditions,
4. Capability to trap into a reserved microprogram area under CE-selected conditions.

The plugs will accept either a banana plug connector or a bare wire.

The sync portion of the CE test panel has the following meanings.

TEST: This lamp is provided to check status of latches, etc. A +3V input to A2E6B12 turns the lamp on.
GND (Ground): This plug is provided to reduce breakage of D08 pins.
1403: +3V print control
RDR: +3V reader clutch
PCH: +3V punch clutch
FILE: +3V share cycle.

The AND hubs provide a 3-way positive input AND circuit with both plus and minus outputs when the three inputs are positive. Input lines (1-IN, 2-IN, 3-IN) float positive when not plugged to a signal. The functions of the hubs are:

1 IN: Input to 3-way positive AND
2 IN: Input to 3-way positive AND
3 IN: Input to 3-way positive AND
+OUT: Positive AND plus output
-OUT: Positive AND minus output.

The MATCH OUT hub is positive at T7 time when the storage-address register contents match the setting of the console address switches, and the MATCH GATE hub is positive. Because the address match circuits are sampled at T7, the MATCH GATE input must occur before T7.

A positive pulse to the COND IN hub causes either a stop or a trap depending on the setting of the diagnostic control switch.

1.23.1 STOP POSITION

A positive input pulse will stop the clock and cause a hard stop.

1.23.2 TRAP POSITION

A positive input pulse will stop the clock and cause a trap to control-storage address 0280. A 64-byte area starting at address 0280 is reserved for CE microprograms.

This area allows the CE to enter microprograms for diagnosing unusual or intermittent failures that do not respond to the primary microdiagnostic maintenance strategy. If desired, a monitor microprogram can be created and executed without affecting the customer problem program.

The system stops every cycle if the diagnostic control switch is placed in either stop or trap positions without the COND IN hub being wired.

1.24 POWER AND COOLING

1.24.1 FAILURE DETECTION, INDICATION, AND ISOLATION

The power system on the Model 25 features comprehensive circuit protection and failure detection facilities. Each dc power supply has an overcurrent-sensing

circuit breaker. An overcurrent condition on any supply causes the associated circuit breaker on that supply to trip mechanically, and the CB-trip light to turn on (light DS1 on the power control chassis). The power-check light on the system console turns on, and a normal power-off sequence occurs. Certain key power supplies have direct overvoltage detection. These are PS-1 (-6), PS-3 (-12), PS-8 (+12), PS-10 (+6), and PS-11 (+6). Detection of an overvoltage condition in these supplies causes the CB for the respective supply to trip, and the power-off sequence to occur as described previously.

A voltage-sensing system determines that all dc voltages are on and are supplying at least a certain minimum output. Failure in any dc supply causes power to be sequenced off and the power-check light on the system console to be turned on.

Thermal sensing switches are provided on logic gates, core storage, and power supply areas. When any of these thermal switches senses a temperature in excess of its specified limit, a normal power-off sequence is initiated and a thermal trip light on the power control chassis is turned on. The thermal trip prevents subsequent power-on sequence until the condition that caused the thermal trip is corrected and the thermal-trip reset switch on the power control chassis is actuated.

A power system diagnostic strategy has been developed based on the power supply failure detection system. This strategy consists of a guided step-by-step evaluation of the power system based on visual indications to isolate power system failures. To this end, a series of power system diagnostic strategy diagrams have been developed. These are included in the first part of the FE maintenance diagram manual for ready access by the customer engineer.

1.24.2 COOLING FACILITIES

Cooling facilities for the Model 25 consist of a number of blowers that force air past the component parts. There are three blowers for the power supply tower, three blowers for each SLT gate, three blowers for each core storage unit, and one blower for the 1403 hammer driver board. Each blower pulls air through an air filter to minimize dust accumulation. Warmed air exits through the grille at the top of the Model 25.

1.24.3 WARM-UP

The core storage units are the only devices in the Model 25 requiring a warm-up period. The temperature of these units must be maintained at from 96F±5F (35.6C±2.8C) to 120F±3F (49C±1.7C). If the temperature is below the limit, the low temp light on the system console turns on. If this light is on, correct operation of the core storage unit is not guaranteed. If the temperature is above the limit, a normal power-off sequence occurs and the thermal trip light on the power control chassis turns on. Thermal trip prevents subsequent power-on sequence until the condition that caused the thermal trip is corrected and the thermal trip reset switch is actuated.

Core storage temperature is controlled by maintaining the array inlet temperature at 105F±3F (40.4C±1.7C). An SCR-controlled heating element provides the necessary heat. After initial adjustment, the temperature is monitored by a thermistor in the array inlet air stream. The thermistor controls the SCR that supplies power to the heating element. The warm-up period varies depending upon the ambient temperature when the Model 25 power is turned on. Generally, the warm-up period takes about two minutes.

1.24.4 CONVENIENCE OUTLETS

Two convenience outlets provide 115 volts 60 Hz, single phase at a maximum of 15 amperes (200, 220, or 235 volts at 8 amperes for 50 Hz). For 60 Hz machines, an isolation transformer provides the correct voltage. For 50 Hz machines, the convenience outlets are powered either from the line or the adaption autotransformer.

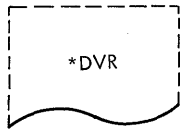
A pair of convenience outlets are mounted on each side of the power supply tower to minimize the necessity for using extension cords.

1.25 MAIN STORAGE DIAGNOSTIC AIDS

1.25.1 X AND Y DECODE NUMBERING SCHEME

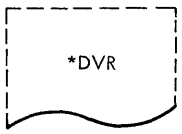
The numbering scheme used to identify the X and Y decode drivers makes it possible to identify the active circuit by knowing which bits are present in the storage address register. See Figure 1-123.

SAR	Bits	9	10	11	12	13	14
RD	WR	-	-	-	1	0	1



X-Decode ALD Representation

SAR	Bits	2	3	4	5	6	7	8
RD	WR	-	1	-	-	1	0	1



Y-Decode ALD Representation

Figure 1-123. X and Y Decode Drivers

X-Decode: The X-decode drivers use storage address register bits 1 and 9 to 14. Three symbols are used in the ALDs to show the conditions necessary to activate a decode driver. They are:

- -: This bit is not used to control this driver.
- 1: This bit must be present in order to activate this driver.
- 0: This bit must not be present in order to activate this driver.

Therefore, the S-decode driver specified in Figure 1-118 is activated when bit 12 of the storage address register is on, bit 13 of SAR is off, and bit 14 of SAR is on. The status of bits 9, 10 and 11 will not affect this driver.

Y-Decode: The Y-decode drivers use SAR bits 2 to 8 and are shown in the ALDs in the same way as the X-decode drivers. Therefore, a Y-decode driver specified as in Figure 1-118 is activated when SAR bits 3 and 6 are on and bits 7 and 8 are off. Bits 2, 4 and 5 will not affect this driver.

1.25.2 SCOPING STORAGE

Use an oscilloscope with a 25- to 60-nanosecond rise-time. The DuMont 766H the Tektronix* 561 S and 453 are oscilloscopes that meet these specifications. Use the oscilloscope probe ground near the point being probed. Use read-call 01 C-B2A3D11 for an oscilloscope sync point.

1.25.2.1 Scoping X and Y Source-Terminating Resistors

When storage problems cannot be easily diagnosed from the console by card substitution, scoping the X and Y terminating resistors may provide information that will assist in locating the trouble. When a failure is common to a large block of storage and cannot be easily isolated to a particular X- or Y-line, scoping the X and Y terminating resistor, while using the Model 25 diagnostic scan functions (MDM starting at Diagram 1-100), may indicate where the trouble might be found.

Because of SLT packaging, and because the array plugs into an SLT large board, a current probe can be used in very few places to check or observe the drive currents. However, all X and Y drive current comes from a group of four resistors, two for the X-lines (one for read and one for write) and similarly for the Y-lines. The resistors are mounted on the swing-open side of the store gate and are connected to the current sources via twisted wire cabling.

An indirect indication of array current is possible by monitoring any of the yellow wires (for example, the yellow wire to pin U4B12 for Y read current). If a current probe is available this can be done directly on the back panel, or alternatively with a voltage probe always on the yellow side connection of the resistors; the latter method will require the opening of the resistor gate (Figure 1-124).

Figures 1-125 through 1-130 show the waveforms for main storage control and drive lines during a specific condition. A variety of situations is represented by these oscilloscope photographs. Because these waveforms will occur only when a specific address or group of addresses is accessed, they will be mixed in with many correct waveforms. Under these conditions they can be difficult to distinguish from incorrect patterns. An attempt should be made to locate the failing address(es) and put the 2025 into an address loop while scoping is performed. Refer to Chapter 2.

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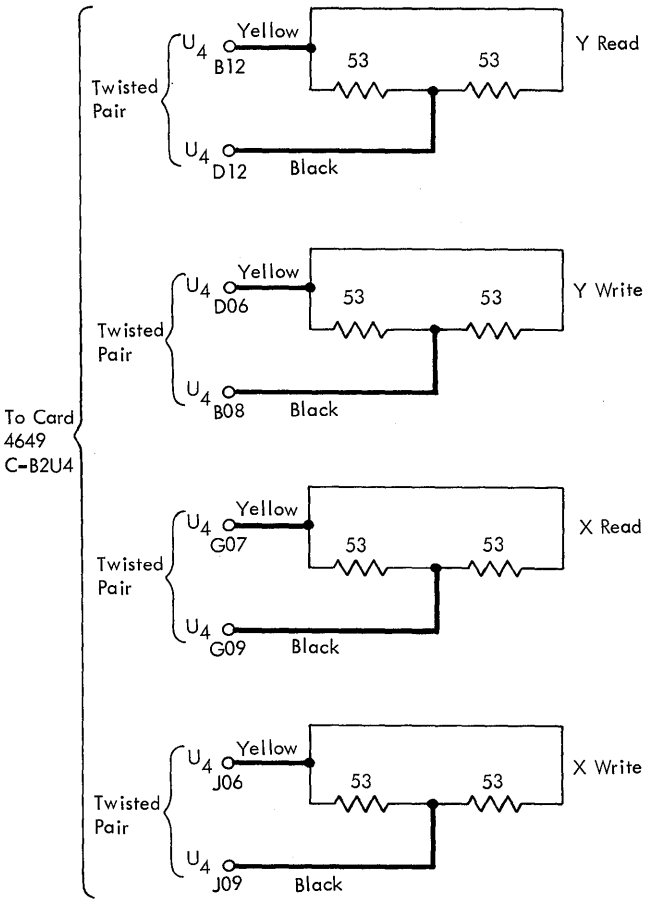
* Trademark of Tektronix, Inc.



NOTE: All the black wires are grounded in card 4649, pins D12, B08, G09, J09 being internally grounded. Some machines have yellow wire grounded.

Figure 1-124. X and Y Source Resistors

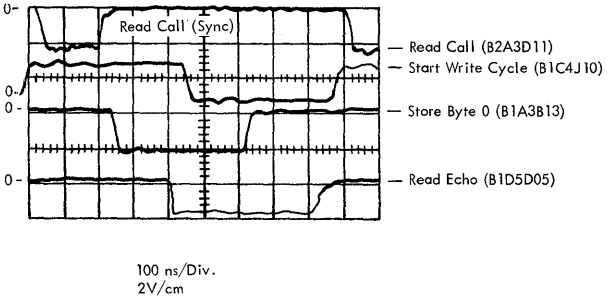


Figure 1-125. Storage Controls

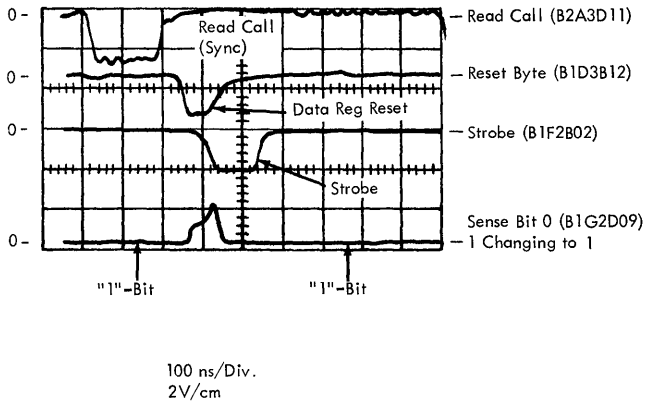


Figure 1-126. Read Cycle Controls

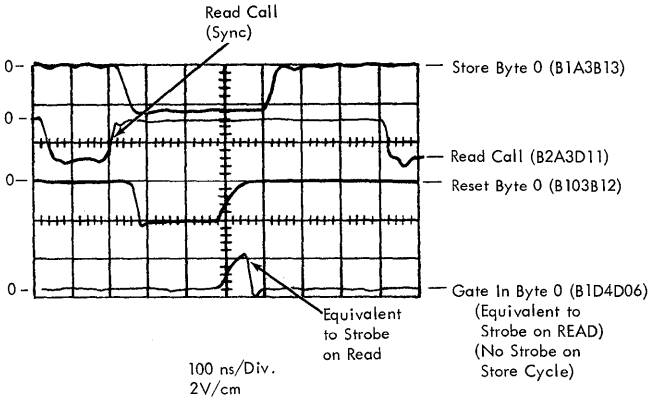


Figure 1-127. Store Cycle Controls

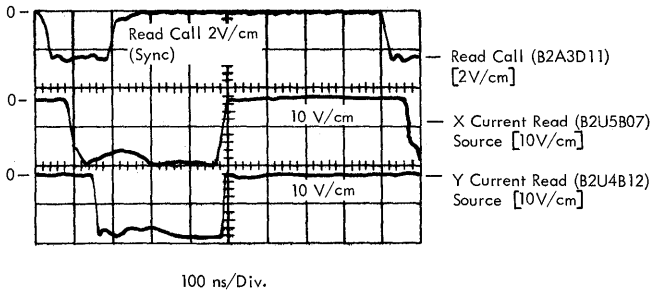


Figure 1-128. X-Y Read Current Source Driver at the Resistor

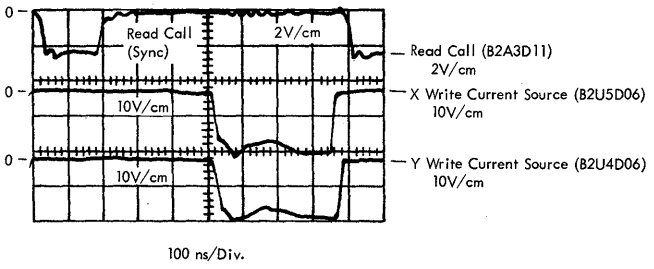


Figure 1-129. X-Y Write Current at Resistors for looping and scanning procedures.

1.25.2.2 Scoping Inhibit Drive Terminating Resistors

Inhibit drive current can be checked in the same way as read or write currents by probing the current-limiting resistors associated with each inhibit driver.

The Z inhibit driver source is essentially two NPN transistors in parallel, each transistor having a 70-ohm wire-wound resistor in series with the emitter. These resistors are mounted on the swing-open side of the BSM gate. The black and red wires are returned to the Z driver card. The yellow wire is common -30V. A pair of resistors is, therefore, common to each particular bit position and is also common to the 0-8K segment A and B, and 8-16K segment A and B.

The current probe can be used on the yellow wire, and the voltage probe at the red or black side of the resistors. The resulting waveforms of a correct inhibit driver are shown in Figure 1-130.

Approximately 760 mA is shared between the 70-ohm resistors (380 mA through each). The voltage swing should be approximately 26V at the read and black wire side of the resistors.

Substitution of the sense amplifier/Z power card can determine the failing location.

1.25.2.3 Array Sense Line Checking

Two methods may be used for checking array sense/inhibit lines.

Figure 1-131 identifies the method to be used with the array plugged to the main storage SLT board. It is possible to meter the connections between sense line input pins and the inhibit line pin.

Figure 1-132 identifies the method to be used with the array removed from the machine. (The removal procedure is described in Chapter 4 of this manual.)

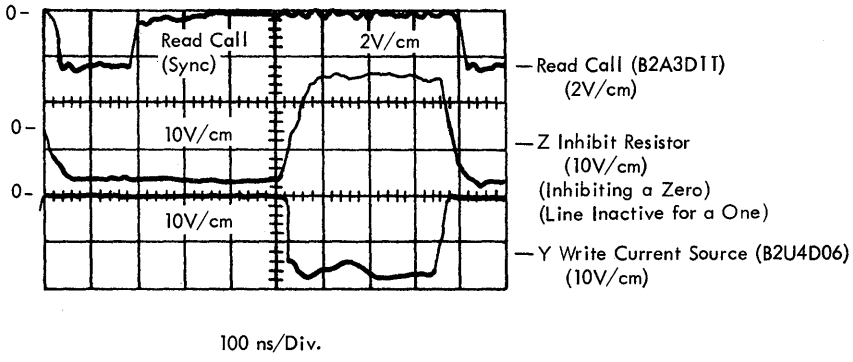


Figure 1-130. Z-Inhibit Driver (Writing a Zero)

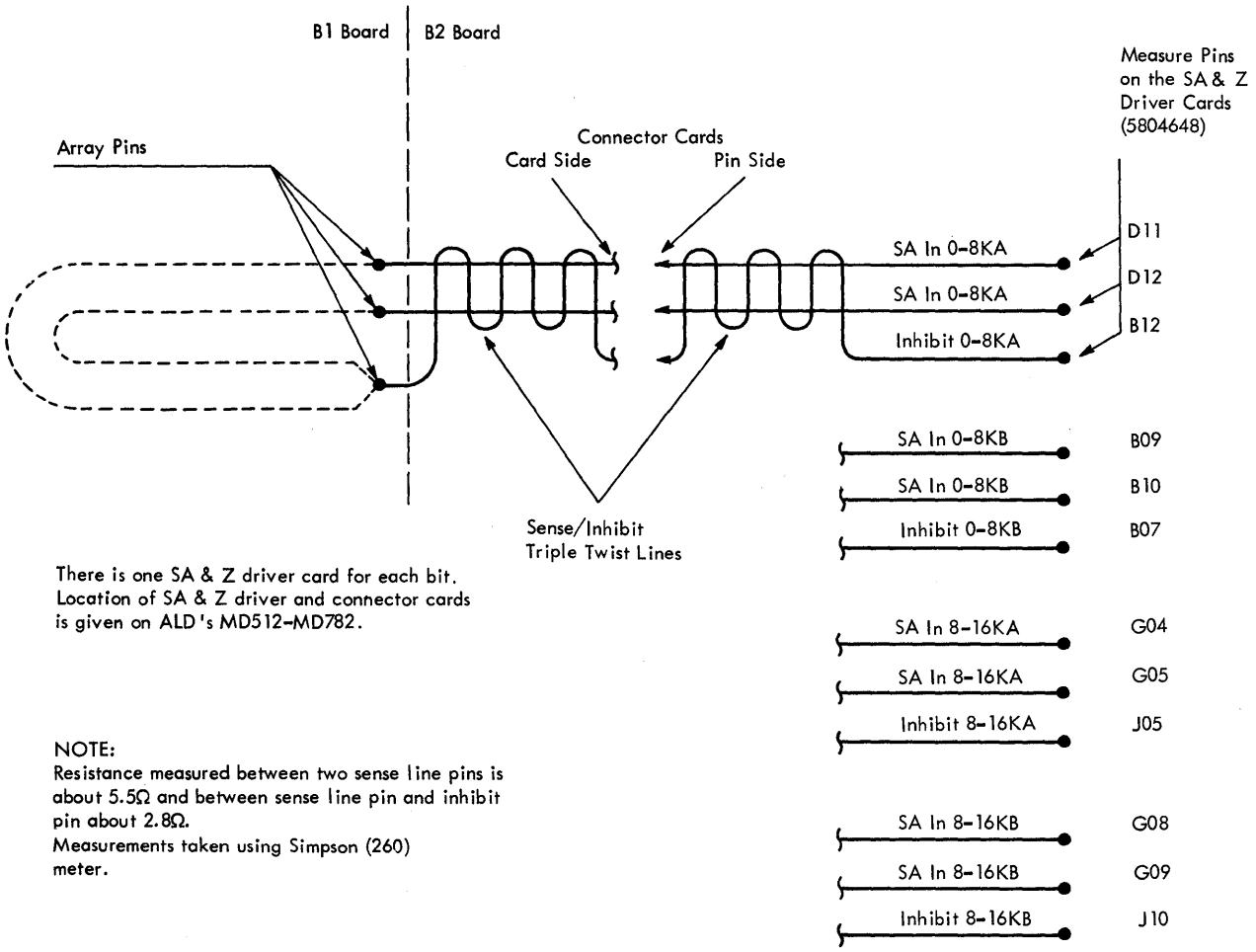


Figure 1-131. Main Storage Array Measurements

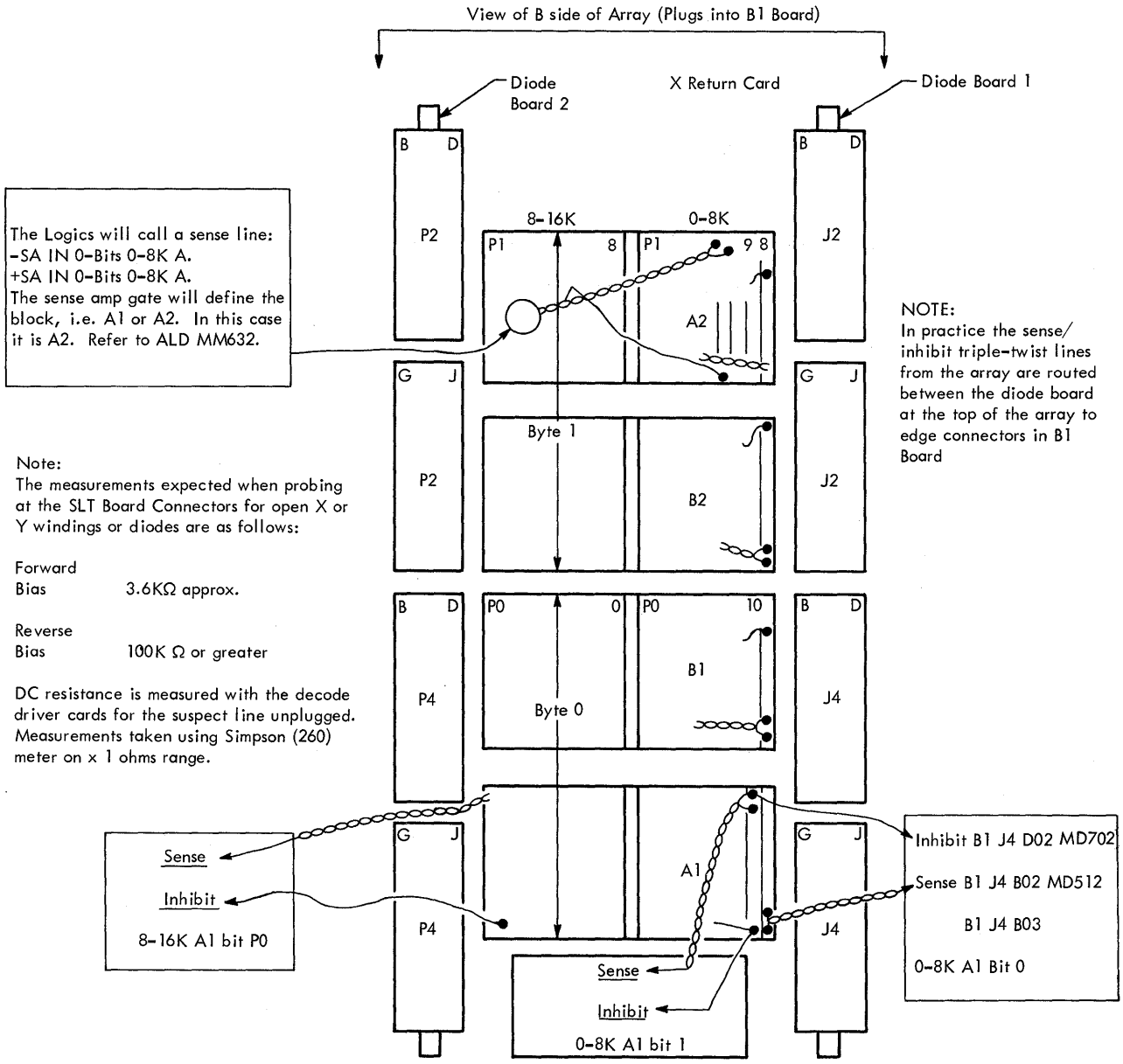


Figure 1-132. Main Storage Array Line Measurements

1.25.2.4 Array X and Y Drive Line Checking

With the aid of MDM 4-27 (Part 4 of 5) and AID pages MD860-MD891, any of the 136 Y-array wires or the 128 X (sections 0-8K or 8-16K) array wires can be ascertained.

SAR bits 2-8 select the Y-lines (SAR bit 8 being the least significant). SAR bits 9-14 select the X-lines (SAR bit 14 being the least significant). SAR bit 1 selects the 0-8K or 8-16K section of the array; the 8-16K section is selected when bit 1 is a 1. SAR bit 15 is ignored.

The following example illustrates checking the continuity of any array drive line without first having to unplug the array.

If an open Y-drive line is suspected, determine SAR bits 2-8. If, for example, they are 1011111, then reference to MDM 4-27 (Part 4 of 5) shows the Y-drive line to be 138, C-side. This particular drive line can be traced to storage logic pages MD412 and MD452.

The continuity of array drive line 138 is checked by placing the leads of an ohmmeter between C-B2E2J02 and C-B2S2J04. The forward resistance is usually between 3.6 kilohms and 4.0 kilohms (that is, two array diodes in series). The dc resistance of the array line itself is approximately 12 ohms. The reverse resistance is normally greater than 100K ohms.

The X-lines have forward resistance of 3.6 kilohms, which is measured with the 5808198 cards still plugged in. The forward resistance is similar to that of any Y-line when these cards are removed.

1.26 LOCAL STORAGE DIAGNOSTIC AIDS

Figures 1-133 through 1-141 show the waveforms for local storage (LS). Figures 1-140 and 1-141 show bad waveforms.

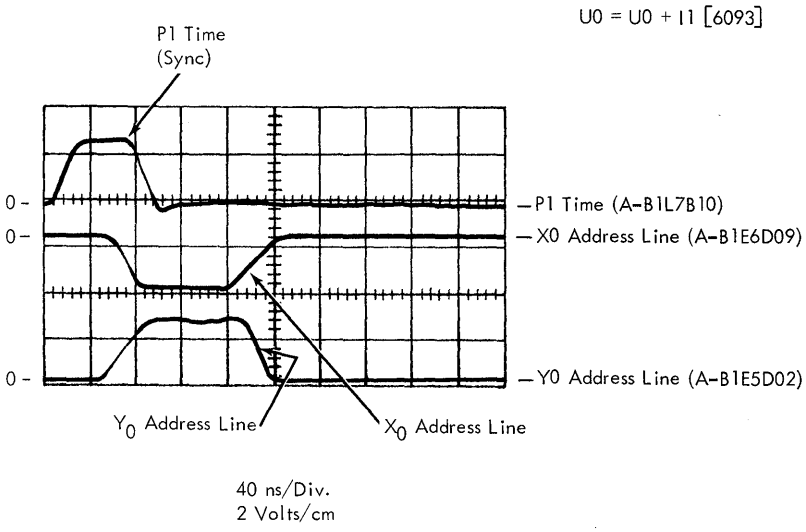


Figure 1-133. LS-Addressing (P1-Time Access)

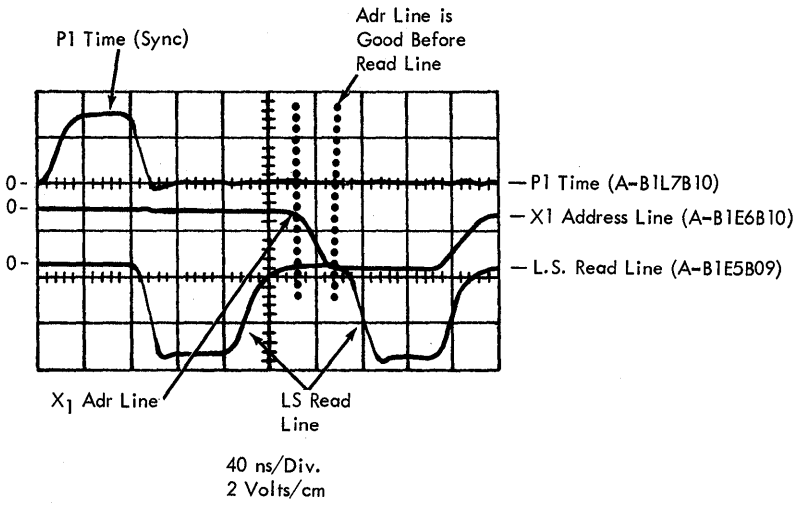


Figure 1-134. LS-Addressing (P3-Time Relationship Between X and Read Line)

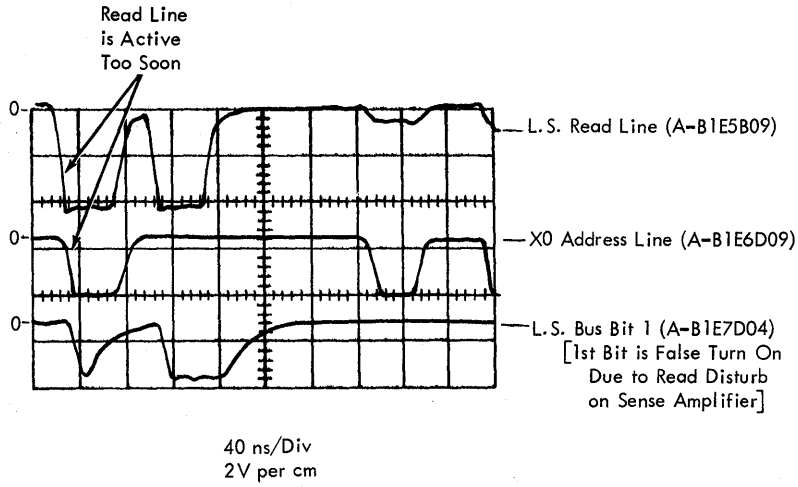


Figure 1-135. LS Bit Output (2 Successive Zeros at P1 and P3 Time)

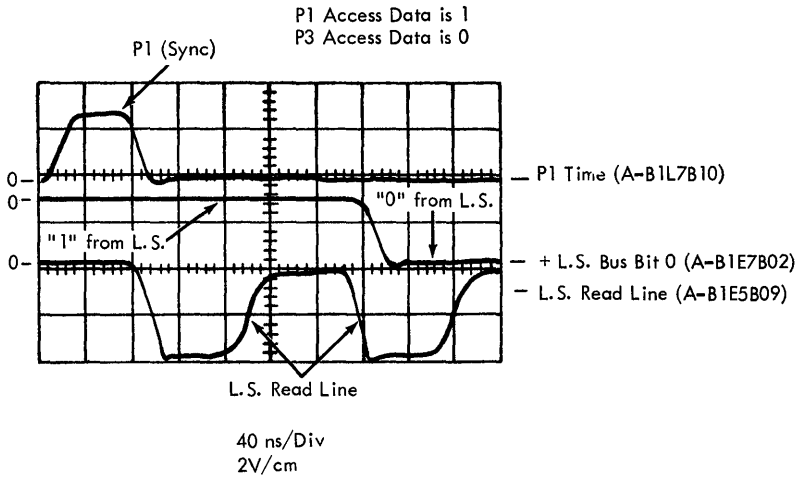


Figure 1-136. LS Bit Output (P1 Access Data is 1, P3 Access Data is 0)

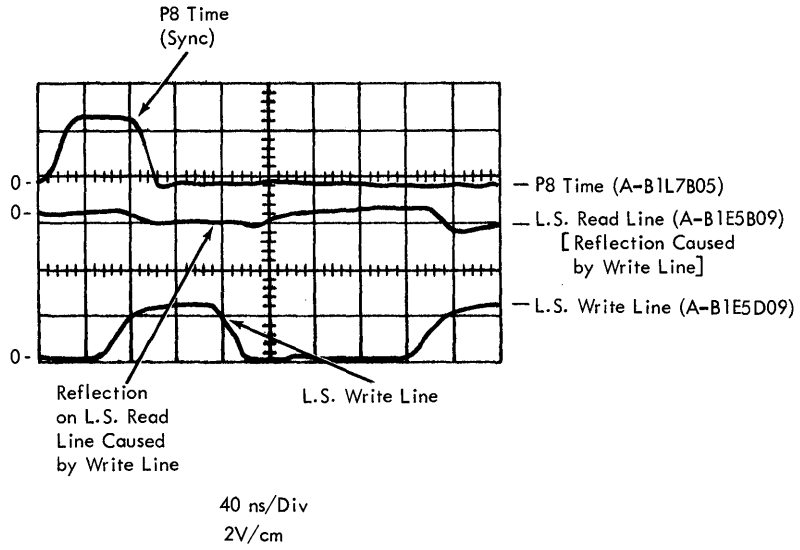


Figure 1-137. LS Write Line (P8-Time)

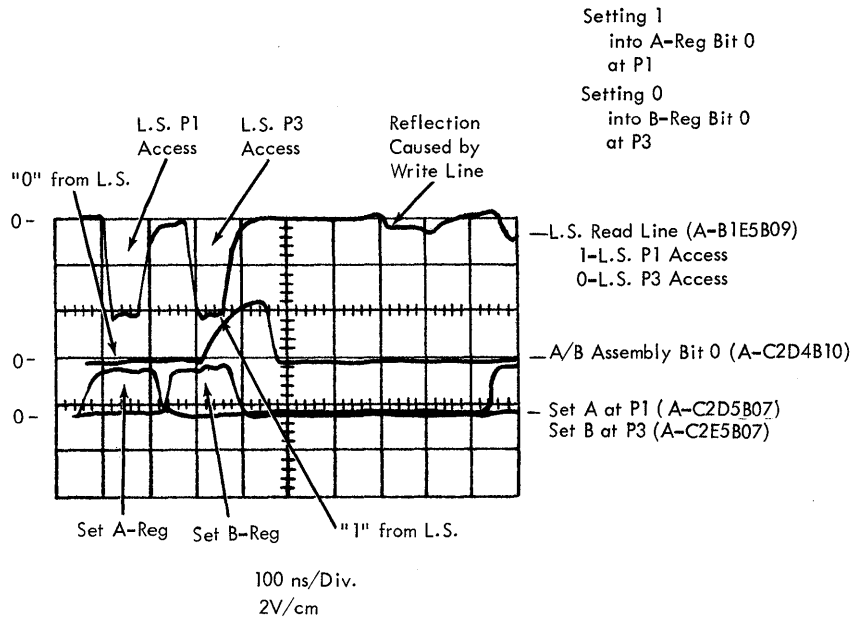


Figure 1-138. AB-Assembly Data From Local Storage

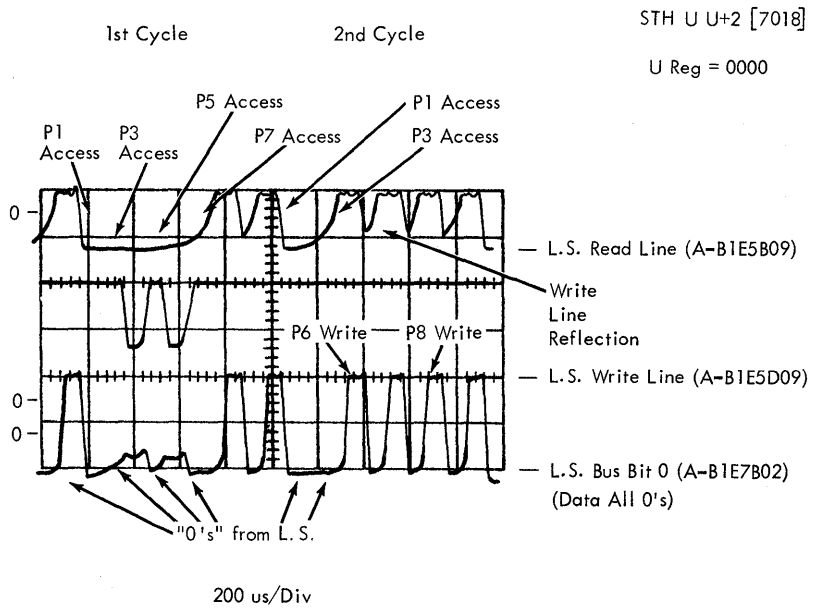


Figure 1-139. Storage Word (WT-2)

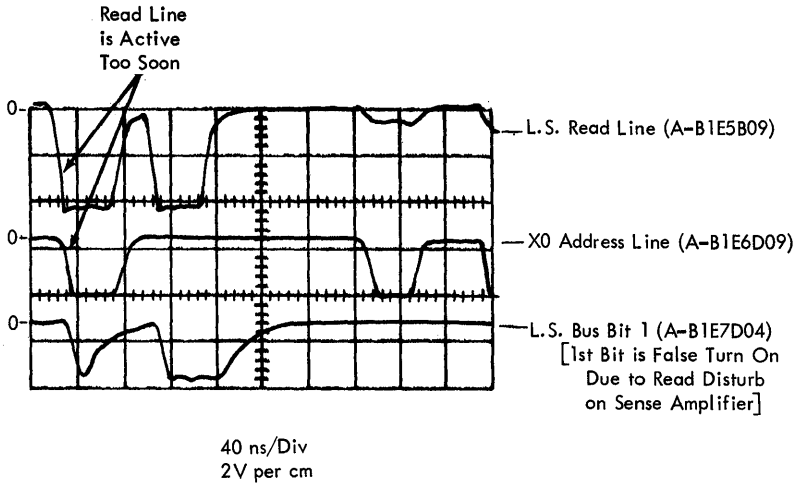


Figure 1-140. Bad Waveforms (Read Line Set Too Early--Zero Delay)

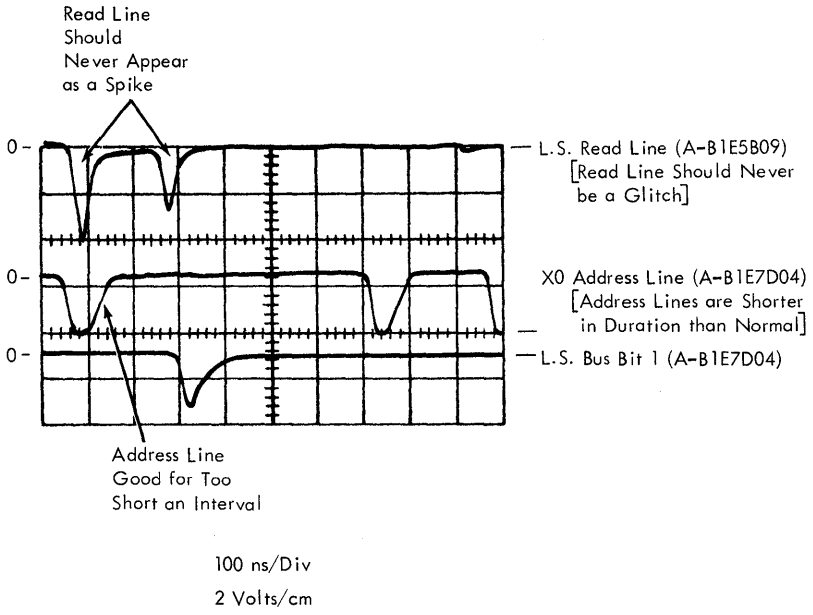


Figure 1-141. Bad Waveforms (LS Address Line Reset Delay Bad--Zero Delay)

Chapter 2. Console and Maintenance Features

Section 1. Basic Unit

2.1 STORAGE PROTECT KEY--DISPLAY

For the storage key to be displayed, the M-register must be set to the 2,048 bytes associated with the CPU storage key. For the protect key associated with an MPX UCW or ICA UCW to be displayed, the M-register must be set to the UCW auxiliary storage address. Therefore, a manual display of auxiliary storage must be done to see the protect key used by an SIO; a manual display of main storage must be done to see the CPU storage key.

After the manual display, turn the mode switch to ALU/EXT position and dial switches CD to 03 (CPU mode external decode 3). Pressing the display switch gates the storage key into byte 1.

The selector channel key can be displayed by using auxiliary storage address XX88 and following the preceding display procedure. This is possible since MPX UCWs cannot be used when channel burst mode is defined.

There are two exceptions to this display procedure. The M-register does not have to be set up to display the effective file protect key. This is possible because the file key is stored in hardware (not STP local storage). To display the effective file protect key, dial 12 in switch CD and dial ALU/EXT.

To check the protect key associated with the integrated 2540, 1403, or 1052 UCW, refer to the auxiliary storage map for module 0 to determine which byte to display. During data transfer, the protect key is stored with the storage key read from STP local storage.

2.2 PATCH CARD GENERATION

This procedure can be used to make a patch card for entering a microprogram into the FE trap area. The system must have the System/360 emulator loaded. Enter the following data into the locations specified, make the punch ready, set IC to 0058, press the start key. The replace Card will punch in EBCDIC format. This replace card can be inserted before the end card of a CSL deck or you can make up a standalone deck in the following manner.

1. Five card loader
2. Four cards from the 360 emulator CSL deck for CS module addresses 0100, 0140, 0180, 01C0 (card numbers 6, 7, 8, and 9)
3. The replace card
4. The end card, blank in column 3.

If the loading device is on the channel, use the following.

1. One-card channel loader
2. Four cards from 360 CSL deck addresses: 0100, 0140, 0180, 01C0 (card numbers 6, 7, 8, and 9).
3. The replace card
4. The end card, blank in column 3.

```
0048-00000 0050   CAW
004C-00000 0000   Spacer to align boundary
0050-0100 0068
  2000 0050       CCW,punch
0058-9D00 000D    Test I/O clear status
005C-4770 0058    Wait for clear status
0060-9C00 000D    Start I/O punch
0064-47F0 0064    Wait
0068-0280         FE trap address
006A-10           10 Cntrl, 20 Aux, 80 PGM
006B-20           No. of halfwords to enter
                   hex
006C-xxxx xxxx
  --etc.          Ctrl words up to 128 hex
                   chars
```

2.3 DEBE-2

Load DEBE-2 from a card reader. When the machine goes to wait state, press the interrupt key. DEBE-2 types out ENTER PROG ID - XX. The correct response to this message is listed as follows.

CCSPACE	Card-to-card 80/80 using units 00C and 00D.
CPSPACE	Card-to-printer 80/80 BCD units 00C and 00E.
CTSPACE	and-to-tape 80/80 using 00C as the card reader. A request will be typed for a tape address.
TCSPACE	Tape-to-card 80/80 using 00D for the card punch. A request will be typed for a tape address.

TDSPACE Tape display) tape-to-printer hex, using 00E for the printer. A request will be typed for a tape address.
TPSPACE Tape-to-printer BCD using 00E for the printer. A request will be typed for a tape address.
TTSPACE Tape-to-tape. Address will be requested.
WTSPACE Write tape mark.
RWSPACE Rewind tape. Address will be requested.
SRSPACE -Space records on tape (forward) address and number of records to be skipped will be requested.
SFSPACE Forward space file on tape. Address will be requested.
BSSPACE Backspace records on tape. Address and number of records to backspace will be requested.

A request for a tape address is in the form MMXXX. The MM refers to the mode set command for 7-track tapes. Type 00 for 9-track tapes.

To put DEBE-2 onto a self-loading tape, change the last card of the DEBE-2 deck column 8 to 12-8-4 punches, load the deck, and at IPL wait, alter storage locations 04A0 and 04A1 to the address of the tape drive you are using to build the DEBE tape. Then, press the interrupt key. DEBE-2 will load itself onto the tape. You may then load DEBE by loading directly from the tape.

DEBE CCW are as follows.

Reader CCW location	1BE0
Punch CCW location	10F0
Print CCW location	1140
Tape in location	1228
Tape put CCW location	1318

Reader CCW	4200 1CF0 0000 0050
Punch CCW	4100 1CF0 0000 0050
Print CCW	0900 1D40 0000 0084
Tape read CCW	0200 1DC8 2000 2710
Tape write CCW	0100 1DC8 2000 0018

2.4 I/O EXERCISER ROUTINE WITH VARIABLE DELAY

This program loop will operate the reader or any I/O device at a repetition rate determined by the setting of console switches ABCD. Any value up to 7FFF may be used. This routine is useful when trying to duplicate intermittent I/O failures that seem to occur due to the time frequency at which the I/O device is operated. The channel and device address is in locations 0408-0409 and 0410-0411. The CCW command code is in location 0428. Eighty columns of data are read into or written from storage starting at location 0600. Start the program at 0400.

```
0400-D203 0048 0424  Move CAW
0406-9D00 000C       Test I/O reader
040A-4770 0406       Wait for clear status
040E-9C00 000C       Start I/O reader
0412-8300 0AD4       Store switches ABCD in
                       0410
0416-0000            Locations for switch
                       bytes
0418-4820 0416       Store switch amount in
                       reg 2
041C-4620 041C       Branch on count reg 2
0420-47F0 0406       Branch to read next
                       card
0424-0000 0428       Spare CAW
0428-0200 0600
  2000 0050          CCW read and feed
```

2.5 CONSOLE INQUIRY PROGRAM

Load the program using the console alter/display routine. Set IC to 0424 and press start. The system will enter wait state. Press the request key. The proceed light should come on. Key in up to eighty characters. Press EOB and ALT if less than eighty characters. The information entered should be typed back. The system will enter wait state. To repeat, press the request key etc.

```
0400-9180 0044    TM attention on
0404-4710 040C    BC SI/O if attention
0408-47F0 041C    BC enter wait
040C-9C00 001F    SI/O to console
0410-4770 040C    BC CC is not zero
0414-9D00 001F    TI/O clear interrupt
0418-4720 0414    BC branch busy
041C-8200 0440    LPSW enter wait
0420-47F0 0420    BC wait loop
0424-5810 0448    Load CAW start here
0428-5010 0048    Store CAW
042C-47F0 041C    Unconditional branch
0430-0A00 0450
  6000 0050       CCW read inquiry
0438-09000450
  0000 0050       CCW write chained
000-800 0000
  0000 0420       PSW problem
0448-0000 0430    Stored CAW
008-000 0000
  0000 0400       PSW I/O new
```

2.6 1401 EMULATOR CSL DECK

This procedure can be used to make a system overlay card for entering auxiliary storage module 0 control data into the 1401 emulator CSL deck. The system must have the 360 emulator loaded. Enter the following data into the locations specified via the console alter/display routine. Make the punch ready, set IC to location 0058, and press the start key. The

configuration card will be punched continuously in EBCDIC format. It should be inserted before the end card of the 1401 emulator CSL deck.

Note: When a blank is specified key 40:

```
0048-0000 0050    CAW
004C-0000 0000    Zeros to align boundary
0050-0100 0068
  2000 0050       CCW-punch
0058-9D00 000D    Test I/O clear status
005C-4770 0058    Wait for clear status
0060-9C00 000D    Start I/O punch
0064-47F0 0064    Wait
0068-7040*        *9040 to be used on 24K
                    systems
006A-20           20- Enter auxiliary
                    storage
006B-1E           Number of halfwords to be
                    entered
006C-XXXX XXXX
  etc.            Enter 120 hex characters
```

2.7 1403 BUFFER LOAD MICROLOOP

This routine repetitively loads one buffer position with data.

1. Manually set I/O to the desired buffer address.
2. Manually set T1 to the desired data character.

Hex Address	Hex Word	Statement
0280	2484	Set Mode K=8
0282	4F8F	PR=10
0284	2004	Set PRA K=20
0286	0000	No-Op
0288	4BBF	PR0=T1
028A	8280	Br to 0280

2.8 SOFT-STOP LOOP--SINGLE CYCLING

At present, the Model 25 does not allow an operator to single cycle through the soft-stop loop. This happens because the start key resets the soft-stop latch and the microloop exits to I-cycle. This is corrected by blocking the reset of the soft-stop latch by the start switch with the diagnostic stop switch.

The procedure to allow single cycle and stay in the loop is to place the diagnostic switch in the stop position. Nothing can be wired to 'condition in' on the CE panel at this time. Exits such as integrated requests, instruction step printout, etc., will be capable of taking the microprogram out of the soft-stop loop. If an I-cycle exit is desired, the operator must place the diagnostic switch back to process position.

2.9 STORAGE SCAN

An operator may be confused when scanning auxiliary storage if the diagnostic switch is in scan, load storage, or test pattern position. The storage unit ignores the second hex digit of the auxiliary storage address when auxiliary storage is addressed (0X00). In scan mode, advance the storage address by +2 each cycle. As a result, addresses 0000, 0100...0F00 access the same auxiliary storage location 0000. If one syncs on ADDR match or does an AS ADDR stop on any auxiliary storage address, the machine will stop sixteen times because it accesses each location sixteen times.

2.10 WORST-CASE STORAGE SCAN DEFINITION

The purpose of the test pattern switch is to scan memory and exercise it with a worst-case pattern. The pattern can be one of the following combinations and must be dialed in switches ABCD: FF00, 00FF, 01FE, FE01.

During the first scan, switch CD is stored in the first four-bytes of storage. AB in the next four bytes, and the pattern switches repetitively in this manner. This same pattern flips every 256 addresses (if ADDR 0000 has a FFFF stored in it, hex address 0100 will have 0000).

Each address of storage is accessed four times before a +2 address update occurs. During the first access, the contents of that location are read out. The second access stores the complement of that location in place of the original data. Then, this complement data is read out, and finally, its complement (the original data) is stored back.

For Example:	ADDR 0000	
1st Cycle	Read Out	FEFE
2nd Cycle	Store	0101
3rd Cycle	Read Out	0101
4th Cycle	Store	FEFE

This process continues for each address of main storage, auxiliary storage, and control storage. Only the protected area of control storage remains unchanged.

2.11 MS ADDRESS STOP PROCEDURE DURING IPL OR CSL

A condition exists when trying to MS-address stop during IPL and CSL because both the device address and the SAR stop address cannot be in switches ABCD. To bypass this condition, the following procedure should be followed.

MS-Address Stop Procedure

During IPL -
1. Set MODE sw to MS ADDR STOP.
2. Set ABCD sw to CTRL STOR ADDR 0ADA.
3. Press CONTROL STORAGE LOAD.
4. Press START.
5. Set MODE sw to Single Cycle Mode.
6. Set BCD sw to the Load Device Addr.
7. Press START sw three (3) times.
8. Set MODE sw to MS ADDR STOP.
9. Set ABCD sw to the desired MS Addr Location.
10. Press START.

During CSL -
1. Set MODE sw to Single Cycle Mode.
2. Set ABCD sw to the Load Device Addr.
3. Press CONTROL STORAGE LOAD.
4. Press START 3 times.
5. Set MODE sw to MS ADDR STOP.
6. Set ABCD sw to the desired MS Addr location.
7. Press START.

2.12 PSW

2.12.1 PSW RESTART

The function of the PSW restart switch is to perform a PSW restart; this means loading the restart PSW from locations 0000-0007 of main storage (initial PSW).

2.12.1.1 Procedure

1. Press PSW RESTART.
2. Press SYSTEM RESET.
3. Note: In this case, it is not necessary to press the start key to begin program execution. If the system-reset switch is pressed without pressing the PSW restart switch, the current PSW will remain effective.

2.12.2 DISPLAY OF CURRENT PSW

The current PSW is displayed from local storage or auxiliary storage locations by setting switches A, B, C, and D, the mode switch as shown in the following, and by pressing the display key.

Current PSW Field	Mode Switch	Switches A,B,C, & D
Condition code	MOD/LS	P0
Program mask & AMWP	MOD/LS	I0,I0
System mask	AS Data	00A8
CPU key and AMWP	AS Data	00A9

Note: The condition code in P0 is coded as follows.

CC	P0 High
0	0
1	5
2	2
3	7

2.13 CONTROL STORAGE LOAD FAILURE DETECTION

Conditions: Loading from 2540 integrated unit, a single card at a time, any core load deck.

2.13.1 DESCRIPTION

This test can be used to troubleshoot a failure to CSL, especially on systems where the 2540 is the only program load device. It tests the BCPL, BDIA, BCHK, BSYS, BPSW, and BSWI microprograms, the CSL latch, the reader start, feed, and the data transfer circuits. It also allows the CE to check the contents of the first bootstrap card that contains a microprogram to start the next bootstrap cards and the control program to load.

The BNSR routine is contained on the first two of the five native bootstrap cards. The native bootstrap routine (BNSR) is entered at address 0100 from either the handloaded native bootstrap routine, or the resident control storage load routine (BCPL). Card number one is loaded into control storage starting or the BCPL routine. Address 0100 is branched to and card number two is loaded into the addresses following those occupied by card number one (this data forms the BNSR routine). The information contained in cards number three, four, and five of the native bootstrap is loaded into auxiliary storage to form a translate table which is used to translate the remaining CSL deck into the hex characters that are to be loaded into the control storage area and certain auxiliary and program storage locations.

The CSL procedure, up to the first actual control storage card, is shown in MDM 5-19. The handload procedure is covered in the descriptive text preceding the BCPL routine.

2.13.2 PRCCEDURE

1. Set switches A, B, C, and D to EE0C.
2. Press SYSTEM RESET.
3. Press CONTROL STORAGE LOAD (CSL)
   The CPU should be in a loop with the system light on. If this does not occur, it indicates a failure in the permanent CSL routine.
   Make certain that the CSL light is on. It may be necessary to restart in single-cycle mode to determine that the permanent CSI microprogram does not contain errors and that it correctly executes each statement.
4. Set switches A, B, C, and D to 407A (807A for 24K, 807A for 32K, C07A for 48K).
5. Set the mode switch to AS ADR STOP.
6. Place the core load deck in the reader and press the reader start key. The reader will feed one card and stop with the address match light on.
7. Press the CPU start key and a second card should feed.
8. At this time, the first bootstrap card has been read at first read. The contents of this card should now be stored in control storage locations 4100 to 4177 as follows.

9	Row	0100-CC05	2040	2F53	3CC9	2D07
8	Row	010A-4606	5EEF	DE0C	5A9F	5360
7	Row	0114-6931	C496	5B3F	F020	6348
6	Row	011E-8122	73C8	736A	F08C	0D04
5	Row	0128-2407	2D04	2B08	2FFF	C48A
4	Row	0132-5404	7F48	05FD	C4B4	4406
3	Row	013C-5469	2E63	2E4D	2F45	2F1B
2	Row	0146-8152	794A	F0FB	221D	F4D6
1	Row	0150-6EF3	2785	2265	5EDF	DD56
0	Row	015A-5ADF	5B9F	6340	63D1	C4E2
11	Row	0164-CA6D	FE77	5ECB	8180	5ECD
12	Row	016E-1CFB	C4F8	2C83	8180	817C

To check whether this card read correctly, set switches A, B, C, and D to address 4100 (8100 for 24K machine, 8100 for a 32K machine, C100 for a 48K machine), set the diagnostic control switch to SCAN STOR and the mode switch to MS DATA. Press CTRL ADR SET and then press the CPU start key. Each depression of the start key will cause the next consecutive halfword to be displayed. In this way it can be determined if the card reads correctly. A further depression of the start key should cause the remaining bootstrap cards and the control program to be read.

If the alter/display routine has not been disturbed, display the bootstrap card on the PR-KB:

1. Turn the mode switch to MS DATA (single cycle mode).
2. Press SYSTEM RESET (reset CSL).
3. Turn the mode switch to PROCESS.
4. Press PR-KB ALTER/DISPLAY.
5. Type DC 0100 on PR-KB (bootstrap card will be typed out on the PR-KB).

After the first feed cycle, the above read-in area should have all bits on in each byte. Because on the first feed cycle the card did not pass the first read brushes and nothing was read, all bits will be on (inverse logic). If all bits are not on at this time, it means not data was transferred.

2.13.3 READER CHECKS DURING CSL

If a reader check occurs during control storage load, it is not necessary to reload the whole CSL deck. Add the 5 bootstrap cards to the CSL deck prior to the card that caused the reader check and try to CSL again. In this way, it is possible to complete a CSL in increments on a reader that is giving intermittent reader checks.

2.14 CHECKSUM ROUTINE--BCHK

The checksum routine (BCHK), is entered upon completion of the resident CPU microdiagnostic (BDIA). These routines are executed whenever the CSL, system reset, or load keys are pressed.

The checksum routine performs an Exclusive OR on the contents of control storage with the exception of locations 0002-000D and 0280-02BF.

Locations 0002-000D contain the handloaded identification labels of the individual core loads. When a CSI operation is performed, an identification label is selected from this area and placed in location 0EC4 where it becomes part of the area that is subjected to the Exclusive Or result to be zero.

The handloaded labels are:

Address	Label
0002	*E60/*E61 (Model 25 mode)
0004	*E62
0006	*E63
0008	*E40 (1401/1460 mode)
000A	*E50 (1440 mode)
000C	*E20 (Model 25 mode).

2.15 INITIALIZING PROCEDURE--CHECKSUM

Effective from the microprogram level EC128226 and later, the initialization procedure should be as follows.

Checksum:

A. Do hand load as per instruction in BCPL routine.

B. CSL the emulator deck in CE mode.

C. At the completion of CSL (when the CSL light goes out), the logout should be:

1. For *E60 emulator:
EC level

8226 0E60 0BAD 0000
8226 0E60 0BAD XXXX

XXXX = (0BAD) (YYYY)

where YYYY is the checksum printed on the first page of the associated listing as well as punched in columns 21-24 of the header card (first card) of the CSL deck.

Store the checksum YYYY into location 0002 of control storage.

2. For *E40 emulator"

8226 0E60 0bad 0000
8226 0E60 0 ad XXXX
0000

Again XXXX should be the result of Exclusive ORing 0bad and YYY, where YYYY is the checksum printed on the first page of the associated listing as well as punched in columns 21-24 of the header card (first card) of the CSL deck.

Store the checksum YYYY into location 0008 of control storage.

3. For *E50 Emulator:

Same as Item 2 except that the second halfword of the first two lines of the logout should be 0E50 instead of 0E40 and the checksum YYYY should be stored in 000A instead of in 0008.

D For this procedure to be verified, the deck should be CSLed again and the following logout should occur (the same logout should occur from this point on whenever the deck is CSLed):

```
*E60 --  8226  0E60  YYYY  0000
*E40 --  8226  0e40  YYYY  0000
         0000
*E50 --  8226  0e50  YYYY  0000
         0000
```

E. If the fourth halfword of the logout in Item D is nonzero when the logout occurs:
1. After the deck is CSLed, it indicates that either the CSL deck is bad (the actual checksum of the deck is different from YYYY), or YYYY might be entered erroneously.
2. After the system reset or load button has been pressed with the XSL deck resident in core, it indicates either that the control storage has been altered or possibly a core storage failure.

2.16 SYSTEM CONFIGURATION--CSL

Nonstandard address of integrated attached devices or selector channel buffered devices:

A. For *E60 emulator:

The CSL deck contains a set of standard addresses as defined in the AAAB routine (auxiliary storage module 0 assignment map).

A system configuration card is needed only when a system is using nonstandard addresses. Such a configuration card can be punched as per instruction in the BCPL routine and inserted in the CSL deck prior to the end card (last card of the deck with blank column 3).

B. For *E40, *E50 emulator:

Refer to Appendix A - system initializer card of the SRL manual of IBM 1401/1460 and 1440 Compatibility Features, Form A24-3512.

On every EC update of the CSL decks, it is important for the systems with configuration to have the system configuration card removed from the CSL decks being replaced, and inserted into the new decks.

C. Figure 2-1 shows the I/O devices having standard addresses.

DEVICE	STANDARD ADDRESS
1443 or 1445	0B-84
2540 Reader	0C-85
2540 Punch	0D-86
1403	0E-87
1404 or 2nd 1403	0F-94
2540	15-95

Figure 2-1. Standard Address of Devices

2.17 BCPL ROUTINE

The BCPL routine is normally resident in control storage, and is used to load the initial record of either the channel or native bootstrap routines.

If the BCPI routine has been altered, the appropriate hand-load information must be entered to be sure of correct CSI operation. Switch settings for CSL:

Switches
A, B=CC CSI from channel
A, B=DD CSL from integrated 2560
A, B=EE CSI from integrated 2540
A, B=FF CSL from integrated 2311
Switches C, D set to actual unit address

2.17.1 PROCEDURE FOR PUNCHING CSL CARDS

Refer to BCPI routine in *E60 microprogram listing.

Columns
1-2 Contain starting address to be loaded.
Contains code information:
Hex 80 = Data is for program storage.
Hex 40 = Last CSL card of deck.
Hex 20 = Data is for auxiliary storage.
Hex 10 = Data is for control Storage.
4 Contains the number of halfwords to be loaded.
5-68 Contain the data.
69-72 Optional, can be used for any information.
73-77 *NNN9 (where N is core load ID).
78-80 XXX (three digit number indicating sequence of patches).

WARNING

Do not punch cards to load into auxiliary module 1, 3, 4.

2.17.2 RESTRICTIONS WHEN PUNCHING CSL CARDS

Columns
1-2 All addresses should be even:
Control Storage - These addresses should be in the range of 0000-3FFF only.
Auxiliary Storage-The 2nd hex character in column 1 should be a zero.
Program Storage - The address must be in the range of the system.
3 Coded information
4 Count Field - If a count of 0 is indicated, 257 halfwords will be loaded.
5-68 Data Field - Can be anything.
69-72 Optional - Can be used for any information. Not used by CSL.
73-77 *NNN9 (where N is core load ID; e.g., E60, 1C0, 300, etc.
78-80 XXX (three digit indicating sequence of patches).

When a full deck is being loaded with replace cards, the replace cards should go just before the end card. When loading replace cards only, it is necessary to put the control storage cards (normally 4) for module 01XX in the deck. Order of the cards is: bootstrap cards, control storage cards for module 01XX, replace cards, end card.

2.17.3 EXAMPLE OF PUNCHING AND LOADING A REPLACE CARD

Assume that the device address for the 1403 on the burst channel needed to be changed to -0A0.

The standard address for the 1403 on the burst channel is -0E- and is located in auxiliary storage module 0, at address -87-.

The card to change this would be punched in the following manner.

Column(s)		
1	(Hex 00)	This addresses module 0.
2	(Hex 86)	Although the change is for address 87, the hex address represented by column 2 must be even.
3	(Hex 20)	This indicates that information is for auxiliary storage.
4	(Hex 01)	This indicates one halfword to be loaded.
5	(Hex 0D)	This represents the device address of the 2540 punch that must be reloaded because of the addressing restriction imposed by column 2.
6	(Hex 0A)	This represents the device address replacing the standard address for the 1403 on the burst channel.
69-72	(e.g. 0086)	This indicates the beginning address of patch.
73-77	(e.g. *E609)	This indicates that patch is for *E60 core load.
78-80	(e.g. 0001)	This indicates the first patch to the deck.

A CSL must be performed to load this reconfiguration card into the system. The reconfiguration card must precede the end

card, and must be present in that position for all CSLs using that particular core load deck.

Each time a new EC level deck is received, all reconfiguration cards in the deck being replaced must be removed and inserted in front of the end card in the new deck.

2.18 METERING SWITCH (CE SWITCH)

The metering switch enables operation of one of two use meters. It is operated by a removable key. Two positions of the metering switch are:

1. Normal. Enable process meter, disable CE meter.
2. CE. Disable process meter, enable CE meter.

The 2025 console is provided with two direct-reading meter counters that record operating time: a customer meter and a customer engineer meter. The position of a key switch determines whether the customer meter or the CE meter is operating. The customer engineer holds the key for this switch, and when he is performing either scheduled or unscheduled maintenance in the PCU, he sets the switch to cause the CE meter to operate. One of these meters (determined by key switch setting) operates when:

1. The CPU clock is running and the CPU is not in the wait state, or not in the soft-stop loop.
2. The metering-in signal is up on an I/O channel.
3. Any file is selected.

The last two conditions do not cause the meter to run if the hard-stop latch is set. The meter, when started, is forced to operate for a minimum of 400 milliseconds.

The system indicator is on when either meter is running.

Note: The use-meter key switch must be in the CE position to permit any alteration of the contents of control storage.

2.19 DISPLAY OPERATIONS

Any core-storage locations can be displayed from the system control panel. The position of the mode switch specifies the source of the information to be displayed, as follows.

MS DATA	Core storage (program storage or control storage, depending upon the address being used)
AS DATA	Auxiliary storage
MOD/LS	Arithmetic modifier and local storage
ALU/EXT	Arithmetic-logic unit and external facilities
C	C-register (control register)
B/A	B-register and A-register (the inputs to ALU and core storage)
W	W-register (storage-address register backup register).

Only those data-flow components the operator needs to display are discussed. Other functions of the mode switch (C, B/A, and W) are used by the customer engineer, as is the control-storage area of main storage.

2.19.1 PROGRAM STORAGE DISPLAY

Press the stop key and wait until the manual light comes on. Set the mode switch to MS DATA. Set switches A, B, C, and D to the program-storage address to be displayed: for 16K systems, this address is from hexadecimal 0000 through 3FFF; for 24K systems, this is 0000-5FFF; for 32K systems, 0000-7FFF; and for 48K systems, 000-BFFF. Press the display key. The addressed halfword is displayed in the byte-0 and byte-1 indicators.

2.19.2 CONTROL-STORAGE DISPLAY

This procedure is identical to the display of program storage except that switches A, B, C, and D are used to address a control-storage location. For 16K systems, this is hexadecimal 4000-7FFF; for 24K or 32K systems, 8000-BFFF; and for 48K systems, C0000-FFFF.

The procedure for displaying control storage is intended only for customer engineering use.

2.19.3 AUXILIARY-STORAGE DISPLAY

Press the stop key and wait until the manual light comes on. Set the mode switch to AS DATA. Set switches A, C, and D to the auxiliary-storage address to be displayed. (Switch B is not used.) This address is from 0x00 through 7xFF for 16K systems; 0x00-5xFF and 8x00-BxFF for 24K systems; 0x00-BxFF for 32K systems, and 0x00-FxFF for 48K systems.

Normally, only the general and floating-point registers, and the MPX UCW areas of auxiliary storage, are displayed by the user.

2.20 STORE OPERATIONS

Information can be manually stored into any core-storage location. A halfword (two bytes) is always affected. If a single bytes is to be changed, the remainder of the halfword must be reentered. The store operation must be preceded by a display operation of the location to be altered.

For all store operations, the manual and the allow-manual lights must be on.

Note: Storage into a control-storage location requires that the use-meter key switch be in the CE position.

2.20.1 PROGRAM-STORAGE STORE

To alter the contents of a halfword in the program storage:

1. Set the mode switch to MS DATA.
2. Turn switches A, B, C, and D to the location to be altered.
3. Press the display key. The byte-0 and byte-1 indicators show the present contents of this halfword location.
4. Set the data halfword into switches A., B, C, and D. If only part of the halfword is to be changed, the unchanged portion must be included as part of the two bytes.
5. Press the store key. Th byte-0 and byte-1 lights indicate the new information that has been entered into the location specified in step 2.
6. Repeat steps 2 through 5 for each halfword to be changed.

2.20.2 CONTROL-STORAGE STORE

This function is identical to the program storage store procedure, except that control-storage addresses are used, the use-meter key-switch must be in the CE position, and the enable control storage store key must be pressed.

2.20.3 AUXILIARY-STORAGE STORE

To alter the contents of a halfword in auxiliary storage:

1. Set the mode switch to AS DATA.
2. Set switch A, C, and D to the address of the location. (Switch B is not used.)
3. Press the display key.
4. Enter the new data into switches A, B, C, and D.
5. Press the store key.
6. Repeat steps 2 through 5 for each halfword to be changed.

Note: Except for changes to the general and floating-point registers and for customer engineering diagnostic purposes, undisturbed after it has been initialized using the CSL procedure.

2.21 ADDRESSING, CONSOLE PRINTER-KEYBOARD

The integrated console printer-keyboard attachment is addressed as if it were connected to channel 0. The 16-bit address developed from the I/O instruction identifies the attachment and the printer-keyboard. The device address is not limited by the usual channel-0 UCW addressing requirements because the attachment has its own UCW that is not device-address dependent. In theory, the printer-keyboard may have any address from:

Binary	Hex
0000 0000	00
to	to
1111 1111	FF

In practice, the integrated PR-KB is assigned an address of 1F to standardize with other System/360 usage. This addressing makes use of one of the channel-0 subchannel addresses and prevents its use for the channel. If channel configurations require use of the subchannel, the PR-KB address can be changed by the customer engineer.

Under no condition should an address assigned to any other I/O device be assigned to the console printer-keyboard.

2.22 PROGRAM-CONTROLLED OPERATIONS

2.22.1 CHANNEL COMMANDS

Valid commands for PR-KB operations are:

Code Bits 0123 4567	Command Name
0000 0001	Write
0000 0011	No-Op
0000 0100	Sense
0000 1000	TIC
0000 1001	Write with ACR (Automatic Carrier Return)
0000 1010	Read

Any command code (issued to PR-KB) with a bit structure other than those listed, results in unit-check status (bit 6) and command reject sense (bit 0) indications.

2.23 CONSOLE PRINTER MANUAL ALTER/DISPLAY

This facility provides for altering or displaying the contents of:

- auxiliary storage
- control storage
- program storage
- print buffer (display only).

Two advantages provided by this facility are:

1. Current I/O operations (data transfers and chaining) do not overrun, as they might if alter/display operations were initiated from the system console.
2. The console printer provides a printed copy specifying the operation (alter or display), the location(s) accessed, and the data used.

2.23.1 SETUP

To initiate an alter or display operation, the operator must first press the PR-KB alter/display button (on the CPU console) and wait for the proceed light and the alter/display light to turn on. If the printer-keyboard is busy executing another operation, these lights do not turn on until that operation is ended.

When these lights turn on, the operator types a two-character sequence. Depending on the desired operation, these characters (called the operation characters) can be:

First Characters	Specifies
a	alter operation
d	display operation

Second Character	Specifies
a	auxiliary storage
c	*control storage
p	program storage
b	**print buffer

*Can be done only in CE mode.
**Display only.

2.23.2 ADDRESSING

Next, the operator must type an address for:

Area	Address Format (lowercase* hexadecimal)
auxiliary storage	xxxx
control storage	xxxx
program storage	xxxx

*Uppercase characters can be used if they do not differ from the lowercase character.

The four-digit hexadecimal address for control storage is typed as it appears on the microprogram listing; i.e., 0000 through 3FFF only.

2.23.2.1 Execution of Alter or Display

After the operation character and address have been typed, the console printer advances to the beginning of a new line.

1. For a display operation:
The keyboard is locked and printing begins starting with the contents of the specified address. After 16 hexadecimal digits (4 halfwords) have been printed, the console printer stops, the keyboard unlocks, and the proceed light turns on. At this point the operator has two choices:
   a. Successive blocks of 4 halfwords can be printed by pressing the spacebar (or any other valid character) after each block is printed.
   b. This particular pass of the alter/display routine can be terminated by pressing either the ECB key or cancel key. This causes a return to the beginning of the routine, allowing the operator to initiate another alter or display operation.

2. For an alter operation:
The keyboard is unlocked and the data to be stored can be typed immediately. However, it is good practice to first verify the address in the typed input message.

2.23.2.2 End Operation

Either the ECB key or the cancel key (in conjunction with the alternate coding key) can be used to end an alter or display operation, except when the keyboard is locked during a display printout. Pressing either key causes a return to the beginning of the alter/display routine so that the operator can perform another display or alter operation.

An alter or display operation is normally ended by pressing the ECB key after the required data has been typed. If the cancel key is used to end an alter operation, the last character is stored only if it completes a byte. (This is explained later in this section.)

An exit is not made from the alter/display routine until:
1. the ECB key or cancel key is operated to end the current alter or display operation; then
2. the CPU start key is pressed.

Therefore, the operator can perform as many alter and/or display operations as desired without exiting from the routine. Until the exit is accomplished, CPU instruction processing is stopped.

CPU instruction processing is resumed when, after an exit is made from the alter/display routine, the start key on the CPU console is pressed.

During an alter operation, data is altered on a byte basis. For example, assume that the byte data to be entered is af, but that the operator types sf instead of af. The characters sf are stored. The operator must then press either the EOB or the cancel key to return to the beginning of the routine for a retry of the entire operation.

If the error is noticed before the f is typed, the byte is not stored. If the cancel key is then operated (before the f is entered), a return to the beginning of the routine is made, and the operation can be retired if desired. In either case, the entire manual operation must be repeated to store the af. If the operator types one too many characters (such as aff for the foregoing example), the operation is not repeated.

2.24 MESSAGE FORMATS

The microprogram initiates a line feed and carrier return after sixteen halfwords have been printed on a line (for either alter or display). Data is column-justified, and blanks are provided between halfwords for either display or alter data. Also, the routine provides offsetting of two spaces at the left margin if an odd-starting address is specified for alter or display of main, auxiliary, or control storage (see following formats).

All input typing is lowercase (uppercase can be used if the uppercase character does not differ from the lowercase character). All output printing of hexadecimal alpha characters is in uppercase. In the following formats, x represents any valid hexadecimal digit.

2.24.1 ALTER STORAGE

The second operation character can be a (auxiliary), c (Control), or p (program).

Note: Valid only if in CE mode.

```
Input message:      aa xxxx
                 Address------↑

Input data:
  (odd address):      xx xxxx xx (EOB)
  (even addresses): xxxx xxxx xxxx.....xxxx
                    xxxx (EOB)          ↑
  Carrier rtn after 16th halfword-------┘
```

2.24.2 DISPLAY STORAGE

The second operation character can be a (auxiliary), c Control), or p (program).

Input message: dp xxxx
Address------↑

Output data:
(odd address): xx xxxx xxxx xxxx
(even address): xxxx xxxx xxxx xxxx

2.25 ERRORS

The error message, INVALID CHAR, is printed if any one of the following operator errors is made.

1. An operation character is other than:
First character: a or d
Second character: a, c, p, or b

2. A character other than a valid hexadecimal digit is typed for an address or input alter data.

3. A key other than EOB or cancel is operated while the alternate coding key is pressed.

A keyboard check causes a return to the beginning of the alter/display routine.

The error message, INVALID ADDR, is printed if the program, control, or auxiliary storage address is invalid for the system.

Note: Address checking is performed by the alter/display microprogram (not by storage-wrap checking circuits in the hardware).

The valid address boundaries for the various systems are as follows.

System size: 16K
Program Storage Address Range: 0000-3FFF
Control Storage Address Range*: 0000-3FFF
Auxiliary Storage Address Range: 0x00-7xFF

System Size: 24K
Program Storage Address Range: 0000-5FFF
Control Storage Address Range*: 0000-3FFF
Auxiliary Storage Address Range: 0x00-5xFF
and 8x00-BxFF

System Size: 32K
Program Storage Address Range: 0000-7FFF
Control Storage Address Range*: 0000-3FFF
Auxiliary Storage Address Range: 0x00-BxFF

System Size: 48K
Program Storage Address Range: 0000-BFFF
Control Storage Address Range*: 0000-3FFF
Auxiliary Storage Address Range: 0x00-FxFF

* The four-digit hexadecimal address for control storage is typed as it appears on the microprogram listing; i.e., 0000 through 3FFF.

The following are examples of the invalid-address error message.

1. If the address typed in the input message is invalid, the error message is printed after the console printer advances to a new line.

Input message: dp 4000
Invalid address (16K)...↑

Data: INVALID ADDR
Error message...↑

Input message: aa 8000
Invalid address (16K)...↑

Data: INVAIID ADDR
Error message...↑

2. If an invalid address is encountered during the alter or display operation (such as storage wrap), the error message begins begins on the same line with the data.

Input message: ac 3FFE
Assume 16K system.....↑

Data: xxx INVAIID ADDR

Note: First two bytes are valid. Error message applies to addresses beyond this point.

Input message: dp 3FFF

Data: xx INVALID ADDR
2 blanks for odd addr.↑

2.26 LOGOUT

The PR-KB logout is a microprogram function that prints (in hexadecimal notation) the information area of program storage. This typeout is initiated for each machine check (when the machine-check mask bit is the current PSW, bit 13, is set to 1). Problem programs are not affected by this logout. The SEREP problem program is used to interpret and print information from the logout area (refer to Figure 1-116).

Subsequent to the PR-KB logout, a System/360 machine-check interruption is initiated. Existing restart procedures and problem programs that do not act directly upon the diagnostic logout area (such as BPS, DOS, CITEP, etc.) are applicable to the Model 25 within the limits of core storage.

The program storage byte locations and contents of the diagnostic logout area are as follows.

Address Decimal)	Bit	Contents
130		Machine-check (MC) register
	0	File control check
	1	Storage protection check
	2	Storage address check
	3	Control-word parity latch
	4	Storage-data parity latch
	5	AIU error latch
	6	A-register parity latch
	7	B-register parity latch
128		Microprogram mask (MMSK) register
	0	Channel high trap
	1	2311 disk control trap
	2	Channel low trap
	3	2540 reader trap
	4	2540 punch trap
	5	Communications bit service
	6	Communications character service
	7	Level-1 priority hold
132-133		Address of control word at which the machine check occurred.
129		Branch condition (BA) register
	0	Channel-0 interrupt
	1	Mode bit 0
	2	Mode bit 1
	3	Mode bit 2
	4	IPL latch
	5	IS zone bit 0
	6	LS zone bit 1
	7	IS zone bit 2
131		Count of machine-check errors (low-order 6-bits; 2-7):
		Bits 0 1
		0 0=Machine Check
		1 1=Interface Control Check

2.27 SUGGESTED RESTART PROCEDURES FOR INTEGRATED PR-KB

An I/O error causes an interruption condition. The condition causing the interruption is indicated in the CSW (Channel Status Word). The CSW (a doublewcrd) is located in CPU main storage locations 40 through 47 (hexadecimal). Bit 38 of the CSW, when on, indicates a unit-check condition. This bit is bit 6 of the byte at main storage address 44 (hexadecimal).

When unit-check is detected by the program, a sense command should be executed for the PR-KB. Sense information sent from the attachment provides more detailed information concerning the cause of the unit-check. As a result of program analysis of the sense information, an error message should be made available to the operator to indicate the condition.

The following information describes the minimum actions that should be performed when the program detects unit-check status in the CSW.

The actions are related to particular sense indications that can occur. These bits are analyzed by the program. The choice of action(s) to be taken by the operator must be established at the installation.

2.27.1 COMMAND REJECT (SENSE BIT 0)

Provide an operator message and exit from this error-recovery procedure. Command reject occurs because of a programming error and indicates that a command not valid to the PR-KB was received at the attachment.

2.27.2 INTERVENTION REQUIRED (SENSE BIT 1)

The PR-KB enters a not-ready condition (intervention-required light on) because one of the following has occurred.

1. The not-ready key is operated. (Possible operator error).
2. The PR-KB has run out of forms.

The intervention-required light on indicates the operator should:

1. load new forms if the PR-KB is out of forms and then press the ready key, or
2. press the ready key if the PR-KB is not out of forms.

2.27.3 BUS-OUT CHECK (SENSE BIT 2)

Not used for PR-KB operations.

2.27.4 EQUIPMENT CHECK (SENSE BIT 3)

Provide an operator message to indicate failure to read the input message and do one of the following.

1. If there is no additional error recovery procedure, continue operation but consider the PR-KB inoperative.
2. If there is an additional error recovery procedure defined, exit to it. If the additional error recovery procedure fails, continue the operation but consider the PR-KB inoperative.

Equipment check is indicated for read operations only, and it indicates that bad parity was detected on a bit pattern sent from the keyboard to the CPU. The read command operation, however, is not terminated until its normal ending point, even if equipment check occurs.

2.27.5 SENSE BITS 4, 5, 6, AND 7

Not used for PR-KB operations.

2.28 EXTERNAL TO CPU FACILITIES (1052)

2.28.1 TI (1052 DATA IN)

This location is accessed by a move word with AS-decode=A. TI is set to the keyboard bit pattern when a character key is operated. The contents of TI are then moved to the A-register, in the CPU, where a parity check is made on the byte.

Bit	Name	Value	Signifies
0	UC	0	Lowercase
1	UC	0	Lowercase
0	UG	1	Uppercase
1	UC	1	Uppercase (Both 0 and 1 are set to a value of 1 for an uppercase character.)
2	KB bit B --		Bits 2 through 7
3	KB bit A --		represent the character
4	KB bit 8 --		bit pattern from the
5	KB bit 4 --		keyboard.
6	KB bit 2--		
7	KB bit 1 --		
P	KB bit C --		Bit C is set or reset to maintain odd parity.

2.28.2 TR (1052 TILT/ROTATE REGISTER)

This register can be tested (diagnostic) to determine if a correct translation from the EBCD interchange code bit pattern to the tilt/rotate code has been made. A move word with AS-DECCDE=B can be used to move TR contents to local storage where the bits can be tested. A branch word cannot be used to test TR directly.

Bit	Name	Signifies (when bit=1)
0	Tilt bit 1	Bits 0 through 7
	Tilt bit 2	are coded to cause the
2	Rotate bit 5	desired function or
3	Rotate bit 2A	tilt/rotate magnet
4	Rotate bit 2	activation.
0	Tilt bit 1	Bits 0 through 7
1	Rotate bit 5	desired function or
3	Rotate bit 2A	tilt/rotate magnet
4	Rotate bit 2	activation.
5	Rotate bit 1	
6	Uppercase Character	
7	Function Cycle	

2.28.3 TD (1052 DIAGNOSTIC BRANCH CONDITIONS)

A branch (on condition or on mask) word having an AS-decode=D can be used to test the contents of the TD-register.

Bit	Name	Signifies (when bit is on)
0	---	
1	---	
2	RD-WR Share Latch	
3	New Line Latch	
4	Key Switch On CE Mode	
5	Shift Cycle Latch	
6	Lowercase Decode	
7	Uppercase Decode	

2.28.4 TT (1052 BRANCH CONDITIONS)

A branch (on condition or on mask) word with AS-decode=E can be used to test the contents of TT. Bits in TT are set/reset by circuit conditions in the 1052.

Bit	Name	Signifies (when bit value = 1)
0	Attention	The request key has been operated.
1	Not-ready to ready	Ready key pressed and forced not-ready to ready request.
2	Intervention Required	The 1052 is out of forms or the not-ready key has been operated.
3	Alter/Display	The alter/display key on the CPU console has been operated.
4	Keyboard check	A parity check was detected on a bit pattern sent from the 1052 keyboard to the CPU A-register.
5	Alt coding key	The alternate-coding key is in its operated position.
6	1052 share request	On when the 1052 requests service for status or data transfer.
7	Logout latch	Branch bit to test if logout latch is on or off.

2.28.5 TU (1052 DIAGNOSTIC BRANCH CONDITIONS)

A branch (on condition or mask) word with AS-decode=F can be used to test the contents of TU. TU contains the bit values set into TA by the microprogram or 1052 hardware.

Bit	Name	Signifies (when bit value = 1)
0	Read latch	A read operation (command, or read portion of alter/display) is in progress.
1	Write latch	A write operation (command, write portion of alter/display, or logout) is in progress.
2	Microforce latch	On if status is queued at the 1052 attachment.
3	Alter/display active	An alter/display operation is in progress.
4	Cycle interlock latch	Output of cycle interlock latch used to check if 1052 is in the process of a print cycle.
5	Ready latch	Used to check if 1052 is in ready condition.
6	Initialize printer	On when in uppercase and initializing 1052 to lowercase.
7	Printer busy	On when 1052 is performing some operation and until ready for another operation.

2.29 CPU TO EXTERNAL FACILITIES (1052)

2.29.1 TA

A set/reset word with CS-decode=F is used to set/reset bits in TA. TA bits are set/reset to signify the conditions described for the same bits in the TU-register description. Setting bit 6 of TA causes the testable TU bit-6 condition of initialize printer. Resetting TA bit 6 causes a pulse to reset a 1052 share-request condition.

Bit 7 of TA (not testable in TU), when set, causes a force-share-request pulse; bit 7, when reset, causes a reset of the attention latch.

Bit 5 is set to indicate that the TA diagnostic singleshot is set. Bit 5 is reset when the TA attachment is reset (normally under diagnostic control).

2.29.2 TE (1052 DATA OUT)

A move word with AS-decode=F can be used to set a bit pattern in this register. TE (an 8-bit register) is set with the EBCDIC bit pattern from the CPU during a print operation.

Section 1B. 1403 Procedures

2.30 ADDRESSING, 1403 PRINTER ATTACHMENT

The one-byte unit address of the 1403 used with the printer attachment control is set into auxiliary storage by the CSL routine. This address is used to select the printer prior to each command.

The integrated 1403 is normally addressed 0E for compatibility with other System/360 usage. This permits the maximum interchange of programs when required. This addressing makes use of one of the channel-0 subchannel addresses and prevents its use for the channel. If channel configurations require the use of the subchannel, the 1403 address can be changed by the customer engineer to any address between 00 and FF that is not used by another channel-0 device. The integrated 1403 has its own subchannel (UCW) that is not dependent on the address assignment.

2.31 COMMANDS, 1403 PRINTER ATTACHMENT

The following commands are for a write operation with various carriage functions.

Command Byte 0 1 2 3 4 5 6 7	Function
0 0 0 0 0 0 0 1	Write and No Space After Print
0 0 0 0 1 0 0 1	Write and Space 1 Line After Print
0 0 0 1 0 0 0 1	Write and Space 2 Lines After Print
0 0 0 1	Write and Space 3 Lines After Print
1 0 0 0 1 0 0 1	Write and Skip to Channel 1 After Print
1 0 0 1 0 0 0 1	Write and Skip to Channel 2 After Print
1 0 0 1 1 0 0 1	Write and Skip to Channel 3 After Print
1 0 1 0 0 0 0 1	Write and Skip to Channel 4 After Print
1 0 1 0 1 0 0 1	Write and Skip to Channel 5 After Print
1 0 1 1 0 0 0 1	Write and Skip to Channel 6 After Print
1 0 1 1 1 0 0 1	Write and Skip to Channel 7 After Print
1 1 0 0 0 0 0 1	Write and Skip to Channel 8 After Print
1 1 0 0 1 0 0 1	Write and Skip to Channel 9 After Print
1 1 0 1 0 0 0 1	Write and Skip to Channel 10 After Print
1 1 0 1 1 0 0 1	Write and Skip to Channel 11 After Print
1 1 1 0 0 0 0 1	Write and Skip to Channel 12 After Print

The following commands are for independent carriage operations.

Command Byte 0 1 2 3 4 5 6 7	Function
0 0 0 0 1 0 1 1	Space 1 Line Immediately
0 0 0 1 0 0 1 1	Space 2 Lines Immediately
0 0 0 1 1 0 1 1	Space 3 Lines Immediately
1 0 0 0 1 0 1 1	Skip to Channel 1 Immediately
1 0 0 1 0 0 1 1	Skip to Channel 2 Immediately
1 0 0 1 1 0 1 1	Skip to Channel 3 Immediately
1 0 1 0 0 0 1 1	Skip to Channel 4 Immediately
1 0 1 0 1 0 1 1	Skip to Channel 5 Immediately
1 0 1 1 0 0 1 1	Skip to Channel 6 Immediately
1 0 1 1 1 0 1 1	Skip to Channel 7 Immediately
1 1 0 0 0 0 1 1	Skip to Channel 8 Immediately
1 1 0 0 1 0 1 1	Skip to Channel 9 Immediately
1 1 0 1 0 0 1 1	Skip to Channel 10 Immediately
1 1 0 1 1 0 1 1	Skip to Channel 11 Immediately
1 1 1 0 0 0 1 1	Skip to Channel 12 Immediately

The following commands are for operations that cause no printing or carriage motion.

Command Byte 0 1 2 3 4 5 6 7	Function
0 0 0 0 0 0 1 1	No-Op
0 1 1 1 0 0 1 1	Block Data Check*
0 1 1 1 1 0 1 1	Allow Data Check*
1 1 1 0 1 0 1 1	Gate Load*
1 1 1 1 0 0 1 1	Load MCS and Fold*
1 1 1 1 1 0 1 1	Load MCS and No Fold*
0 0 0 0 0 1 0 0	Sense

* Valid only with MCS feature.

2.32 CHECKS (1403)

Several kinds of checks are performed while the printer is operating.

2.32.1 PLB PARITY CHECK

The data bits in the data register are checked for proper parity when the data is written into the buffer. The check bits are not included in the parity check.

2.32.2 HAMMER CHECK

This check occurs if the hammer drivers and compare circuitry do not operate properly. Each of the conditions detected sets the hammer check latch. In addition, unique combinations of check bits (C1, C2, and C3) are set to indicate which error causes the hammer check. The check planes can be analyzed to help correct the error-causing condition. Listed here are the error conditions detected and the check planes that are set.

Hammer driver on but no compare--PIC, C2
Compare but hammer driver did not turn on--PIC, C1, C2
Compare with PIC already on--PLC, C1, C2, C3
Hammer driver on with PLC already on--PLC, C2, C3
No compare at last scan--PLC, C3

Any other combinations of PLC with C1, C2, or C3 indicate failures in the check circuitry. The PIC bit alone indicates proper operation.

2.32.3 COIL-PROTECT CHECK

This check occurs when a condition occurs that may cause damage to hammer coils and drivers. The +60V return to the hammer coils is opened by turning off the 60V control contactor. This contactor is controlled by a reed relay. If no check exists, the reed relay is picked and the +60V control is present.

A coil-protect check can occur for 3 reasons.

1. The hammer check circuitry detects that a hammer driver is on but should not be. This is detected for each hammer driver when printing is taking place.
2. A special current sense reed relay assembly detects that +60V control current of at least 3 amps is being drawn by the hammer coils at a time when no hammer drivers should be on. This detects any hammer coil current that occurs when no printing is taking place.
3. The special current sense reed relay assembly is checked during printing to see if the reed relay picks if a hammer driver is on. This ensures that the check as stated in item 2 is operative.

The check in item 1 can be blocked by operating the coil protect check bypass switch S3. This switch blocks setting the coil-protect check latch due to a hammer check. This switch should be used only if it has been determined that a false error is causing the check. Eliminating this check may delay detecting a coil-protect check until printing is complete. This switch causes the printer attention light on the console to light. All of the preceding checks can be prevented from dropping the +60V control by operation of the current-limit switch S4. This switch opens a short circuit across a 100-ohm resistor in the +60V line to the hammer coil returns. With this resistor in the circuit, a maximum of 600mA can be drawn through any one circuit. This limited current prevents damage to hammer coils and drivers even if they are on all of the time. A relay operated by the switch blocks the coil-protect check from dropping the +60V control.

2.32.3.1 Hammer Driver Coil--Fuses

There are four 6-amp fuses in the 2025: F30, F31, F32 and F33. Their purpose is to protect the hammer coil return wiring in the 1403 and the 1403 signal cables. Under certain power-down conditions, these fuses may blow because all of the hammer drivers may be on for up to 50 milliseconds. The power-down condition that may cause this problem is the loss of one of the logic voltages that control the addressing matrix to the hammer drivers. Another condition that may blow one or more of the fuses is a short on one of the hammer coil return lines in the 1403.

After the fuse has blown, coil protect checks occur. Print ready is off, print check is on, and the chain motor is not running because +60V CTR1 is turned off. If this condition occurs only when printing is attempted, the S3 switches should be turned on. If the coil protect check no longer occurs, one or more of the fuses is probably blown.

The power-check light is also turned on if any fuse (F30 through F35) is open. A power-down condition does not occur. The light is turned off when the open fuses are replaced. Because these fuses have ceramic cases, it is necessary to check them with a meter or test light.

2.32.4 SYNC CHECK

This check occurs when the PCC counter gets out of step with the chain or train. This is detected at home gate time, which is generated by an extra drum pulse from the chain or train, and indicates that the PCC should contain a count of hex 01 (non-MCS).

A resync circuit is used to resync the PCC automatically at MCS Home, except if a sync check could cause an improperly printed line. A reset is given to the printer-in-sync latch just before the home-gate time, unless a block-reset latch is on. The block-reset latch is set when a

print line starts and is reset by the next MCS home gate that occurs when printing is not taking place.

2.32.5 ADDITIONAL CHECKS

Additional checks such as forms check etc., occur due to conditions in the printer.

2.32.5.1 Forms Check

This light indicates paper feed trouble or that the carriage-stop key has been operated. This light must be turned off by the check-reset key before the print start key is effective.

2.32.5.2 End Of Forms

When an end-of-forms condition occurs, unit-check (status bit 6) is sent to the channel at the next initial selection. Subsequently, intervention required (sense bit 1) is sent during a sense operation. Also, the printer-ready light turns off and the printer end-of-forms light turns on when the end->-forms condition occurs.

To reset the printer, press the printer start key. The remaining lines of the form are then printed under program control. (The operator does not press the start key for each remaining line to be printed. He presses the start key only once.) Alternately, the single-cycle key can be used. In this case, one line of print occurs for each operation of the single-cycle key.

When a hole is sensed in channel 1 (either space or skip to or by channel 1) of the carriage tape, the operation is terminated with the end-of-forms light on. Therefore, you must provide a carriage tape with a hole in channel 1 for proper ending of the printing operation. If there is no hole in channel 1, printing continues even though there are no forms in the printer. (Printing does not occur for any command following one in which the channel-1 hole is sensed.)

To make the printer ready after channel 1 has been sensed, correct the end-of-forms condition and press the 1403 start or single-cycle key.

2.33 SUGGESTED RESTART PROCEDURES FOR 1403

An I/O error causes an interruption condition. The condition causing the interruption is indicated in the CSW (Channel Status Word). The CSW (a double word) is located in CPU main storage locations 40 through 47 (hexadecimal). Bit 38 of the CSW, when on, indicates a unit-check condition. This bit is bit 6 of the byte at main storage address 44 (hexadecimal).

When unit-check is detected by the program, a sense command should be executed for the 1403 that caused the unit-check. Sense information sent from the 1403 attachment provides more detailed information concerning the cause of the unit-check. As a result of program analysis of the sense information, an error message should be made available to the operator to indicate the condition. Depending on installation procedures, the error message can be printed out.

The following information describes the minimum actions that should be performed when the program detects unit-check status in the CSW.

The actions are related to particular sense indications that can occur. These bits are analyzed by the program. The choice of action(s) to be taken by the operator must be established at the installation.

2.33.1 COMMAND REJECT (SENSE BIT 0)

Provide an operator message and exit from this error recovery procedure. Command reject occurs because of a probable programming error and indicates that a command or a command sequence not valid to the 1403 was received at the 1403 attachment.

2.33.2 INTERVENTION REQUIRED (SENSE BIT 1)

The printer enters a not-ready condition (ready light off) because one of the following has occurred.

1. The 1403 stop key is pressed. (Possible operator error.)

2. A mechanical interlock, such as the print unit, is open. (Possible operator error.)

3. A forms check. When the forms-check light is on, paper feed trouble has occurred or the carriage-stop key has been pressed. The program should provide an operator message and exit from this error recovery procedure. The operator should then perform one of the following.
   a. Correct the not-ready condition, accept the record, and allow the application program to proceed without further retries of the command, or
   b. Correct the not-ready condition and

restart the program from a logical restart point. The logical restart point should be determined at the installation and specified to the operator.

4. End of forms. If an end-of-forms has occurred, the end-of-forms light is on and the ready light is off. To reset the printer, press the printer start key. The remaining lines of the form are then printed under program control. (The start key is pressed only once.)

When a hole is then sensed in channel 1 of the carriage tape (either space to, or skip to or by channel 1., the operation is terminated with the end-of-forms light on and the ready light off. Printing does not occur for the line at which the channel-1 hole is sensed. Therefore, a carriage tape with a hole punched in channel 1 should be on the carriage. If there is no hole in channel 1, printing continues even if no forms are in the printer. If no skip-to-channel-1 command is issued, lines are printed (after the last form) until the channel-1 punch is sensed.

The program should provide an operator message and exit from this error recovery procedure when the end-of-forms indication is detected. The operator should then perform a forms runout (as just described) and satisfy the requirements of the application program.

5. Sync check. This condition can occur whenever the print chain or train is out of synchronism with the print circuitry. Depending upon when the sync check occurs, one of the following conditions exists.
   a. The sync check occurred during a print operation and one line was printed.
   b. The sync check occurred during printing and two lines were printed. Provide an operator message and exit from this error recovery procedure. The operator should then:
   c. Correct the not-ready condition (press the check-reset key and then the start key) and allow the application program to proceed without further retries of the command, or
   d. Correct the not-ready condition (press the check-reset key and then the start key) and restart the program from a logical point.

6. Coil-Protect Check. A condition occurred that could cause possible damage to the print-hammer coils or hammer-driver circuits. A coil-protect check resets the printer to a not-ready condition, turns on the print check light, and turns off the power (+60V Ctrl) to the hammer coils. Depending upon when the coil-protect check occurs, one of the following conditions exists.
   a. The check occurred when no printing was in progress (no line was printed).
   b. The check occurred during a print operation (one line was printed). The line may be only partially printed.
   c. The check occurred during carriage motion. The carriage motion may not have been completed.
   Provide an operator message and edit from this error recovery procedure. The operator should then:
   d. Correct the not-ready condition (press the check-reset key and then the start key) and allow the application program to proceed without further retries of the command, or
   e. Correct the not-ready condition (press the check-reset key and then the start key) and restart the program from a logical point.

7. The single-cycle key is pressed (possible operator error).

2.33.3 BUS-OUT CHECK (SENSE BIT 2)

Not used.

2.33.4 EQUIPMENT CHECK (SENSE BIT 3)

Equipment check indicates that a program-resettable malfunction is detected in the printer controls.

Provide an operator message and exit from this error recovery procedure. The operator should then:
1. Accept the record and indicate that the application program is to proceed without further retries of the command, or
2. Cause the application program to restart from a logical point.

If the error persists, call the customer engineer.

2.33.5 DATA CHECK (SENSE BIT 4)--MCS ONLY

Data check indicates that a data character sent to the printer does not compare equally with data loaded in the MCS table. Print does not occur for the print position for which the unmatching code applies. The remainder of the line prints correctly.

Data check normally indicates improper data in the data record sent to be printed, but the MCS table may have been loaded improperly.

Provide an operator message and exit from this error recovery procedure. The operator should then:

1. Accept the record and indicate that the application program is to proceed without further retry of the command, or
2. Cause the application program to restart from a logical point.

2.33.6 SENSE BIT 5

Not used.

2.33.7 SENSE BIT 6

Not used.

2.33.8 CHANNEL 9 (SENSE BIT 7)

The carriage brushes sensed channel 9 during the previous carriage space. Accept the record and indicate that the program is to proceed without further retries of the command. Local installation practices may indicate other action to be taken.

2.34 USE METER (1403)

The use meter for the integrated 1403 printer is conditioned when the printer is ready and a write operation is performed. The meter remains conditioned until the carriage space or restore key is operated.

The use meter records time when it is conditioned and the CPU customer use meter is operating.

2.35 RESETS (INTEGRATED 1403)

A power-on reset places the integrated 1403 in a reset state; all 1403 check circuitry is reset, and the 1403 is placed in the not-ready state. A system reset places the 1403 in the same condition as a power-on reset, except that if the 1403 is ready when the system reset is given, it remains ready after the system reset is completed.

System reset should not be given while a printer operation is in progress because the results of the operation are unpredictable.

2.36 EXTERNAL TO CPU FACILITIES (1403)

2.36.1 PRI (PRINT LINE BUFFER DATA-IN)

This 8-bit register is used during diagnostic operations to provide data from the PLB to the CPU data flow.

A move word with AS-decode=B is used to move data from PRI to local storage.

2.36.2 PRT (PRINT LINE BUFFER ADDRESS REGISTER DATA-IN)

This 8-bit register is used to send PIB addresses to the CPU data flow during a diagnostic operation.

A move word with AS-decode=A is used to move the address from PRT to local storage.

2.36.3 PRS (1403 SENSE/STATUS CONDITIONS)

The AS-decode=E for a move or branch (on condition or on mask) word accessing this external facility. Bit significance is:

PRS

Bit	Name	Significance if Bit On
0	Device-end	Device-end has occurred.
1	Print ready	The printer is in the ready state.
2	Channel 9	A channel-9 punch has been sensed in the carriage tape during a space (not skip) operation.
3	Channel 12	A channel-12 hole has been sensed in the carriage tape during a space (not skip) operation.
4	Initial ready	The printer has gone from the not-ready to the ready state.
5	Hammer check	A hammer check has been detected.
6	Parity check	A parity check has been detected during a PLB readout or store.
7	Print request	Set on when device-end occurs for a command, or when the printer goes from the not-ready to the ready state, or if channel-end was queued by the channel, or if the diagnostic request gate latch is on and the printer clock is at time 7-0.

2.36.4 PRD (DIAGNOSTIC CONDITIONS)

The AS-decode=F in a move or a branch (on condition or on mask) word accesses this diagnostic external. The diagnostic conditions listed here are defined by the settings of PRB bits 0, 1, and 2. See the PRB description in the CPU to External Facilities (1403). For example, if PRB bits 0, 1, and 2=000, diagnostic decode 1 will be used when PRD is addressed.

2.36.4.1 Diagnostic Decode 1

Here, the 8-bit PRD register contains the print character counter data-in; i.e., chain position.

2.36.4.2 Diagnostic Decode 2

PRD Bit	Name	Significance if Bit On
0	Print control latch	Printing is occurring.
1	Print scan latch	If bit-0=1, this bit is turned on every time a PSS pulse occurs.
2	PSS gate latch	Set on by PSS pulses from the printer.
3	Home gate latch	Set on when home pulse is detected.
4	SS3 trigger	The operation is in subscan 3.
5	Print compare	The PCC and PIB data match.
6	Last scan latch	Print complete has occurred and the last scan (for checking) is in progress.
7	Sync check latch	The chain or train and PCC were out of synchronism at home-gate time.

2.36.4.3 Diagnostic Decode 3

PRD Bit	Name	Significance if Bit On
0	Carriage busy	An immediate carriage command is in progress.
1	Space drive	On for space or skip operations.
2	Skip drive	On for skip operations.
3	Carriage settling	The carriage is in the 15. 7 us carriage settling interval.
4	Carr brush 1	Bits 4-7 display the contents of the carriage brush register.
5	Carr brush 2	
6	Carr brush 4	
7	Carr brush 8	

2.36.4.4 Diagnostic Decode 4

PRD Bit	Name	Significance if Bit On
0	PIC	Print line complete.
1	PIB C1	Bits 1-3 indicate check
2	PLB C2	conditions as a result
3	PIB C3	of a print operation.
4	MCS mode	A chain with an MCS emitter is installed on the printer, or a train has operated the MCS switch on a 1403-N1.
5	Space extended	The output of the hammer driver being addressed is over 40V.
6	E1 emitter	The output of the magnetic emitter in the printer that indicates the carriage has moved one space.
7	Channel 1	A channel-1 punch has been sensed in he carriage tape during a carriage operation.

2.37 CPU TO EXTERNAL FACILITIES (1403)

2.37.1 PRC (CARRIAGE CONTROL REGISTER DATA-OUT)

A move word with AS-decode=D is used to set bits in PRC.

PRC Bit	Name	Significance if Bit On
0	Skip	Bits 0-4 are set to the
1	Carr Ctl 8	value of the modifier
2	Carr Ctl 4	bits in the command to
3	Carr Ctl 2	be executed. This
4	Carr Ctl 1	setup indicates to the printer the number of spaces to be spaced or the channel to which to slip.
5	Not used	---
6	---	If bits 6-7 are 11, a
7	---	printer-busy condition and an immediate carriage control operation are indicated.

K-Bit	Name and Significance if Set/Reset Bit = 1 (when K-Bit = 1)
0	Set single-cycle mode latch
1	Reset single-cycle mode latch
2	Not used
3	Set diagnostic gate latch latch
4	Reset diagnostic requires gate latch
5	Set diagnostic decode-2 latch
6	Set diagnostic decode-3 latch
7	Set diagnostic decode-4 latch. Bits 5-7 (diag decodes 2-4) are set to allow the various diagnostic modes used in the PRD external. If bits 5, 6, and 7 are all off, diagnostic mode 1 is specified. The diagnostic decode latches remain on until another PRB set word is given. If neither bit 5, 6, nor 7 is on, the diagnostic decode 1 comes on.

K-Bit	Name and Significance if Set/Reset Bit = 0 (when K-Bit = 1)
0	Not used
1	Set single-cycle clock run latch
2	Not used
3	Not used
4	Set diagnostic PSS pulse latch (set PSS gate)
5	Reset diagnostic PSS pulse latch
6	Not used
7	Not used

2.38 MCS TABLE--UTILITY PROGRAM

Utility Program Number 360P-UT-048 is available to load the table. In addition, the program gives the option of using folding and blocking data checks. Diagnostic functions are also performed to ensure that the data cards are correct.

Section 1C. 2311/DAC Procedures

2.39 ADDRESSING--2311 DISK STORAGE DRIVE

From one to four 2311 DASDs can be attached to channel 1 through a single integrated attachment. The addresses for these units consist of three parts:

- Channel address
- Control unit address
- Device address.

The channel address is always 01. The control unit address can be any address within the range of 8 through F (hex). The device address can be 0 through 3 (hex).

The DAC is limited to the control of one to four 2311 disk storage drives connected directly to the control unit interface in the CPU. No additional 2311s can be attached to the system through the channel because of the data transfer rate of the channel. The 16 address bits develcped from the I/O instruction identify the DAC and the disk drive for the operation.

The program views the disk attachment as if it is a channel with an attached control unit and disk drives. The sixteen bits of the I/O address are assigned as follows.

Channel Number (Bits 16 to 23)
01 Hex (Channel 1)

Control-Unit Number (Bits 24 to 27)
8-F Hex (Assigned at Installation)

Bit 28 set to 0 for system compatibility

Device Number (Bits 29 to 31)
000 Unit 1
001 Unit 2
010 Unit 3
011 Unit 4.

For example, a system with four 2311s with the control unit address assigned as 9 would have the following addresses:

2311	Channel Address	Control Unit and Device Address
0	01	90
1	01	91
2	01	92
3	01	93

If fewer than four 2311s are attached, the device address for each can be any value in the range 0-3, providing each has a different device address and all have the same control unit address. In the previous example, if only two 2311s were attached, the addresses could be 90 and 91, 91 and 92, or 90 and 92, etc.

In any case, two (or more) different addresses cannot be assigned to the same 2311.

The 2311 control unit address must be different than of any other device attached to channel 1 through the standard I/O interface.

2.40 OPERATION COMMANDS, DAC

Figure 2-2 lists the channel commands recognized by the DAC for control of the attached 2311 units. These commands are presented to the DAC in the first byte of each channel command word (CCW) from the processing unit. Any other command configuration except that of the transfer-in-channel command is considered invalid by the DAC.

Type	Command Name	Single Track	Multi-Track
Control	No Operation	03	--
	Recalibrate	13	--
	Restore	17	--
	Set File Mask	1F	--
	Seek	07	--
	Seek Cylinder	0B	--
	Seek Head	1B	--
	Space Count	0F	--
Sense	Sense I/O	04	--
Read	Read Home Address	1A	9A
	Read Count	16	92
	Read Record Zero	16	96
	Read Data	06	86
	Read Key and Data	0E	8E
	Read Count, Key and Data	1E	9E
	Read IPL	02	--
Write	Write Home Address	19	--
	Write R0	15	--
	Write Count, Key and Data	1D	--
	Erase	11	--
	Write Data	05	--
	Write Key and Data	0D	--
Search	Search Home Address Equal	39	B9
	Search ID Equal	31	B1
	Search ID High	51	D1
	Search ID Equal or High	71	F1
	Search Key Equal	29	A9
	Search Key High	49	C9
	Search Key Equal or High	69	E9
	*Search Key and Data Equal	2D	AD
	*Search Key and Data High	4D	CD
	*Search Key and Data Equal or High	6D	ED

*Used with File Scan feature (standard).

Figure 2-2. DAC Commands

The commands are chained to execute the desired sequence of events. The transfer-in-channel command (Figure 2-3) is

used to repeat search commands until the desired area is located. A read or write command is then given for the desired data. Each of the channel commands is acted upon in the same manner as a control unit connected to a System/360 channel. The usual status is returned after initialization and at the completion of the command. Sense information is developed for unusual conditions and is available through the sense command. A parity error that occurs during the transfer of the CCW causes a machine check.

TIC Command Code		
Decimal	Hexadecimal	Binary
X8	X8	XXXX1000
Positions Marked "XX" Are Ignored		

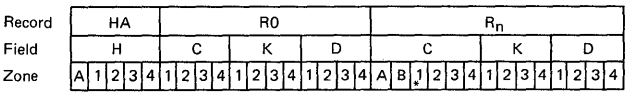
Figure 2-3. Operation Code for TIC Command

2.41 SENSE CONDITIONS, DAC

Six bytes of sense-conditions information are provided by the DAC to completely identify the setting of unit-check. These six bytes are transferred to the system by issuing a sense command (Figure 2-4).

2.42 TRACK ORIENTATION

Figure 2-5 shows the relationship of the fields and zones to the track format and Figure 2-6 shows the initializing states of fields and zones and the command sequences required to perform a data command.



Field	Definition
H	Home-address area (including gaps)
C	Count area (including gaps)
K	Key area (including gaps)
D	Data area (including gaps)

Zone	Definition
1	Pre-record gap (including address marker)
2	Record
3	Cyclic code
4	Post-record gap
A	Constant gap of 12-ones bytes in the count field, or 28 all-zeros bytes in the home-address field.
B	The 4.9% variable gap between records.

Notes: The index point immediately precedes the home-address area.
* Location of the address marker.

Figure 2-5. Track Orientation

	Sense Byte 0	Sense Byte 1	Sense Byte 2	Sense Byte 3
Bit 0	Command Reject	Data Check in Count Field	Unsafe	Ready
Bit 1	Intervention Required	Track Overrun		On Line
Bit 2		End-of-Cylinder		Unsafe
Bit 3	Equipment Check	Invalid Sequence	Selected Status	
Bit 4	Data Check	No Record Found	Cyclic-Code Check	On Line
Bit 5	Overrun	File Protected	Unselected File Status	End of Cylinder
Bit 6	Track-Condition Check	Missing Address Marker		
Bit 7	Seek Check			Seek Incomplete

Figure 2-4. Sense-Byte Summary (DAC)

Command	Command Sequence	Initial Field and Zone State	Field and Zone State at End of Command
Read Count, Key and Data	None	C1	D4
Read Key and Data	None	C1	D4
	After Search ID	C4	D4
Read Data	None	C1	D4
	After Search ID	C4	D4
	After Search Key	K4	D4
Write Count, Key and Data	Search Equal ID	C4	D4
	Search Equal Key	K4	D4
	Write R0	D4	D4
	Write Count, Key and Ddata	D4	D4
Write Key and Data	Search Equal ID	C4	D4
Write Data	Search Equal ID	C4	D4
	Search Equal Key	K4	D4
Search ID	None	C1	C4
Search Key	None	C1	K4
	After Read or Search ID	C4	K4
Search Key and Data	None	C1	D4
	After Read or Search ID	C4	D4
Search Home Address	None	HA	H4
Read R0	None	HA	D4
	After Read or Search Home Addrs	H4	D4
Write R0	Write Home Address	H4	D4
	Search Equal Home Address	H4	D4
Read Home Address	None	HA	H4
Write Home Address	None	HA	H4
Read Initial Program Load	None	C1	D4
Read Count	None	C1	C4
Erase	Search Equal ID	C4	D4
	Search Equal Key	K4	D4
	Write R0	D4	D4
	Write Count, Key and Data	D4	D4
No Operation	None	Reset Condition	

Figure 2-6. Track Orientation Field and Zone State Summary

2.43 TRACK INITIALIZATION (DEFECTIVE-TRACK DETERMINATION)

The following procedure must be followed by track-initialization programs for the IBM 2311 files. This procedure is intended to write home addresses on each track and to analyze the condition of the recording surface. The program should be written to handle the tracks in cylinder mode to reduce running time.

1. Read home address. Verify that the track has not been previously flagged. This step must be bypassed by operator action when initializing the recording surface for the first time. Unless specifically optioned by the operator, no program should change the flagging of a previously flagged alternate or defective track.

2. Write home address and record zero (R0) with a maximum-length data field on all tracks. The data pattern should be hexadecimal 55.

3. Read home address and R0 of each track to ensure that the data can be recovered successfully. If an error occurs, go to step 7.

4. Repeat step 2, using a data pattern of hexadecimal 00.

5. Repeat step 3. If an error occurs, go to step 7.

6. Rewrite home address and a standard length record 0 on all good tracks. Read and verify that these records can be recovered successfully. If an error occurs, go the step 7. The surface analysis is now complete.

7. When an error occurs, an analysis of the sense information must be made. If the error is a data-check in the count

field an/or a data-check, an attempt is made to reread the home address and R0 ten times on the track in question. If a data check (also includes a count-field data check) occurs a second time on the track, the track must be flagged as defective. Tc tc step 8. Other errors should be handled as defined in Section 2.44. If all ten rereads are successful, return to the program at point of exit.

8. Assign an alternate track.

9. Write home address and R0 on the defective track. Set the hcme-address flag byte to hexadecimal 02. The home address is the physical address of the defective track. The R0 count field contains the address of the alternate track. The content and length of the data-field length (DL) should be kept to a minimum (but greater than zero) to avoid spanning the track defect. No other records should be written on the track.

10. Read-check the home address and R0. If a data check (also includes a count-field data check) or missing address marker and no-record found errors occur, go to step 14. Other errors should be handled as in Section 2.44, Error Recovery Procedure, DAC.

11. Seek the alternate track.

12. Write home address and record zero cn the alternate track. Set the home-address flag byte to hexadecimal 01. This home address is the physical address of the alternate track. The R0 count field normally contains the address of the original defective track. Surface analysis must be completed on the alternate track candidates before they can be assigned as alternates.

13. Continue initialization on next track.

14. Track flogging requires a perfect recording surface from the index point to the end of record zero. If attempts to write home address and R0 indicate that this area is defective, the recording medium (disk pack) must be repaired.

The basic requirement is cne pass through the test (steps 2-5). An option should be provided to increase the number of tests to 255.

Additional requirements for programs that write the home address and R0 area (and in particular, Surface Analysis, Diagnostic, and other track utility programs such as UT069, UT098, and DASDI) are as follows.

1. Unless specifically optioned by action of the operator, no program should change the flagging of a previously flagged alternate or defective track.

2. Specific action by an operator should be required to unflag a track.

3. Provision must be made to flag or unflag individual or groups of tracks.

4. Operating programs that have provisions for dynamically flagging tracks must perform the 14 steps given previously.

2.44 ERROR RECOVERY PROCEDURES, 2311 DAC

2.44.1 ERROR MESSAGES, 2311 DAC

The following two error messages should be included in the operating environment of all DAC users.

Message 1 (should be printed on all uncorrectable errors).
a. Message code
b. Error type-read, write, or control
c. Unit designation, cell number, cylinder number, head number and head position; i.e., device addresses and seek address.
d. Channel designation
e. Status and sense bytes sent to CPU

Message 2 (should be printed periodically, upon completion of a run, or in response to operator request).
a. Unit designation
b. Number of entries into error routine
c. Number of uncorrectable errors.

2.44.2 ERROR CONDITIONS TABIE, 2311 DAC

This section gives the recommended corrective action for the error conditions that may occur when using IBM 2311 units attached to the System/360 Model 25 through the disk attachment control The recovery procedures are listed in the Action column. These are given in detail following the Error Condition Table (Figure 2-7).

Sense Bit and Name	Explanation	Error Type	Action
Byte 0, bit 0 (Command Reject)	The DAC has received an invalid command code.	Program error	1
Byte 0, bit 0 (Command Reject) and byte 0, bit 7 (Seek Check)	The DAC has received an invalid seek address.	Program error	1
Byte 0, bit 0 (Command Reject) byte 1, bit 3 (Invalid Sequence)	The DAC has received an invalid sequence of commands.	Program error	1
Byte 0, bit 0 (Command Reject) and byte 1, bit 5 (File Protected)	The DAC has received a command that violates the Inhibit Write portion of the File Mask.	Program error	1
Byte 0, bit 1 (Intervention Required)	The specified 2311 unit is: 1. Not on line, or 2. Not available for use due to cover interlock open, file motor off, etc.	Equipment error	2
Byte 0, bit 3 (Equipment check) and	An unusual condition has been detected in the DAC or the file unit. The condition is indicated by sense-byte 2.	Equipment error	2
Byte 2, bit 0 (Unsafe) or	A file malfunction has been detected.		
Byte 2, bit 4 (Cyclic Code Check) or	Circuitry used to generate the cyclic-code check did not function properly.		
Byte 2, bit 3 (Selected Status) or	Microprogram decode of the status byte yielded self-contradictory results.		
Byte 2, bit 5 (Unselected Status)	The status line from the files is on, but no file has been selected.		
Byte 0, bit 4 (Data Check)	The DAC has detected an error in the data field received from the file.	Equipment error	8
Byte 1, bit 6 (Missing Address Marker)	The DAC has received: 1. Two index points without an intervening address marker, or 2. Two successive count fields with equal bit conditions in bit 0 of the flag bytes.	Equipment error	5
Byte 0, bit 5 (Overrun)	The DAC access to main storage was suppressed longer than one byte time on the 2311, or a chained CCW was received too late to be properly executed.	Equipment error	3
Byte 0, bit 6 (Track Condition Check)	1. A Search, Read, or Write command was attempted on a flagged defective track (track-condition bit 6 was set to 1). Exceptions: HA and R0 operations. 2. Command chaining and multitrack code signals indicate that operations from an alternate track are to continue on the next higher-order track.	Program error	6
Byte 0, bit 7 (Seek Check)	The 2311 has been unable to complete the Seek because: 1. The access mechanism failed to reposition properly, or 2. The home-address-compare failed after automatic head switching on a multitrack operation	Equipment error	4
Byte 1, bit 0 (Data Check in count Field) and byte 0, bit 4, (Data Check)	The DAC has detected an error in the count field received from the 2311.	Equipment error	8
Byte 1, bit 1 (Track Overrun)	The index point was detected before writing was completed	Program error	1
Byte 1, bit 2 (End of Cylinder)	An end-of-cylinder was detected before the CCW command chain was completed while in multitrack mode.	Program error	1
Byte 1, bit 4 (No Record Found) and not byte 1, bit 6 (missing address marker)	Two index points were detected while executing a chain of CCWs with no intervening Read or Write operation on the data field of any record, or Read HA or Read R0 CCW. Note: This could be an expected condition on Search command chains.	Program error or equipment error	7
Byte 1, bit 5 (File Protect)	The DAC has received a Seek, a multitrack Read, or multitrack search that violated the Seek File Mask.	Program error	1
Byte 1, bit 4 (No Record Found) and byte 1, bit 6 (Missing Address Marker)	Home address or R0 cannot be found on the track.	Equipment error	9

Figure 2-7. Error Condition Table 2311/DAC (Part 1 of 2)

Action	Recovery Procedure
1	Exit with Program Error indication.
2	Repeat original sequence once. If the error condition still occurs, print Message 1 for the operator and/or customer engineer notification. This is considered an uncorrectable error; the recovery procedure depends on the application.
3	Repeat the original sequence ten times if the error persists. After ten unsuccessful retries, print Message 1 for the operator and/or CE notification.
4	Issue a Recalibrate command. Seek to the original address. Repeat the original sequence ten times if the error persists. Print Mesaage 1 and exit with the error indication.
5	Repeat the original sequence ten times if the error persists. After ten unsuccessful retries, the error is said to be "hard". At this point, the hard-error recovery procedure may be employed at the user's option. Print Mesasge 1 and exit with the error indication and option information.
6	If this is an alternate track, use the defective-track address, plus 1, in the Seek command. (This is found in the ID field of the R0 count area.) Resume the operation after searching to the desired track position. If this is a defective track, use the alternate-track address in the Seek command. (This is found in the ID field of the R0 record.) Resume the operation after searching to the desired track position.
7	Issue a Read Home Address command to verify that the correct track has been reached. (Correct cylinder is sufficient on multitrack operation.) If the correct cylinder (and/or track) is found, perform Action 1. If the incorrect cylinder (and/or track) is found, perform Action 4.
8	Repeat the original sequence sixteen times if the error persists. After sixteen unsuccessful retries, issue instructions to Recalibrate, and then Seek to the original cylinder. Repeat first two steps sixteen times if the error persists. After sixteen unsucceesful retries of second step (a total of 256 entries for the data), the data-error is said to be "hard". At this point, the hard-error recovery operations may be employed at the user.s operation. Print Message 1 and exit with the data-error indication and option information.
9	Issue a Recalibrate and then a Seek to the original address. Repeat the operation that failed. Repeat the first two steps twice if the error persists. Issue a Read HA to a different track in some cylinder. If the Read HA is successful, return to the original track and perform Action 3. If the Read HA is unsuccessful after two tries and causes the same error indication, print Message 1 for operator and/or CE notification.

Figure 2-7. Error Conditicn Table 2311/DAC (Part 2 of 2)

2.45 ADDRESSING, INTEGRATED 2540 ATTACHMENT

The integrated 2540 attachment is addressed as if it were connected to channel 0. The sixteen-bit address developed from the I/O instruction identifies the attachment and the reader or punch unit. The device address is not limited by usual channel-0 UCW addressing requirements because the attachment has its own UCWs that are not device address dependent. In theory, the attachment may have any address from:

Binary	Hex
0000 0000	00
to	to
1111 1111	FF

In practice, the integrated 2540 is assigned an address of 0C for the reader and 0D for the punch, to standardize with other System/360 usage. This addressing makes use of two of the channel-0 subchannel addresses and prevents their use for the channel. If the channel configurations require the use of the subchannels, the 2540 addresses can be changed by the customer engineer.

Under no condition should an address assigned to any other I/O device be assigned to either the 2540 reader or punch.

2.46 ERROR RECOVERY ROUTINE--INTEGRATED PUNCH

This procedure is included at the beginning of the Native Punch Trap Routine (ETRP).

For examining punch-check problems, the following procedure can be followed.

1. SAR delay stop at the address labeled PCH CHK in this routine.

2. When PCH CHK is detected the processor will stop with the punch attention light on.

3. Display of error logout (auxiliary storage 50F6-50FF) can be performed using 1052. The bit significance of the error logout is as follows.

AR	50F6	50F7	50F8	50FF
BIT	01234567	01234567	01234567	01234567
Col	1--8	9--16	17--24	73--80

When bit=1, that column is in error.

4. Manually clear logout area after analysis is completed.

5. The punch image for a card in error is located in auxiliary storage 400C through 4083. The format for this area starting at address 400C is 10 bytes, for the 12 row of the card, the next 10 bytes for the 11 row etc. A bit being a zero in this area designates a hole in the card.

The registers are used as follows.
GC=Trap count
V=Auxiliary storage address modification
D05=1 normal write indicator
D07=1 12-row punch

2.47 ERROR RECOVERY ROUTINE--INTEGRATED READER

The reader check logout format is as follows.

AUX ADR	10F6	10F7	10FF
BITS	01234567	01234567	01234567
COL	1 THRU 8	9 THRU 16	73 THRU 80

The format for the row form in auxiliary storage (4FA0 through 5017) is as follows. The first 10 bytes, row 9 of card; the next 10 bytes, row 8 of the cards; etc. A bit being zero signifies a punched hole.

2.48 2540 RESTARTS FROM ERROR CONDITIONS

The 2540 uses the flexible System/360 command set; therefore, different external error conditions can each require different restart procedures, depending on whether the 2540 operation is reading, punching or PFR. If the program provides some programmed message to indicate the 2540 sense conditions (such as PR-KB typeout), the operator can use this message to determine which specific restart procedure he should follow. To locate the error card for read-check and validity-check errors, the operator should be familiar with the with the type of processing used by the program; that is, whether the program is reading and stacking each card with a single command, or delaying the stacker selection until the data from the card is analyzed.

Figure 2-8 shows the various 2540 error indications and appropriate restart procedures for standard operations, and for PFR operations.

Indications	Restart Procedures
Reader Feed Stop Light (Only) Sense Bit 1--Intervention Required (Only) Note: If read check/bit 3 or validity check/bit 4 indications accompany feed stop/bit 1, follow procedure for read check or validity check.	1. Remove cards from stacker R1. 2. Open hopper joggler gate and remove cards from hopper. 3. Open covers and remove any jammed cards from read feed. Reconstruct any damaged cards. 4. With joggler gate still open, press reader start key to clear feed. 5. Remove cards just run out into stacker R1, place them and any reconstructed cards, in proper sequence, ahead of cards removed from hopper, and replace this deck in hopper or ahead of cards in file feed magazine. 6. Close joggler gate. 7. Press reader start key.
Reader Feed Stop Light Reader Check Light Sense Bit 1--Intervention Required (Only)	This combination of error indications accompanies a 2540 read clutch failure; there may be cards in stacker R1 that have not been read. Restart the job from the last checkpoint.
Read Check Light Sense Bit 3--Equipment Check (If card is read and stacked with single command.)	1. Remove cards from stacker R1. Determine (perhaps with aid from programmed message) which was last card read into processing unit, and correct any off-registration punching in it. Place this corrected card in stacker R1. 2. Open joggler gate and remove cards from hopper. 3. With joggler gate open, press reader start key to clear read feed. 4. Remove cards from stacker R1 and place them ahead of cards removed from hopper. Place this deck in hopper or ahead of cards in file feed magazine. 5. Close joggler gate. 6. Press reader start key.
Read Check Light Sense Bit 3--Equipment Check (If stacker selection is delayed.)	1. Remove cards from stacker R1. 2. Follow steps 2-6 of preceding procedure, correcting any off-registration punching in first card run out into stacker R1.
Validity Check Light Sense Bit 4--Data Check (If card is read and stacked with single command)	1. Remove cards from stacker R1. Determine (perhaps with aid from programmed message) which was last card read into processing unit (this card may be in another stacker) and correct any errors in this card. Place the corrected card in stacker R1. 2. Open joggler gate and remove cards from hopper. 3. With joggler gate open, press reader start key to clear read feed. 4. Remove cards from stacker R1 and place them ahead of cards removed from hopper. Place this deck in hopper or ahead of cards in file feed magazine. 5. Close joggler gate. 6. Press reader start key.

Figure 2-8. Restart Procedures--Standard and PFR Operation (Part 1 of 3)

Indications	Restart Procedures
Validity Check Light Sense Bit 4—Data Check (If stacker selection is delayed.)	1. Remove cards from stacker R1. 2. Open joggler gate and remove cards from hopper. 3. With joggler gate open, press start key to clear read feed. 4. Locate and correct invalid character(s) in first card in stacker R1. 5. Place corrected card ahead of cards in stacker R1. Place all cards in stacker R1 ahead of cards removed from hopper. Place this deck in hopper ahead of cards in file feed magazine. 6. Close joggler gate. 7. Press reader start key.
Punch Feed Stop Light (Only) Sense Bit 1—Intervention Required Only) (If the 2540 is not performing PFR operations.)	1. Remove cards from stacker P1. 2. Remove cards from hopper. 3. Open covers and remvoe any jammed cards from punch feed. 4. Press punch start key to clear punch feed. 5. Discard last card punched (2540 will repunch this card automatically). 6. Replace blank cards in hopper and press punch start key. Last card will be repunched automatically and 2540 enters ready status.

Figure 2-8. Restart Procedures--Standard and PFR Operation (Part 2 of 3)

Indications	Restart Procedures
Punch Feed Stop (Only) Sense Bit 1—Intervention Required (Only) (If 2540 is performing PFR operation.)	1. Remove cards from stacker P1. 2. Remove cards from hopper. 3. Open covers and remove any jammed cards from punch feed. Press punch start key to clear feed. 4. Any card removed or run out from between punch station and punch check brushes should be reconstructed, because it has been punched but not punch checked. 5. Place reconstructed cards and cards run out into stacker P1 in proper sequence ahead of cards removed from hopper, and place this deck in hopper. 6. Press punch start key. 7. Reconstruct internal data in the system as necessary to restart at the Start I/O instruction that caused the first card removed or run out to be read at the PFR station. Note: In some programs, reconstruction of internal data may not be provided for. In that case, restart the job from the last checkpoint.
Punch Check Light Sense Bit 3—Equipment Check (If 2540 is not performing PFR operation and using stacker P1.)	1. Remove cards from hopper. 2. Press punch start key to clear punch feed. 3. Remove last four cards from stacker P1. The last two cards are blank; the first two should be discarded. 4. Replace blank cards and cards removed from hopper in hopper. 5. Reconstruct internal data in the system as necessary to restart at the Start I/O instruction that caused the first card removed from stacker P1 to be punched. Note: In some programs, reconstruction of internal data may not be provided for. In that case, restart the job from the last checkpoint.
Punch Check Light Sense Bit 3—Equipment Check (If 2540 is not performing PFR operation and is not using stacker P1.)	1. Examine and correct, if necessary, error card, which is last card in stacker P1. (2540 automatically routes error cards to stacker P1.) 2. Place this card in appropriate stacker. 3. Press punch start key. 4. The 2540 will force the card following the error card into stacker P1, also. Place this card in the appropriate stacker. Note: Because the error card and the card following it are both directed to stacker P1, the program can correct a non-PFR punch check without operator intervention by repunching both cards and directing them to appropriate stackers. The operator can then discard all cards in stacker P1 at the end of the job.
Punch Check Light Sense Bit 3—Equipment Check (If 2540 is performing PFR operation.)	1. Remove cards from punch hopper. 2. Press punch start key to clear feed. 3. Remove last four cards from stacker P1. The last two cards are correct; pre-punching in the first two must be reconstructed. 4. Place the two reconstructed cards, the two correct cards, and the cards removed from the hopper, in that sequence, in the hopper. 5. Reconstruct internal data in the system as necessary to restart at the Start I/O instruction that caused the first reconstructed card to be read at the PFR station. Note: In some programs, reconstruction of internal data may not be provided for. In that case, restart the job from the last checkpoint.

Figure 2-8. Restart Procedures--Standard and PFR Operations (Part 3 of 3)

2.49 JAM REMOVAL

For a description of how card jams can be cleared from the 2540, refer to IBM 2540 Component Description and Operating Procedures, Form A21-9033.

2.50 EXTERNAL TO CPU FACILITIES (2540)

2.50.1 RP1 (READER-PUNCH DATA IN)

Bits are shifted into this register during reading from read station 1 or from the PFR brushes. A move word with AS-decode=B is used to move the contents of RP1 to auxiliary storage.

2.50.2 RP2 (READER-PUNCH DATA IN)

The same as RP1, but for the read station 2 and punch check brushes. A move word with AS-decode=A is used to move the contents of RP2 to auxiliary storage.

2.50.3 RS (READER BRANCH CONDITIONS)

A branch (on condition or on mask) word with AS-decode=D is used to test the following conditions.

Bit: 0
Name: Not gate read complete
Value: 0
Signifies: No cards in read feed, or a card is passing read station 2.

Bit: 1
Name: Reader ready
Value: 1
Signifies: The reader is in the ready state.

Bit: 2
Name: Reader unit exception gate
Value: 1
Signifies: All cards have been run out of the read feed and end-of-file is on.

Bit: 3
Name: Reader check
Value: 1
Signifies: A hole-count, shift-register, or address check occurred in the reader.

Bit: 4
Name: Reader validity check
Value: 1
Signifies: More than one punch was detected in rows 1-7 of a single card column during reading in data mode 1.

Bit: 5
Name: Reader hardware DE
Value: 1
Signifies: Device-end is set on because of either an overrun condition or a not-ready to ready transition.

Bit: 6
Name: Reader status request
Value: 1
Signifies: Set on for channel-end or device-end.

Bit: 7
Name: 1400 unit exception
Value: 0
Signifies: The last card has passed the read station 2 and end-of-file is on.

2.50.4 PS (PUNCH BRANCH CONDITIONS)

A branch (on condition or on mask) word with AS-decode=F is used to test these conditions.

Bit: 0
Name: Punch ready
Value: 1
Signifies: The punch is in the ready state.

Bit: 1
Name: Not 4-bit mod pull on
Value: 0
Signifies: A normal run-in has occurred (two feed cycles).

Bit: 2
Name: PFR unit exception gate
Value: 1
Signifies: The last card has passed the punch station and end-of-file is on.

Bit: 3
Name: Punch check
Value: 1
Signifies: A hole count, shift register, or address check occurred in the punch.

Bit: 4
Name: PFR validity
Value: 1
Signifies: More than one punch was detected in rows 1-7 of a single card column of a card read at the PFR brushes.

Bit: 5
Name: Punch hardware DE
Value: 1
Signifies: Device-end is set on because of either an overrun condition or a not-ready to ready transition.

Bit: 6
Name: Punch status request
Value: 1
Signifies: Set on for channel-end or device-end.

Bit: 7 Not used

2.50.5 RPS (READER AND PUNCH BRANCH CONDITIONS)

A branch (on condition or on mask) word with AS-decode=E is used to test these conditions.

Bit: 0
Name: Available
Value: 1
Signifies: The 2540 is on line.

Bit: 1
Name: Data available (CSL)
Value: 1
Signifies: A branch condition during a CSL operation with the reader. Indicates to the microprogram to perform the same action as that occurring during reader traps.

Bit: 2
Value: 1
Signifies: 1400 time out.

Bit: 3
Name: 2540 Pch Trap Rqst
Value: 1
Signifies: Punch trap request or stacker conditions when using microdiagnostic *500.

Bit: 4
Name: Punch brush CL
Value: 1
Signifies: Card at prepunch check brushes.

Bit: 5
Name: Punch decode D
Value: 1
Signifies: Diagnostic function. Indicates that data is being sent to the punch out of PC in single-cycle operation.

Bit: 6
Name: Reader select D
Value: 1
Signifies: Same as bit 5 but for data from the reader brushes to RP1 and RP2.

Bit: 7
Name: Punch select D
Value: 1
Signifies: Same as bit 6, but for data from PFR and punch check brushes to RP1 and RP2.

2.50.6 RPD1 (DIAGNOSTIC READER/PUNCH BRANCH CONDITIONS)

A branch (on condition or on mask) word with AS-decode=8 is used to test these conditions.

Bit: 0
Name: Tens AR A
Value: 1
Signifies: Address for brushes or punch magnets.

Bit: 1
Name: Tens AR B
Value: 1
Signifies: Same as bit 0.

Bit: 2
Name: Tens AR C
Value: 1
Signifies: Same as bit 0.

Bit: 3
Name: Tens AR D
Value: 1
Signifies: Same as bit 0.

Bit: 4
Name: Tens AR E
Value: 1
Signifies: Same as bit 0.

Bit: 5
Name: Pch Address Reg Check
Value: 1
Signifies: Address check in diag op.

Bit: 6
Name: Pch overrun check
Value: 1
Signifies: Punch overrun in diag op.

Bit: 7
Name: Pch shifting reg sync check
Value: 1
Signifies: Shift register check in diagnostic operation.

2.50.7 RPD2 (DIAGNOSTIC READER/PUNCH BRANCH CONDITIONS)

A branch (on condition or on mask) word with AS-decode=9 is used to test these conditions.

Bit: 0
Name: Unit AR A
Value: 1
Signifies: Address for brushes or punch magnets.

Bit: 1
Name: Units AR B
Value: 1
Signifies: Same as bit 0.

Bit: 2
Name: Units AR C
Value: 1
Signifies: Same as bit 0.

Bit: 3
Name: Units AR D
Value: 1
Signifies: Same as bit 0.

Bit: 4
Name: Units AR E
Value: 1
Signifies: Same as bit 0.

Bit: 5
Name: Reader address reg check
Value: 1
Signifies: Address check in diag op.

Bit: 6
Name: Reader overrun check
Value: 1
Signifies: Reader overrun in diag op.

Bit: 7
Name: Reader shift reg sync check
Value: 1
Signifies: Shift register check in diagnostic operation.

2.51 CPU TO EXTERNAL FACILITIES (2540)

The following are set on or off by means of a set/reset word in which the CS decode has the value listed.

2.5.1.1 R = K (CS DECODE = B)

Bit: 0
Name: Reader check
Value: 1
Signifies: Set on to indicate a hole-count error in reader.

Bit: 0
Name: Reader check
Value: 0
Signifies: Reset reader sense byte.

Bit: 1
Name: Read feed
Value: 1
Signifies: Signals reader to feed cards.

Bit: 2
Name: Read select stacker R2
Value: 1
Signifies: Sets up for stacker selection in R2.

Bit: 3
Name: Read select stacker R3
Value: 1
Signifies: Same as bit 2, but for stacker R3.

Bit: 4
Name: Validity check
Value: 1
Signifies: Set on when more than one hole is read from columns 1-7 of a single card column in the reader.

Bit: 5
Name: Sense set reader
Value: 1
Signifies: Sets reader-check light on if bit 0 is on.

Bit: 6
Name: Reader status latch
Value: 1
Signifies: Set at channel-end or device-end so that reader can request to present status in channel 0IB.
Value: 0
Signifies: Reset reader status and reader queued latches.

Bit: 7
Name: Reader queued
Value: 1
Signifies: Blocks attachment from sending reader status to channel 0IB (Interrupt Buffer).
Value: 0
Signifies: Reset reader device-end.

2.51.2 P = K (CS DECODE = F)

Bit: 0
Name: Punch check
Value: 1
Signifies: Set on to indicate a hole-count error in the punch; turns punch-check light on.

Bit: 0
Name: Punch check
Value: 0
Signifies: Resets punch sense byte.

Bit: 1
Name: Punch feed
Value: 1
Signifies: Signals the punch to feed cards.

Bit: 2
Name: Punch select stacker P2
Value: 1
Signifies: Sets up for stacker selection in P2.

Bit: 3
Name: Punch select stacker P3
Value: 1
Signifies: Same as bit 2, but for stacker P3.

Bit: 4
Name: PFR validity check
Value: 1
Signifies: Set on when more than one hole is read by the PFR brushes, from columns 1-7 of a single card column.

Bit: 5
Name: Punch restart gate (PFR write and feed comd)
Value: 1
Signifies: Prevents rerun-in of 3 cards; provides for normal run-in of 2 cards after a PFR write and feed command in which a feed check occurred, or a feed check and a punch check occurred simultaneously.

Bit: 6
Name: Punch status latch
Value: 1
Signifies: Set at channel-end or device-end so that punch can request to present status in channel 0IB.
Value: 0
Signifies: Reset device-end, punch status, and punch queued latches.

Bit: 7
Name: Pch queued
Value: 1
Signifies: Blocks attachment from sending punch status to channel 0IB.

2.51.3 RP = K (CS DECODE = D)

Bit: 0
Name: Unit-exception status reader accepted.
Value: 1
Signifies: Indicates to reader circuits that reader ready can be turned off (i.e., the last card has been read and stacked on an end-of-file operation and unit-exception status has then been accepted by channel 0).

Bit: 1
Name: 1400 latch
Value: 1
Signifies: Causes a delayed feed for 1400 operations. Value 0 not used.

Bit: 2
Name: Reader card interlock
Value: 1
Signifies: Set on when any command is accepted by the reader. Resets when device-end is sent, for the command, to channel 0IB.

Bit: 3
Name: Reader machine check
Value: 1
Signifies: Machine check occurred during reader trap microprogram. Value 0 not used.

Bit: 4
Name: Punch command interlock
Value: 1
Signifies: Same as bit 2, but for the punch.

Bit: 5
Name: Punch machine check
Value: 1
Signifies: Machine check occurred while microprogram was in a punch trap. Value 0 not used.

Bit: 6
Value: 1
Signifies: Reader device-end.

Bit: 7
Value: 1
Signifies: Punch device-end.

2.51.4 D = K (CS DECODE = 9)

Bit: 0
Name: R/P diagnostic latch
Value: 1
Signifies: Allows other diagnostic external lines to function.

Bit: 1
Name: R/P diagnostic singleshot
Value: 1
Signifies: Simulates reader or punch scan impulse to start read or punch (i.e., shifting into RP1 and RP2 or out of PO).

Bit: 2
Name: R/P diagnostic single cycle
Value: 1
Signifies: Allows bits to be shifted one at a time through RP1 and RP2 or PO.

Bit: 3
Name: Diagnostic reset shift reg (reset)
Value: 1
Signifies: Simulates a machine reset.

Bits: 4,5,6,7 Not used

2.51.5 PC (CARD-PUNCH DATA OUT)

Bits are set into this 8-bit register from P (punch image area of auxiliary storage). From PC the bits are then shifted out to the punch magnet latches during punching. A storage word with AS-decode=F is used to load PC from the punch-image area of auxiliary storage.

2.52 MULTIPLEXER CHANNEL DEVICE ADDRESSING

The multiplexer channel address (eight high-order bits of the 16-bit address) is 00 hex. Device addressing on the multiplexer channel depends upon how a device and its control unit operate with the channel. The Model 25 multiplexer channel has 32 subchannels, each of which is associated with an individual device address. For devices that have their own control unit self-contained, and for control units that operate two or more devices simultaneously (such as the 2821), individual subchannel addresses are assigned to each device. These addresses are designated with a 0-bit in the high-order position of the device address. All of the 32 subchannels can be assigned to individual control units using the addressing shown in Figure 2-9.

Subchannel (UCW)	Device Address Binary	Hex
0 to 31	0000 0000 to 0001 1111	00 to 1F

Figure 2-9. Subchannel Addresses

For a third class of control units that can operate two or more devices of which only one can operate at a time, a single subchannel can be used with a special addressing scheme. The first eight subchannels also can be addressed and operated as shared subchannels. In this case, the 0-bit position of the device address is set to 1. The remaining three bits of the high-order byte are used to designate the subchannel instead of the normally used three bits in the low-order byte. The bits of the low-order byte are then used to designate the device address. The comparable addresses for use of the subchannel as individual control unit and as shared control unit are shown in Figure 2-10.

In assigning device addresses, be careful that a single subchannel is not addressed by both its individual address and by its shared address. If this were to happen, the operation data in the UCW could be accessed by both device operations and result in transmission errors for both devices. In addition these addresses should not be assigned to any of the integrated I/O devices assigned to channel 0 in a manner that would prevent the use of a UCW as either individual or shared. An example of this lockout would be the addressing the 2540 Reader as 01 and the 2540 Punch as 9X. Any attempt to use either of these addresses for channel devices would result in operating either the reader or punch of the 2540. The channel UCW-1 could not be used for the channel because the 2540 is selected first. The integrated I/O devices have their own UCWs.

UCW	Individual C.U. Address Binary		Hex	Shared C.U. Address Binary		Hex
0	0000	0000	00	1000	XXXX	8X
1	0000	0001	01	1001	XXXX	9X
2	0000	0010	02	1010	XXXX	AX
3	0000	0011	03	1011	XXXX	BX
4	0000	0100	04	1100	XXXX	CX
5	0000	0101	05	1101	XXXX	DX
6	0000	0110	06	1110	XXXX	EX
7	0000	0111	07	1111	XXXX	FX

Share Bit
UCW Address Bits
Device Address

Figure 2-10. Subchannel Addresses Individual and Shared Control Unit

2.53 SELECTOR CHANNEL DEVICE ADDRESSING

The selector channel address (eight high-order bits of the 11-bit address) is 01 hex. Device addressing on the selector channel may in theory be any of the 256 possible bit combinations. The addressing is limited at two points by the integrated disk storage devices that are also assigned to channel 1 and addresses 9X (Hex). The value of X ranges from 0 to 3 for the four possible disk drives. The remaining addresses have no special significance in the processing unit, and may be assigned as required by the program for the selector channel devices.

2.54 CHANNEL AND UNIT ADDRESSING RESTRICTIONS

No more than one addressing bit structure can be assigned to a specific I/O unit. Also, the same unit address may not be assigned to two or more devices.

2.54.1 CHANNEL 1

When the BURSTCH (selector channel) core load is loaded, device addresses 00 through

FF are valid. Integrated 2311 units however, can be 0x-Fx and consume sixteen of these 256 possible address combinations.

2.54.2 CHANNEL 0 (EXCEPT 16K AND 24K SYSTEMS WITH BOTH THE MPX CHANNEL AND ICA FEATURES)

When the standard interface channel feature is installed and the BYTECH (multiplexer) core load is contained in control storage on 32K and 48K systems, the following device addresses may be used.

Device Address	Usage
00-1F	MPX Channel single-unit adapter (SUA) addresses
20-3F	Communications attachment addresses*
40-7F	Invalid (condition code 3)
80-FF	MPX channel multiple-unit adapter (MUA) addresses
00-FF	Integrated 1052, 1403, and 2540**

* If the Integrated Communications Attachment (ICA) feature is not installed, use of these addresses results in condition code 3.

** Although these integrated attachment features can use any address (00-FF), they should be assigned an address outside the ranges allocated for the MPX addressing capabilities of these facilities are not decreased.

	0	7	8	F
0	SUA 00 or MUA 8x		SUA 10	
1	SUA 01 or MUA 9x		SUA 11	
2	SUA 02 or MUA Ax		SUA 12	
3	SUA 03 or MUA Bx		SUA 13	
4	SUA 04 or MUA Cx		SUA 14	
5	SUA 05 or MUA Dx		SUA 15	
6	SUA 06 or MUA Ex		SUA 16	
7	SUA 07 or MUA Fx		SUA 17	
8	SUA 08		SUA 18	
9	SUA 09		SUA 19	
A	SUA 0A		SUA 1A	
B	SUA 0B		SUA 1B	
C	SUA 0C		SUA 1C	
D	SUA 0D		SUA 1D	
E	SUA 0E		SUA 1E	
F	SUA 0F		SUA 1F	

*(Except 16K and 24K Systems having both MPX and ICA features)

Figure 2-11. *Auxiliary Storage Module 2 (Channel)

Figure 2-11 is a map of auxiliary storage module 2 showing single-unit addresses and multiple-unit addresses (inside the figure), and the corresponding UCW addresses (figure coordinates), for systems except 16K and 24K systems having both the MPX channel and ICA features.

Eight UCWs (00-07) can be used either by SUA or MUA device addresses. Thirty-two subchannels are available (Figure 2-12).

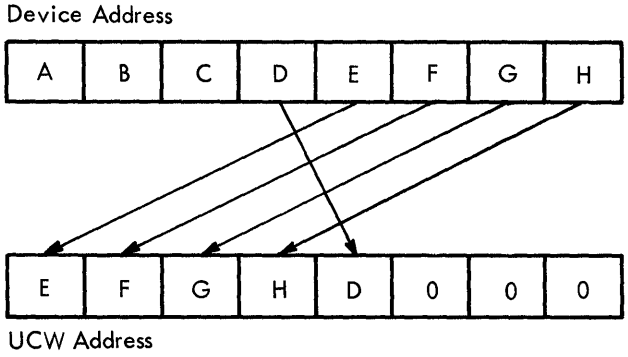
MUA Device Addrs	SUA Device Addrs	Corresponding UCW Address
8x	00	00
--	10	08
9x	01	10
--	11	18
Ax	02	20
--	12	28
Bx	03	30
--	13	38
Cx	04	40
--	14	48
Dx	05	50
--	15	58
Ex	06	60
--	16	68
Fx	07	70
--	17	78
--	08	80
--	18	88
--	09	90
--	19	98
--	0A	A0
--	1A	A8
--	0B	B0
--	1B	B8
--	0C	C0
--	1C	C8
--	0D	D0
--	1D	D8
--	0E	E0
--	1E	E8
--	0F	F0
--	1F	F8

*For all versions except the Combinational Versions of ICA and MPX Channel and 16K or 24K Program Storage

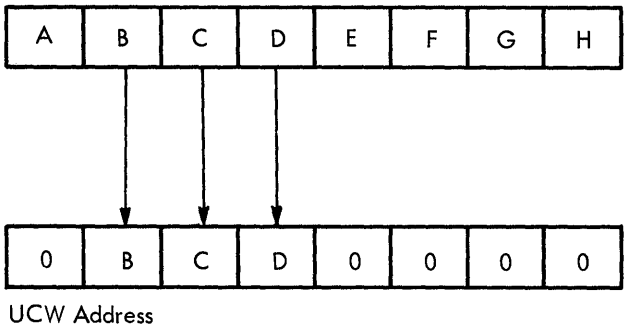
Figure 2-12. *UCW Allocations (Channel)

The device address is used to develop the UCW address (except for 16K and 24K systems having both the multiplexer channel and ICA features) as shown in Figure 2-13.

For single-unit addresses (SUA), A=0, B=0, C=0 for MPX, and C=1 for ICA:



For multiple-unit addresses (MUA), A=1, and E, F, G. and H are ignored:



* Except for 16K and 24K systems having both the multiplexer channels and ICA features.

Figure 2-13. *UCW Formulation (Channel)

2.54.3 CHANNEL 0 (16K AND 24K SYSTEMS WITH BOTH THE MPX CHANNEL AND ICA FEATURES)

When the standard interface is operated on 16K and 24K system as a multiplexer channel (BYTECH loaded), the following device addresses are used.

Device Address	Usage
00-07	Invalid*
08-0F	MPX channel SUA UCWs
10-17	Invalid
18-1F	MPX channel SUA UCWs
20-27	Communications UCWs/LCWs**
28-7F	Invalid
80-FF	MPX channel MUA UCWs
00-FF	Integrated 1052, 1403, & 2540***

* Invalid addresses cause setting of condition code 3.
** If the ICA feature is not installed, these addresses are invalid.
*** Unit addresses for these devices should not be assigned in the ranges reserved for the MPX channel or ICA feature.

Figure 2-14 gives the UCW allocations for the multiplexer channel and integrated communications feature for 11K and 24K systems having both these features. Multiple-unit addresses (80-FF) and the corresponding single-unit addresses (18-1F) are mutually exclusive. Sixteen MPX subchannels are available with this system configuration.

MUA Device Addrs	SUA Device Addrs	Corresponding UCW Address		Feature
9x	18	C0		MPX Channel
Cx	19	C8		
9X	1A	D0		
Dx	1B	D8		
Ax	1C	E0		
Ex	1D	E8		
Bx	1E	F0		
Fx	1F	F8		
--	08	40		
--	09	48		
--	0A	50		
--	0B	58		
--	0C	60		
--	0D	68		
--	0E	70		
--	0F	78		
		(UCW)	LCW	
--	20	80	00	Integr.
--	21	88	08	Comm.
--	22	90	10	Attach.
--	23	98	18	(ICA)
--	24	A0	20	
--	25	A8	28	
--	26	B0	30	
--	27	B8	38	

Figure 2-14. MPX and ICA UCW Allocations for 16K and 24K Systems

Figure 2-15 represents a map of auxiliary storage module 2 for 16K and 24K systems having both the MPX and ICA

features. It shows the SUA, MUA, and ICA device addresses and the corresponding UCW addresses.

	0	7 8 F
0	ICA	ICA
1	ICA	ICA
2	ICA	ICA
3	ICA	ICA
4	SUA 08	SUA 09
5	SUA 0A	SUA 0B
6	SUA 0C	SUA 0D
7	SUA 0E	SUA 0F
8	ICA	ICA
9	ICA	ICA
A	ICA	ICA
B	ICA	ICA
C	SUA 18 or MUA 8x	SUA 19 or MUA 9x
D	SUA 1A or MUA 8x	SUA 1B or MUA Bx
E	SUA 1C or MUA Cx	SUA 1D or MUA Dx
F	SUA 1E or MUA Ex	SUA 1F or MUA Fx

*Auxiliary storage module 2 for 16K and 24K systems with both the MPX and ICA features

Figure 2-15. *Auxiliary Storage Module 2 (Channel)

The algorithm used to build UCW addresses from device addresses for this system configuration differs from other versions, as shown in Figure 2-16.

2.54.4 ASSIGNING INTEGRATED 1052, 1403, 2311, AND 2540 DEVICE ADDRESSES

The microprogram assembler system (MAS) assigns the device addresses shown in Figure 2-17. These standard addresses are placed in fixed auxiliary storage locations by the CSI deck.

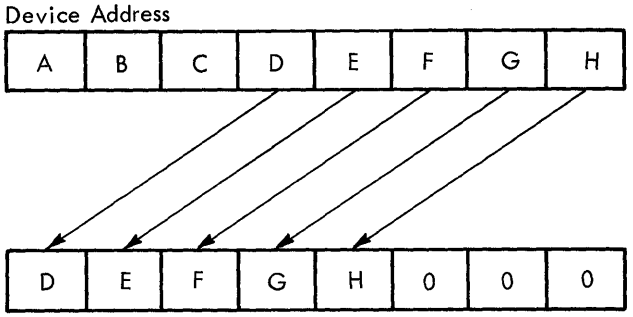
The device addresses for the integrated attachments can be anywhere within the range of 00 through FF. The address to be used for any integrated attachment can be changed by changing the contents of the auxiliary storage location specified for that device in Figure 2-19.

MAS inserts FF in the auxiliary storage location for any of these optional attachment features not selected in the particular core load.

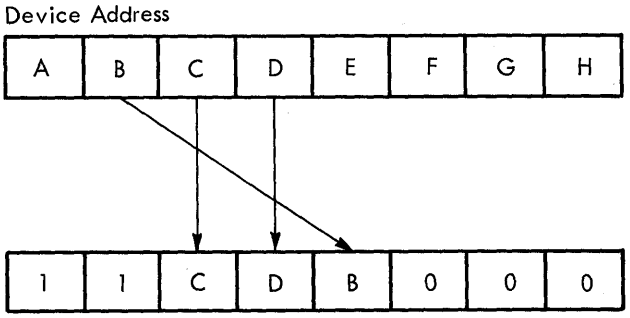
Putting FF in the auxiliary storage location for devices not included in the core load inhibits the use of FF as a device address for any device on the same channel.

If FF is desired as a valid device address, the CE or SE must replace the FF, inserted by MAS for all attachment features not included, with any unused device address. This can be done by punching a card with the beginning data address, length of data field, and data to be loaded and by inserting the card in the MAS core load deck. The detailed instructions for preparing additional CSL cards are presented at the beginning of the BCPL microprogram routine.

For single-unit addresses (SUA), A=0, B=0, C=0 for MPX, and C=1 for ICA:



For multiple-unit addresses (MUA), A=1, and E, F, G, and H are ignored:



* For 16K and 24K systems having both the MPX and ICA features.

Figure 2-16. *UCW Formulation (Channel)

		Standard Device Address	AS-Location of Device Address
Chnl 0	1052 Printer-Keyboard	1F	00B4
	2540 Reader	0C	00B5
	2540 Punch	0D	00B6
	1403 Printer	0E	00B7
Chnl 1	2311 Disk Storage Drive (control unit address)	0090	0084

Figure 2-17. Standard Integrated Attachment Device Addresses and AS-Locations

2.55 MULTIPLEXER-CHANNEL UNIT CONTROL WORDS

A UCW (unit control word) contains the information necessary to sustain an I/O operation for a device. The UCW format for Channel-0 devices operated through the standard I/O interface is shown in Figure 2-18 and Figure 1-68.

Byte					
0	1	2 and 3		4 and 5	6 and 7
Chnl Status	Flags and Op	Data Address		Cnt	Next CCW Address
		Unit Status at Interrupt	Unit Addrs at Interrupt		

Note: Fields in this figure are defined in the associated text.

Figure 2-18. Channel-0 UCW Format (Standard I/O Interface)

The number of UCWs available for devices attached to channel 0 via the standard I/O interface depends upon:
1. the program-storage size, and
2. the optional features installed on the system.

For 16K and 24K systems with both the multiplexer channel and integrated communications attachment features, 16 UCWs are available for the multiplexer channel. For all other systems, 32 UCWs are available for the multiplexer channel.

These UCWs are in addition to the UCWs allocated for the integrated 1052, 1403 2540 reader, 2540 punch, and communications lines.

The following definitions apply to the most common usage of the UCW bits (Figure 2-18). Refer to the microprogram listings for exceptions during execution of various channel microprogram routine. Unless otherwise noted, the bit value is 1.

2.55.1 CHANNEL STATUS (BYTE 0)

Bit	Meaning
0	*Secondary
1	Incorrect length
2	Program check
3	Protection Check
4	**Channel data check
5	Channel control check
6	Interface control check
7	*Interrupt in interrupt buffer

*Bits 0 and 7 indicate the following.

0 7	Indicate
0 0	Handling data, excepting data
0 1	Handling data, exception status
1 0	Status queued at I/O device
1 1	Status in IB (Interrupt Buffer)

** Channel data check can be set on only during input operations. The parity check is detected in the CPU A-register, and no machine check occurs.

2.55.2 OP-FLAG (BYTE 1)

Bit	Meaning
0	CDA (data chain in progress)
1	CC (command chain in progress)
2	SLI (Suppress Length Indication)
3	SKIP
4	PCI (Program Controlled Interruption)
5	*Active
6	**Op 1
7	**Op 2

* The active bit is on from the time that an operation is initiated at the device associated with the UCW until channel-send of the operation (i.e., such as for the last command of a command chain) has been stored in the CSW.

** Op-0 and Op-1 signify (when the active bit=1):

6 7	Indicate
0 0	Count zero (expecting channel-end)
0 1	Output command (write or control)
1 0	Read forward command (read or sense)
1 1	Read backward command (read backward)

2.55.3 DATA ADDRESS (BYTES 2 AND 3)

Two bytes are used to maintain the current data address for the command operation; any System/360 Model 25 program-storage location can be specified with a two-byte address.

When status (channel-end) is presented by the device for the operation, the unit status byte is placed in the high-order address byte location. The device address is placed in the low-order address byte location. (The data address is no longer needed at that time.)

2.55.4 COUNT (BYTES 4 AND 5)

These two bytes contain the current count for the operation.

2.55.5 NEXT CCW ADDRESS (BYTE 6 AND 7)

These two bytes contain the address of the next CCW.

2.56 SELECTOR CHANNEL CONTROL INFORMATION

The information necessary to sustain an I/O operation on the selector channel is kept either in the IS-register reserved for the channel (U, V, G, and D in zone 7) or in K-addressable auxiliary storage locations.

The channel status, op-flag byte, count, and data address are kept in the and data address are kept in the channel IS-registers.

The next CCW address is kept in K-addressable auxiliary storage because this information is needed only if command chaining or data chaining is performed.

2.56.1 CHANNEL STATUS (LS ZONE 7 REGISTER G0)

Bit	Meaning
0	Program-control interruption
1	Incorrect length
2	Program check
3	Protection check
4*	Channel data check
5	Channel control check
6	Interface control check
7**	Initial status received.

* This bit is meaningful only when the burst latch is on. When off, this bit indicates that the channel is handling data, expecting data. When on, it indicates that data transfer is complete and channel-end has been presented by the I/O device.

** Channel data check can be set on only during input operations. The parity check is detected in the CPU A-register; no machine check occurs.

2.56.2 OP FLAG (LS ZONE 7 REGISTER G1)

Bit	Meaning
0	CDA (chain data in progress)
1	CC (command chain in progress)
2	SLI (suppress length indication)
3	Skip
4	PCI (program controlled interruption)
5*	General purpose
6**	Op 1
7**	Op 2

* This bit is used to store various indications and conditions at different points in the microprogram routines.

** When the burst latch is on, the Op-1 and Op-2 bits have the following significance.

6	7	Meaning
0	0	Count zero (excepting channel end)
0	1	Output command (write or control)
1	0	Read forward command (read or sense)
1	1	Read backward command (read backward)

2.56.3 DATA ADDRESS (LS ZONE 7 REGISTER V)

Two bytes are used to maintain the correct data address for the command operation; any System/360 Model 25 program storage location can be specified with a 2-byte address.

When channel-end status is presented by the device for the operation, the unit status is placed in the high-order address-byte location (the data address is no longer needed at this time).

2.56.4 COUNT (LS ZONE 7 REGISTER U)

These two bytes contain the current data count for the operation.

2.56.5 NEXT CCW ADDRESS (AUXILIARY STORAGE LOCATION 008A)

These two bytes contain the address of the next CCW.

2.57 CHANNEL ERROR-HANDLING PHILOSOPHY AND LOGOUT

Error conditions that can be detected by the Model 25 channel interface are:

1. Incorrect Length
2. Program Check
3. Protection Check
4. Channel Data Check
5. Channel Control Check
6. Interface Control Check.

These error conditions are discussed in the System/360 Principles of Operation.

2.57.1 CHANNEL STATUS BYTE

Channel status bits, stored in the CSW for Model 25 channel operations, are defined as follows.

Incorrect Length (Bit 41): This condition is tested at channel-end time. The suppress incorrect length flag causes this indication to be suppressed.

Program Check (Bit 42): All program checks (except when the data address used exceeds the installed program storage capacity) are detected by the microprogram.

Program checks caused by attempting to address a program storage location above the installed capacity are detected by circuitry.

Protection Check (Bit 43): A circuitry test is made for this condition. In the Model 25, a protection check can occur only when data is being stored into core storage; that is, only when a read or sense is being executed.

Channel Data Check (Bit 44): This condition is detected by setting a circuitry latch whenever the bus-in is being stored or gated into local storage or core storage. If incorrect parity exists during such an operation, the channel data check bit is set on.

If the latch is set when unit status or unit address is being gated into local storage (because of incorrect parity), an interface control check is indicated. Also, see Section 2.57.2.2 for errors that apply to the integrated attachments.

Channel control checks can occur only when the CPU check control switch is in the process position. When this switch is in the disable position, the check is ignored. When in stop, a hard stop occurs in the microprogram step in which the error occurred. The appropriate error lights are turned on.

Channel Control Check (Bit 45): This error indicates that a machine check occurred during a channel-high or channel-low priority trap (MMSK bit 0 or 2 on).

Interface Control Check (Bit 46): Except as noted in the Channel Data Check section (unit status or address), this condition is detected by microprogramming.

Chaining Check (Bit 47): This indication is not used on the Model 25.

2.57.2 LOGOUT

The channel performs a logout for two types of errors:
1. Channel Control Check (logged synchronously on the 1052), and
2. Interface Control Check (logged asynchronously in main storage).

2.57.2.1 Channel Control Check Logout

The channel microprogram initiates a logout on the 1052 only on channel control checks. A channel control check is a machine check while in a channel high or low priority trap.

The logout is as follows, When a channel control check trap occurs, this routine stores into the program storage starting at hex location 80 and prints out on the PR-KB (console printer-keyboard) through the ALDP routine, the following information.

80	Trap priority register (MMSK)
81	Branch condition register (BA)
82	Machine-check register (MC)
83	Error Count
84-85	Backup Address. Address of the microword where the machine check occurred.

Trap Priority (MMSK) Register

Bit 0	Channel high pricrity trap
1	2311 Disk Control trap
2	Channel low pricrity trap
3	2540 Reader trap
4	2540 punch trap
5	Communication bit service trap
6	Communication character service trap
7	Level-1 priority hold.

Branch Condition (BA) Register

Bit 0	Channel-0 Interrupt Latch
1	Mode Bit 0
2	Mode Bit 1
3	Mode Bit 2
4	IPI Latch
5	LS Zone Bit 0
6	LS Zone Bit 1
7	LS Zone Bit 2.

Machine Check (MC) Register

Bit 0	File Control Check
1	Storage Protect Parity Check
2	Storage Address Parity Check
3	Control Word Parity Check.
4	Storage Data Parity Check
5	ALU Error Check
6	A-Register Parity Check
7	B-Register Parity Check.

Machine-check trap occurs only if the M-bit (bit 13) of the PSW is on.

Because the logout latch is set here, no CPU instruction is executed before the printout of the logout area is completed.

Any previous PR-KB operation in process, such as alter/display display, instruction step address typeout, or normal 1052 functions, are terminated.

When a machine check or channel control check is detected, MMSK bit 9 is set and remains set until the check is subsequently logged out on the 1052. If a second machine check or channel control check occurs while MMSK-9 is still on, the CPU clock is stopped with the appropriate error light on.

The flowchart in Figure 2-19 shows the channel control check operation. This check can occur only when the check control switch is set to the process position.

2.57.2.2 Interface Control Check Logout

The channel performs an asynchronous logout in main storage when an interface control check is detected by the microprogram. The following information is logged.

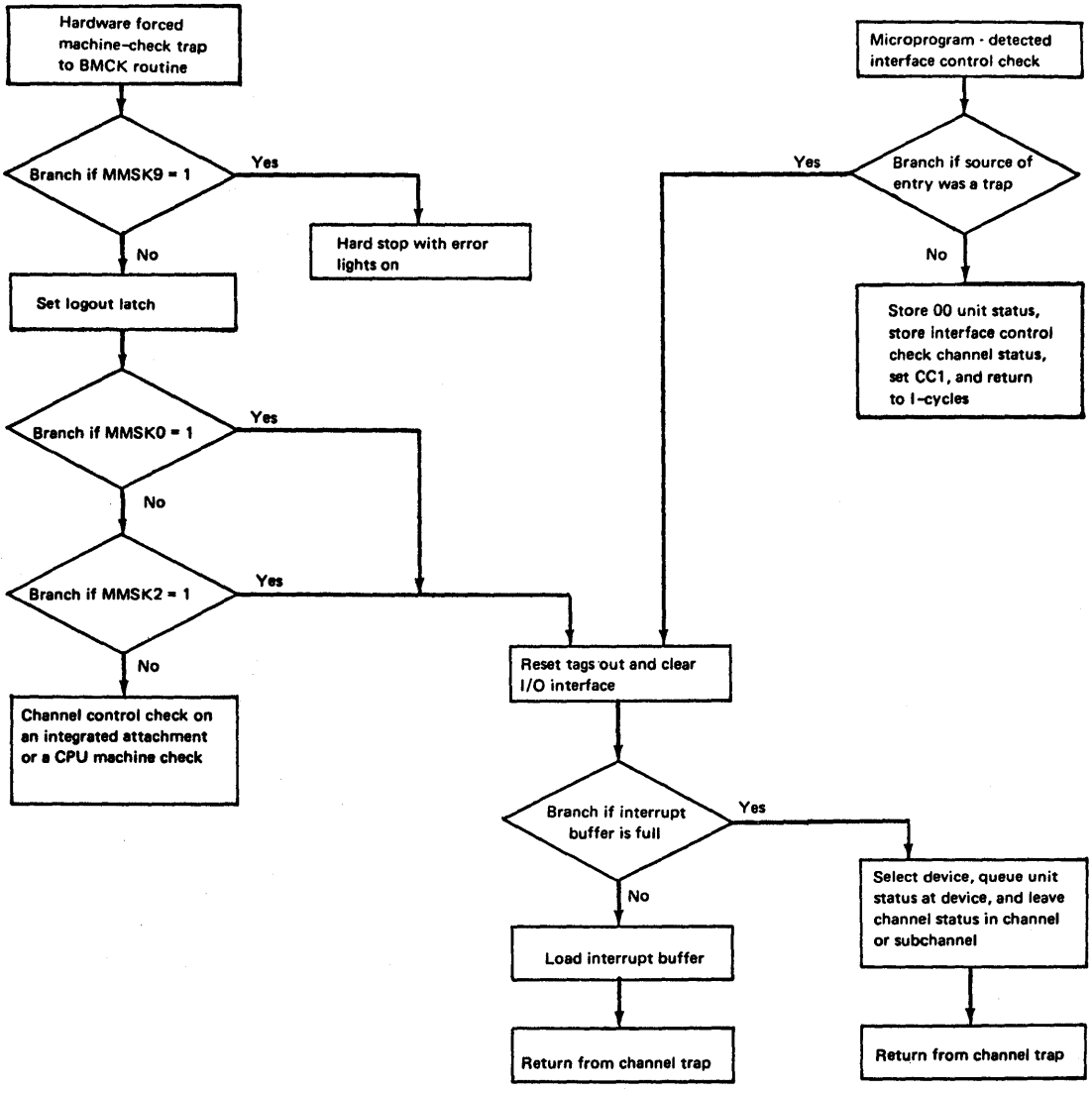


Figure 2-19. Channel Control Check Flowchart

Storage

Location	Contents
80	Trap priority register (MMSK)
81	Branch condition register (BA)
82	GS channel external conditions
83	Error count (6 Bits, 2-7; Bits 0, 1=11)
84	GT channel external conditions
85	GD channel external conditions
86-87	Unit identification halfword.

Trap Priority (MMSK) Register

Bit 0 Channel high priority trap
1 2311 Disk Control trap
2 Channel low priority trap
4 2540 Punch trap
5 Communication Bit service trap
6 Communications character service trap
7 Level-1 priority hold.

Branch Condition (BA) Register

Bit 0 Channel-0 Interrupt Latch
1 Mode Bit 0
2 Mode Bit 1
3 Mode Bit 2
4 IPI Latch
5 LS Zone Bit 0
6 LS Zone Bit 1
7 IS Bit 2.

GS Channel External Conditions

Bit 0 Data chain request
1 Buffered device latch
2 Channel-1 burst latch
3 channel parity-error latch
4 Initial selection latch
5 Channel-1 interruption latch
6 Spare
7 Suppress control latch

GT Channel External Conditions

Bit 0 Address in
1 Not select-in
2* Service-in
3* Status-in
4 Operational-in
5 Not request-in
6 Channel identification latch
7 Channel diagnostic latch

* Service-In and Status-In conditions from the interface are detectable in GT only if neither Command-Out nor Service-Out have yet been brought up in response to Service-In or Status-In.

GD Channel External Conditions

Bit 0 Operational-out
1 Service-out
2 Address-out
3 Command-out
4 Spare
5 Select-out
6 Spare
7 Suppress-out

Unit Identification Halfword

Byte 0

Bits 0 1 2	Meaning
0 0 0	Integrated 1052, 1403, or 2540
0 0 1	Multiplexer channel
0 1 X	Selector channel
1 0 0	Integrated communications attachment

If bits 0-2 indicate the MPX channel feature, bits 3-6 are used for various functions under microprogram control.

If bits 0-1 indicate the selector channel feature, bits 2-6 are used as a timeout counter for interface sequences.

Bit 7 is used to indicate whether any unit or channel status may be stored directly in a CSW, or whether the interruption must be put in the interrupt buffer and subsequently cleared by an I/O instruction or an I/O interrupt.

Byte 1, for the selector channel or multiplexer feature, contains the current device address.

GA (Channel Conditions)

A set/reset word with CS-field=B is used to set or reset bits in GA. The set/reset bit in the set/reset word is ignored whether the bits are to be set or reset. The K-bit values determine which bits are set or reset. If a K bit=1, the corresponding bit in GA is set; if a K bit=0, the corresponding bit in GA is reset.

Bit	Meaning
0	Selective reset. Drops operational-out for 6 microseconds.
1	Service-out
2	Address-out
3	Command-out
4	Initial selection (Inhibits low-priority traps during an initial selection sequence. That is, data or chaining traps for channel 0, chaining or status traps for channel 1.)
5	Select-out
6	Channel reset (diagnostic). Resets channel latches.
7	Spare

2.58 STANDARD INTERFACE HARDWARE

The standard interface hardware is identical for the multiplexer or selector versions of the channel. The function of the channel (multiplexer or selector) depends entirely upon the microprogram (BYTECH or BURSTCH).

Figure 2-20 is a summary of GA- and GB-register definitions.

		GA Register	GB Register
KH0	8	Not Op-Out (Set Only)	Data Chain Request Latch
KH1	4	Service-Out (Set/Rst)	Chnl ID Latch (Chnl 0 if 0; Chnl 1 if 1)
KH2	2	Address-Out (Set/Rst)	Burst Latch
KH3	1	Command-Out (Set/Rst)	Set Buffered Device Latch if 1; Reset Chnl Par-Error Latch if 0
KL0	8	Initial Selection (Set/Rst)	Channel Diagnostic Latch
KL1	4	Select-Out (Set/Rst)	Chnl 1 Interrupt Buffer
KL2	2	Diagnostic Chnl Reset	Not Used
KL3	1	Not Used	Suppress-Out Control

Figure 2-20. GA- and GB-Register Definitions

Note: All of the GA and GB latches may be displayed in one of the GS, GD, GT, or GB/IN channel external displays (see Figure 2-21).

Display Bit	GS=C	GT=D	GD=E
0	Data Chain Reg Latch	Addrs-In	Op-out
1	Buffered Dev Lat	Not Sel In	Serv-Out
2	Burst Lat	Serv-In	Adrs-Out
3	Chnl Par Ck Lat	Stat-In	Cmd-Out
4	Initial Selection	Op-In	Spare
5	Chnl 1 IB	Not Reg In	Sel-Out
6	Spare	Chnl ID (Sel)	Spare
7	Supp Ctrl Latch	Channel Diag Lat	Suppress Out

Figure 2-21. Display of GA and GB External Facilities

2.59 EXTERNAL TO CPU FACILITIES (CHANNEL)

2.59.1 GS (CHANNEL BRANCH CONDITIONS)

A branch (on condition or mask) word with AS-decode=C can be used to test the following conditions. Unless otherwise noted, a bit must be on (set to 1) for the meaning to be applicable.

GS

Bit	On If	Meaning
0	GB0=1	Data chain request latch
1	GB3=1	Buffered device latch
2	GB2=1	Burst latch (used only for channel 1; signifies that a burst operation is in progress).
3	-----	Channel parity-error latch. A parity error has been detected on a byte received bus in.
4	GA4=1	Initial selection latch. Blocks channel-low priority traps.
5	GB5=1	Channel-1 interruption latch (on to indicate that channel 1 has status to present to the CPU).
6	------	STP trap inhibit latch.
7	GB7=1	Suppress control latch. Indicates that a command chain is in progress and that a new CCW is being fetched by the channel.

2.59.2 GT (CHANNEL BRANCH CONDITIONS)

A branch (on condition or mask) word with AS-decode=D can be used to test the following conditions. These bits are in in-tags for the I/O interface.

GT

Bit	Meaning
0	Address-in
1	Not select-in
2*	Service-in
3*	Status-in
4	Operational-in
5	Not request-in
6	Channel identification latch
7	Channel diagnostic latch

* Service-in and Status-in conditions from the interface are detectable in GT only if neither command-out nor service-out has yet been brought up in response to service-in or status-in.

2.59.3 GD (CHANNEL DIAGNOSTIC REGISTER)

A branch (on condition or on mask) word with AS-decode=E can be used to test these bits (from channel to interface).

GD

Bit	On If	Meaning
0	GA0=0	Operational-Out
1	GA1=1	Service-Out
2	GA2=1	Address-Out
3	GA3=1	Command-Out
4	-----	Saved GB/IN Bit 1
5	GA5=1	Select-Out
6	-----	Not 1400 word separator
7	GB7=1*	Suppress-Out

* Suppress-out is also testable if the interruption buffer latch is on.

2.59.4 GB/IN (CHANNEL BUS-IN)

A branch (on condition or on mask), storage, or move word with AS-deccde=F can be used tc access these bits. Bits 0 through 7 of GB/IN correspond tc bits 0 through 7 of the interface bus-in lines.

2.60 CPU TC EXTERNAL FACILITIES (CHANNEL)

2.60.1 GB/OUT (CHANNEL BUS-OUT)

A storage or move word with AS-deccde=F can be used to set the bus-out register. This is the same decode used for the bus-in lines. The specific operation determines whether data is tc be received into the bus-in (GB/IN) from the interface, or set into the bus-out (GB/OUT) from the CPU.

2.61 HANDICAD ROUTINE FOR CHANNEL

When the BCPL Routine has been altered or destroyed and a CSL from a card reader on the channel is not possible, the handload routine as shown in Figure 2-22 must be entered.

Addr	Word	Statement	Comment
0010	3210	SET MMSK K=81	Blcck traps
0012	2610	SET BC K=01	Set logout latch
0014	2C07	P0=0	Zerc cut switch
0016	2413	G0=0$K01	Start setup of addr 0100
0018	51AF	TO=SWCD	SWCD equal device addr.
001A	802C	BR	Eranch tc location 002C
002C	2486	SET MCDE K=38	Set channel mode, PCU zcne
002E	2507	G0=0	Finish setup of addr 0100
0030	2B08	SET GA K=40	Set service out
0032	C9B3	BR IF GT4=1	Branch on OP-IN
0034	4FAF	GB/CUT=TO	Send device address out
0036	2B04	SET GA K=20	Raise address out
003,	2B44	SET GAK=24	and select out
003A	C9BA	BR IF GT4=0	Wait for OP IN
003C	2B40	SET GA K=04	Reset address out
003E	CDBE	BR IF GT0=0	Wait for address in
0040	2B23	T1=0$K02	Build read command
0042	4FBF	GB/CUT=T1	Send cut read command
0044	2B42	SET GA K=14	Raise command out
0046	FDC6	BR IF GT3=0	Wait here for status
004	5FBF	T1=GB/IN	Read status
004A	C4CA	BR IF ZNZ	Iccp here if invalid stat
004C	2B48	SET GA K=44	Set service out
004E	FDCF	BR IF GT3=1	Wait for
0050	EDCE	BR IF FT2=0	data
0052	5FFF	H1=GB/IN	Get data byte
0054	F05B	BR IF G07=1	BR if bcotstrap reading
0056	7F48	STB H1 AS, G+1	Not boot info, stor in aux
0058	F05E	BR IF G07=0	Uncenditicnal branch
005A	6F48	STB H1 CS, G/1	Put boot in cntrl storage
005C	055D	Z=G1 K50	Check if all data in,
005E	C4CC	BR IF ZNZ	if nct, get more.
0060	8100	BR	Branch to bootstrap

Figure 2-22. Handload Routine for Channel

2.62 NONOPERATIONAI IINES

All ICA lines are in a nonoperational state at shipment. If an I/O instructicn is issued to a line, a condition code of 3 (nonoperational) is set. To make the lines cperational, refer to microprogram routine GASN or the Model 25 Installation Instructions.

2.63 STATION SELECTION FEATURE

If the Station Selection feature is installed (check the front cf the microprogram listing for ADPREP), line addresses must be entered into storage via patch cards at ICPL time. Refer to microprogram routine GASN or the Model 25 Installation Instructions.

2.64 JUMPER OPTIONS

Refer to logic pages HA000 for the jumpering options associated with the ICA and related data sets and/or modems.

2.65 STORAGE PROTECT KEY--DISPLAY

Refer to Section 2.1.

2.66 MULTIPLE CHARACTER SET

This feature allows the use of print chains or trains of other than 48-character size. The printer translate table must be loaded with utility program UT048 when the MCS feature is installed.

2.67 EXTERNAL INTERRUPTION

This feature allows the Model 25 to respond to signals from an external device or another CPU. An external interruption also can occur from the interrupt key on the system control panel (standard on the Model 25) or from the interval timer (special feature). An external interruption can occur only when PSW bit 7 (system mask) is set to 1. The specific interruption sources identified by PSW bits 24-31 are as follows.

Interruption Code Bit	External Interruption Cause
24	Interval timer
25	Interrupt key
26	External signal 2
27	External signal 3
28	External signal 4
29	External signal 5
30	External signal 6
31	External signal 7

The interval-timer and interruption-key lines are available from within the CPU.

2.68 2560 PROCEDURES

2.68.1 HANDLOAD ROUTINE FOR 2560

When the BCPL routine has been altered or destroyed and a CSL from the 2540 is not possible, the handload routine as shown in Figure 2-23 must be entered manually. For bootstrap information, refer to the AKXXX logic pages.

Addr	Word	Statement	Comment
0010	3210	SET MMSK K=81	Block all traps
0012	2610	SET BC K=01	Set logout latch
0014	2C07	P0=0	Zero handload flag register
0016	2413	G0=0$K01	Build high half CS addr 0100
0018	80AC	BR	BR to 00AC
00AC	240E	SET MODE K=70	Put in mod/20, 2560 mode
00AE	2F04	SET MFA K=20	Select sec. feed (Note 1)
00B0	2507	G1=0	Low half CS addr G=0100
00B4	DAB8	BR IF MFT5=0	BR to 00B8 if NPRO req.
00B6	FD33	BR IF P12=1	BR if not ready
00B8	2F10	SET MFA K=01	Set read ex.
00BA	DAC6	BR IF MFT5=0	Check NPRO
00BC	CAB9	BR IF MFT4=1	BR on no data available
00BE	58FF	H1=MFR1	Read 1/2 byte
00C	5AEF	H0=MFR2	Read the other 1/2
00C2	4EF3	H1=H0XH-H1L	Put two 1/2 bytes together
00C4	6F48	STB H1 CS, G+1	Store them
00C6	2B14	SET MFC K=21	Rst NPRO, and rd. ex.
00C8	055D	Z=G1 K50	Check for 80 bytes
00CA	C4B4	BR IF ZNZ	If not 80, go to 00B4
00CC	8100	BR	BR to bootstrap addr 0100

Note 1: To use the primary feed, replace this word with 2F80. The start key must be pressed at the end to complete the CSL (last card).

Figure 2-23. Handload Routine for 2560

Chapter 3. Preventive Maintenance

Section 1. Basic Unit

a. Perform the following maintenance every 26 weeks:
   1. Test lamps using the lamp test key on the console. Replace lamps as necessary.
   2. Check blowers and replace filters every 26 weeks. Filters may require more frequent replacement depending on cleanliness of environment.

b. Replace coil protect relay, part 2532227, under the following conditions.
   1403 Model 2 or 7
   Every 18 months based on average usage of 2 to 2.5 million lines per month.
   1403 Model N1
   Every 12 months based on average usage of 5 to 5.5 million lines per month.

   This schedule should be adjusted proportionally for any deviation from average usage.

c. Run usage meter test every 6 months.

d. 1052-7: Refer to the Selectric I/O Keyboardless Printer FE Maintenance Manual, Form 225-3207; 1052-1053 Keyboard Printer FE Instruction-Maintenance Manual, Form 225-3179.

Section 2. Features

I/O DEVICE MAINTENANCE

Scheduled maintenance for I/O devices is included in the maintenance manual for the particular device.

Chapter 4. Checks, Adjustments, and Removals

Section 1. Basic Unit

4.1 CPU TIMING

Timing for the CPU is developed from a crystal controlled oscillator. The CPU clock is located in board position B2-C4 and D4 on the A-gate.

4.1.1 SPECIFICATIONS

1. Oscillator frequency: 5.56 MHz ± .03%.
2. T-Pulses (Figure 4-1 and 4-2):
   a. Width--180 ns +25/-10 ns, measured from the 1.2V level of the leading or rising edge to the 1.9V level of the trailing, or falling edge.
   b. Level--each pulse has a down level of 0.49V to 1.06V, and an up level of 2.68V to 3.33V.
   c. Overlap--adjacent T-pulses are overlapped by 90 ns +25/-10 ns as measured from the 1.2V level of the rising pulse to the 1.9V level of the falling pulse.
   d. Skew--the skew between T0 pulse and T2 pulse (and subsequent alternate pulses) on the transmission line is +30/-25 ns, as measured from the 1.9V level of the falling pulse to the 1.2V level of the rising pulse.
3. Clock Pulses On the Boards: (applies to nets driven by line receiver-power driver):
   a. T-pulses--(180 ns) have +20/-40 ns tolerance as measured from the 0.3 volt level of the rising pulse to the 1.8 volt level of the falling pulse.
   b. P-pulses--(90 ns) have +20/40 ns control tolerance as measured from the 0.3 volt level of the rising pulse to the 1.8 volt level of the falling pulse.

4.2 CORE STORAGE ARRAY TEMPERATURE CONTROL

4.2.1 COOLING

The BSM (Basic Storage Module) provides the SLT cards with forced air cooling with fans operating at 208-volts ac 60-cycle single phase, or 220-volts ac 50-cycle single phase.

4.2.1.1 Specification

The maximum temperature anywhere within the BSM must not exceed 133F(55C).

4.2.2 HEATING

A heater, fan, and associated control circuitry provide a wide temperature range by maintaining the core array at a fixed elevated temperature. The heater element, control circuits, temperature adjustment, and temperature sensing devices are packaged in a complete heater subassembly that is part of the BSM.

4.2.2.1 Specifications

1. The array inlet temperature must be maintained at 105±3F(40.4±1.7C).
2. The low temperature light on the console must go off when the array inlet temperature exceeds 96±5F(35.6±2.8C).
3. The thermal trip mechanism (normally closed switches) operates at over and under temperatures of 120±3F and 96±5F(49±1.7C and 35.6±2.8C).

4.2.2.2 Heater Adjustment

Do not attempt to adjust the array inlet temperature if the machine ambient temperature is greater than 95F(35C).

1. With power on, allow five minutes for warm-up.
2. Carefully insert a nonmetallic thermometer (part 5392366 or equivalent) through the array cover access hole and into the rear of the heater plenum. The thermometer should extend about 3.25 in. (82,6 mm) into the unit and the tip should be slightly downward.
3. The heater adjustment potentiometer is adjusted from the front of the heater box. Turn the potentiometer clockwise to decrease the temperature or counterclockwise to increase the temperature until a stabilized temperature of 105±3F(40.4±1.7C) is indicated. Allow about three minutes for the thermometer to record properly.
4. Remove thermometer.

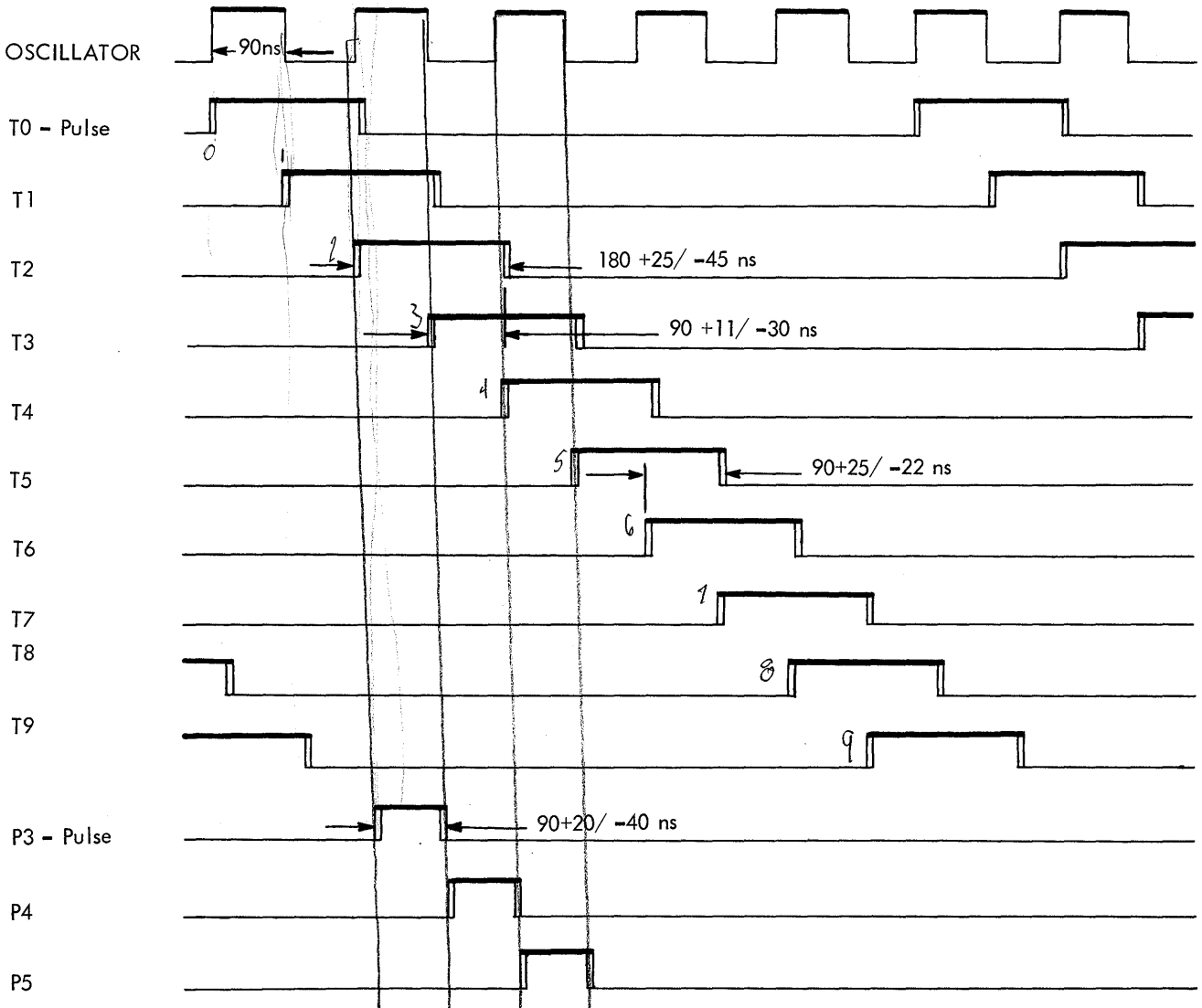


Figure 4-1. CPU Timing Pulses

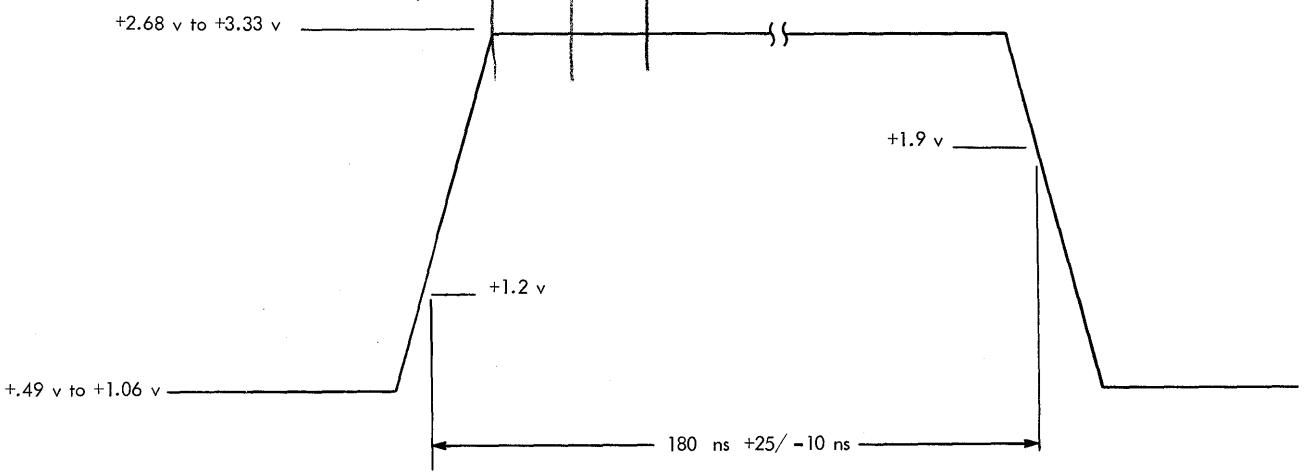


Figure 4-2. T-Pulse

4.3 SCHMOO CURVE (MAIN STORAGE)

4.3.1. EXAMPLE OF SCHMOO CURVE PROCEDURE

Figure 4-3 shows an example of a typical four-point schmoo procedure. It is used for plotting the optimum storage strobe and voltage operating point. A no-failure voltage and strobe setting is selected as a starting point. The voltage is varied over its range up and down to a point of failure, and varied from that failing point into the no-failure range (1 in Figure 4-3). The no-failure points are determined at four different strobe settings by running the worst-case patterns (Section 4.3.4.1) with the diagnostic control switch set at TEST PATTERN. Switches A, B, C, D must equal FF00, 00FF, 01FE, or, FE01.

Once the no-failure voltages have been plotted, the optimum strobe setting for a single BSM is a point where the difference between the upper and lower BSM limits is greater than 5.0 volts (2 in Figure 4-3). At a strobe setting ± 10 ns from optimum, the difference between the high and low voltage setting must be greater than 3.0 volts (3 in Figure 4-3).

For a double BSM, the difference between the upper and lower BSM limits at optimum strobe must be greater than 3.6 volts. At a strobe setting ±10 ns from optimum, the worst-case diagnostic must still run successfully. In both cases the strobe setting must be between 35 ns and 55 ns. It should be the earliest setting that will meet requirements, and 35 ns should be used if possible.

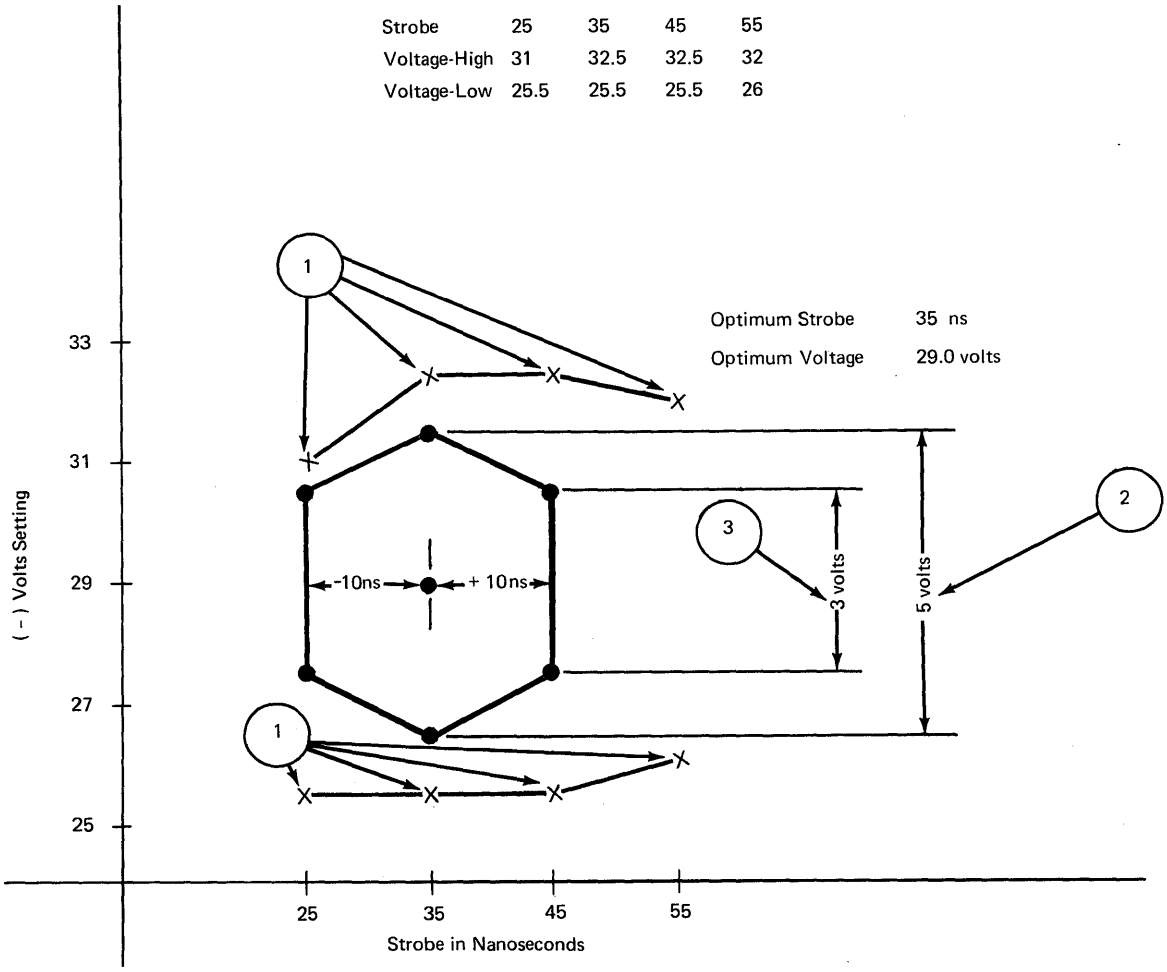


Figure 4-3. Schmoo Curve Example (Single BSM)

4.3.2 WHEN TO SCHMOO

A four-point strobe and a two-point strobe schmoo procedure are given. The four-point strobe schmoo procedure should be used only when an array is replaced. The two-point strobe schmoo procedure should be used only under the following conditions.

1. When any one of the following cards is replaced or identified as a trouble area.
   a. Sense amp, part 58004648
   b. Source driver, part 58004649
   c. Strobe, part 58007237
   d. Clock, part 58001762
2. An intermittent problem exists and it is desired to increase the failure rate to isolate the trouble within the memory area.
3. On a new memory installation.

4.3.3 SERVICE CHECKS

Refer to Section 4.3.6, Checkout Procedures.

4.3.4 WORST-CASE PATTERNS

The worst-case test patterns are run from the console by the customer engineer as a diagnostic to test the storage unit for a failing condition. The test is done with the diagnostic control switch set to TEST PATTERN, and the check control switch set to STOP.

4.3.4.1 Worst-Case Test

Each test should be run for approximately fifteen seconds with switches A, B, C, and D set as follows.

	A	B	C	D	Test Description
1st Test	0	0	F	F	Checks worst-case zeros (adds noise to cores)
2nd Test	F	F	0	0	Checks worst-case one's (subtracts noise from cores)
3rd Test	0	1	F	E	Checks parity bits
4th Test	F	E	0	1	Checks parity bits

4.3.5 FOUR-POINT STROBE SCHMOO PROCEDURE

Note: For measuring critical voltages, use Weston* 901 (or equivalent)

1. Set the -30 voltage (XYZ) to -29 volts ±0.5 volts.

2. The schmoo timing points are taken at 25 ns, 35 ns, 45 ns, and 55 ns.

3. Refer to logic MD008 for instruction on how to set the strobe card. The strobe card is part 5807237 and is plugged in B1E3.

4. Start the schmoo at a setting of 35 ns.

5. Run worst-case patterns (Section 4.3.4.1) at -29 volts. If failures are noted (stor data light turns on), lower the voltage until a running point can be found. To restart the test after failure, press CHECK RESET then START. If no running point can be found, consult memory strategy diagrams in the 2025 Maintenance Diagram Manual (MDM).

6. Increase voltage in one volt increments and run the worst-case patterns until a failure occurs.

7. Decrease the voltage in one-half volt increments and run the worst-case patterns until no failure occurs. Record this voltage as the upper voltage limit for this particular strobe setting. Figure 4-3 shows an example that can be used as reference for this procedure.

8. Start at running point found in step 5, repeat steps 6 and 7 in the opposite direction, and record the setting found in step 7 as the lower voltage limit for this strobe setting.

9. Repeat this procedure, beginning at step 5, using strobe settings of 25 ns, 40 ns, and 55 ns, and plot these values on a graph (Figure 4-3) .

10. The optimum strobe setting for a single BSM is at a point where the difference between the upper and lower BSM limits (on the graph) is greater than 5.0 volts. At a strobe setting ± 10 ns from optimum, the difference between the upper and lower BSM limits must be greater than 3.0 volts.

    For a double BSM, the difference between the upper and lower BSM limits at optimum strobe must be greater than 3.6 volts. At a strobe setting ±10 ns from optimum, the worst-case diagnostic must still run successfully. In both cases the strobe setting must be between 35 ns and 55 ns. It should be the earliest setting that will meet requirements, and 35 ns should be used if possible.

11. Set the voltage midway between the upper and lower limits (steps 7 and 8) for the optimum strobe setting.

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*Trademark of Sangamo Electric Co., U.S.A.

4.3.6 CHECKOUT PROCEDURES

1. Check to see if all logic voltages are within tolerances, that the array heater is operating, and that the array temperature is properly adjusted (Section 4.2).
2. Measure the voltage on B1U2D07 (referenced to B1U2D08) using a Weston 901 meter (or equivalent). The sense-amplifier voltage is set to -18 volts ± 0.1 volt accuracy (see decal) by means of the potentiometer on the card located in B1U2.
   At EC 799307, 16K and 32K BSM sizes have the -18V set at -17.6V. The 32K BSM remains at -18V.

   CAUTION

   This is a critical, highly regulated voltage that is set under controlled conditions at the factory before shipment. The voltage setting should be changed only when the card that generates it is replaced. It should then be set using a Weston 901 meter (or equivalent). In case of array replacement, this voltage should not be touched.

3. Changing any memory card should not change the timing more than 5 ns.
4. The optimum strobe setting of the System/360 Model 25 memory should fall between 35 to 55 ns.

4.3.6.1 Scoping Main Storage

Refer to Section 1.31 for main storage diagnostic information and scope waveforms.

4.3.7 TWO-POINT SCHMOO PROCEDURE

Note: Use a Weston 901 meter (or equivalent) when measuring the -18 voltage. The -18 volt supply should not be changed, and should measure as follows.

8K (16K bytes) -17.6 volts
12K (24K bytes) -17.6 volts
16K (32K bytes) -18.0 volts

1. Record the voltage at which memories are set.
2. Vary the voltage 2 volts above that voltage.
3. Run the worst-case patterns (Section 4.3.4).
4. Vary the voltage 2 volts below value recorded in step 1.
5. Run the worst-case patterns. If machine does not fail at this voltage setting, restore the voltage to that recorded in step 1. (This indicates that memory is within operating schmoo tolerance; return to routine in)MDM.)
6. If machine fails during steps 3 or 5 (indicated when STOR DATA lights on console), measure the -18 volt supply between, B1U2D07 and B1U2D08 (MD999) to ensure it is not grossly in error.
   If the spread from high to low operating limits is still below 4 volts, a memory component failure is indicated. Set the voltage and strobe as recorded in step 1, indentify the circuit failure, and re-schmoo the memory (starting at step 2).
7. Vary the -30 volt supply 0.2 volts toward the voltage recorded in step 1.
8. Repeat the worst-case pattern that failed in step 6.
9. If failures continue, repeat step 7 and step 8 until no failure is detected and record the voltage setting used in this step.

   CAUTION

   Do not exceed -35 volts.

10. Set the voltage 4 volts from the limit recorded in step 9 toward the original setting (step 1).
11. If the worst-case patterns run at voltage setting in step 10, set the voltage midway between the high and low operating limits.
12. If the worst-case patterns do not run at the voltage setting in step 10, increase the strobe timing on the failing BSM, 5 ns.

    Note: The failing BSM can be identified by the higher address-bit of the failing address. 0=lower BSM, which is adjacent to power supply; 1=higher BSM, which is adjacent to console.
13. Repeat procedures starting at step 1 and attempt to establish a 4-volt spread from the high to low operating limits.

4.4 MAIN STORAGE REPLACEMENT

4.4.1 REMOVING THE 0-32K UNIT

1. Ensure that power to the system is off.
2. Disconnect the wires from terminal blocks TB12-L and U. These are the terminal blocks at the heater box. Label the wires if necessary.
3. Remove the power-input cable from LBC-1 (mounted on top of CSU frame). Number the wires if necessary.
4. Remove the ribbon cable connectors from B1A3, B1A2, and B2A2. Remove the cable clamp and cables.
5. Lift the storage unit free of its hinges and remove.
6. Replace in the reverse order.

4.4.2 REMOVING THE 32-64K UNIT

1. Ensure that power to the system is off.
2. Disconnect the wires from terminal blocks TB12-L and U. These are the terminal blocks at the heater box. Label the wires if necessary.
3. Remove the power-input cable from LBC-1 and 2 (mounted on top of the BSM frame). Number the wires if necessary.
4. Remove the ribbon cable connectors from B1A2, B1A3 and B2B2. (These are cables from the adjacent 32K unit.) Remove the cable clamp and cables.
5. Lift the storage unit free of its hinges and remove.
6. Replace in the reverse order.

4.4.3 ARRAY CHANGING

To remove the array from either storage unit:

1. Ensure that power to the system is off.
2. Viewing the core storage unit from the card side, remove the outrigger by loosening the screws on the BSM frame and array. Lift the outrigger up to remove.
3. Open the two side doors (right and left side of array).
4. Disengage the four locking screws in the array cover and remove the cover.
5. Loosen the two screws on the underside of the cross member that separates the B1 and B2 card areas. These screws hold the sense cable clamp and the array to the frame.
6. Remove the top cover (B1 board card area) and unplug the sense cables.
7. Remove the two screws holding the heater plenum to the array.
8. Remove the six screws (four on card side, two on opposite side) in the bracket holding the heater plenum to the BSM frame.
9. Viewing the BSM from the front, place one hand beneath the heater plenum to the BSM frame (located immediately above the terminal blocks). The heater can now be lowered down away from the array.
10. Using the diode board stiffeners and/or the U-shaped bracket (not diode boards), pull the array out by rocking it up and down slightly until it comes free from the large board. Cover the top of the array (C-side) and carefully feed the sense cables down through the card area as the array is removed.
11. Replace in the reverse order.

4.4.4 CHANGING DIODES

If diode or drive-line trouble is suspected in storage, follow the storage address lines in storage logic through the read/write drivers and eventually to the pin numbers on the array diode cards.

The logic shows the layout of the array diode cards and diode pack. The removal procedure is:

1. Extract the array from the logic boards.
2. Place the array carefully on a flat work area.
3. Unsolder the four diode-pack pin connections, taking care not to apply excessive heat or to damage any land pattern.
4. Extract the defective diode-pack and replace it with a tested spare.
5. Inspect the card for damage.
5. Inspect the card for damage.
6. Replace the array.

Note: Diode card location on array ALD page MD007. Diode-pack location on diode card ALD page MD007. Diode-pack pin location on ALD page MD007, Note 2. Diode cards land patterns on ALD pages MD860-MD890.

4.5 LOCAL STORAGE

Two delay lines are used in the local storage (B150 stack) circuit (01A-B1E2). The tolerance on the delay lines is ± 4.5 for the 90 ns delay line and + 3.0/-2.0 for the 30 ns delay line. The 30 ns delay line controls the sense amplifier gate pulse (LS Read Line), and the 90 ns delay line controls the bit timing pulse (LS Write Line) and the width of the X- and Y-address lines.

4.5.1 SCOPING LOCAL STORAGE

Refer to Section 1.32 for local storage waveforms.

4.5.2 INITIAL DELAY LINE SETTINGS

The initial settings for the two delay lines are:
LS Read Line -- 30 ns
LS Write Line -- 90 ns.

4.5.3 DELAY LINES (LOCAL STORAGE) ADJUSTMENT

1. Store the following arithmetic into an unused portion of control storage (FE trap area). U0=U0 + U1 (hexword 6013) followed by an unconditional branch back to this word.

Example:

Hexword

Address	Hexword
0280	6013
0282	8270

2. Sync the scope on word type 3 (01A-B1G7B05).
3. Scope and record the duration from the 10% fall -LS ADDR X0 to the 10% fall -LS READ LINE (ALD-CC131). Refer to Figure 4-4.

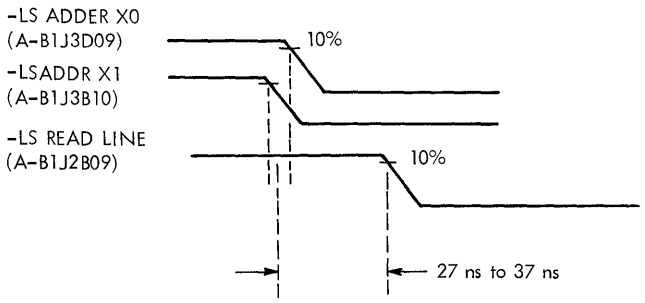

Figure 4-4. LS Address Lines and Read Line

4. Scope and record the duration from the 10% fall of -LS ADDR X1 to the 10% fall of -LS READ LINE. Refer to Figure 4-4.
5. Take the average of the durations recorded in steps 3 and 4. The average of these two durations must fall between 27 ns to 37 ns. If the average does not meet this requirement, plug the appropriate jumpers to increase or decrease the delay.
6. Scope -LS ADDR X0 and +LS WRITE LINE using the same sync as in step 2. These two signals must be coincident for a minimum of 70 ns from the 10% point of the rising edge to the 10% point of the falling edge (Figure 4-5).
7. Scope +LS ADDR Y0 to ensure that the same coincidence holds true as in step 6 (Figure 4-5). If not, the delay line value must be increased to satisfy this requirement.

Note: In Figure 4-5, points E and F must fall inside points A and B, and C and D, for a minimum of 70 ns. The +LS WRITE LINE may fall outside address pulses if there is no second address selected.

4.5.4 LOCAL STORAGE/STORAGE PROTECT CARDS

Machines with the storage protect feature use a local storage card in the storage protect circuits (the cards are identical). If the local storage card is suspected to be failing, it can be swapped with the storage protect card.

Refer to Appendix A for detailed operation and circuit specifications.

4.6 SCR CIRCUITS

There are three spare indicator SCR circuits for use as replacements for defective SCR light drivers. The load input pins, wire number and cable position on the SCR boards in cable part 2532050 are as follows.

Location	Wire No.	Cable Position
A2A2B10	19	20
D1N7B10	39	20
C2N7D09	57	9

The wires 19, 39, and 57 are connected to the SCR in the respective paddle card. The console-end of these spare wires are taped back in a group. Figure 4-6 shows the point from which continuity can be checked to find the correct spare wire at the console-end of the cable.

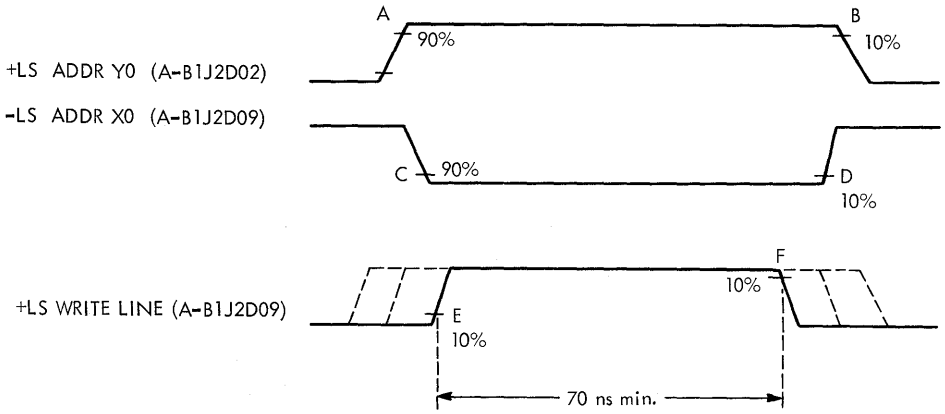

Figure 4-5. Local Storage Address Lines and Write Line

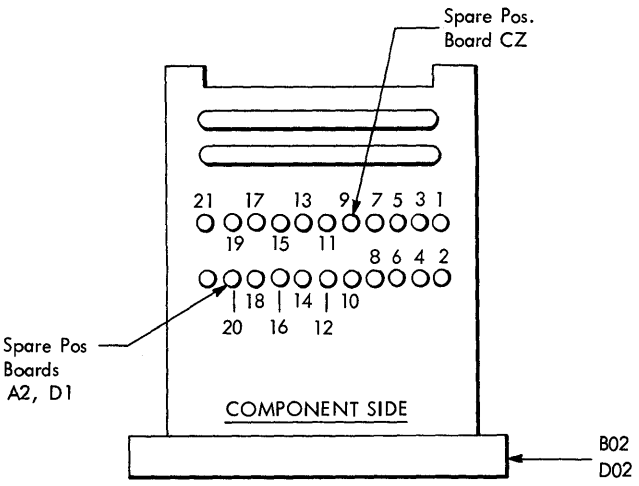

Figure 4-6. SCR Card Cable-Connecting Terminals

4.6.1 REPLACEMENT

Connect the signal to the input pin of the spare circuit to be used. Replace the wire to the indicator lamp with the spare cable lead to be used.

4.7 SYSTEM RESET, IPL, OR CSL--SINGLESHOT

The CPU contains a singleshot that is activated when the system reset, IPL, or ICPL switches are pressed. Its purpose is to prevent switch bounce noise from stopping the CPU clock.

4.7.1 ADJUSTMENT

1. Turn the process switch to single cycle and press the system reset key.
2. Adjust the singleshot (logic PF 251) to 30 ms ±5 ms, using the upper potentiometer (Figure 4-7).

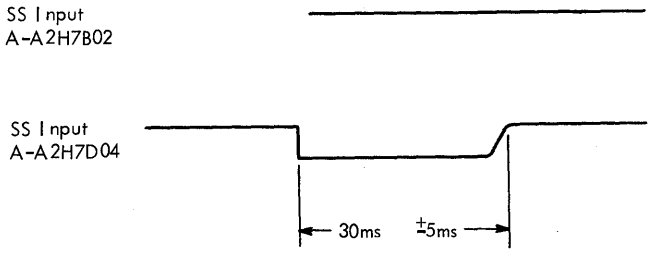

Figure 4-7. System Reset, IPL or CSL (Singleshot)

4.8 OPERATIONAL OUT--SINGLESHOT

The System/360 standard interface contains a singleshot (A-E1G7) with an adjustable potentiometer on it to adjust the operational-out signal.

4.8.1 ADJUSTMENT

Scope A-E1G7D12 and adjust the lower potentiometer on A-E1G7, while pressing the system reset key, to obtain a negative pulse of 8.0 us +1/-0 us.

4.8.2 CHECKOUT PROCEDURE

Operational-out singleshot is checked in routine 3 (YM03) in the channel microdiagnostic *600. See instructions in routine YM03 for adjustments.

4.9 2540 ATTACHMENT

The optional 2540 attachment consists of two SLT boards located in the A-gate, E2, and E3. Three leading-edge time delay cards are located at A-E3D5, A-E3E5, and A-E3E4.

4.9.1 SPECIFICATIONS

The 2540 attachment clock is driven from a 1.667 megahertz oscillator located in the A-E3 board. This provides a 4.8 us clock cycle for communication with the 2540 and the attachment in the CPU.

The timing for the three leading-edge time delay cards are as follows.

Location	Timing
A-E3D5	150 us, +20/-0 us
A-E3E5	2.2 ms, +50/-50 us
A-E3E4	5.5 ms, +0/-100 us

4.9.2 ADJUSTMENTS

The adjustments for the three leading-edge time delay cards are made using the following routines in the nonresident microdiagnostics.

Card Location	Microdiagnostic	Logic
A-E3D5	VM07 (Reader-Punch)	RT015
A-E3E5	VM08 (Reader-Punch)	RT021
A-E3E4	VM20 (Reader-Punch)	RT041

4.10 PR-KB (1052-7)--SINGLESHOTS

The PR-KB attachment circuitry is located on the A-gate, A2 board. The circuitry

contains two singleshot cards having two adjustable singleshots per card.

4.10.1 SPECIFICATIONS

The singleshots must be adjusted so that when the input signal goes from its negative level to its positive level, the output of the singleshots will go to a negative level for the following durations.

Number: SS1
Duration: 28.0 ms (+15.0 ms/-1.0 ms)
Location: A-A2G7D04 (PF021) Upper Pot.

Number: SS2
Duration: 500 ns (+100 ns/-100 ns)
Location: A-A2G7D06 (PF021) Lower Pot.

Number: SS3
Duration: 40.0 ms (±15%)
Location: A-A2H7D06 (PF021) Lower Pot.

4.10.2 ADJUSTMENT

Refer to TYDD diagnostic routine *110. This describes the procedure to adjust and check the PR-KB singleshots.

4.11 2311 READ CLOCK ADJUSTMENT

The 2311 read clock card is located in the B-gate in E3-board, J5-socket. This adjustment procedure makes use of the write clock signal as an input to the read clock to allow the adjustment to be made without using a disk drive.

Note: Use a Tektronix* 453 oscilloscope or equivalent.

SCOPE SETUP
Chan 1: B-E3J5J10 (FA 111)
Chan 2: B-E3J5G02 (FA 111)
Sync: Minus Internal Chan 1

1. Jumper B-D3M5D05 to ground (D08 pin). This resets the chain-end and NTO-OP latches (FA 651).
2. Jumper B-E3J3B04 (FA 109) to B-E3K6B09 (FA 111). This feeds write pulses into the read clock.
3. Jumper B-E3J5G04 (FA 111) to ground (D08). This forces the read clock to use the long time constant.
4. SYNC minus (-) on Channel 1. This is the 800 ns write pulse (Figure 4-8). Make certain that points A and B are exactly 8 divisions apart. If they are not, adjust the scope until they are.
5. Display Channel 2 and adjust potentiometer on B-E3J5 (FA 111) until the 10% level of the rising clock pulse is 640(+0,-5) ns from point A.
6. Remove all jumpers.

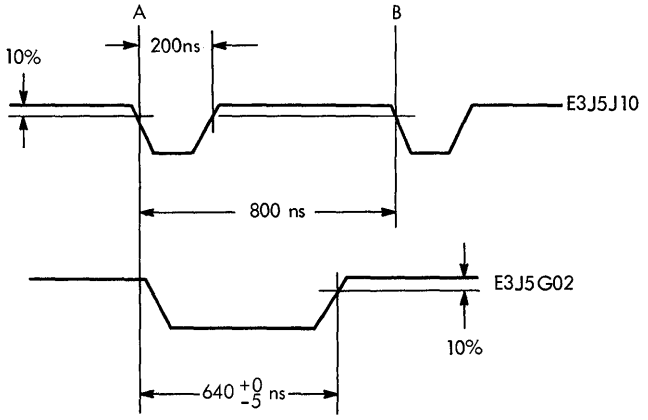

Figure 4-8. Read Clock Traces

4.12 DAC--SINGLESHOTS

4.12.1 SPECIFICATIONS

Recalibrate Time Out SS1	16 ms (± 5%)
Recalibrate Time Out SS2	16 ms (± 5%)
Head Conditioning SS	60 us (± 5%)
Index SS (2)	400 ns (± 5%)
Control Tag SS	1.0 us (minimum)

4.12.2 ADJUSTMENTS

All singleshot adjustments for the DAC are made while using microdiagnostic *300, routine 6. First, load *300, set switches ABCD to 0106, press and release SET IC, and press and release START. This forces a loop on routine 6. For the adjustment to be performed, the sense switch specified in the adjustment must be on. Only one section sense switch can be on at any one time.

4.12.2.1 Head Conditioning Singleshot (FA131)

1. Turn section sense switch 2 on.
2. Sync the scope on 01B-E3G7D12 (negative).
3. Look at the output on E3G7D04 and adjust to 60 us ± 5%.

4.12.2.2 Index and Delta Index Singleshots (FA131)

1. Turn section sense switch 3 on.
2. Sync the scope on 01B-E3G3D12 (neg).
3. Look at the output on E3F2D13 and adjust to 400 ns ± 5% by varying the

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*Trademark of Tektronix, Incorporated

bottom potentiometer.
4. Look at the output on E3F2B13 and adjust to 400 ns ±5% by varying the bottom potentiometer.

4.12.2.3 Control Tag Singleshot (FA225)

1. Turn section sense switch 4 on.
2. Sync the scope on 01B-E3F2D02 (negative).
3. Look at the output on E3F2D12 and adjust to one microsecond (minimum) by adjusting the upper potentiometer.

4.12.2.4 Recalibrate Singleshots (FA611)

1. Turn section sense switch 5 on.
2. Sync the scope on 01B-C3C2B10 (negative).
3. Look at the output on C3C2D11 and adjust to 16 ms ± 5% by varying the upper potentiometer.
4. Sync the scope on 01B-C3C2D13 (negative).
5. Look at the output on C3C2D12 and adjust to 16 ms ± 5% by varying the lower potentiometer.

4.13 DAC--TIME DELAY CIRCUITS

4.13.1 SPECIFICATIONS

The DAC contains two time-delay cards that have two delay circuits on each card. These delay circuits are pluggable in increments of 5 ns with a maximum of 125 ns delay per circuit.

These circuits are plugged at 75 ns and 125 ns in the 2025 DAC.

4.13.2 CHECK

1. Loop *300 routine 05.
2. Scope delays as indicated in Figure 4-9.
3. Refer to ALD ZZ016 for card plugging if necessary.

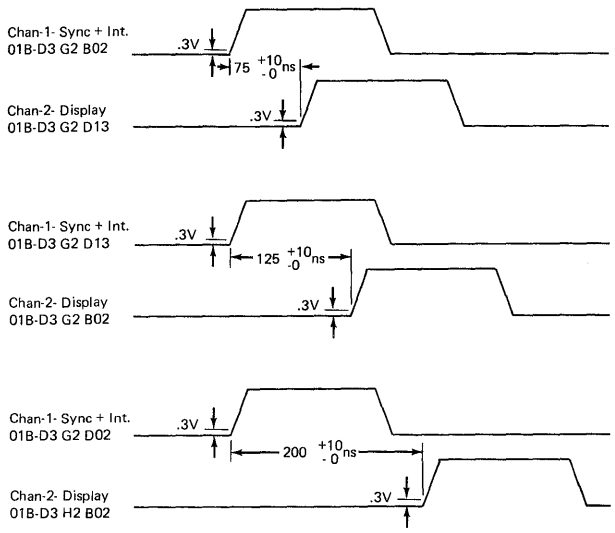


Figure 4-9. DAC Time Delay

4.14 1403 ATTACHMENT (FIGURE 4-10)

An optional integrated printer attachment may be provided in the CPU. This attachment is capable of operating either a 1403-2, 1403-7, or 1403-N1 printer. The attachment is housed in the CPU frame on the A-gate. Three boards, B3, C3, and D3, contain the control logic. A fourth board, H-P1, contains hammer, magnet, and indicator drivers, including associated interface circuitry for the printer. The H-P1 board is located in the power tower.

The integrated printer attachment uses SLT circuits of the 30 nanosecond group for all areas except for the hammer and magnet drivers, and interface to the printer. The hammer and magnet drivers are mounted on SLT cards and use discrete transistors capable of providing the current necessary to operate the printer. The hammer driver and the switch level set cards contain SLD modules of the 100-nanosecond group.

The print buffer consists of 168 positions of 13 bits. Of the 13 bits, nine are used for data and parity. The remaining four bits are used for checking purposes.

4.14.1 TIMING (FIGURE 4-11)

The attachment clock for the 1403 Model 2 or 7 is an eight-point clock controlled by a 720-KHz oscillator having a ±0.1% stability. The clock runs only during printing and produces 11.1-microsecond pulses.

The attachment clock for the 1403 Model N1 is an eight-point clock controlled by a 1667-KHz oscillator having a ±0.03% stability. The clock runs only during

printing and produces 4.8-microsecond pulses.

The timing pulses necessary during loading of the buffer from the CPU are provided by the microprogram.

4.14.2.1 PSS (B3E3D04) PR262

Adjust to 15 us +5 us/-0 us, with the printer idling and T-casting closed.

4.14.2 SINGLESHOT ADJUSTMENTS (FIGURE 4-12)

Refer to Section 4.18 for MCS feature.

Name of Unit or Item	Model 2	Model 7	Model N1
Cartridge Type	Chain	Chain	Train
Number of Print Positions	132	120	132
Max. Printing Speed (LPM)	610*	610*	1127**
Chain Motor Speed (RPM)	3600	3600	3600
Chain Velocity (IPS)	90.3	90.3	206.0
Time Required for Type to move .001" (Microseconds)	11.1	11.1	4.8
Settling for Calibration of Print-Timing Dial with Print Density Lever set at C	20	20	--
Timing Disk Speed (RPM)	750	750	1714
Time Required to Print One Line with Single Space (Milliseconds)	98.3	98.3	53.2
Carriage Interlock Time	21.4	21.4	20.7
Carriage Type (Speed)	Dual 33in./sec 75in./sec	Single 33in./sec	Dual 33in./sec 75in./sec

*750 (LPM) with MCS feature **1419 (LPM) with MCS feature

Figure 4-10. IBM 1403 Reference Chart

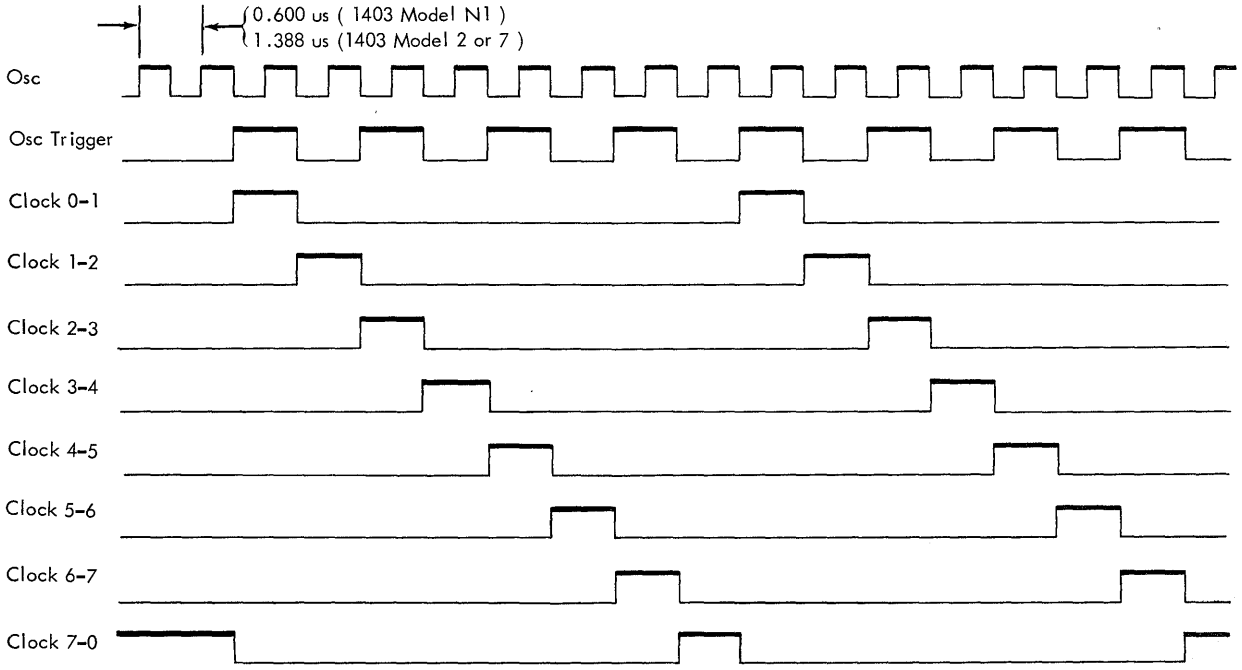


Figure 4-11. Print Clock

Name	Location	Length	Tolerance
PSS	B3 E3D04	15us.	+5, -0
Strobe Delay	B3 M2D04	250ns.	Note 1
Home Gate (Model 2, 7)	B3 F3B03 (Upper)	340us.	±20us.
Home Gate (Model N1)	B3 F3B03 (Upper)	160us.	±15us.
Coil Protect	B3 D3B03 (Upper)	3.5ms	±350us.
Coil Protect	B3 C4B03 (Upper)	1.5ms	± 150us.
Coil Protect	B3 D3D10 (Lower)	2.0ms	±200us.
Coil Protect	B3 C4D10 (Lower)	5.0ms	±500us.
Single Space	B3 L6B03	5.5ms	Note 2
Double Space	B3 F3B07	9.8ms	Note 2
Triple Space	B3 L6D10	13.8ms	Note 2

Note 1: This value is given as a starting point - see Buffer Adjustment

Note 2: These values are given as a starting point. The exact value varies with each printer and must be obtained by using the procedure outlined in Diagnostic Section *420, Routine WESS.

Figure 4-12. 1403 Singleshots

4.14.2.2 Home Gate (B3F3B03)-(Upper) PR252

Model 2 or 7: Adjust using diagnostic routine WE06 in Section *400. This provides a range of 320 to 360 microseconds.

Model N1: Adjust using diagnostic routine WE06 in Section *400. This provides a range of 145 to 175 microseconds.

4.14.2.3 Coil Protect PR691

Adjust using diagnostic routine WE26 in Section *400. The diagnostic fires the singleshots, and the resulting waveforms can be observed on the oscilloscope.

4.14.3 Delays (Figure 4-13)

Name	Input	Output	Length
Carriage Settling Delay	B3 H7D02	B3 H7D13	See 4.14.3.2
Speed Limit	B3 J2D05	B3 J2D13	See 4.14.3.1

Figure 4-13. 1403 Delays

4.14.3.1 Speed Limit Delay PR262

Adjust using diagnostic routine WE29 in Section *400.

1403-2 or 1403-7 without MCS: A minimum of 46 print scans must be taken before the last scan is allowed. This gives a maximum speed of 610 lines per minute.

1403-2 or 1403-7 with MCS: A minimum of 35 print scans are taken before the last scan is allowed. This gives a maximum speed of 750 lines per minute.

1403-N1 without MCS: A minimum of 45 print scans must be taken before the last scan is allowed. This gives a maximum speed of 1127 lines per minute.

1403-N1 with MCS: A minimum of 30 print scans must be taken before the last scan is allowed. This gives a maximum speed of 1419 lines per minute.

4.14.3.2 Carriage Settling Delay (PR742)

Adjust using diagnostic routine WE51 in Section *420 after setting the single-space singleshot. For the 1403-2 or 1403-7, this will give a combined single space and carriage settling range of 20.4 to 21.4 ms. For the 1403N1 this gives a combined single space and carriage settling range of 20.6 to 20.9 ms.

4.14.4 BUFFER SERVICE CHECKS

Refer to Section 4.14.6.

4.14.5 BUFFER ADJUSTMENT

1. Set all voltages are specified in Chapter 5.
2. Initially set Vsl to +3V with respect to ground (PR551) using the upper potentiometer.

4.14.5.1 Vxy Adjustment

1. Estimate the temperature of the room. Measure Vxy (01A-C3L2D11) with respect to ground.
2. Set Vxy using the lower potentiometer ofC3L2 to the appropriate value with respect to the room temperature:

   60F (15.6C) +1.6V
   70F (21.1C) +1.5V
   80F (26.7C) +1.4V
   90F (32.2C) 1.3V

Note: If air conditioning ducts or floor cutouts allow air colder than room temperature at the input to Gate-A in the C-board area, use the Vxy setting for the next lower temperature. If such cooling conditions are present, check Vxy after the gates have been closed to verify that the voltage is at the desired value. It may be necessary to readjust for the proper setting.

4.14.5.2 Strobe Adjustment

1. Attempt to write all bits in the buffer (Diagnostic Routine WE15, Section *400); disregard any errors.
2. Sync the scope on '-0 x+4x Strobe SA' (PR551) (01A-C3L2B04).
3. Observe the output of the PLB1 sense amplifier, '-0 PLB sense 1' (PR561) (01A-C3K2B02).
4. Adjust the strobe delay singleshot in 01A-B3M2 until the sense amplifier output appears. Adjust the singleshot potentiometer to obtain an output pulse of maximum width. If the maximum width occurs over a range, adjust the potentiometer to the center of the range.

4.14.5.3 Vsl Adjustment

1. Loop on the 1403 buffer voltage routine (WE16 in Section *400), set sense switches to continue after errors, and print an asterisk (*) only on errors.
2. Adjust the upper potentiometer on C3L2 clockwise until an error message prints (or until a print check occurs).
3. Adjust the potentiometer clockwise until the error conditions show up and set the Vsl .1 volt more negative than the high failure level of Vsl.

   Note: The range between the failure points should be at least .3V. A range of less than .3V may indicate a bad component such as a sense amplifier.

4. The buffer should now be adjusted properly to track effectively over its specified operating temperature range. If any of the buffer components (sense amplifier, driver, etc.) are replaced, the Buffer Adjustments procedure (Section 4.14.5) must be repeated to obtain optimum operation.

4.14.6 BUFFER CHECKOUT PROCEDURES

Loop the ripple print routine to test accuracy of buffer adjustments.

4.15 2560 ATTACHMENT

4.15.1 BLOCK FEED CHECK JUMPER

When the block feed check jumper is installed, all 2560 feed checks are prevented. To scope the feed and feed check circuitry:

1. Set up a short instruction loop according to the type of feed check, using MFT 72.
2. Connect the block feed check jumper (MF 506), and load blank cards in the selected hoppers.

Control and check circuitry can then be scoped as desired. Sync signals are FCB 1 to 6, trailing edge, or those signals that initiate a feed cycle.

4.15.2 ADJUSTMENTS

4.15.2.1 Singleshots

The monitor-controlled 2560 diagnostic coreload *820, routines UM35 and UM36, describes the adjustment of all singleshots in the 2560 attachment feature for both print and nonprint 2560s.

4.15.2.2 Feed Cells

Refer to the publication, Model 25 Pluggable Display and External Field Definitions, and plug the display cable in the location that brings the signal, 'any feed cell dark,' to the indicator lights. Adjust the feed cells as described in the 2560 FEMM.

4.16 INTEGRATED COMMUNICATIONS ATTACHMENT

4.16.1 TIMEOUT OSCILLATOR

The timeout oscillator contains two 115-ms singleshots. The singleshots are running continuously: adjust each one to 115 ±5ms while scoping the output pin. See ALD page HA064.

4.16.2 TIMEOUT CLOCK SINGLESHOT

The 350-ns timeout clock singleshot is started every 460 ns, and should be adjusted to 350 ±35ns while scoping the output pin. See ALD page HA064.

4.16.3 SYSTEM RESET SINGLESHOTS

There are two 5-microsecond system reset singleshots. One is started by the system reset switch on the console (Note 4 on ALD HA064). The second is used by the ICA microdiagnostics and can be scoped by looping the entire section or any routine in *700 (Note 5 on ALD HA064).

4.16.4 A-CLOCK SINGLESHOT

There is one 2.5-microsecond A-clock singleshot per start/stop base board. The singleshot runs continuously and can be adjusted while the output pin is being scoped. See ALD HA137 for EIA boards (B-X1). See ALD HA337 for TLG boards (B-Y1).

4.17 EXTERNAL INTERRUPTION AND DIRECT CONTROL FEATURES

The external interruption and direct control features are combined here because installation of the direct control feature requires that the external interruption feature also be installed. The external interruption feature, however, can be installed without the direct control feature.

Both features are plugged on board A1-A3.

4.17.1 SPECIFICATIONS

Signals on the direct control interface are of three types:

1. The direct-control bus-out and the direct-control bus-in lines carry static levels that remain on the lines until changed by the CPU program or by the external equipment.
2. The timing-out, read-out, write-out, and external bus-in lines carry pulses.
3. The hold-in line may carry either a pulse or a static signal.

These signals are shown in Figures 4-14 and 4-15. In these figures, all pulses are considered positive and the up-level is considered a logical one.

When the CPU power is off, all outputs to the outbound busses or tag lines must be at a logical zero.

4.17.2 ADJUSTMENTS

Although circuit adjustments cannot be made to these features, the circuit cards of any given type must operate satisfactorily in any socket location specifying that type. Selection or interchange of cards to obtain satisfactory performance is unnecessary and should not be done.

4.18 INTERVAL-TIMER ADJUSTMENT

The singleshot located at A-A3J7 must be adjusted as follows. Scope the signal at A-A3H3D05 (CT011). Adjust the singleshot to give a 10-millisecond ± 10% positive going pulse at this point for 60-cycle machines, or an 11-millisecond ± 10% positive going pulse for 50-cycle machines. It is not necessary to have the CPU clock running to make this adjustment. The singleshot must be functioning all the time power is on.

4.18.1 SERVICE CHECK AND CHECKOUT PROCEDURE

To test the interval-timer feature, first run microdiagnostic *200. Timer switch must be on to run this test. Next place the machine in single-cycle mode and press system reset. Display the interval-timer register; it must be zero. Now alternately press start and then display the interval-timer register. Each time this is done, there is a 50% chance that the register will be advanced. Each time it does advance, it is increased by only one count. When a count of one has been reached, turn the interval-timer switch off. The interval-timer register should continue to advance. When all bits of the C-register are on (interval-timer register equals 15), press the start button ten more times. The value in the interval timer must not change.

Leaving the interval-timer switch off and the machine in single-cycle mode, press system reset. Display the interval-timer register; it must be zero. Press start ten times. The interval-timer register must still be zero.

4.19 STORAGE PROTECTION FEATURE ADJUSTMENT

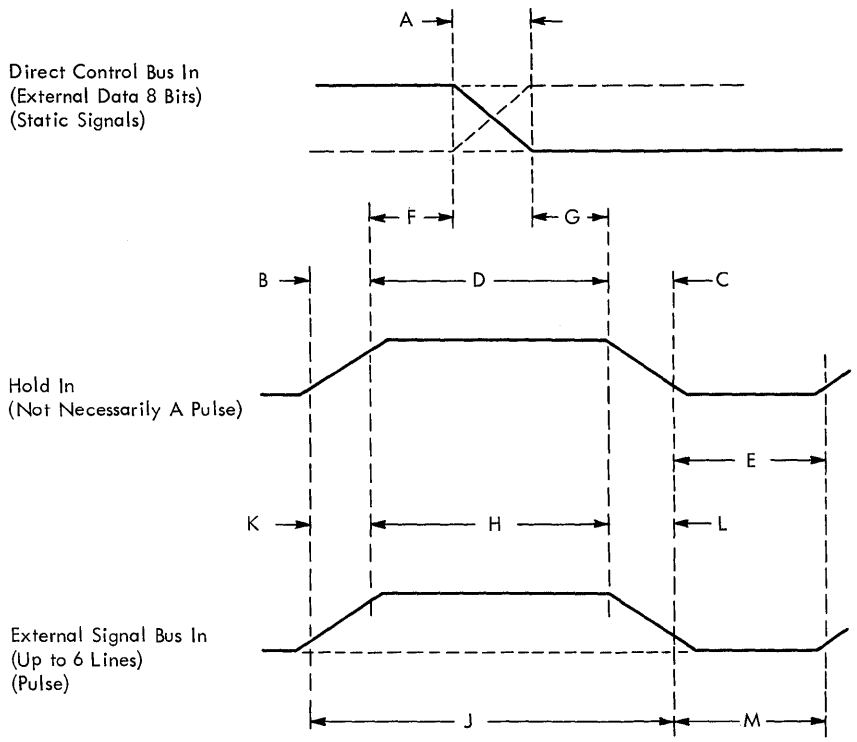
Figure 4-16 shows the time relationship of the STP1 local storage compared to the CPU word type 2. A delay line is used to adjust the STP local storage read line. This delay line has a tolerance of +3 to -2 nanoseconds and can be adjusted by using the following procedure.

1. Store the storage word 5210, followed by an unconditional branch back to this word, into an unused portion of control storage.

   Example:

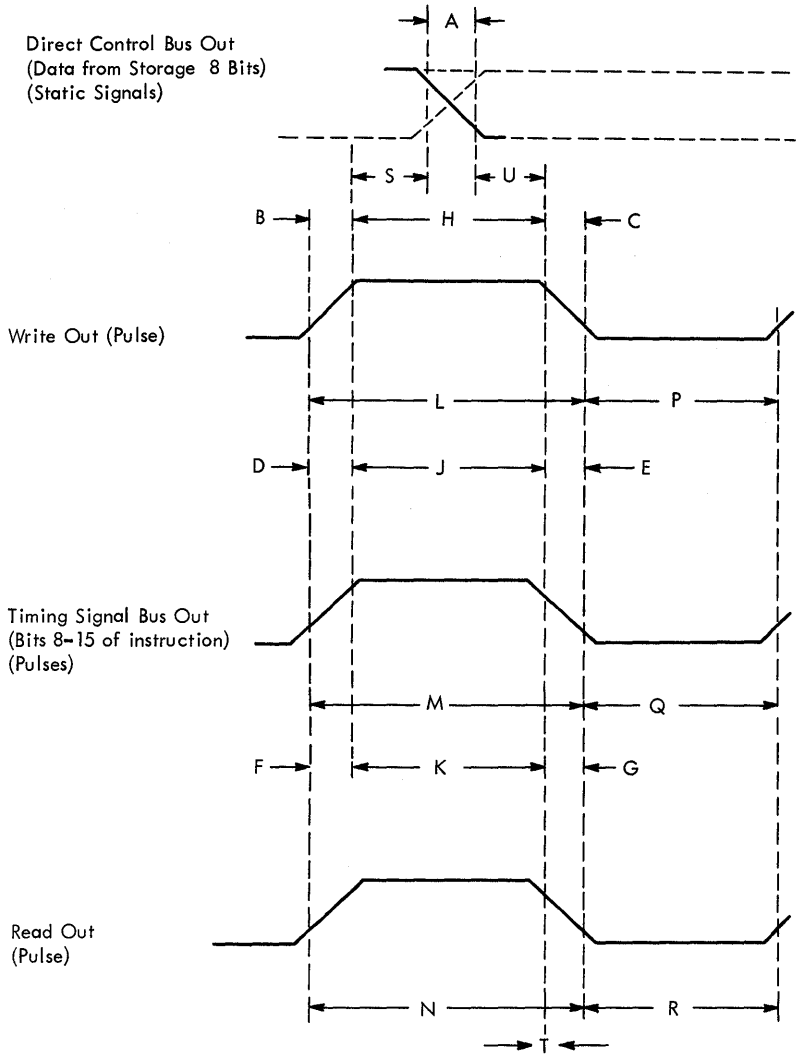
Address	Contents	
0280	5210	(FE Trap Area)
0282	8280	

2. Sync on word type 2 (location 01A - B1C7B03).
3. Scope and record the duration from the 10% rise of 'Y0 ADDR LINES STP1' to the 10% fall of 'STP1 READ LINE' (ALD - XQ007).
4. The duration (Figure 4-17) must be between 27 ns and 37 ns. If this requirement is not met, the delay line must be plugged to satisfy this condition.



A. B. C. K. L.	No minimum transition duration specified
D	Minimum is 500 nsec. no maximum specified
E	Minimum is 500 nsec. no maximum specified
F	Minimum overlap between data change. 100 nsec. no maximum specified
G	Minimum overlap after data change. 100 nsec. no maximum specified
H	Minimum duration 500 nsec.
J	Maximum including transition 1000 nsec.
M	Minimum down level between pulses not specified

Figure 4-14. Direct Control Signals Originating Outside the CPU



A. B. C. D. E. F. G	Maximum transition time is 200 nsec.
H. J. K	Minimum duration is 500 nsec.
L. M. N	Maximum including transition. 100 ns.
B. D	Leading edges coincidental within skew tolerances
F. D	Leading edges coincidental within skew tolerances
S	Overlap start Write Out to change D. C. P. O. 100 nsec. (MIN)
U	Overlap change of D. C. P. O to finish of Write Out 100 nsec. (MIN)
T	Earliest time to sample hold line during read direct.
P. Q. R	Minimum down time between pulses is 500 nsec.

Figure 4-15. Direct Control Signals Originating within the CPU

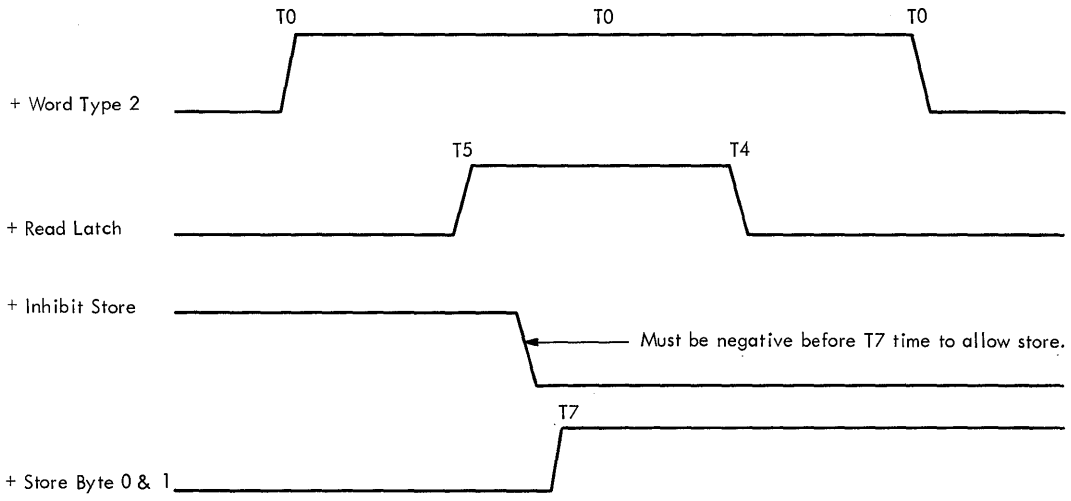


Figure 4-16. STP1 Time Relationship to Word Type 2

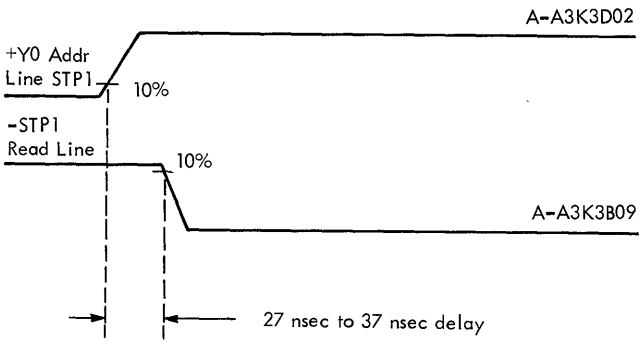


Figure 4-17. STP1 Read Line Delay

Chapter 5. Power Supplies

5.1 GENERAL INFORMATION

Electrical power requirements for the 2025 processing unit and integrated input/output attachment features, including the associated I/O devices, are supplied through the 2025 processing unit.

The ac service into the 2025 processing unit is 208/230V, 60 amps, 3-phase, 60 Hz ac for domestic machines. For World Trade machines, provision is made for 50 Hz, 195/220/235V, delta input, or 50 Hz, 380/408V, Y-input.

The dc supplies are ferroresonant for all levels.

The dc supplies are sequenced. The ac power to the 2311 disk drives and the 2560 MFCM is also sequenced.

Some of the power supplies and associated components are used only with certain integrated I/O attachments. Where possible, these components are specified in feature groups, and are installed only when the associated features are installed.

The following is a listing of the power supplies by group.

Basic Power Group:

+3 50A	
-3 @ 30A	
+6 @ 40A	
+12 @ 13A	
-12 @ 13A	
-30 @ 8A	Core storage
7.25V ac @ 2	Console indicators
41V ac @ ---	Meter power pack
115V ac @ 15A	Convenience outlets and 1052 motor
+24 @ 4.5A	Sequence circuitry

Ferrotransformer T1 Supplies:

+48 @ 3A	Console typewriter, communications

Power requirements supplied from the processing unit for integrated I/O attachment devices are as follows.

1403/2540 Power Group:

-6 @ 4A
-20 @ 4A

1403 Power Group:

+6 @ 16A Hammer drivers
+60 @ 20A Hammer drivers

2311 Power Group:

-36 @ 2A

2560/Communications Power Group:

+3 @ 45A
+6 @ 32A

2560 Power Group:

+20 @ 1A

5.2 INPUT POWER

Input power for domestic installations is 208 volts ±10% or 230 volts ±10%, 60 ±.5 hertz, 60-amperes three-phase four-wire (the fourth wire is equipment ground) shielded cable. The shield and ground wire are bonded to the input line filter case at the cable entry point.

Input power for World Trade installations is 200, 220, 235/380, or 408 volts ±10%, 50 ±.5 hertz, 60-amperes three-phase five-wire shielded cable (the fourth wire is neutral for a WYE system and not used on DELTA, and the fifth wire is equipment ground. The shield and ground wire are bonded to the input line filter case at the cable entry point. An autotransformer is provided for 200 volts, 235 volts, or 408 volts, 50 hertz inputs.

Power supply logics YA 011, YA 092, and YA 101 show input connections to voltage sensitive units and YA 031 shows the power on/off sequence. The 2025 power supply is described in detail under Power Supply in the IBM 2025 FE Theory of Operations Manual, Form Y24-3527.

5.3 POWER CONVERSION

Ferroresonant regulators feeding full wave bridge rectifiers are used to transform the systems ac input voltage to the dc voltage required by the series regulators and the special power requirements. The special power requirements do not require close regulation.

5.4 AC OUTPUTS

5.4.1 CONVENIENCE OUTLETS

For domestic machines, two convenience outlets provide 115 volts, 60 hertz, single

phase, at a maximum of 15 amperes for the CPU. For World Trade, two convenience outlets provide 200, 220, or 235 volts at 8 amperes for the CPU. Integrated units can draw up to 8 amperes per unit. The convenience outlets for the CPU and the integrated attachments cannot exceed a total of 15 amperes.

5.4.2 BLOWERS

The CPU has three blowers in the power supply tower, three blowers per SLT gate, and three blowers in each M2-I unit. These blowers require 208 or 230 volts, 60 hertz, or 220 volts at 50 hertz, single phase.

5.5 DC OUTPUTS

The power system of the 2025 supplies dc outputs as shown in Figure 5-1.

All dc voltages must be within the tolerances indicated in Figure 5-1 (excluding transient noise) at any card socket in the CPU. Therefore, each power supply must maintain its output voltage in accordance with its individual performance specification. The distribution tolerance must not exceed ±2% within the CPU and devices with reference established at the point of the external entry into the device.

5.5.1 MARGINAL CHECKING JACK RECEPTACLE (P1)

A jack receptacle (P1) located on the 2025 relay panel provides +12 volts for marginal checking the 2540 (logic YA 241).

5.6 POWER ON/OFF SEQUENCING

See timing power supply logic YA 031.

5.6.1 POWER ON/OFF OF CPU AND INTEGRATED I/O UNITS

5.6.1.1 +6, -3, +3, and -30 Voltages

The +6, -3, and +3 voltages must be within a sensed percentage of their rated level prior to bringing up the -30 volts used by storage. The -30 volt supply must be down to or below a sensed level before removing +6, +3, or -3. Whenever the +6 volt supply is between +5.4 volts and +2.0 volts for more than 100 ms, -30 volts should be dropped to less than -10 volts. Any loss of the +6 volts should result in the removal of -30 volts from the BSM (basic storage modules).

5.6.1.2 +6, +3, -3, and +60 Voltages

The +6, +3, -3, and +60 volts direct must be up within a sensed percentage of their rated level prior to applying the +60 volts

Supply Rating	Maximum Current Permitted (Avg.)	Power Supply Location No.	Tolerance at Circuits	Setting ±0.5%	Position	Feature
+12V 13A	11.7 A	8	±4%	12.24	PS-TB1-2, TB1-5	Basic
-12V 13A	13.0 A	3		12.24	PS-TB1-2, TB1-5	Basic
- 3V 30A	30.0 A	6		3.01	*A-LBA1	Basic
- 6V 4A	4.0 A	1		6.24	PS-TB1-5, TB1-2	1403, 2540
+ 3V 45A	42.0 A	2		3.12	PS-TB1-2, TB1-5	2560, Comm
-30V 8A	8.0 A (9.0A at 34.5V)	12		(Per Mem Spec)	**M2ILB	Basic
***+ 6V 40A	47.0 A	10	±4%	6.02	*A-LBA1	Basic
+60V 20A	20.0 A	14	±10%	N/A	N/A	1403
+ 6V 16A	15.5 A	11	+4%			
			-7%	6.02	TB25-15, 13	1403
-30V 2A	2.0 A	4	±4%	36.72	PS-TB1-2, TB1-5	2311
-20V 4A	4.0 A	Developed from T1	±10%	N/A	N/A	Basic
+24V 4.2A	4.2 A	Developed from T3	±15%	N/A	N/A	Basic
+48V 3A	3.0 A	Developed from T1	±10%	N/A	N/A	Basic
+ 6V 32A	30.0 A	5	±4%	6.24	PS-TB1-2, TB1-5	2560, Comm
+ 3V 50A	50.0 A	9	±4%	3.01	*A-LBA1	Basic
+20V 1.0A	1.0 A	Developed from T7	±10%	N/A	N/A	2560

*See logic page YA251 ** See logic page YA271 *** +6V @ 50A on machines with EC133539

Figure 5-1. DC Outputs

controlled output to the 1403. This makes the three-phase ac power available for the motors. The +60 volts controlled must be down to or below a sensed level before removing other dc voltages used by the 1403.

5.6.1.3 2311 DC Power

The first dc power on the 2311 is the +6, +3, and -3 volts; then the ac power-on control line is activated. The first step in power-off is to deactivate the 'power-on control' line, remove ac power, and finally remove dc voltages. The 2311 heads extended prohibit sequence down until the heads retract or an EPO occurs.

5.6.1.4 2540 DC Power

The -20 volt dc power to the 2540 is applied at the same time as the -30 volts is supplied to main storage.

5.6.1.5 2560 AC Power

The ac to the 2560 is applied after the dc voltages and removed before the dc voltages.

5.6.2 POWER ON/OFF TO CHANNEL CONTROLLED I/O UNITS

A maximum of eight I/O control units can be controlled by the CPU channels. These units are powered up after all CPU and integrated I/O units have been sequenced on. The channel controlled I/O units step their power on one at a time. When the last I/O unit has completed its power-on sequence under remote control and the memory temperature is above the low limit, the system power-on reset line is deactivated and the system power-on light is turned on.

Power off occurs in the same sequence as power on, with the following exception: if the 2311 heads are extended at the time of power off, the power-down sequence is prohibited until the heads retract or an EPO occurs.

5.7 EMERGENCY POWER-OFF (EPO)

Operation of the emergency-pull switch removes primary power within two seconds from the CPU and every I/O control unit attached to a channel simultaneously, and without stepping down. An emergency power-off can cause the data in main storage to be lost. Operation of the emergency-pull switch sets a mechanical latch within the switch mechanism that must be manually reset before power can be restored.

5.8 OVERCURRENT, UNDERVOLTAGE, AND OVERVOLTAGE SENSE

When an overcurrent or an overvoltage condition occurs on dc power supplies with an overcurrent CB, the following events take place.

1. A circuit breaker is tripped and the CB trip light is on.
2. A normal power-off sequence is initiated.
3. A power-check light is energized on the console.

The dc power supplies not provided with an overcurrent CB are fused for overcurrent protection. Loss of the supply outputs when system power is on initializes a normal power-off sequence and turns on the power-check light on the console panel. Loss of the +24 volt supply causes a random power off and does not light the power check light.

Loss of any dc supply (except the +24 volt) below its sensed rating initiates a normal power-off sequence and lights the power-check light on the console panel.

The 20-volt, 24-volt, 36-volt, 48-volt, and 60-volt dc supplies do not require overvoltage circuits.

5.8.1 SYSTEM-RESTART/POWER-CHECK LIGHT RESET

System restart can not be accomplished without first pressing the power-off button to reset the power-check light. Inability to reset the power-check light indicates the power failure is caused by an overcurrent, overvoltage, or thermal-trip condition. The system power-off button must be pressed after resetting the condition at the power tower.

5.9 THERMAL SENSING

Thermal sensing switches are provided on logic gates, main storage, and power supply areas. Whenever any of these thermal switches senses a temperature in excess of their specified limit, the following occurs.

1. A normal power-off sequence is initiated.
2. The thermal-trip light on the power tower is turned on and remains on until the condition is corrected and the thermal reset switch is actuated.
3. The power-check light on the console is turned on.

5.10 SERVICE CHECKS AND CHECKOUT PROCEDURES (FIGURE 5-2)

Continued problems with the 2025 power supplies could be an indication that:

1. Line in use is out of specification. The voltage must be within ±10% of rated input line voltage. (See Physical Planning Manual, Form C22-6820, for complete requirements.)
2. Transformer taps set for wrong line voltage. If the voltage is ever changed, the correct Feature Bill of Material should be ordered through Plant Field Engineering. These B/Ms contain complete instructions for the 2025 conversion as well as the correct voltage nameplate tags. The voltage nameplate must always reflect the voltage for which the machine is wired. When the B/M is ordered and installed, Machine Level Control Department is advised of the change in the machine voltage wiring.
3. On thermal failures, check blowers and filters for sufficient air flow. Room temperature can also be a factor.

Logic Page	Descripton	Part Number	EC133201	EC133323	EC133539
YA011	Switching Instruction for Input Voltage	2542161			
YA021	Machine Layout Data (Door Side)	2542162	2543021	2470741	
YA022	Machine Layout Data (Gate Side)	2542163		2470739	
YA031	Power "On" - "Off" Sequence	2542164			
YA041	Component Data Location Chart	2542165	2543022		
YA042	Component Data Location Chart	2542166			2470747
YA043	Terminal Location Chart	2542167			
YA061	Connector Reference Chart	2542168			
YA071	External Cable Connections	2542169		2470740	
YA072	External Cable Connections	2542170			
YA091	AC Power Control	2542171	2543023		
YA092	Control Transformer and Conv. Outlet Power Dist.	2542172			
YA101	AC Distribution	2542173			
YA111	AC - Distribution to 1052 and Blower Circuits	2542174			
YA131	1403 AC - Control and Distribution	2542175		2470732	
YA132	Solid State Switch and 1403 Motors	2542191			
YA141	1403 +60V Control and Disteibution	2542176		2470733	
YA151	System Power Control	2542177			
YA161	System Power Control	2542178			
YA171	EPO and PWR "On" Control for I/O Control Units	2542179			
YA181	Voltage Sense Circuits CB Trip Sense Circuits, Over Temperature Circuits	2542180			
YA185	Lamp Supply and Time Meter Circuit	2542181			
YA191	Ferro Mid Pack T1, T2, and Power Supplies PS1, PS4	2542182			
YA201	Ferro Mid Pack T6, T7, and Power Supplies PS2, PS5, PS11, PS12	2542183			
YA211	-3V - Power Supply and Distribution	2542184			
YA221	+3V - Power Supply and Distribution	2542185			
YA231	+6V - Power Supply and Distribution	2542186			
YA241	+12V, -12V - Power Supply and Distribution	2542187			
YA251	DC Distribution to Gate "A"	2542188			
YA261	DC Distribution to Gate "B"	2542189			
YA271	DC Distribution to Gate "C1", Gate "C2" and Gate 01H01-A (Hammer Driver Board)	2542190			
YA112		2539396			
YA182		2470789			

Figure 5-2. Power Supply Logic Pages

5.11 MID-PAC POWER SUPPLY

5.10.1 MID-PAC TROUBLESHOOTING PROCEDURES

The following procedure is recommended for troubleshooting the Mid-Pac power supply. Only the most probable conditions are indicated.

5.11.1.1 High Voltage

Either a defective amplifier card or a shorted series regulator power transistor. To determine which of these is causing the high voltage, remove the amplifier card and press the power-on key just long enough to determine whether voltage is present. Voltage being present indicates that one or more of the power transistors (normally clamped to 0-volts with the amplifier removed) is shorted. If no output voltage is present, the amplifier card is probably defective. It may be necessary to disconnect the output cable and remove the overvoltage card. Never remove the overvoltage card with the dc output cable connected to the module if power is to be applied to the machine.

5.11.1.2 Low Output Voltage

Low output voltage usually is caused by a defective amplifier card.

5.11.1.3 DC Module Circuit Breakers (Individual Tripping)

Either a shorted series regulator power transistor, or a short in the logic wiring (load). To determine which condition is causing the circuit breaker to trip, remove the amplifier card. If the circuit breaker trips with the card removed, the power transistor is shorted. If the circuit breaker does not trip with the card removed, the short is probably somewhere in the load circuits.

CAUTION

The CPU should not be running when tools or scopes are plugged into the convenience outlet.

If necessary, normal processor operation may be interrupted to utilize the convenience outlet by:

1. pressing STOP.
2. connecting tools.
3. pressing START.

5.11.2 SERVICE CHECKS AND CHECKOUT PROCEDURES

5.11.2.1 Mid-Pac DC Outputs

All dc voltages must be within rated tolerances when measured anywhere in the CPU Logic area such as memory units and logic gates. Refer to Figures 5-1 and 5-2 for a chart and reference of the Mid-Pac power system.

Measure and monitor the output voltage at the designated test point for the applicable power supply. Vary the red knurled knob of the potentiometer on the SMS card until the meter reads the specified voltage. Use a Weston 901 meter or equivalent.

Chapter 6. Locations

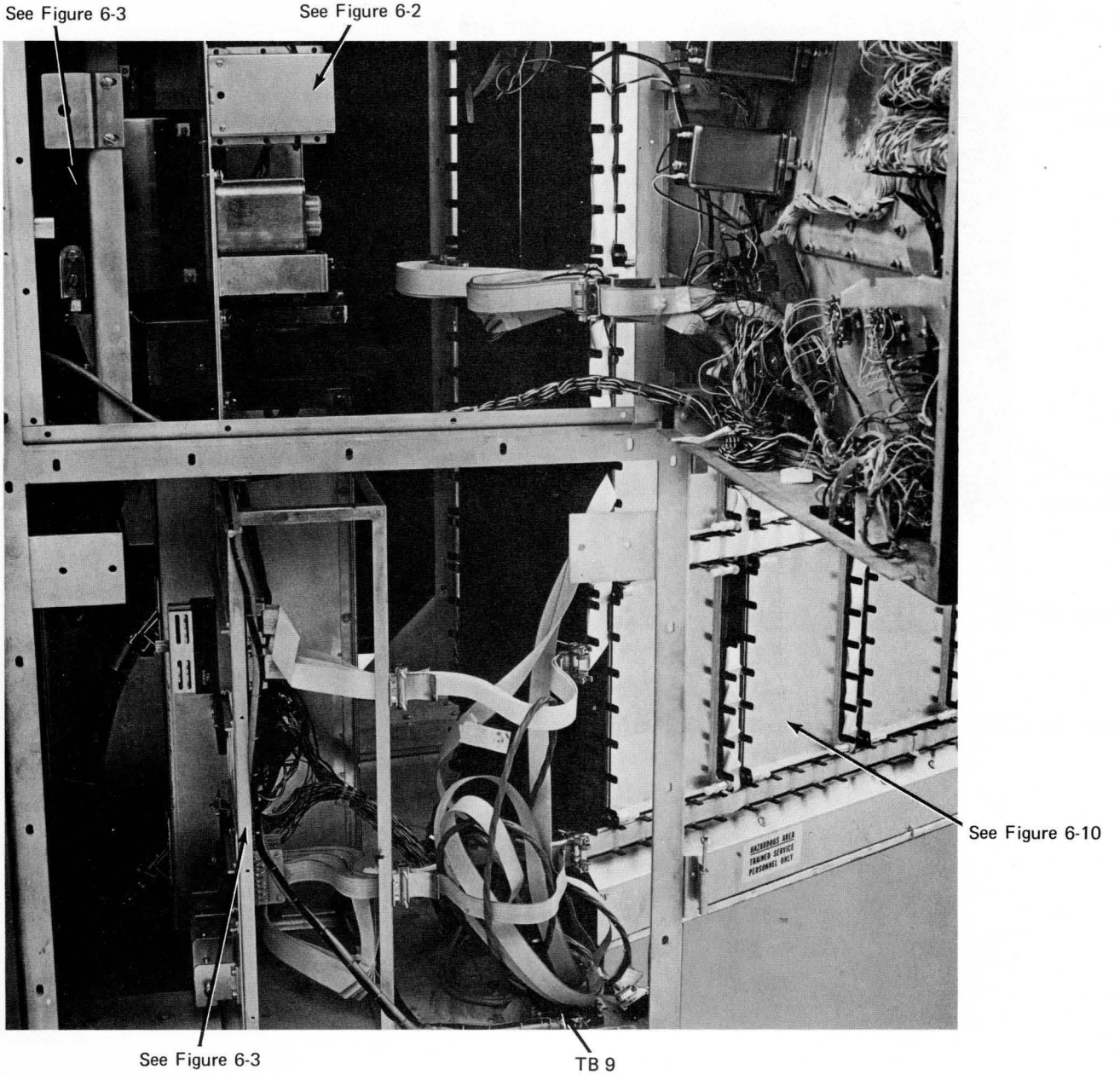


Figure 6-1. E-Gate (Connector Rack)

Chapter 6. Locations

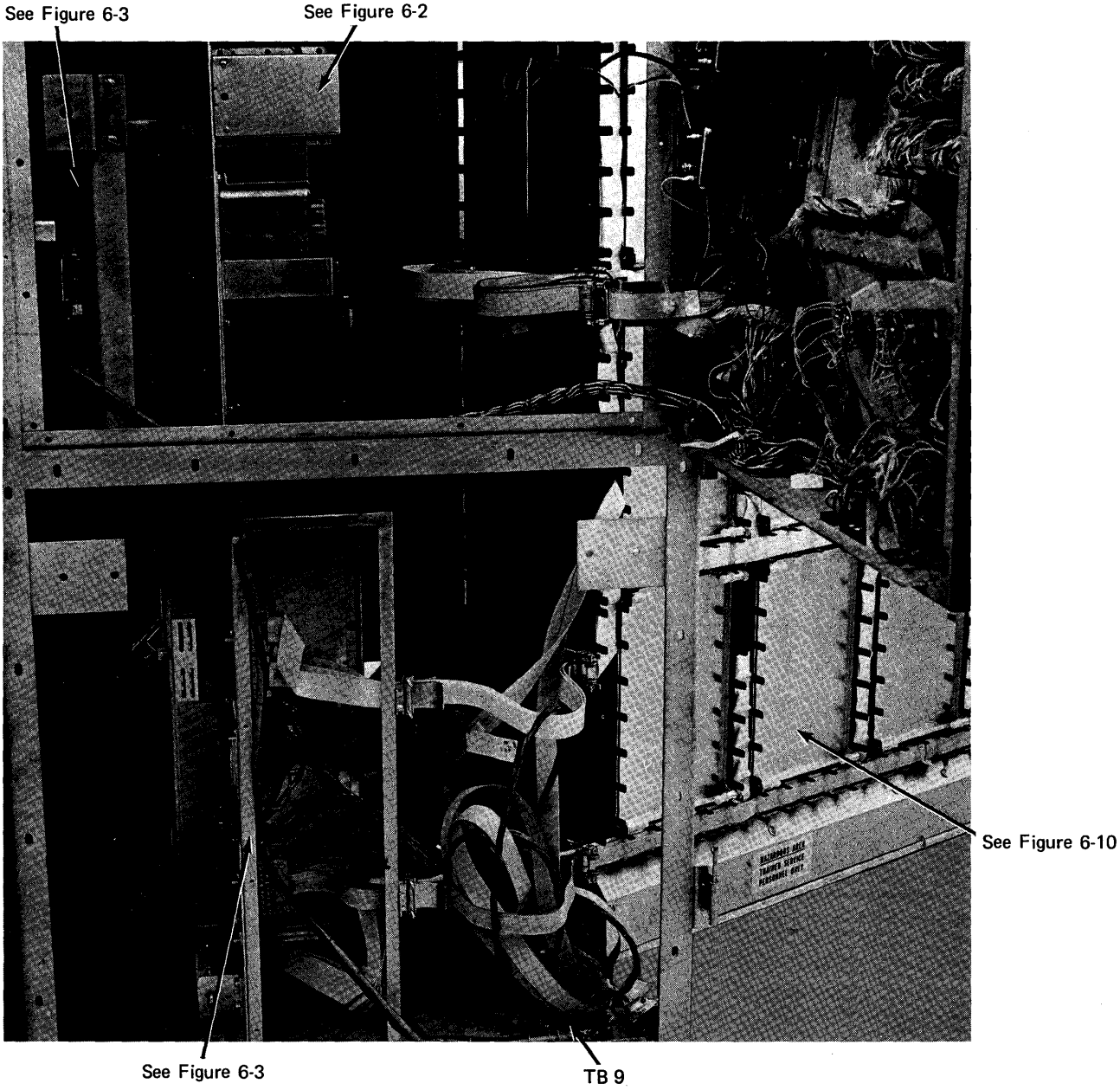


Figure 6-1. E-Gate (Connector Rack)

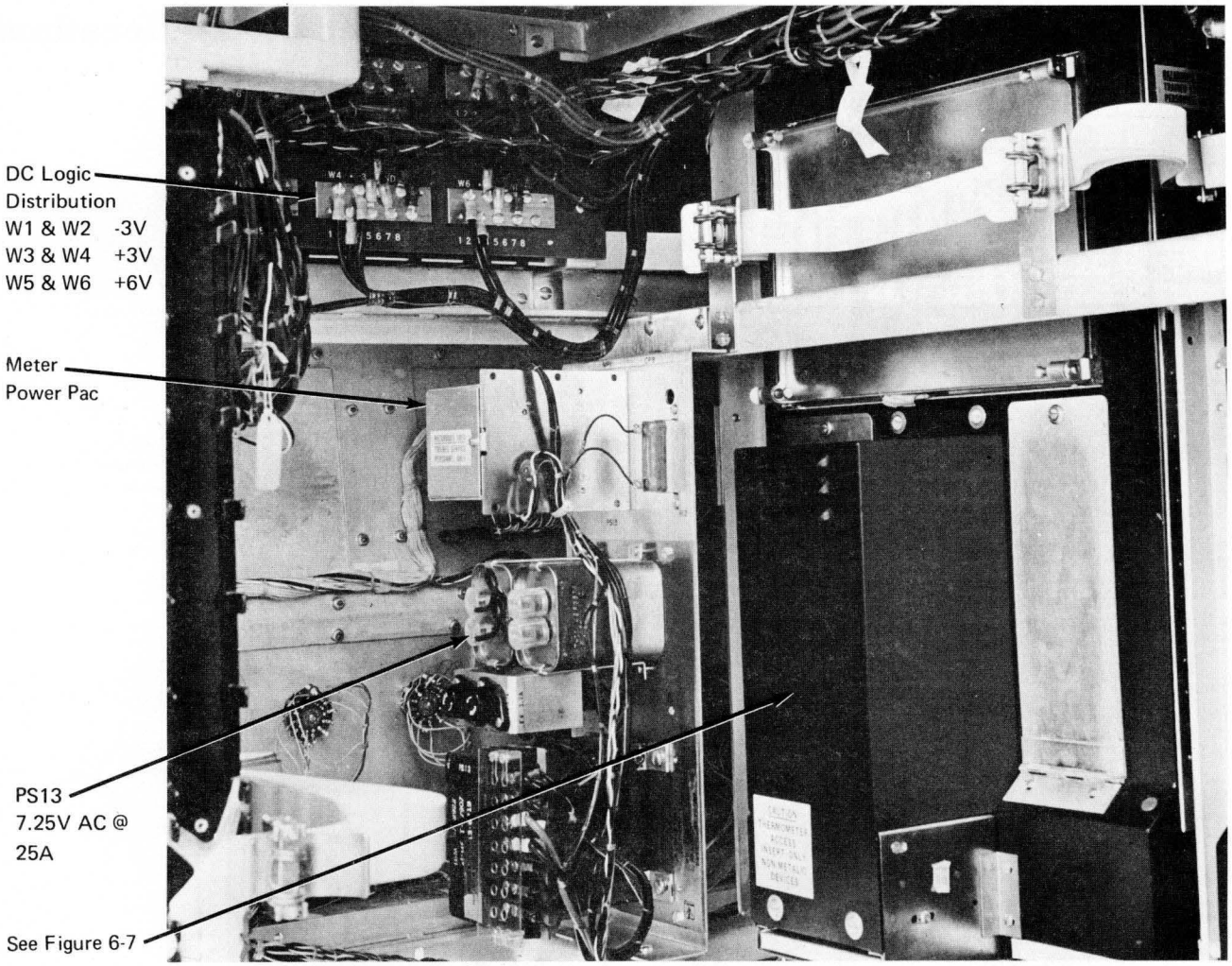


Figure 6-2. DC Distribution and Power Supplies

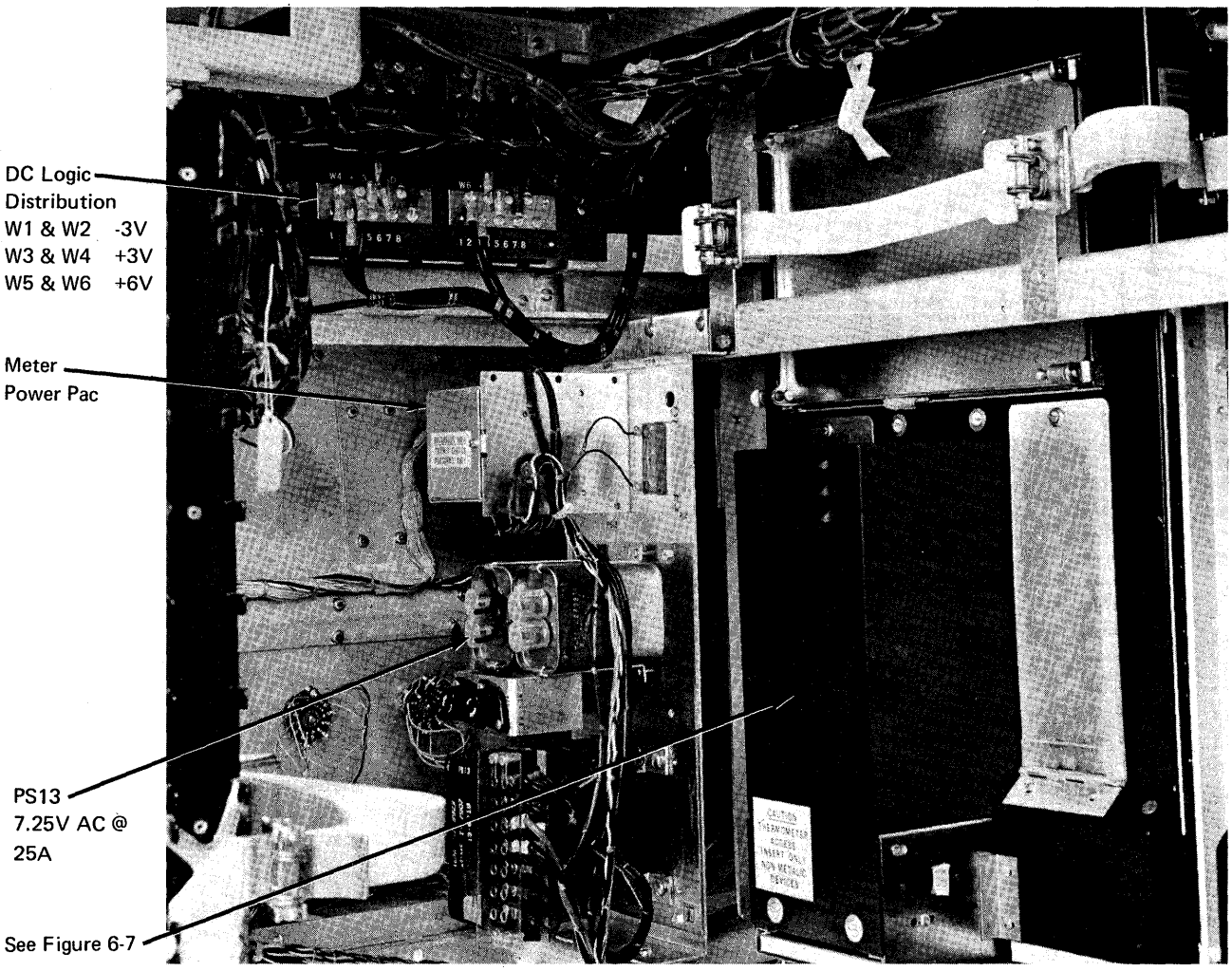


Figure 6-2. DC Distribution and Power Supplies

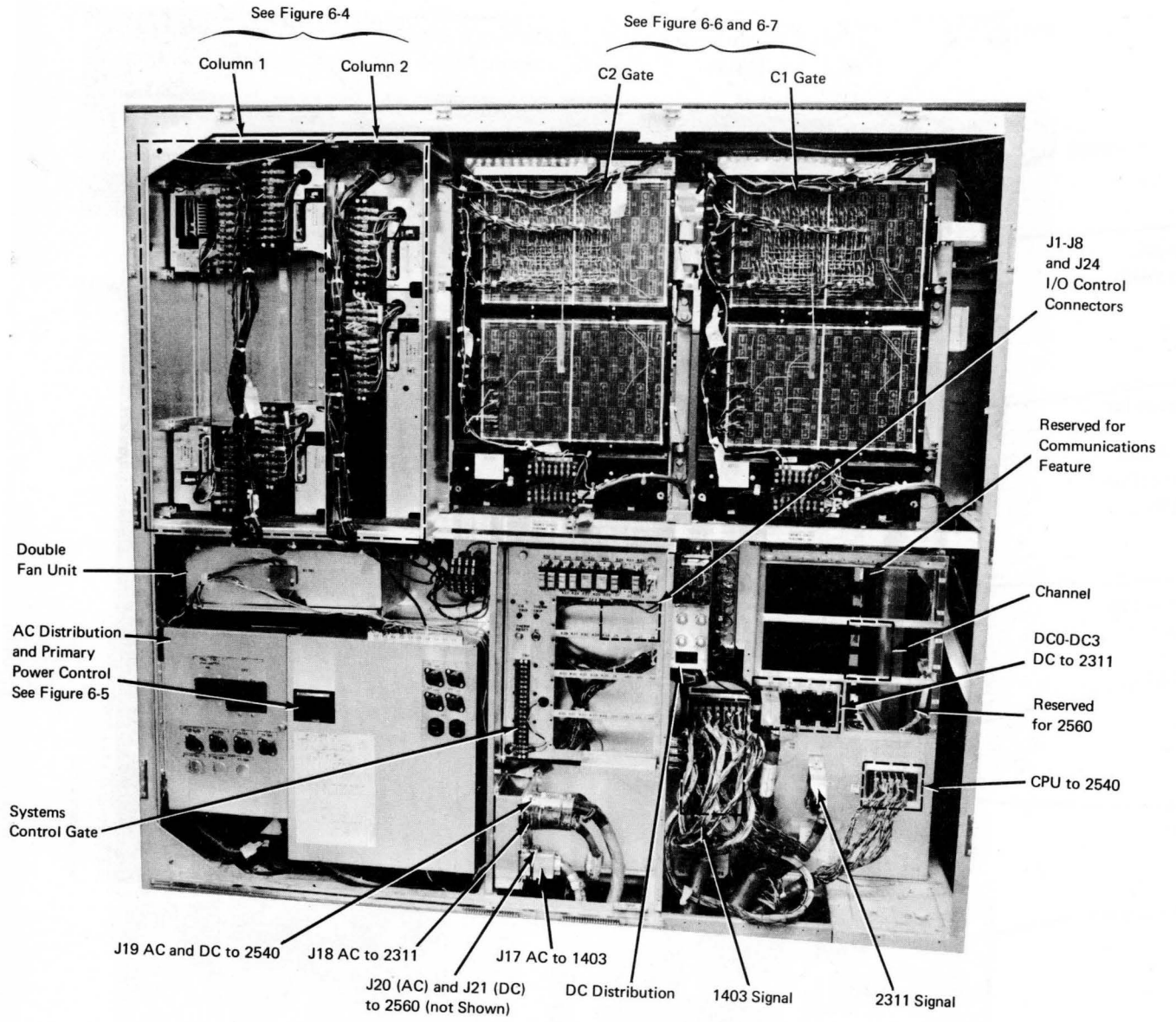


Figure 6-3. Left Side

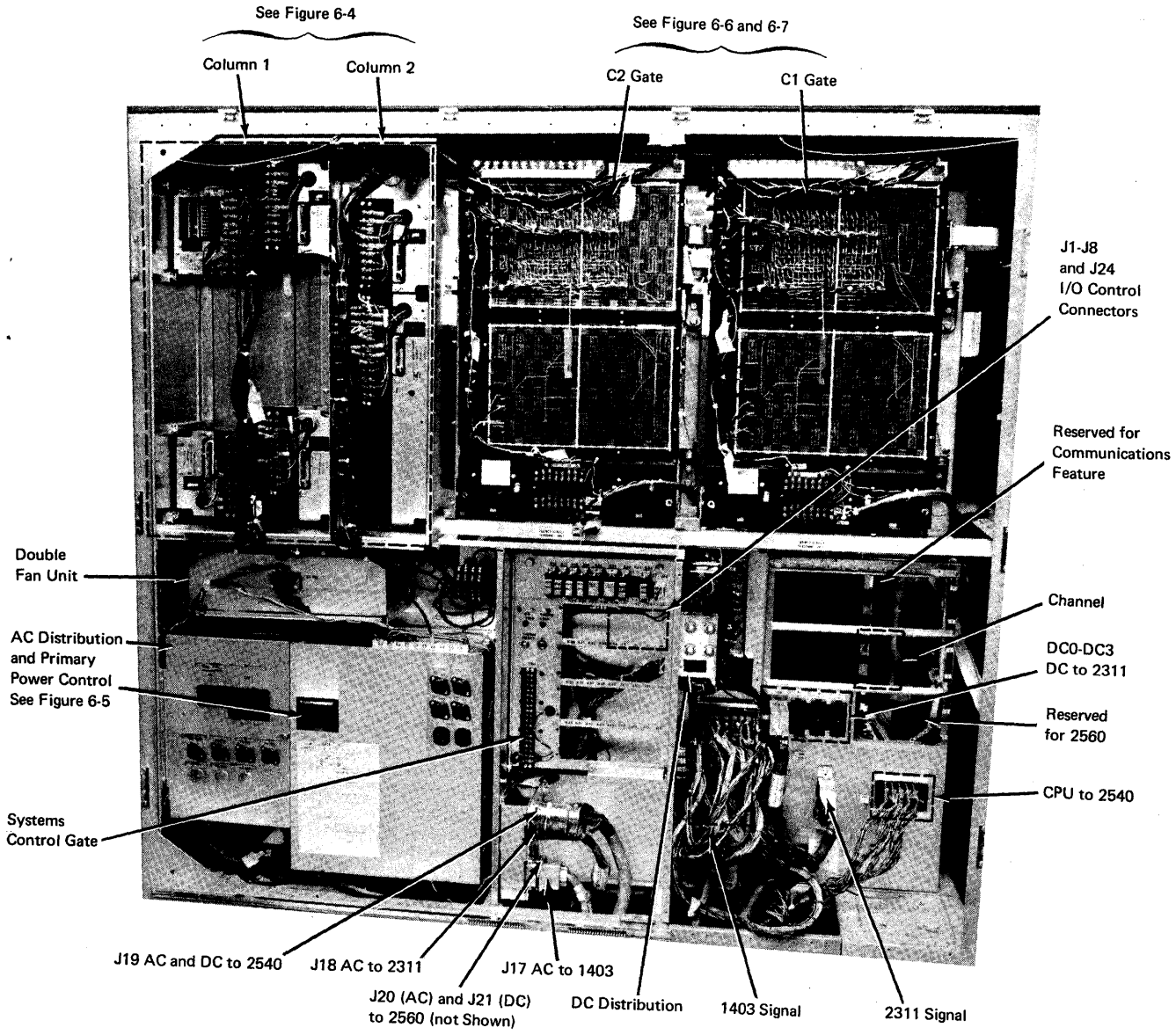


Figure 6-3. Left Side

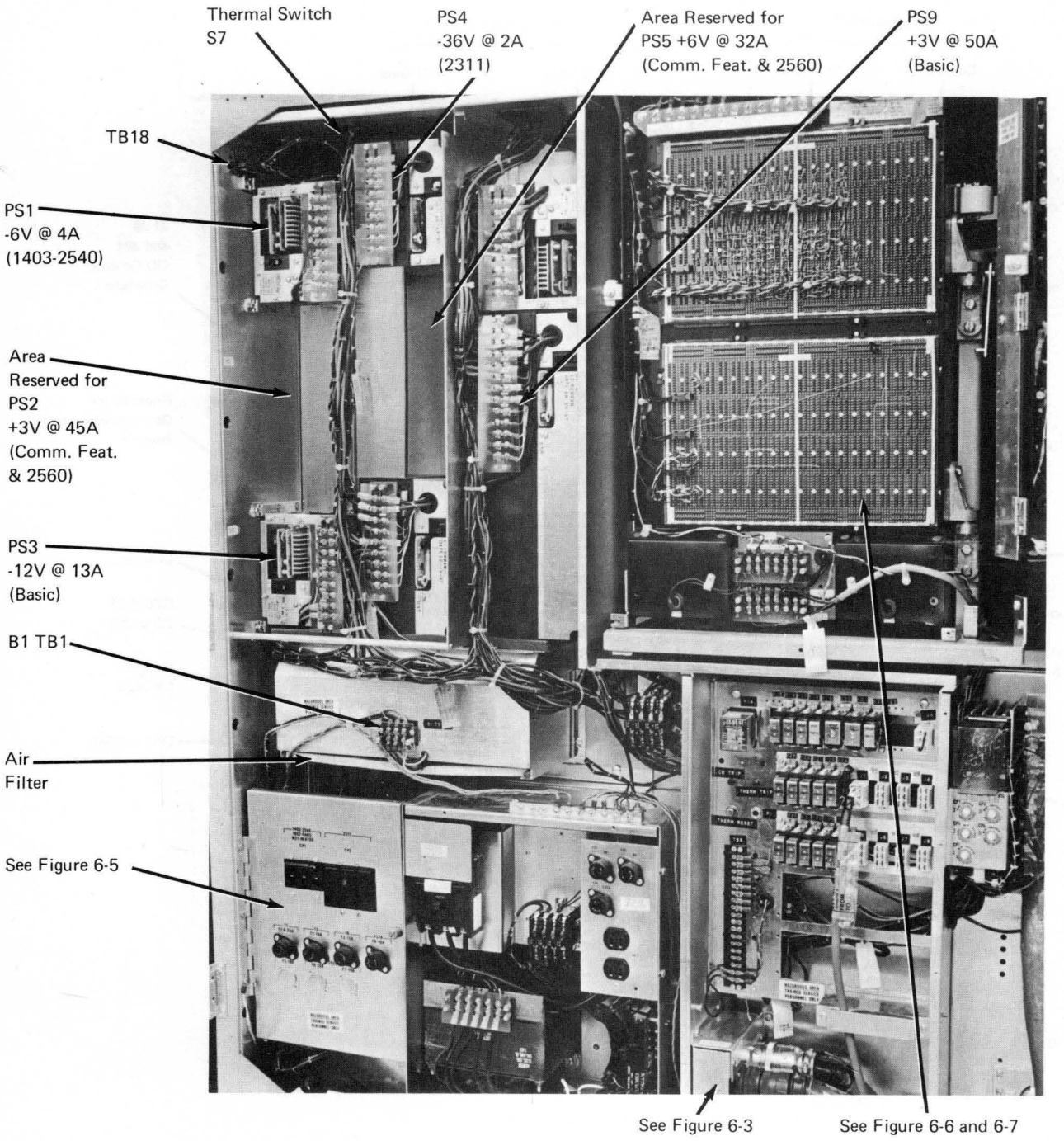


Figure 6-4. Power Supplies (Left Side)

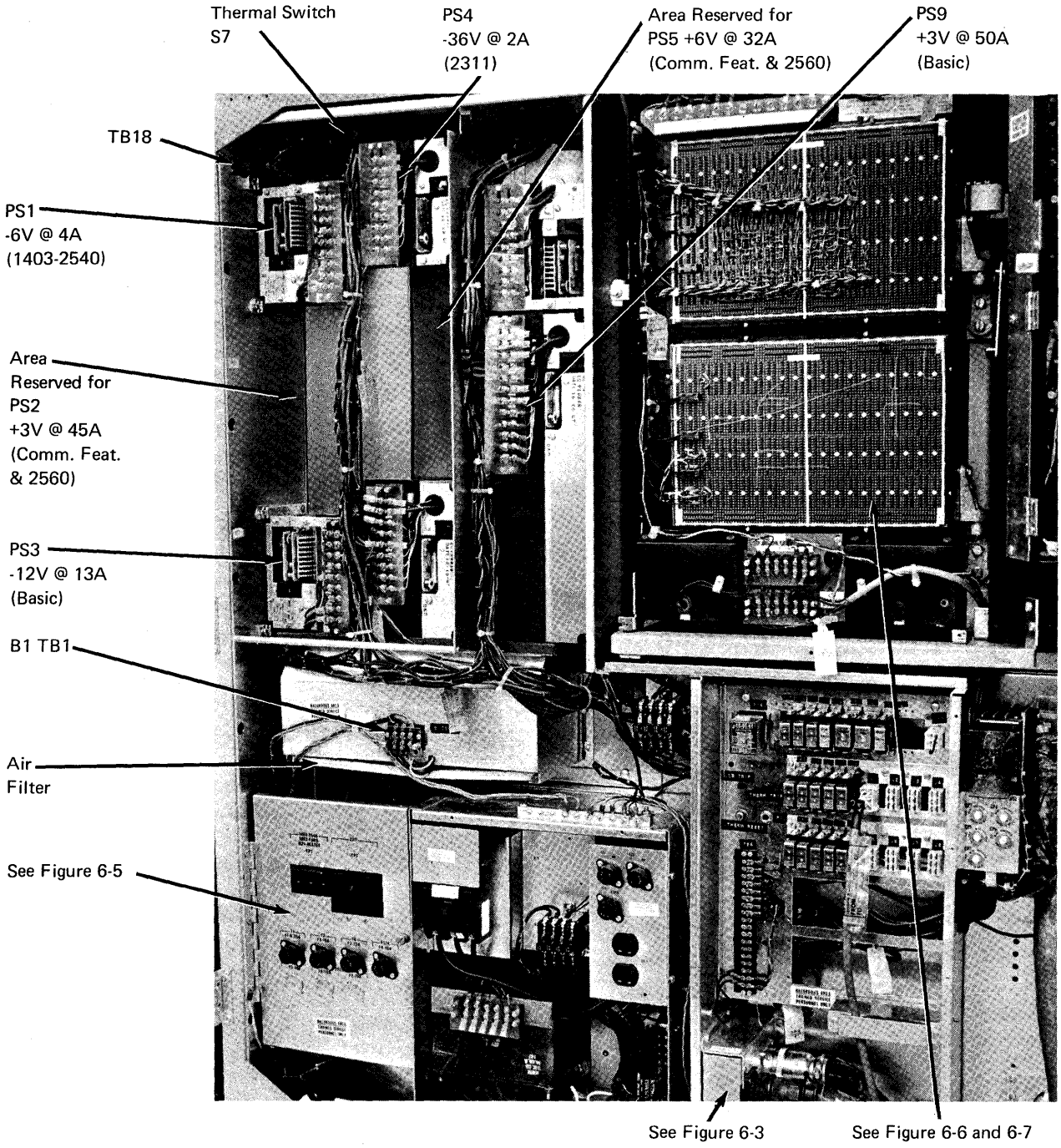


Figure 6-4. Power Supplies (Left Side)

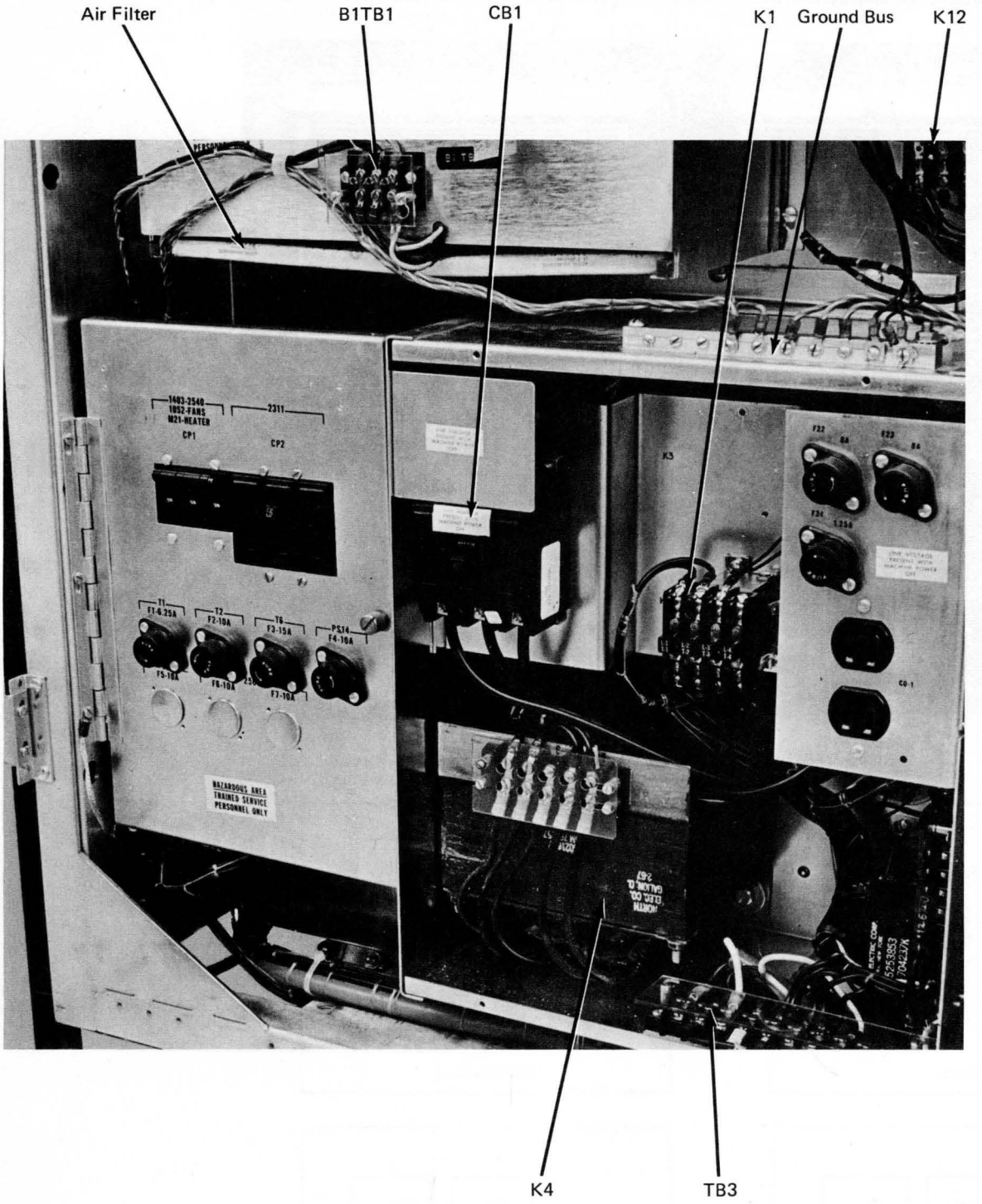


Figure 6-5. Fuses (Lower Left Side)

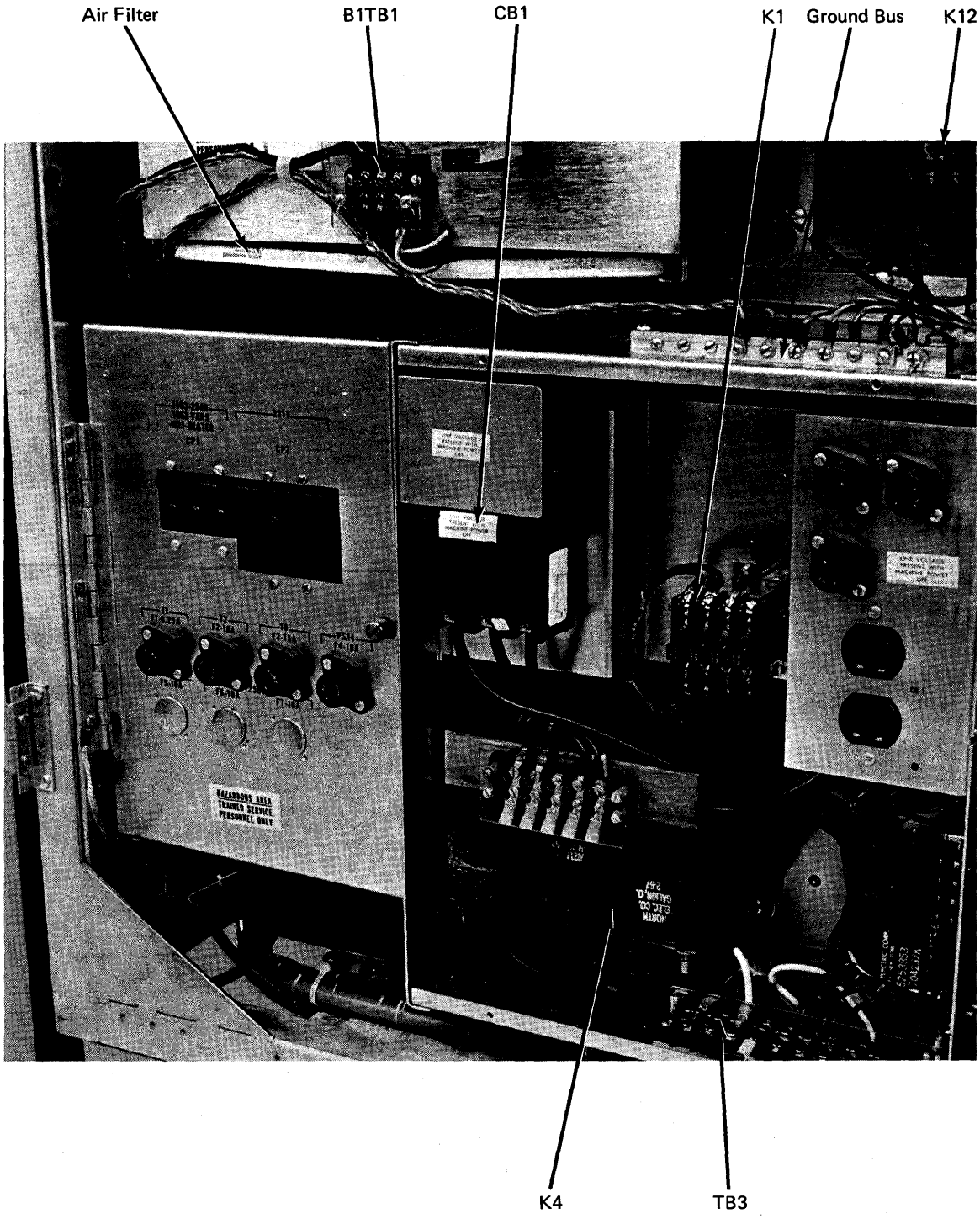
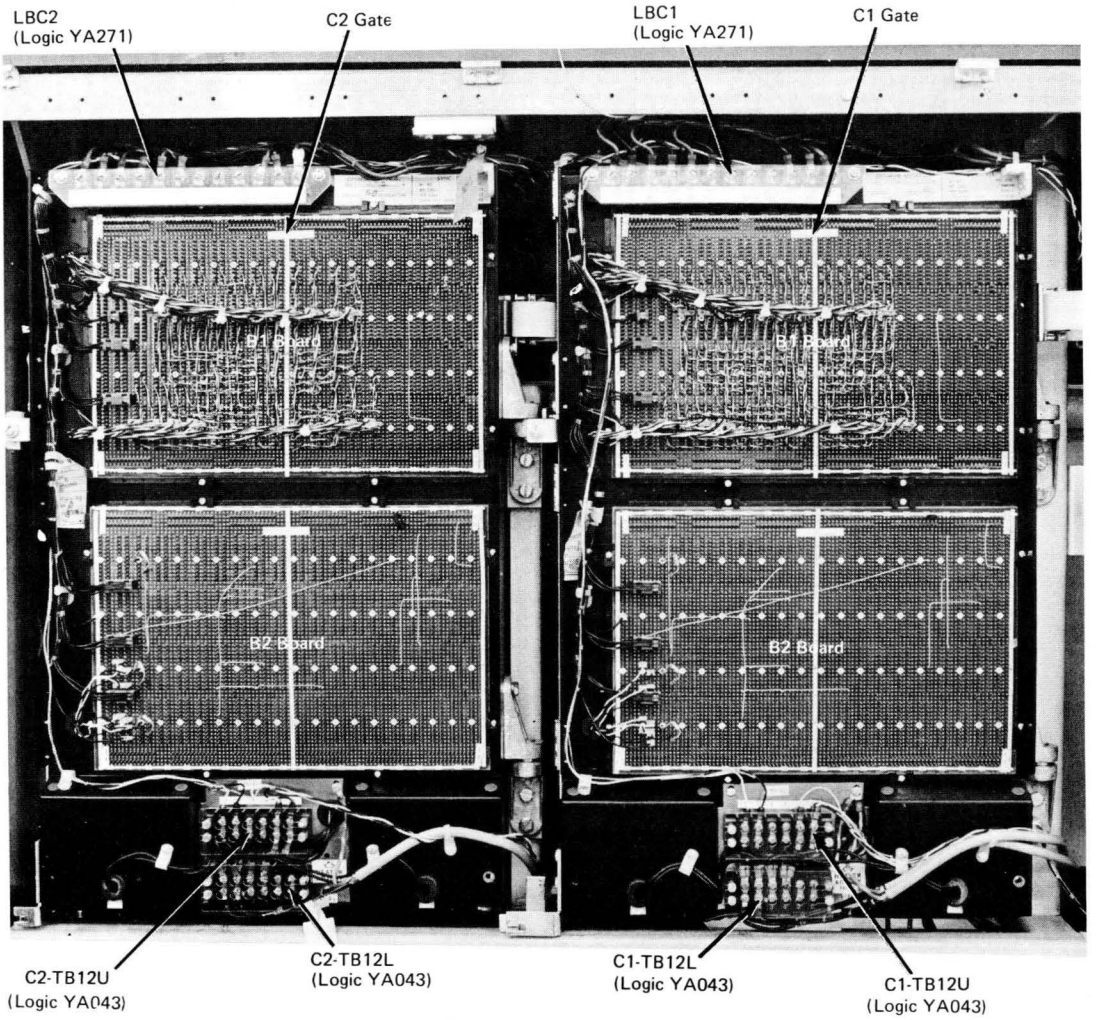


Figure 6-5. Fuses (Lower Left Side)



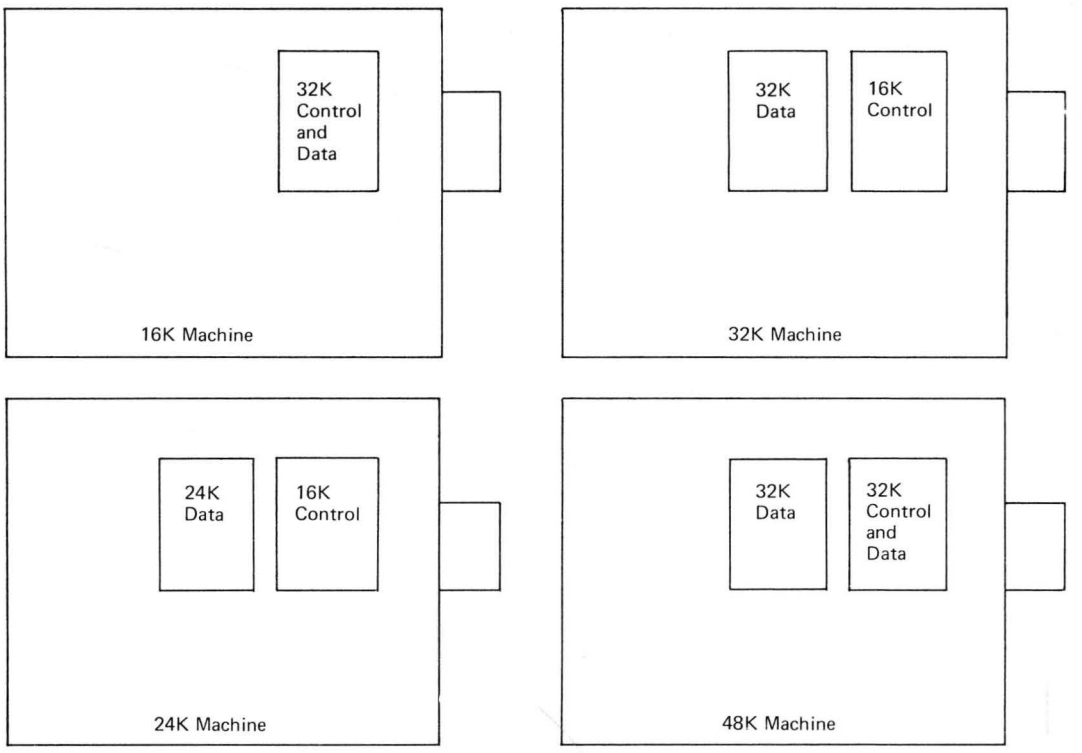
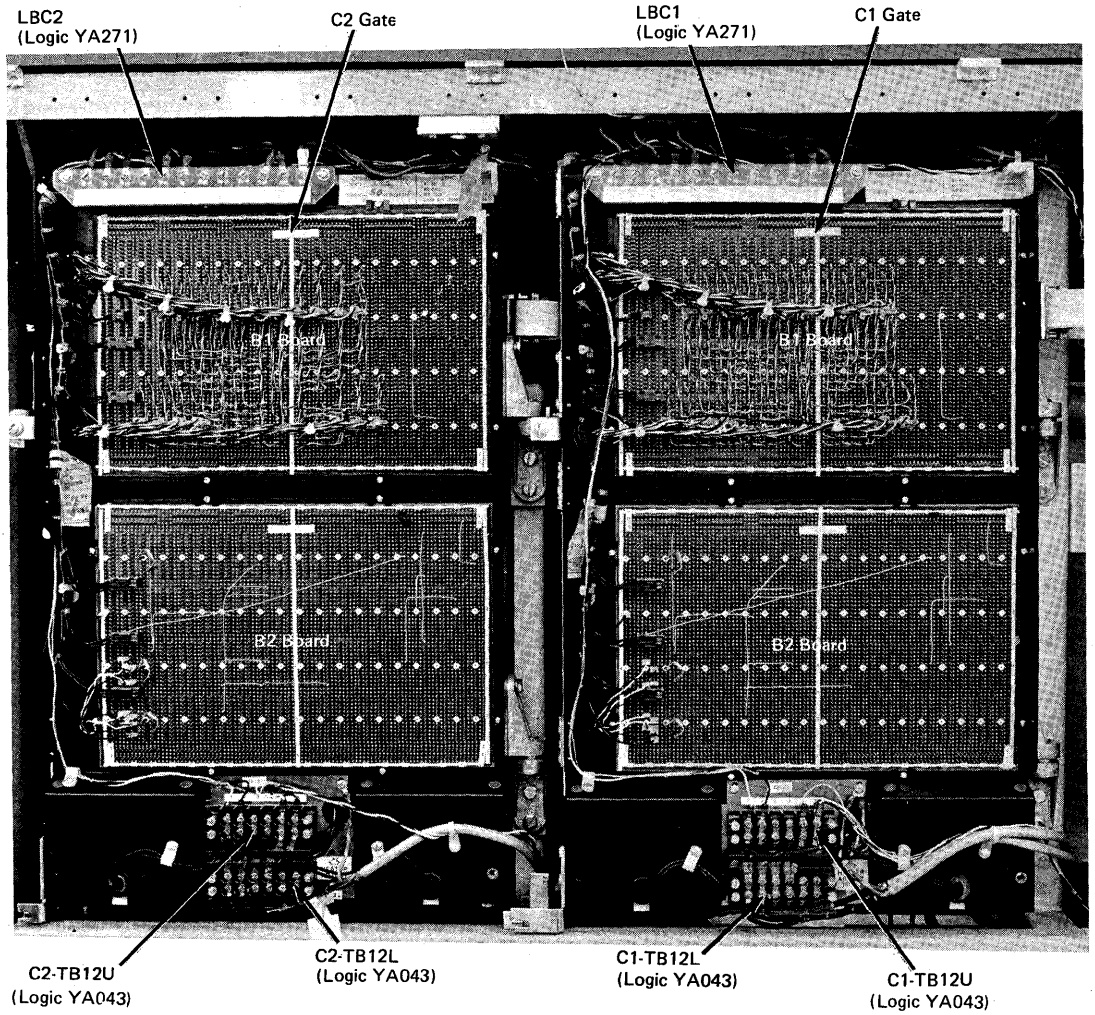


Figure 6-6. Main Storage Units (Pin Side)



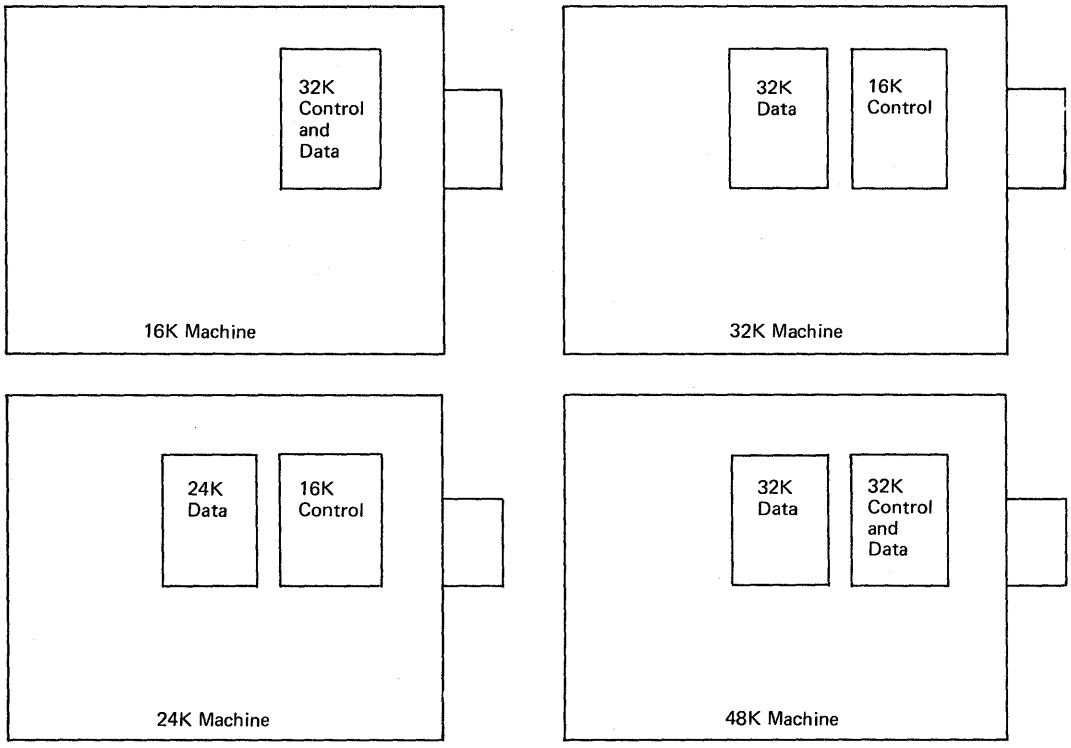


Figure 6-6. Main Storage Units (Pin Side)

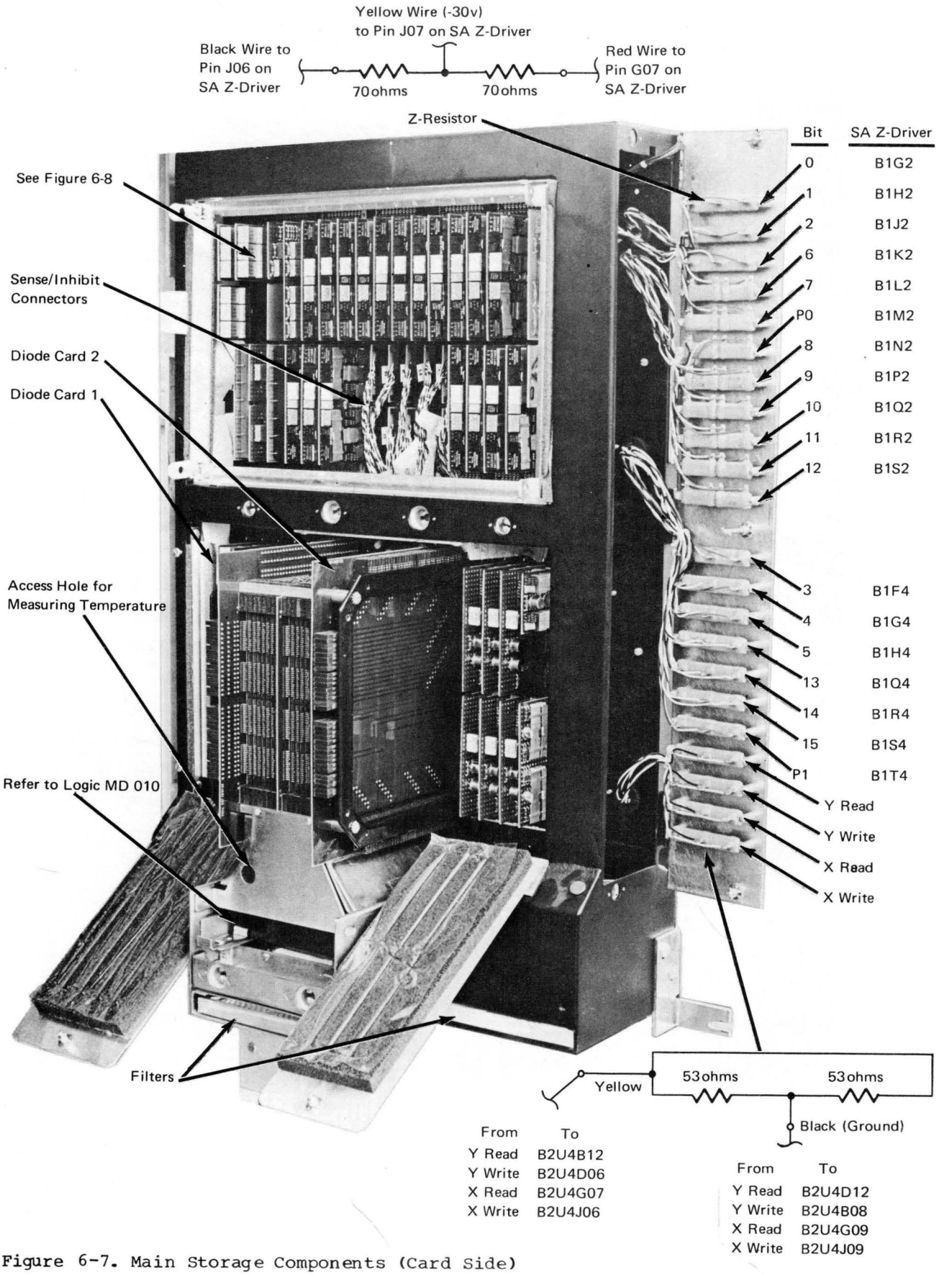


Figure 6-7. Main Storage Components (Card Side)

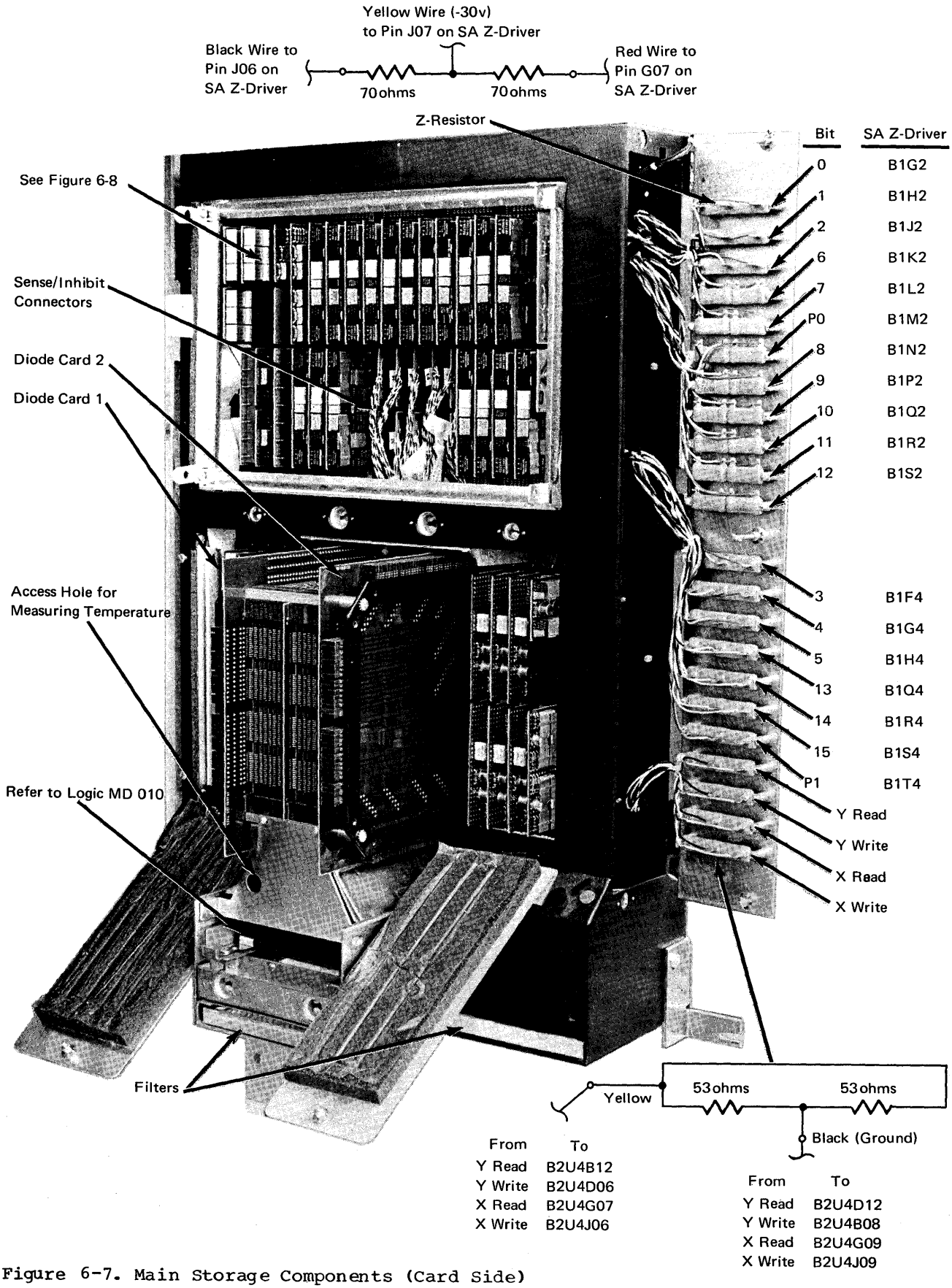


Figure 6-7. Main Storage Components (Card Side)

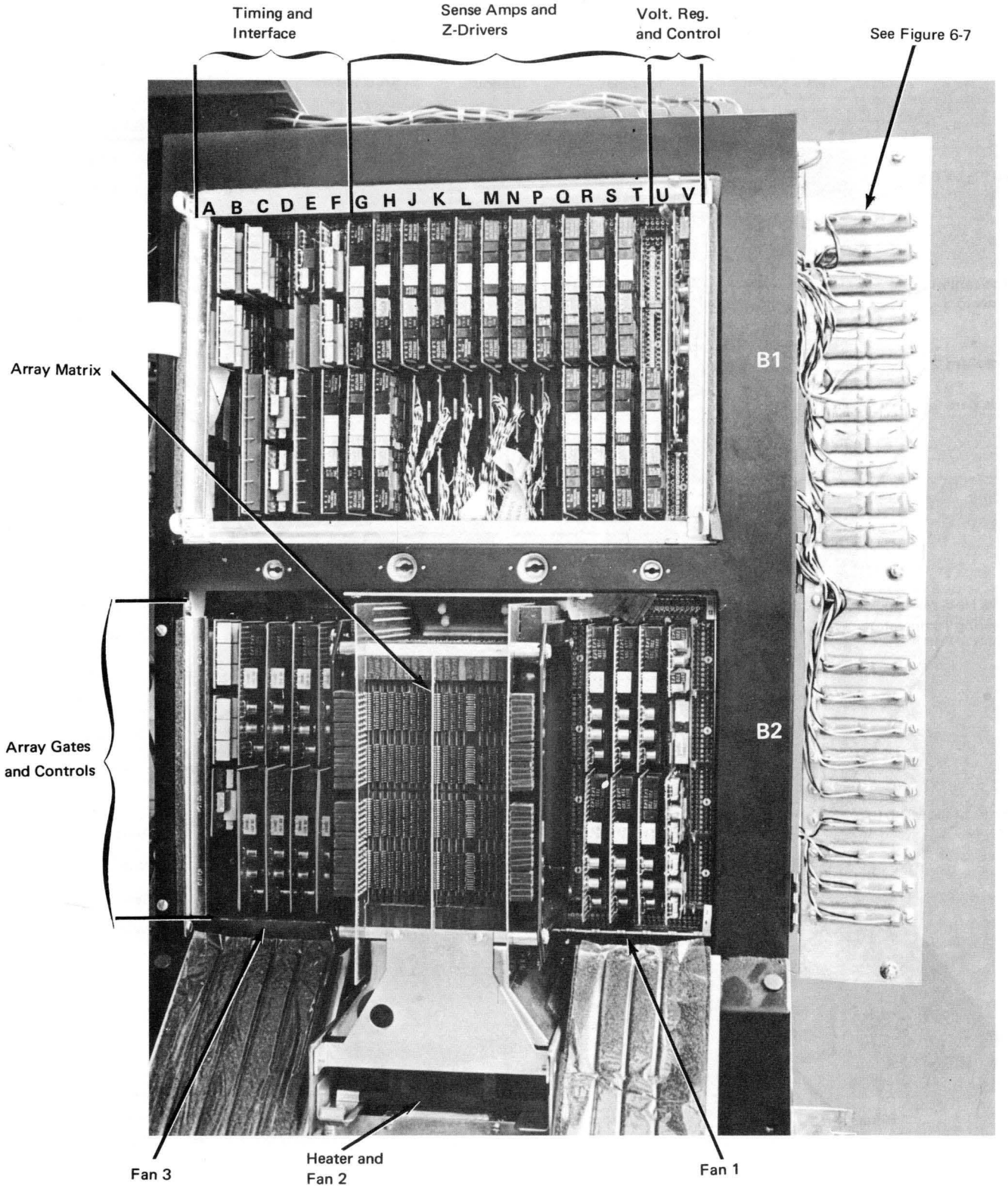


Figure 6-8. Main Storage Components (Card Side)

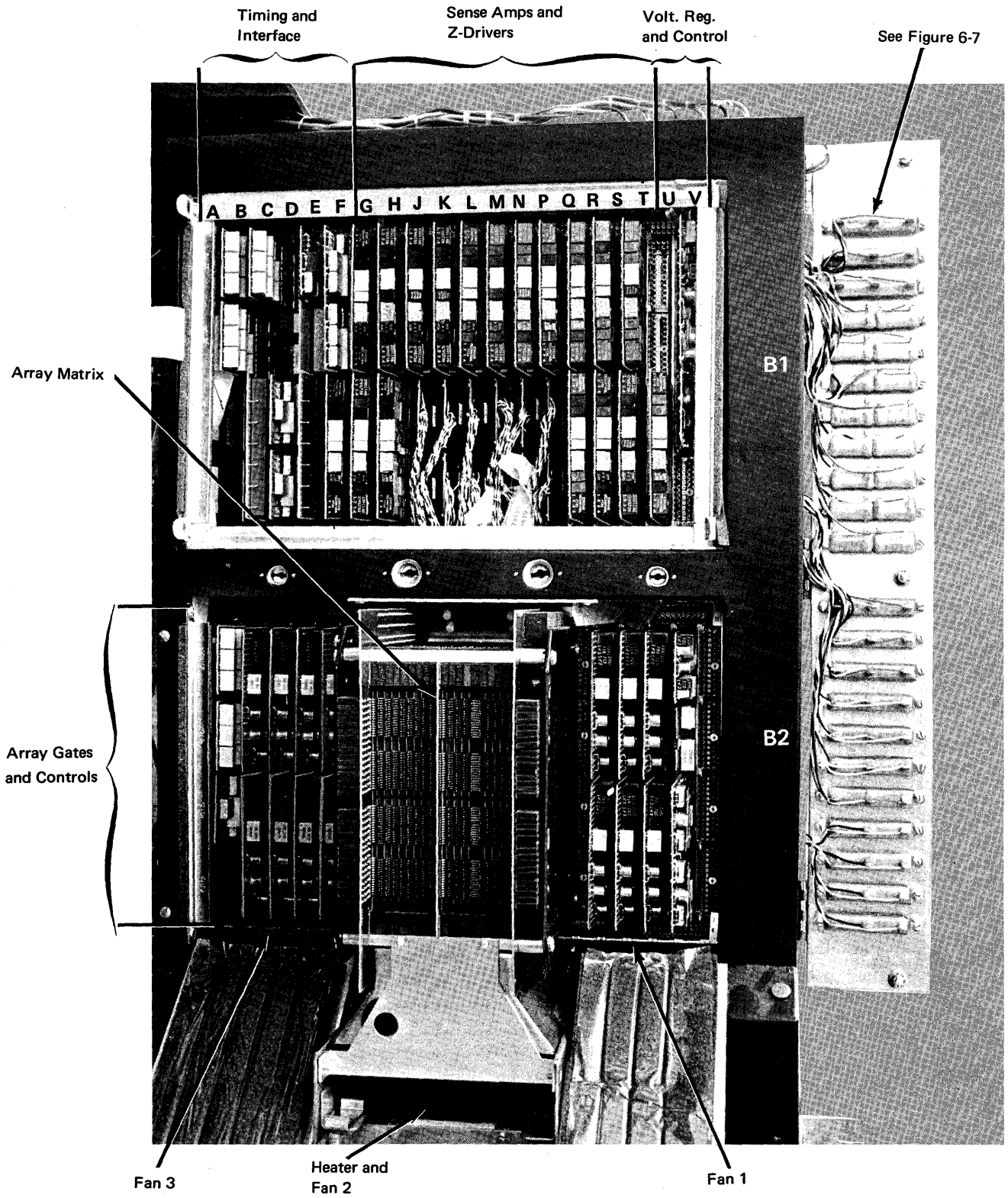


Figure 6-8. Main Storage Components (Card Side)

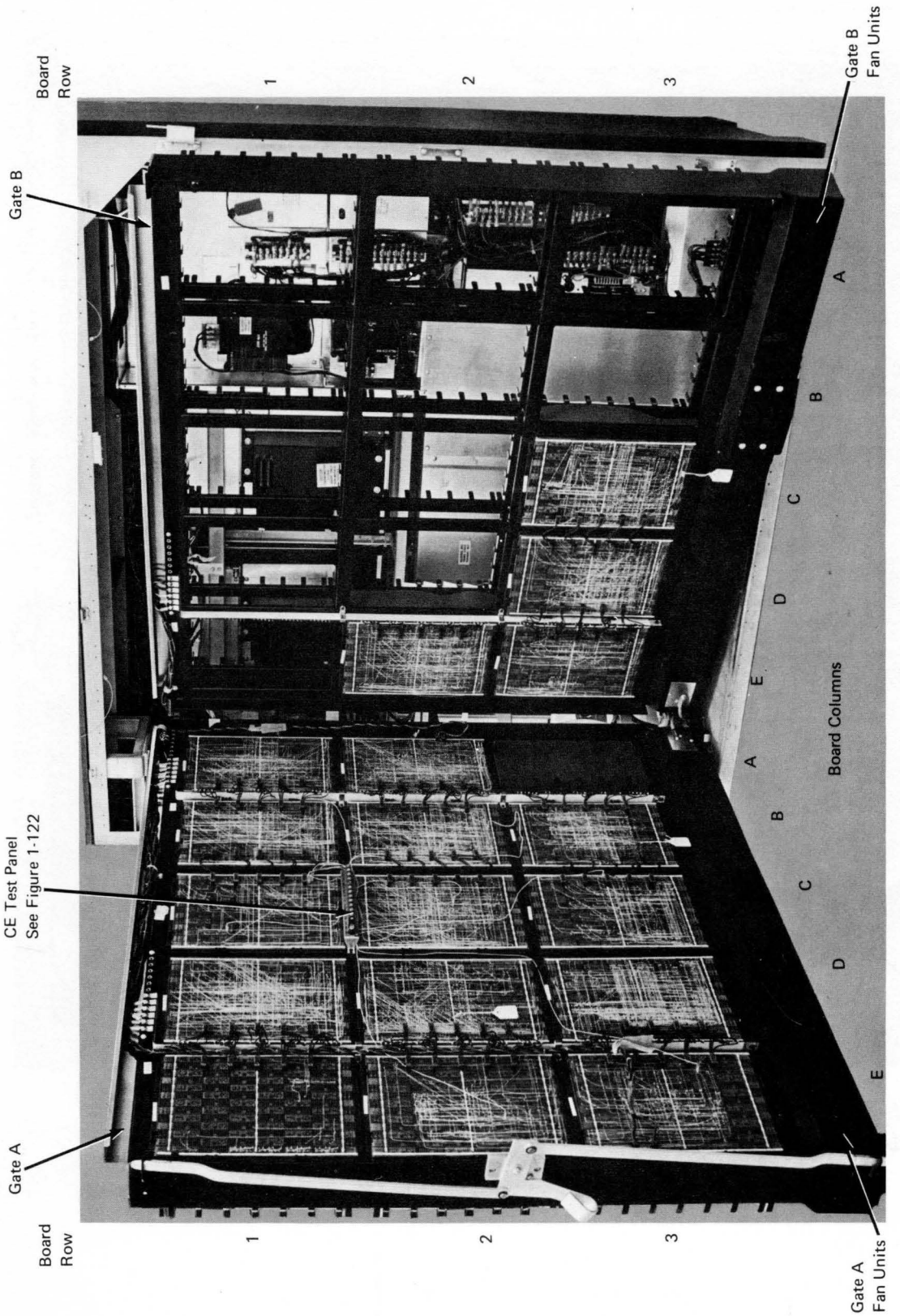


Figure 6-9. Logic Gates A and B (Open)

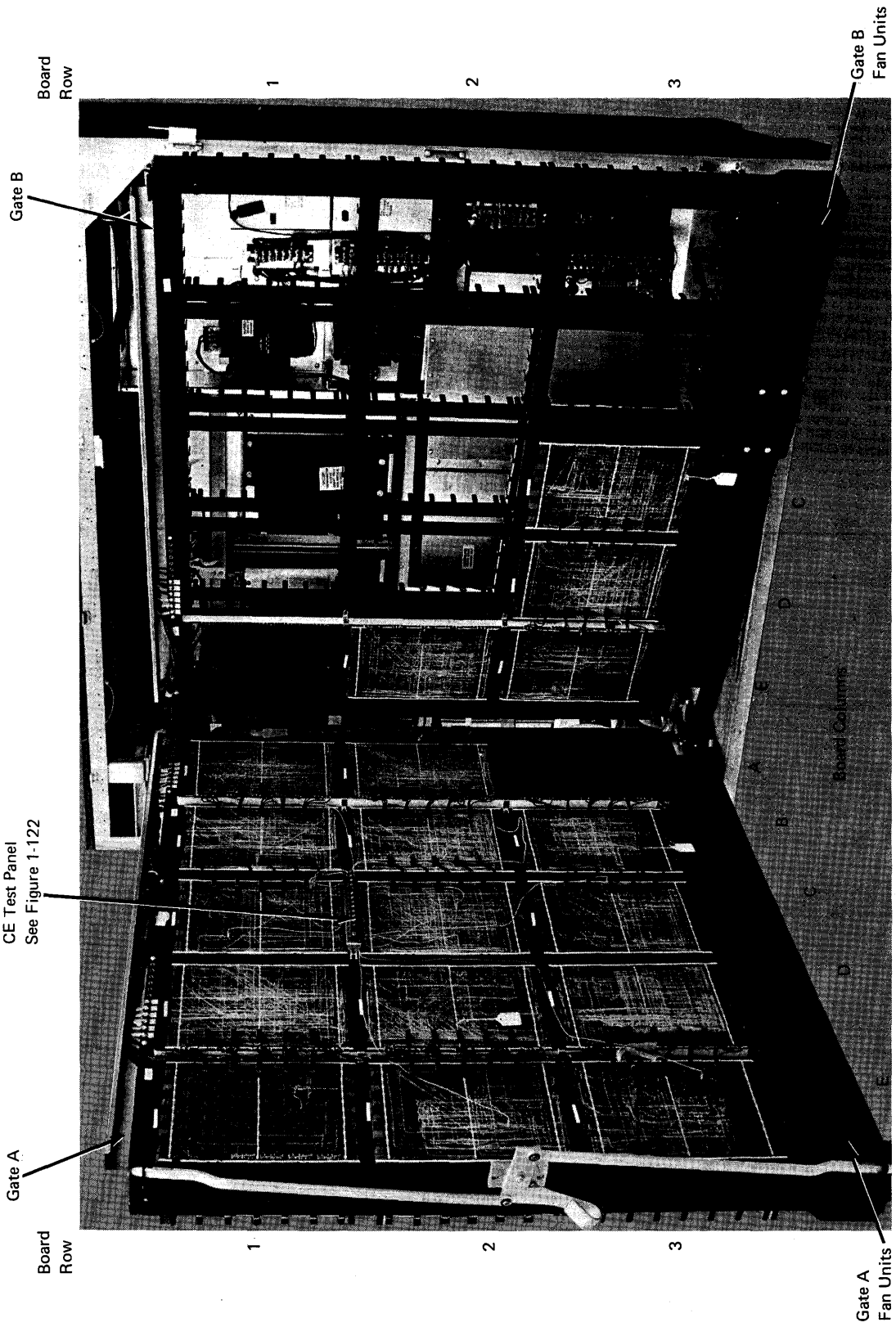


Figure 6-9. Logic Gates A and B (Open)

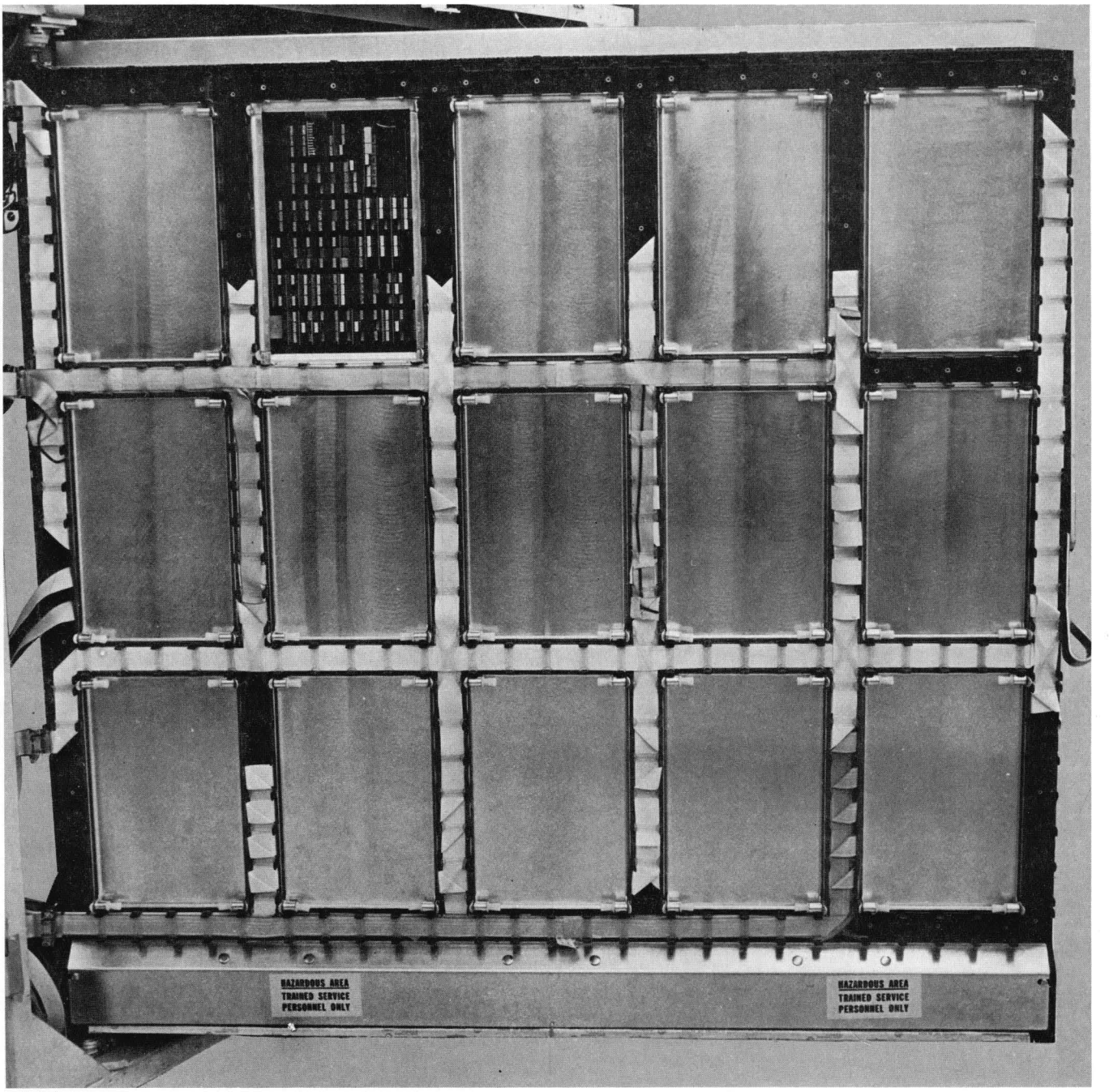


Figure 6-10. Logic Gate A (Card Side)

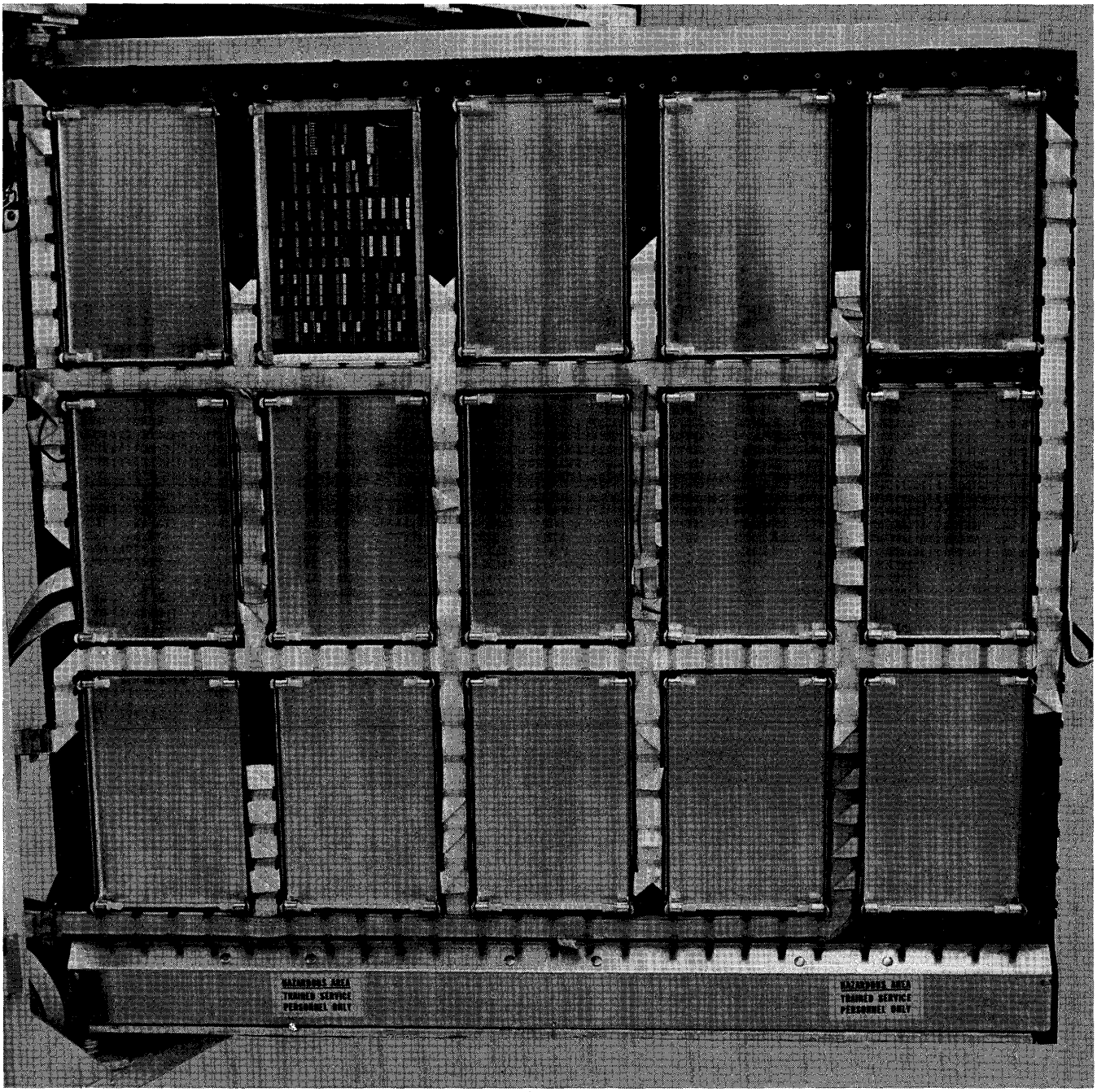


Figure 6-10. Logic Gate A (Card Side)

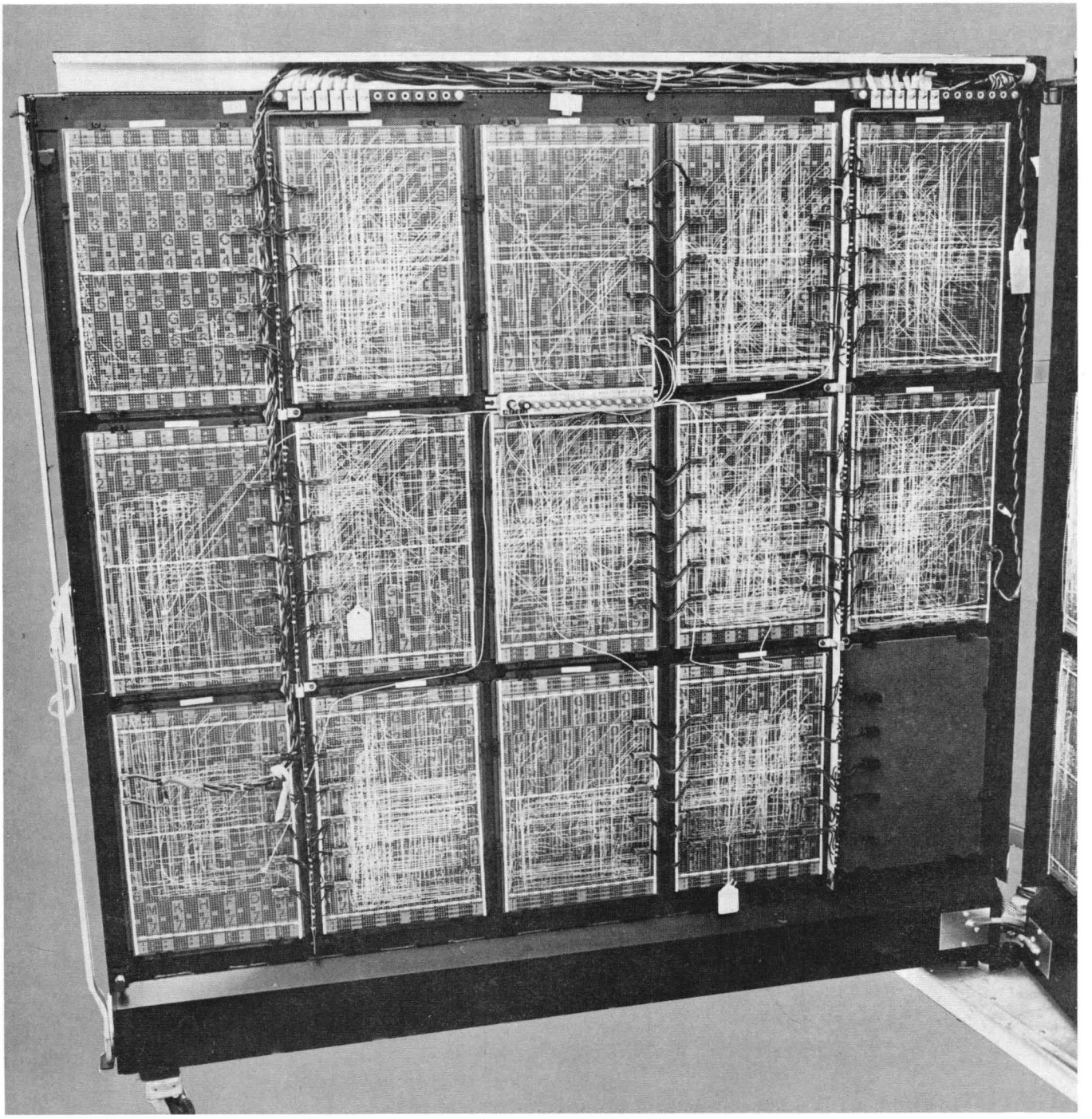


Figure 6-11. Logic Gate A (Pin Side)

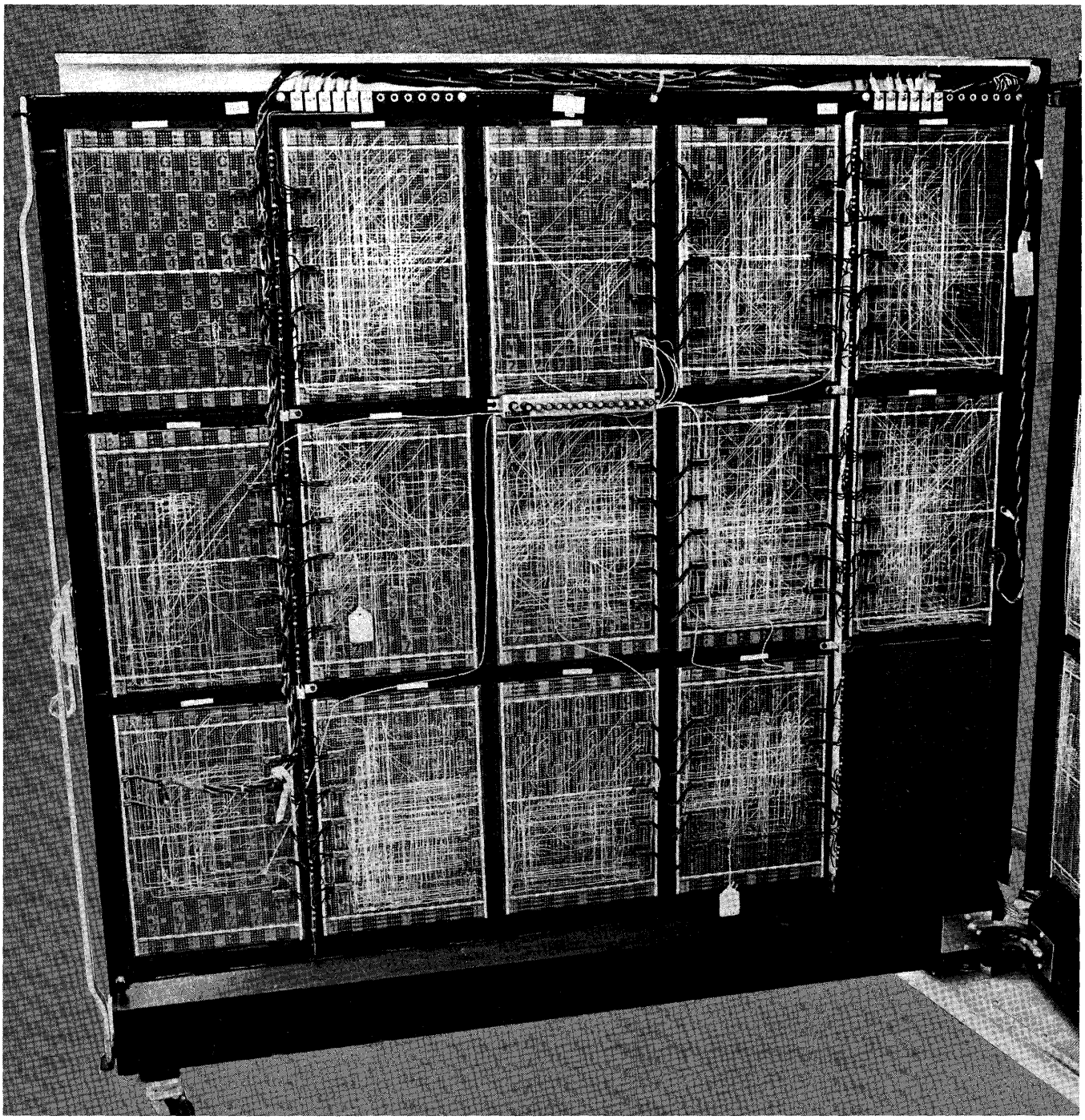


Figure 6-11. Logic Gate A (Pin Side)

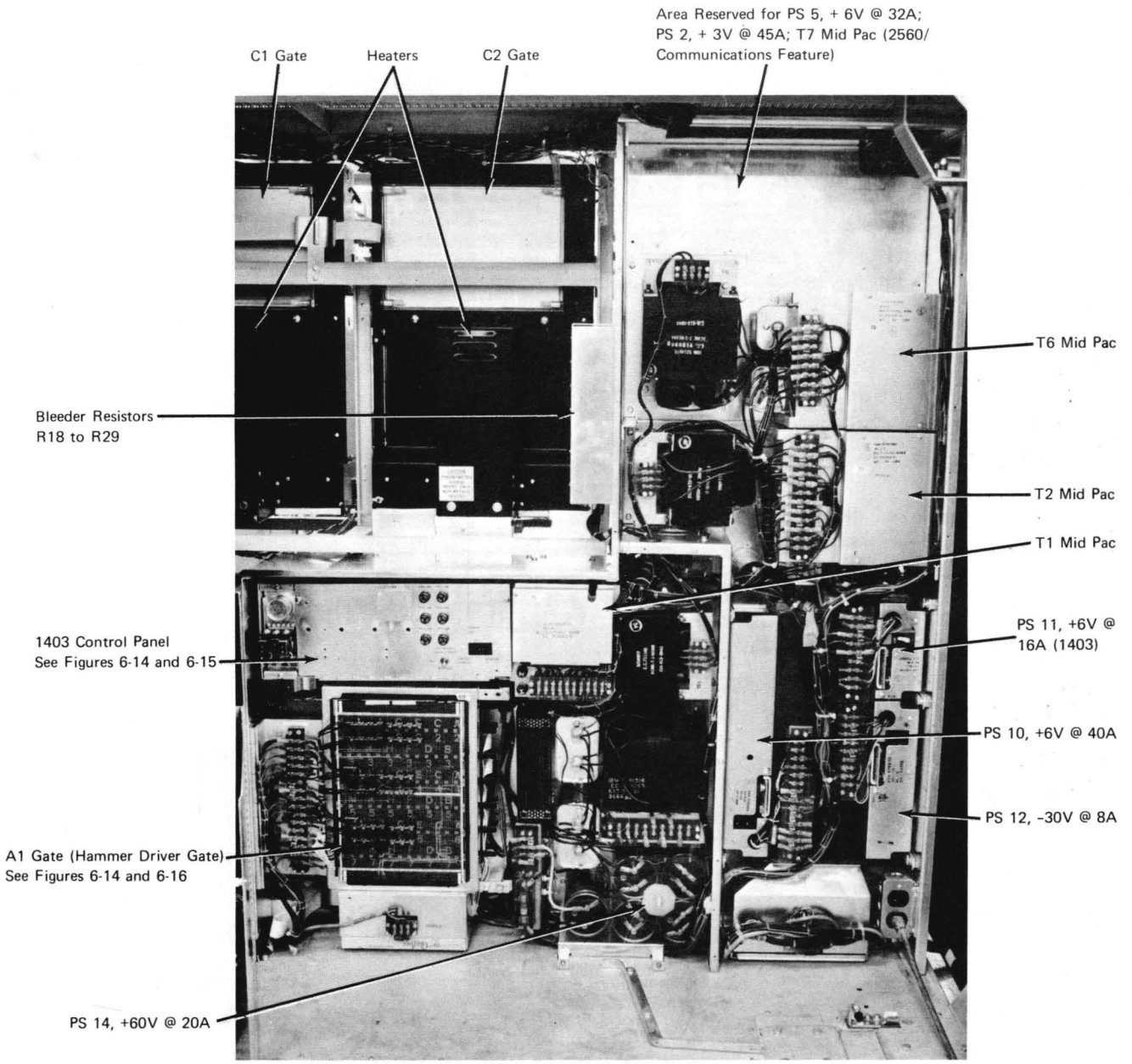


Figure 6-12. Right Side (Behind Logic Gates)

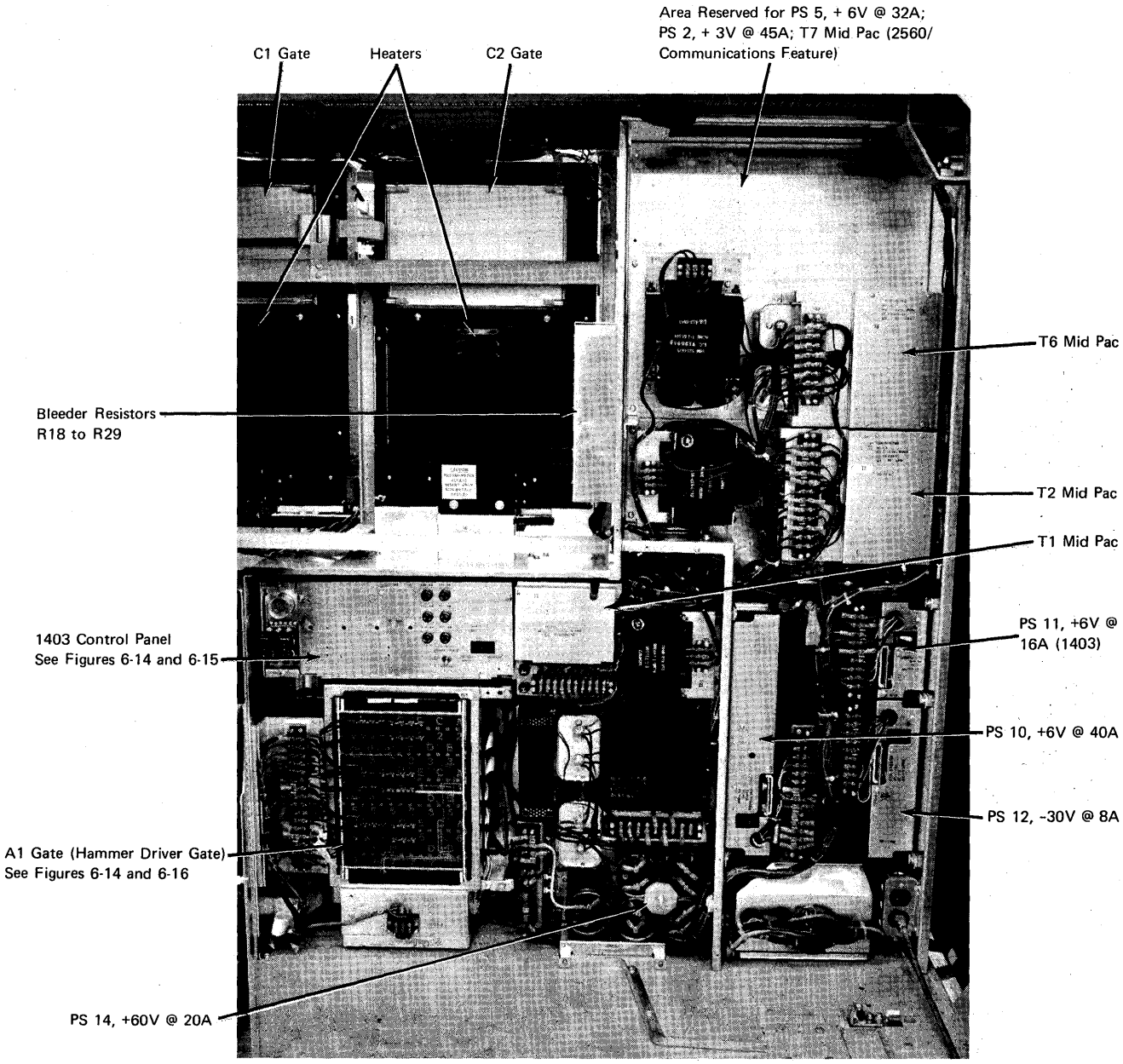


Figure 6-12. Right Side (Behind Logic Gates)

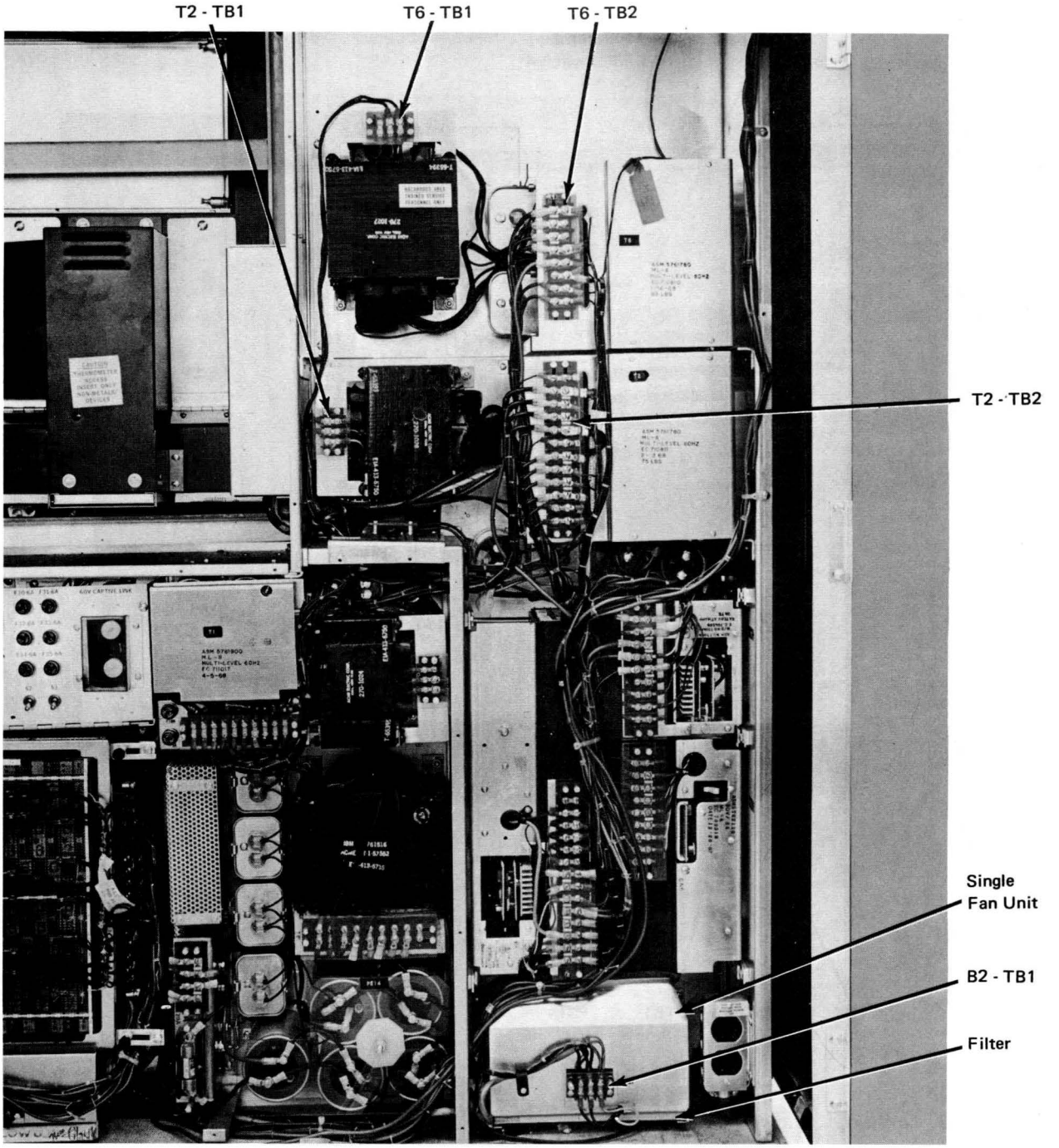


Figure 6-13. Power Supplies (Right Side)

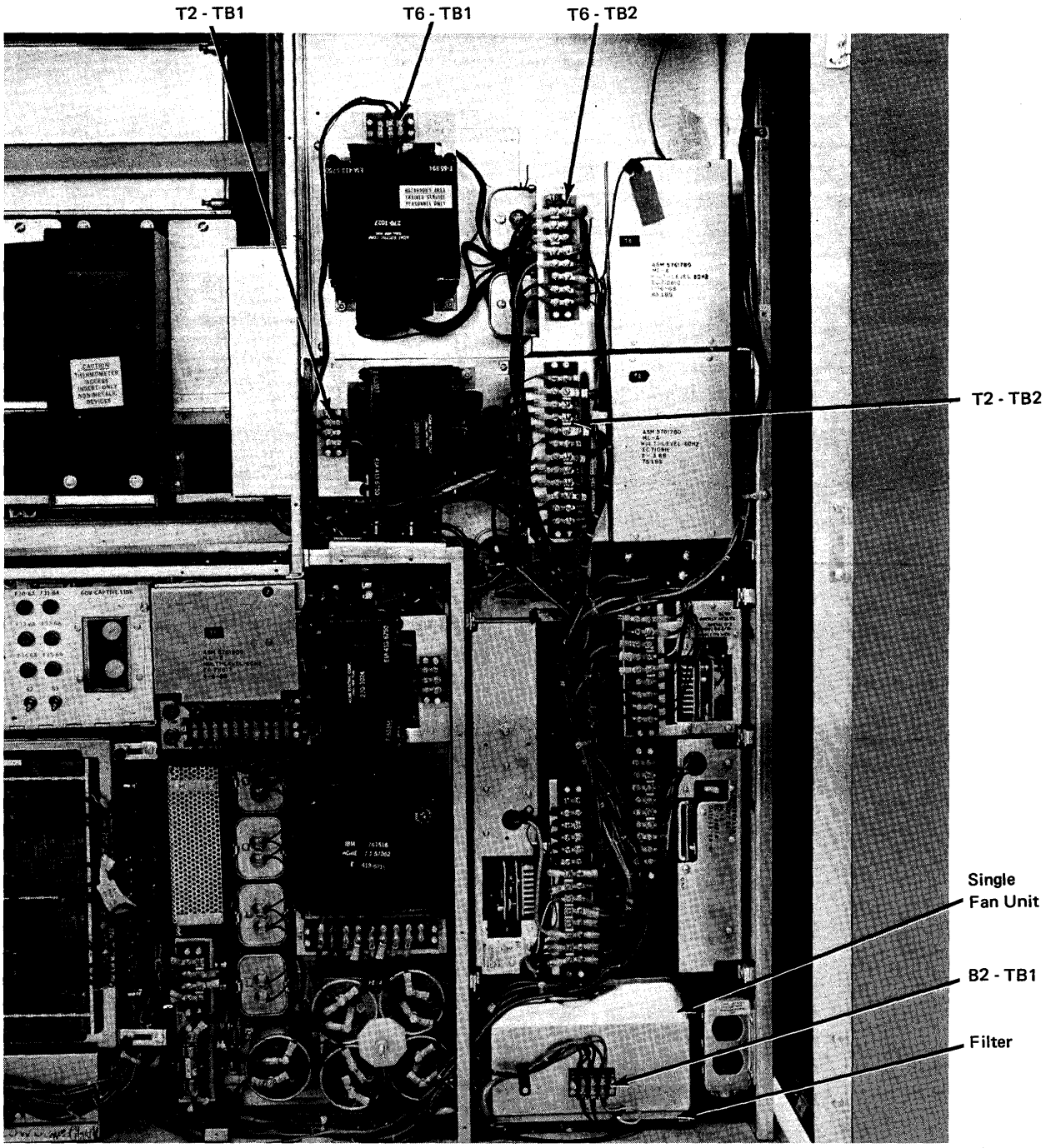


Figure 6-13. Power Supplies (Right Side)

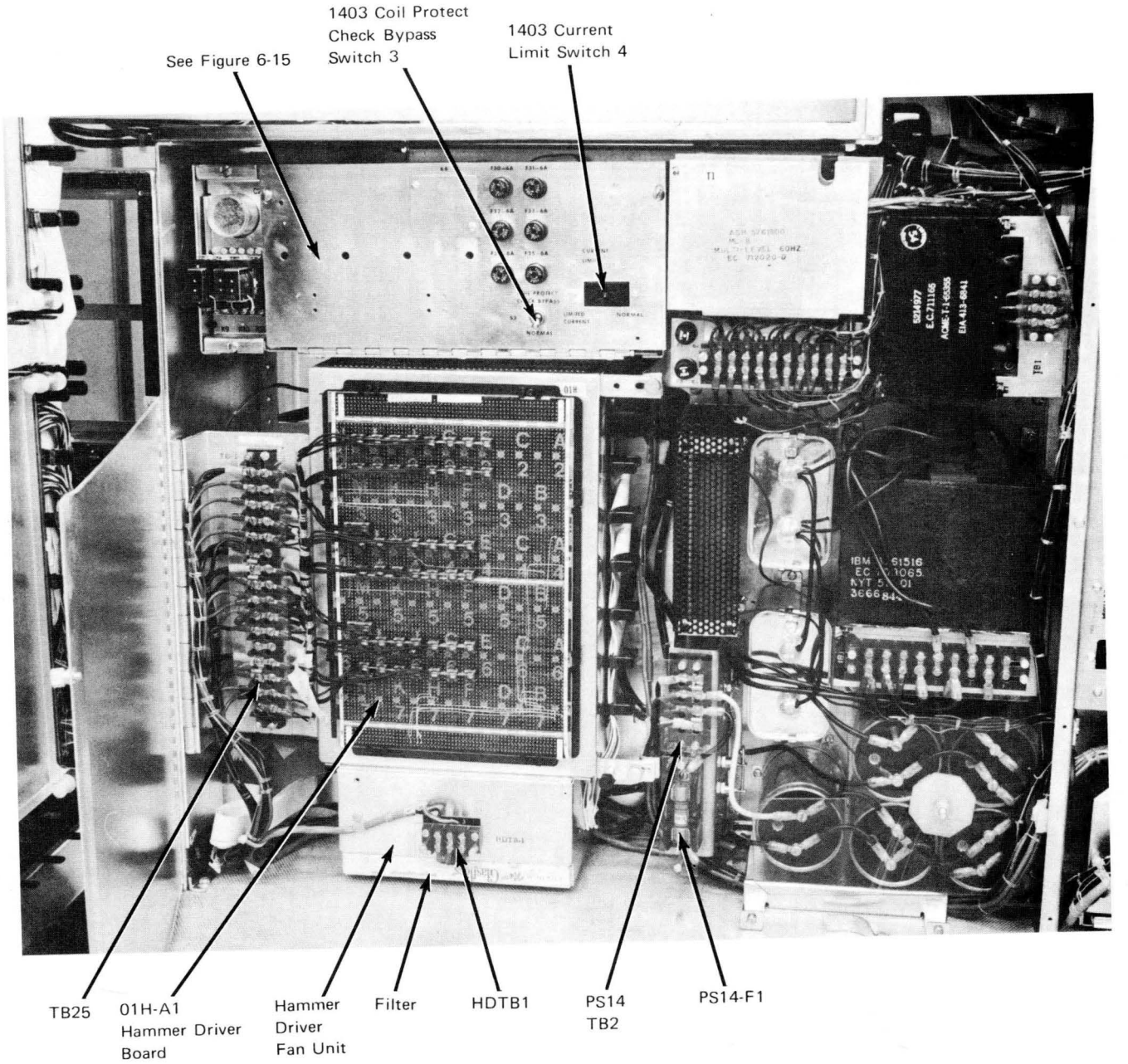


Figure 6-14. 1403 Controls (Right Side)

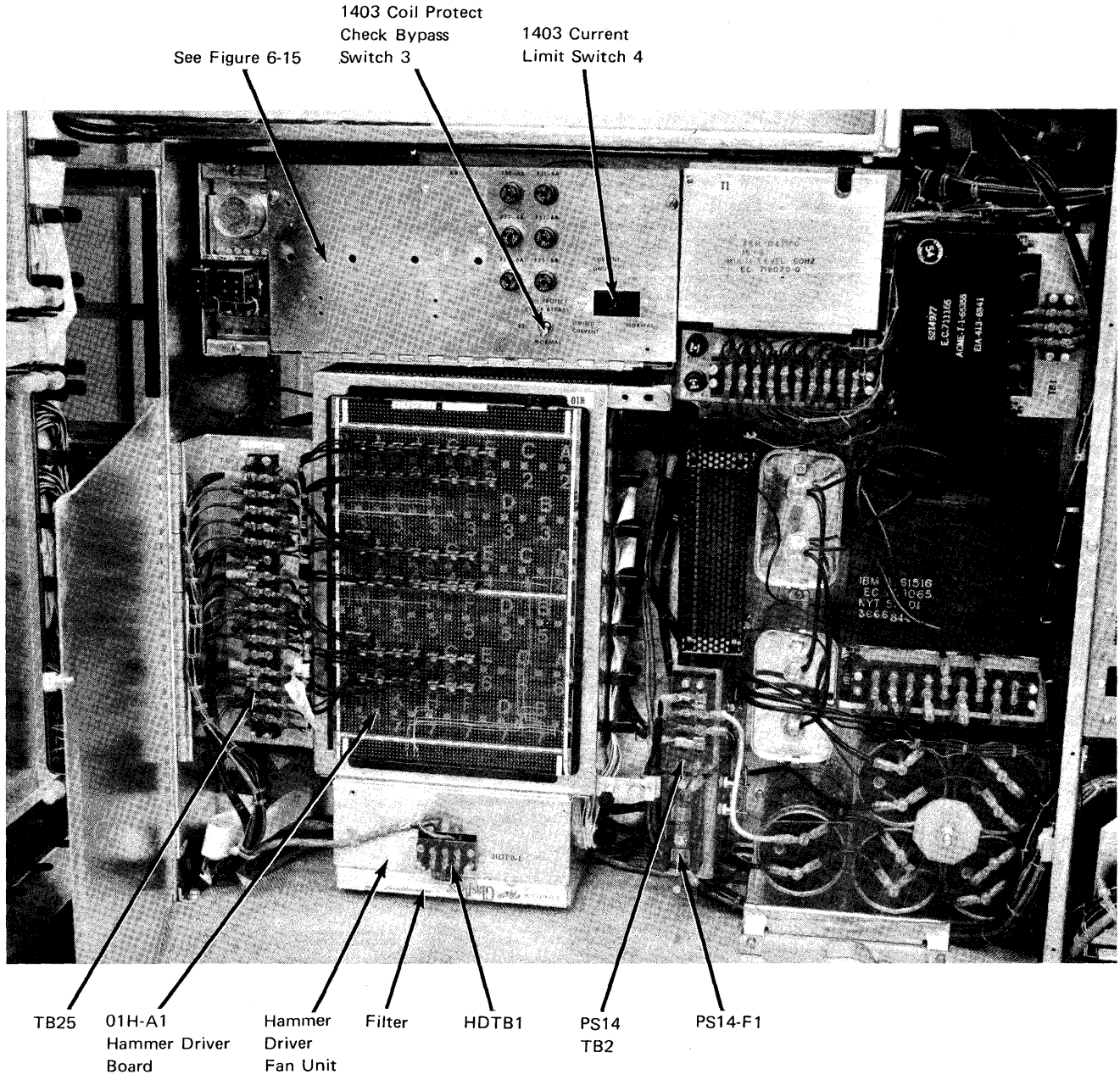


Figure 6-14. 1403 Controls (Right Side)

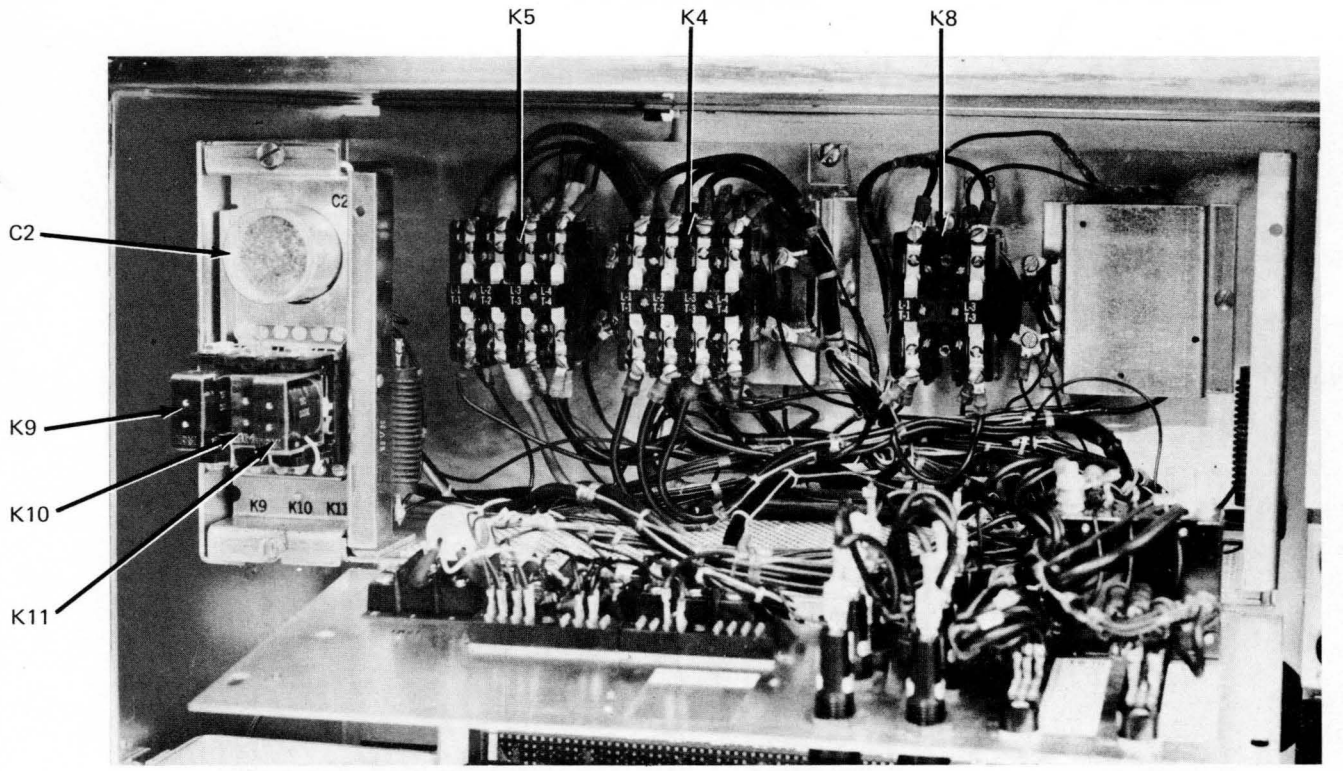


Figure 6-15. 1403 Control Panel (Open)

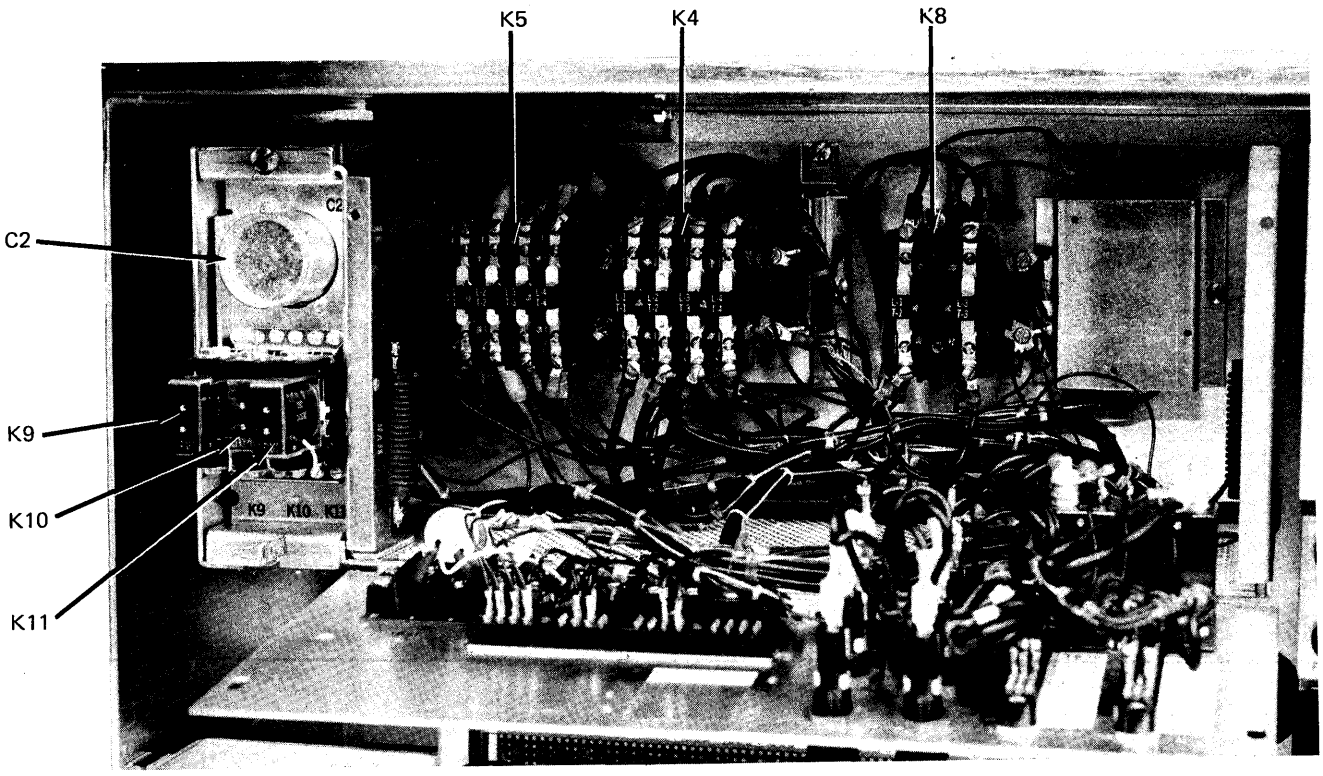


Figure 6-15. 1403 Control Panel (Open)

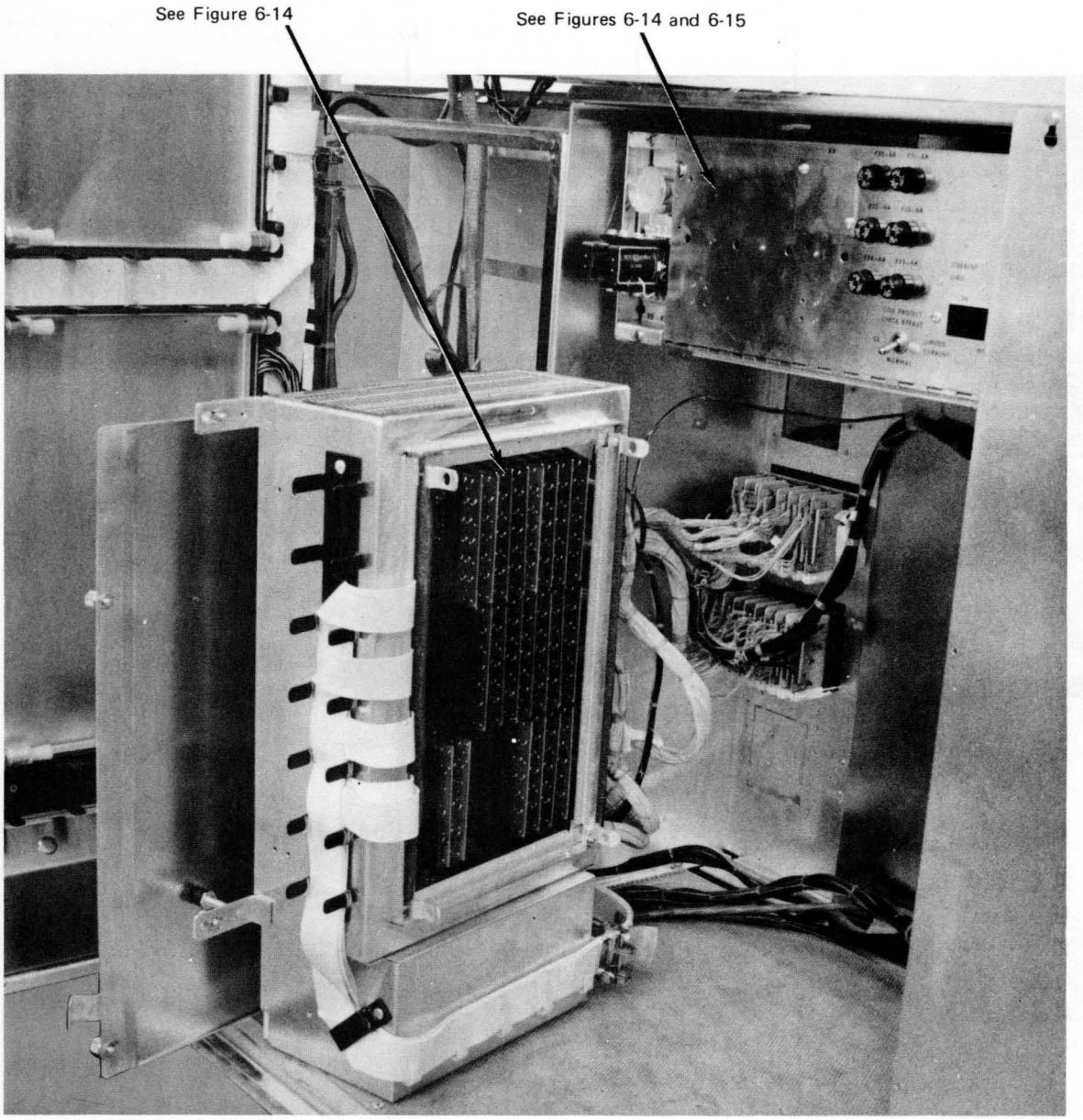


Figure 6-16. Hammer Driver Gate (Open)

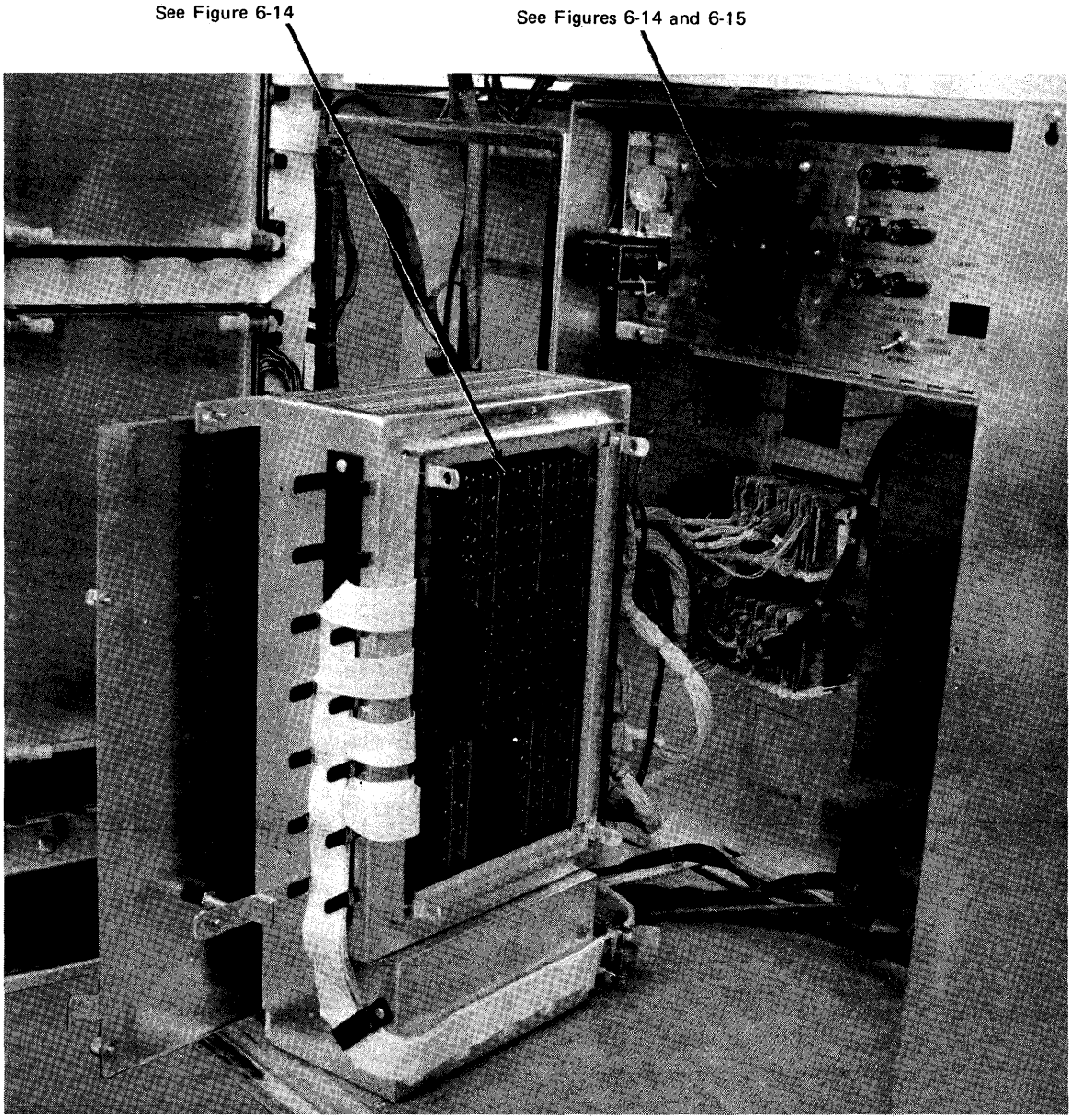


Figure 6-16. Hammer Driver Gate (Open)

Appendix A. Special Circuits

A.1 LOCAL STORAGE CARD AND STORAGE PROTECTION CARD

A.1.1 FUNCTIONAL DESCRIPTION

A 64 X 10 self-contained functional three-dimensional storage-array card (including word drivers, storage elements, bit drivers, sense amplifiers and a voltage regulator) is used for local storage and storage protection. When the storage protection feature is present, the two cards (Figure A-1) can be swapped for diagnostic purposes. The inputs to the storage unit are an 8X by 8Y matrix.

Two modes of operation are possible:
1. A write operation, or
2. A nondestructive read operation (NDR).

The NDR operation is accomplished by supplying a valid address (one X- and one Y-line selected), and sampling the output by conditioning the sense amplifier gate on. (If minimum access time is not needed, the sense amplifier gate can be left on at all times.) The write operation requires a valid address input, 10 data inputs, and a bit driver timing pulse (timed write instruction), all of which must be coincident. All signal input and output lines are compatible with SLD/SLT circuits.

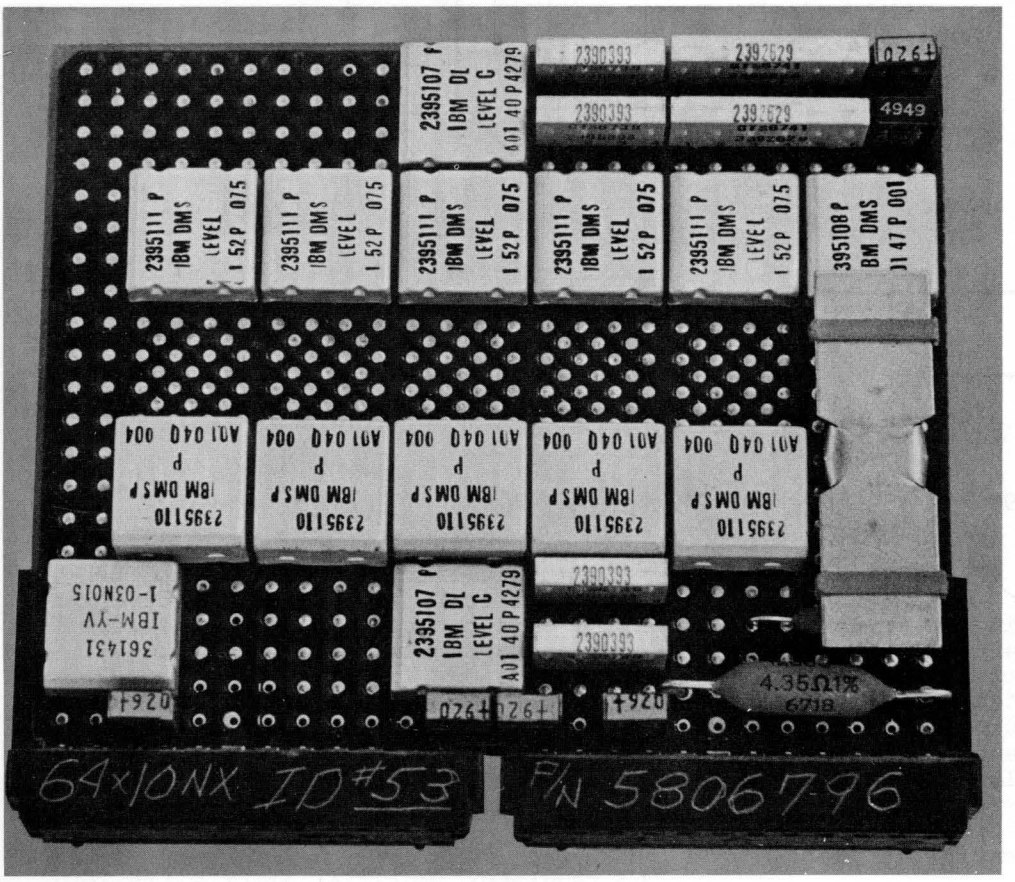


Figure A-1. Local Storage and Storage Protection Card

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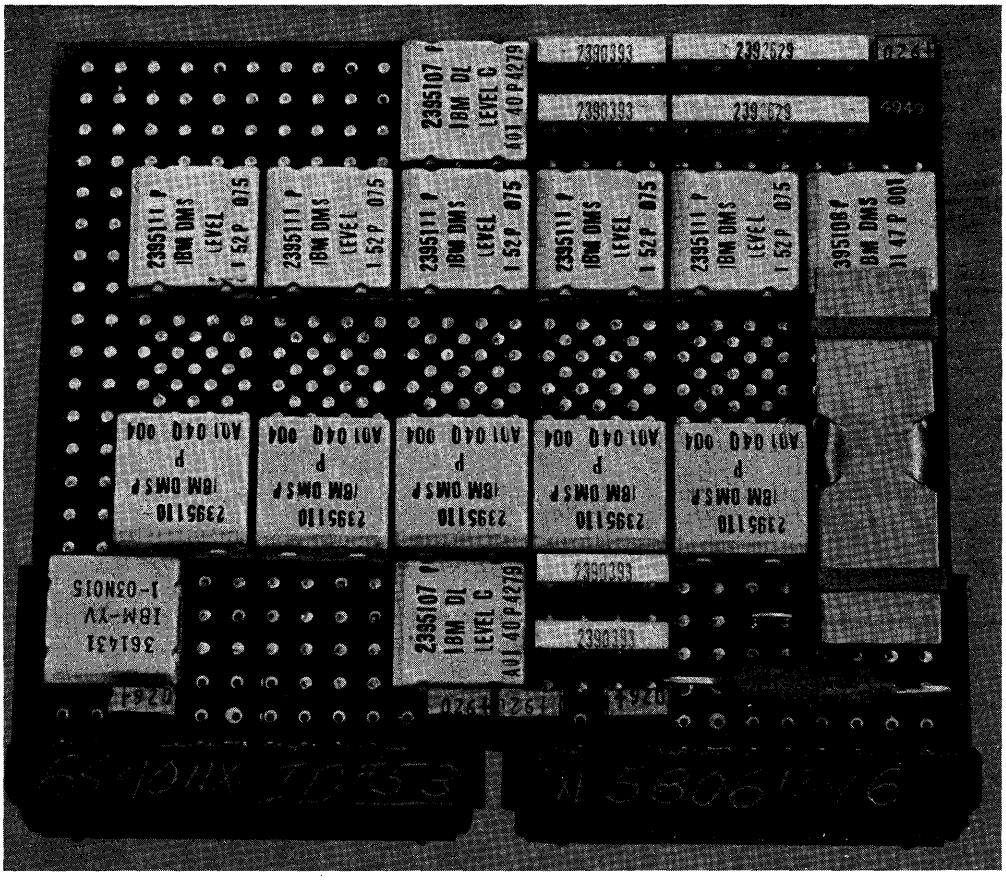

Figure A-1. Local Storage and Storage Protection Card

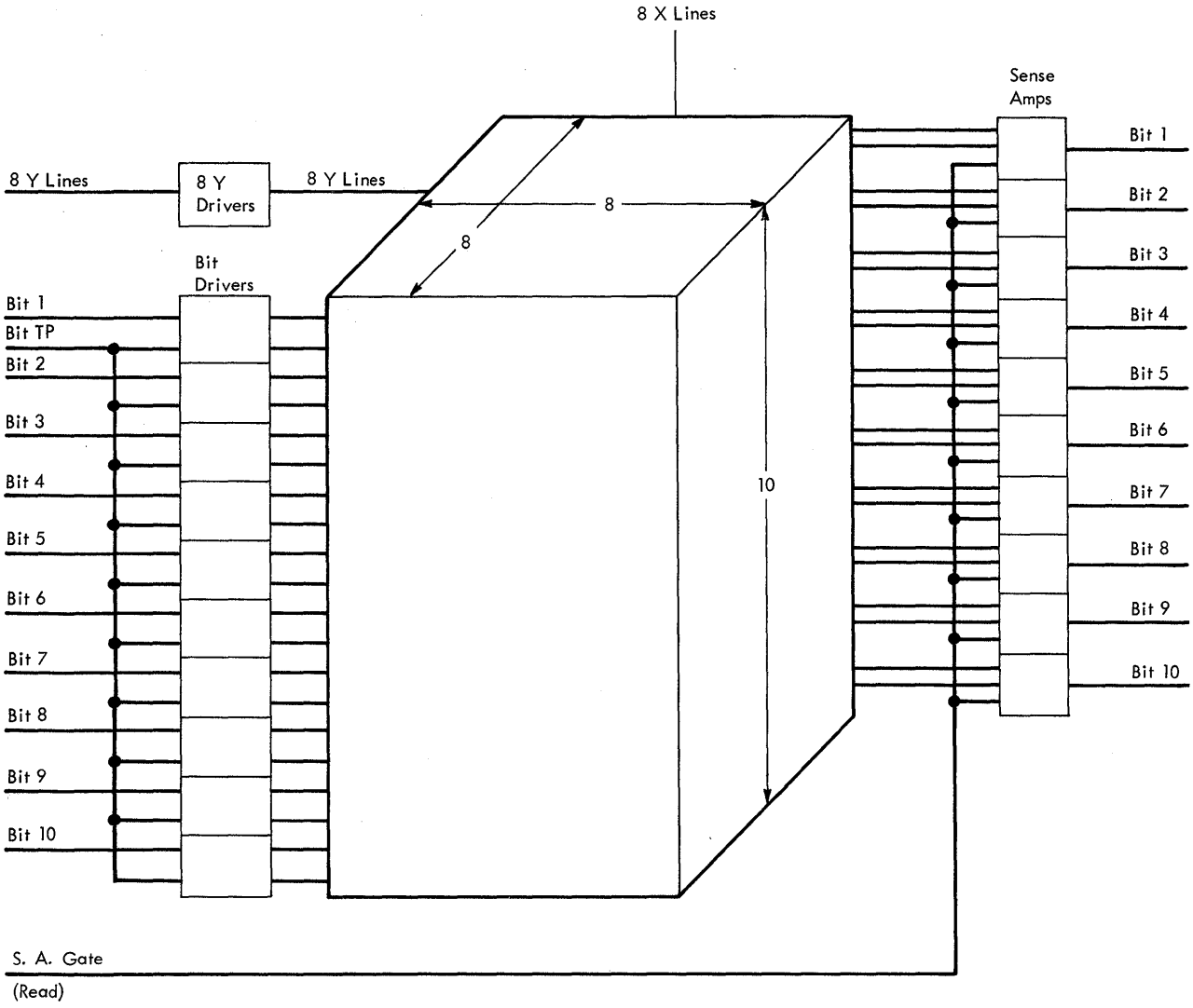

Figure A-2. Local Storage and Storage Protection Addressing

A.1.2 CIRCUIT OPERATION (FIGURE A-2)

An address is selected in the array with the coincidence of a positive Y-line and a negative X-line. This condition selects 10 storage cells, one in each bit or plane. Selection of a cell causes current to flow in either the bit-one sense zero-line or the bit-zero sense-one line, depending on the state of the storage cell. The differential sense amplifier, when gated, provides an output indicative of the polarity of the input.

For the selected cell to be written into, the bit-one or bit-zero driver is turned on, depending on input data. The cell is left in the appropriate state when the bit driver is turned off.

Because the array module cannot be powered directly from +6 volts, circuitry on the card provides the proper levels (+2 volts and approximately 3.25 volts).

There are two parts to the regulator circuitry:
1. a two-volt shunt regulator, and
2. a series-dropping resistor.

The regulator amplifier absorbs the load change while a resistor in parallel with it conducts the major portion of the current. The series-dropping resistor provides a voltage drop from +6 volts to approximately 3.25 volts. The storage latches are connected (all in parallel) between +2 volts and 3.25 volts.

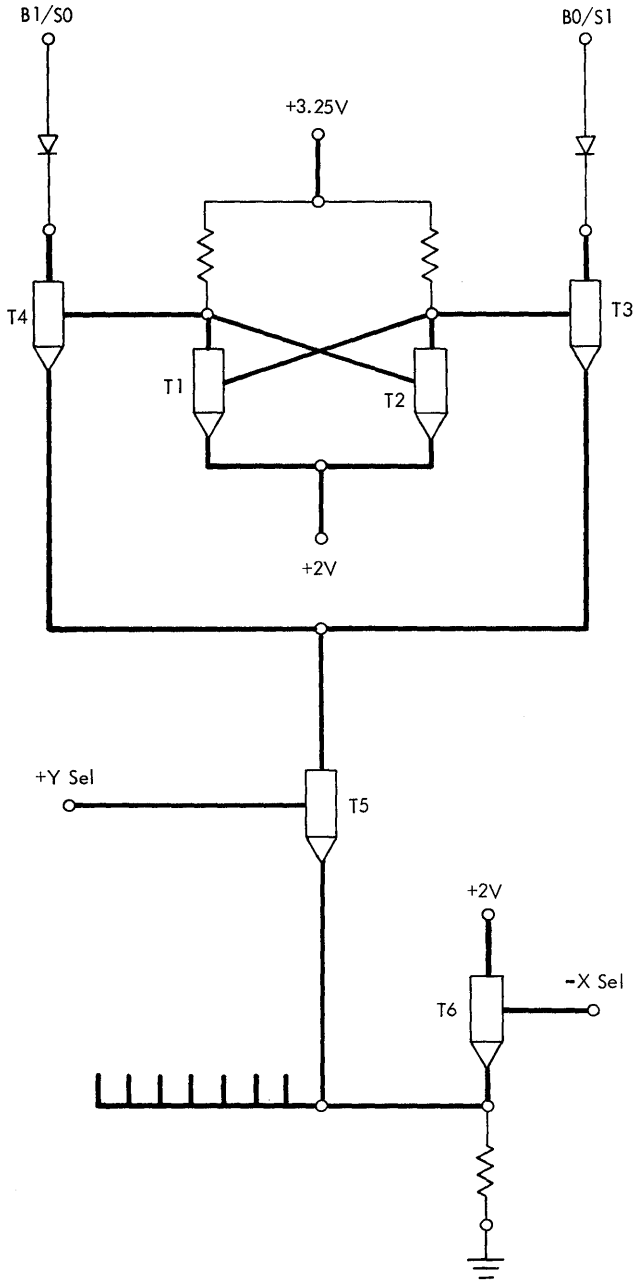

Figure A-3. Basic Storage Cell

A.1.2.1 Cell

A.1.2.1.1 Steady-State Operation: In Figure A-3, the inboard transistors T1 and T2 form a direct-coupled saturating flip-flop. Under steady-state conditions, one transistor is saturated with a collector voltage of approximately 2.2 volts while the other is cut off with a collector voltage of approximately 2.8 volts. Assuming a 1 is stored in the cell, transistor T1 is on and T2 off. The base of T1 and T3 is 2.8 volts while the base of T2 and T4 is 2.2 volts.

A.1.2.1.2 Read Operation: To read information from the cell requires the coincidence of X- and Y-voltage pulses. The X-voltage at the base of T6 is decreased from 2.6 volts to .7 volts while the Y-voltage at the base of T5 is increased from 0 volts to 1.7 volts. Thus, T6 is turned off and T5 is turned on. Due to the state of the flip-flop, T3 is enabled and the sense current, which is determined at the emitter of T5, flows to B0. In the case of a 0 being stored, the state of the flip-flop is reversed and T4 is enabled.

A.1.2.1.3 Write Operation: To write into the cell requires the coincidence of X, Y, and either B0 or B1. Assuming a 1 is stored in the cell and a 0 is to be written, transistor T1 is on and transistor T2 off. The base of T1 and T3 is at 2.8 volts. The X- and Y-lines are pulsed as previously indicated for a read cycle. B0 is decreased from 5 volts to approximately 1.5 volts. With the collector voltage of T3 reduced to saturation level, the enabled transistor T3 conducts all of its emitter current through the base and pulls down the collector voltage of transistor T2, which in turn tends to turn off transistor T1. As T1 turns off, its collector voltage rises and turns on T2. At the completion of this process a steady-state condition is reached with T1 off and T2 on. Thus, the saturating flip-flop is in its opposite condition and the 0 is stored in the cell.

A.1.3 STORAGE MODULE

The storage module is a one-half inch by one-half inch module consisting of a single substrate with twenty-three SLT input/output pins and eleven interstitial (feed through) pins.

Two 64-bit chips arranged in an 8Y by 8X by 1-bit configuration are mounted on the substrate making the module organization 64 by 2 bits. Nominal power dissipation per module is approximately 275 mw.

A.1.4 PERIPHERAL CIRCUITS (FIGURE A4)

X-Drivers: The X-driver is similar in configuration to the SLD100 A0I circuit except that it is clamped out of saturation. The driver input is a two-way AND circuit. There are four drivers per module and four load resistors per R-pack.

Y-Drivers: The Y-driver is a saturating emitter follower. It has one input and cannot be used as an AND circuit. There

are four complete circuits per module including load resistors.

Bit Drivers: A one and a zero driver is required for each bit. The bit-1 driver is identical to the X-driver. The bit-0 driver is slightly different in that an input diode is used to clamp the output down level to a higher voltage. The bit-one driver is used as an inverter for the data input to the zero driver.

Sense Amplifier: The first stage of the sense amplifier is a gated differential amplifier followed by a level translating PNP stage and a saturating inverter. There are four bit drivers and two sense amplifiers on a stacked module.

Voltage Regulator: Plus-two volts is defined by a shunt regulator consisting of a differential amplifier and an emitter follower that drives the common emitter output transistor. The larger versions have two emitter followers. The reference voltage is generated by a resistor divider.

Cell and Drive Circuit: See Figure A-4 for a representation of the drive circuits with a cell.

Y-Inputs	X-Inputs
0 D02	0 J09
1 B03	1 G10
2 B04	2 J10
3 D04	3 J11
4 B05	4 G12
5 D05	5 J12
6 D06	6 G13
7 B07	7 J13

In	Data	Out
D10	1	B10
D07	2	B08
D13	3	B12
D11	4	D12
G03	5	G04
G02	6	J02
J05	7	G07
G05	8	J04
G08	9	G09
J07	10	J06

Bit T. P.	D09	+6	B11,G11
S. A. GATE	B09	GND	D08,J08
+2.0 Test Pin	B02	Not Used	D03,J03,B06,G06
+3.2 Test Pin	B13		

A.1.5 PIN ASSIGNMENTS

Card pin assignments for the communicating lines and power connections to and from the storage card are as follows.

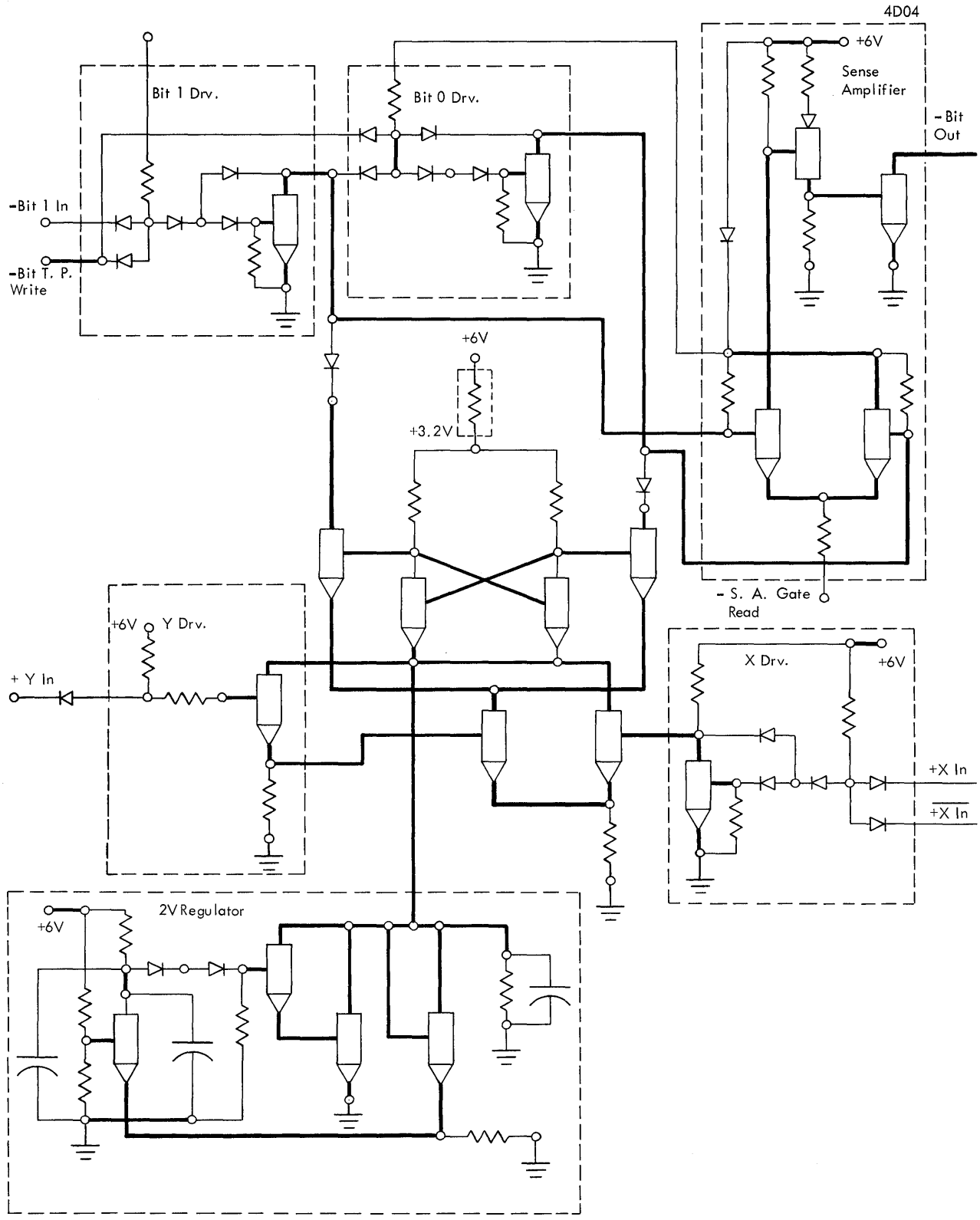

Figure A-4. Composite View of Circuits

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READER'S COMMENT FORM

IBM 2025 Processing Unit FEMM Y24-3528-1

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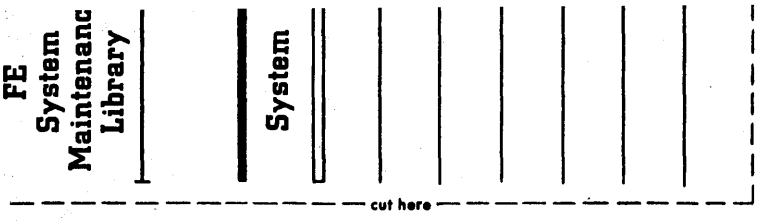

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