2211784

2211784

FORM O-2572-1 (10-66)

FIELD ENGINEERING DIAGRAM MANUAL

FOR

2841 STORAGE CONTROL - STAGE 2

MACHINE TYPE NUMBER, MODEL NUMBER (IF APPLICABLE) AND MACHINE NAME

CONSISTS OF THE FOLLOWING:

FORM NUMBER (BASE FEDM)* Y26-4137-1

FORM NUMBER (FES)**

NOTES

XI THE FEDM AND ITS FES'S INCLUDE A SYSTEM DATA FLOW DIAGRAM, UNIT DATA AND CONTROL DIAGRAM, I/O OPERATION DIAGRAMS, AND CONDENSED LOGIC FLOW CHARTS AS APPLICABLE TO THE UNIT(S) BEING SHIPPED.

XII WHEN A FEDM IS ORDERED FROM MECHANICSBURG, ALL APPLICABLE SUPPLEMENTS WILL BE AUTOMATICALLY SUPPLIED. SUPPLEMENTS CAN BE ORDERED SEPARATELY BY APPLICABLE FORM NUMBER.

* FIELD ENGINEERING DIAGRAM MANUAL
** FIELD ENGINEERING SUPPLEMENT

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	DATE	CHANGE NO.	NOTE	DEVELOPMENT NO.	2211784
NAME	FEDM ID DWG					413343			X PRINT TO ENG. SPEC. NO.		
DESIGN			MODEL								
DETAIL											
CHECK			DRAW								
APPRO			CHECK								

IBM Field Engineering
Maintenance Diagrams

2841 Storage Control–Stage 2

SY26-4137-1

IBM Field Engineering
Maintenance Diagrams

2841 Storage Control – Stage 2

SY26-4137-1

PREFACE

This manual contains flow charts, timing charts, and special-purpose diagrams to assist in the maintenance activity on the IBM 2841 Storage Control -Stage 2.

Simplified drawings have been prepared for functions which are not readily perceptible in the system diagrams, or for which the logic requires multiple pages.

The system diagrams at the engineering level of the equipment should be used in preference to the maintenance diagrams wherever there is a conflict between the two types of diagrams.

Second Edition

This edition (Form Y26-4137-1) is a merge reprint of form Y26-4137-0 and supplement Y26-0605.

Specifications contained herein are subject to change from time to time. Any such change will be reported in subsequent revisions or Field Engineering Supplements.

Copies of this and other IBM publications can be obtained through IBM Branch Offices.

A form is provided at the back of this publication for your comments.

This manual was prepared by the IBM Systems Development Division, Product Publications, Dept. 455, Bldg. 014, San Jose, California 95114.

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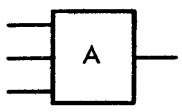
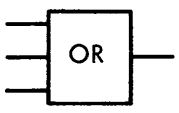
In positive logic representation, signal levels are disregarded. The negator (N block symbol) is used to invert logic, not level. Passive elements (such as drivers and pulse shapers) generally are not shown, since they contribute nothing to the logic.

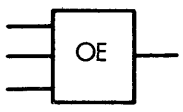
LOGICAL ELEMENTS



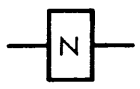
AND



OR

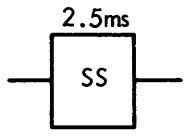


Exclusive-OR

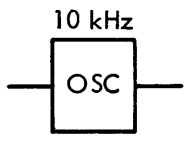


NOT
(Negator)

TIMING ELEMENTS

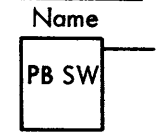


Single-Shot

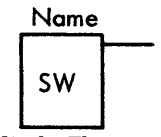


Oscillator

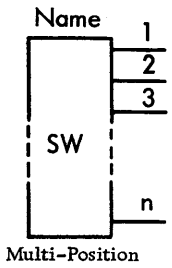
SWITCHES



Momentary

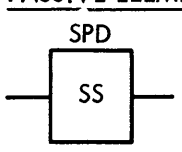


Single-Throw

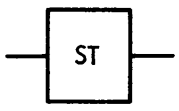


Multi-Position

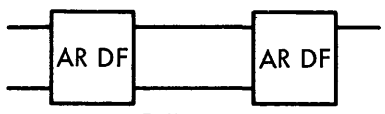
PASSIVE ELEMENTS



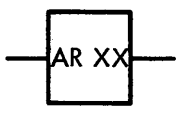
Sample-Pulse
Driver



Schmitt
Trigger



Differential
Amplifiers

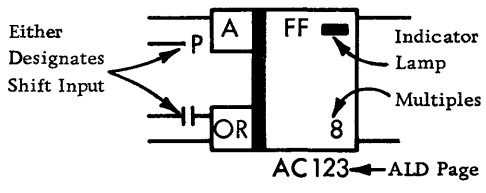


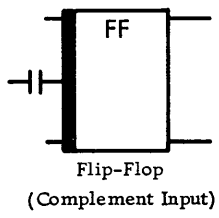
Single-Ended
Amplifiers

XX Abbreviations

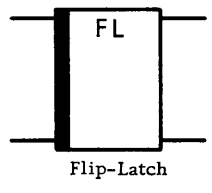
V = Voltage Amplifier
LD = Line Driver
LT = Line Terminator
MD= Magnet Driver
HD= Head Driver
ID = Indicator Driver
CD= Core Driver

STORAGE ELEMENTS

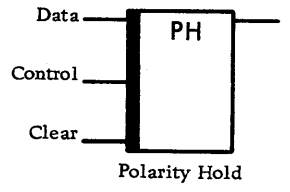




Flip-Flop
(Complement Input)

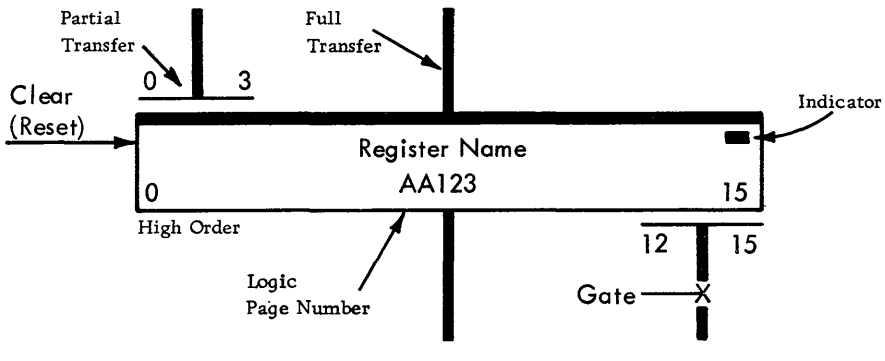


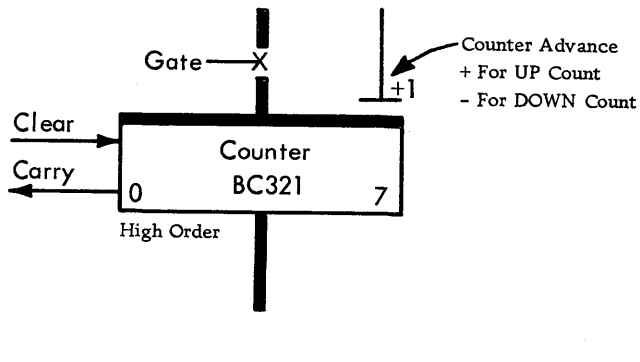
Flip-Latch



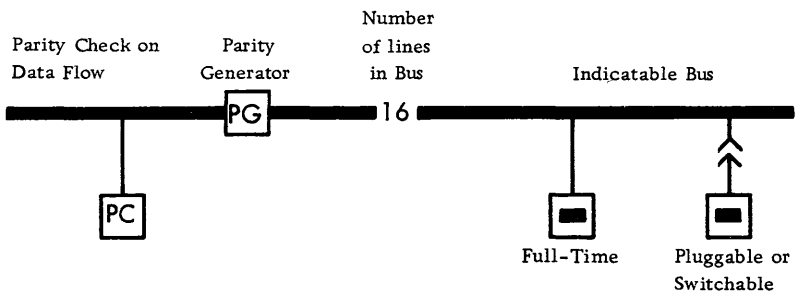
Polarity Hold

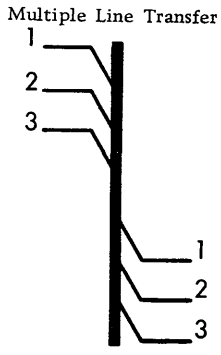
REGISTERS AND COUNTERS

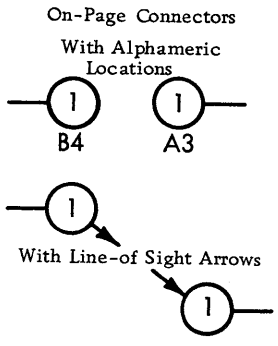


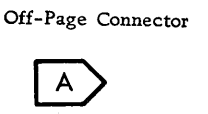


MISCELLANEOUS

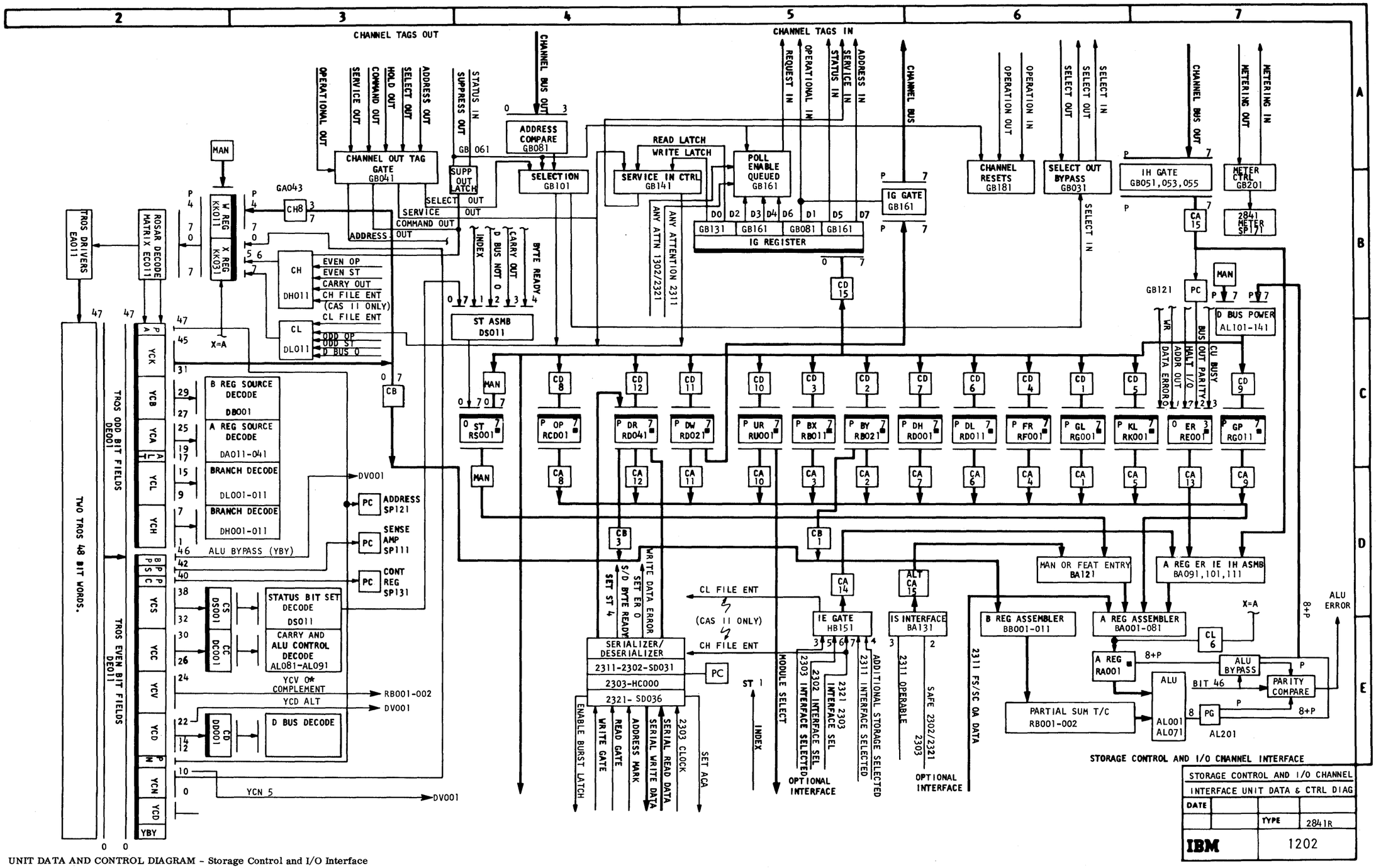




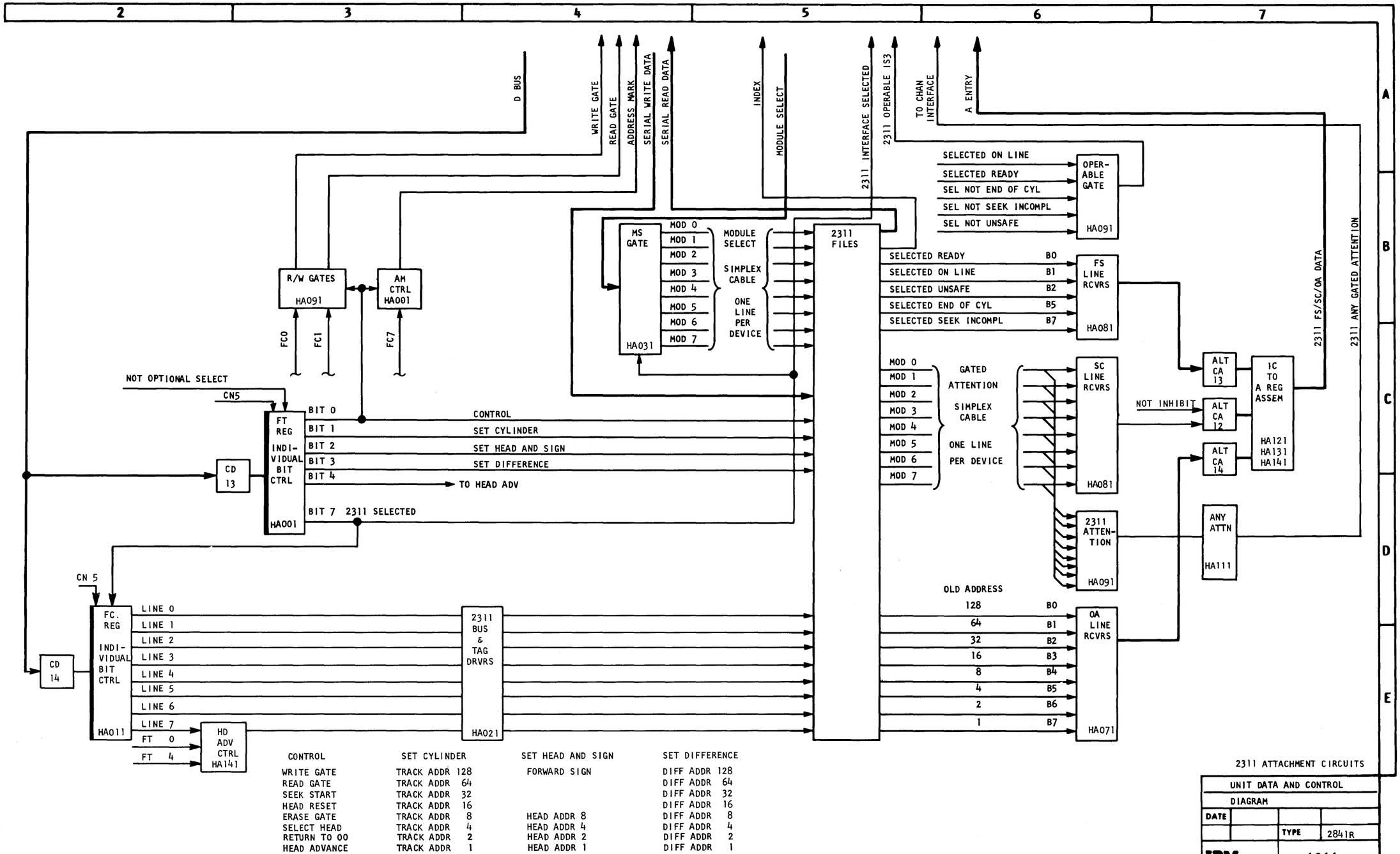




14093 B



UNIT DATA AND CONTROL DIAGRAM - Storage Control and I/O Interface

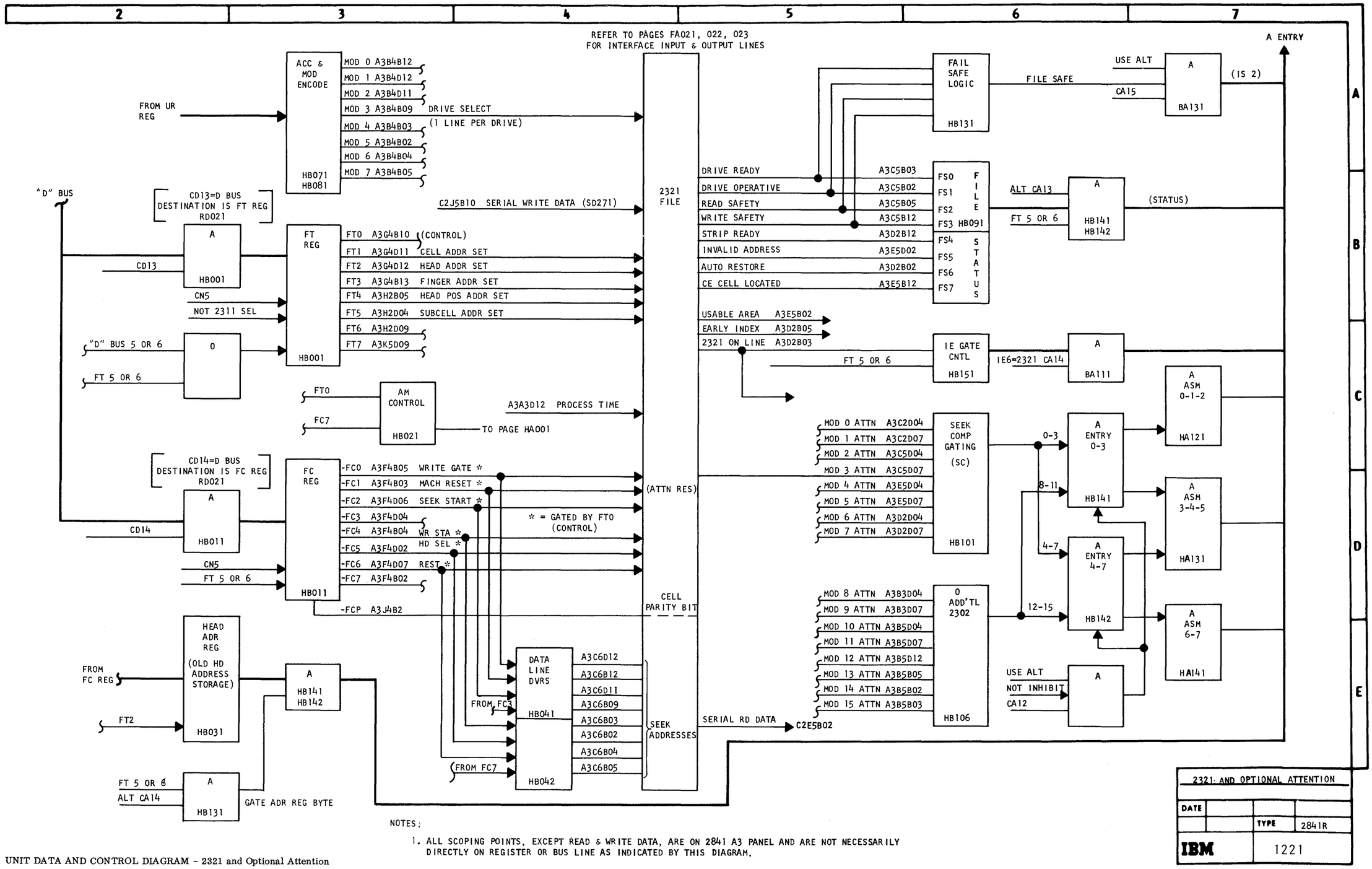


CONTROL	SET CYLINDER	SET HEAD AND SIGN	SET DIFFERENCE
WRITE GATE	TRACK ADDR 128	FORWARD SIGN	DIFF ADDR 128
READ GATE	TRACK ADDR 64		DIFF ADDR 64
SEEK START	TRACK ADDR 32		DIFF ADDR 32
HEAD RESET	TRACK ADDR 16		DIFF ADDR 16
ERASE GATE	TRACK ADDR 8	HEAD ADDR 8	DIFF ADDR 8
SELECT HEAD	TRACK ADDR 4	HEAD ADDR 4	DIFF ADDR 4
RETURN TO 00	TRACK ADDR 2	HEAD ADDR 2	DIFF ADDR 2
HEAD ADVANCE	TRACK ADDR 1	HEAD ADDR 1	DIFF ADDR 1

2311 ATTACHMENT CIRCUITS

UNIT DATA AND CONTROL DIAGRAM			
DATE			
		TYPE	2841R
IBM		1211	

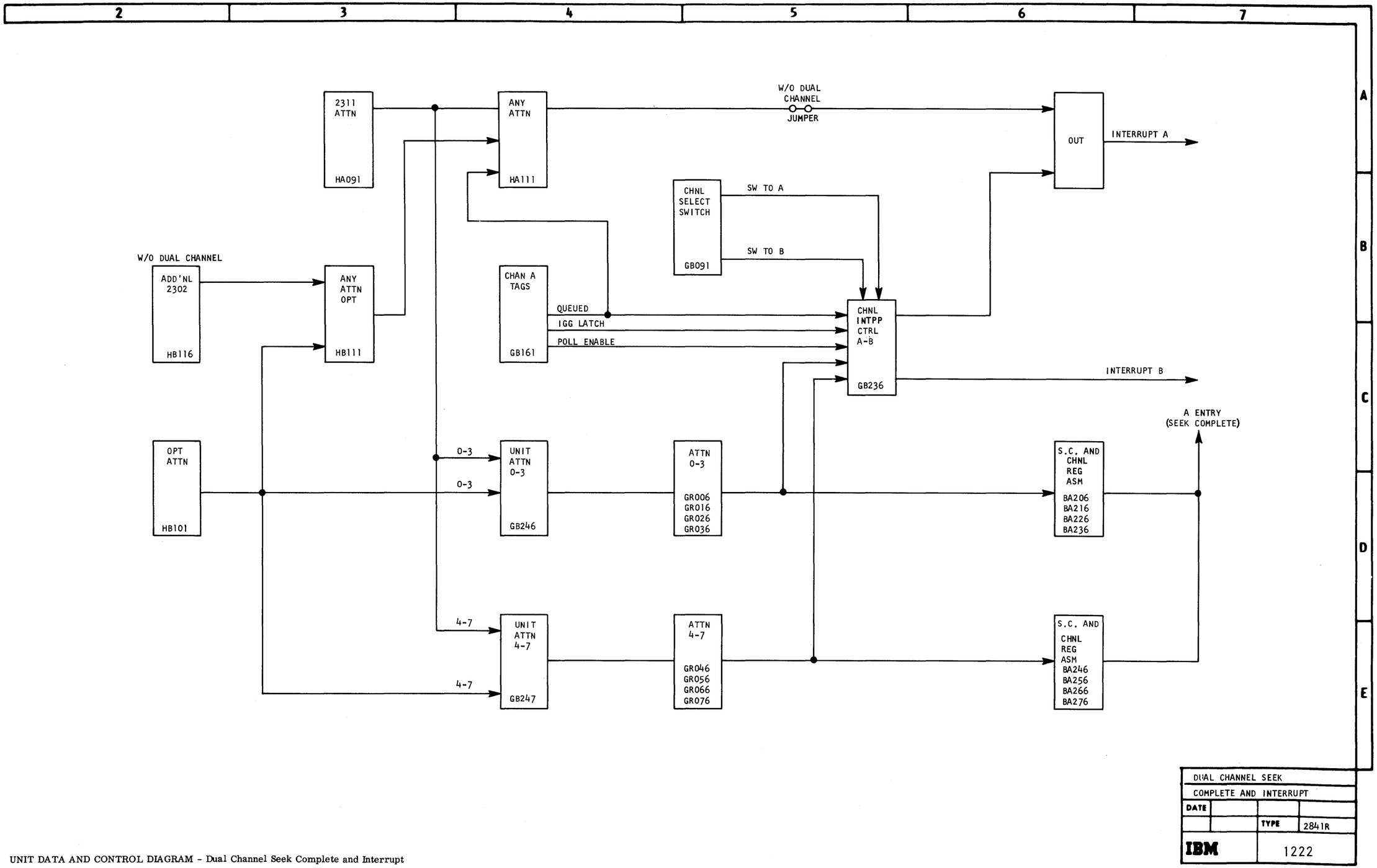
UNIT DATA AND CONTROL DIAGRAM - 2311 Attachment Circuits



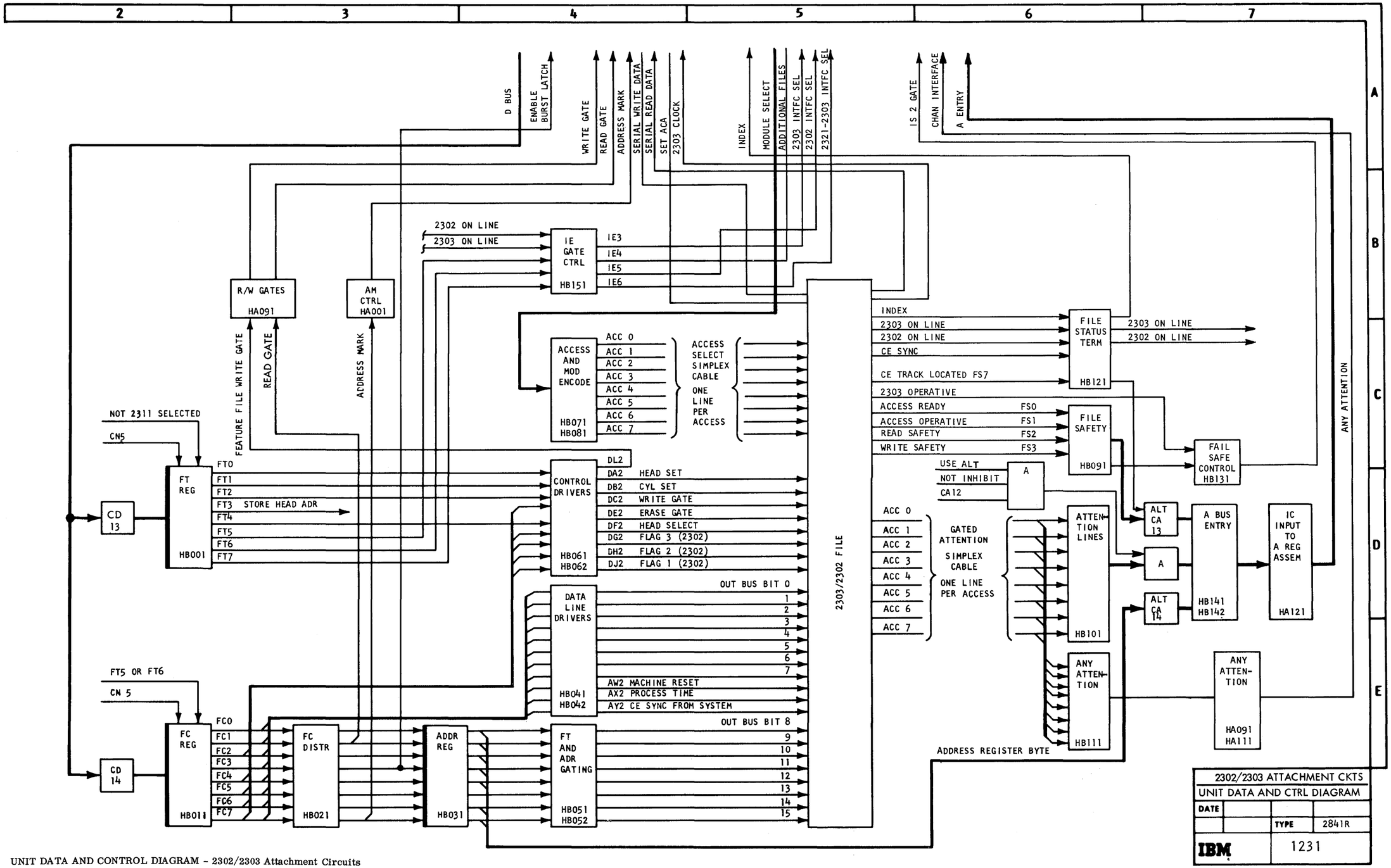
UNIT DATA AND CONTROL DIAGRAM - 2321 and Optional Attention

NOTES:

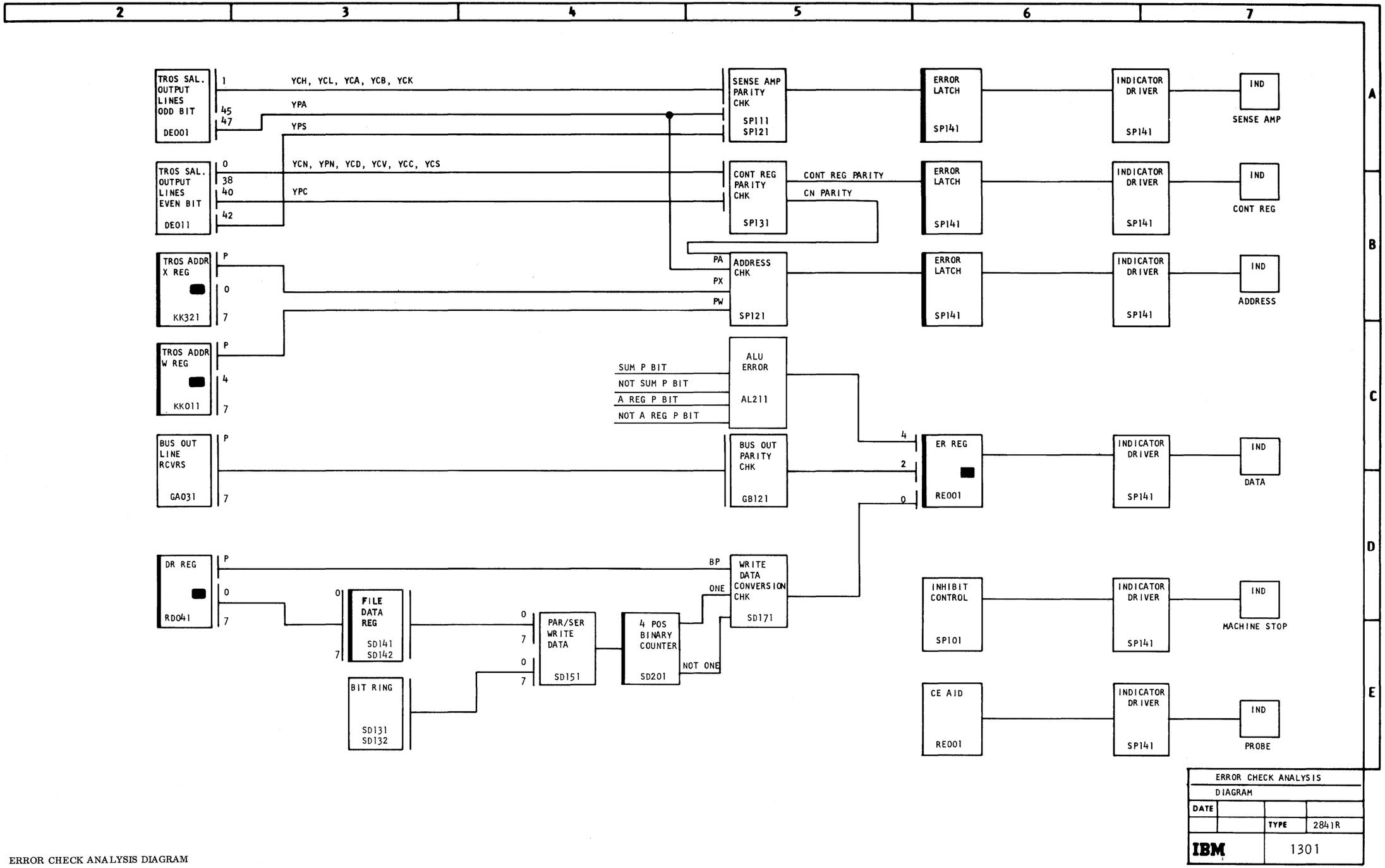
1. ALL SCOPING POINTS, EXCEPT READ & WRITE DATA, ARE ON 2841 A3 PANEL AND ARE NOT NECESSARILY DIRECTLY ON REGISTER OR BUS LINE AS INDICATED BY THIS DIAGRAM.



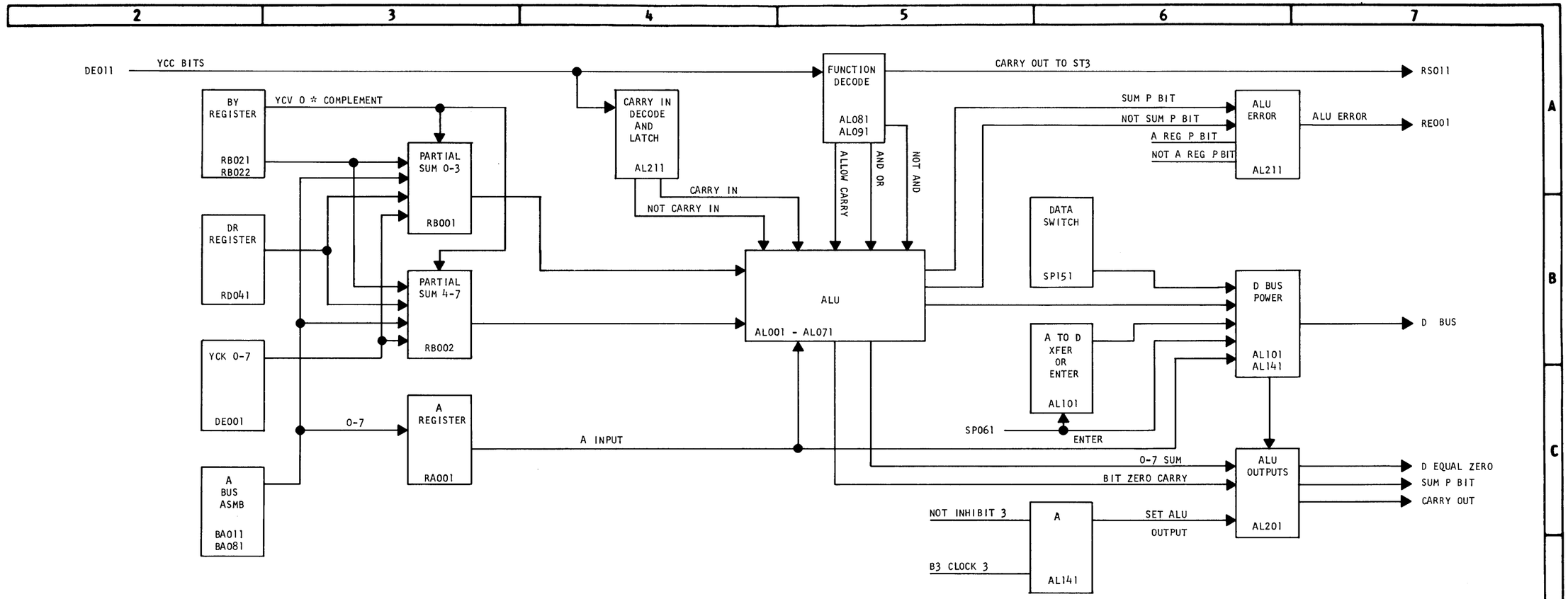
UNIT DATA AND CONTROL DIAGRAM - Dual Channel Seek Complete and Interrupt



UNIT DATA AND CONTROL DIAGRAM - 2302/2303 Attachment Circuits



ERROR CHECK ANALYSIS DIAGRAM

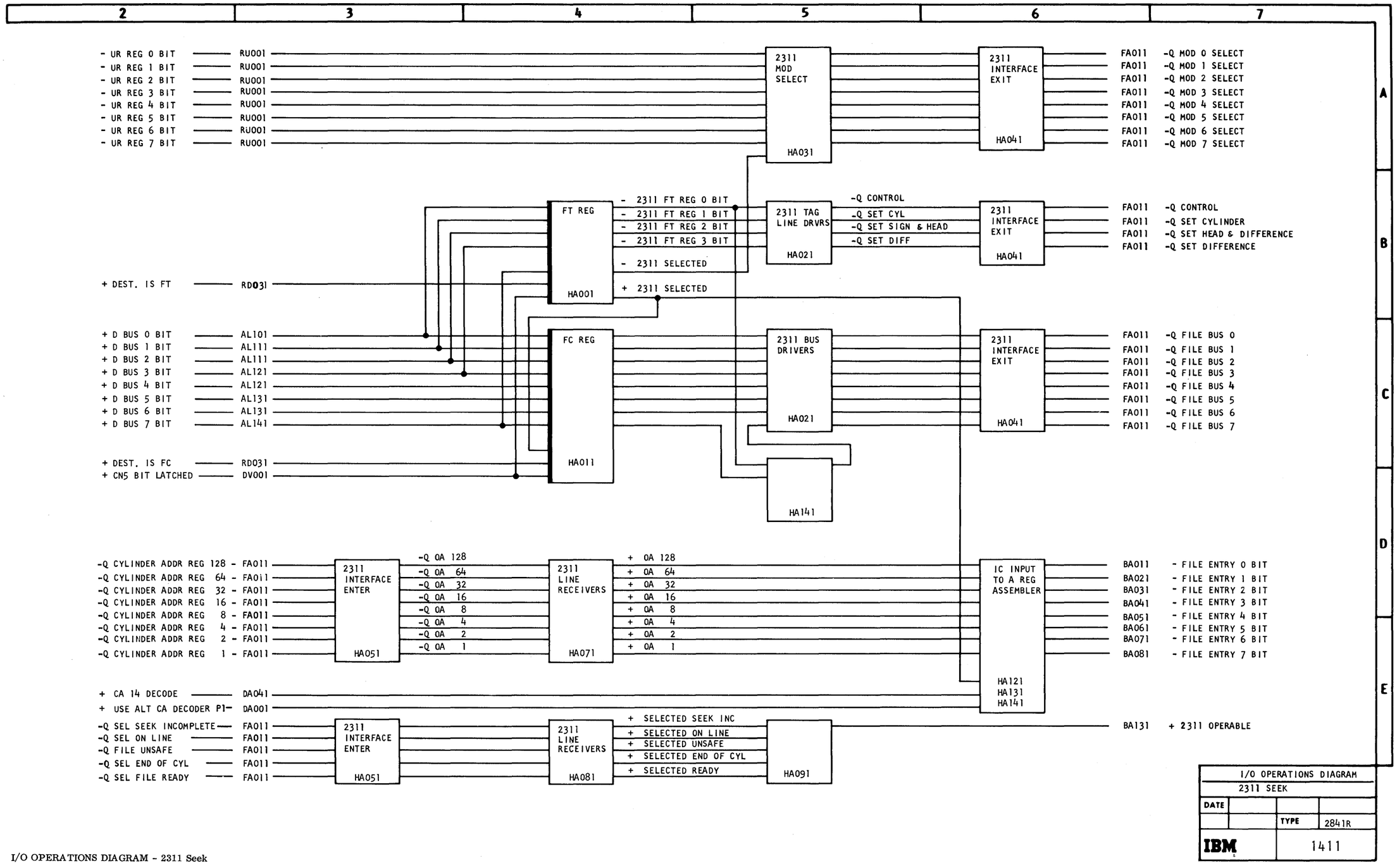


C C FIELD 3 BITS			
BIT 0	BIT 1	BIT 2	
0	0	0	ADD OPR - NO FORCED CAR IN - NO CAR OUT TO ST3
0	0	1	ADD OPR - FORCE CAR IN - NO CAR OUT TO ST3
0	1	0	AND OPERATION
0	1	1	OR OPERATION
1	0	0	ADD OPR - NO FORCED CAR IN - LAT CAR OUT TO ST3
1	0	1	ADD OPR - FORCE CAR IN - LAT CAR OUT TO ST3
1	1	0	ADD OPR - ADD IN ST3 - LATCH CARRY OUT TO ST3
1	1	1	EXCLUSIVE OR

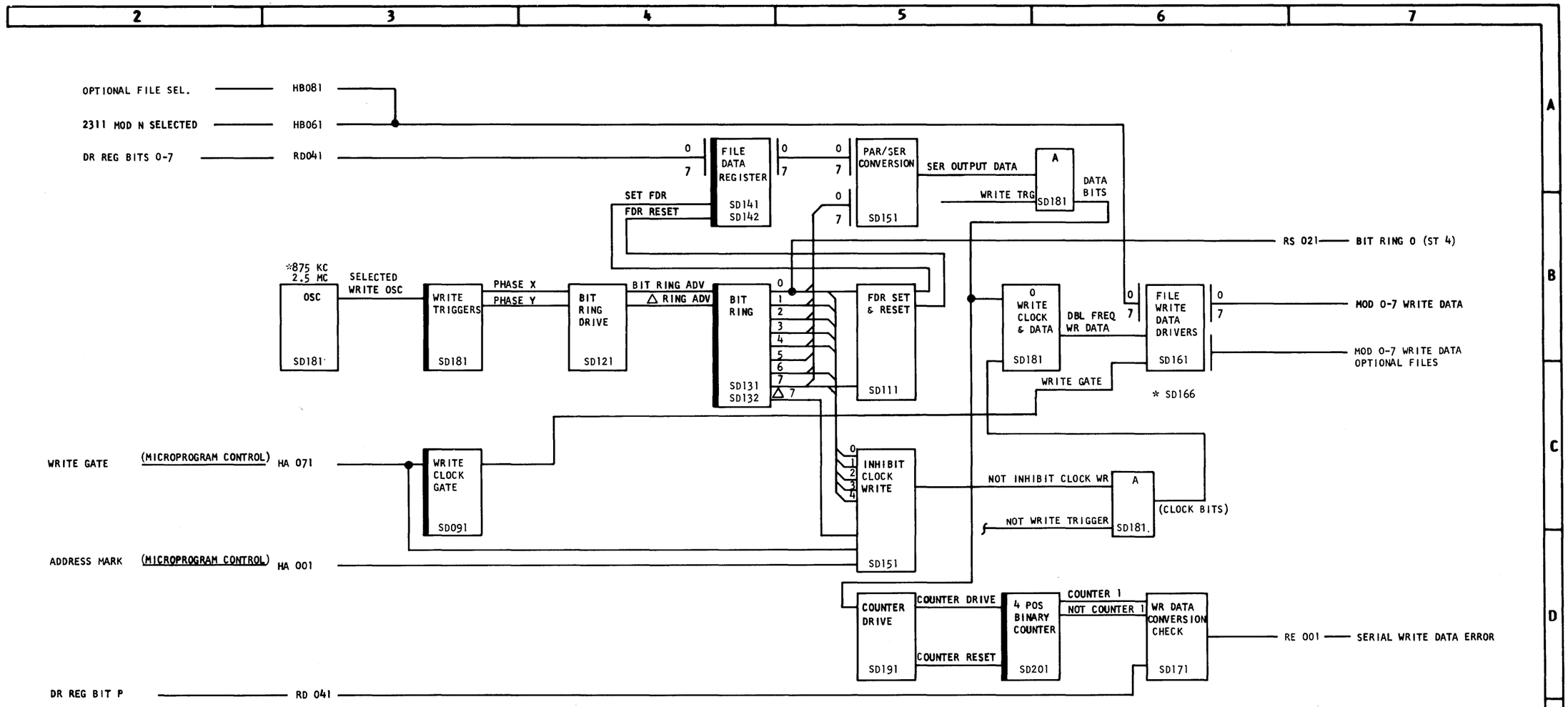
ALU CONTROL LINES						
	AND	$\overline{\text{AND}}$	A/OR	$\overline{\text{A/OR}}$	CARRY	$\overline{\text{CARRY}}$
ADD	OFF	ON	ON	OFF	OFF	ON
EXCLUSIVE OR	OFF	ON	ON	OFF	ON	OFF
AND	ON	OFF	OFF	ON	ON	OFF
OR	OFF	ON	OFF	ON	ON	OFF

BIT N	ALU ALXXX	D POWER ALYYY
0	AL001	AL101
1	AL011	AL111
2	AL021	AL111
3	AL031	AL121
4	AL041	AL121
5	AL051	AL131
6	AL061	AL131
7	AL071	AL141

I/O OPERATIONS DIAGRAM			
STORAGE CONTROL ALU			
DATE			
		TYPE	2841R
IBM		1401	



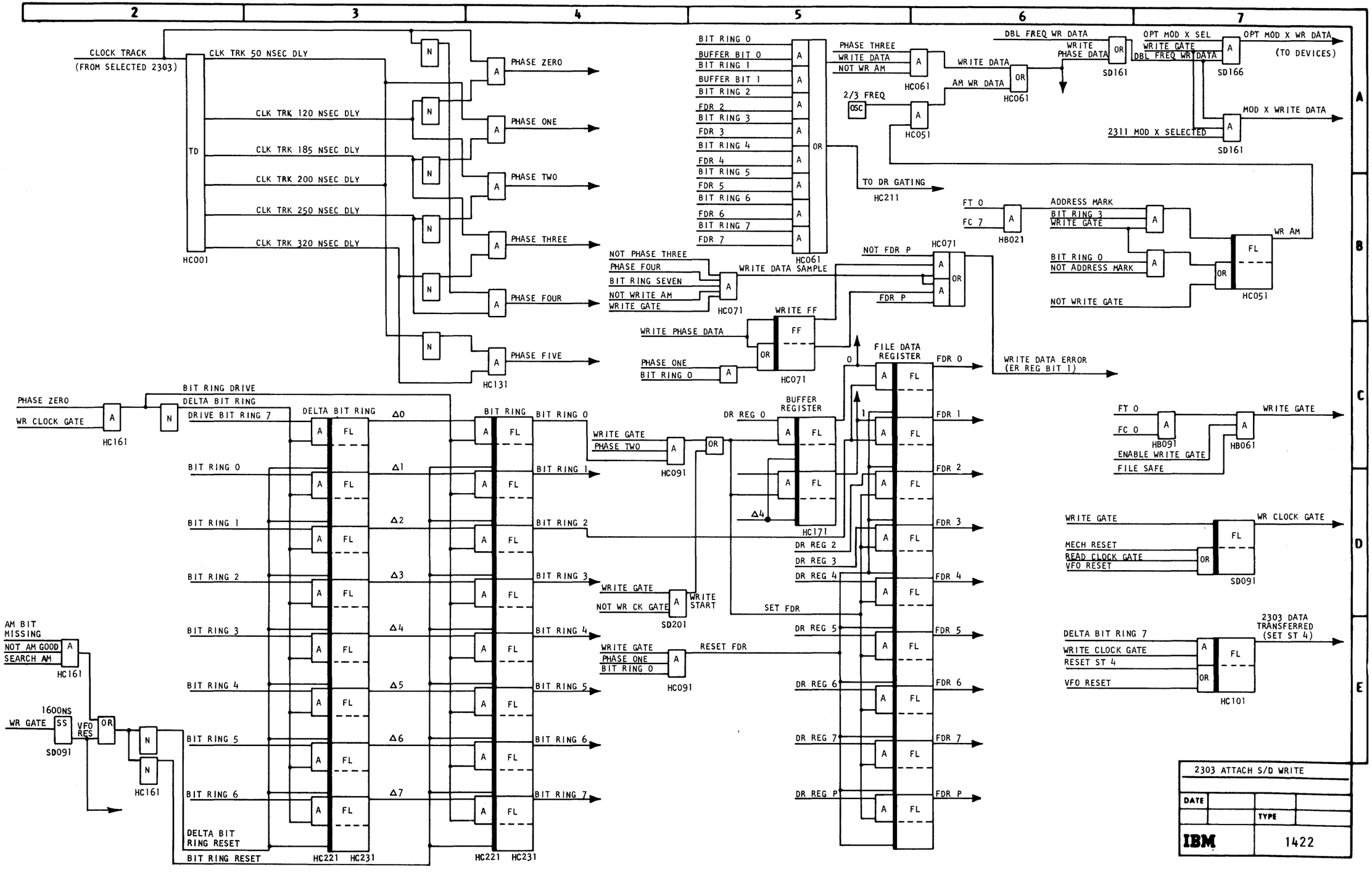
I/O OPERATIONS DIAGRAM - 2311 Seek



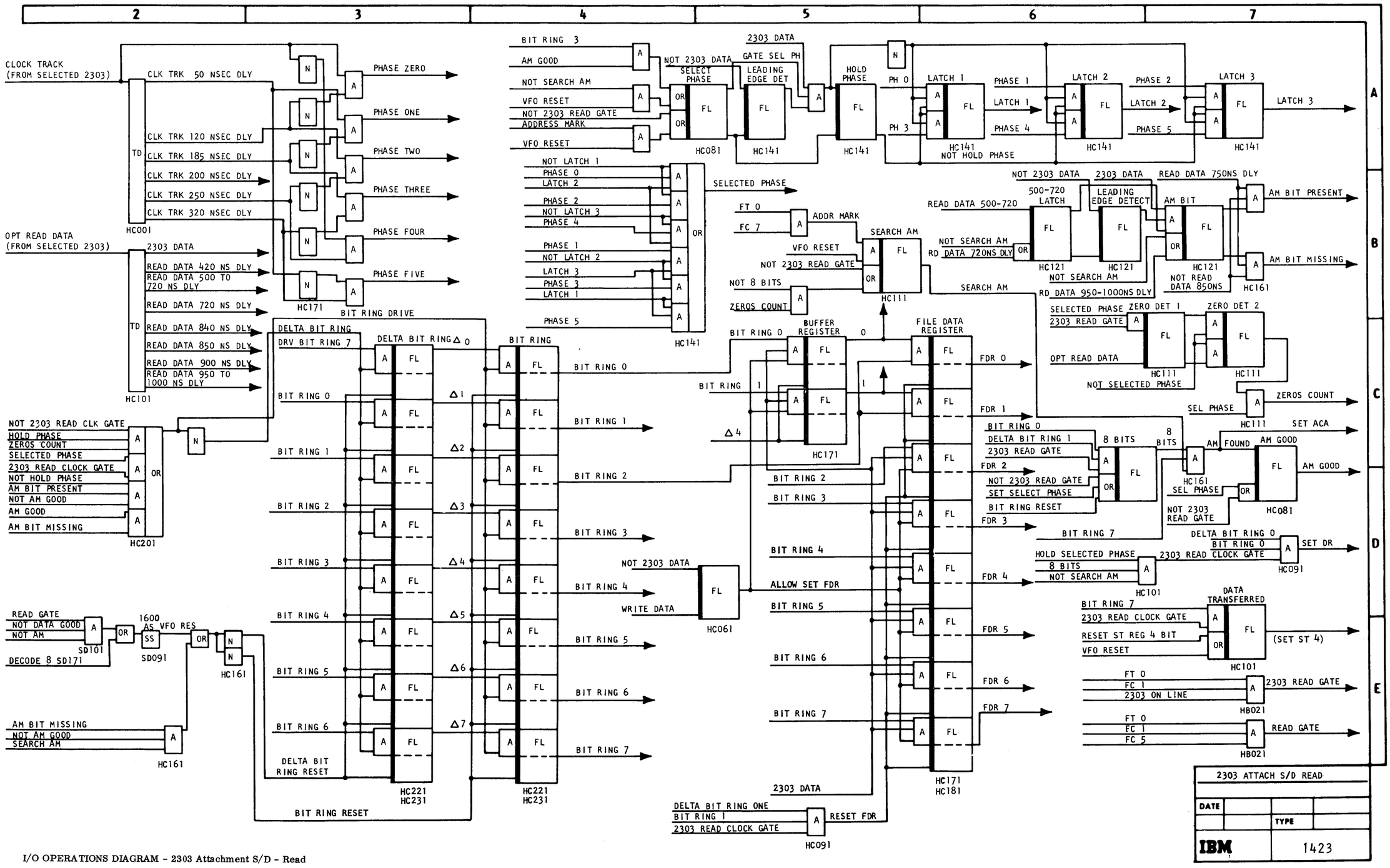
* = 2321 REFERENCE

I/O OPERATIONS DIAGRAM - Write/Write AM

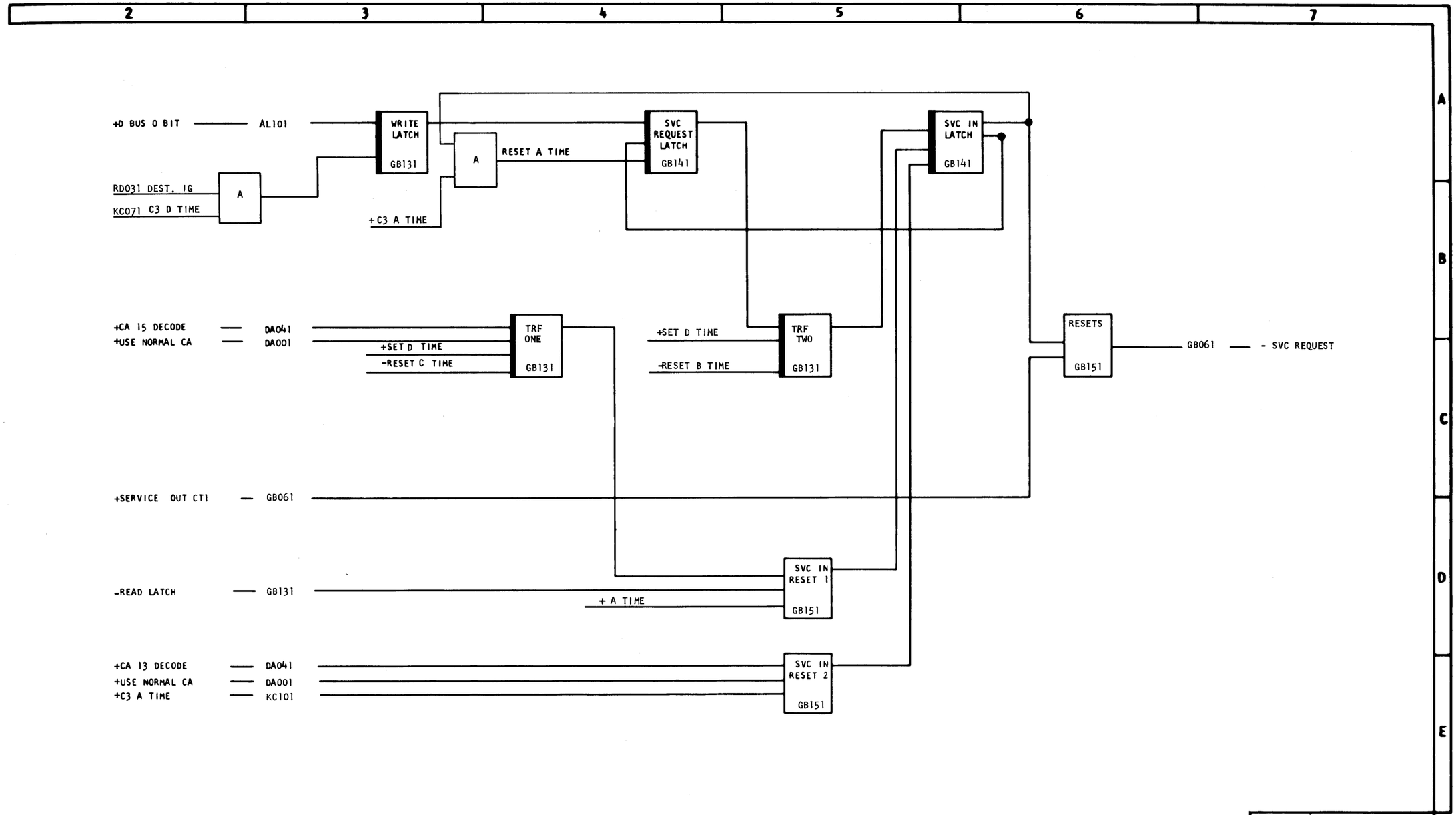
I/O OPERATIONS DIAGRAM			
WRITE/WRITE AM			
DATE			
		TYPE	2841R
IBM		1421	



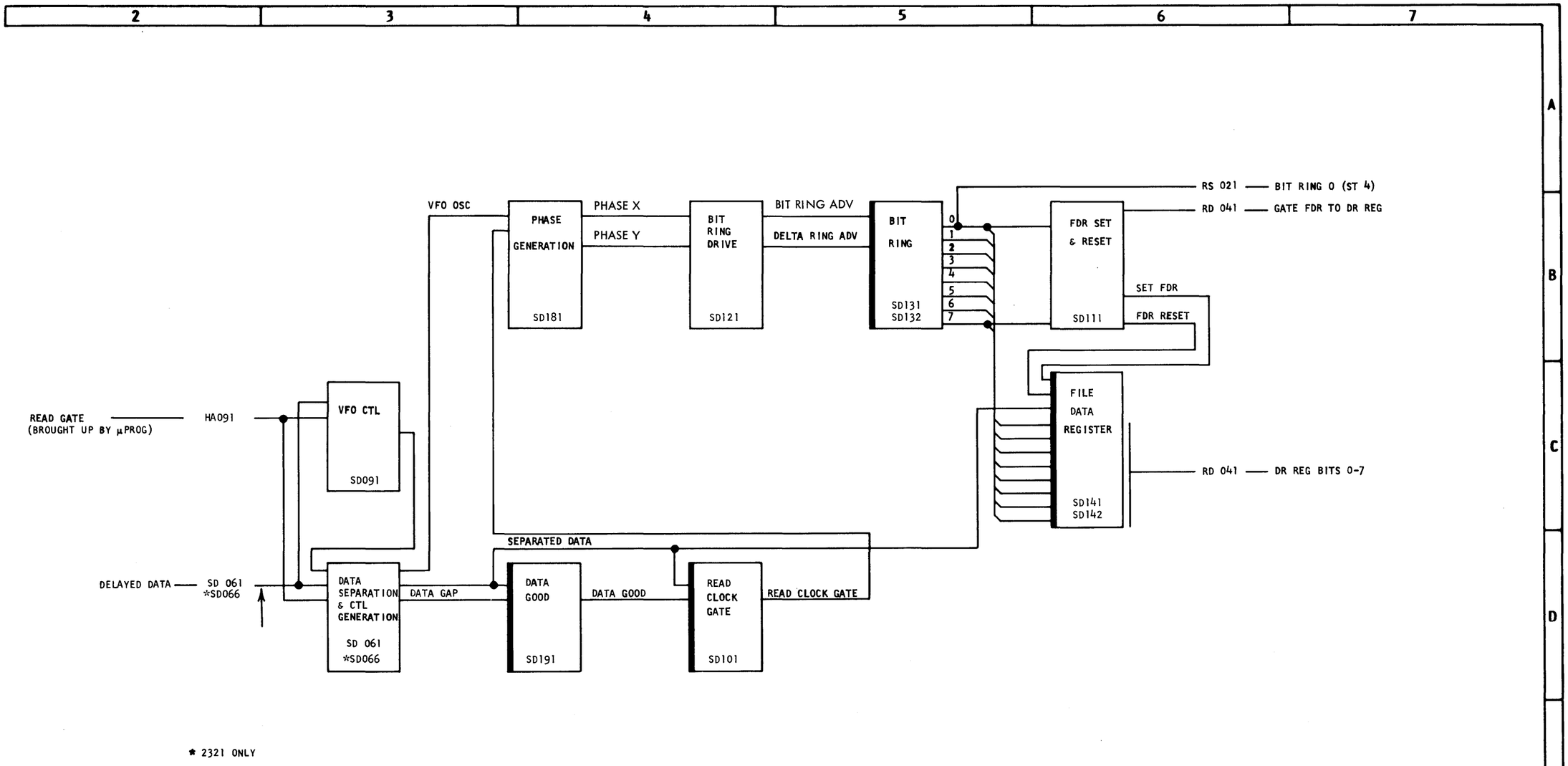
I/O OPERATIONS DIAGRAM - 2303 Attachment S/D - Write



I/O OPERATIONS DIAGRAM - 2303 Attachment S/D - Read

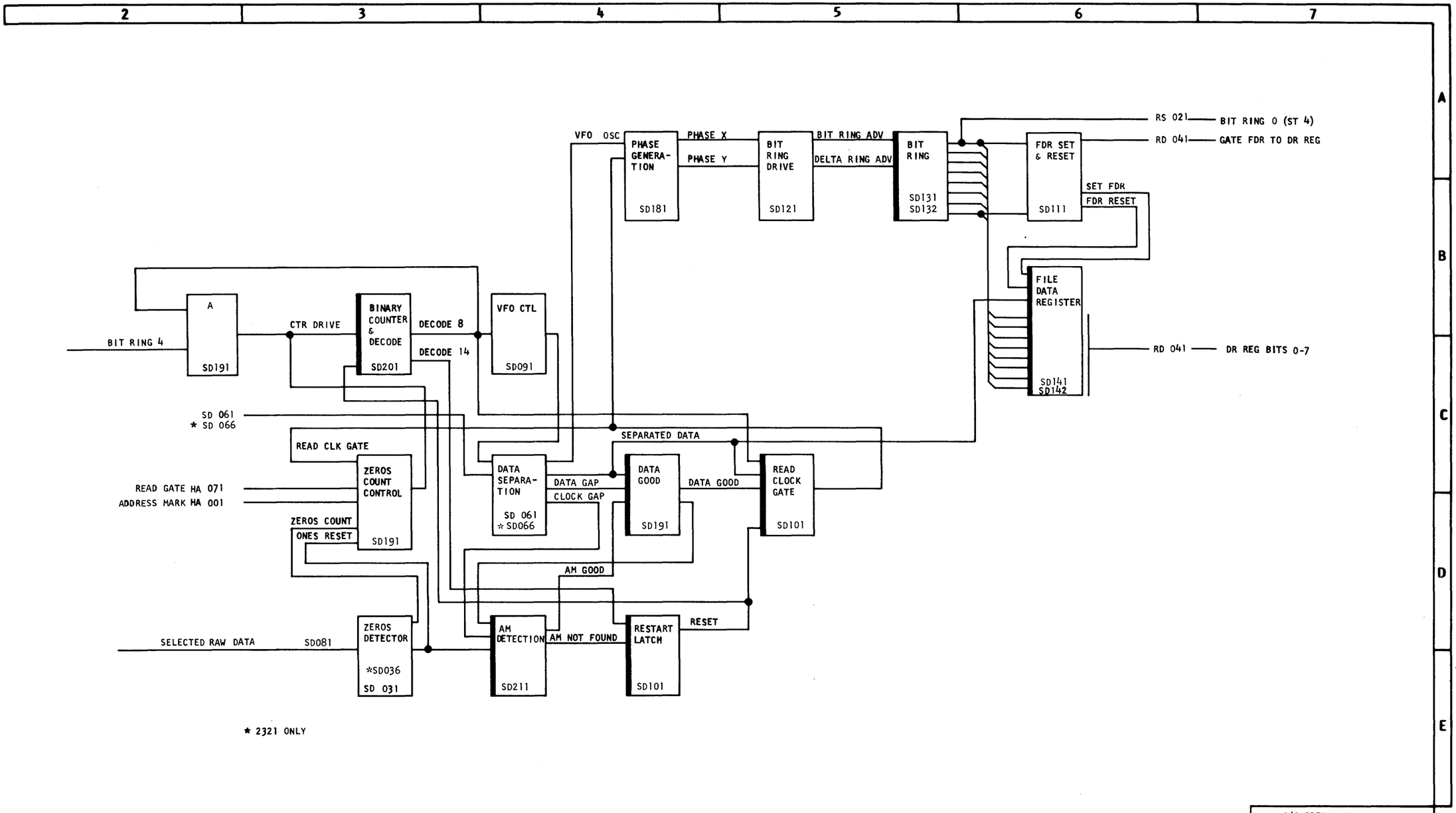


I/O OPERATIONS DIAGRAM - Channel Data Trnasfer - Write



* 2321 ONLY

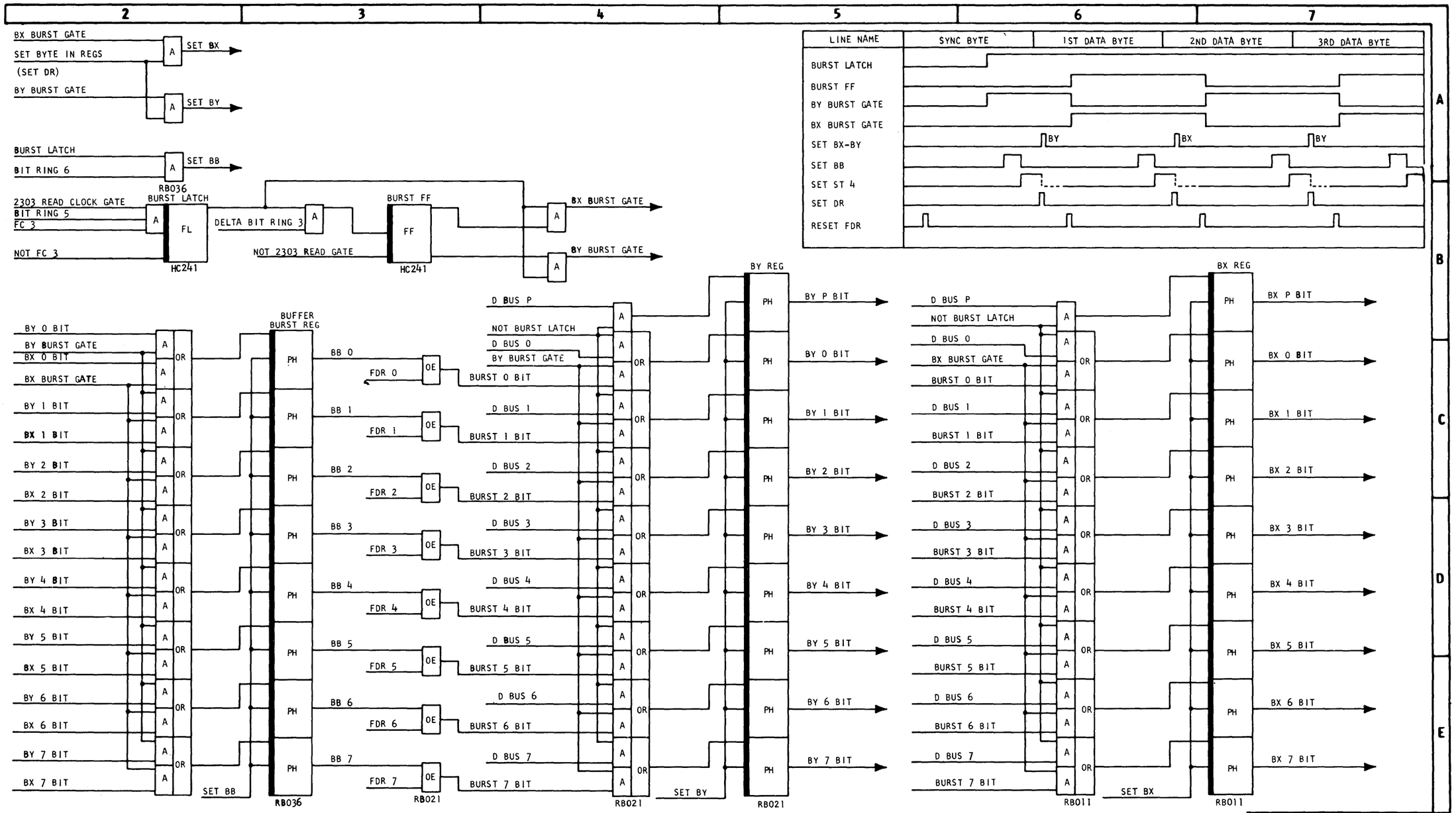
I/O OPERATIONS DIAGRAM			
READ			
DATE			
		TYPE	2841R
IBM		1431	



* 2321 ONLY

I/O OPERATIONS DIAGRAM - Read Address Mark

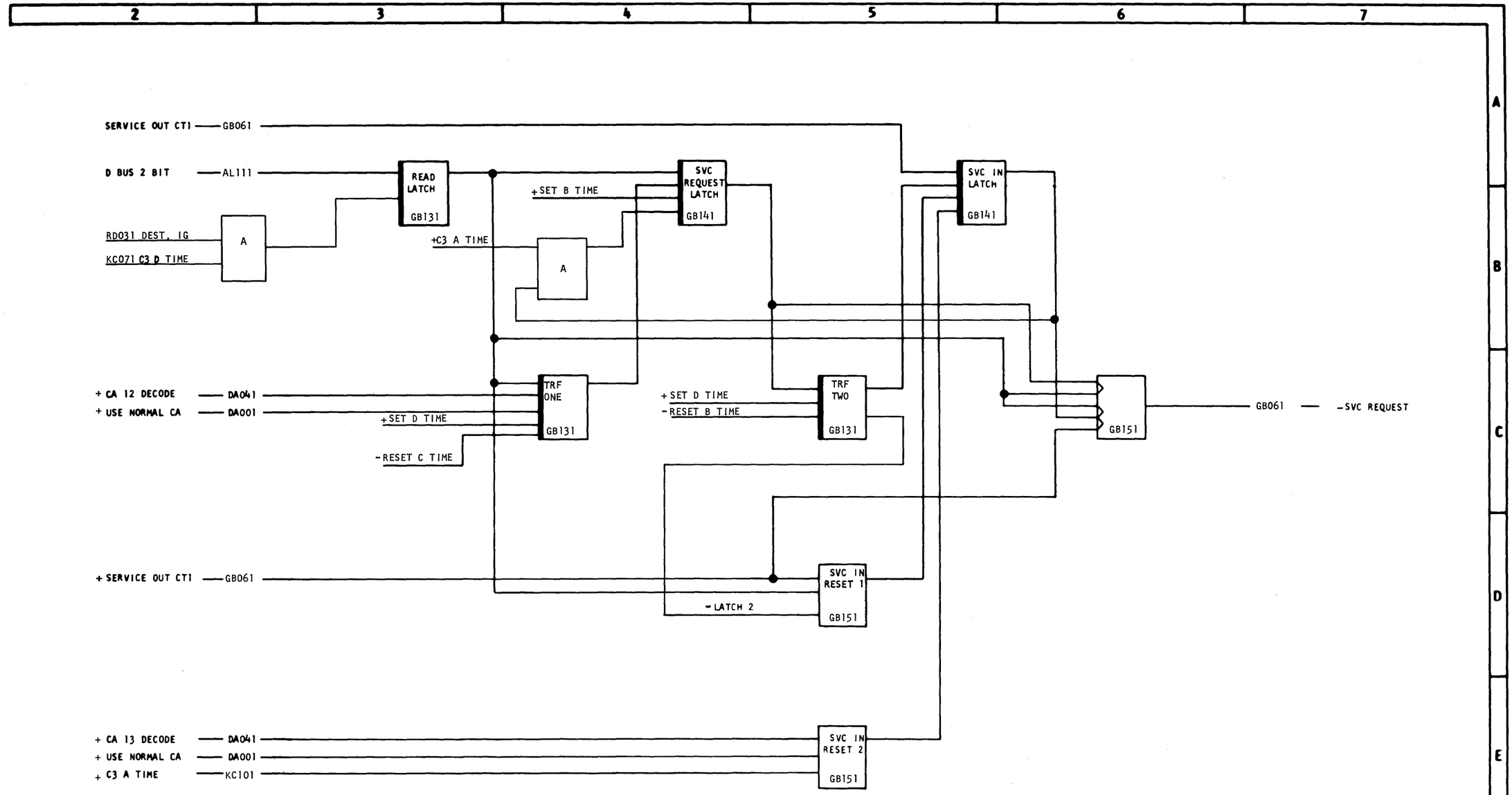
I/O OPERATIONS DIAGRAM			
READ ADDRESS MARK			
DATE			
		TYPE	2841R
IBM	1433		



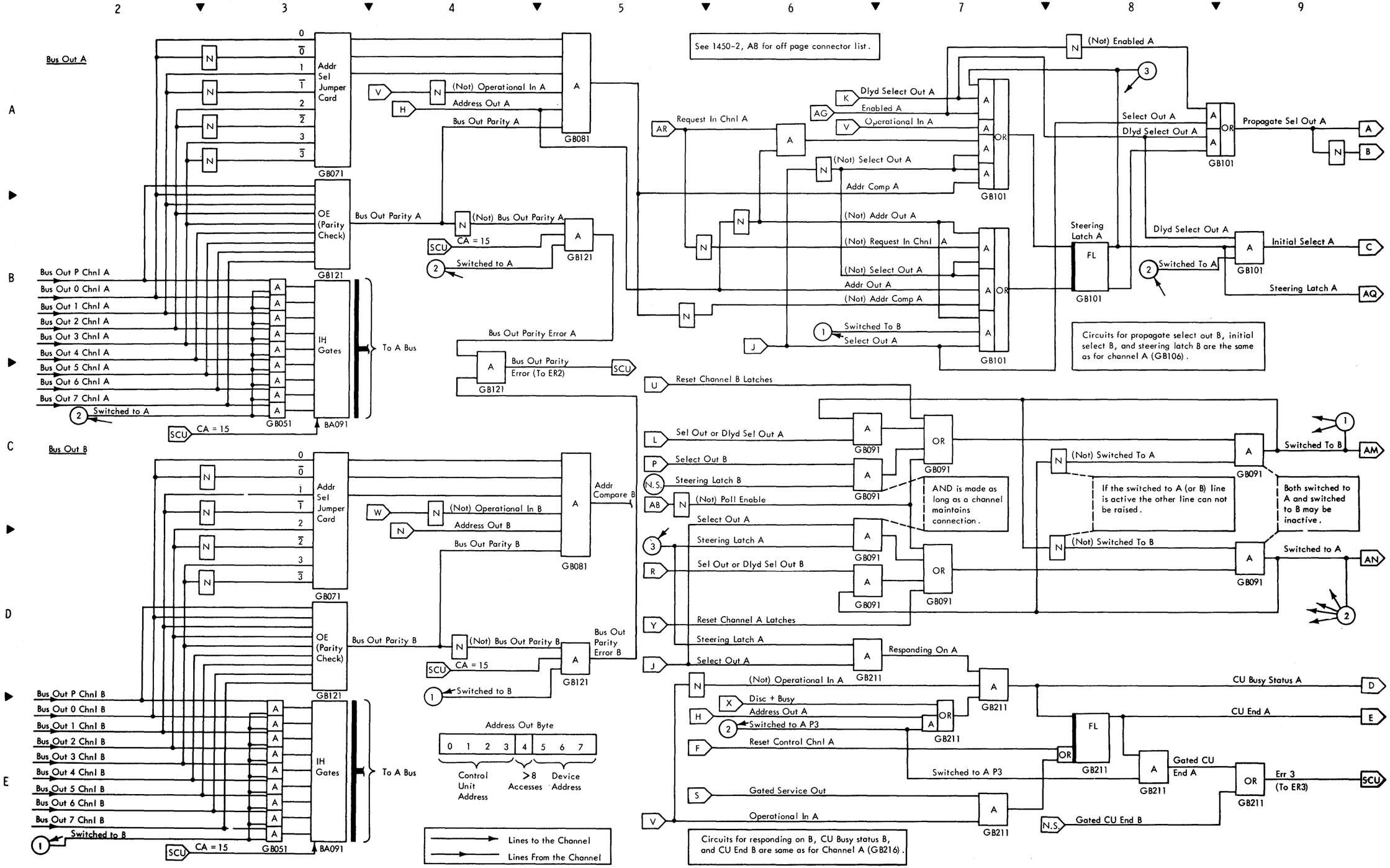
BURST CHECK DATA FLOW
2303 ATTACHMENT

DATE			
		TYPE	2841R
IBM		1434	

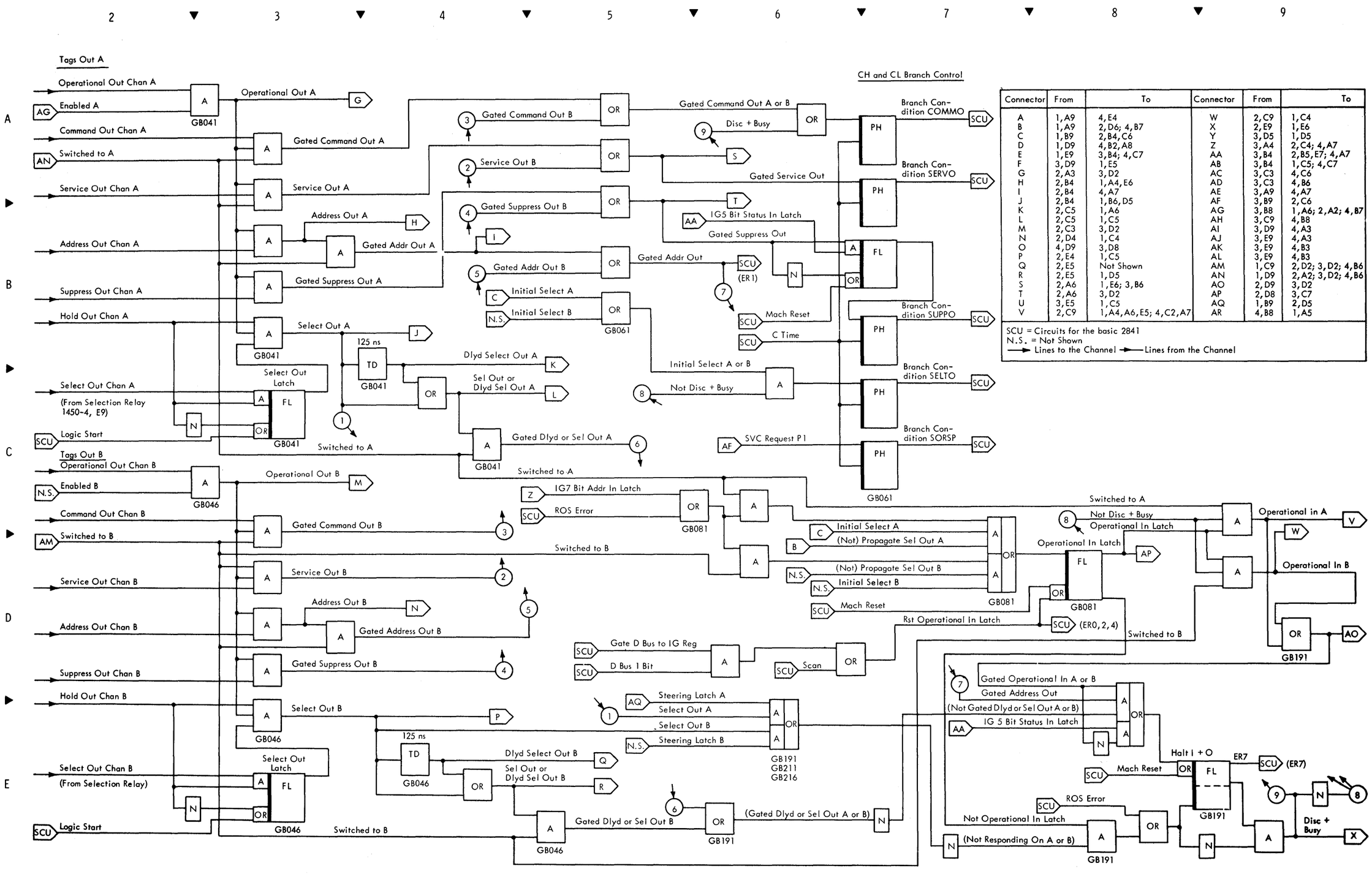
I/O OPERATIONS DIAGRAM - 2303 Attachment S/D - Burst Check Data Flow



I/O OPERATIONS DIAGRAM - Channel Data Transfer - Read

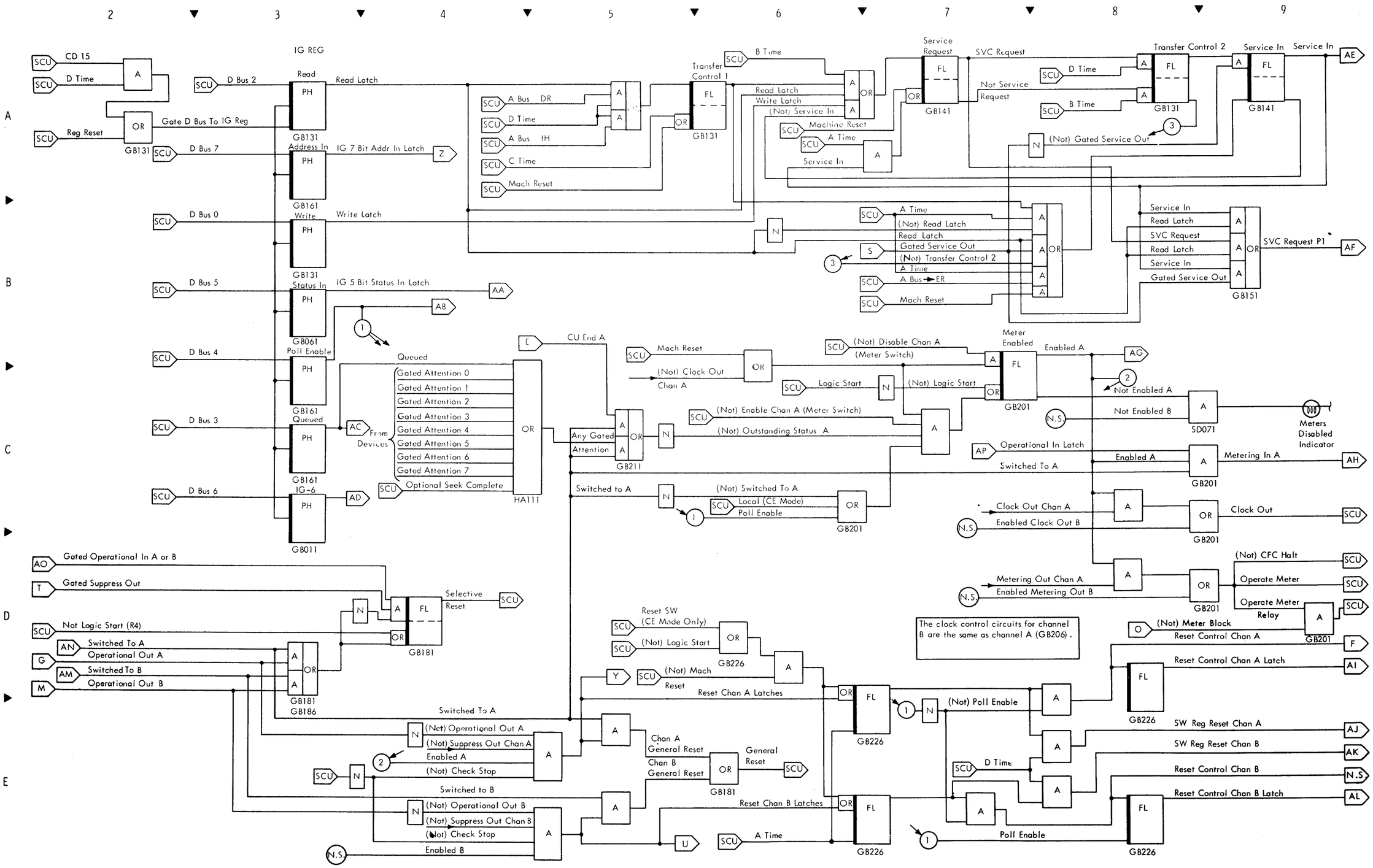


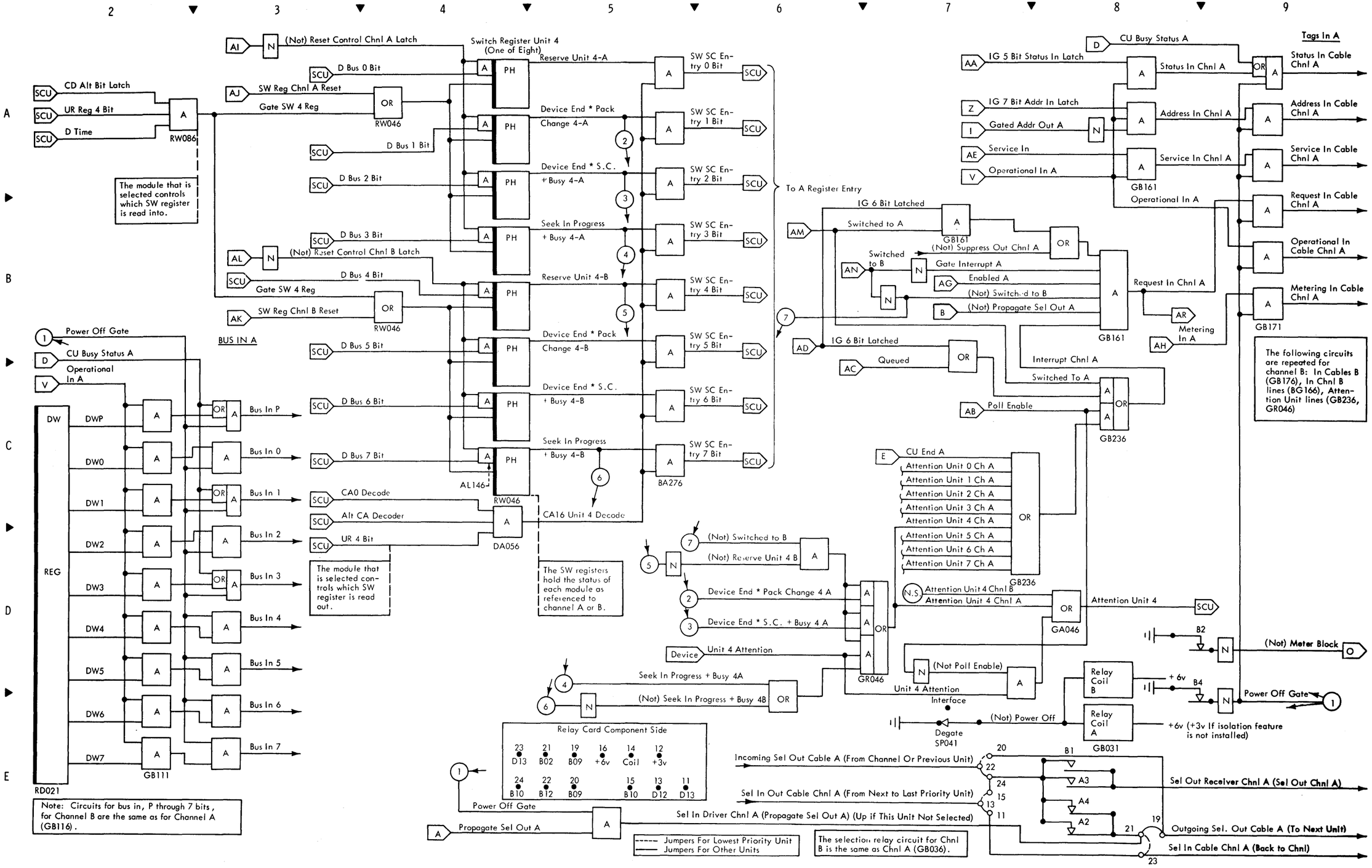
Two Channel Interface - Part 1

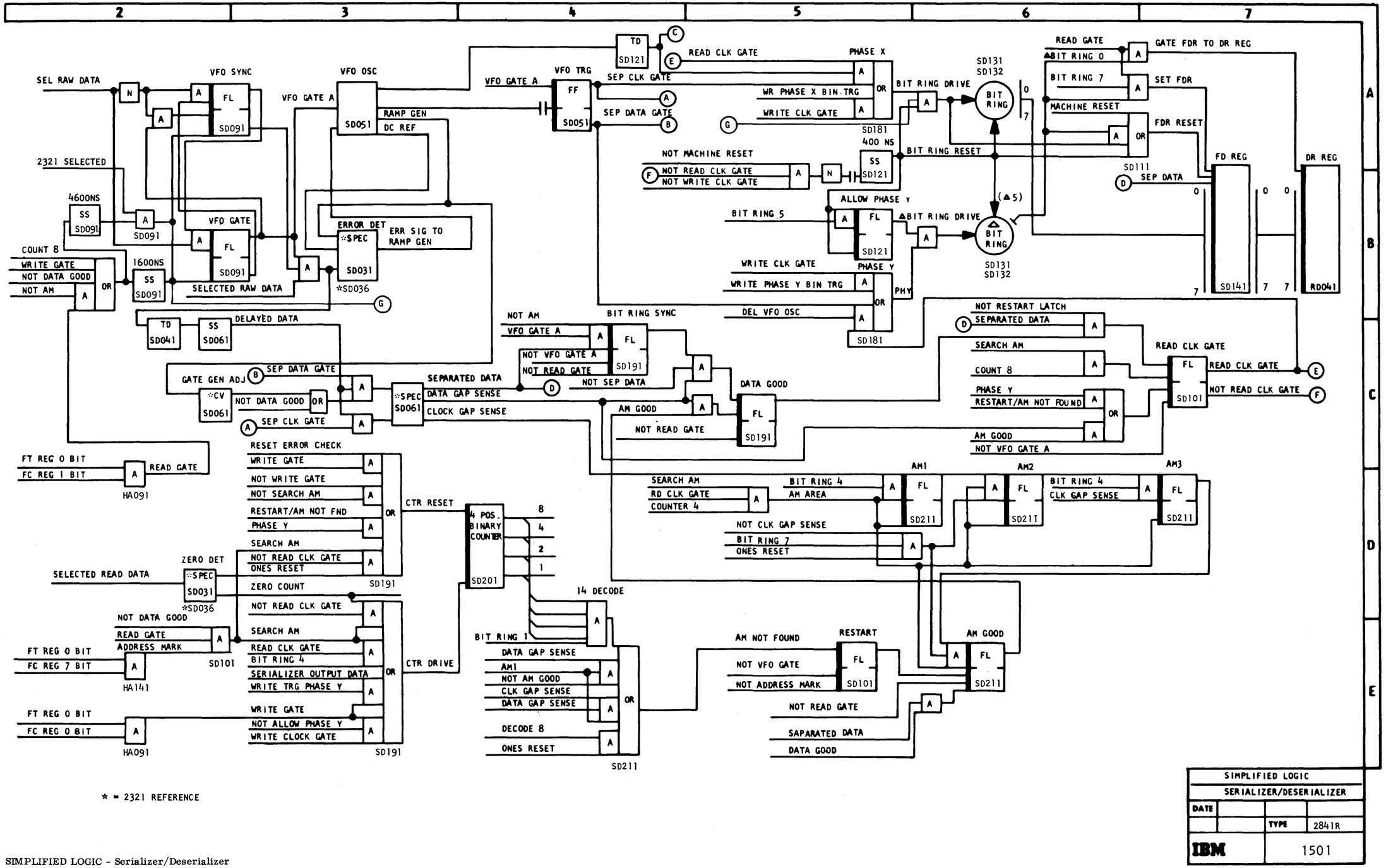


Connector	From	To	Connector	From	To
A	1,A9	4,E4	W	2,C9	1,C4
B	1,A9	2,D6; 4,B7	X	2,E9	1,E6
C	1,B9	2,B4,C6	Y	3,D5	1,D5
D	1,D9	4,B2,A8	Z	3,A4	2,C4; 4,A7
E	1,E9	3,B4; 4,C7	AA	3,B4	2,B5,E7; 4,A7
F	3,D9	1,E5	AB	3,B4	1,C5; 4,C7
G	2,A3	3,D2	AC	3,C3	4,C6
H	2,B4	1,A4,E6	AD	3,C3	4,B6
I	2,B4	4,A7	AE	3,A9	4,A7
J	2,B4	1,B6,D5	AF	3,B9	2,C6
K	2,C5	1,A6	AG	3,B8	1,A6; 2,A2; 4,B7
L	2,C5	1,C5	AH	3,C9	4,B8
M	2,C3	3,D2	AI	3,D9	4,A3
N	2,D4	1,C4	AJ	3,E9	4,A3
O	4,D9	3,D8	AK	3,E9	4,B3
P	2,E4	1,C5	AL	3,E9	4,B3
Q	2,E5	Not Shown	AM	1,C9	2,D2; 3,D2; 4,B6
R	2,E5	1,D5	AN	1,D9	2,A2; 3,D2; 4,B6
S	2,A6	1,E6; 3,B6	AO	2,D9	3,D2
T	2,A6	3,D2	AP	2,D8	3,C7
U	3,E5	1,C5	AQ	1,B9	2,D5
V	2,C9	1,A4,A6,E5; 4,C2,A7	AR	4,B8	1,A5

SCU = Circuits for the basic 2841
N.S. = Not Shown
→ Lines to the Channel →— Lines from the Channel


2
3
4
5
6
7
8
9
A
B
C
D
E
IG REG
CD 15
D Time
Reg Reset
Gate D Bus To IG Reg
GB131
D Bus 2
Read
Read Latch
GB131
D Bus 7
Address In
IG 7 Bit Addr In Latch
Z
GB161
D Bus 0
Write
Write Latch
GB131
D Bus 5
Status In
IG 5 Bit Status In Latch
AA
AB
GB061
D Bus 4
Poll Enable
GB161
D Bus 3
Queued
AC
From Devices
GB161
D Bus 6
IG-6
AD
GB011
A Bus DR
D Time
A Bus tH
C Time
Mach Reset
Transfer Control 1
GB131
B Time
Read Latch
Write Latch
(Not) Service In
Machine Reset
A Time
Service In
Service Request
GB141
SVC Request
Not Service Request
D Time
B Time
Transfer Control 2
GB131
Service In
GB141
Service In
AE
(Not) Gated Service Out
A Time
(Not) Read Latch
Read Latch
Gated Service Out
(Not) Transfer Control 2
A Time
A Bus ER
Mach Reset
Service In
Read Latch
SVC Request
Read Latch
Service In
Gated Service Out
GB151
SVC Request P1
AF
Queued
Gated Attention 0
Gated Attention 1
Gated Attention 2
Gated Attention 3
Gated Attention 4
Gated Attention 5
Gated Attention 6
Gated Attention 7
Optional Seek Complete
HA111
E
CU End A
OR
Any Gated Attention
GB211
Switched to A
(Not) Switched To A
Local (CE Mode)
Poll Enable
GB201
Mach Reset
(Not) Clock Out Chan A
(Not) Disable Chan A (Meter Switch)
Logic Start
(Not) Logic Start
Meter Enabled
Enabled A
GB201
AG
Not Enabled A
Not Enabled B
SD071
Meters Disabled Indicator
(Not) Enable Chan A (Meter Switch)
(Not) Outstanding Status A
AP
Operational In Latch
Switched To A
Enabled A
Metering In A
AH
GB201
Clock Out Chan A
Enabled Clock Out B
Clock Out
SCU
GB201
Metering Out Chan A
Enabled Metering Out B
(Not) CFC Halt
Operate Meter
Operate Meter Relay
GB201
AO
Gated Operational In A or B
T
Gated Suppress Out
Not Logic Start (R4)
AN
Switched To A
Operational Out A
G
AM
Switched To B
Operational Out B
M
GB181
GB186
Selective Reset
GB181
Switched To A
(Not) Operational Out A
(Not) Suppress Out Chan A
Enabled A
(Not) Check Stop
Switched to B
(Not) Operational Out B
(Not) Suppress Out Chan B
(Not) Check Stop
Enabled B
Reset SW (CE Mode Only)
(Not) Logic Start
(Not) Mach Reset
GB226
Reset Chan A Latches
Reset Chan B Latches
Chan A General Reset
Chan B General Reset
General Reset
GB181
A Time
U
Y
GB226
(Not) Poll Enable
Poll Enable
D Time
SW Reg Reset Chan A
SW Reg Reset Chan B
Reset Control Chan B
Reset Control Chan B Latch
AJ
AK
N.S
AL
GB226
The clock control circuits for channel B are the same as channel A (GB206).
O
(Not) Meter Block Reset Control Chan A
F
Reset Control Chan A Latch
AI
GB226

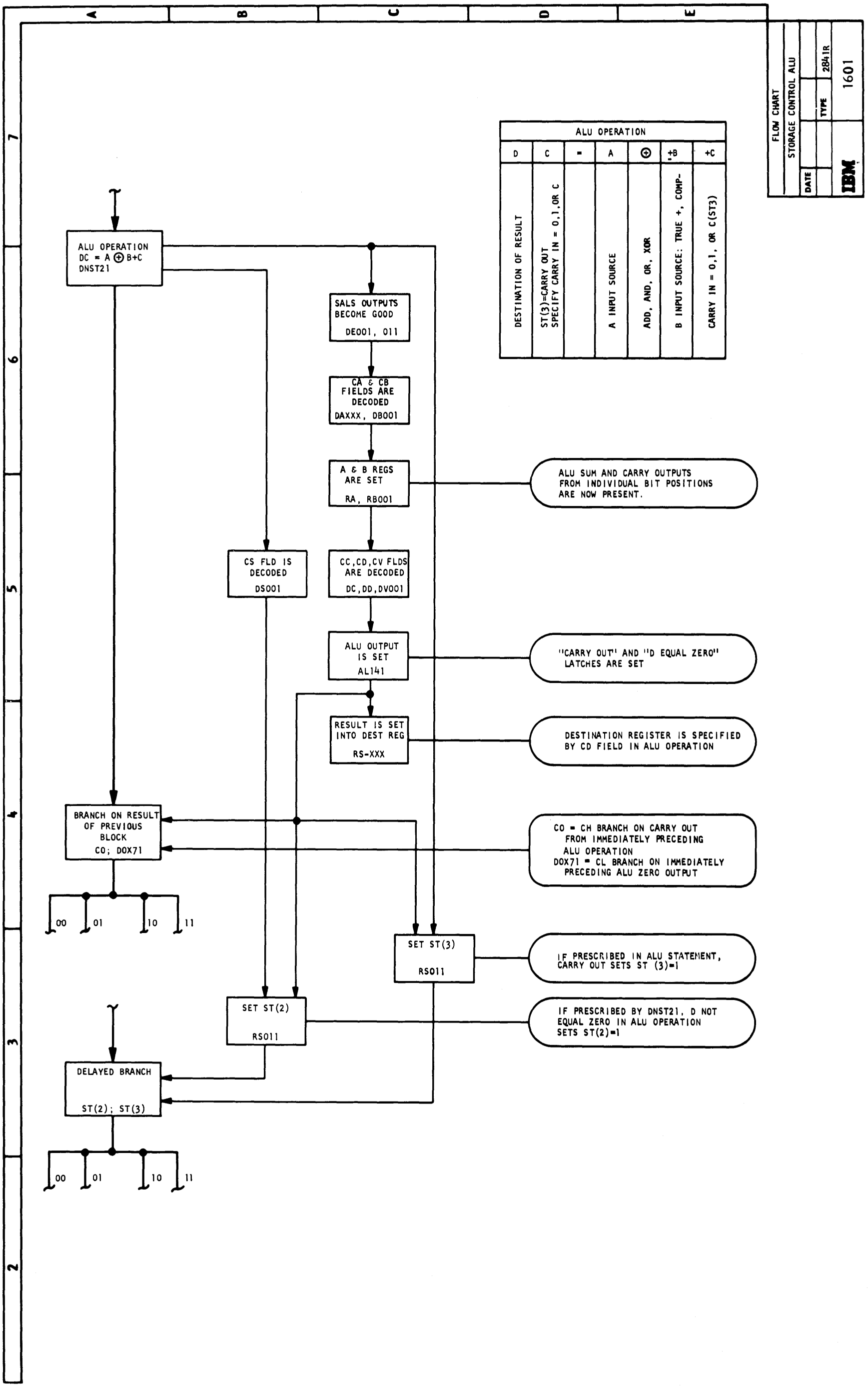

2
3
4
5
6
7
8
9
A
B
C
D
E
CD Alt Bit Latch
UR Reg 4 Bit
D Time
RW086
The module that is selected controls which SW register is read into.
(Not) Reset Control Chnl A Latch
D Bus 0 Bit
SW Reg Chnl A Reset
Gate SW 4 Reg
RW046
D Bus 1 Bit
D Bus 2 Bit
D Bus 3 Bit
(Not) Reset Control Chnl B Latch
D Bus 4 Bit
Gate SW 4 Reg
SW Reg Chnl B Reset
BUS IN A
D Bus 5 Bit
D Bus 6 Bit
D Bus 7 Bit
CA0 Decode
Alt CA Decoder
UR 4 Bit
The module that is selected controls which SW register is read out.
Switch Register Unit 4 (One of Eight)
Reserve Unit 4-A
Device End * Pack Change 4-A
Device End * S.C. + Busy 4-A
Seek In Progress + Busy 4-A
Reserve Unit 4-B
Device End * Pack Change 4-B
Device End * S.C. + Busy 4-B
Seek In Progress + Busy 4-B
AL146
CA16 Unit 4 Decode
DA056
The SW registers hold the status of each module as referenced to channel A or B.
SW SC Entry 0 Bit
SW SC Entry 1 Bit
SW SC Entry 2 Bit
SW SC Entry 3 Bit
SW SC Entry 4 Bit
SW SC Entry 5 Bit
SW SC Entry 6 Bit
SW SC Entry 7 Bit
BA276
To A Register Entry
Power Off Gate
CU Busy Status A
Operational In A
DW
DWP
DW0
DW1
DW2
DW3
DW4
DW5
DW6
DW7
REG
RD021
GB111
Bus In P
Bus In 0
Bus In 1
Bus In 2
Bus In 3
Bus In 4
Bus In 5
Bus In 6
Bus In 7
Note: Circuits for bus in, P through 7 bits, for Channel B are the same as for Channel A (GB116).
Relay Card Component Side
23 D13
21 B02
19 B09
16 +6v
14 Coil
12 +3v
24 B10
22 B12
20 B09
15 B10
13 D12
11 D13
Propagate Sel Out A
Power Off Gate
Incoming Sel Out Cable A (From Channel Or Previous Unit)
Sel In Out Cable Chnl A (From Next to Last Priority Unit)
Sel In Driver Chnl A (Propagate Sel Out A) (Up if This Unit Not Selected)
Jumpers For Lowest Priority Unit
Jumpers For Other Units
The selection relay circuit for Chnl B is the same as Chnl A (GB036).
Sel Out Receiver Chnl A (Sel Out Chnl A)
Outgoing Sel. Out Cable A (To Next Unit)
Sel In Cable Chnl A (Back to Chnl)
IG 6 Bit Latched
Switched to A
GB161
(Not) Suppress Out Chnl A
Switched to B
Gate Interrupt A
Enabled A
(Not) Switched to B
(Not) Propagate Sel Out A
Request In Chnl A
Metering In A
IG 6 Bit Latched
Queued
Interrupt Chnl A
Switched To A
Poll Enable
GB236
CU End A
Attention Unit 0 Ch A
Attention Unit 1 Ch A
Attention Unit 2 Ch A
Attention Unit 3 Ch A
Attention Unit 4 Ch A
Attention Unit 5 Ch A
Attention Unit 6 Ch A
Attention Unit 7 Ch A
(Not) Switched to B
(Not) Reserve Unit 4 B
Device End * Pack Change 4 A
Device End * S.C. + Busy 4 A
Device
Unit 4 Attention
Seek In Progress + Busy 4A
(Not) Seek In Progress + Busy 4B
GR046
Attention Unit 4 Chnl B
Attention Unit 4 Chnl A
GA046
Attention Unit 4
(Not Poll Enable)
Unit 4 Attention Interface
Degate SP041
(Not) Power Off
Relay Coil B
Relay Coil A
GB031
+6v
+6v (+3v If isolation feature is not installed)
(Not) Meter Block
Power Off Gate
CU Busy Status A
IG 5 Bit Status In Latch
Status In Chnl A
IG 7 Bit Addr In Latch
Gated Addr Out A
Address In Chnl A
Service In
Service In Chnl A
Operational In A
GB161
Request In Chnl A
Metering In A
GB171
Tags In A
Status In Cable Chnl A
Address In Cable Chnl A
Service In Cable Chnl A
Request In Cable Chnl A
Operational In Cable Chnl A
Metering In Cable Chnl A
The following circuits are repeated for channel B: In Cables B (GB176), In Chnl B lines (BG166), Attention Unit lines (GB236, GR046)



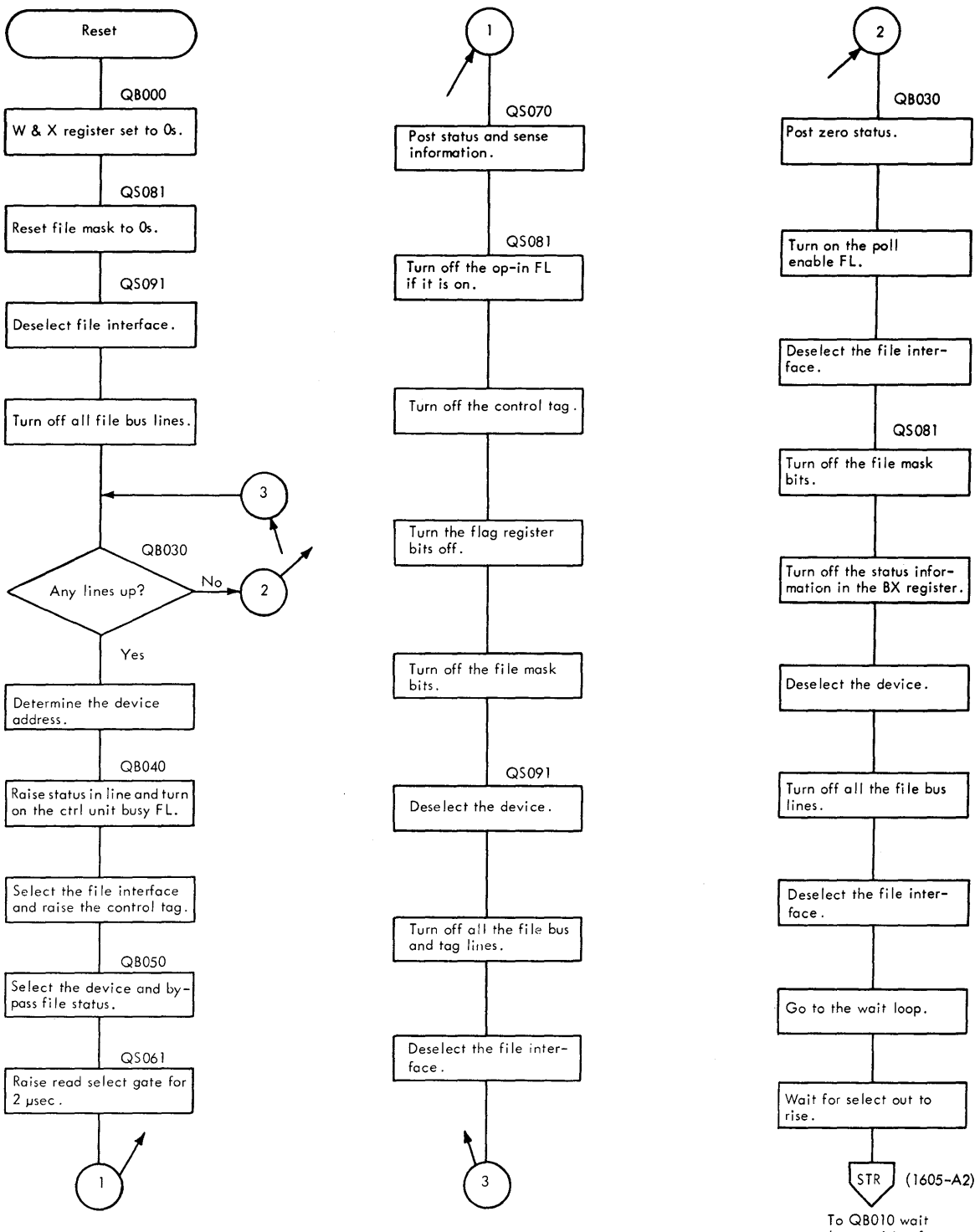
* = 2321 REFERENCE

SIMPLIFIED LOGIC - Serializer/Deserializer

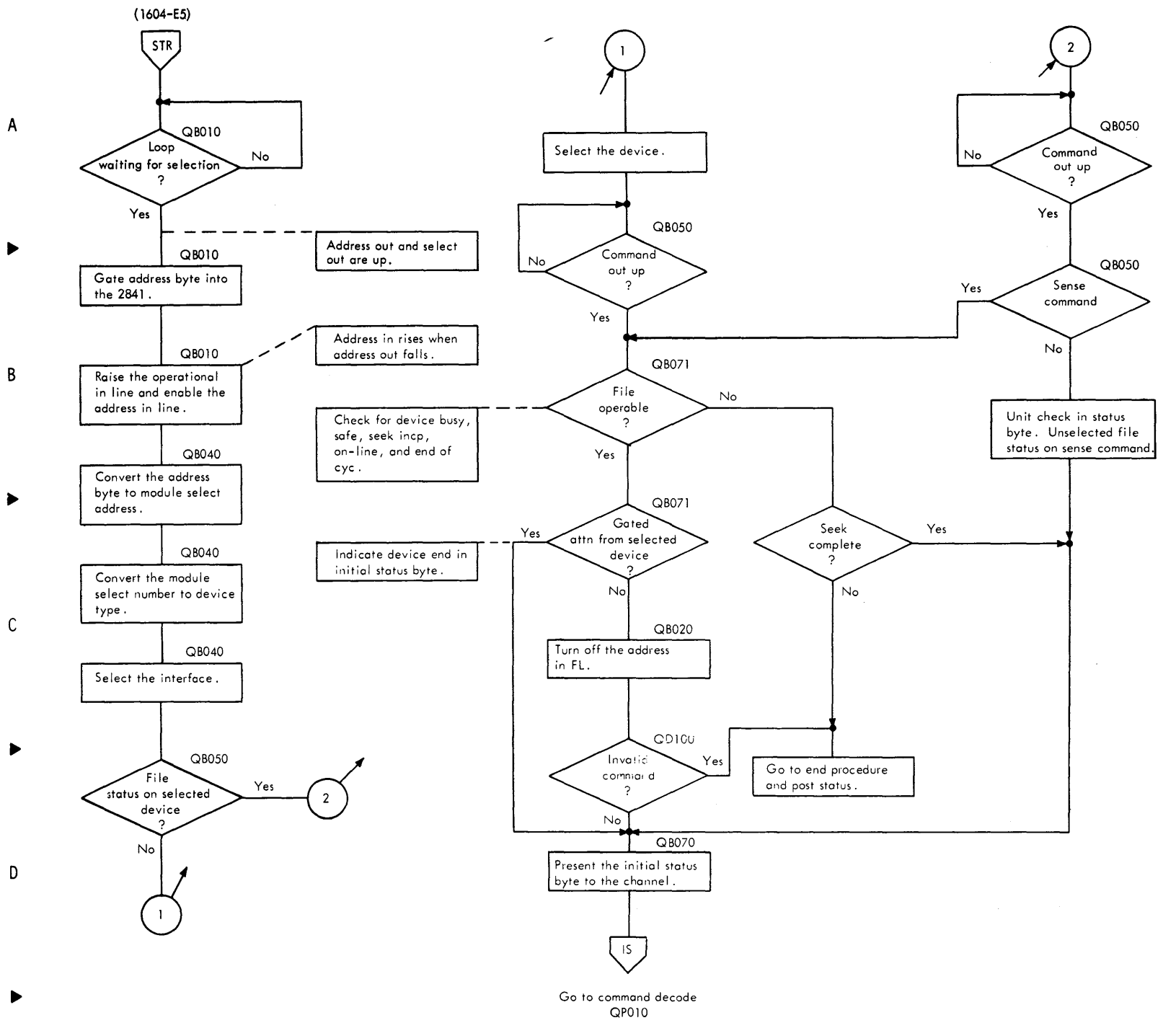
SIMPLIFIED LOGIC			
SERIALIZER/DESERIALIZER			
DATE			
		TYPE	2841R
IBM		1501	



FLOW CHART - Storage Control - ALU



Note: Machine reset and system reset operations are recognized by the ST7 bit. ST7-1 means not system reset. ST7 is also turned on to end reset operation. The 2841 loops from QS030 to QS091 until all outstanding attentions are reset.



FLOW CHART - Initial Selection

2 ▼ 3 ▼ 4 ▼ 5 ▼ 6

A

▶ End procedure determines if a chained or unchained end of operation exists and presents the ending status. Also, in end procedure the 2841 does some of its internal housekeeping in order to save time. For example, erase gate must be dropped 40 μsec after write gate. Instead of just counting 40 μsec, the 2841 starts to process ending procedure but keeps track of the time and turns off erase gate at the proper time. And if the operations are chained, the 2841 must keep track of the time in order to make sure the channel presents the next instruction in time. For example, when doing a search ID equal chained to read data, the read data instruction must be presented in 60 μsec because of device speed or else the 2841 reads the wrong data.

The 2841 keeps track of time by bumping a counter every other micro program word (I.E. every microsecond). (BX + 0 + 1 ⟶ BX). By initially setting BX equal to a number and branching on carry (counter overflow), the 2841 can keep track of time. The size of the number set in BX varies depending on the amount
B of time delay needed for a device or an instruction operation.

Therefore all through ending procedure, the 2841 is continually checking carry and index. If either carry or index is detected, the 2841 branches to these routines. When entering these routines, the program is under control of the ST register bits 0, 6, & 7 as shown in chart below.

▶

ST ⟶	0	6	7	
	1	1	1	Formatting: Do nothing
	0	1	1	Turn off write gate
	0	0	1	Turn off erase gate
C	1	0	1	Check safe
	1	0	0	Head selected: Read, write, both off
	1	1	0	Read gate on
	0	1	0	Head is not selected

▶ Entrance to end procedure is done on QS010 or QS020 for the majority of the instructions.

D

▶

E

▶

F

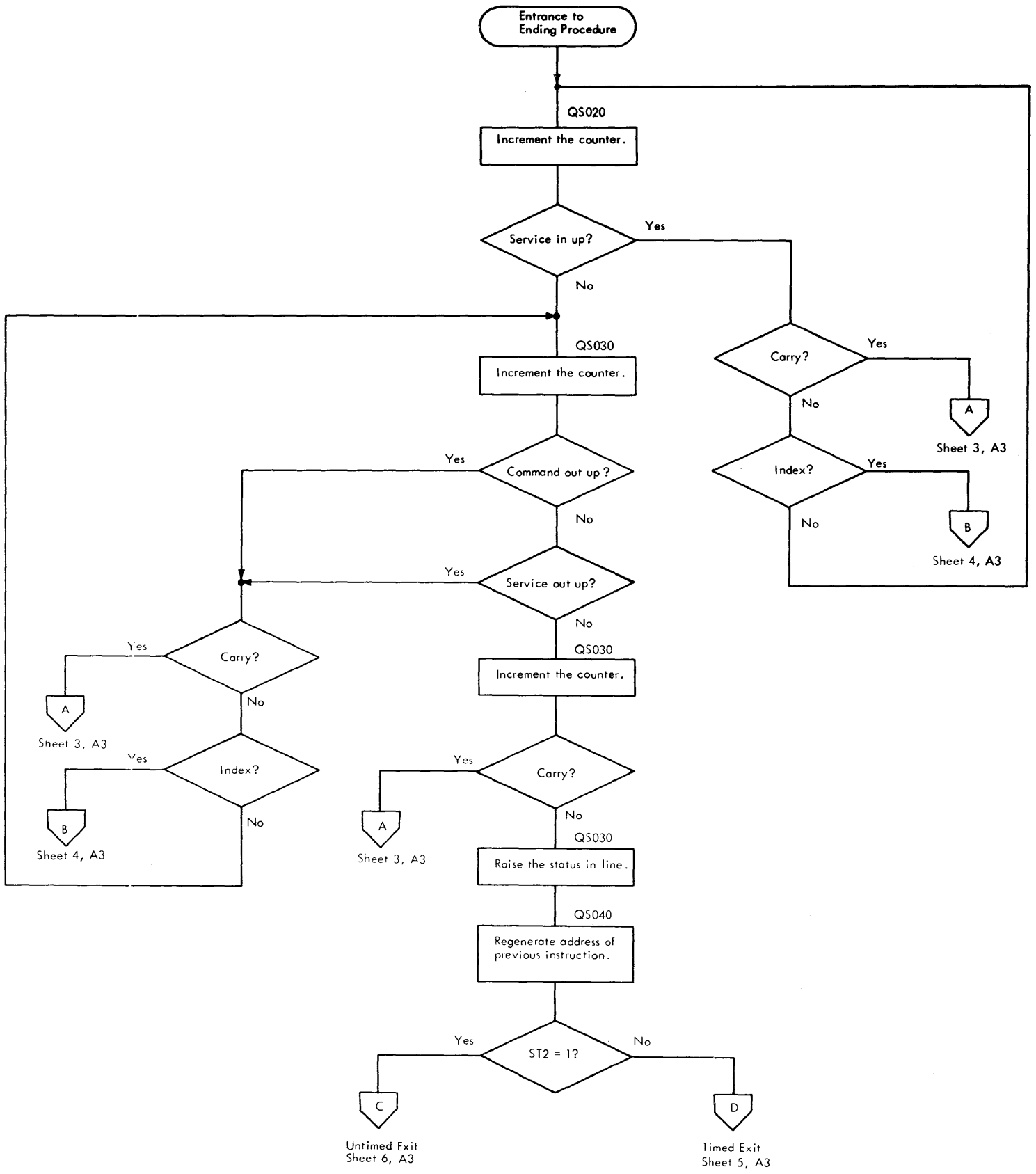
▶

G

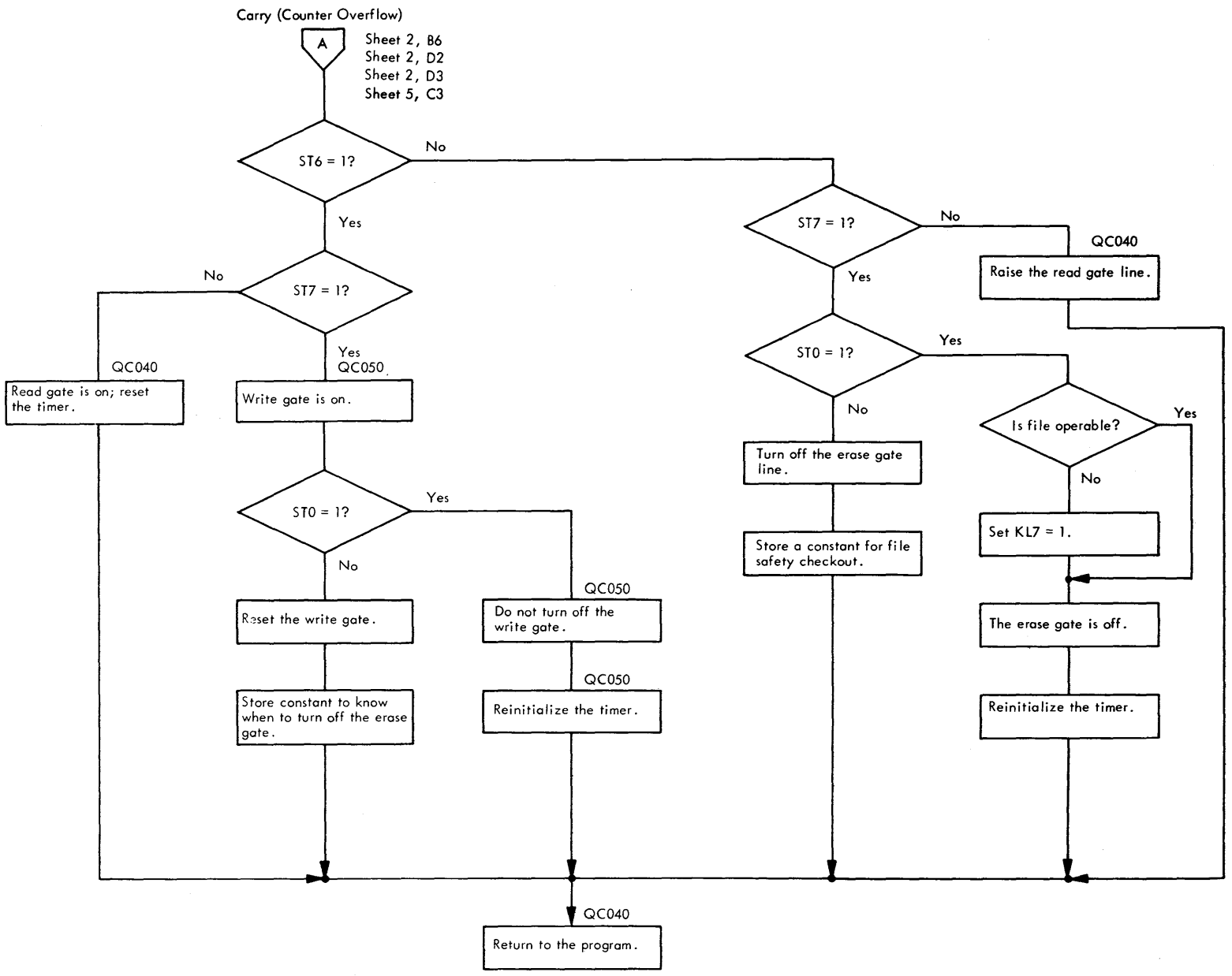
▶

H

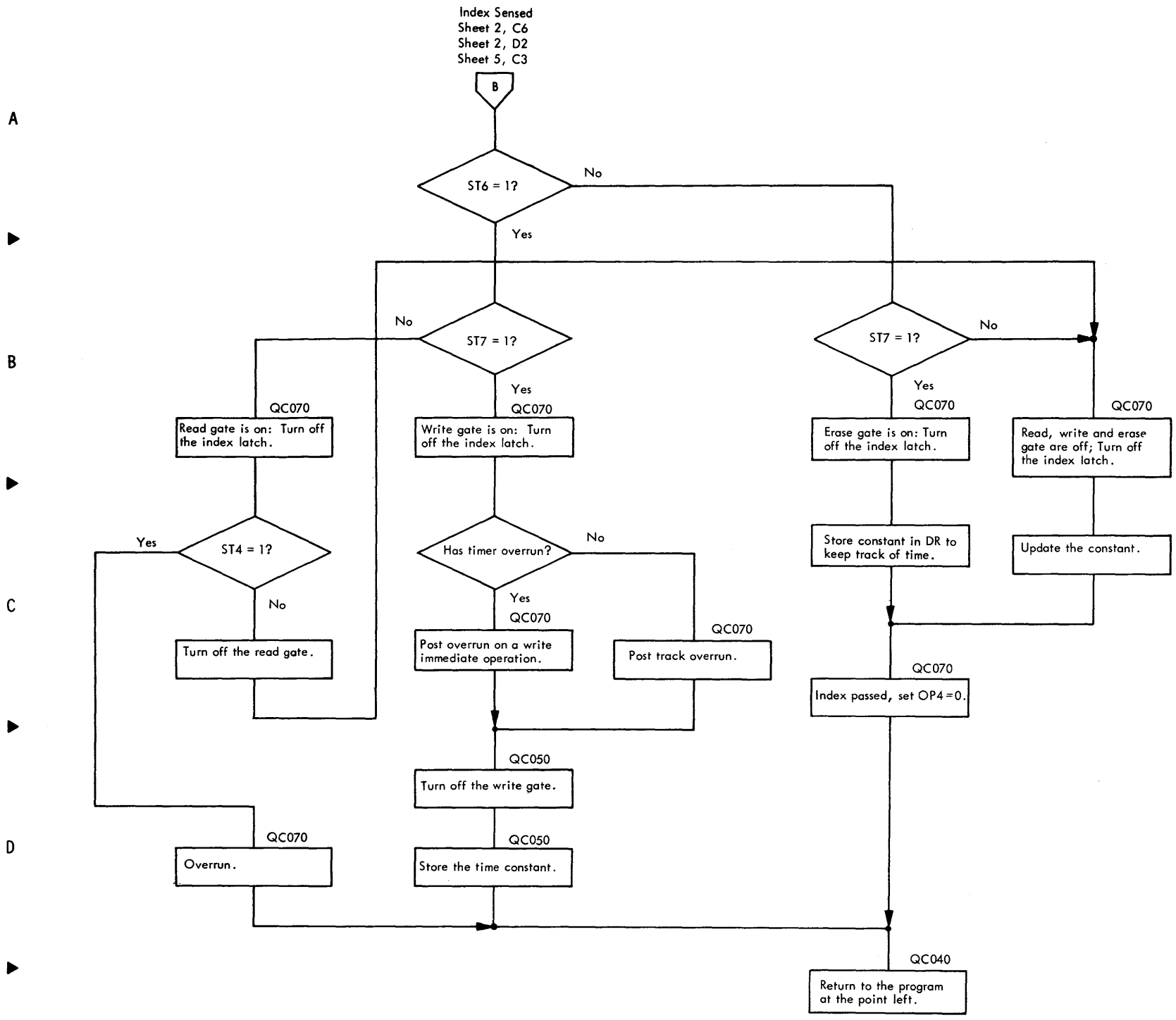
FLOW CHART - End Procedure - Part 1



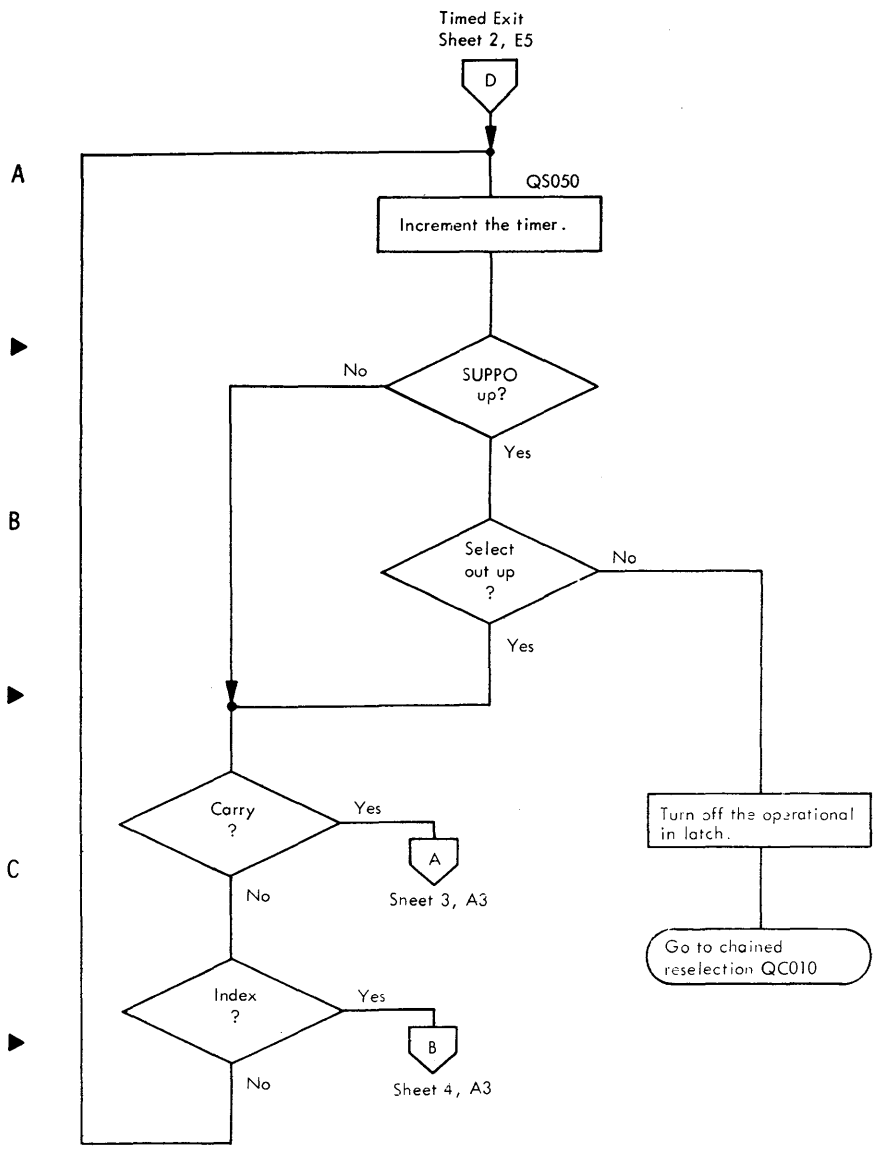
FLOW CHART - End Procedure - Part 2

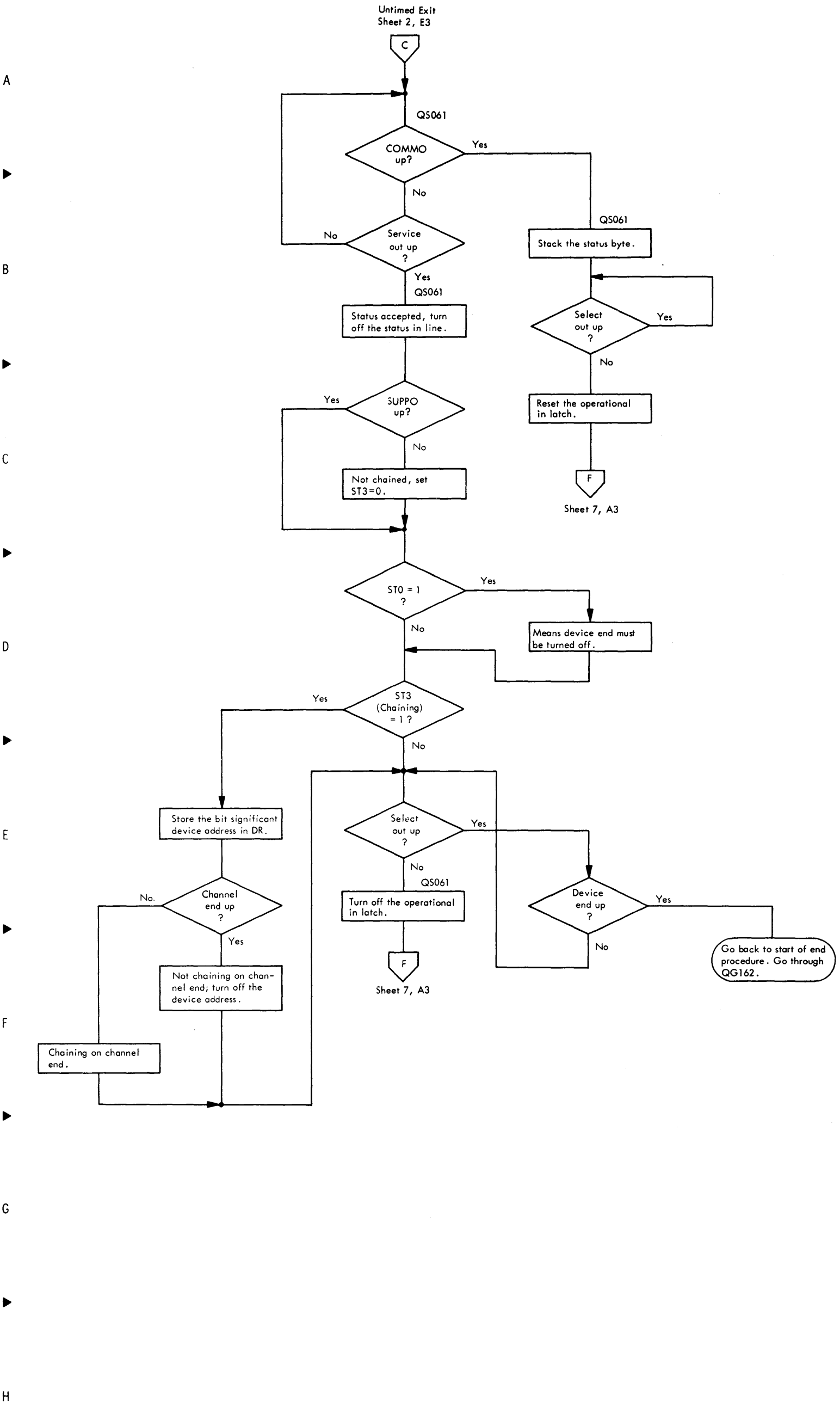


FLOW CHART - End Procedure - Part 3

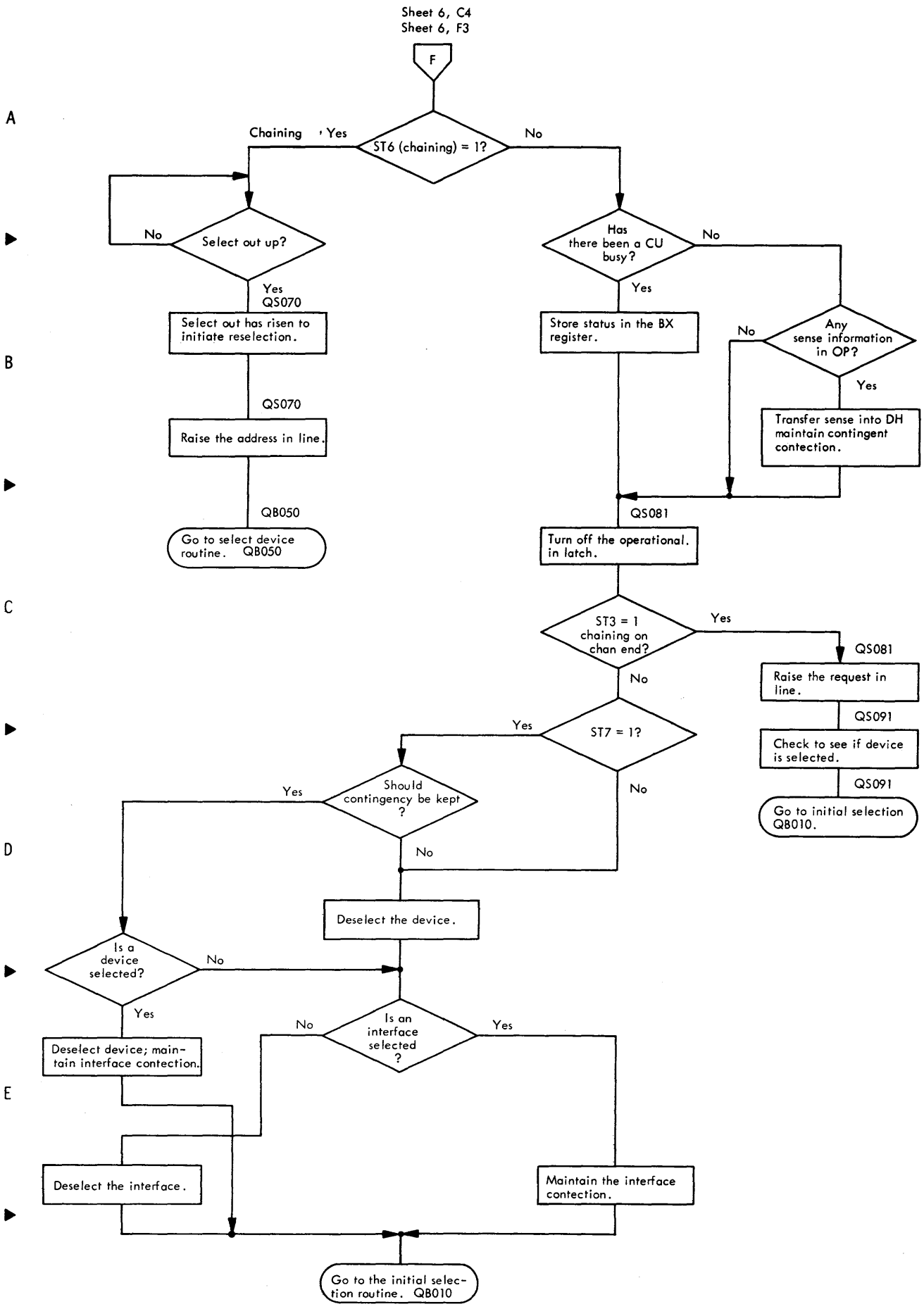


FLOW CHART - End Procedure - Part 4

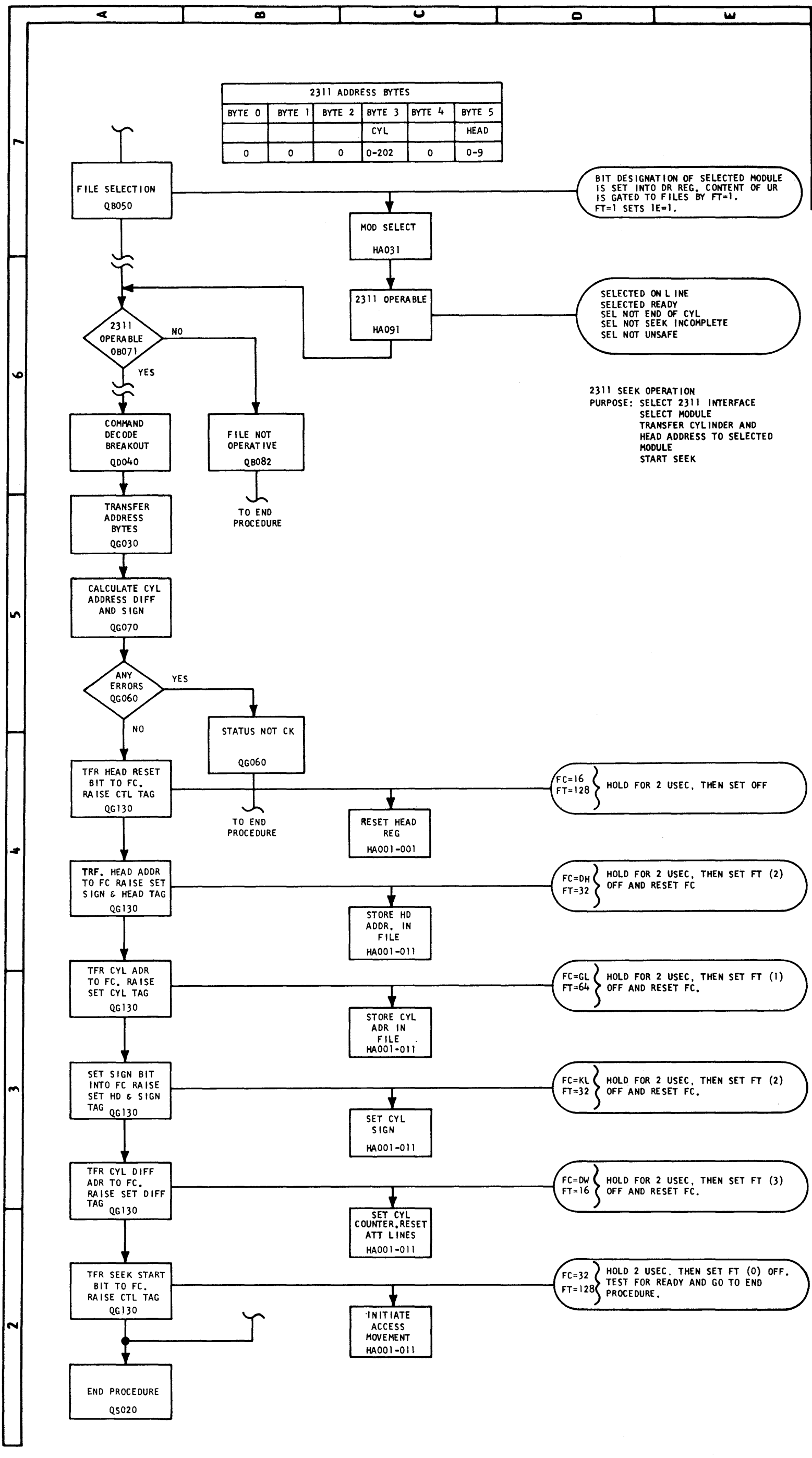

Timed Exit
Sheet 2, E5
D
QS050
Increment the timer.
SUPPO up?
No
Yes
Select out up ?
No
Yes
Carry ?
Yes
A
Sheet 3, A3
No
Index ?
Yes
B
Sheet 4, A3
No
Turn off the operational in latch.
Go to chained reselection QC010



FLOW CHART - End Procedure - Part 6


Sheet 6, C4
Sheet 6, F3
F
ST6 (chaining) = 1?
Chaining
Yes
No
Select out up?
No
Yes
QS070
Select out has risen to initiate reselection.
QS070
Raise the address in line.
QB050
Go to select device routine. QB050
Has there been a CU busy?
No
Yes
Store status in the BX register.
Any sense information in OP?
No
Yes
Transfer sense into DH maintain contingent contection.
QS081
Turn off the operational. in latch.
ST3 = 1 chaining on chan end?
Yes
No
QS081
Raise the request in line.
QS091
Check to see if device is selected.
QS091
Go to initial selection QB010.
ST7 = 1?
Yes
No
Should contingency be kept ?
Yes
No
Deselect the device.
Is a device selected?
No
Yes
Deselect device; maintain interface contection.
Is an interface selected ?
No
Yes
Deselect the interface.
Maintain the interface contection.
Go to the initial selection routine. QB010

2311 ADDRESS BYTES					
BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5
			CYL		HEAD
0	0	0	0-202	0	0-9



FLOW CHART - 2311 Seek

2321 SEEK (BBCCHH)

FLOW CHART 2321 SEEK — DATE — TYPE 2841R — 1613 — IBM

SELECT 2321 INTERFACE QB040

FT(6) SELECTS 2321 INTERFACE

FILE SELECTION QB050

MODULE SELECT HB071

BIT DESIGNATION OF SELECTED FILE IS SET INTO UR, AFTER WHICH, FILE BECOMES SELECTED

2321 OPERABLE QB050

FILE NOT OPERATIVE QB050

END PROCEDURE

2321 OPERABLE HB091

SELECTED ON LINE
SELECTED DRIVE READY
DRIVE OPERATIVE
SEL NOT UNSAFE

COMMAND DECODE BREAKOUT QE060

PRESENT STATUS QE010

SET SEEK LIMIT QG020

TFR ADDR BYTES FROM CHAN. CHECK SEEK LIMITS DURING TRANSFER QG030, 040, 050

DL = HEAD ADDRESS
DH = HEAD POSITION
GL = FINGER ADDRESS
KL = SUBCELL
DW = CELL

TEMPORARY LOCATION OF ADDRESSES APPEAR IN ABOVE REGISTERS ENTERING QG110

CONVERT FINGER AND HD POS ADDR. QG110

HEAD POS & FINGER ADDR "WEIGHTED" PER CHART ON CLD PAGE QA007

TFR HD ADDR TO FC, RAISE "SET HD ADDR" QG130, 131, 140

FT = 32. HOLD FOR 3 USEC THEN SET FT (2) OFF

HD ADDR SET HB061

TFR HD POS TO FC, RAISE "SET HD POS" QG130, 131, 140

FT = 8. HOLD FOR 3 USEC, THEN SET FT (4) OFF

HD POS SET HB051 FA023

TFR FNGR ADDR TO FC, RAISE "SET FNGR ADDR" QG130, 131, 140

FT =16. HOLD FOR 3 USEC, THEN SET FT (3) OFF

FNGR ADDR SET HB051 FA023

TFR SUBCELL ADDR TO FC, RAISE "SET SUBCELL ADDR" QG130, 131, 140

FT = 4. HOLD FOR 3 USEC, THEN SET FT (5) OFF

SUBCELL ADDR SET HB051 FA023

TFR CELL ADDR TO FC, RAISE "SET CELL ADDR" QG130, 131, 140

FT = 64. HOLD FOR 3 USEC

CELL ADDR SET HB052 FA023

TFR "SEEK START" TO FC, RAISE CONTROL TAG QG130

FC=32, FT=128 — HOLD FOR 3 USEC THEN SET FT(0) OFF, TEST FOR READY, GO TO END PROC.

SEEK START HB061 FA021

END PROCEDURE QS020

2321 ADDRESS BYTES					
BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5
BIN	BIN	CYL	CYL	HEAD	HEAD
0	0-9	0-19	0-9	0-4	0-19
NOT USED	CELL	SUBCELL	FINGER	HD POS	HD ELEMENT

CELL	00	01	02	03	04	05	06	07	08	09
SUBCELL	0-19	0-19	0-19	0-19	0-19	0-19	0-19	0-19	0-19	0-19

RECEIVED FROM CHANNEL IN THIS ADDRESS FORMAT

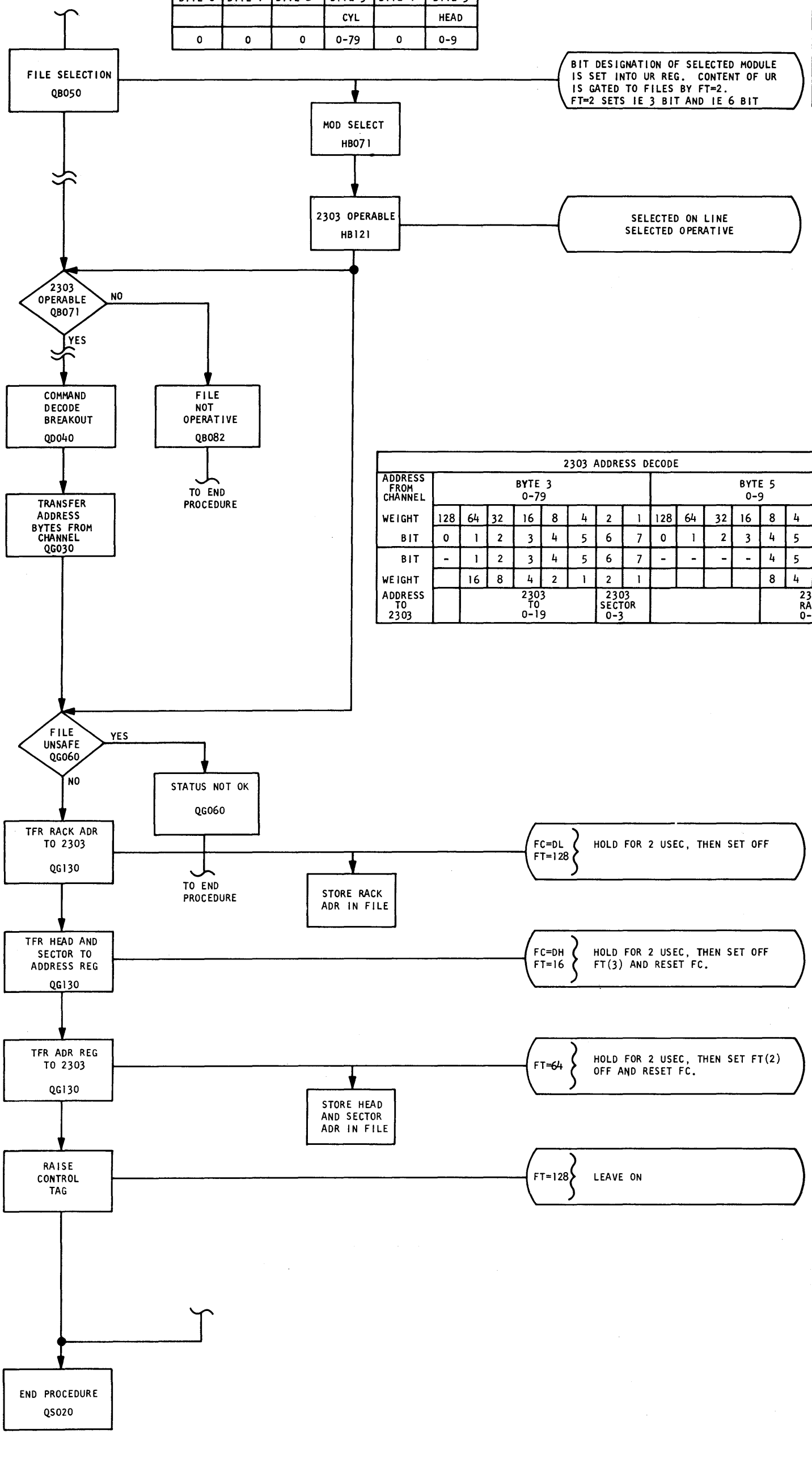
CELL	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19
SUBCELL	0-9	0-9	0-9	0-9	0-9	0-9	0-9	0-9	0-9	0-9	0-9	0-9	0-9	0-9	0-9	0-9	0-9	0-9	0-9	0-9

CONVERTED TO THIS ADDRESS FORMAT

NOTE:
ADDRESSES ON THIS CHART ARE EXPRESSED IN DECIMAL ALTHOUGH THEY ARE ACTUALLY RECEIVED FROM CHANNEL IN "HEX" FORM

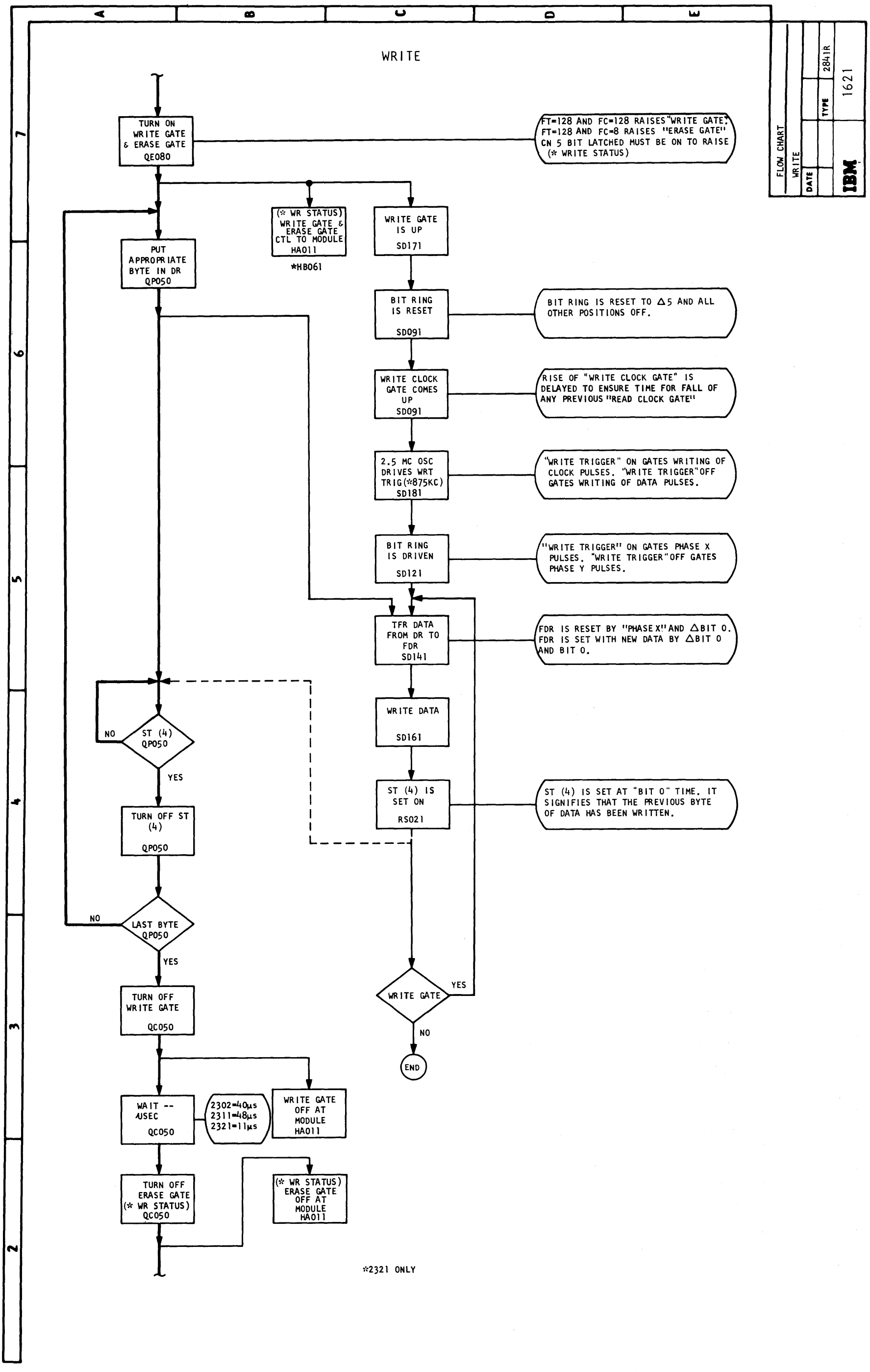
FLOW CHART - 2321 Seek

2303 ADDRESS BYTES					
BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5
			CYL		HEAD
0	0	0	0-79	0	0-9



2303 ADDRESS DECODE																
ADDRESS FROM CHANNEL	BYTE 3 0-79								BYTE 5 0-9							
WEIGHT	128	64	32	16	8	4	2	1	128	64	32	16	8	4	2	1
BIT	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
BIT	-	1	2	3	4	5	6	7	-	-	-	-	4	5	6	7
WEIGHT		16	8	4	2	1	2	1					8	4	2	1
ADDRESS TO 2303		2303 TO 0-19					2303 SECTOR 0-3						2303 RACK 0-9			

FLOW CHART - 2303 Seek



FLOW CHART - Write

2303 WRITE

FLOW CHART
2303 WRITE
DATE
TYPE 2841 R
IBM 1622

TURN ON WRITE GATE & ERASE GATE QE080

FT=128 AND FC=128 RAISES "WRITE GATE".
FT=128 AND FC=8 RAISES "ERASE GATE".
CN 5 BIT LATCHED MUST BE ON TO RAISE.

PUT APPROPRIATE BYTE IN DR

WRITE GATE & ERASE GATE CTL TO MODULE HA011
* HB061

WRITE GATE IS UP
HB091

WRITE START COMES ON TO TFR 1ST BYTE FR DR TO FDR SD201

THIS IS DONE TO INSURE THAT THE FIRST BYTE WRITTEN CONTAINS ALL ONES

BIT RING IS RESET SD091

BIT RING IS RESET TO Δ 1 AND ALL OTHER POSITIONS OFF.

WRITE CLOCK GATE COMES UP SD091

RISE OF WRITE CLOCK GATE IS DELAYED TO ENSURE TIME FOR FALL OF ANY PREVIOUS READ CLOCK GATE.

PHASE Ø DRIVES BIT RING HC161

TFR DATA FROM DR TO FDR HC171

FDR IS RESET BY PHASE 1 AND BIT 0
FDR IS SET WITH NEW DATA BY BIT 0 AND PHASE-2

WRITE DATA HC061

ST (4) IS SET ON RS021

ST (4) IS SET AT DELTA BIT 7 TIME. IT SIGNIFIES THAT THE PREVIOUS BYTE OF DATA HAS BEEN WRITTEN.

NO
ST (4) QP330
YES

TURN OFF ST (4) QP330

ST (4) IS SET OFF RS021

NO
LAST BYTE QP050
YES

TURN OFF WRITE GATE QC050

WRITE GATE
YES
NO

END

HARDWARE

WAIT 8 μSEC QS050

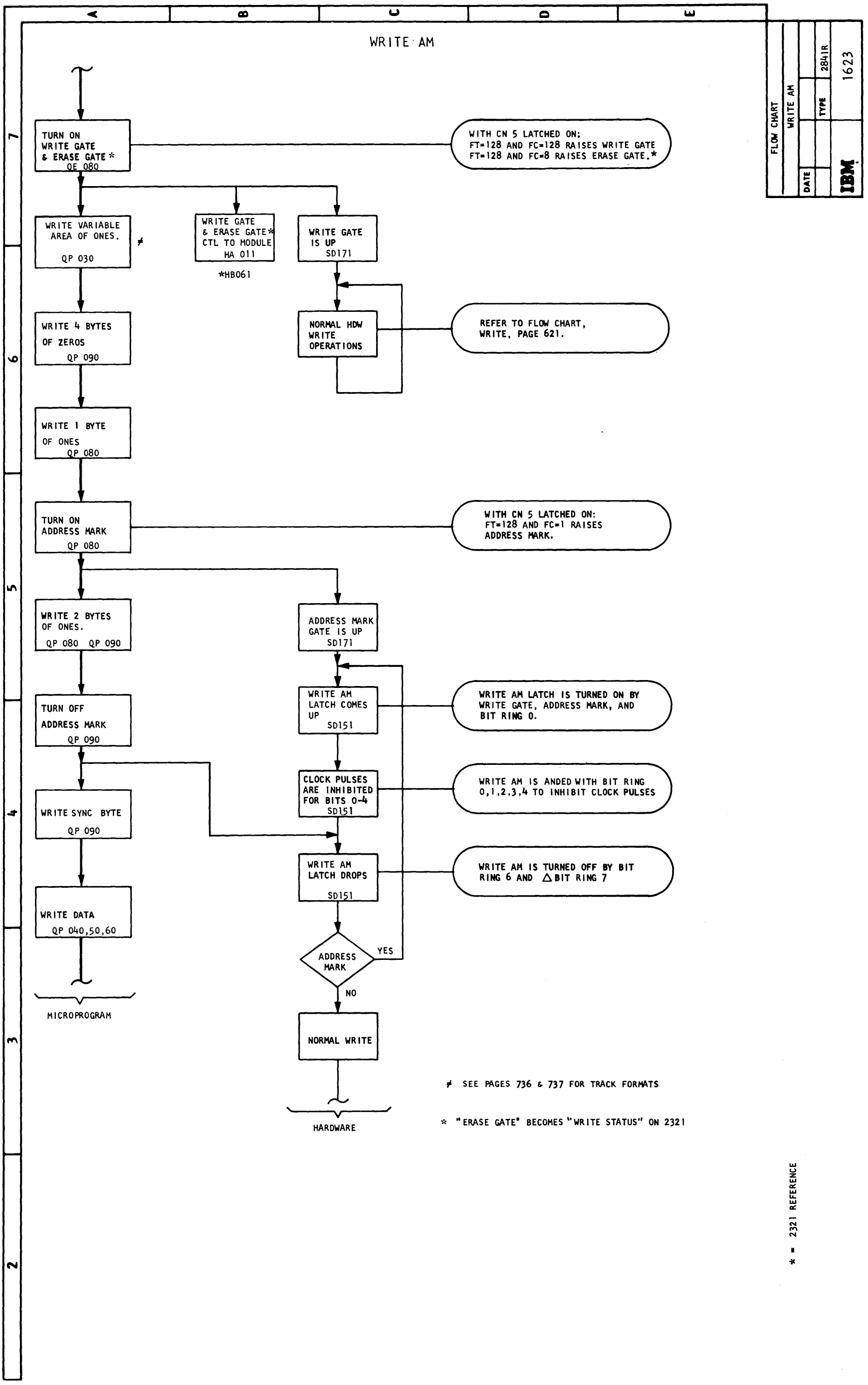
WRITE GATE OFF AT MODULE HB061

TURN OFF ERASE GATE (* WR STATUS) QC050

(* WR STATUS) ERASE GATE OFF AT MODULE HB061

MICROPROGRAM

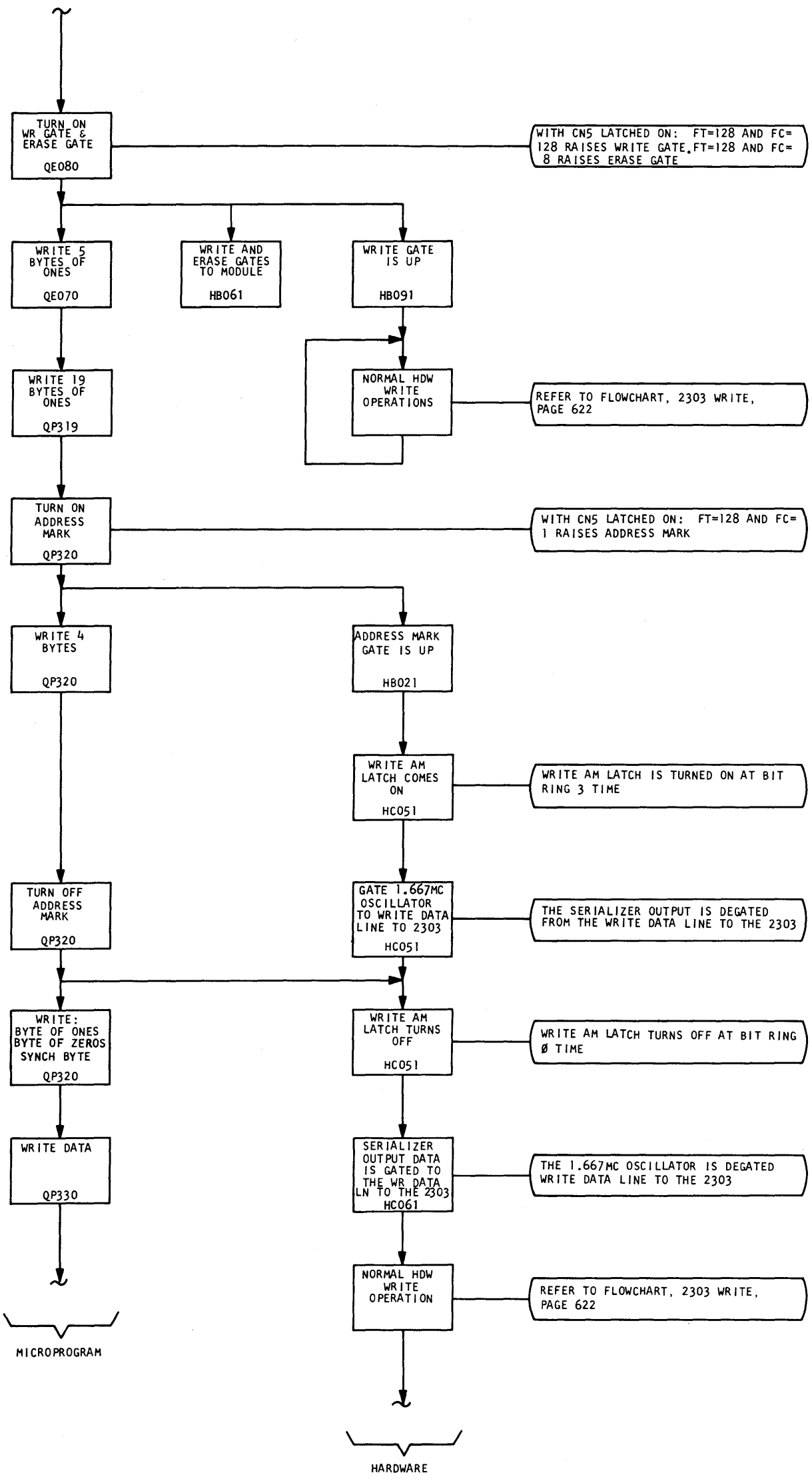
FLOW CHART - 2303 Write



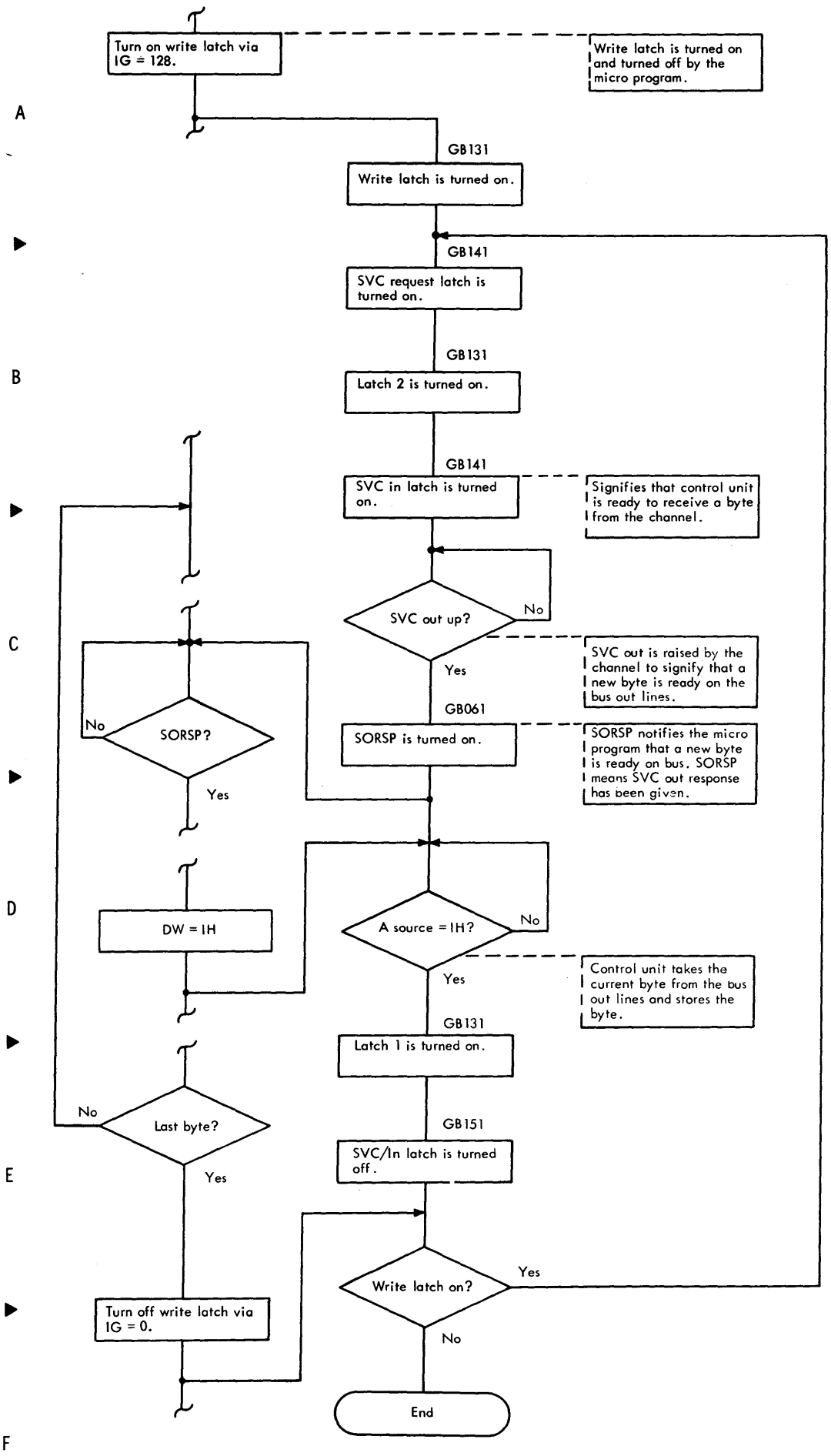
FLOW CHART - Write Address Mark

2303 WRITE AM

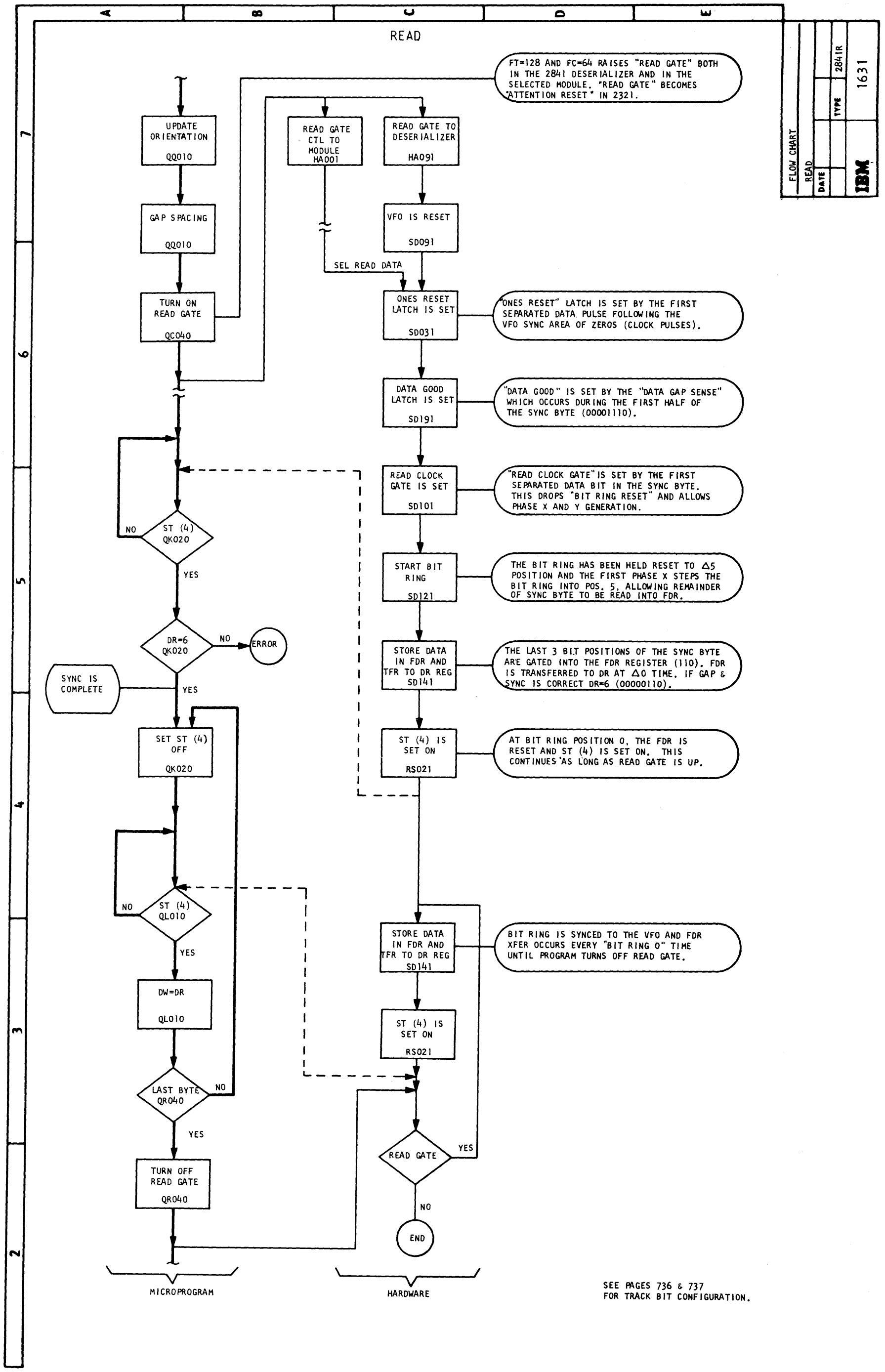
FLOW CHART
2303 WRITE AM
DATE
TYPE
1624
IBM



FLOW CHART - 2303 Write Address Mark

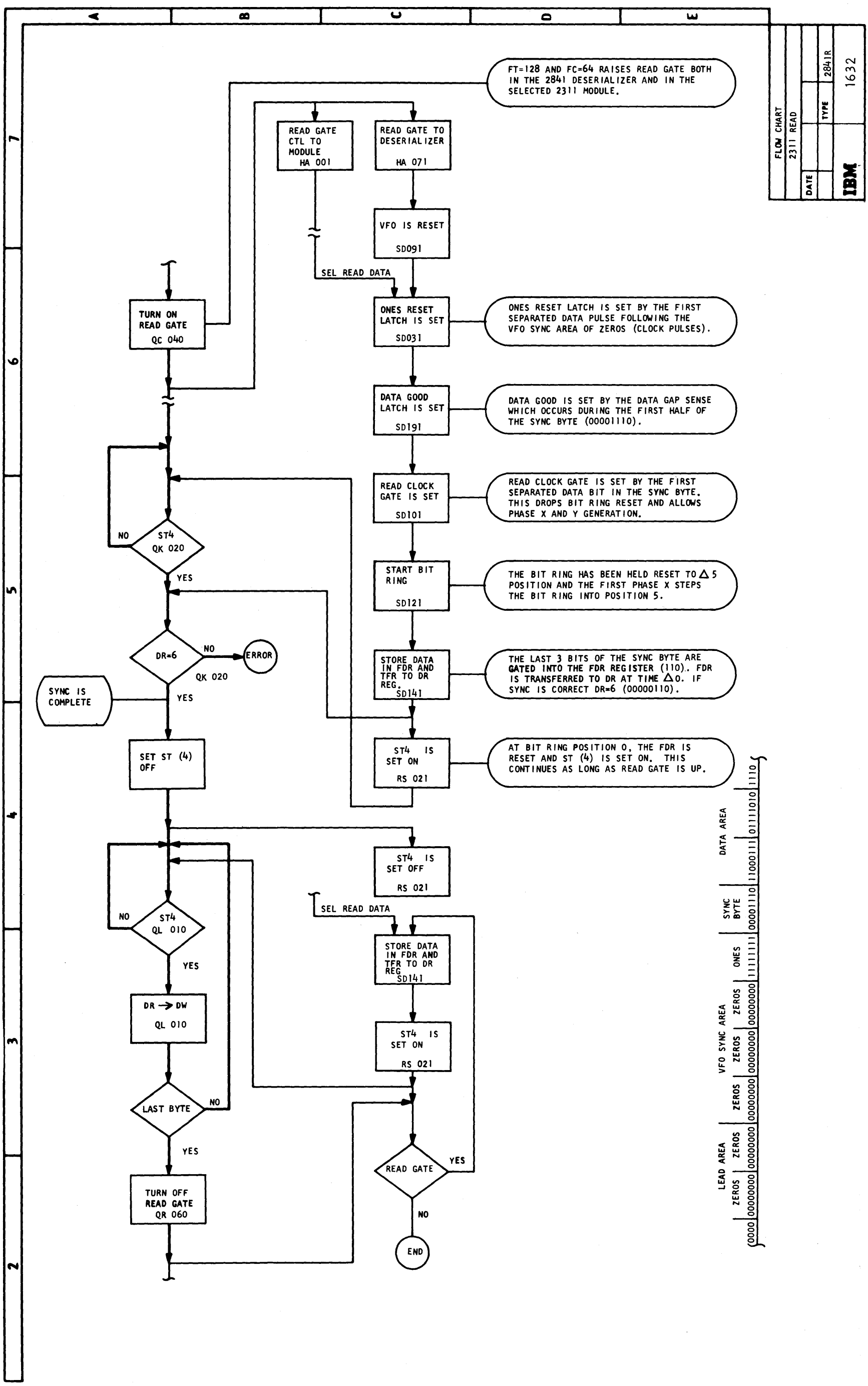


FLOW CHART - Channel Data Transfer - Write

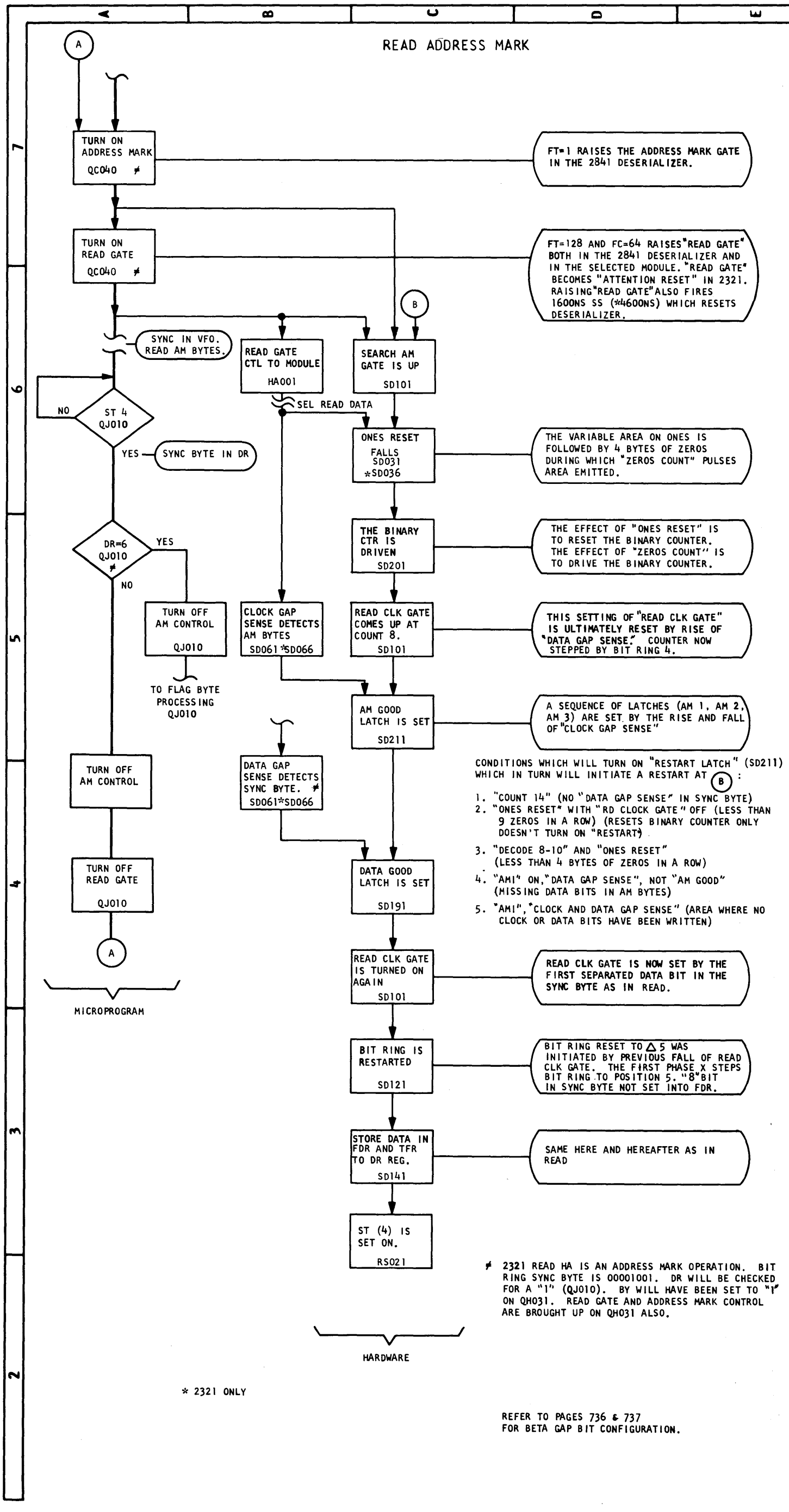


SEE PAGES 736 & 737
FOR TRACK BIT CONFIGURATION.

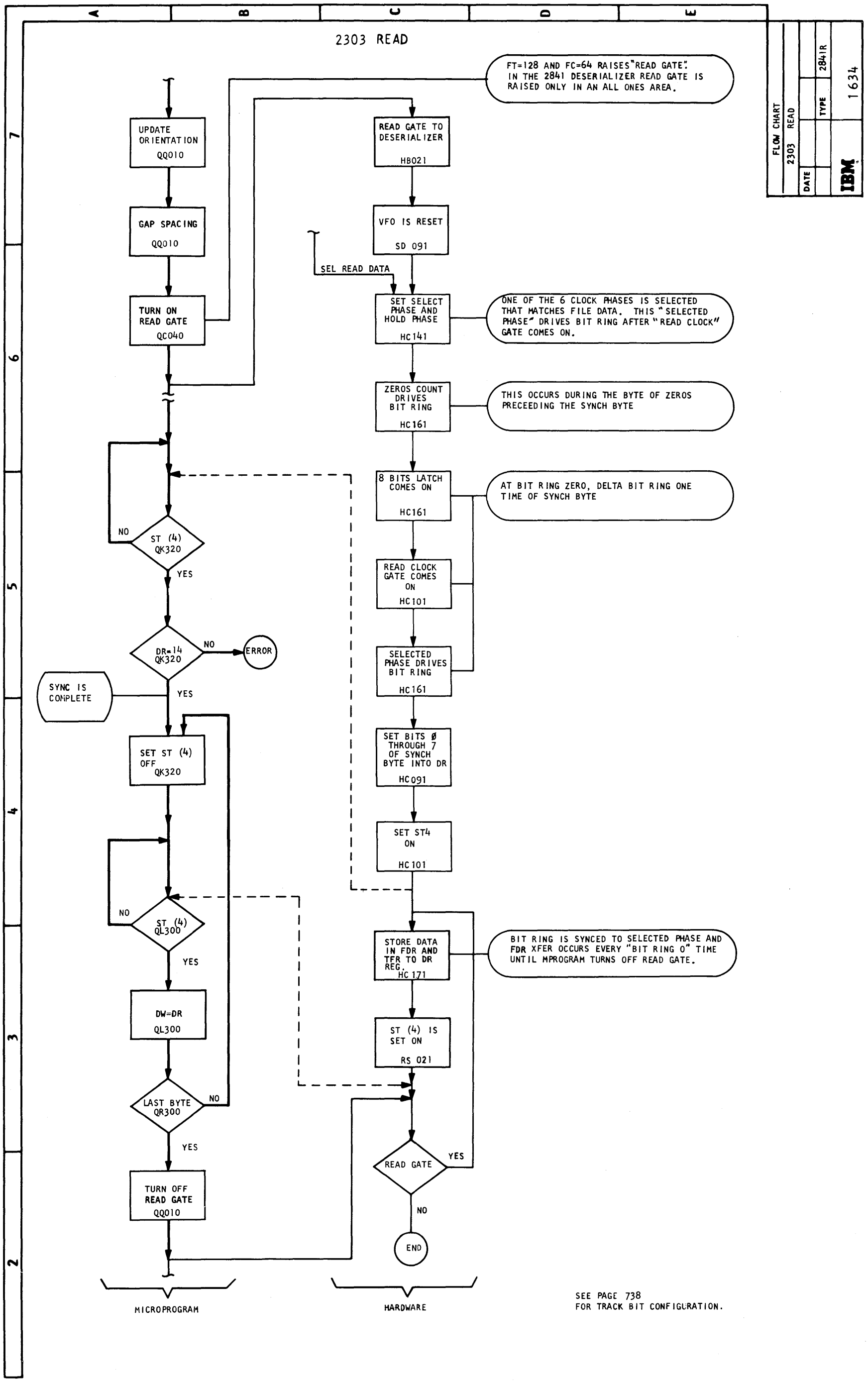
FLOW CHART - Read



FLOW CHART - 2311 Read

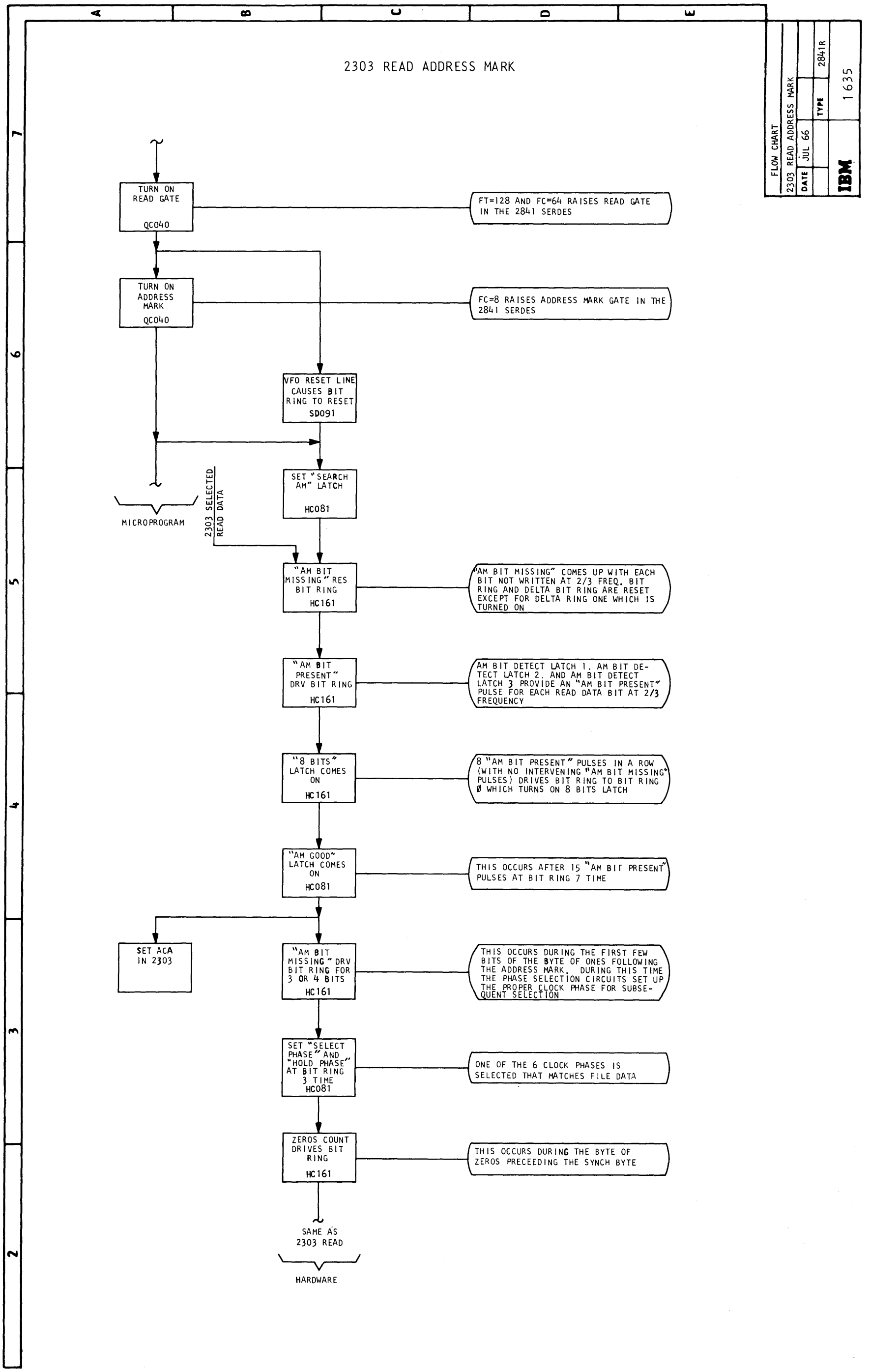


FLOW CHART - Read Address Mark

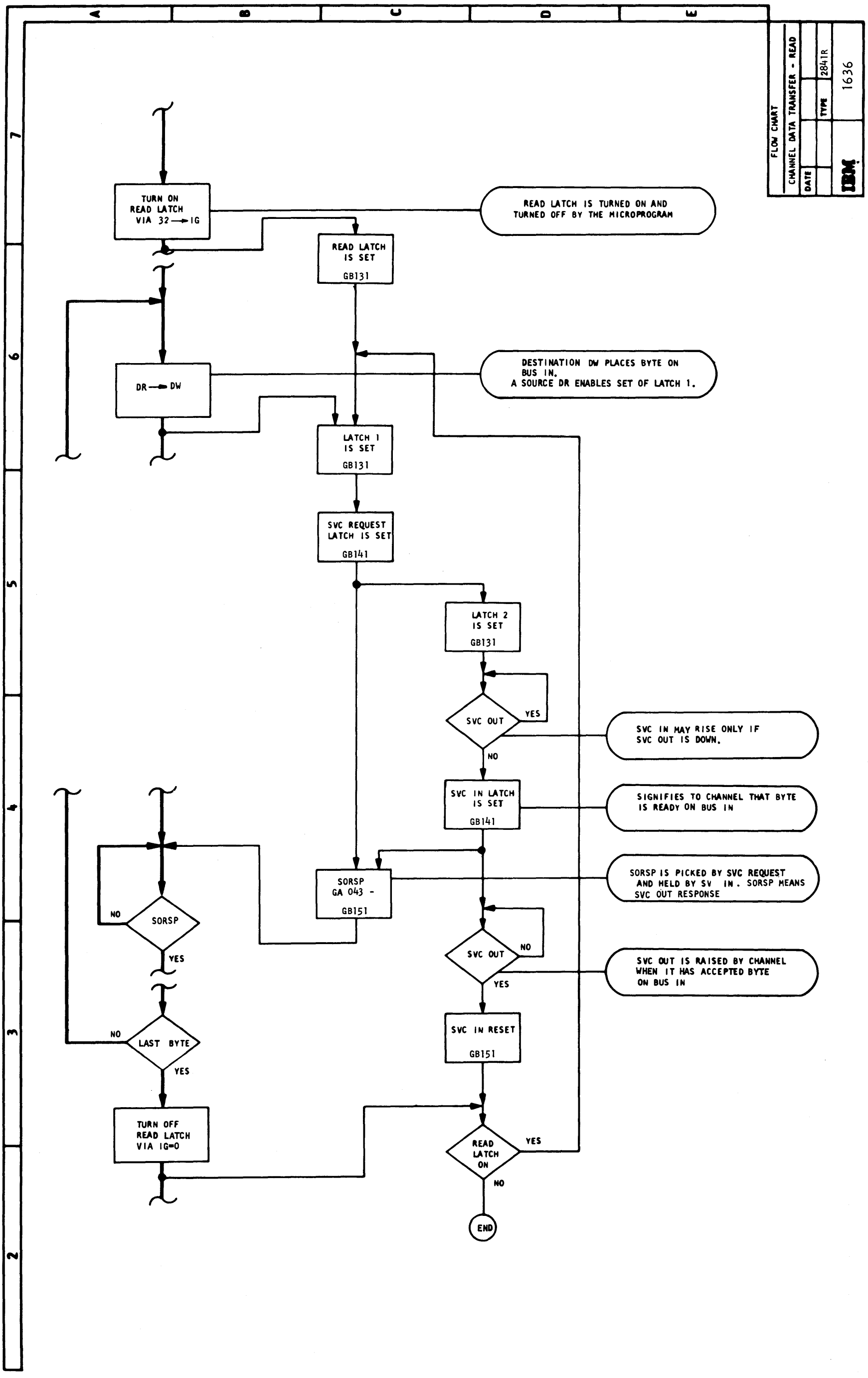


SEE PAGE 738
FOR TRACK BIT CONFIGURATION.

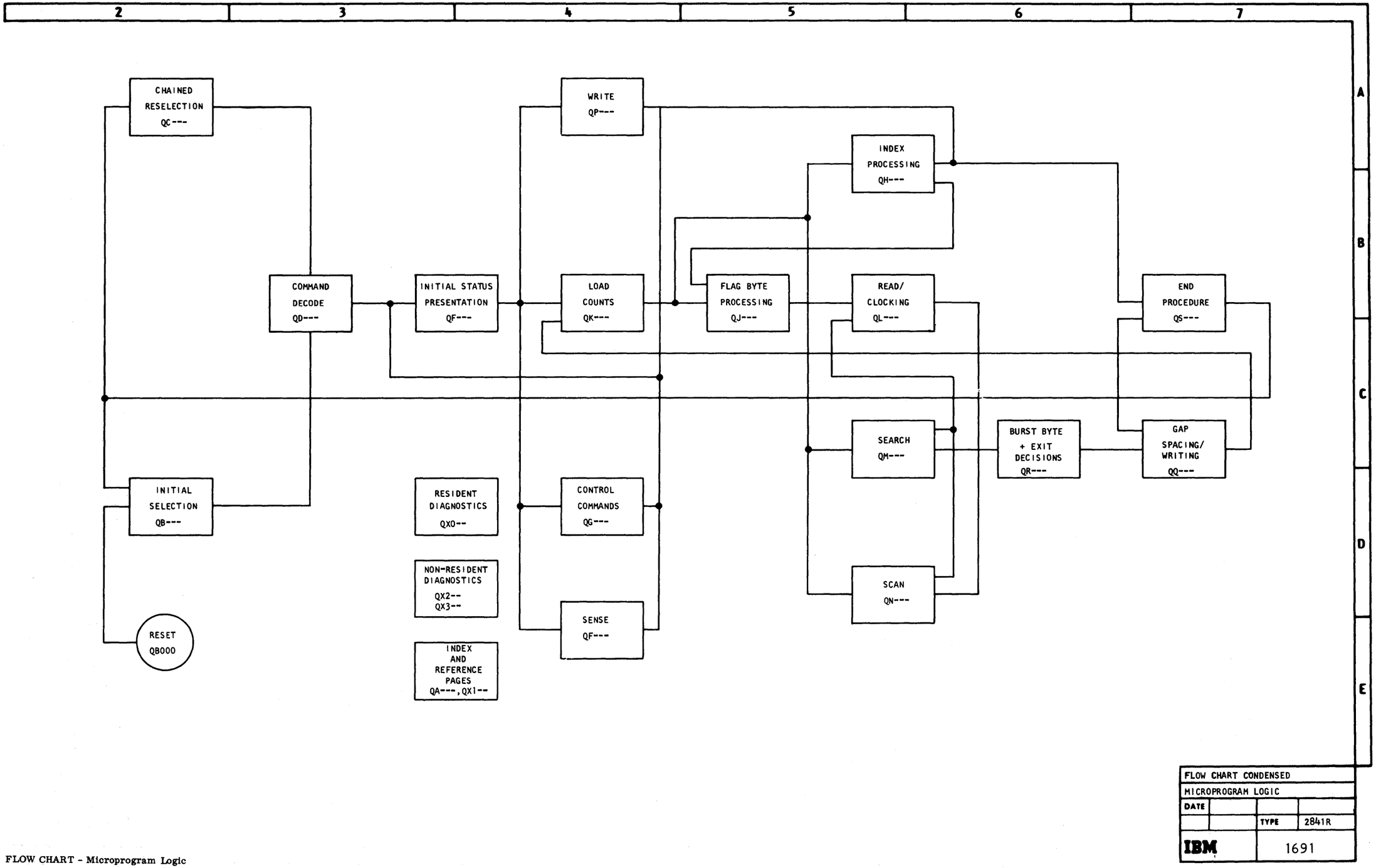
FLOW CHART - 2303 Read



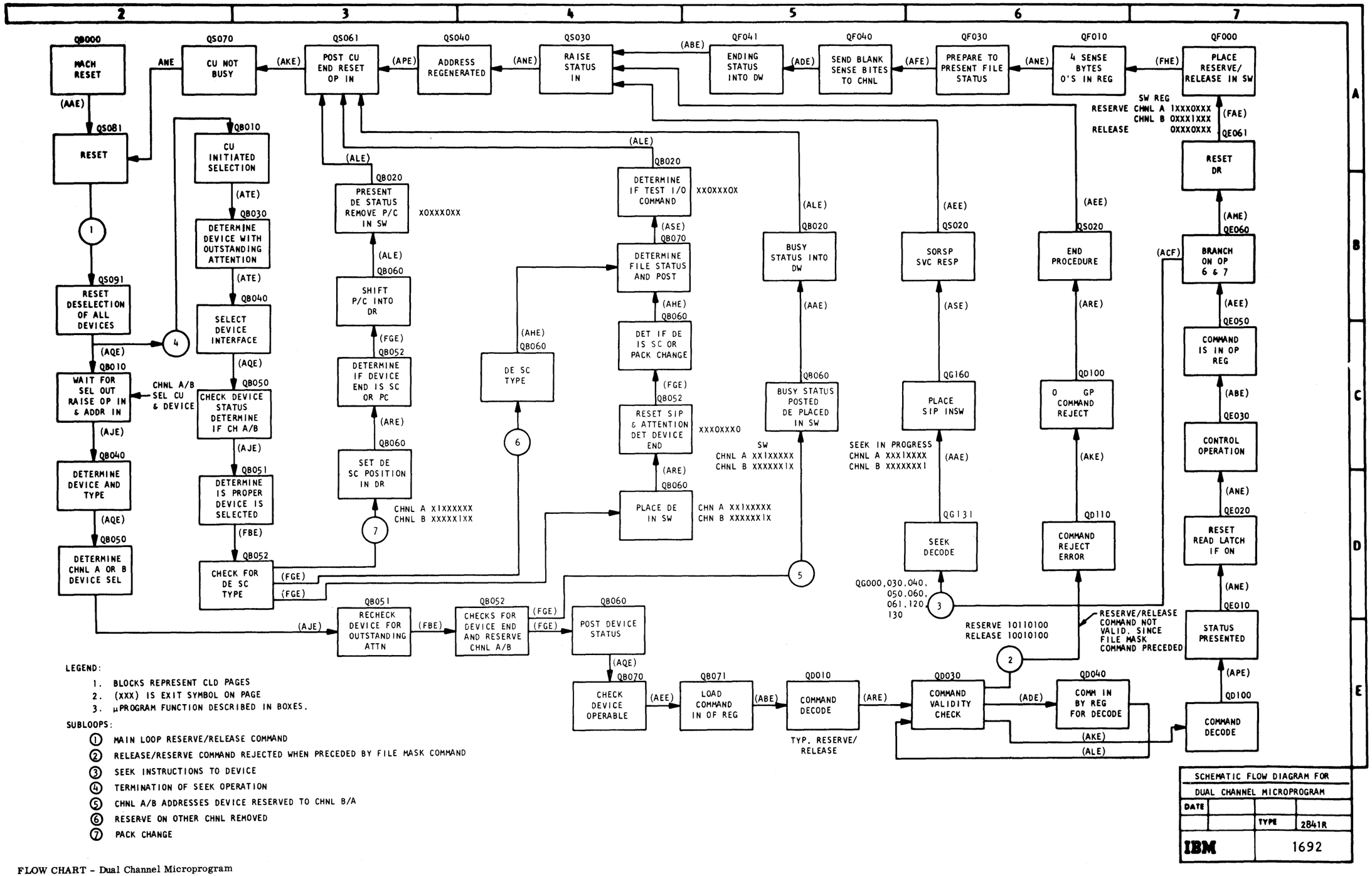
FLOW CHART - 2303 Read Address Mark



FLOW CHART - Channel Data Transfer - Read



FLOW CHART - Microprogram Logic



LEGEND:

1. BLOCKS REPRESENT CLD PAGES
2. (XXX) IS EXIT SYMBOL ON PAGE
3. μPROGRAM FUNCTION DESCRIBED IN BOXES.

SUBLOOPS:

① MAIN LOOP RESERVE/RELEASE COMMAND
② RELEASE/RESERVE COMMAND REJECTED WHEN PRECEDED BY FILE MASK COMMAND
③ SEEK INSTRUCTIONS TO DEVICE
④ TERMINATION OF SEEK OPERATION
⑤ CHNL A/B ADDRESSES DEVICE RESERVED TO CHNL B/A
⑥ RESERVE ON OTHER CHNL REMOVED
⑦ PACK CHANGE

SCHEMATIC FLOW DIAGRAM FOR DUAL CHANNEL MICROPROGRAM			
DATE			
		TYPE	2841R
IBM		1692	

FLOW CHART - Dual Channel Microprogram

2 | 3 | 4 | 5 | 6 | 7

NO.	SIGNAL NAME	SP	LOGIC	LEVEL
1	MACHINE CYCLES A B C D			+3,0
2	RESET { SELECTIVE GENERAL MANUAL			
3	RESET 1	C1L4 D04	KG001	+3,0
4	W REG RESET	C1E4 D04	KG001	0,+3
5	REG RESET 1	C1D6 D07	KG001	+3,0
6	REG RESET 2	C1D6 B08	KG001	+3,0
7	RESET 2	C1D4 D07	KG001	+3,0
8	INHIBIT 1	C1B5 D12	SP101	+3,0
9	INHIBIT 2	C1B5 B10	SP101	+3,0
10	INHIBIT 3	C1F3 B07	SP101	+3,0
11				
12				
13				
14				
15				
16				
17				
18				
19				
20				

TIME SCALE OR CYCLE

A B C D 500 NANOSEC MACHINE CYCLES (125 NANOSEC PER PHASE A, B, C, D)

OCCURS AT RANDOM TIME

A | B | C | D | E

NORMAL & CE MODE

CE MODE ONLY

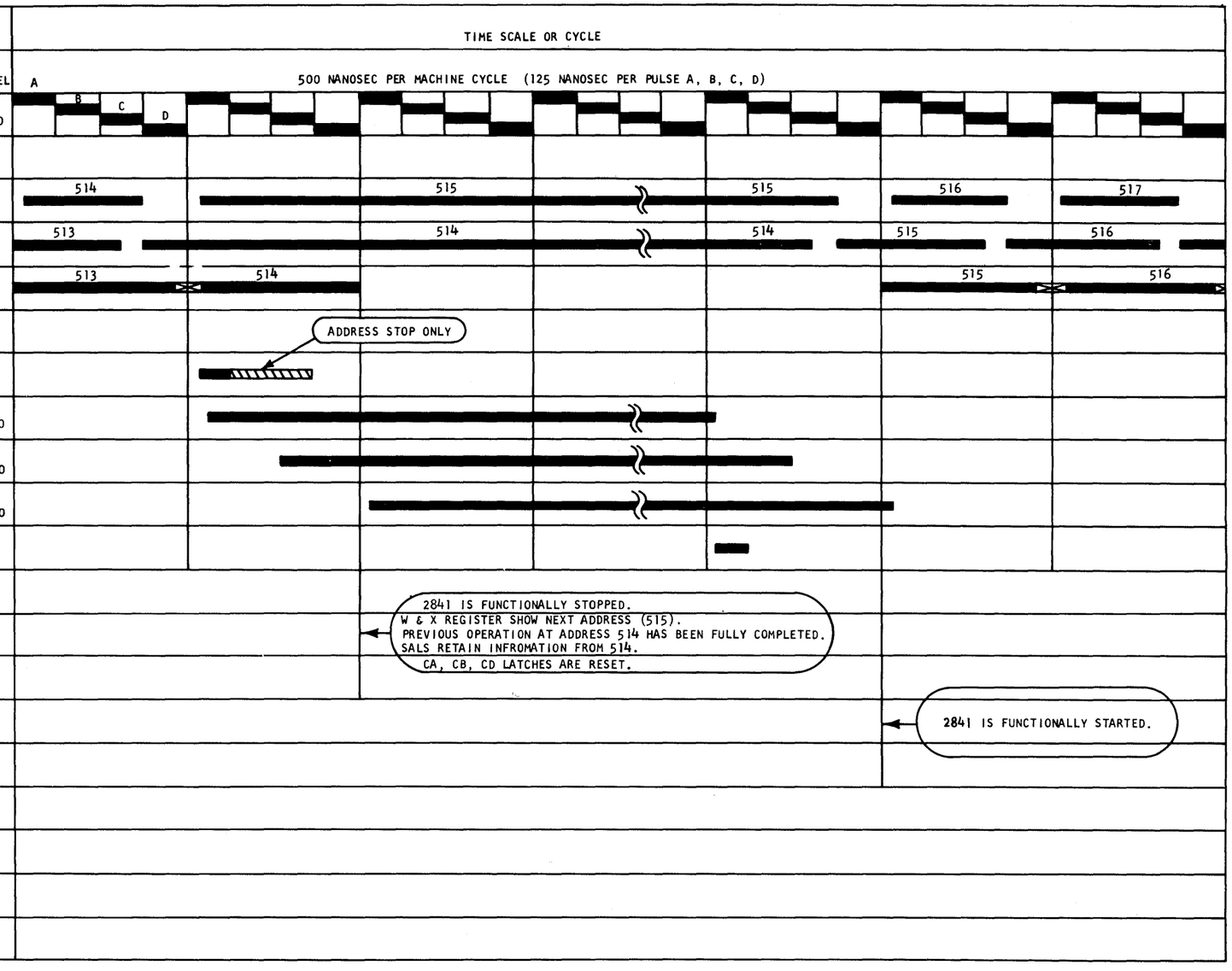
RANDOM TIME

TIMING CHART			
RESET			
DATE			
		TYPE	2841R
IBM		1701	

1701

TIMING CHART - Reset

NO.	SIGNAL NAME	SP	LOGIC	LEVEL
1	MACHINE CYCLES A B C D			+3,0
2				
3	ADDRESS REGISTER (SAMPLE ADDRESS SHOWN)			
4	SALS OUTPUT (ADDRESSED LOCATION)			
5	ALU OPERATION			
6				
7	TIMED STOP (STOP KEY, ERROR, ETC)		SP101	
8	INHIBIT 1 ①	C1B5 D12	SP101	+3,0
9	INHIBIT 2 ②	C1B5 B10	SP101	+3,0
10	INHIBIT 3 ③	C1F3 B07	SP101	+3,0
11	TIMED START (START KEY, NORMAL RESET)		SP101	
12				
13				
14				
15				
16				
17				
18				
19				
20				



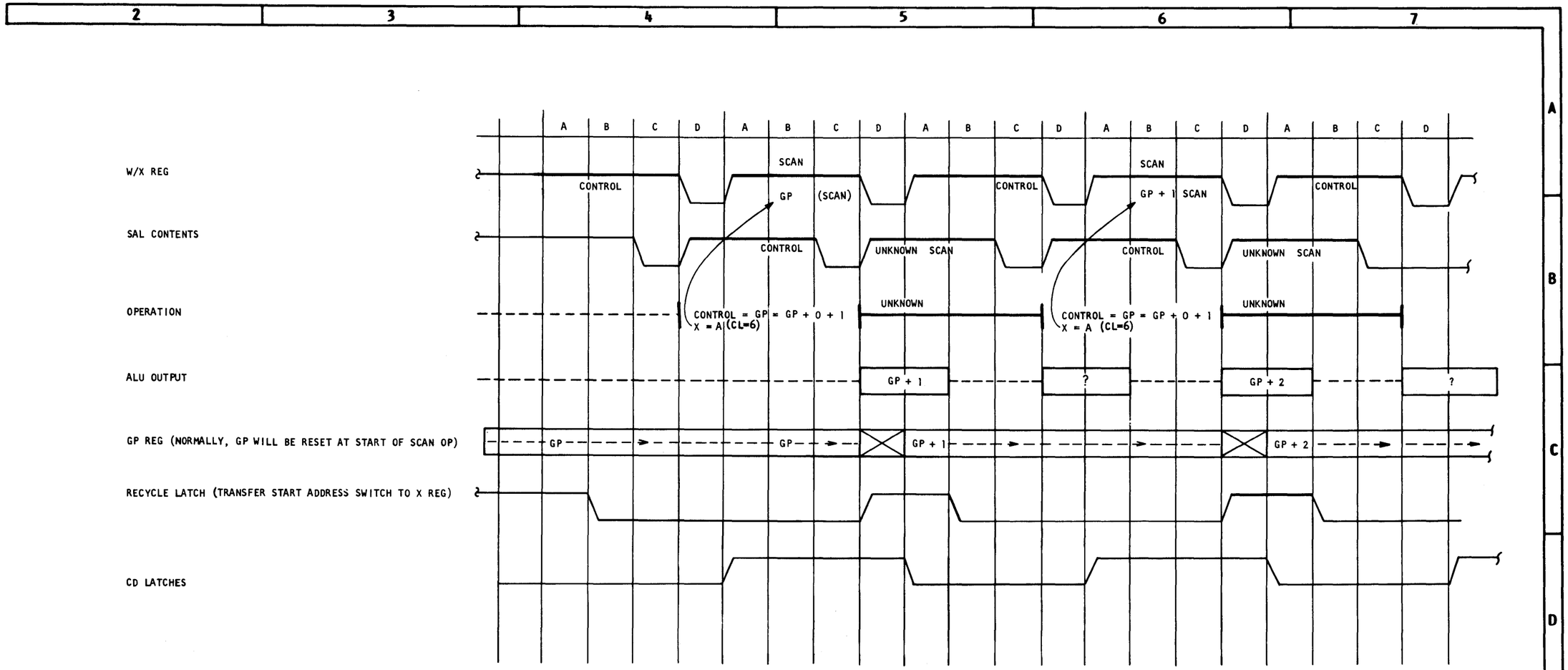
NOTES:

① BLOCK SALS RESET & SET, TURN ON MACHINE STOP INDICATOR.
② BLOCK CA, CB, CD LATCH SET; BLOCK W & X REGISTER SET.
③ BLOCK ALU OUTPUT.

TIMING CHART			
START - STOP TIMING			
DATE			
		TYPE	2841R
IBM		1702	

1702

TIMING CHART - Start - Stop Timing



TROS SCAN

700

[GP = GP + 0 + 1
X = A]

XXXXX

TYPICAL SCAN CONTROL WORD

TIMING CHART			
T.R.O.S. SCAN			
DATE			
		TYPE	2841R
IBM		1703	

1703

TIMING CHART - T.R.O.S. Scan

NO.	SIGNAL NAME	SP	LOGIC	LEVEL	TIME SCALE OR CYCLE: 500 NANOSEC MACHINE CYCLES (125 NANOSEC PER PHASE A,B,C,D)
1	MACHINE CYCLES A B C D			+3-0	
2	SALS OUTPUTS		DE001 DE011		
3	CA & CB DECODES		DA001 DB001		
4	A BUS GOOD		BA001		
5	SET A & B REG.	B2H5 D10, D04	RA011	+3-0	
6	A & B REG		RA001 RB001		
7	CC, CV, CD DECODE		DC001 DV001 DD001		
8	SUM BIT & CARRY BIT		ALXXX		
9	SET ALU OUTPUT	B2G4 D04	AL141	+3-0	
10	SET SOURCE REG	B1L7 D02	KC021	+3-0	
11					
12					
13					
14					
15					
16					
17					
18					
19					
20					

TIMING CHART
STORAGE CONTROL ALU
DATE
TYPE 2841R
IBM 1704

1704

TIMING CHART - Storage Control - ALU

NO.	SIGNAL NAME	SP	LOGIC	LEVEL	TIME SCALE OR CYCLE
					OVERALL TIME SCALE IS FUNCTION OF MICROPROGRAM AND FILE DELAYS
1	MOD SELECT		HA031		UR REG SET AT ANY D TIME
2	2311 OPERABLE		HA091		RISE DEPENDS ON 2311 STATUS
3					
4	TRANSFER HEAD RESET				5 CYCLES
5	TRANSFER CYLINDER ADDRESS				5 CYCLES
6	SET SIGN BIT AND HEAD ADDRESS				5 CYCLES
7	TRANSFER CYLINDER DIFFERENCE ADDRESS				5 CYCLES
8	TRANSFER SEEK START				9 CYCLES
9					
10					A
11	MACHINE CYCLES				A B C D
12	CN 5 LATCHED				
13	FT REG				
14	FC REG				
15					
16					
17					
18					
19					
20					

TIMING CHART			
2311 SEEK			
DATE			
		TYPE	2841R
IBM		1711	

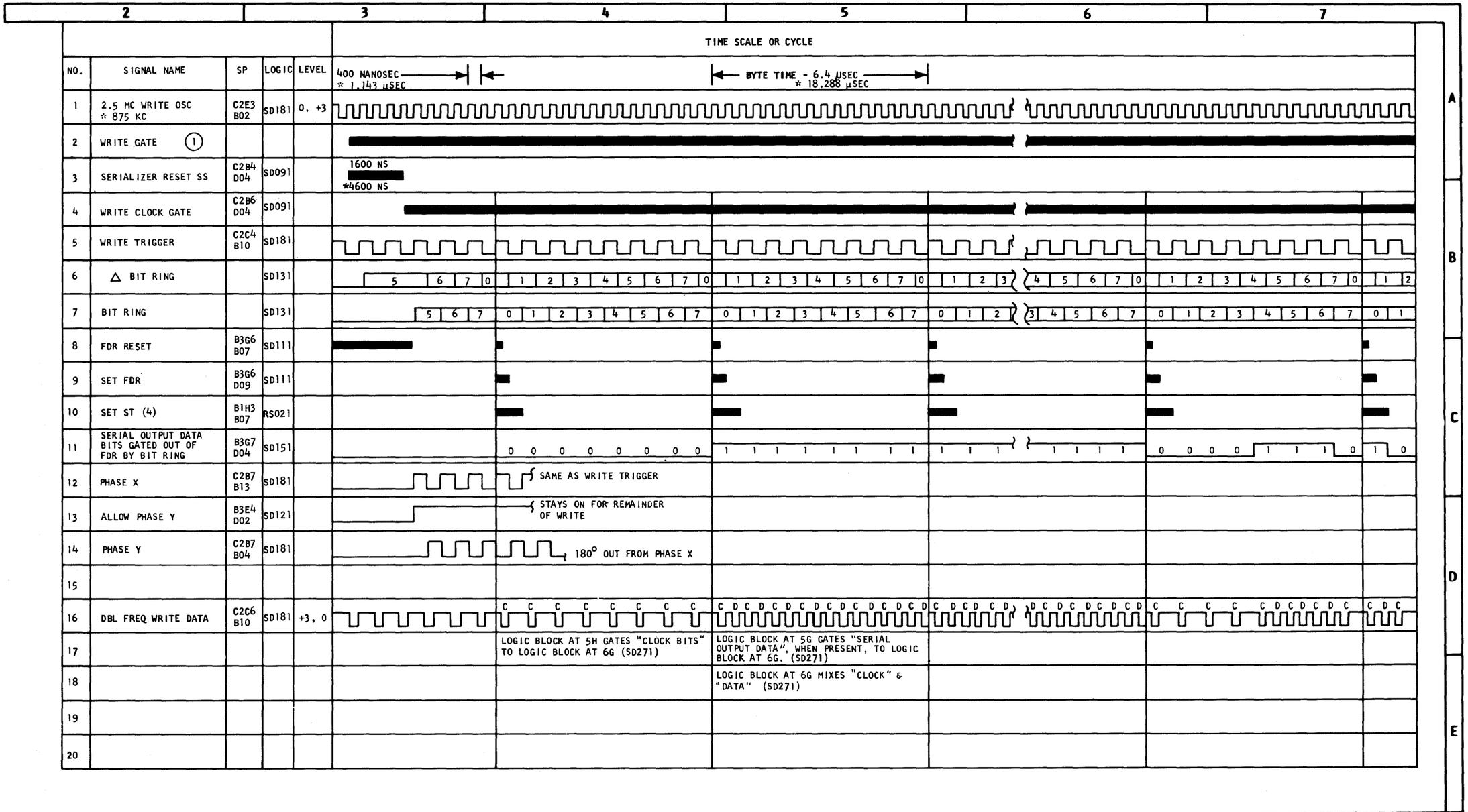
1711

NO.	SIGNAL NAME	SP	LOGIC	CLD PAGE	TIME SCALE OR CYCLE
					OVERALL TIME SCALE IS FUNCTION OF MICROPROGRAM AND FILE DELAYS
1	MOD SELECT		HB071	QB050	UR REG SET AT ANY D TIME
2	2321 OPERABLE		HB091	QB070	RISE DEPENDS ON 2321 STATUS
3					
4	TRANSFER HEAD ADDR & SET	A3A2 B12	HB062	QG130	
5	TRANSFER HEAD POS ADDRESS & SET	A3N7 D05	HB051	QG130	
6	TRANSFER FINGER ADDR. & SET	A3N7 D04	HB051	QG130	APPROX 6µs DEPENDING ON
7	TRANSFER SUBCELL ADDR. & SET	A3N7 D02	HB051	QG130	WHICH ADDR IS BEING SET; 3µs
8	TRANSFER CELL ADDR & SET	A3N7 D13	HB052	QG130	
9	TRANSFER SEEK START	A3A2 B10	HB061	QG130	
10					
11					
12					
13	FT REG		HB001	QG130	
14	FC REG		HB011	QG130	
15					
16					
17					
18					
19					
20					

TIMING CHART			
2321 SEEK			
DATE			
		TYPE	2841R
IBM		1712	

1712

TIMING CHART - 2321 Seek



NOTES:

(1) TURNED ON VIA MICROPROGRAM (QE080)

* 2321 REFERENCE

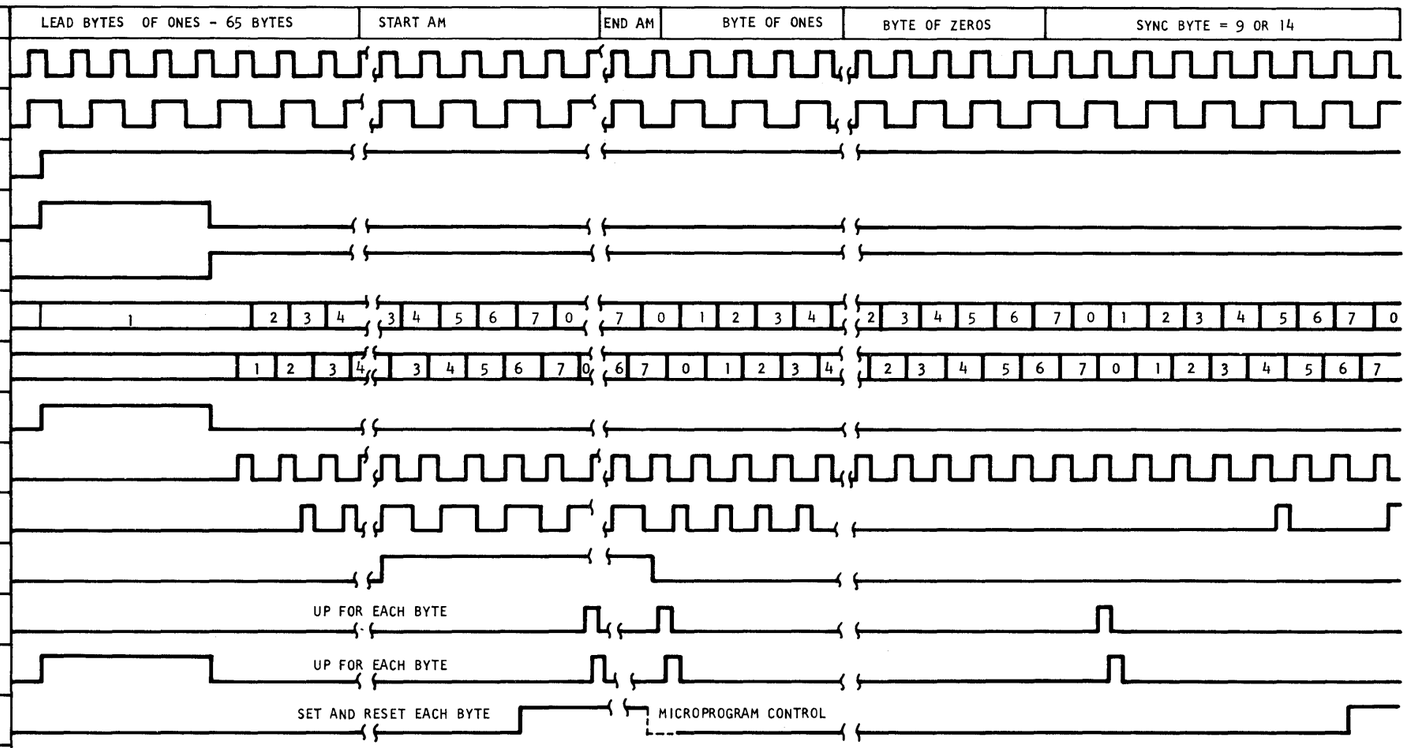
TIMING CHART			
WRITE			
DATE			
		TYPE	2841R
IBM		1721	

1721

TIMING CHART - Write

2	3	4	5	6	7

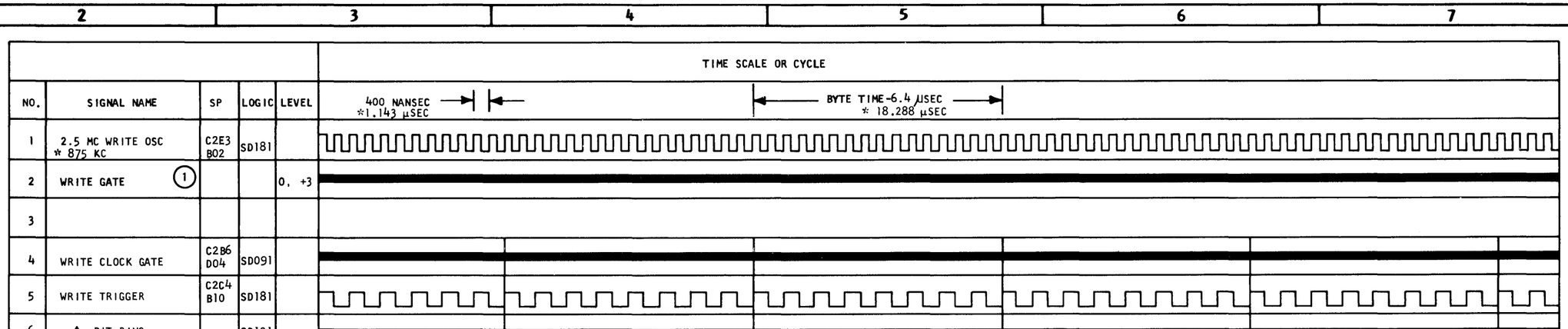
NO	SIGNAL NAME	LOGIC PAGE	TEST POINT	LVL
	2303 CLOCK			
	2/3 FREQUENCY OSC.			
	WRITE GATE			
	VFO RESET			
	WRITE CLOCK GATE			
	DELTA BIT RING			
	BIT RING			
	BIT RINGS RESET			
	BIT RING DRIVE			
	WRITE PHASE DATA			
	WRITE AM			
	RESET FDR			
	SET FDR			
	2303 DATA TRANSFERRED (SET ST 4)			



TIMING DIAGRAM			
2303 ATTACHMENT S/D WRITE			
DATE			
		TYPE	2841R
IBM		1722	

TIMING CHART - 2302 Attachment S/D Write

NO.	SIGNAL NAME	SP	LOGIC	LEVEL
1	2.5 MC WRITE OSC * 875 KC	C2E3 B02	SD181	
2	WRITE GATE (1)			0, +3
3				
4	WRITE CLOCK GATE	C2B6 D04	SD091	
5	WRITE TRIGGER	C2C4 B10	SD181	
6	△ BIT RING		SD131	
7	BIT RING		SD131	
8	FDR RESET	B3G6 B07	SD111	
9	SET FDR	B3G6 D09	SD111	
10	SET ST (4)	B1H3 B07	RS021	
11	SERIAL OUTPUT DATA (BITS GATED OUT OF FDR BY BIT RING)	B3G7 D04	SD151	
12				
13	ADDRESS MARK (1)			
14	WRITE AM LATCH	B3C5 B08	SD151	
15	INHIBIT CLOCK WR DATA	B3A6 B08	SD151	
16	DBL FREQ WRITE DATA	C2C6 B10	SD181	+3, 0
17				
18				
19				
20				



NOTES:

(1) TURNED ON VIA MICROPROGRAM - WRITE GATE ON QE080, AM ON QP080

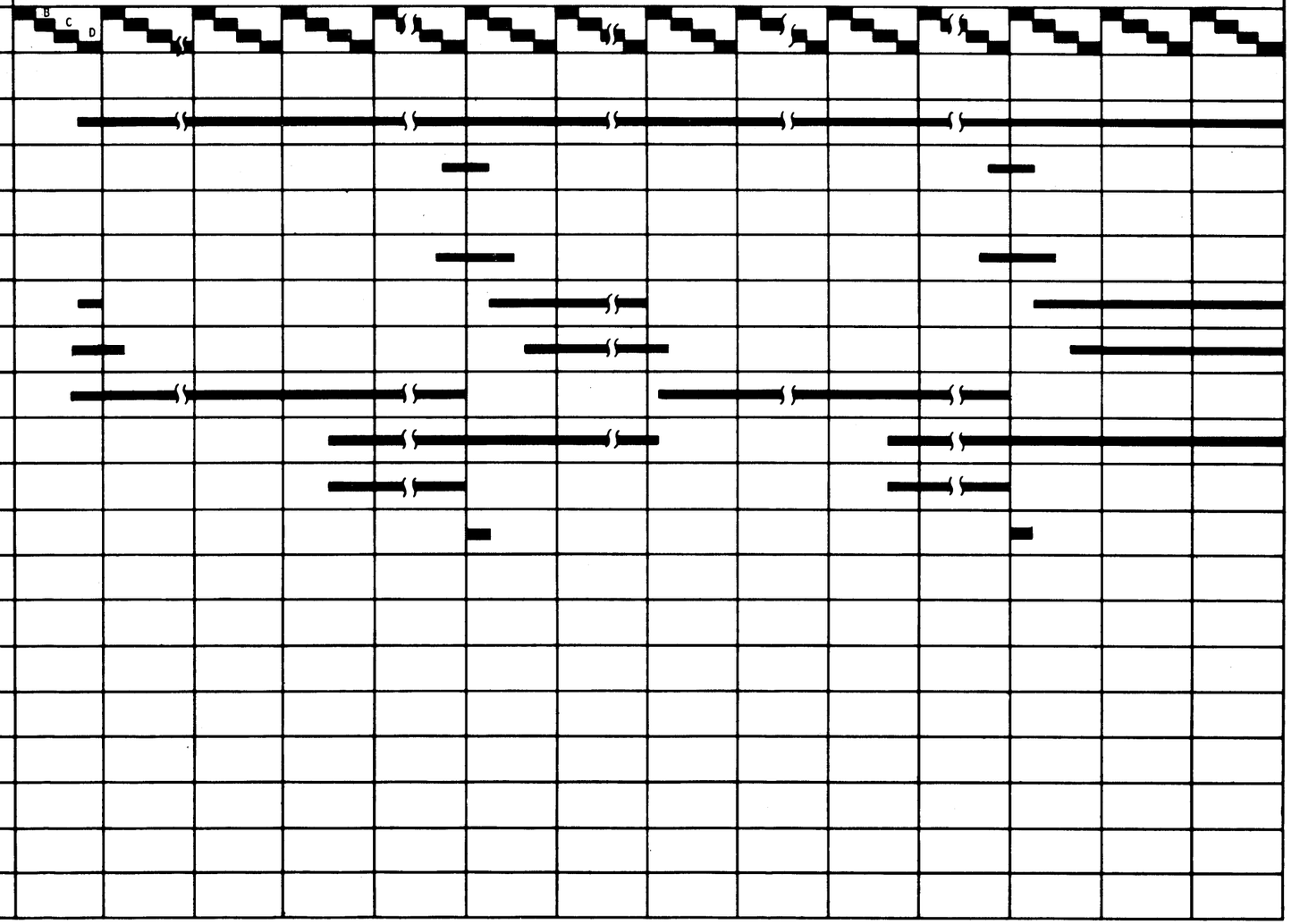
* 2321 REFERENCE

TIMING CHART			
WRITE AM			
DATE			
		TYPE	2841R
IBM		1723	

1723

TIMING CHART - Write Address Mark

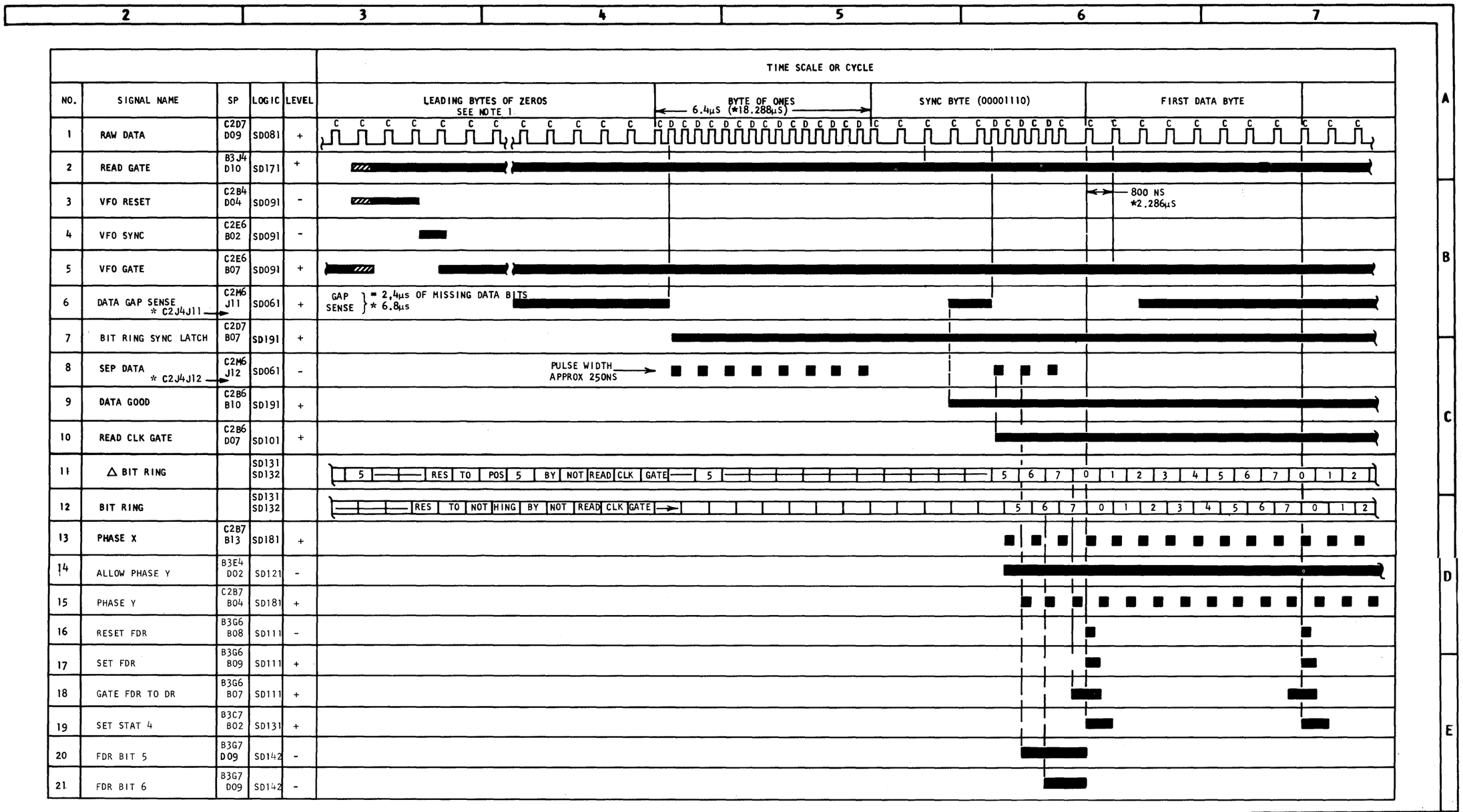
NO.	SIGNAL NAME	SP	LOGIC	LEVEL
1	MACHINE CYCLES A B C D			
2				
3	WRITE LATCH	C3F3 D04	GB131	0, +3
4	A SOURCE = IH		GB131	
5				
6	TRANSFER 1	C3H3 B08	GB131	
7	SVC REQUEST	C3H3D05	GB141	
8	TRANSFER 2	C3H3 D04	GB131	
9	SVC IN	C3H3 B02	GB141	
10	SVC OUT	C3J6 B13	GB061	
11	SERVICE REQUEST	C3H4 B09	GB151	+3, 0
12	SVC/IN RESET 1		GB151	
13				
14				
15				
16				
17				
18				
19				
20				



TIMING CHART
CHANNEL DATA TRANSFER - WRITE
DATE
TYPE 2841R
IBM 1725

1725

TIMING CHART - Channel Data Trnasfer - Write



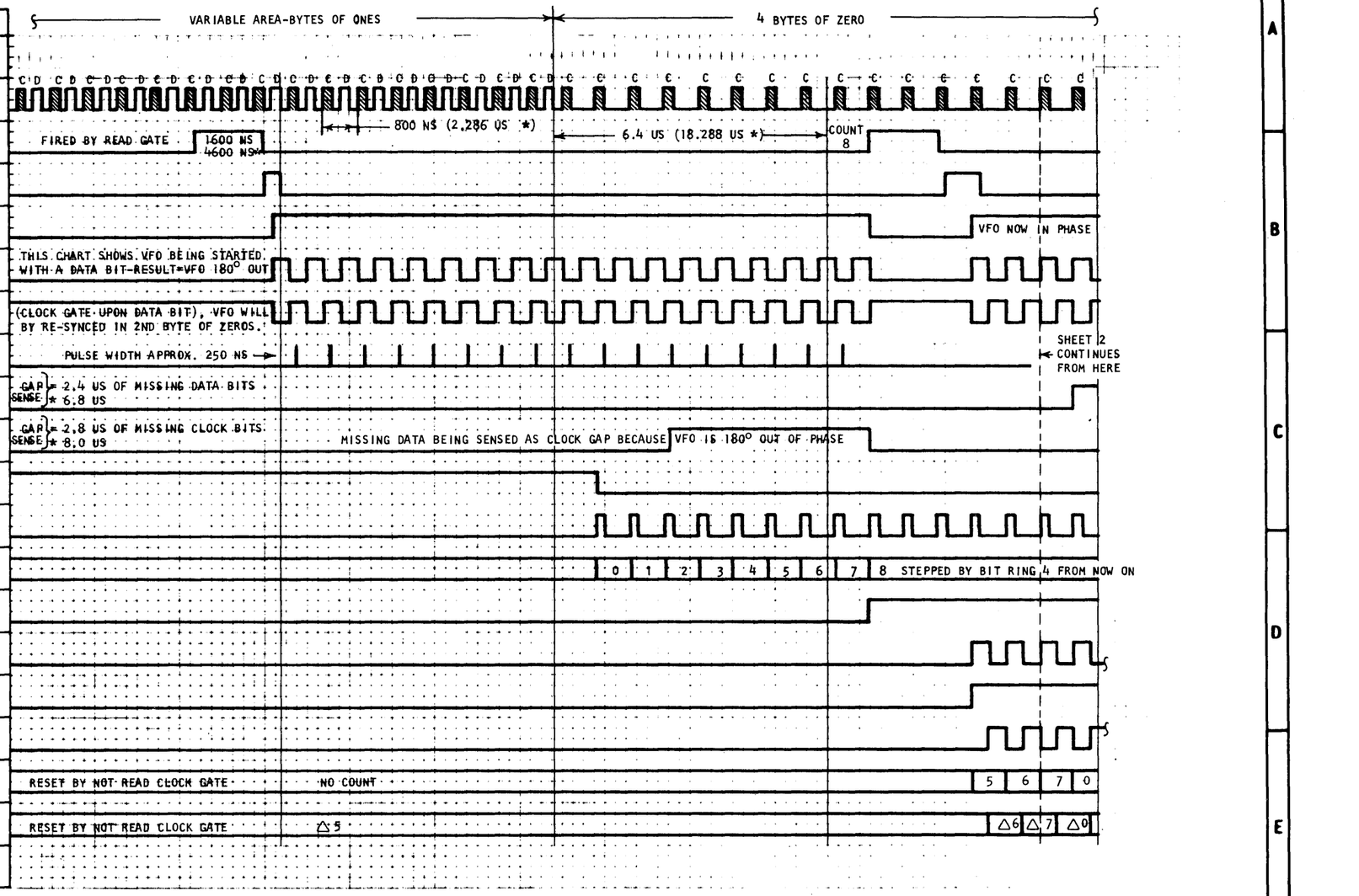
NO.	SIGNAL NAME	SP	LOGIC	LEVEL
1	RAW DATA	C2D7 D09	SD081	+
2	READ GATE	B3J4 D10	SD171	+
3	VFO RESET	C2B4 D04	SD091	-
4	VFO SYNC	C2E6 B02	SD091	-
5	VFO GATE	C2E6 B07	SD091	+
6	DATA GAP SENSE * C2J4J11	C2M6 J11	SD061	+
7	BIT RING SYNC LATCH	C2D7 B07	SD191	+
8	SEP DATA * C2J4J12	C2M6 J12	SD061	-
9	DATA GOOD	C2B6 B10	SD191	+
10	READ CLK GATE	C2B6 D07	SD101	+
11	△ BIT RING		SD131 SD132	
12	BIT RING		SD131 SD132	
13	PHASE X	C2B7 B13	SD181	+
14	ALLOW PHASE Y	B3E4 D02	SD121	-
15	PHASE Y	C2B7 B04	SD181	+
16	RESET FDR	B3G6 B08	SD111	-
17	SET FDR	B3G6 B09	SD111	+
18	GATE FDR TO DR	B3G6 B07	SD111	+
19	SET STAT 4	B3C7 B02	SD131	+
20	FDR BIT 5	B3G7 D09	SD142	-
21	FDR BIT 6	B3G7 D09	SD142	-

* 2321 ONLY

NOTES:
1. SEE PAGES 736 &737 FOR GAP BIT CONFIGURATION
2. PHASE Y PULSES MAY OCCUR BEFORE ALLOW PHASE Y, BUT THESE ARE NOT FUNCTIONAL

TIMING CHART			
READ			
DATE			
		TYPE	2841R
IBM		1731	

NO	SIGNAL NAME	SCOPE POINT	LOGIC PAGE
1	RAW DATA	C2E5B02	SD011
2	VFO RESET SS	C2B4D04	SD091
3	VFO SYNC	C2E6B02	SD091
4	VFO GATE	C2E6B07	SD091
5	SEP CLOCK GATE	C2K4B09 *C2J2B09	SD051 *SD056
6	SEP DATA GATE	C2K4B05 *C2J2B05	SD051 *SD056
7	SPEARATED DATA	C2M6J12 *C2J4J12	SD061 *SD066
8	DATA GAP SENSE	C2M6J11 *C2J4J11	SD061 *SD066
9	CLOCK GAP SENSE	C2M6J13 *C2J4J13	SD061 *SD066
10	ONES RESET	C2M6D02 *C2J4D02	SD031 *SD036
11	ZEROS COUNT	C2M6D02 *C2J4D02	SD031 *SD036
12	BINARY COUNTER		SD201
13	READ CLOCK GATE	C2B6D07	SD101
14	PHASE X	C2B7B13	SD181
15	ALLOW PHASE Y	B3E4D02	SD121
16	PHASE Y	C2B7B04	SD181
17	BIT RING		SD131 SD132
18	DELTA BIT RING		SD131 SD132



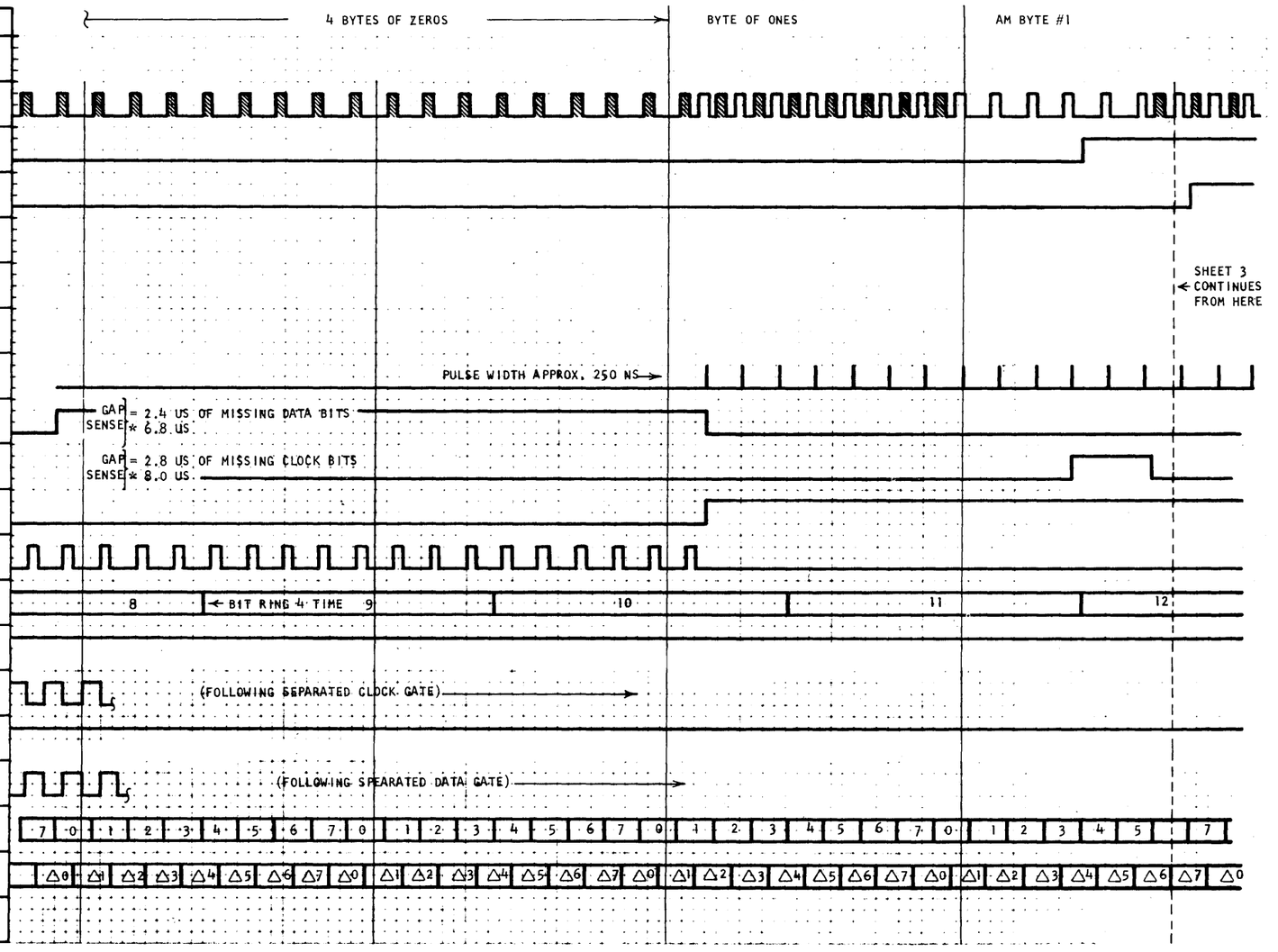
* 2321 ONLY

TIMING CHART - READ ADDRESS MARK			
DATE			
		TYPE	2841R
IBM		1733	

1733

TIMING CHART - Read Address Mark (Page 1 of 3)

NO	SIGNAL NAME	SCOPE POINT	LOGIC PAGE
1	RAW DATA	C2E5B02	SD011
2	AM 1	B3H6B04	SD211
3	AM 2	B3H6B07	SD211
4	AM 3	B3H6B12	SD211
5	AM GOOD	B3H3D11	SD211
6	DATA GOOD	C2B6B10	SD191
7	SEPARATED DATA	C2M6J12 *C2J4J12	SD061 *SD066
8	DATA GAP SENSE	C2M6J11 *C2J4J11	SD061 *SD066
9	CLOCK GAP SENSE	C2M6J13 *C2J4J13	SD061 *SD066
10	ONES RESET	C2M6D02 *C2J4D02	SD031 *SD036
11	ZEROS COUNT	C2M6B04 *C2J4B04	SD031 *SD036
12	BINARY COUNTER		
13	READ CLOCK GATE	C2B6D07	SD101
14	PHASE X	C2B7B13	SD181
15	ALLOW PHASE Y	B3E4D02	SD121
16	PHASE Y	C2B7B04	SD181
17	BIT RING	-	SD131 SD132
18	DELTA BIT RING	-	SD131 SD132
19	STAT 4	C2D7D12	*SD066



* 2321 ONLY

TIMING CHART - READ ADDRESS MARK

DATE

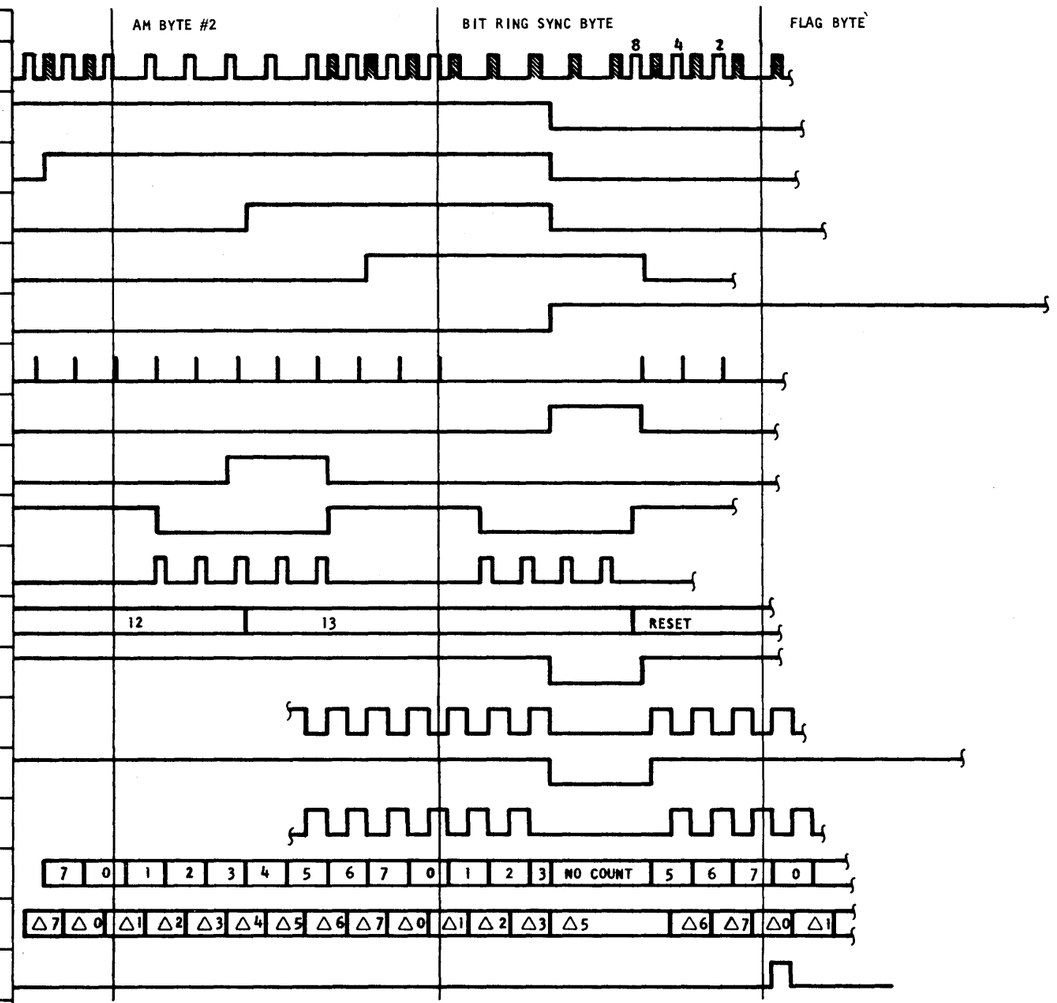
TYPE 2841R

IBM 1733

TIMING CHART - Read Address Mark (Page 2 of 3)

NO	SIGNAL NAME	SCOPE POINT	LOGIC PAGE
1	RAW DATA	C2E5B02	SD011
2	AM 1	B3H6B04	SD211
3	AM 2	B3H6B07	SD211
4	AM 3	B3H6B12	SD211
5	AM GOOD	B3H3D11	SD211
6	DATA GOOD	C2B6B10	SD191
7	SEPARATED DATA	C2M6J12 *C2J4J12	SD061 *SD066
8	DATA GAP SENSE	C2M6J11 *C2J4J11	SD061 *SD066
9	CLOCK GAP SENSE	C2M6J13 *C2J4J13	SD061 *SD066
10	ONE'S RESET	C2M6D02 *C2J4D02	SD031 *SD036
11	ZERO'S COUNT	C2M6B04 *C2J4B04	SD031 *SD036
12	BINARY COUNTER		
13	READ CLOCK GATE	C2B6D07	SD101
14	PHASE X	C2B7B13	SD181
15	ALLOW PHASE Y	B3E4D02	SD121
16	PHASE Y	C2B7B04	SD181
17	BIT RING		SD131 SD132
18	DELTA BIT RING		SD131 SD132
19	SET STAT 4	C2D7D12	*SD066

* 2321 ONLY



TIMING CHART - READ ADDRESS MARK			
DATE			
		TYPE	2841R
IBM		1733	

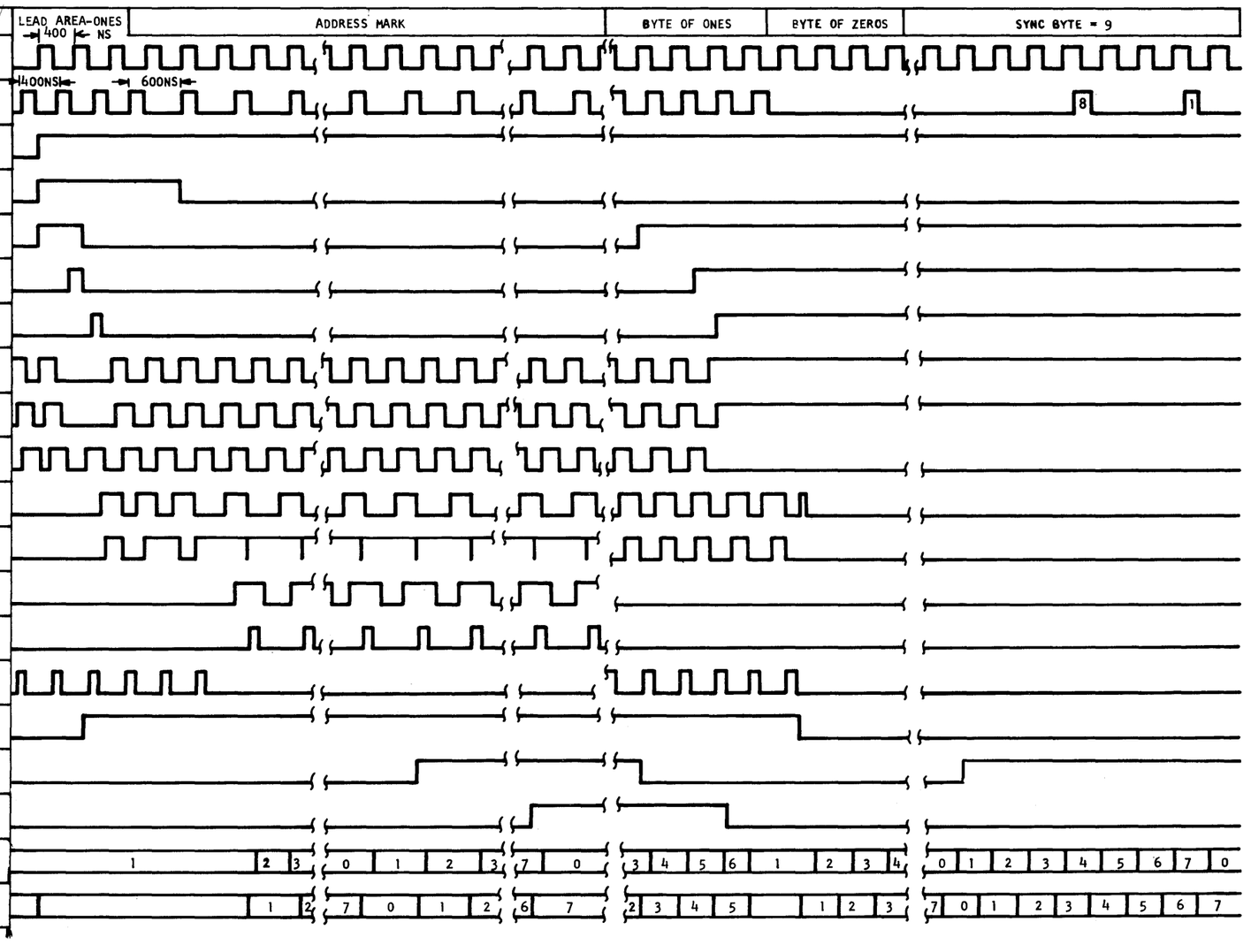
1733

TIMING CHART-Read Address Mark (Page 3 of 3)

2	3	4	5	6	7

SHEET 1 OF 2

NO	SIGNAL NAME	LOGIC PAGE	TEST POINT	LVL
	2303 CLOCK			
	2303 DATA			
	READ GATE			
	VFO RESET			
	SELECT PHASE LATCH			
	LEADING EDGE DETECTOR			
	HOLD PHASE			
	LATCH 1			
	LATCH 2			
	LATCH 3			
	AM DET. 1			
	AM DET. 2			
	AM DET. 3			
	AM BIT PRESENT			
	AM BIT MISSING			
	SEARCH AM			
	8 BITS			
	AM GOOD			
	DELTA BIT RING			
	BIT RING			



A B C D E

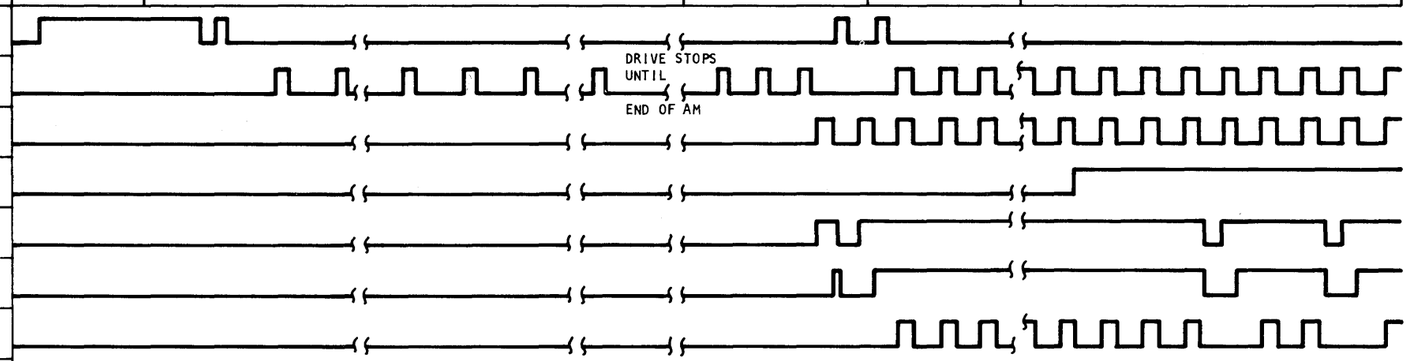
TIMING DIAGRAM			
2303 ATTACHMENT S/D READ AM			
DATE			
		TYPE	2841R
IBM		1734	

TIMING CHART - 2303 Attachment S/D Read AM (Page 1 of 2)

2	3	4	5	6	7

SHEET 2 OF 2

NO	SIGNAL NAME	LOGIC PAGE	TEST POINT	LVL
	DELTA AND BIT RING RESET			
	BIT RING DRIVE			
	SELECTED PHASE			
	2303 READ CLOCK GATE			
	ZEROS DET. 1			
	ZEROS DET. 2			
	ZEROS COUNT			

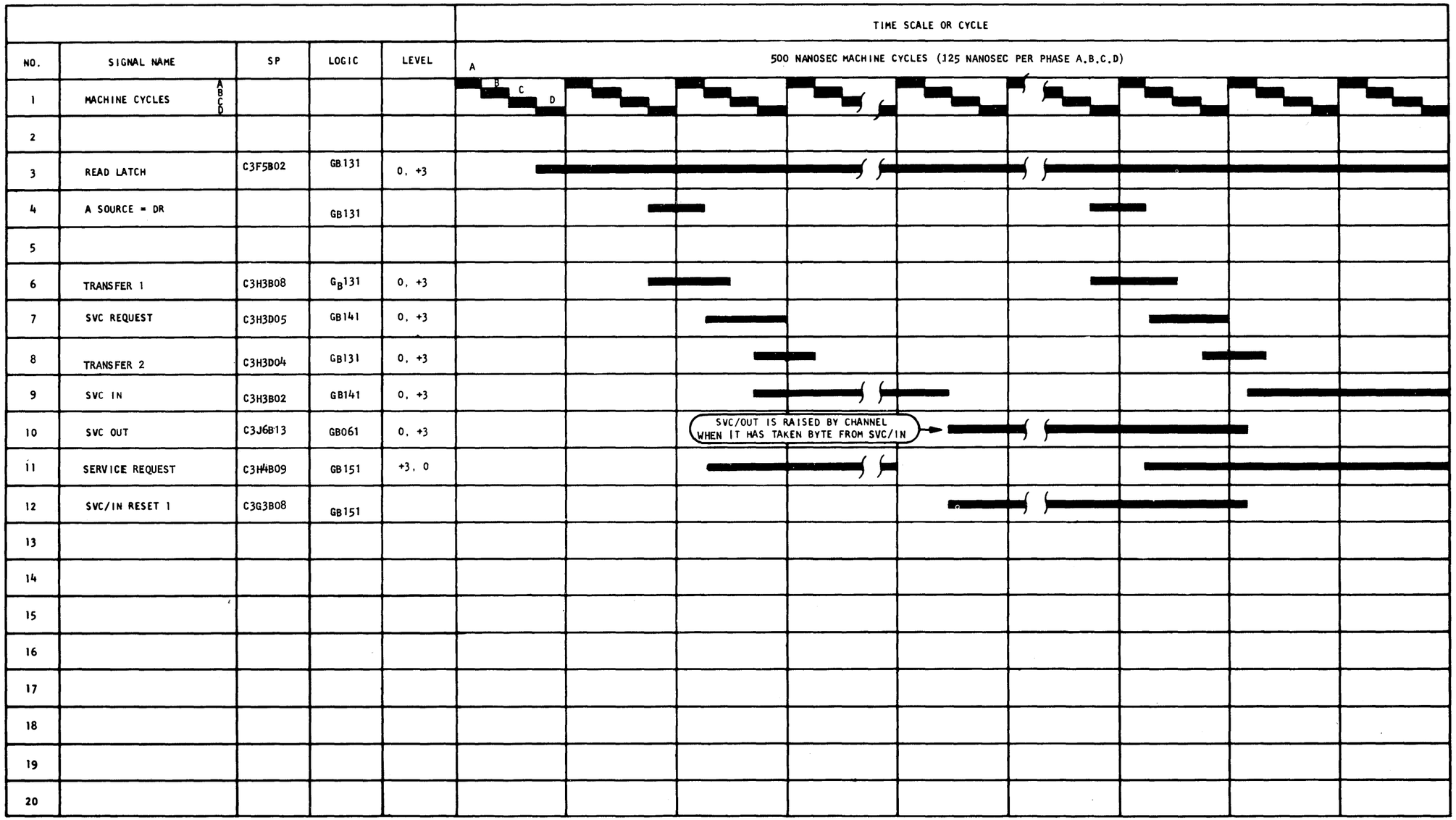


A
B
C
D
E

TIMING DIAGRAM			
2303 ATTACHMENT S/D READ AM			
DATE			
		TYPE	2841R
IBM	1734		

TIMING CHART - 2303 Attachment S/D Read AM (Page 2 of 2)

NO.	SIGNAL NAME	SP	LOGIC	LEVEL
1	MACHINE CYCLES A B C D			
2				
3	READ LATCH	C3F5B02	GB131	0, +3
4	A SOURCE = DR		GB131	
5				
6	TRANSFER 1	C3H3B08	G_B131	0, +3
7	SVC REQUEST	C3H3D05	GB141	0, +3
8	TRANSFER 2	C3H3D04	GB131	0, +3
9	SVC IN	C3H3B02	GB141	0, +3
10	SVC OUT	C3J6B13	GB061	0, +3
11	SERVICE REQUEST	C3H4B09	GB151	+3, 0
12	SVC/IN RESET 1	C3G3B08	GB151	
13				
14				
15				
16				
17				
18				
19				
20				



TIMING CHART			
CHANNEL DATA TRANSFER-READ			
DATE			
		TYPE	2841R
IBM		1735	

TIMING CHART - Channel Data Transfer-Read

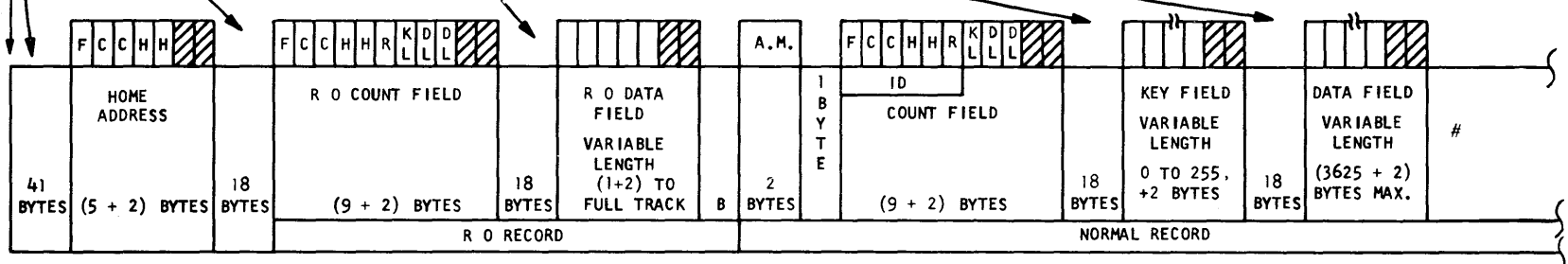
2302 - 2311 TRACK FORMAT

LEAD AREA-36 BYTES			VFO AREA-4 BYTES				BIT RING SYNC AREA 1 BYTE
ZEROS	ZEROS	ZEROS	ZEROS	ZEROS	ZEROS	ONES	4 BITS ZEROS 3 BITS ONES 1 BIT ZERO
0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1	0 0 0 0 1 1 1 0

LEAD BYTE	LEAD AREA 12 ZEROS		VFO AREA-4 BYTES				BIT RING SYNC AREA 1 BYTE
	ZEROS	ZEROS	ZEROS	ZEROS	ZEROS	ONES	4 BITS ZEROS 3 BITS ONES 1 BIT ZERO
1 1 0 0 1 1 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1	0 0 0 0 1 1 1 0

LEAD BYTE	LEAD AREA 9 ONES		VFO AREA-7 BYTES 6 BYTES ZEROS				BIT RING SYNC AREA 1 BYTE
	ONES	ONES	ZEROS	ZEROS	ZEROS	ONES	4 BITS ZEROS 3 BITS ONES 1 BIT ZERO
1 1 0 0 1 1 0 0	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1	0 0 0 0 1 1 1 0

INDEX



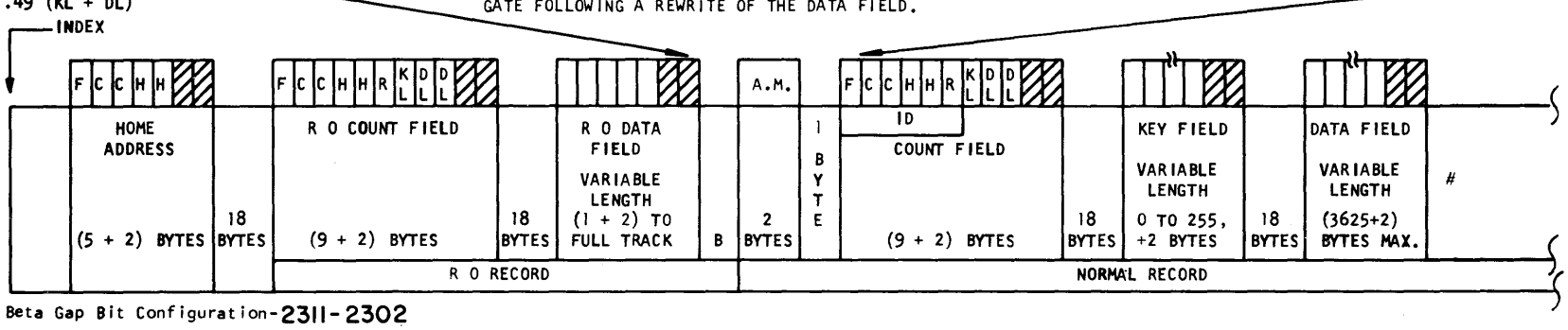
HA or Alpha Gap Bit Configuration- **2302**

LEAD BYTE *	VARIABLE AREA 21 BYTES MIN. OF GOOD DATA	VFO AREA-5 BYTES					ADDRESS MARK AREA 2 BYTES		BIT RING SYNC BYTE
	ONES	ZEROS	ZEROS	ZEROS	ZEROS	ONES	ONES 5 BITS MISSING CLOCK PLUSES NO CLOCK	ONES 5 BITS MISSING CLOCK PLUSES NO CLOCK	4 BITS ZEROS 3 BITS ONES 1 BIT ZERO
1 1 0 0 1 1 0 0	1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	0 0 0 0 1 1 1 0

VARIABLE AREA=21 + .49 (KL + DL)

* LEAD BYTE FOLLOWING A DATA FIELD MAY HAVE A "GLITCH" IN IT DUE TO THE DROPPING OF WRITE GATE FOLLOWING A REWRITE OF THE DATA FIELD.

INDEX



Beta Gap Bit Configuration- **2311-2302**

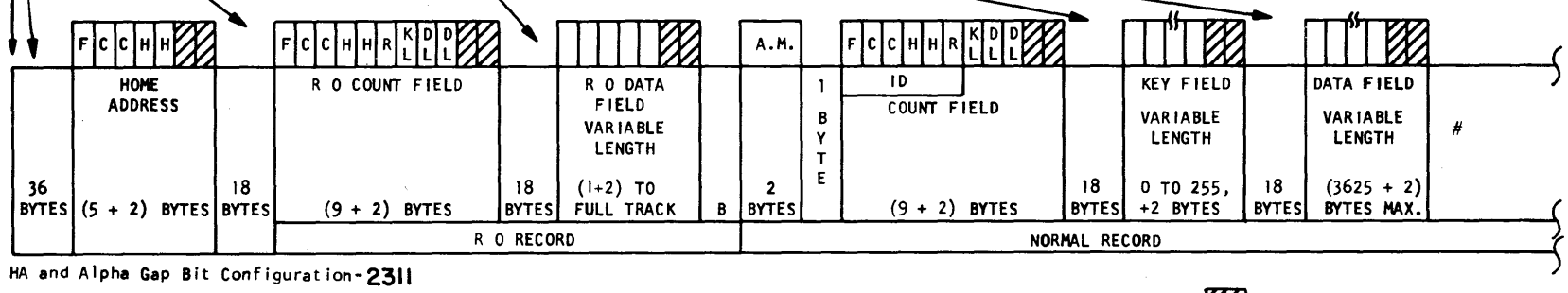
LEAD AREA-30 BYTES			VFO AREA-4 BYTES				BIT RING SYNC AREA 1 BYTE
ZEROS	ZEROS	ZEROS	ZEROS	ZEROS	ZEROS	ONES	4 BITS ZEROS 3 BITS ONES 1 BIT ZERO
0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1	0 0 0 0 1 1 1 0

LEAD BYTE	LEAD AREA 12 ZEROS		VFO AREA-4 BYTES				BIT RING SYNC AREA 1 BYTE
	ZEROS	ZEROS	ZEROS	ZEROS	ZEROS	ONES	4 BITS ZEROS 3 BITS ONES 1 BIT ZERO
1 1 0 0 1 1 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1	0 0 0 0 1 1 1 0

LEAD BYTE	LEAD AREA 9 ONES		VFO AREA-7 BYTES 6 BYTES ZEROS				BIT RING SYNC AREA 1 BYTE
	ONES	ONES	ZEROS	ZEROS	ZEROS	ONES	4 BITS ZEROS 3 BITS ONES 1 BIT ZERO
1 1 0 0 1 1 0 0	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1	0 0 0 0 1 1 1 0

= ON LAST RECORD OF TRACK, "ONES" ARE WRITTEN AFTER 2nd BURST BYTE UNTIL INDEX.

INDEX



HA and Alpha Gap Bit Configuration- **2311**

= CYCLIC CHECK

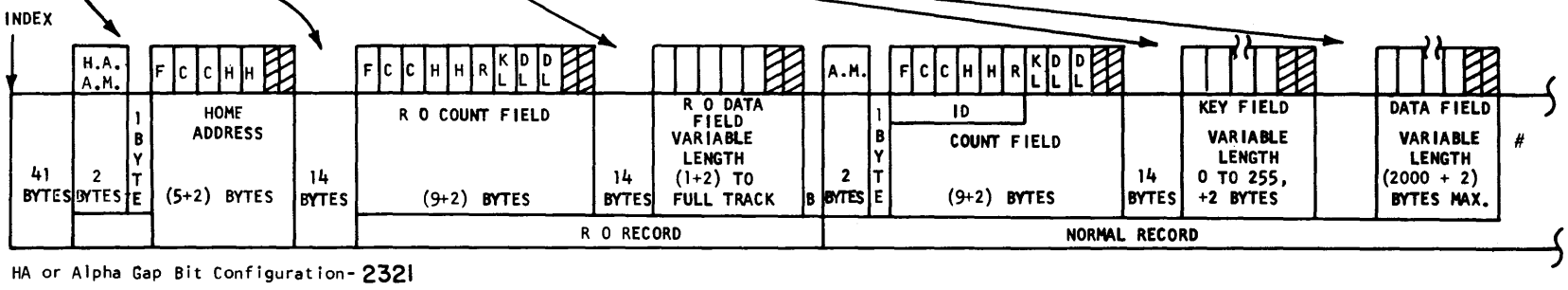
TIMING CHART - 2302/2311 Track Format

2321 TRACK FORMAT

LEAD AREA 36 BYTES ONES	VFO AREA-5 BYTES				ADDRESS MARK AREA 2 BYTES		BIT RING SYNC AREA 1 BYTE
	ZEROS	ZEROS	ZEROS	ONES	ONES 5 BITS MISSING CLOCK PULSES NO CLOCK	ONES 5 BITS MISSING CLOCK PULSES NO CLOCK	4 BITS ZEROS 1 BIT ONE 2 BITS ZEROS 1 BIT ONE
1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	0 0 0 0 1 0 0 1

LEAD BYTE	LEAD AREA 8 ZEROS		VFO AREA-4 BYTES				BIT RING SYNC AREA 1 BYTE
	ZEROS	ZEROS	ZEROS	ZEROS	ZEROS	ONES	4 BITS ZERO 3 BITS ONES 1 BIT ZERO
1 1 0 0 1 1 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1	0 0 0 0 1 1 1 0

LEAD BYTE	LEAD AREA 3 ONES		VFO AREA-9 BYTES 8 BYTES ZEROS				BIT RING SYNC AREA 1 BYTE
	ONES	ONES	ZEROS	ZEROS	ZEROS	ONES	4 BITS ZERO 3 BITS ONES 1 BIT ZERO
1 1 0 0 1 1 0 0	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1	0 0 0 0 1 1 1 0

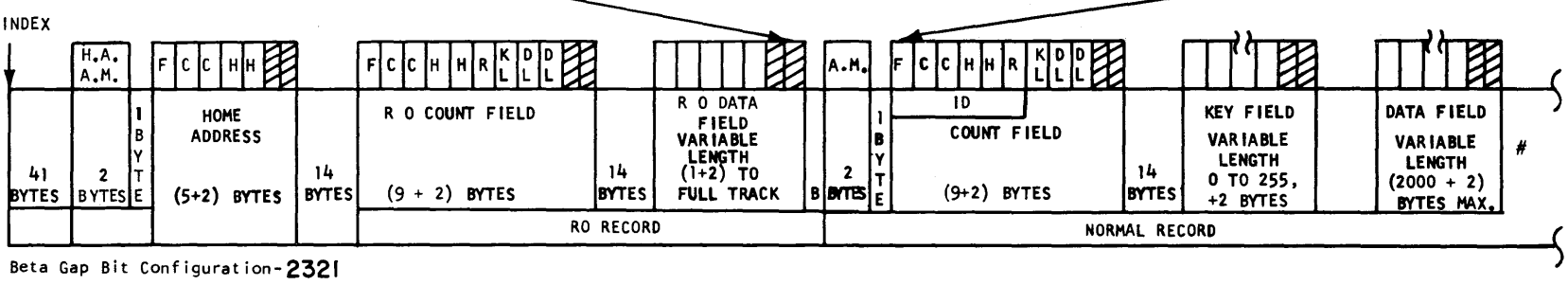


HA or Alpha Gap Bit Configuration- 2321

LEAD BYTE *	VARIABLE AREA 48 BYTES MIN. OF GOOD DATA	VFO AREA-5 BYTES				ADDRESS MARK AREA 2 BYTES		BIT RING SYNC BYTE
	ONES	ZEROS	ZEROS	ZEROS	ONES	ONES 5 BITS MISSING CLOCK PLUSES NO CLOCK	ONES 5 BITS MISSING CLOCK PLUSES NO CLOCK	4 BITS ZEROS 3 BITS ONES 1 BIT ZERO
1 1 0 0 1 1 0 0	1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	0 0 0 0 1 1 1 0

VARIABLE AREA= 48+.49(KL+DL)

* LEAD BYTE FOLLOWING A DATA FIELD MAY HAVE A "GLITCH" IN IT DUE TO THE DROPPING OF WRITE GATE FOLLOWING A REWRITE OF THE DATA FIELD.



Beta Gap Bit Configuration- 2321

= CYCLIC CHECK

\# = ON LAST RECORD OF TRACK, BYTES OF "ONES" ARE WRITTEN AFTER 2nd BURST BYTE (CC), UNTIL INDEX.

0	1	2	3	4	5	6	7
X	X	←	NOT	USED	→	X	X

FLAG BYTE – ALL FILES

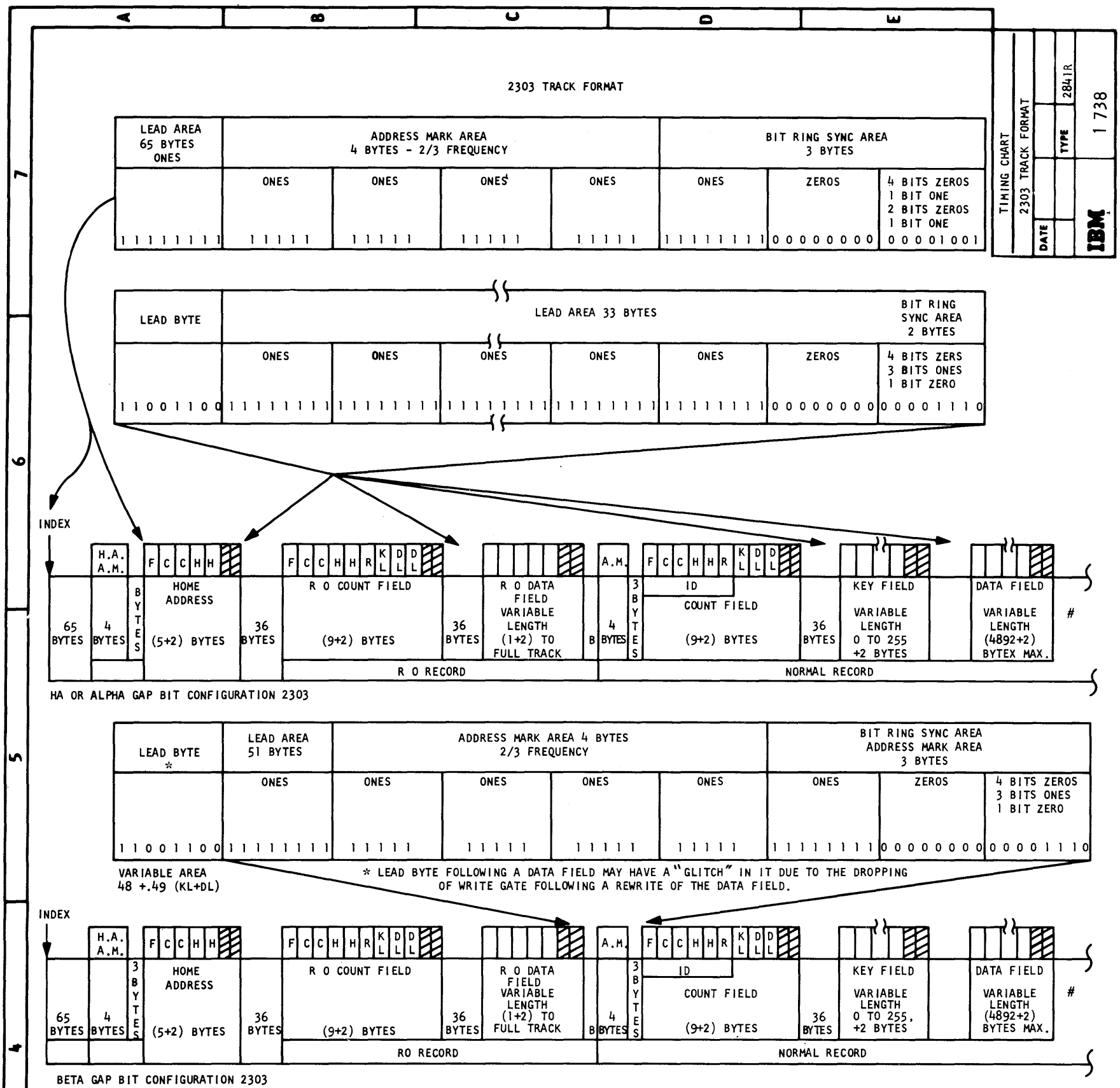
0 = NOT ALTERNATE TRACK
1 = ALTERNATE TRACK

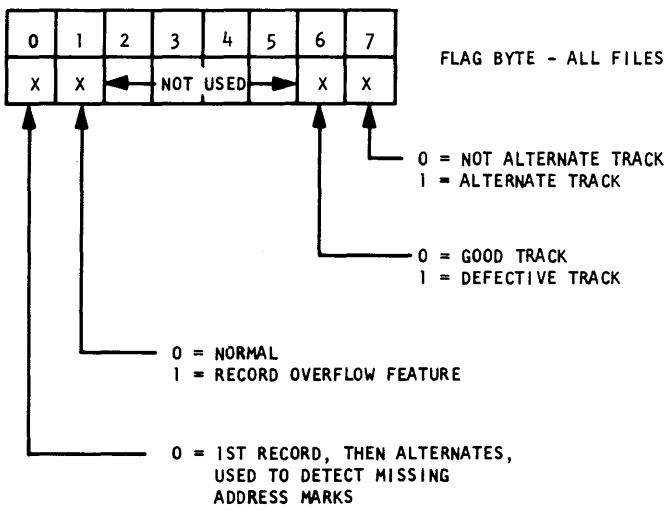
0 = GOOD TRACK
1 = DEFECTIVE TRACK

0 = NORMAL
1 = RECORD OVERFLOW FEATURE

0 = 1ST RECORD, THEN ALTERNATES, USED TO DETECT MISSING ADDRESS MARKS

TIMING CHART-2321 Track Format





TIMING CHART - 2303 Track Format

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Easy to read and understand?	☐	☐
Organized for convenient use?	☐	☐
Complete?	☐	☐
Well illustrated?	☐	☐
Written for your technical level?	☐	☐

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For advanced knowledge of the subject?	☐	As a student in a class?	☐
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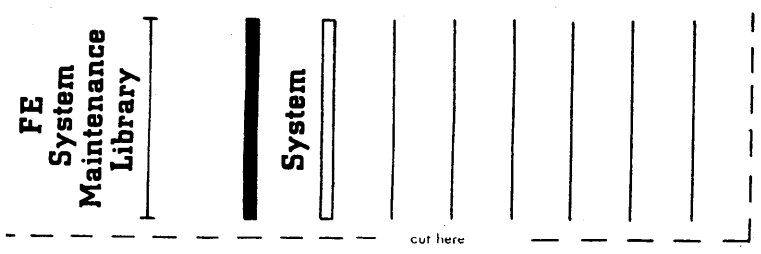

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