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2841

Storage Control Unit

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2841

Storage Control Unit

PREFACE

This manual describes the theory and operation of the IBM 2481 Storage Control Unit with the IBM 2311 Disk Storage Unit.

The following is a list of companion and pre-requisite manuals necessary for understanding of the 2841.

IBM Field Engineering Diagram Manual,
2841 Storage Control Unit (Form 227-3644)

IBM Systems Reference Library Manual,
System 360 Component Descriptions
(Form A26-5988)

IBM Field Engineering Preschool Manuals,
System/360

IBM Systems Reference Library Manual,
System/360 Principles of Operation
(Form A22-6821)

IBM Field Engineering Maintenance Manual,
2841 Storage Control Unit (Form 227-3615)

IBM Field Engineering Manual of Instruction,
SLT Packaging

IBM Installation Manual, 2841 Storage Control
Unit (included in System Diagram Manual)
IBM Maintenance Diagram Manual, 2841 Storage
Control Unit (included in System Diagram
Manual

It is assumed that the student has completed IBM System/360 preschool training and has been trained on the 2311 Disk Storage Unit.

Because the 2311 is the standard device used with the 2841, most of the references in Chapters 1 through 4 of this manual are to operation with the 2311 interface.

The users of this manual are cautioned that machine specifications are subject to change at any time and without prior notice by IBM. Wiring diagrams (logics) at the engineering change level of that specific machine are included in each machine shipment.

This edition (Form 227-3614-2) is a major revision of Form 227-3614-1. The latter is made obsolete by this revision.

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If the form has been detached, comments may be directed to:

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CHAPTER 1 INTRODUCTION	1, 1	2.4 TRANSFORMER READ ONLY STORAGE - TROS	2, 4
1.1 GENERAL INFORMATION	1, 1	2.4.1 Purpose and Use of TROS	2, 4
1.2 PHYSICAL DESCRIPTION	1, 2	2.4.2 Characteristics and Capacity	2, 5
1.2.1 Dimensions	1, 2	2.4.3 Principles of Operation	2, 5
1.2.2 Power Requirements	1, 2	2.4.4 Module Physical Construction	2, 6
1.2.3 Cable Entry	1, 2	2.4.5 TROS Tape Deck	2, 7
1.2.4 Operator's Position	1, 2	2.4.6 Addressing TROS	2, 7
1.2.5 Environmental Conditions	1, 2	2.4.7 Decoding the Address Register	2, 8
1.2.6 Power Control	1, 2	2.4.8 TROS Functional Operation	2, 9
1.3 FUNCTIONAL DESCRIPTION	1, 2	2.4.9 Array Layout	2, 9
1.3.1 System/360 Channel Interface	1, 2	2.4.10 TROS Output Word	2, 10
1.3.2 Arithmetic/Logical Unit (ALU)	1, 2	2.4.11 Control Latches	2, 10
1.3.3 Serializer/Deserializer Unit (SERDES)	1, 2	2.4.12 TROS Address Check	2, 10
1.3.4 Fourteen General Purpose Registers	1, 3	2.4.13 TROS Sense Amplifier Check	2, 11
1.3.5 Transformer Read-Only-Storage (TROS)	1, 3	2.4.14 TROS Control Register Check	2, 11
1.3.6 Device Interfaces	1, 3	2.5 ARITHMETIC/LOGICAL UNIT (ALU)	2, 11
1.3.7 Basic Write Data Flow	1, 3	2.5.1 ALU General Description	2, 11
1.3.8 Basic Read Data Flow	1, 3	2.5.2 Summary of ALU Statements	2, 12
1.4 TRACK FORMAT	1, 3	2.5.3 ALU Functional Description and Basic Timing	2, 14
1.4.1 Index Marker	1, 3	2.6 SERIALIZER/DESERIALIZER UNIT	2, 15
1.4.2 Home Address Area	1, 3	2.6.1 SERDES General Description	2, 15
1.4.3 Track Descriptor Record (R0)	1, 4	2.6.2 Write Operation	2, 15
1.4.4 Data Record	1, 5	2.6.3 Read Operation	2, 16
1.4.5 Gaps	1, 6	2.7 CHANNEL INTERFACE ATTACHMENT	2, 18
1.4.6 Error Detection	1, 6	2.7.1 Initial Selection Sequence	2, 18
1.5 PROGRAMMING	1, 7	2.7.2 Data Transfer Sequences	2, 19
System/360 I/O Interface	1, 7	2.7.3 Ending Sequence	2, 20
1.6 CHANNEL INTERFACE INTRODUCTION	1, 7	2.7.4 Short Control Unit Busy Sequence	2, 20
1.7 INTERFACE LINES	1, 7	2.7.5 Halt I/O Instruction	2, 21
1.7.1 Bus Lines	1, 8	2.7.6 Polling Interrupts	2, 21
1.7.2 Scan Controls	1, 8	2.7.7 Resets	2, 22
1.7.3 Outbound Tag Lines	1, 9	2.8 CE PANEL	2, 23
1.7.4 Inbound Tag Lines	1, 11	2.8.1 CE Switches	2, 23
1.7.5 Interlock Lines	1, 11	2.8.2 CE Indicators	2, 24
1.7.6 Special Controls	1, 12	2.9 CAS MICROBLOCK	2, 25
1.8 INTERFACE OPERATIONS	1, 13	2.9.1 TROS Bit Assignment Chart	2, 25
1.8.1 Initial Selection Sequence	1, 13	2.9.2 Microblock Symbolology	2, 27
1.8.2 Data Transfers	1, 14	2.9.3 Sample Usage of Microblocks	2, 28
1.8.3 End Operation	1, 14		
CHAPTER 2 FUNCTIONAL UNITS	2, 1	CHAPTER 3 THEORY OF OPERATION	3, 1
2.1 MACHINE CLOCK	2, 1	3.1 STATUS INFORMATION	3, 1
2.2 REGISTERS	2, 1	3.2 SENSE INFORMATION	3, 2
2.2.1 General Purpose Registers	2, 1	3.2.1 Sense Byte 0	3, 2
2.2.2 A Register	2, 1	3.2.2 Sense Byte 1	3, 3
2.2.3 B Register	2, 1	3.2.3 Sense Byte 2	3, 4
2.2.4 DR Register - Data Read Register	2, 2	3.2.4 Sense Byte 3	3, 4
2.2.5 ST Register - Status Register	2, 2	3.2.5 Sense Byte 4	3, 5
2.2.6 ER - Error Register	2, 2	3.2.6 Sense Byte 5	3, 5
2.2.7 Miscellaneous Registers and Controls	2, 2	3.3 MISCELLANEOUS OPERATIONS	3, 5
2.3 2311 INTERFACE ATTACHMENT	2, 3	3.3.1 Multiple Track (M/T) Operation	3, 5
2.3.1 FT - File Tag Register	2, 3	3.3.2 End-of-File	3, 5
2.3.2 FC - File Control Register	2, 3	3.3.3 Defective Surfaces	3, 6
2.3.3 MS - Module Select Gates	2, 4	3.3.4 Initial Program Load (0000 0010)	3, 8
2.3.4 SC - Seek Complete Gates	2, 4	3.3.5 File Protection	3, 8
2.3.5 FS - File Status Gates	2, 4	3.4 COMMAND FLOW CHARTS	3, 9
2.3.6 OA - Old Address Gates	2, 4		
2.3.7 IE - Input Element Gates	2, 4		

3.5	CONDENSED MICRO PROGRAM LOGIC	3.9	CHAPTER 5 FEATURES	5.1
3.5.1	General	3.9	5.1 2302, MODELS 3 AND 4, 2321,	
3.5.2	Initial Selection	3.10	ATTACHMENT	5.1
3.5.3	Command Decode	3.10	5.1.1 Device Attachment Limits	5.2
3.5.4	Initial Status Presentation	3.11	5.1.2 2302 Operation	5.2
3.5.5	Load Counts	3.11	5.1.3 2321 Operation	5.2
3.5.6	Write Operations	3.11	5.2 ADDITIONAL STORAGE FEATURE	5.2
3.5.7	Control Operations	3.11	5.3 FILE SCAN FEATURE	5.3
3.5.8	Sense Operations	3.11	5.4 TWO-CHANNEL SWITCH FEATURE	5.3
3.5.9	Flag Byte Processing	3.11	5.4.1 Device Reserve Command (1011 0100)	5.4
3.5.10	Index Processing	3.12	5.4.2 Device Release Command (1001 0100)	5.4
3.5.11	Read/Clocking	3.12	5.4.3 Device Status	5.4
3.5.12	Search Operations	3.12	5.4.4 Miscellaneous	5.5
3.5.13	Scan Operations	3.12	5.4.5 Two Channel Switch Circuit Description	5.6
3.5.14	Burst Byte and Exit Decisions	3.12	5.5 RECORD OVERFLOW FEATURE	5.6
3.5.15	Gap Spacing Operations	3.12	5.5.1 Formatting Overflow Records	5.6
3.5.16	End Procedure	3.13	5.5.2 Processing Overflow Records	5.6
3.5.17	Chained Reselection	3.13	5.5.3 Unusual Conditions	5.7
3.5.18	Command Orientation Summary	3.13		
CHAPTER 4	POWER SUPPLIES AND SEQUENCING	4.1	CHAPTER 6 APPENDIX	6.1
4.1	GENERAL POWER SUPPLY DESCRIPTION	4.1	6.1 CAS I	6.1
4.1.1	Power Supply Components	4.1	6.1.1 TROS Bit Assignment Chart	6.1
4.1.2	Thermal Considerations	4.1	6.1.2 Micro Block Symbology	6.3
4.1.3	Marginal Checking	4.1	6.1.3 Sample Usage of Micro Block	6.4
4.1.4	Power Distribution	4.1	6.1.4 Feature Device Command Flow Charts	6.4
4.1.5	Power Interlocks	4.2	INDEX	I.1

1.1 GENERAL INFORMATION

- Provides a method of attaching serial direct access storage units to System/360.
- Up to eight 2841's may be attached to a channel.
- Basic 2841 can control up to eight - 2311 Disk Storage Units.
- Types of units - 2311 (standard) - 2302, and 2321 (optional).
- Any combination of units can be connected to one 2841.
- 2841 uses Solid Logic Technology.
- 2841 uses Read Only Storage for control.

The IBM 2841 Storage Control Unit (SCU) is designed to attach serial direct access storage devices to IBM System/360, Model 30 and above. The SCU provides all the buffering and control necessary to attach these devices to the I/O channels through the standard I/O interface (Figure 1-1).

The 2841 provides the ability to interpret and execute commands, translate data as it moves between the serial-by-bit direct access device and the parallel-by-byte System/360 interface, check the integrity of the information that is transmitted to and from the device, and furnish status information to the using system.

The design of the 2841 is such that circuits common to all direct access devices are housed in one section of the unit while circuits associated with a specific device are housed in a separate area.

The available features for the 2841 Storage Control are:

1. 2311 Attachment (standard part of 2841).
2. 2302 Attachment (Optional).
3. 2321 Attachment (Optional).
4. Additional Storage 2302 (Optional).
5. Two-Channel Switch (Optional).
6. File Scan (Optional).
7. Record overflow (Optional)

2302 Attachment: This feature provides the circuitry required to attach a 2302 Disk Storage to a system via the 2841. This feature is described in Chapter 5.

2321 Attachment: The 2321 Attachment Feature provides the circuitry required to attach a 2321 Data Cell Drive to a system via the 2841. This feature is described in Chapter 5.

Two-Channel Switch: The Two-Channel Switch Feature provides the switching circuitry required to attach the 2841 Storage Control to a second channel. This feature is described in Chapter 5.

Additional Storage: The Additional Storage Feature provides circuitry to attach up to 16 access mechanisms to a 2841. The additional eight access mechanisms must be 2302 accesses. This feature is described in Chapter 5.

File Scan: The File Scan Feature provides an automatic rapid search for a specific identifier condition. This feature is described in Chapter 5.

Record Overflow: The Record Overflow Feature allows a record to overflow from one track to another. This feature is described in Chapter 5.

As the 2311 Disk Storage is the standard unit, this manual is primarily written for 2311 operations. The other units and additional features are described in Chapter 5.

The 2841 is packaged in Solid Logic Technology and utilizes Read Only Storage (ROS) to control its operations.

The use of disk storage provides IBM System/360 with the ability to either sequentially or randomly record and retrieve externally stored data. It permits the immediate access to specific areas of information without the need to sequentially examine all data recorded in the same file. The fast speed of access to data storage locations enables the user to maintain up-to-the minute files and to make frequent direct reference for the retrieval of stored data, regardless of the time of record insertion or the physical location of the data.

The extensive data storage capacity, swift access to recorded data, high data transmission rates, and broad flexibility of file maintenance and organization provided by disk storage devices introduce new and advanced data processing methods and faster simplification of procedures.

1.2 PHYSICAL DESCRIPTION

The physical characteristics of the 2841 are: (Figures 1-2 through 1-10.)

1.2.1 Dimensions

Height	60" (from floor)
Depth	30"
Width	44"
Weight	800 lbs.

Two swinging covers in front and two swinging covers in back.

1.2.2 Power Requirements

Voltage:	3-phase 208 vac $\pm 10\%$, 30 amp, 60-cycle, four wire cable (fourth wire is equipment ground)
Plug:	Russell & Stoll FS 3760
Mating Connector:	FS 3934
KVA:	1.9

NOTE: The 2841 can be adapted to operate on the following 50-cycle, 3 phase voltages in accordance with IBM Corporate Standard 3-2-5103-0:

1. 195 volts $\pm 10\%$
2. 220/380 volts $\pm 10\%$
3. 235/408 volts $\pm 10\%$

1.2.3 Cable Entry

Power and signal cables enter the unit from underneath. A raised floor is desirable but not required.

1.2.4 Operator's Position

The control unit has no operator's position other than the Meter Enable switch on the front of the 2841 (Figure 1-2).

1.2.5 Environmental Conditions

	<u>Operating</u>	<u>Non-Operating</u>
Temperature	60-90°F	50-110°F
Relative Humidity	8-80%	8-80%
Maximum Wet Bulb	78°	80°

1.2.6 Power Control

The control unit may be placed in a local or remote mode by means of a switch in the control unit. When in the remote mode, power sequencing is controlled by the processor. When in the local mode, the power switches in the control unit must be operated. In this mode the processor cannot control sequencing. The switch is normally in the remote position. When power is present in the control unit, it is available to all devices attached to the unit.

1.3 FUNCTIONAL DESCRIPTION (Figure 1-11)

- The 2841 consists of six logical sections:
 1. System/360 Channel Interface
 2. Arithmetic/Logical Unit
 3. Serializer/Deserializer Unit
 4. Fourteen General Purpose Registers
 5. Transformer Read-Only Storage Unit
 6. Device Interfaces
 - a. 2311 Disk
 - b. 2302 Disk
 - c. 2321 Data Cell Drive

1.3.1 System/360 Channel Interface

The System/360 Channel interface provides a method of attaching I/O control units to System/360 channels.

1.3.2 Arithmetic/Logical Unit (ALU)

ALU can add, subtract, OR, AND, exclusive OR, and generate correct parity.

1.3.3 Serializer/Deserializer Unit (SERDES)

SERDES is used to convert parallel-by-byte data to serial-by-bit data when writing, and serial-by-bit data to parallel-by-byte data when reading.

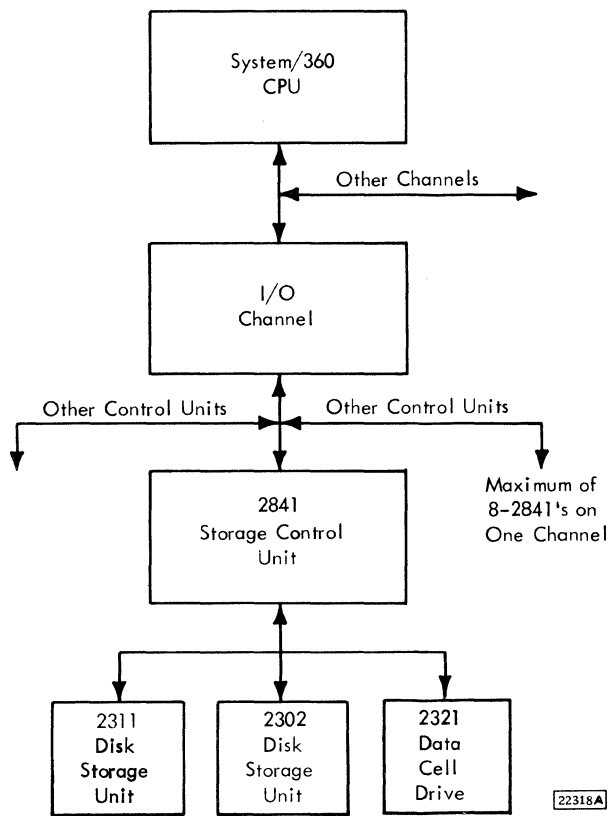
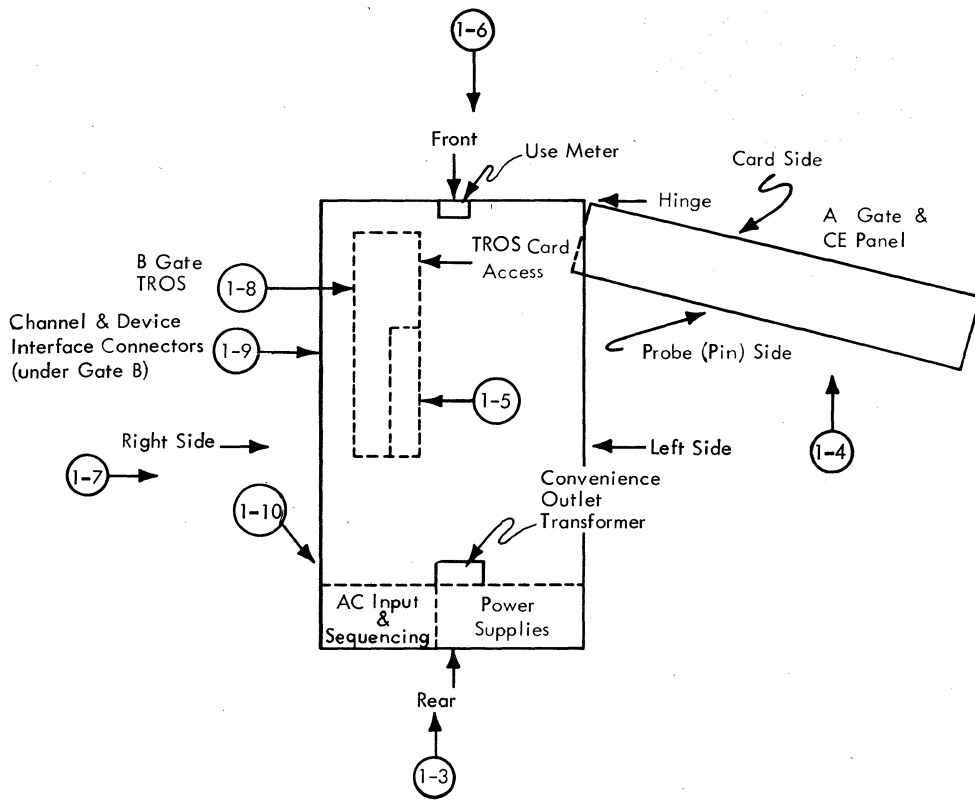


Figure 1-1. 2841 Storage Control Unit Configuration



○ = Refer to Designated Picture For View of 2841

22342A

Figure 1-2. Top View of 2841

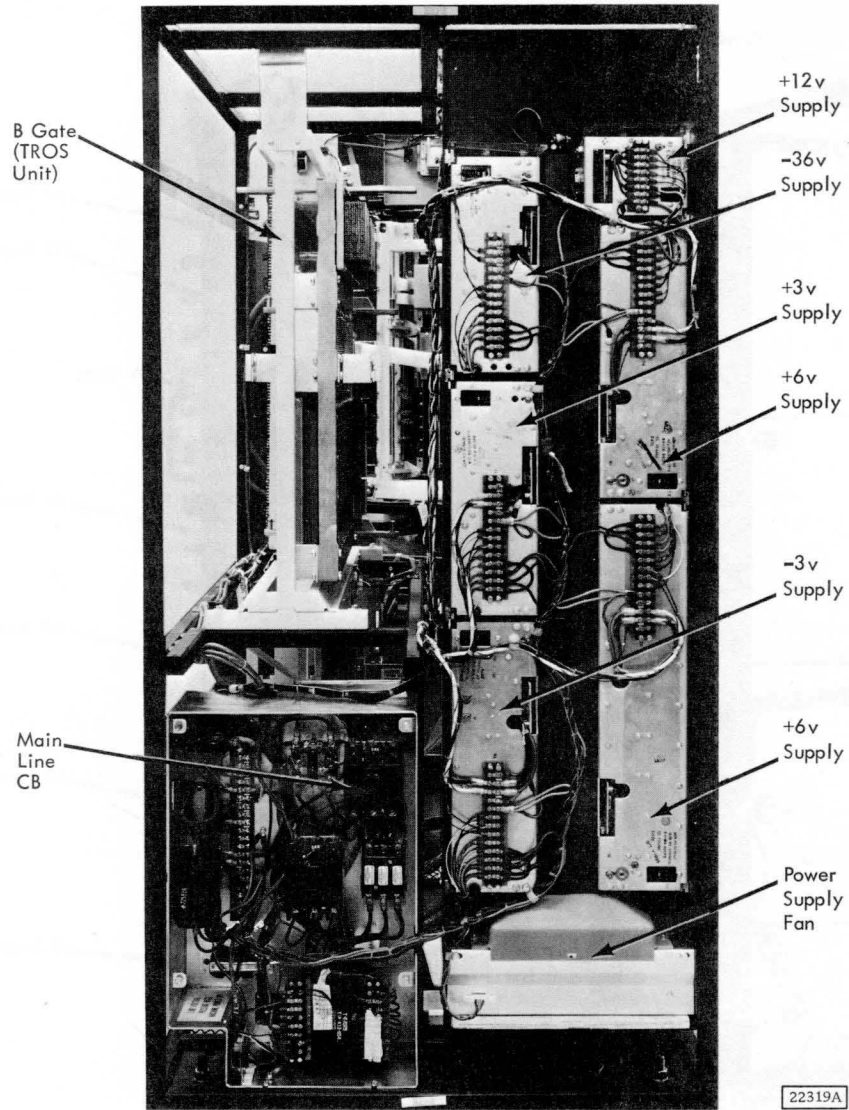


Figure 1-3. Rear View of 2841

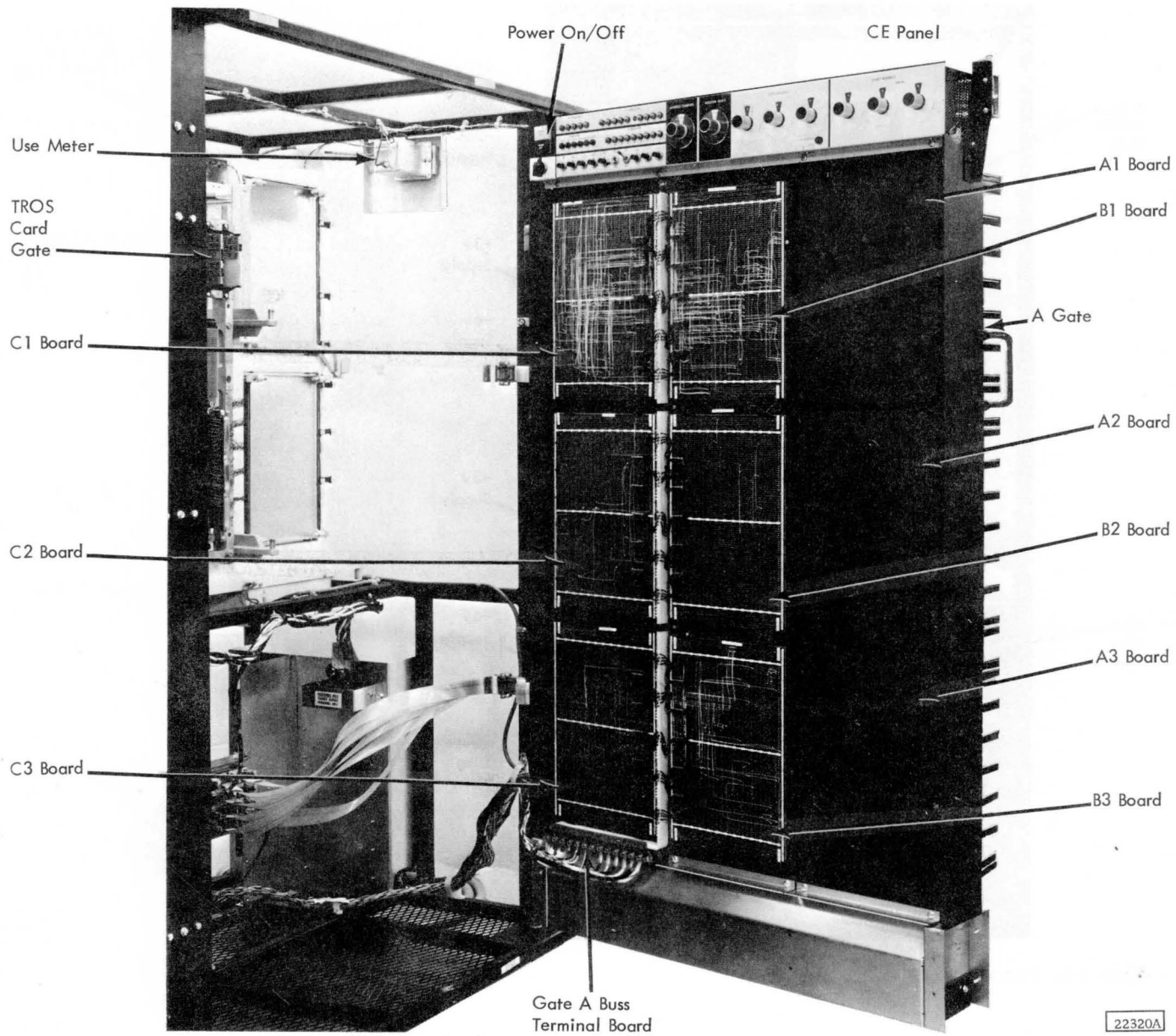


Figure 1-4. Gate A and CE Panel

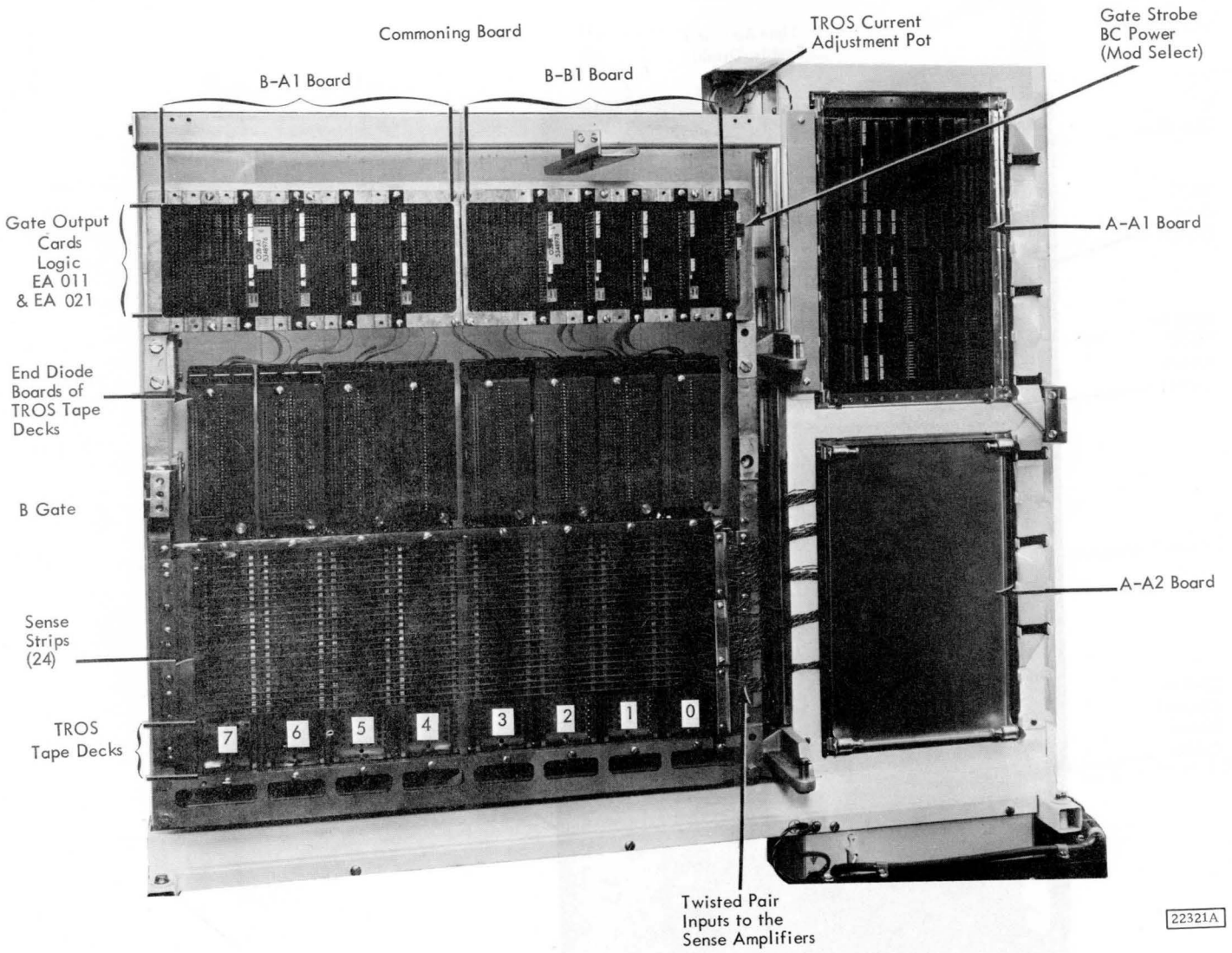


Figure 1-5. Right Side View of 2841 TROS Unit

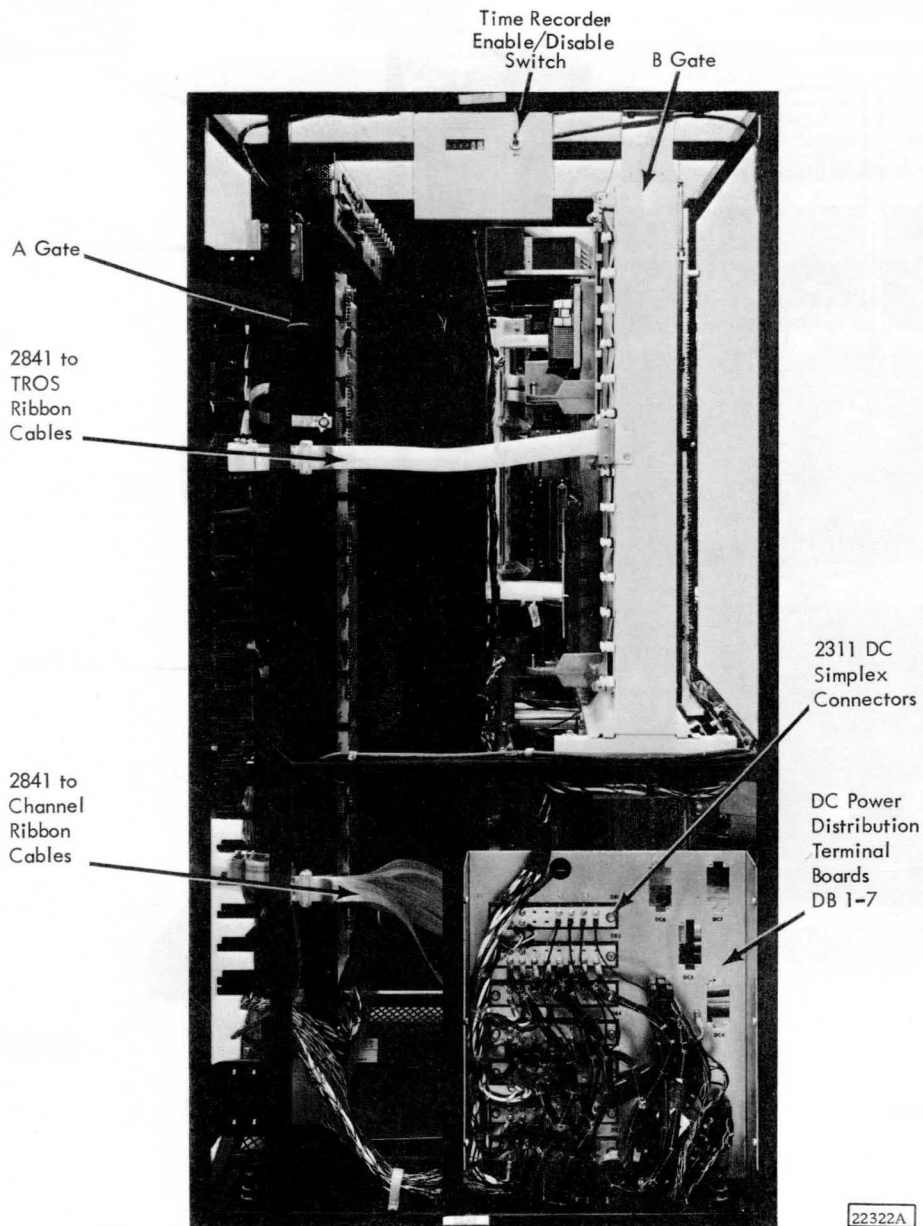


Figure 1-6. Front View of 2841

Gate B (TROS)

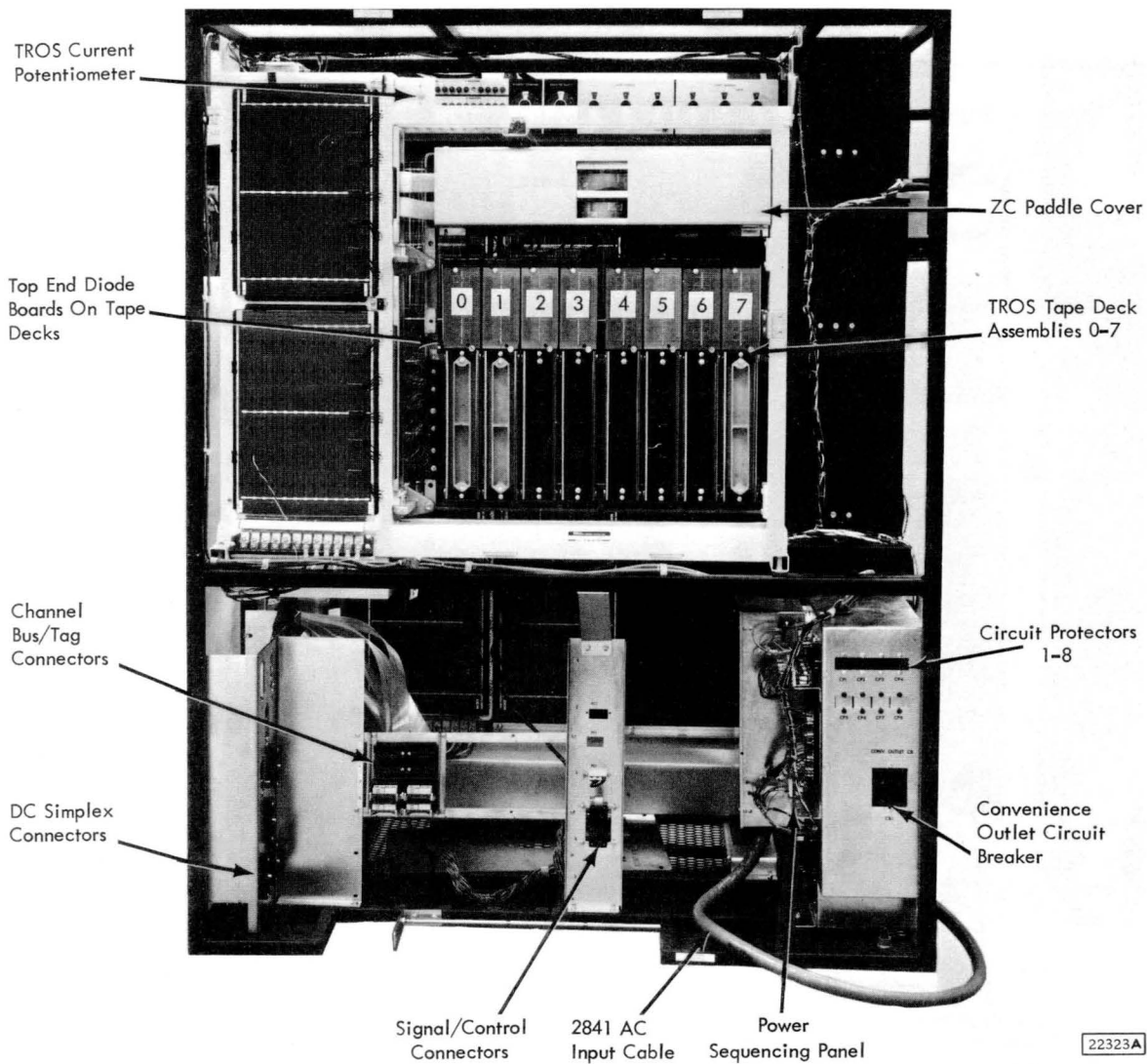


Figure 1-7. Right Side View of 2841

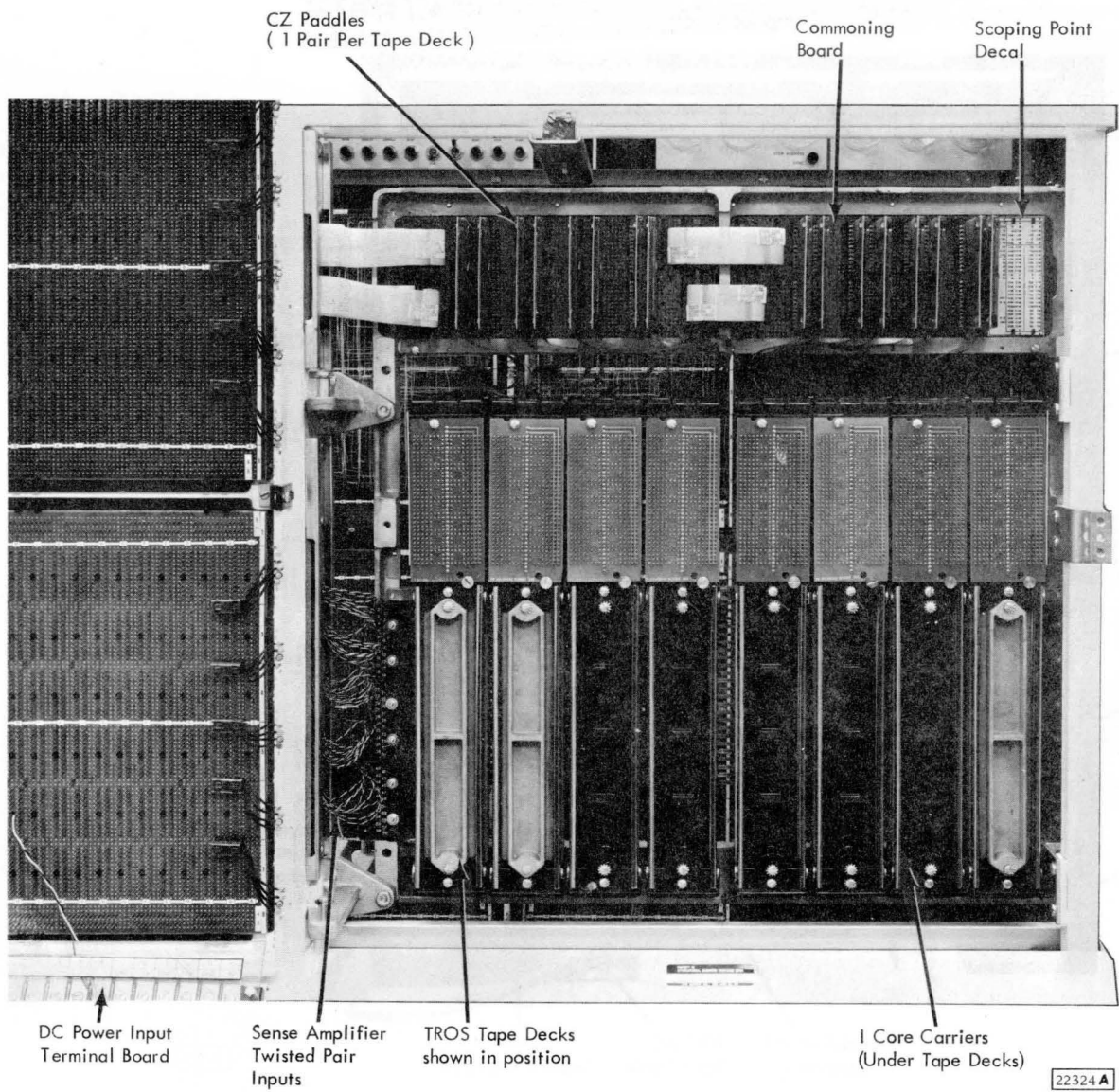


Figure 1-8. 2841 TROS Unit - Tape Deck Side

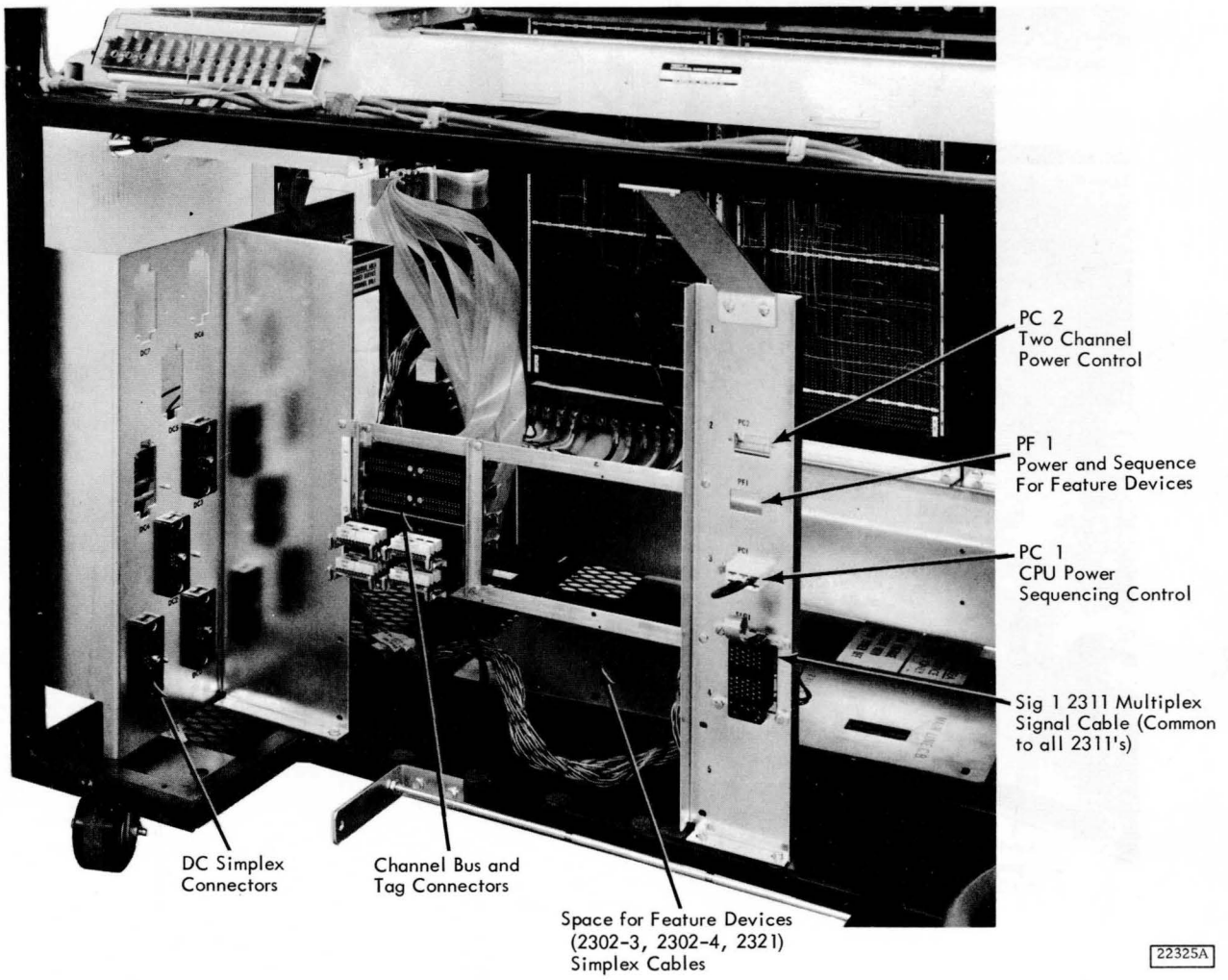
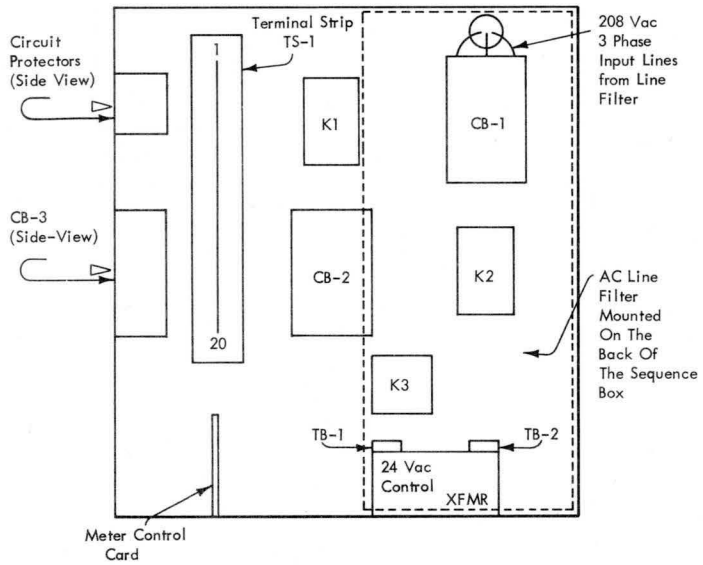
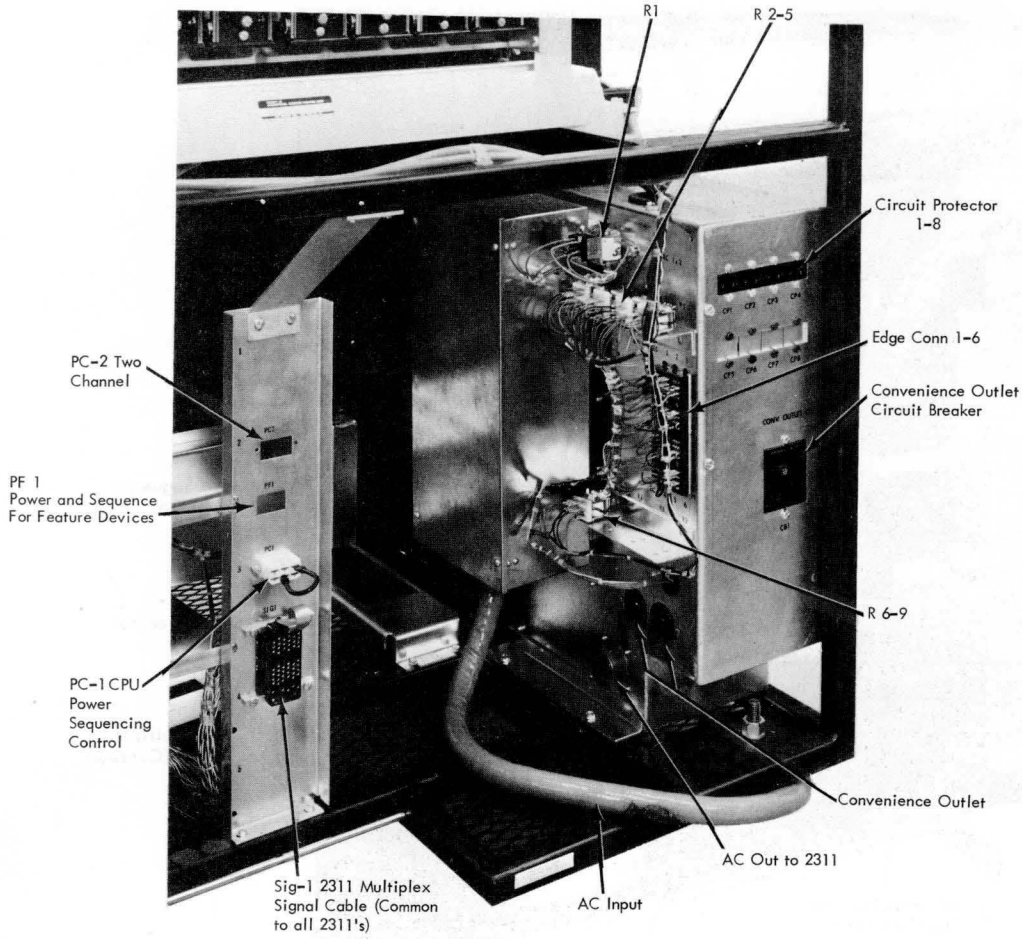
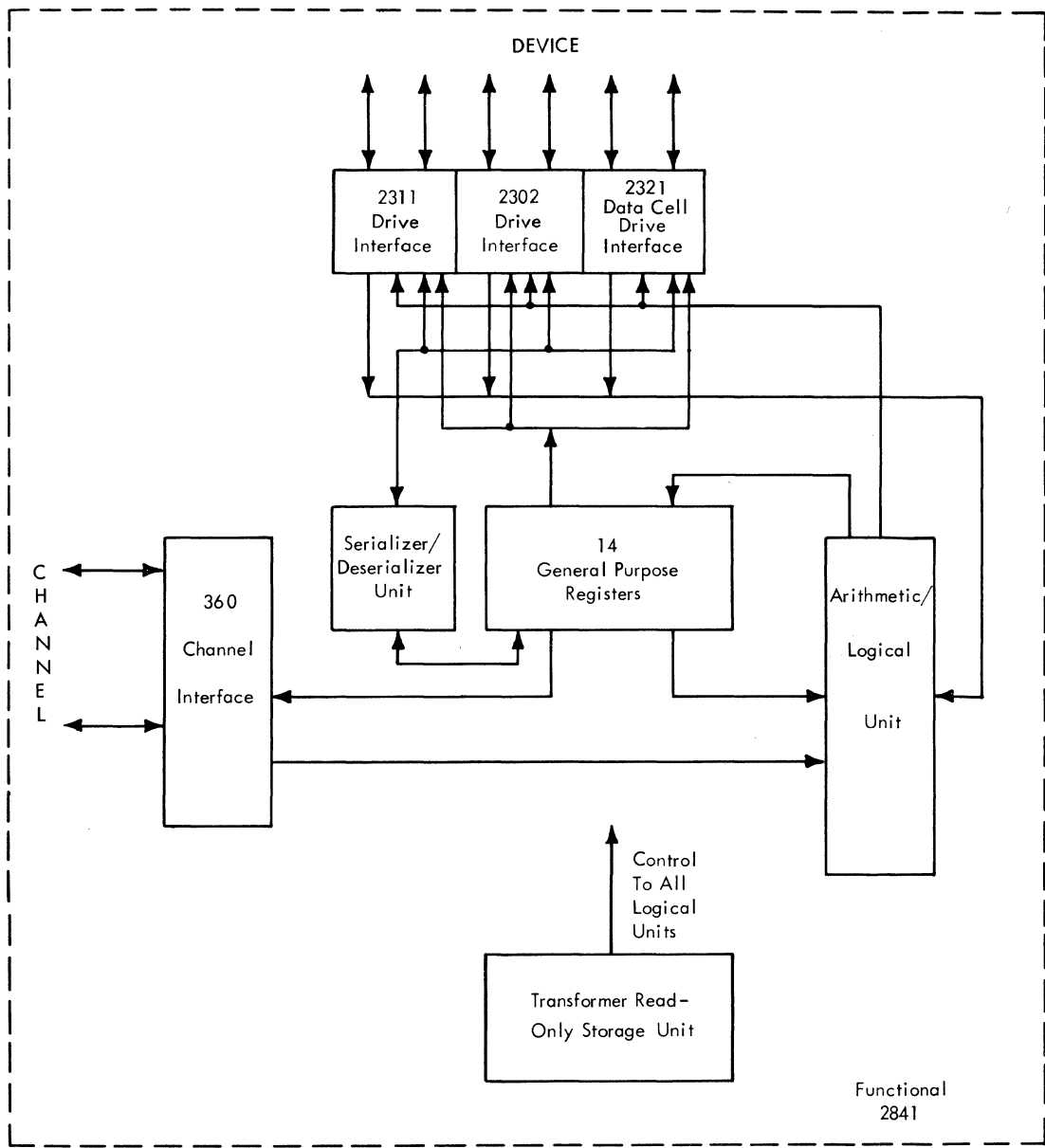


Figure 1-9. 2841 Device/Channel Cabling



22326 A

Figure 1-10. Power Sequencing Panel Area



22327A

Figure 1-11. Functional Data Flow

1.3.4 General Purpose Registers

There are 14 general purpose registers within the 2841. They are used for various purposes by the microprogram. A more detailed description of the usage of these registers is included in Chapter 3.

1.3.5 Transformer Read-Only-Storage (TROS)

TROS consists of 2,048 addressable words. Each word is 48 bits in length and is one step in a sequence of words called a microprogram. The TROS storage cycle is 500 ns. TROS furnishes control for all logical units within the 2841. A more detailed description of TROS is included in Chapter 2.

1.3.6 Device Interfaces

The device interfaces contain data and control lines unique to a particular device type.

1.3.7 Basic Write Data Flow

1. A byte of data is requested from channel by the channel interface.
2. Channel places the byte on the bus-out lines and notifies the channel interface that the data is ready.
3. The byte is transferred from the channel interface through ALU (No arithmetic operation is performed on it.) to one of the general purpose registers.
4. The byte is transferred from the general purpose register to SERDES.
5. SERDES converts the parallel-by-byte data to serial-by-bit data, and sends this data through the device interface to the device.
6. Each of these operations is under control of TROS except for the parallel to serial conversion within SERDES.

1.3.8 Basic Read Data Flow

1. Serial-by-bit data from the device is read-in through the device interface and sent to SERDES.
2. SERDES converts the serial-by-bit data to parallel-by-byte data.
3. When SERDES has a complete byte (8 bits), the byte is transferred to one of the general purpose registers. TROS is notified of this transfer.
4. The byte is transferred from this general purpose register through ALU to another general purpose register. Correct parity is generated when the byte is transferred through ALU.

5. The channel interface notifies the channel that the 2841 has a byte ready for transfer.
6. When the channel is ready to receive the byte, the channel interface is notified and the byte is placed on the Bus In lines.
7. The channel takes the byte and notifies the 2841 of this action.

1.4. TRACK FORMAT

- A track consists of these areas and records:
 1. Home Address
 2. Record Zero
 3. One or more variable length data records
- An Index Marker indicates the physical beginning of each track.
- Record Zero (Track Descriptor Record) has been designed for a special purpose - Flagging.
- An Address Marker designates the beginning of data records.
- Each record is self-formatting. That is, it contains information defining the length of the records.
- Each record contains:
 1. Count area
 2. Data area
 3. Possibly a key area.
- Two areas facilitate the finding of data: Identifier (part of count) and Key Area.

The following information concerning track format (Figure 1-12) pertains to the 2311 drive. However, all units which attach to the 2841 use basically a common track format differing mainly in the maximum capacity of an individual track.

1.4.1 Index Marker

The index marker (IX) indicates the physical beginning of each track. All tracks use the same index marker.

1.4.2 Home Address Area

The home address area (HA) consists of seven bytes which define track condition and the physical location within the storage device. There is one HA area per track. This must be the first area written on each

track and is created by a write HA operation. Contained within HA are five data bytes.

Byte	Name	Bits	Function
1	Flag	0-5	No purpose - always zero
		6	Track Condition 0 - good track 1 - defective track
		7	Track Use 0 - primary track 1 - alternate track
2,3	Cylinder**	All	Specifies cylinder address
4,5	Head**	All	Specifies head address
6,7	Code Check	All	Error detection

Example: Assume the track is good, the cylinder is 173, the head is 3. Then the HA area equals:

```

F  C  C  H  H  CC  CC
0  0  173  0  3  *  *

```

*Value assigned by microprogram during a write HA operation

**There is a requirement that the data recorded in the cylinder and head bytes agree with the physical address of the track. The requirement is that the HH bytes must differ by one in ascending sequence from surface to surface.

1.4.3 Track Descriptor Record (R0)

The first record following home address on each track is the track descriptor record (record zero). It is created by a write R0 operation. Although it may be used to store data, R0 has been designed to enable an entire track's data to be moved to an alternate track if a portion of the recording surface becomes defective. This process is called "flagging" and is described in Chapter 3.

Contained within R0 are a count area and a data area. Although a key area may be included, IBM Programming Systems do not require a key area in R0.

1.4.3.1 Count Area

This area is always 11 bytes in length. It can be divided into four logical sections.

1. Flag, Byte 1. This byte is generated by the microprogram as R0 is written. Bits 0-5 equal zero. Bits 6 and 7 are propagated from bits 6 and 7 of the HA flag byte.
2. Identifier (ID), Bytes 2-6. This section is composed of five bytes—cylinder, cylinder, head, head, record number (CCHHR). (CCHH) is normally identical to the (CCHH) recorded in the HA Area. (R) is the record number of this record. In the case of R0, the record byte is always zero.

Basically, the user has two ways in which to locate data. One of these is by searching for a particular ID, that is, a particular (CCHHR). Therefore, the purpose of the ID section of a count area is to furnish the user a method for locating the desired information. The second method is searching for a particular key area.

3. Format, Bytes 7-9. On some previous disk storage systems, records were of fixed length (1401-1311), or a separate track (format track) was used (7631-1301) to describe the length of a record. Records on devices attaching to the 2841 can be of variable lengths, therefore, some method was needed to define these record lengths. Bytes 7, 8, and 9 of each count field fully describe the record length as follows:

Byte 7—Key Length (KL). This byte defines the number of bytes (excluding code check bytes) in the key area. If the record has no key area, the KL byte is zero. KL can indicate a key length of 0 to 255 bytes. Normally for R0, the byte is 0.

Bytes 8 and 9—Data Length (DL). These two bytes define the number of bytes (excluding code check bytes) in the data area. Two bytes (16 bits) can indicate a data length of 0 to 65,535 bytes.

Zero data length indicates an end-of-file record. This may be used for any purpose by the user. The maximum quantity appearing in these two bytes for a 2311 is 3625.

4. Code Check—Bytes 10 and 11. Used for error detection.

1.4.3.2 Key Area

The use of a key area in R0, is at the discretion of the programmer. Standard use of R0 by IBM Programming Systems does not include a key area.

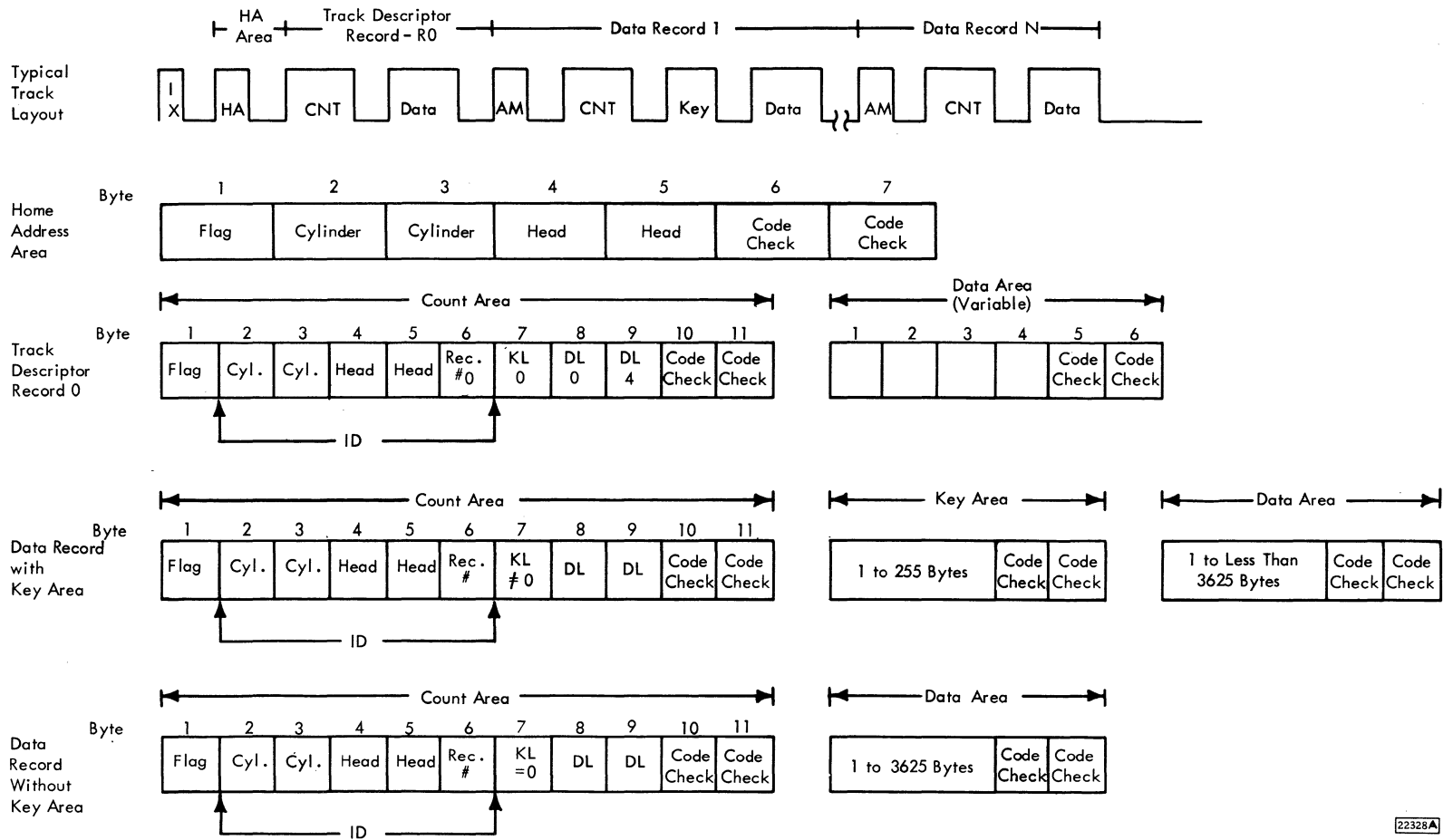


Figure 1-12. 2841 and 2311 Data Track Format

22328A

Refer to Data Record Key Area for a description of key area.

1.4.3.3 Data Area

The length and content of the data within R0 is dependent upon the type of IBM Programming System used.

In Figure 1-12, the data area is four plus two code check bytes long.

In Figure 1-12 if the track is good, the four data bytes contain the same information as is recorded in CCHH of the R0 count area.

If the track is bad, the four data bytes contain the cylinder and head address of the alternate track. Refer to Flagging in Chapter 3, for a more detailed description of this process.

Code check bytes are recorded at the end of the data area for error detection.

1.4.4 Data Record

One or more data records may follow R0 on a track. Count areas make each record self-formatting for maximum data organization and flexibility. Before each data record is an address marker area, a count area and a data area. Depending upon the type of file organization, there may be a key area between count and data areas.

1.4.4.1 Address Marker

This 3-byte area indicates the beginning of each data record. Address markers are written by the 2841 as data records are created. They are used by the 2841 to locate the beginning of a record for searching, writing, and reading operations. This allows the 2841 to begin an operation anywhere on the track instead of at index point.

1.4.4.2 Count Area

This 11-byte area describes the key and data areas which follow. Bytes 2-9 are created in the CPU by the program used to write the record.

Flag: Byte 1 of the count area is generated by the 2841 as each record is written. It is not sent from the CPU.

Bit	Function
0	0 for even-count records (R ₀ , R ₂ , R ₄ , R ₆). 1 for odd-count records (R ₁ , R ₃ , R ₅). Used by the 2841 to ensure that all address markers (and records) are present. The 2841 signals a missing address marker when two consecutive, identical bits are encountered (unless an index point intervenes).
1	Used with Record Overflow feature. 0 for all non-overflow records and for the last record of an overflow chain. 1 for each record except the last segment of an overflow record.
2	Zero
3	Zero
4	Zero
5	Zero
6	Track Condition 0 indicates operative track 1 indicates defective track
7	Track Use 0 indicates primary track 1 indicates alternate track

Bits 6 and 7 are propagated from the flag byte of the preceding record.

Cylinder - Bytes 2 and 3 contain the cylinder number of the track on which the data is stored.

Head - Bytes 4 and 5 contain the read/write head number of the track on which the data is stored. Generally the cylinder and head information are identical to the cylinder and head information recorded in the HA Area.

Record Number - Byte 6 designates the sequential number of the record on the track.

Key Length - Byte 7 specifies the number of bytes in the Key Area. This may vary from 0 to 255 bytes (0 meaning no Key Area).

Data Length - Bytes 8 and 9 specify the number of bytes in the Data Area. This may vary from 0 to 3625 bytes for a 2311.

Cyclic Code Check - Bytes 10 and 11 are used for error detection. See Error Detection.

1.4.4.3 Key Area

As mentioned previously, the user has two ways of locating his data, one of which is searching for a particular ID (CCHHR).

Another way of locating data is by searching for a particular key area. The key area length ranges from 1 to 255 bytes. The key area could contain identifying information about a record, such as serial number, social security number, policy number, etc.

Cyclic code check bytes are recorded at the end of the key area for error detection.

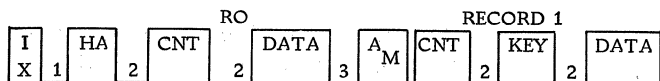
1.4.4.4 Data Area

This area contains the information identified by the count (ID) and key areas. This area may vary in length from 1 to 3625 bytes for a 2311.

Cyclic code check bytes are recorded at the end of the data area for error detection.

1.4.5 Gaps

Gaps are used to separate records and areas within records on the tracks. There are three types of gaps.



Gap 1 - The gap between index and the HA area. A fixed length-36 bytes. This gap is referred to as the HA gap.

Gap 2 - The gap between the end of HA and R0 count field. Also the gap between areas of a record. Fixed length-18 bytes. This gap is referred to as the alpha (α) gap.

Gap 3 - The gap between the end of the data area of one record and the beginning of the count area of the next record. Variable length-27 bytes plus 5% of the sum of the previous records key and data length. This gap is referred to as the beta (β) gap. The beta gap also contains two address mark bytes.

A more detailed description of the contents of these gaps is in Chapter 2, under the heading - Serializer/Deserializer Unit.

Gap size and byte contents vary with the feature devices (refer to Chapter 5).

1.4.6 Error Detection

As information is being transferred from the parallel-by-bit using system to the serial-by-bit device (write), the 2841 strips off the parity bit associated with each byte. Parity bits are not recorded on the storage devices. For transfer to the channel (read) the 2841 assembles the serial-by-bit device data into a parallel-by-bit byte, adds a parity bit, and transmits the complete byte to the using system.

In the serial/direct access storage devices, checking the validity of the recorded information is accomplished by adding a string of 16 bits (two bytes) to the end of each area. This type of checking is called cyclic code checking.

Code checking is accomplished by first filling two 1-byte registers with all bits. Then each character read or written is exclusive ORed to one of the two registers. All even numbered characters go to the same register and all the odd characters go to the other. The final result is two "hash" total characters. These are used as the two code check characters.

For a write operation the two bytes of cyclic check code are added to the end of the record and written on the track.

On a read operation, the process is continued until the cyclic code bytes on the end of the record are operated upon. If no error has occurred, the result is all zeros in the cyclic code check registers.

Example: Write

	Register 1
Set to ones	1 1 1 1 1 1 1 1
1st Char.	<u>1 1 1 1 0 0 0 1</u>
Result	0 0 0 0 1 1 1 0
3rd Char.	<u>1 1 1 1 0 0 1 1</u>
Result	1 1 1 1 1 1 0 1

Code Check byte one

Register 2

Set to ones	1 1 1 1 1 1 1 1
2nd Char.	<u>1 1 1 1 0 0 1 0</u>
Result	0 0 0 0 1 1 0 1
4th Char.	<u>1 1 1 1 0 1 0 0</u>
Result	1 1 1 1 1 0 0 1

Code Check byte two

Example: Read

Register 1

Set to ones	1 1 1 1 1 1 1 1
1st Char.	<u>1 1 1 1 0 0 0 1</u>
Result	0 0 0 0 1 1 1 0
3rd Char.	<u>1 1 1 1 0 0 1 1</u>
Result	1 1 1 1 1 1 0 1
Code Check one	<u>1 1 1 1 1 1 0 1</u>
Result	0 0 0 0 0 0 0 0

Register 2

Set to ones	1 1 1 1 1 1 1 1
2nd Char.	<u>1 1 1 1 0 0 1 0</u>
Result	0 0 0 0 1 1 0 1
4th Char.	<u>1 1 1 1 0 1 0 0</u>
Result	1 1 1 1 1 0 0 1
Code Check two	<u>1 1 1 1 1 0 0 1</u>
Result	0 0 0 0 0 0 0 0

The cyclic code check used in the 2841 has the following checking properties:

1. Detects all errors in which an odd number of bits is wrong.
2. Detects single bursts of errors that are 16 bits or less in length.

1.5 PROGRAMMING

Refer to SRL, Form Number A26-5988 for input/output operations and programming of the 2841.

A summary of the 2841 operation codes is included in table 1.

SYSTEM/360 I/O INTERFACE

1.6 CHANNEL INTERFACE INTRODUCTION

- The IBM System/360 Interface:
 1. Provides a method of attaching I/O units to the IBM System/360.

2. Consists of 34 lines.
3. Accommodates up to eight control units.

The input-output interface provides a uniform method of attaching input/output (I/O) control units to IBM System/360 channels. The interface can accommodate up to eight control units with addressing capabilities for up to 256 I/O devices.

The interface establishes requirements for signal transfers between control units and the servicing channel. Therefore, interface lines provide a common information format and signal sequence for all input/output devices. Figure 1-13 categorizes interface lines according to their general functions.

Except for signals that establish priority among control units, all interface signals are sent over a common bus. Any interface signal that the channel generates is available to all control units, but, only one control unit at a time is logically connected to the interface. After a control unit is selected, it remains logically connected to the interface until the control unit transmits or receives the required information or until the channel signals the control unit to disconnect.

The rise and fall of signals transmitted over the interface are interlocked with the corresponding responses. This interlocking makes the interface applicable to a wide variety of circuits and data rates, and permits the connection of control units of different circuit speeds.

Each control unit contains an address card that designates its interface address; no two control units on the same interface can have identical addresses. To begin an I/O operation, the channel must transmit the address of the desired unit.

Interface adapter circuits located in each control unit:

1. Convert interface line sequences and coded commands to the control lines necessary to operate the control unit.
2. Establish communication between the control circuits in the unit and the interface.

1.7 INTERFACE LINES

- Interface lines are divided into five types:
 1. Bus lines.
 2. Scan controls.
 3. Tag lines.
 4. Interlock lines.
 5. Special controls.

Figure 1-14 shows channel and control unit connections to the interface. Observe that the select

lines (select-out and select-in) connect serially through each control unit for the purpose of establishing priority; other lines connect in parallel.

1.7.1 Bus Lines

- Bus lines carry information between the channel and control unit.
- There are nine bus-in lines and nine bus-out lines.

Information is transmitted over the interface from the channel to the control unit on bus-out, and from the control unit to the channel on bus-in. Bus-in and bus-out each contain eight information lines and one line for odd parity.

Information on the in and the out bus is arranged so that bit position 7 of a bus always carries the lowest-order bit within an eight-bit byte. The highest-order bit is in position 0.

1.7.1.1 Bus-Out

- Bus-Out transfers information from the channel to the control unit.
- There are eight data lines and one parity line.

The nine bus-out lines transfer information from the channel to control units. The channel conditions an outbound tag line to identify the type of data transmitted on bus-out lines. For example, when the address-out tag and bus-out lines are active concurrently, information on bus-out lines designates an address.

Tag lines control the period during which bus-out lines contain valid information. When transferring the address of an I/O device, information on bus-out lines is valid from the rise of address-out to the rise of one of the following: operational-in, select-in, or status-in. When transferring information other than an address, signals on bus-out lines are valid from the rise of the identifying outbound tag to the fall of the responding inbound tag.

1.7.1.2 Bus-In

- Bus-In transfers information from the control unit to the channel.
- There are eight data lines and one parity line.

The nine bus-in lines transfer information from the selected control unit to the channel. The control

unit conditions an inbound tag line to identify the type of information transmitted on bus-in lines. For example, when the status-in tag and bus-in lines are active concurrently, bus-in lines contain a status byte.

Tag lines control the period during which bus-in lines contain valid information. Signals on bus-in lines are valid 100 nanoseconds (ns) after the rise of the identifying inbound tag to the rise of the responding outbound tag.

1.7.2 Scan Controls

- Select-out, hold-out, and select-in are controlled by the channels. Request-in is controlled by the control unit.
- The scan controls are independent of CPU non-I/O operations.
- Scan controls enable the channel to contact control units attached to it.
- Scan controls permit control units to request service from the channel.
- Scan controls establish contact between the channel and the control units on a priority basis.

1.7.2.1 Select-Out

- Select-out connects each control unit in series.
- It determines the priority of control units.

The select-out lines provide the loop that allows the channel to interrogate each control unit in priority sequence.

Logically, the select-out line connects serially through each control unit by connecting:

1. The channel to the control unit having the highest priority.
2. A control unit to the next control unit in descending priority sequence.

The physical location of a control unit (with respect to the channel) does not establish the unit's designated priority. For example, the control unit farthest from the channel might be the first unit to which select-out logically connects; this unit would then be the unit to which the highest priority is assigned.

When an I/O control unit receives the select-out signal it must either raise its operational-in line in response to it (request service) or immediately propagate the select-out signal to the next control unit in

Table 1. Bit Structure of 2841 Op Codes

	0	1	2	3	4	5	6	7
	M/T	HI	=	C	K	D	CHANNEL	
Write Data	0	0	0	0	0	1	0	1
Write Key, Data	0	0	0	0	1	1	0	1
Write Count, Key, Data	0	0	0	1	1	1	0	1
Write Home Address	0	0	0	1	1	0	0	1
Write R0	0	0	0	1	0	1	0	1
Control Erase	0	0	0	1	0	0	0	1
Search Equal ID	-	0	1	1	0	0	0	1
Search Equal Key	-	0	1	0	1	0	0	1
Search Equal Home Address	-	0	1	1	1	0	0	1
Search Equal Key, Data	-	0	1	0	1	1	0	1
Search Hi ID	-	1	0	1	0	0	0	1
Search Hi Key	-	1	0	0	1	0	0	1
Search Hi Key, Data	-	1	0	0	1	1	0	1
Search Hi Equal ID	-	1	1	1	0	0	0	1
Search Hi Equal Key	-	1	1	0	1	0	0	1
Search Hi Equal Key, Data	-	1	1	0	1	1	0	1
Read Data	-	0	0	0	0	1	1	0
Read Key, Data	-	0	0	0	1	1	1	0
Read Count, Key, Data	-	0	0	1	1	1	1	0
Read Home Address	-	0	0	1	1	0	1	0
Read R0	-	0	0	1	0	1	1	0
Read Count	-	0	0	1	0	0	1	0
Read Initial Program Load (IPL)	0	0	0	0	0	0	1	0
Control Seek (BBCHH)	0	0	0	0	0	1	1	1
Control Recalibrate	0	0	0	1	0	0	1	1
Control Restore	0	0	0	1	0	1	1	1
Control Space Count	0	0	0	0	1	1	1	1
Control No Op	0	0	0	0	0	0	1	1
Control Cyl. Seek (CCHH)	0	0	0	0	1	0	1	1
Control Head Seek (HH)	0	0	0	1	1	0	1	1
Control Set File Mask	0	0	0	1	1	1	1	1
Test I/O	0	0	0	0	0	0	0	0
Sense I/O	0	+	+	+	0	1	0	0
Write Spec-Count, Key, and Data (used with Record Overflow)	0	0	0	0	0	0	0	1
Reserved	0	0	1	0	0	0	1	1

Note: On Search and Read commands B0 can be either 0 or 1. If "0", head switching will not take place when Index Point is detected. If 1, head switching will take place when Index Point is detected. On a Sense Command Bits 1, 2, and 3 of the Code are "don't care" conditions (+).

22329A

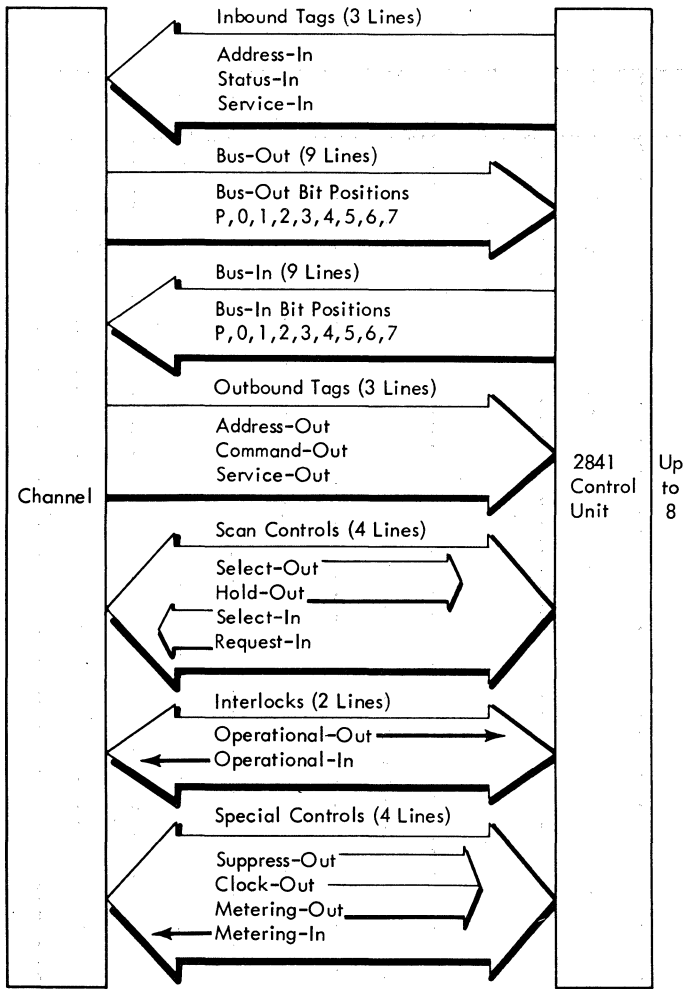


Figure 1-13. Interface Lines

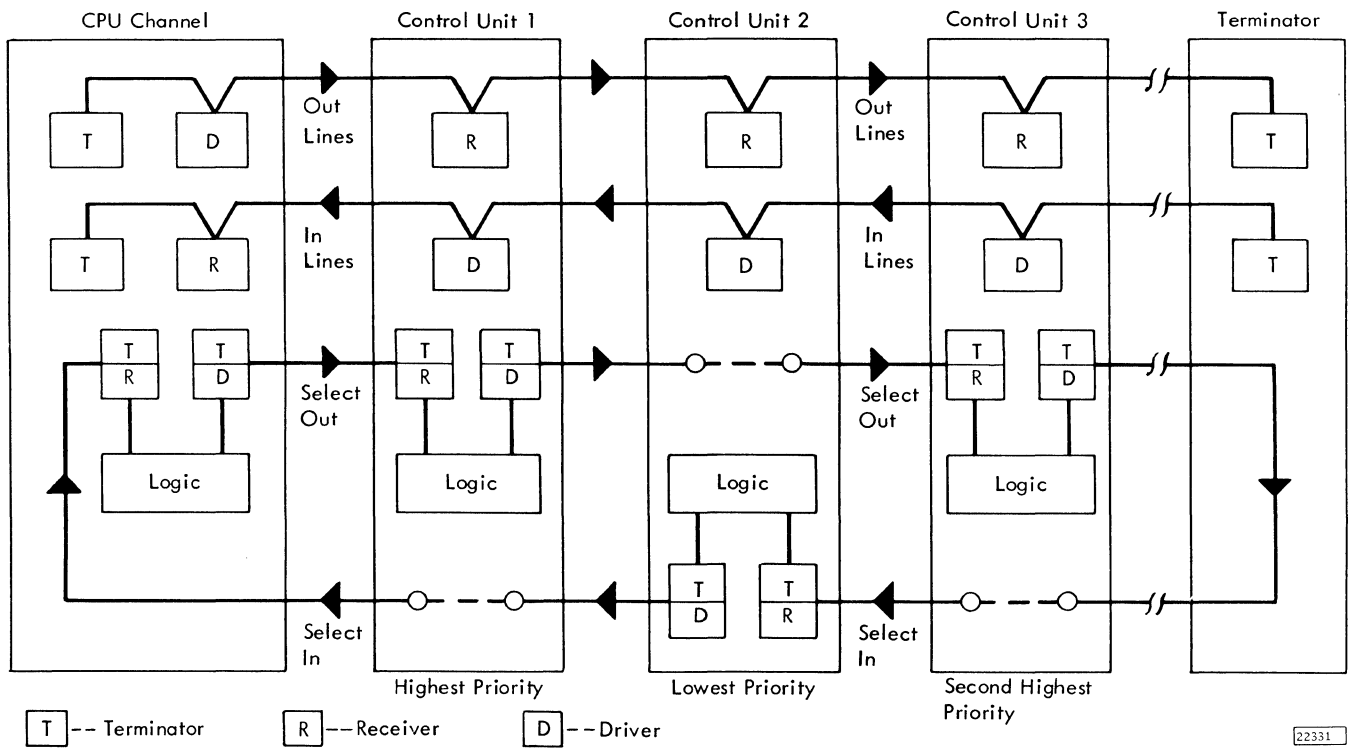


Figure 1-14. Interface Connections

the series. Once a control unit has propagated select-out, it cannot raise its operational-in line until the next incoming select-out line to the control unit rises.

The channel must hold select-out active until it receives a signal on either the select-in or the address-in line. When select-out is transferred to the control unit with the lowest priority, the control unit either 1) raises its operation-in line, and later, its address-in line, initiating a signal sequence with the channel, or 2) sends the incoming select-out to the channel. The signal on the select-out line's return path to the channel is called select-in.

If a control unit conditions operational-in when the incoming select-out is active, it does not transfer select-out to the next control unit (or select-in to the channel). By conditioning operational-in, the control unit interrupts the channel's scan loop. Then, the control unit transmits an address byte on bus-in lines and conditions address-in. The control unit must hold operational-in active until communication with the channel is complete. The channel can drop select-out after receiving address-in, or can hold select-out active through the complete I/O operation. In no case can the control unit cancel operational-in before the channel drops select-out.

1.7.2.2 Select-In

- The select-out line's return path to the channel is select-in.

The control unit provides an option of connecting its selection logic in series on either the select-out or select-in line (Figure 1-14). Descending-order priority from the channel can be established on the select-out line, and the remaining control units can maintain the descending-order priority from the channel on the select-in logic. For clarity, in this manual, the selection logic is assumed to be connected to the select-out line.

Select-in is a line from the lowest-priority control unit to the channel. It is the outgoing select-out line of that control unit and provides a return path to the channel for the select-out signal. The definition of the select-in line is the same as that of a select-out line coming from any control unit.

1.7.2.3 Request-In

- This is a request for service from the control unit to the channel.
- May initiate a polling sequence at the channel.

A control unit conditions the request-in line to indicate that it will initiate a signal sequence when select-out polls that unit again. The channel need not condition select-out to scan the attached control units until the request-in line indicates that a control unit requires servicing. This operation allows the control unit with the highest priority to receive attention in a minimum amount of time after the request-in line is conditioned. To illustrate the function of request-in, consider the following example:

Assume that the highest interface priority is assigned to the I/O device with the highest data rate and that the device with the slowest data rate has the lowest priority. The unit with the lowest priority can wait longest for service; so, each time that the request-in line is conditioned, that unit is the last to be polled. Because the I/O device with the highest priority can wait the least time for service, each request-in indication causes that unit to be polled first.

1.7.2.4 Hold-Out

- Hold-out is used in conjunction with select-out.
- It allows the channel to cancel the effects of select-out and control polling.

The channel conditions the hold-out line to all control units in parallel to allow select-out to perform its designated function in a control unit. The hold-out line allows the channel to cancel the effects of select-out at each control unit at the same time. If the channel is holding select-out active and cancels hold-out, no control unit can make use of select-out; a unit can only propagate the incoming select-out to the next unit. Therefore, the channel receives select-in in the shortest possible time.

1.7.3 Outbound Tag Lines

- These lines carry instructional signals to an attached control unit.
- They identify information on bus-out lines.
- Two out-tags cannot be active at the same time.
- Each line remains active until an inbound tag responds to it.

1.7.3.1 Address-Out

- Address-out normally identifies information on bus-out as an address.

- On a halt-I/O instruction, address-out instructs the control unit on the interface to disconnect.

The channel transmits a signal over the address-out line (Figure 1-15) to indicate either of two conditions:

1. Address-out initiates selection of an I/O device causing all attached control units to attempt to decode the address on bus-out lines. Because each control unit address is different, only one unit can decode the address. If the control unit that recognizes the address is not busy, it must respond by conditioning operational-in when select-out is conditioned to that control unit. Address-out precedes the rise of select-out by at least 400 nanoseconds. The channel must hold address-out active until it receives operational-in, select-in, or status-in. Select-in indicates that no control unit decoded the address. This occurs when the specified control unit is off line. Status-in indicates that the designated control unit is busy and cannot be interrupted to execute another operation. The channel responds to the status-in reply by canceling select-out. It then waits for status-in to fall and cancels address-out.
2. On a Halt I/O instruction, address-out instructs the control unit on the interface to disconnect. If the unit is selected, the channel will:
 - a. Condition the select-out line (may already be up).
 - b. Receive operational-in from a control unit, (will already be up).
 - c. Condition the address-out line.
 - d. Cancel select-out and hold address-out active until the control unit allows operational-in to fall.

The control unit must cancel operational-in within 6 microseconds (μsec) after receiving the interface disconnect indication. The I/O operation proceeds to the normal end, but the data is not transferred across the interface.

1.7.3.2 Command-Out

- This indicates a command byte on bus-out in response to address-in during channel initiated selection.
- It means "proceed" in response to address-in during control unit initiated selection.
- It causes the control unit to stack the status-in response to status-in.
- It means "stop" in response to service-in.

The channel conditions the command-out line (Figure 1-16) to respond to a signal on an inbound tag line. During the initial selection sequence, the channel activates command-out to reply to address-in, indicating that a command byte is on bus-out lines. This command byte specifies the I/O operation to be performed. Only at this point in the initial selection sequence does command-out cause the selected control unit to decode the byte on bus-out lines.

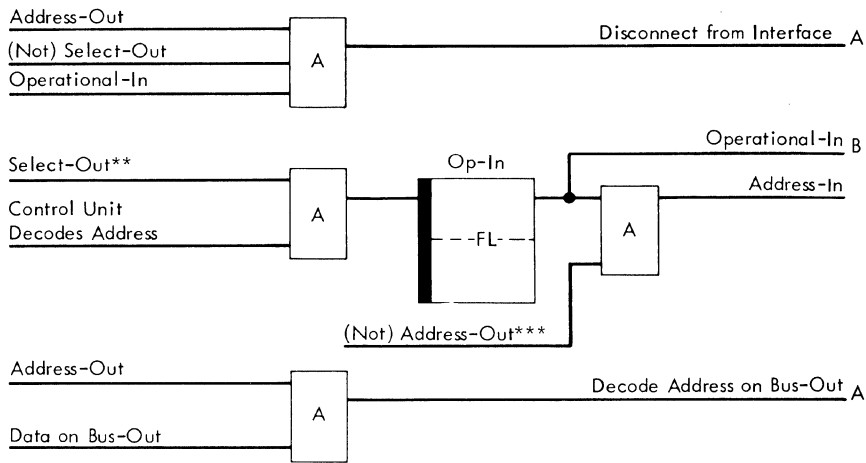
A command-out response to service-in means "stop" and causes the control unit to terminate the data transfer. Whether during the initial selection sequence or at the end of the operation, the command-out reply to status-in causes the selected control unit to stack (hold) the status data. The control unit can present the stacked status only if suppress-out and address-out are down when select-out rises at the control unit.

1.7.3.3 Service-Out

- This identifies information on bus-out as data in response to service-in on write, search, and control operations.
- It indicates that the channel received data in response to service-in on read, and sense operations.
- It indicates that the channel accepted the status information in response to status-in.
- It indicates chaining in response to status-in with suppress-out active.

Service-out, a line from the channel to all attached control units, is used to signal the selected device in recognition of a signal on the service-in or status-in line (Figure 1-17). A signal on the service-out line indicates to the selected device that the channel has accepted the information on bus-in or has provided on bus-out the data requested by service-in.

When service-out is sent in response to service-in during read or sense operations, or to status-in, the service-out signal must rise after the channel accepts the information on bus-in. In these cases, the rise of service-out indicates that the information is no longer required to be valid on bus-in. When service-out is sent in response to service-in during a write, search, or control operation, the rise of service-out indicates that the channel has provided the requested information on bus-out. In this case, the signal must rise after the information is placed on the bus. Service-out must stay up until the fall of the associated service-in or status-in signal.



* Control Unit must drop Op-in within 6µsec.

** Select-out rises a minimum of 400 ns after address-out

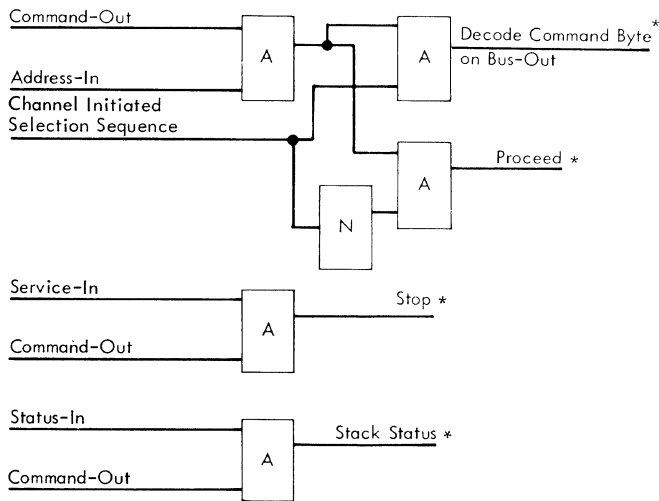
*** Rise of Op-in causes address-out to fall.

A Meaning to 2841

B Logical Circuit

22332 A

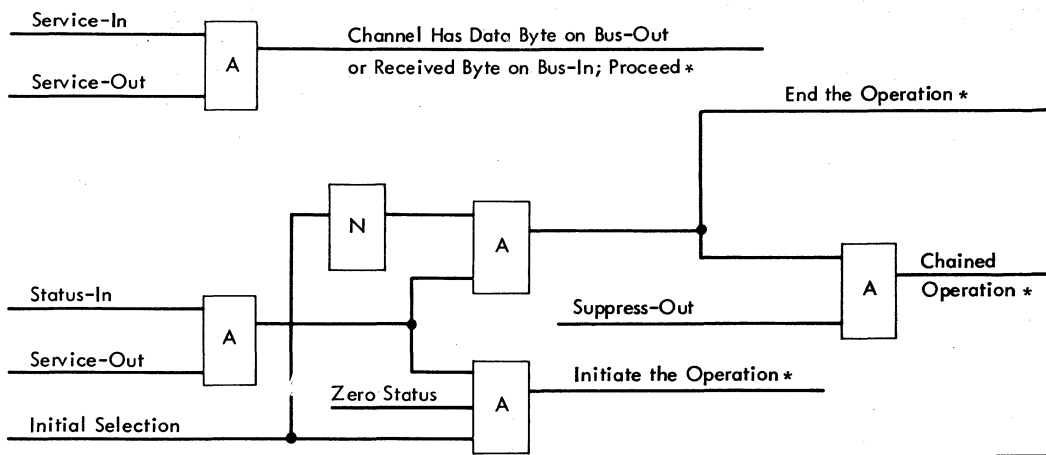
Figure 1-15. Address - Out



*Logical Meaning To Control Unit

22333 A

Figure 1-16. Command - Out



*Logical Meaning at Control Unit

22334A

Figure 1-17. Service - Out

Service-out cannot be up concurrently with any other "out" tag.

A service-out response to status-in while suppress-out is up indicates to the control unit that the operation is being chained. See Suppress-Out for further details. The status is accepted by the channel.

1.7.4 Inbound Tag Lines

- These lines carry instruction signals from the control unit to the channel.
- They identify information on bus-in lines.
- They remain active until an outbound tag responds to it.
- Two "in" tags cannot be active at the same time.

Control units transmit instructional signals to the channel over inbound tag lines. Two or more inbound tag lines cannot be active concurrently. The control unit must hold the inbound tag line active until the channel responds by conditioning an outbound tag line. The control unit must then cancel the signal on the inbound tag line to allow the channel to drop the responding outbound tag line.

1.7.4.1 Address-In

- This identifies information on bus-in as an I/O unit address.
- The channel responds with command-out.

Address-in is a line from all attached control units to the channel (Figure 1-18). It is used to signal the channel that the address of an I/O unit is on bus-in. The channel responds to address-in with command-out.

Address-in remains active until the rise of command-out. It must then fall in order that command-out can fall.

1.7.4.2 Status-In

- This identifies information on bus-in as status information.
- It remains up until command-out or service-out rises, or until select-out falls if Address-In is up.

A control unit activates the status-in line to indicate to the channel that a status byte is on the bus-in lines (Figure 1-19). The status byte has a fixed format and contains bits describing the current status at the control unit.

Status-in must remain up until the channel responds with:

1. Service-out, indicating that the channel accepted the status.
2. Command-out, indicating that the channel has suppressed the status.

If status-in is the control unit's reply to address-out, during initial selection, it must remain up until select-out falls.

1.7.4.3 Service-In

- This identifies information on bus-in on data read or sense operations.
- It indicates a control unit request for data on write and control operations.
- It remains up until command-out or service-out rises.

A control unit activates the service-in line (Figure 1-20) to:

1. Signal the channel that a data byte is on the bus-in lines (read, or sense operations).
 2. Request that the channel transmit a data byte on the bus-out lines (write, search, or control operations).
- The channel responds to service-in with:
1. Service-out, when data is accepted or transmitted.
 2. Command-out, to stop data transfers and end the operation.

1.7.5 Interlock Lines

- These lines permit only one control unit on the interface at a time.
- They gate the tag lines.
- They reset the control unit.

1.7.5.1 Operational-Out

- Gates on all interface lines except suppress-out.

- Operational-out provides a reset to the control units.

Operational-out originates at the channel, rising when the CPU is power-on reset. It stays up as long as the channel is operable. The fall of operational-out resets control units on the interface either selectively or concurrently depending on the status of suppress-out, a special control line (Figure 1-21). Operational-out is a gate on all outbound tag lines. They have no effect if operational-out is down. If the channel drops operational-out while a control unit is operating on the interface, the operation must be reset. If the operational-out and the suppress-out lines are down concurrently for 6 microseconds, all control units operating in the on-line mode are reset.

1.7.5.2 Operational-In

- This line signals the channel that a device is selected.
- It remains up until select-out falls and the signal sequence is completed.

To initiate an interface signal sequence, a control unit conditions operational-in while the incoming select-out line to the control unit is up. The control unit must, at the same time, block select-out from reaching the next control unit. No other control unit can connect to the interface while operational-in is up.

When operational-in is raised for a particular signal sequence, it must stay up until all required information is transmitted between the channel and the device. Operational-in must drop at the same time, or after the rise of the outbound tag associated with the transfer of the last byte of information, if select-out is down. For burst-mode devices, operational-in can drop if select-out is down or drops after receipt of the stop signal sequence.

Signals on bus-in and on the inbound tag lines are significant only when operational-in is up except in the case of the control-unit-busy selection sequence. When operational-in is down, the channel must disregard any signals on these lines. On the other hand, each control unit must provide interlocks to ensure that it does not place any signals on bus-in and the incoming tag lines unless its operational-in line is up.

1.7.6 Special Controls

- The four special-purpose lines are:
 1. Clock-Out.
 2. Metering-Out.
 3. Metering-In.
 4. Suppress-Out.

1.7.6.1 Clock-Out

- This indicates when the CPU is in a halt or wait condition.
- It designates when the control unit is free to change status.

The clock-out line (Figure 1-22) carries signals from the channel to indicate to each control unit that the processing unit is not in the halt or wait condition. Because a control unit can switch between the enable and disable states only when the processing unit is halted or waiting, clock-out designates the interval at which a control unit is free to change states. When the customer meter that registers processing unit time is disabled and the meter that indicates CE processing unit time is recording, the channel does not condition clock-out.

1.7.6.2 Metering-Out

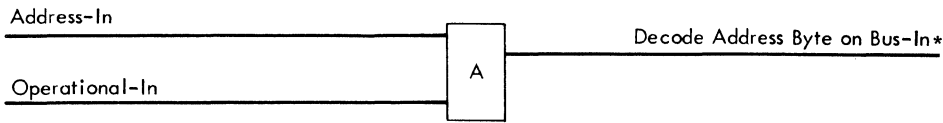
- This conditions customer meters to register time.

The channel transmits metering-out to each control unit when the customer meter is recording processing unit time. Metering-out causes customer meters to register time in each control unit that is not disabled.

1.7.6.3 Metering-In

- This indicates to the channel that the customer meter is recording time.

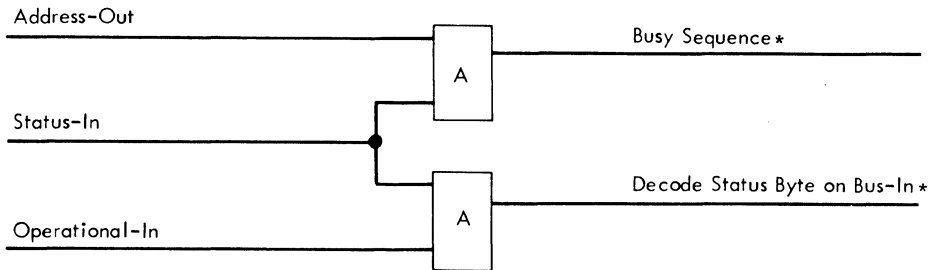
A control unit transmits metering-in to the channel when the customer meter on the control unit is recording time. Metering-in causes the customer meter that records use of the processing unit to accumulate time even though the processing unit may be in the halt or wait condition.



*Meaning to Channel

22335

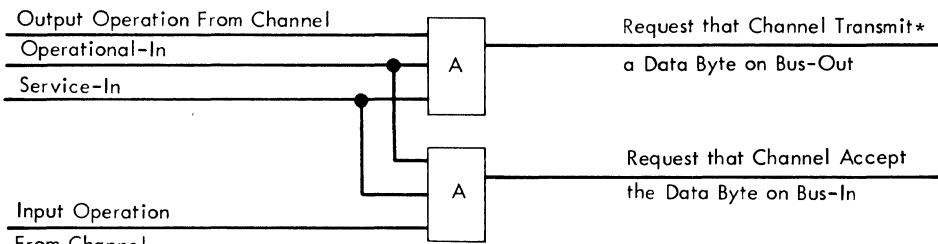
Figure 1-18. Address - In



*Meaning to Channel

22336

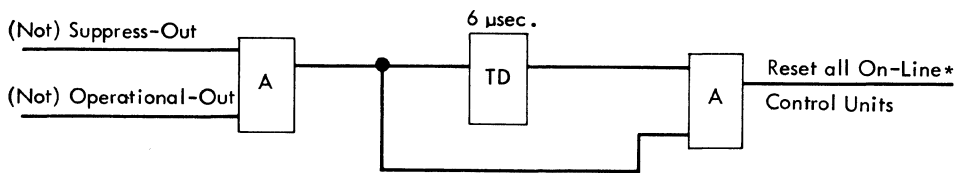
Figure 1-19. Status - In



*Meaning to Channel

22337

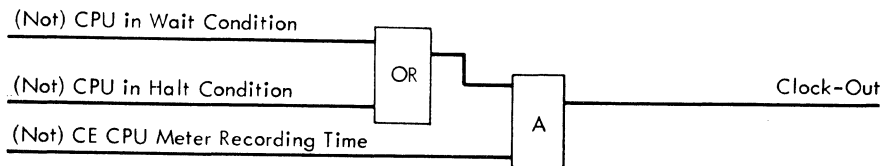
Figure 1-20. Service - In



*Meaning to Control Units

22338

Figure 1-21. Operational - Out



22339

Figure 1-22. Clock - Out

1.7.6.4 Suppress-Out

- The suppress-out line has these functions:
 1. Suppress status.
 2. Suppress data transfer.
 3. Chain command control.
 4. Selective reset.

Suppress-out is used alone or with an outbound tag line to provide the following special functions (Figure 1-23).

Suppress Status: When a control unit ends an I/O operation, it transmits a status byte on bus-in lines and conditions the status-in tag line to the channel. The status byte indicates whether errors were encountered in performing the operation and signals the channel that the operation is complete. A channel may respond to status-in with command-out, causing the control unit to stack the status data.

The next time select-out rises at a control unit holding stacked status data, that control unit will not activate the interface to present the status byte if suppress-out is active. The channel must condition suppress-out at least 250 ns before the control unit receives select-out to ensure that the stacked status data is not transmitted. The rise of suppress out, after a control unit begins a status cycle, does not interfere with the transmission of the status byte. If a control unit conditions request-in to offer status data, and suppress-out rises before the control unit receives select-out, suppress-out drops request-in.

Suppress Data Transfer: For noncyclic I/O devices (buffered I/O devices, not applicable to 2841) that can wait for data transfers without indicating an overrun condition, suppress-out blocks service-in. The channel must condition suppress-out at least 250 nanoseconds before the previous service-out tag drops to ensure that the subsequent request for data or offer of data will be suppressed.

Chain Command Control: To indicate a chained command, the channel conditions suppress-out after the selected control unit begins the cycle to transfer the ending status byte and before the channel responds to status-in with service-out. The active state of the suppress-out line and the service-out response to status-in combine to hold selection of the control unit and the I/O device. The next command from channel must be directed to that control unit and I/O device.

Selective Reset: If the channel conditions suppress-out at least 250 nanoseconds before allowing operational-out to fall and holds suppress-out active until 250 ns after operational-out rises again, only the I/O device presently operating on the interface is reset.

1.8 INTERFACE OPERATIONS

1.8.1 Initial Selection Sequence

- In this sequence the channel:
 1. Selects a control unit and device.
 2. Specifies the operation to be performed.
- The sequence is standard for all units and operations.

The interface signal sequence in which the channel selects a control unit and I/O device and specifies an operation to be performed is called the initial selection sequence (Figure 1-24). Regardless of the unit selected or the operation designated, the signal sequence in the initial selection is standard.

The channel begins the initial selection sequence by transmitting an address byte on bus-out lines and conditioning address-out. The address byte selects the unit to execute the operation. Each control unit attached to the interface attempts to decode the address, but, because all interface addresses are different, only one unit can interpret the coded byte.

When select-out is active at the control unit that successfully decodes the address byte, that control unit conditions either:

1. Status-in, indicating that the selected unit is busy and cannot execute another operation, or
2. Operational-in, indicating that the designated unit will complete the initial selection sequence. However the operational-in response to address-out does not commit the control unit or the channel to perform an operation.

If no control unit decodes the address byte (specified control unit is off line, the address byte is invalid, etc), the control unit with the lowest priority propagates select-in to the channel when its incoming select-out is conditioned. The select-in or status-in reply to address-out causes the channel to cancel-out and terminate the selection sequence.

When operational-in causes the channel to drop address-out, the selected control unit transmits an address byte on bus-in lines and conditions the address-in line. The channel compares this address to the address it placed on the bus-out lines to ensure that the right device has answered.

After checking the address, the channel responds to address-in by transmitting a command byte and conditioning command-out to the control unit. The command byte designates one of the thirty-four operations and establishes conditions to control execution of the operation.

The control unit must then drop address-in, and after command-out falls, the control unit places its status information on bus-in and raises status-in. If the I/O device is available, the status byte is zero. If the channel accepts this status byte, it responds with service-out. This signal completes the initial selection sequence.

Polling: When a control unit that does not have operational-in up requires service, it raises its request-in line to the channel. The next time select-out rises at any control unit requiring service and no I/O selection is being attempted by the channel (address-out down), the control unit places the address of the device on bus-in. It then signals on both the address-in and the operational-in lines, and removes the request-in signals. When the channel recognizes the address, a command-out signal is sent to the control unit, indicating "proceed." After address-in drops, the channel responds by dropping the command-out signal. The remainder of the sequence is the same as a channel-initiated initial selection sequence.

1.8.2 Data Transfers

- A control unit can send data to, or request data from the channel.
- Service-in and service-out are the controlling tag lines.

Data transfer may be requested by a control unit after a selection sequence. To transmit to the channel, the control unit places a data byte on bus-in and raises service-in; the tag and the validity of bus-in must be held until an outbound tag is raised in response. To request data from the channel, service-in is raised. The channel places the data on bus-out and signals with service-out. The channel maintains the validity of bus-out until service-in falls. When service-in falls, the channel responds by dropping service-out.

1.8.3 End Operation

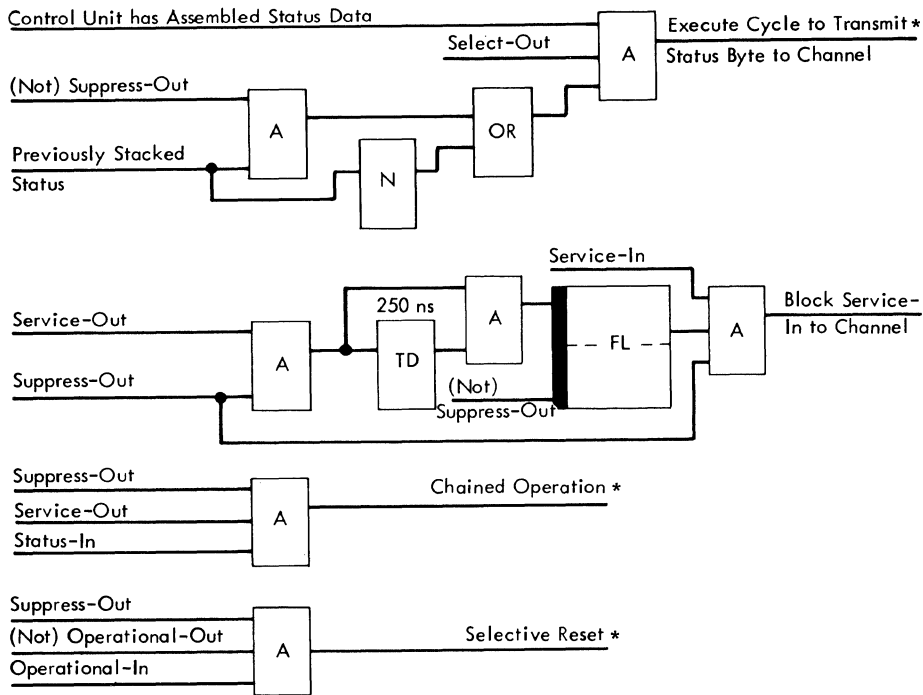
- An operation is completed when the control unit and device present ending status to the channel.
- The channel acknowledges receipt of the status byte with service-out or command-out.

When any I/O operation except test I/O and command immediates have proceeded to their normal end, the control unit assembles and transmits a second status byte to the channel. The meaning and format of this status byte are identical to the purpose and format of the status byte transmitted during the initial selection sequence.

To acknowledge receipt of the status byte, the channel conditions either service-out or command-out. Service-out indicates that the channel has accepted the status data and resets the operation. Command-out causes the control unit to stack the status.

If the channel conditions suppress-out 250 ns before select-out rises at the control unit holding stacked status data, the control unit does not transmit the status byte again until suppress-out drops. When the channel cancels suppress-out, and select-out to the unit is active, the control unit sends its address, and retransmits the status byte to the channel (Polling).

If the channel does not condition suppress-out before select-out rises at the control unit holding stacked status data, the control unit initiates another cycle to transmit the status byte again.



*Meaning to 2841
 **Not used by 2841

22340

Figure 1-23. Suppress - Out

1	Operational-Out	
2	Address-Out	
3	Select-Out ***	
4	Operational-In	
5	Address-In	
6	Command-Out*	
7	Status-In	
8	Service-Out*	

* A multiplex channel will respond to status-in with either command-out or service-out. Normally, a selector channel will respond to status-in with only service-out.

** Depending on the channel controlling the operation, select-out might drop during the initial selection sequence or remain active after the sequence is complete. Operational-in cannot drop until select-out is inactive.

*** Select-Out and Hold-Out up together.

22341

Figure 1-24. Initial Selection Sequence

2.1 MACHINE CLOCK

- Provides basic timing pulses for 2841.

The machine clock consists of a four latch ring counter (Figure 2-1) which gives four equal timed output pulses of 250 ms duration each. These pulses are labeled clock 1, 2, 3 and 4 and are distributed to each board of logic within the machine.

Each board converts these pulses to form other pulses, clock A, B, C and D. Each one of these pulses is 125 ns in duration. (Figure 2-2.)

The clock is free running and is only stopped during a Power On Reset. This resets clock 1, 2, and 3 and turns on clock 4.

2.2 REGISTERS (Figure 2-3)

- The basic 2841 contains 19 registers; A, B, GP, ER, GL, BY, BX, FR, KL, DL, DH, OP, ST, UR, DW, DR, W, X, and IG
- A, B, W, X and IG registers have specific uses as explained later.
- All registers except ER and W contain 8 bits
- The abbreviation used to designate each register has a specific meaning during particular operations but no meaning at all during other operations. The use of these registers within a particular micro programming sequence is covered in detail in Chapter 3.
- The A and B registers are entry points to ALU.
- The DR register can be used as a general purpose register. In Read or Write sequences, it is used as a buffer to SERDES.
- The ST register is primarily used by the micro-program for branching decisions.
- The ER register is used to hold conditions that occur during an operation; namely—Write Data Error, Halt I/O, Bus Out Parity, Control Unit Addressed while Busy, ALU check, and Address Out.
- The W and X registers are used for TROS Addressing.

- The IG register is used for channel control.
- ID and IH are gates for bus-in and bus-out.

2.2.1 General Purpose Registers (Figure 2-3)

The following 11 registers contain 8 bits plus parity and use polarity hold latches. The register abbreviations are explained but it should be understood that these registers are general purpose in nature and may or may not serve the particular function designated by their abbreviation. Chapter 3 contains a detailed explanation of the use of these registers in a particular micro programming sequence.

1. GP - General Purpose register
2. GL - Gap Length register (not used for this purpose)
3. BY - Code Check Burst register
4. BX - Code Check Burst register
5. FR - Flag register
6. KL - Key Length register (not used for this purpose)
7. DL - Data Length Low register
8. DH - Data Length High register
9. OP - Operation Code register
10. UR - Unit Address register
11. DW - Data Write register

All of the general purpose registers (Figure 2-3) have an output to ALU on the A-bus. In addition the BY Register may also be gated to ALU on the "B" bus. UR is also used to select a particular file.

2.2.2 A Register (Figure 2-3)

This register serves as the common entry to the arithmetic/logic Unit from the A-Bus. It contains 8 bits plus parity and uses polarity hold latches.

2.2.3 B Register (Figure 2-3)

This register serves as the common entry to ALU from the B-bus. It contains 8 bits plus parity and uses polarity hold latches. The output of the B-register may enter the ALU in true or ones complement form under micro program control.

2.2.4 DR Register - Data Read Register (Figure 2-3)

The DR register consists of 8 bits plus parity and uses polarity hold latches. Inputs to DR are from CE switches, ALU (D-Bus), or the file data register (in SERDES) when reading. Outputs of DR are to the A or B-register assemblers, or to FDR (in SERDES) when writing.

It should be noted that, when reading, DR may or may not contain good parity since parity is not assigned until the read byte is transferred from DR through ALU to one of the general purpose registers.

It should also be noted that the transfer of data from FDR to DR (Read) is not under micro program control. Whenever FDR has a byte (8 bits), this byte will be transferred to DR. The micro program is notified of this transfer by setting of status register bit 4 (means DR is full on a read). The micro-program must move this byte out of DR within approximately 6.4 μ sec (2311) or the next byte from the 2311 will destroy the original byte in DR. When writing, the transfer of data from DR to FDR is also outside of micro program control. Whenever FDR is empty, DR will be transferred to FDR. The micro program will be notified of this transfer by the setting of status register bit 4 (DR has been used on a Write). Unless the microprogram reloads DR with a new byte of data within approximately 6.4 μ sec (2311), the original byte will be retransferred to FDR and written on the disk storage again.

2.2.5 ST Register - Status Register (Figure 2-3)

The status register (ST) consists of 8 bits (no parity) and uses flip latches. The ST is used by the micro-program for branching control. That is, bits in the status register may be set and reset under micro-program control to indicate conditions within the machine; i. e., ST 6 on could mean write gate is on, ST 7 could mean erase gate is on. The microprogram can, at a later time, branch on status bits to the proper routine, i. e., ST 6 on and index - drop write gate.

The ST register has inputs from the D-Bus (in CE Mode only) and the status assembly logic (one bit at a time). It has outputs to the A-Bus (in CE Mode only) and the CH-CL branching circuits.

The following status bits have definite meanings. ST(1) - Turned on with a selected index pulse after a micro program statement of 1 \rightarrow ST(1). The statement 1 \rightarrow ST(1) turns on the allow index latch.

A CL decode of 14 (CL statement INDEX) allows the micro program to branch on ST(1) after it is set by the index pulse.

ST(1) is reset by the statement 0 \rightarrow ST(1).

ST(4) - Read Operation - Turned on when FDR is transferred to DR. Means DR is full. Write operation - Turned on when DR transferred to FDR. Means DR has been used.

The other status bits are used by the microprogram for different meanings in different sequences. Chapter 3 has a more detailed discussion of the use of status bits within a particular microprogram sequence.

2.2.6 ER - Error Register (Figure 2-3)

This register is used to hold conditions that occurred during an operation. It consists of five flip latches.

ER(0) is set on if there is a serial data error in SERDES during writing. ER(0) lights the data check lamp. Op In reset resets the ER(0) flip latch and turns off the lamp.

ER(1) is not a latch. However, address out is gated into the ER(1) assembler for testing by the microprogram.

ER(2) is set on if bus out parity is detected on the command or data bytes. ER(2) lights the data check lamp. Op In reset resets the ER(2) flip latch and turns off the lamp.

ER(3) is set on during the short control unit busy sequence. When the control unit goes not busy, the microprogram initiates a control unit end polling interrupt sequence. A more detailed description of the short control unit busy sequence is found under Channel Interface Attachment.

ER(4) is set on under the following situation:

1. ALU bypass being used - (A Reg to D Bus), and,
2. A Reg Parity does not agree with parity computed by ALU, and
3. Bus Out Parity did not occur on this byte.

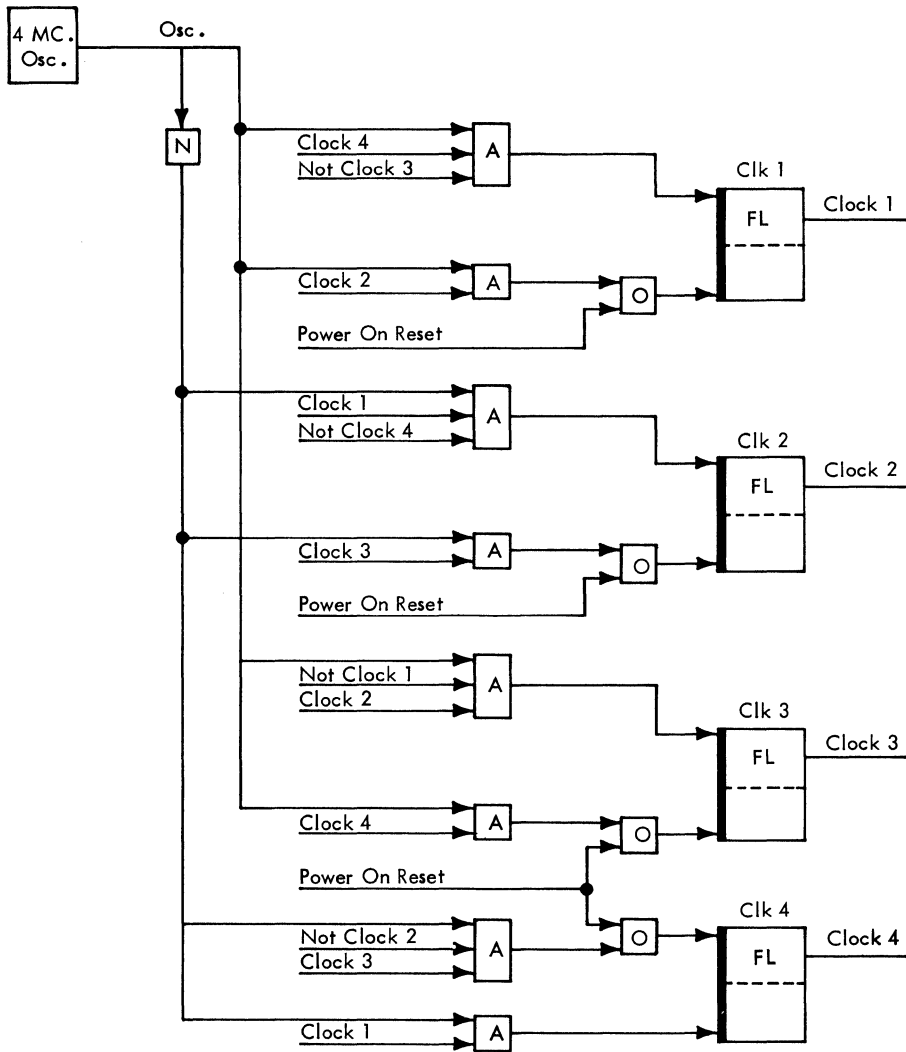
ER(4) will light the data check lamp and the machine will stop.

ER(7) is set on by a halt I/O command. It is also used in the short control unit busy sequence in setting of ER(3).

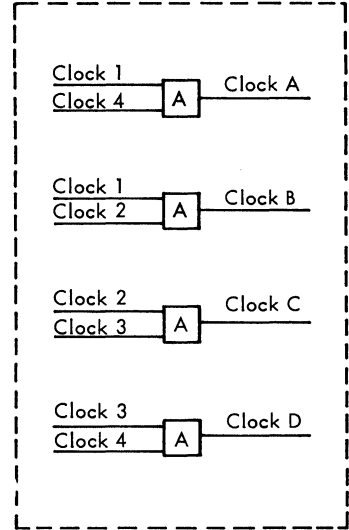
2.2.7 Miscellaneous Registers and Controls (Figure 2-3)

2.2.7.1 TROS Addressing Registers

The W and X registers are used to address the transformer read only storage. W and X contain 12 bits giving the 2841 the ability to address 4096 individual TROS words. Since the 2841 has only 2048 words (2K), the high order bit of the W register is not used.

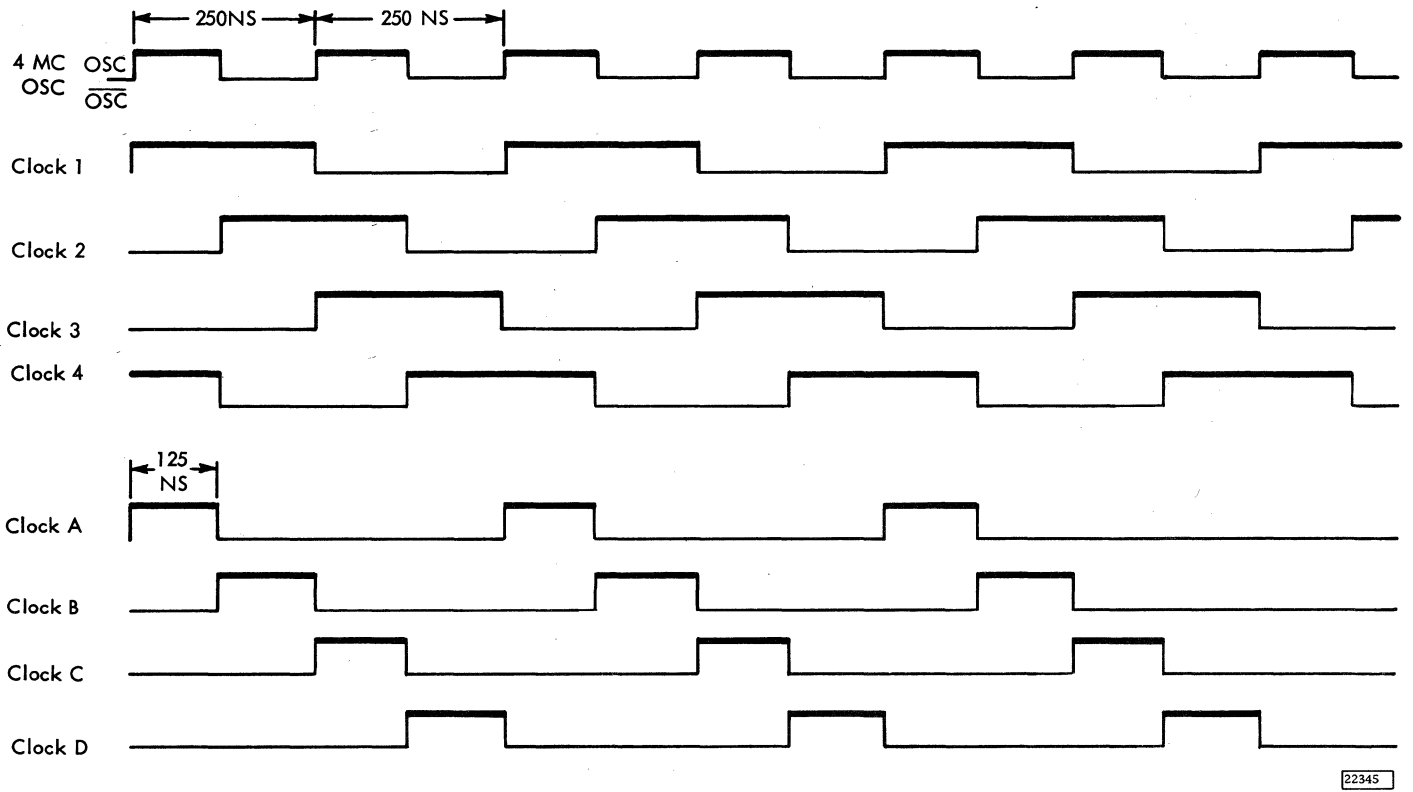


Typical Board Clock Pulse Assembler



22344A

Figure 2-1. 2841 Machine Clock



22345

Figure 2-2. Machine Clock Timing

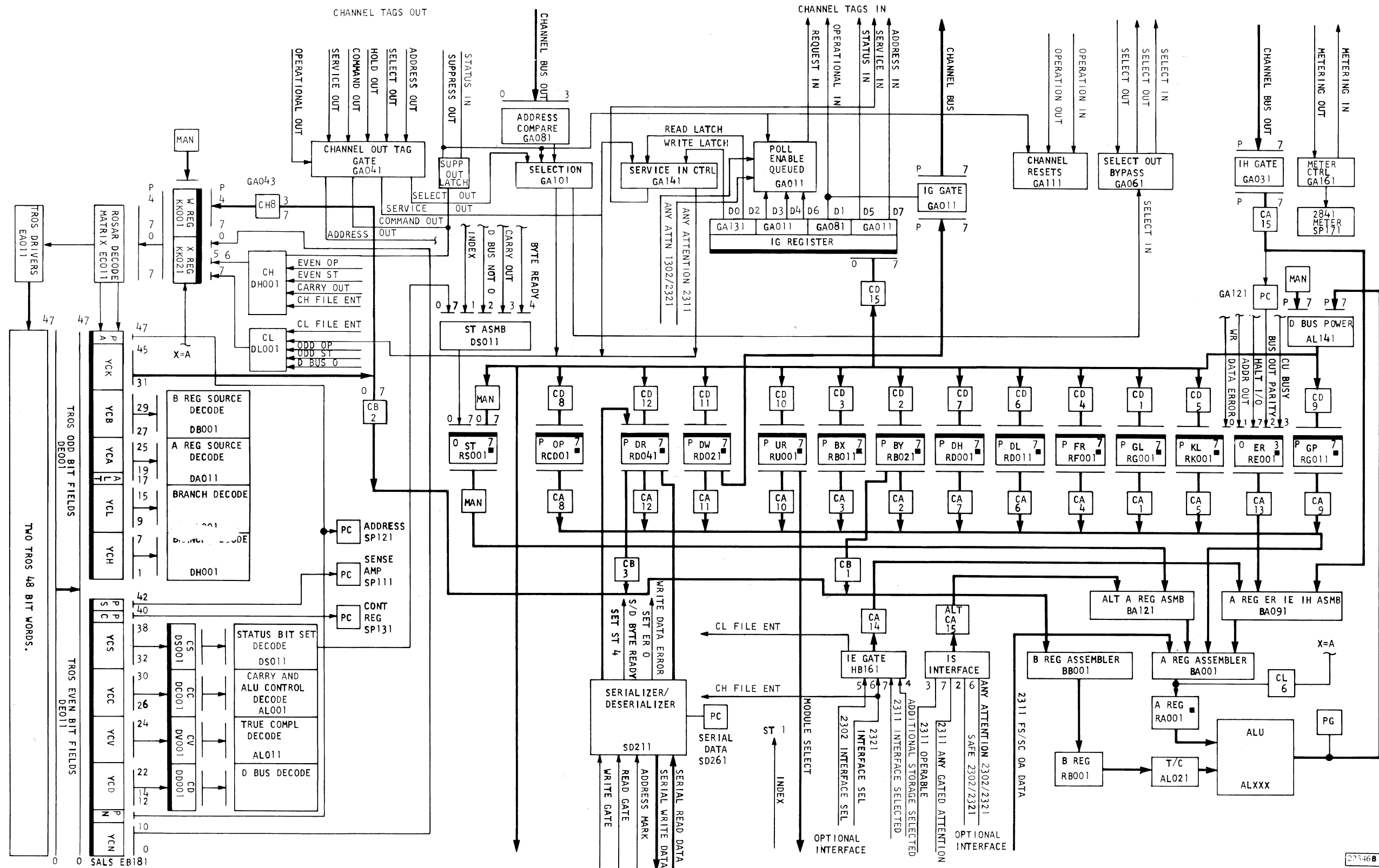


Figure 2-3. Storage Control and I/O Channel Interface

2.2.7.2 Channel Control Register (IG)

The IG register is used to raise and lower tag in (i. e., address in, status in) lines to the channel. IG consists of 8 latches.

- IG0 - Write latch - Used to set up the service in/out controls for write, search, and control operations
- IG1 - Operational In (Op In). Used to reset Op In Latch.
- IG2 - Read latch - Used to set up the service In/out controls for read and sense operations.
- IG3 - Queued latch - Used for presenting any status other than device end through the polling interrupt sequence. Raises request In if suppress out is down.
- IG4 - Poll Enable latch - Allows any gated attention to initiate a polling interrupt sequence. Raises request in if Suppress Out is down.
- IG5 - Status In
- IG6 - Used for presenting outstanding device end to a multiplexor channel when command word chaining is indicated. This is accomplished by means of a non-suppressible polling interrupt sequence. Raises request in (not gated by Suppress Out).
- IG7 - Address In. Also conditions operational in.

2.2.7.3 Service In/Out Controls

In addition to IG, five latches (latch 1, latch 2, Service request, service in, and initial select are used for controlling the service in/out responses to channel.

2.2.7.4 Bus Out Gates

IH is a set of 9 gates. It allows bus out to be gated to the A Bus.

2.2.7.5 Bus In Gates

ID is a set of 9 gates. It is tied directly to the DW register and is used for gating data to channel.

2.3 2311 INTERFACE ATTACHMENT (Figure 2-4)

- The 2311 interface attachment consists of:
 1. Two registers (FC and FT).
 2. Four gating networks (MS, SC, FS, OA).
 3. Associated assemblers.

Assignment of device type (2311-2321-1302) to a module address is done by the CE, as requested by the customer, by changing constants in the microprogram. For the 2311, the microprogram sets FT register bit 7 to select the 2311 Interfaces.

Unit selection is done by decoding the three position field with the microprogram. A binary zero (000) decodes to UR register bit 0 and a binary seven (111) decodes to UR register bit 7.

2.3.1 FT - File Tag Register (Figure 2-4)

The file tag register consists of eight polarity-hold latches. It is used to raise and lower tag lines to the 2311, and to identify the file type (FT-7) to the 2841. Polarity hold latches are used so that individual bits in the register may be turned on or off without affecting the remainder of the register. The D Bus Output (Figure 2-5) is the control input to the polarity hold latch. CN-5 is the data input to the latch.

Example 1

Assume the following:

1. FT is equal to zero
2. ALU statement says $128 \rightarrow FT$. CN-5 equals a one.

All eight FT latches have a data input of one but only BIT 0 has control. Therefore bit 0 is the only latch affected and is turned on.

Example 2

Assume the following:

1. FT equals 128
2. ALU statement says $128 \rightarrow FT$
3. CN-5 equals 0

All FT latches have a data input of zero. Bit 0 is the only latch that has control. Therefore bit 0 is the only latch affected and is reset.

2.3.2 FC - File Control Register (Figure 2-4)

The file control register consists of eight polarity-hold latches and is similar to FT in operation. It is used in conjunction with the FT register to define an operation to the device. For example:

1. FC = 2, FT = 0 - Return to zero
2. FC = 2, FT = 1 - Load CAR in 2311 with 2
3. FC = 2, FT = 2 - Select head 2 - go backward when you receive Seek Start
4. FC = 2, FT = 3 - Load the 2311 Difference Counter with 253 (ones complement of FC)

FC (Figure 2-5) uses polarity-hold latches and CN-5 so that individual latches may be affected without disturbing the remainder of the register. For example:

Assume:

FT = 0 - Control tag
 140 → FC - Head select, write and erase gates are on

The microprogram is operating on a write CKD command. When index is detected write gate is dropped.

Solution:

Index reached - ALU statement will say 128 → FT and CN-5 equal to zero. All latches have a zero data input. Only a 0 has control, therefore, only bit 0 is affected and is turned off.

2.3.3 MS - Module Select Gates (Figures 2-3, 2-4)

MS is a set of gates used in selecting a particular file. The unit address register (UR) contains the module select number (one of the 8 bits on). This is fed to MS. If FT bit 7 is on, the contents of UR will be gated through MS to the 2311.

2.3.4 SC - Seek Complete Gates (Figures 2-3, 2-4)

SC is a set of gates used in gating gated attention (Seek Complete) from a 2311 to the 2841 "A" Bus.

In addition all gated attentions are OR'ed together and placed on bit 7 of the IS (Interface Status) gates. The microprogram may then test IS, bit 7, for any gated attention before checking the individual bits in SC. Any gated attention is also sent to the channel interface. If the poll enable latch is on and the channel is not selected to some other control unit, any gated attention will cause "request in" to be raised. This initiates a polling interrupt sequence with the channel.

2.3.5 FS- File Status Gates (Figures 2-3, 2-4)

FS is a set of gates used in gating file status from a selected 2311 to the 2841 "A" Bus. Five status bits are transferred from the 2311 to the 2841.

Name	Bit Positions in FS
Ready	0
On Line	1, 4
Unsafe	2
End-of-Cylinder	5
Seek Incomplete	7

Unsafe and seek incomplete are error conditions. End-of-Cylinder indicates that an attempt has been made to advance the head address register in the 2311 past 9.

Ready, on line, safe, not end-of-cylinder and not seek incomplete are AND'ed together to develop file operable. File operable feeds IS bit 3. The microprogram can test this one bit to see if the file is functioning properly. If IS bit 3 is not on, then the microprogram can test FS to find out which condition caused the device to go not operable.

2.3.6 OA - Old Address Gates (Figures 2-3, 2-4)

OA is a set of gates used in gating the cylinder address register in the selected 2311 to the 2841 A bus.

2.3.7 IE - Input Element Gates (Figure 2-3)

The 2311 interface has a FT register. The 2302, 2321, and interfaces share another FT register. Particular bits in these registers are used to indicate to the microprogram which type of device is selected. This is necessary since there are small differences in the internal operation of the 2841 for different devices. A summary of FT bits used and IE bit positions affected follows:

2311	FT-7 feeds IE-7
2302	FT-5 feeds IE-5
2321	FT-6 feeds IE-6

2.4 TRANSFORMER READ ONLY STORAGE - TROS

2.4.1 Purposes and Use of TROS

- Output of TROS controls machine functions.

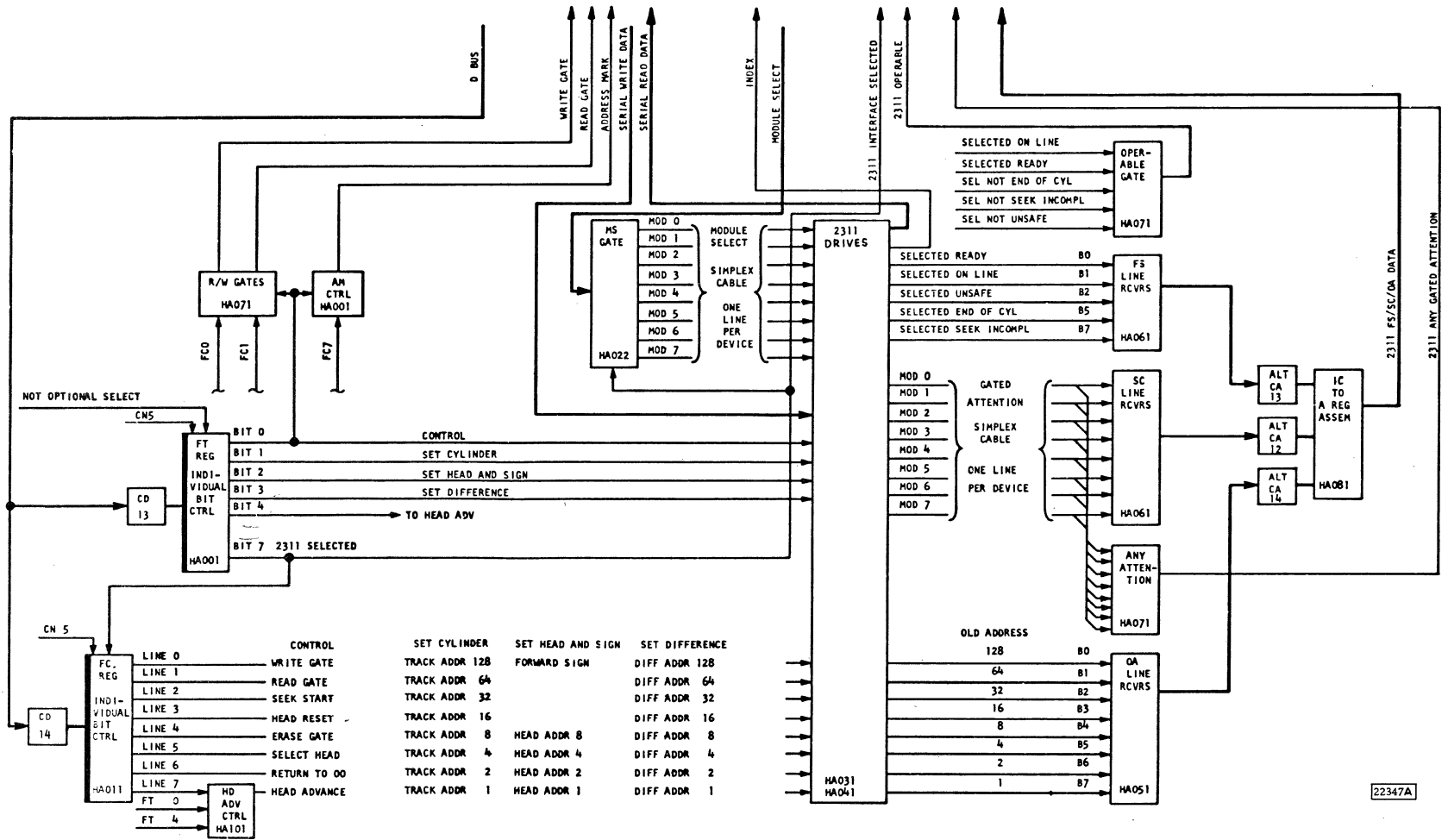


Figure 2-4. 2311 Attachment Circuits

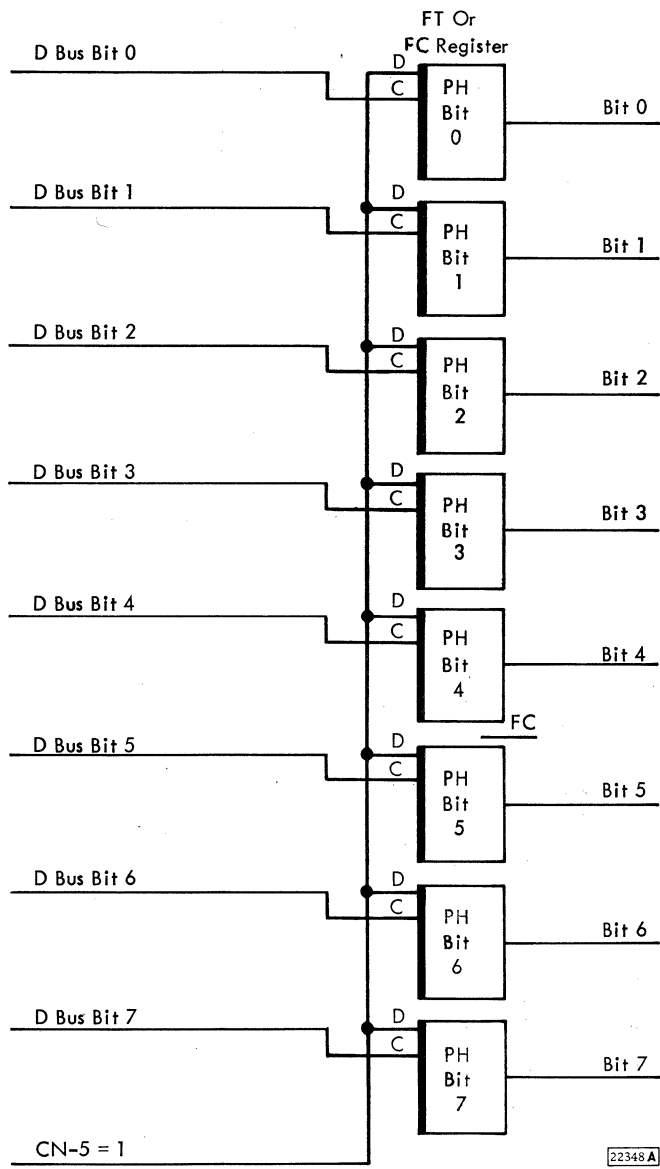


Figure 2-5. FT or FC Register

- One output word of 48 bits is read out at a time.
- Output of word is called a microinstruction.
- A chain of microinstructions is called a microprogram.

The contents of any TROS word can be read out and stored in latches. This latched information is decoded and used to control machine functions. Part of the information read out of a particular TROS word is used to determine the next TROS word to be addressed.

The TROS words are addressed in a particular sequence, and this sequence of addresses is called a microprogram. To perform any operation in the machine, the various parts of the 2841 (ALU, registers, status bits, etc.) are controlled by the microprogram to perform certain functions in a certain sequence.

2.4.2 Characteristics and Capacity

- TROS contains fixed predetermined information.
- TROS can only be read out.
- A 12 bit address is used to select the next word to be read out.

TROS contains fixed, predetermined information which can only be read out. The stored information can be altered only by physically changing TROS.

TROS units can be built in various storage capacities. The 2841 uses a 2K model of TROS and it is the only model of TROS discussed in this manual. There are 2,048 TROS words in the 2K model of TROS.

A 12 bit address register (W and X) is used to address the 2,048 words in the TROS unit. The TROS word in the 2841 is 48 bits long, and has a maximum possible length of 60 bits. The 12 additional bits are not presently used in any of the 2841 words.

TROS is built up of modular units, each having 256 addressable words, and each word having a length of 48 bits. The TROS for the 2841 contains 8 modules and has a capacity of 2,048 words.

2.4.3 Principles of Operation (Figure 2-6)

- TROS uses the current transformer principle.

- Sixty transformers are selectively linked with a drive line to provide one TROS word output (only 48 transformer positions are actually used).
- A drive line links with a transformer in position where a 1-bit output is required.
- A drive line bypasses a transformer in positions where a 0-bit output is required.
- Each of two drive lines on one flexible plastic tape links the selected transformers.
- One of the two drive lines on each tape is selected to read out a TROS word.
- The TROS transformer consists of a U-core and an I-core.
- Etched copper drive lines on plastic tape are selectively interrupted by punched holes to either link or not link transformers.

Transformer Principle: When a current pulse is passed through the primary winding of a transformer, it induces a current pulse in the secondary winding. If no primary current pulse flows (or there is no primary winding), there is no output in the secondary winding. This is the principle of TROS operation.

Drive Line Linkage with Transformers: The primary of the transformer is an addressed drive line and the secondary of the transformer forms the sense winding. When a drive line links with a transformer core, a current pulse in this drive line induces a current pulse in the secondary winding. If the same drive line by-passes a transformer, no current pulse is induced in that particular sense winding. A pulse in the sense winding represents a 1-bit, no sense winding output represents a 0-bit. Additional drive lines could be used in a similar manner.

Example (Figure 2-6):

A current pulse in drive line A gives an output of 101.

A current pulse in drive line B gives an output of 011.

The 60 transformer cores associated with each TROS tape give an output of 60 bits (only 48 are used). Two drive lines for each set of 60 cores allow two different bit configurations depending on which drive line is selected.

TROS drive lines are etched in copper on flexible plastic tapes. On each tape, two drive lines are

printed, both in the form of a ladder network. Holes are punched between the rungs of the ladder so that U-cores can be inserted through the tapes to mate with the I-cores (Figure 2-7).

Transformer Cores: The core of a TROS transformer consists of two parts, a U-core and an I-core. Both the U-core and the I-core are made of soft, low-remanence ferrite. To reduce flux leakage, the U and I cores are first coated with an insulating material and then copper plated. A sense winding of 35 turns is wound on the I-core and the U-cores are gapped on their outside face to prevent the plating from acting as a short circuited turn.

Interrupting the Drive Lines to Store a Logical 0 or 1: Each leg of the U-core, when inserted in the tape, is encircled by the sides of the ladder network and two of its rungs. By physically interrupting either side of the ladder, the conductor (drive line) may bypass or link with the core (Figure 2-8). In (A) of Figure 2-8, note where the sides of the ladder must be punched to obtain a logical 0 from a given bit position. In (B) of Figure 2-8, note where the sides of the ladder must be punched to obtain a logical 1 from a given bit position. The asterisked arrows in Figure 2-8 are intended to show the direction in which the current in the conductor tends to wrap, or link with the U-core. In both (A) and (B) of Figure 2-8, note that the currents for an A word and B word logical 1, wrap the U-core in the same direction thus giving the same polarity signal to the sense amp for a logical 1. The currents for a Logical 0 in both A and B words bypass the cores, however a very small current noise signal is generated. The logical signal is blocked at the sense amplifier.

2.4.4 Module Physical Construction (Figure 2-9)

A TROS module is the building block for every TROS array. The following description refers to numbered references on both Figures 2-9 and 2-10.

Plastic Tapes (Figure 2-9): The 128 plastic tapes (18, 19) are contained in a tape deck carrying a total of 256 TROS words. Holes are punched between the ladder network of the tape to accept the U cores (21) which pass through the tapes to mate with the I-cores (4). The I cores (4) are held in a core carrier assembly consisting of parts (3), (5), and (6).

Core Carrier Assembly (Figure 2-10). The core carrier assembly consists of a core carrier (1) into which the I-cores (2) are inserted. Springs (3) are placed behind the I-cores to ensure proper contact with the U-cores. The springs and the I-cores are held in position by clipping the strips (4) into the core

carrier. The sense windings are wound round the core carrier, encircling the I pieces. The ends of the sense windings are connected to the pins on the contact strip. On one end of the core carrier there is a boss (5) to enable correct visual orientation when placing the core carrier onto the support rods (1 Figure 2-9). If assembled incorrectly it would be impossible to connect the module to the TROS gate.

Module Assembly (Figure 2-9): The tapes are lifted on and off the module by the rails (9) and located by means of the aligning pins (20), screwed into the support (8). The blocks (2) carry the two rods (1) for the core-carrier assemblies to clip onto. There are thirty carriers. The support (8) and chassis (7) screw into the blocks (2) and are spaced by the rails (9).

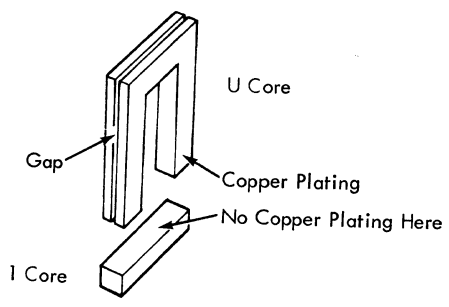
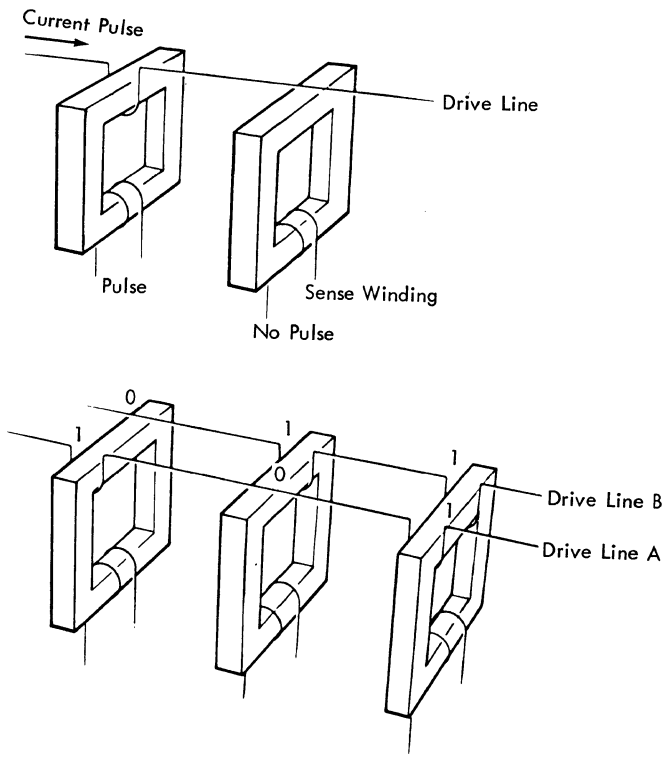
The U-cores (21) are held in the module by the retainer (22) and insulator (23). The retainer (22) screws into the support (8) and chassis (7), and forces the U-cores (21) against the I-cores.

Connections to the Module: Connected to the chassis are the module end boards (10) to carry the diodes (11) used for TROS word addressing and connections to the tapes in the tape deck. The diode board nearest the I-cores is defined as the bottom end board, and the diode board nearest the U-core retainer (22) as the top end board.

The connections to the TROS tape consist of pins placed in plated thru holes in the diode board on which the four tape terminal connections are pressed.

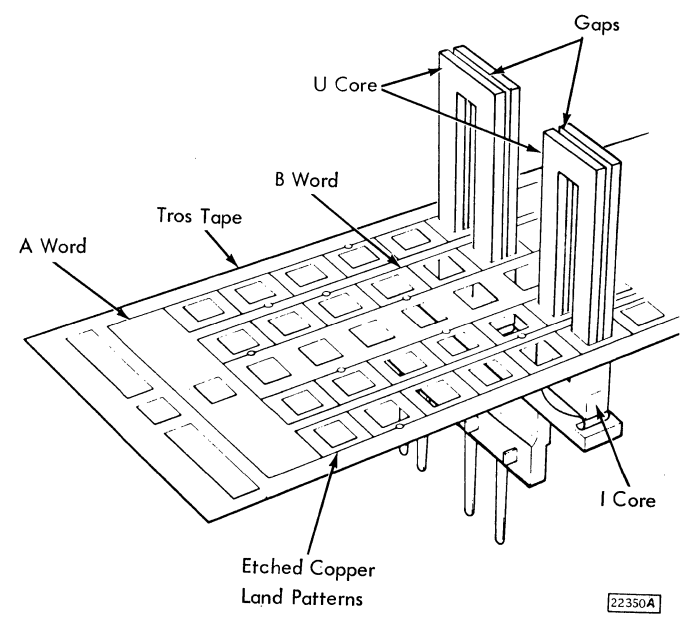
Input/output connections to the module end boards are made by the C and Z tapes and paddles (12), (13) and (14). The C and Z tapes have pins passing through plated holes in the diode boards (10) and soldered to printed circuitry on the diode boards. The C and Z tapes (12) (13) are clamped to the chassis (7) by the clamps (17) so as to relieve any strain in the connections to the diode boards (10).

Laminar Bus (Figure 2-11): When a number of modules have been assembled, the sense windings associated with each particular bit of a module are connected in parallel. In Figure 2-11 the sense windings for a particular bit in each of the 8 modules are shown connected in parallel with a 200 ohm terminating resistor. The terminating resistor is shown connected to the laminar bus. Each laminar bus consists of four conductors printed on a strip of non-conducting material. Each conductor has pins connected to it, coinciding with the pins on the core carrier. The pins of the core carrier are soldered to those of the laminar bus bars.



22349A

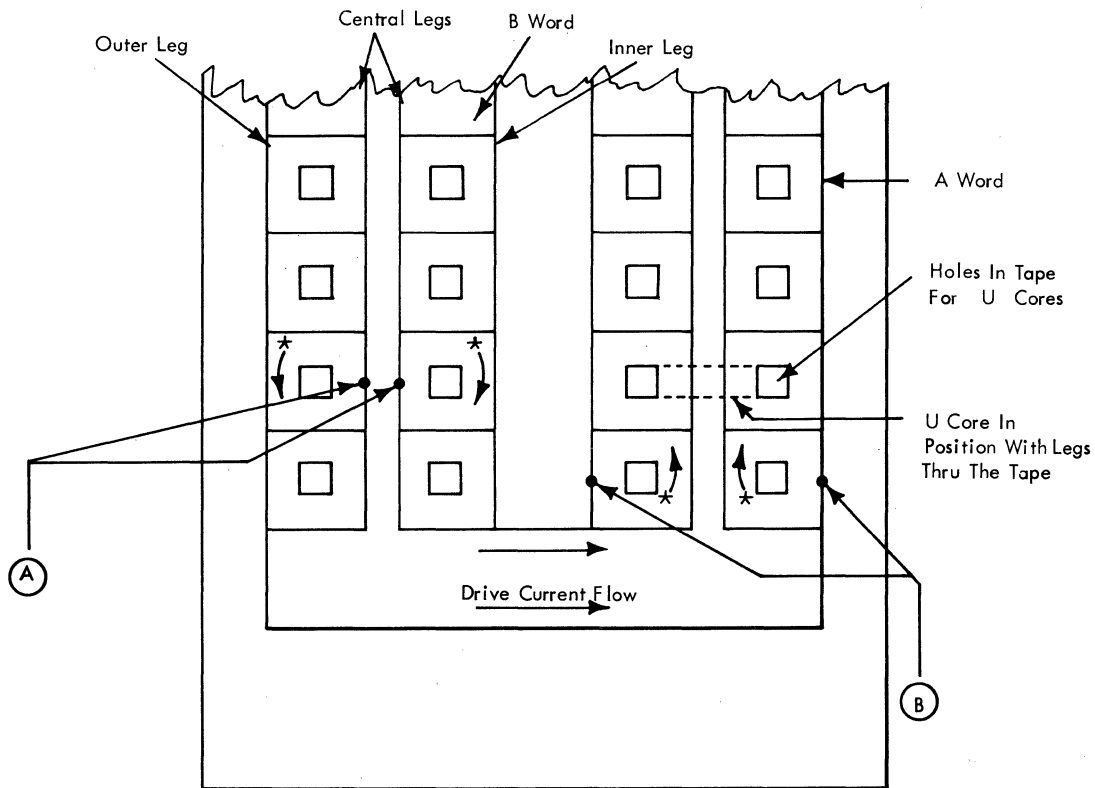
Figure 2-6. Principle of TROS



22350A

Figure 2-7. Tape With U and I Core

Tros Tape Section - Showing Punching For Logical 1 & Logical 0 In A & B Words



(A) Punching Shown For A Logical 0 In These Bit Positions

(B) Punching Shown For A Logical 1 In These Bit Positions

Note: To Program A Logical 0 In An A Word The Central Leg Must Be Punched - To Program A Logical 0 In A B Word The Central Leg Must Be Punched

Note: To Program A Logical 1 In An A Word The Outer Leg Must Be Punched - To Program A Logical 1 In A B Word The Inner Leg Must Be Punched

★ The Arrows Indicate Direction Of Current Flow As The Conductor Tends To Wrap Around The Core - It Will Be Noted That For A Logical 1 The Current Wraps In One Direction-While For A Logical 0 The Current Wraps In The Other Direction

22351A

Figure 2-8. TROS Tape Section

1. Rod
2. Block
3. Carrier
4. 1 Core
5. Spring
6. Strip
7. Chassis
8. Support
9. Rail
10. Diode Board
11. FDD Substrate
12. I/O Cables
13. I/O Cables
14. I/O Cable Card
15. Cable Clamp
16. Terminating Pins
17. Clamp
18. Tape Stack
19. Tape Stack
20. Alignment Pin
21. 2 Banks Of 24 U Cores
22. Retainer
23. Insulator

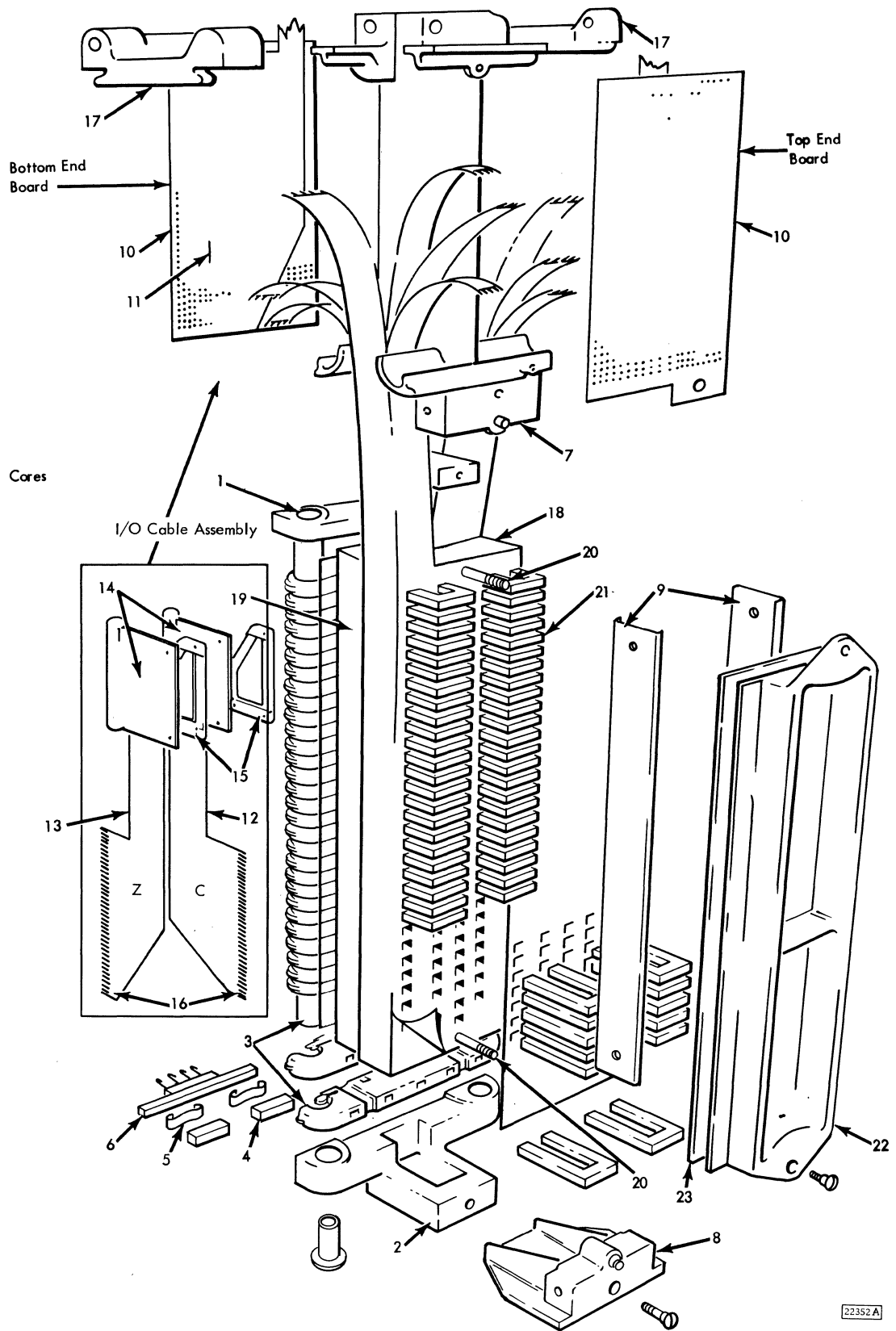
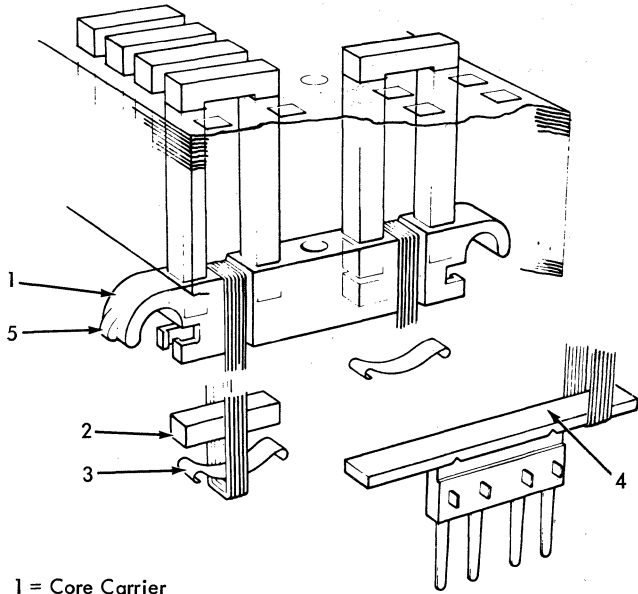


Figure 2-9. TROS Module



- 1 = Core Carrier
- 2 = 1 Core
- 3 = Compression Spring
- 4 = Contact Strip
- 5 = Locating Boss

22353

Figure 2-10, Core Carrier Assembly

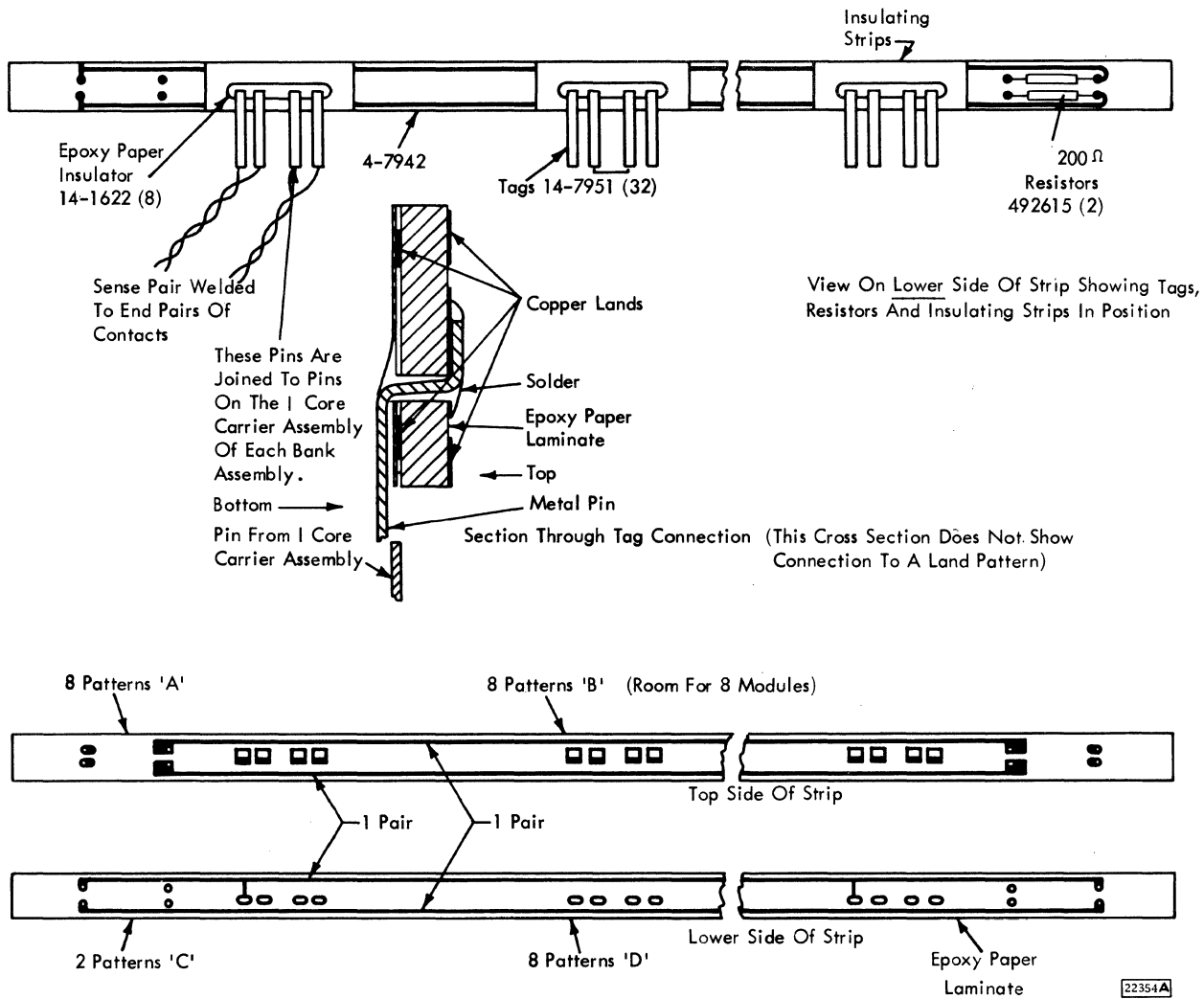


Figure 2-11. Laminar Bus

2.4.5 TROS Tape Deck

- The TROS tape deck is numbered from top to bottom: 64-127, 63-0.
- Three types of tapes reduce inter-tape capacitance.
- A Resistance tape isolates tape 127 from tape 63 and provides a resistance loop around each leg of each U-core to dampen resonance.

2.4.5.1 Tape Numbering and Identification (Figures 2-13 and 2-14)

The upper 64 tapes in the module are in an inverted position with respect to the lower 64 tapes. This creates more space for the connection of the tape ends to the module end boards. The bottom of the module is defined as the side nearer to the I-cores. The tapes in the lower half of the tape deck are numbered 0 - 63 from the bottom up. The tapes in the upper half of the tape deck are numbered 64-127 from the top down.

On the end of the TROS tape there are two copper tabs which serve to identify the tape (Figure 2-14). The seven digit number represents the part number of the tape. The three high order positions of the part number will be 221 to identify the tape as belonging to the 2841. The fourth position of the part number represents the module where the tape is located.

The nine digit number is broken down as follows: the three high order digits represent the sequence number of the tape in the tape deck, the low order 6 digits represent the E/C level of the tape. Above the E/C level is a letter (A, B or C) to identify the type of tape for tape stagger purposes (Figure 2-12).

2.4.5.2 Types of Tapes - A, B and C

To reduce the capacitance between the drive wires on adjacent tapes, three different types of tapes are used. On each type the conductor pattern is displaced from the U-core hole by a different amount. These three types are labelled A, B and C and are arranged sequentially throughout the deck of tapes.

2.4.5.3 Resistance Tape (Figure 2-15)

To damp any resonance which might be caused by inter-tape capacity and flux leakage, a distributed

loss is introduced. This is achieved by including in each module a plain plastic resistance tape on which single turns of resistance foil are etched. These resistance loops are also covered with a plastic insulating layer. The single resistance loops encircle each leg of each U-core, and have an approximate resistance of 0.6 ohms.

The tapes in the tape deck are divided equally into sections, with end terminations passing on either side of the chassis. Since all tapes are similar in their basic construction, the bottom set of tapes is completely reversed with respect to the top set. Therefore, to prevent the wiring on tape #63 and tape #127 from touching, the resistance tape is located between these two tapes.

2.4.6 Addressing TROS

- 12-bit address register is used to address TROS.
- Addressing of any of the 2,048 words of TROS is accomplished by the outputs of a 32 by 64 matrix; 32 gates and 64 drivers form the inputs to the matrix.
- Each of the eight TROS modules is addressed by a matrix made up of the 64 drivers and four of the 32 gates.
- One driver and one gate are required to address any of the 2,048 TROS words.

Addressing for the 256 word lines of a single module (Figure 2-16) is accomplished by a matrix made up of 64 drivers and four gates. The 64 drivers are common to all eight modules. Module 0 (Figure 2-16) is driven by 4 of the 32 gates (Gates 0 - 3). Module 1 is driven by gates 4 - 7 etc.

To address any word in TROS, a drive circuit is needed at one end of the drive line, and a gate circuit at the other end. For example (Figure 2-16), the drive line for word 5 is energized by turning on driver 1 and gate 0. The diodes on the driver side of the drive line prevent back circuits through other drive lines and drivers.

Module End Boards: The 128 tapes in a module are terminated on two module end boards (Figure 2-17)

on which are also mounted the isolating diodes in the form of FDD (four double diode) substrate blocks. The commoning of lines on the module end boards is as follows:

Drive Commoning: Because 64 drivers are used for 256 word lines, four word lines from each module are commoned to one driver. The 4 word lines are the A and B lines on any particular tape together with A and B lines on the corresponding tape in the other (upper or lower) half of the module. For example, the A and B words on tape 95, together with the A and B words on tape 32 are common to driver 32 (Figure 2-17).

Gate Commoning: Each module has 256 word lines and 4 gates with 64 word lines commoned to each gate. In the upper half of the module, all the A lines are taken to one gate, all the B lines to another gate and similarly in the lower half of the module. The leads to the gates are numbered 0 - 31. Gates 0 - 3 are connected to module 0, gates 4-7 are connected to module 1 etc. For example, the B words of tapes 64 through 127 are commoned to gate 3 and the A words of tapes 64 through 127 are commoned to gate 2. In the lower deck all the A words are commoned to gate 0, all the B words to gate 1.

Diode Substrate: The diodes in series with the word lines of the driver are in FDD substrate blocks in the module end boards. Each board carries 16 substrate blocks, each containing eight diodes. Figure 2-18 shows the printed circuit on the ends of the boards, and the layout of the isolating diodes.

2.4.7 Decoding the Address Register (Figure 2-19a)

- Bits 11-6 of the address register develop the gate address.
- Bits 5-0 of the address register develop the driver address.
- The binary weight of the address register positions 10-6 gives the gate number.
- The binary weight of the address register positions 10, 9, 8 give the module number 0-7.
- The binary weight of the address register positions 7, 6 give the gate number (0, 1, 2, 3) on each module.
- The binary weight of the address register positions 5-0 gives the driver number.

Gate Decoding: the gate and module numbers can be determined by either of two methods. Once the gate and module numbers are known, the decoder circuit required to develop the module and gate can be found:

1. The binary weight of positions 10-6, gates only, (Figure 2-19b) gives the number of the gate. Example: 11001 = Gate 25. From Figure 2-19b, gate 25 goes to module 6. Decoder outputs of 5 and 20 are required. The switching in the decoder required to give these outputs can now be determined. Note that the relation between gate 25 and decoder outputs 5 and 20 is not significant. Regard the decoder output line number as line labels only.
2. The binary weight of positions 10, 9, 8 gives the module number. The binary weight of positions 7, 6 gives the gate number (0, 1, 2, 3) on each module (Figure 2-19a). For example, module 6 gate 0 is gate 24, module 6 gate 1 is gate 25, etc.

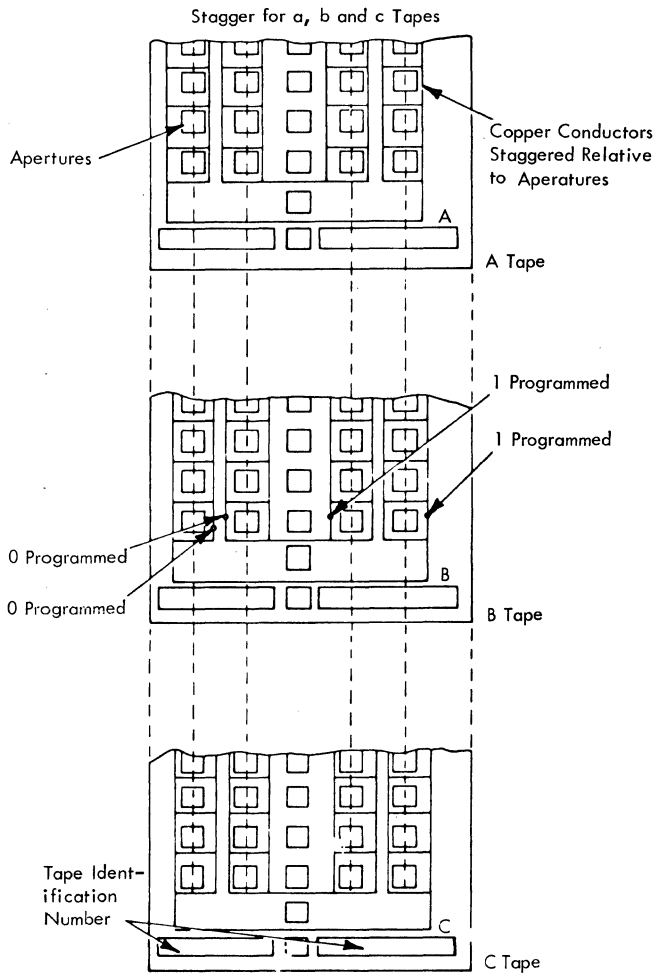
Once the module and gate are determined, the required switching can be found as noted in item 1.

Driver Decoding: the driver number and decoder switching can be determined by either of two methods.

1. The binary weight (address) of positions 5-0 gives the driver number (Figure 2-19c). A study of the matrix, once the driver is known, gives the required decoder output lines. For example, driver 16 requires decoder output lines 0 and 20. The example bit pattern of 010000 gives this decoder output.
2. Bits 2, 1, 0 can be decoded to give the decoder output low order octal digit. Bits 5, 4, 3 can be decoded to give the decoder high order octal digit. Example: In Figure 2-19c, 0 and 20. The interaction of these two lines in the matrix gives driver 16.

Determining Tape Number: After the driver is selected, the tape number can be determined by examining the bit in position 7 (X0). From Figure 2-17, gates 0, 1 select tapes 0 to 63 and gates 2, 3 select tapes 64-127. If X0 is on, gate 2 or 3 is selected and the actual tape number is determined by subtracting the previously determined driver number from 127 (Figure 2-19a). If X0 is off, the driver number equals the tape number.

Determining A or B Word: A or B word on this tape is determined by examining the bit in position 6 (X1). From Figure 2-17, gates 1 and 3 are connected to B



22355A

Figure 2-12. Tape Stagger

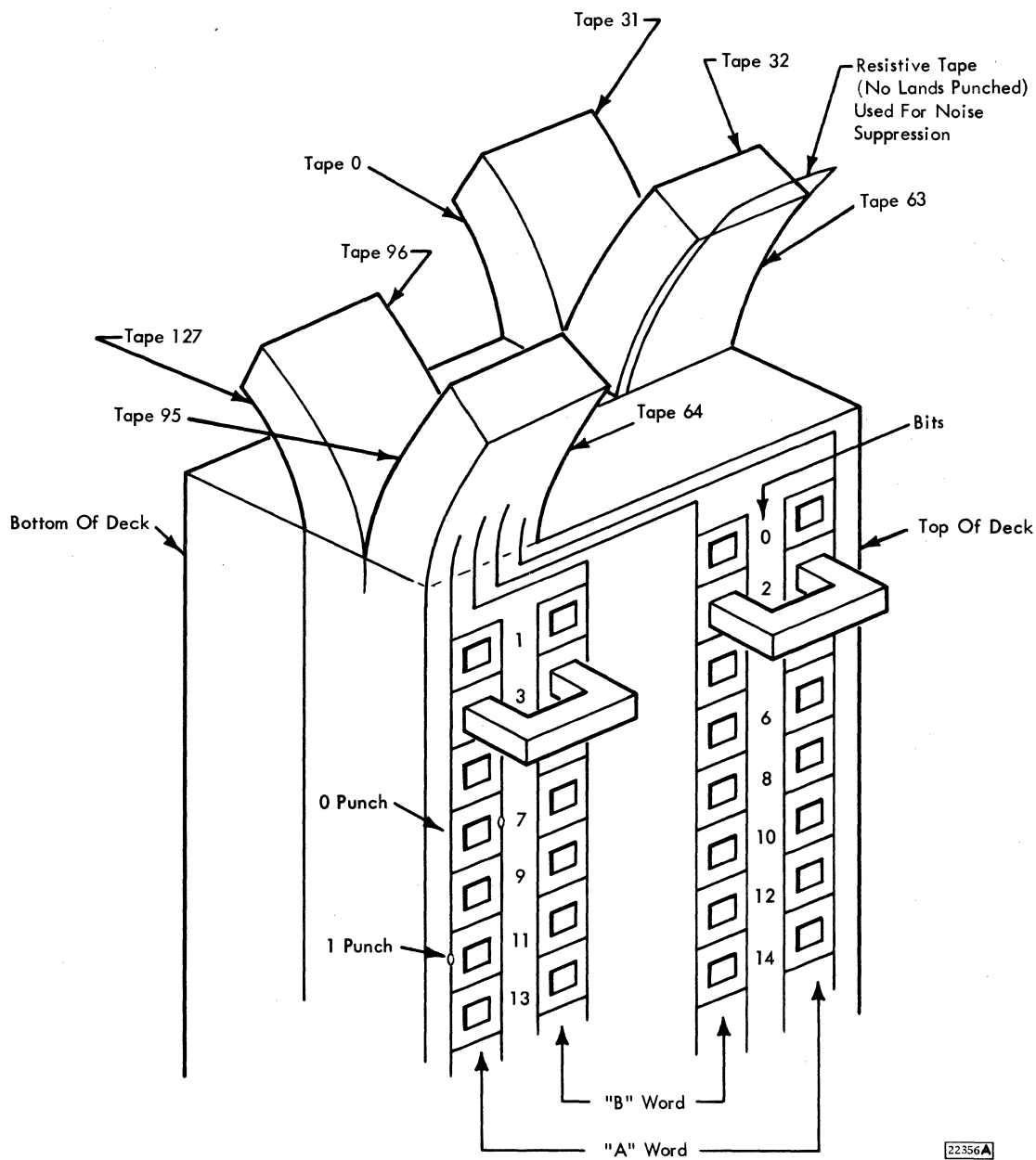


Figure 2-13. TROS Tape Deck

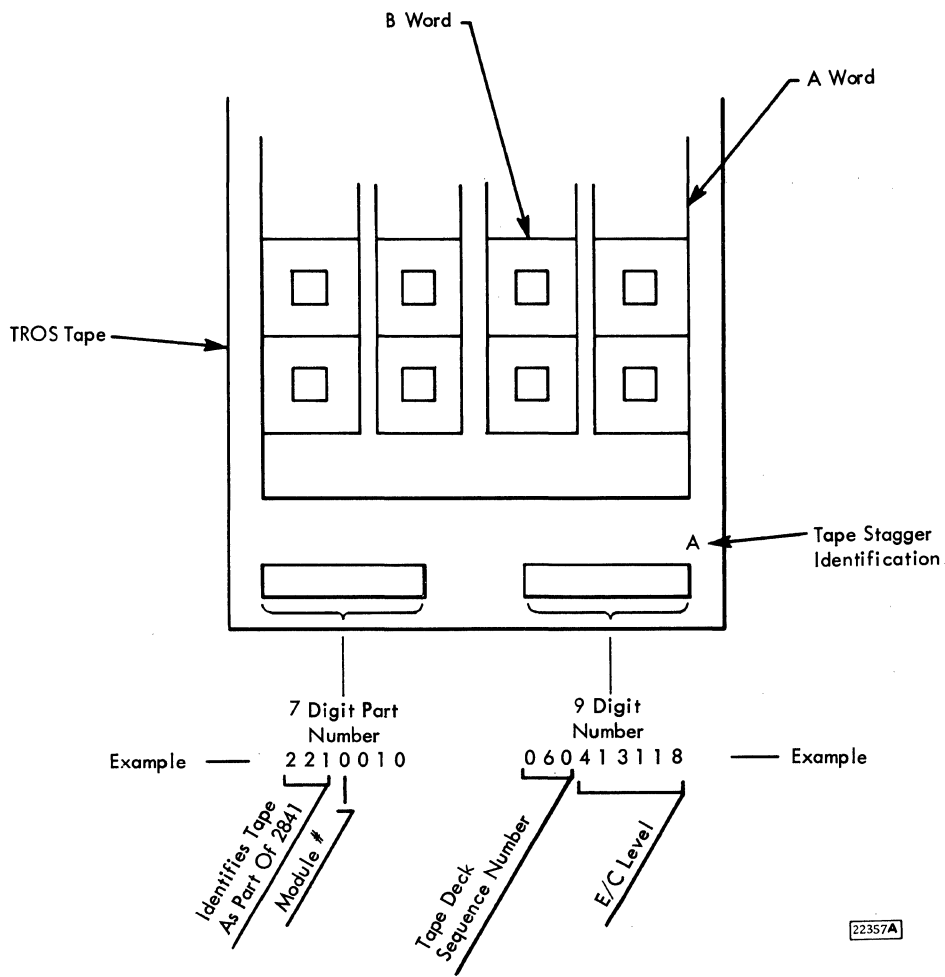


Figure 2-14. TROS Tape Identification

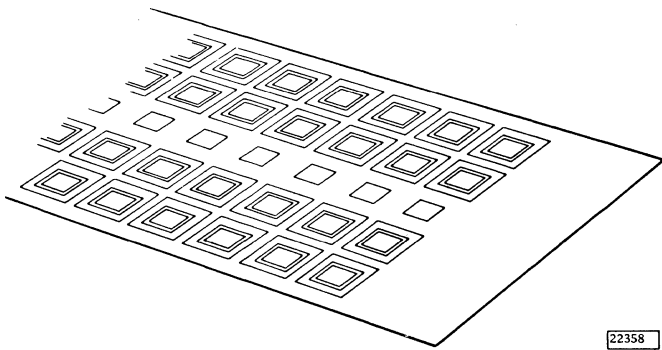


Figure 2-15. Resistance Tape

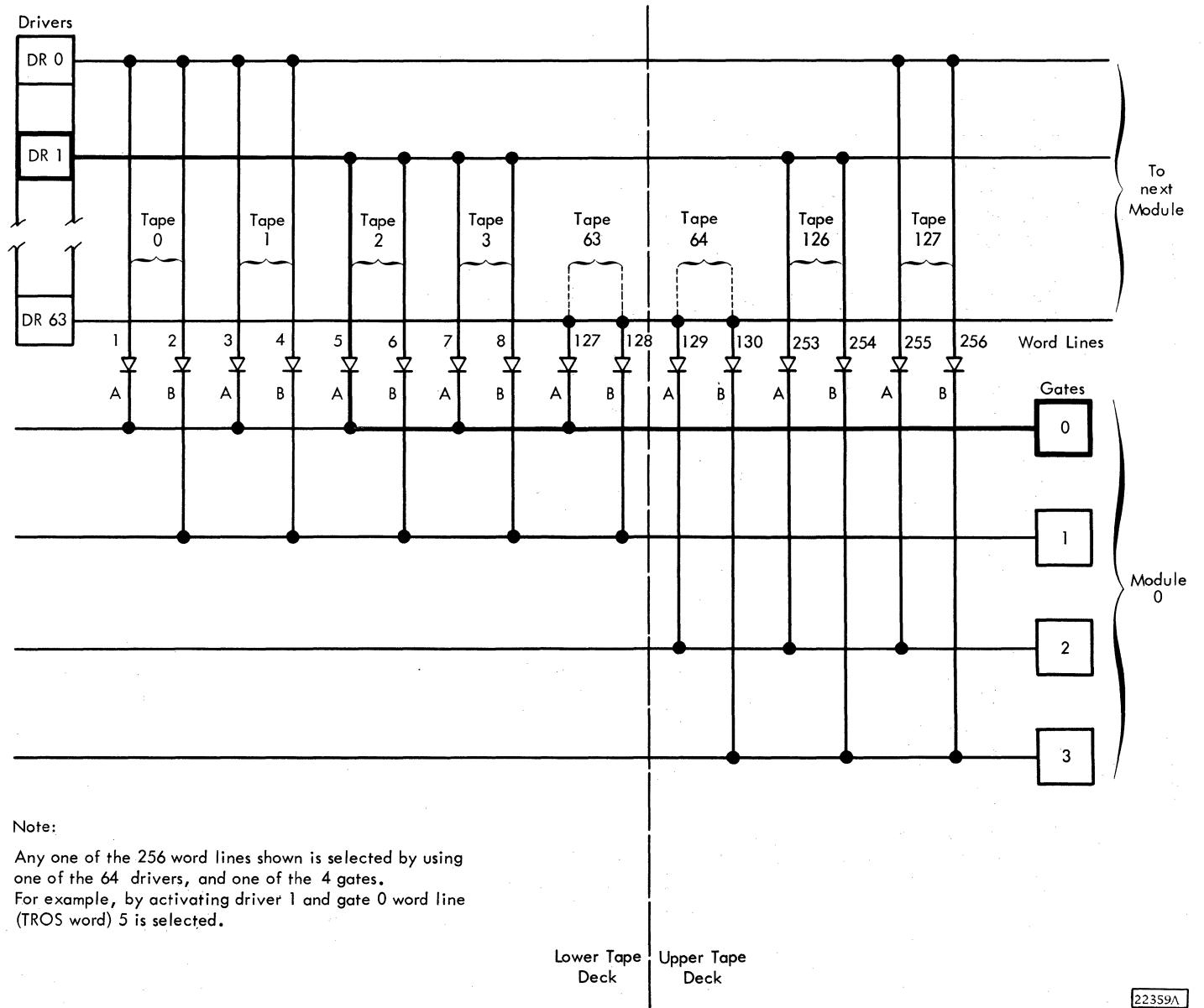


Figure 2-16. Principle of Driving and Gating

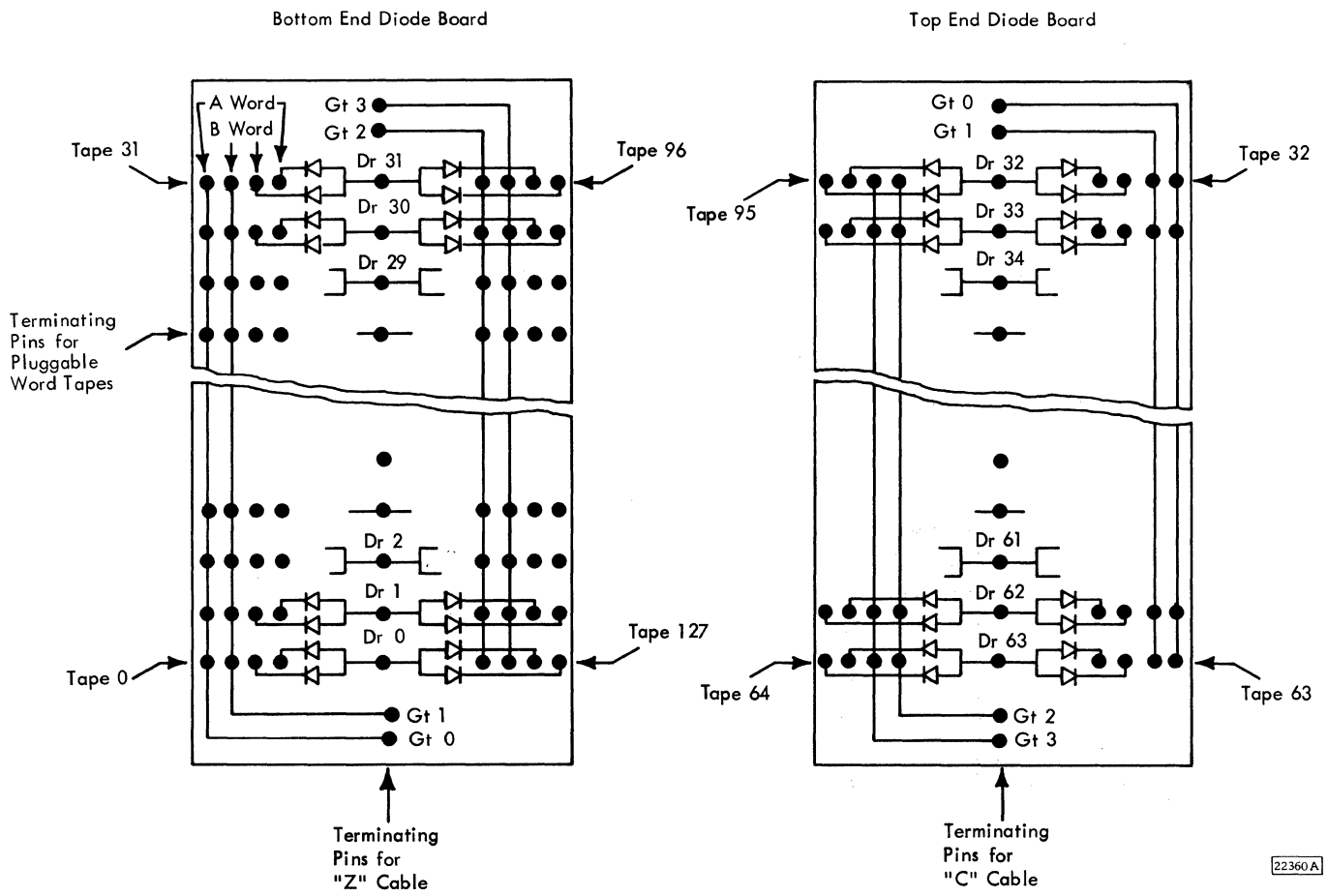
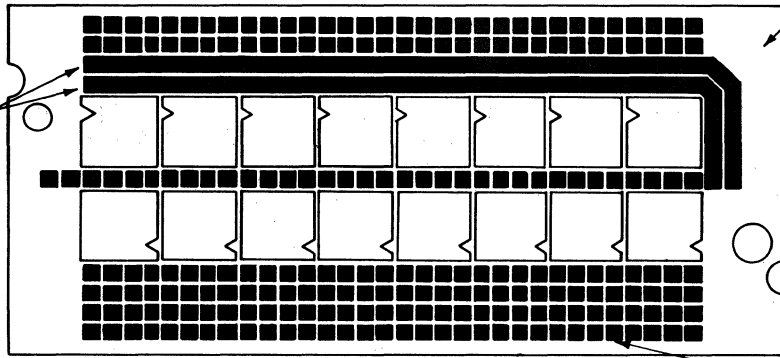
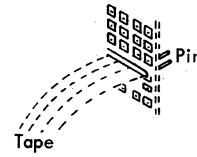
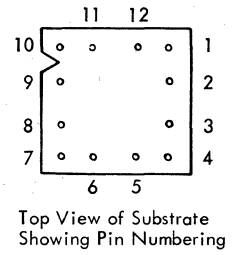
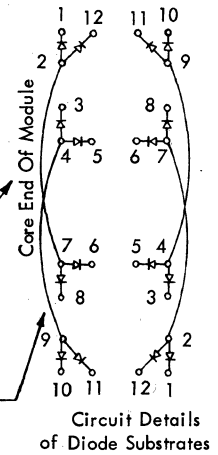


Figure 2-17. Diode Boards on Tape Modules

0.040" Epoxy Glass Laminate
with Etched Copper Land Pattern
on Both Sides



View Showing
Terminations of a
Tape Fitted to Land
Pattern of Card.



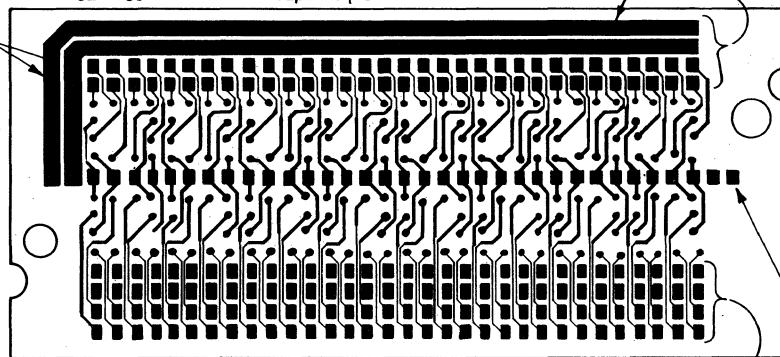
Connector End of Module
Gate
Commoning
Lands

32 33 ----- Tape Sequence Numbers ----- 62 63

All in This Row Thus

All in This Row Thus

Details of Gate and
Driver Wires which are
Connected to the C
Cable Here



95 94 ----- Tape Sequence Numbers ----- 65 64

D D G0 G1 32 33 ----- D D 62 63 G2 G3

Note: All tape positions and tape
cable terminations have plated
through holes between top and
underside land patterns.

22361A

Figure 2-18. Module End Board Showing FDD Sub Strates

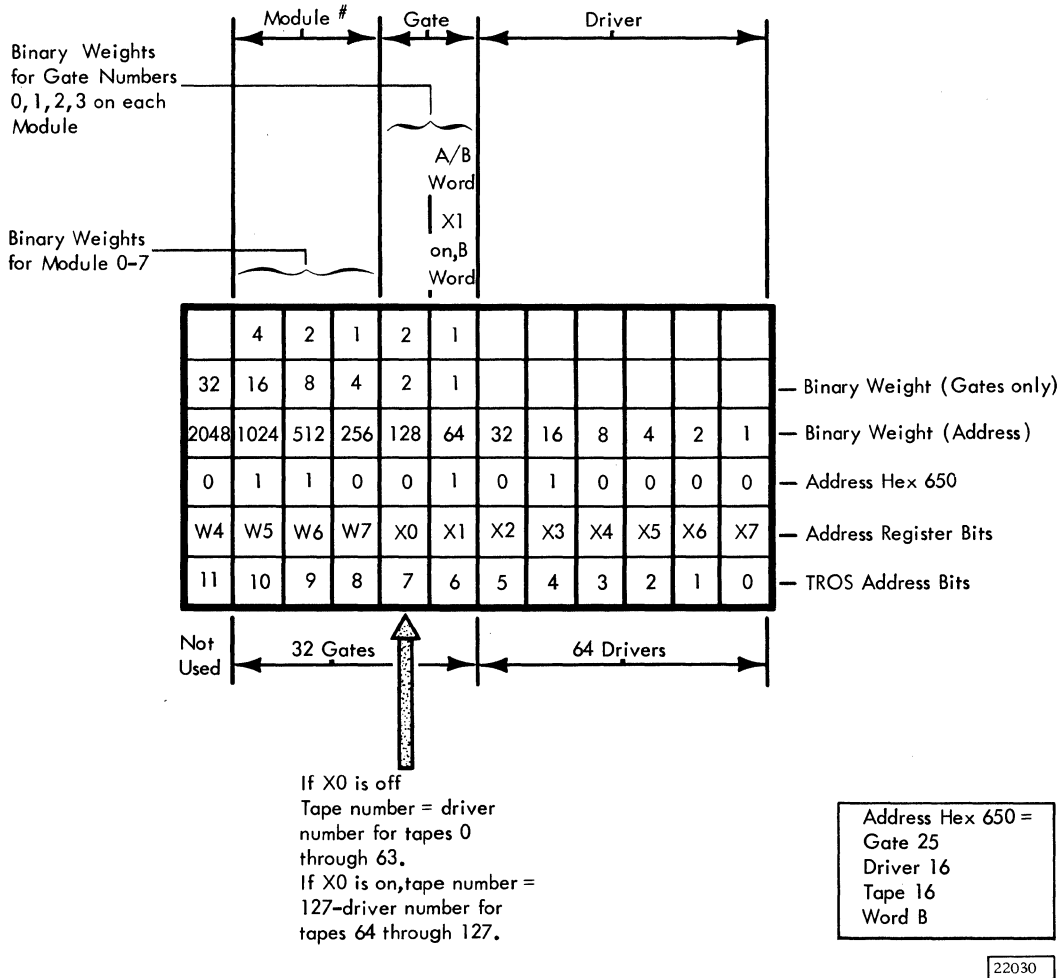


Figure 2-19a. TROS Address Decode

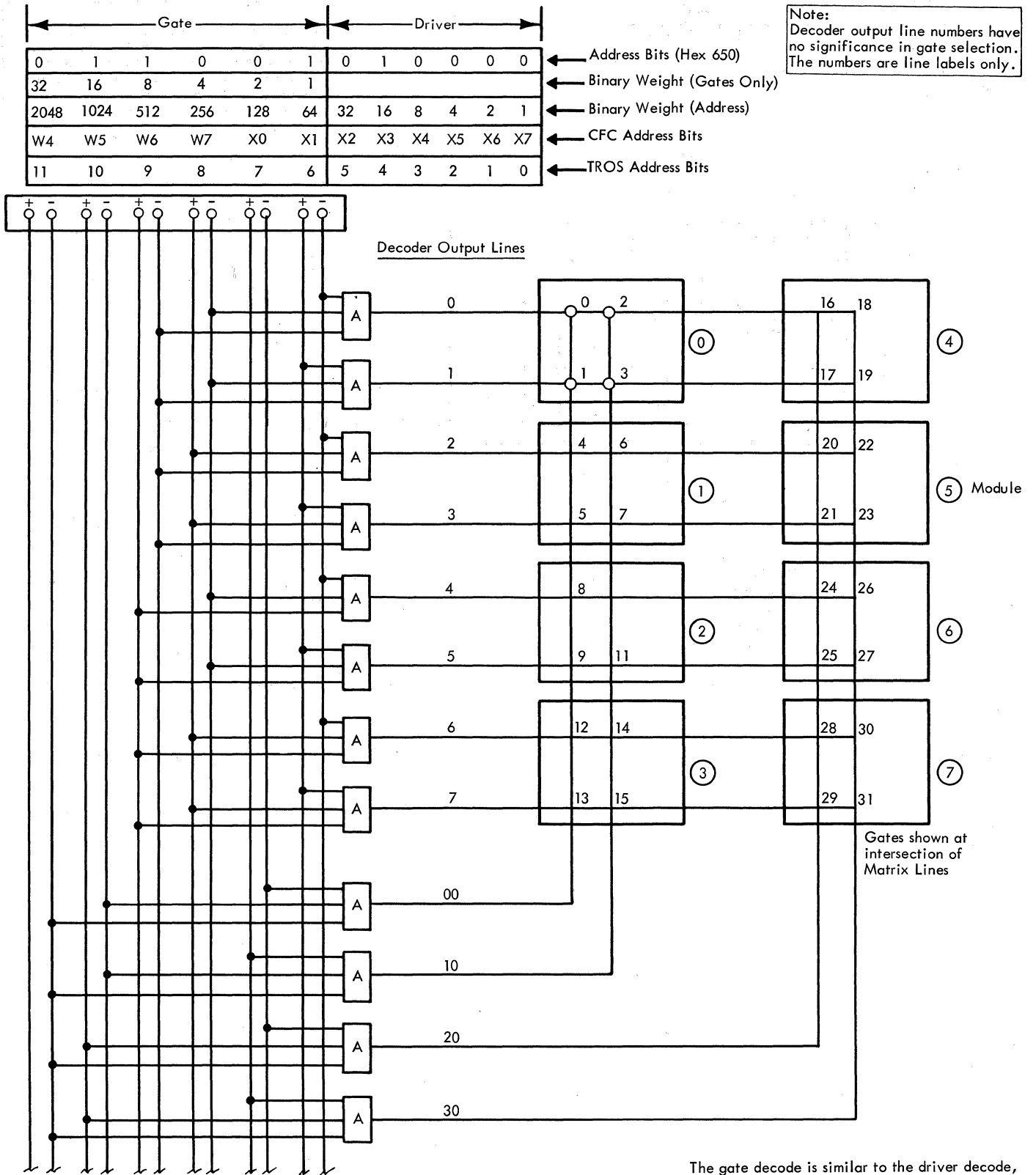
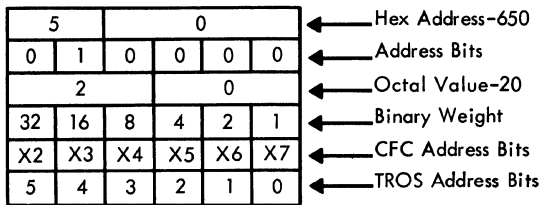
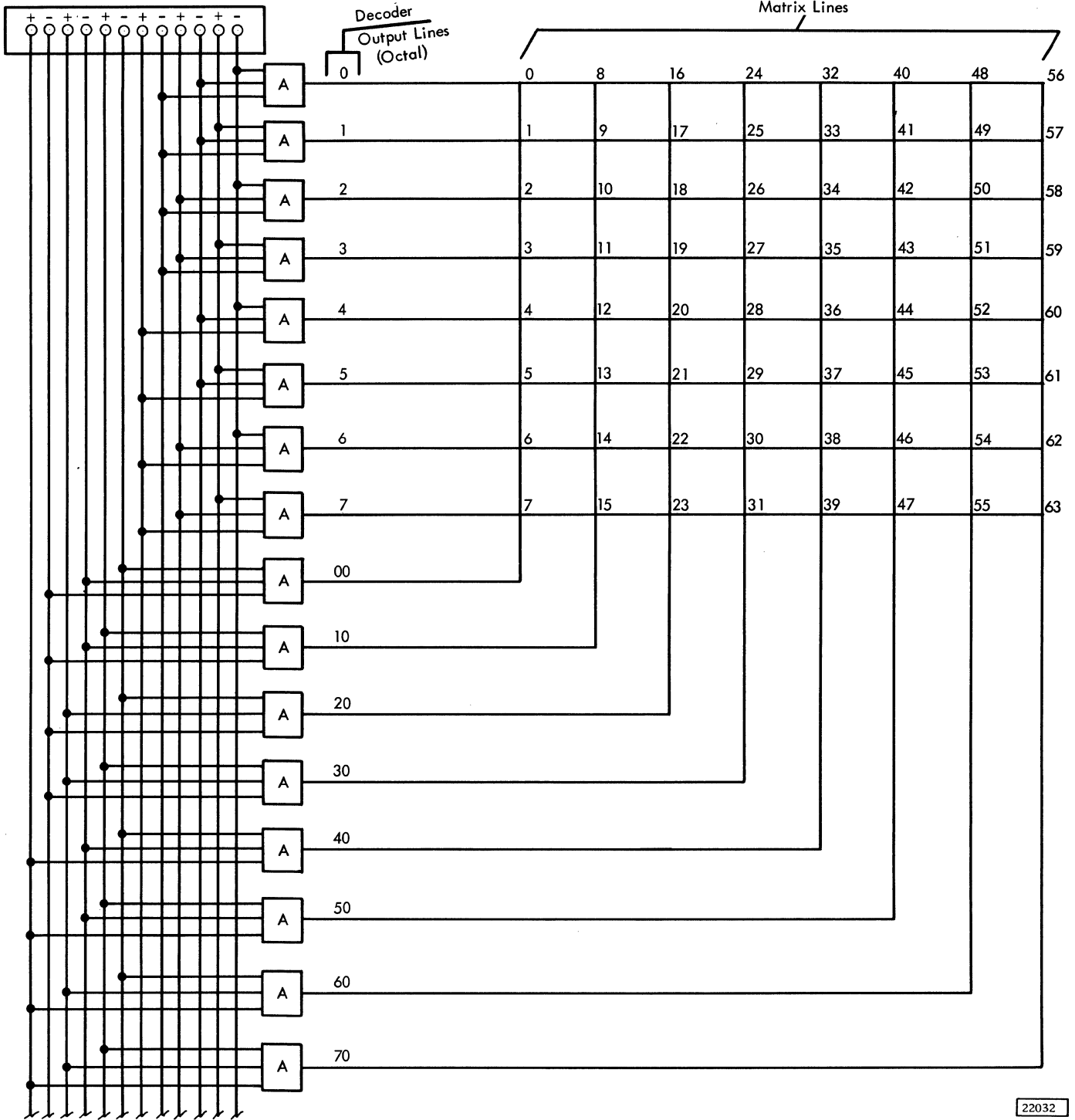


Figure 2-19b. Gate Decode

The gate decode is similar to the driver decode, but it is not a true octal decode. Note the combination of bits used. Thus, two decoder outputs do not combine to give the gate in octal. However, by weighting the six binary bits as shown, the selected lines do give the indicated gate.



Note:
 An octal decode scheme is used. Bits 0, 1, 2 are decoded into the low order octal digit. Bits 3, 4, 5 are decoded into the high order octal digit. The combination of two decoder outputs gives the driver in octal.



22032

Figure 2-19c. Driver Decode

words. If X1 is on, gate 1 or 3 is developed and thus a B-word is addressed.

2.4.8 TROS Functional Operation

- TROS timing is developed from a 2841 clock pulse in a delay line.
- TROS cycle time is 500 ns.
- Voltage level at input to sense amplifier is restored so the sense amplifier can accept information to be read.
- The W and X address registers are decoded to select a gate and driver.
- The gate strobe switches on the selected gate.
- The driver is selected and when the driver strobe comes on, array current flows through the selected word line.
- The sense strobe samples the 48 sense line outputs to turn on the selected sense amplifier.
- Non-selected drivers are isolated by reverse biased diodes.

2.4.8.1 TROS Timing (Figures 2-20 and 2-21)

The timing for TROS is obtained by feeding a 2841 clock pulse to TROS every 500 ns, putting this clock pulse into a series of delay lines, and tapping the delay line at various points to obtain the required time pulses (Figure 2-21).

NOTE: These time pulses are inter-related and a failure at one point in the delay circuitry could alter the entire TROS timing. A procedure for checking the TROS timing is outlined in the IBM Field Engineering Maintenance Manual, 2841 Storage Control Unit (Form 227-3615).

The TROS can continually cycle at a speed of 500 ns. Figure 2-21 shows the internal and external timing of TROS. The cycle starts when a 2841 clock pulse is fed into the delay line.

The sense amplifier is designed so that before a sense pulse appears at the input, the input of the threshold stage must be restored to a controlling level by applying a constant sense restore voltage for a time. The restore circuit is activated by the sense restore strobe.

While the sense amplifier threshold is being restored (Figure 2-21), the W and X Address register is decoded to select a gate and driver as shown on Figure 2-20. When the gate strobe appears at the selected gate, the gate switches on.

Until a driver is selected, no array current can flow. The selected gate has time to bring the 64 word lines connected to its output down to near ground potential, giving a quicker rise of the array current.

Simultaneously with the gate, the driver collector supply is turned on, the driver to be activated is selected, and after the driver strobe has activated the selected driver, the array current starts to flow.

The sense strobe appears at the input to the sense amplifiers about 100 ns after the start of the array current. In these 100 ns the noise of zeros being read dies away while the one's, being much longer, are still present. The sense latches have been reset, and are now set with the new TROS word.

The driver collector supply is turned off, stopping the array current.

2.4.8.2 Isolating Non-selected Drivers

The only forward biased diode at the driver collector supply output is the diode connected to the selected driver. The other seven diodes become reverse biased as soon as the array current starts to flow, isolating the other 56 not-selected drivers.

At this point, the function of the diodes in series with the word lines also becomes apparent; the 63 not-selected word lines connected to the driver have a not-selected gate at their other end. All these gate outputs are positive. When the current starts to flow through the selected word line, the voltage at the driver output drops to 1-2 volts, reverse biasing the 63 diodes of the not-selected word lines, 3-4.5 volts. In this way, the load capacitance formed by the 63 not-selected word lines is isolated from the driver output, resulting in a faster rise of the array current.

2.4.8.3 TROS Inhibit

TROS inhibit, prevents the setting and resetting of the sense latches by inhibiting the generation of the sense reset and sense strobe pulses. The last word set into the sense latches before the rise of inhibit remains unchanged until the fall of inhibit.

2.4.9 Array Layout

- Logic carried on two large boards.
- Logic carried to TROS array via two module connection (commoning) boards.

The general layout of the 2K TROS, as used in the 2841 is shown on Figure 2-22. The entire TROS array is considered as C-gate in the 2841, however the card locations in the ALD's do not reflect this C-gate notation. The decoders, drivers, timing cards, sense amplifiers and sense latches are on the two large boards to the left of the TROS array. These boards are designated A1 and A2, and are considered the A-gate of the TROS.

The connection between the TROS modules and the large circuit boards (A1 and A2) is via the two module connection or commoning boards. These commoning boards are considered the B-gate of the TROS and will carry this notation in the ALD's. All necessary module interconnection wiring for drivers and gates is done on this board. The C and Z paddle connectors from the TROS modules are plugged into the module connection boards that carry the gate circuit cards, and the gate strobe card. There is one gate circuit card for each module, and one gate strobe card for every eight modules.

2.4.10 TROS Output Word

- Output word (48 bits long) split into 15 separate control fields.
- Each control field controls a separate part of the 2841 hardware.

The 48 bit word is split into 15 control fields as follows:

Field CN - output bits 0, 2, 4, 6, 8, 10 - used to provide bits 0 - 5 of the X register for the next word to be addressed in the micro-program.

Field PN - output bit 12 - used to maintain odd parity in the CN field.

Field CD - output bits 14, 16, 18, 20, 22 - used to control the destination of the information on the D bus.

Field CV - output bit 24 - used to gate the true or complement side of the B-register to ALU.

Field CC - output bits 26, 28, 30 - used to control carry functions and logical operation of ALU.

Field CS - output bits 32, 34, 36, 38 - used to control set and reset of the ST register.

Field PC - output bit 40 - used to maintain overall odd parity of the following fields CC, CD, CS, CV, and PA fields.

Field PS - output bit 42 - used to maintain overall odd parity of the following fields, CA, CB, CK, CH, CL and PA fields.

Field BP - output bit 46 - when active (1-bit) the A register is presented directly to the D bus. The A register is also presented directly to the ALU for parity checking. If the output of ALU and the D register do not match, an ALU check is indicated.

Field CH - output bits 1, 3, 5, 7 - used to control the X register bit position 6 for branching purposes.

Field CL - output bits 9, 11, 13, 15 - used to control the X register bit position 7 for branching purposes.

Field CA - output bits 17, 19, 21, 23, 25 - used to control the A register data source.

Field CB - output bits 27, 29 - used to control the B register data source.

Field CK - output bits 31, 33, 35, 37, 39, 41, 43, 45 - used to provide a constant to the B register or W register.

Field PA - output bit 47 - used to check W and X register parity.

Bit 44 - Not used.

2.4.11 Control Latches

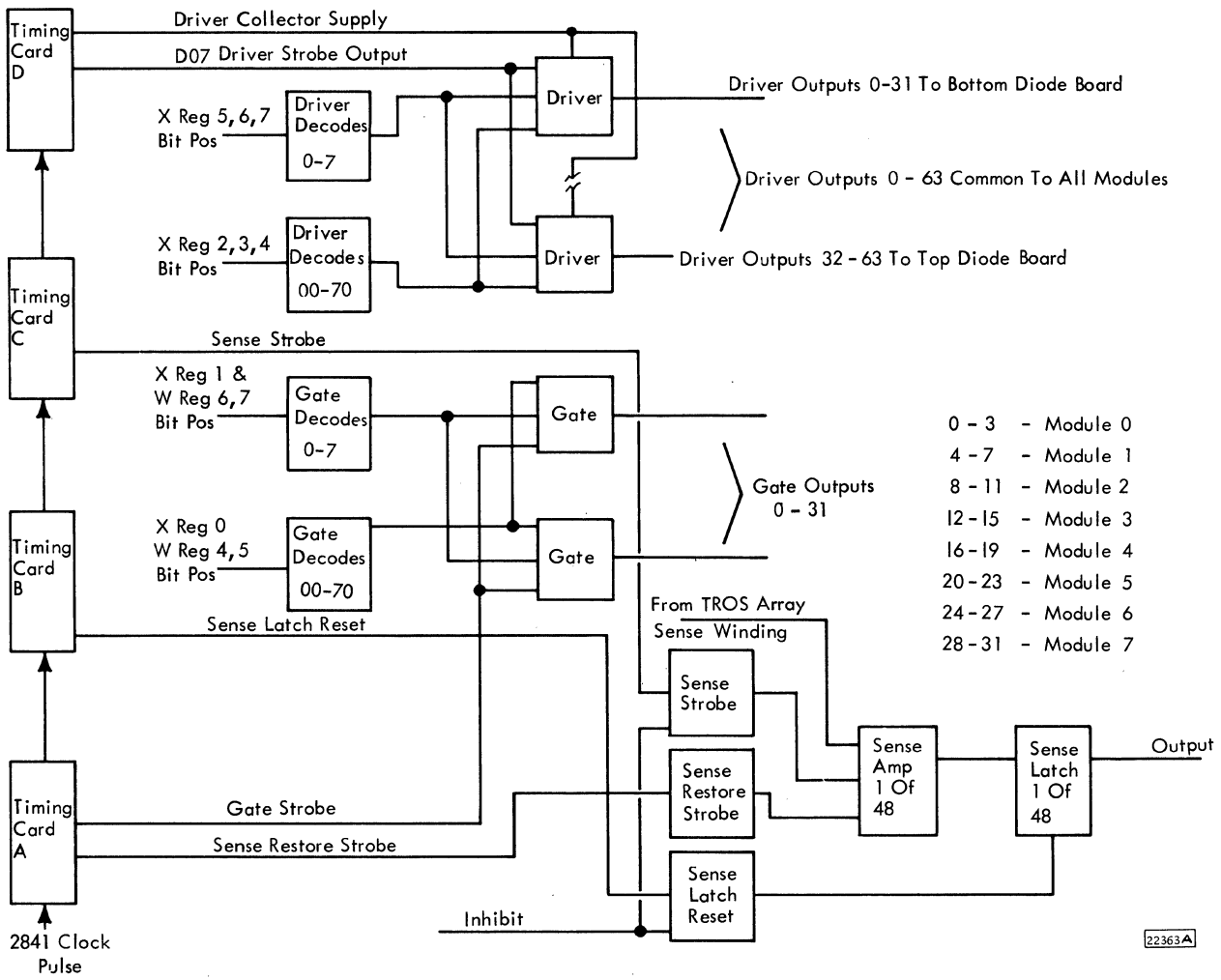
The following fields of the TROS word have control latches, set from the sense latches at Clock 1 time and reset at A time.

CD, CV, CC, CS, CN5

The purpose of the control latch is to have the control field output available for a whole cycle (500 nanoseconds) as the sense latch output is available from D to approximately C time.

2.4.12 TROS Address Check

- Detects internal addressing failure.
- Causes an address check
- 2841 stops with the control word information of the word in which the error occurred.
- 2841 stops with the SALS latches set with the data of the word addressed that was in error.



2-20. TROS Logic Layout

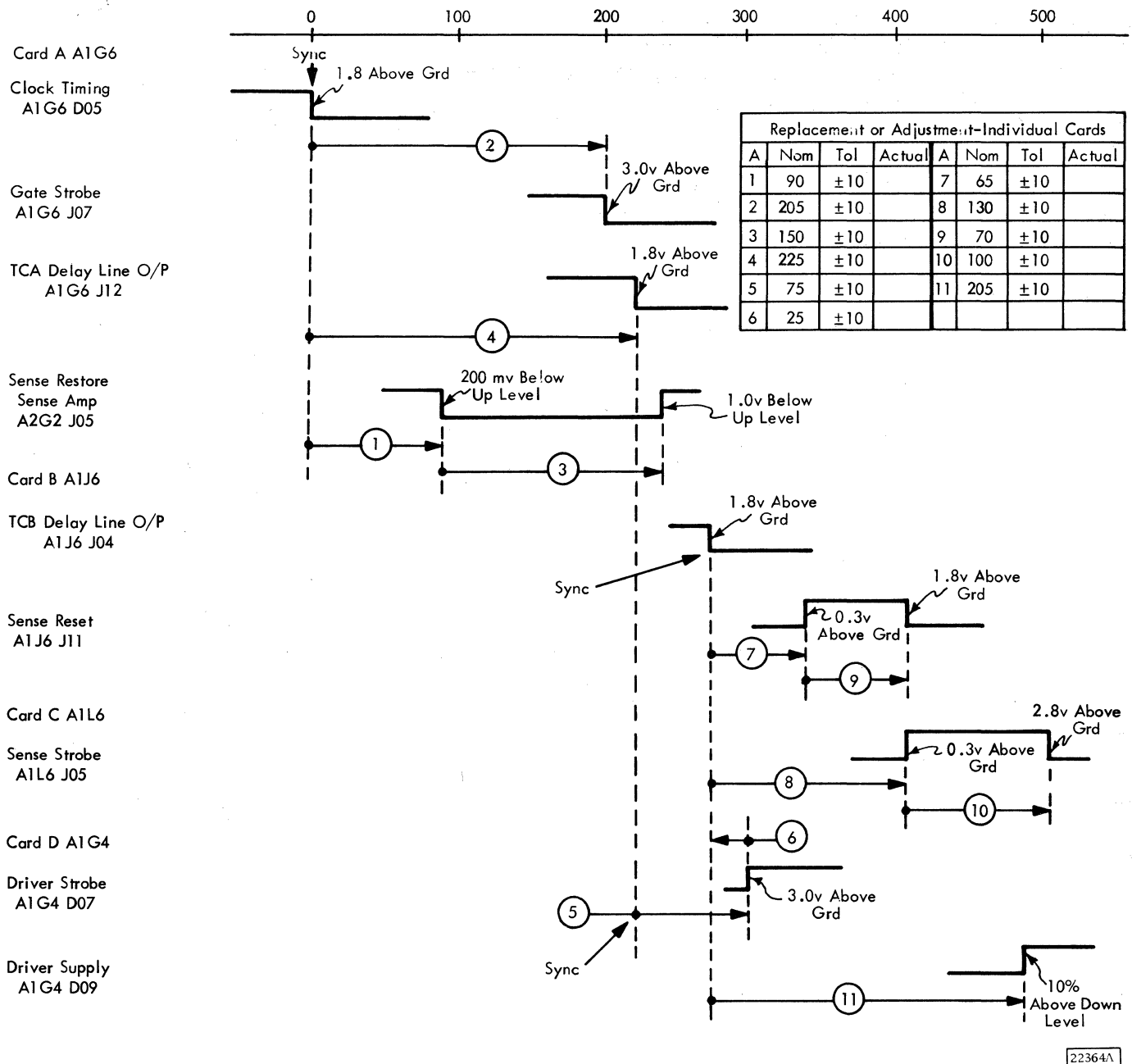


Figure 2-21. TROS Timing

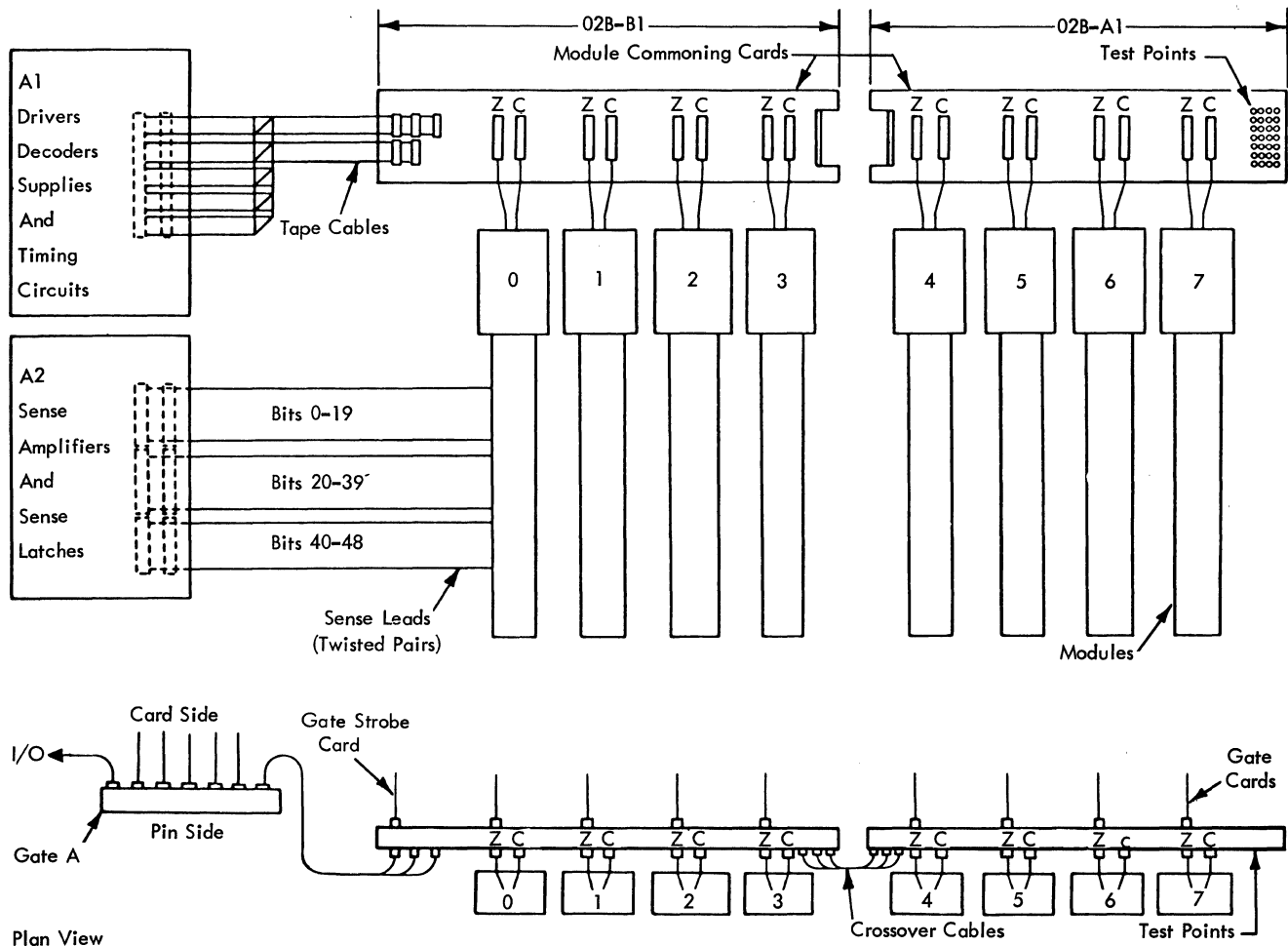


Figure 2-22. General Arrangement of TROS Hardware

22367

The W and X register parity bits are exclusive-Ored and the results set into a polarity hold latch at clock 2 time of every cycle. The output of the polarity hold latch is analyzed along with the PA bit and/or the CN field parity at A time of every cycle (SAL's will be good); if an address check condition is present, the address error latch is set and the 2841 comes to a "hard" stop.

As a result of turning on the address error latch, three inhibit lines are brought up which have the following functions:

1. Inhibit 1 - comes up with address error and prevents the reset and setting of the SALS, the SAL's will therefore contain the information from the word which was in error.
2. Inhibit 2 - comes up with inhibit 1 and clock 3 to block CA, CB and CD latch set and the W and X register set. Since the W and X registers are set at clock 4 time, this is too late to keep the address of the word that actually failed; therefore the W and X registers contain the address of the next word in the micro program, and under an address error condition cannot be relied upon to be correct.
3. Inhibit 3 - comes up with Inhibit 2 and Clock 1 to block further ALU output.

2.4.13 TROS Sense Amplifier Check

- Detects failure of SALS in certain fields of the TROS word.
- Even bit count causes a Sense Amp Error.

The CA, CB, CK, CL, CH, PS, and PA fields are checked for a total odd bit count at A time of every cycle. The PS bit is punched in the TROS tape to make the total bit count odd. A total even bit count causes the sense amp error latch to turn on at an A-time and the 2841 to come to a hard stop. Once the Sense Amp Error latch is set, the sequence of bringing up the inhibit lines is the same as described for ROS address check. The sense amp error will be indicated on the CE console, along with the address of the next word in the micro program. The information in the SALS will be that of the word in which the error occurred.

2.4.14 TROS Control Register Check

- Detects failure of the SALS in those fields of the TROS word which feed the Control register latches.

- Even bit count causes a Control register check.

The CC, CD, CV, CS, PC, BP fields are checked for a total odd bit count at A time of every cycle. The PC bit is punched in the TROS tape to make the total bit count odd. A total even bit count causes the control register error latch to turn on at A time and the 2841 to come to a hard stop. Once the control register error latch is set, the sequence of bringing up the inhibit lines is the same as described for ROS address check. The control register error will be indicated on the CE console, along with the address of the next word in the microprogram. The information in the SALS will be that of the word in which the error occurred.

2.5 ARITHMETIC/LOGICAL UNIT (ALU)

- ALU has inputs from the A and B register and carry control.
- The B register entry may be in true or ones complement form. This is controlled by the CV field decode.
- ALU can:

Add, Subtract (Add with one's complement input from the "B" register), AND, OR, and Exclusive OR.

- The type of ALU function is controlled by the CC field decode.
- The output of ALU is placed on the D Bus. It may be directed to any of the general purpose registers under microprogram control.
- ALU output may be tested for zero by the microprogram.
- ALU output of not zero may be used to turn on status register, Bit 2.
- A carry out of the high order position may be used to turn on status register, Bit 3.
- ALU generates correct odd parity anytime it performs an operation.
- ALU may be bypassed by the bypass microprogram statement.

2.5.1 ALU General Description (Figure 2-23)

The arithmetic/logic unit (ALU) is used to perform add, subtract, AND, OR, and exclusive OR operations

within the 2841. It also assigns parity (odd) to data passing through it.

Inputs to ALU are from the A Reg, B Reg, and the carry in latch. The input from the B Reg may be in true or one's complement form. This is determined by the CV field decode section of the ROS word. The type of operation performed by the ALU is determined by the CC field decode section of the ROS word. There are eight different ALU (CC decode) operations.

The output of ALU can be gated to the D Bus. In addition two latches, D equal zero and Carry Out, monitor the results of the ALU operations and may be tested by the microprogram.

The A register can be transferred to the D Bus directly, thereby, bypassing ALU. This operation is effected by placing bit 46 (bypass) of the ROS word On. When bypassing ALU, the ALU will still receive the A and B register inputs. The ALU will compute parity for the byte. If the A register parity does not agree with the ALU computed parity (parity bits only are compared), and ALU check latch will turn on stopping TROS and lighting the data check lamp. The A to D transfer is negated if bus out parity occurred on the byte. In this case the byte will go through ALU to the D Bus. ALU will correct parity. The microprogram will remember that bus out parity occurred by means of the ER register, bit 2 latch.

Five symbols are used to represent the five arithmetic operations of ALU:

- + True Add/Positive
- Complement Add/Subtract
- . AND - Logical
- Ω OR
- * Exclusive OR

2.5.2 Summary of ALU Statements (No ALU bypass) (Refer to CLD page QA004)

CC Decode of 000: A CC decode of zero causes the ALU to add/subtract the A and B register outputs with a carry in of zero from the carry in latch. The CC decode of 000 does not set the carry out in status register 3. This operation is represented symbolically as follows:

$-A \pm B + 0 \rightarrow D$ Note: Carry in of zero does not always appear in ALU statement

For example:

$$DR = 163_{(10)}, KL = 29_{(10)}$$

ALU statement $KL + DR \rightarrow GL$

A reg Input (KL)	00011101	-	29	
B reg Input (DR)	10100011	-	163	₍₁₀₎
D Bus Output (GL)	11000000	-	192	₍₁₀₎

CC decode of 001: A CC decode of one causes ALU to add/subtract the A and B register output with a carry in of one from the carry in latch. The CC decode of 001 does not set status register 3. This operation is represented symbolically as follows:

$A \pm B + 1 \rightarrow D$

For example:

$$BY = 143_{(10)}, DH = 7_{(10)}$$

ALU statement $DH + BY + 1 \rightarrow BX$

A Reg Input (DH)	10001111		143	
B Reg Input (BY)	00000111		7	₍₁₀₎
Carry In		1	1	
D Bus Output (BX)	10010111		151	₍₁₀₎

CC Decode of 010: A CC decode of two causes ALU to AND the A and B register outputs. This operation is represented symbolically as follows:

$A \cdot B \rightarrow D$ Note: The B register may be gated in complement. In this case the statement symbolically would be:

$A \cdot \bar{B} \rightarrow D$

For example:

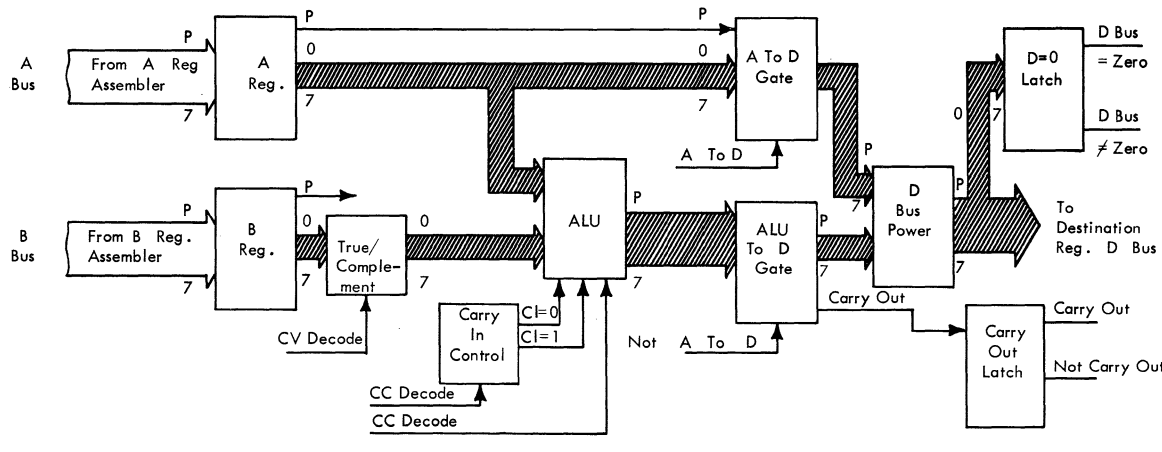
$$KL = 181_{(10)}, DR = 52_{(10)}$$

ALU statement $KL \cdot DR \rightarrow GL$

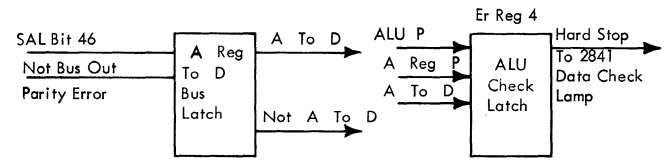
A Reg Input (KL)	10110101		181	
B Reg Input (DR)	00111000		52	₍₁₀₎
D Bus Output (GL)	00110000		48	₍₁₀₎

CC Decode of 011: A CC decode of three causes ALU to OR the A and B register outputs. This operation is represented symbolically as follows:

$A \Omega B \rightarrow D$



C.V. FIELD 1 BITS	
Bit 0	
0	True B Register Input
1	Complement B Input



	ALU CONTROL LINES					
	LM	\overline{LM}	N	\overline{N}	Connect	$\overline{Connect}$
Add	Off	On	On	Off	Off	On
Exclusive Or	Off	On	On	Off	On	Off
And	On	Off	Off	On	On	Off
Or	Off	On	Off	On	On -	Off

C C FIELD 3 BITS			
Bit 0	Bit 1	Bit 2	
0	0	0	Add Operation - No Forced Carry In - No Carry Out To St 3
0	0	1	Add Operation - Force Carry In - No Carry Out To St 3
0	1	0	And Operation
0	1	1	Or Operation
1	0	0	Add Operation - No Forced Carry In - Latch Carry Out To St 3
1	0	1	Add Operation - Force Carry In - Latch Carry Out To St 3
1	1	0	Add Operation - Add In St 3 - Latch Carry Out To St 3
1	1	1	Exclusive Or

22377A

Figure 2-23. ALU Block Diagram and Control

Note: The B register may be gated in complement. In this case the statement symbolically would be:

$$A \ominus B \rightarrow D$$

For example:

$$BY = 29_{(10)}, GP = 207_{(10)}$$

ALU statement $GP \ominus BY \rightarrow KL$

A Reg Input GP	11001111	207	(10)
B Reg Input (BY)	00011101	29	(10)
D Bus Output (KL)	11011111	223	(10)

CC Decode of 100: A CC decode of four causes ALU to add/subtract the A and B register outputs with a carry in of zero from the carry in latch. The carry out from the high order position of ALU is stored in status register 3. This operation is represented symbolically as follows:

$$A \pm B + 0 \rightarrow DC$$

Note: The carry in of zero may not be shown. The C on the left side of the equal sign means store the carry out in status register, bit 3.

For example:

$$\#1: DR = 19_{(10)}, BX = 128_{(10)}$$

ALU statement $BX + DR \rightarrow GLC$

A Reg Input (BX)	10000000	128	(10)
B Reg Input (DR)	00010011	19	(10)
D Bus Output (GL)	10010011	147	(10)

(No carry out.
Reset ST 3.)

$$\#2: DR = 93_{(10)}, BX = 204_{(10)}$$

ALU statement $BX + DR \rightarrow GLC$

A Reg Input (BX)	11001100	204	(10)
B Reg Input (DR)	01011101	93	(10)
D Bus Output (GL)C←	00101001	41	(10)

(Carry Out of
one Set ST 3.)

CC Decode of 101: A CC decode of five causes ALU to add/subtract the A and B register outputs with a

carry in of one from the carry in latch. The carry out from the high order position of ALU is stored in status register 3. This operation is represented symbolically as follows:

$$A \pm B + 1 \rightarrow DC$$

For example:

$$BY = 223_{(10)}, OP = 32_{(10)}$$

ALU statement $OP + BY + 1 \rightarrow BYC$

A Reg Input (OP)	00100000	32	(10)
B Reg Input (BY)	11011111	223	(10)
Carry In (1)	1	1	
D Bus Output (BY) C←	00000000	0	

(Carry out of one.
Set ST 3.)

CC Decode of 110: A CC decode of six causes ALU to add/subtract the A and B register outputs with a carry in equal to the present condition of status register 3. The carry out from the high order position of ALU is stored in status register 3. This operation is represented symbolically as follows:

$$A \pm B + C \rightarrow DC$$

Note: A "C" in the carry in position of the ALU statement means to use the present condition of ST3 as the carry in to the low order position of the ALU.

For example:

$$DR = 28_{(10)}, KL = 36_{(10)}, ST 3 = 1$$

ALU statement $KL + DR + C \rightarrow GPC$

A Reg Input (KL)	00100100	36	(10)
B Reg Input (DR)	00011100	28	(10)
Carry In (ST 3)	1	1	
D Bus Output (GP)	01000001	65	(10)

(No carry out.
ST 3 reset
at end of
operation.)

CC Decode of 111: A CC decode of seven causes the ALU to exclusive OR the A and B register outputs.

This operation is represented symbolically as follows:

$$A \nabla B \rightarrow D$$

NOTE: The B register may be gated in complement form. In this case the symbolic statement is:

$$A \nabla -B \rightarrow D$$

For example:

$$BY = 53_{(10)}, \quad GL = 150_{(10)}$$

ALU statement $GL \nabla BY \rightarrow KL$

A Reg Input (GL)	10010110	150	(10)
B Reg Input (BY)	00110101	53	(10)
D Bus Output (KL)	10100011	163	(10)

Subtract Functions: The five different add/subtract functions can be made into subtract functions by transferring the complement of the B register to ALU. This is accomplished by making the CV field decode equal to one.

For example:

$$GL = 38_{(10)}, \quad BY = 24_{(10)}$$

ALU statement $GL - BY \rightarrow KL$

A Reg Input (GL)	00100110	00100110	
B Reg Input (BY)	00011000 complement	11100111	
		C ← 00001101	
			$13_{(10)}$

Notice that the answer is $13_{(10)}$ and is off by one. This is because one's complement subtraction is used. Notice also that there was a carry out. This sets the carry out latch in the ALU. The carry out latch can be tested by the microprogram. If the microprogram is interested in the true result it can obtain it by either adding one to the KL register, or by executing the ALU statement:

$GL - BY + 1 \rightarrow KL$

A Reg Input (GL)	00100110	
B Reg Input (BY)	00011000 complement	11100111
Carry In (1)		1
D Bus Output (KL)	C ← 00001110	14
		(10)

Note: Twos complement subtraction.

2.5.3 Functional Description and Basic Timing (Figure 2-23 and 2-24).

Functionally the operation of the ALU can be thought of as beginning in D time of the previous machine cycle (a machine cycle is A, B, C, and D time). During this time, CA and CB fields of ROS are decoded. They control the gating of information to the A and B buses.

A Time

1. A and B buses gated to A and B registers. The A and B registers are latched up.
2. The CC, CV, and CD field decodes are reset and set. The set overrides the reset.
3. The applicable ALU control lines (LM, \overline{LM} , N, \overline{N} , Connect, $\overline{Connect}$) rise and ALU begins performing the arithmetic function.

B Time

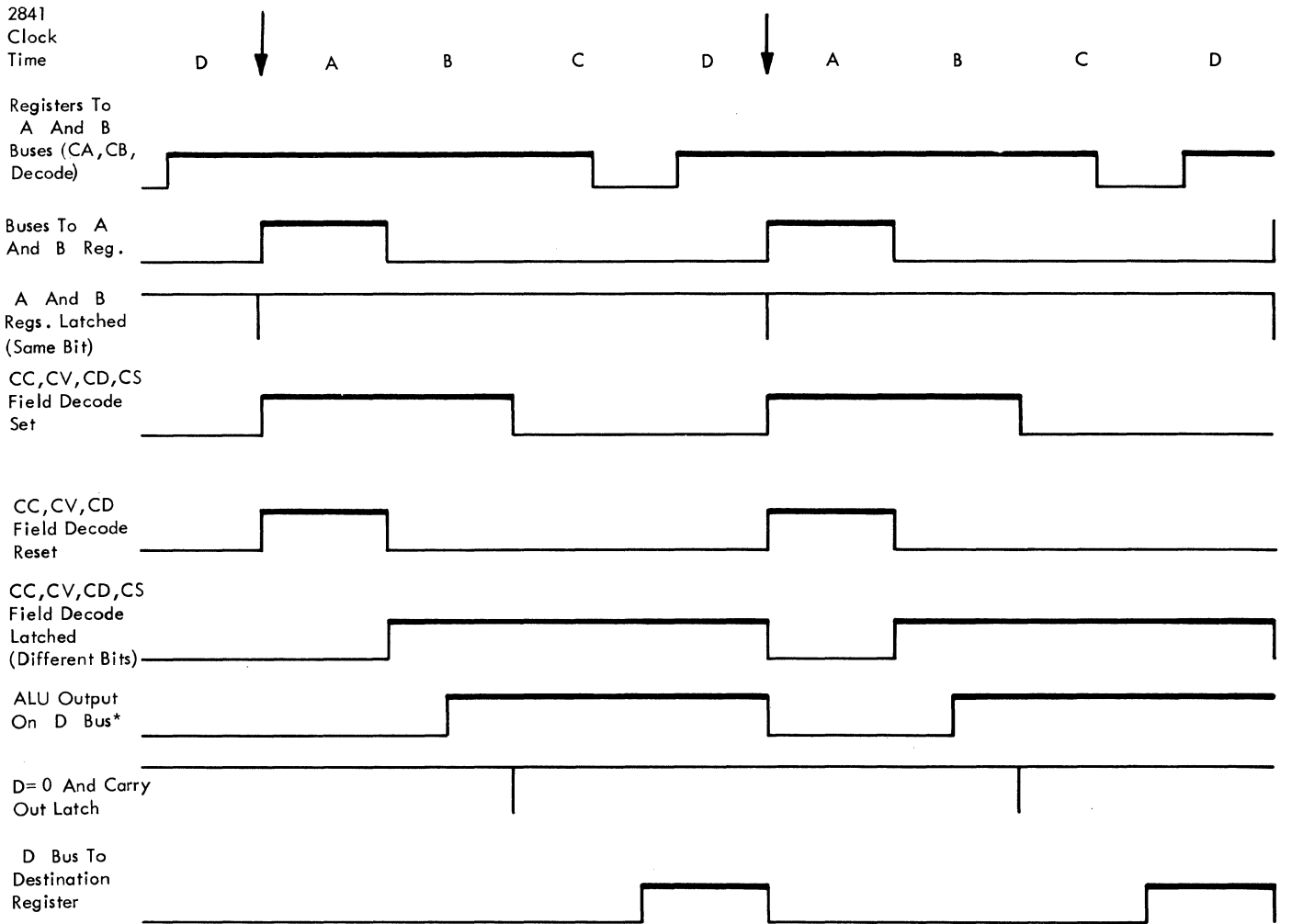
1. The CC, CV, CD reset is removed. These latches remain latched through D time.
2. ALU finishes the arithmetic operation. The answer is now on the D bus.

C Time

1. The D bus is sampled for zero. If it is zero, the D = 0 latch is set.
2. Carry out from the high order position of ALU is sampled. If there is a carry out, the carry out latch will be set.
3. CA and CB decodes are reset.

D Time

1. The register (if any) designated by the CD field is loaded with the output of ALU.
2. Status register 3 is set or reset if the arithmetic operation was one which stored the carry out in ST 3 ($\rightarrow DC$).
3. Status register 2 is set now if the ROS word contained a DNST 21 statement and the D bus did not equal zero.
4. The next ROS word is now available for field decoding.



* Could be A Register if ALU Bypass On

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Figure 2-24. ALU Basic Timing

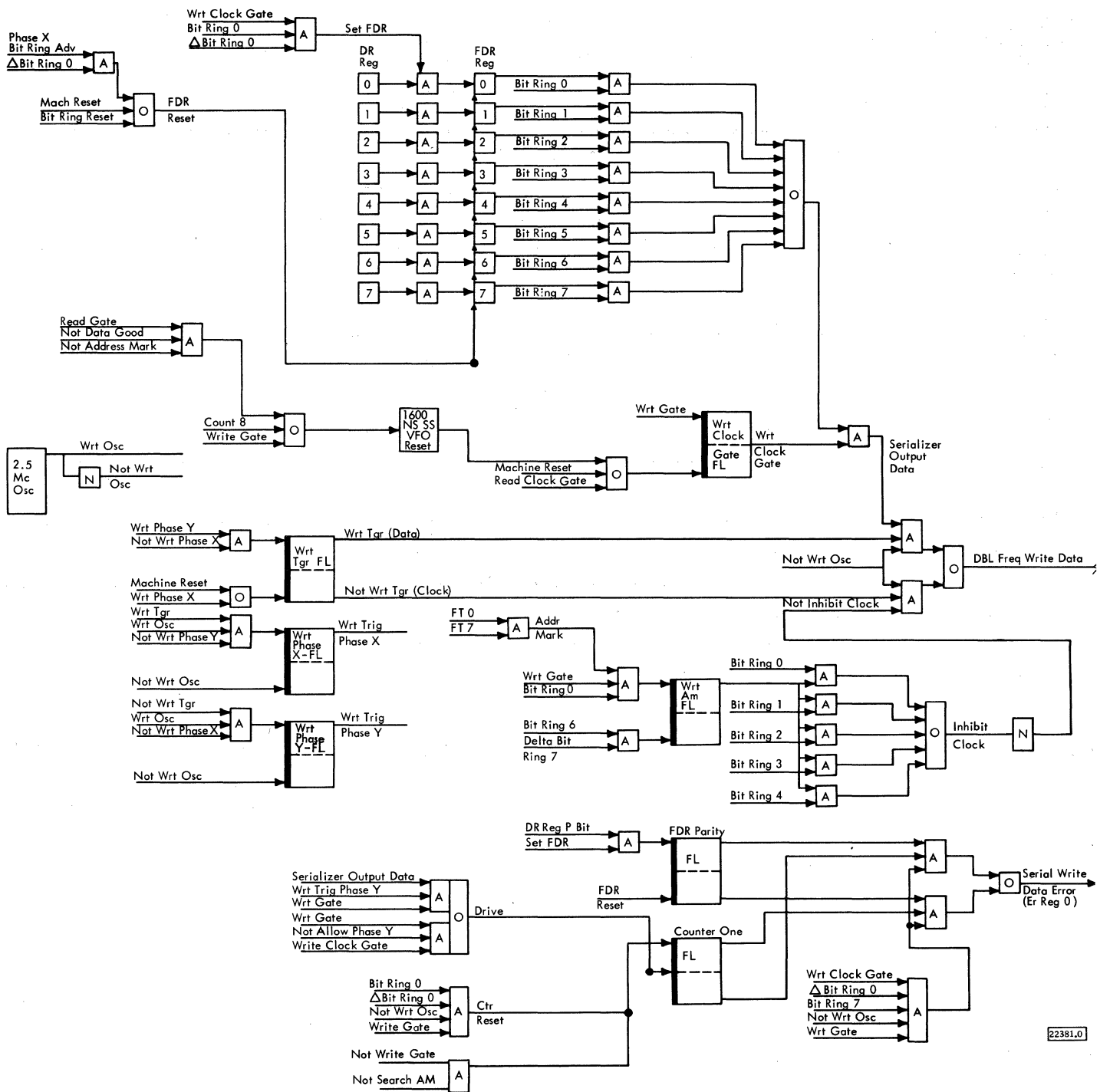
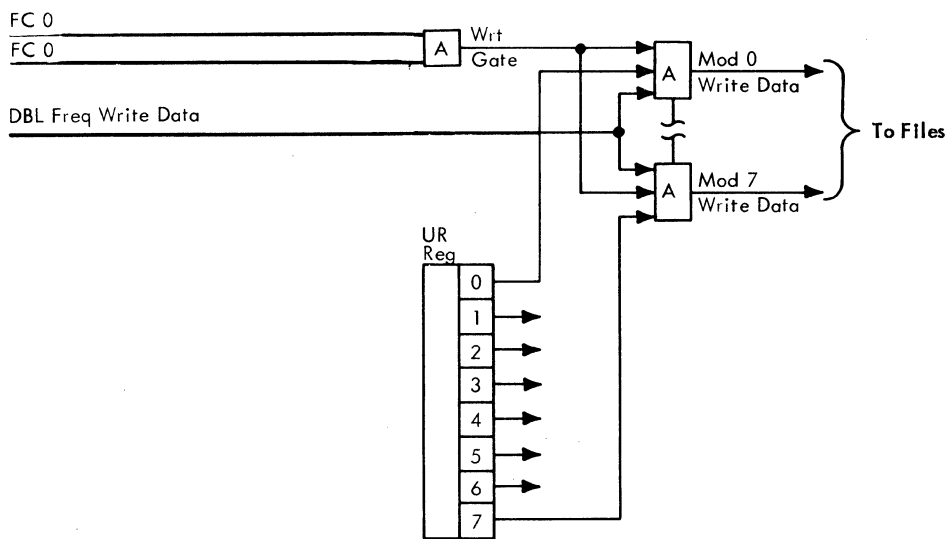
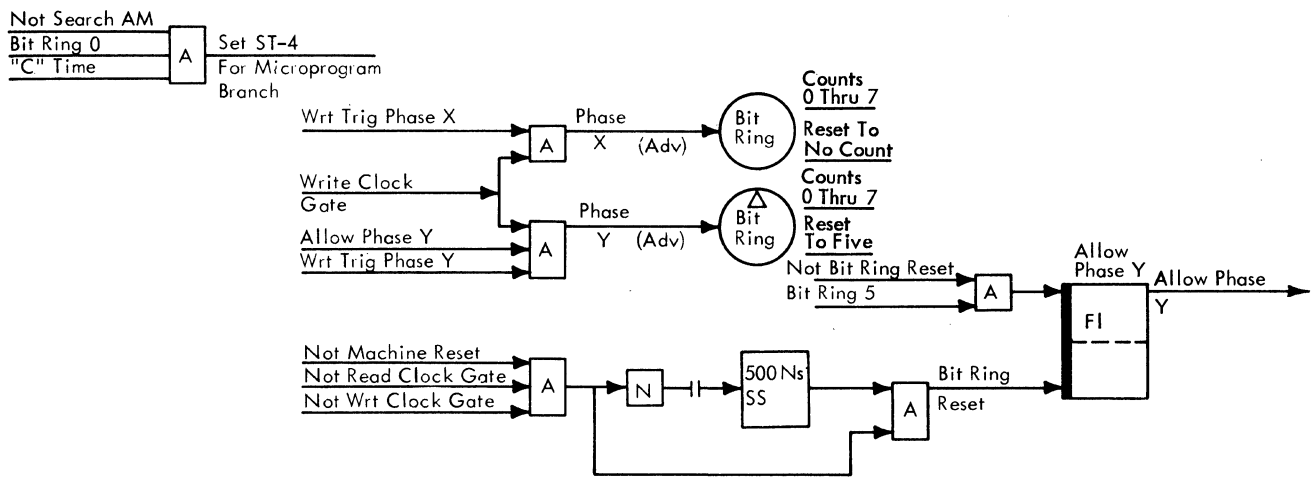


Figure 2-25. SERDES Write Circuits



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Figure 2-25. SERDES Write Circuits

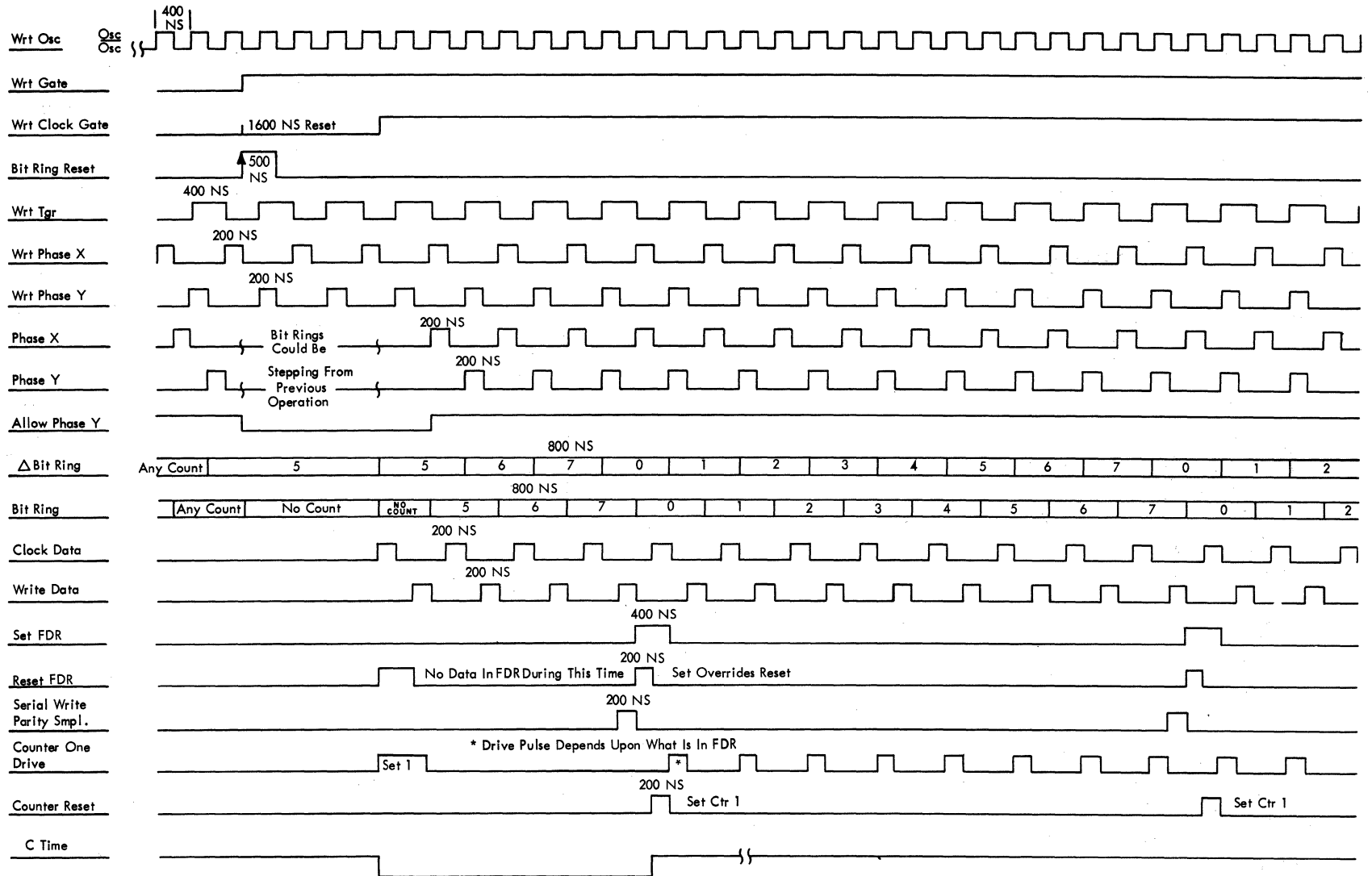


Figure 2-26. SERDES Write Timing Chart

ALU Bypass

If the microprogram is using ALU Bypass, the ALU statement will appear as follows:

A + B → D Bypass

The bypass appearing in the ALU statement means that bit 46 of the ROS word is a one. All ALU times remain the same with the exception that the A register is gated to the D bus.

If the ALU computed parity does not agree with A register parity, the ALU check latch is turned on, stopping the 2841 TROS unit.

IP bypass statements appear only in blocks that do not have a B register entry statement.

2.6 SERIALIZER/DESERIALIZER UNIT

- Changes parallel-by-byte data to serial-by-bit data when writing on the disk storage.
- Changes serial-by-bit data to parallel-by-byte data when reading from the disk storage.
- Generates clock pulses used in NRZI double frequency writing.
- Separates data from clock pulses when reading.
- Checks byte parity when writing.
- Finds address markers under control of the microprogram.

2.6.1 SERDES General Description

The serializer deserializer unit (SERDES) is used for the writing and reading of data on disk storage.

SERDES is controlled externally by the microprogram with three lines. (Figures 2-3 and 2-4.

1. Read Gate.
2. Write Gate.
3. Address Marker Search Line.

Read gate on enables SERDES to read data from the selected device.

Read gate on and the address marker search line up cause SERDES to look for an address marker in the data coming in from the selected device. The microprogram is notified when an address marker is found by the setting of status register 4.

Write gate on enables SERDES to write clock and data pulses on the selected device. Write gate and

address marker Search line cause SERDES to write an address marker byte on the device.

SERDES can be divided into three functional sections:

1. Write Section: This area contains a 2.5 mc crystal oscillator, write clock and data controls, write address marker controls, and a write parity check circuit.
2. Read Section: This area contains a variable frequency oscillator (VFO), used in synchronizing the frequency of the 2841 read circuits to the frequency of the data coming in from the device selected. Also contained in this section are read control circuits used in detecting address markers.
3. Common Section: Both the read and write section share some common circuits, namely:
 - a. Two bit rings (Δ bit ring and bit ring)
 - b. The file data register (FDR). The bit rings and the FDR do parallel-to-serial conversion when writing, and serial-to-parallel conversion when reading.

2.6.2 Write Operation: (Figures 2-25, 2-26)

- Write oscillator, write trigger, write phase X and write phase Y triggers are running all the time.
- Write operation begins with microprogram bringing up write gate.
- 1600 ns single-shot used to delay turn on of write clock gate for 1600 ns and reset VFO gate A which in turn will reset read clock gate if on - bit ring will reset with the turn off of read clock gate.
- 400 ns single-shot fires with the coincidence of not read clock gate, not write clock gate and not machine reset. Used as the set pulse to reset the bit ring triggers all off except $\Delta 5$ in conjunction with the bit ring reset gate.
- Allow phase Y latch insures that the bit ring receives the first advance pulse (phase X).
- Coincidence of write gate, write clock gate, and not allow phase Y provides an advance pulse to the 4 position counter so that counter one is turned on before parity is checked the first time.

For a detailed description of the intricate write timings, correlate Figure 2-26 timing chart to Figure 2-25 SERDES Write Circuits.

2.6.3 Read Operation

2.6.3.1 Description of VFO Components (Figures 2-27 and 2-28)

- Synchronize 2841 to device data.
- Separate clock and data pulses.
- Generate data or clock gap sense.
- Determine if incoming data is a zero or one.

Ramp Generator and VFO Trigger: (Figures 2-29 and 2-28) The Ramp Generator consists of a constant current source generating a linear ramp. The frequency of this ramp is nominally 2.5 MC. The discharge (negative going portion of the sweep) is used to complement the VFO trigger. One state of this trigger is used as a clock pulse gate; the other for a data pulse gate.

The Ramp Generator is started with a VFO Gate A input. It is always running except:

1. During a Write Operation.
2. During VFO reset time in a read operation.

The frequency of the ramp is variable and is under control of the error signal generated by the error detector.

Error Detector: The error detector is used to control the frequency of the ramp generator. This is necessary since the frequency of the incoming data may not be the same as the nominal frequency of the ramp. The synchronizing of the read data and the 2841 is accomplished in the following way:

1. A clock or data pulse arrives from the device and samples the ramp output.
2. If the sample time is correct (the device and 2841 are in step), no error signal is generated.
3. If the input pulse samples early or late on the ramp, an error level of negative or positive polarity is generated on the error signal line and begins to correct the frequency output of the ramp generator. When the 2311 and 2841 are in step again, the error signal will be minimal.

This frequency correction is continuously taking place whenever a device is selected. It is not designed to correct for an instantaneous frequency

change, but rather a gradual change (i. e., speed of drive).

Gate Generator: The gate generator is a differentiating network that converts the ramp to a non-symmetrical square wave. The gate generator output is used to develop separated data.

The circuit is adjusted for a 280 ns up level centered on the delayed data pulse during the VFO adjustment procedure.

Adjustable Delay Line and Single-Shot: It is desirable to have the data and clock pulses centered on their respective outputs of the VFO trigger. It is necessary, due to inherent delays in the other circuits (namely VFO trigger), to introduce a fixed delay in the data line. This is accomplished through use of a tapped delay line, adjustable in increments of 5 ns, from 0 to 125 ns. During the VFO adjustment procedure, the delayed data is centered on one of the outputs of the VFO trigger.

The single-shot serves as a pulse shaping network for clock and data pulses.

Gap Sensor: This circuit is used to detect clock and data gaps.

If separated data is absent for 2.4 μ sec, data gap sense rises.

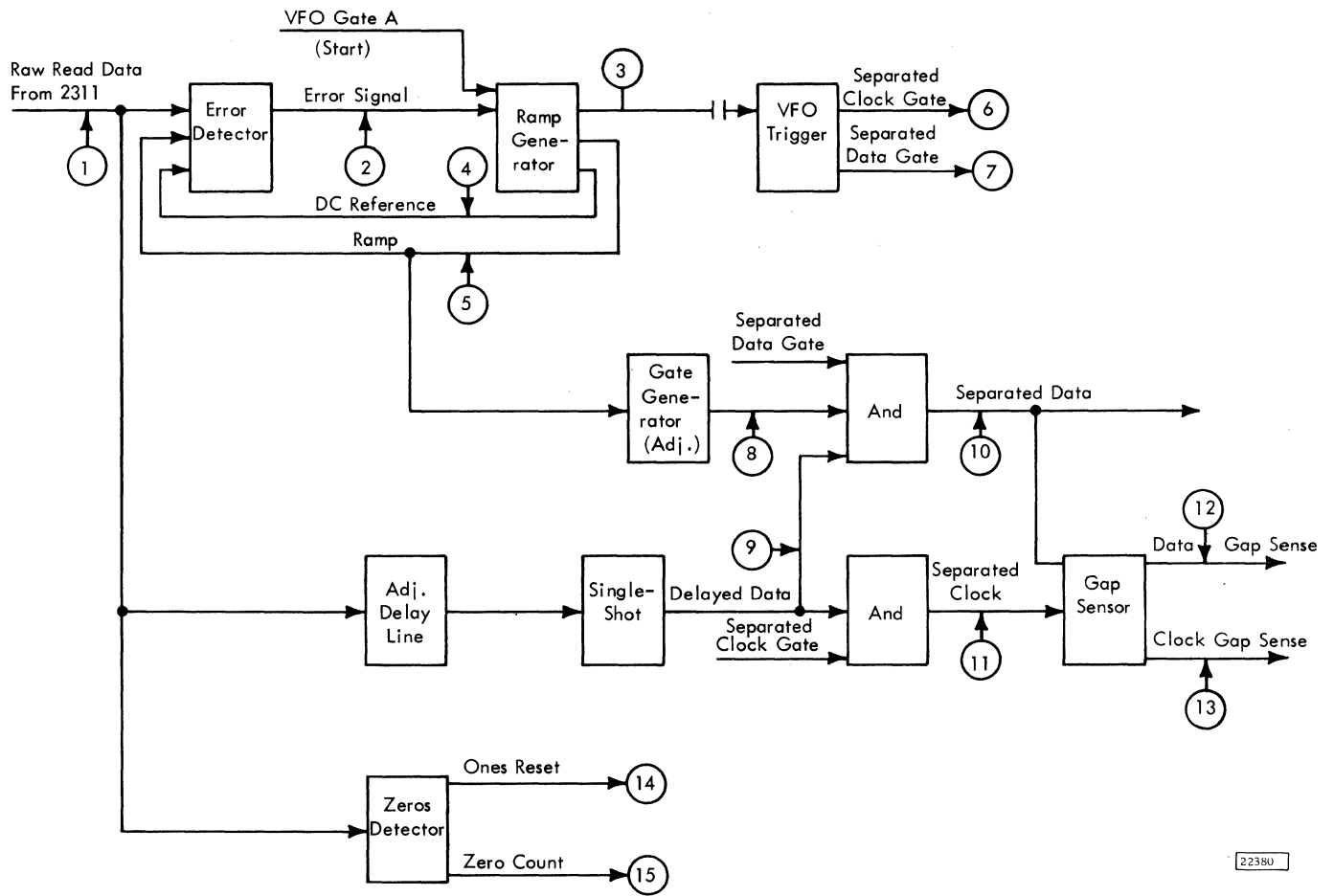
If separated clock is absent for 2.8 μ sec, clock gap sense rises.

Zeros Detector: When looking for an address marker, the VFO may be 180° out-of-sync. Therefore, some type of circuit is needed to identify a particular area as having a zero or a one.

The zeros detector accomplishes this by looking at an 800 ns period without regard to which pulse is clock and which one (if any) is data. If it finds one pulse during the period, it raises the zero count line. Two pulses in the period raise the ones reset line. Ones reset remains up until the next zero is detected.

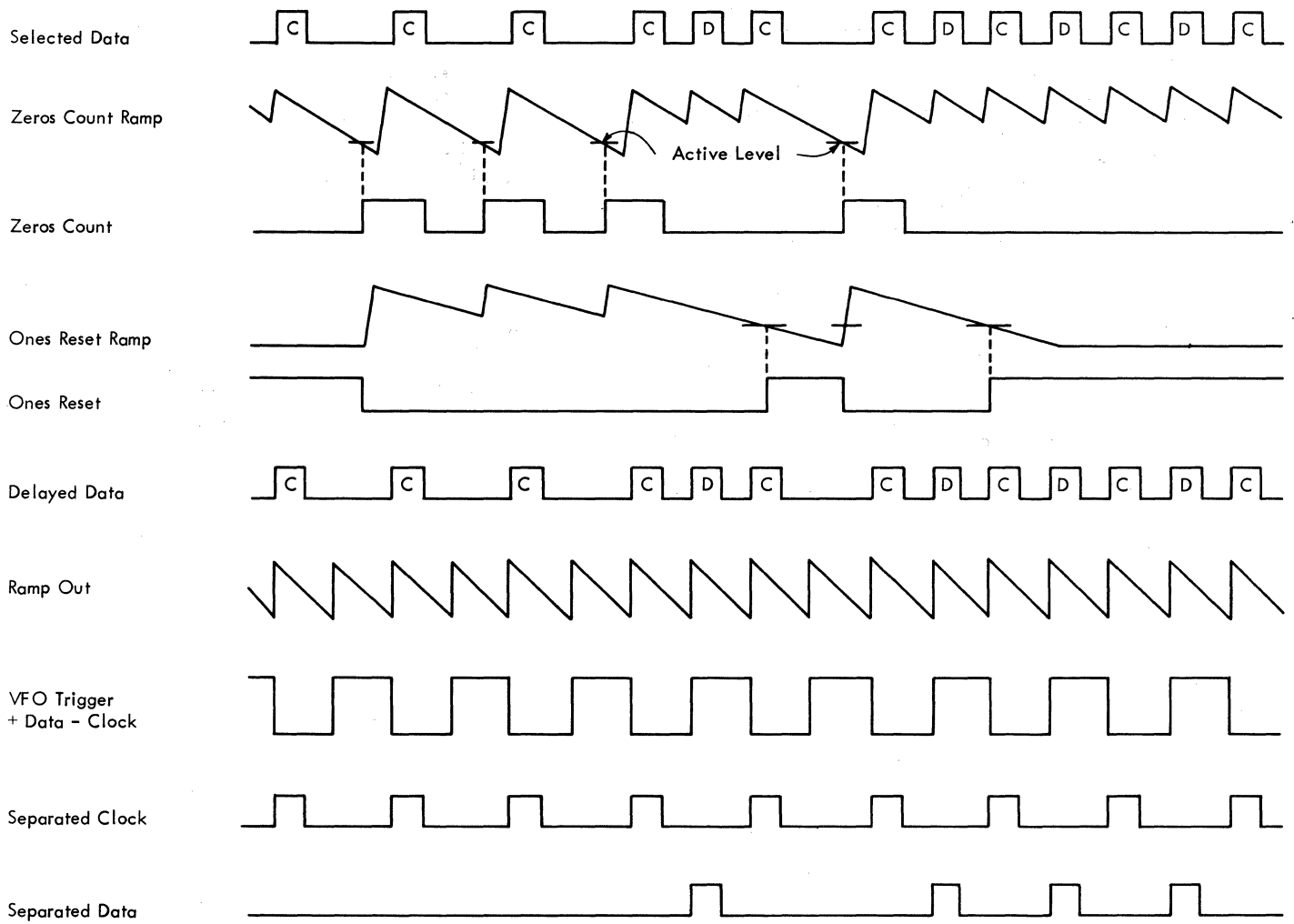
2.6.3.2 HA or Alpha Gap Sequence (Figures 2-29, 2-30 and 2-31)

- Microprogram knows the track orientation of the read heads when attempting to synchronize in an alpha or HA Gap.
- Operation is initiated with the raising of read gate by the microprogram in the leading zeros area.
- VFO synchronizes in remaining bytes of zeros.



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Figure 2-27. Variable Frequency Oscillator Circuit Operation



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Figure 2-28, VFO Circuits Timing Chart

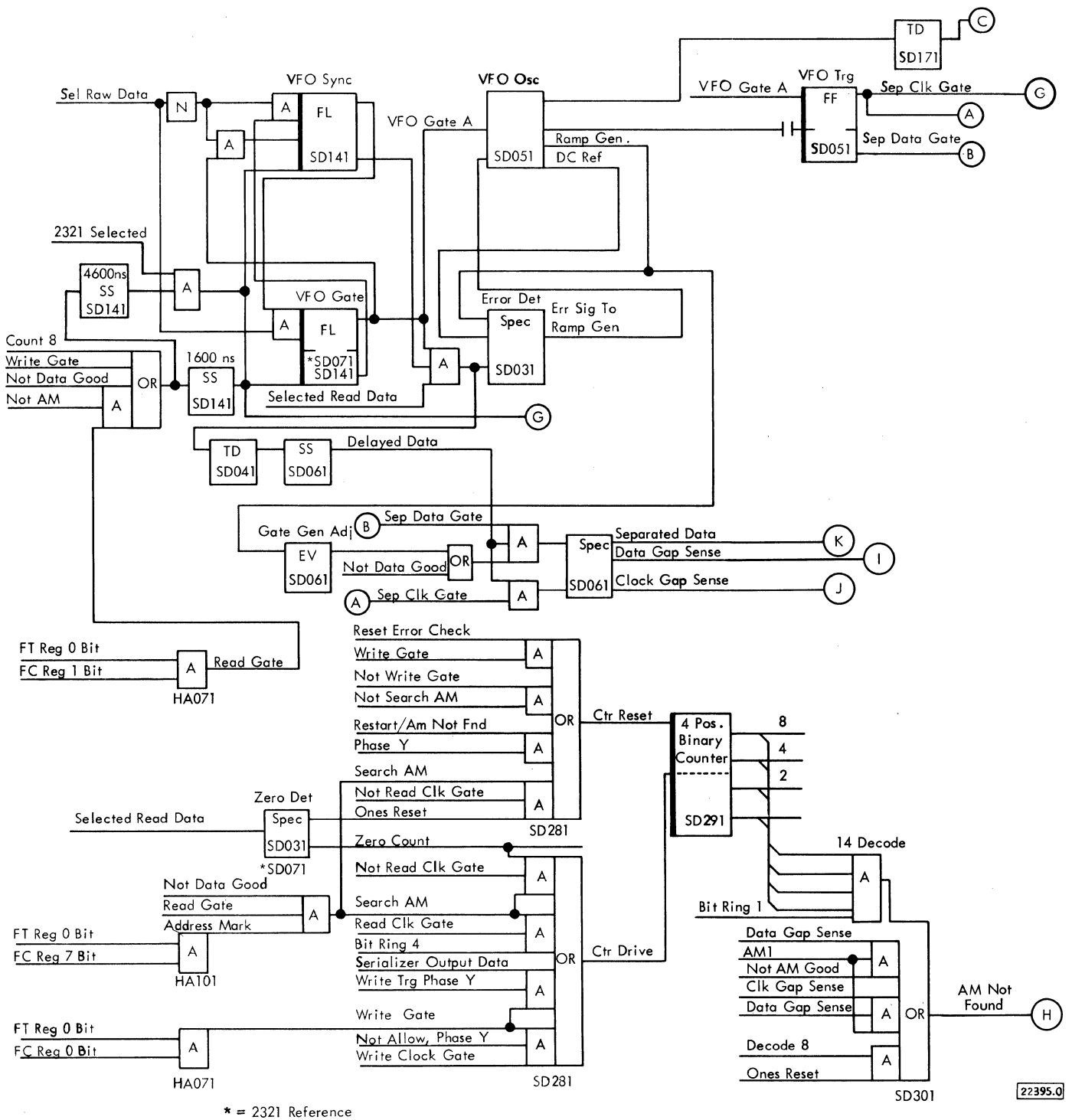


Figure 2-29. SERDES Read Circuits

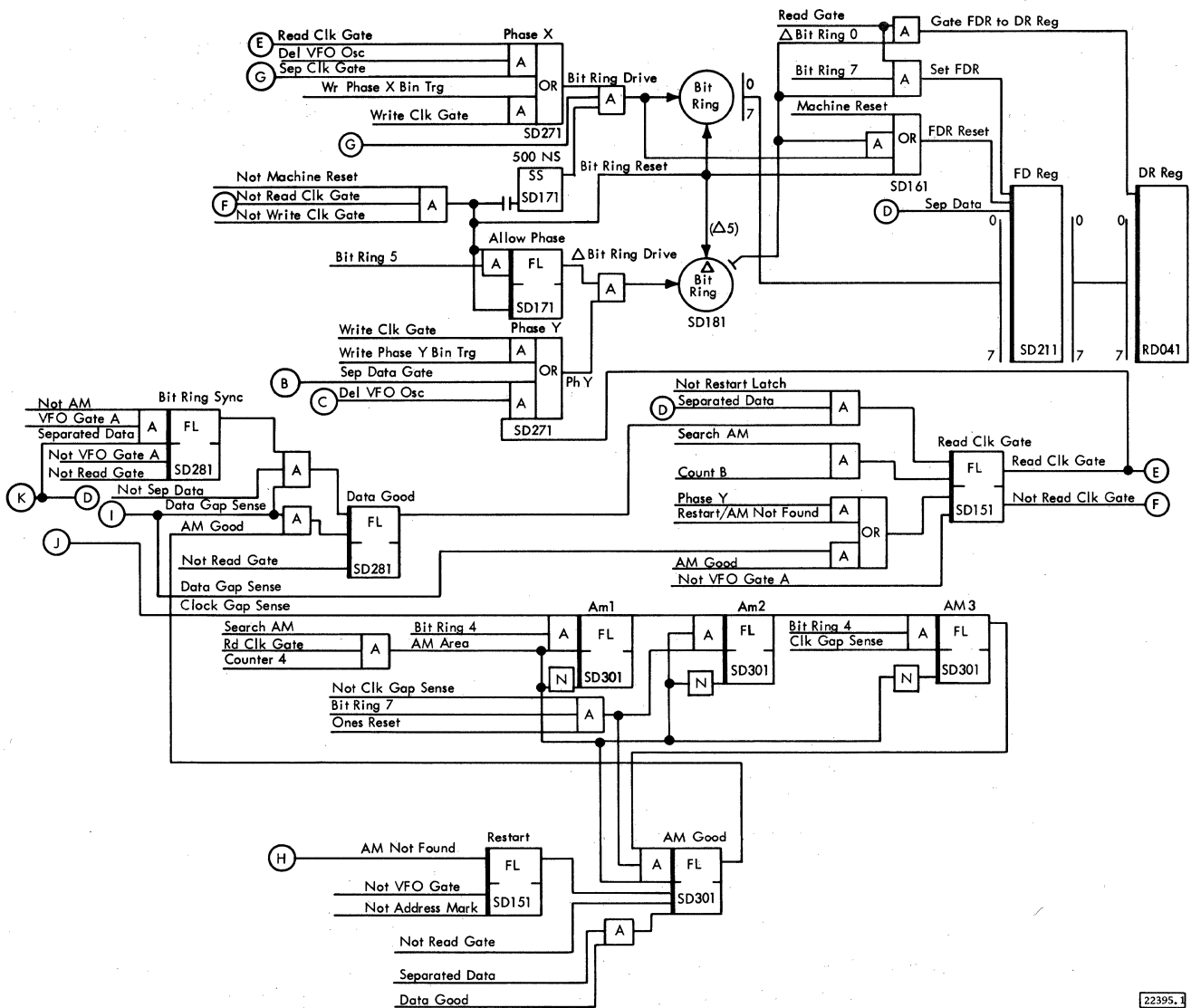
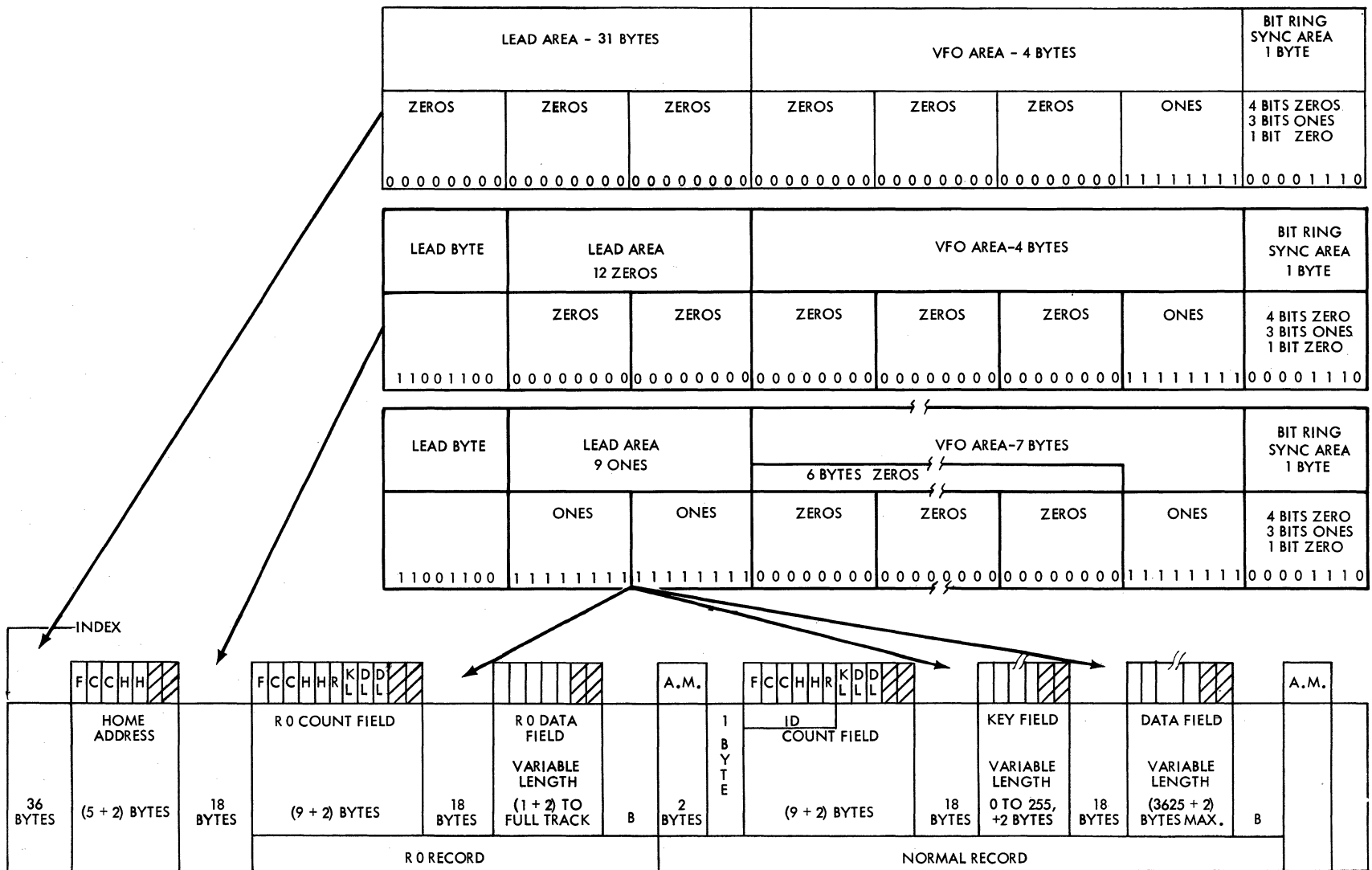


Figure 2-29. SERDES Read Circuits



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Figure 2-30. HA and Alpha Gap Bit Configurations 2311

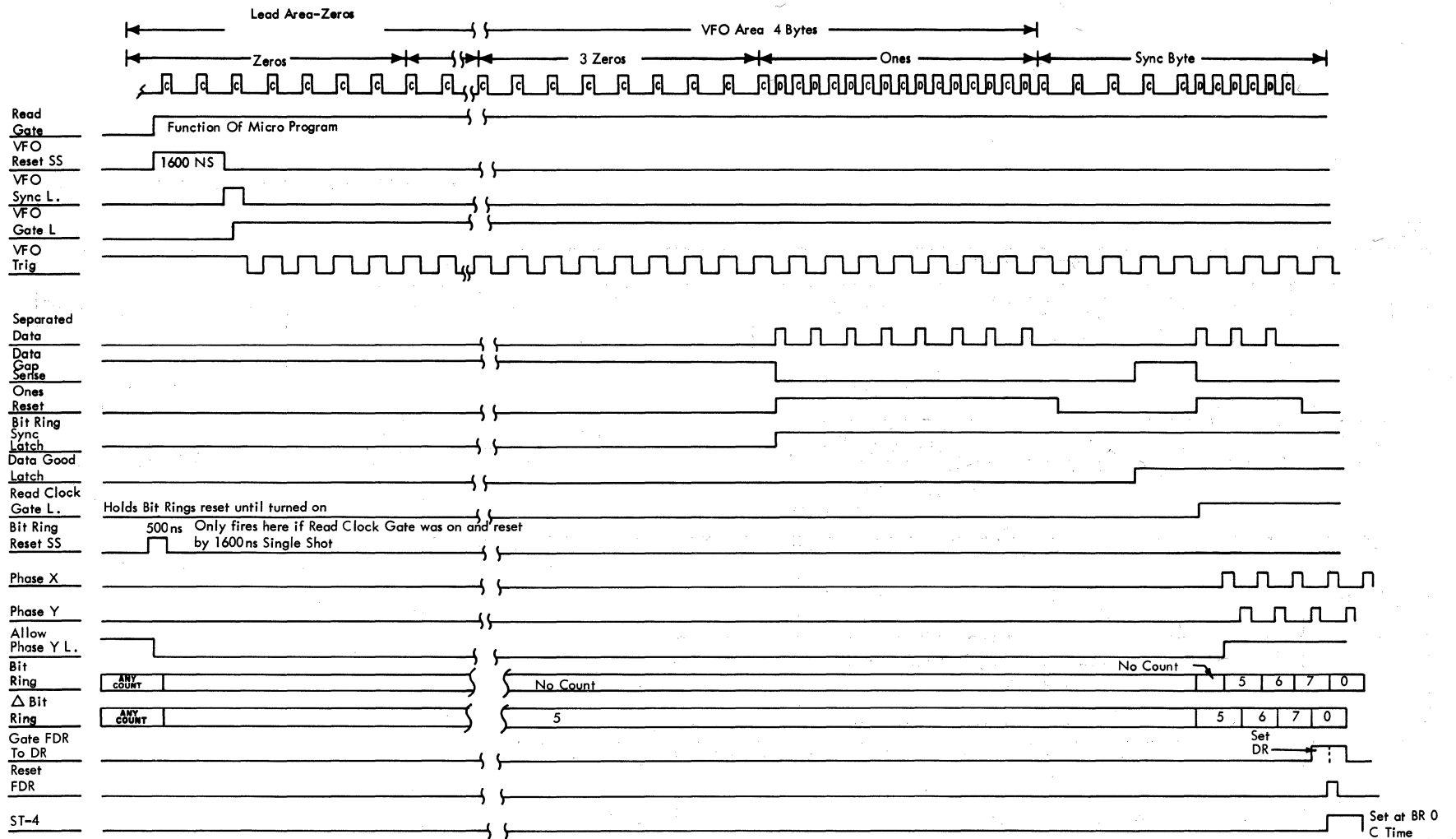


Figure 2-31. HA or Alpha Gap Timing Diagram

- Bit rings are freed after the turning on of read clock gate.
- Allow phase Y latch insures that the bit ring is stepped first.
- DR is loaded with the last three bits of the sync byte.
- ST 4 is set to tell the microprogram that SERDES has found a sync byte.

General: (Figures 2-29 and 2-30 and 2-31). The HA and alpha gaps are similar in content. The only exception is that HA has more bytes of leading zeros. This is necessary due to the time required for head switching that can occur at Index.

Synchronization of the VFO with read data is initiated when the microprogram raises read gate.

For a command which operates on HA, the microprogram branches on Index, delays a fixed amount of time into the HA Gap, and then raises read gate.

When synchronizing in an alpha gap (i. e., between key and data areas), the microprogram must stay in a timing loop. During this loop read gate is down. When the timeout occurs (approximately 80 μ sec), the microprogram raises read gate in the leading zeros area of the alpha gap. The dropping and raising of read gate in this gap accomplishes two things:

1. The VFO and bit rings are resynchronized on the data from the data area. This is necessary since the key and data areas may not have been written with the same command.
2. The microprogram does not have to count the number of bytes in the gap. The microprogram is notified by SERDES when the sync byte is in DR by the setting of ST 4.

Description: Figure 2-31 shows the timing relationship of the circuitry in Figure 2-29.

Read gate raising resets the VFO sync latch and VFO gate latch for 1600 ns. The VFO sync latch allows the VFO gate latch to turn on with the next clock pulse. The ramp generator is started with VFO gate A.

During the remaining bytes of zeros, the ramp's frequency is adjusted to the read data frequency by the error detector circuit. During this time the bit rings are held reset; bit ring to no latches on, and delta bit ring to 5.

The bit ring sync latch is set with the first data bit in the gap.

Data good is set with data gap sense. Read clock gate is set with the first data bit of the sync byte. Allow phase Y latch is off so that the first bit ring advance is a phase X pulse and steps the bit ring to 5.

Bit ring 5 turns on the allow phase Y latch and allows bit 5 of the sync byte to be set into FDR.

The bit rings continue to step, allowing separated data to be placed in FDR. Although the sync byte equals 14(10) only the last three bits are gated into FDR and consequently to DR at bit ring 0 time. The microprogram is notified of this action by the setting of ST 4 (bit ring 0, C time, and not search AM). DR should equal 6(10).

2.6.3.3 Beta Gap Sequence

- Microprogram does not know the orientation of the read heads.
- Operation is started when the microprogram raises read gate and address marker search.
- VFO synchronizes on the read data and looks for a particular combination of bits.
- If bits are incorrect, the operation is restarted.
- Eventually, proper bit configuration is found.
- DR is loaded with last three bits of sync byte.
- ST 4 is turned on.

General: (Figures 2-29, 2-32, and 2-33). The beta gap is unique in that it contains two address marker bytes. These should be the only bytes (on a track) that have missing clock bits.

The microprogram will initiate the beta gap sequence by raising read gate and the address marker search line. The microprogram will generally not know where the heads are located in relation to the track data when it raises these lines. SERDES, therefore, looks for the data gap (address marker), and notifies the microprogram (by setting ST4) when it has found an address marker and read the sync byte.

Description: Figure 2-32 shows the timing relationship of the circuitry in Figure 2-29.

The microprogram raises read gate and the address marker search line. This can happen anywhere on the track. Figure 2-34 shows this happening in the last byte of ones in the beta gap.

The VFO sync latch is held reset for 1600 ns. The bit rings are held reset due to the read clock gate

being off. When the reset times out, the VFO is started with the incoming data. The timing chart shows the VFO being started with a data pulse, therefore the VFO is 180° out-of-sync.

The zeros detector finds one bits in the read data and raises the ones reset line. This holds the 4-position binary counter off.

The zeros detector finds zero bits in the read data, resets ones reset and raises zeros count. Since the read clock gate is off at this time, each zeros count pulse will step the 4-position counter until it reaches 8. After nine zeros in a row, the possibility exists that this is a beta gap.

A decode of count 8 resets the VFO circuits, and turns on the read clock gate latch. The VFO circuits are reset here so that they may resync in a zeros only area. After 1600 ns the VFO circuits have resynchronized. Read clock gate turning on removes the reset to the bit rings. The allow phase Y latch ensures that the bit ring is stepped before the delta bit ring. The bit rings start stepping. Since read clock gate is on, bit ring 4 is used to step the 4-position counter. During the remaining bytes of zeros, the ramp's frequency is adjusted to the read data frequency by the error detector circuit.

The AM-1, -2, -3, and AM good latches are sequenced, by clock gap sense, in AM bytes 1 and 2. Data gap sense, occurring in the sync byte, resets the read clock gate latch and sets the data good latch.

Read clock gate dropping:

1. Resets AM 1, 2, and 3 latches.
2. Resets the Bit Rings so their count can be adjusted for bits 5, 6, and 7 of the sync byte.

Data good setting drops the search AM line and allows the AM good latch to set with the next separated data pulse.

Read clock gate is set again with the first data pulse of the sync byte. The allow phase Y latch ensures that the bit ring is stepped before the delta bit ring.

The bit rings step. Bits 5, 6, and 7 of the sync byte are gated into FDR, and subsequently into DR at bit ring 0 time. The microprogram is notified that SERDES has found an address marker by the setting of ST 4 (Bit Ring 0, C time, and not search AM).

The microprogram checks DR for 6. If it is 6 the operation continues. If it is not 6 the microprogram will drop read gate and AM search, delay, and reinitialize the operation. In this case, if SERDES cannot find a good address marker, unit check in the

status byte and no record found in the sense data will be indicated if index is passed twice.

Restart Conditions:

1. Ones reset when the read clock gate is off will reset the 4-position counter. This means that fewer than 9 zeros in a row were read.
2. Count of 8 in the counter and ones reset. This is the area where the VFO is resynced on clock pulses. If a one bit is here, the VFO may still be out of sync with the read data.
3. AM 1 on, data gap sense, and not AM good. Checking for missing data bits in two AM bytes.
4. AM 1 on, clock and data gap sense. This could occur in some area where no clock or data had been written.
5. Counter 14. No data gap sense in an area SERDES thought should have been the sync byte.

Restart conditions 2, 3, 4, and 5 reset:

1. The Read Clock Gate latch.
2. The 4 Position Counter.
3. The AM Good latch.
4. AM 1, 2, and 3 latches when Read Clock gate drops.

2.7 CHANNEL INTERFACE ATTACHMENT (Figure 2-34)

- The channel interface consists of seven sections.
 1. Selection Controls Out.
 2. Tags Out.
 3. Selection Controls In.
 4. Tags In.
 5. Bus Out.
 6. Bus In.
 7. Service In/Out Controls.

The various sequences which the channel interface goes through are presented to tie together the seven sections. The microprogram philosophy is introduced where necessary to accomplish the sequence.

2.7.1 Initial Selection Sequence (Figure 2-34)

- The initial selection sequence is used to connect the channel to the 2841.
- Initial selection ends with the transfer of the initial status byte.

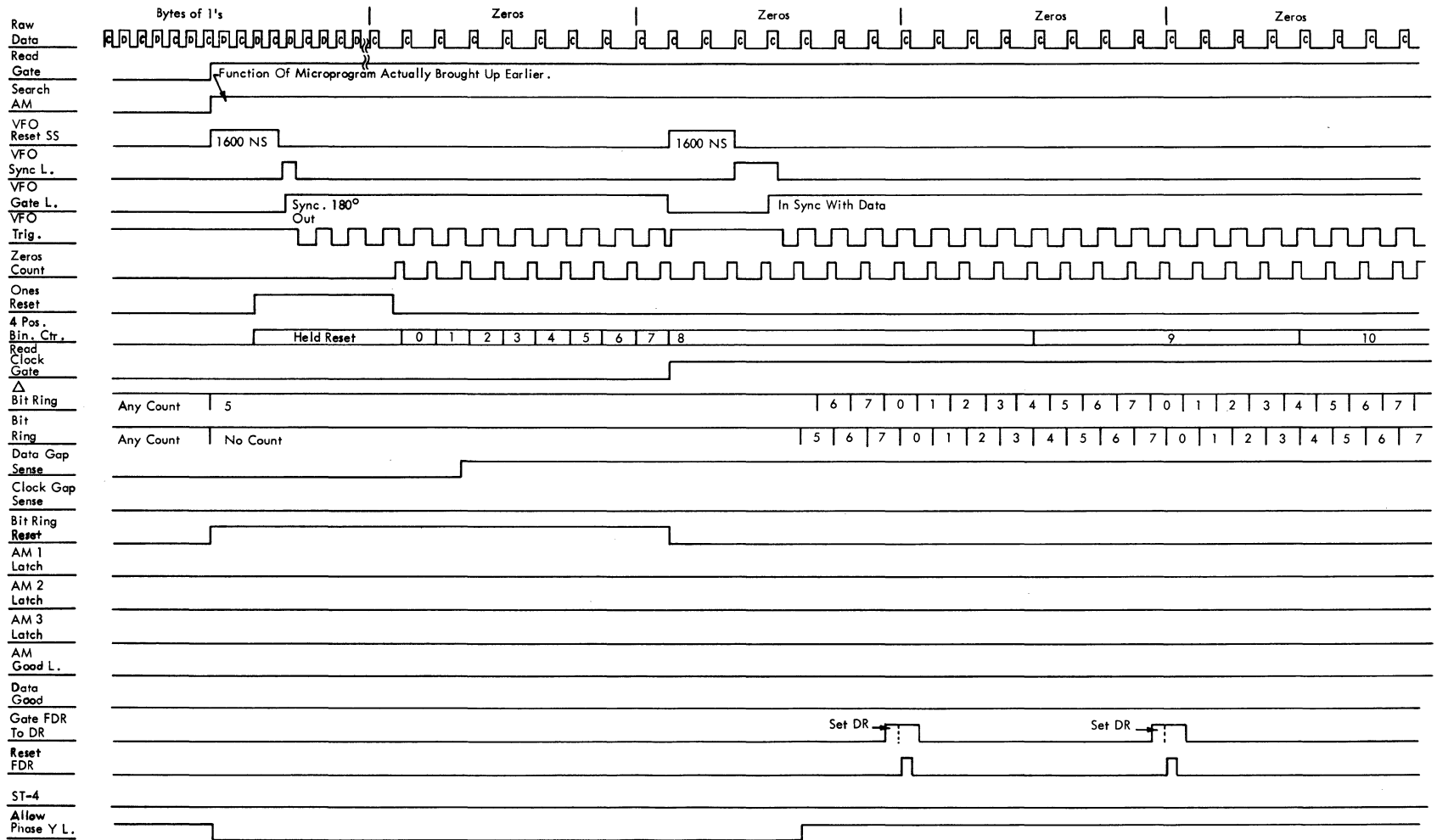


Figure 2-32. Beta Gap Timing Diagram (Sheet 1 of 2)

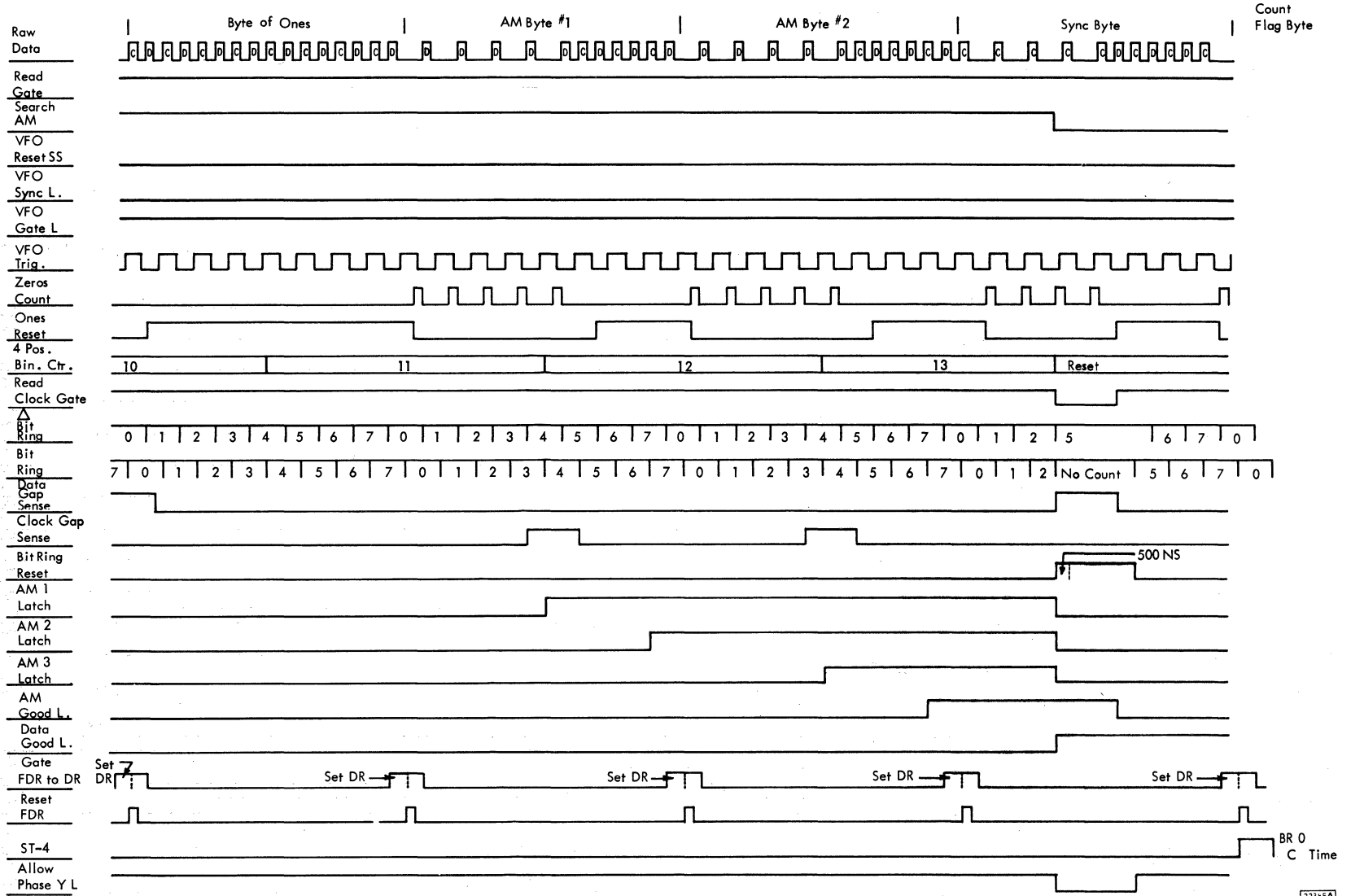


Figure 2-32. Beta Gap Timing Diagram (Sheet 2 of 2)

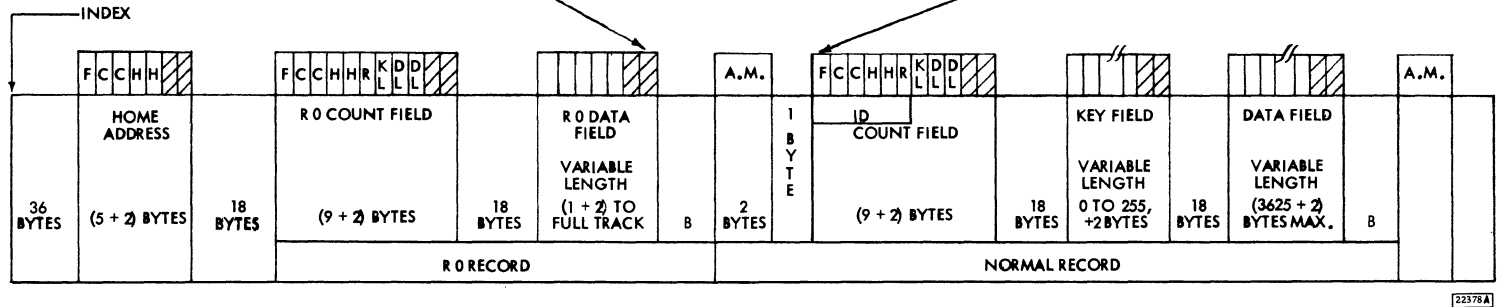
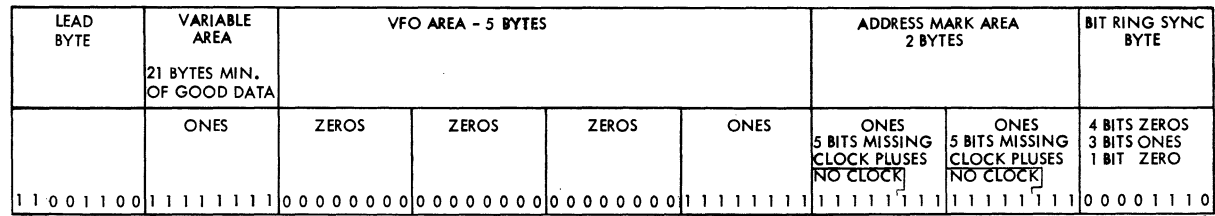
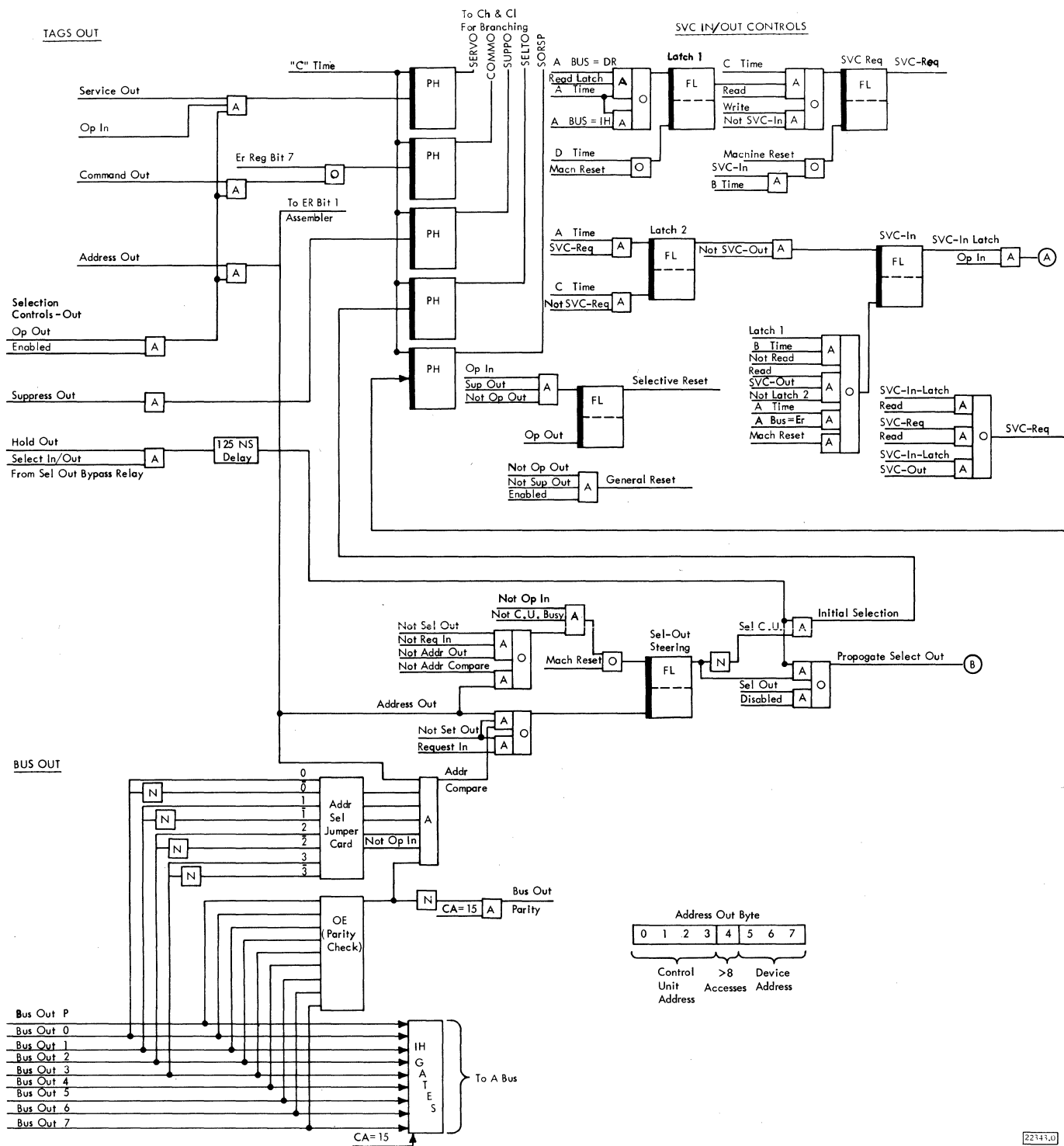
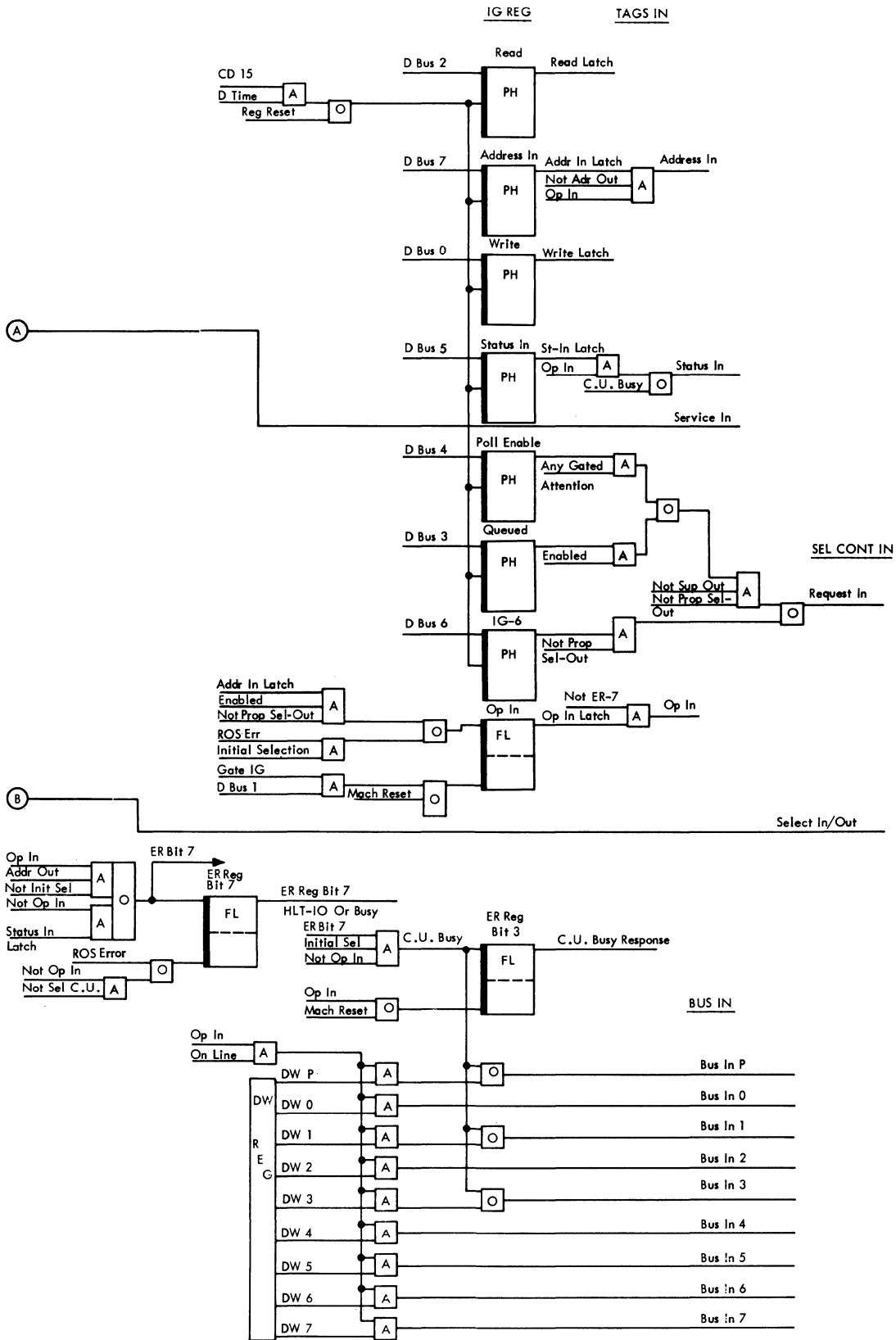


Figure 2-33. Beta Gap Bit Configuration - 2311 - 2302



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Figure 2-34. 2841 Channel A Attachment Control and Data Flow



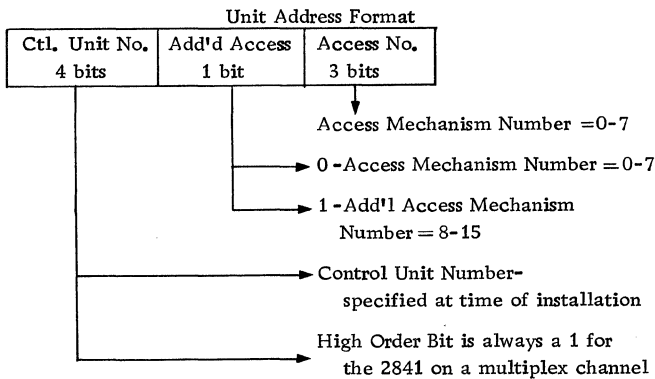
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Figure 2-34a. Channel A Attachment Control and Data Flow.

The initial selection sequence is as follows:

1. Initial condition - Select out Steering latch is on.
2. Channel places an address byte on bus out and raises address out.

The address byte contains the access and control unit number:



The control unit number may be any configuration selected by the customer at installation.

3. The 2841 compares bits 0, 1, 2, and 3 of the address out byte with its prewired address. It also checks parity (odd) of the entire byte. If the address is the same (address compare) and parity is good, the select out steering latch is reset. If the address doesn't compare or the byte has incorrect parity, the select out steering latch is left on.
4. Channel raises select out.

If the select out steering latch is off (address compare and good parity), initial select is raised in the 2841. Up to this time, the 2841 has been operating on channel timing. It is now necessary to get in step with the microprogram timing. The SELTO latch is turned on at the next 2841 clock C time. SELTO is a condition that can be tested by the microprogram.

NOTE: If the select out steering latch is on (address did not compare or bad parity), select out is propagated to the next control unit.

5. The microprogram branches on SELTO, goes through several ROS words, and sets the Address In latch with the ALU statement 1 → IG (D bus bit 7).
6. The address in latch on causes Op in to be sent to channel.
7. Op in causes the channel to drop address out.

8. Address out dropping causes address in to be sent to channel. Before raising address in, the 2841 microprogram places the Address in byte in the DW register.
9. Command out is sent from the channel. The COMMO latch is set on at the next "C" time. The microprogram will branch on COMMO recognizing that command out has been sent.
10. The microprogram drops address in with the ALU statement 0 → IG.
11. Channel drops command out.
12. The microprogram loads the DW register with the status byte and raises status in with the ALU statement 4 → IG ("D" bus, bit 5).
13. Channel responds to status in with service out. The SERVO latch is turned on at the next C time.
14. The microprogram causes status in to drop with the ALU statement 0 → IG.
15. Channel drops service out.
16. This completes initial selection.

2.7.2 Data Transfer Sequences (Figure 2-34)

- The 2841 contains circuitry that controls the service in/service out responses to the channel.
- The controls are in read mode for read and sense commands.
- The controls are in write mode for write, search, and some control commands.

The service in out controls are used for two types of operations:

1. Data transferred to channel - read or sense.
2. Data transferred to the 2841 - write, search or control.

2.7.2.1 Read Operation (Figures 2-34 and 2-35)

1. The microprogram sets the read latch with the ALU statement, 32 → IG.
2. When a byte of data is ready for transfer to channel, the microprogram issues the ALU statement DR → DW (DR is placed on the A bus).
3. This statement sets DW (Bus In) with the byte of data and allows Latch 1 to set at the following A time.
4. The service request latch sets the following C time raising SORSP. SORSP is tested by the microprogram. In a read operation, it means that the channel has not yet responded to service in with service out.

5. Latch 1 is reset at D time.
6. Latch 2 is set at A time.
7. Latch 2 setting and not service out cause the service in latch to be turned on, raising service in to channel.
8. The service request latch is reset at B time. SORSP is held up by the service in latch.
9. Latch 2 is reset at C time.
10. The channel responds with service out. (The byte has been transferred to the channel.)
11. The SORSP line falls.
12. The SORSP latch resets at C time. This means to the microprogram that the byte has been transferred to channel.
13. The microprogram and the service in/out controls repeat steps 2-12 for each byte.
14. When the microprogram is finished with the read operation, it resets the read latch with the ALU statement 0→IG.

2.7.2.2 Write Operation (Figures 2-34 and 2-36)

1. The microprogram sets the write latch with the ALU statement 128→IG.
2. The service request latch is set.
3. Latch 2 sets at the following A time.
4. Latch 2 and not service out set the service in latch, raising service in to channel.

NOTE: The 2841 has requested a byte of data. SORSP is down and stays down until the channel raises service out saying that there is a byte of data on bus out.

5. Channel raises service out.

NOTE: If channel raises command out instead of service out, the microprogram will recognize this and reset the Svc in Latch with a ER→D ALU statement.

6. The SORSP latch sets at the following C time.
7. The microprogram recognizes SORSP and performs the ALU statement, IH →register x. The byte of data is now stored within the 2841.
8. Latch 1 sets the following A time.
9. The service in latch resets the following B time dropping the SORSP line.
10. The SORSP latch resets the following C time.
11. Latch 1 resets the following D time.
12. Steps 2-11 are repeated for each byte of data.

13. When the microprogram is finished with the write operation, it resets the write latch with the ALU statement 0→IG.

2.7.3 Ending Sequence (Figure 2-34)

- The ending sequence is used to present an ending status byte to the channel, and to disconnect from the channel.

The ending sequence is as follows:

1. The microprogram places the ending status byte in the DW register.
2. The microprogram raises status in with the ALU statement 4→IG (D Bus, bit 5).
3. Channel responds with service out or command out.
4. The 2841 drops status in with the ALU statement 0→IG.
5. The microprogram waits for select out to fall (SELTO).
6. The microprogram drops Op in with the ALU statement 64→IG (D Bus, bit 1).

2.7.4 Short Control Unit Busy Sequence (Figure 2-36)

- The short control busy sequence is a means of indicating control unit status to the channel without going through the initial selection sequence.
- It is used when the 2841 is addressed with a new start or test I/O and the 2841 is still busy.
- If addressed while busy, the 2841 takes a polling interrupt when it goes not busy. Control unit end is indicated in the status byte.

Definition: A means of indicating control unit status to channel without going through the initial selection sequence. Status in in response to address out.

The short control unit busy sequence is used by the 2841 in the following situations:

1. No chaining, and
2. The last command in the chain was a Write, and
3. Channel End and Device End have been transferred to the channel, and
4. Write Gate or Erase Gate are still on, and

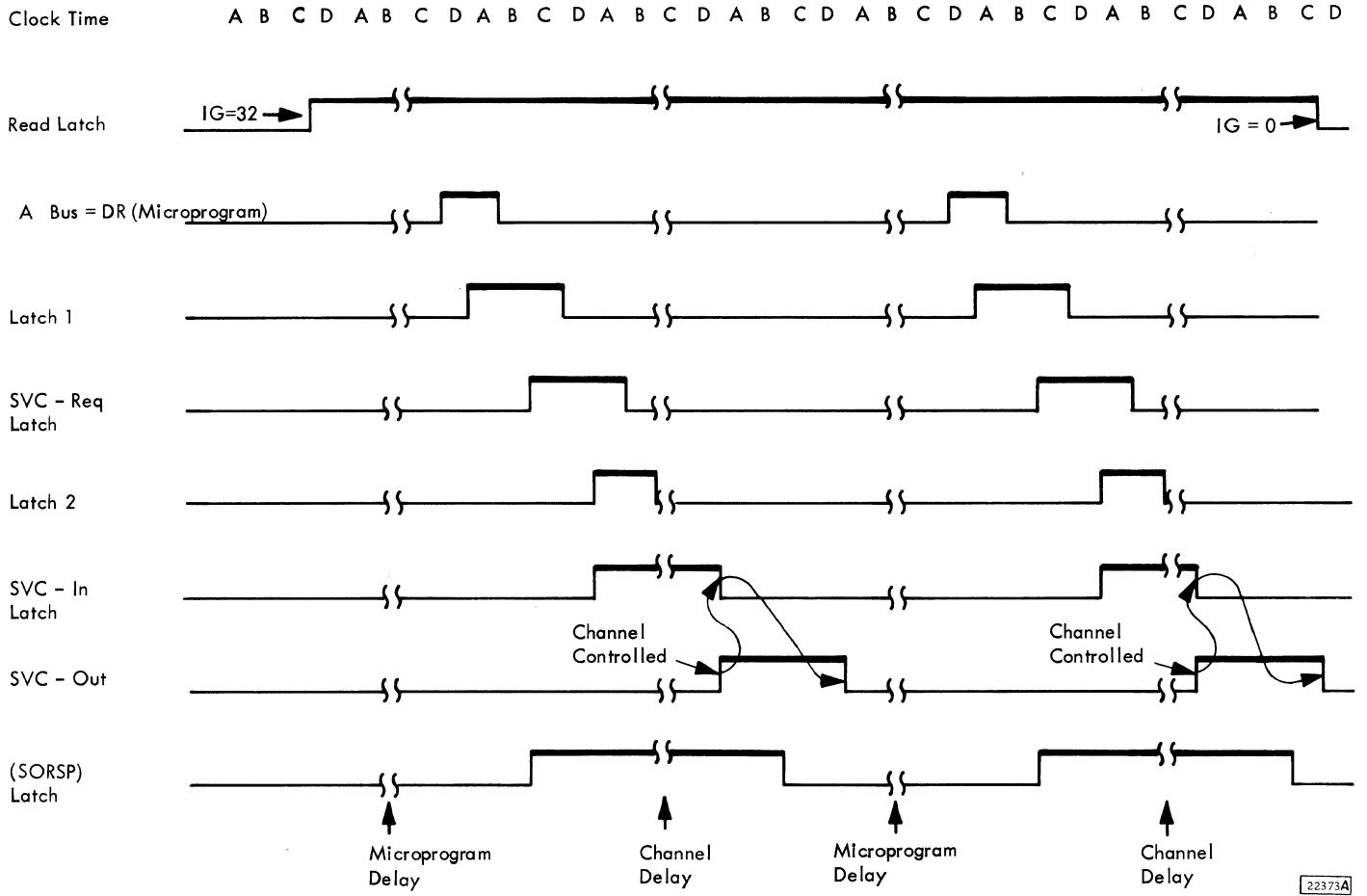


Figure 2-35. SVC IN/OUT Timing for Read and Sense Operations

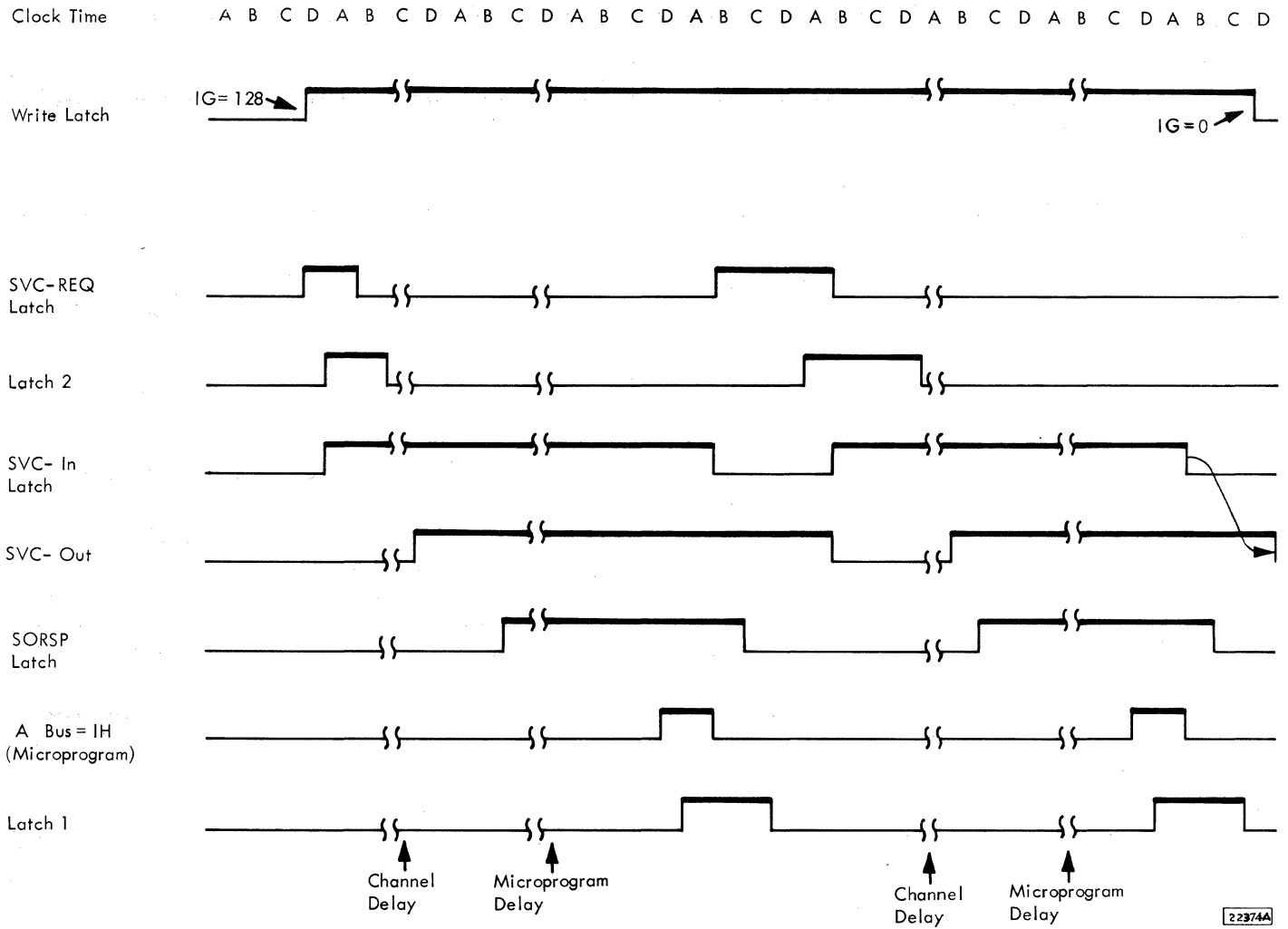


Figure 2-36. SVC IN/OUT Timing for Write, Search, and Control Operations

NOTE: During write key data and write data operations, erase gate is on for approximately 60 μ secs after channel end-device end.

During Write HA, R0, CKD operations, write gate is on to index. Erase gate is on for approximately 60 μ secs past index.

5. A start or test I/O instruction is given to the 2841.

Operation: (Figure 2-34)

1. After dropping Op in at the end of one of the write commands, and the program is not chaining, the 2841 sets the status in latch. Status in is not sent to channel since Op in is down.
2. Not Op in and the status in latch on raise ER bit 7.
3. At this time, ER register, bit 7 is held reset.

NOTE: Assume the 2841 is addressed while busy.

4. Address out and address compare reset the select out steering latch raising the select control unit line. This allows ER register, bit 7 to set.
5. Channel raises select out. The initial selection line raises bringing up the CU Busy line and setting the ER register, bit 3 latch.
6. The CU busy line:
 - a. Brings up the parity, status modifier, and busy bits on bus in (CU busy), and,
 - b. Raises status in to channel.

NOTE: The 2841 does not through the normal initial selection sequence.

7. Channel drops select out and address out.
8. Select out dropping, drops the initial selection line.
9. Initial selection line dropping, drops the CU busy line. (Status in drops)
10. The CU busy line drops. This causes the select out steering latch to be set (initial condition).
11. Set of the select out steering latch drops the select control unit line.
12. Drop of the select control unit line causes the ER register, bit 7 latch to reset.

The only latch not in its original condition after this operation is ER register, bit 3. When the microprogram finishes with the write operation, it tests ER register, bit 3. If it is on, the microprogram sets up to take a control unit end polling interrupt.

2.7.5 Halt I/O Instruction (Figure 2-34)

- The halt I/O instruction causes the 2841 to release the channel immediately.
- The operation in progress continues to its ending point.
- When the operation in progress is finished the 2841 initiates a polling interrupt sequence.

The halt I/O instruction causes the 2841 to release the channel immediately, stopping the transfer of data. The operation in progress when the halt I/O was given proceeds to its ending point.

When the operation reaches its ending point, the microprogram initiates a polling interrupt sequence.

2.7.5.1 Halt I/O Sequence

Assume some operation in progress. Therefore, Op in is up.

1. Channel drops select out (may already be down on multiplexor channels).
2. Channel raises address out.
3. The ER register, bit 7 latch is turned on.
4. Op In to channel is degated.
5. Command out is forced up within the 2841.
6. This completes the halt I/O line sequencing to channel.

Command out is forced up so that the microprogram can branch on it. This normally means that the channel's byte count has gone to zero and tells the 2841 to stop the data transfer. However, the microprogram will also find ER register, bit 7 on. This means halt I/O to the microprogram and will cause it to reset Op in. Op in dropping resets the ER register bit 7 latch causing command out to drop internally within the 2841.

If the 2841 is not working on any command when the halt I/O is given, the 2841 will ignore the halt I/O.

2.7.6 Polling Interrupts (Figure 2-34 and 2-37)

- A polling interrupt is a means of connecting the 2841 to the channel without giving a start or test I/O command.
- The sequence is normally used to present a status byte after the channel and the 2841 have disconnected.

A channel can tell the control unit to hold (stack) the interrupt by raising command out in response to status in.

2.7.6.1 Polling Interrupt, Definition

Polling interrupt is a means of connecting the 2841 to the channel and of presenting an outstanding status byte without giving a start or test I/O command to 2841.

2.7.6.2 Polling Interrupt Routine

The 2841 uses the polling interrupt sequence in the following command word sequences to present outstanding status information to the channel.

1. Not chaining - A seek command to a different cylinder or restore command is given. Channel end occurs. The channel and 2841 disconnect. Device end is still outstanding. The microprogram turns on the poll enable latch. When gated attention occurs, a polling interrupt sequence is initiated to present a device end status byte to the channel.
2. The 2841 is addressed with a new start or test I/O command while busy (after a write command). The 2841 indicates control unit busy to the channel on the start or test I/O. When the 2841 goes not busy it initiates a polling interrupt sequence with control unit end in the status byte.
3. A halt I/O is given to the 2841 while it is operating on some command. The 2841 disconnects from the channel. When the original command reaches its logical ending point, a polling interrupt is initiated with the applicable status information in the status byte.
4. Not chaining - The 2841 has presented channel and device end after a write command. Write gate or Erase gate are still up because the field has not been completed. The 2311 drive goes inoperable for some reason (not ready, not on line or unsafe, etc.). The 2841 initiates a Polling Interrupt Sequence with the Control Unit End and Unit Check bits on in the status byte.
5. Assume:
 - a. Multiplexor Channel.
 - b. Cylinder Seek or Restore command.
 - c. Command Word Chaining.
 - d. Channel End presented to the channel.
 - e. Select Out is down from the channel.

The 2841 then drops Op In disconnecting from channel. The microprogram sets the IG-6 latch so that any Gated Attention can raise Request In, thereby, initiating a Polling Interrupt Sequence with Device End in the status byte. During the time between channel and device end, channel has kept Suppress Out up. This prevents any other control unit from initiating a Polling Interrupt. Note that when Request In is raised by means of IG-6 and Gated Attention, Suppress Out from the channel cannot suppress the Polling Interrupt request. This is the only type of 2841 Polling Interrupt that cannot be suppressed by the channel.

6. Changing a 2311 from Not Ready to Ready initiates a Polling Interrupt Sequence with Device End in the status byte.

2.7.6.3 Stacked Status

Definition: Anytime the channel returns Command Out in response to Status In, it means to hold (stack) this status byte in the 2841.

The channel and the 2841 disconnect. The 2841 attempts to transmit this stacked Status Byte to the channel by means of the Polling Interrupt Sequence.

2.7.7 Resets (Figure 2-34)

General Reset

The channel is able to reset all on line control units by dropping Operational Out and not raising Suppress Out. This provides a general reset to the 2841. All registers are reset and the microprogram restarts in address zero.

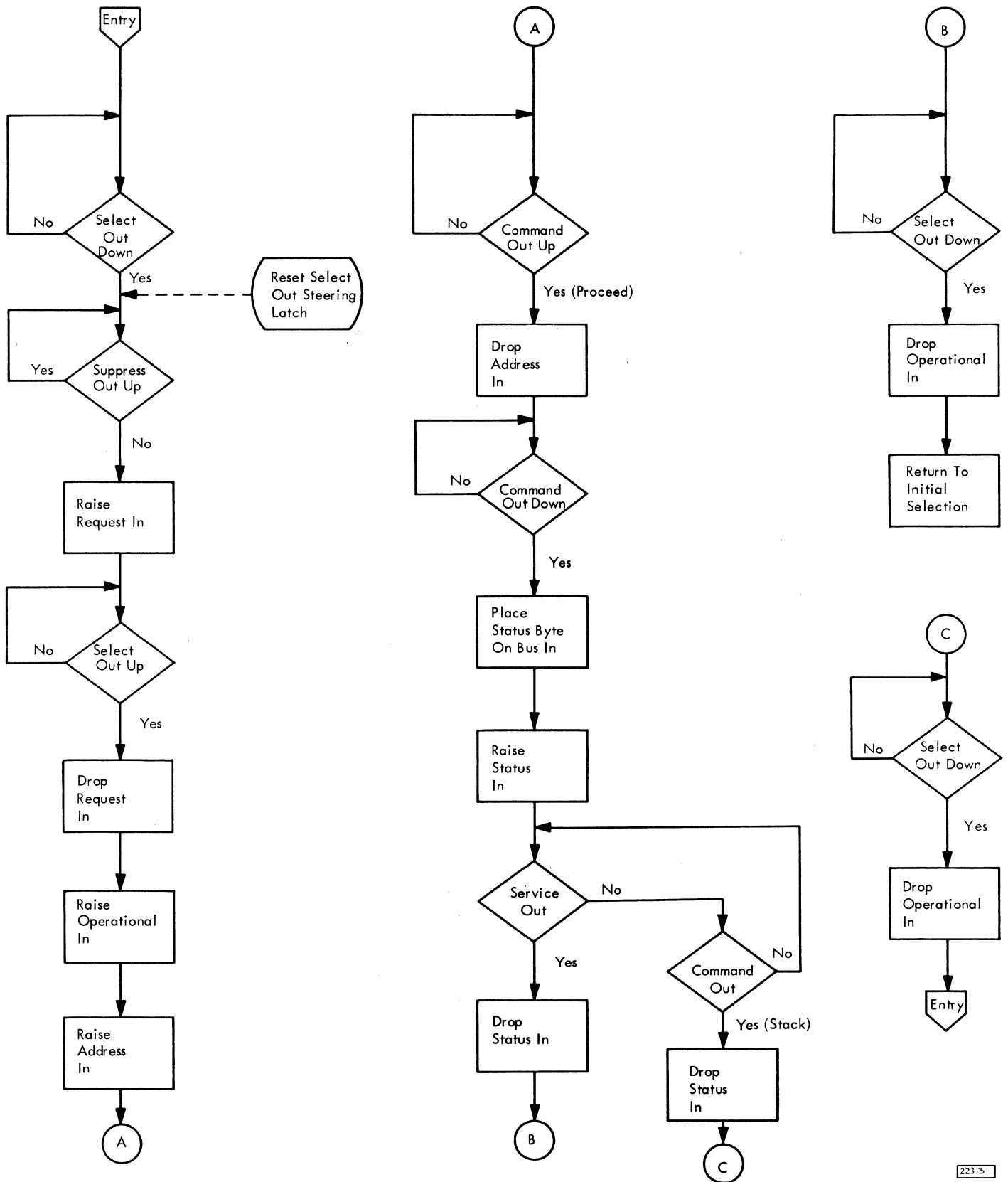
2.7.7.1 Selective Reset

Channel issues a Selective Reset by raising Suppress Out and dropping Operational Out. If the 2841 has Operational In up, all 2841 registers are reset (with the exception of ST(7), reset on) and the microprogram restarts in address zero.

An example of why the channel might issue a Selective Reset follows:

Assume: ROS Error in 2841 while not selected to channel.

ROS Error stops the microprogram and attempts to set the Op In Latch. When channel next addresses the 2841, initial select rises setting the Op In latch. No other lines are raised on the interface. Channel decides that something is wrong with one of the



22375

Figure 2-37. Channel and 2841 Polling Interrupt Sequence Interface

control units. Some channels may attempt Halt I/O routine first. Note that ROS Error stops the ER register, bit 7 from being turned on; therefore Halt I/O does nothing within the 2841 (Op In is still on).

Eventually the channel gives a Selective Reset. This resets the error condition, drops Op In, and allows the microprogram to begin operating at address zero.

2.8 CE PANEL (Figure 2-38)

- Allow Customer Engineer control of 2841 operations.
- Displays error checks.
- Displays Read Only Storage Address Register.
- Displays A Register output.
- Displays BX, BY, DH, DL, DR, DW, FR, GL, GP, KL, OP, UR, ST, ER, and SW Registers by reading them into the A Register.
- Allows setting of a byte of data into a selected register.
- Allows stopping on errors.
- Allows stopping at a preset address.
- Allows starting the microprogram at a preset address.
- Provides for single microprogram step operation.
- Provides a sync pulse at a preset address.
- Provides for recycling between two microprogram addresses.
- Provides for local power control.

2.8.1 CE Switches

2.8.1.1 Normal/CE

The Normal/CE switch in the Normal (on line) position allows power sequencing and signals from the using system to control the 2841. The Normal/CE switch in the CE (local) position degrades signals to and from the using system. Power control is then under control of the 2841 Power On/Off Switch.

2.8.1.2 Lamp Test

When depressed, in either CE or Normal, lights all lamps.

The Following Switches are Active Only in CE Mode.

2.8.1.3 Register Select.

Allows selection of certain registers for display or data entering.

2.8.1.4 Display

Displays the selected register data in the A register lamps. The contents of the selected register are displayed only as long as the display button is depressed.

2.8.1.5 Enter

Enters data, stored in the two low order Start Address switches, into the selected register.

2.8.1.6 Set ADDR

Places the address contained in the Start Address switches into the W and X registers.

2.8.1.7 Check Reset

Resets Sense Amplifier Control register, Address, and Data Check indicators.

2.8.1.8 Reset

Resets all indicators and registers.

2.8.1.9 Stop

The sense latch reset and sense strobe lines are inhibited. The TROS continues to cycle internally. The 2841 is functionally stopped.

2.8.1.10 Start

Starts TROS at the address sitting in the W and X registers.

2.8.1.11 Single Step

Operate TROS for one machine cycle each time the Start switch is depressed.

2.8.1.12 Check Stop/Run

Check Stop Position - causes TROS to stop on a Sense Amplifier, Control register, Address, or Data Check error. The Probe Latch can also be jumpered into this circuit in order to stop the 2841 at a given point in the micro program.

Run - Machine does not stop-on-errors. In Normal mode TROS stops for four error conditions:

1. Sense Amplifier.
2. Control register.
3. Address.
4. Data Check (ALU - ER 4 bit).

2.8.1.13 Address Compare

Run: The micro program runs to its own ending point.

Stop: The microprogram runs to the address set in the Stop Address switches.

Recycle: The micro program runs to the address set in the Stop Address switches. It then restarts at the address set in the Start Address switches.

NOTE: Do not recycle on scan words, 004, 100, 200, etc.

Scan: A position of the switch, used in conjunction with micro diagnostic statements (GP + 0 + 1 → GP, A → X), which allow one of the TROS module's 256 words to be read out repetitively for parity checking by the ROS parity checking circuits.

2.8.1.14 Start Address

Two functions:

1. The two low order switches are used as a data source. When the enter switch is depressed the selected register is loaded.
2. All three switches are used as a starting address for the micro program. The switch output is loaded into W and X registers when the Set Address switch is depressed.

2.8.1.15 Stop Address

The stop address switch is used in conjunction with the Address Compare switch to control the sequence of the micro program. When the micro program

stops at the Stop Address switch setting, that address has not yet been read out of TROS.

NOTE: The Stop Address Sync hub furnishes a negative going pulse in either CE or Normal. The sync pulse is 325 ns in duration. The Sync pulse starts at D time of the cycle where the contents of the W and X registers are the same as the address in the three stop address switches. This Sync pulse is useful in tracing an operational CAS micro program through CLD's.

2.8.2 CE Indicators

The W, X and A registers are always displayed. In CE mode, the A register can be loaded with a selected register by depressing and holding the Display switch.

2.8.2.1 Sense Amp

When on indicates a parity error in CA, CB, CK, CH, CL, PA, or PS Control fields.

2.8.2.2 Control Register

When on indicates a parity error in CV, CS, CD, CC, BY, or PC control fields.

2.8.2.3 Address

When on indicates a parity error in X register P bit, W register P bit, CN, PN, or PA TROS fields.

2.8.2.4 Machine Stop

When on indicates that TROS is stopped. The machine clock is still running. The contents of TROS sense amplifier latches are frozen. TROS continues to cycle.

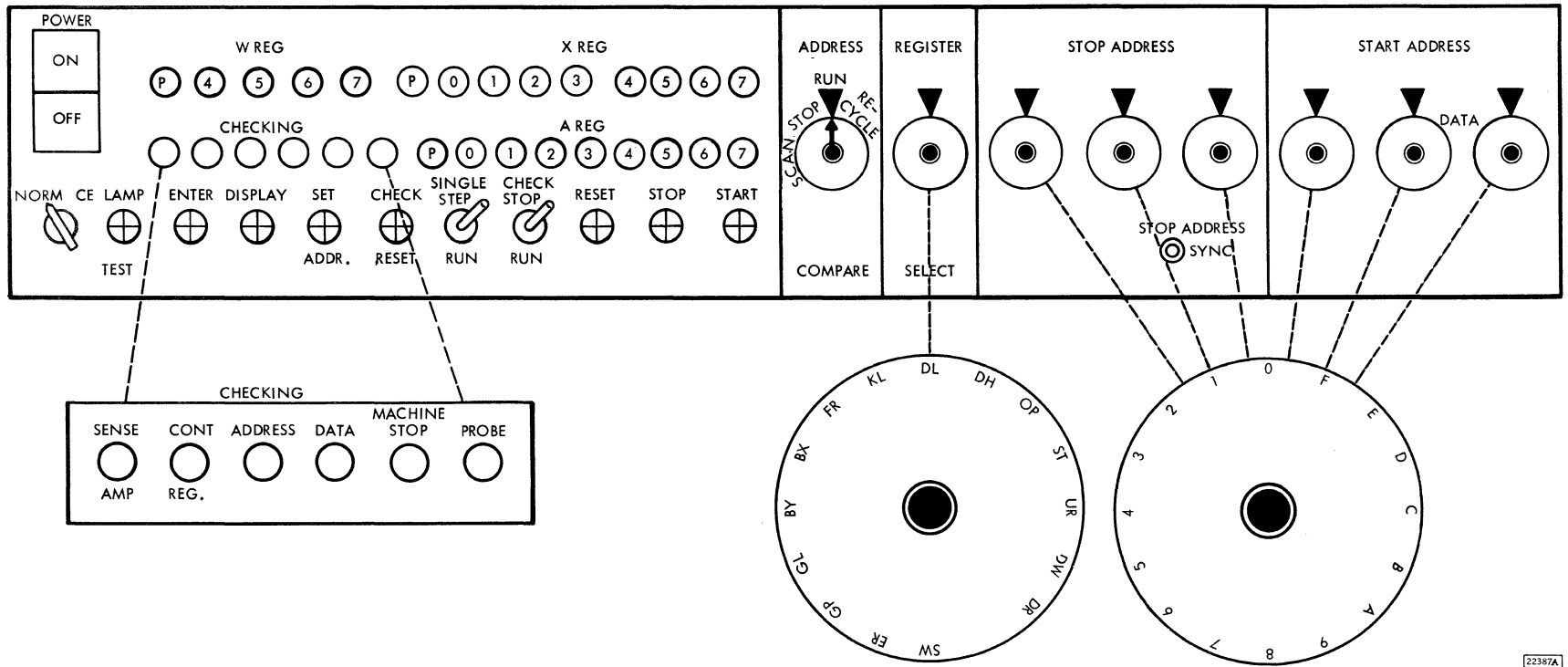
2.8.2.5 Probe

The Probe indicator is used as a diagnostic tool. See Check Stop/Run switch.

2.8.2.6 Data Check

The Data Check indicator is on for three reasons:

1. Serial Write Data Error.
2. Bus Out Parity Error.
3. ALU Error is developed when a bypass ALU statement is used and A Reg Parity does not agree with ALU parity. ALU error also turns



22387A

2-38. CE Panel

on the Machine Stop indicator in Normal mode, or in CE mode if the Check Stop/Run is in the Check Stop position.

2.9 CAS MICROBLOCK

- 48 bits are read from TROS each 500 nano-seconds (ns).
- The 48 bits form one TROS word.
- The word is divided into 15 fields.
- Collectively, the fields define the 2841 operation for the next 500 ns.

48 bits are read out of the TROS array every 500 ns and are called a TROS word. The word is divided into 15 fields. Collectively, these fields define the operation of the 2841 for the next 500 ns.

This section of the manual defines these fields, shows how they are represented in a microblock, and includes a sample usage of several microblocks to perform a logical function (Seek).

2.9.1 TROS Bit Assignment Chart (Figure 2-39)

The TROS word is divided into 15 control fields. Each one of these fields performs a particular function during one machine cycle. A description follows:

2.9.1.1 CN

The value contained in CN is loaded into the six high order bits of the X register. In addition, CN-5 is used as the data source when loading the FT register and FC register.

2.9.1.2. PN

PN is a parity bit for the CN and PN fields. Total parity should be odd.

2.9.1.3 CD

The value contained in this field gates the output of ALU (A register if Bypass bit on) to one of seventeen destinations (i.e., 7→DH would gate the output of ALU to the DH register).

NOTE: Even though the data was loaded into a register, it is still on the D Bus and can be tested by the

microprogram. $A + B \rightarrow D$ means to place the output of ALU on the D Bus only.

2.9.1.4 CV

The value contained in CV determines if the B register is gated in True or Ones Complement form to ALU.

2.9.1.5 CC

The value contained in CC determines the ALU operation. There are eight different ALU statements. Five different symbols are used to indicate the arithmetic operation:

- + Add Positive
- Complement Add/Subtract
- . AND
- Ω OR
- ⊕ Exclusive OR

CC=0: Add or Subtract (CV) the A and B register outputs. Carry In of zero to the low order ALU position. Example: $KL+BY+0 \rightarrow DH$

CC=1: Add or Subtract (CV) the A and B register outputs. Carry In of one to the low order ALU position. Example: $KL+BY+1 \rightarrow DH$

CC=2: AND the A and B register outputs. Example: $KL . BY \rightarrow DH$

CC=3: OR the A and B register outputs. Example: $KL \Omega BY \rightarrow DH$

CC=4: Add or Subtract (CV) the A and B register outputs. Carry In of zero to the low order ALU position. If there is a Carry Out of the high order ALU position, set ST(3). Example: $KL+BY+0 \rightarrow DHC$

CC=5: Add or Subtract (CV) the A and B register outputs. Carry In of one to the low order ALU position. Carry Out, set ST(3). No Carry Out, reset ST(3). Example: $KL+BY+1 \rightarrow DHC$ (C means set ST(3)).

CC=6: Add or Subtract (CV) the A and B register outputs. Use the present condition of ST(3) as a Carry In to the low order position of ALU. If there is a Carry Out, set ST(3). No Carry Out, reset ST(3). Example: $KL+BY+C \rightarrow DHC$

CC=7: Exclusive OR the A and B Reg outputs. Example: $KL \oplus BY \rightarrow DH$

2.9.1.6 CS

The value contained in this field controls the setting and resetting of individual bits in the Status register; i. e., CS=6 (DN ST 21) means if the D Bus does not equal zero set ST(2) to a one. The only way to turn ST(2) off is with a CS=5 (0→ST2) statement.

2.9.1.7 PC

PC is the parity bit for CV, CS, CD, CC, BY and PC fields. Total parity should be odd.

2.9.1.8 PS

PS is the parity bit for CA, CA Alt., CB, CK, CH, CL, PA and PS fields. Total parity should be odd.

2.9.1.9 BP

The value contained in BP determines whether the ALU or A register output is placed on the D Bus. With this bit on, a parity check of the A register P bit and the ALU generated P bit is made. An error hard stops the 2841 with the Data Check lamp on. Example: KL+0 → DH, BYPASS.

2.9.1.10 CH

The value contained in CH allows a particular condition in the machine to be tested. X register bit 6 is set or reset depending upon the result of the test. A summary of CH branching conditions follows:

CH=0: Set X 6 off.

CH=1: Set X 6 on.

CH=3, D, E, or F - Test an OP register bit. If it is on, set X 6. If not, reset X 6.

CH=2, 4, 5 or 6 - Test a ST register bit. If it is on, set X 6. If not, reset X 6.

CH=7: Test 2321 Interface selected. If it is on, set X 6. If not reset X 6.

CH=8: Reset X 6. Gate bits, 3, 4, 5, 6, and 7 of the CK field to the W register if the microblock contains a CK→W statement.

CH=9: Test the ALU Carry Out Latch. If on, set X 6. If not, reset X 6.

CH=A: Test Command Out. If on, set X 6. If not, reset X 6.

CH=B: Test Suppress Out. If on, set X 6. If not, reset X 6.

CH=C: Not used

2.9.1.11 CL

The value contained in CL allows a particular condition in the machine to be tested. X register bit 7 is set or reset depending upon the result of the test. A summary of CL branching conditions follows:

CL=0: Set X 7 off

CL=1: Set X 7 on

CL=2, 3, or 4: Test a ST register bit (3, 5 or 7). If on, set X 7. If off, reset X 7.

CL=5: Test the ALU, D=0 latch. If on, set X 7. If off, reset X 7.

CL=6: Do not gate CN 0-5 and the results of the CH and CL branch tests to the X register. Instead, gate the contents of the A bus to the X register. This statement should only be used when the address compare switch is in SCAN, since it actually gives a 256-way branch.

CL=7: Test optional Interface selected. If it is on, set X 7. If off, reset X 7.

CL=8: Test service out. If it is on, set X 7. If off, reset X 7.

CL=9: Test Service-Out Response. If it is on, set X 7. If off, reset X 7.

CL=A: Test Select Out. If it is on, set X 7. If off, reset X 7.

CL=B, C, D, or F: Test an Op register bit. If on, set X 7. If off, reset X 7.

CL=E: Test for Index. If Index, set X 7, if not, reset X 7.

NOTE: Before Index can be gated to the CL Branching Circuits, the microporgram must allow Index by issuing the CS statement 1→ST1.

TROS Tape (SAL Bit) →	17	19	21	23	27	29	31	33	35	37	39	41	43	45	09	11	13	15	01	03	05	07	47	42	00	02	04	06	08	10	12	14	16	18	20	22	24	26	28	30	32	34	36	38	40	25	46
Word Bit Position →	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46
Field Name →	CA Field				CB	CK Field							CL Field				CH Field		PA	PS	CN Field					CD Field			CD ALT	CV	CC			CS			PC	CA ALT	BP								
Field Bit Position →	1	2	3	4	0	1	0	1	2	3	4	5	6	7							0	0	0	1	2	3	4	5	0	0	1	2	3	0	0	1	2	0	1	2	3	0	0	0			
Binary Value →	8	4	2	1	2	1	128	64	32	16	8	4	2	1	-				-		-	-	-					-	-	8	4	2	1	16	1	4	2	1	8	4	2	1	-	16	-		
Use →	A Reg Entry				B Ent	W Reg or B Reg Entry							Branch X7				Branch X6		P	P	Next Address X0-5					Destination			ALU Control			ST Control															
	16	0					CK3 Becomes W Reg Parity on K→W Statements.							0→X7				0→X6		N	N	Except on A→X Statements when the next Address is the Contents of the Register Defined by the CA Field in the ALU Statement. CNS is Sometimes Shown as a 1 or 0 in the Leg Selector when it is used as a Control of Certain Registers					Normal	Alt	See Note 5					Not Used			N	O	T								
	17	1	GL	Stop	None	SW	None							1→X7				1→X6		O	O						D	SW	A+B→D					0→ST0			N	O	T								
	2		BY											ST3				ST0		E	E						BY		A.B→D					1→ST0			E	E									
	3		BX											ST5				OP6									BX		A∩B→D					0→ST1													
	4		FR											ST7				ST2		3	3						FR		A+B→DC					1→ST1			3		4								
	5		KL											D=0				ST4							KL		A+B+1→DC					0→ST2															
	6		DL											A→X				ST6							DL		A+B+C→DC					DNST21 Note 1															
	7		DH											File Note 2				File Note 2							DH		A×B→D					0→ST3															
	8		OP											SERVO				K→W(0→X6)							OP		A-B→D					1→ST3															
	9		GP											SORSP				Carry							GP		A-B+1→D					0→ST4															
	10		UR											SELTO				COMMO							UR		A.-B→D					0→ST5															
	11		DW											OP1				SUPPO							DW		A∩-B→D					1→ST5															
	28	12	DR	SC										OP3				Unused							DR		A-B→DC					0→ST6															
	29	13	ER	FS										OP5				OP0							FT		A-B+1→DC					1→ST6															
	30	14	IE	OA										Index				OP2							FC		A-B+C→DC					0→ST7															
	31	15	IH	IS										OP7				OP4							IG		A×-B→D					1→ST7															

- NOTE 1 DNST21 says set ST2 to 1 if D bus is non-zero. ST2 is never set to zero by this statement.
- NOTE 2 File branching is a hardware decode of the IE register; Where CH.CL 00 = 2302, 01 = 2311, 11 = 2321.
- NOTE 3 PA is parity bit for address of the word reading out PA.
 PS is parity bit for CA, CB, CK, CL, CA ALT, PA
 PC is parity bit for CD, CD ALT, CV, CC, CS, BP
 PN is parity bit for CN.
- NOTE 4 BP is set by bypass statement in line 3 of microprogram box. It Activates the ALU checking circuits.
- NOTE 5 CC decode of 4,5 or 6 sets ST3 with carry out (DC).
 CC decode of 6 sets carry in with contents of ST3 (+C).

22391A

2-39. TROS Bit Assignment Chart

2.9.1.12 CA

The value contained in CA gates a particular source to the A Bus. i.e. CA=0 places zero on the A Bus. CA=D places the contents of ER on the A Bus.

CA=11, STOP, is a special use of the CA field. This statement is used in the microdiagnostics. Check Stop/Run switch in the Check Stop position and the Stop statement stops the 2841. Refer to ALU microdiagnostic for examples of the Stop statement.

2.9.1.13 CB

The value contained in CB gates a particular source to the B Bus. i.e. CB=0 places zero on the B Bus. CB=3 places the contents of DR on the B Bus.

2.9.1.14 CK

The value in the CK field is used as a constant data source by the micro program. i.e. KL+9 →DL. The nine is in the B entry position in the ALU statement. To gate CK to the B Bus, it is necessary to make the CB field equal 2.

Bits 3, 4, 5, 6, and 7 may also be gated to the W register module switching in TROS. This is accomplished by making the CH field 8 and issuing a CK → W (i.e. 3 → W) statement. CK 3 is used as W register parity bit.

2.9.1.15 PA

PA is the parity bit for the combined W and X registers.

W														
P	4	5	6	7	P	0	1	2	3	4	5	6	7	Hex address 58B ↓
1	0	1	0	1	1	1	0	0	0	1	0	1	1	

The sum of the bits is even, therefore, PA is punched for a output of one from TROS tape.

2.9.2 Microblock Symbology

- The microblock is divided into eight lines of information.
- Each line identifies a particular function of the machine.

2.9.2.1 Line 1 (Figure 2-40)

Line 1 contains a leg identifier and the hexadecimal address of the microblock.

The leg identifier consists of two characters which are indicative of the setting of X register, bits 6 and 7 for this block. Valid symbols and their meanings follow:

- 0 Appropriate X bit is off
- 1 Appropriate X bit is on
- X Setting of appropriate X bit is not shown in leg identifier.

The hexadecimal address consists of three digits. The first one represents the value set in the W register. The other two represent the value set in the X register.

2.9.2.2 Line 2

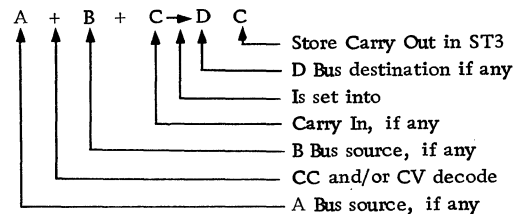
Line 2 contains an emit value. This represents a binary picture of the CK field when the CK field is used in ALU statements. It is identified by an E on the left side of the microblock, i.e. KL + 29 →BY; emit value = 00011101.

2.9.2.3 Line 3

Line 3 contains the ALU statement. It is identified by an A on the left side of the block. A summary of the line ALU arithmetic symbols follows:

- + Add Positive
- Complement Add/Subtract
- . AND
- Ω OR
- ⊕ Exclusive OR

Symbolic ALU Statement:



A summary of the eight ALU statements follows. The DH, KL, and BY registers are used in the examples.

CC Decode

0	KL ±BY → DH
1	KL ±BY + 1 → DH
2	KL . BY → DH or KL . -BY → DH
3	KL Ω BY → DH or KL Ω -BY → DH
4	KL ±BY → DHC
5	KL ±BY + 1 → DHC
6	KL ±BY + C → DHC
7	KL ∓BY → DH or KL ∓-BY → DH

Line 3 also contains the BYPASS statement.

2.9.2.4 Line 4

Line 4 is not presently used.

2.9.2.5 Line 5

Line 5 contains the status register set/reset statement. The line is identified by a C on the left side of the microblock.

The status set/reset statement, if any, takes the format shown in the bit assignment chart (Figure 2-44).

2.9.2.6 Line 6

Line 6 is used for the branching test statements. It is identified by an R on the left side of the microblock. Refer to the bit assignment chart (Figure 2-39) for the conditions which may appear in this area.

NOTE: CK→W statement appears in the CH position. It causes X register 6, to be reset.

2.9.2.7 Line 7

Line 7 contains Replaceable Word Code information. The line is identified by an F on the left side of the block.

The Replaceable Word Code is defined as follows:

Every announced feature is assigned a code number, starting with 1 and progressing to 999. The basic machine has no number assigned.

When a location in the ROS is used by more than one option (basic or feature), each definition of the word, as shown by a CAS logic block, must contain the code of the feature which requires the word. If two or more features require the installation of the same word, all the feature numbers must appear in the block, with a , or / to indicate and or "or." Only one type symbol can appear in a block.

If a ROS word location is not assigned a basic or feature use, or assigned only to a feature and the

feature is not installed, then the contents of that location is zero with correct parity in all fields, and the next address (CN field) is its own physical address.

Examples:

F = 4, Indicates that this word is installed if feature 4 is installed.

F = 1, 2, 6. Indicates that this word is installed only if feature 1 and 2 and 6 are installed at the same time.

F = 1/2/12. Indicates that this word is installed by either feature 1 or 2 or 12 or any combination of them.

Initial replaceable word code assignment:

2302	1
2321	2

Additional Storage	5
File Scan	6
Record Overflow	7
2 Channel Switch	8

2.9.2.8 Line 8

Line 8 contains a drawing coordinate, leg selector, and box serial designation.

The drawing coordinate and box serial designation are used mainly by engineering and design automation in physically locating the blocks on a CAS sheet.

The leg selector consists of two or three characters. If there are three, the first one (left most) represents the condition of CN-5. It is used as a data input to the FT and FC registers, and is always a one or a zero.

The other two characters indicate X register, bits 6 and 7 settings for the next microblock. Valid characters and their meanings follow:

- 0 Set appropriate X bit to 0
- 1 Set appropriate X bit to 1
- X Setting of the appropriate X bit is not shown in the leg selector (look at C line)
- * Setting of appropriate X bit is under control of condition tested in CH or CL branching statement.

2.9.3 Sample Usage of Microblocks (Figure 2-41)

This example shows how several microblocks may be joined to perform a logical function. In the example,

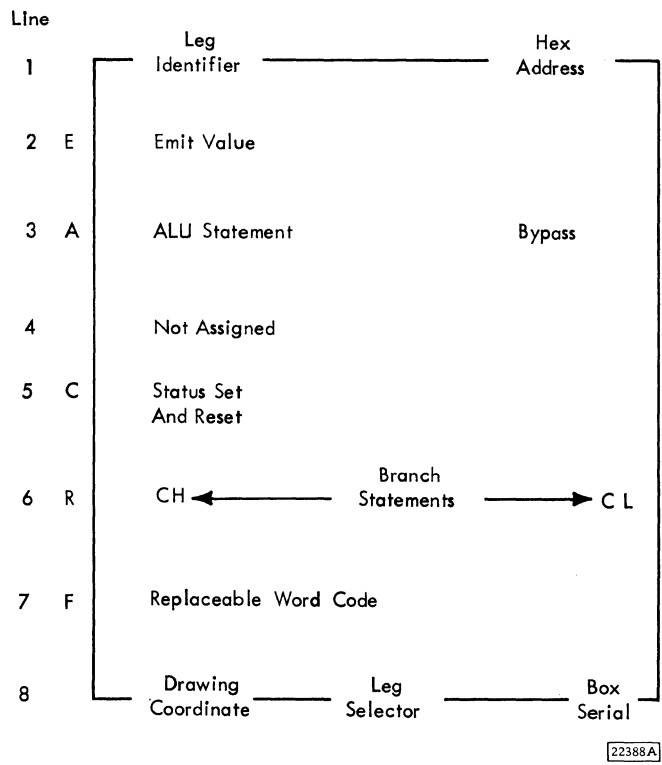


Figure 2-40. CAS Microblock

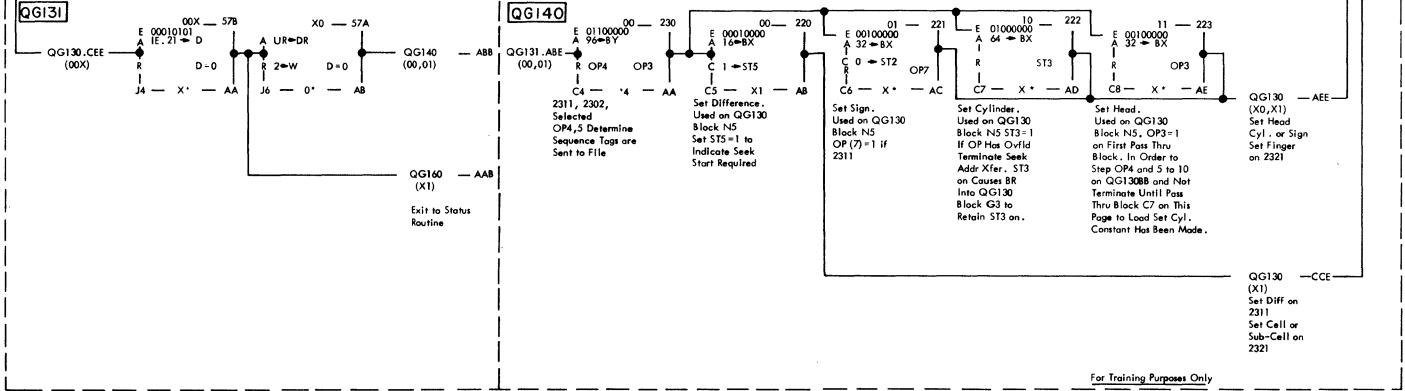
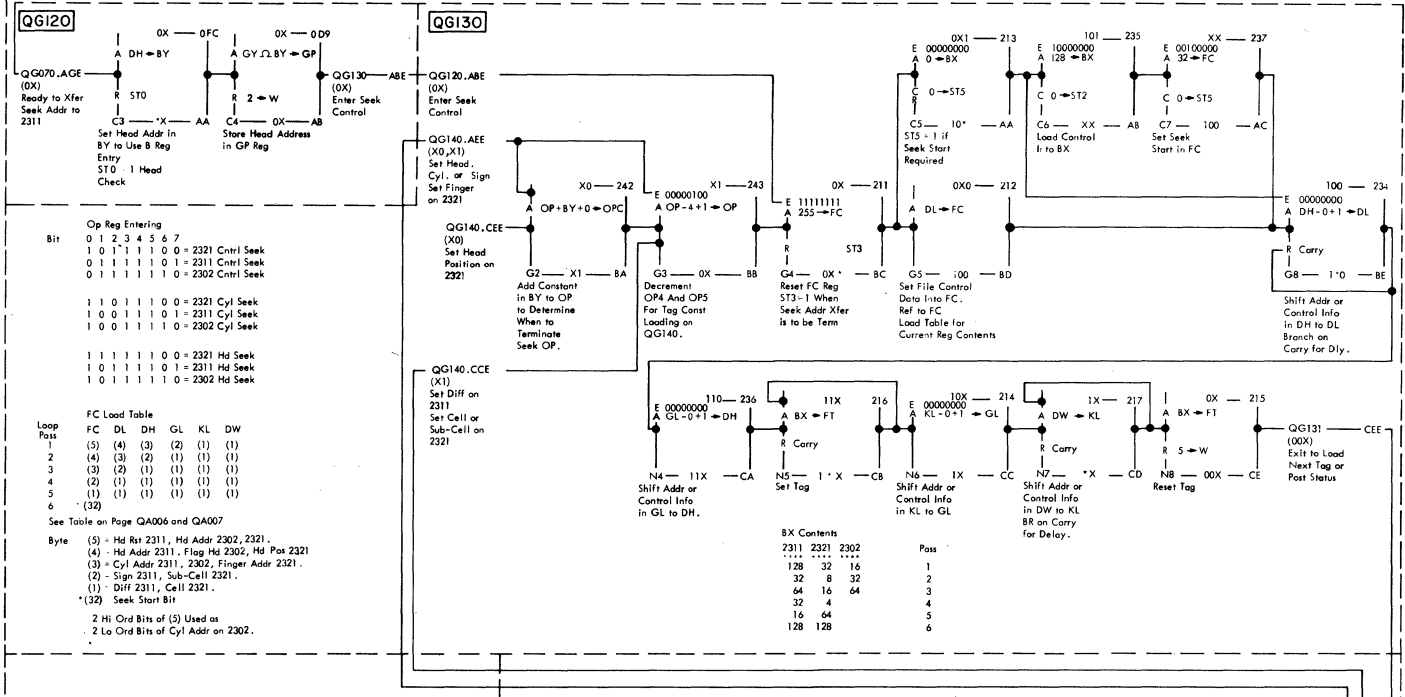
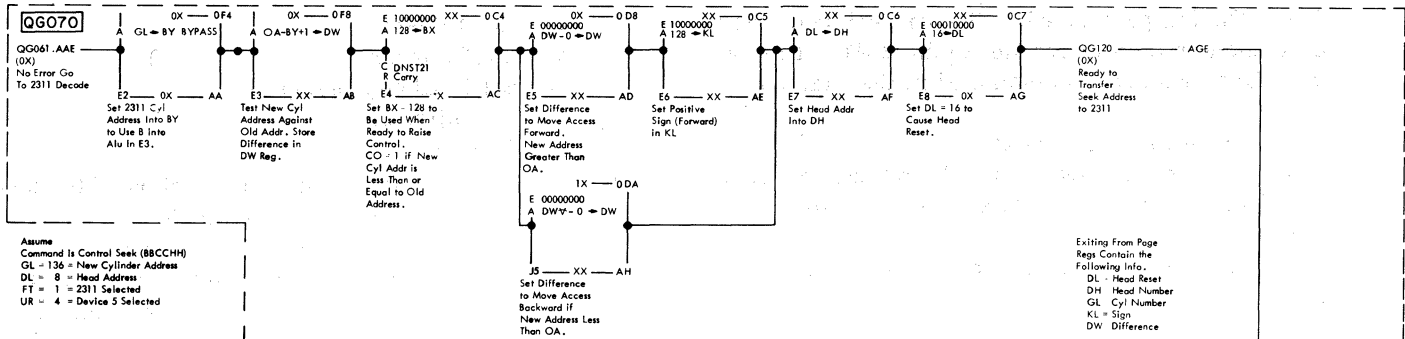


Figure 2-41. Sample Usage of Microblocks

a Seek CCHH is performed. The six Seek bytes have been transferred from channel to the 2841. The following functions are accomplished in the example:

1. 2311 - Module 5 selected.
2. The difference between the old cylinder address and the new cylinder address is computed.
3. File Operable is tested.
4. Five Seek control lines are raised to the 2311.
 - a. Head Reset
 - b. Set Cylinder
 - c. Set Head and Direction
 - d. Set Difference
 - e. Seek Start
5. Ending status is posted and transferred to channel. Three assumptions are made:
 - a. The old cylinder address was 100.
 - b. KL contains the new cylinder address, 136.
 - c. DR contains the head select address, 8.

3.1 STATUS INFORMATION

- The status byte consists of eight bits.
- It is used to notify channel of the condition of the 2841.
- All 2841 commands, with the exception of Seeks and Command Immediates, transmit two (initial and ending) status bytes to channel.
- Cylinder Seeks and the Restore commands transmit three bytes (initial, channel end, device end) to channel.
- Command Immediates (No-Op and Release) transmit one status byte (channel and device end in initial) unless they are chained after a write command. In this case, they transmit two (initial and ending).

The Status Byte contains information which reflects the status of the 2841 and the selected device attached to the 2841. The significance of each bit in the Status Byte is listed below:

Bit	Name	Note
0	Attention	Not used
1	Status Modifier	Used with Search and Control Unit Busy.
2	Control Unit End	The Control Unit has finished a operation.
3	Busy	Addressed Access Mechanism is moving or used in conjunction with Status Modifier to indicate Control Unit Busy.
4	Channel End	The Control Unit has received all the data from the channel needed to do the operation called for and the channel is freed.
5	Device End	Indicates that an access mechanism is free to be used.
6	Unit Check	Indicates that a Control Unit or programming error or device hardware check has been detected.
7	Unit Exception	End-of-File.

A more detailed description follows:

Attention (Bit 0): Not Used.

Status Modifier (Bit 1): This bit is set whenever a Search High, Search Equal or a Search High or Equal command has been executed and the condition satisfied.

The Status Modifier is also set whenever the 2841 is busy. This bit in conjunction with the Busy bit signifies Control Unit Busy.

Control Unit End (Bit 2): This bit is set if a Control Unit Busy Status has been generated previously and the busy condition has been terminated. Bit 2 is also set with Unit Check when Unit Check occurs after Device End.

Busy (Bit 3): The Busy bit may indicate either device busy or control unit busy:

1. **Device Busy:** The Busy bit indicates that the selected device is busy. It will be set when a new command chain is initiated while the selected access mechanism is still in motion due to a previous Seek command. Busy is also included in the response to any command except Test I/O if there is outstanding status for the device.
2. **Control Unit Busy:** The Busy bit in conjunction with the Status Modifier bit indicates the control unit is busy. It will be set when a new command chain is initiated while the 2841 is causing a track to be erased following a Format Write Command or an Erase command. It is also set if an attached 2321 is addressed while performing an automatic strip restore.

Channel End (Bit 4): This bit is set when the channel to control unit operation is completed.

Device End (Bit 5): This bit indicates that an access mechanism is free to be used. After a Seek or a Restore command, Device End is presented to the channel together with the Unit Address to indicate a Seek Complete. It is generated simultaneously with Channel End at the end of all other commands. Device End is also generated when an attached device goes from a Not Ready to a Ready condition.

Unit Check (Bit 6): This bit is set whenever an unusual or error condition is detected in the 2841 on the selected device. Sense Bytes 0, 1 and 2 provide detailed information as to the nature of the condition. Channel End and Device End are always presented with Unit Check unless the Unit Check is presented in Initial Selection Sequence.

Unit Exception (Bit 7): This bit indicates that an End-of-File has been detected during a Read IPL, Read R0, Read CKD, Read KD, Read D, Write KD, Write D or Search-Key-Data operation. It is not set for Read Count, Write CKD or Search Key or ID commands. Unit Exception results from a data length of zero. The Key Field, if any, is transferred.

All 2841 commands result in two status bytes (initial and ending) with the following exceptions:

1. Immediate Commands: No-Op and Release are processed as immediate commands only if the Control Unit is not writing or erasing at the time the command is received (chained). If not writing or erasing, channel and Device End are indicated in the initial status byte (one status byte only). If writing or erasing, zero is transmitted in the initial status byte. Channel and device end are indicated in the ending status byte when the 2841 finishes writing or erasing.
2. SEEK type commands: A Seek (CCHH, or BBCCHH) that causes the access to move or a Restore command results in three status bytes:
 - a. Initial
 - b. Channel End after data transfer from the CPU.
 - c. Device End after the device has stopped seeking (Gated Attention).
3. A third status byte may occur on write commands if channel has already accepted Device End. This could occur, i.e., if the device went unsafe while completing a formatting write. In this case a status byte containing Control Unit End and Unit Check would be transmitted to channel via the polling interrupt sequence.

3.2 SENSE INFORMATION

Six bytes of Sense Condition information are provided by the 2841 to completely identify the setting of the Unit Check bit in the Status Byte. These six bytes are transferred to the channel by issuing a Sense command.

3.2.1 Sense Byte 0

Command Reject (Bit 0): This bit indicates that the 2841 has received an invalid operation code, an invalid sequence of commands, or an invalid Seek Address. Detection of a Bus Out parity with a command does not set Command Reject. If a Write File Mask is violated, Command Reject is set along with File Protect.

Intervention Required (Bit 1): This bit indicates that the specified device is:

- a. Not physically attached to the system.
- b. The specified device is physically attached to the system, but it is not available for use because the motor is not On, a cover interlock is Open, etc.

Bus Out Parity (Bit 2): This bit indicates that a data parity error has been detected during the transfer of information from the channel to the 2841. This check is an odd redundancy check that occurs on Control, Write and Search operations. The check is done by the 2841. A parity error detected during command transfer is a Bus Out check and not a Command Reject.

Equipment Check (Bit 3): This bit indicates that an unusual condition is detected in the Control Unit or Device Unit. The conditions that are covered by the bit are defined in Sense Byte 2.

Data Check (Bit 4): This bit indicates that a data error has been detected in the information received from the device.

Overrun (Bit 5): This bit indicates that a Service Out signal was not received in the 2841 within a specified time allowed after Service In or that a chained CCW was issued but that it was received too late to be properly executed. Detection of an overrun during reading or writing causes an immediate stop of data transmission. When writing, the remaining portion of the record area is padded out with valid zeros.

Defective Track (Bit 6): (Track Condition Bit 6 = 1) — A Track Condition check is generated for a defective track whenever:

1. Any Read or Search (except Search HA, Read HA, Read R0) is attempted on the track in either multi track or single track mode. The interrupt occurs prior to transmission of any data to or from the channel.
2. An overflow record being read, written, or searched overflows to a track flagged as defective. The interrupt occurs after the last byte on the previous track has been operated on and before the first byte for the defective track is requested from or sent to the channel. In this case, Overflow Incomplete is also set. Bits 1, 6, and 7 in Sense Byte 2 are also set to define the operation in process at the time of the interrupt.

Alternate Track (Bit 6): (Track Condition Bit B7 = 1)

— A Track Condition check is generated when command chaining and multiple track mode signals indicate that operations are to continue on the next high-ordered track or the record is not the last segment of an overflow record. The Track Condition Check indication inhibits the incremental head switching.

Seek Check (Bit 7): This bit indicates that the device has been unable to successfully complete a Seek due to:

1. The transferred Seek address is outside the valid address boundaries of the device. The unused bytes must contain zeros. This condition also sets Command Reject.
2. Less than six bytes of Seek address is sent. This condition also sets Command Reject.
3. Failure of hardware which results in the access mechanism failing to detent correctly.
4. On Multi-track operations, the Home Address of the track advanced to does not compare with the physical address.

3.2.2 Sense Byte 1

Data Check in Count Field (Bit 0): This bit indicates that a data error has been detected in a Count Field read from the device. Data Check in Byte 0 is also turned on. Error detection is the same as described for Data Check (Byte 0, Bit 4). The operation is terminated at the end of the Count Field.

Track Overrun (Bit 1): This bit indicates that writing has not been completed by the time Index Point is detected. This type of error is detected during a Write-R0, Write-Count, Key and Data, Write-Key and Data, Write Data or Space Count operations.

If the bad record is read with subsequent Read commands, the Track Overrun condition is not set.

End-of-Cylinder (Bit 2): This bit indicates that the CCW Command Chain has not been completed, but that end-of-cylinder has been detected.

Invalid Sequence (Bit 3): This bit indicates that an attempt has been made to execute an invalid sequence of CCW's. Invalid sequences are normally related to Write operations. Invalid sequences also occur if two Set File Mask CCW's operations are attempted in the same chain of CCW's, if head switching is attempted without prior seeking, or if a Space Count is preceded by a Write command. Command Reject (Bit 0 - Byte 0) is also turned on when an Invalid Sequence is encountered.

No Record Found (Bit 4): The No Record Found function is included in the 2841 so that the programmer may use a sequence such as:

Search ID (MTM Off)
TIC* - 8
Read Data

without the possibility of the program getting trapped in an endless loop in the event that the desired record is not contained on the track being searched. The No Record Found function occurs as follows:

1. An Index Passed condition is turned on whenever Index point is sensed on the device.
2. The Index Passed condition is turned off whenever the 2841 performs a read operation in a HA or data field area, any write command, a sense command or any control command.
The Index Passed bit is also reset when chaining is broken.
3. No Record Found condition occurs whenever the 2841 senses Index point while performing a single track read or search operation other than Read 0, or Read HA and the Index Passed latch is already on.
4. A No Record Found condition occurs when Index is sensed while executing a Space Count command following HA and no address mark is found. A No Record Found condition occurs with Missing Address Mark when neither HA or R0 can be found on the track.

The following programming notes apply:

1. Read CKD, Read Key Data and Read Data reset the Index Passed bit at the time the data field is read from the track. Hence, No Record Found may occur while one of these commands is being executed; most notably, No Record Found will occur when one of these commands is given and there is no address mark detected on the track.
2. The programmer should insure that spurious No Record Found conditions cannot occur. For example, in the sequence:

Read Count
Search Key
Tic* - 16
Search ID (of Count Field read above)
TIC* - 8
Read Key Data

the Index Passed bit is not reset prior to the Read Key Data command and Index point is passed once after the key is located prior to orienting on the desired ID. If the Index Passed latch is on at the time the desired key was found

(this cannot be predicted if the sequence was started with random orientation), then No Record Found condition will occur. The sequence may be corrected by inserting a Read HA or Read R0 immediately prior to the Search ID command (this is the best method since the added command will also eliminate unnecessary Search ID sequences between the located Key and the end of the track) or a NOP may be inserted. Also a Read HA or Read R0 could be included at the beginning of the sequence.

File Protected (Bit 5): This bit indicates that a Seek or Write CCW or MTM Read or Search command was issued that violates the file mask. The Command Reject bit is also set on detection of this condition if a Write File Mask is violated.

Missing Address Markers (Bit 6): A missing Address Marker is detected during the execution of any command or chain of commands which operate on successive count fields on a track. The detection is accomplished by identifying that two successive records on a track have equal bit conditions in Bit 0 of the Flag bytes. Under normal conditions, bit 0 of the Flag Byte is always a zero for all even-numbered records and is always a one for all odd-numbered records.

Upon detection of a missing Address Marker, bit six of Sense Byte One (Missing Address Marker) will be turned on for all commands or chained commands except Search ID CCW's. The Search ID CCW is used to pass over the Missing Address Marker so that the remaining data on the track can be retrieved. Data Check is also to be set on Missing Address Marker errors.

Overflow Incomplete (Bit 7): This bit is used with the optional Record Overflow feature. It is set as follows:

1. Overflow to a bad track — Set Overflow Incomplete and Track Condition Check.
2. Overflow from an Alternate Track — Set Overflow Incomplete and Track Condition Check.
3. Overflow to File Protected Boundary — Set Overflow Incomplete, File Protected.
4. Overflow to Wrong Track — Head number compares unequal — Set Overflow Incomplete and Seek Check.
5. Overflow to end of cylinder—Set Overflow Incomplete and End of Cylinder.

3.2.3 Sense Byte 2

Unsafe (Bit 0): This bit is used to indicate that a device malfunction has been detected. Some of these malfunctions are:

- More than one head has been selected.
- The device is trying to read and write at the same time.
- The Write gate is Off and Write Driver is On.
- The Write gate is On and the Write Driver is Off.
- The Erase Driver is Off and the Erase gate is On.
- The Erase driver is On and the Erase gate is Off.
- One of the DC file voltages has been lost (2311 only).

Bit 1: Reserved

Serializer/Deserializer Check (Bit 2): This bit indicates that a bit has been either lost or gained when the parallel channel data is converted to serial data during a Write Operation.

Bit 3: Not Used

2841 ALU Check (Bit 4): The micro program has detected an impossible condition, indicating an equipment malfunction.

Unselected Status (Bit 5): This bit indicates that some bit in the File Status lines is on without any module being selected. This indicates a device malfunction of some kind since no bit should be on prior to selection.

Bit 6: Reserved

Bit 7: Reserved

3.2.4 Sense Byte 3

This byte is used to present eight device interface lines to the CPU for diagnosis. The interface lines presented for each device type are shown below.

Byte 3	2311	2321	2302
0	Ready	Drive Ready	Access Ready
1	On Line	Drive Operative	Access Operative
2	Unsafe	Read Safety	Read Safety
3	-----	Write Safety	Write Safety
4	On Line	Strip Ready	On Line
5	End of Cylinder	Invalid Address	-----
6	-----	Auto Restore	-----
7	Seek Incomplete	CE Cell Located	CE Cylinder Located

3.2.5 Sense Byte 4

This byte is all zeros. It is included for compatibility with other control units.

3.2.6 Sense Byte 5

This byte is zero at all times except when overflow incomplete occurs (Byte 1, Bit 7). Information on the bit meanings is given in Chapter 5 - Record Overflow.

Sense Information Summary

Status Byte Condition	Sense Bit Condition	Sense Bit Position
Unit Check	Command Reject-includes Invalid Command, Invalid Sequence, & File Protected.	Byte 0, Bit 0
	Intervention Required	Bit 1
	Bus Out Parity	Bit 2
	Equipment Check	Bit 3
	Data Check	Bit 4
	Overrun	Bit 5
	Track Condition Check	Bit 6
	Seek Check	Bit 7
	Data Check in Count Field-also causes Byte 0, Bit 4 (Data Check) to be turned on.	Byte 1, Bit 0
	Track Overrun. Indicated on Write	Bit 1
	End-of-Cylinder	Bit 2
	Invalid Sequence-also causes Command Reject (Byte 0, Bit 0) to be turned on.	Bit 3
	No Record Found	Bit 4
	File Protected-also causes Command Reject (Byte 0, Bit 0)	Bit 5
Missing Address Marker-also causes Data Check (Byte 0, Bit 4)	Bit 6	
Overflow Incomplete	Bit 7	
Unsafe	Also turn on Equipment Check Byte 0, Bit 3	Byte 2, Bit 0
Not Used		Bit 1
Serializer/Deserialzer Check		Bit 2
Not Used		Bit 3
2841 ALU Check		Bit 4
Unselected Status		Bit 5

3.3 MISCELLANEOUS OPERATIONS

3.3.1 Multiple Track (M/T) Operation

The 2841 has the ability to automatically select the next sequentially numbered head on an access mechanism under control of B0 of the Command byte. Head switching will not take place at Index Point if B0 is a 0. Head switching will take place at Index Point if B0 is a 1. If A seek CCW must be given in each chain of commands in which a M/T command is given.

The M/T bit is recognized on all Read and Search commands. Therefore, a certain amount of discretion should be used when making B0 a 1-bit. For example, if during a Search operation the M/T bit is a "1" and Index is encountered before the search condition is satisfied, the head will automatically switch to the next track. The operation will continue until the End-of-Cylinder is detected. This condition can occur if the Search was initiated beyond the point where the record was located on the track. On the other hand, by correctly utilizing the M/T bit, it is possible to search a complete cylinder of ID's or Keys.

Each time head switching occurs, the units cylinder and head number (CHH) in the Home Address of the new track is read by the 2841. If the head number is incorrect, Seek Check is set.

3.3.2 End-of-File

The End-of-File indication is written by executing a Write-Count, Key, and Data CCW that has a data length of zero indicated in the Count Area. Execution of the Write-Count, Key, and Data CCW with a DL of zero, causes the 2841 to automatically write one byte of 0's in the Data portion of the End-of-File record. The KL portion of the Count Area can either be zero or up to 255 bytes. If KL = 0, the End-of-File record will contain the contents of the Count Area and the Data Area (one byte of 0's). If KL = 0, the key whose length is specified by KL will be written in the Key area of the End-of-File record.

As a logical file is being read, the Count Area of the records is examined. Detection of a DL of zero in the Count Area causes a Unit Exception signal to be generated. The Unit Exception signal is always generated at the normal ending time of the Read operation that was scheduled to be performed. No data from the Data Area will be transferred.

NOTE: Key data will be transferred.

The Unit Exception is possible during Read IPL, Read R0, Read CKD, Read KD, Read D, Write KD, Write D, and Search KD operations.

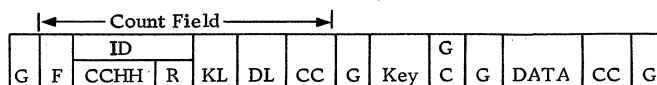
3.3.3 Defective Surfaces

- Provision is made so that a logical file of more than one track can be continued when a track with a defect is found.
- The defect must not be in the Record zero area.
- The condition of the track and the alternate track are indicated in the Flag bytes.
- The address of the alternate track is written in the Record Zero Data field.

The 2841 has the ability to handle defective recording areas that may appear during the life of the storage medium. The instrument that permits defective areas to be circumvented is the Track Descriptor Record (R0). Implementation of the R0 concept is dependent upon the availability of a perfect recording area on each track that extends from the Index Point to the end of R0.

R0 is always the first record on the track following the Home Address. The schematic representation of R0 is:

Track Descriptor Record - R0



F = Flag Byte. Bits 6-7 of the Flag Byte are called the Track Condition bits and are used to determine the condition of the track. This condition code is propagated to all records on that track. The significance of the Track Condition Bits is as follows:

- B6 = 0 = good track
- B6 = 1 = defective track
- B7 = 0 = not an alternate track
- B7 = 1 = alternate track

B0 of the Flag Byte is used internally by the 2841 to check for missing Address Marks. B1 is used for Record Overflow feature. B2 - B5 of the Flag Byte are not used.

ID = Identifier. The ID includes cylinder, head and record number. Cylinder number is two bytes in length. Head number is two bytes in length. Record number is 1 byte long and identifies the sequential position of the record on the track. The total ID is 5 bytes long.

KL = Key Length. The Key Length is 1 byte long and contains the length of the Key area.

DL = Data Length. The Data Length specifies the number of bytes in the data portion of the record. DL is two bytes long.

CC = Code Check Bytes. This is a series of bits used for error detection purposes. CC is two bytes long.

G = Gap. The gap separates the various areas associated with the record.

K = Key. The Key area is used to identify the Data area.

D = Data. This is the information associated with the record. The Data area can be variable in length.

Note that an R0 type record is not preceded by an Address Marker.

Read-R0 and Write-R0 are special commands that are associated with the R0 function. Read-R0 operates the same as a Read CKD with the exception that it never sets track condition. Write R0 operates the same as Write CKD.

The R0 (alternate) approach to the defective area problem permits entire tracks to be repositioned independently of the way the file is organized, i.e., random or sequential. In either case, the following conditions prevail:

1. Original Track (Good)
In this case, the Track Condition bits (B6, B7) are set at 00.

2. Original Track (Defective)
In this case the Track Condition bits are set to 10.
3. Alternate Track (Good)
In this case the Track Condition bits are set to 01.
4. Alternate Track (Defective)
In this case the Track Condition bits are set to 11.

The sequence of events that are required to move the data from a defective track to a good track is as follows:

1. Determine track is defective by repeated write and read-check operations.
2. If track is considered to be defective, assign alternate track.
3. Read as much information as possible from defective track into central processing unit.
4. In CPU change Count portion of R0 of original track to address of alternate track.
5. Set Flag Byte to 10 and put Flag Byte and Home Address in core memory. Execute a Write-Home Address command to change Track condition bits. Chain to write R0.
6. Re-write new R0 on defective track. The balance of the track is erased.
7. Set ID (CCHH) of Alternate track R0 equal to ID (CCHH) of original defective track.
8. Set Flag Byte of alternate track Home Address to 01 to indicate alternate track.
9. Initiate Seek to alternate track.

10. Command Chain from Seek to Set File Mask to Write-HA to Write-R0.
11. Copy data from original track onto alternate track.

During normal processing runs, detection of a defective recording area and the selection of its alternate area could be accomplished in the following manner:

1. Assume access mechanism has been properly positioned and desired head selected.
2. Execution of a command causes the Track Condition bits to be examined.
3. If the Track Condition bits indicate that this track is defective, Channel End, Device End, and Unit Check (Track Condition Check on Sense) signals are generated.
4. The interrupt routine associated with R0 causes count (address of alternate track) to be read into core memory.
5. This address is used to select alternate track (Seek operation).
6. At the completion of the Seek operation, the access mechanism is positioned on the alternate track and the proper head selected.
7. It is now possible to process the sequence of instructions called for in item two.
8. If multiple track mode and command chaining operation is being used, Channel End, Device End and Unit Check will occur at Index time, Track Condition occurs on a Sense. The using system then issues a Seek to the address of the original track plus one. Normal operation resumes when the desired track is reached.

The procedures described above apply when it is necessary to relocate an entire track and to process on a relocated track. It is also possible on sequentially organized data files, where the track is not preformatted, to handle defective areas as they are detected thus eliminating the need to relocate an entire track unnecessarily.

One method that might be used in this instance is:

1. Write desired records on selected track.
2. Read-check track just written.
3. If error is detected, rewrite and read check several times to determine if defective area exists.
4. When defective area is found, Search on last good ID or Key and execute appropriate Write commands. Execution of the last Write command causes the remainder of the track to be erased.

3.3.4 Initial Program Load (00000010)

- Provides a method of setting a program into the CPU from an access mechanism.

An Initial Program Loading (IPL) procedure is provided for the initiation of processing when power is turned On or when the contents of storage are not suitable for further processing.

The IPL procedure for random access devices is as follows:

1. The channel, control unit, and access mechanism from which the first IPL information is to be read are determined by setting the IPL Load Unit switches on the system console to the desired address.
2. Depressing the IPL Key on the system Console, causes a complete system reset including all 2841 registers.
3. At the completion of the reset operation, the IPL hardware initiates a Start I/O command and forms the initial CCW which is a Read command (00000010) with the Command Chain bit On.
4. Execution of the Read command causes the selected access mechanism to move to track zero (cylinder zero, head zero). A search for Index Point is initiated.
5. When Index Point is sensed, the micro program causes Home Address and R0 to be skipped over and the data portion of record 1 to be read into core memory. This data is a PSW and two CCW's. The two CCW's that are read into core memory are used to control the progress of the read-in procedure.

3.3.5 File Protection

- Logical file areas are protected from inadvertent change by the use of Set File Mask commands.

File protection is accomplished by the logic circuits in the 2841 Storage Control and the checks within the Control Programs serving the system.

The 2841 portion of the File Protection function utilizes Set File Mask commands and its associated controls.

The Set File Mask command is a Control Command whose bit structure is 000 11111. Execution of a Set File Mask command causes one byte of data to be transferred from the Channel to the 2841. At the completion of the transfer, a Channel End and Device End signal are generated. The byte of data that is sent to the 2841 describes the Write and Seek functions that can be performed.

The significance of the File Mask Bits is:

B0 B1

- | | | |
|---|---|--|
| 0 | 0 | Inhibit Write Home Address and Write R0 |
| 0 | 1 | Inhibit <u>all</u> Write Commands |
| 1 | 0 | Inhibit Write Home Address — Inhibit Write R0 — Inhibit Write Count, Key, and Data |
| 1 | 1 | Permit <u>all</u> Write Commands |

B3 B4

- | | | |
|---|---|--------------------------------------|
| 0 | 0 | Permit all Seek and Restore Commands |
| 0 | 1 | Permit Seek CCHH & Seek HH CCW's |
| 1 | 0 | Permit Seek HH CCW |
| 1 | 1 | Inhibit <u>All</u> Seek Commands |

B2 B5 B6 B7

- | | | | |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
|---|---|---|---|

NOTE: For the 2841 Storage Control, B2, B5, B6, and B7 of the mask must be zero. If these bits are not zero, the mask is considered to be invalid and a Unit Check signal is generated. When a subsequent Sense command is executed, a Command Reject is signalled.

A Set File Mask command can be issued any place within a CCW chain. At the completion of the CCW chain the File Mask is reset to all zeroes. A Set File Mask command can only be issued once within any given CCW chain. If an attempt is made to issue more than one Set File Mask command with a given CCW chain, a Unit Check signal is generated in the Status Byte. A subsequent Sense command will signal Command Reject and Invalid Sequence.

If a Write Command is issued that violates the File Mask set, the Write Command is not executed, and a Unit Check signal is generated in the Status Byte. A subsequent Sense Command signals Command Reject and File Protect.

If a Seek command is issued that violates the File Mask set, the Seek command is not executed, and a Unit Check signal is generated in the Status Byte. A subsequent Sense command signals File Protect.

A system reset or selective reset causes the File Mask to be set to all zero's.

3.4 COMMAND FLOW CHARTS (Figures 3-1 thru 3-20)

Included in this section are 2841 command flow charts. These charts present, in a logical fashion, the sequence which the 2841 goes through for a

particular Op Code. Basic error checks are included. All Op Codes are not included, however, it should be realized that some commands differ only slightly, i.e., a Search Key Equal and a Search Key High command differ only in the area where the actual comparison occurs.

These charts are at a higher level than the individual microblocks on the CLD's.

To locate a routine in the CLD's refer to the Maintenance Diagram flow charts in the ALD's.

3.5 CONDENSED MICRO PROGRAM LOGIC (Figure 3-21)

The purpose of this section is to give the overall organization of the micro program. A functional description of each section of the program is included.

Register usage and bit coding is given on CLD pages QA008 and QA009. Status register and OP register bit usages are given on the CLD pages on entry to a section of the micro program.

The micro program is printed on the CLD's in full feature form. To follow the CLD's you must use the blocks that are in the machine depending on the features installed. (Refer to Microblock Symbology, line 7 for Replaceable Word Code assignments.)

At times you will need to refer to the TROS bit assignment chart (Figure 2-45), Figures 2-3 and 2-4, and the CLD's to follow the flow.

3.5.1 General (Figure 3-21)

The operational microprogram is divided logically into five general sections and several sub-sections within each section. These sections are:

1. Select the 2841
 - a. Initial Selection
 - 1) Channel Initiated (Start or Test I-O)
 - 2) Polling Interrupt (2841 initiated)
 - b. Chained Reselection (command word chaining)
2. Command Decode
3. Initial Status Presentation
 - a. Write Immediate
 - b. Not Write Immediate
4. Command Execution
 - a. Load Counts
 - b. Control Commands
 - c. Read and Clocking Commands
 - d. Write Commands
 - e. Search/Scan Commands
 - f. Gap Spacing Routine
 - g. Burst Byte and Exit Decisions
 - h. Decode Sense Information.

5. End Procedure
 - a. Disconnect from channel
 - b. Deselect file

3.5.2 Initial Selection

After a power on reset or at the end of a chain of commands, the micro program enters the initial selection routine. The program loops, waiting for SELTO to rise. Two ways for SELTO to rise are:

1. A Start or Test I/O is given and the control unit part of the Address Out byte matches the pre-wired 2841 CU Address.
2. The 2841 raising Request in (Polling Interrupt) allows SELTO to rise when channel transmits Select Out.

SELTO up causes the 2841 to branch out of the loop to microblocks which test for type of selection. SELTO can be raised by one of the following:

- a. SELTO comes up via polling interrupt and is most likely a result of any Gated Attention from unchained SEEK commands.
- b. SELTO comes up via polling interrupt with ST (2) on, indicating some status information stacked in the 2841.
- c. If SELTO comes up via polling interrupt with ST (2) on, this indicates that the 2841 was addressed while finishing a write operation. This condition indicates that the CU was busy when addressed and is not now busy causing **Request In** to be set by the Queued latch. The CU now will transmit a CU End Status byte.
- d. SELTO was raised from channel by a Start or Test I/O command.
- e. In this case outstanding status is also held in the 2841.

The following items are accomplished in the initial selection routine:

1. Operational In raised.
2. Poll Enabled and Queued latches reset.
3. The File Mask information is reset.
4. The device part of the Address Out byte is converted from 3-bit channel coding to one of eight bit mod select type coding.
5. Address In is raised.
6. The module select number is used in determining the type of device selected. This is accomplished by two CE punched ROS words. It is necessary for the 2841 to know the device type

since there are slight differences in the micro programming for each type.

7. The device type interface is selected. For 2311 this is accomplished with an 1→FT statement. This selects the 2311 File Tag interface register, thereby routing the output of UR to 2311's. 2→FT or 4→FT selects the feature device File Tag register, and blocks the 2311 File Tag register. In this way, the output of UR is routed to the feature devices.
8. The interface is checked for unselected status. If there is any, the micro program posts unselected status, waits for Command Out, goes to the end procedure, transmits Unit Check to channel, and expands the error into 3 sense bytes, when a Sense Command is received.
9. Select a file by placing module select number in UR.
10. Wait for Command Out.
11. Check operable. If inoperable, expand into either Off Line, Busy, Unsafe, Seek Incomplete, or End-Of-Cylinder indication.
12. Check Gated Attention. If Gated Attention from a selected device is up on a Test I/O operation, Device End in initial status byte is set. Device End and Busy are set in the initial status byte on a Start I/O operation. For both commands Device End is cleared if channel does not stack the status byte.
13. Raise Control Tag and Head Select.
14. The micro program now exits to command decode.

3.5.3 Command Decode

Command Decode has entries from initial and chained reselection. In this section, the command is first decoded into either Control, Read, Search, Write, or Test/Sense I/O. The commands are then further decoded into IPL, HA, Count, Key, Data (or combinations of these), Control, Sense or Test I/O. Testing of the command by the File Mask is done in this section. If the command violates the mask, the program exits to End Procedure. In this section, the original command byte is destroyed and a new one formed. (Refer to QA009 for coding of the orientation data which identifies where the last command ended.)

All of these commands exit to the Initial Status Presentation routine in order to present initial status to the channel. As the micro program must have a method of entering the section of the micro program selected by the command decode after presenting status, the OP register is set with a constant to allow branching to the selected section.

In addition, one of the register is set with a code to indicate to the micro program the types of

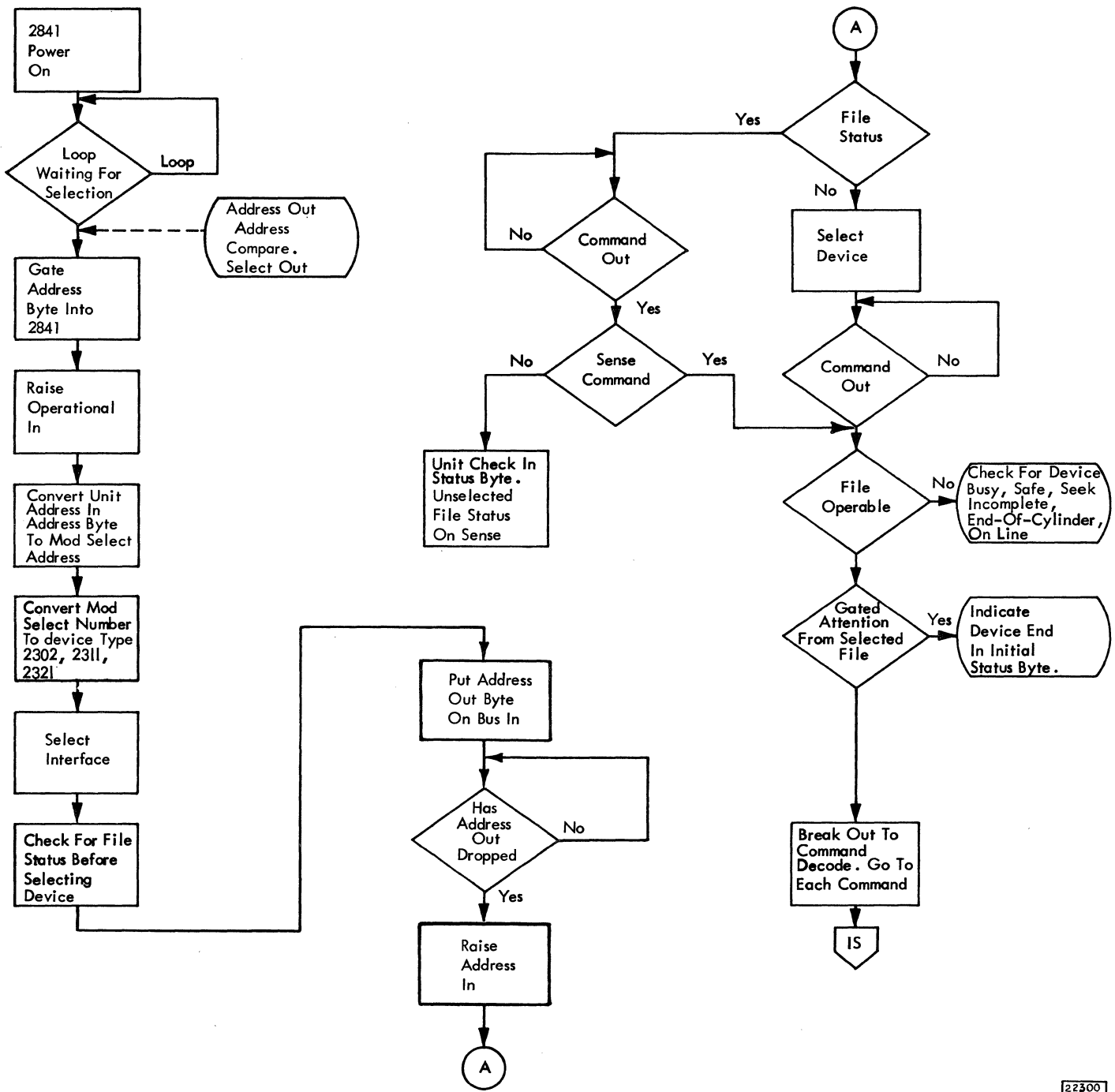


Figure 3-1. Initial Selection

22300

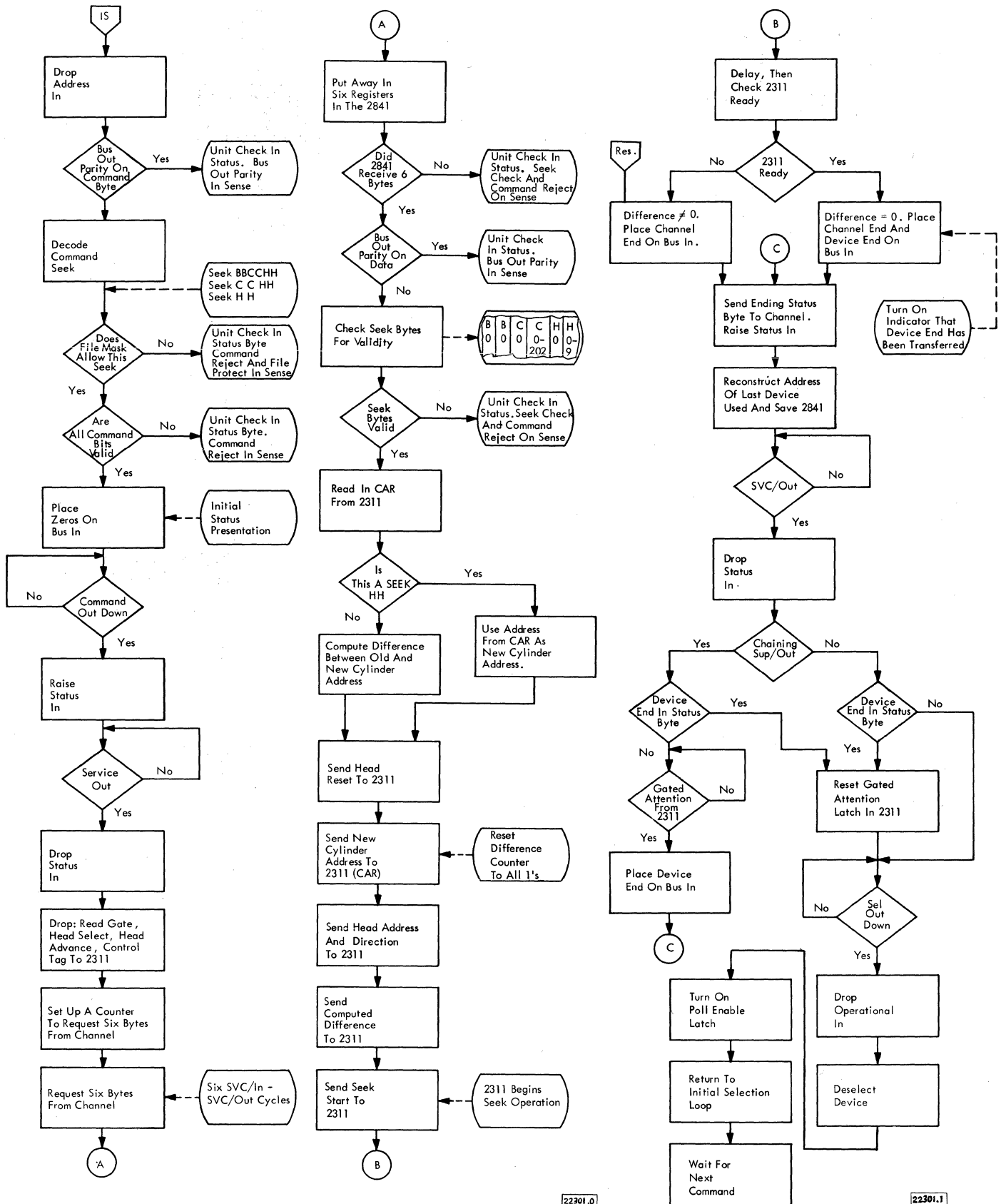


Figure 3-2. Seek for 2311

22301.0

22301.1

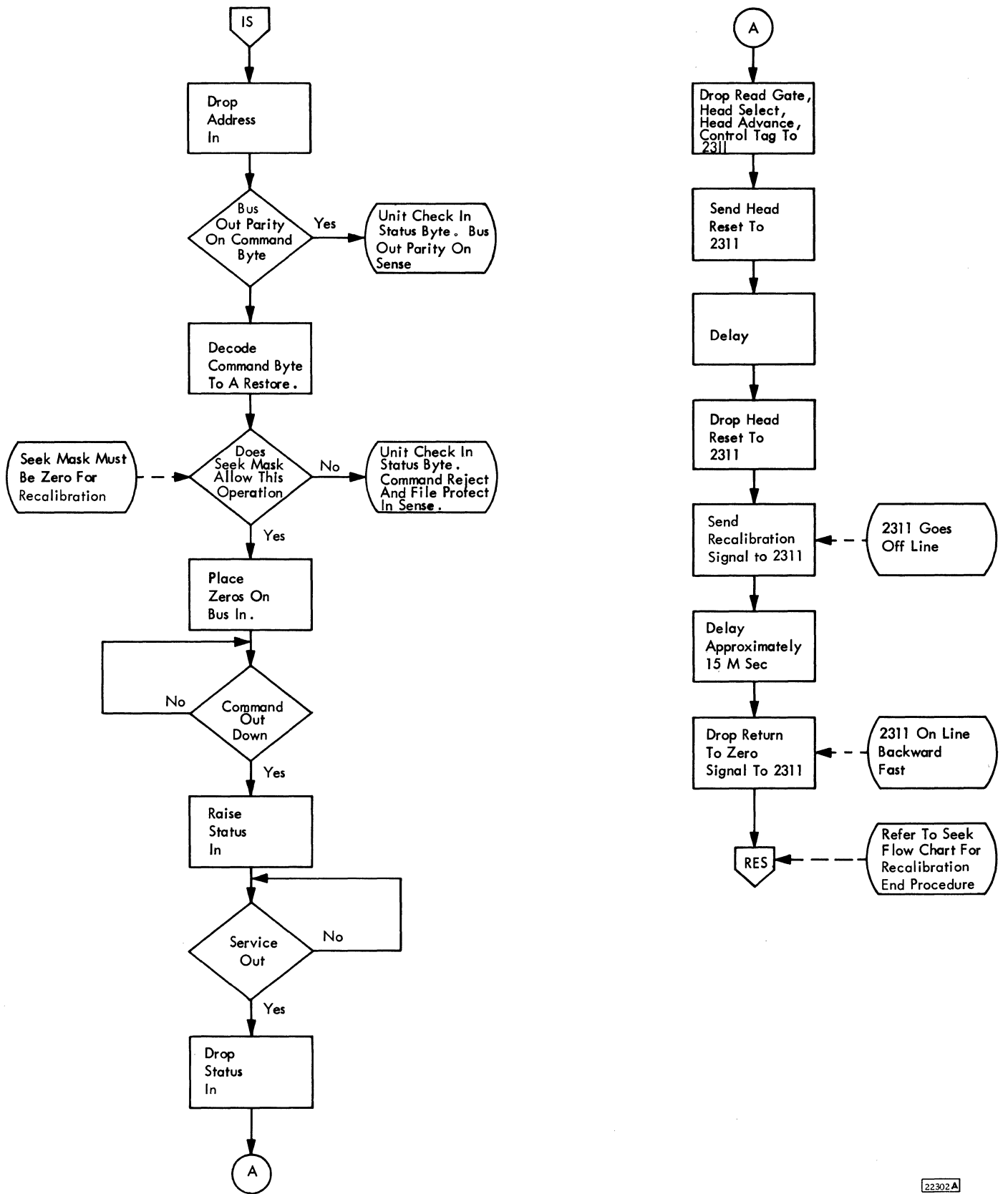
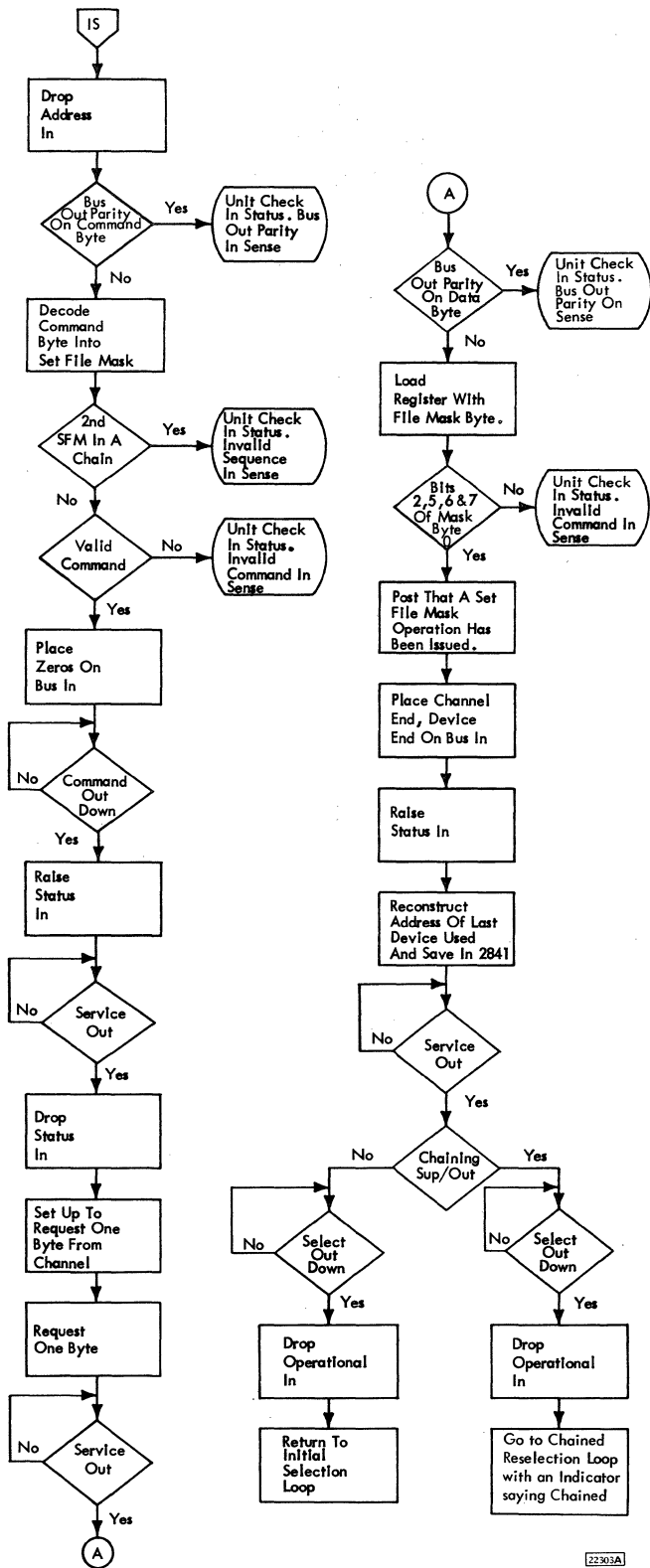


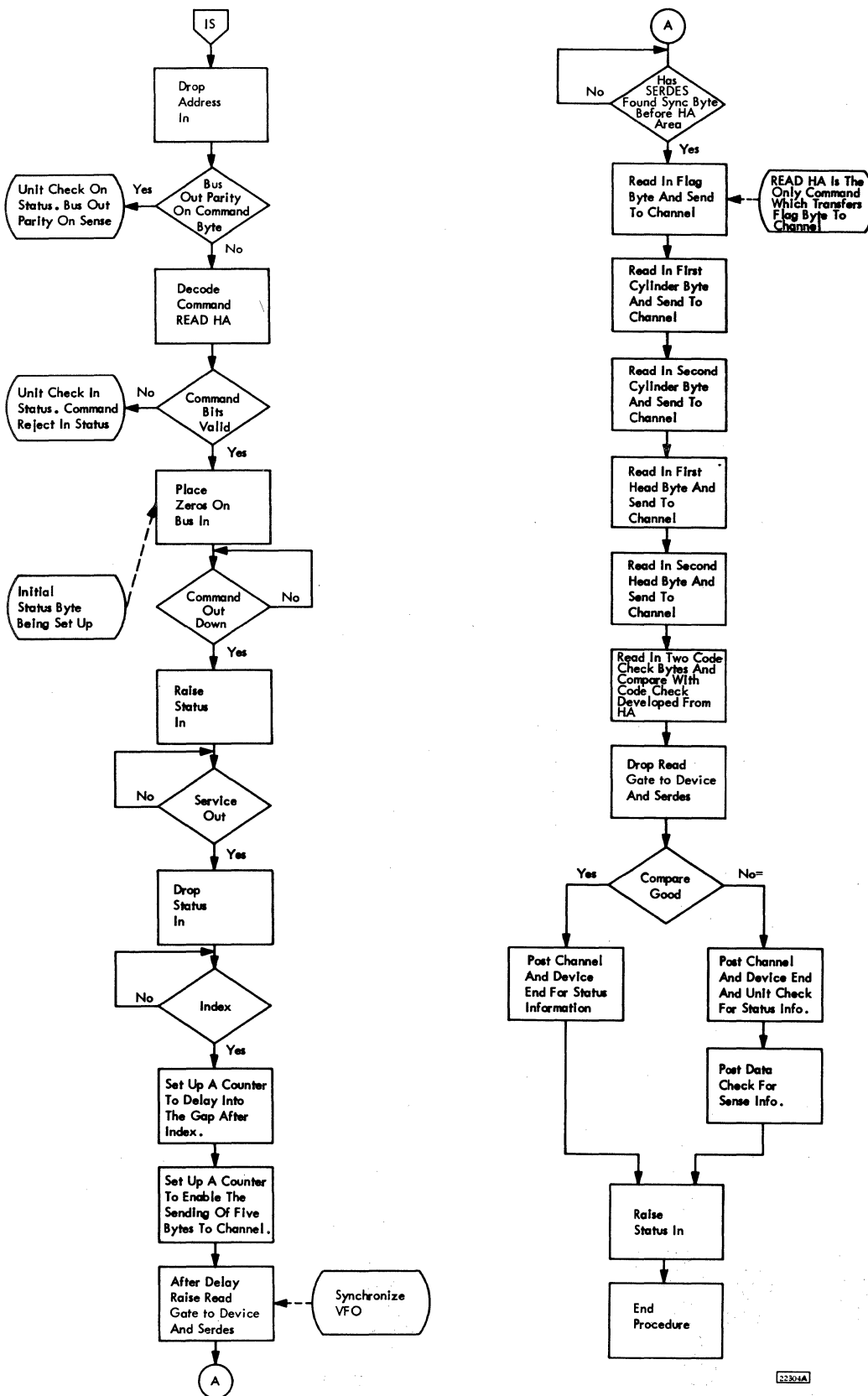
Figure 3-3. Recalibrate

22302A



22303A

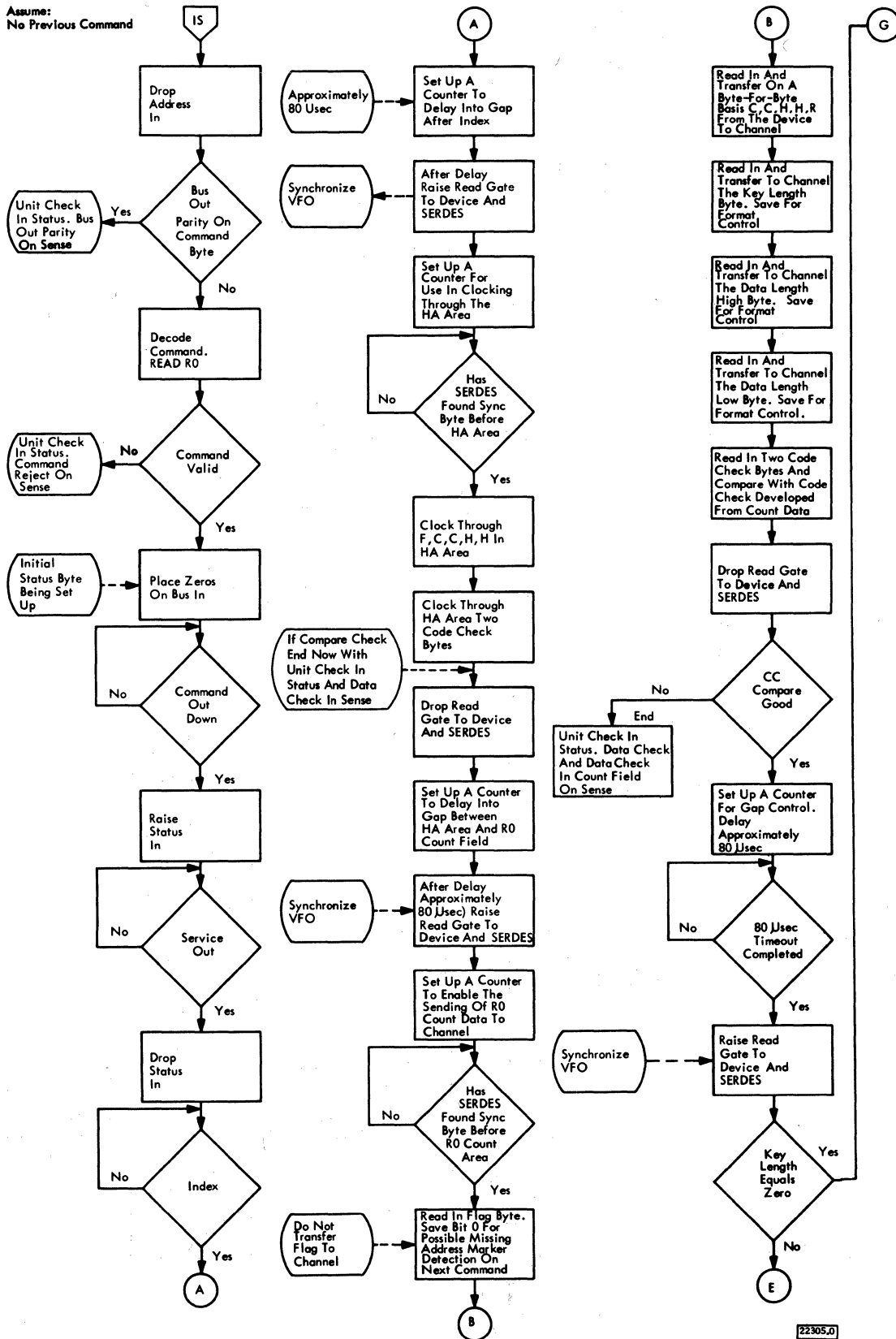
Figure 3-4. Set File Mask for 2311



22304A

Figure 3-5. Read Home Address to a 2311

Assume:
No Previous Command



22305,0

Figure 3-6. Read Record Zero to a 2311

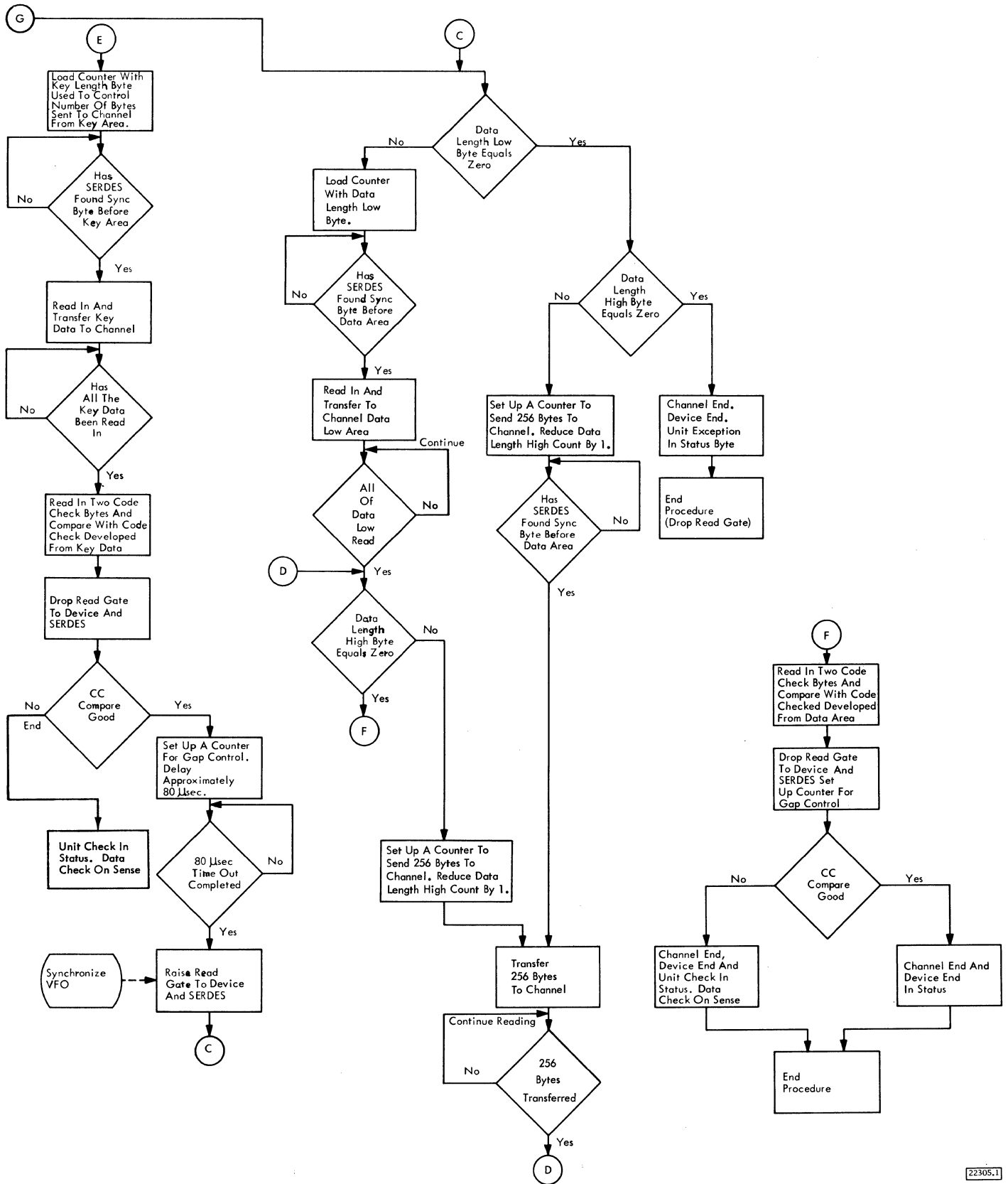


Figure 3-6. Read Record Zero to a 2311

Assume:

No Previous Commands

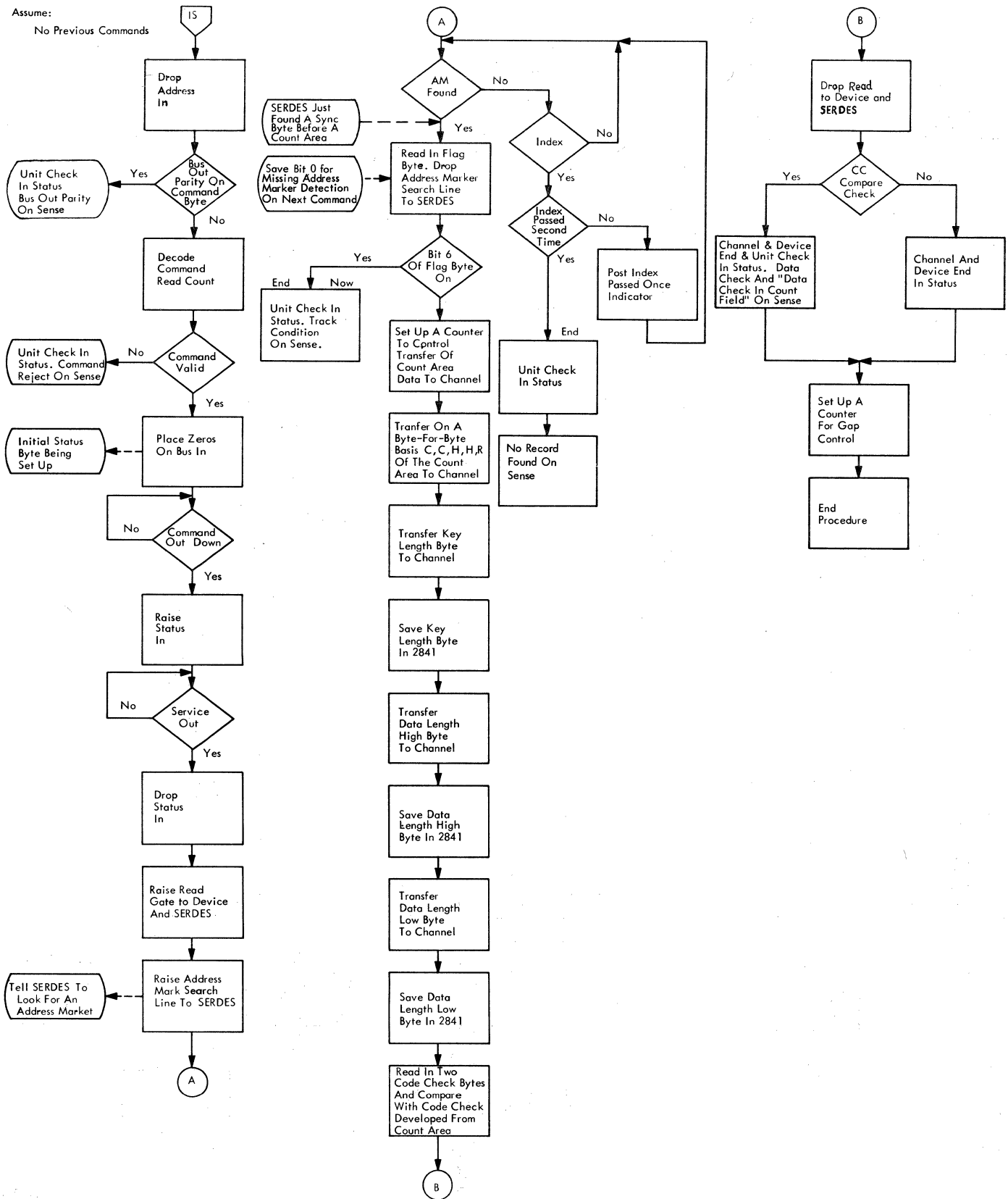
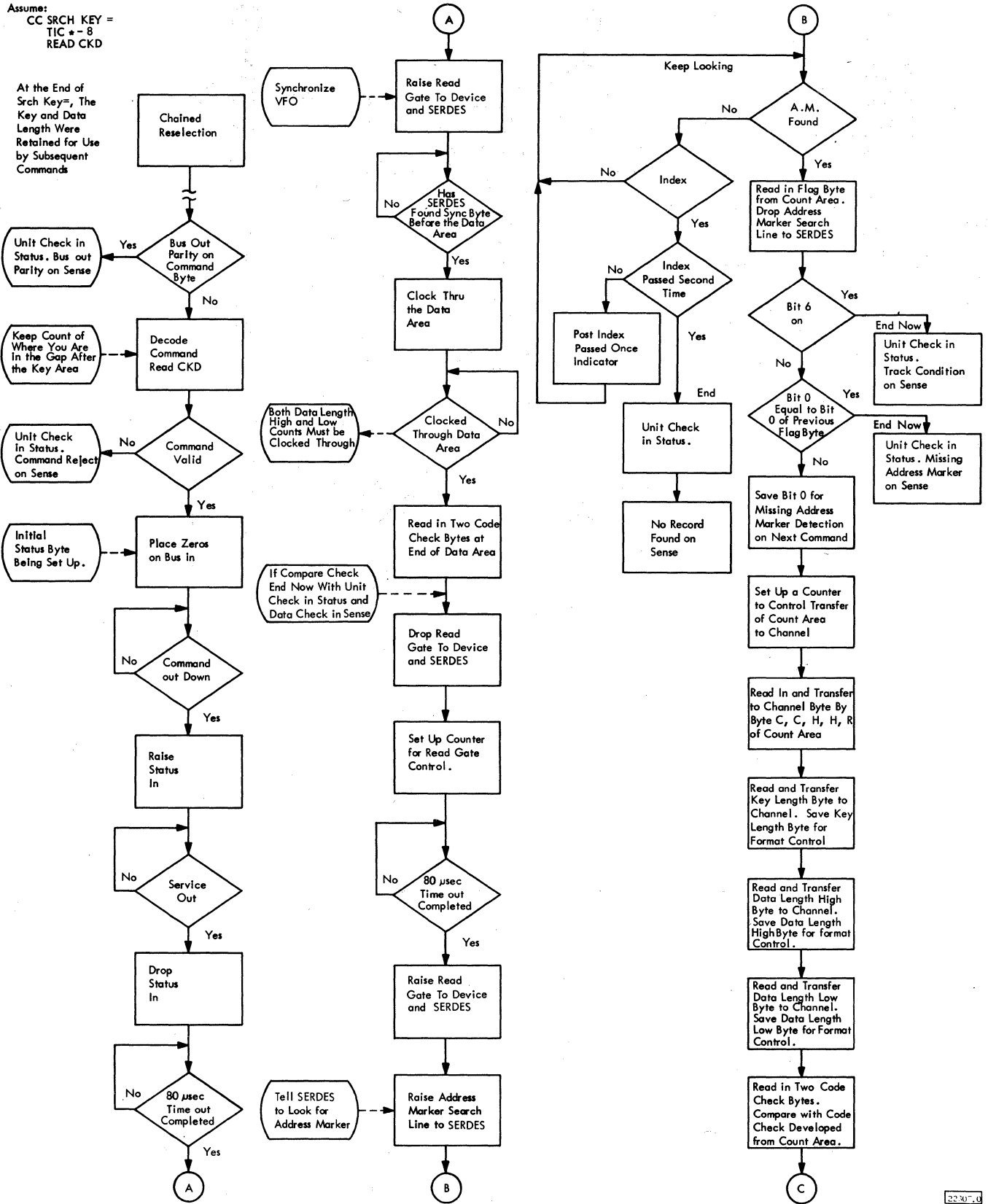


Figure 3-7. Read Count

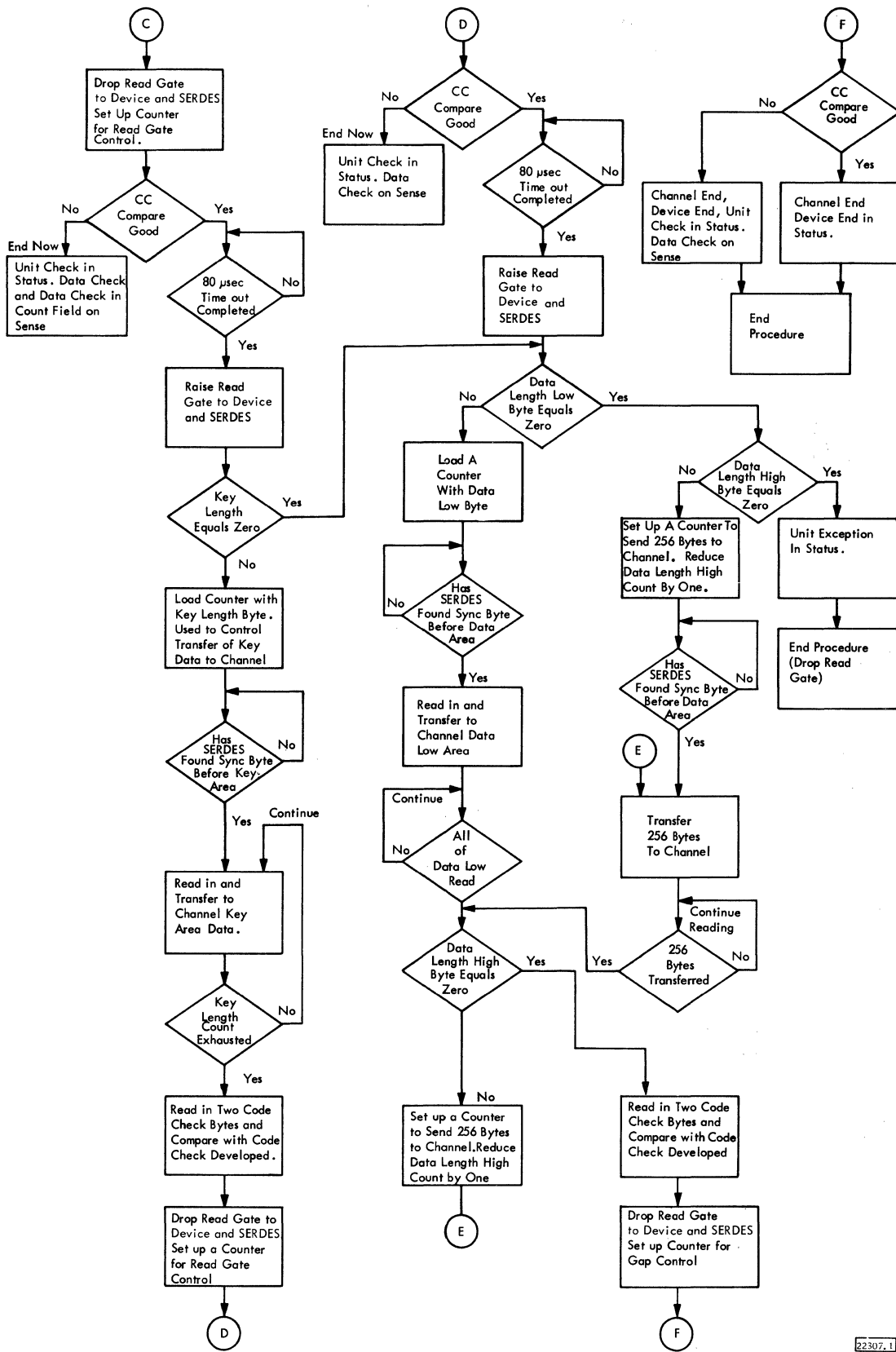
Assume:
 CC SRCH KEY =
 TIC + 8
 READ CKD

At the End of
 Srch Key=, The
 Key and Data
 Length Were
 Retained for Use
 by Subsequent
 Commands



22-307-0

Figure 3-8. Read Count - Key - Data



22307.1

Figure 3-8. Read Count - Key - Data

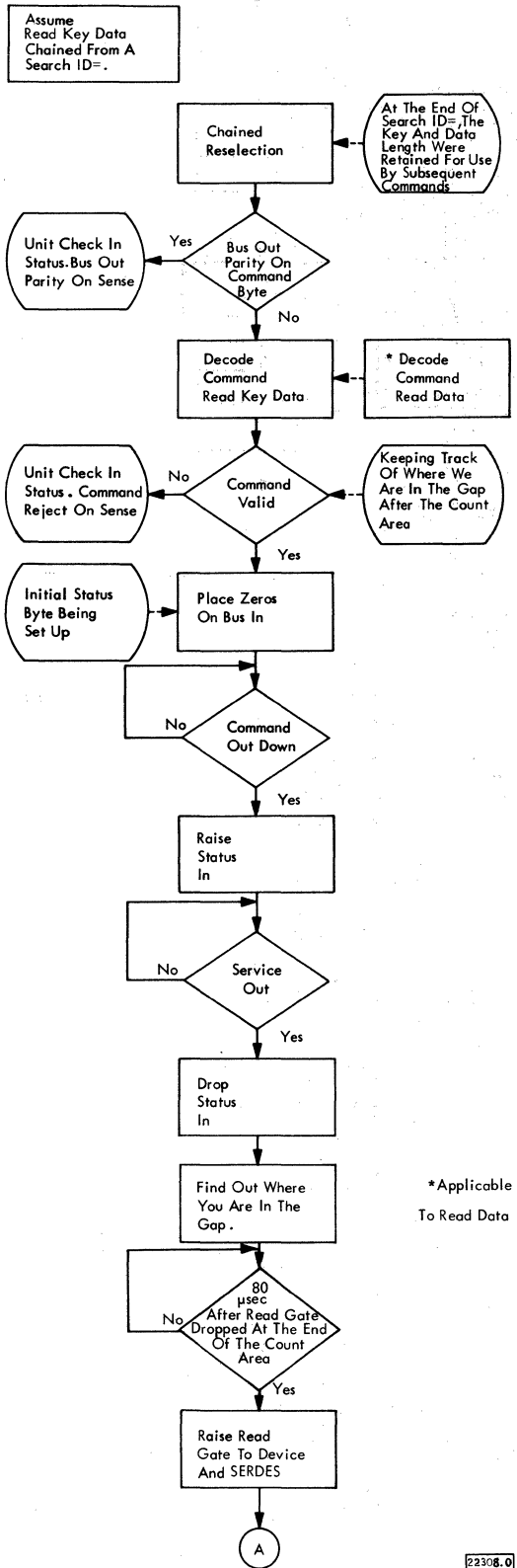


Figure 3-9. Read Data and Read Key - Data to a 2311

Program: SIO
 CC Seek CCHH
 CC SFM (To Allow
 Wrt HA) Wrt HA

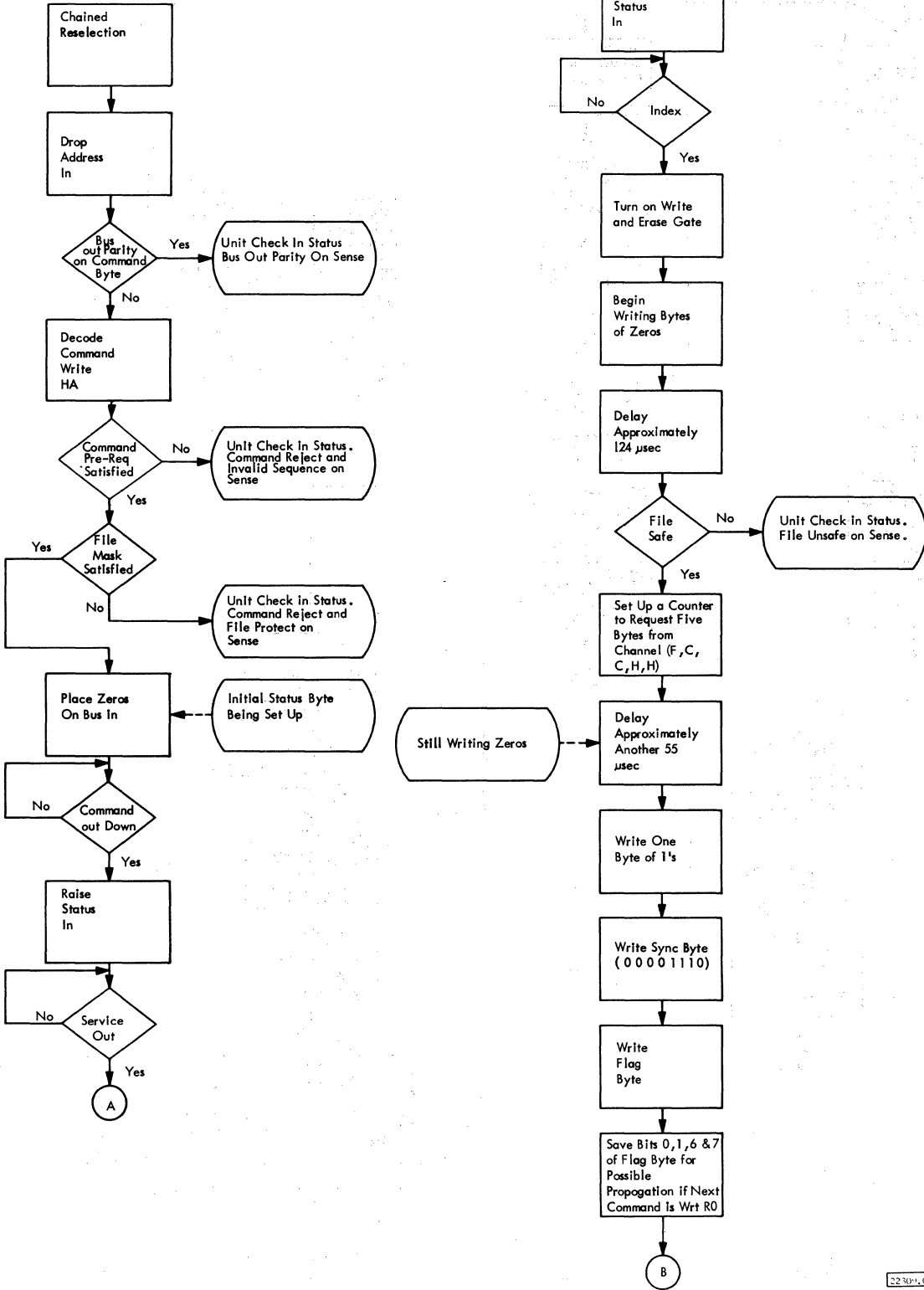
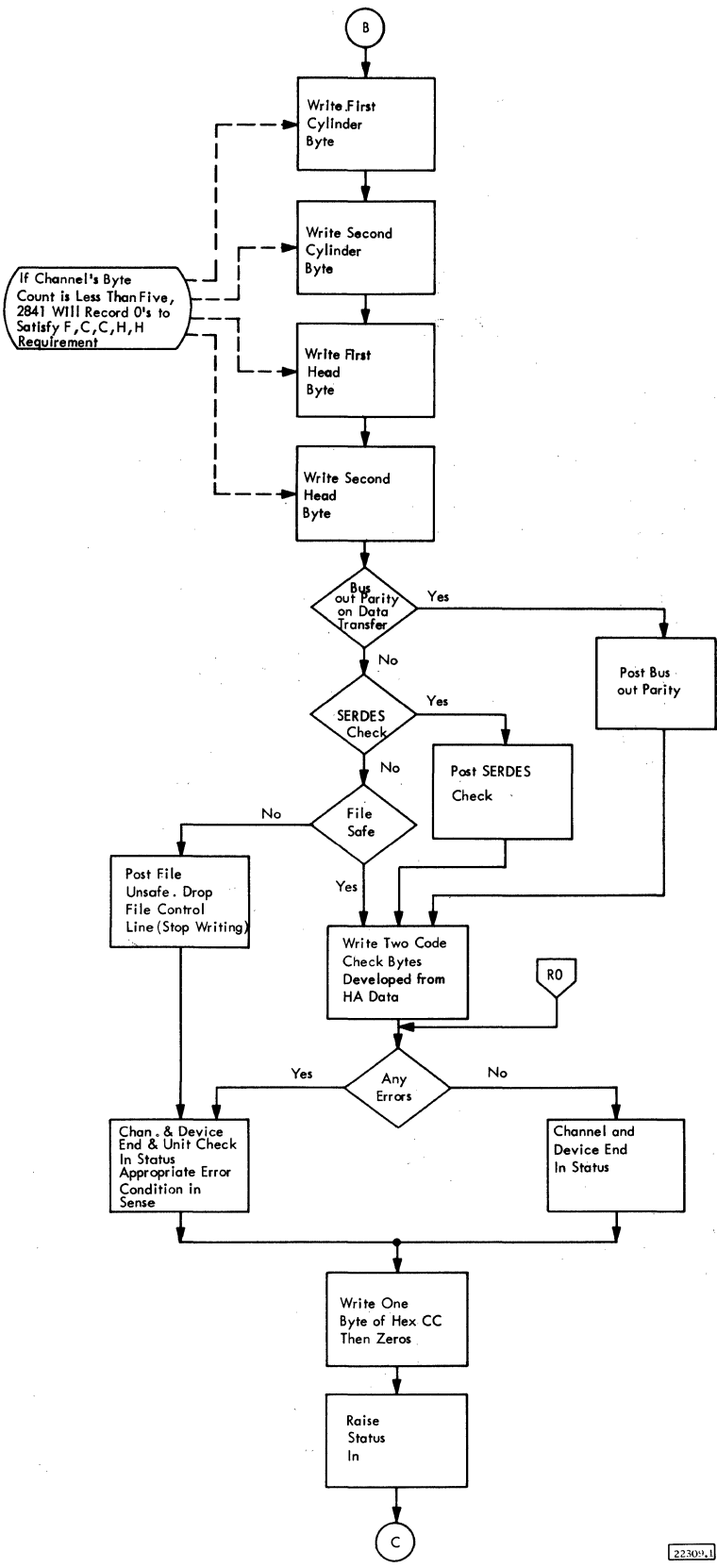


Figure 3-10. Write Home Address for 2311



22309.1

Figure 3-10. Write Home Address for 2311

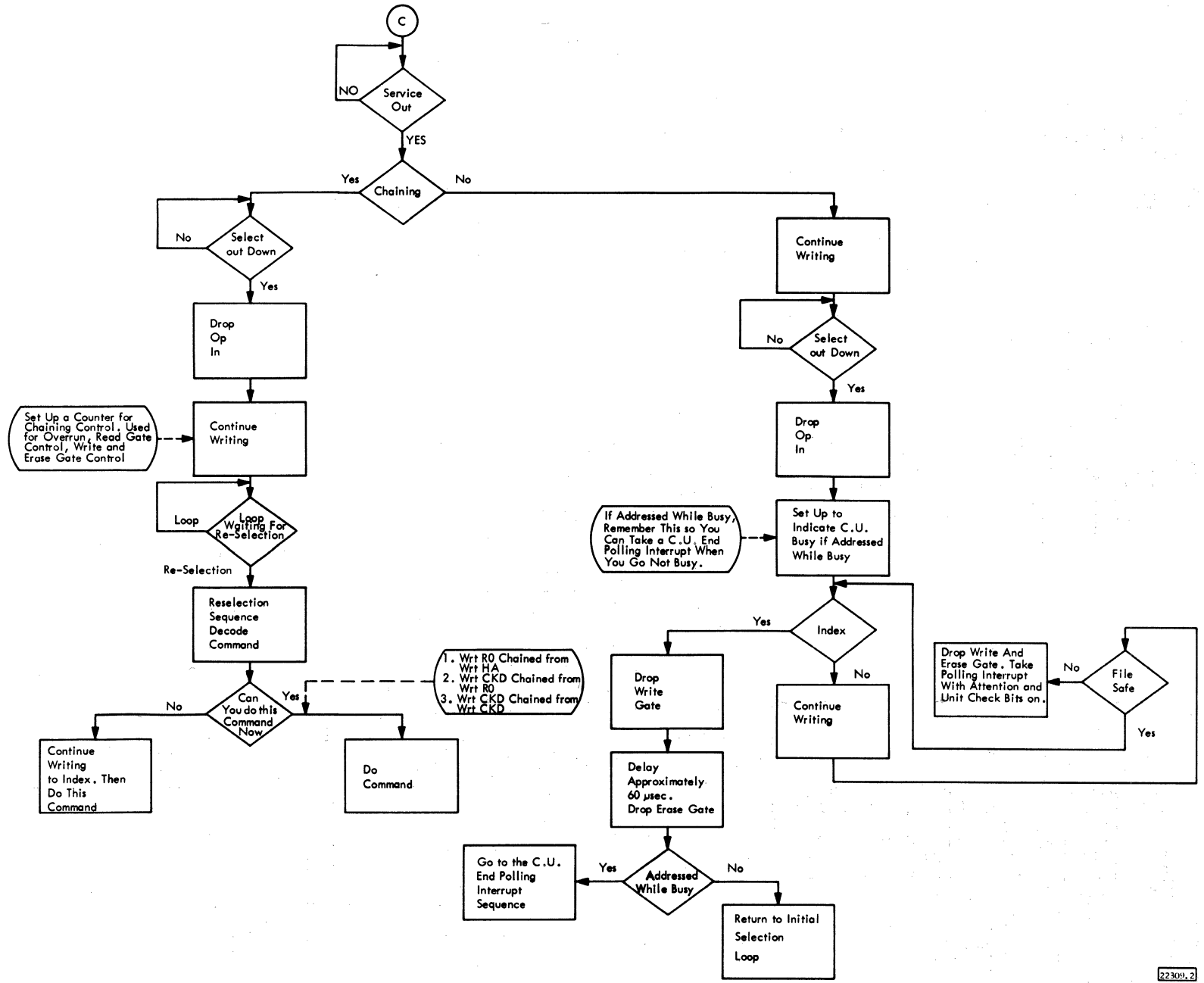


Figure 3-10. Write Home Address for 2311

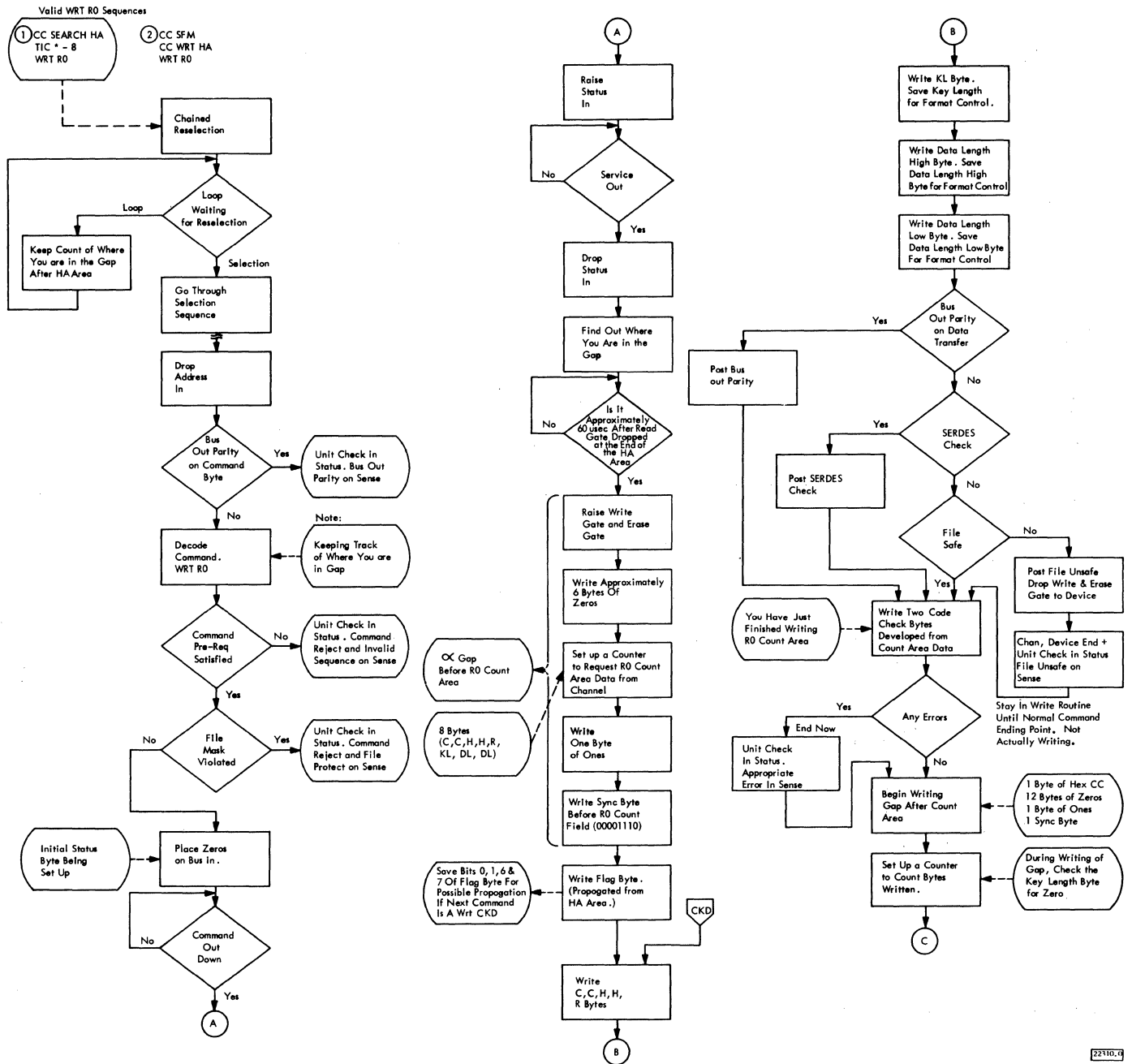


Figure 3-11. Write Record Zero for 2311

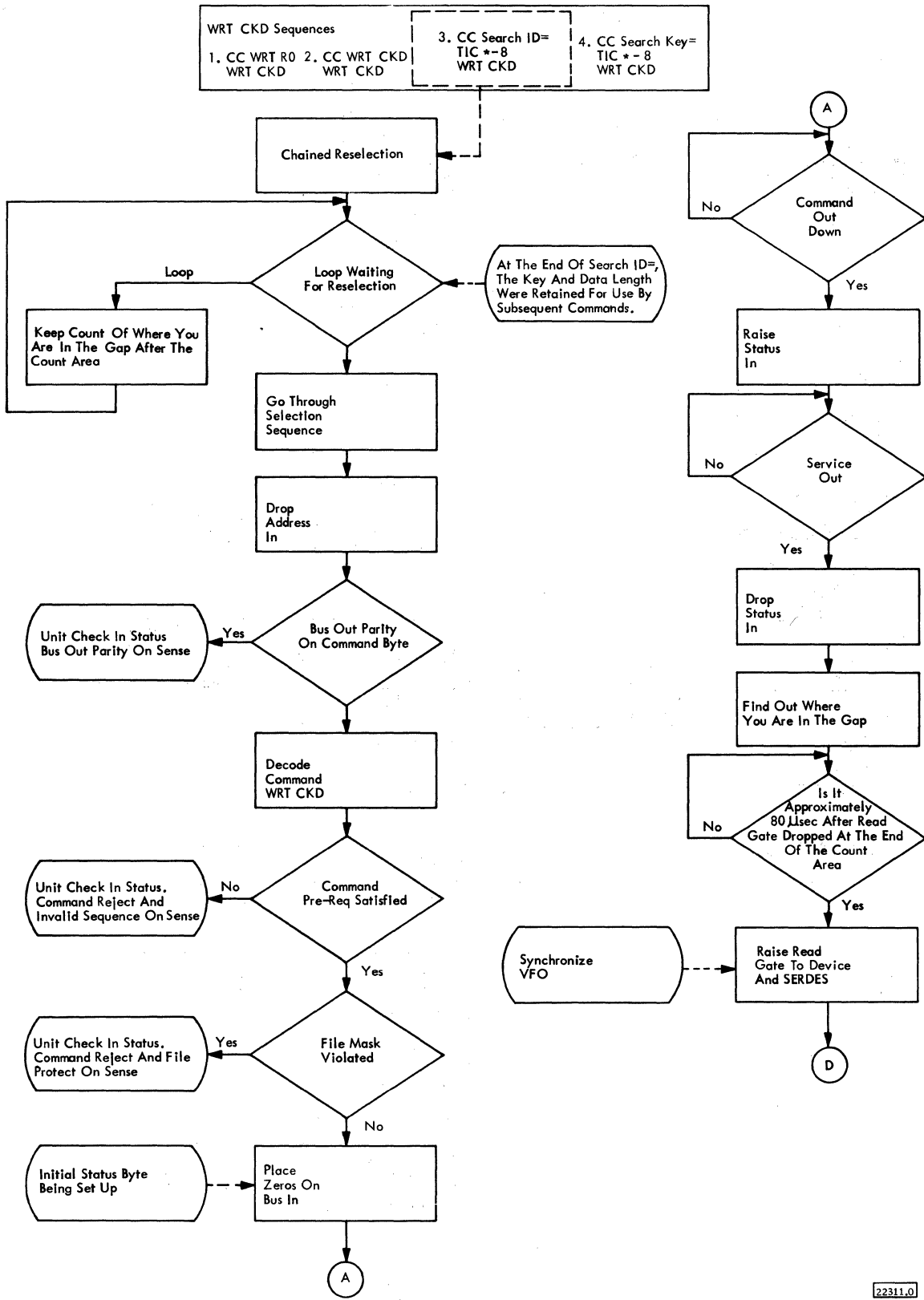


Figure 3-12. Write Count - Key - Data for 2311

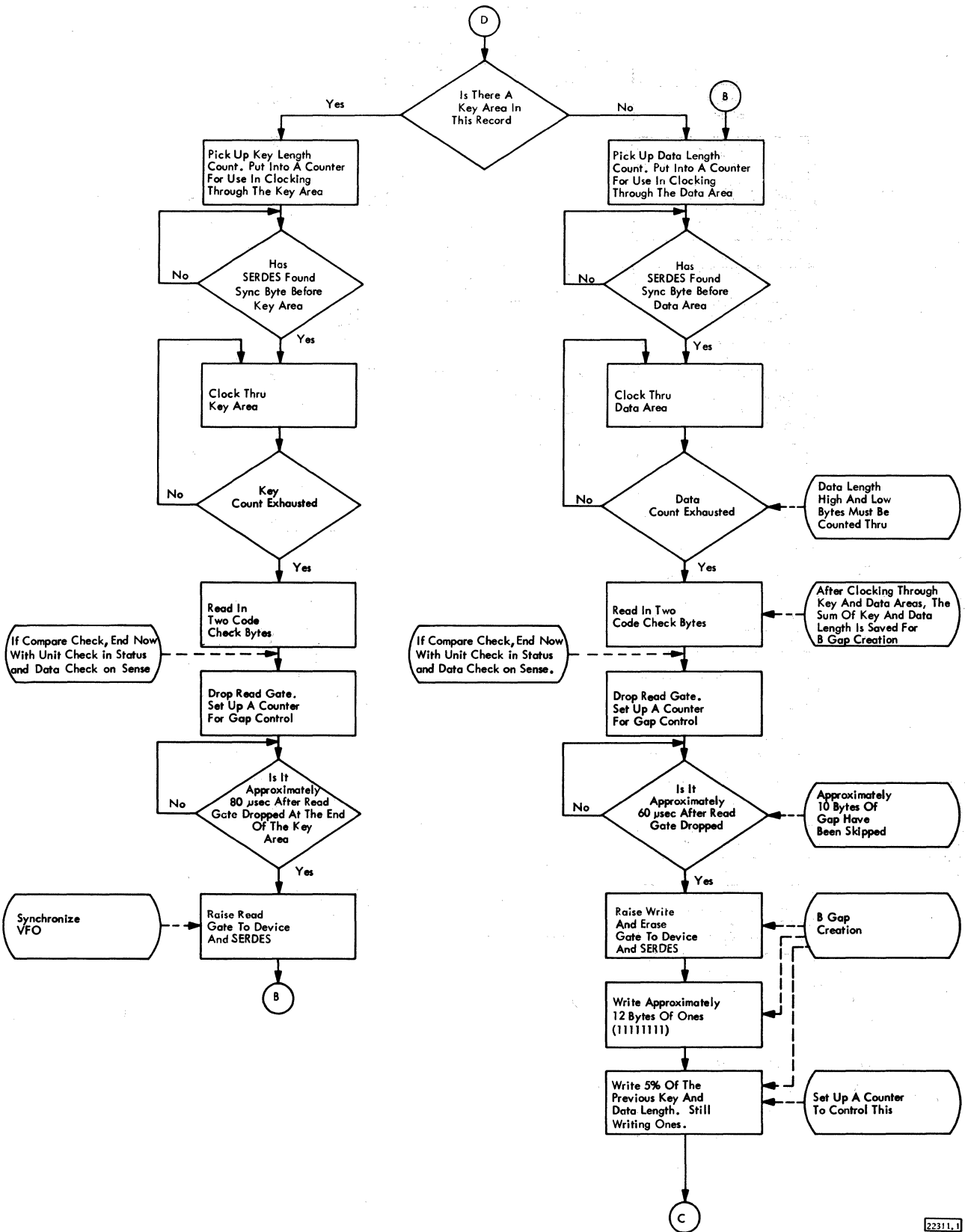


Figure 3-12. Write Count - Key - Data for 2311

2231 L 1

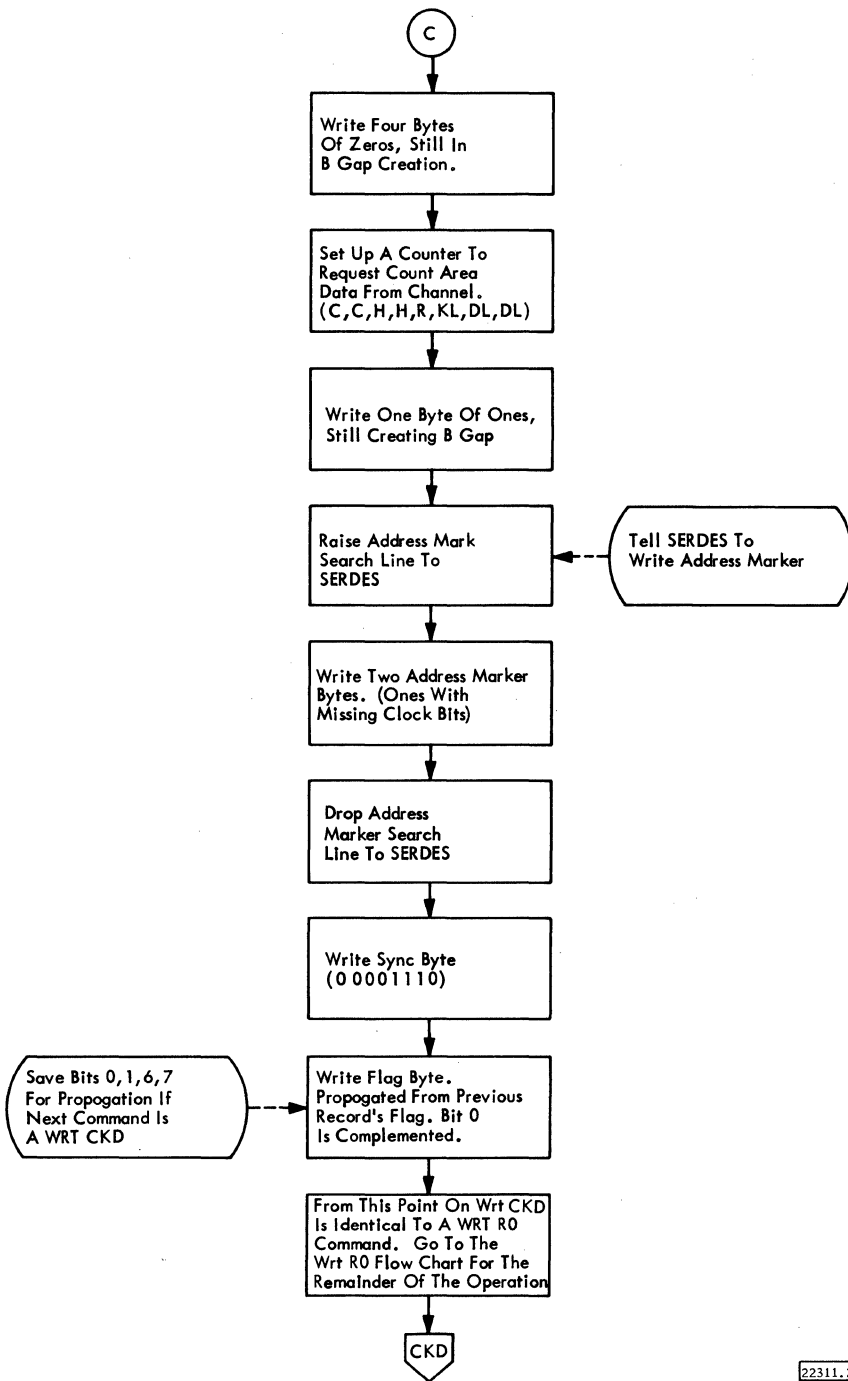


Figure 3-12. Write Count - Key - Data for 2311

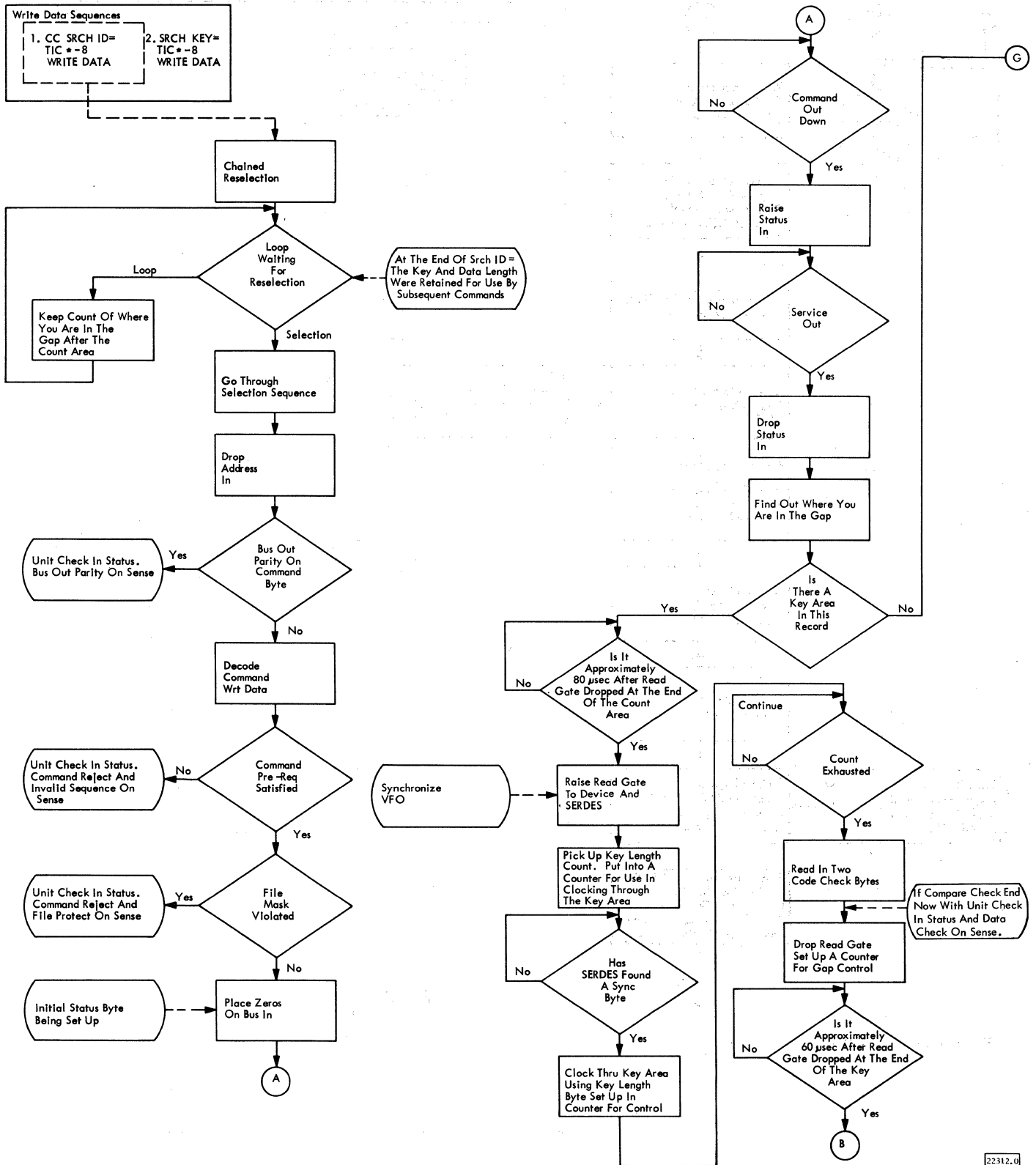
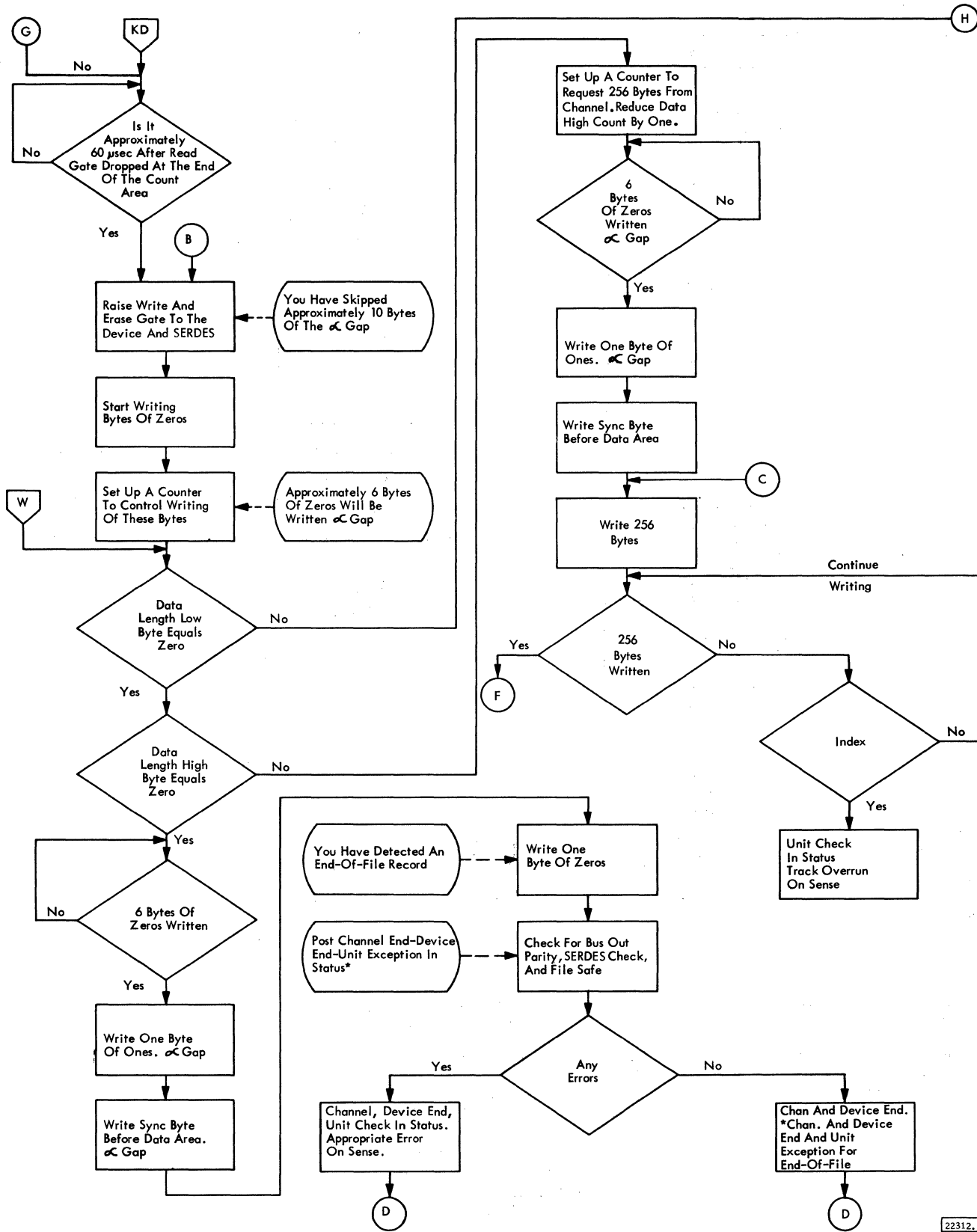
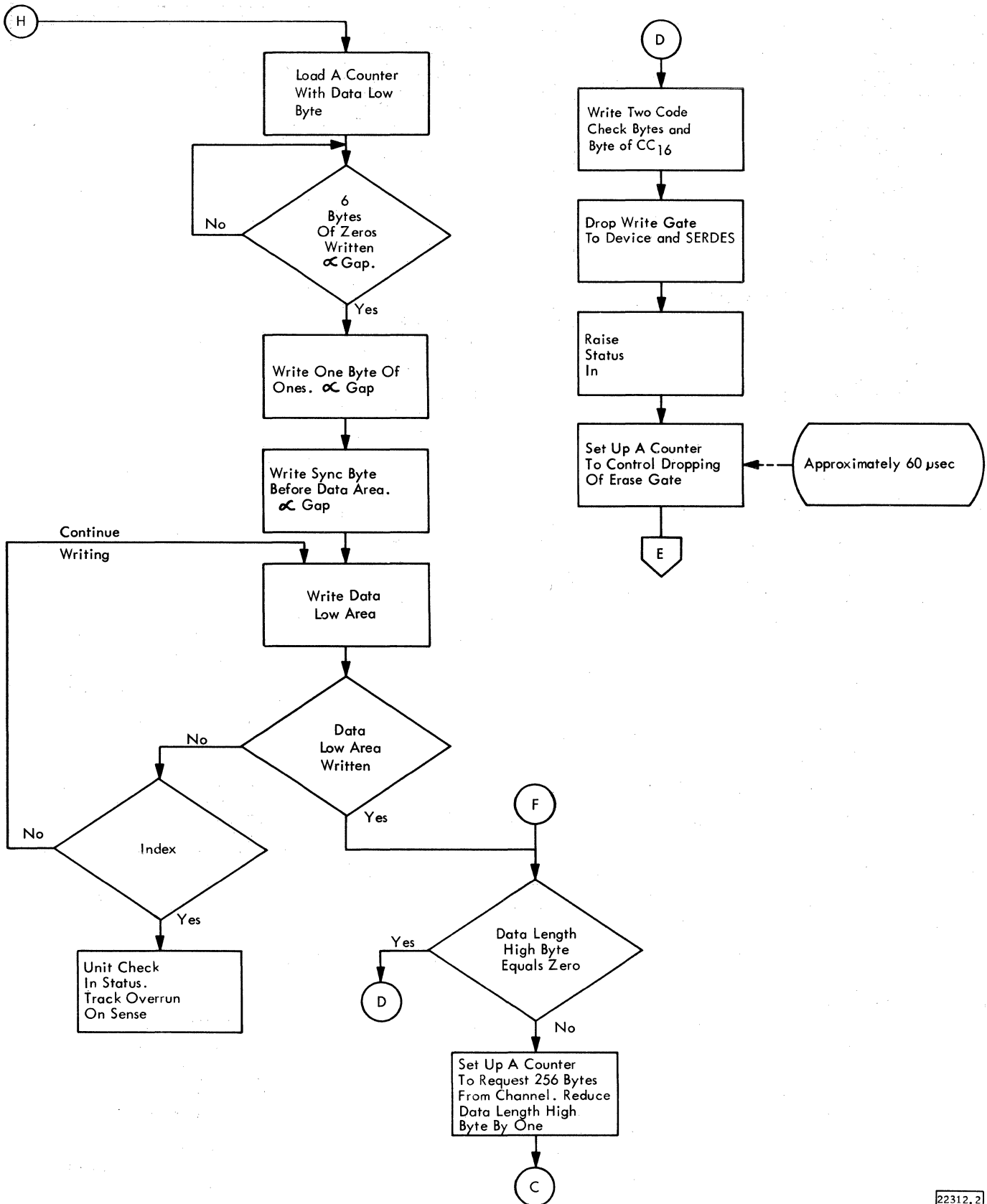


Figure 3-13. Write Data



22312.1

Figure 3-13. Write Data



22312.2

Figure 3-13. Write Data

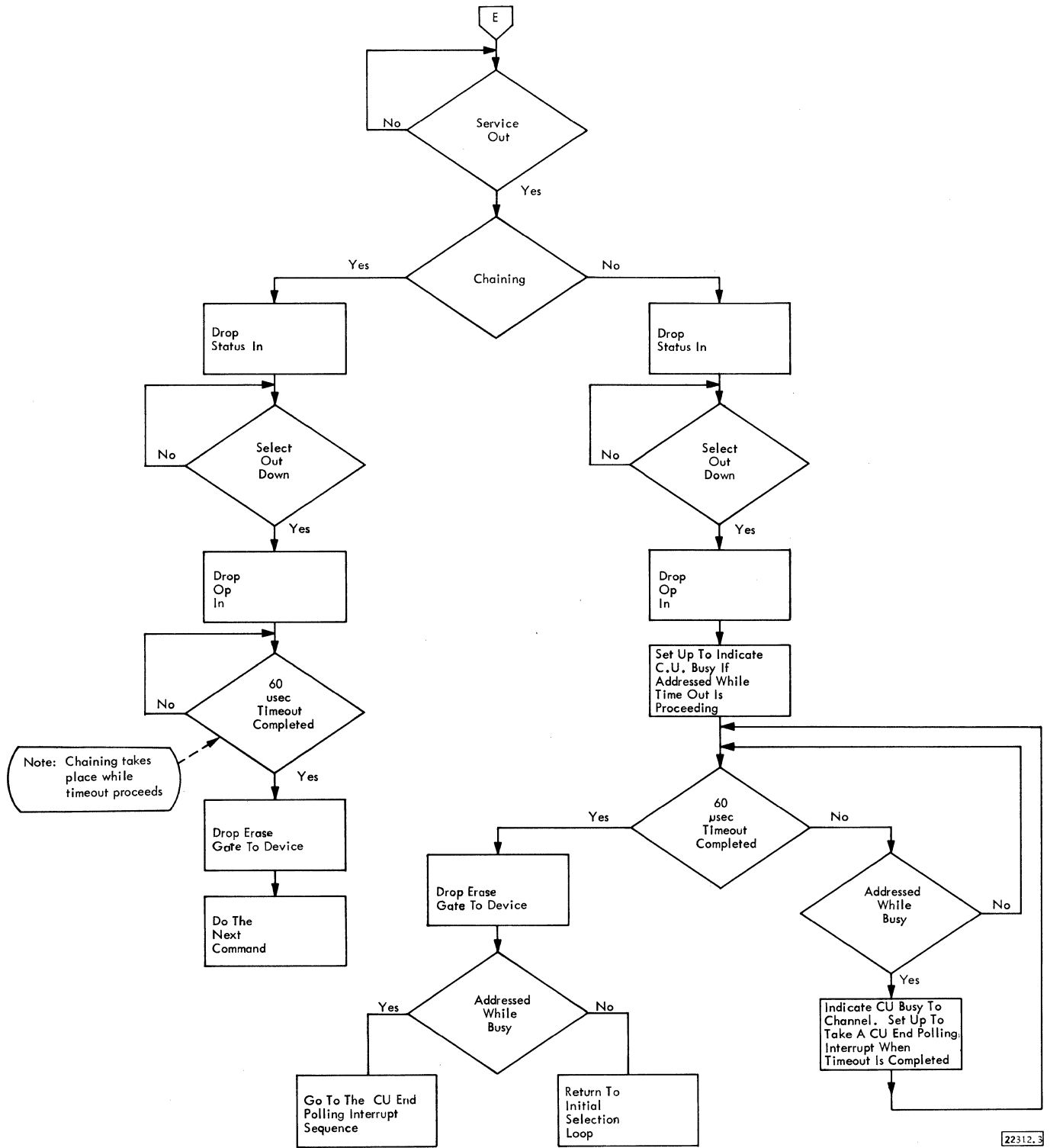


Figure 3-13. Write Data

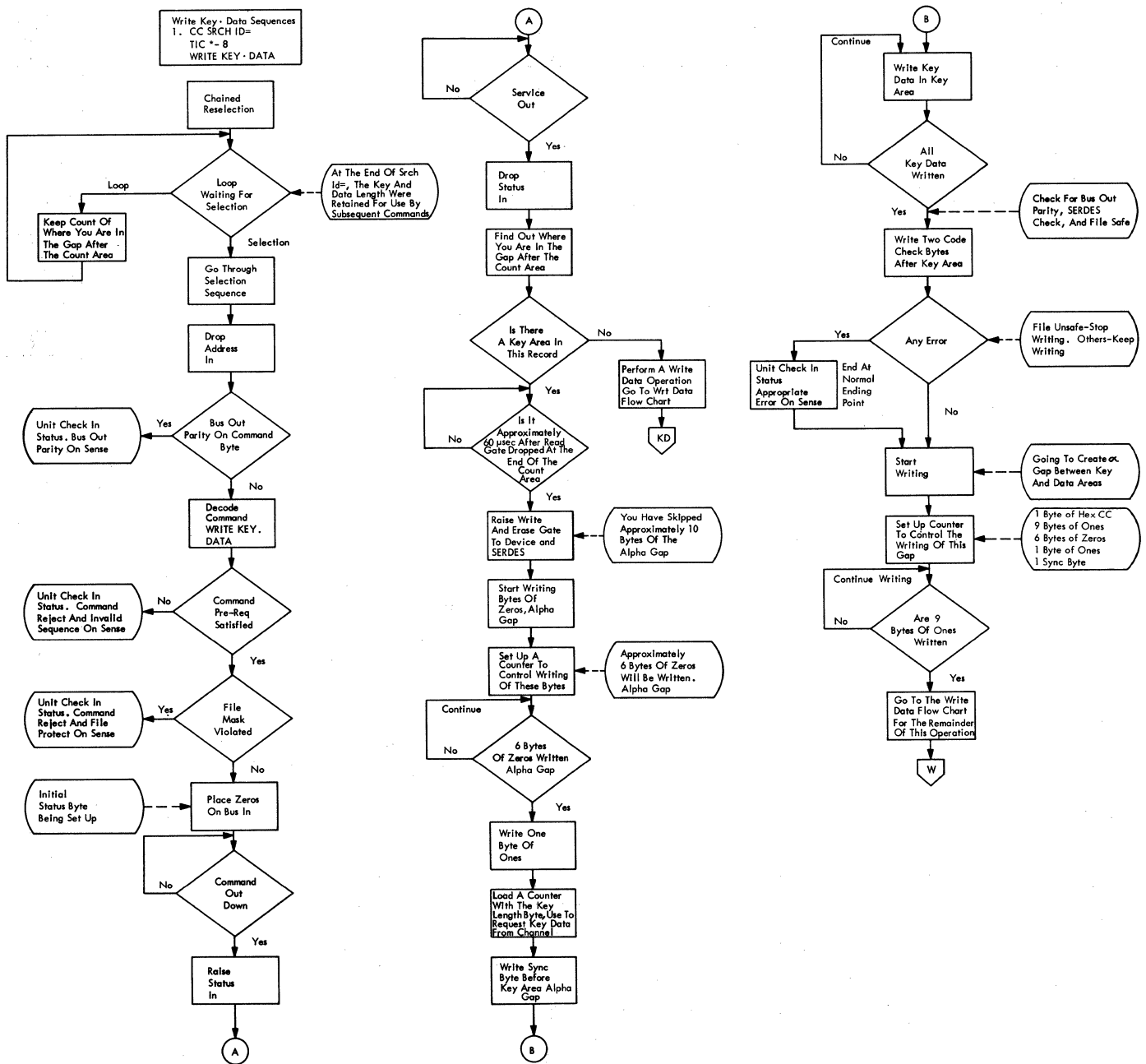


Figure 3-14. Write Key - Data

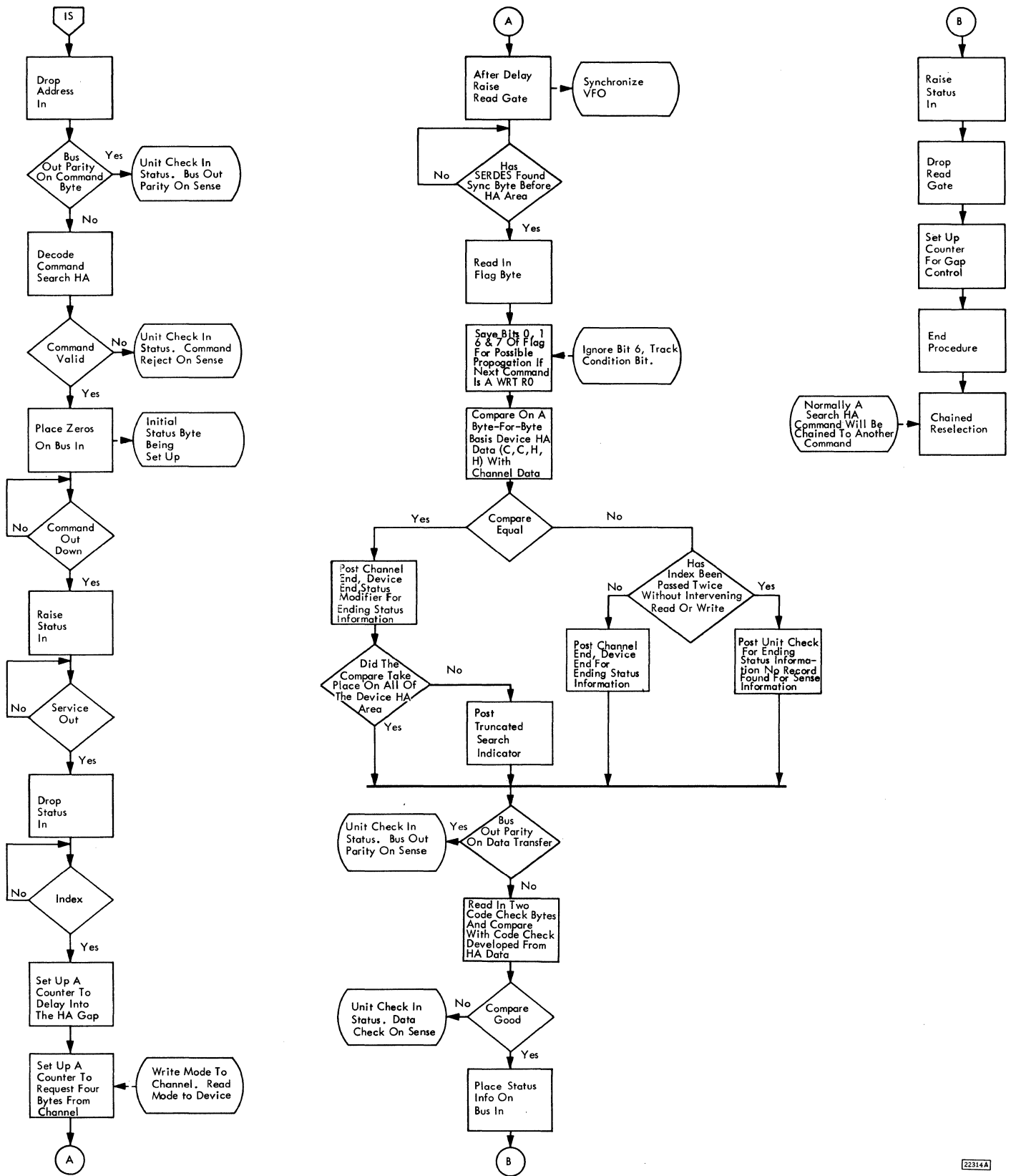
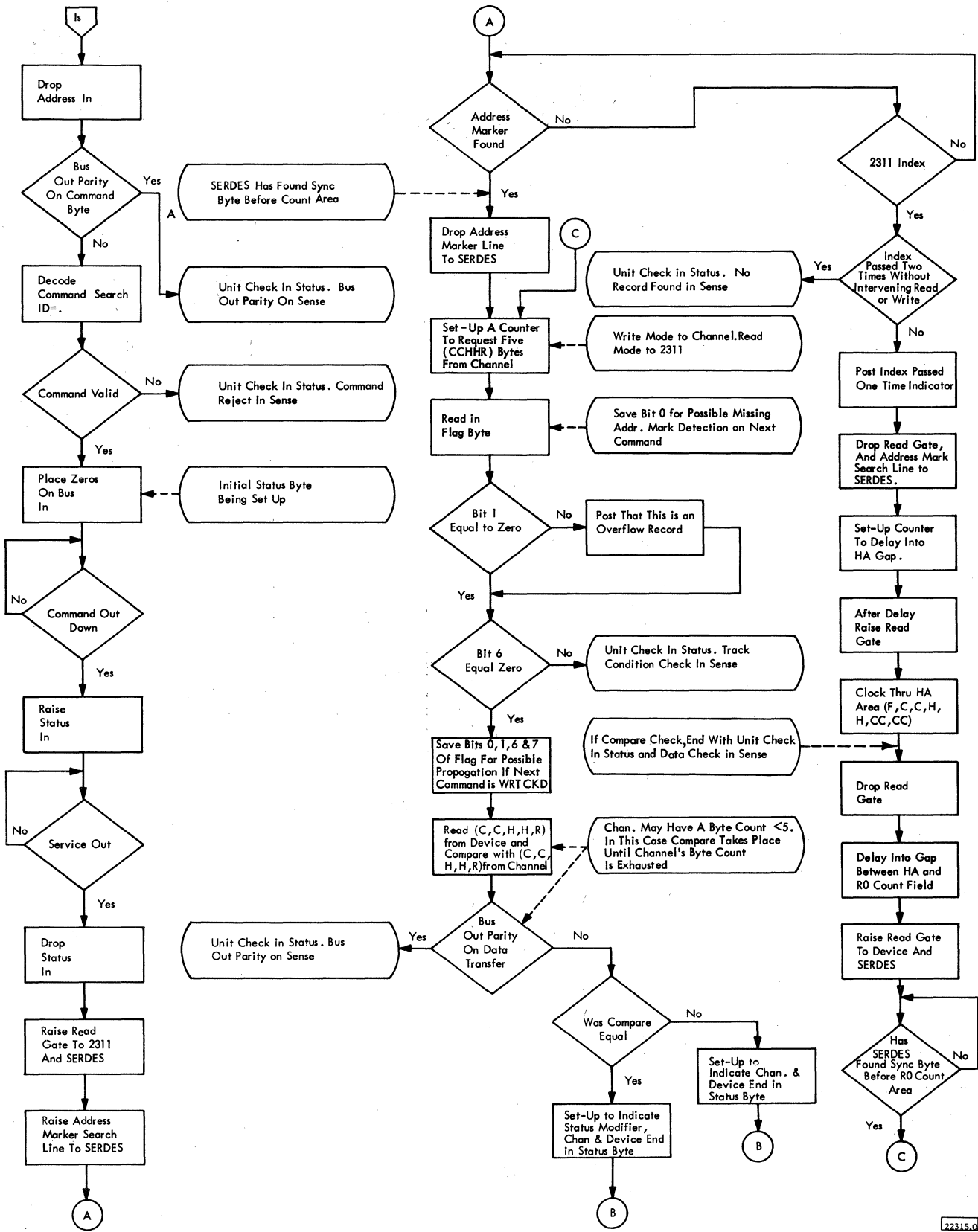


Figure 3-15. Search Home Address



22315.0

Figure 3-16. Search ID Equal

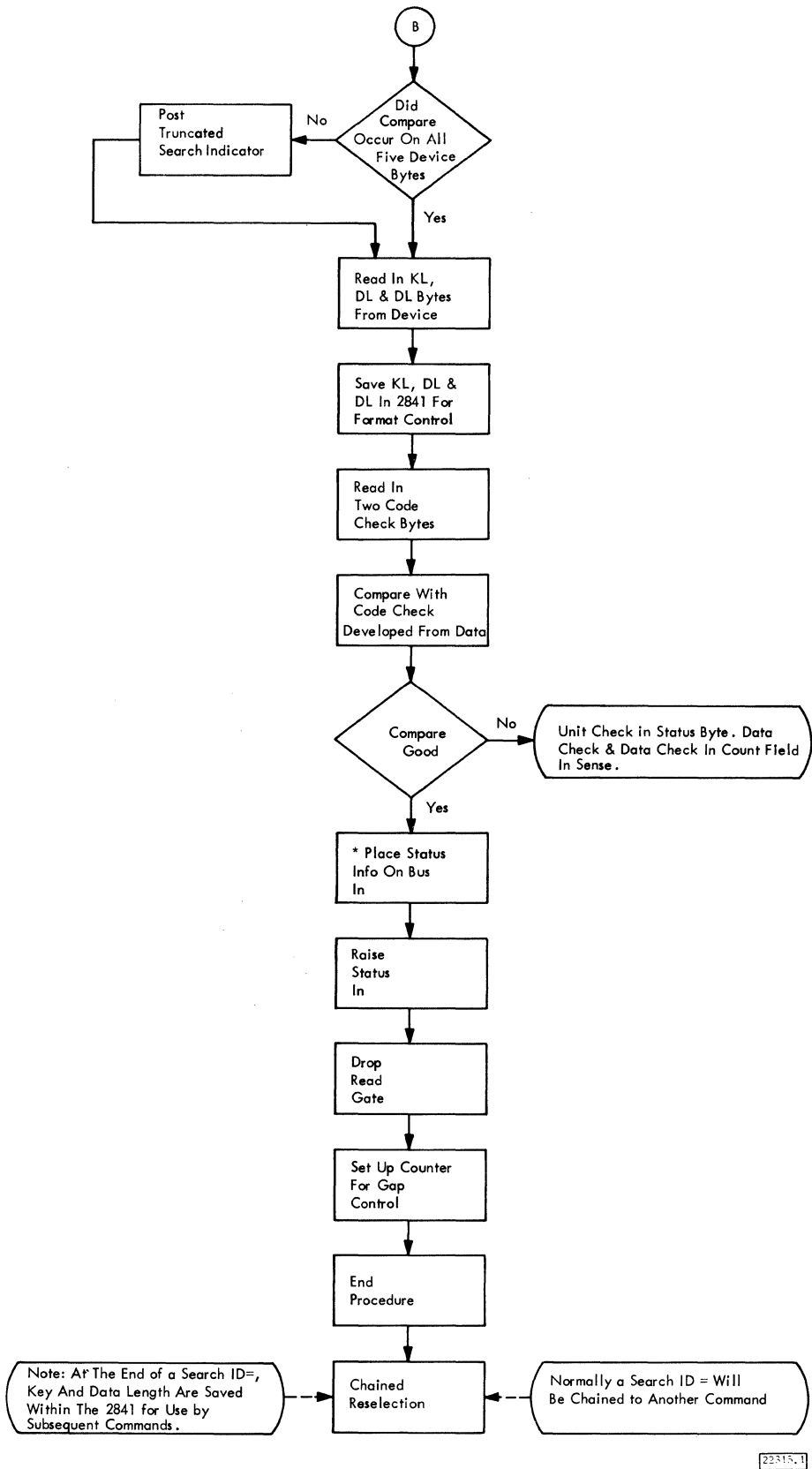


Figure 3-16. Search ID Equal

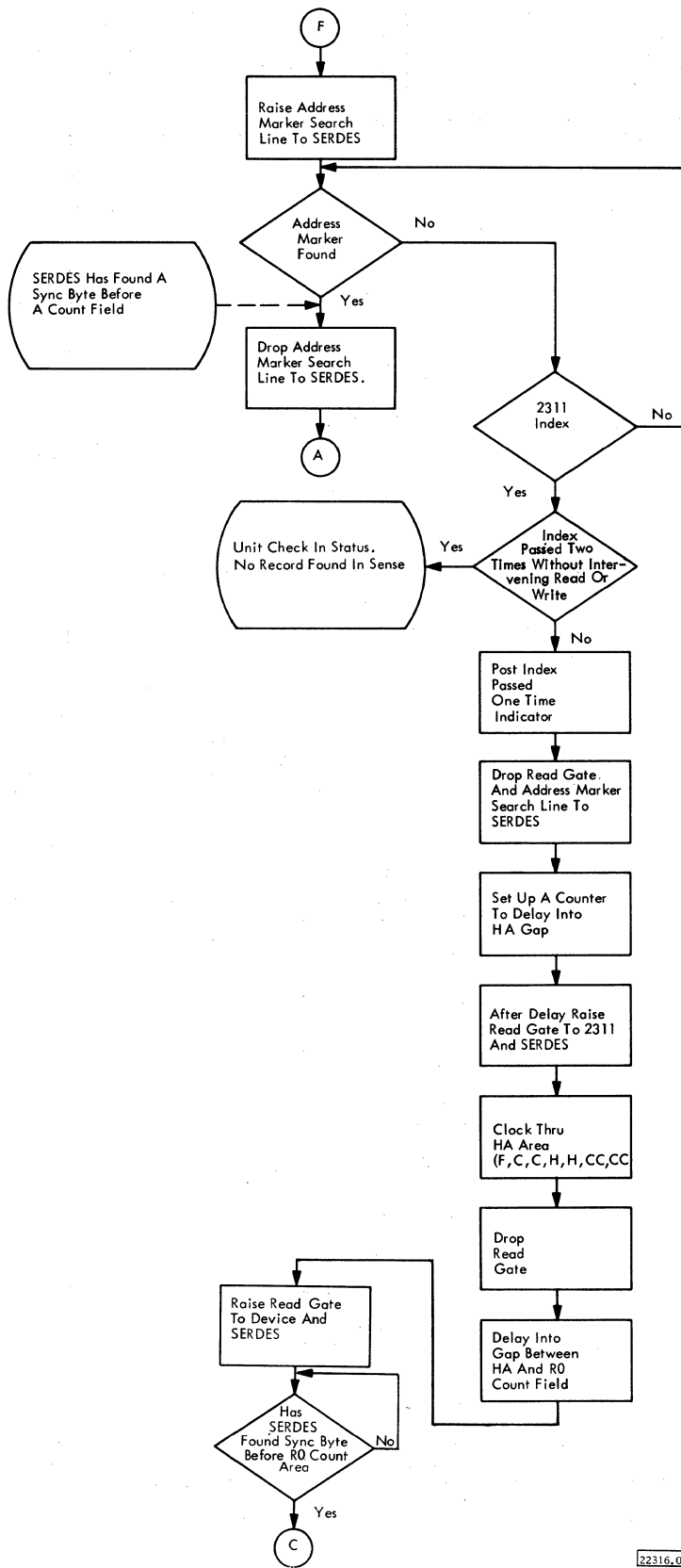
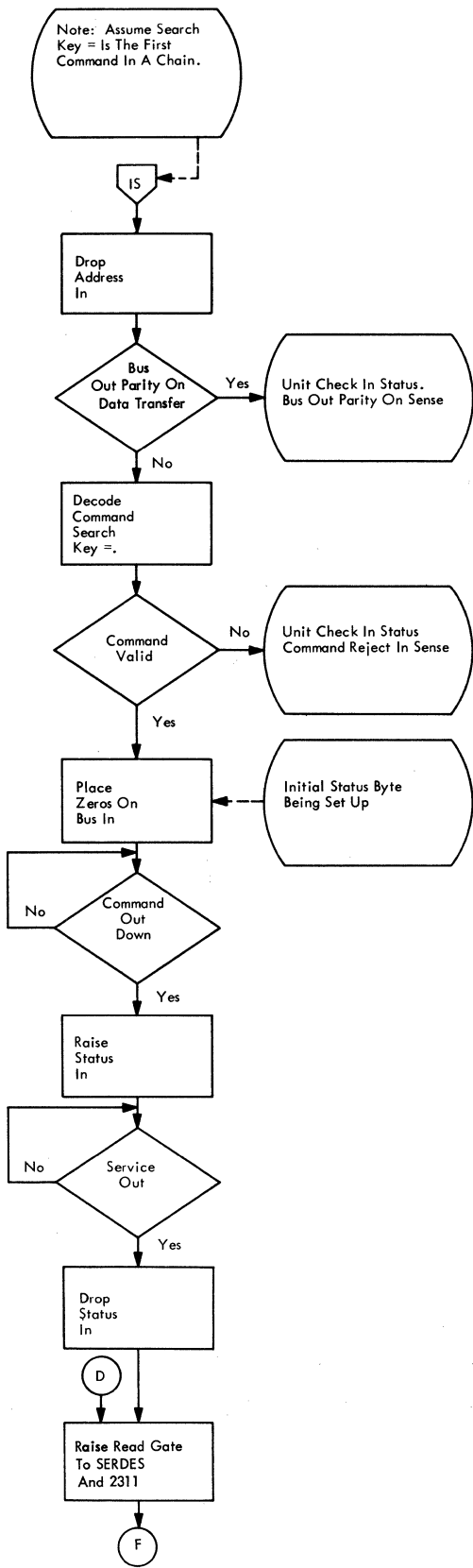


Figure 3-17. Search Key Equal

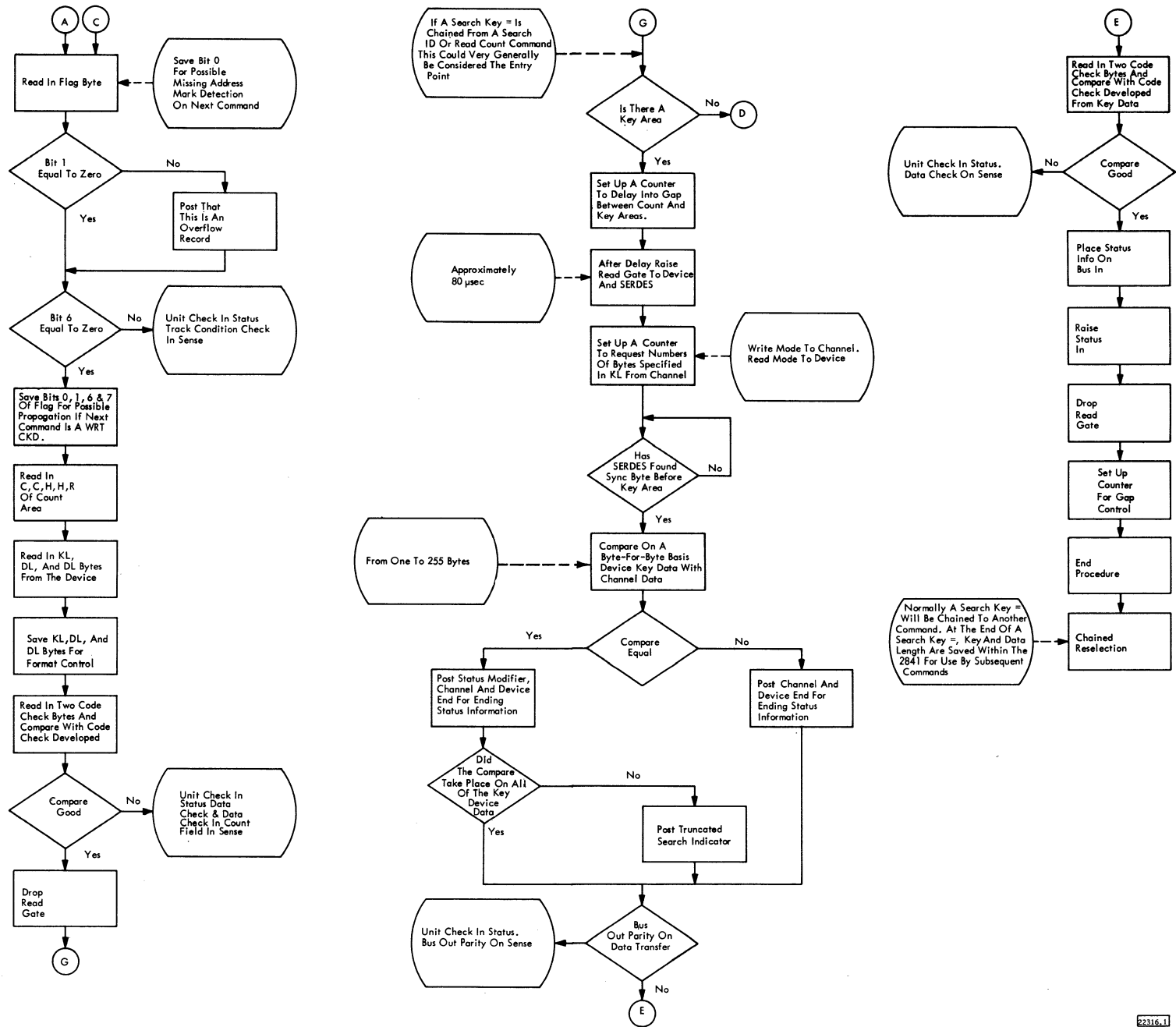
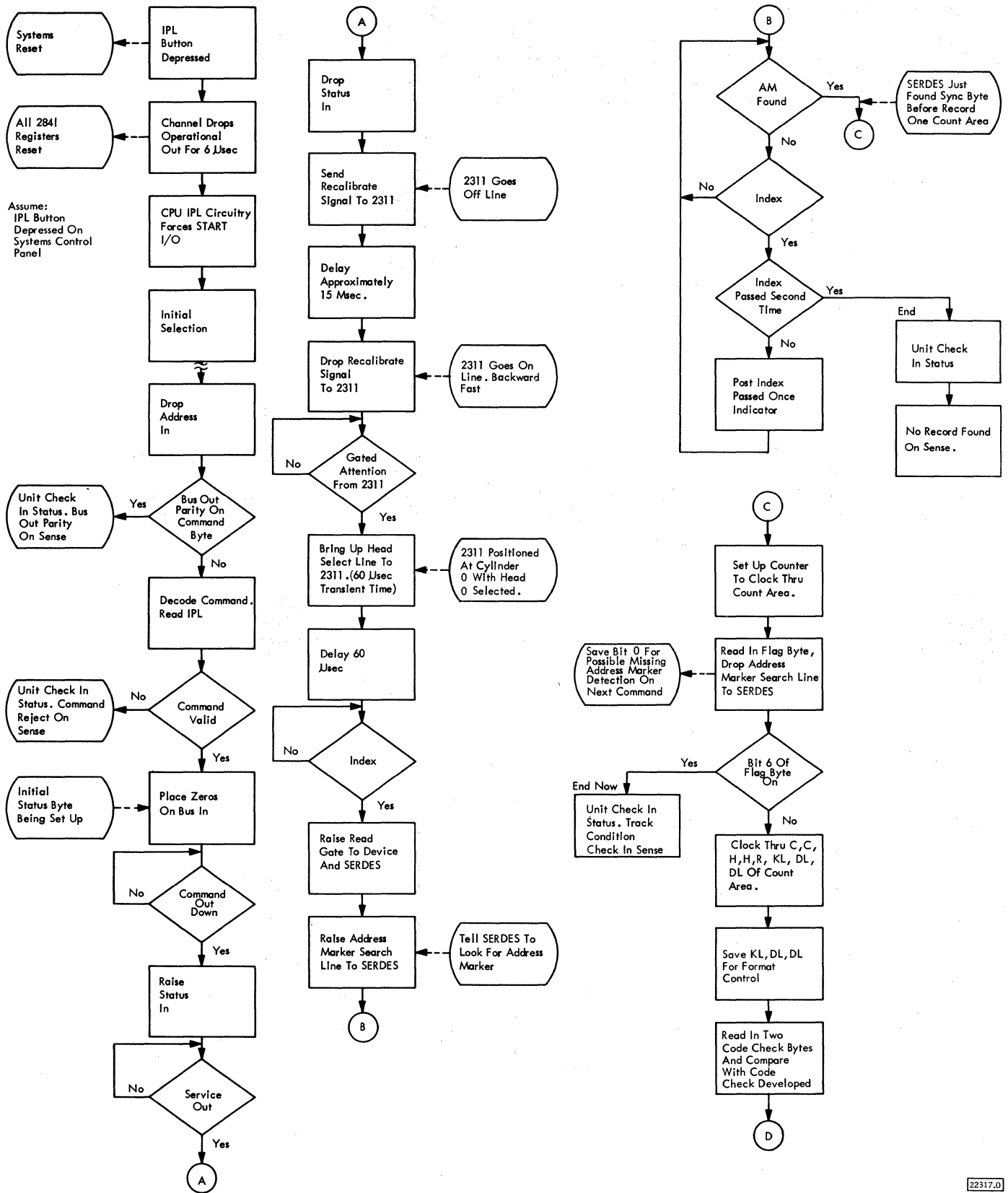


Figure 3-17. Search Key Equal



22317.0

Figure 3-18. Initial Program Load for 2311

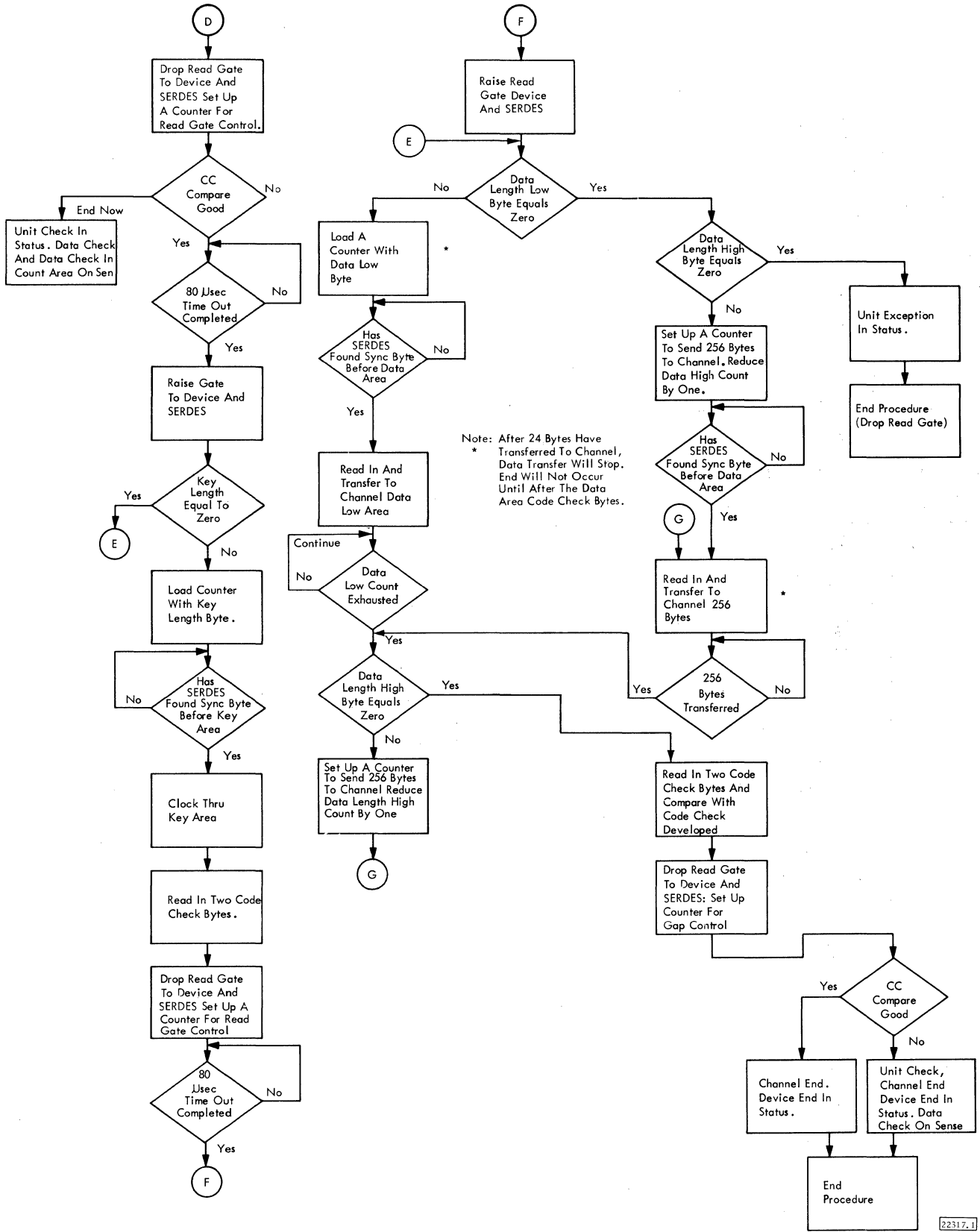


Figure 3-18. Initial Program Load for 2311

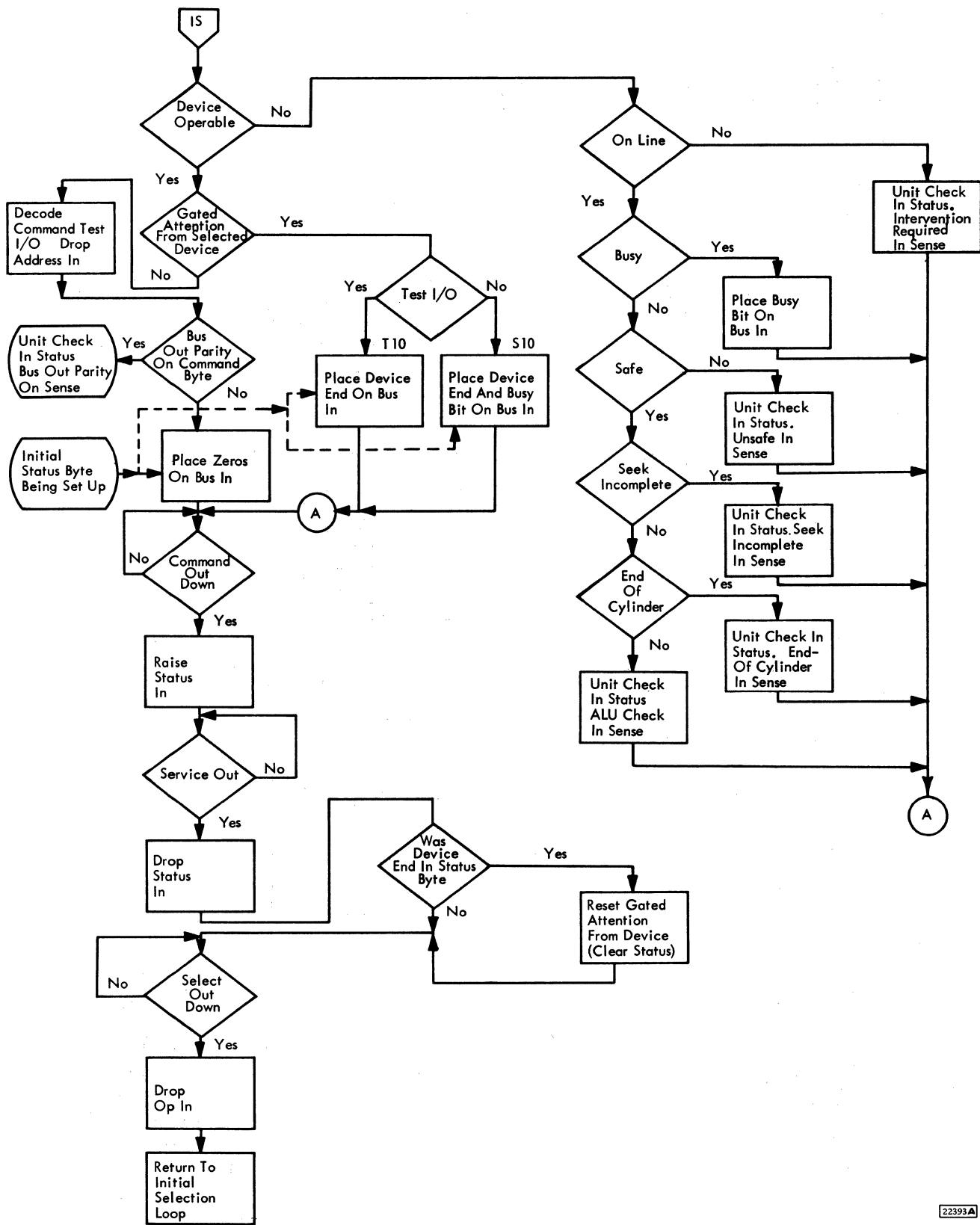


Figure 3-19. Test I/O, or Start I/O with Device In Operable or Outstanding Status

22393A

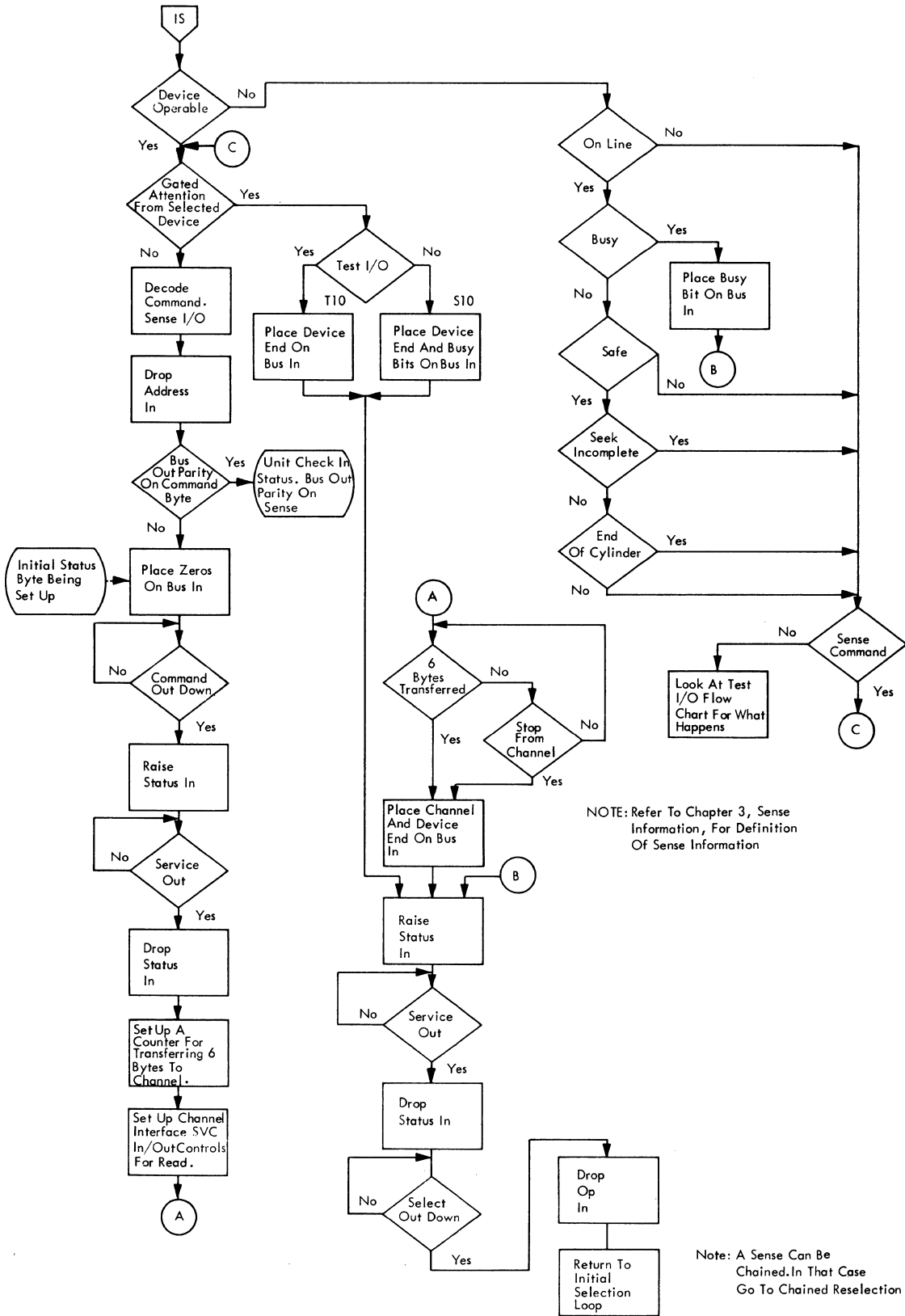


Figure 3-20. Sense I/O

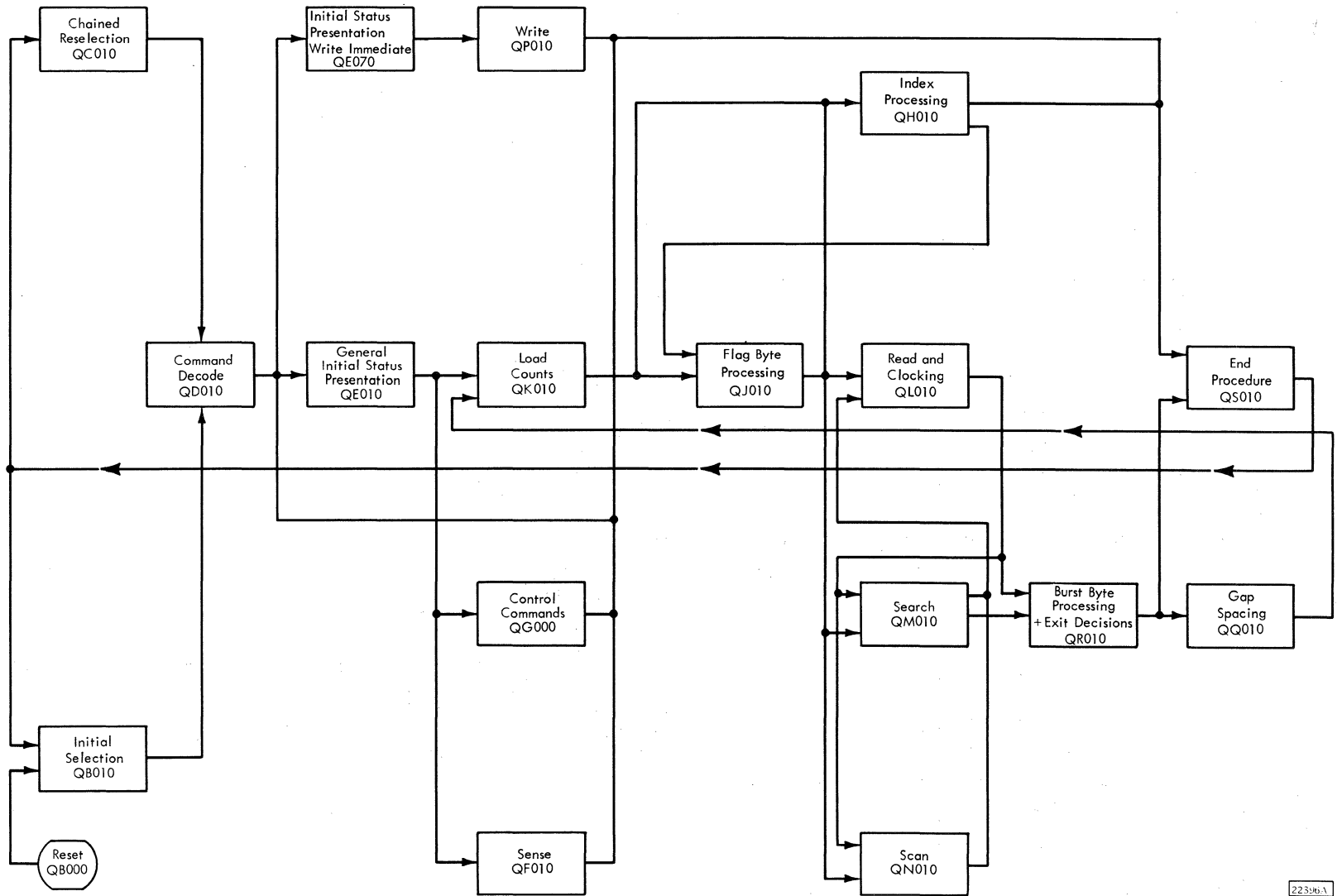


Figure 3-21. Condensed Micro Program Logic

fields, if any, to space over before starting the execution of the command.

Examples:

1. An unorientated Read Data command with the MTM bit off. BY equals: 00010110. This indicates a Read Data operation, with a skip of two fields before execution.
2. A Write Data command chained from a Search Key Equal. BY equals: 10011000. The last command ended after a Key Area. The micro program next begins in a data area.

3.5.4 Initial Status Presentation

3.5.4.1 Not Write Immediate

This section is used to present initial status to the channel. In addition, the timing relationship to the track is maintained if the micro program is oriented to the track. Also, Index is checked in case Read or Write gate is still up. Read gate, if down, is turned on by the Initial Status routine. If the command does not need Read gate up, it is reset in the command section.

3.5.4.2 Write Immediate

This area is used to present initial status to channel for all commands which begin writing immediately. The timing relationship to the track is maintained.

At the proper time, Write and Erase Gates are raised. Based on the previous setting of ST register bits, the micro program either begins writing bytes of zeros (alpha gap), or continues writing bytes of ones (After a formatting write, not HA).

If there are no errors, exit is to the Load Counts section. OP now contains the type of operation and the track orientation necessary to accomplish the operation.

3.5.5 Load Counts

The Load Count routine is used on Read and Search/Scan operations. It checks the type of command (CKD, KD, D), the present orientation to the track and sets up to read or clock the next field. The routine must maintain the totals of key length and data length for use in the Gap Spacing routine.

Load Count also checks for End-Of-File, data length of zero condition, missing key area, and key length zero. The Load Count routine sets up the controls to handle these conditions in the Read or Search/Scan routines.

3.5.6 Write Operations

The Write routine is entered from either the General section or the Write Immediate section of Initial Status. The Write routine writes gaps (including Address Marks), handles Service In/Service Out responses to receive data from the channel, and ST4 responses to supply bytes to SERDES.

This routine has its own load count section. It must keep track of orientation to the track for formatting the track and writing the Beta gap. The Alpha gap is written in the gap spacing routine. The routine loops within itself until the last area is written. It then exists to the End Procedure.

3.5.7 Control Operations

The Control command section is a group of routines which handle the Control commands. The device type and the type of operation to be done are determined. Seek limits are set up depending on device type. The Service In/Service Out responses are handled in order to transfer the address data to the 2841. The address data limits are checked. The address data is decoded. The address data and the proper tags are sent to the devices. The tags vary depending on the device type.

This section also handles the Set File Mask command. The mask data is received from the channel and stored for use on seek and write commands. The checking of commands with the File Mask is done in the Command Decode section.

The Space Count and Erase commands are handled in the Write section even though Space Count is classed as a control command.

3.5.8 Sense Operations

The Sense I/O routine is entered from the Initial Status Presentation routine after the status byte has been accepted by the channel.

A test is made to see if the sense information is stored. If the information is not stored, the routine transfers bytes of zeros to the channel with the exception of the File Status byte. If the information is stored, up to six bytes of information are transferred to the channel depending on the count in the CCW. The routine controls the Service In/Service Out responses for the transfer and keeps track of how many bytes have been transferred. Exit is made to End Procedure.

3.5.9 Flag Byte Processing

The Flag Byte Processing routine is entered on all Address Mark Search, Read or Search HA and Read,

Write or Search R0 operations. This routine checks for missing Address Marks, Overflow Records, and track condition bits. On Search HA commands, the routine also stores the Flag byte to be used in writing Flag bytes on other records on the same track.

Exit is to the Read/Clocking or Search/Scan routine if the track condition is good. If the track condition is defective, exit is to End Procedure.

3.5.10 Index Processing

The Index Processing routine may be entered from Initial Selection on Read, Write, Search HA or R0 operations.

This routine checks for missing Address Marks, No Record Found indications and timing conditions when Index is needed to control the operation.

On Write Home Address operations, the Index Processing routine requests the Flag byte from the channel and sets up to control the size of the HA gap.

On Multi-Track operation, this routine handles head advancing and checks for an End-Of-Cylinder condition.

3.5.11 Read/Clocking

The Read/Clocking routine is entered from Flag Byte Processing, Search/Scan or Gap Spacing.

The Read routine must service the ST4 responses from SERDES, transfer the byte through ALU to insert the parity bit if needed, generate burst bytes and handle the Service In/Service Out responses to transfer the information to the channel. The routine also handles field count decrementing to determine when the field operated on has been completed.

The routine is used for clocking over areas that are not needed for the command being done, ie: key area on a Read Data CCW. This is done by not setting up the Service In/Service Out response. Therefore, no data is transferred to the channel. Burst byte generation is done but errors do not cause an exit to End Procedure while clocking.

Orientation to the track is updated in the Read/Clocking routine so that the proper decisions may be made in the Burst Byte and Exit Decisions section.

3.5.12 Search Operations

The Search routine handles the Service In/Service Out responses in write mode in order to transfer data from the channel. The Search routine also handles the ST4 responses from SERDES in order to transfer data from the device. The routine transfers data through the ALU for parity generation. Burst

bytes are also generated. The data from the channel and the data from the device are compared on a byte-for-byte basis for high, low or equal as determined by the command. The routine sets controls which later cause setting of the Status Modifier if the conditions are satisfied.

Exits are made to Burst Byte Processing or Clocking routines as called for by the type of command.

3.5.13 Scan Operations

The Scan routine replaces the search routine if the Scan feature is installed.

Search operations work in the same manner as before.

Scan operations are the same as Search operations with these exceptions:

1. The Scan routine must be able to suspend comparing when a mask byte (Hex FF) is received from the channel.
2. Because Scan operates on the Data area as well as on Count and Key areas, the Scan routine must decrement a two-byte count.

Exit is made to Burst Byte Processing or Clocking routines.

3.5.14 Burst Byte and Exit Decisions

Entry to the Burst Byte and Exit Decisions section is from Read/Clocking or Search/Scan routines.

This routine reads the two Code Check bytes and Exclusive or's the two check bytes with the generated burst bytes, and checks both bytes for zero. If the result is not zero, set burst error condition for use in the Sense bytes.

Track orientation is updated in this routine and an exit decision is made to return to Read/Clocking or Search/Scan by way of the Gap Spacing routine or exit to End Procedure.

3.5.15 Gap Spacing Operations

Entries to the Gap Spacing routine are from the Burst Byte and Exit Decision routine, or from the gap Writing routine. The Gap Spacing routine contains a timer which is set up to control the resetting of Read gate and the timing out and turning on of read gate. Read gate is turned on in order to read the Sync byte in the gap to locate the next record. Exit from the Read gap spacing routine is to the Index Processing routine on overflow records or to the Initial Status Presentation routine. Entry to the Initial Status routine is made after the presentation of

status is complete in order to make decisions on entering the next area.

The Gap Writing routine contains a timer to control the number of bytes written in the gap. The routine also controls the byte configuration for the gaps. The number of bytes written varies depending upon the type of device being used. This routine writes up to, but not including, the Sync byte which is taken care of in the Write routine. Exit from the Gap Writing routine is back to the Write routine.

3.5.16 End Procedure

Entry to the End Procedure routine is made from Command Decode, Initial Status Presentation, Write, Index Processing, Burst byte or Exit Decisions routines. Entry is also made from any place where an error may have occurred or an end of operation detected. End Procedure determines if a chained or unchained end of operation exists and presents the ending status of the operation.

To present the ending status, the Status In/Service Out response within the End Procedure routine is controlled. This routine also sets up a timer on chained operations to determine if the next command is received without an over-run condition. The End Procedure routine also regenerates the Address of the selected device for use in the Chained and Initial Selection routines.

Exits from the End Procedure timed section for chaining operations are to the Chained Reselection section. Exit from the End Procedure untimed

routine is to the Initial Selection loop to wait for the next operation.

3.5.17 Chained Reselection

Entry to Chained Reselection is from End Procedure in operations that are indicated as being chained from the previous operation. Because the next operation must come within a given amount of time in order to prevent running into the next area of the track, a timer is maintained to control the turning on and off of Read gate, Write gate and Erase gate.

Checks are made within this routine for Index, in case Index may enter into the sequence of the operation. If an Index is detected, the program exits to the Index Processing routine. A check is also made to see if the selected device is safe or unsafe. If the device is found to be unsafe, the routine exits back to End Procedure in order to indicate to the channel that the selected device can no longer be used.

Before exiting from the Chained Reselection routine, an indicator is set up to indicate to command decode, whether the device is oriented for a write or a not write condition. Exit from the Chained Reselection routine is to Command Decode in order to wait for the command and decode it before going on with the next operation.

3.5.18 Command Orientation Summary

Refer to Table 2 for the valid orientation at the beginning and end of each command.

Table 2. Command Orientation Summary

Command	Command Prerequisite	Valid Orientation State at Beginning of Command	Orientation State at Completion of Command
Read CKD	None	AM	Data
Read KD	None	Count AM	Data
Read D	None	Count Key	Data
Write CKD (Also Write Special CKD)	Search Equal Count or Key Write CKD Write R0	Count Key Data	Data
Write KD	Search Equal Count	Count	Data
Write D	Search Equal Count or Key	Count Key	Data
Search ID	None	AM or IP AM	Count
Search Key	None	Count AM	Key
Search Key-Data	None	Count	Data
Search Home Address	None	IP Home Address	Home Address
Read R0	None SFM Search Equal Home Address	IP Home Address	Data
Write R0	Write HA	Home Address	Data
Read HA	None	IP	Home Address
Write HA	SFM	IP	Home Address
Read IPL	None	AM	Data
Read Count	None	AM	Count
Control Space Record	Search (any) Read (any) Search Equal Count or Key	AM	Reset Orientation
Control Erase	Write CKD	Count Key	Data
Control NOP	Write R0 None	Data Any	Reset Orientation

22023

4.1 GENERAL POWER SUPPLY DESCRIPTION

The 2841 contains the necessary power supplies for the operation of 2841 circuitry and certain voltages for the attached devices. The 2841 power supplies furnish the following voltages for internal use:

+6 vdc, +3 vdc, -3 vdc, +12 vdc, -36 vdc

In addition, the 2841 supplies the following voltages to the attached 2311's in the subsystem:

+6 vdc, +3 vdc, -3 vdc, -36 vdc

Power input to the 2841 is 208/230 vac 3 phase 30 amperes. Taps are provided on the input transformers of the power supplies to match the voltage supplied by the customer.

Each power supply is equipped with a voltage regulator card and a circuit breaker for over-current protection. The output voltage of each of the supplies can be adjusted by means of a potentiometer on the supply. For more information on power supplies refer to IBM Field Engineering Manual of Instruction Solid Logic Technology Power Supplies, form 223-2799.

All power supplies are brought up together except the +12 vdc supply which must wait until +6 vdc comes up.

The 2841 provides a controlled ground to the attached 2311's to control power on and off sequencing of the 2311's. The 2841 also provides 208/230 vac, 3 phase power to the attached 2311's via CB-2.

Power on/off control of the 2841 is controlled by the CE/NORMAL (Remote) switch. With the CE/NORMAL switch in the CE position, power must be brought up and down by means of the ON/OFF switch on the 2841 CE panel. With the CE/NORMAL switch in the NORMAL position, power on and off is under control of the using system and the CE panel controls are inoperative. Emergency Power Off can drop power regardless of the position of the CE/NORMAL switch. (Figures 4-1, 4-2, 4-3, 4-4)

4.1.1 Power Supply Components

4.1.1.1 Circuit Breakers

CB - 1 (50~only) 8A - Convenience outlets -115v
 CB - 2 20A - AC power to 2311's

CB - 3 30A - 2841 power supplies (not +12v)
 - 2841 fans
 - 3 phase ac power to 2841

4.1.1.2 Circuit Protectors

CP - 1 3A - +6 vdc power supply no.2
 CP - 2 3A - -3 vdc, -36 vdc
 CP - 3 3A - +3 vdc, + 6 vdc no. 1
 CP - 4 1A - 24 vac, +12v

4.1.1.3 Contactors

K - 1 - convenience outlet contactor
 K - 2 - 2311 and power supplies contactor
 K - 3 - Emergency Power Off contactor
 (There will be no 24 vac control power if K3 is not up)

4.1.2 Thermal Considerations

There are four thermal cutout switches. One is mounted in the TROS gate "A". One is mounted above board B1 and one is mounted above board C2. The fourth thermal is mounted above the power supplies. Opening of any of the thermal switches drops R6 which drops R4 and R5 causing a normal power down sequence.

4.1.3 Marginal Checking

No facilities for marginal checking are provided in the 2841 other than actually varying the voltages at the power supplies.

4.1.4 Power Distribution

The power supply outputs are fed to bus bars on the front side of the 2841. From these bus bars the voltages are distributed to various points in the machine.

The A gate receives its power via a laminated T bus which ends in terminal strips on the bottom of the A gate. The A gate receives the following voltages:

-36 vdc -3 vdc
 +12 vdc +6 vdc
 +3 vdc ground bus

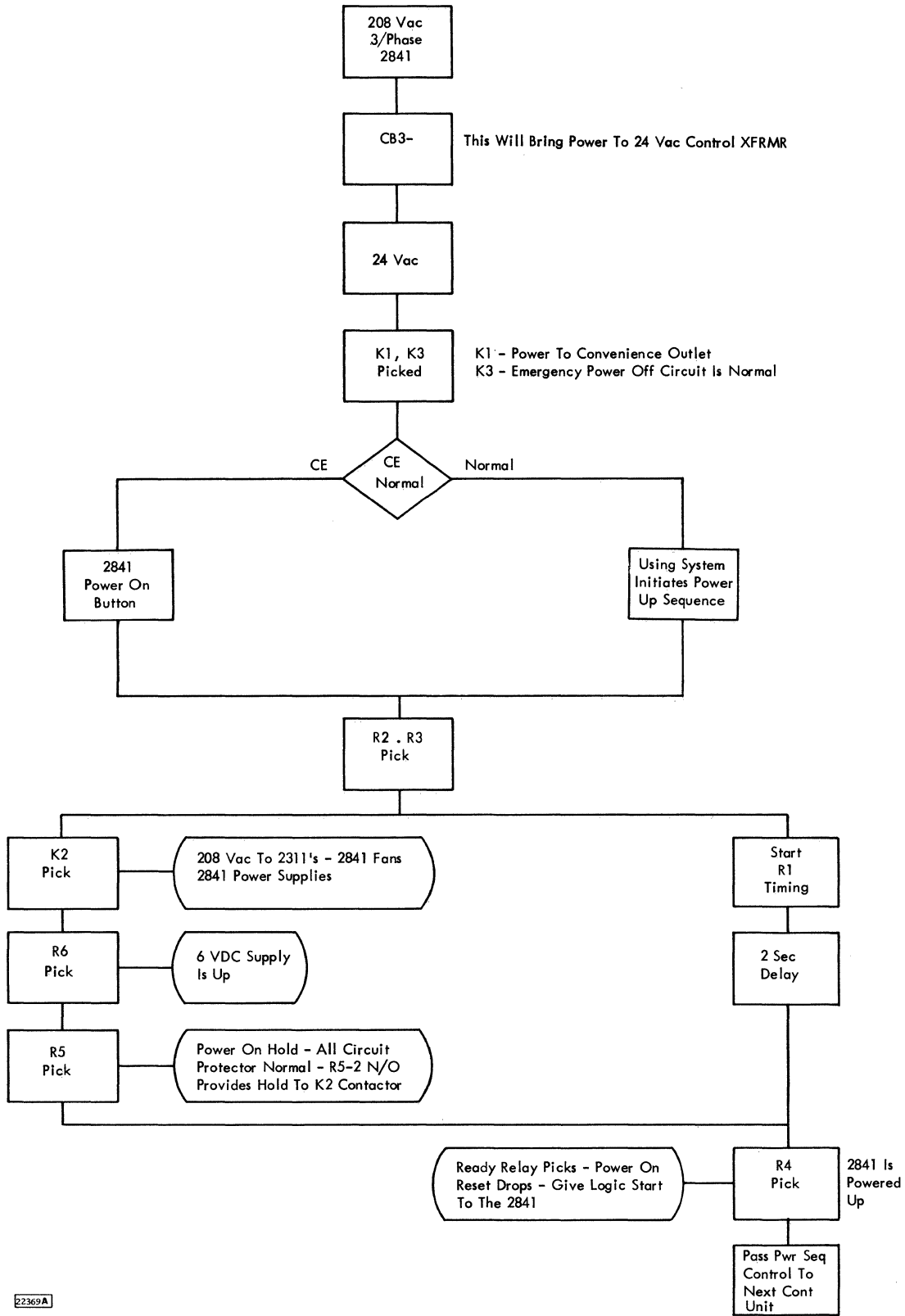
The TROS gate receives the following voltages via a laminated T bus on boards A1 and A2 on the TROS array:

- + 3 vdc
- 3 vdc
- + 6 vdc
- ground bus

Cooling fans for the A gate, TROS array and the power supply stack receive their ac power from terminal strip TS-1 located within the ac sequencing box on the left side of the 2841.

4.1.5 Power Interlocks

Relay 1 is a 2 second time delay relay which begins timing when power sequencing is started on the 2841 (CE or NORMAL (REMOTE)). Two seconds after the sequencing has begun, the power on hold control is transferred to Relay 5, if Relay 5 has not picked at this time, power will sequence down. The 2 second time delay also allows 2 seconds for power on surge current to settle down before allowing the next control unit to begin its power up sequence.



22369A

Figure 4-1. Power On Sequence

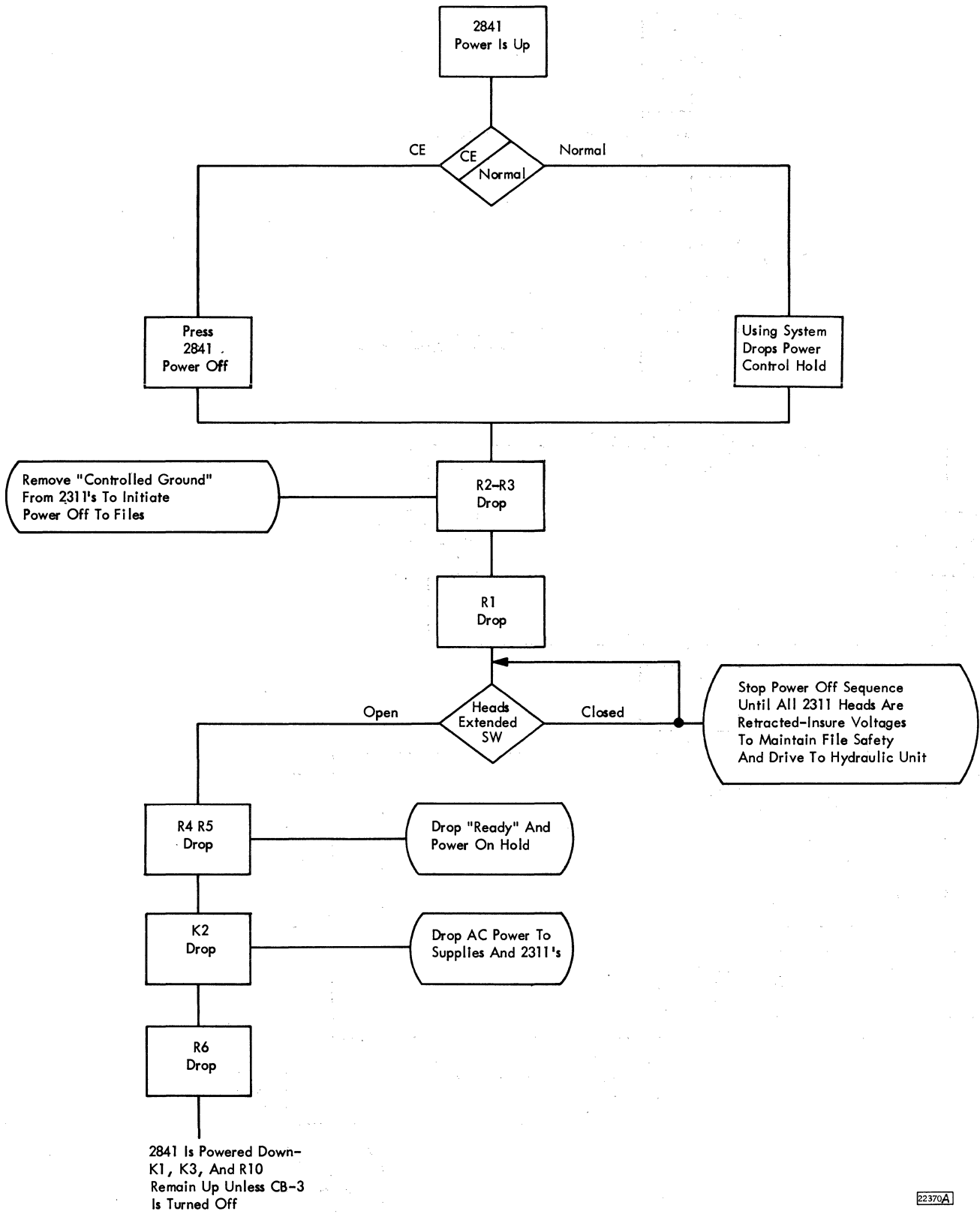


Figure 4-2. Power Off Sequence

22370A

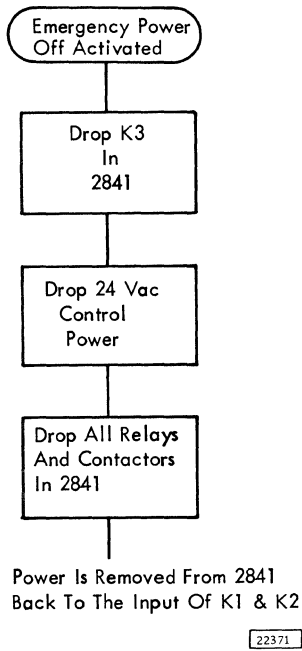
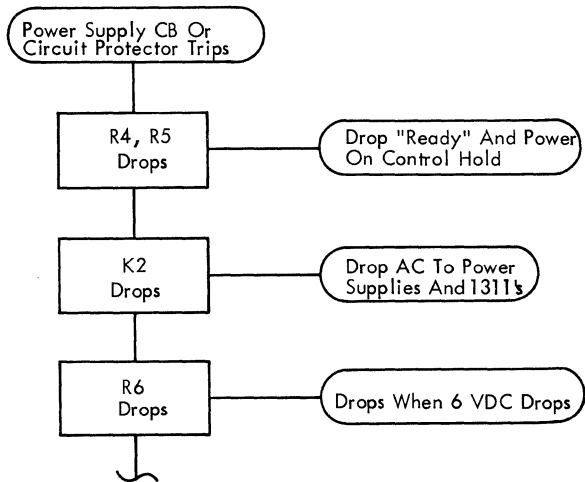


Figure 4-3. Power Off Sequence - Emergency Power Off



At This Point The 2841 Will Not Automatically Sequence Up When The Circuit Breaker Is Restored - Place The CE/Normal Switch In CE (This Activates The Power On/Off Controls On The 2841 CE Panel)- Press The Power Off To Restore The 2841 Power Sequencing Controls- Press Power On (On 2841) To Bring Power Back Up Again.

22372

Figure 4-4. Power Off Sequence - Power Supply Overload or Circuit Protection Trip

5.1 2302 MODELS 3 AND 4, 2321, ATTACHMENT

- Provides circuitry to attach 2302 Models 3 and 4, and 2321 devices.
- Provides signals to control device operation.
- Provides signals to the basic 2841 from the devices.
- Circuitry for all three devices is on one large SLT board A3.

Board A3 provides the circuitry to attach the 2302, Models 3 and 4, and 2321 to the basic 2841-2311. (Figures 5-1 to 5-11)

Signals provided by the micro program are developed and sent to the devices to control the operations. Signals from the devices are gated so that they may be used by the micro program.

Selection of the feature interface is done by the micro program checking the unit address with

constants set in the micro program by the CE to assign the device type to a unit address.

The micro program selects the 2311 interface with the statement FT = 1; the feature interface is selected with a FT = 2 or FT = 4 statement. A description of the interface lines for these feature devices is included in the applicable device FEMI.

The attachment consists of the same basic units as the 2311 attachment; FT and FC registers, Module Selection, Attention and File Status gating.

The FT and FC bit decodes vary from the 2311 decodes and vary with each of the devices. The micro program varies the set up of the control lines and timings for the type selected.

Table 1 shows the differences in capacity and timing for the devices controlled by the 2841. Tables 2 and 3 shows the differences in line names and controls for the devices controlled by the 2841.

The addressing scheme for the seek address varies with the different devices as shown in the following chart:

Type	Cell Number		Cylinder Number		Head Number	
	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5
2311	0	0	0	0-202	0	0-9
2302 Mod. 3 Mod. 4	0	0	0	0-249	0	0-45
2321	0	0-9	0-19 Subcell	0-9 Strip	0-4 Bar	0-19 Head No.
Example of a 2311 binary address (bit configuration)	Cell Number 0 00000000 00000000		Cylinder Number 163 00000000 10100011		Head Number 5 00000000 00000101	

5.1.1 Device Attachment Limits

5.1.1.1 Attachment Limits of Basic 2841

A maximum of eight 2311's may be attached.

5.1.1.2 Feature Device Attachment:

This feature permits the installation of 2321 or 2302 direct access storage devices. Any combination of devices that does not exceed eight accesses can be installed. For this count, the number of accesses per physical device is:

<u>Storage Device</u>	<u>Number of Accesses Per Device</u>
2311	1
2321	1
2302-3	2
2302-4	4

Examples:

1. 8-2321's
2. 4-2311's
4-2321's
3. 2-2302-4's
4. 4-2321's
1-2302-4
5. 4-2311's
2-2321's
1-2302-3

In all cases the 2302 must be an even module select number. The 2302-3 must connect to either D, F, H, or K I/O connector. The 2302-4 must connect to either D or H I/O connector. 2321's must always be the first units connected to the 2841 on the multiplex cable.

5.1.2 2302 Operation

- Provide selection, address transfer and head selection of 2302.

When the channel command calls for a 2302 operation, the micro program determines that a feature device is called for and gives a FT = 4 statement to select the Feature attachment. FT bit 5 and not FT bit 6 determines that the 2302 is selected. (Figures 5-1, 5-2, 5-4, and 5-5)

The operation is the same as for a 2311 with the exception of the Head Address transfer to the 2302, which is a 16 bit address for the 2302. First, the units byte is placed in the Address register and then the high order byte is placed in the FC register. The Address register and the FC register are gated to the 2302 as a 16 bit word.

The 2302 has the same bit rate and format as the 2311 and uses the same read and write circuits in SERDES. The HA gap is larger than the HA gap for the 2311 (Figure 5-16).

5.1.3 2321 Operation (Figures 5-1, 5-3, 5-4, and 5-5)

- Provide selection, address transfer and head selection of 2321.

The 2321 operation is different than the 2311 and 2302. The address transfer sequence and timing are shown in Figure 5-5.

The slower byte rate of the 2321 requires the use of a 875 kc Write oscillator. The selection of a 2321 operation gates the 875 kc oscillator and de-gates the basic 2.5 mc oscillator.

The slower byte rate also requires a different VFO circuit. The operation of this VFO is the same as the basic VFO but at a slower timing rate. The Block Bit Ring Advance Single Shot is timed for 4600 ns instead of 1600 ns. (Figures 5-17 thru 5-20)

The track format is changed for the 2321 by the addition of an Address Mark ahead of the HA field.

On the 2321 if a defect is found on the strip in the HA or Record 0 areas they may be moved approximately 800 bytes from index. This is done by making the Flag byte bits 1 and 6 ones and by doing a Write HA CCW.

5.2 ADDITIONAL STORAGE FEATURE

- This feature allows attachment of additional units of 2302 Models 3 and 4 to a basic 2841.
- A maximum of sixteen accesses in any combination of 2311, 2321, 2302-3, 2302-4 is provided.
- All accesses above the basic eight must be 2302-3's or 2302-4's.
- Maximum of eight units.

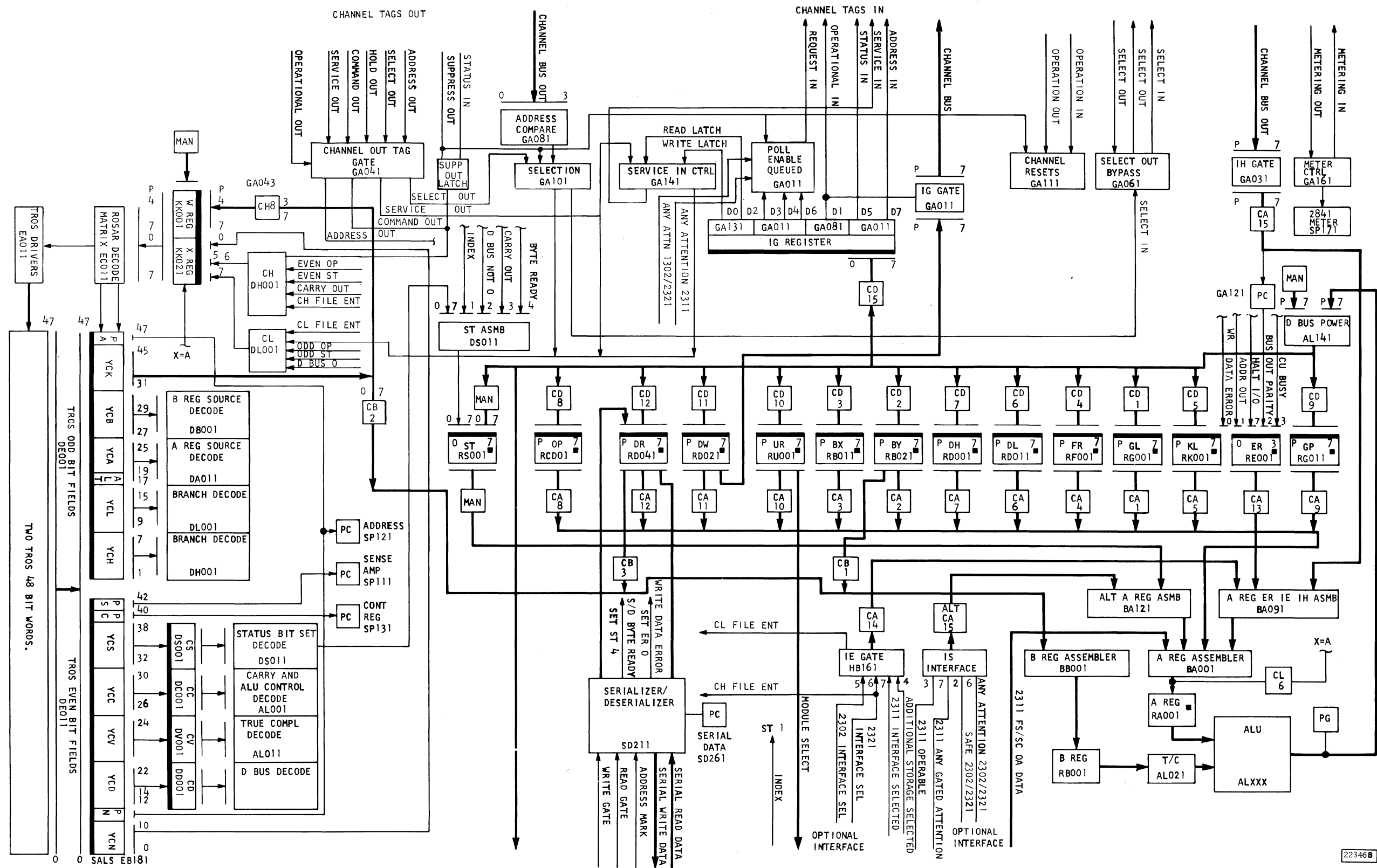


Figure 5-1. 2841 Attachment Data Flow

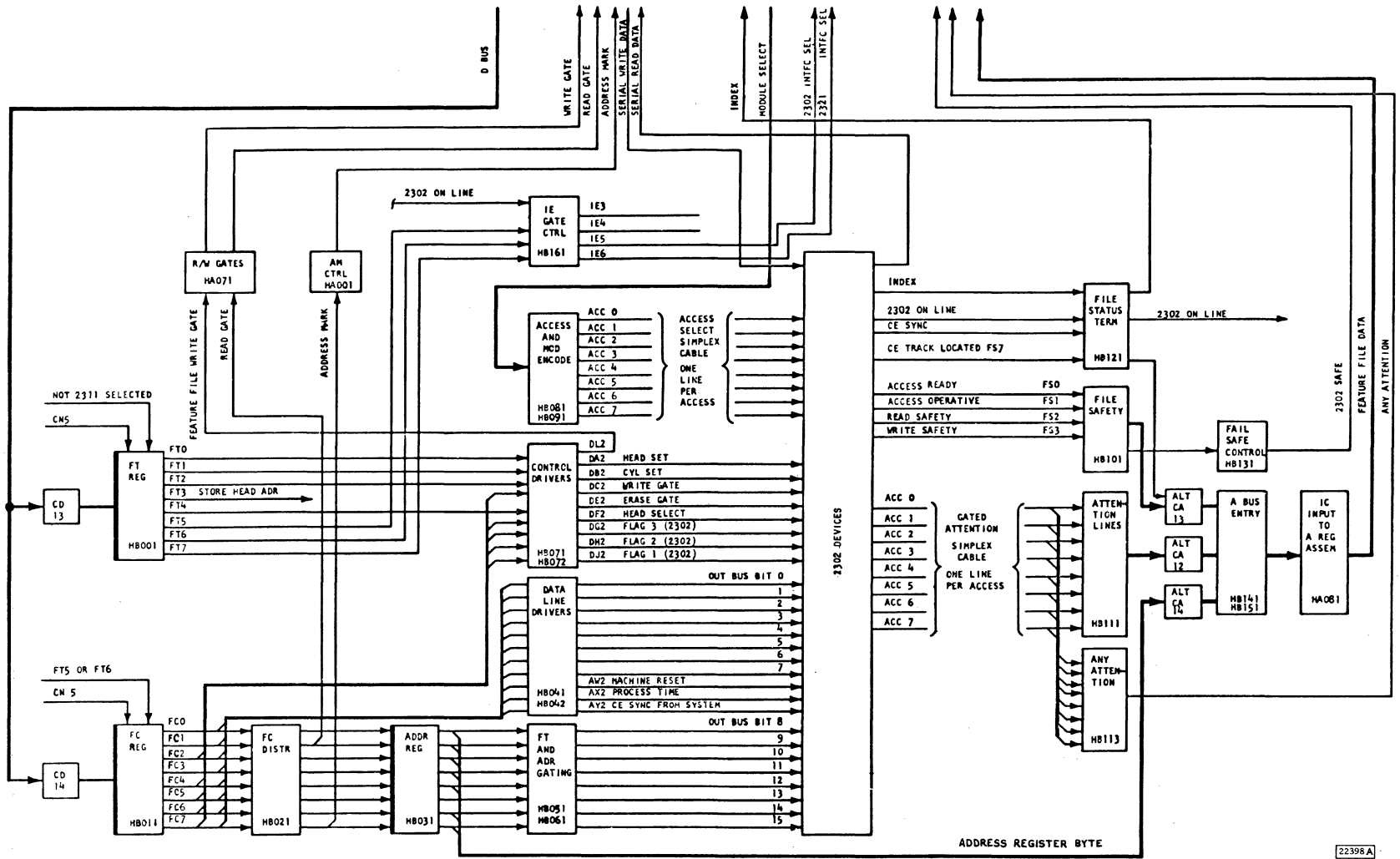


Figure 5-2. 2302 Attachments Circuits

22398A

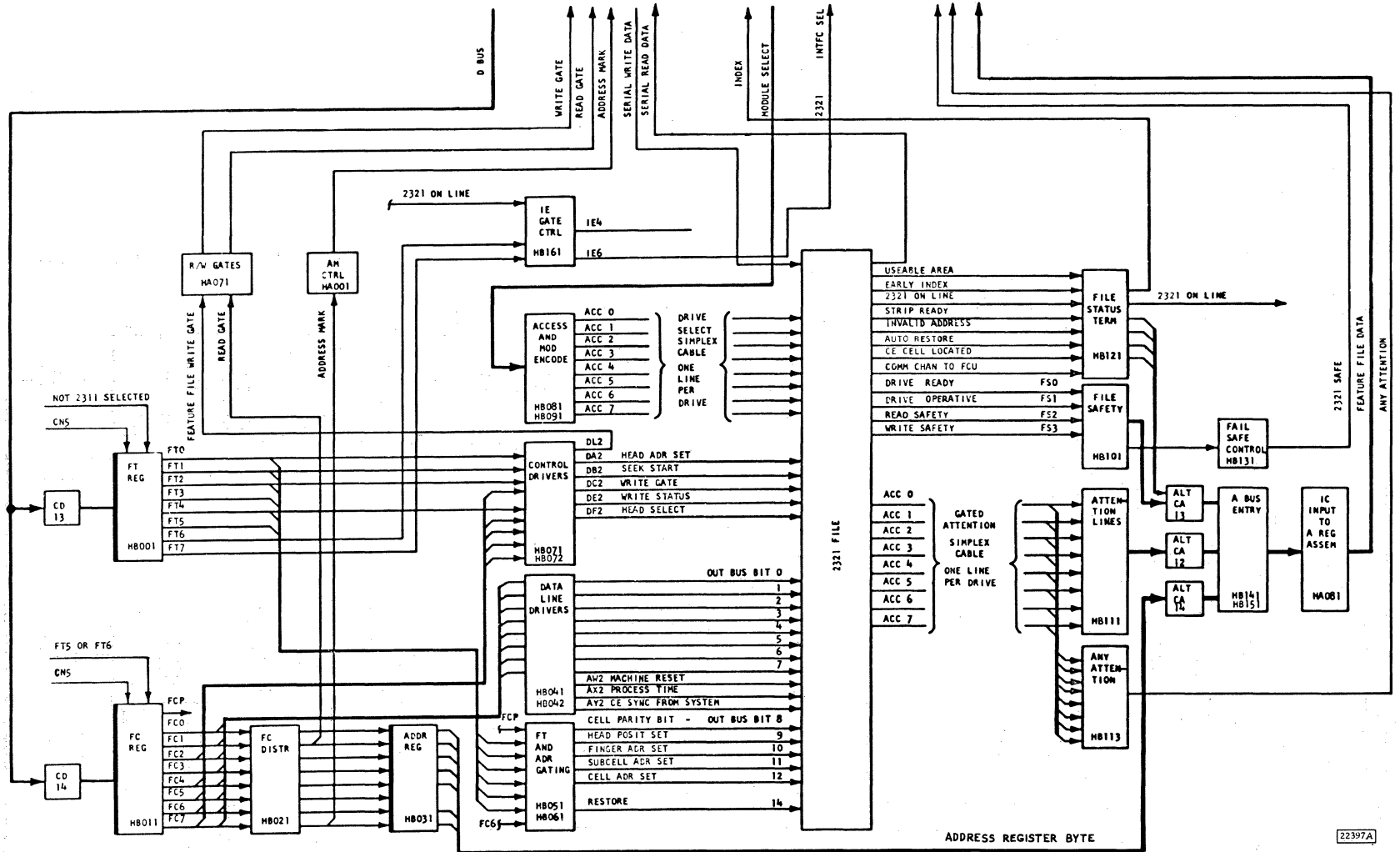


Figure 5-3. 2321 Attachment Data Flow

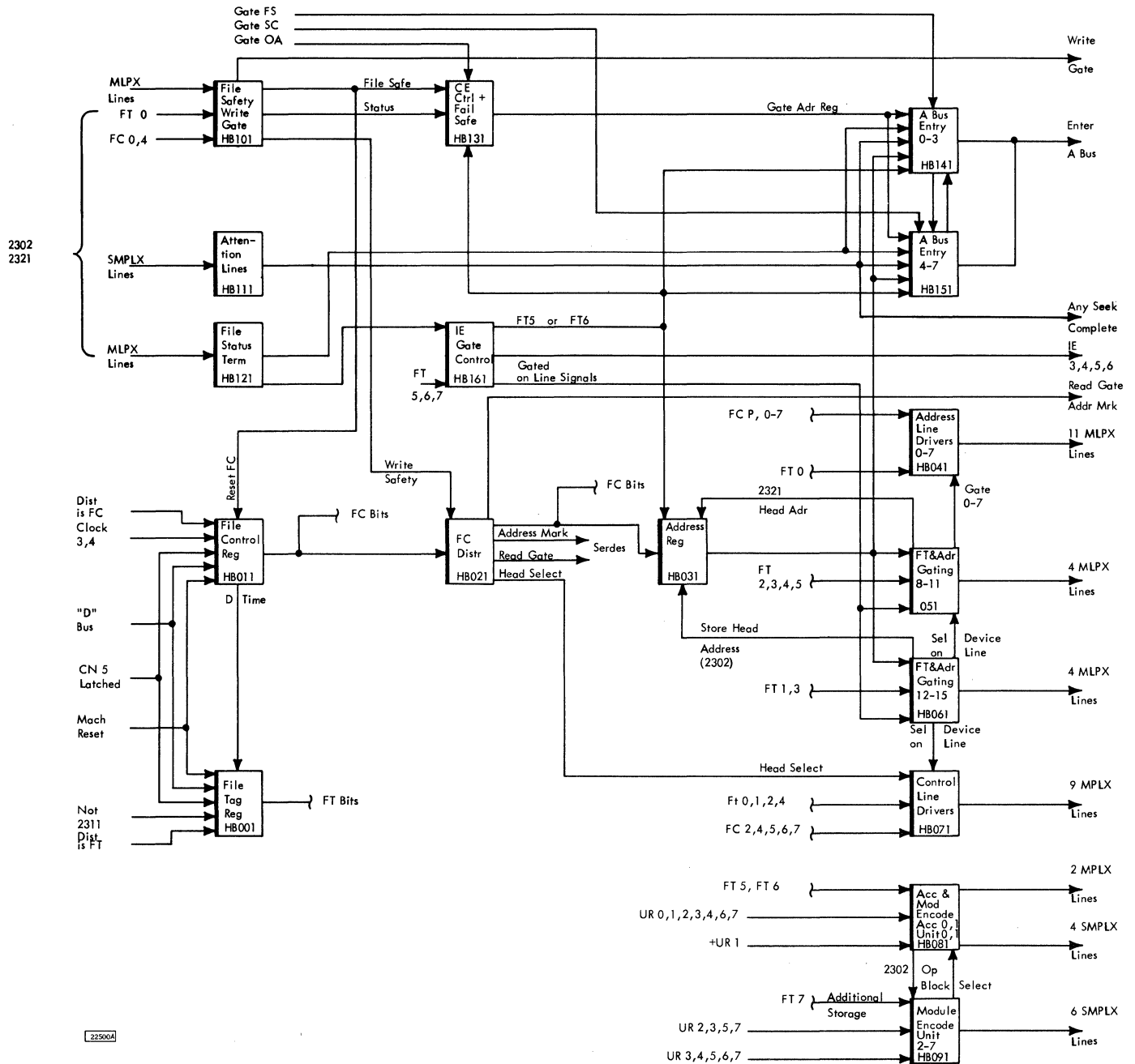
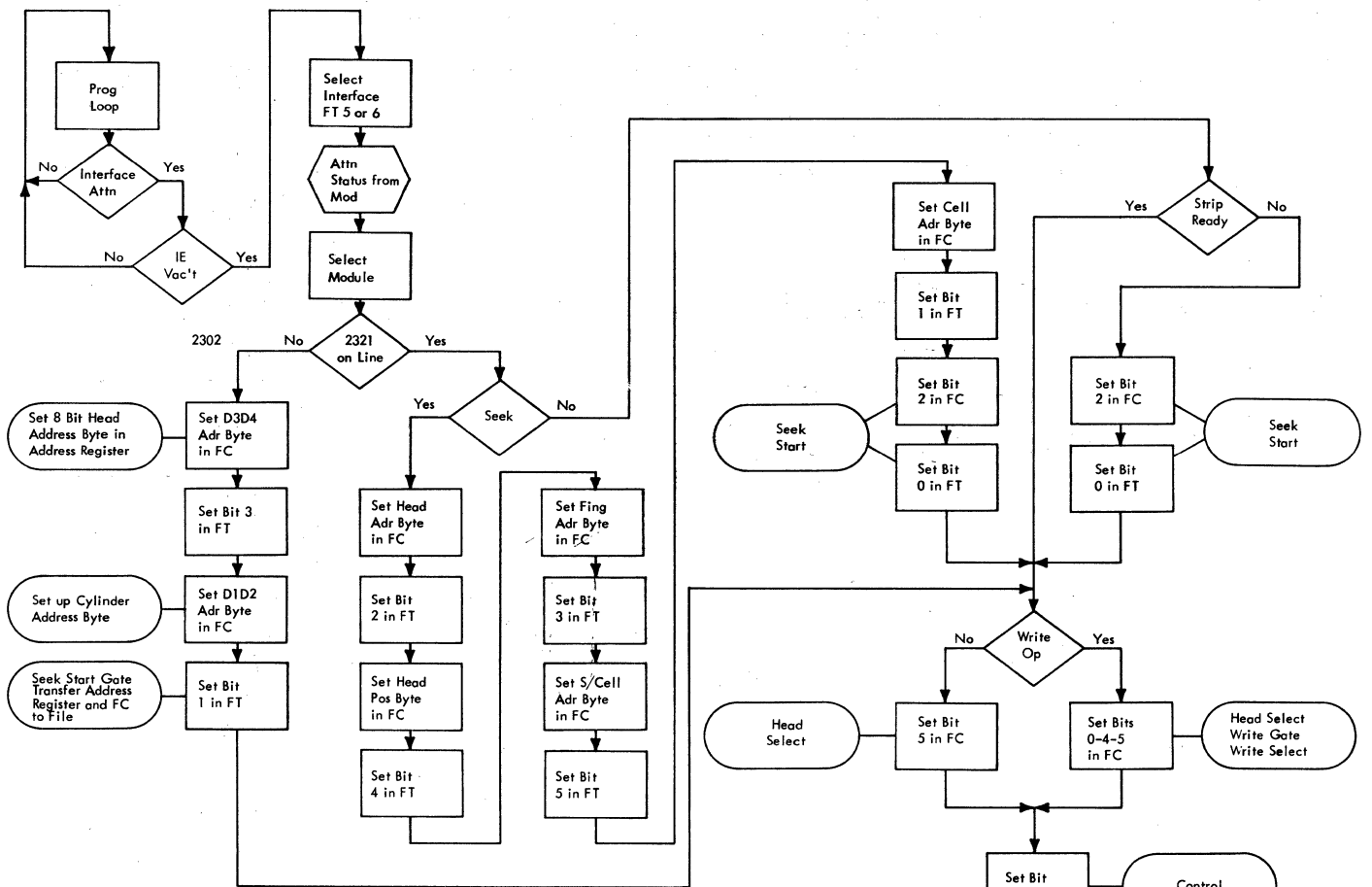
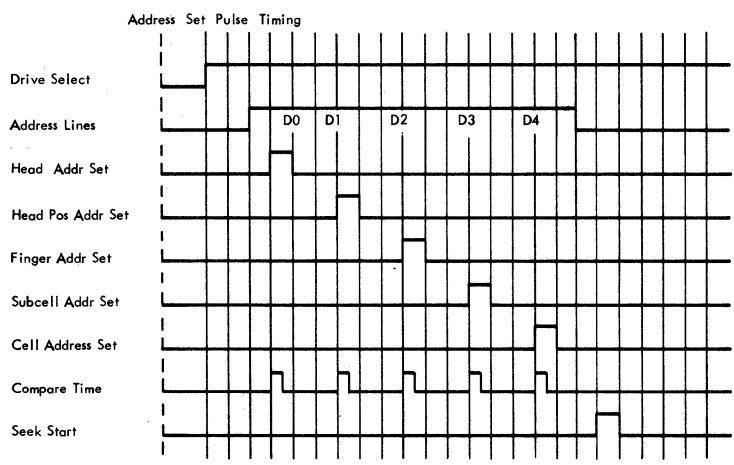


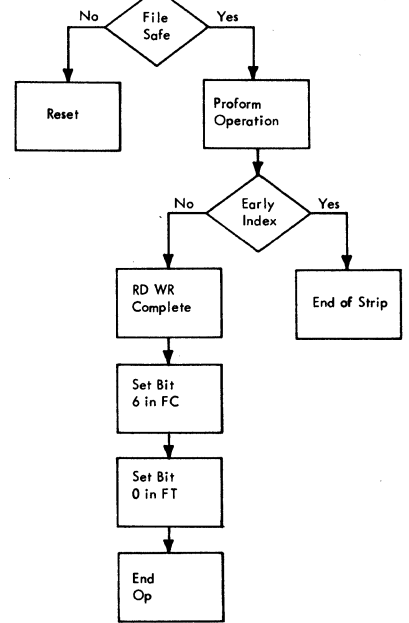
Figure 5-4. Feature Device Interface



FT 0 = Control
 FT 1 = Cell Adr Set = Cyl Set
 FT 5 = Subcell Adr Set
 FT 3 = Finger Adr Set = Adr Set
 FT 4 = Head Posit Set
 FT 2 = Head Adr Set = Head Set
 FC 0 = Write Gate
 FC 1 = Read Gate
 FC 2 = Seek Start
 FC 4 = Write Status Erase Gate
 FC 5 = Head Select
 FC 6 = Restore
 FC 7 = Address Mark



Notes:
 1. Set pulse duration is 2 usec minimum.
 2. Address lines shall be activated from 2 usec before leading edge of set pulse to 2 usec after trailing edge of set pulse.



22501A

Figure 5-5. Serial Address Sequence

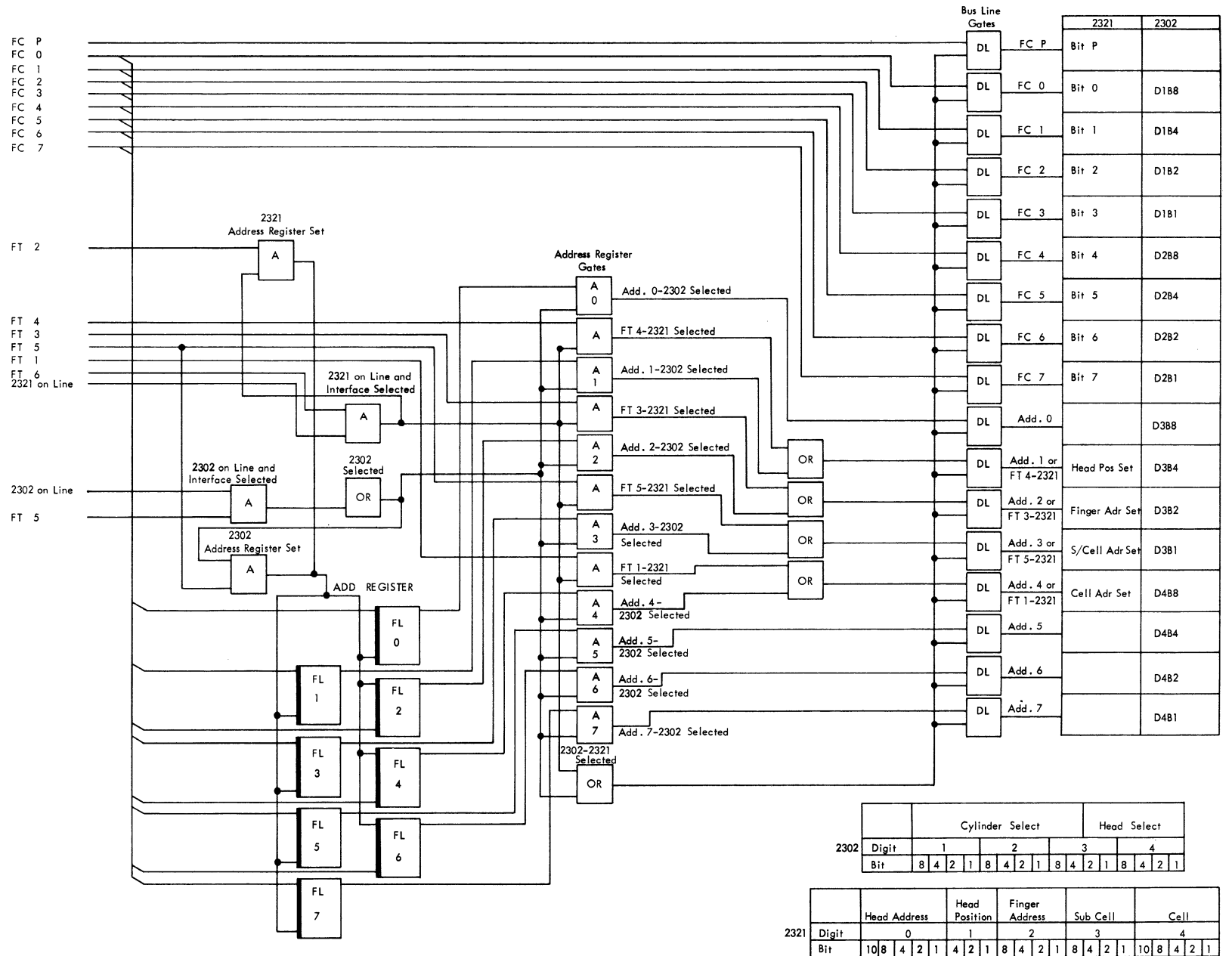
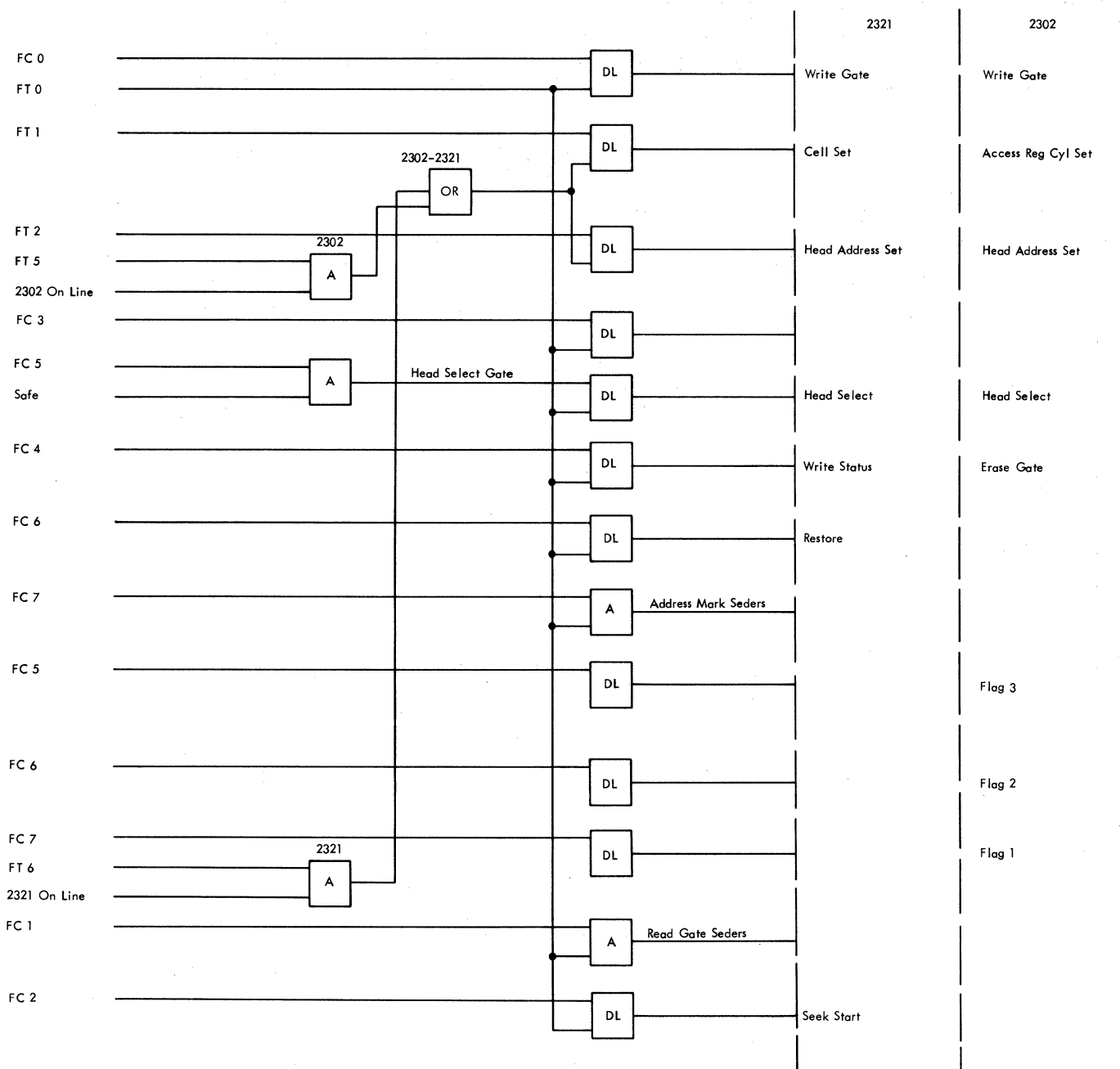
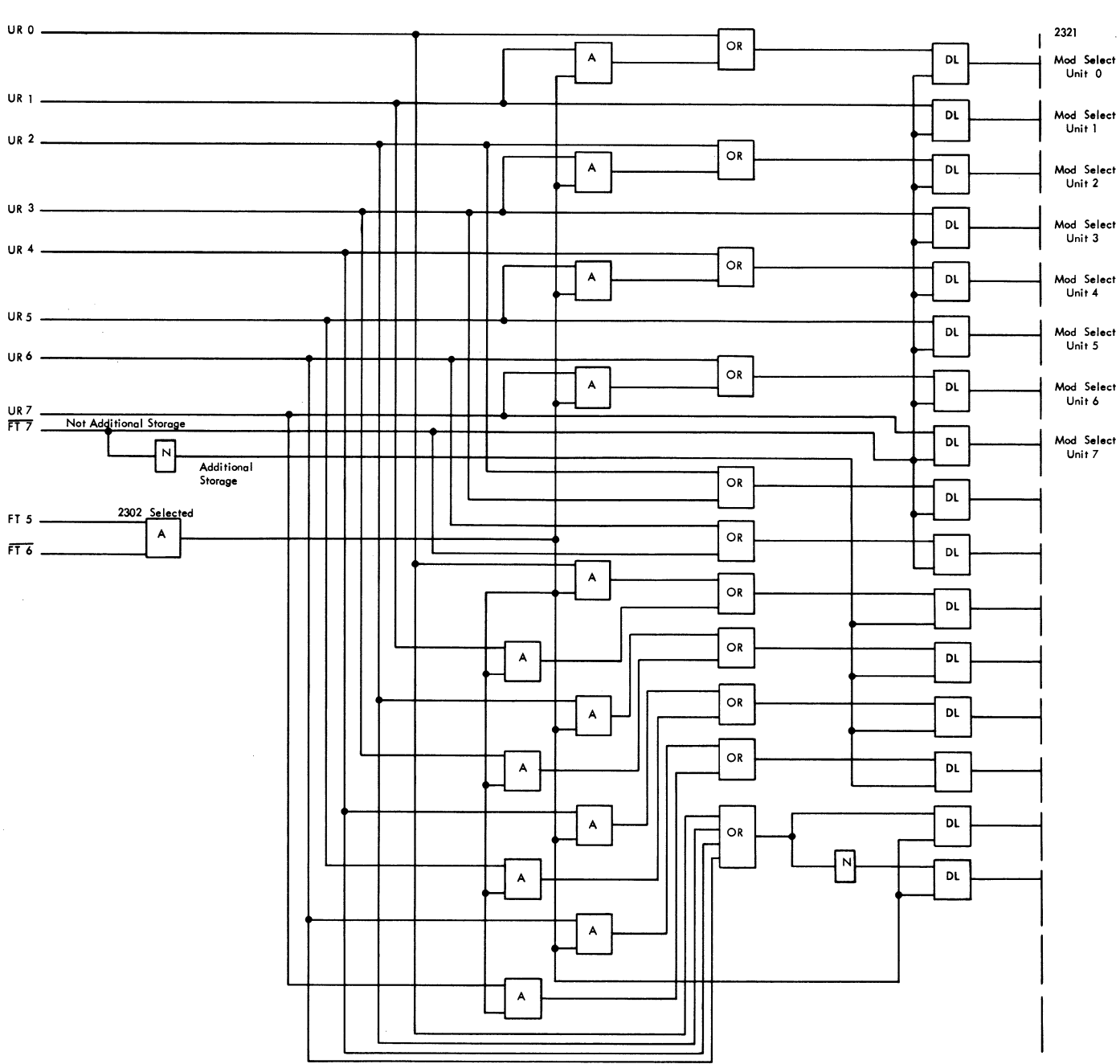


Figure 5-6. Address Register



22503A

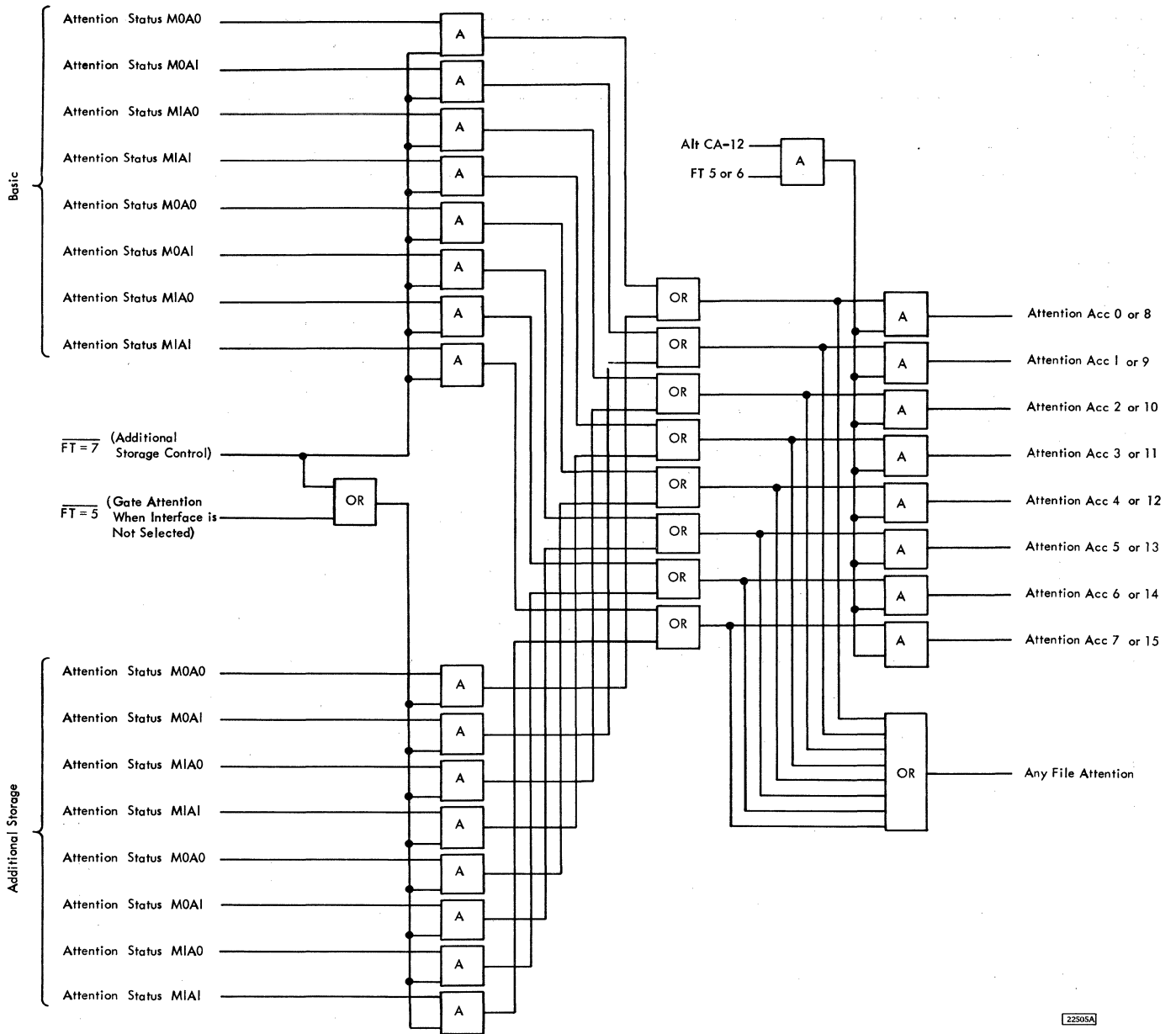
Figure 5-7. Device Control Gate



2302	
Model 3	Model 4
Mod 0 Unit 0	Mod 0 Unit 0
Mod 0 Unit 1	Mod 0 Unit 1
Mod 0 Unit 2	Mod 0 Unit 2
Mod 0 Unit 3	Mod 0 Unit 3
	Mod 1 Unit 0
	Mod 1 Unit 1
	Mod 0 Unit 2
	Mod 1 Unit 2
	Mod 0 Unit 3
	Mod 1 Unit 3
ACC 0	ACC 0
ACC 1	ACC 1

22504A

Figure 5-8. Module Select Gate



22505A

Figure 5-9. Seek Complete Gate

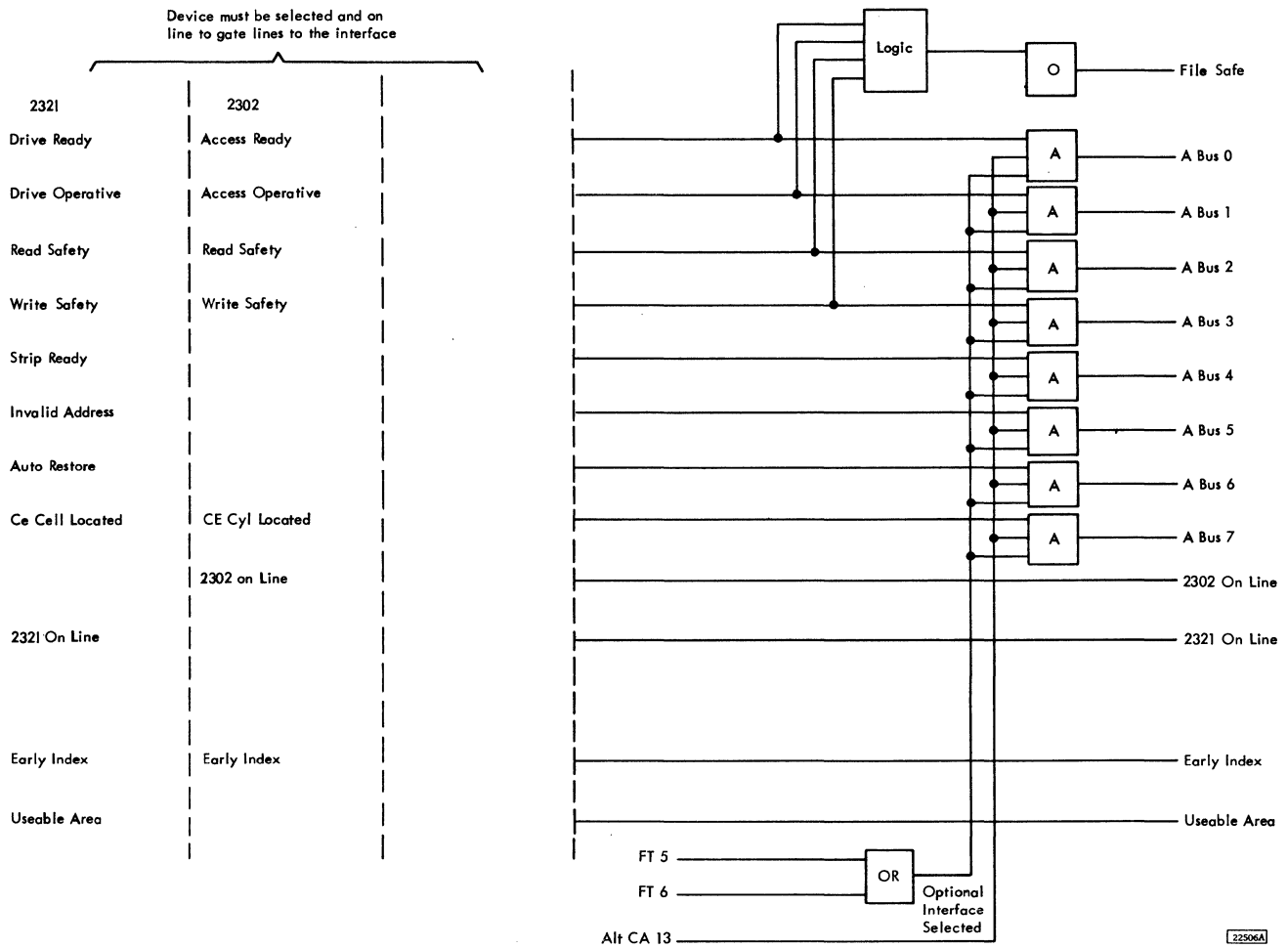


Figure 5-10. File Status

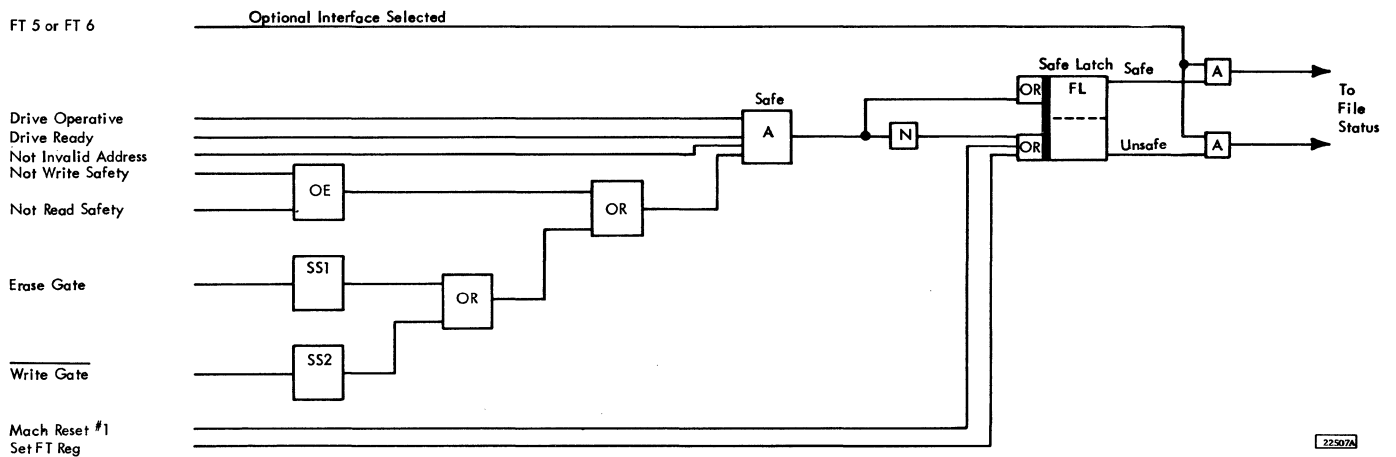


Figure 5-11. Fail Safe

The 2302-3 has two access mechanisms in each physical unit. Two consecutive access addresses must be assigned to each unit beginning with an even address (0-1, 2-3, 14-15).

The 2302-4 has four access mechanisms in each physical unit. Four consecutive access addresses must be assigned to each unit beginning with an address divisible by four (0, 1, 2, 3-12, 13, 14, 15).

It is presumed that there will be no more than one 2302-3 on a 2841. This is because one 2302-4 has the same functions as two 2302-3's for substantially less rental.

The hardware capability is:

1. Standard. A total of two physical 2302-3 or 2302-4 units attached to a 2841 in any of the following combinations:

2302-3	2302-4	Total Accesses
2	0	4
1	1	6
0	2	8

2. Standard plus Additional Storage Feature. A total of four physical 2302-3 or 2302-4 units attached to a 2841 in any of the following combinations:

2302-3	2302-4	Total Accesses
4	0	8
3	1	10
2	2	14
1	3	14
0	4	16

Two additional I/O connectors are added to the feature file connectors. They are addressed with a Module Select of 8 and 12 respectively.

As shown in Figure 5-8, the FT register bit 7 with the optional interface selected, gates the section of the additional accesses.

5.3 FILE SCAN FEATURE (Figures 5-12 and 5-13)

- The File Scan feature allows search operations on the Data field.

The File Scan function provides an automatic rapid search for a specific identifier or condition. The search applies to both the Key and Data Scan operation, a control mask consisting of bytes of information

on which a comparison is or is not to be made is placed in core storage. The bytes on which a comparison is not to be made are identified as a special configuration of bits (all one's). A Scan command must be given for each data field to be scanned.

This feature provides three new commands, each of which may be used in multitrack mode.

- Search Key - Data Equal (0010 1101)
- Search Key - Data High (0100 1101)
- Search Key - Data High or Equal (0110 1101)

If a logical comparison on equal is encountered, Channel End, Device End, and Status Modifier signals are generated. If a logical comparison is unequal, only Channel End and Device End signals are generated.

The length of the search is dependent upon the setting of the M/T bit of the Search Command and the sequence of commands given by the channel. If the M/T bit is a 1, the search continues until the specified condition is met or until the End-of-Cylinder is encountered. Should the M/T bit be a 0, the search continues until the condition is satisfied or until two Index Points are sensed at which time Unit Check (No Record Found), Channel End, and Device End signals are generated.

A KL of zero compares Data only to the core mask.

If the CCW Count is greater than (KL+DL), the Search operation is completed when (KL+DL) equals zero. The 2841 terminates the command with a Channel End and Device End. The Status Modifier is generated if the logical comparison was satisfied.

If a Bus Out Parity Error, Overrun, or Data Check is detected during a Search-Key and Data Equal operation, a Unit Check, Channel End, and Device End signal is generated at the completion of the command.

5.4 TWO-CHANNEL SWITCH FEATURE

- The Two-Channel Switch feature provides the circuitry required to attach the 2841 Storage Control to a second channel. Switching from one channel to the other is done electronically under program control.

The Two-Channel switch feature allows the 2841 Storage Control to be switched to either one of two channels or to a neutral position. (Figure 5-14)

The Channel Selection switch has three positions: Channel A, Channel B and neutral. When the switch is in the neutral position, the 2841 is selected by the first channel to complete the selection sequence. In the event both channels attempt to select the 2841 simultaneously, the tie is resolved by the switch logic.

Once the 2841 has been selected by a channel, it remains selected to that channel until ending status is presented. At that time the channel selection switch returns to neutral unless:

1. The channel indicates command chaining,
2. The last status byte was part of a channel-initiated signal sequence and was stacked by the channel,
3. The last status byte contained Unit Check, or
4. No command other than Test I/O or No Op has been initiated since condition (3) occurred.

While a channel connection is being maintained as a result of condition (3) or (4) above, the 2841 will not respond to polling by the channel except to present stacked status, or Control Unit End. Once this connection is terminated, the sense information is reset by any signal sequence other than Test I/O, Sense I/O, or No Op over either interface.

If Channel A (B) attempts to select the 2841 while the 2841 is selected to Channel B (A), the 2841 responds to Channel A (B) with the short Control-Unit-Busy sequence. (Under no circumstances will the 2841 post Control Unit Busy and Control Unit End in the same status byte.) This short Control-Unit Busy sequence may occur on any channel-initiated selection sequence (IPL, Test I/O, and all initial commands of a CCW chain).

Whenever the short Control-Unit-Busy sequence occurs, the 2841 attempts (by means of the Request In line) to present to Channel A (B) a status byte containing Control Unit End after the Channel Selection switch returns to the neutral position. The address byte associated with this status condition is the base address of the 2841 on that channel. This pending Control Unit condition, in itself, will not cause the 2841 to appear busy to Channel B (A) as long as the Channel Selection switch is not actually connected to Channel A (B)

Both Request-In lines may be up at one time if the Channel Selection switch is in the neutral position. The Request-In line on one channel is de-gated

whenever the Channel Selection switch is connected to the other channel.

The 2841 responds with Unit Check (Command Reject) to all commands in the sense group other than Sense I/O, Device Reserve or Device Release regardless of whether or not the Two-Channel Switch Feature is installed.

5.4.1 Device Reserve Command (1011 0100)

The Device Reserve command includes all of the functions of the Sense I/O Command, and in addition, causes the addressed device to become reserved to the channel issuing the command. Once a device becomes reserved to a channel, it remains reserved until that channel causes the 2841 to execute a Device Release command addressed to that device or to perform a system reset.

A Device Reserve command is executed regardless of any abnormal device status conditions such as off line, unsafe, etc.

A Device Reserve command which is preceded in the same command chain by a Set File Mask command is rejected with Unit Check (Command Reject and Invalid Sequence).

The Device Reserve command is rejected with Unit Check (Command Reject) by a 2841 which does not have the Two-Channel Switch Feature installed.

5.4.2 Device Release Command (1001 0100)

The Device Release Command includes all of the functions of the Sense I/O Command, and in addition, causes the reservation of the addressed device to be terminated.

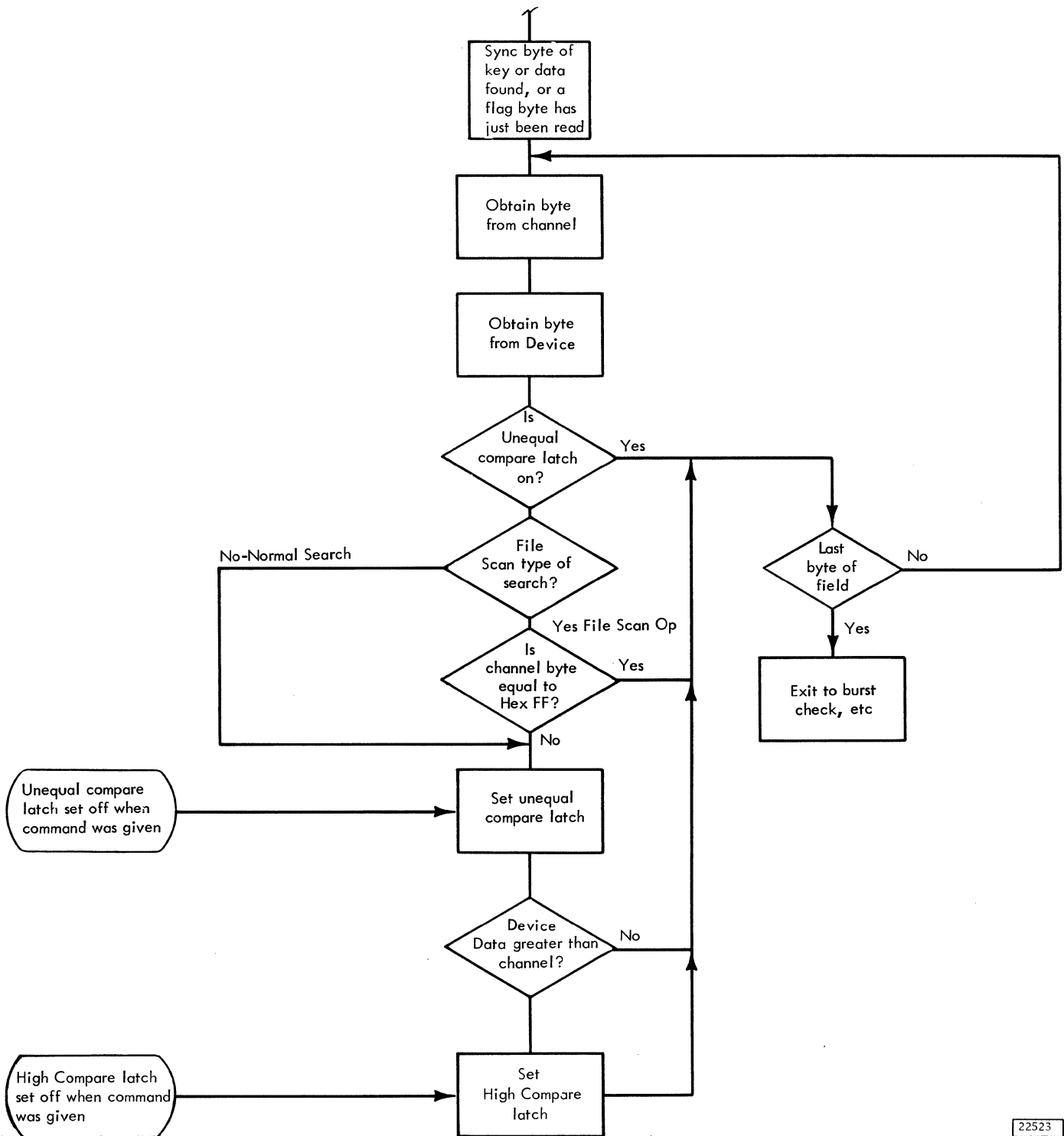
A Device Release Command is executed regardless of any abnormal device status conditions such as off line, unsafe, etc.

A Device Release command which is preceded in the same command chain by a Set File Mask command is rejected with Unit Check (Command Reject and Invalid Sequence).

The Device Release command is rejected with Unit Check (Command Reject) by a 2841 which does not have the Two-Channel Switch Feature installed.

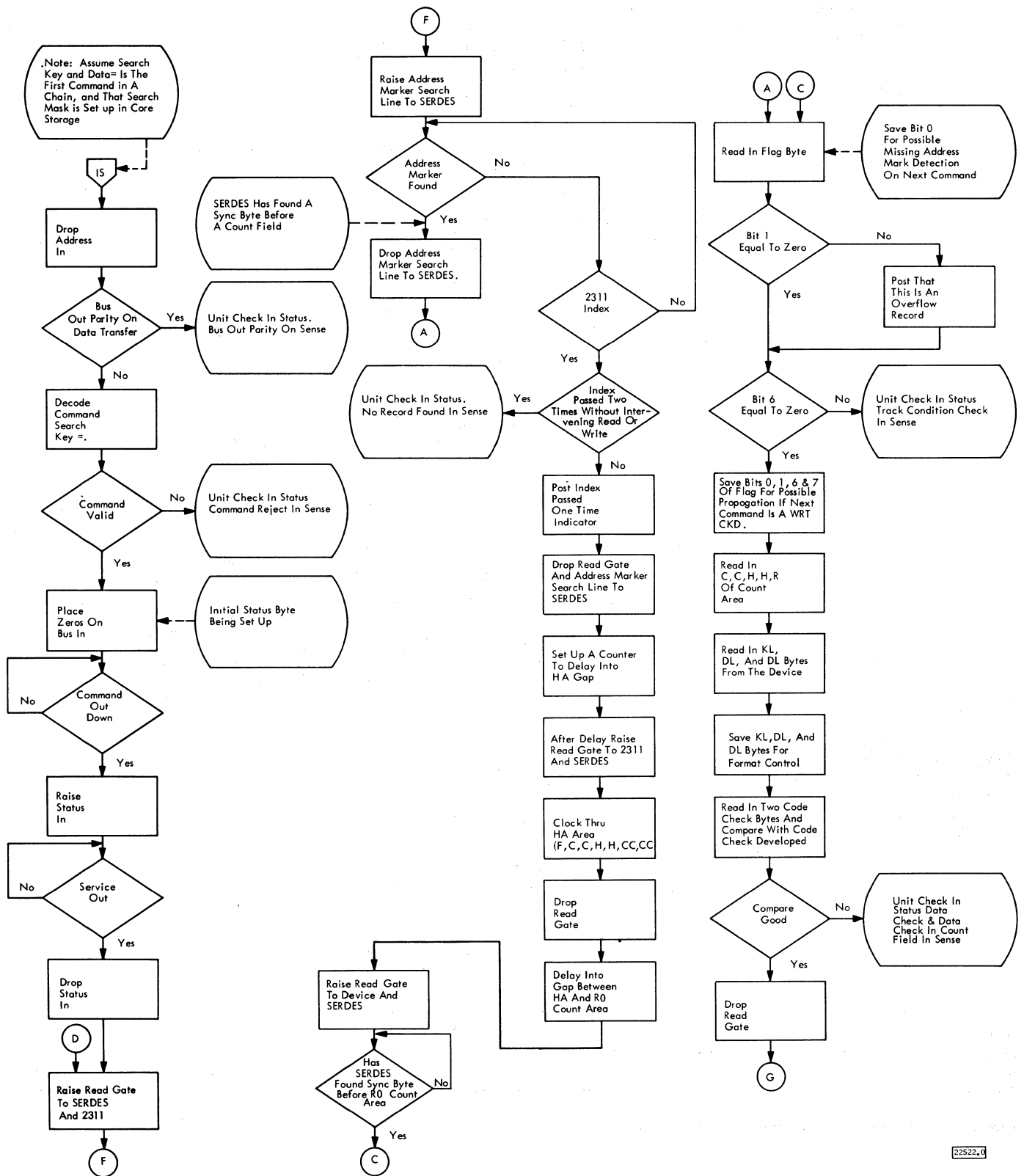
5.4.3 Device Status

Whenever a device is busy for any reason, including reservation to Channel A (B), any command from Channel B (A) addressed to that device is rejected



22523

Figure 5-13. Expansion of Search/Scan Data Compare Loop



22522-9

Figure 5-12. Search/Scan Key and Data Equal

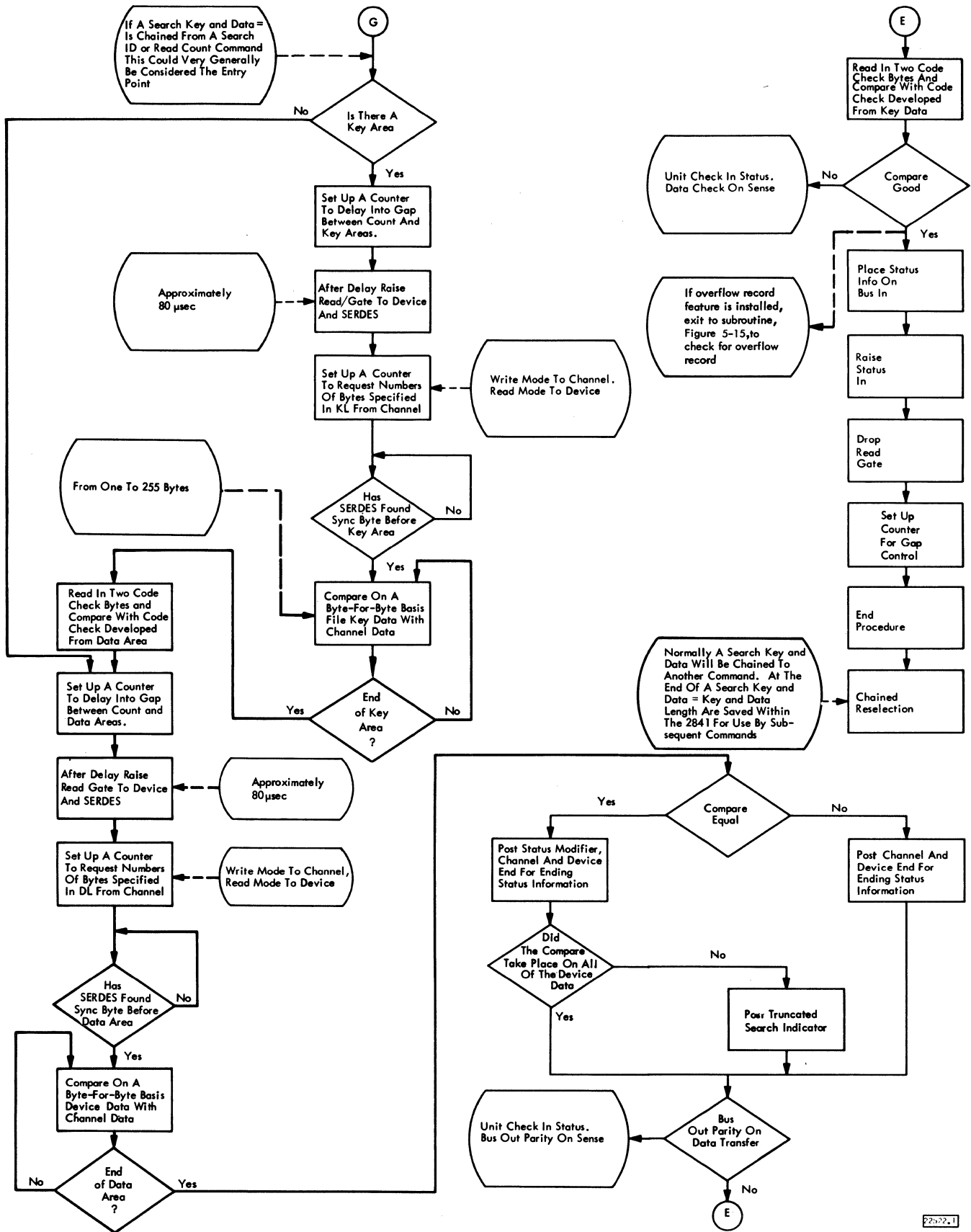


Figure 5-12. Search/Scan Key and Data Equal

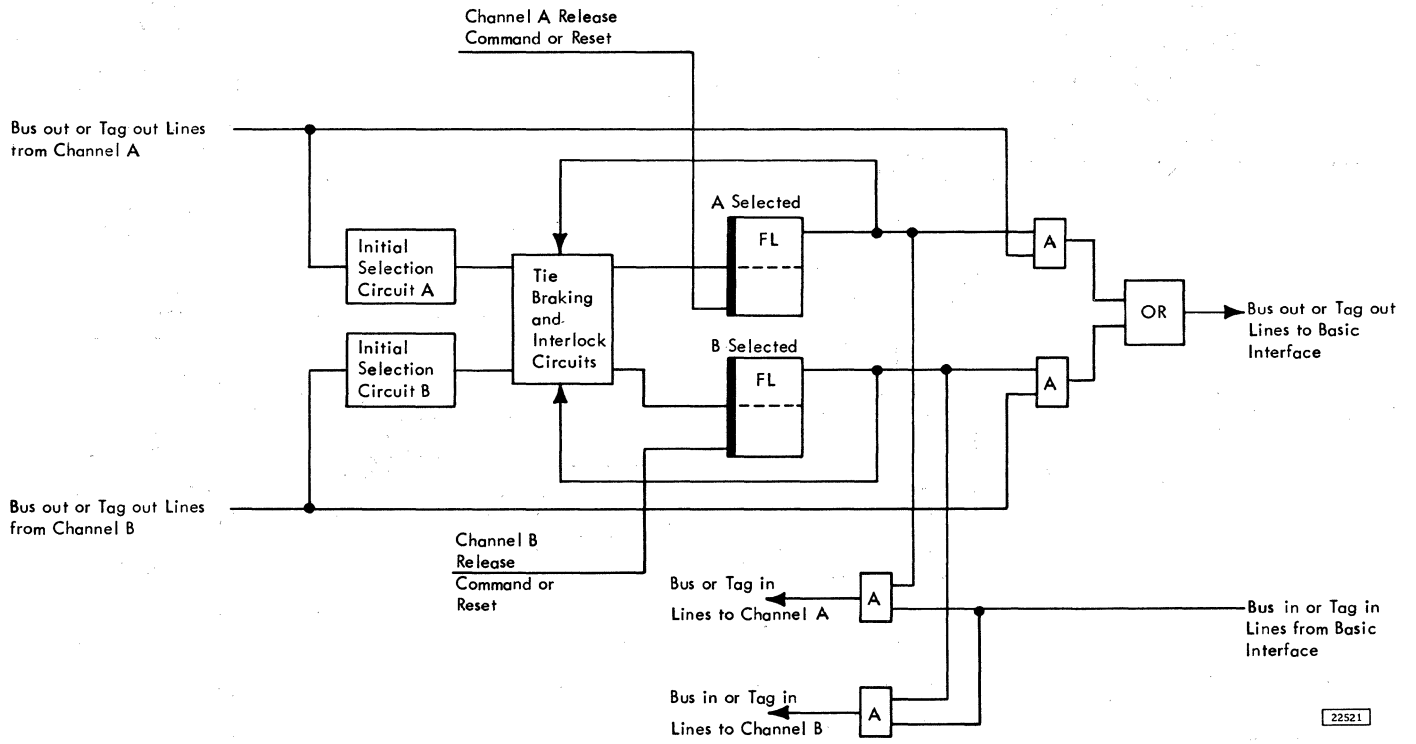


Figure 5-14. Two Channel Switch Data Flow

with Busy Status. This in turn, causes the 2841 to attempt (by means of the Request In line) to present to Channel B (A) a status byte containing Device End after the busy condition is terminated. The address byte associated with this status byte is the same as that associated with the Busy Status byte.

No Request In will be presented on Channel A (B), as long as the requesting device is reserved on Channel B (A).

Device End status resulting from any channel command which causes mechanical motion of an access is presented to the channel that issued the command.

Device End status resulting from a not-ready to ready transition is presented to both channels. Each channel must accept this Device End before it can use the device.

If, as a result of control unit-initiated switching, a channel stacks a status byte containing Device End or Control Unit End alone, the Channel Selection Switch returns to neutral and the control unit is not Control Unit Busy to other device addresses from either channel, but will attempt to present the stacked status again under control of Suppress Out.

5.4.4 Miscellaneous

5.4.4.1 Addressing

The base address (four high-order bits) of the 2841 on one channel is independent of the base address of the 2841 on the other channel. However, the four low-order address bits for any attached device must be the same on both channels. Bit position 4 of all device addresses must be zero.

5.4.4.2 System Reset

A system reset can be initiated by either channel at any time. A system reset causes all reservations and status conditions stored in the 2841 and related to the resetting channel to be reset. Reservations, operations, and status conditions related to the other channel will not be affected. Both channels may initiate system resets at the same time. If a channel initiates a system reset when the Channel Selection switch is not selected to the other channel, the 2841 performs a machine reset. A selective reset is effective only when the operational in tag is up at the channel interface. A selective reset has no effect on device reservations or status.

5.4.4.3 Interface Timing

Occasionally, an interface signal sequence may require more than 32 μsec . This cannot occur on any CCW following the first CCW in a chain. All signal sequences require less than 64 μsec . This is an exception to the interface definition.

5.4.4.4 Use Meter

A single usage meter records process time in the 2841; however, a separate meter Enable Switch is provided for each channel interface. These switches allow each interface to be disabled independently and provide a partitioning capability. While in the disabled state, an interface always propagates Select-Out and cannot raise any inbound Tag line. In order to disable a channel interface, the following conditions must exist:

1. The Enable Switch for that channel must be in the Disable position,
2. The channel selection switch in the 2841 must not be selected to that channel, and
3. The Clock Out line from that channel must be down.

In order to allow a channel interface to return to the enabled state, the following conditions must exist:

1. The Enable Switch for that channel must be in the Enable position, and
2. The Clock Out line from that channel must be down.

Programming Note: If a CPU is allowed to enter the Stopped or Wait state when the 2841 contains outstanding status, the status may be made unavailable if the meter Enable Switch has previously been set to Disable.

The Clock Out line to the attached devices will be up if either interface is enabled and has Clock Out up.

5.4.4.5 Power Control

A power control interface is provided for each channel. If either channel indicates power On, the 2841 turns on. The 2841 will turn off only if both channels indicate power Off. The normal CE power control is available as described in Chapter 4.

The emergency power off (EPO) lines from both channels must be dropped in order to release the 2841 EPO relay. The dropping of the EPO lines is controlled by channel power control circuit externally of the 2841.

5.4.5 Two Channel Switch Circuit Description

Figure 5-14 shows the data flow of the two channel switch. All lines to or from the channels are gated between the channels and the basic interface.

Initial Selection circuits for each channel, control the circuits to prevent both A and B channel selection triggers from being set on at the same time. When one of the Select triggers is on, the other channel cannot select the 2841 until the first channel releases the 2841. The trigger that is on gates the lines to and from that channel.

When both triggers are off, the switch is in the neutral position and may be selected by either channel.

When the Two Channel Switch feature is installed in the 2841, an additional general purpose register (SW) is added. The SW register is used to indicate to the micro program the status of each device as it applies to channels A and B. Meanings of the bits are shown on CLD QA 008.

5.5 RECORD OVERFLOW FEATURE

- The Record Overflow feature allows a logical record to be more than one track in length.

The Record Overflow feature allows a logical record to overflow from one track to another. Record Overflow is useful in achieving a greater data packing efficiency and in formatting records which exceed the capacity of a track. The limiting factor in the size of a record which can be overflowed is the cylinder boundary.

5.5.1 Formatting Overflow Records (Figure 5-15)

The portion of an overflow record which is written on one track is called a record segment. Each record segment is processed as a normal record during Format Write operations. The Write Special CKD CCW (0000 0001) is the command used for formatting all segments of an overflow record except for the last segment. The last segment is written by the normal Write CKD CCW.

The Write Special CKD CCW causes a 1-bit to be written in bit position one of the Flag Byte of the record segment being written. Otherwise, the Write Special CKD CCW functions just like the normal Write CKD CCW. Note that a Write Special CKD CCW is not a valid prerequisite for a normal Write CKD CCW and results in the record flagged as a segment of an overflow record being the last record on a track.

When formatting overflow records, all segments other than the first must be recorded in the first record "bucket" following the R0 record on a track.

All segments, other than the first segment, are normally recorded without a Key Field, since only the Key Field of the first segment has significance.

All segments of an overflow record, other than the first and the last segments, are the only records on the track following the R0 record.

An overflow record may be formatted with a sequence of CCW's similar to the following. This sequence assumes that a Set File Mask instruction was performed prior to the initiation of the Scan Sequence.

- | | |
|----------------------|--|
| 1. Seek | Position access mechanism and select head. |
| 2. Search ID | Determine beginning location. |
| 3. Write Special CKD | Write first segment. |
| 4. Seek Head | Select next head. |
| 5. Search H.A. or R0 | Locate next record. |
| 6. Write CKD | Write last segment. |

Items 3, 4 and 5 are repeated as often as needed.

5.5.2 Processing Overflow Records

The Read Data, Read Key and Data, Read Count-Key and Data, Write Data, Write Key and Data CCW's operate on an overflow record as though it were a normal record.

The 2841 detects that bit position one in the Flag Byte is a one bit. After completing the read or write operation in the first segment, the 2841 causes a search for the Index Point. At Index Point, the next sequential Head is selected and a comparison of Head number in the Home Address is done. If the comparison is equal, the 2841 searches for the first Address Marker on the track. Then, under control of the data count in the Count Field, it processes the Data Field of this record segment. This operation continues

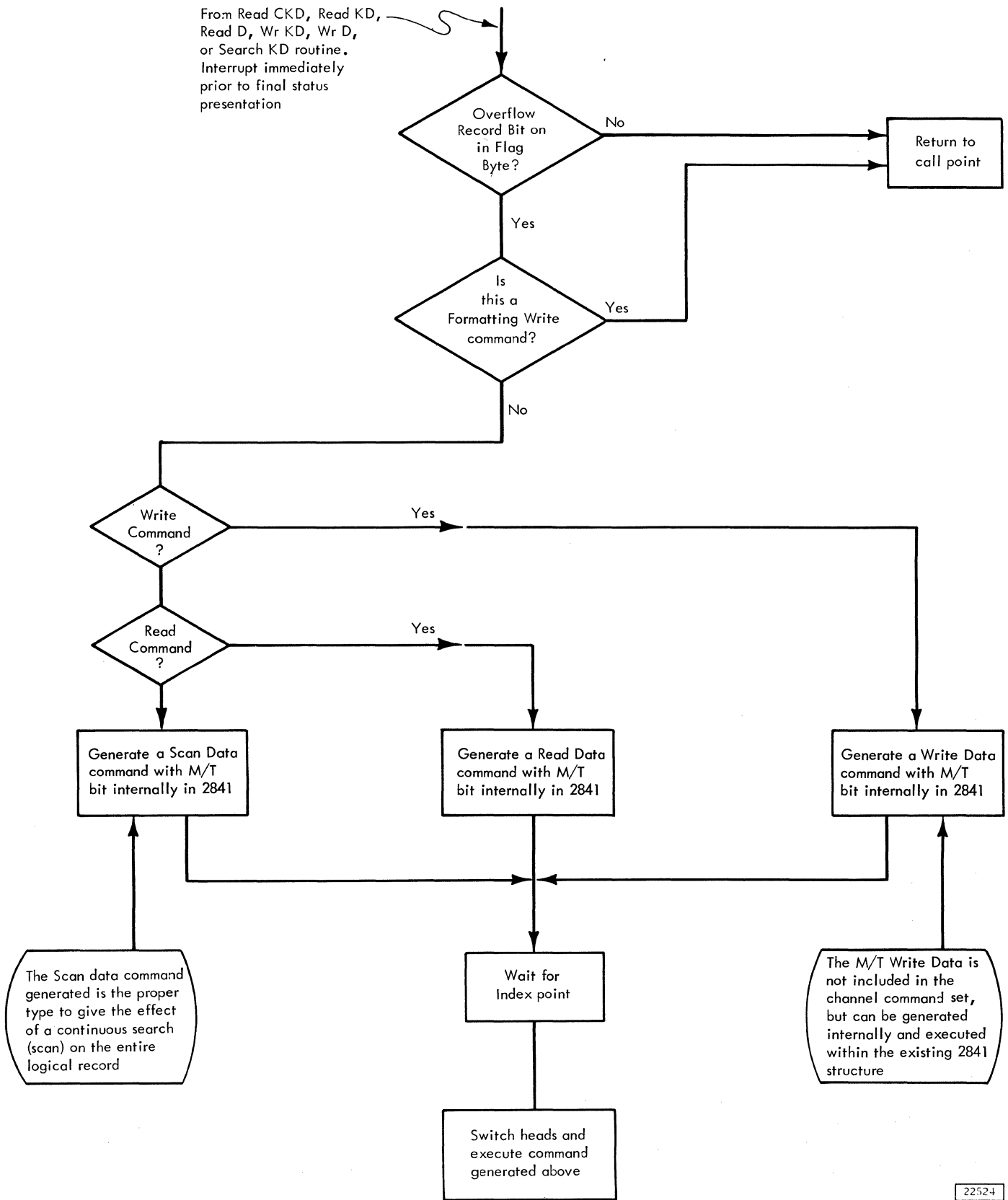


Figure 5-15. Execution of Commands with Overflow Record Feature

until the 2841 detects a record segment which contains a zero bit in bit position one of the Flag Byte. At the end of this record segment, the operation is terminated.

Only the Data Fields of all record segments except the first segment are processed when reading or writing. (i.e., Read CKD reads CKD of the first segment and data only of all other segments.) A CCW chain which starts operation on a record segment other than the first segment is processed as though it started on the first segment. This type of operation may make it desirable to repeat the Key Field in all record segments if the chain of CCW's is dependent on a satisfied Search Key Equal.

Search ID, Search Key and Read Count CCW's operate on each record segment as though each segment were a normal record.

5.5.3 Unusual Conditions

In addition to the checks provided in normal processing of any record, certain conditions can occur which are unique to overflow records. The commands stop immediately on detecting the following conditions:

Overflow To a Bad Track. Overflow Incomplete and Track Condition occur when overflowing to a track which has been flagged as being bad and two additional sense bytes, Bytes 4 and 5, are presented to the channel.

1. Byte 4 - This byte is all zeroes. It is a dummy byte inserted for control unit compatibility of byte 5 with other control units.
2. Byte 5 - This byte is zero at all times except when overflow incomplete occurs (Byte 1, Bit 7). When overflow incomplete occurs, this byte has one of the following configurations.
 - 00000110 - A read command was in progress when the overflow incomplete interrupt occurred.
 - 00000101 - A non-formatting write command was in progress.
 - 00100101 - A search key-data equal command was in progress, and the compare was equal to this point.

01000101 - A search key-data high command was in progress, and the compare was equal to this point.

01100101 - A search key-data high or equal command was in progress, and the compare was equal to this point.

01010101 - Any search key-data was in progress and the compare was low, or a search equal key-data was in progress and the compare is unequal to this point. (i.e., it has already been determined that no Status Modifier would be set in the entire logical record.)

01110101 - A search high or high-equal key data command was in progress, and the compare was high to this point. (i.e., It has already been determined that a status modifier would be set in the logical record.)

Byte 5 is used by programming systems to resume the scan loop after seeking to a new track.

Overflow From an Alternate Track. Overflow Incomplete and Track Condition Check sense bits are set if an attempt is made to overflow from a track flagged as an alternate.

Overflow to a File Protected Boundary. Attempting to overflow in violation of a file mask sets Overflow Incomplete, File Protected, and Command Reject sense bits.

Overflow to a Track with Incorrect Head Number. Overflow Incomplete and Command Reject sense bits are set if the Head number compare is unequal during an overflow. This condition occurs if the last Seek Address issued to the 2841 is not the address of the track with the overflow record and an overflow record is being read or written.

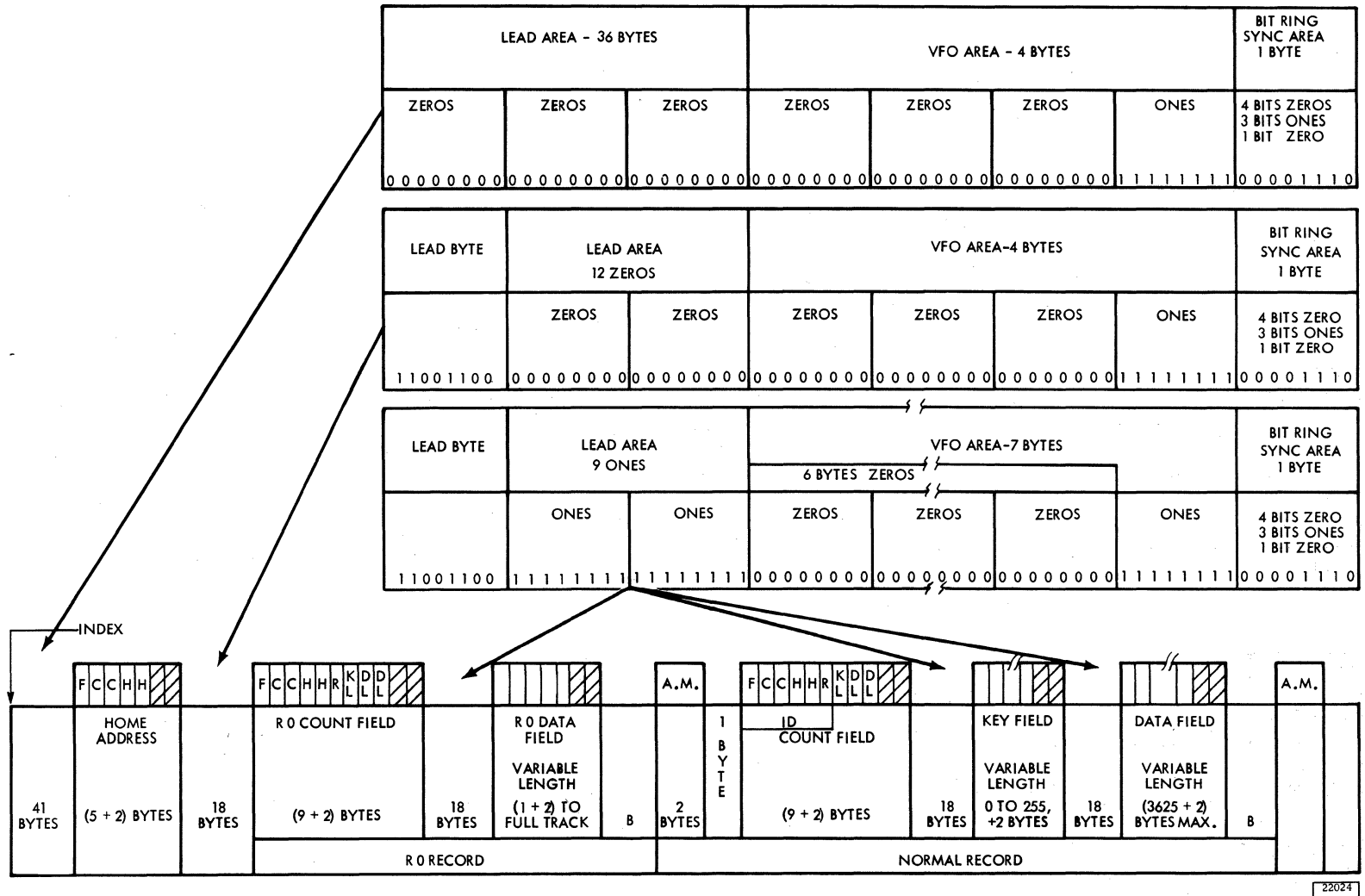


Figure 5-16. HA or Alpha Gap Bit Configuration - 2302

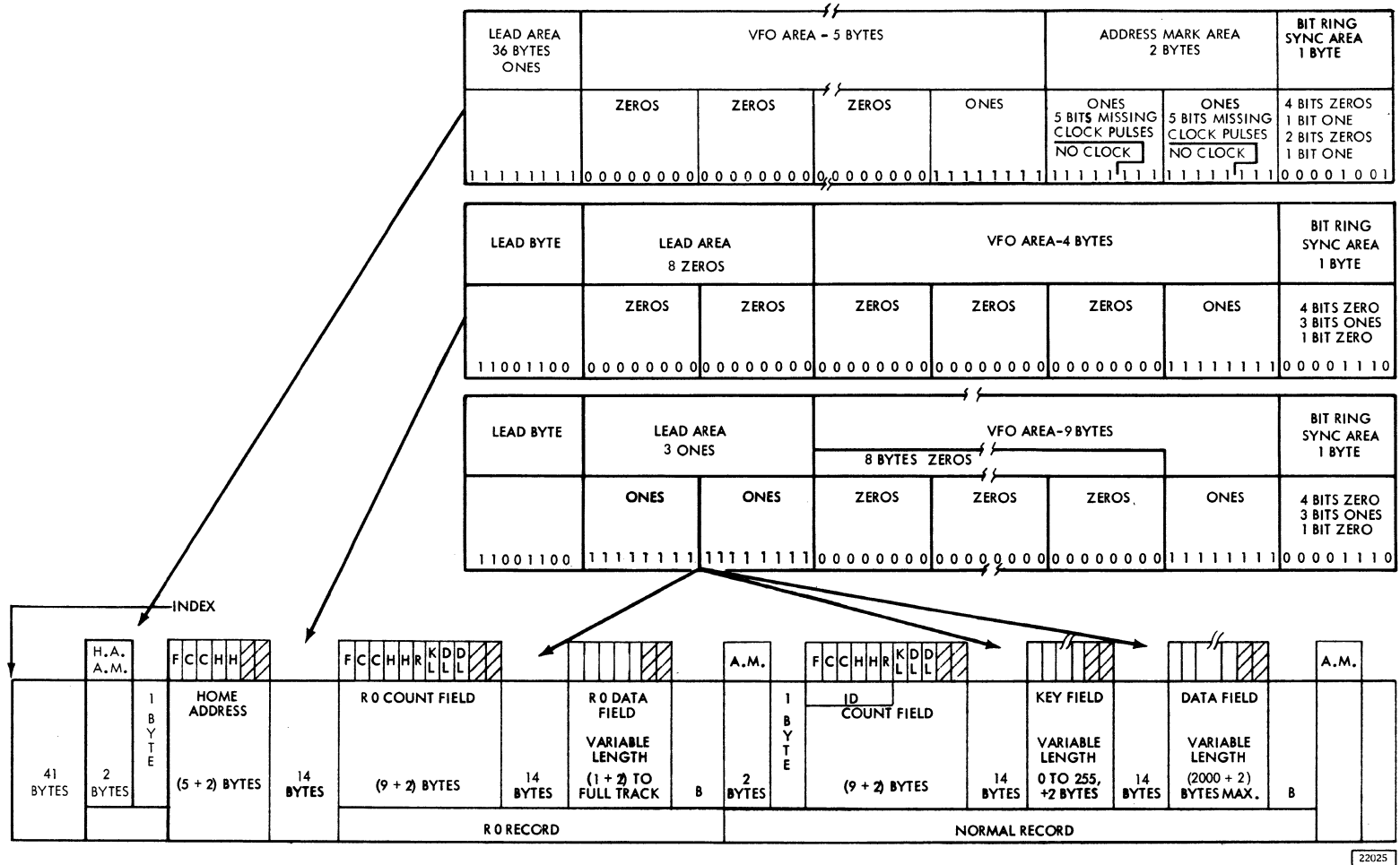


Figure 5-17. HA or Alpha Gap Bit Configuration - 2321

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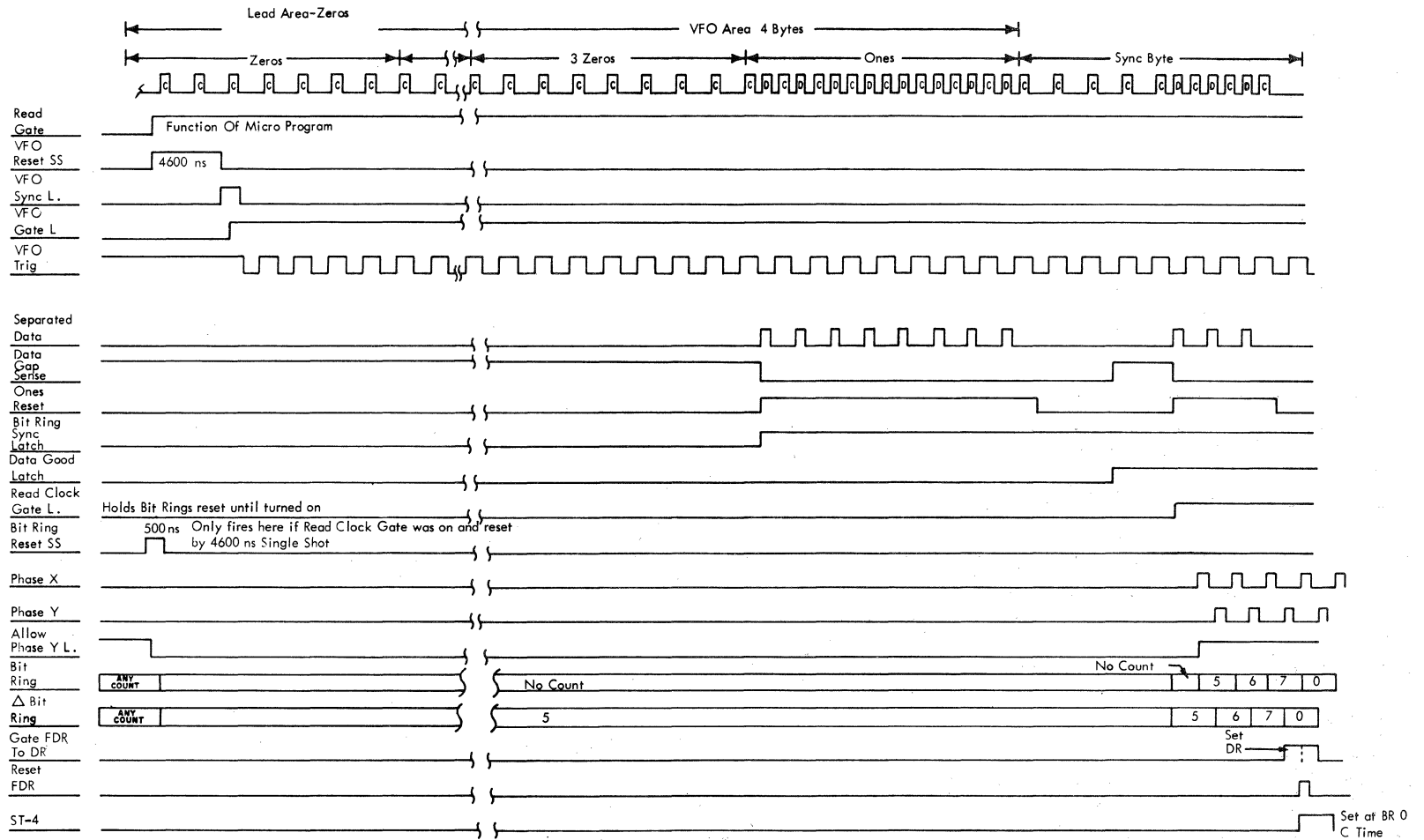


Figure 5-18. HA or Alpha Gap Timing Diagram - 2321

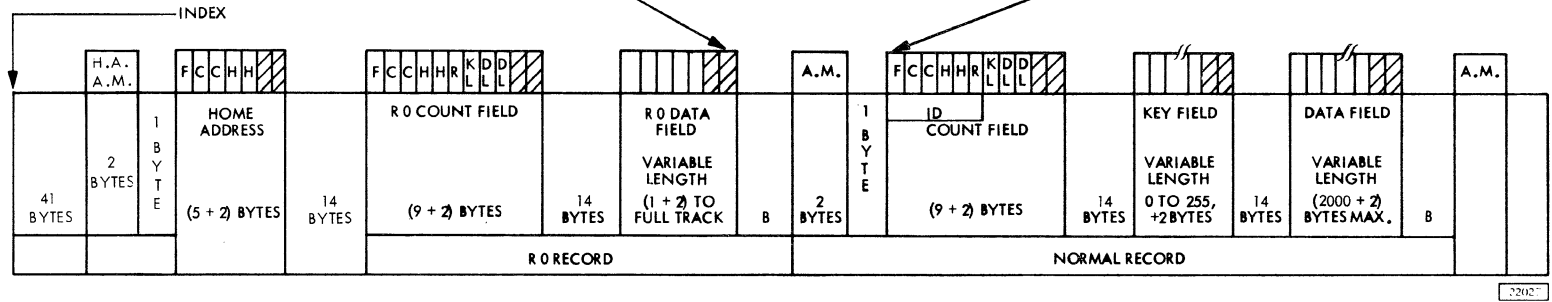
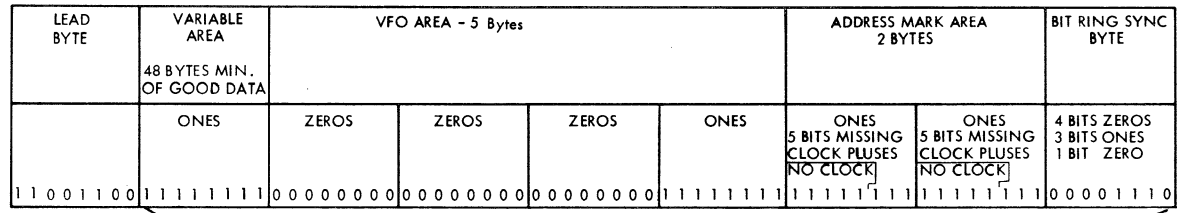


Figure 5-19. Beta Gap Bit Configuration - 2321

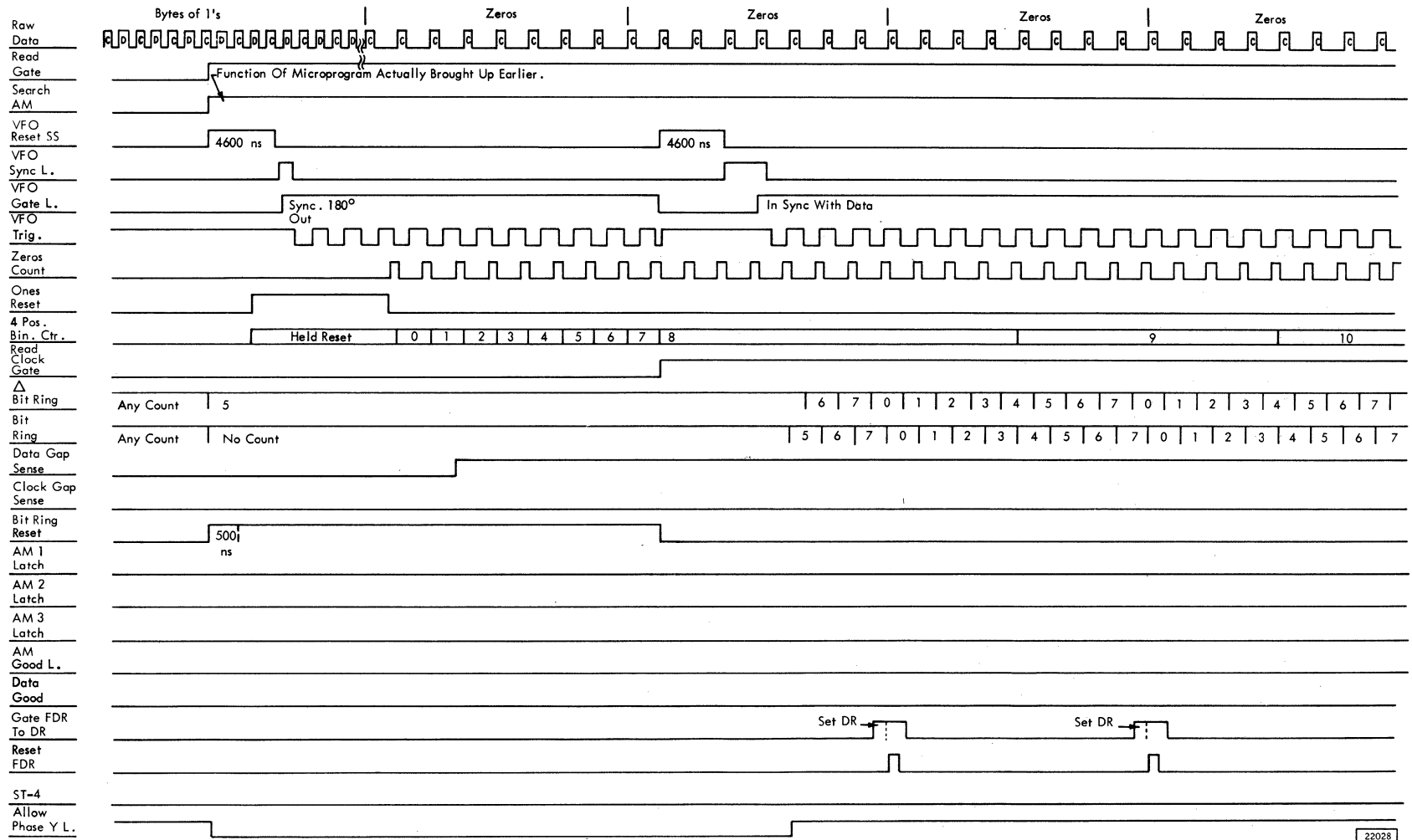


Figure 5-20a. Beta Gap Timing Diagram Sheet 1 - 2321

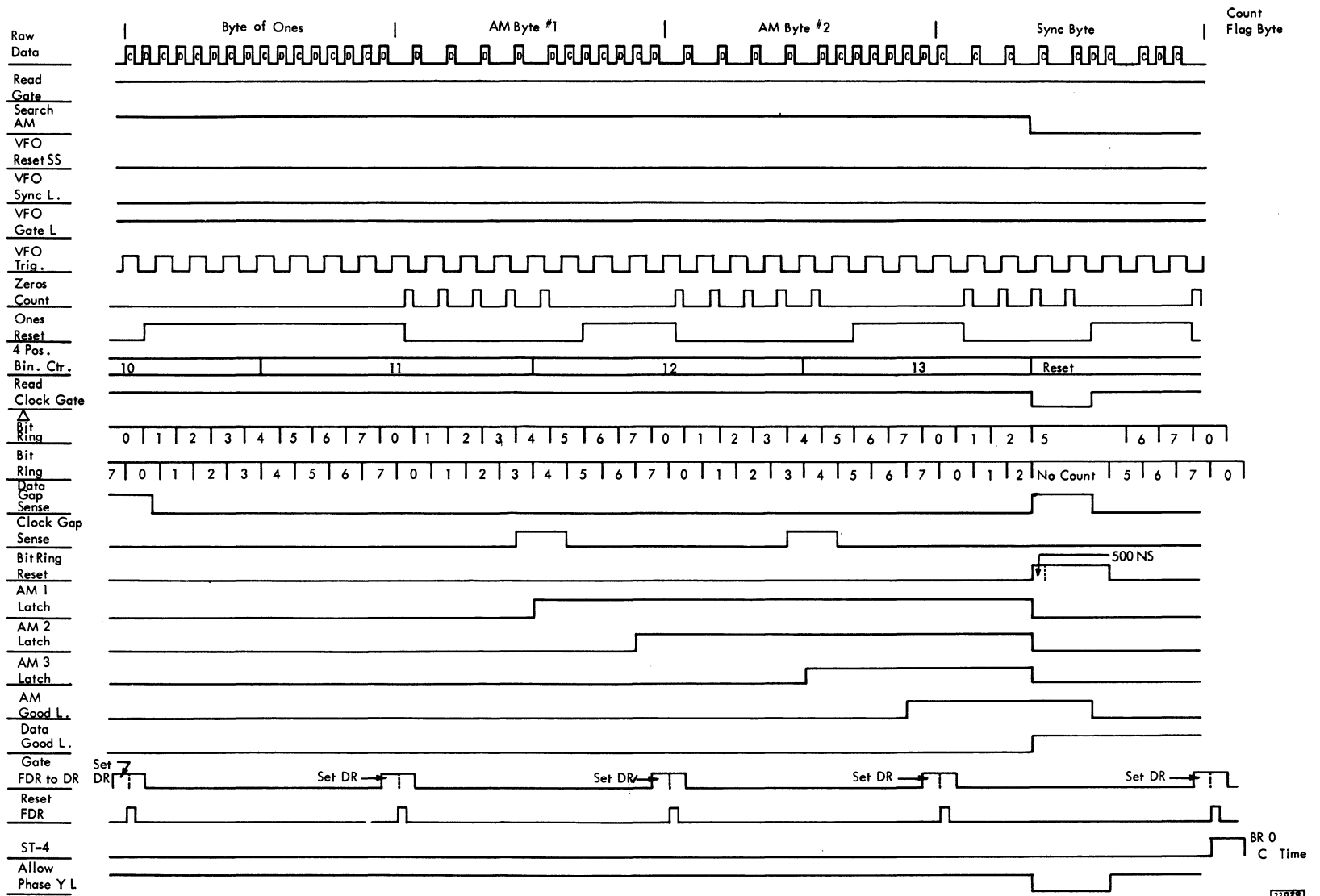


Figure 5-20b. Beta Gap Timing Diagram Sheet 2 - 2321

6.1 CAS I

6.1.1 TROS Bit Assignment Chart (Figure 6-1)

The TROS word is divided into 15 control fields. Each one of these fields performs a particular function during one machine cycle. A description follows:

6.1.1.1 CN

The value contained in CN is loaded into the six high order bits of the X register. In addition, CN-5 is used as the data source when loading the FT register, FC register and the IG register, bits 3 and 4.

6.1.1.2 PN

PN is a parity bit for the CN and PN fields. Total parity should be odd.

6.1.1.3 CD

The value contained in this field gates the output of ALU (A Register if Bypass bit on) to one of seventeen destinations (i.e., CD=7 gates the output of ALU to the DH register).

NOTE: Even though the data was loaded into a register, it is still on the D Bus and can be tested by the micro program. CD=0 means to place the output of ALU on the D Bus only.

6.1.1.4 CV

The value contained in CV determines if the B register is gated in True or Ones Complement to ALU.

6.1.1.5 CC

The value contained in CC determines the ALU operation. There are eight different ALU statements. Five different symbols are used to indicate the arithmetic operation:

- + ADD
- SUBTRACT
- * AND
- v OR
- Δ EXCLUSIVE OR

CC=0: Add or Subtract (CV) the A and B-register outputs. Carry In of zero to the low order ALU position. Example: $DH=KL+BY+0$

CC=1: Add or Subtract (CV) the A and B-register outputs. Carry In of one to the low order ALU position. Example: $DH=KL+BY+1$

CC=2: AND the A and B-register outputs. Example: $DH = KL*BY$

CC=3: OR the A and B-register outputs. Example: $DH=KLVBY$

CC=4: Add or Subtract (CV) the A and B register outputs. Carry In of zero to the low order ALU position. If there is a Carry Out of the high order ALU position, set ST(3). Example: $DHC=KL+BY+0$

CC=5: Add or Subtract (CV) the A and B register outputs. Carry In of one to the low order ALU position. Carry Out, set ST(3). No Carry Out, reset ST(3). Example: $DHC=KL+BY+1$

CC=6: Add or Subtract (CV) the A and B register outputs. Use the present condition of ST(3) as a Carry In to the low order position of ALU. If there is a Carry Out, set ST(3). No Carry Out, reset ST(3). Example: $DHC=KL+BY+C$

CC=7: Exclusive OR the A and B-register outputs. Example: $DH=KLBY$

6.1.1.6 CS

The value contained in this field controls the setting and resetting of individual bits in the status register; i.e., CS=6 means if the D Bus does not equal zero, set ST(2) to a one. The only way to turn ST(2) off is a CS=5 statement.

6.1.1.7 PC

PC is the parity bit for CV, CS, CD, CC, BY and PC fields. Total parity should be odd.

6.1.1.8 PS

PS is the parity bit for CA, CB, CK, CH, CL, PA and PS fields. Total parity should be odd.

6.1.1.9 BY

The value contained in BY determines whether the ALU or A-register output is placed on the D Bus. With this bit on, a parity check of the A-register P bit and the ALU generated P bit is made. An error hard stops the 2841 with the Data Check lamp on. Example: (DH=KL+0, D=A)

6.1.1.10 CH

The value contained in CH allows a particular condition in the machine to be tested. The X-register 6 is set or reset depending upon the result of the test. A summary of CH branching conditions follows:

CH=0: Set X 6 off.

CH=1: Set X 6 on.

CH=3, D, E, or F - Test an OP register bit. If it is on, set X 6, if not, reset X 6.

CH=2, 4, 5, or 6 - Test a ST-register bit. If it is on, set X 6, if not, reset X 6.

CH=7: Test CT-7 (Initial Select or Polling Interrupt). If it is on set X 6, if not reset X 6.

CH=8: Reset X 6. Gate bits 3, 4, 5, 6, and 7 of the CK field to the W-register if the microblock contains a W=CK statement.

CH=9: Test the ALU Carry Out latch. If on, set X 6, if not, reset X 6.

CH=A: Test CT-2 (Command Out). If on set X 6, if not, reset X 6.

CH=B: Test CT-4 (Suppress Out). If on, set X 6, if not, reset X 6.

CH=C: Test CT-6 (Address Out). If on, set X 6, if not, reset X 6.

6.1.1.11 CL

The value contained in CL allows a particular condition in the machine to be tested. X-register 7 is set or reset depending upon the result of the test. A summary of CL branching conditions follows:

CL=0: Set X 7 off.

CL=1: Set X 7 on.

CL=2, 3, or 4: Test a ST-register bit. If on, set X 7, if off, reset X 7.

CL=5: Test the ALU, D=0 latch. If on, set X 7, if off, reset X 7.

CL=6: Do not gate CN 0-5 and the results of the CH and CL branch tests to the X-register. Instead, gate the contents of the A bus to the X-register. This statement should only be used when the address compare switch is in the SCAN position, since it actually gives a 256-way branch.

CL=8: Test CT(1) (Service Out). If it is on, set X 7, if off, reset X 7.

CL=9: Test CT(3) (Service-Out Response). If it is on, set X 7, if off, reset X 7.

CL=A: Test CT(5) (Select Out). If it is on, set X 7, if off, reset X 7.

CL=B, C, D, or F: Test an OP register bit. If on, set X 7, if off, reset X 7.

CL=E: Test for Index. If Index, set X 7, if not, reset X 7.

NOTE: Before Index can be gated to the CL Branching Circuits, the micro program must allow Index by issuing the CS statement ST(1)1.

6.1.1.12 CA

The value contained in CA gates a particular source to the A Bus. i.e. CA=0 places zero on the A Bus, CA=13 places the contents of ER on the A Bus.

CA=17, STOP, is a special use of the CA field. This statement is used in the microdiagnostics. The Check Stop/Run switch in the Check Stop position and the Stop statement stops the 2841. Refer to ALU microdiagnostic for examples of the Stop statement.

6.1.1.13 CB

The value contained in CB gates a particular source to the B Bus. i.e. CB=0 places zero on the B Bus. CB=3 places the contents of DR on the B Bus.

6.1.1.14 CK

The value in the CK field may be used as a constant source by the micro program. i.e. DL=KL+9. The nine is in the B entry position in the ALU statement.

Figure 6-1. CASI - TROS Bit Assignment Chart

Value	Field	CN	PN	CD	CV	CC	CS	PC	PS	BY	CH	CL	CA	CB	CK	PA
10	16	Bits	0 1 2 3 4 5	0 1 2 3 4		0 1 2	0 1 2 3				0 1 2 3	0 1 2 3	0 1 2 3 4	0 1	0 1 2 3 4 5 6 7	
0	0	To "X" Reg		"D" Bus	True	Add/Sub. CI = 0	No. Oper.			Alu To D	X 6 To 0	X 7 To 0	Zero	Zero	To "B" Reg Or "W" Reg	
1	1	0-5		GL	Comp	Add/Sub. CI = 1	ST (0) 0			"A" Reg To D	X 6 To 1	X 7 To 1	GL	BY		
2	2	CN-5 Also Used As		BY		And	ST (0) 1				ST (0)	ST (3)	BY	CK		
3	3	Data Input To FT & FC		BX		Or	ST (1) 0				OP (6) 1	ST (5)	BX	DR		
4	4	& IG, Bits 3 & 4		FR		Add/Sub. CI=0 ST (3) = CO	ST (1) 1				ST (2)	ST (7)	FR			
5	5			KL		Add/Sub. CI=1 ST (3) = CO	ST (2) 0				ST (4)	DOX 71	KL			
6	6			DL		Add/Sub. CI= ST(3),ST(3)=CO	DN ST 21				ST (6)	X=A	DL			
7	7			DH		Exclusive Or	ST (3) 0				CT (7)	Not Used	DH			
8	8			OP			ST (3) 1				W=CK X6 To 0	CT (1)	OP			
9	9			GP			ST (4) 0				CO	CT (3)	GP			
10	A			UR			ST (5) 0				CT (2)	CT (5)	UR			
11	B			DW			ST (5) 1				CT (4)	OP (1)	DW			
12	C			DR			ST (6) 0				CT (6)	OP (3)	DR			
13	D			FT			ST (6) 1				OP (0)	OP (5)	ER			
14	E			FC			ST (7) 0				OP (2)	ST (1)	IE			
15	F			IG			ST (7) 1				OP (4)	OP (7)	IH			
16	10			SW									SW			
17	11										Set X 6 To One	Set X 7 To One	Stop*			
18	12										If Condition	If Condition				
19	13										Checked Is On.	Checked Is On.				
20	14															
21	15															
22	16															
23	17															
24	18															
25	19															
26	1A															
27	1B															
28	1C												SC			
29	1D												FS			
30	1E												OA			
31	1F												IS			

* Diagnostic Use Only

To gate CK to the B Bus, it is necessary to make the CB field equal 2.

Bits 3, 4, 5, 6, and 7 may also be gated to the W-register module switching in TROS. This is accomplished by making the CH field 8 and issuing a W=CK (i.e. W=3) statement.

6.1.1.15 PA

PA is the parity bit for the combined W and X-registers, for example:

W					X									
P	4	5	6	7	P	0	1	2	3	4	5	6	7	Hexadecimal Address 58B
1	0	1	0	1	1	1	0	0	0	1	0	1	1	

The sum of the bits is even, therefore, PA is punched for a one in the TROS tape.

6.1.2 Microblock Symbology.

- The microblock is divided into eight lines of information.
- Each line defines a particular function of the machine.

6.1.2.1 Line 1 (Figure 6-2)

Line 1 contains the symbolic and hexadecimal addresses of the microblock. The Symbolic Address consists of five characters as follows:

1	2	3	4	5
A	B	C	X	X

1. Character one is an alphabetic character
2. Character two is an alphabetic character
3. Character three can be either alphabetic, a zero, or a one.
4. Characters four and five may be X, zero, or one.

Alphabetic characters I, O, and U are not used in character three position.

The Hexadecimal Address consists of three digits. i.e. 40A. The first digit represents the value set in the W-register. The next two digits represent the value set in the X-register.

6.1.2.2 Line 2

Line 2 is not used.

6.1.2.3 Line 3

Line 3 can be used for some appropriate statement concerning the function of the micro block.

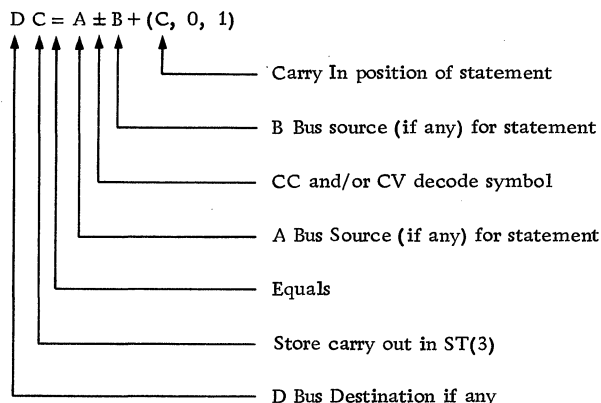
6.1.2.4 Line 4

Line 4 will contain a module switching statement when the micro program switches from one TROS module to another. An example of this is W=4. This means set the W-register to module 4.

6.1.2.5 Line 5

Line 5 contains the ALU statement. A summary of the eight ALU functions and how they appear on line 5 follow. The DH, KL, and BY registers are used in the examples. A general example is presented first.

General



CC Decode:

- 0 DH = $KL \pm BY$
- 1 DH = $KL \pm BY + 1$
- 2 DH = $KL * BY$ or $DH = KL * -BY$
- 3 DH = $KL \vee BY$ or $DH = KL \vee -BY$
- 4 DHC = $KL \pm BY$
- 5 DHC = $KL \pm BY + 1$
- 6 DHC = $KL \pm BY + C$
- 7 DH = $KL \Delta BY$ or $DH = KL \Delta -BY$

6.1.2.6 Line 6

Line 6 is used for the Status register statement. i.e. ST(5)1. This means to set ST(5) to a one.

6.1.2.7 Line 7

Line 7 can contain high and/or low branching tests. X-register 6 and/or 7 will be modified depending upon the result of the tests.

CH decodes 0, 1, and 8 do not appear on this line. CL decodes 0, 1, and 7 do not appear on this line.

6.1.2.8 Line 8

Line 8 contains the symbolic address of the next ROS word and the coordinate of the micro block on a CLD (CAS Logic Diagram) page.

The symbolic address contains five characters as follows:

1. Characters one and two are alphabetic.
2. Character three may be alphabetic or numeric. CN-5 (when it is important, FT, FC, and IG bits 3 & 4) is indicated as zero, or a one in this position.
3. Characters four and five indicate X register bits 6 and 7 settings for the next micro block. Valid characters and their meanings are listed below:
 - 0 Set appropriate X bit to 0
 - 1 Set appropriate X bit to 1
 - X Setting of appropriate X bit is not shown in go to address.
 - Setting of appropriate X bit is under control of condition tested in CH or CL branching statement.

6.1.3 Sample Usage of Microblock (Figure 6-3)

This example shows how several micro blocks may be joined to perform a logical function. In the example, a Seek CCHH is performed. Six Seek bytes are transferred from channel to the 2841. The following functions are accomplished in the example:

1. 2311 - Module 5 is selected.
2. The difference between the old cylinder address and the new cylinder address is computed.
3. File Operable is tested.
4. Five Seek control line are raised to the 2311.
 - a. Head Reset
 - b. Set Cylinder
 - c. Set Head and Direction
 - d. Set Difference
 - e. Seek Start
5. Ending status is posted and transferred to channel. Three assumptions are made:
 - a. The old cylinder address was 100.
 - b. KL contains the new cylinder address, 136.
 - c. DR contains the head select address, 8.

6.1.4 Feature Device Command Flow Charts (Figures 6-4 thru 6-14)

Included in this section are the command flow charts for the changes in the micro program for the Feature devices. The charts are included in Chapter 6 as they are valid for CAS I only.

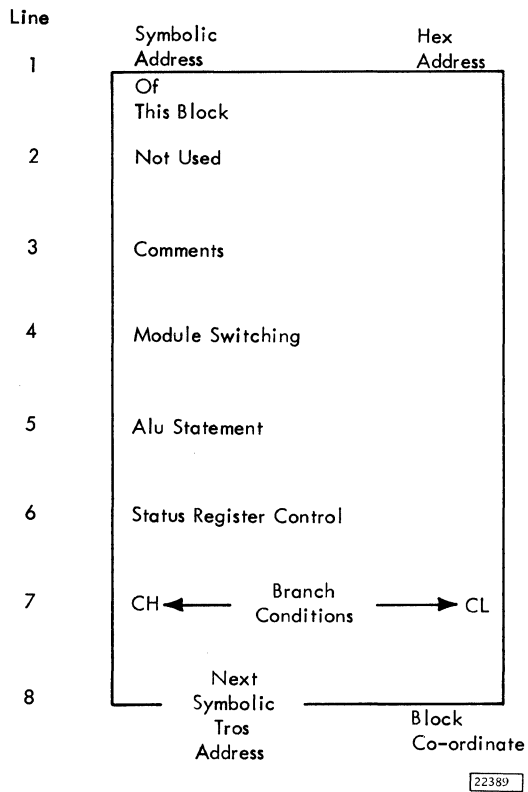


Figure 6-2. CAS1 - TROS Microblock

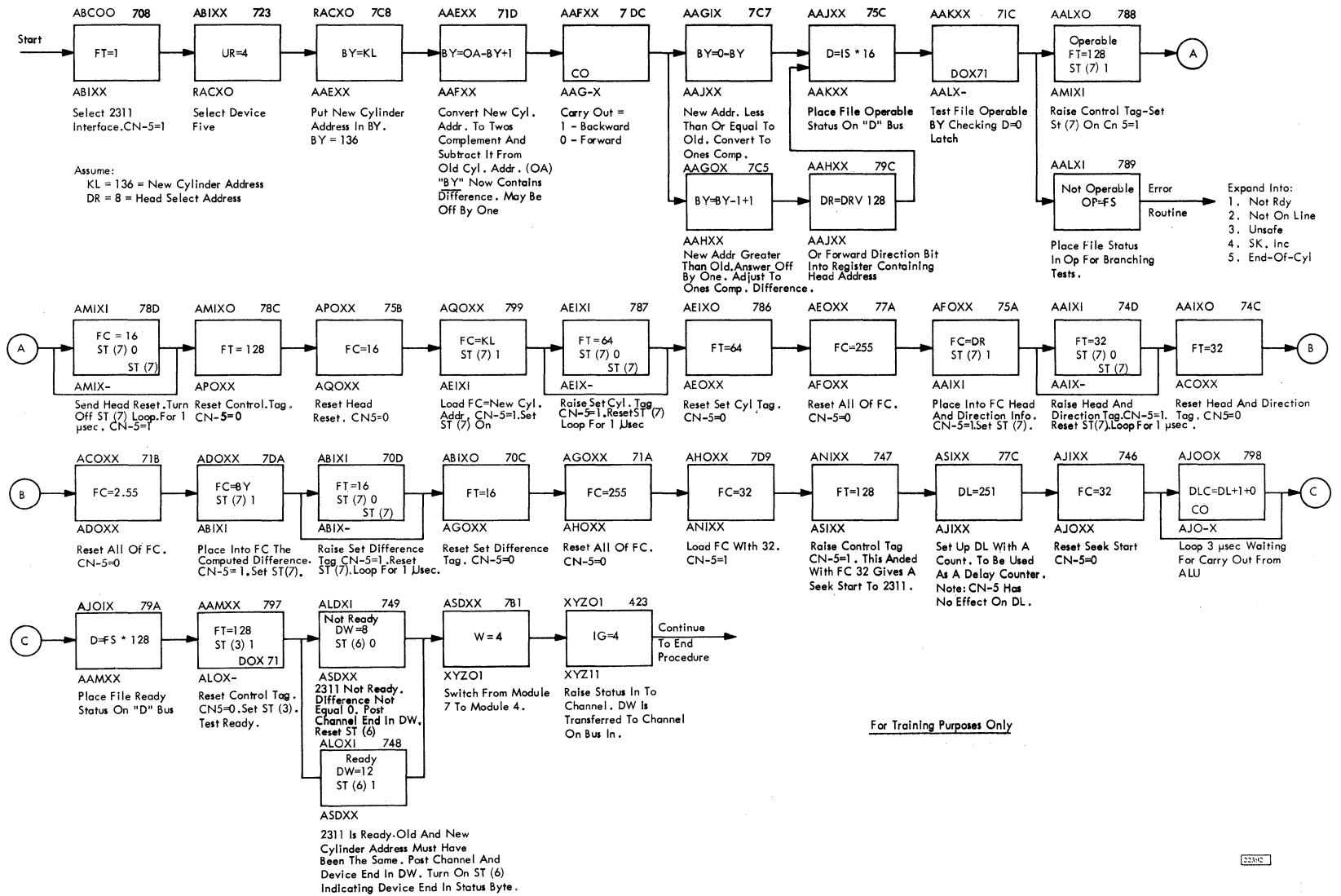
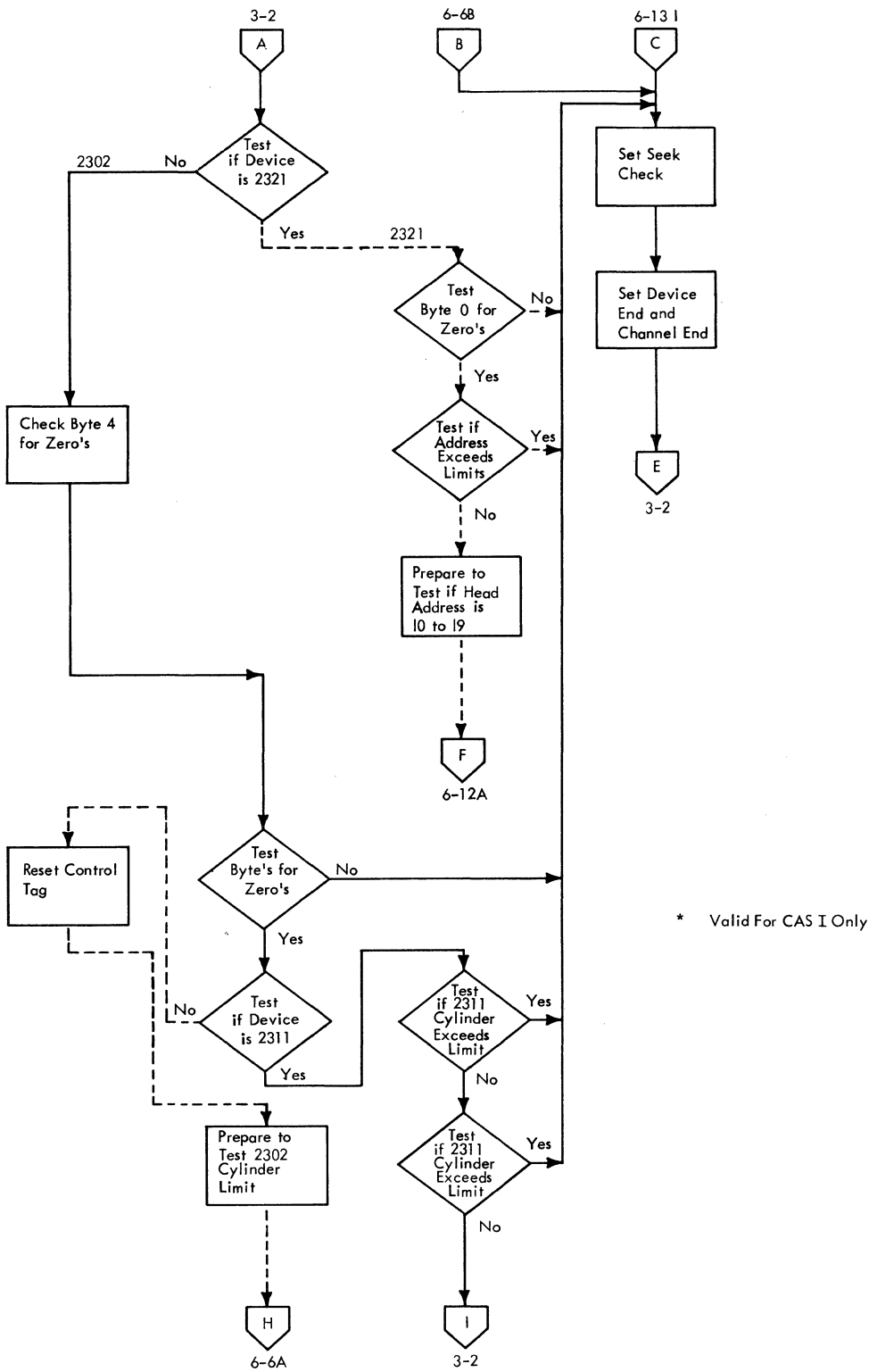


Figure 6-3. Sample Usage of Microblock



Note: Dotted Lines are for Optional Files

22508A

Figure 6-4. Address Check and Limit Test

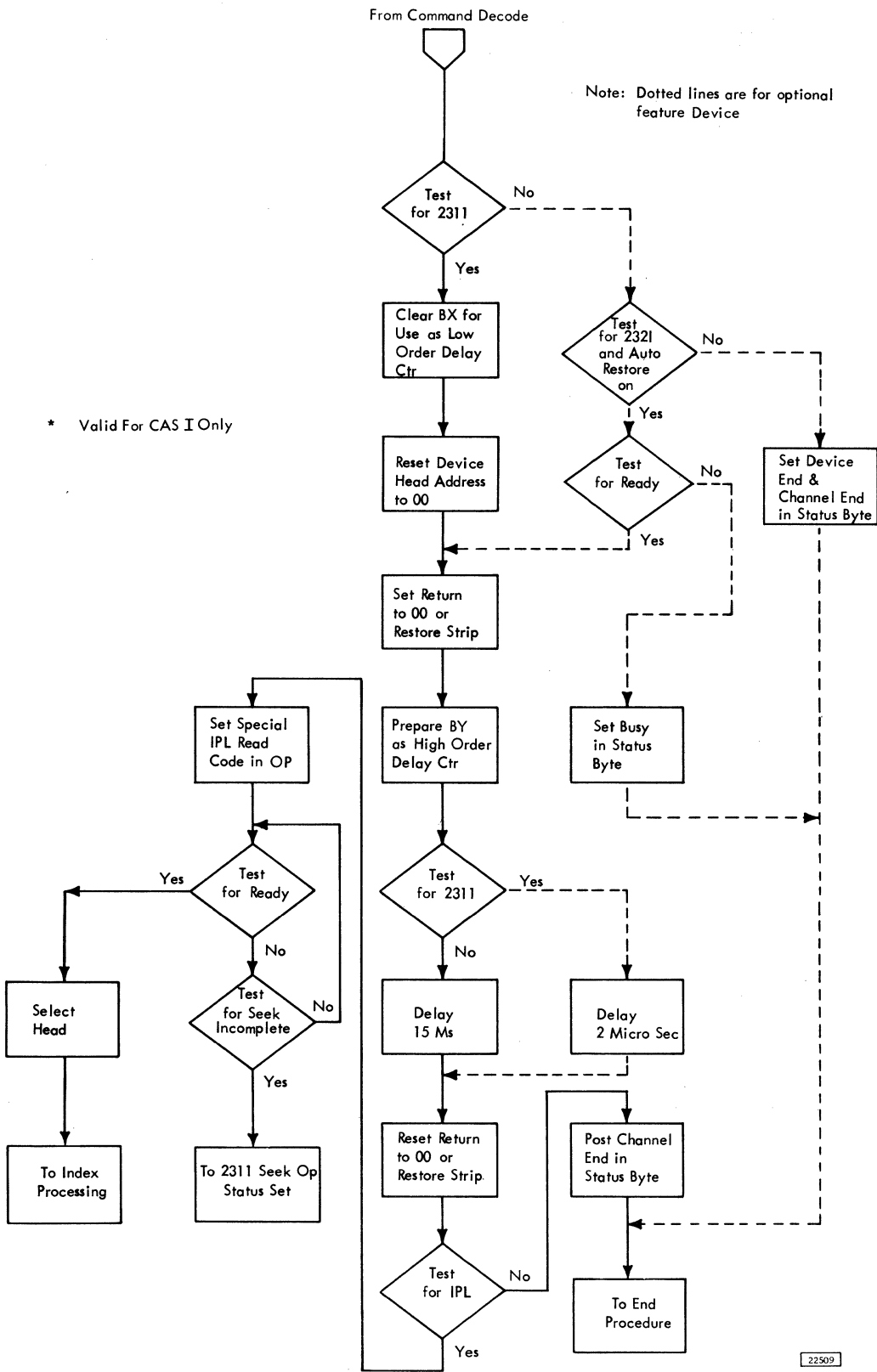


Figure 6-5. Restore Option

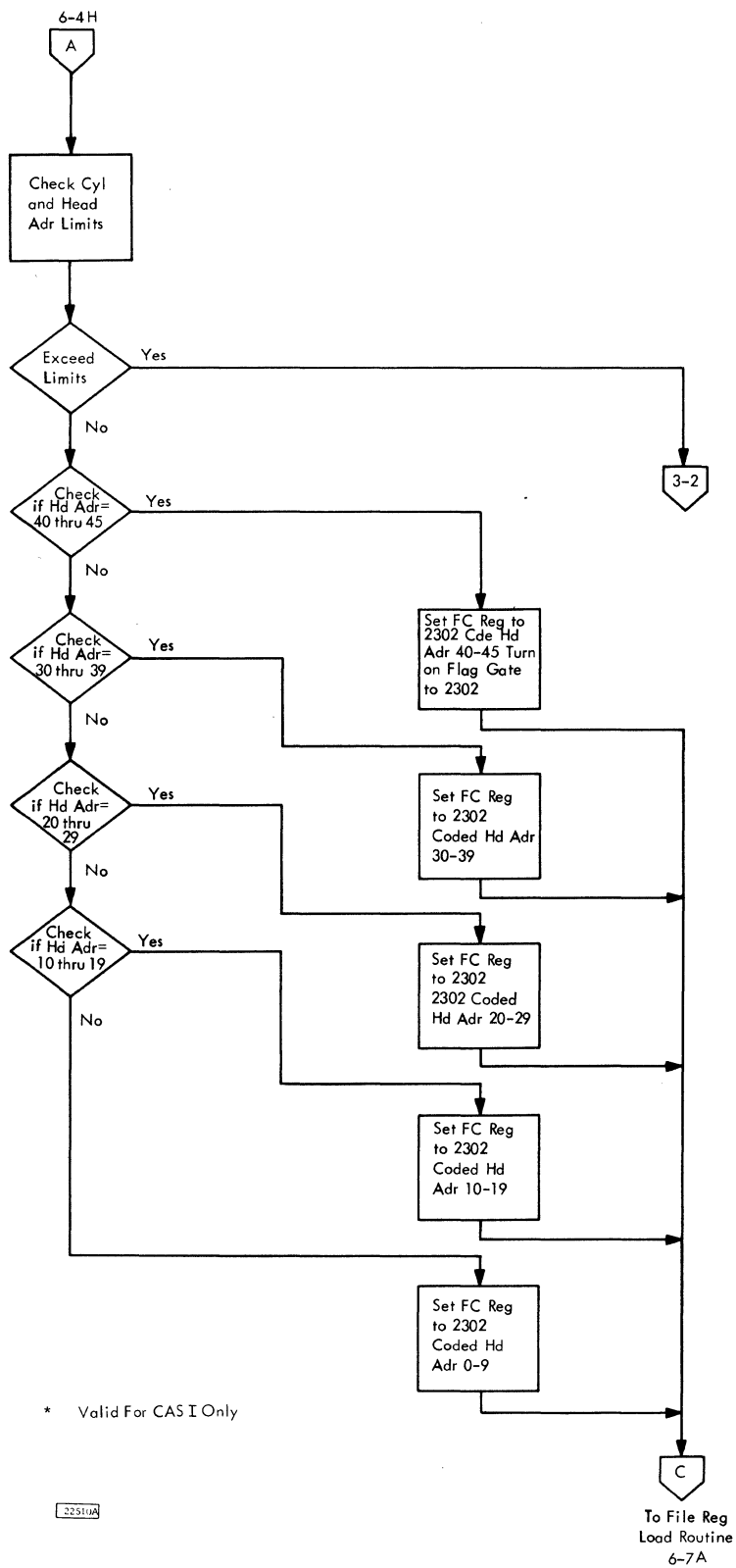


Figure 6-6. 2302 Seek Address Decode - 1

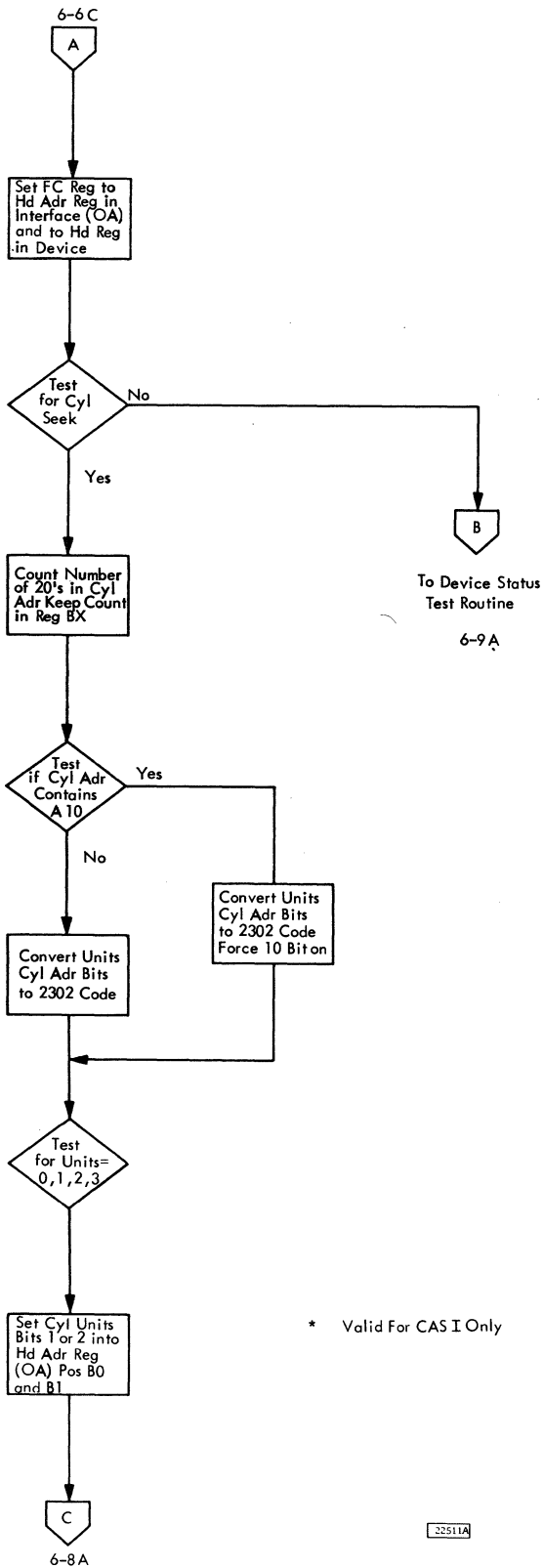


Figure 6-7. 2302 Seek Address Decode - 2

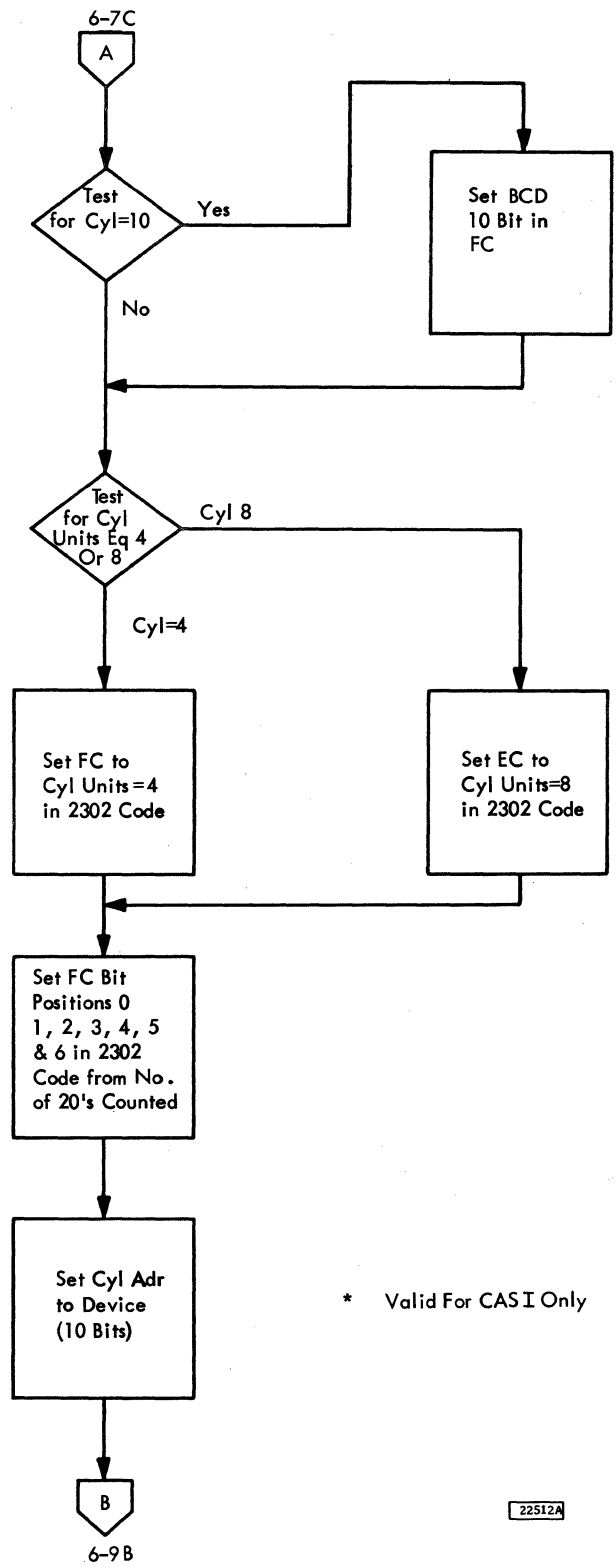


Figure 6-8. 2302 Seek Address Decode - 3

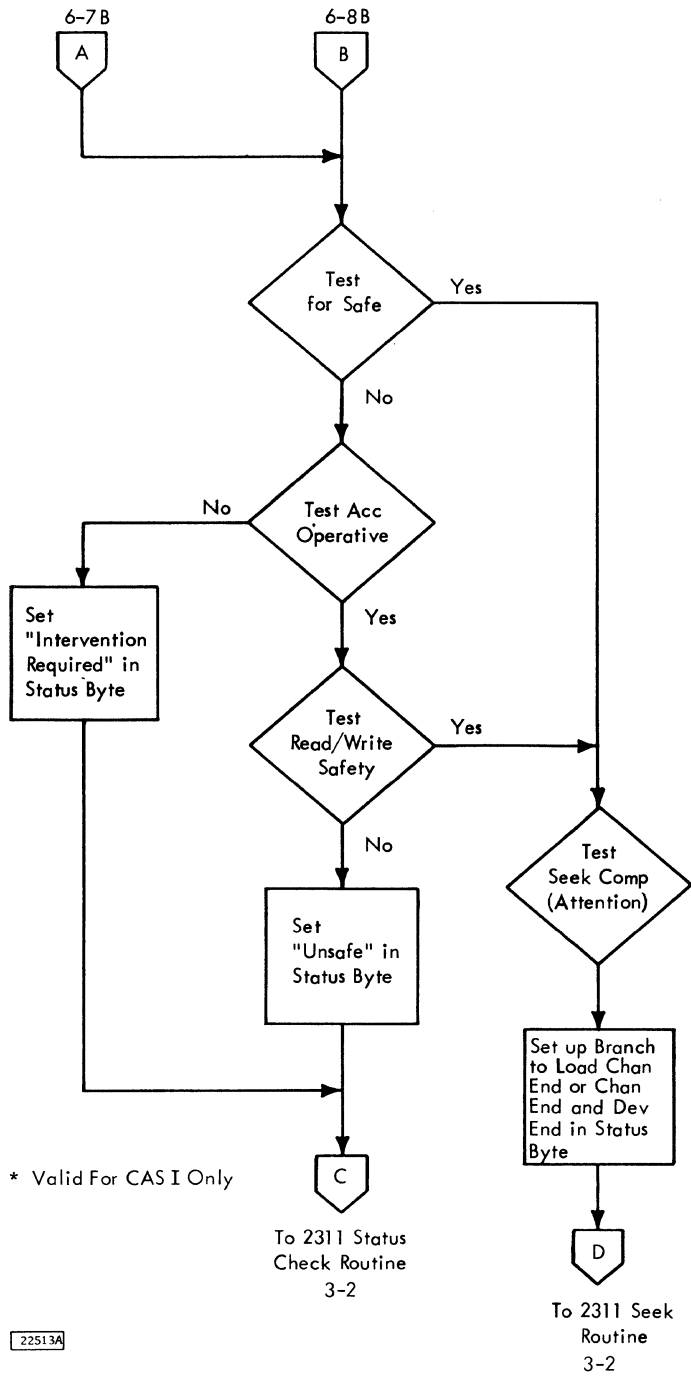
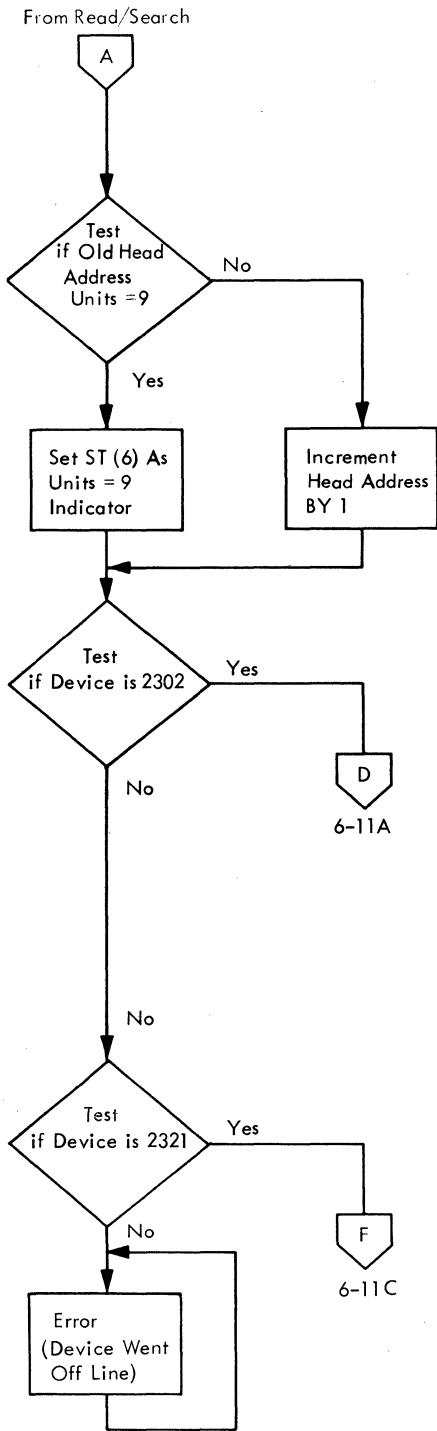


Figure 6-9. 2302 Seek Address Decode - 4



* Valid For CAS I Only

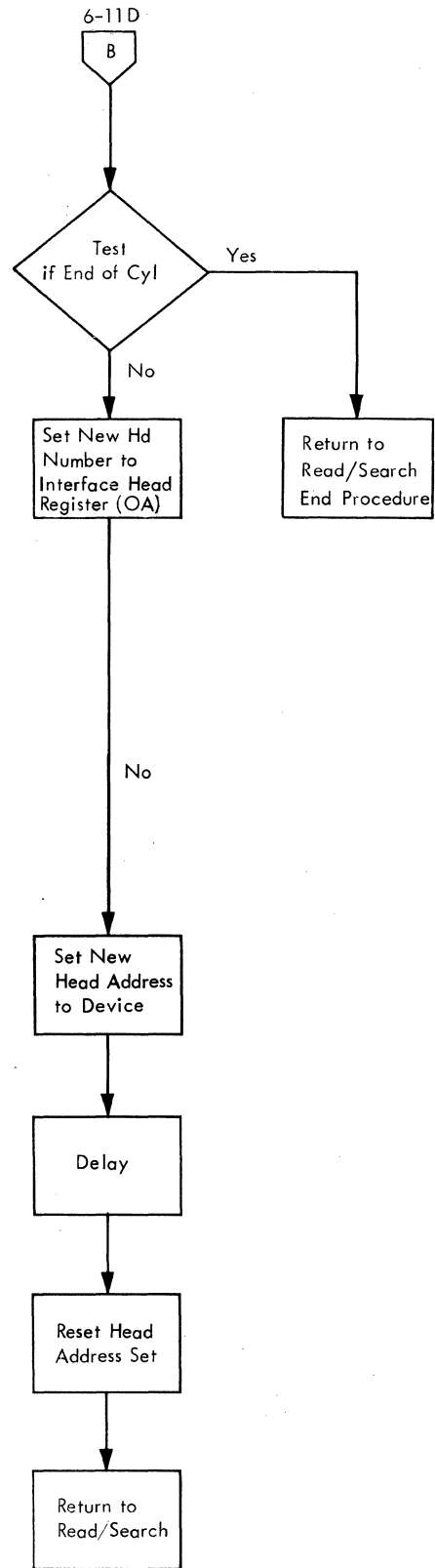
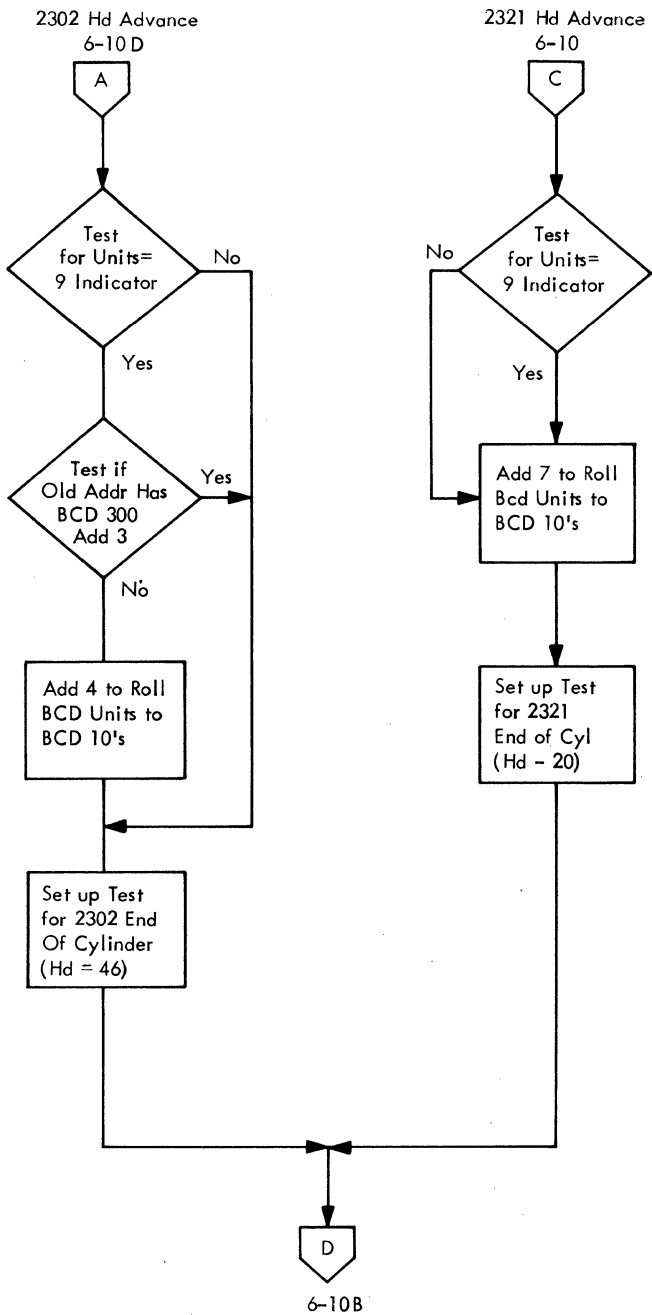


Figure 6-10. Head Advance Entry and Exit

2251-4A



* Valid For CAS I Only

22515A

Figure 6-11. Head Advance - Increment Address

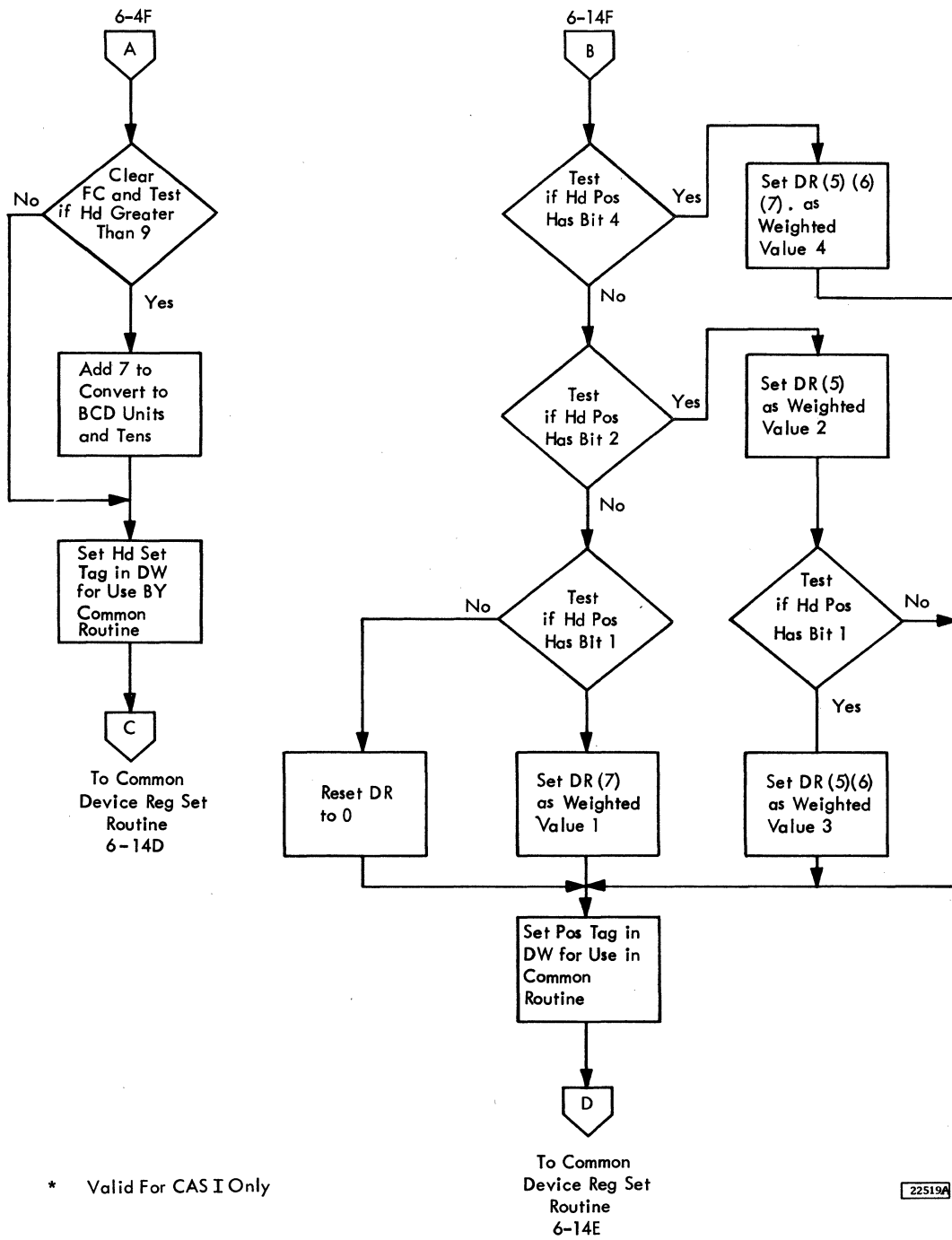


Figure 6-12. 2321 Head Address and Head Position Decode

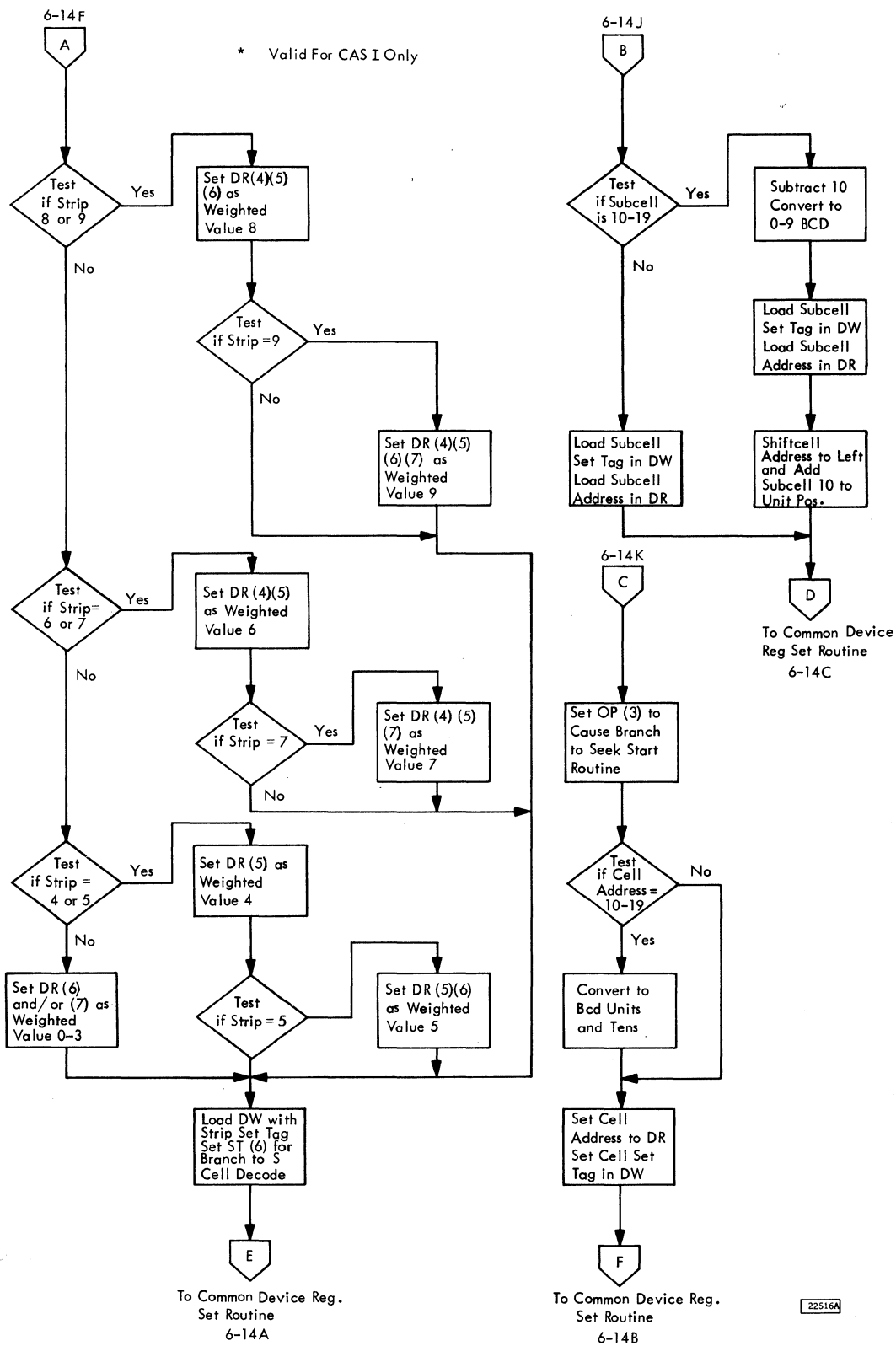


Figure 6-13. 2321 Strip, Subcell and Cell Decode

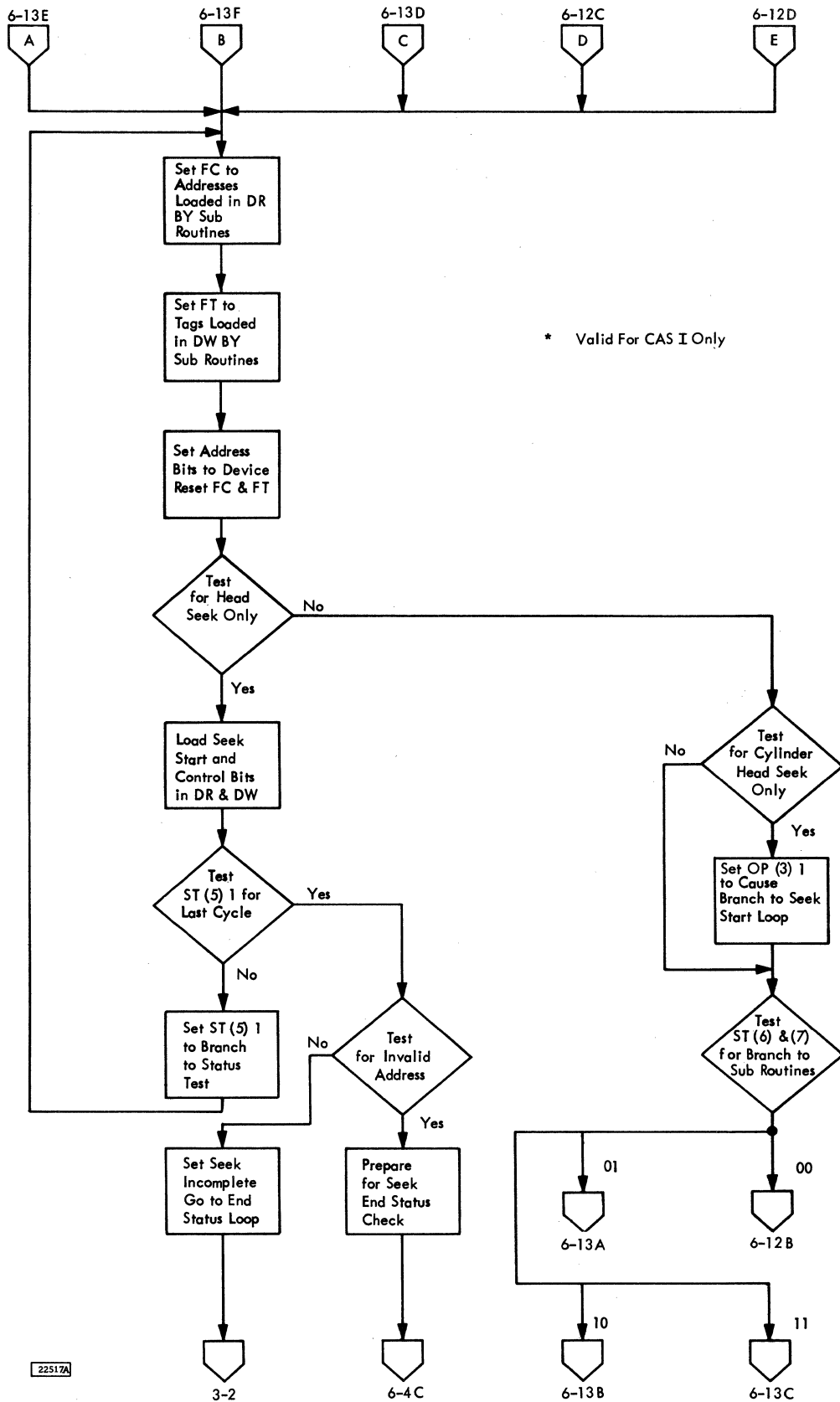


Figure 6-14. 2321 Common Devices Register Set Routine

- A register, 2.1
- Additional storage feature, 5.2
- Address compare switch, 2.24
- Address-in line, 1.11
- Address marker, 1.5
- Address-out line, 1.9
- Address register decoding, 2.8
- Addressing, two channel switch, 5.5
- Alternate track sense bit, 3.3
- ALU basic timing, 2.14
- ALU check sense bit, 3.4
- ALU functional description, 2.14
- ALU general description, 2.11
- ALU statement summary, 2.12
- ALU statements, 2.25
- Appendix, 6.1
- Arithmetic/logical unit, 1.2, 2.11
- Array layout, 2.9
- Attachment feature, 5.1
- Attachment limits, 5.2
- Attachment operation, 2302, 5.2
- Attachment operations, 2321, 5.2
- Attention status bit, 3.1

- B register, 2.1
- Beta gap sequence, 2.17
- Burst byte and exit decisions, micro program, 3.12
- Bus in gates, 2.3
- Bus-in lines, 1.8
- Bus interface lines, 1.8
- Bus out gates, 2.3
- Bus-out lines, 1.8
- Bus-out parity sense bit, 3.2

- Cable entry, 1.2
- Cabling, device/channel, 1.2.9
- CAS microblock, 2.25
- CAS 1, 6.1
- CAS 1 feature device command flow charts, 6.4
- CAS 1 micro block symbology, 6.3
- CAS 1 sample usage of micro block, 6.4
- CAS 1 TROS bit assignment chart, 6.1
- CC decode, 2.12
- CE indicators, 2.24
- CE panel, 2.23
- CE panel, 1.2.4
- CE switches, 2.23
- Chain command control, 1.13
- Chained reselektion, micro program, 3.13
- Channel control register, 2.3
- Channel end status bit, 3.1
- Channel interface attachment, 2.18
- Channel interface introduction, 1.7
- Channel interface, system/360, 1.2
- Check reset switch, 2.23
- Check stop/run switch, 2.24
- Circuit breaker, 4.1
- Circuit protectors, 4.1
- Clock, 2.1
- Clock-out line, 1.12

- Code checking, 1.6
- Command decodes micro program, 3.10
- Command flow charts, 3.9
- Command orientation summary, 3.13
- Command-out line, 1.10
- Command reject sense bit, 3.2
- Configuration of 2841, 1.2.1
- Control address indicator, 2.24
- Control fields, 2.10
- Control operations, micro program, 3.11
- Control unit end status bit, 3.1
- Control unit busy status bit, 3.1
- Control register indicator, 2.24
- Contactors, 4.1
- Core carrier assembly, 2.6
- Count area, 1.5
- Cylinder selection, 1.5
- Cyclic check code, 1.6

- Data flow, basic read, 1.3
- Data flow, basic write, 1.3
- Data record, 1.5
- Data area, 1.5
- Data check in count field sense bit, 3.3
- Data check indicator, 2.24
- Data check sense bit, 3.2
- Data read register, 2.2
- Data track format, 1.4.1
- Data transfer sequences, 2.19
- Data transfers, 1.14
- Defective surfaces operation, 3.6
- Defective track sense bit, 3.2
- Delay lines, adjustable, 2.16
- Device end status bit, 3.1
- Device interfaces, 1.3
- Devices recording, 2.8
- Dimensions, 1.2
- Display switch, 2.23
- Driver isolation, 2.9

- End of cylinder sense bit, 3.3
- End operation, 1.14
- End procedure, 3.13
- Ending sequence, 2.20
- End-of-file operation, 3.5
- Enter switch, 2.23
- Environmental conditions, 1.2
- Equipment check sense bit, 3.2
- Error detection, 1.6
- Error detector, 2.16
- Error register, 2.2

- Features, 5.1
- Feature, additional storage, 5.2
- Feature, file scan, 5.3
- Feature, record overflow, 5.6
- Feature, two-channel switch, 5.3
- File control register, 2.3
- File protected sense bit, 3.4
- File protection operation, 3.8

- File scan feature, 5.3
- File status gates, 2.4
- File tag register, 2.3
- Flag, 1.5
- Flag byte processing, micro program, 3.11
- Format, track, 1.3
- Formatting overflow records, 5.6
- Functional description, 1.2
- Functional units, 2.1

- Gap sensor, 2.16
- Gap spacing, micro program, 3.12
- Gaps, 1.6
- Gate A, view, 1.2.4
- Gate generator, 2.16
- Gate recording, 2.8
- General power supply description, 4.1

- Halt I/O instruction, 2.21
- Halt I/O sequence, 2.21
- Head selection, 1.5
- Hold-out line, 1.9
- Home address area, 1.3

- Immediate commands, 3.2
- Inbound tag lines, 1.11
- Index marker, 1.3
- Index processing, micro program, 3.12
- Initial program load operation, 3.8
- Initial selection, micro program, 3.10
- Initial selection sequence, 1.13, 2.18
- Initial status presentation, micro program, 3.11
- Input element gates, 2.4
- Interface lines, 1.7
- Interlock lines, 1.11
- Interface attachment, 2.3
- Interface connections, 1.8.3
- Interface lines, 1.8.2
- Interface operations, 1.13
- Interface timing, two channel switch, 5.5
- Intervention required sense bit, 3.2
- Invalid sequence sense bit, 3.3
- I/O interface, system/360, 1.7
- Isolation of drivers, 2.9

- Key area, 1.6

- Laminar bus, 2.6
- Lamp test switch, 2.23
- Load counts, micro program, 3.11

- Machine clock, 2.1
- Machine probe indicator, 2.24
- Machine stop indicator, 2.24
- Metering-in line, 1.12
- Microblocks sample usage, 2.28
- Microblock symbology, 2.27
- Micro program logic, condensed, 3.9
- Miscellaneous operations, 3.5
- Missing address marker sense bit, 3.4

- Module assembly, 2.6
- Module end boards, 2.7
- Module select gates, 2.4
- Multiple track operation, 3.5

- No record found sense bit, 3.3
- Normal/CE switch, 2.23

- Old address gates, 2.4
- OP code bit structure, 1.8.1
- Operator's position, 1.2
- Operational-in line, 1.12
- Operational-out line, 1.11
- Outbound, tag lines, 1.9
- Overflow incomplete sense bit, 3.4
- Overflow record formatting, 5.6
- Overflow record processing, 5.6
- Overrun sense bit, 3.2

- Physical description, 1.2
- Polling, 1.14
- Polling interrupt routine, 2.22
- Polling interrupts, 2.21
- Power control, 1.2
- Power control, two channel switch, 5.5
- Power distribution, 4.1
- Power interlocks, 4.2
- Power requirements, 1.2
- Power sequencing, 4.1
- Power sequencing panel, 1.2.10
- Power supply, 4.1
- Power supply components, 4.1
- Power supply marginal checking, 4.1
- Power supply thermal considerations, 4.1
- Processing overflow records, 5.6
- Programming, 1.7

- Ramp generator, 2.16
- Read/clocking, micro program, 3.12
- Read operation, 2.20
- Record overflow feature, 5.6
- Record number, 1.5
- Registers, 2.1
- Registers and controls, miscellaneous, 2.2
- Registers, general purpose, 1.3, 2.1
- Register select switch, 2.23
- Request-in line, 1.9
- Resets, 2.22
- Reset, selective, 2.22
- Reset switch, 2.23
- Resistances tape, 2.7
- Restart conditions, 2.18

- Scan controls interface lines, 1.8
- Scan operations, micro program, 3.12
- Search operations, micro program, 3.12
- Seek check sense bit, 3.3
- Seek commands, 3.2
- Seek complete gates, 2.4
- Select-in line, 1.9

- Select-out line, 1.8
- Selective reset, 1.13, 2.22
- Sense amp indicator, 2.24
- Sense bytes, 3.2, 3.5
- Sense information, 3.2
- Sense operations, micro program, 3.11
- SERDES general description, 2.15
- SERDES read operation, 2.16
- SERDES write operation, 2.15
- Serializer/deserializer unit (SERDES), 1.2, 2.15
- Service-in line, 1.11
- Service in/out controls, 2.3
- Service-out line, 1.10
- Set addr switch, 2.23
- Short control unit busy sequence, 2.20
- Single stop switch, 2.23
- Special controls, interface lines, 1.12
- Stacked status, 2.22
- Start address switch, 2.24
- Start switch, 2.23
- Status information, 3.1
- Status register, 2.2
- Status-in line, 1.11
- Status modifier status bit, 3.1
- Stop address switch, 2.24
- Stop switch, 2.23
- Subtract functions, 2.14
- Suppress data transfer, 1.13
- Suppress-out line, 1.13
- Suppress status, 1.13
- Symbology, micro block, 2.27
- System reset, two channel switch, 5.5

- Tape identification, 2.7
- Tape number determination, 2.8
- Tape numbering, 2.6
- Tapes plastic, 2.6
- Tape resistance, 2.7
- Tape types, 2.7
- Theory of operation, 3.1
- Timing of TROS, 2.9
- Track format, 1.3
- Track descriptor record (RO), 1.4
- Track overrun sense bit, 3.3
- Transformer read-only-storage (TROS), 1.3, 2.4

- TROS address check, 2.10
- TROS addressing, 2.7
- TROS addressing register, 2.2
- TROS array layout, 2.9
- TROS bit assignment chart, 2.25
- TROS characteristics and capacity, 2.5
- TROS control latches, 2.10
- TROS control register check, 2.11
- TROS drive commoning, 2.8
- TROS functional operation, 2.9
- TROS gate commoning, 2.8
- TROS inhibit, 2.9
- TROS module assembly, 2.6
- TROS module physical construction, 2.6
- TROS output word, 2.10
- TROS principles of operation, 2.5
- TROS purpose, 2.4
- TROS sense amplifier check, 2.11
- TROS tape deck, 2.7
- TROS timing, 2.9
- TROS transformer principle, 2.5
- TROS use, 2.4
- TROS word control fields, 2.25
- Two channel switch circuit description, 5.6
- Two-channel switch feature, 5.3

- Unit check status bit, 3.1
- Unit exception status bit, 3.2
- Use meter, two channel switch, 5.5
- Unsafe sense bit, 3.4
- Unselected status sense bit, 3.4
- Unusual conditions, 5.7

- VFO triggers, 2.16
- View of 2841, front, 1.2.6
- View of 2841, rear, 1.2.3
- View of 2841, right side, 1.2.7
- View of 2841, top, 1.2.2
- View of TROS right side, 1.2.5
- View of TROS tape deck, 1.2.8

- Write operations, micro program, 3.11

- Zero detector, 2.16

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FIGURE(S)

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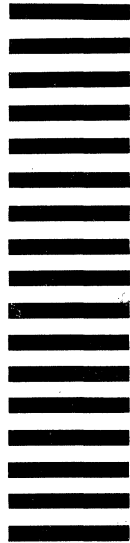
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