HP 13255

DISPLAY MEMORY/DMA MODULE

Manual Part No. 13255-91250

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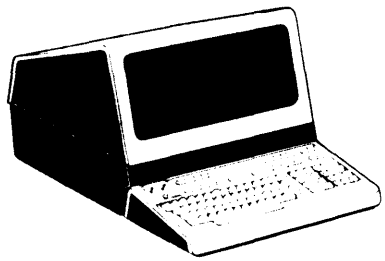
DATA TERMINAL
TECHNICAL INFORMATION



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1.0 INTRODUCTION.

The Display Memory/Direct Memory Access (DMA) module is one printed circuit assembly (PCA) of a two PCA set. The second PCA is the Display Timing/Control module (02640-60267). This board set interfaces into the 264X terminal environment by performing the functions of display memory management, CRT drive signal generation, and video generation.

The Display Memory/DMA subsystem replaces three separate boards in the first generation 264X hardware (DMA, enhancements, and memory). Resident in this module is the 21.34 MHz. video dot clock, 16K bytes of dynamic RAM, processor/backplane interface, a PROM controlled DMA state machine, and timing circuitry and registers to prepare and store the proper character cell information needed by the Display Control/Timing module.

The Display Memory/DMA module takes care of all tasks associated with display memory management and display direct memory access (DMA). Included among these tasks are display memory timing, processor and DMA memory access timing resolution, ASCII and enhancement data routing, bus interfacing, and timing generation. Each line of characters and associated enhancements and control codes is fetched from display memory by following a linked list which begins at the top address of logical memory. The DMA state machine within this module follows this list and controls the routing of data according to the information fetched from the list.

A private interface to the Display Timing/Control module is provided over a topplane through which the two boards communicate timing information and memory data.

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1.0 INTRODUCTION.

The Display Memory/Direct Memory Access (DMA) module is one printed circuit assembly (PCA) of a two PCA set. The second PCA is the Display Timing/Control module (02640-60267). This board set interfaces into the 264X terminal environment by performing the functions of display memory management, CRT drive signal generation, and video generation.

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A private interface to the Display Timing/Control module is provided over a topplane through which the two boards communicate timing information and memory data.

2.0 OPERATING PARAMETERS

A summary of operating parameters for the Display Timing/ Control module is contained in tables 1.0 through 6.1.

Table 1.0 Physical Parameters

PART NUMBER	NOMENCLATURE	Size (L x W x D) +/-0.100 Inches	Weight (Pounds)
02640-60250	Display Memory/DMA PCA	12.9 x 4.0 x 0.5	0.48
NUMBER OF BACKPLANE SLOTS REQUIRED: 1			

Table 2.0 Reliability and Environmental Information

Environmental:	(X) HP Class B ( ) Other:
Restrictions:	Type tested at product level
Failure Rate:	2.972 (percent per 100 hours)

Table 3.0 Power Supply and Clock Requirements - Measured
(At +/-5% Unless Otherwise Specified)

+5 Volt Supply	+12 Volt Supply	-12 Volt Supply	-42 Volt Supply
@ 1.5 A	@ 40. mA	@ 50. mA	N/A
115 volts ac		220 volts ac	
N/A		N/A	
Clock Frequency:	21.34 MHz 4.915 MHz		

Table 4.0 Switch Definitions

PCA Designation	Function	
	Closed	Open
Display Memory/ DMA Module		
1,2,3,4	2647F compatible mode	Standard 264X mode
	Closing switches 1-4 causes this module to operate under 2647F backplane mode. Opening these switches allows this module to be installed into a standard 264X series terminal.	

Table 5.0 Connector Information (Display Memory/DMA PCA)

Connector and Pin No.	Signal Name	Signal Description
P1, Pin 1	+5V	+5 Volt Power Supply
-2	GND	Ground Common Return (Power and Signal)
-3	SYS CLK	4.915 MHz System Clock
-4	-12V	-12 Volt Power Supply
-5	$\overline{\text{ADDR0}}$	Negative True, Address Bit 0
-6	$\overline{\text{ADDR1}}$	Negative True, Address Bit 1
-7	$\overline{\text{ADDR2}}$	Negative True, Address Bit 2
-8	$\overline{\text{ADDR3}}$	Negative True, Address Bit 3
-9	$\overline{\text{ADDR4}}$	Negative True, Address Bit 4
-10	$\overline{\text{ADDR5}}$	Negative True, Address Bit 5
-11	$\overline{\text{ADDR6}}$	Negative True, Address Bit 6

Table 5.1 Connector Information (Display Memory/DMA PCA Cont'd)

Connector and Pin No.	Signal Name	Signal Description
P1, PIN 12	$\overline{\text{ADDR7}}$	Negative True, Address Bit 7
-13	$\overline{\text{ADDR8}}$	Negative True, Address Bit 8
-14	$\overline{\text{ADDR9}}$	Negative True, Address Bit 9
-15	$\overline{\text{ADDR10}}$	Negative True, Address Bit 10
-16	$\overline{\text{ADDR11}}$	Negative True, Address Bit 11
-17	$\overline{\text{ADDR12}}$	Negative True, Address Bit 12
-18	$\overline{\text{ADDR13}}$	Negative True, Address Bit 13
-19	$\overline{\text{ADDR14}}$	Negative True, Address Bit 14
-20	$\overline{\text{ADDR15}}$	Negative True, Address Bit 15
-21	$\overline{\text{I/O}}$	Negative True, Input Output/Memory
-22	GND	Ground Common Return (Power and Signal

Table 5.2 Connector Information (Display Memory/DMA PCA Cont'd)

Connector and Pin No.	Signal Name	Signal Description
P1, Pin A	GND	Ground Common Return (Power and Signal)
-B	$\overline{\text{POLL}}$	Negative True, Polled Interrupt Identification Request
-C	+12V	+12 Volt Power Supply
-D	PWR ON	System Power On
-E	$\overline{\text{BUS0}}$	Negative True, Data Bus Bit 0
-F	$\overline{\text{BUS1}}$	Negative True, Data Bus Bit 1
-H	$\overline{\text{BUS2}}$	Negative True, Data Bus Bit 2
-J	$\overline{\text{BUS3}}$	Negative True, Data Bus Bit 3
-K	$\overline{\text{BUS4}}$	Negative True, Data Bus Bit 4
-L	$\overline{\text{BUS5}}$	Negative True, Data Bus Bit 5
-M	$\overline{\text{BUS6}}$	Negative True, Data Bus Bit 6

Table 5.3 Connector Information (Display Memory/DMA PCA Cont'd)

Connector and Pin No.	Signal Name	Signal Description
P1, PIN N	$\overline{\text{BUS7}}$	Negative True, Data Bus Bit 7
-P	$\overline{\text{WRITE}}$	Negative True, Read/Write Type Cycle
-R	$\overline{\text{ATN2}}$	Negative True, CTU and Polled Interrupt Request
-S	$\overline{\text{WAIT}}$	Negative True, Wait Control Line
-T	PRIOR IN	Bus Controller Priority In
-U	PRIOR OUT	Bus Controller Priority Out
-V	ADDR16	Positive true, Address Bit 16
-W	ADDR17	Positive True, Address Bit 17
-X	ADDR18	Positive True, Address Bit 18
-Y	$\overline{\text{REQ}}$	Negative True, Request (Bus Data Currently Valid)
-Z	ATN	Negative True, Data Comm Interrupt Request

Table 5.4 Connector Information (Display Memory/DMA PCA Cont'd)

Connector and Pin No.	Signal Name	Signal Description
P3, Pin 1	GND	Ground
-2	I/O STROBE	Cursor Control Strobe from Display Mem/DMA
-3	$\overline{103}$	Graphics Sync. signal--Character 103
-4	DSPCLK	Positive True form of 21.34 Mhz Dot clock
-5	$\overline{\text{I/O SELECT}}$	Negative True--Cursor control select line
-6	$\overline{AB6}$	Negative True--ASCII Bit 6
-7	$\overline{AB5}$	Negative True--ASCII Bit 5
-8	$\overline{AB4}$	Negative True--ASCII Bit 4
-9	$\overline{AB3}$	Negative True--ASCII Bit 3
-10	$\overline{AB2}$	Negative True--ASCII Bit 2
-11	$\overline{AB1}$	Negative True--ASCII Bit 1

Table 5.5 Connector Information (Display Memory/DMA PCA Cont'd)

Connector and Pin No.	Signal Name	Signal Description
P3, PIN 12	$\overline{AB0}$	Negative True--ASCII Bit 0
-13	GND	Signal Ground
-14	$\overline{MEMCYC}$	Clock with ~840 nsec. period defining display memory cycles
-15	EDROW	End of Data Row Pulse
-16	SHFTCLK	Line Buffer Load Clock
-17	Qa	Enhancement Alignment Clock
-18	$\overline{SLOAD}$	Negative True, (Low) Indicates that CRT Controller self-load is in progress
-19	VSCLK	Video Shift Clock--Line Buffer Display Clock
-20	$\overline{XBITS2}$	External Video Bit Stream (Graphics)
-21	GND	Signal Ground
-22	$\overline{XBITS1}$	External Video Bit Stream (Unused)

Table 5.6 Connector Information (Display Memory/DMA PCA Cont'd)

Connector and Pin No.	Signal Name	Signal Description
P3, Pin A	$\overline{\text{DSPCLK}}$	Negative True form of 21.34 Mhz dot clock
-B	GND	Signal Ground
-C	$\overline{\text{D2}}$	Graphics Sync. signal--Dot 2
-D	GND	Signal Ground
-E	ZERO	Start Top-of-Frame Pulse
-F	CHARCLK	Character Rate Clock
-H	$\overline{\text{CHARCLK}}$	Character Rate Clock (negative true)
-J	VBLANK	Vertical Blanking--Graphics Sync. Signal
-K	EB5	Positive True--Enhancement Bit 5
-L	EB4	Positive True--Enhancement Bit 4
-M	EB3	Positive True--Enhancement Bit 3
-N	EB2	Positive True--Enhancement Bit 2
-P	EB1	Positive True--Enhancement Bit 1

Table 5.7 Connector Information (Display Memory/DMA PCA Cont'd)

Connector and Pin No.	Signal Name	Signal Description
P3, PIN R	EB0	Positive True--Enhancement Bit 0
-S	HSYNC	Horizontal Sync from CRT Controller
-T	GND	Signal Ground
-U	I/O BIT 5	Status Bit from Display Memory/DMA module
-V	I/O BIT 6	Status Bit from Display Memory/DMA module
-W	DMAROW=CURROW	(high) indicates that the cursor is on the same character row as the DMA module
-X	SHFTEN	Enable signal for Line Buffer Loading
-Y	GND	Signal Ground
-Z	$\overline{\text{RFSHEN}}$	(low) indicates that Display Memory refresh is enabled

Table 6.0 Module Bus Pin Assignments-Display Memory/DMA PCA

Function Performed: Set Cursor Y Position
Turn Display On/Off
Turn DMA On/Off
Invoke Skipeol and Mayeop Modes

Poll Bit: Not Applicable

Module Address: (ADDR 11,10,9,4) = (0111)

Function Specifier: ADDR5 = 1

Data Bus Bit Interpretation:

B7 (high) Indicates Display Off

B6 (high) Indicates DMA Off

B5 (high) Indicates Skipeol or Mayeop mode may be invoked

B4 Cursor Y Position $\overline{BIT4}$

B3 Cursor Y Position $\overline{BIT3}$

B2 Cursor Y Position $\overline{BIT2}$

B1 Cursor Y Position $\overline{BIT1}$

B0 Cursor Y Position $\overline{BIT0}$

Value	Bus Signal
X	ADDR 15
X	ADDR 14
X	ADDR 13
X	ADDR 12
0	ADDR 11
1	ADDR 10
1	ADDR 9
X	ADDR 8
X	ADDR 7
X	ADDR 6
1	ADDR 5
1	ADDR 4
X	ADDR 3
X	ADDR 2
X	ADDR 1
X	ADDR 0
B7	BUS 7
B6	BUS 6
B5	BUS 5
B4	BUS 4
B3	BUS 3
B2	BUS 2
B1	BUS 1
B0	BUS 0

1=Logical 1=Bus Low
0=Logical 0=Bus High
X=Don't Care

Table 6.1 Module Bus Pin Assignments-Display Memory/DMA PCA

Function Performed: Set Cursor X Position
Turn Display Memory Refresh On/Off

Poll Bit: Not Applicable

Module Address: (ADDR 11,10,9,4) = (0111)

Function Specifier: ADDR5 = 0

Data Bus Bit Interpretation:

B7 (high) Indicates Display Memory Refresh Off

B6 Cursor X Position $\overline{BIT6}$

B5 Cursor X Position $\overline{BIT5}$

B4 Cursor X Position $\overline{BIT4}$

B3 Cursor X Position $\overline{BIT3}$

B2 Cursor X Position $\overline{BIT2}$

B1 Cursor X Position $\overline{BIT1}$

B0 Cursor X Position $\overline{BIT0}$

Value	Bus Signal
X	ADDR 15
X	ADDR 14
X	ADDR 13
X	ADDR 12
0	ADDR 11
1	ADDR 10
1	ADDR 9
X	ADDR 8
X	ADDR 7
X	ADDR 6
0	ADDR 5
1	ADDR 4
X	ADDR 3
X	ADDR 2
X	ADDR 1
X	ADDR 0
B7	BUS 7
B6	BUS 6
B5	BUS 5
B4	BUS 4
B3	BUS 3
B2	BUS 2
B1	BUS 1
B0	BUS 0

1=Logical 1=Bus Low
0=Logical 0=Bus High
X=Don't Care

3.0 FUNCTIONAL DESCRIPTION.

Refer to the block diagram (Figure 1), schematic diagram (Figures 2,3), timing diagram (Figures 3,4), component location diagram (Figure 5), and parts list located in the appendix.

3.1 DMA FUNCTIONS

3.1.1 The DMA state machine interprets each byte read from display memory according to the following chart:

LOGICAL DATA	INTERPRETATION
0xxxxxxx	ASCII character
10xxxxxx	Enhancement
111xxxxx or 1101xxxx	MSB byte of link address
1100xxxx or 11001xxx	Software flag
11001100	End of line marker
11001110	End of page marker

3.1.2 Each byte from display memory is latched into an eight bit register (U45). The contents of the register are interpretted by a 256 X 4 PROM (U55) and five DMA control signals are generated (CHAR, $\overline{\text{ENH}}$, $\overline{\text{LINK}}$, $\overline{\text{EOL}}$, and $\overline{\text{EOP}}$). If a byte is deemed to be a character, it is latched into U25 and presented over the topplane to the Display Control/Timing module. For every character latched into U25, two events occur. U49-4 is strobed by U211-8 and precharges the "shift-in" clock (SHFTCLK) used by the line buffer shift registers on the

Display Control/Timing board. The next rising edge of U24-12 causes SHFTCLK to go low, thereby shifting the next character/enhancement pair into the line buffers. U211-8 also strobes a modulus 80 counter (U411 and U511) through U34-9,8. This counter keeps track of how many characters have been loaded into the line buffers. The eightieth character causes U311-6 to go high, thereby signalling the DMA machine to stop operation until the beginning of the next character row.

3.1.3 Enhancement bytes result in the six least significant bits of that byte being latched into U26. U26 is strobed for each enhancement encountered in the linked list and is cleared at the beginning of each character row and when blank fill is initiated.

3.1.4 An end-of-line marker sets up a mode in which the DMA machine is idle, U26 is cleared, and each machine cycle causes an ASCII 20H to be latched into U25 and loaded into the line buffers. This blank fill action continues until eighty characters have been loaded into the line buffers. The end-of-line mode is is turned off by U711 at the beginning of the next data row.

3.1.5 An end-of-page marker sets up a blank fill mode identical to that described above except that the end-of-page mode is not turned off by U711 until the end of the current display frame.

3.1.6 A link byte causes the DMA machine to latch the link byte itself (MSB), and the next sequential byte (LSB) into the four counter/sequencer IC's (U12, U22, U23, and U33). A jump is then performed and the DMA machine resumes operation at the "linked" address.

3.1.7 If a software flag is read by the DMA machine a NOP is executed and no action taken by the machine until the next byte is read.

3.2 PROCESSOR ACCESS CONTENTION

3.2.1 The Display Memory/DMA module operates within 840 ns cycles. At the end of the current board cycle, the outputs of the DMA control PROM's (U19 and U29) are latched into U110 and U210 and configures the DMA machine for the following board cycle. If a processor display memory read or write is initiated, U68-8

causes the $\overline{\text{WAIT}}$ line to go low through U510-10,8 and U710-9,8, and U79-6 goes high to indicate a processor operation is pending. Halfway through each board cycle, the DMA machine strobes U69-3 and samples the processor status. If a processor operation is pending, a display memory read or write is recognized, the DMA machine enables bus buffers U52, U53, U54, and U44 (U44--reads only), tri-states U32, U12, U22, U23, and U33, and generates a RAS/CAS cycle. Towards the end of the board cycle, when the data transfer has been

accomplished, U39-11 sets U611-6 into the $\overline{\text{WAIT}}$ "off" state, and the next falling edge of the system clock

restores the $\overline{\text{WAIT}}$ signal to the "go" condition. During a processor read, U44 drives the bus during the

entire duration of $\overline{\text{REQ}}$.

3.2.2 The DMA machine grants the first available cycle to to the processor operation. There are two conditions which cause the processor to be denied the next sequential board cycle; display memory refresh, and the execution of a link sequence. Four or five cycle burst refresh is performed every scan line and a processor operation during this time will be delayed until the end of the refresh burst. If the first byte of a link has been read by the DMA machine, a processor operation (and for that matter, refresh) is held off until the second byte of the link is read and latched into the counter/sequencers.

3.2.3 During a processor I/O operation the $\overline{\text{WAIT}}$ line is pulled low by U66-6 through U510-9,8 and U710-9,8. During the next board cycle, U79-8 generates a strobe (I/O STROBE) that is used by the Display Control/Timing module to latch cursor data and mode information. The DMA machine is not affected by a processor I/O operation. The $\overline{\text{WAIT}}$ "off" condition is set at the end of the strobe through U39-10,8 and U111-11,13. The next falling edge of the system clock clears the $\overline{\text{WAIT}}$ line through U611.

3.3 REFRESH TIMING

3.3.1 Refresh is accomplished in burst mode, four or five refresh cycles occuring every scan line. Five cycles normally occur, four cycles occur only when the DMA machine cycle immediately before refresh is begun is the first half of a link. When this occurs, refresh is held off for one cycle while the second half of the link address is latched into the counter/sequencers.

4.0 HARDWARE DESCRIPTION

4.1 ADDRESS/DATA BUS BUFFERS/DRIVERS

4.1.1 The address and data bus buffers and drivers (U44, U52, U53, U54) are enabled only during processor display memory accesses. At this time all other "local" bus drivers are tri-stated. The local address bus ($\overline{\text{LA0}}$-$\overline{\text{LA13}}$) and display RAM data-out bus ($\overline{\text{LA0}}$-$\overline{\text{LA7}}$) are pulled high, the local display RAM data-in bus ($\overline{\text{D0}}$-$\overline{\text{D7}}$) is not.

4.1.2 During a procesor display memory READ, U44 is driving the backplane for the entire duration of $\overline{\text{REQ}}$. The data out of display RAM is passed transparently onto the backplane and latched at the end of the current board cycle.

4.2 RAM ADDRESS MULTIPLEXERS

4.2.1 The fourteen local address lines are split into two groups of seven and each group is selected by U48-9.

The row address is composed of $\overline{LA0}$-$\overline{LA7}$ and is changed to the column address ($\overline{LA8}$-$\overline{LA13}$) approximately 100 ns. after $\overline{RAS}$ goes low. The row address is again restored at the ouytputs of U42 and U43 at the end of $\overline{RAS}$.

4.3 REFRESH COUNTER

4.3.1 The refresh address counter (U35) is configured as an eight bit counter, of which only the least seven significant bits are used. The counter is strobed by the rising edge of U38-6 through U67-2,12 during valid refresh $\overline{RAS}$'s. U66-8 determines valid refresh cycles and accounts for DMA link fetches during the first cycle of the refresh period.

4.3.2 U32 is enabled only during valid refresh cycles, and drives the row addresses only.

4.4 DISPLAY MEMORY

4.4.1 Display memory consists of eight 16K x 1 RAM's. INTEL 2117-4 or equivalent RAM's are necessary to meet the access time requirement of no greater than 250 ns.

4.4.2 The data-in bus ($\overline{D0}$-$\overline{D7}$) comes directly from the backplane , buffered through U54. The data-out bus ($\overline{LD0}$-$\overline{LD7}$) is distinct from the data-in bus, and has several destinations: through U44 and onto the backplane, to the DMA machine address sequencers (U12, U22, U23, and U33), to the storage latch for the byte decoder (U45), to the ASCII character latch (U25), and to the enhancement latch (U26) through a bank of inverters (U46).

4.4.3 The hardware is configurable for both three supply and single supply RAM's. For three supply operation, load jumpers W1 and W2, and for single supply operation, load jumpers into the adjacent, unmarked jumper positions. This replacement of the jumpers routes +5 to all supply pins except ground.

4.5 DISPLAY CLOCK (VIDEO DOT CLOCK)

4.5.1 The display clock (21.34 MHz) is generated by a packaged oscillator (U47). This clock rate differs from the first generation 264X hardware (21.06 MHz) by 1.3% and is derived from the following formula:

DOT RATE = (DOTS PER CHARACTER) * (CHARACTERS PER SCAN LINE) * (SCAN LINES PER FRAME) * (FRAMES PER SECOND)
= 9 * 104 * 380 * 60 = 21.34 MHz

4.5.2 Note that the increase in frequency from the first generation 264X hardware stems from increasing the number of scan lines per frame from 375 to 380. This increase facillitates the use of the CRT controller on the Display Timing/Control module.

4.5.3 Note also that in 50 Hz mode, the number of scan lines per frame increases to 456 in order to use the same video dot frequency.

4.5.4 The display clock is buffered by U37-5,6 and U36-3,6. These two gates allow an external clock to be impressed upon the system. Grounding U37-4 (or test point "INH") inhibits the resident video clock and allows a clock of another frequency to be connected to U36-4,5 (or test point "EXT"). This port is the primary clock input for DTS-70 testing.

4.6 MOD 9 CHARACTER COUNTER

4.6.1 The display clock is divided by nine with a high speed counter (U24). The most significant digit (U24-11) is the character clock and pulses high once per character. This pulse train is sent over the topplane and fed directly to the CRT controller, among other places.

4.6.2 One half of U27 divides the character clock by two and defines the length of the board cycles (i.e. $\overline{\text{MEMCYC}}$ and MEMCYC). Each board cycle is 840 ns. long. At the beginning of each board cycle, $\overline{\text{MEMCYC}}$ goes low and U27-9 is clocked low. The next rising edge of U24-14 causes this zero to be shifted into the serial-in/parallel-out shift register (U38). The appearance of a low value at U38-3 (the first shift position) presets U27-9 back to the high state, where it remains until the beginning of the next board cycle. The next seven rising edges of U24-14 cause this low state to progress from U38-3 to U38-13 and effectively create eight clock phases in each board cycle. These eight phases are used to create all memory timing and control the operation of the DMA state machine.

4.7 $\overline{\text{RAS}}$/$\overline{\text{CAS}}$ GENERATION

4.7.1 Memory timing in this module is relatively conservative, most events occuring on even 85 ns. intervals.

If a memory cycle is pending, U110-2 ($\overline{\text{MCYC}}$) goes low just prior to the first character clock in a board cycle. This allows U38-3 to strobe $\overline{\text{RAS}}$ (U48-4) low through U28-12,11. Approximately 85 ns. later, U38-4 goes low and the row address is changed to the column address through U48-10,9. 85 ns. after the address swap, $\overline{\text{CAS}}$ is brought low by U38-5 through U28-10,8 and U48-5,7.

4.7.2 When a low level is shifted into U38-10, $\overline{\text{RAS}}$ is brought high, and the row address is restored to the outputs of the address multiplexers. This timing allows

for a very long $\overline{RAS}$ precharge time, and is arbitrary as far as the RAM address goes.

$\overline{CAS}$ returns to a high state as a result of the first character clock (U24-11) of the next board cycle through U410-1,3 and U48-6,7.

4.8 MISCELLANEOUS BOARD CYCLE TIMIMG

4.8.1 Qd, the signal at U38-6, occurs in the middle of a board cycle. It is used for general timing at U510-13 and U69-3 and to mask the second character clock in a board cycle at U410-2.

4.8.2 The sample clock (U38-10) will pulse low 200 ns. after $\overline{CAS}$ goes low. The data at the output of the RAM array is latched into U45 and U25 with the sample clock.

4.8.3 The increment clock (U38-11) strobes the MOD 80 character counter (U411/U511) through U310-3,1, U211, and U34-9.8. This clock phase also releases the "processor wait" mode through U78-1,2, U39-13,11, U111-12,13, and U611.

4.8.4 The video shift clock (P3-19 and U49-9) is basically a train of eighty 200+ ns. pulses. This pulse train is synchronized by P3-X and is used by the recirculating line buffers in the Display Timing/Control module.

4.8.5 $\overline{DOT\ \overline{2}}$ (P3-C and U28-6) is a synchronization signal used by the graphics board set (02640-????? and -?????) and aligns the graphics output within the character cell. Care must be taken that a negative edge of P3-A occurs during the active low portion of $\overline{DOT\ \overline{2}}$ for proper graphics module operation.

4.8.6 The next state clock (U310-10) is a positive pulse at the end of each board cycle. This clock strobes the registers of the DMA state machine (U110, U210, and U57-11) and configures those devices for the upcoming board cycle.

4.9 DMA ADDRESS SEQUENCERS

4.9.1 Direct memory access address sequencing is performed by four 2911A integrated circuits (U12, U22, U23, U33). These are four bit-slice, bipolar, 60 ns. parts--Good Stuff! See some National or AMD spec sheets for details.

4.9.2 The DMA address is forced to zero at the end of each frame by the action of P3-J (vertical blanking) through

U57-3 and pin #9 ($\overline{\text{ZERO}}$) of each 2911A. This physical 0000 maps into a logical FFFF through the inverted bus structure. In fact, The binary "up" counter internal to the 2911A sequencer becomes a binary "down" counter with the inverted bus. It is with these counters that the DMA address sequencing is performed.

4.9.3 During link operations, the bank of 2911A's fetches the two bytes of a sixteen bit link address through the external data port (pins 4,5,6,7 of each 2911A). Control signal JUMP (U58-8) causes the latched data to be impressed onto the local address bus resulting in a sequencing "jump" to the link address.

4.10 ZERO ADDRESS GENERATOR

4.10.1 The start of vertical blanking forces U57-5 low and U57-6 (P3-E) high. These signals force the DMA address to 0000, reset the DMA machine to top-of-frame, and clear the DMA row counter in the Display Timing/Control module.

4.10.2 The zero signal is returned to its inactive state with the first 2911A clock of the frame through U34-3,4. The rising edge of this clock latches the 0000 address inside the 2911A and then removes the zero condition so that proper address sequencing can be performed.

4.11 HSYNC SYNCRONIZATION

4.11.1 HSYNC (P3-S) is a signal sent from the CRT controller in the Display Timing/Control module. This signal occurs once per raster line within the horizontal retrace interval, and is used to force the DMA state machine into memory refresh mode.

4.11.2 The CRT controller does not allow for specific start-up states (i.e. ther are no preset or clear capabilities). As a consequence it is impossible to determine the exact alignment of HSYNC (nine char. wide) within the two character wide board cycle.

4.11.3 The circuit consisting of U69 (FF#2), U79-1,2,3 and U59-1,2,3 guarantees that the output signal, U69-9, is aligned properly within the board cycle.

In the middle of a board cycle, $\overline{\text{MEMCYC}}$ goes high. When HSYNC is present, U69-9 is clocked high by

$\overline{\text{MEMCYC}}$. When HSYNC returns to its inactive state,

the next low level of $\overline{\text{MEMCYC}}$ clears U69-9. This alignment provides proper synchronization between the DMA state machine and the hardware it controls.

4.11.4 A high state at U59-8 (HSYNC+SLOAD) indicates that a burst refresh period is pending. If a link is not being fetched by the DMA machine, the board is configured into refresh mode. If a link is being fetched, this configuration is held off for one board cycle with U66-9 and the state machine logic.

4.11.5 After burst refresh has been accomplished, HSYNC, U59-8, U57-9, and U66-8 become sequentially inactive, and the board is configured for DMA and processor operations.

4.12 ASCII AND ENHANCEMENT STORAGE LATCHES

4.12.1 These two devices (U25 and U26) are used to store character data from display memory and present this data over the topplane to the Display Timing/Control module. U25 is strobed by the sample clock (U38-10) every board cycle. The enhancement latch, U26, is strobed by the increment clock through U78-1,2 and U410-10,8 only when an enhancement is fetched from memory as determined by U28-1,2,3 and U67-3,4,5,6. Characters are stored in U25 in complemented form and enhancements are stored in true form through the action of the inverter bank of U46.

4.12.2 When a character is fetched from memory, U25 is loaded with that character, U26 already contains the proper enhancement. A strobe is sent over the topplane shifting this character cell data into one set of the recirculating line buffers in the Display Timing/Control module.

4.13 DISPLAY MEMORY BYTE DECODER

4.13.1 The display memory byte decoding circuitry determines the type of data fetched during each DMA board cycle. U45 is strobed by the sample clock, and its outputs are impressed upon the address lines of U55, a 256X4 PROM. A character byte causes U56-10,8 to go high, thereby disabling the PROM outputs. All other types of memory data are decoded by the PROM and the proper output is brought low. These outputs configure the board into the proper mode to respond correctly to the byte that has been fetched.

4.13.2 The contents of the display memory byte decoder PROM are as follows:

```
HP PART NUMBER: 1816-1484
USED ON ASSEMBLY 02640-60250 (DISPLAY MEMORY/DMA) U55
FUNCTION: DISPLAY MEMORY BYTE DECODER
OUTPUT DEFINITION:
     01--ENHANCEMENT          (NEGATIVE TRUE)
     02--LINK                 (    "        " )
     03--END OF LINE          (    "        " )
     04--END OF PAGE          (    "        " )
ROM GENERIC PART NUMBER: 7611A (256X4)
ROM CONTENTS:

$A0000.
D,D,D,D,D,D,D,D,D,D,D,D,D,D,D,D,
D,D,D,D,D,D,D,D,7,B,F,F,F,F,F,F,
E,E,E,E,E,E,E,E,E,E,E,E,E,E,E,E,
E,E,E,E,E,E,E,E,E,E,E,E,E,E,E,E,
D,D,D,D,D,D,D,D,D,D,D,D,D,D,D,D,
D,D,D,D,D,D,D,D,7,B,F,F,F,F,F,F,
E,E,E,E,E,E,E,E,E,E,E,E,E,E,E,E,
E,E,E,E,E,E,E,E,E,E,E,E,E,E,E,E,

$A0080.
D,D,D,D,D,D,D,D,D,D,D,D,D,D,D,D,
D,D,D,D,D,D,D,D,7,B,F,F,F,F,F,F,
E,E,E,E,E,E,E,E,E,E,E,E,E,E,E,E,
E,E,E,E,E,E,E,E,E,E,E,E,E,E,E,E,
D,D,D,D,D,D,D,D,D,D,D,D,D,D,D,D,
D,D,D,D,D,D,D,D,7,B,F,F,F,F,F,F,
E,E,E,E,E,E,E,E,E,E,E,E,E,E,E,E,
E,E,E,E,E,E,E,E,E,E,E,E,E,E,E,E,

  SUM=0D90
```

4.14 DISPLAY MEMORY BUS DECODING

4.14.1 In the 264X memory mapping scheme, display memory resides in the top 16K bytes of a 64K address space.

(i.e. $\overline{\text{ADDR 14}}$ and $\overline{\text{ADDR 15}}$ are physically 00). In the first generation 264X hardware (i.e. 2642A and earlier models), P1-V,W, and X are bottomplane contention and arbitration signals. The second generation hardware removes this contention and uses these three bottomplane lines as address lines, essentially giving the terminal a total address space of 8 times 64K bytes. Within this scheme, display memory resides in the top 16K bytes of the bank accessed when P1-V,W, and X become physically 111. When using this board set with the first generation hardware, the switch bank at U18 should be set to all "open" causing this module to ignore the bus contention signals. In the 2647F, this switch bank should be set to all "closed" in order to respond to the display/IO bank only.

4.14.2 The pertinent signals generated by this block of circuitry are U68-8 (MEMSELECT) and U710-11 ($\overline{\text{uPREAD}}$). MEMSELECT indicates that the processor is accessing display memory and $\overline{\text{uPREAD}}$ indicates that the processor is performing a display memory read. This latter signal enables U44 to drive the bottomplane data bus with the memory data-out.

4.15 CURSOR CONTROL BUS DECODING AND CRT CONTROLLER STROBE GENERATION

4.15.1 Cursor control is achieved through two I/O ports, one for cursor column and one for cursor row. A processor I/O write to either port causes P3-5 (U66-6 or $\overline{\text{I/O SELECT}}$) to go low. P3-5 sets up the proper CRT controller address for cursor control and eventually allows U24-12 to generate an I/O STROBE on P3-2 through U79-9,8.

4.16 BUS INTERPRETATION AND $\overline{\text{WAIT}}$ GENERATION

4.16.1 This portion of circuitry essentially synchronizes the processor (with its 4.915 MHz. clock) with the display memory cycles defined previously. In order to do this successfully, the $\overline{\text{WAIT}}$ line (P1-S) is pulled low immediately upon the decoding of either a display memory access or an I/O access. This causes the processor to go into numerous "wait" states while this module completes its present actions and prepares for external interaction.

4.16.2 Upon the receipt of either MEMSELECT or I/O SELECT, U510-8 goes high, P1-S goes low and U79-11 goes high. Halfway through each board cycle, U69-3 is strobed and the processor status is sampled. If a processor operation is pending, U69-5 will go high and U69-6 will go low.

4.16.3 If it is a display memory access that has caused this, U79-6 will go high, signalling to the DMA state machine that the processor wants into display memory. This status line is sampled several hundred nanoseconds later by the DMA state machine to allow for possible "runt" pulses at U69-5 due to the lack of proper setup time at U69-2. The same delay is true for the I/O STROBE. If an I/O write is pending, the DMA state machine doesn't care and U111 goes high, allowing an I/O STROBE to be generated on P3-2.

4.16.4 The completion of a display memory access is signalled by U39-11 going high. The completion of an I/O write is signalled by U39-8 going high. Either of these events causes U611-1 to be strobed through U111-11,12,13 and U611-5 will go low and U611-6 will go high. A low state at U611-5 clears U69-1 and disables the processor status line and the I/O STROBE. The high state at U611-6 is clocked into a low state at U611-9 by the next falling edge of the system clock (P1-3). U611-9 going low causes the $\overline{\text{WAIT}}$ condition to be released, allowing the processor to proceed on its merry way. When $\overline{\text{REQUEST}}$ (P1-Y) is brought high by the processor, this $\overline{\text{WAIT}}$ generation machine is primed for another processor access.

4.17 PROM DRIVEN DMA STATE MACHINE

4.17.1 The DMA state machine consists of two 60 ns. 256X4 PROMs and two schottky latches. The address lines of the PROMs are the basic status lines of this module and convey such information to the DMA state machine as the present mode of operation, frame timing, processor status, and refresh timing. U29 is the cycle arbitrator and determines whether the pending board cycle is a processor operation (uPOP), a normal DMA cycle (DMACYC), or a DMA link operation (DMACYC and RE1). U19 controls the special DMA modes. Its outputs are end-of-line (EOL), end-of-page (EOP), skip end-of-line ($\overline{\text{SKIPEOL}}$), and $\overline{\text{END EOL+EOP}}$.

4.17.2 The contents of the two DMA state machine PROM's are as follows:

HP PART NUMBER: 1816-1485
USED ON ASSEMBLY 02640-60250 (DISPLAY MEMORY/DMA) U29
FUNCTION: DMA CYCLE ARBITRATOR
OUTPUT DEFINITION:

O1--DMA CYCLE	(POSITIVE TRUE)
O2--MICROPROCESSOR CYCLE	(" ")
O3--MEMORY CYCLE	(NEGATIVE TRUE)
O4--REGISTER ENABLE 1	(POSITIVE TRUE)

ROM GENERIC PART NUMBER: 7611A (256X4)
ROM CONTENTS:

```
$A0000.
C,C,C,C,9,9,C,C,C,C,C,C,9,9,C,C,
4,2,4,2,1,2,4,2,4,4,4,4,4,4,4,4,
C,C,C,C,9,9,C,C,C,C,C,C,9,9,C,C,
4,2,4,2,4,2,4,2,4,4,4,4,4,4,4,4,
1,2,4,2,1,2,4,2,4,4,4,4,4,4,4,4,
1,2,4,2,1,2,4,2,4,4,4,4,4,4,4,4,
4,2,4,2,4,2,4,2,4,4,4,4,4,4,4,4,
4,2,4,2,4,2,4,2,4,4,4,4,4,4,4,4,

$A0080.
4,4,4,4,1,1,4,4,4,4,4,4,4,4,4,4,
4,2,4,2,1,2,4,2,4,4,4,4,4,4,4,4,
4,4,4,4,1,1,4,4,4,4,4,4,4,4,4,4,
4,2,4,2,4,2,4,2,4,4,4,4,4,4,4,4,
1,2,4,2,1,2,4,2,4,4,4,4,4,4,4,4,
1,2,4,2,1,2,4,2,4,4,4,4,4,4,4,4,
4,2,4,2,4,2,4,2,4,4,4,4,4,4,4,4,
4,2,4,2,4,2,4,2,4,4,4,4,4,4,4,4,

  SUM=045E
```

HP PART NUMBER: 1816-1486
USED ON ASSEMBLY 02640-60250 (DISPLAY MEMORY/DMA) U19
FUNCTION: END OF MODES CONTROL
OUTPUT DEFINITION:

01--END OF LINE	(POSITIVE TRUE)
02--END OF PAGE	(" ")
03--SKIP END OF LINE	(NEGATIVE TRUE)
04--END EOL OR EOP	(" ")

ROM GENERIC PART NUMBER: 7611A (256X4)
ROM CONTENTS:

```
$A0000.
F,E,D,C,F,E,D,C,6,E,4,C,6,E,4,C,
F,E,D,C,F,E,F,E,6,E,4,C,6,E,6,E,
F,E,D,C,B,E,9,C,6,E,4,C,2,E,0,C,
F,E,D,C,F,E,D,C,6,E,4,C,6,E,4,C,
C,C,C,C,C,C,C,C,4,C,4,C,4,C,4,C,
C,C,C,C,C,C,C,C,4,C,4,C,4,C,4,C,
C,C,C,C,8,C,8,C,4,C,4,C,0,C,0,C,
C,C,C,C,C,C,C,C,4,C,4,C,4,C,4,C,

$A0080.
5,4,D,C,5,4,D,C,4,4,4,C,4,4,4,C,
5,4,D,C,5,4,D,C,4,4,4,C,4,4,4,C,
5,4,D,C,1,4,9,C,4,4,4,C,0,4,0,C,
5,4,D,C,5,4,D,C,4,4,4,C,4,4,4,C,
4,4,C,C,4,4,C,C,4,4,4,C,4,4,4,C,
4,4,C,C,4,4,C,C,4,4,4,C,4,4,4,C,
4,4,C,C,0,4,8,C,4,4,4,C,0,4,0,C,
4,4,C,C,4,4,C,C,4,4,4,C,4,4,4,C,

  SUM=08A8
```

4.18 CHARACTER AND BLANK FILL SHIFT CLOCK GENERATOR

4.18.1 The line buffers resident in the Display Timing/Control module are loaded with a row of characters under the control of the Display Memory/DMA module. When a valid ASCII character is "DMA'ed" from display memory, U211-8 will go low through the action of U211-1,11,12,13. When blank fill mode is invoked (i.e. under end-of-line or end-of-page conditions), U111-4 will go high, U25 will be loaded with an ASCII 20H (blank) every DMA cycle, and U211-8 will go low through the action of U211-4,5,6. U211-8 goes low as a result of INCCLK (U38-11) through U310-3,1. This clock comes late in a board cycle. The low state at U211-8 strobes the eighty character counter (U411 and U511) through U34-9,8, and presets U49-5 to a high state. U49-5 goes directly over the topplane to the Display Timing/Control module and determines when a valid character/enhancement pair is loaded into a line buffer. The actual load occurs early in the following board cycle, when U49-5 goes low through the action of Qc (U24-12). Note that U49-6 is fedback to this clock generator through U37-13,11, U78-11,10, and U310-2,1. This circuitry prevents errant clocking of the eighty counter as the decoded outputs of U411 change states, particularily at character sixty-four.

4.19 EIGHTY CHARACTER COUNTER

4.19.1 The eight bit counter made from U411 and U511 counts the number of valid character/enhancement pairs that have been loaded into the line buffers in the Display Timing/Control module. The count is incremented by U211-8 as described above. When a count of eighty has been reached, U311-6 goes high from U411-14,12 and U311-4,5. U311-6 (80) is a status line to the DMA state machine. When U311-6 goes high, the DMA state machine discontinues direct memory access because eighty characters have been loaded into the line buffers. Direct memory access is restarted at the beginning of the next data or character row as indicated by P3-15, EDROW (end of data row).

4.20 JUMP TO LINK ADDRESS COORDINATION CIRCUITRY

4.20.1 The circuit block made up from U58, 1/2 of U711, and 1/2 of U510 controls the sequence of events that are necessary to fetch a link address from display memory and perform a "jump" to the fetched address to begin direct memory access at the link address. The events are very specific and exact and are defined as follows:

1) a link byte is read from display memory as identified by its characteristic code,
2) the DMA state machine goes into a mode by which the link byte and the next sequential byte of display memory are latched within the DMA address sequencers (U12, U22, U23, and U33),
3) upon latching the second byte of the link address, the address sequencers are configured to impress the internal latch contents onto the display memory address bus (as opposed to the internal incrementer contents as during "normal", sequential DMA),
4) the first DMA cycle immediately following the latching of the second address byte is performed at the link address and a jump has been completed.

4.20.2 When a link byte has been fetched from display memory,

$\overline{\text{LINK}}$ (U55-11) will go low, U29-9 will go high, and during the following board cycle U210-7 will be high

and U210-6 ($\overline{\text{RE1}}$--register enable #1) will be low.

$\overline{\text{RE1}}$ being low causes the display memory link byte to be latched into U23 and U33 on the rising edge of the 2911 clock (U311-8), and presets U711-8,9

($\overline{\text{LINK}}$'' and LINK'') to states that indicate to the DMA state machine that a link operation is being performed. RE1 is delayed by one board cycle (U210-7 to U210-4) and creates the signals RE2 and

$\overline{\text{RE2}}$ (U210-2,3). The DMA state machine fetches the next sequential byte from display memory and this byte is latched into U12 and U22.

4.20.3 $\overline{\text{RE2}}$ presets U58-6 indicating that both bytes of the link have been fetched and latched. U58-11 is clocked the beginning of every DMA cycle. The normal state of U58-6 is high such that "normal" DMA cycles are performed with U58-8 (JUMP) low. Once U58-6 is preset low, a high state gets clocked into U58-8, and the first DMA cycle following this event is performed using the latched link bytes as the DMA address instead of the "normal" incrementer address of the 2911's.

4.20.4 As this jump is performed, U58-9 clears U58-6 back to the non-jump state, and U711-11 is clocked through the two gates from U510. This removes the LINK'' signal from the input of the DMA machine, and allows the state machine to continue with "normal" DMA.

4.20.5 Note that events can occur between the latching of the second link byte and the actual jump such as display memory refresh and processor memory access. Also note that U711-8 keeps the second byte of the link from being interpretted as a character through U211-13.

4.21 SKIP END-OF-LINE CIRCUITRY

4.21.1 The skip end-of-line circuit prevents the DMA state machine from misinterpreting the software data structure as the processor is adding characters to the screen. Two status bits imbedded in the "cursor row" byte latched in the Display Timing/Control module (I/O BIT5 and I/O BIT6) indicate when a skip end-of-line operating mode is applicable. When skip end-of-line mode is invoked, U19-10 and U110-15 will go low and preset U610. EDR (end data row) samples the status of U610-9 through U410-13,12,11 and if EOL's are to be skipped, U610-5,6 will be preset. These outputs prevent the DMA state machine from reacting to EOL's (U56-11,12,13), characters (U311-1,2,3), and enhancements (U28-1,2,3).

4.21.2 Skip end-of-line moded is turned off when a link is fetched that points to the beginning of the next row on the screen. This is indicated by the least significant nibble of the link address being 1111. Under these circumstances, U65-6 will go high, and U610-5,6 will be clocked to their "normal" state when the second register enable signal (RE2) goes high.

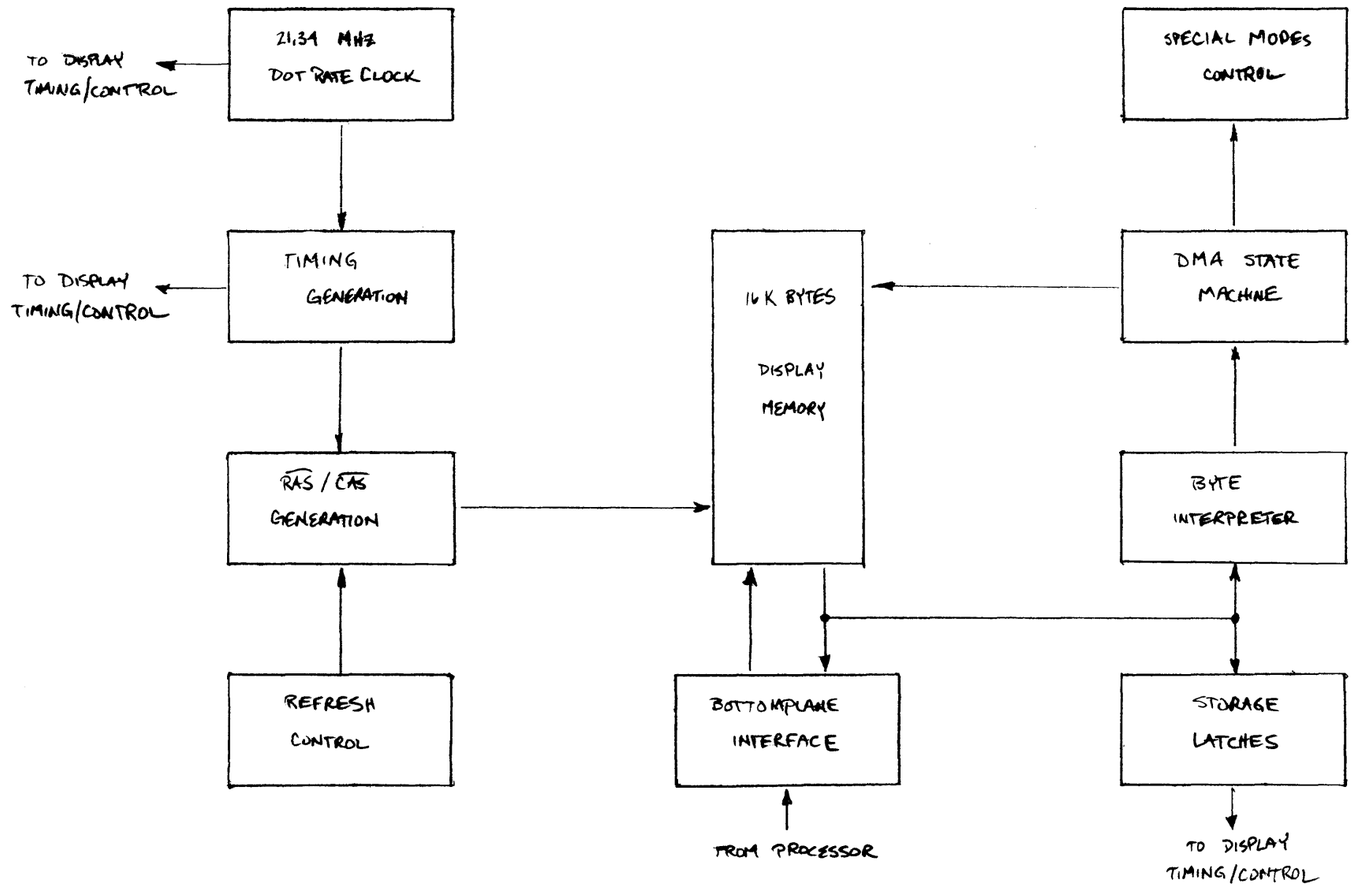
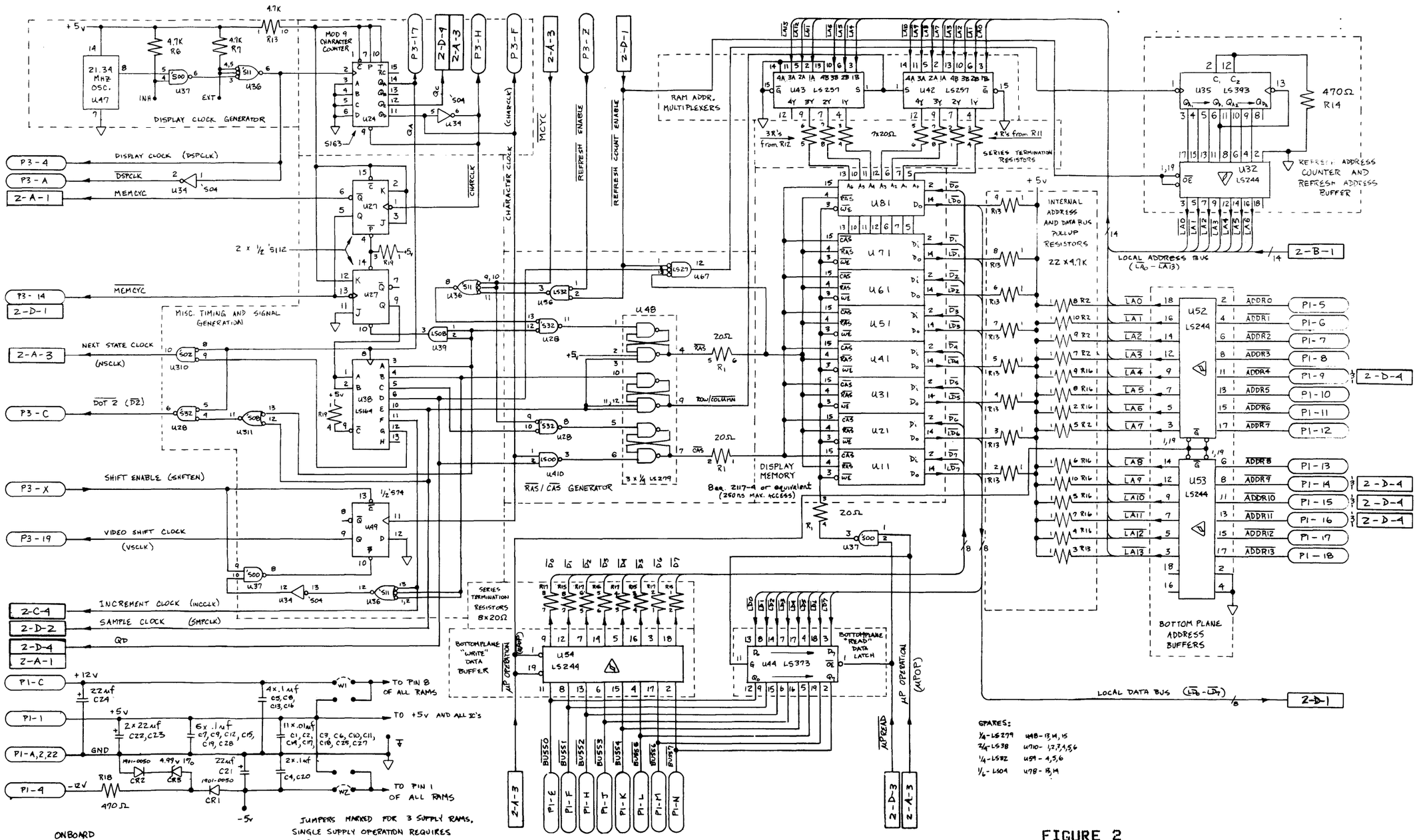


FIGURE 1
02640-60250 BLOCK DIAGRAM
FEB-01-82 13255-91250



EDGE CONNECTION: XX-XX — CONNECTOR - FINGER

ONBOARD CONNECTION: X-X-X — PAGE - V. COORDINATE - H. COORDINATE

FIGURE 2
DISPLAY MEMORY/DMA SCHEMATIC (PAGE 1)
FEB-01-82 13255-91250

DMA ADDRESS SEQUENCERS

LOCAL ADDRESS BUS ($\overline{LA_0}$ - $\overline{LA_{13}}$)

LOCAL DATA BUS ($\overline{LD_0}$ - $\overline{LD_7}$)

CHARACTER AND BLANK FILL SHIFT CLOCK GENERATOR

80 CHARACTER COUNTER

JUMP TO LINK ADDRESS COORDINATION CKTRY.

SKIP END OF LINE CKTRY.

START AT TOP OF DISPLAY MEMORY "ZERO" ADDRESS GENERATOR

HSYNC SYNCRONIZATION AND REFRESH ENABLE CKTRY.

NEXT LINE POINTER FLAG

EOL OR EOP INHIBIT LATCH

ASCII + ENHANCEMENT STORAGE LATCHES

DISPLAY MEMORY BYTE DECODER

PROM DRIVEN DMA STATE MACHINE

BUS INTERFERENCE AND WAIT GENERATION CKTRY.

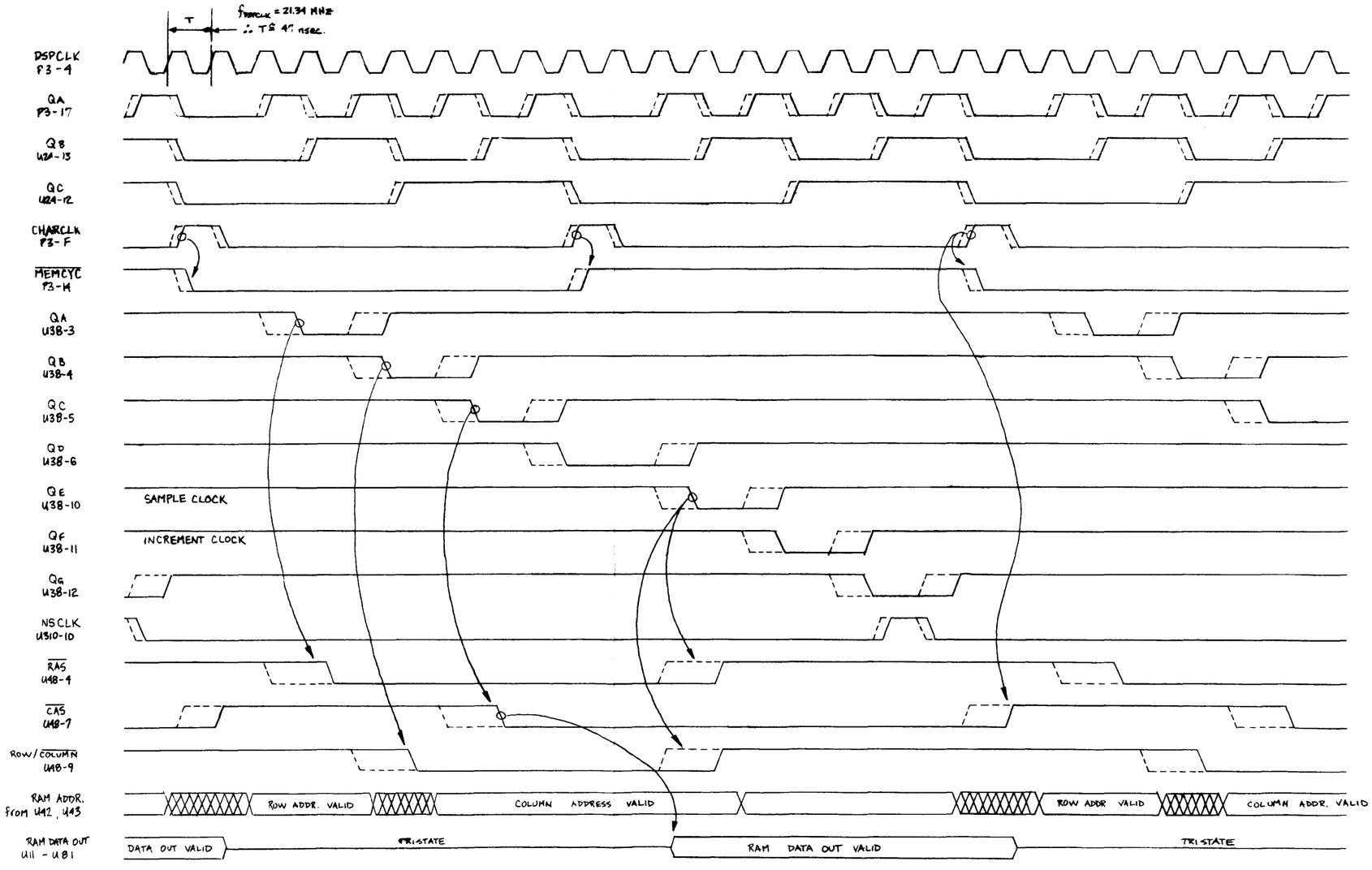
CURSOR CONTROL BUS DECODE AND CRT CONTROLLER STROBE GEN.

DISPLAY MEMORY BUS DECODE

EDGE CONNECTION: XX-XX — CONNECTOR - FINGER

ONBOARD CONNECTION: X-Y-X — PAGE - V. COORDINATE - H. COORDINATE

FIGURE 3
DISPLAY MEMORY/DMA SCHEMATIC (PAGE 2)
FEB-01-82 13255-91250



SOLID LINES INDICATE WORST CASE DELAY TIMES
DOTTED LINES INDICATE MINIMAL (N 1-2nsec) DELAY TIMES

FIGURE 4
DISPLAY MEMORY AND MISC. TIMING
FEB-01-82 13255-91250

MISCELLANEOUS BOARD TIMING

I. $\overline{\text{MEMCYC}}$ DEFINES THE LENGTH OF ONE BOARD CYCLE
((A1) to (A2) ⇒ ONE CYCLE)

II. U38 (LS164) IS USED TO GENERATE SEVEN CLOCK PHASES USED TO CONTROL ALL BOARD TIMING.

- (B) THIS EDGE STARTS $\overline{\text{RAS}}$
- (C) THIS EDGE SWAPS ROW AND COLUMN ADDRESSES
- (D) THIS EDGE STARTS $\overline{\text{CAS}}$
- (E) THIS LOW SAMPLES RAM DATA OUT
- (F) THIS LOW STOPS $\overline{\text{RAS}}$ AND ROW/$\overline{\text{COLUMN}}$. INCREMENTS EIGHTY CHARACTER COUNTER
- (G) THIS LOW GENERATES NSCLK

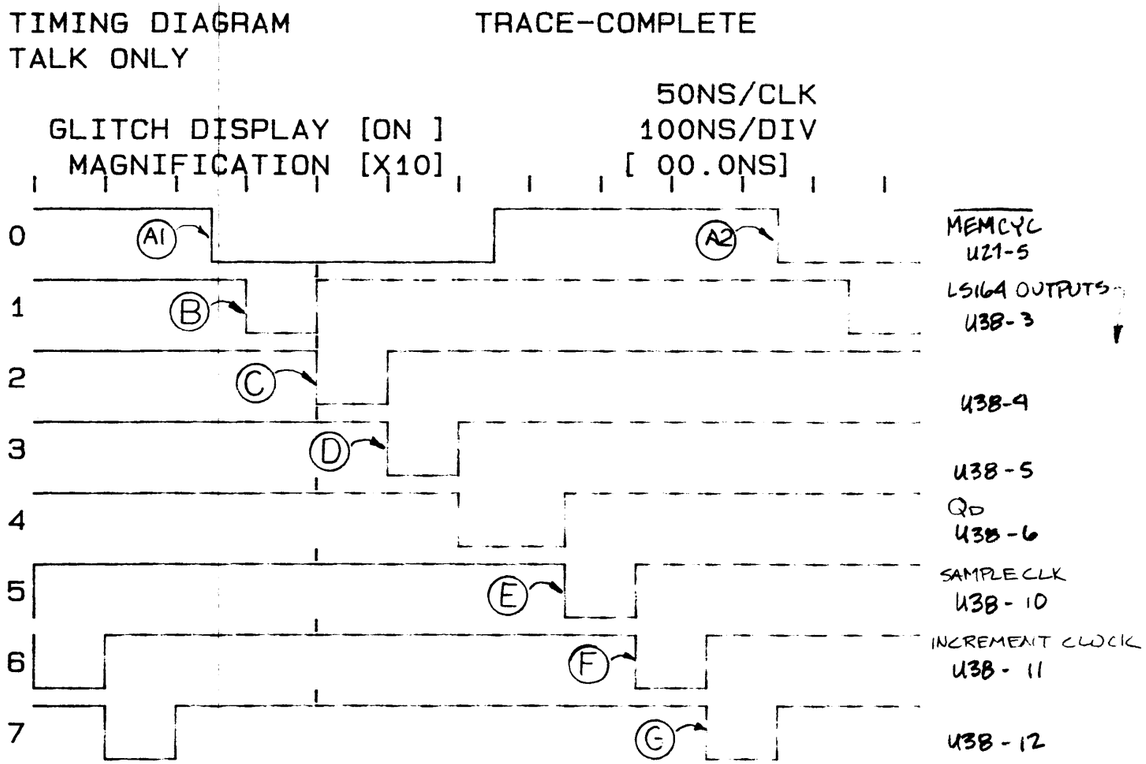


FIGURE 5
MISCELLANEOUS BOARD TIMING
FEB-01-82 13255-91250

$\overline{RAS}$ / $\overline{CAS}$ GENERATION

I. $\overline{MEMCYC}$ AND MEMCYC DEFINE THE LENGTH OF A BOARD MEMORY CYCLE. (A1 to A2 ⇒ ONE CYCLE)

II. LENGTH OF $\overline{CAS}$ HOLDS RAM DATA-OUT VALID THROUGH DURATION OF BOARD CYCLE.

III. NSCLK SIGNALS THE END OF A BOARD CYCLE.

IV. $\overline{D2}$ IS A SYNCHRONIZATION SIGNAL TO THE GRAPHICS MODULE

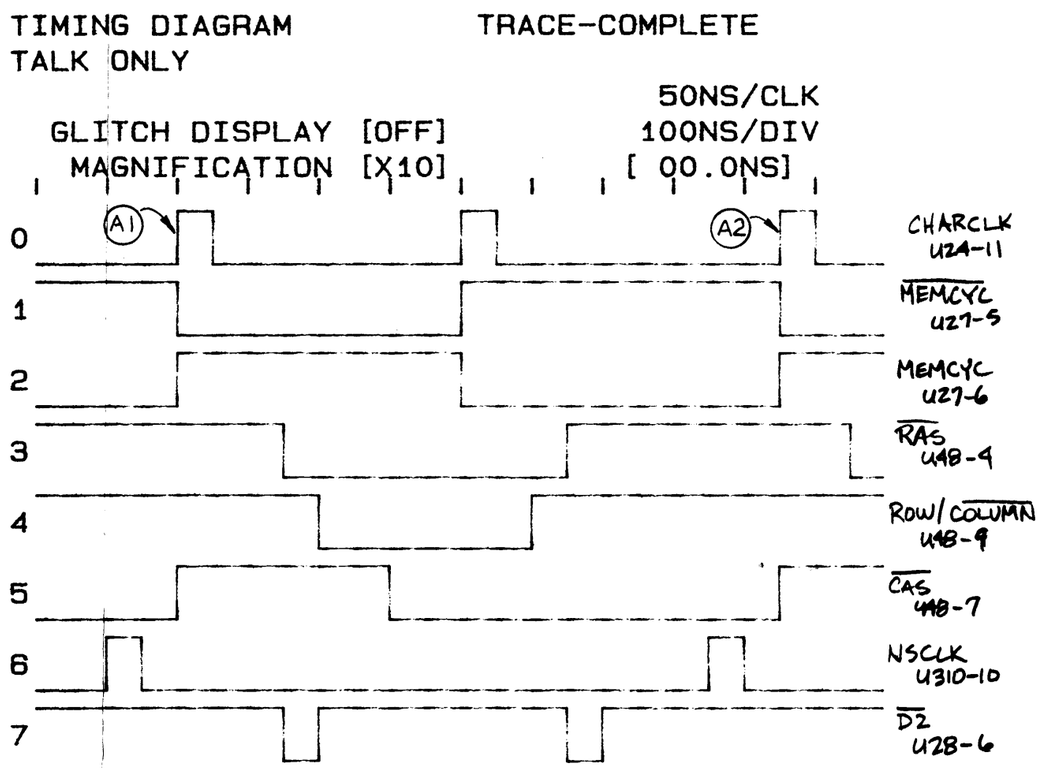


FIGURE 6
RAS/CAS GENERATION
FEB-01-82 13255-91250

REFRESH TIMING (A)

I. SHFTEN ROUGHLY CORRESPONDS TO HORIZONTAL RETRACE PERIOD.

II. HSYNC COMES FROM CRT CONTROLLER IN DISPLAY TIMING/CONTROL MODULE, HSYNC FORCES THE DMA STATE MACHINE TO DO MEMORY REFRESH.

III. VSCLK IS USED BY THE DISPLAY TIMING/CONTROL MODULE TO RECIRCULATE CHARACTER DATA FOR VIDEO DISPLAY

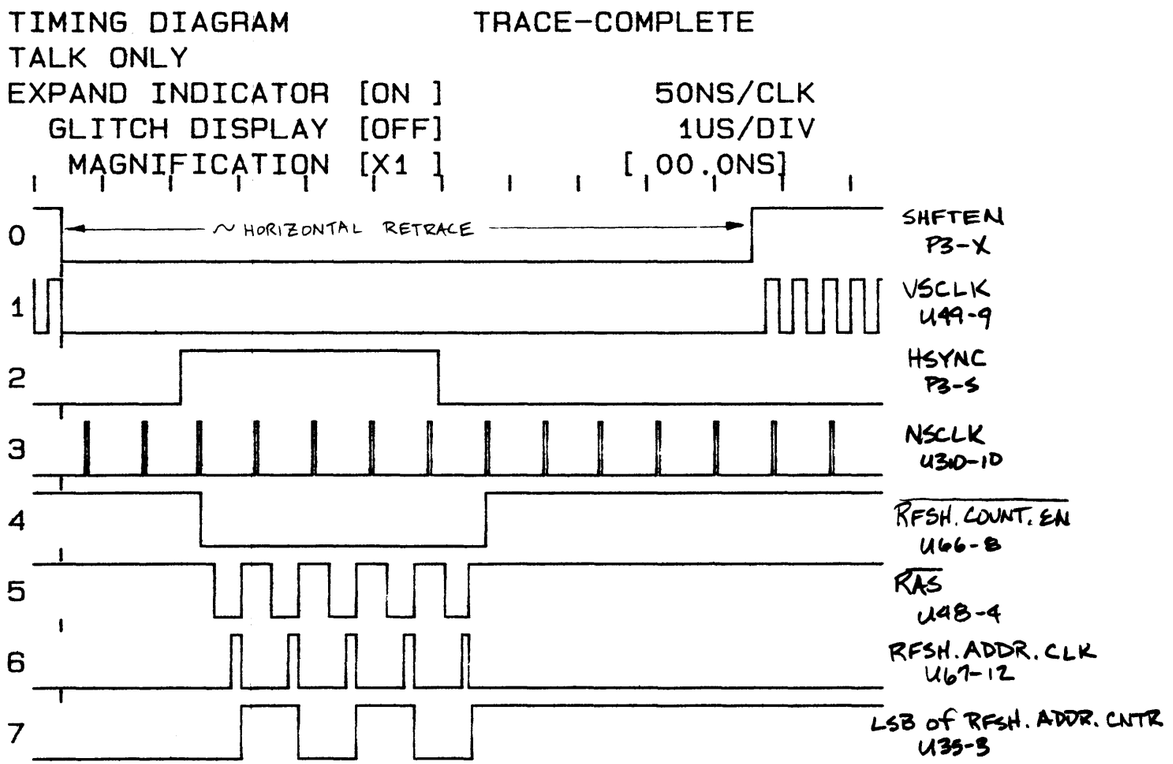


FIGURE 7
REFRESH TIMING (A)
FEB-01-82 13255-91250

REFRESH TIMING (B)

I. SHFTEN ROUGHLY CORRESPONDS TO HORIZONTAL RETRACE PERIOD.

II. HSYNC CAUSES REFRESH TO OCCUR DURING EACH HORIZONTAL RETRACE PERIOD.

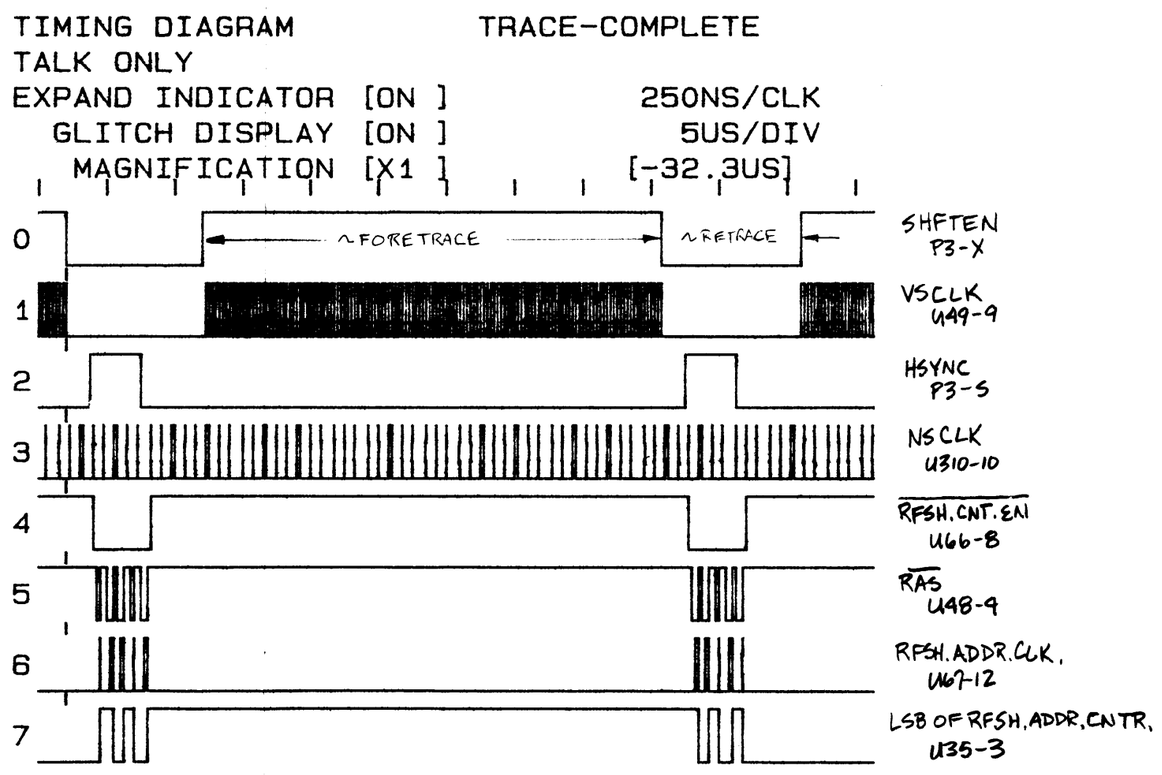


FIGURE 8
REFRESH TIMING (B)
FEB-01-82 13255-91250

PROCESSOR DISPLAY MEMORY ACCESS (A)

I. EACH $\overline{\text{REQUEST}}$ CYCLE INDICATES A PROCESSOR MACHINE CYCLE,

II. WAIT (LOCAL) IS DERIVED FROM ADDRESS BITS 14, 15, 16, 17, AND 18,

III. DISPLAY MEMORY ACCESS (A) OCCURS BETWEEN SUCCESSIVE DMA CYCLES,

IV DISPLAY MEMORY ACCESS (B) OCCURS DURING MEMORY REFRESH. NOTE THAT PROCESSOR ACCESS IS DELAYED UNTIL REFRESH IS COMPLETE,

V. MPREQ SIGNALS THAT A PROCESSOR ACCESS IS PENDING,

VI MPOP DISPLAYS WHICH BOARD CYCLE IS GRANTED FOR PROCESSOR ACCESS.

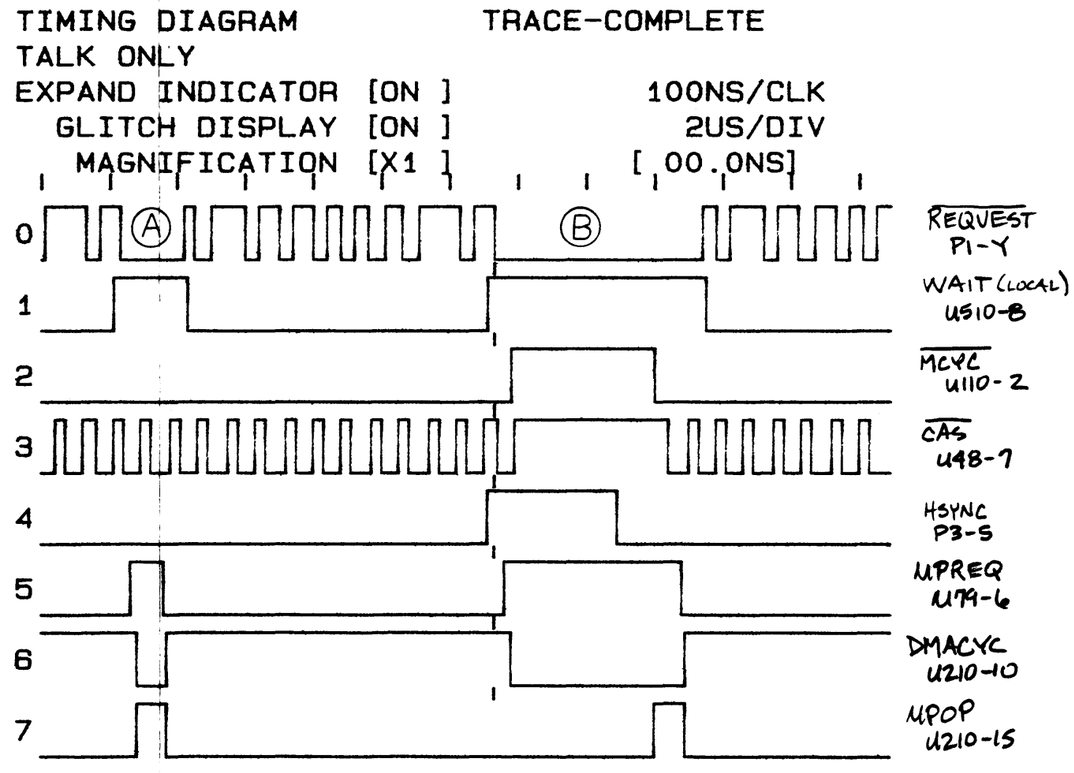


FIGURE 9
PROCESSOR DISPLAY MEMORY ACCESS (A)
FEB-01-82 13255-91250

PROCESSOR DISPLAY MEMORY ACCESS (B)

I. EACH $\overline{\text{REQVEST}}$ CYCLE INDICATES A PROCESSOR MACHINE CYCLE.

II. WAIT (LOCAL) IS DERIVED FROM ADDRESS BITS 14,15,16,17 AND 18.

III. DISPLAY MEMORY ACCESS (A) OCCURS BETWEEN SUCCESSIVE DMA CYCLES (i.e. DMACYC HIGH)

IV. DISPLAY MEMORY ACCESS (B) OCCURS WHEN DMA IS NOT ACTIVE.

V. MPREQ SIGNALS THAT A PROCESSOR ACCESS IS PENDING.

VI. MPOP DISPLAYS WHICH BOARD CYCLE IS GRANTED FOR PROCESSOR ACCESS.

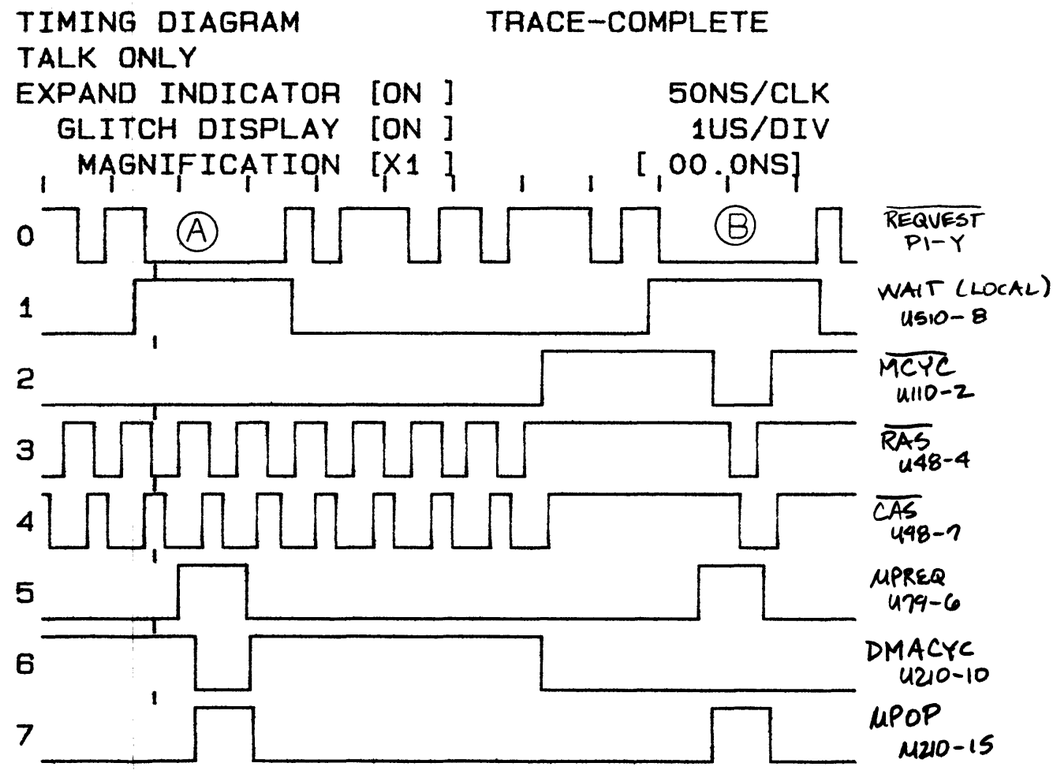


FIGURE 10
PROCESSOR DISPLAY MEMORY ACCESS (B)
FEB-01-82 13255-91250

JUMP TO LINK ADDRESS TIMING (A)

I. $\overline{\text{LINK}}$ INDICATES WHEN A LINK BYTE HAS BEED DMA'ED FROM DISPLAY MEMORY.

II. JUMP DISPLAYS THE PARTICULAR DMA CYCLE IN WHICH THE "LINK" ADDRESS IS IMPRESSED UPON THE DISPLAY MEMORY ADDRESS BUS.

III. JUMPS (A) AND (B) SHOW AN UNINTERRUPTED "DOUBLE LINK" OR "LINK TO A LINK" SEQUENCE.

IV. JUMP (C) IS INTERRUPTED BY A BURST REFRESH PERIOD, AND THE JUMP IS DELAYED BY SEVERAL BOARD CYCLES.

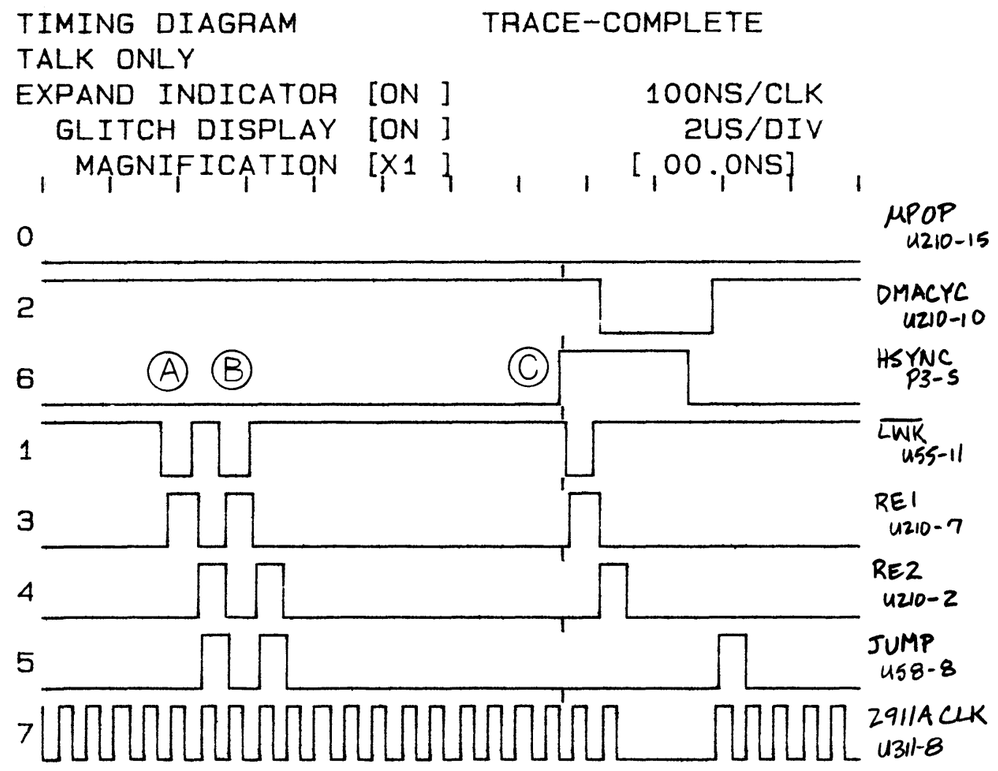


FIGURE 11
JUMP TO LINK ADDRESS (A)
FEB-01-82 13255-91250

JUMP TO LINK ADDRESS TIMING (B)

I. $\overline{\text{LINK}}$ INDICATES WHEN A LINK BYTE HAS BEEN DMA'ed FROM DISPLAY MEMORY.

II. JUMP DISPLAYS THE PARTICULAR DMA CYCLE IN WHICH THE "LINK" ADDRESS IS IMPRESSED UPON THE DISPLAY MEMORY ADDRESS BUS.

III. JUMP (A) IS A "NORMAL", UNINTERRUPTED JUMP SEQUENCE.

IV. JUMP (B) IS INTERRUPTED BY A PROCESSOR ACCESS AND DELAYED ONE BOARD CYCLE

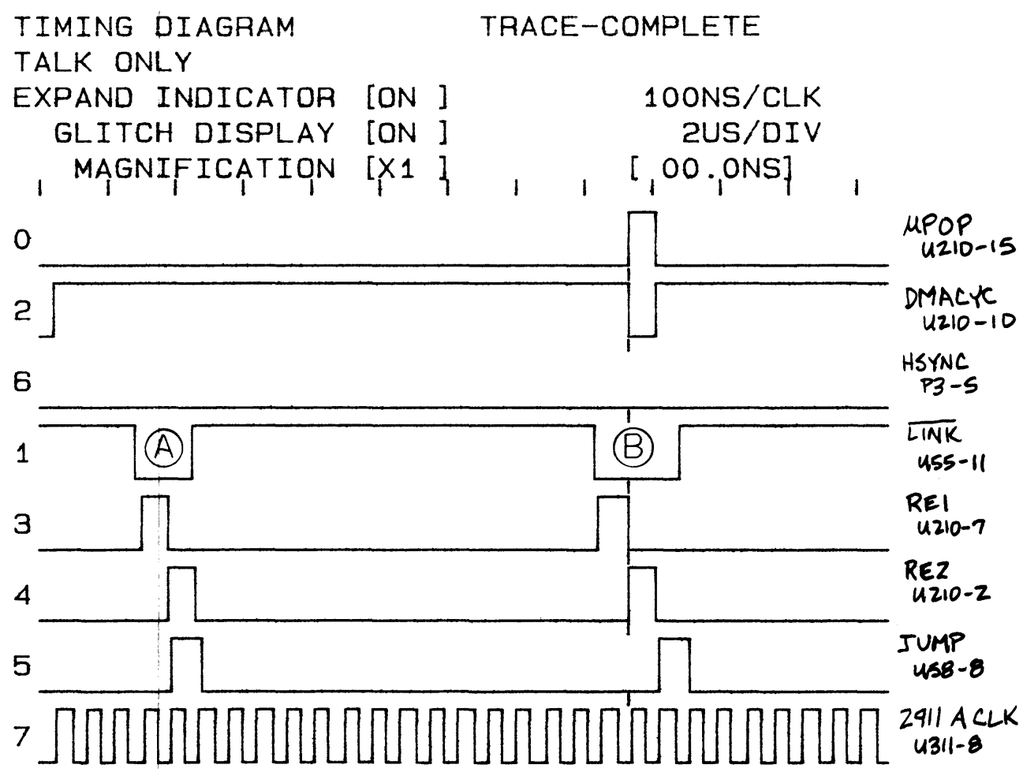


FIGURE 12
JUMP TO LINK ADDRESS (B)
FEB-01-82 13255-91250

END OF EIGHTY CHARACTER LINE

I. SHFTCLK IS GENERATED WHENEVER A CHARACTER IS DMA ED FROM DISPLAY MEMORY.

II. EIGHTY (80) GOES HIGH WHEN THE EIGHTIETH CHARACTER HAS BEEN FETCHED.

III. EIGHTY (80) CAUSES DMA TO CEASE 'TILL THE NEXT CHARACTER ROW BEGINS

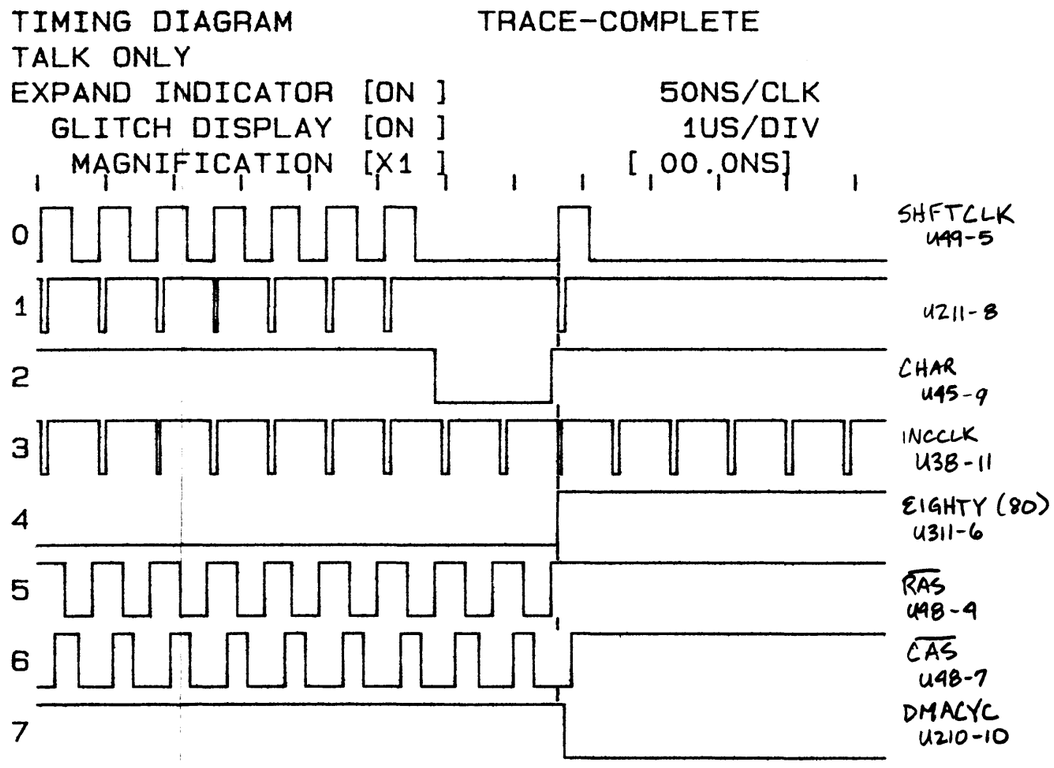


FIGURE 13
END OF EIGHTY CHARACTER LINE
FEB-01-82 13255-91250

END-OF-LINE (EOL) AND END-OF-PAGE (EOP)

I. THIS TIMING DIAGRAM DISPLAYS THE LAST SEVEN ROWS OF ONE FRAME AND THE FIRST ROW OF ANOTHER

II. VBLANK IS REPRESENTATIVE OF THE VERTICAL RETRACE PERIOD

III. EDROW MARKS THE BEGINNING OF THE "NEXT" DATA ROW

IV. (A) MARKS A ROW OF CHARACTERS DMA'ED FROM DISPLAY MEMORY FOR DISPLAY ON ROW 18.

V. ROWS 19 AND 20 ARE BLANK LINES ON THE SCREEN CREATED BY EOL'S.

VI. ROWS 21, 22, 23 ARE BLANK ON THE SCREEN AS A RESULT OF AN EOP.

VII. A LOW STATE ON SIGNAL EIGHTY (80) INDICATES THAT DMA OR BLANK FILL IS ACTIVE. A HIGH STATE INDICATES THAT THE DMA IS "OFF" OR INACTIVE.

VIII (B) MARKS DMA FOR ROW 24, WHICH DOESN'T EXIST AND IS NEVER DISPLAYED.

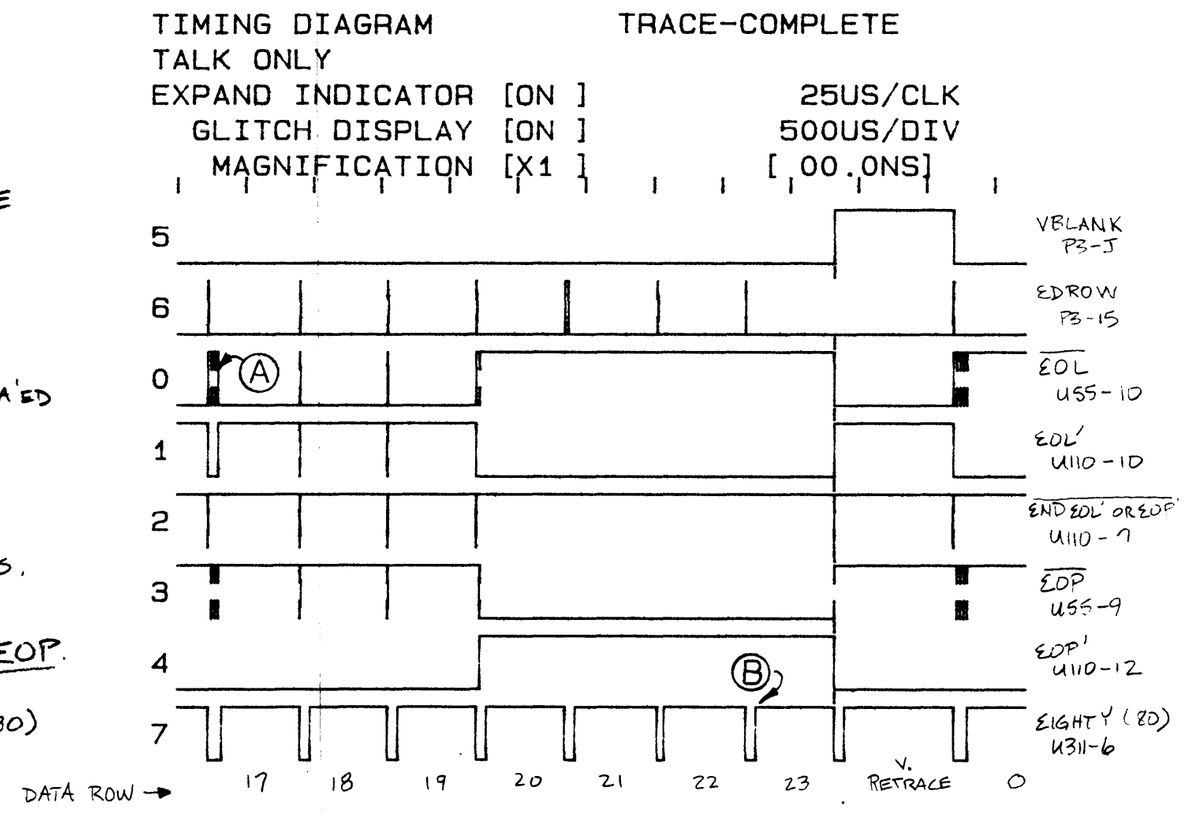


FIGURE 14
END OF LINE AND END OF PAGE
FEB-01-82 13255-91250

SKIP END-OF-LINE TIMING

I. THIS DIAGRAM DISPLAYS A TYPICAL TIMING SEQUENCE FOR A SKIP END-OF-LINE OPERATION.

II. $\overline{\text{SKIPEOL}}$ IS GENERATED BY THE DMA STATE MACHINE, GIVEN THE PROPER EVENTS OCCUR.

III. U610-9 IS SAMPLED BY EDR AND CAUSES SKIPEOL' TO SWITCH STATES.

IV. SKIPEOL' AND $\overline{\text{SKIPEOL}}'$ MASK EOL'S, CHARACTERS, AND ENHANCEMENTS.

V. EACH LINK SEQUENCE STROBES U610 TO ATTEMPT TO END THE SKIPEOL' MODE. IF NEXT LINE POINTER FLAG IS HIGH, THE LINK POINTS TO DATA ON THE SAME CHARACTER ROW AND SKIPEOL' MODE IS NOT TERMINATED. (A)
IF NEXT LINE POINTER FLAG IS LOW, THE LINK POINTS TO DATA ON THE NEXT CHARACTER ROW AND SKIPEOL' MODE IS TERMINATED. (B)

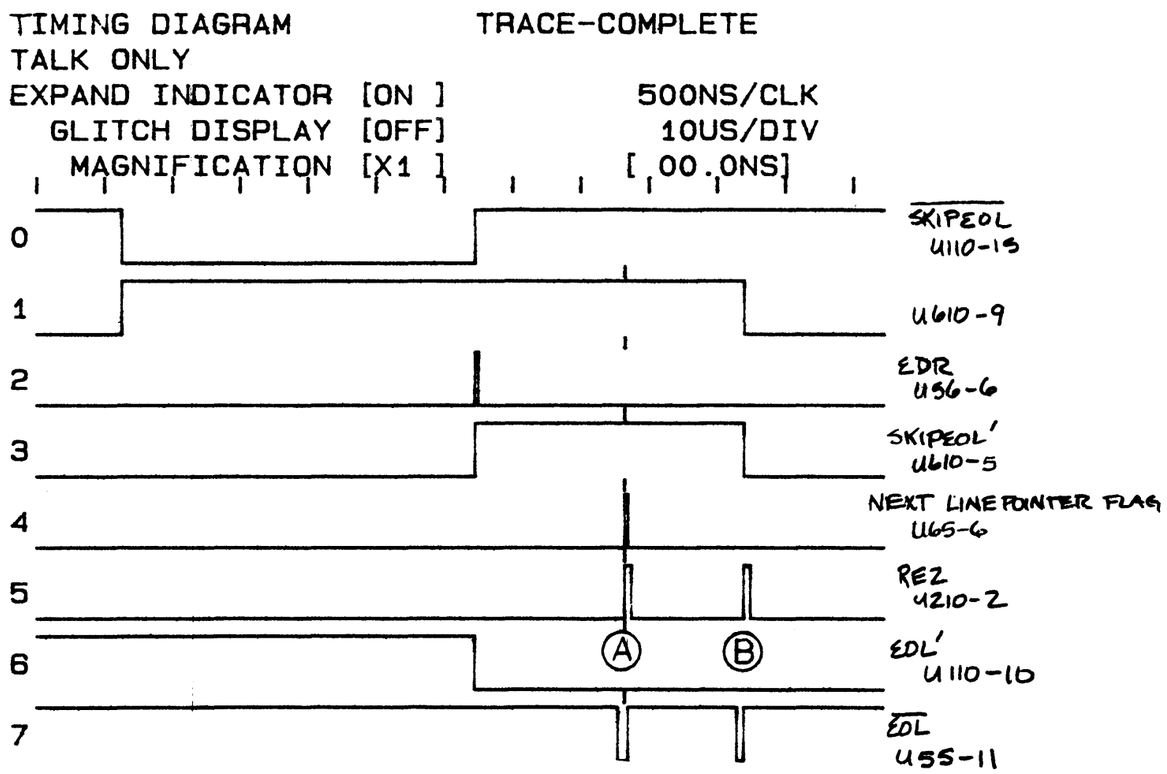


FIGURE 15
SKIP END OF LINE
FEB-01-82 13255-91250

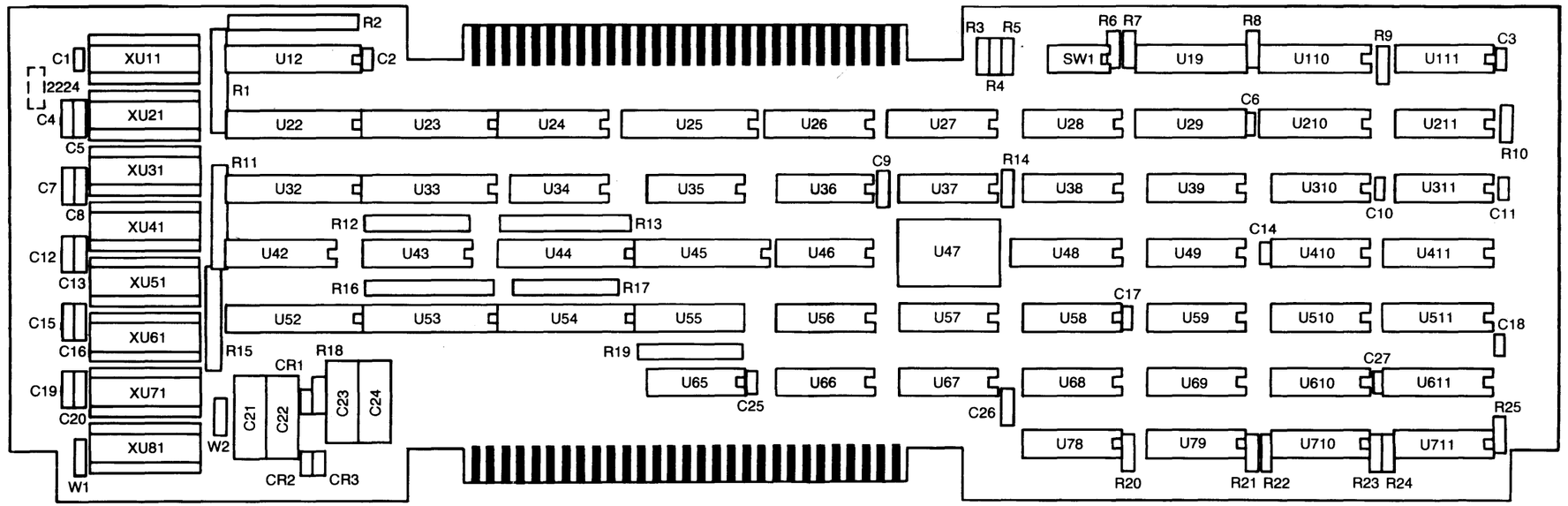


FIGURE 16
COMPONENT LOCATION DIAGRAM
FEB-01-82 13255-91250

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	02640-60250	2	1	DISPLAY MEMORY/DMA PCA DATE CODE: A-2218-42	28480	02640-60250
C1	0160-4554	7	11	CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C2	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C3	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C4	0160-4557	0	12	CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C5	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C6	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C7	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C8	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C9	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C10	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C11	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C12	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C13	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C14	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C15	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C16	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C17	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C18	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C19	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C20	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C21	0180-2879	7	4	CAPACITOR-FXD 22UF+50-10% 25VDC AL	28480	0180-2879
C22	0180-2879	7		CAPACITOR-FXD 22UF+50-10% 25VDC AL	28480	0180-2879
C23	0180-2879	7		CAPACITOR-FXD 22UF+50-10% 25VDC AL	28480	0180-2879
C24	0180-2879	7		CAPACITOR-FXD 22UF+50-10% 25VDC AL	28480	0180-2879
C25	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C26	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C27	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
CR1	1901-0050	3	2	DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
CR2	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
CR3	1902-3092	1	1	DIODE-ZNR 4.99V 2% DO-35 PD=.4W	28480	1902-3092
R1	1810-0322	9	5	NETWORK-RES 8-SIP20.0 OHM X 4	01121	408B200J
R2	1810-0279	5	3	NETWORK-RES 10-SIP4.7K OHM X 9	01121	210A472
R3	0683-1035	1	4	RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R4	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R5	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R6	0683-4725	2	8	RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
R7	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
R8	0683-4715	0	3	RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
R9	0683-1025	9	1	RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R10	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
R11	1810-0322	9		NETWORK-RES 8-SIP20.0 OHM X 4	01121	408B200J
R12	1810-0322	9		NETWORK-RES 8-SIP20.0 OHM X 4	01121	408B200J
R13	1810-0279	5		NETWORK-RES 10-SIP4.7K OHM X 9	01121	210A472
R14	0683-4715	0		RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
R15	1810-0322	9		NETWORK-RES 8-SIP20.0 OHM X 4	01121	408B200J
R16	1810-0279	5		NETWORK-RES 10-SIP4.7K OHM X 9	01121	210A472
R18	0683-4715	0		RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
R19	1810-0205	7	1	NETWORK-RES 8-SIP4.7K OHM X 7	01121	208A472
R20	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
R21	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
R22	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R23	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
R24	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
R25	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
R76	1810-0322	9		NETWORK-RES 8-SIP20.0 OHM X 4	01121	408B200J
SW1	3101-2063	8	1	SWITCH-RKR DIP-RKR-ASSY 4-1A .05A 30VDC	28480	3101-2063
U11	1818-1397	6	8	IC-RAM 16K (PLAST)	S0545	UP416C-3(SELECTED)
U12	1820-2523	7	4	IC-2911A	28480	1820-2523
U19	1816-1486	0	1	IC-ROM 256 X 4 HM7611	34371	HM3-7611A-5 PROGRAMMED
U21	1818-1397	6		IC-RAM 16K (PLAST)	S0545	UP416C-3(SELECTED)
U22	1820-2523	7		IC-2911A	28480	1820-2523
U23	1820-2523	7		IC-2911A	28480	1820-2523
U24	1820-1453	0	1	IC CNTR TTL S BIN SYNCHRO POS-EDGE-TRIG	01295	SN74S163N
U25	1820-1730	6	2	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
U26	1820-1196	8	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS174N
U27	1820-0629	0	1	IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U28	1820-1449	4	1	IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U29	1816-1485	9	1	IC-ROM 256 X 4 HM7611	34371	HM3-7611A-5 PROGRAMMED
U31	1818-1397	6		IC-RAM 16K (PLAST)	S0545	UP416C-3(SELECTED)
U32	1820-2024	3	4	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U33	1820-2523	7		IC-2911A	28480	1820-2523

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U34	1820-0683	6	1	IC INV TTL S HEX 1-INP	01295	SN74S04N
U35	1820-1989	7	1	IC CNTR TTL LS BIN DUAL 4-BIT	07263	74LS393PC
U36	1820-0686	9	1	IC GATE TTL S AND TPL 3-INP	01295	SN74S11N
U37	1820-0681	4	1	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U38	1820-1433	6	1	IC SHF-RGTR TTL LS R-S SERIAL-IN PRL-OUT	01295	SN74LS164N
U39	1820-1201	6	3	IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
U41	1818-1397	6		IC-RAM 16K (PLAST)	S0545	UP416C-3(SELECTED)
U42	1820-1438	1	2	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS257AN
U43	1820-1438	1		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS257AN
U44	1820-2102	8	1	IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U45	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
U46	1820-1199	1	2	IC INV TTL LS HEX 1-INP	01295	SN74LS04N
U47	1813-0228	0	1	OSCILLATOR- 21.34MHZ	28480	1813-0228
U48	1820-1440	5	1	IC LCH TTL LS QUAD	01295	SN74LS279N
U49	1820-0693	8	1	IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
U51	1818-1397	6		IC-RAM 16K (PLAST)	S0545	UP416C-3(SELECTED)
U52	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U53	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U54	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U55	1816-1484	8	1	IC-ROM 256 X 4 HM7611	34371	HM3-7611A-5 PROGRAMMED
U56	1820-1208	3	3	IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
U57	1820-1112	8	5	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U58	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U59	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U59	1820-1208	3		IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
U61	1818-1397	6		IC-RAM 16K (PLAST)	S0545	UP416C-3(SELECTED)
U65	1820-1905	7	1	IC GATE TTL LS NOR DUAL 5-INP	07263	74LS260PC
U66	1820-1202	7	1	IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
U67	1820-1206	1	1	IC GATE TTL LS NOR TPL 3-INP	01295	SN74LS27N
U68	1820-1201	6		IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
U71	1818-1397	6		IC-RAM 16K (PLAST)	S0545	UP416C-3(SELECTED)
U78	1820-1199	1		IC INV TTL LS HEX 1-INP	01295	SN74LS04N
U79	1820-1201	6		IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
U81	1818-1397	6		IC-RAM 16K (PLAST)	S0545	UP416C-3(SELECTED)
U110	1820-1076	3	1	IC FF TTL S D-TYPE POS-EDGE-TRIG CLEAR	01295	SN74S174N
U111	1820-1144	6	1	IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
U210	1820-1191	3	1	IC FF TTL S D-TYPE POS-EDGE-TRIG COM	01295	SN74S175N
U211	1820-0691	6	1	IC GATE TTL S AND-OR-INV	01295	SN74S64N
U310	1820-1322	2	1	IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U311	1820-1367	5	1	IC GATE TTL S AND QUAD 2-INP	01295	SN74S08N
U410	1820-1197	9	1	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U411	1820-1876	1	2	IC CNTR TTL S BIN SYNCHRO POS-EDGE-TRIG	34335	AM74S161N
U510	1820-1208	3		IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
U511	1820-1876	1		IC CNTR TTL S BIN SYNCHRO POS-EDGE-TRIG	34335	AM74S161N
U610	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U611	1820-1212	9	1	IC FF TTL LS J-K NEG-EDGE-TRIG	01295	SN74LS112AN
U710	1820-1209	4	1	IC BFR TTL LS NAND QUAD 2-INP	01295	SN74LS38N
U711	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
W1	8159-0005	0	2	RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	8159-0005
W2	8159-0005	0		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	8159-0005
XU11	1200-0853	8	8	SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0853
XU21	1200-0853	8		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0853
XU31	1200-0853	8		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0853
XU41	1200-0853	8		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0853
XU51	1200-0853	8		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0853
XU61	1200-0853	8		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0853
XU71	1200-0853	8		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0853
XU81	1200-0853	8		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0853
	0360-1682	0	6	TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
	8150-2333	3		WIRE 30AWG W 42V TEFZEL 1X30 105C	28480	8150-2333

MFR NO.	MANUFACTURER NAME	ADDRESS		ZIP CODE
80545	NIPPON ELECTRIC CO	TOKYO	JP	
00000	ANY SATISFACTORY SUPPLIER			
01121	ALLEN-BRADLEY CO	MILWAUKEE	WI	53204
01295	TEXAS INSTR INC SEMICOND CMPNT DIV	DALLAS	TX	75222
04713	MOTOROLA SEMICONDUCTOR PRODUCTS	PHOENIX	AZ	85008
07263	FAIRCHILD SEMICONDUCTOR DIV	MOUNTAIN VIEW	CA	94042
16299	CORNING GLASS WKS COMPONENT DIV	RALEIGH	NC	27604
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO	CA	94304
34335	ADVANCED MICRO DEVICES INC	SUNNYVALE	CA	94086
34371	HARRIS SEMICON DIV HARRIS-INTERTYPE	MELBOURNE	FL	32901
50088	MOSTEK CORP	CARROLLTON	TX	75006