HP 13255

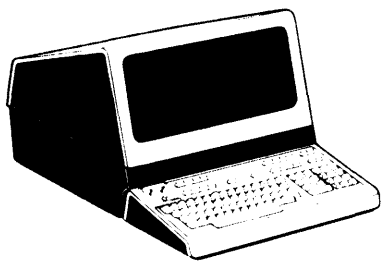
CONTROL MEMORY W/ BANK SELECT MODULE

Manual Part No. 13255-91221

REVISED

OCT-10-78

DATA TERMINAL
TECHNICAL INFORMATION



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1.0 INTRODUCTION.

The Control Memory w/ Bank Sel. Module provides 256 bytes of RAM and 32K bytes of ROM. The module communicates with the processor over a top plane bus. This allows the processor to operate at its maximum rate by eliminating the bus contention and handshake protocol of the bottom plane bus.

The ROMs contain the operating firmware for the terminal. The RAM provides for a fast access scratchpad for stack operations and program variables.

2.0 OPERATING PARAMETERS.

A summary of operating parameters for the Control Memory w/ Bank Sel. Module is contained in tables 1.0 through 5.1.

Table 1.0 Physical Parameters

Part Number	Nomenclature	Size (L x W x D) +/-0.100 Inches	Weight (Pounds)
02640-60221	Control Memory PCA	12.5 x 4.0 x 0.5	0.56
02640-60216	Prom Control Memory PCA	12.5 x 4.0 x 0.5	0.56

Number of Backplane Slots Required: 1

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NOTICE

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NOTE: This document is part of the 264XX DATA TERMINAL product series Technical Information Package (HP 13255).

1.0 INTRODUCTION.

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Number of Backplane Slots Required: 1			

Table 2.0 Reliability and Environmental Information

Environmental: (X) HP Class B ( ) Other:
Restrictions: Type tested at product level
Failure Rate: .8132 (percent per 1000 hours) 3.424 (with 16 ROMs loaded on PCA)

Table 3.0 Power Supply and Clock Requirements - Measured
(At +/-5% Unless Otherwise Specified)

+5 Volt Supply	+12 Volt Supply	-12 Volt Supply	+42 Volt Supply
@ 830 mA	@ 830 mA	@ mA	@ mA
		NOT APPLICABLE	NOT APPLICABLE

115 volts ac	220 volts ac
@ A	@ A
NOT APPLICABLE	NOT APPLICABLE

Clock Frequency: MHz
NOT APPLICABLE

Table 4.0 Switch Definitions

PCA Designation	Function	
	CLOSE	OPEN
ROM DISAB (0,2,4,...,30)	The corresponding 2K block of ROM is enabled.	The corresponding 2K block of ROM is disabled.
-- BS	Respond to BANK SEL. line equal to a '0'.	Respond to BANK SEL. line equal to a '1'.
-- DR	Respond to DISB. ROM line equal to a '0'.	Respond to DISB.ROM line equal to a '1'.
--- A15	Respond to ADDR15 line equal to a '0'.	Respont to ADDR15 equal to a '1'.
--- BSE	Enables BANK SEL. line.	Disables BANK SEL. line.
--- DRE	Enables DISB. ROM line.	Disables DISB. ROM line.
RAM DIS	The RAM is disabled	The RAM is enabled .
LOW RAM	The RAM start address is equal to the '36K' switch.	The RAM start address is equal to the '36K' switch plus 256(decimal).

Table 4.0 Switch Definitions
(continued)

PCA Designation	Function	
	CLOSE	OPEN
36K	The start address of the RAM is equal to 36K .	The start address of the RAM is equal to 62K + 512 .
SLOW	ROM or PROM memory cycles are slower (500 ns.) .	ROM or PROM memory cycles are normal (400 ns.) .
W1	Connects pin 21 of socket to A10. This jumper must be installed to use ROMS.	Disconnects pin 21 from A10. Jumper must be removed to use PROMS.
W2	Connects pin 21 of socket to VCC. This jumper must be installed to use PROMS.	Disconnects pin 21 from VCC. Jumper must be removed to use ROMS.
W3	Connects pin 19 of socket to A10 . This jumper must be installed to use PROMS.	Disconnects pin 19 from A10. Jumper must be removed to use ROMS.
W4	Connects pin 19 of socket to +12 volts. This jumper must installed to use ROMS.	Disconnects pin 19 from +12 volts. Jumper must be removed to use PROMS.

5.0 Connector Information

Connector and Pin No.	Signal Name	Signal Description
P1, Pin 1	+5V	+5 Volt Power Supply
-2	GND	Ground Common Return (Power and Signal)
Pin -3 through Pin -22		Not Used
P1, Pin -A	GND	Ground Common Return (Power and Signal)
-B		Not Used
-C	+12V	+12 Volt Power Supply
Pin -D through Pin -S		Not Used
-T	PRIOR IN	Bus Controller Priority In
-U	PRIOR OUT	Bus Controller Priority Out
Pin -V through Pin -Z		Not Used

Table 5.1 Connector Information

Connector and Pin No.	Signal Name	Signal Description
P3, Pin 1	GND	Ground
- 2	ADDR0	Address Bit 0
- 3	ADDR1	Address Bit 1
- 4	ADDR2	Address Bit 2
- 5	ADDR3	Address Bit 3
- 6	ADDR4	Address Bit 4
- 7	ADDR5	Address Bit 5
- 8	ADDR6	Address Bit 6
- 9	ADDR7	Address Bit 7
-10	ADDR8	Address Bit 8
-11	ADDR9	Address Bit 9
-12	ADDR10	Address Bit 10
-13	ADDR11	Address Bit 11
-14	ADDR12	Address Bit 12
-15	ADDR13	Address Bit 13
-16	ADDR14	Address Bit 14
-17	ADDR15	Address Bit 15
-18	$\overline{\text{TOP ACTIVE}}$	Negative True, (Low) Indicates Top Plane Module Address Recognition. (High Causes a Bottom Plane Bus Cycle)
-19	READ	High Indicates Top Plane Bus Data Should Be Gated On
-20	WRITE	High Indicates Top Plane Bus Data is Valid
-21	SYNC.PHASE1	High indicates beginning of a memory cycle
-22	GND	Ground

Table 5.1 Connector Information (Cont'd.)

Connector and Pin No.	Signal Name	Signal Description
P3, Pin A	GND	Ground
-B	DBIT0	Data Bit 0
-C	DBIT1	Data Bit 1
-D	DBIT2	Data Bit 2
-E	DBIT3	Data Bit 3
-F	DBIT4	Data Bit 4
-H	DBIT5	Data Bit 5
-J	DBIT6	Data Bit 6
-K	DBIT7	Data Bit 7
Pin -L		Not Used
Pin -M	BANK SEL.	Bank select bit , used like annother address line.
Pin -N		Not Used
-P	$\overline{I/O}$	Negative True, (Low) Indicates (A15 A14 A13 A12) = (1000)
Pin -R	SYNC	Sync signal from the processor (8080A-2)
Pin -S		Not Used
-T	WO	High Indicates Write or Output Cycle
-U	DISABLE ROM	Used as annother bank select bit .
-V		Not Used
-W		
-X	MEMR	High Indicates Current Cycle is a Memory Read
-Y		Not Used
-Z	GND	Ground

3.0 FUNCTIONAL DESCRIPTION. Refer to the block diagram (figure 1), schematic diagram (figure 2), timing diagram (figure 3), component location diagram (figure 4), and parts list (02640-60221) located in the appendix. The 02640-60216 PROM Control Memory PCA uses the same block, timing, and component location diagrams and parts list.

The Control Memory w/ Bank Sel. Module provides program storage in Read Only Memory (ROM) for the Processor (8080A-2) Module which controls the functions of the terminal. Via its communication over a top plane bus, this module permits the processor to operate without any wait states during instruction fetch and stack operations. The block diagram shows the functional configuration of the module.

PROMS may be used instead of the ROMS by straping the board as listed in table 4.0. The mixing of PROMS and ROMS is not possible on the same PCA.

3.1 DATA AND ADDRESS DRIVER LOGIC .

3.1.1 The data drivers are bidirectional buffers which present minimum loading to the CPU and synchronize the movement of data along a bidirectional bus on the PCA. The drivers are enabled only when the control logic determines that data is required at the CPU or at the local RAM. There is one set of drivers for transferring information from the PCA to the CPU and another for bringing data from the CPU to the local RAM.

3.1.2 Data on the top plane bus (P3 connector) is applied to the inputs of U24 and U34, and driven onto the internal bidirectional data bus (D0 through D7). Data from the ROMs (16-2K by 8 bits) is driven onto this same internal bidirectional bus. Address information is buffered on the processor (8080A-2) PCA, driven onto the top plane bus, and then through U25,U35 & U44 to the ROM and RAM input pins.

3.1.3 The least significant 11 address lines distribute address information throughout the ROM and RAM arrays. The highest order bits are examined by exclusive NOR gates to determine whether or not the PCA is being addressed.

3.2 ROM OR PROM ARRAY AND RAM MEMORY.

3.2.1 The Control Memory PCA is designed to work with the Advanced Micro Devices 16K ROM (part number AM9216BDC), which can be ordered with two programmable chip selects. In order to function properly in this PCA, both programmable chip selects must be specified to be active low. The ROM chips are mask programmed, 400 nanoseconds access time, 16K bits organized as 2K by 8 bits. The use of PROMS (2K by 8 bits) may be used instead of ROMS by changing the straps W1-W4 (Intel 2716 or TI 2516JL).
The speed of these parts is less than the ROMs , therefore , the SLOW switch should be closed (see table 4.0).

3.2.2 The RAM chips are N-channel MOS which contain 1K bits that are organized as 256 by 4 bits.

3.3 RAM ENABLE LOGIC .

3.3.1 The 256-byte RAM is made up of two 256 by 4 static N-channel mos chips. An 8-bit comparator determines when the RAM block is being addresssed. The constant being applied to the comparator is set as per the description of the switch settings (see table 4.0) .
When the comparator recognizes the address applied to it , the RAMs are enabled and the ROMs are disabled . The comparator logic also returns a TOP ACTIVE signal through the TOP ACTIVE logic.

3.3.2 The CPU provides all the set up and hold times required by the memory chips. Figure 3 shows the read and write timing relationships. The WO signal is used to disable the RAM outputs and to direct data from the processor to the RAMs. The WRITE pulse causes the RAMs to memorize the current state of the data lines and store that information at the location addressed by the address lines.

3.4 ROM OR PROM ENABLE AND BANK SELECT LOGIC .

3.4.1 Each of the 2K ROM chips may be individually disabled. This feature permits substitution of specialized firmware for specific applications without requiring a complete new set of mask programmed ROMs. If a 2K ROM is de-selected, the ROM ENABLE logic will not return a negative $\overline{\text{TOP ACTIVE}}$ signal when an access is made to that 2K block. It is possible with a PROM PCA for a PROM to reside in the same address space as the disabled ROM, thus the substitution is accomplished.

3.4.2 The BANK SELECT LOGIC allows the placement of the 32K ROM array at 1 of 8 32K blocks . The block is selected by lines A15 , DIS ROM , and BANK SELECT useing switches $\overline{\text{A15}}$, $\overline{\text{DR}}$, $\overline{\text{B.S.}}$, BSE , and DRE as described in table 4.0 .

3.4.3 The output of the 2K decoders (U21 and U22) is NAND'ed with the BANK SELECT and READ logic (described in section 3.5) to enable the appropriate column of ROMs . The flip-flop (U52) is used by the the row select decoder (U45) to ensure that one ROM is off before annother ROM is selected .

3.5 TOP ACTIVE , SLOW AND READ LOGIC .

3.5.1 The TOP ACTIVE LOGIC recieves enable signals from ROM and RAM enable logic and returns a negitive true $\overline{\text{TOP ACTIVE}}$ signal to the processor (8080A-2) PCA .

3.5.2 The READ LOGIC examines the status from the processor (8080A-2) PCA to determine if the cycle is going to be a read.

This allows the TOP ACTIVE LOGIC to return a $\overline{\text{TOP ACTIVE}}$ signal in time to prevent a bottom plane memory cycle .

3.5.3 The SLOW logic when enabled, allows slower parts to be used in the board. This slower memory cycle is 500 instead of 400ns.

4.0 TIMING CONSIDERATIONS.

4.0.1 The 8080A-2 Processor is driven by a clock which has a basic period of 400 nanoseconds. There are two clock signals which drive the CPU and are generated on the Processor (8080A-2) PCA. These clock signals govern the timing of addresses coming from the CPU and determine the set up times required for information that is returned from the memory to the processor. The timing diagram (figure 3), shows the timing for PHASE1 and PHASE2 and the resultant access time that is availabe at the pins of the CPU.

4.0.2 Addresses become valid at the pins of the processor a maximum of 195 nanoseconds after the rising edge of PHASE2. Data must be valid at the processor 145 nanoseconds before the leading edge of the T2 PHASE2. The time required from output of the address until the data must be valid at the CPU is 457 nanoseconds.

4.0.3 The time required to return the $\overline{\text{TOP ACTIVE}}$ signal is also shown in figure 3 . the $\overline{\text{TOP ACTIVE}}$ signal prevents a bottom plane memory cycle . The timing required for the return of this signal is 105 nanoseconds.

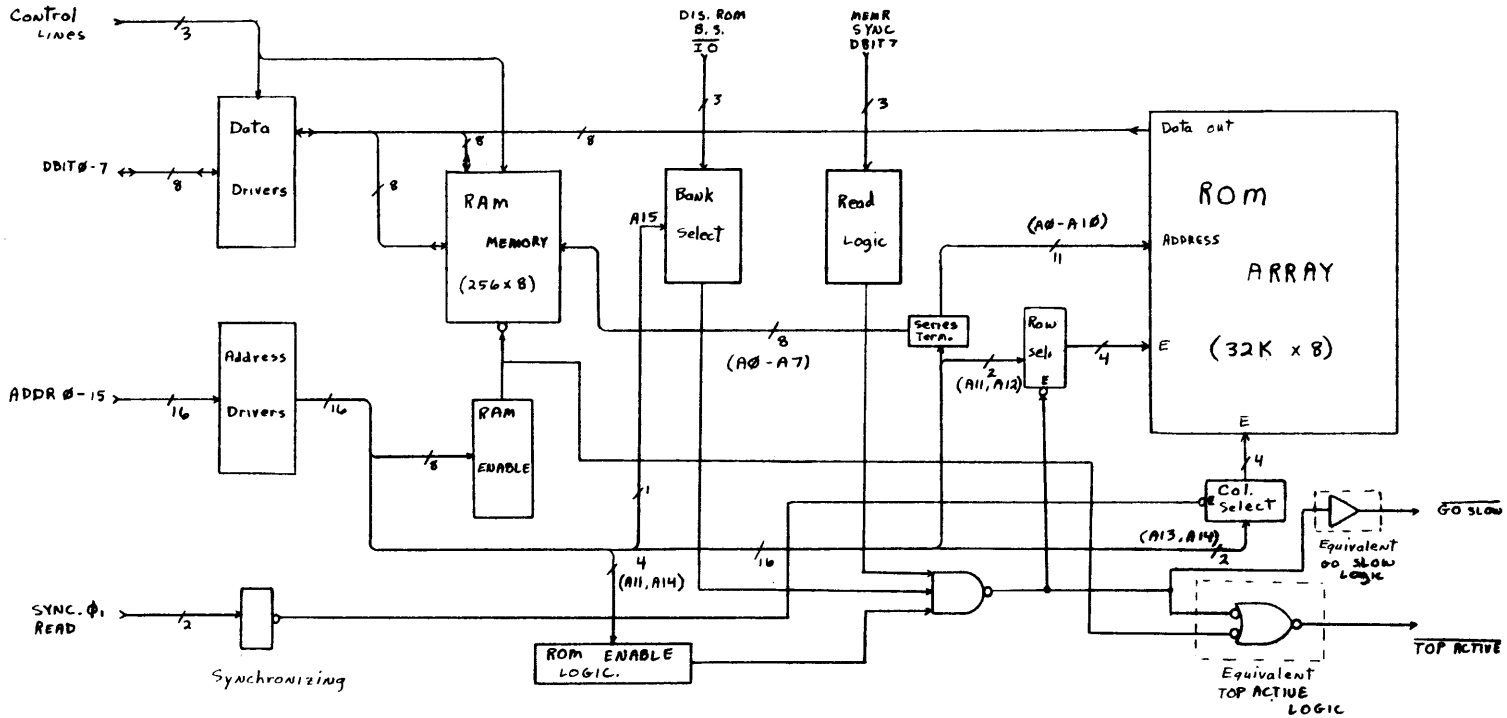


Figure 1
Control Memory Block Diagram
OCT-10-78 13255-91221

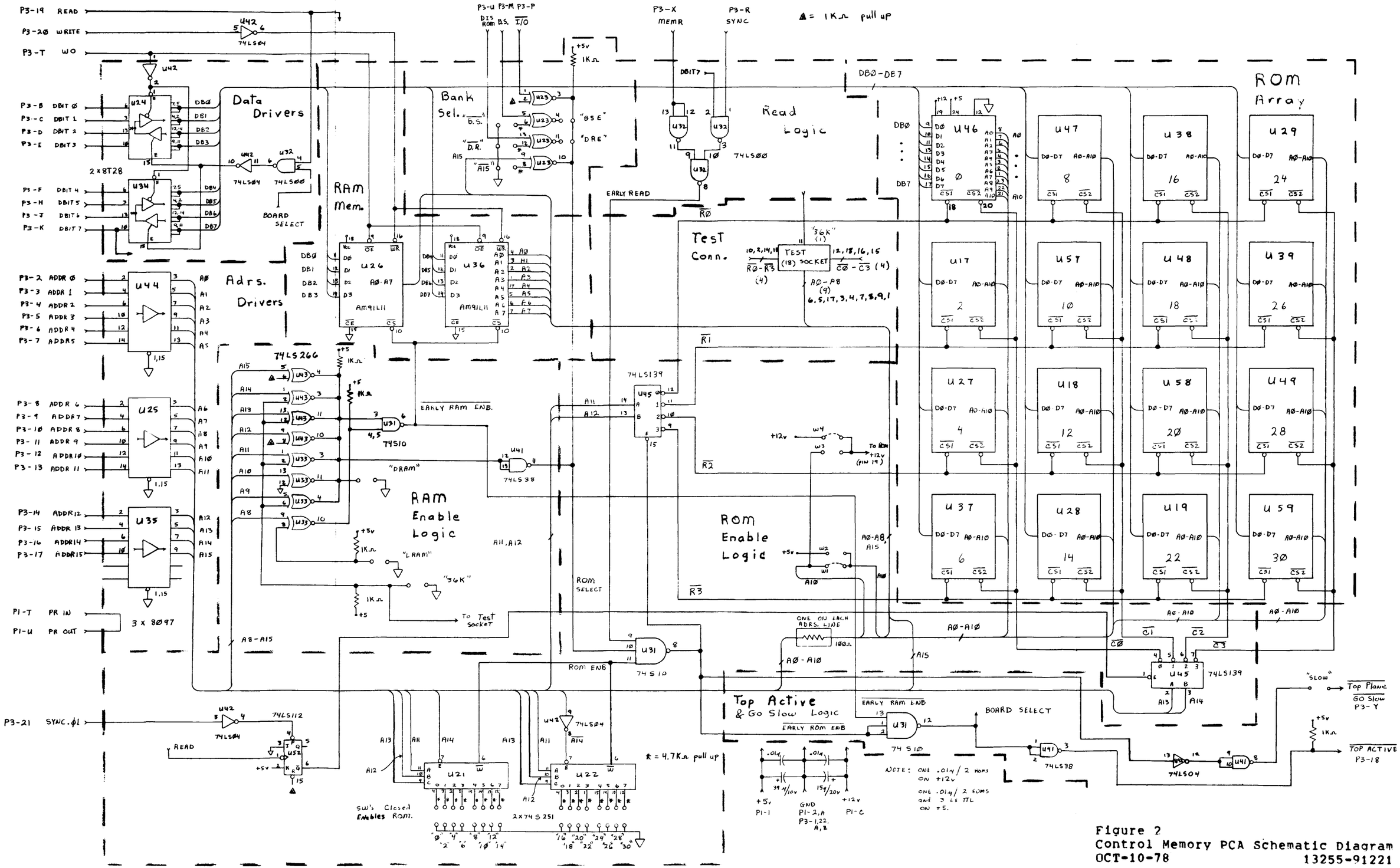
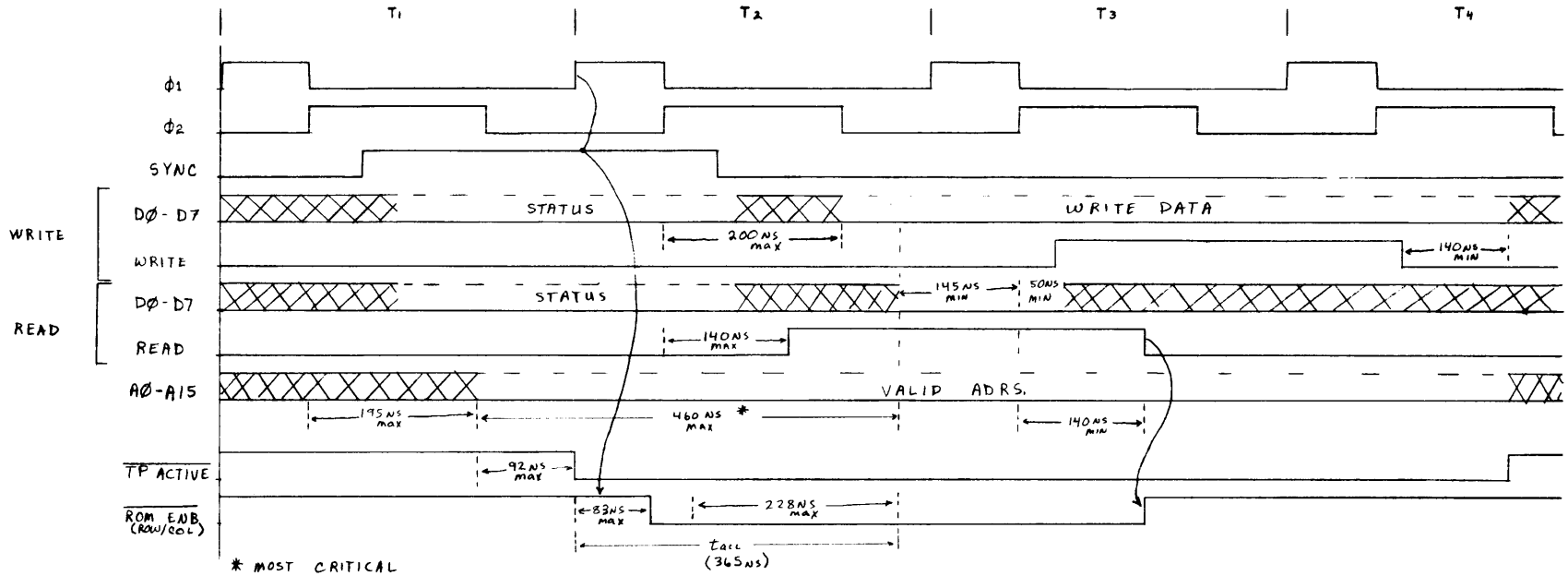


Figure 2
Control Memory PCA Schematic Diagram
OCT-10-78 13255-91221



* MOST CRITICAL

ROM ADRS

$t_{8097} + t_{rom} + t_{8T28} < 460NS$

$22N + 400N + 28NS < 460$

$450NS < 460NS$

TP ACTIVE

$t_{8097} + t_{LS04} + t_{S251} + t_{LS10} + t_{LS10} + t_{LS38} < 105NS$

$92N$ for RAM or $87N$ for ROM $< 105NS$

Read HOLD

READ: 140NS MIN (i.e. Read Signal)

$140NS > 50NS$

ROM ENB (CS_1 or CS_2)

ROM Enable Time from SYNC · ϕ_1

$t_{LS04} + t_{LS112} +$ $t_{LS139} + t_{ROM\ ENB} + t_{8T28} < t_{acc} = 365NS$

$15N + 30N +$ $38NS + 200NS + 28NS < t_{acc}$

$83 +$ 228

$311 < 365NS$

Figure 3
Control Memory Timing Diagram
OCT-10-78 13255-91221

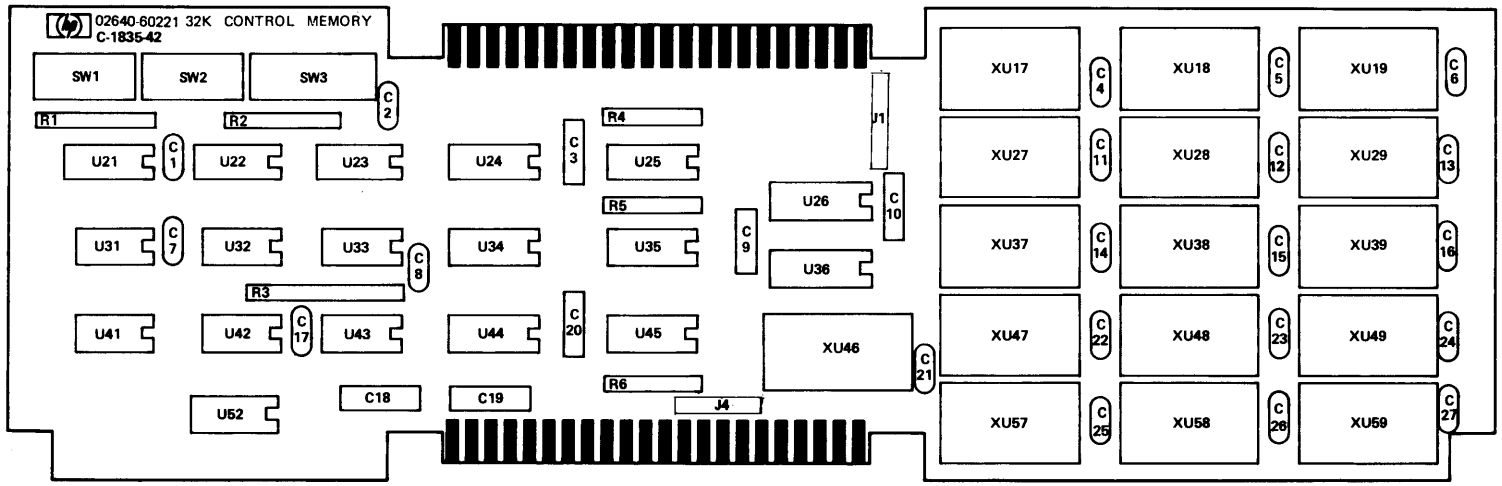


Figure 4
Control Memory PCA Component Location Diagram
OCT-10-78 13255-91221

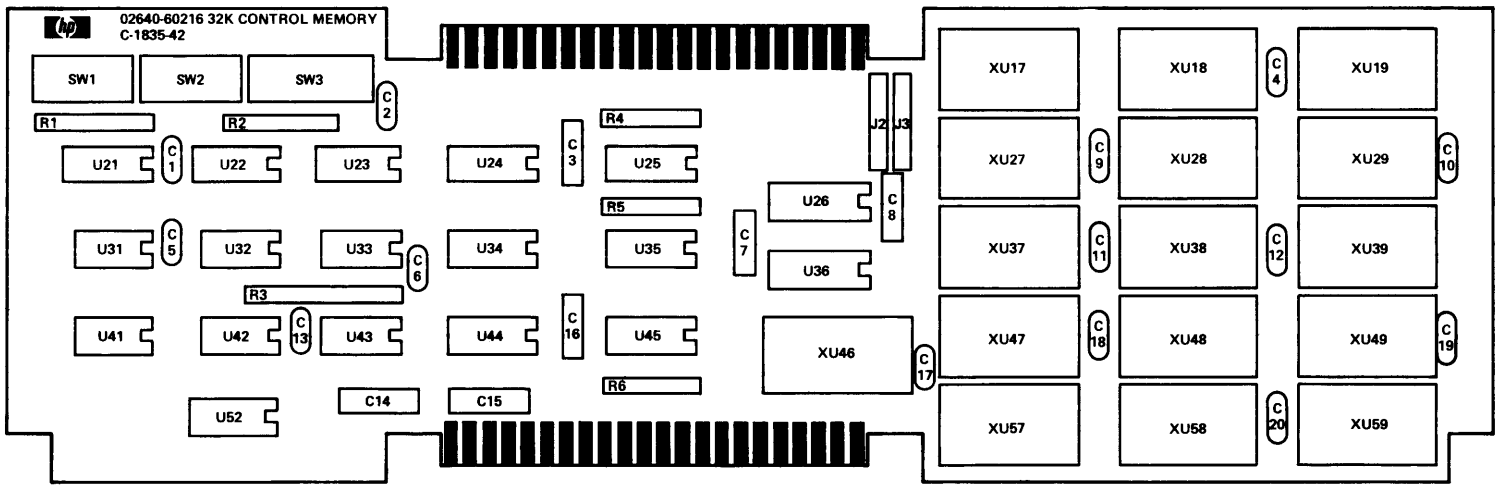


Figure 5
Control Memory PCA Components Location Diagram
OCT-10-78 13255-91221

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
	02640-60221	1	32K B/S CONTROL MEMORY DATE CODE: C - 1835 - 42		
C1, C2	0160-2055	21	CAPACITOR .01UF +80		
C3	0150-0121	4	CAPACITOR 0.1UF		
C4,5,6,7,8	0160-2055		CAPACITOR .01UF +80		
C9, C10	0150-0121		CAPACITOR 0.1UF		
C11,12,13,14,15,	0160-2055		CAPACITOR .01UF +80		
C16, C17	0160-2055		CAPACITOR .01UF +80		
C18	0180-0393	1	CAPACITOR 39UF 10V		
C19	0180-1746	1	CAPACITOR 15UF 10% 20V		
C20	0150-0121		CAPACITOR 0.1UF		
C21,22,23,24,25	0160-2055		CAPACITOR .01UF +80		
C26, C27	0160-2055		CAPACITOR .01UF +80		
R1, R2	1810-0279	2	NETWORK-RESISTOR SIP		
R3	1810-0121	1	RESISTOR NETWORK 8X1K		
R4,5,6	1810-0350	3	NETWORK-RESISTOR		
SW1, SW2	3101-1983	2	SWITCH-TOGGLE 8-1A NS		
SW3	3101-2102	1	SWITCH ROCKER		
U21, U22	1820-1302	2	IC SN74S251N		
U23	1820-1297	3	IC SN74LS266N		
U24	1820-1828	2	IC DIGITAL SIG 8T28		
U25	1820-1049	3	IC DM80 97N		
U26	1818-0197	2	IC AM91L11BDC		
U31	1820-0685	1	IC SN75S10N		
U32	1820-1197	1	IC SN74LS00N		
U33	1820-1297		IC SN74LS266N		
U34	1820-1828		IC DIGITAL SIG 8T28		
U35	1820-1049		IC DM80 97N		
U36	1818-0197		IC AM91L11BDC		
U41	1820-1209	1	IC SN74LS38N		
U42	1820-1199	1	IC SN74LS04N		
U43	1820-1297		IC SN74LS266N		
U44	1820-1049		IC DM80 97N		
U45	1820-1281	1	IC 74LS139		
U52	1820-1212	1	IC SN74LS112N		
XU17-19, 27-29 37-39, 46-49 57-59	1200-0541	16	SOCKET 24 PIN		
	0360-0124	1	STUD SOLDER TERMINAL		
	1200-0614	1	SOCKET IC		
	8159-0005	2	WIRE JUMPERS		

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
	02640-60216	1	32K PROM CONTROL MEMORY DATE CODE: C - 1835 - 42		
C1, C2	0160-2055	14	CAPACITOR .01UF +80		
C3	0150-0121	4	CAPACITOR 0.1UF		
C4,5,6	0160-2055		CAPACITOR .01UF +80		
C7, C8	0150-0121		CAPACITOR 0.1UF		
C9,10,11,12,13	0160-2055		CAPACITOR .01UF +80		
C14	0180-0393	1	CAPACITOR 39UF 10V		
C15	0180-1746	1	CAPACITOR 15UF 10% 20V		
C16	0150-0121		CAPACITOR 0.1UF		
C17,18,19,20	0160-2055		CAPACITOR .01UF +80		
R1, R2	1810-0279	2	NETWORK-RESISTOR SIP		
R3	1810-0121	1	RESISTOR NETWORK 8X1K		
R4,5,6	1810-0350	3	NETWORK-RESISTOR		
SW1, SW2	3101-1983	2	SWITCH-TOGGLE 8-1A NS		
SW3	3101-2102	1	SWITCH-ROCKER		
U21, U22	1820-1302	2	IC SN74S251N		
U23	1820-1297	3	IC SN74LS266N		
U24	1820-1828	2	IC DIGITAL SIG 8T28		
U25	1820-1049	3	IC DM80 97N		
U26	1818-0197	2	IC AM91L11BDC		
U31	1820-0685	1	IC SN75S10N		
U32	1820-1197	1	IC SN74LS00N		
U33	1820-1297		IC SN74LS266N		
U34	1820-1828		IC DIGITAL SIG 8T28		
U35	1820-1049		IC DM80 97N		
U36	1818-0197		IC AM91L11BDC		
U41	1820-1209	1	IC SN74LS38N		
U42	1820-1199	1	IC SN74LS04N		
U43	1820-1297		IC SN74LS266N		
U44	1820-1049		IC DM80 97N		
U45	1820-1281	1	IC 74LS139		
U52	1820-1212	1	IC SN74LS112N		
XU17-19, 27-29 37-39, 46-49 57-59	1200-0541	16	SOCKET 24 PIN		
	0360-0124	1	STUD SOLDER TERMINAL		
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	8159-0005	2	WIRE JUMPERS		

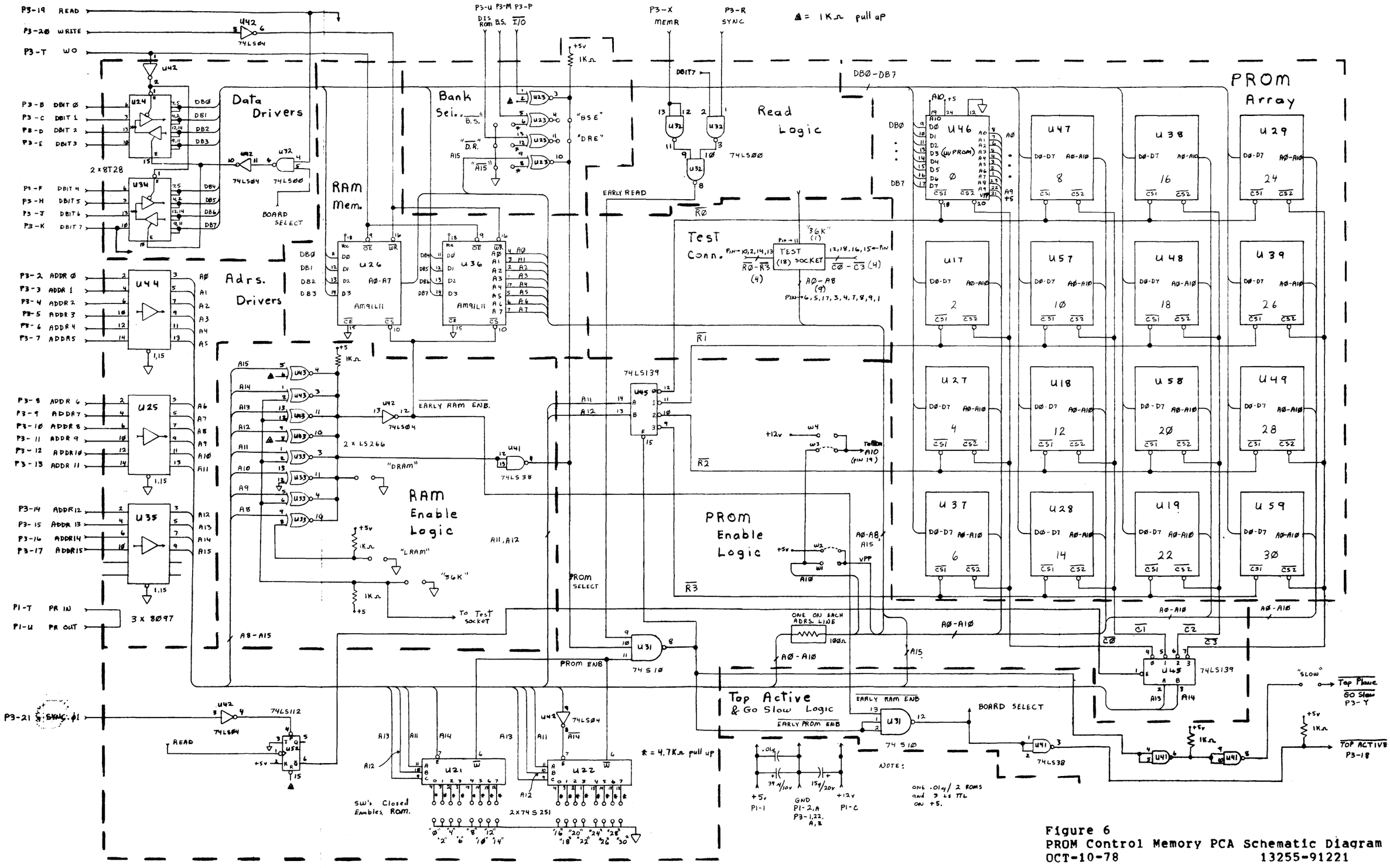

Figure 6
PROM Control Memory PCA Schematic Diagram
OCT-10-78 13255-91221