HEWLETT PACKARD

Mentor Graphics vs HP EE DesignCenter

Competitive Report January, 1989

Electronic Design Division
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For Internal Use Only

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Introduction

This report provides business and technical competitive information on Mentor in comparison to HP's EE DesignCenter products. It is intended as a reference tool for EDD's sales organization and is intended for HP internal use only.

The business section contains both factual information and background material of Mentor. The business information was obtained through Mentor's company press releases, brochures and customer contacts. The information is HP's interpretation of information in the public domain and information obtained through outside consultants and has not been verified. HP does not guarantee its completeness, timeliness or accuracy.

The document also contains technical information on products offered by Mentor as compared to EDD's product offerings. Product comparisons are based on technology comparisons, as opposed to product feature comparisons. Product strengths and weaknesses are also included. The technical information was obtained through field systems engineers and factory-based support engineers research and through the use of paid consultants.

Executive Summary

Mentor Strengths

Mentor has benefited from solid management, giving the company a consistent direction in product development and marketing strategies. In the last year, Mentor has earned consensus recognition from the EDA industry as the leader in electronics CAE. Mentor has achieved this by increasing R&D expenditures in order to make product advances, both in specific product functionality and in breadth of product offerings. As a result, Mentor has a spectrum of products which give the impression of superiority over DesignCenter in performance and functionality. Mentor is currently promoting a new attitude towards their products, changing from one of the "little guys in the market" to "we're the best in the market." Mentor's rise in prices reflects this new attitude of paying for quality products.

- Committed to providing world-class point solutions
- Leader in EDA market share (10.6% overall, 13.4% in workstation EDA)
- Products in CAE, CAD (IC & PCB), CAT, CASE, Documentation & Packaging
- Consistent human interface between products
- Customizable user interface and procedural database access language
- Excellent performance from placer and routers
- Experienced, focused sales force with approximately a 1.5:1 SE:FE ratio
- Marketing strategies
  - -- General-purpose platforms
  - -- System-wide integration
  - -- Major account sale focus
  - -- Strategic selling
  - -- System supplier

HP Strengths

Mentor has been known to walk away from sales where integration with the existing CAD system is requested by the customer. On the other hand, HP is able to provide links in the form of design and test interfaces. HP stresses open systems for interchange of data whereas Mentor stresses installing their complete product system but can address open systems when the issue is raised.

- Open links to other vendors' CAD systems
- Comparably priced for full systems, of which Mentor stresses purchase.
- Hierarchical design support
- On-line rule checking
- Graphical simulation interface
- Superior provider of links to test
- Service and support

Company Background

History

Mentor Graphics Corporation was incorporated in Oregon in April, 1981 and started as one of the original Big 3 in the EDA market in terms of revenue and installed base. Daisy and Valid were the other two. Mentor entered the EDA market in 1982, with its first product, named IDEA, a design capture, simulation and documentation system. Since then, Mentor has expanded its line from a front-end design tool to a full product family of design tools.

Mentor made an early decision to stay with a vendor-supplied platform. This allowed Mentor to avoid problems shared by Daisy and Valid when they attempted manufacturing their own hardware. As a result, Mentor focused development resources on software products, and is now considered the leader in full-spectrum design systems.

General Information

Headquarters

Mentor Graphics Corporation
8500 S.W. Creekside Place
Beaverton, Oregon 97005

Chairman and CEO: Tom Bruggere
President and COO: Gerald Langeler

Number of Employees

Total Employees: approximately 1600, worldwide

R & D Lab :	approx. 350
AM's:	55, North America
DSM's:	14, North America
AE's (SE's):	85, North America
AE Managers:	8, North AMerica

Mentor is the market leader in EDA and has the largest installed base among the major vendors. **Table 1** shows the regional segmentations of Mentor's installed base in units shipped. The figures reflect 1987 data with the total shipped to date figures being cumulative and the remaining figures representing the number shipped in that year. The table also lists figures for systems shipped each year. The last column presents Mentor's Compounded Annual Growth Rate (CAGR) in regional segmentations of their markets. N/A represents not applicable.

Table 1: Regional Segmentations of Mentor's Installed Base
(CAE, PCB and IC workstation, units)

	1983	1984	1985	1986	1987	CAGR 83-87
World Wide Workstations	462	1347	1382	1900	4936	81%
North America	393	1053	879	1246	2982	66%
Europe	69	123	271	512	1276	107%
Far East	0	157	233	143	678	n/a
Rest of World	0	14	0	0	0	n/a
Total Shipped to date	497	1844	3020	4920	9458	109%
CAE Systems	462	1329	1276	1645	4157	73%
PCB Systems	n/a	n/a	n/a	73	366	n/a
IC Systems	n/a	18	106	182	412	n/a

source: Dataquest, July 1988

Target Markets

Mentor considers itself in the top three in each of its target markets. The following lists Mentors opinion of their target markets and Mentor's impression of current market positions.

- **CAE**-computer-aided engineering (1st Mentor, 2nd Daisy/Cadnetix, 3rd Valid)
- **CAD**-computer-aided design (both IC and PCB) (IC Market all four tied for first: Mentor, Cadence, Valid, SCSI)
- **PCB** market (1st Mentor, 2nd Daisy/Cadnetix, 3rd Racal-Redac, 4th Zuken)
- **CAT**-computer-aided test (1st HP, 2nd Mentor/Tektronix, 3rd Teradyne, 4th Genrad)
- **CAEP**-computer-aided electronic packaging (1st Intergraph, 2nd Prime/CV, 3rd Mentor)
- **CASE**-computer-aided software engineering (1st Cadre, 1st Index, 3rd Mentor)
- **CAP**-computer-aided publishing (1st Interleaf, 2nd Xyvision, 3rd Mentor)

Again, the remarks in parentheses are Mentor's rankings of the competition in each area.

Technology Partners

In a very real sense, Apollo computer should be considered a technology partner with Mentor, since the Domain Operating System provides much of Mentor's data base functionality. Much of Mentor's technology is based on tools provided by the Apollo Domain.

While not a true technology partner, Mentor's acquisition of Tektronix's CAE and CASE technologies has positioned them in the computer-aided test (CAT) marketplace. Mentor has also purchased Cadent (fault simulation software) and California Automated Design (gate array and standard cell design and generic routing technology) in order to improve their position in design analysis.

Mentor also has agreements with:

- **Logic Automation**—LSI/VLSI modeling Library for system-level simulation
- **Test Systems Strategies Inc.**— links to automatic test equipment (GenRad)
- **Silicon Compilers**--Genesil silicon compiler integrated with IDEA
- **Seattle Silicon**—Concorde silicon compiler
- **Cadence Inc.**—MSIMON analog simulator, Dracula II IC verification
- **MOSIS**—standard cell libraries
- **NCR**—standard cell libraries
- **Hughes Aircraft**—joint product development agreement
- **Boeing**—joint product development agreement
- **Advanced Micro Devices**—joint product development agreement
- **Motorola**--joint product development
- **Sandia Labs**--joint product development

Financial and Market Share Information

Financials

Mentor has had steady growth since 1983, with an overall Compounded Annual Growth Rate (CAGR) of approximately 69%. This has been their hallmark. By maintaining control over costs, Mentor has generated steady revenue and profit growth. They have shown an increase of revenue and earnings over the last 25 consecutive quarters, while making substantial investments in R&D. Mentor has also maintained the lowest field selling costs of the major EDA vendors.

Over 50% of Mentor's revenue is generated from CAE tools, though printed circuit board layout is reputedly their fastest growing product line. **Table 2** shows regional segmentations of revenue for Mentor between 1983 and 1987. The figures represent millions of dollars per year. N/A represents not applicable.

Table 2: Regional Segmentations of Mentor's Revenue
(CAE, PCB and IC workstations, millions of dollars)

Mentor	1983	1984	1985	1986	1987	CAGR 83-87
Total Revenues	25.8	87.6	136.7	173.5	210.7	69%
North America	21.8	68.6	85.7	100.9	112.6	51%
Europe	4.0	9.0	30.5	41.3	53.1	91%
Far East	0	9.0	20.5	31.4	45.0	n/a
Rest of World	0	1.0	0	0	0	n/a

source: Dataquest, July 1988

Market Share

Mentor is the leader in electronic design automation (according to Dataquest numbers for 1987) and has the largest installed base among the major vendors. In comparison, among vendors of EDA software, HP places fifth.

Figure 1 compares the total revenues of the combined markets of Technical Workstation Platforms of CAE, PCB, and IC. Mentor leads the industry with a 18.9% share as compared to HP's fifth place 5.3% share. When broken down into separate markets, Mentor's majority lead comes from the CAE market with a 30% share (**Figure 2**). Mentor also has the advantage over its competitors in the IC market with a 12.9% share while HP maintains a fourth place 1.9% in this market (**Figure 3**). But in the PCB market, Mentor's 6.5% share falls short of their competitors including HP's 8.6% market share (**Figure 4**).

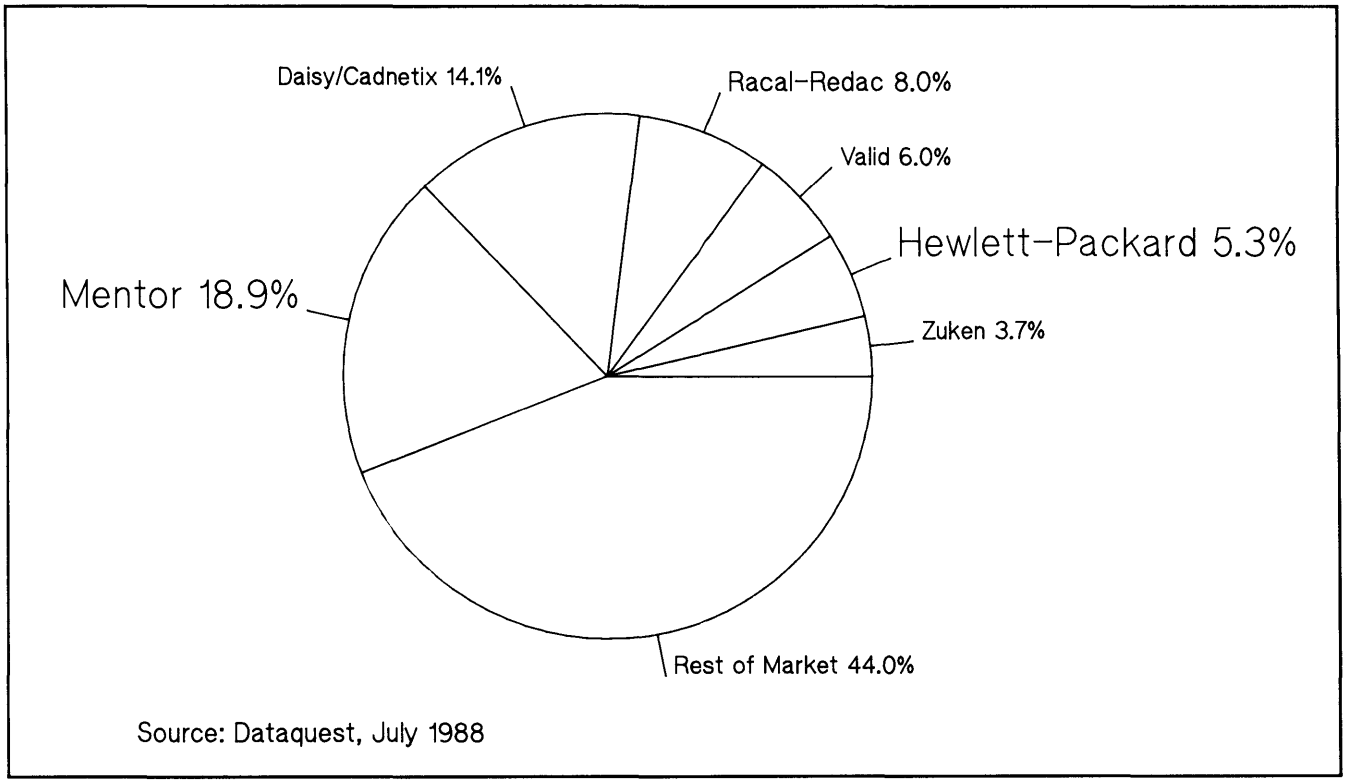

Figure 1: Market Share 1987, Total CAE, PCB, IC Markets

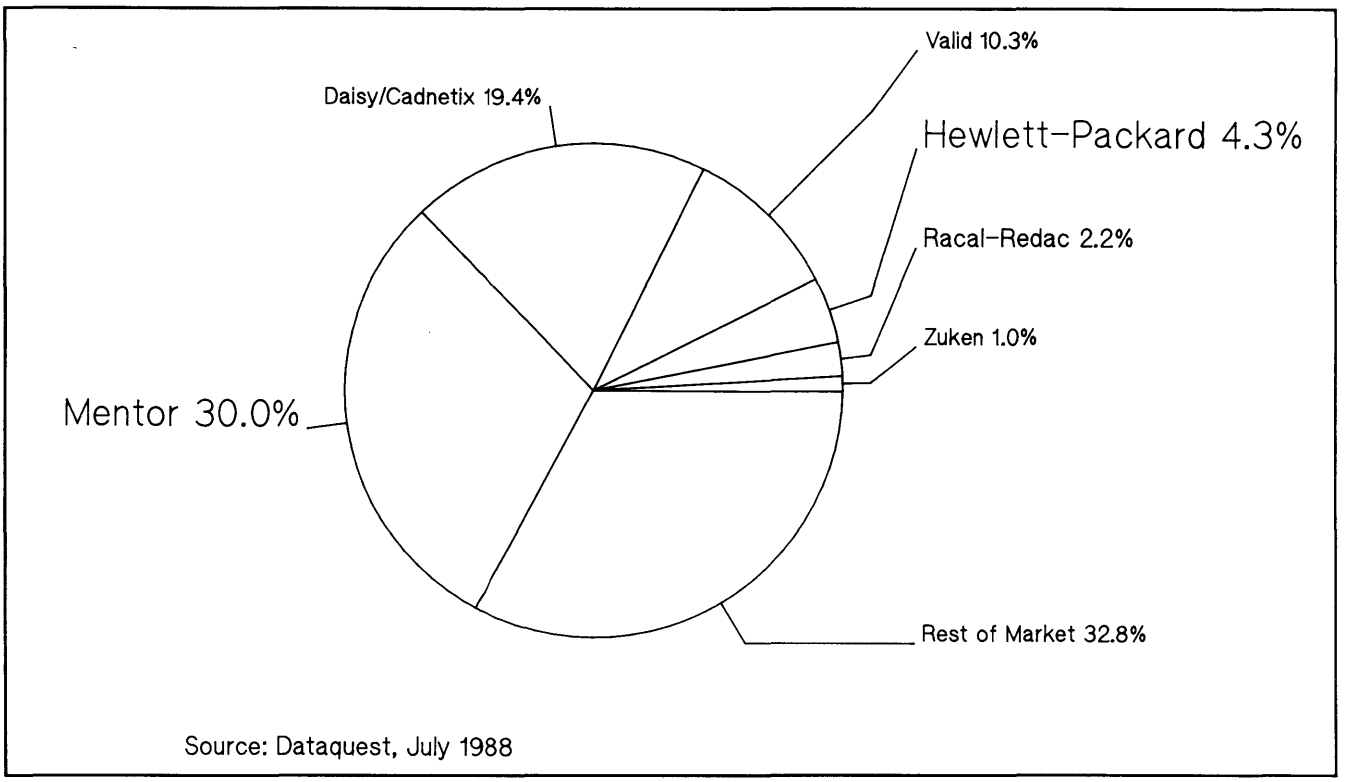

Figure 2: Market Share 1987, CAE Market

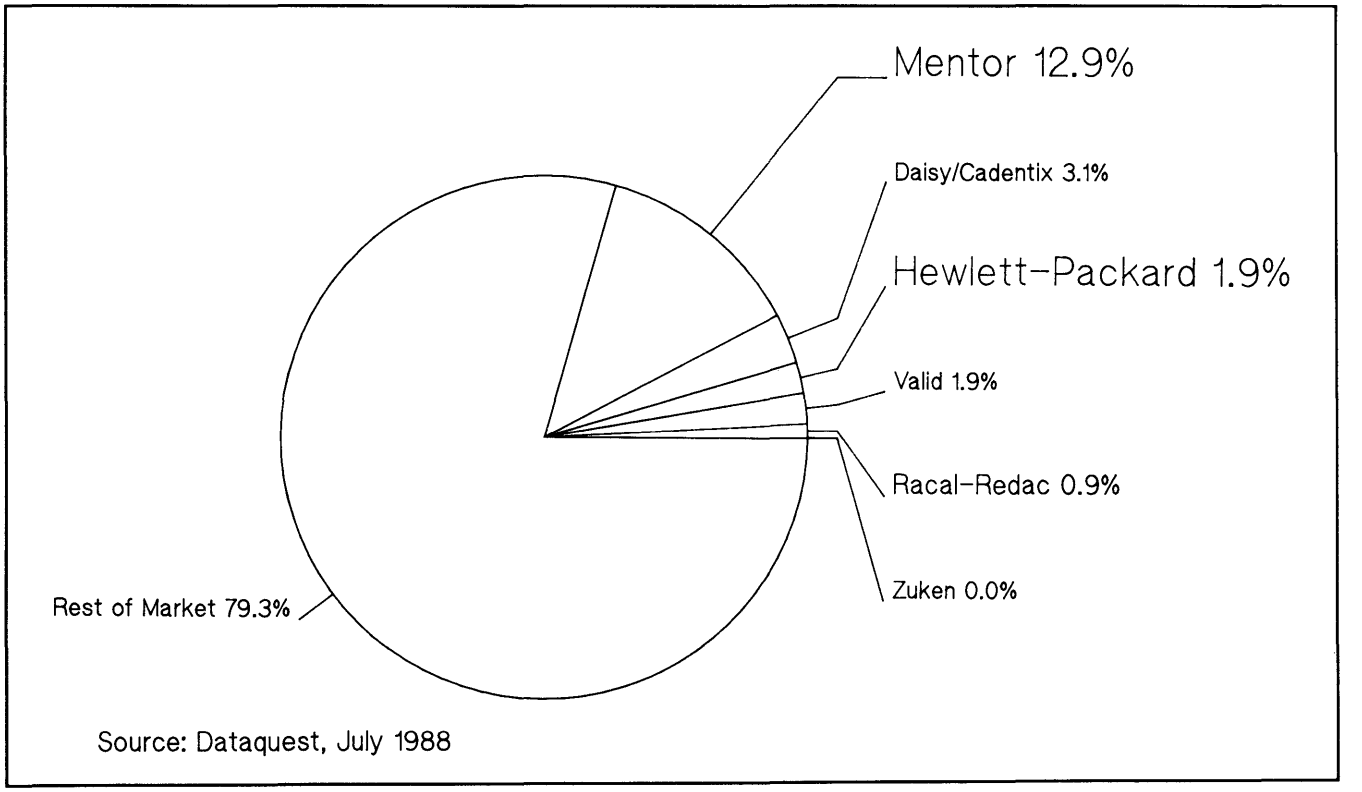

Figure 3: Market Share 1987, IC Market

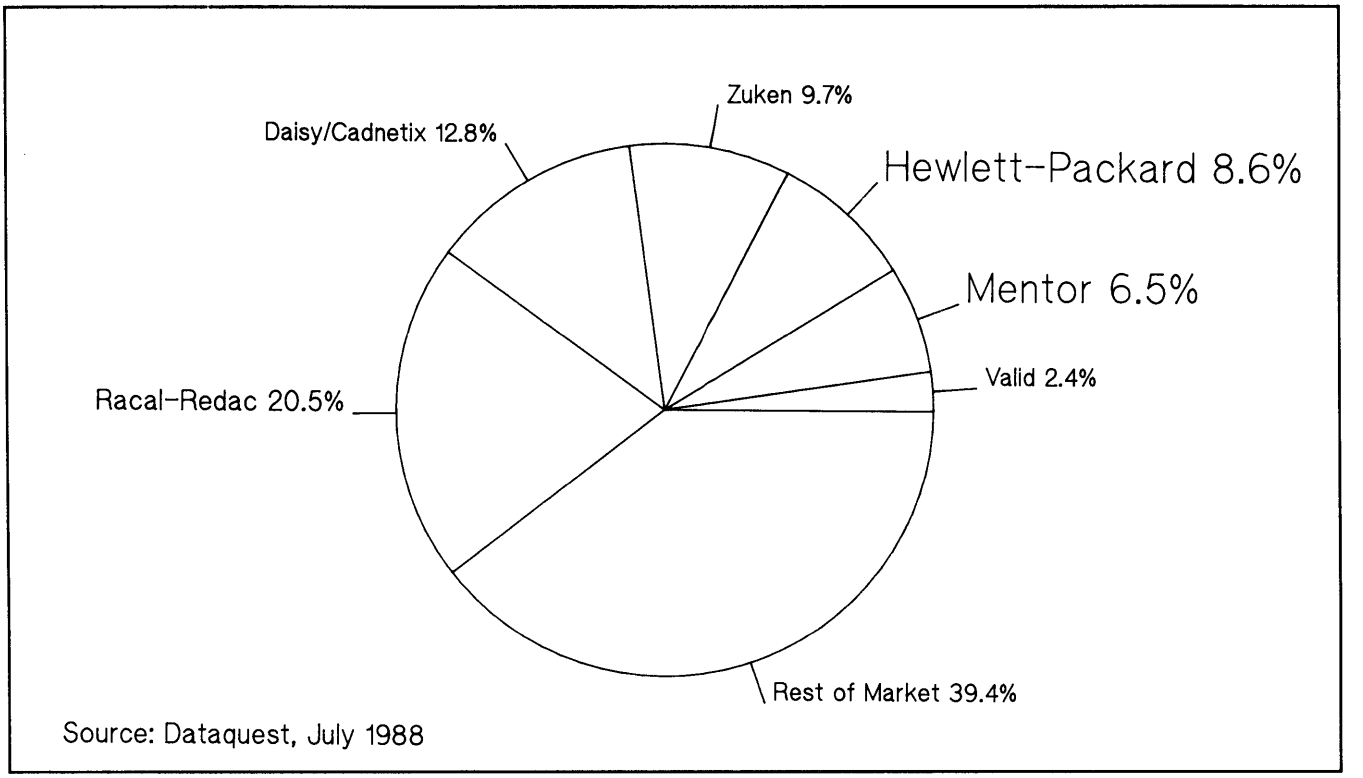

Figure 4: Market Share 1987, PCB Market

Product Family

Platforms

Though they are feeling pressure to adopt a second platform, Mentor runs predominantly on Apollo workstations with the exception of CASE software which also runs on DEC.

Apollo Platforms:

- DN 3500 4 MIP, 25 MHz MC68030 with 68882
- DN 4500 7.5 MIP, 33 MHz MC68030 with 68882
- DN 3010 2 MIP, 12 MHz MC68020 with MC68881 floating point coprocessor
- DN10000 1 to 4 15 MIP CPUs, up to 128 Mb of RAM*

*DN10000 is Apollo's PRISM Architecture. Capable of handling up to four 15 MIP CPUs and 128 Mb RAM.

Software

Mentor is the most broadly diversified company in EE design software. HP/EDD is next. Mentor has recently broadened the product family to include packaging tools.

Mentor offers a number of products, bundled together in "stations". The remarks in parentheses denote the application's coverage:

- Entry Station
  (personal computer based design)
- Capture Station
  (design capture system)
- Design Station
  (design capture and documentation system)
- Idea Station
  (design capture, documentation plus simulation)
- Cell Station
  (standard cell IC system)
- Chip Station
  (full custom IC system)
- Gate Station
  (gate array IC system)
- Board Station
  (printed circuit board system)
- Package Station
  (3D mechanical and thermal analysis)

The applications fit into a matrix which covers not only standard cell IC design, full custom IC design, and gate array design, but also conventional thru-hole printed circuit board technology. For a complete listing of Mentor's and HP's product coverages, see Appendix B.

The following chart from Mentor lists all their products by category.

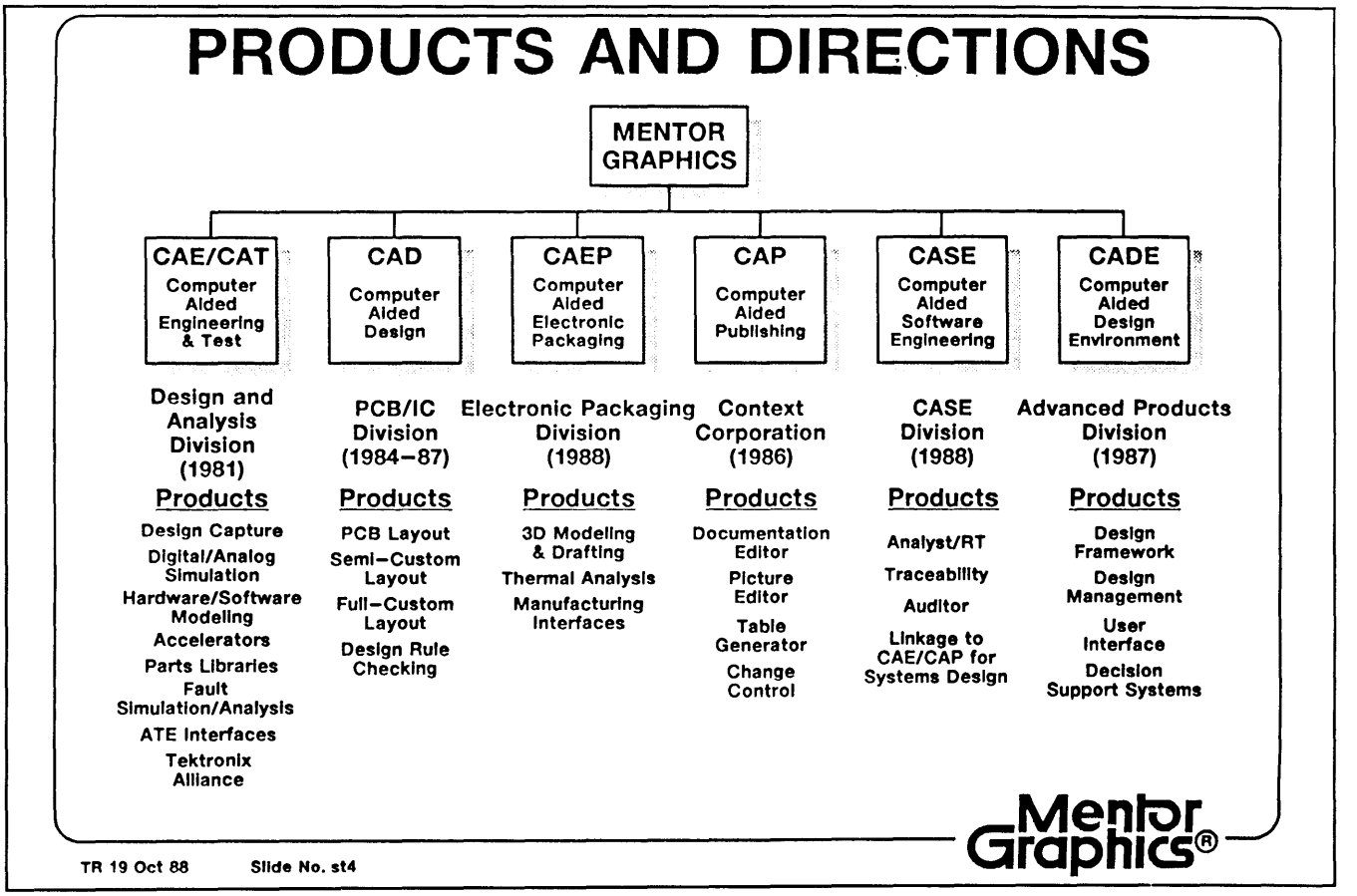

Figure 5: Mentor Products

Pricing Comparison

In 1988, Mentor implemented a new pricing policy, replacing their former policy of aggressive discounting with one based on total gross profit margins. Currently, all pricing discounts (however implemented) must be approved by district or area sales managers, excluding pre-arranged standard purchase agreement discounts. To accompany their new pricing strategy, Mentor has also changed how it wants to be perceived in the market.

Mentor's sales force now pushes their products as the best on the market for which everyone must pay more. HP has a long standing tradition of offering quality products and has marketed them accordingly. Mentor's new pricing policy makes them more comparable to HP's current pricing policy.

Figures 6 and **7** compare pricing on HP and Mentor design capture systems. With Mentor's new pricing policy, HP is now more competitive.

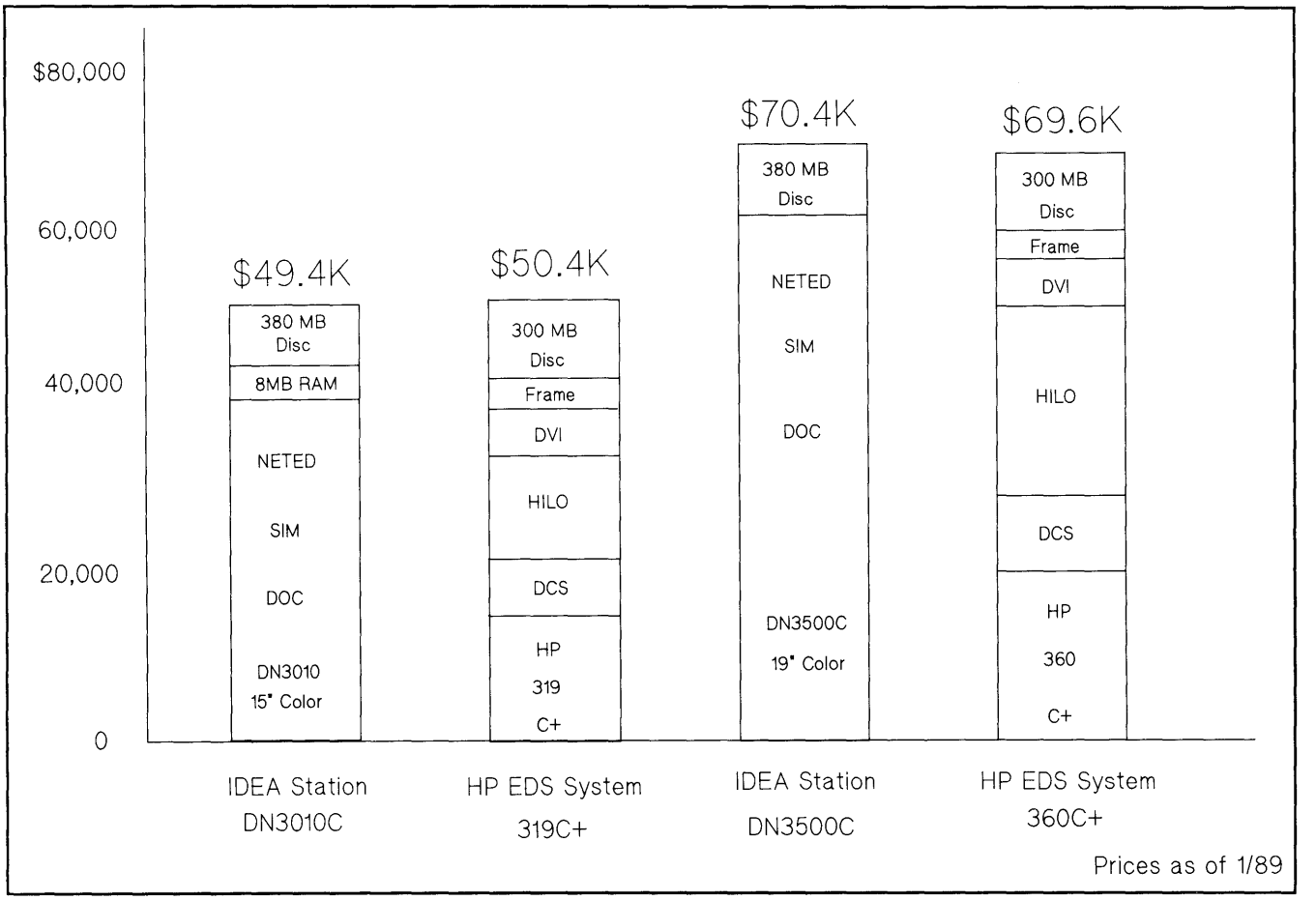

Figure 6: Pricing Comparison, Design Capture Systems

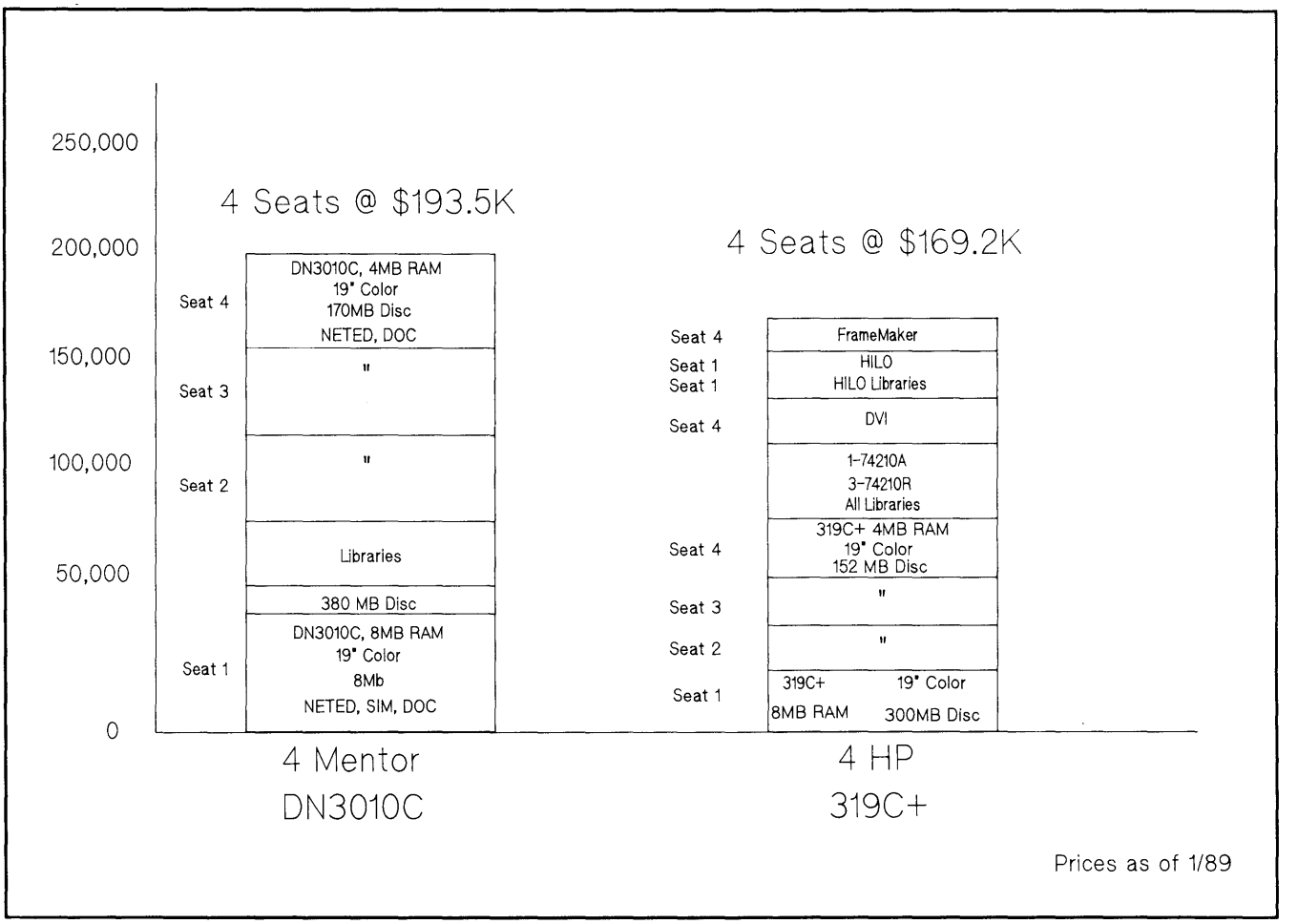

Figure 7: Pricing Comparison, 4 Seat Capture (1 Seat with Simulation)

Figure 8 compares pricing on HP and Mentor physical design systems. HP's pricing on HP DCS and HP PCDS strongly competes against Mentor's Board Station. Board Station support is about $750-$1,150 per month, compared to approximately $585 a month for HP PCDS.

For a price listing of Mentor's individual products and bundled prices see Appendix A.

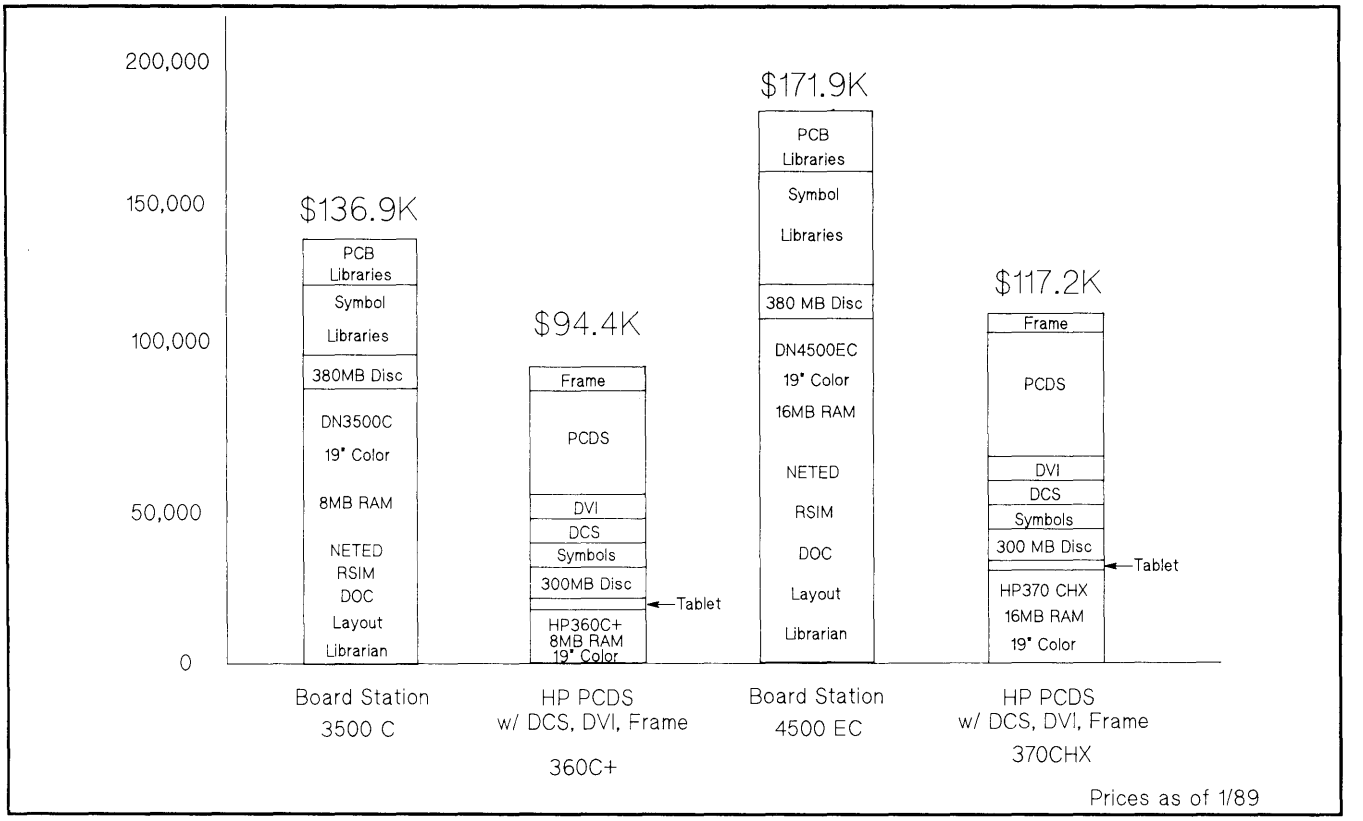

Figure 8: Pricing Comparison, Physical Design Systems

Service and Support

Mentor has been steadily improving their service and support. They currently have an experienced sales force and have ready access to SEs for assistance with the technical aspects of the products. While they cannot claim to do as well as HP (Number 1 ranking by Datapro), Mentor doesn't do too badly. 19.8 % of Mentor's revenue ($41.5 Millon, U.S.) is attributed to service and training. They have almost a 1.5:1 SE:FE ratio. In 1987, Mentor began supporting the Apollo workstations, eroding HP's advantage of offering one-stop sales and service.

Mentor offers three levels of software support: 2 hour response (very fast but limited support), 24 hour response and 72 hour response. Hardware also has three levels of support, keeping the 24 and 72 hour response times, and offering a limited 4 hour response as their premium service. Mentor support prices are listed in the Pricing Comparison found in Appendix A.

Mentor Future Products and Markets

Mentor intends to expand into a new segment every two years. This gives Mentor a strong advantage, since they are selling their own full-spectrum line of products (a Mentor DesignCenter, if you will). Each entry they make brings the opportunity to define exactly what a DesignCenter needs to be. This poses a serious problem for HP. If Mentor defines the mechanical portion of CAE to be packaging, then it predisposes the customer to this solution as opposed to HP's solution of full Mechanical capabilities (like ME-10 & 30). In addition, Mentor is very active in expanding into systems or architectural specification and design. Mentor could well be in a position to define this market, too, by the end of 1989.

Mentor has already stated that it is entering the hybrid circuit design market in the future. Expect substantive enhancements to Mentor's existing products, such as "SHOVE of a trace" in Board Station. Mentor has also made a deal with EEsof that will provide Mentor with microwave/RF CAE tools. This is complimentary with their hybrid circuit design plans.

An agreement between Mentor and Tektronix has been reached to develop links between Mentor's EDA tools and Tektronix's test and measurement instrumentation. This strategy is clearly aimed at HP in the long-term.

Mentor also revealed its plans to move into several design automation segments at the 1987 Dataquest conference. So far, they are ahead of schedule with recent moves into computer-aided software engineering (CASE) and computer aided electronic packaging (CAEP).

Mentor has given no indication of its plans for the PC 386 platform. With HP and Daisy moving to PC 386 platforms, being envisioned as the platform of the future, this oversight might create concern and uncertainty among Mentor's potential customers. This concern could influence customers to choose another vendor.

Mentor Sales Pitches

Mentor has done well recently by using their ads to counter HP ads. They have run ads that feature-by-feature zero in on our product weaknesses. In addition, Mentor claims to be THE total solution provider and tries to broaden the decision criteria beyond a particular application niche to include the entire design cycle.

Mentor has a reputation in the community as being closed systems. However, they are working hard to change this perception. Some examples of how Mentor is trying to change this perception are:

-- First major software vendor to become Open Software Foundation (OSF) sponsor
-- First EDIF sponsor
-- Twelve published links to other systems and several unpublished links
-- Competitive buy back and trade-in programs

Open systems for data exchange is one of HP's stronger sales points. HP's ability to provide links in the form of design and test interfaces should be stressed. HP also offers links to AWB, Computervision, Racal-Redac RINF, Calay, Scicards and bi-directional EDIF links.

Technical Analysis

Introduction

This section contains technical comparisons of Mentor and HP/EDD applications for standard logic design, PLD design and verification, ASIC design and verification and PCB layout. It is also a presentation of the strengths and weaknesses of both Mentor and HP/EDD products.

Spider diagrams are used for comparing the technical applications. Each application is divided by product components or parameters. The parameters establish the axis of the spider diagrams. In some cases, such as standard logic design entry and board layout, there are several subcategories or attributes for each axis.

For each axis, or subcategory, a whole number between 1 and 10 is used by HP field and factory support engineers. The larger the number, the "better" the performance of the application for that measurement axis, or subcategory. A value of 10 indicates the best, or state of the art, for current products on the market. A value of 1 indicates no capability, while a 5 is considered average. Unknown information is left blank and not included in the calculations. The subcategories are averaged and rounded to the nearest integer for plotting on the axis.

Schematic capture, printed circuit board design and documentation product comparisons were accomplished at a service bureau in the U. S. on an Apollo DN3000 with 8 megs of memory. Revision 6.0 of the Board Station software was used. ASIC and simulation product comparisons were evaluated on a Mentor system owned by HP EDD. The hardware used was an Apollo DN460* with 8 megs of memory using a 158 meg disc. The software used was Aegis, Domain revision 9.7 with Idea Station revision 6.1. Mentor's systems were compared to the HP EE DesignCenter current systems (release 2805) except for PCDS where Revision 2.0 was used for comparison.

*The comparison performed was intended purely as a technology comparison not as a performance comparison.

Mentor Idea Station vs. HP EDS

Figure 9 is a diagram of Mentor's and HP's design process as it applys to the APE benchmark design. HP EDS uses an object-oriented data structure. This is different from Mentor's process which creates a multitude of files and then allows the Apollo Domain system to manage them. This difference shows up in the Draw/Edit Schematic step. HP EDS utilizes an on-line checker which gets rid of the Check Sheet and Expand & Resolve for SIM/PCB steps which are needed in the Mentor process.

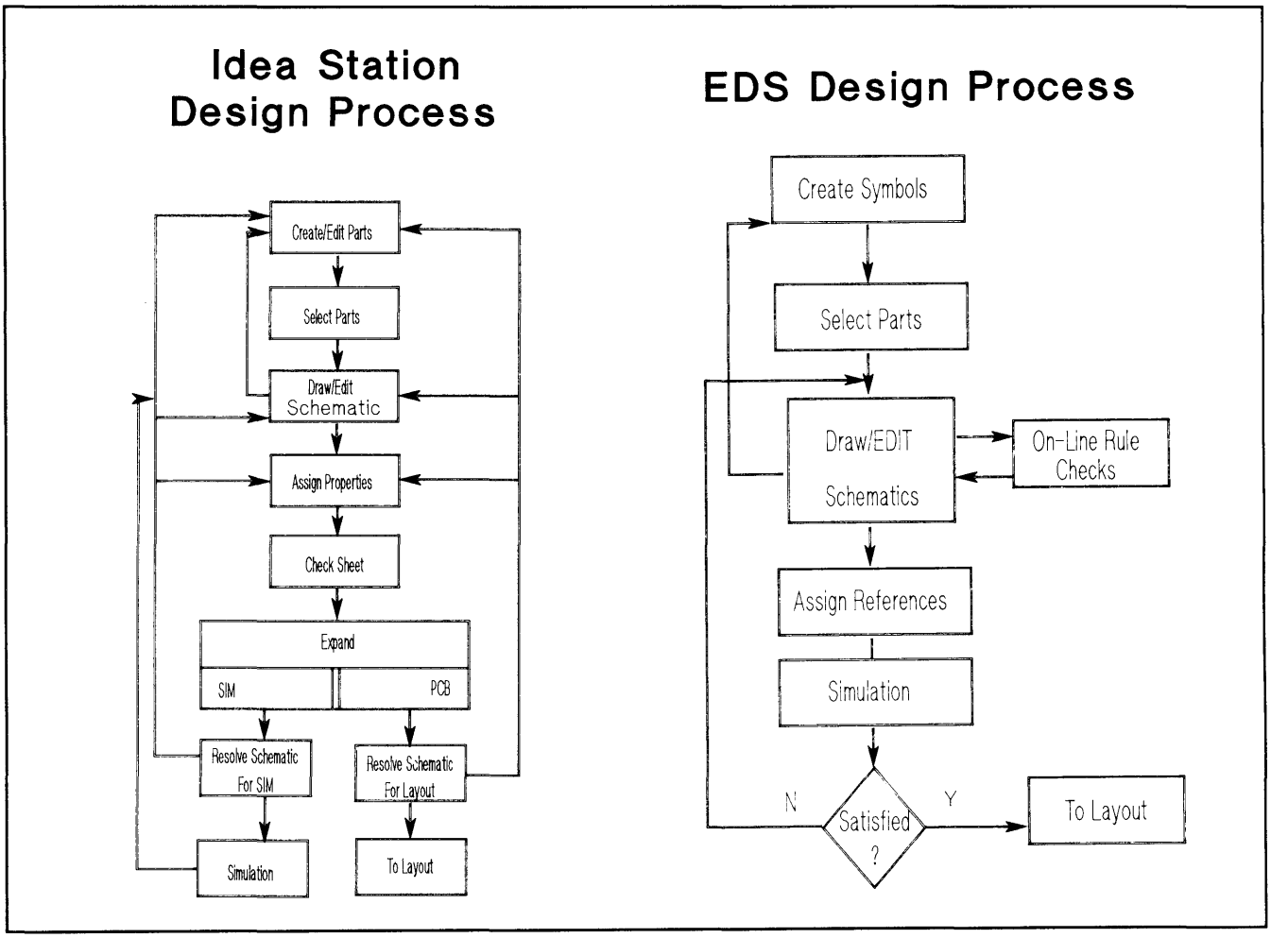

Figure 9: Idea Station Design Process vs. HP EDS Design Process

Figure 10 is a spider diagram showing comparisons of the standard logic design entry systems of Mentor and HP. The parameters and their attributes chosen for Mentor's Idea Station and HP's EDS are:

- User Interface
  - —flexible command entry
  - —operating system access
  - —windowing
  - —customizability
  - —commonality
- Libraries
  - —coverage
  - —completeness
  - —creation
  - —standards
- Editor
  - —graphics performance
  - —speed of design entry
  - —part selection
  - —design rule checking
  - —flat design
  - —hierarchical design
- Capacity
  - —IC design
  - —PCB design
- Data Access
  - —industry standard database
  - —access language
  - —design file access
- Links
  - —EDIF
  - —IGES
  - —test
  - —simulation
  - —layout
  - —documentation
- Technology
  - —PCB
  - —IC
- General
  - —learning tools
  - —revision control
  - —quality
  - —engineering changes

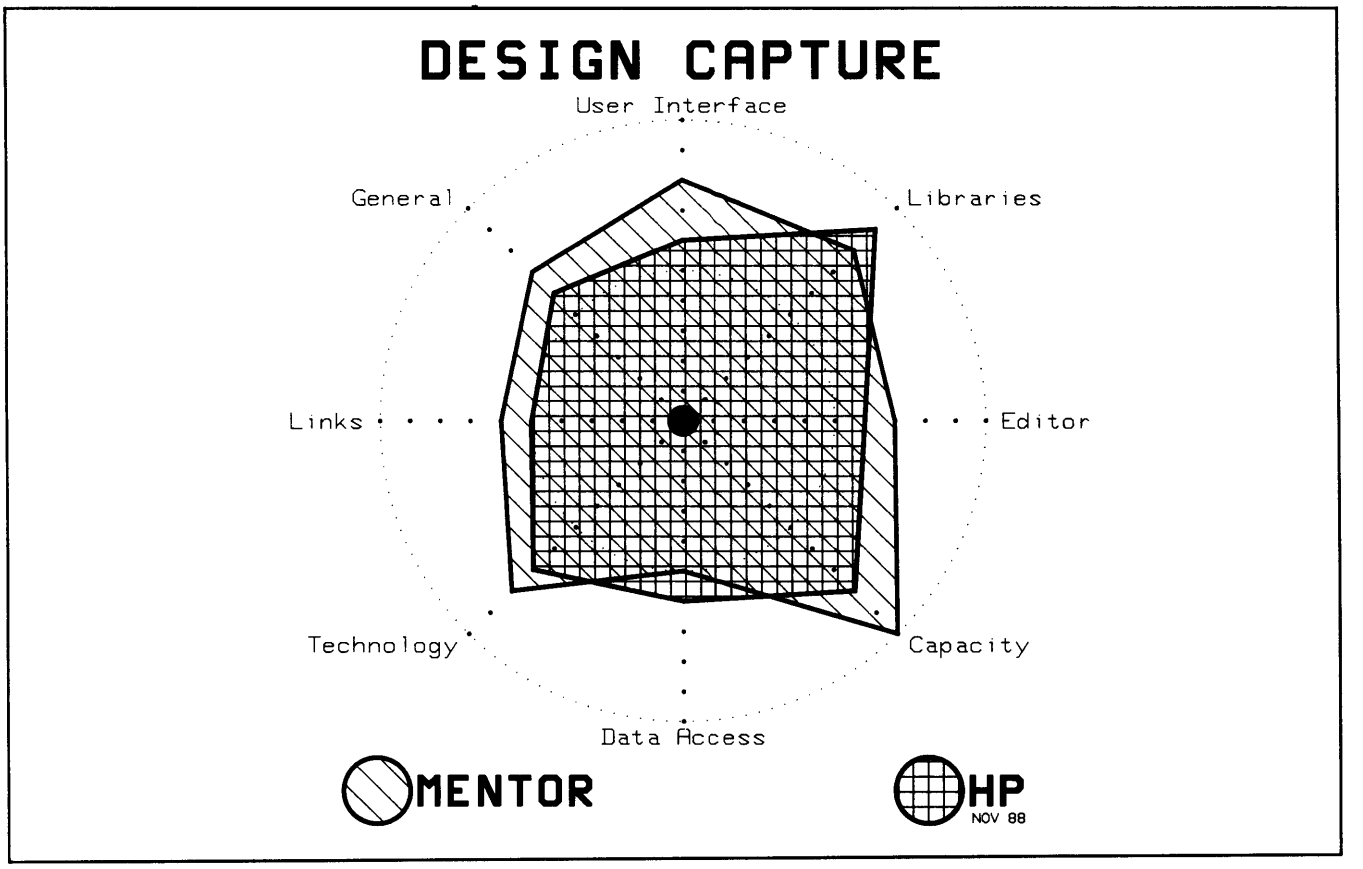

Figure 10: Standard Logic Design Entry

Mentor Idea Station Strengths

- **Graphics Performance** — System response for basic graphical functions (drawing schematics) was superior to HP DCS on equivalent hardware.

- **Flexible Command Entry** — The combination of redundant command-entry mechanisms (pull-down menus; function keys; or keyboard) provide attractive options for a range of users, beginner through expert.

- **Library Access** — The part location portion of the Idea Station library management was superior to HP DCS. It was easy to search through libraries for appropriate parts. Once located, only the data for that part was pulled into the system.

- **Context Window** — The context window shows the area of the design being edited. This makes it simple to move around within the design.

- **Simulation Models** — Three types of models are available (All three model types can exist in one design,):
  1) Quick Parts -- Simulation models created by compiling sheet-based models into a single primitive. Sometimes referred to as LCC or levelized compiled code models.
  2) Sheet Parts -- use an underlying schematic of primitives to define functionality and timing.
  3) BLM (Behavioral Language Models) -- use a C or Pascal-based hardware modeling language to define complex functionality.
  4) HML(Hardware Modeling Library) -- allows actual components to be used in modeling

- **File Management** — Apollo's Domain environment effectively manages the multitude of files generated by the Mentor application.

HP EDS Strengths

- **Database/DDL** — The Design Database Language is included with HP DCS. HP DDL also helps coordinate files. For instance, Mentor places files out of sync if the user expands for SIM but forgets to expand for MISC. Also, HP DDL is easier to use than Mentor's extraction tools.

- **Consistent User Interface** — The user interface for schematic capture, part creation, DVI, documentation page, etc. is consistent in HP EDS.

- **Superior Hierarchical Design Support** --
  HP DCS provides hierarchical design capabilities:
  — All symbol page functionality in top down mode
  — Hierarchical block ("local symbols") are converted into parts at the user's request without closing and saving the design
  — Automatic connector creation on the circuit page
  — Automatic symbol creation
  — Ability to check symbol pin/connector mapping

- **Part Creation** — The symbol, loading, physical, and scion pages make it very easy to create parts in HP DCS. HP DCS's consistent user interface minimizes the confusion and time required when jumping between Mentor's NETED and SYMED.

- **On-line Rule Checking** — On-line rule checking minimizes the time spent debugging the design before it can be expanded for layout (assigning references) or simulation (opening the simulation page). On Mentor, the benchmark PCB required three hours of debugging before EXPAND could be completed successfully. Plus, all the errors were mismatches between pin properties, connectors, splitters, wires, busses, etc.

- **Interactive Graphical Simulation Interface** — Mentor does not have a graphical interface for defining simulation vectors.

PLD Design and Verification

Mentor's PL Designer vs. HP PLDDS

Mentor currently offers a third party product from MINC called PL Design which Mentor had licensed as a standalone PLD solution (Mentor's PL Designer). HP offers the proprietary PLDDS. Mentor recently purchased MINC's PLD technology. Mentor's new product will be called PLDSynthesis and will be integrated with NETED and QuickSim.

Figure 11 shows comparisons of Mentor's current PL Designer and HP PLDDS. The parameters chosen for Mentor's PL Design and HP PLDDS are:

- Test Generation
- CAE Links
- Editors
- Manufacturing Links
- Device Independence
- Coverage
- Usability

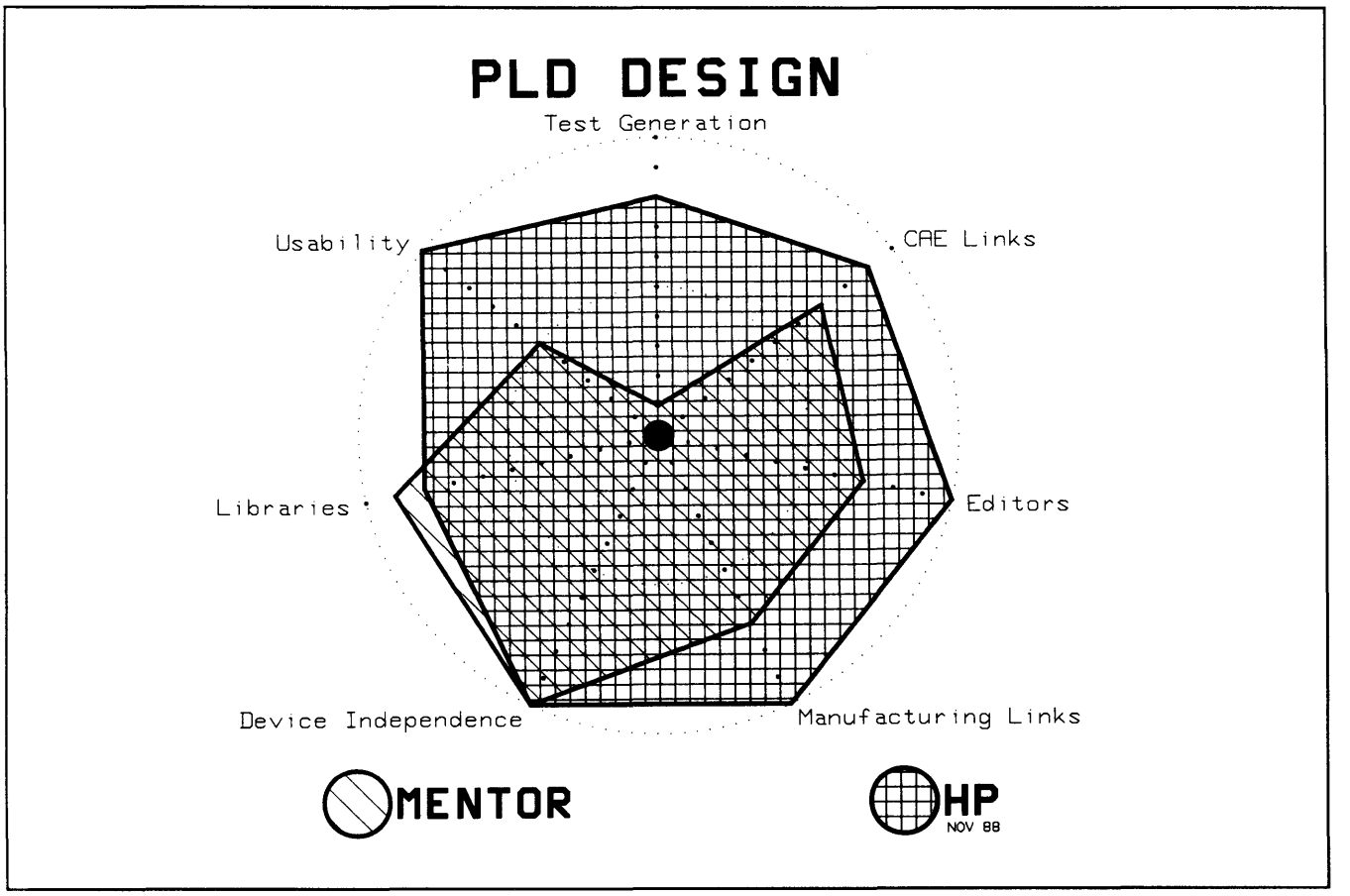

Figure 11: PLD Design

Mentor's PL Designer Strengths*

- **Quicker device support (through more frequent customer updates)**
- **More flexibility in automatic device selection/ partitioning**
- **Lower price**
- **PC support**

*Mentor's new PLDSynthesis will only be featured on Apollo. It will be fully integrated into the Mentor design center environment, i.e. schematic editor, simulation environment, common database, and common documentation.

HP PLDDS Strengths

- **Graphical Debuggers for Schematic, Waveform, and STD entry**
- **Support of Hierarchy for STD entry**
- **Support of mixed abstractions with Hierarchy**
- **Automatic and Functional Test Vector Generation**

Standard Logic Verification

Mentor Simulation Strengths

- **Dynamic display of simulation results** — The ability to dynamically update the graphical simulation output on the screen as the simulator is running. Mentor users maintain that Mentor's simulation display is not very useful in normal work. For example, they claim it is not possible to analyze results in real time as the results scroll by. These capabilities should soon be available on HP with System HILO®.

- **New static timing verifier** — A strong graphical interface. Runs faster than dynamic timing analysis (HP's method) and does not require input stimulus.

HP EDD Simulation Strengths

- **Dual-delay analysis***
- **Hazard monitoring/path trace-back***
- **High-level waveform language, (this is a big issue with Mentor users)***
- **Waveform comparisons**
- **Link to prototype test**

***System HILO release**

Documentation

Mentor DOC (Documentation Preparation System) Strengths

- **Professional writing tool** — Designed for documentation professionals in a team environment. Full WYSIWYG tool.
- **Hot links to graphics** — Graphics information can be imported from the Mentor design products. "Hot links" allow the latest version of the graphics to be extracted from the design products on the network at printing time.
- **Strong revision control** — Outstanding revision control is incorporated in the product allowing total reconstruction of all versions and tracking of all changes.
- **Major project tool** — Designed for the creation of the formal written documents needed to release a product. The Trident submarine project is a quoted example. Mentor uses DOC to generate the manuals for their design products.

HP FrameMaker Strengths

- **Interactive page and document layout**
- **HP FrameViewer** — provides view-only access to FrameMaker documents
- **International FrameMaker** — provides localization in 5 languages.

ASIC Design and Verification

Mentor QUICKSIM vs. HP HILO-3/DVI

Figure 12 is a spider diagram comparing the ASIC design and verification systems from Mentor and HP. The parameters chosen for Mentor's QUICKSIM and HP's DVI/HILO-3 are:

- Simulation/Testor Compatibility
- Modeling Language
- Libraries
- Timing
- Capture/Simulation Integration
- Delay Estimation Annotation
- Performance
- Capacity
- Actual vs. Expected Results

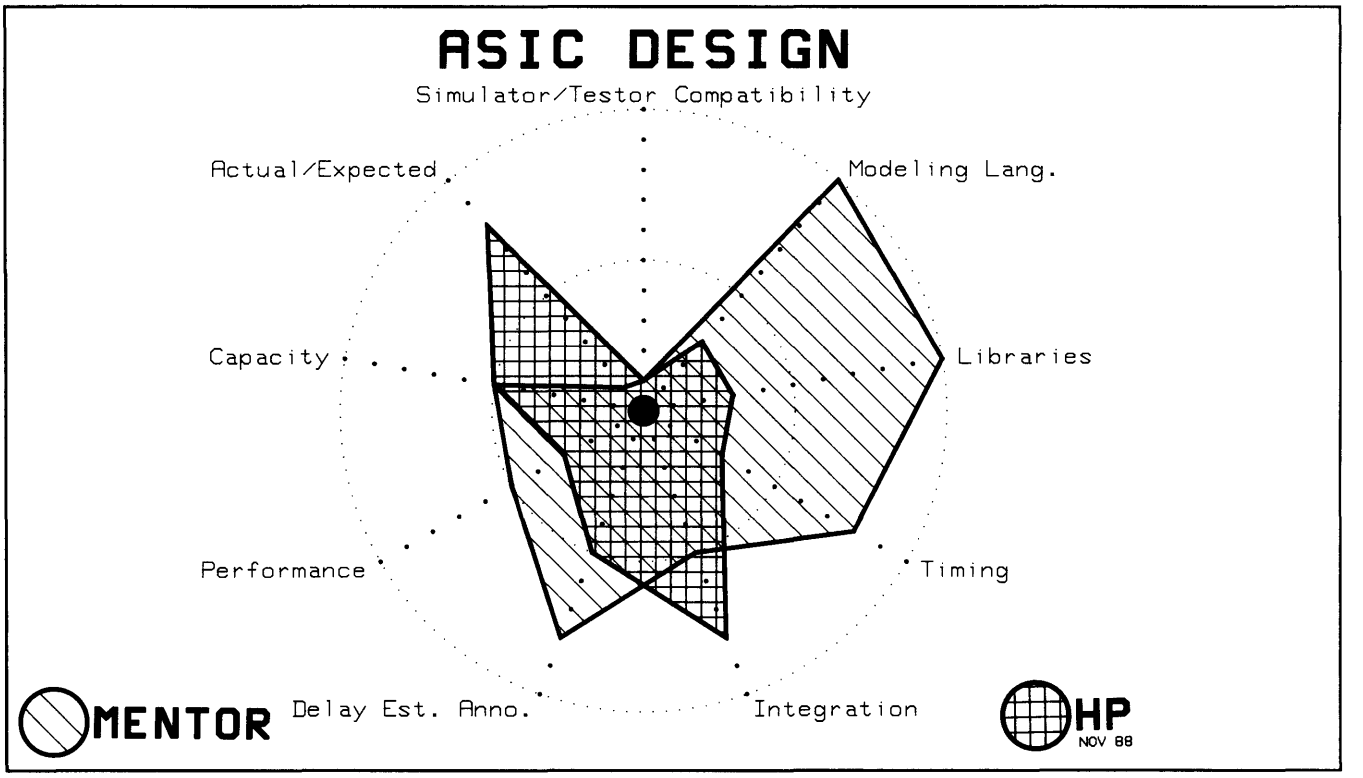

Figure 12: ASIC Design

Mentor QUICKSIM Strengths

- **Library Support**
- **Performance**
- **Behavioral Modeling Language**
- **Interactive Capabilities**
- **Timing Analysis**
- **Delay Estimation, Annotation**

HP DVI/HILO-3 Strengths

- **Integration with Schematic Capture**
- **Ease of Use**
- **Actual vs. Expected Results**

PCB CAD (Board Layout)

Figure 13 is a diagram of the design processes of Mentor Board Station system layout and HP PCDS. Both are very similar in concept.

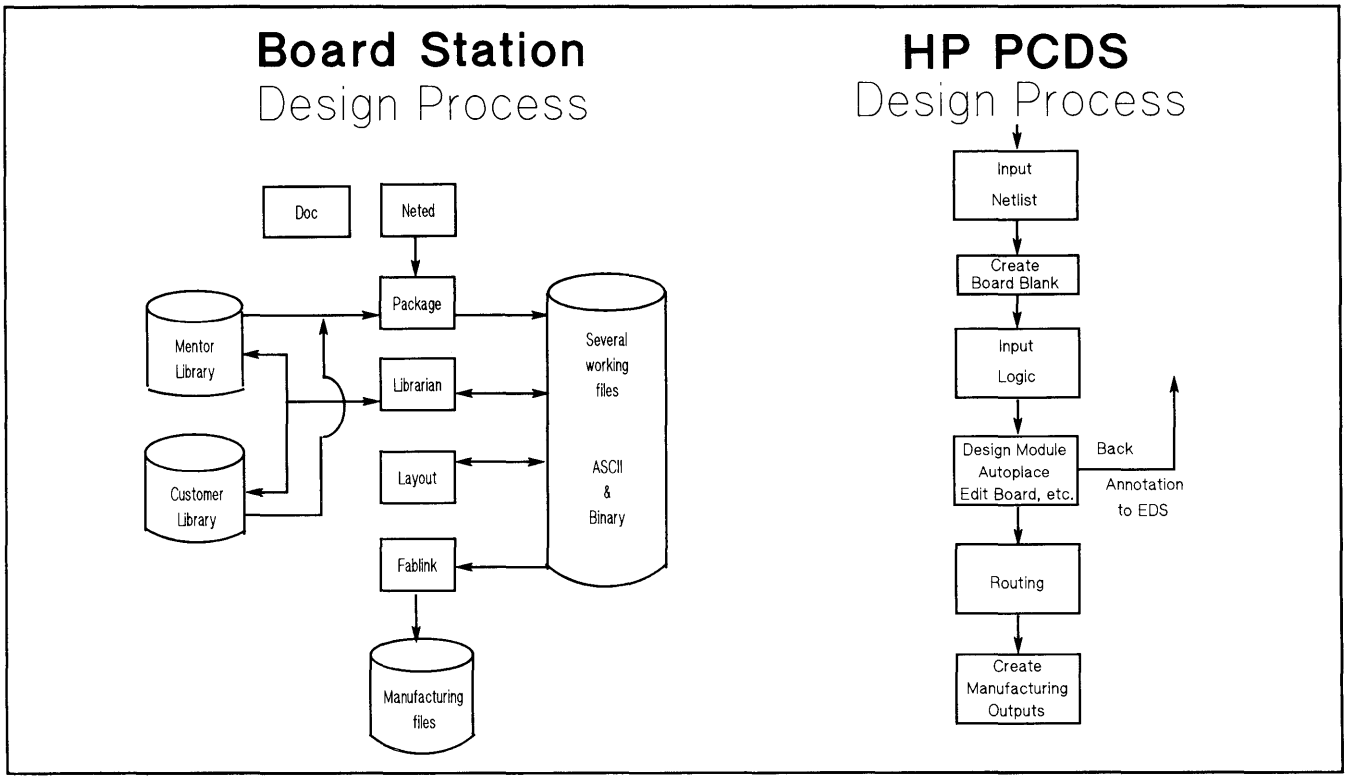

Figure 13: Board Station Design Process vs. HP PCDS Design Process

Board Station:

- **NETED** — (Similar to HP DCS). Provides circuit information to BoardStation.
- **ProtoView** -- Allows engineers to try component packaging and placement before releasing to CAD groups.
- **PACKAGE** — (Similar to HP PCDS's Parts Transfer and ME-10 link). Combines library package information with schematic nets and components. Board blanks are also created with PACKAGE.
- **LIBRARIAN** — (Similar to PCDS's Librarian). Creates new library parts and modifies existing ones.
- **LAYOUT** — (Similar to PCDS's Design Module). Manual and automatic signal/supply routing.
- **FABLINK** — (Similar to PCDS's Fabric or Automatic Phototools). Creates manufacturing output files.

The above process is comparable to HP PCDS's input of the net list followed by board blank creation, addition of logic, running the PCDS design module, and then routing and manufacturing outputs.

Figure 14 is a spider diagram comparing Mentor and HP board layout systems. The parameters and attributes chosen for this comparison are:

- Manufacturing Outputs
  - —panelization
  - —photoplotters
  - —drill
  - —pick and place
  - —assembly drawings
  - —reports
- Library
  - —creation
  - —maintenance
  - —vendor supplied quantity
- Editing
  - —interactive placement
  - —interactive routing
  - —design rule checking
  - —logic information access
- Place & Route
  - —automatic placer
  - —automatic router
- Technology
  - —surface mount
  - —through hole
  - —hybrid thick film
  - —hybrid thin film
  - —multi layer
  - —metal core
  - —ECL
- Links
  - —front end
  - —mechanical engineering
  - —documentation
  - —thermal
  - —test
  - —EDIF
  - —IGES
  - —open system
- General
  - —user interface
  - —customizability
  - —quality
  - —reliability
  - —engineering changes

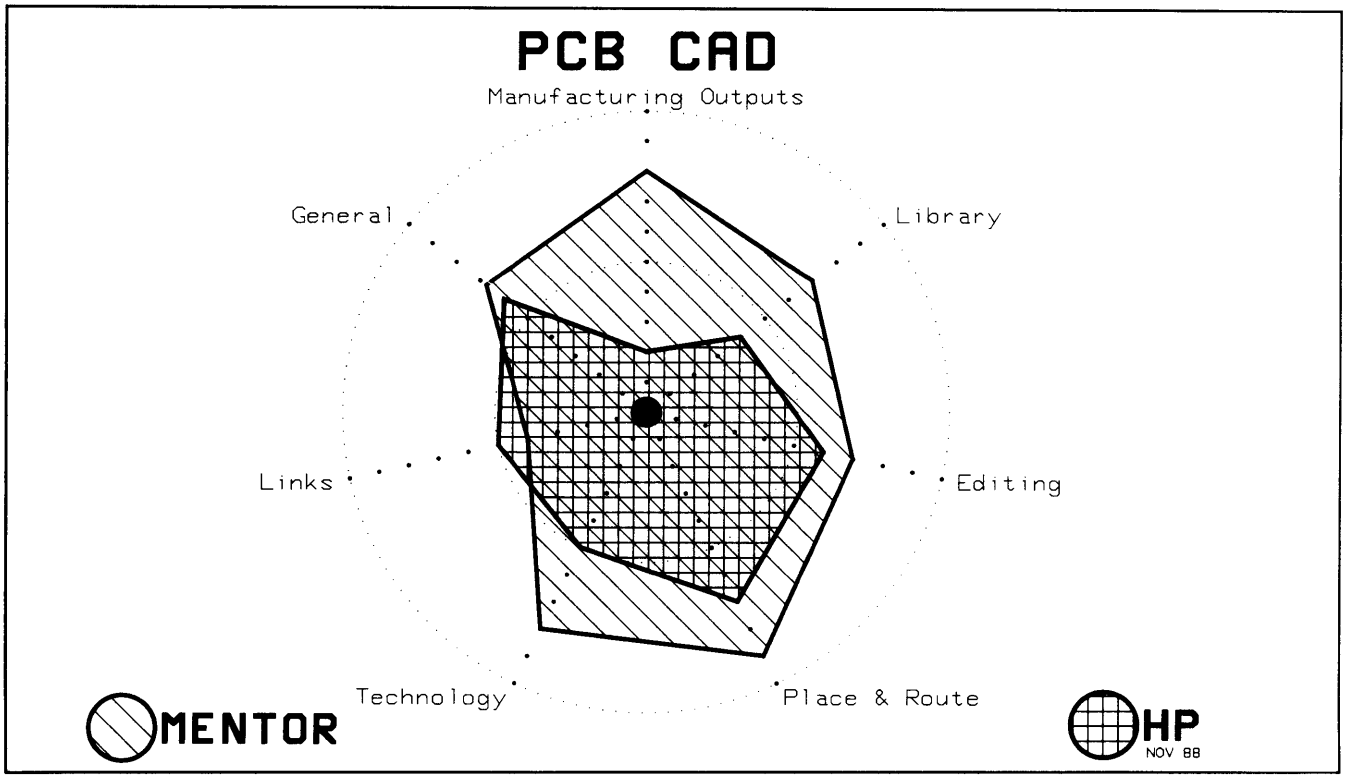

Figure 14: Board Layout

Mentor Board Station Strengths

- **Human Interface** — Includes both new (rev. 6.0, mid 88) pop-up cascading menus (like HP DCS) and older static menus on screen. Pop-up dynamic forms are used for information input. The menus are customizable (like HP EGS) to allow the system to be tuned to site needs. The entire system runs in a windowing environment. Users can create macros with IF/THEN/ELSE constructs that call Board Station and other operating system functions (like ME-10 or HP EGS does). The human interface is consistent with, but not exactly the same, as Mentor's NETED.

- **Interactive** -- Board Station's windowing environment, system speed and access to the operating system are all good and getting significantly better. The interactive routing capabilities are very strong. Clearance bounds are shown when DRC is turned off. Plot, print and screen dump are all easy to perform and quick to respond.

- **Librarian** — Graphical library part creation is very easy to use. The large library of parts has recently added Mil Spec parts. The SMD via and route restricts are a component of parts definition.

- **Router** — Three routers are included (pattern, automatic rip up, & random), which have excellent completion rates and performance. A medium number of vias are inserted. The placer is a full/semi/manual system that also works well and is easy to use. Mentor advertises their placer is the best in the industry.

- **Manufacturing Outputs** -- With Board Station Gerber can be batched and the file is editable. The gerber wheel file can be automatically generated. Panelization is included as part of the system. Fabrication drawings are created with ME-10 like capabilities as part of FABLINK.

- **Good Integration Between Schematic & Layout** — Good information flow between Board Station and NETED, Package Station and DOC. The schematic can be active on the screen of Board Station, allowing identification on the schematic while highlighting both the schematic and printed circuit board of components picked on the schematic. Package design information, board blank and parts placement can move into Board Station from the Package Station. Pictures from Board Station can be transferred to DOC.

- **Product Releases** -- Mentor has been releasing new powerful revisions of products every 6 months. The files are upward compatible. It is easy and quick for a customer to do an update, with complete instructions included so they can do it themselves.

- **Other** -- Mentor offers a complete product line (DesignCenter like concept) including schematic capture, digital simulation, analog simulation, hardware modeler, custom IC, standard cell, gate array, PCB, documentation and package design. Future products will probably include more links to test and hybrid circuit design. The manuals for Board Station are written for PCB designers and look very good (created with DOC). Training includes both regular classes and self paced training. Mentor actively advertises. The theme in their advertising is "We are the best" with a focus on individual products, including Board Station. The price/performance of Board Station is very good.

HP PCDS Strengths

- **HP EDS Front End** — HP EDS competes well with Mentor's NETED. Hierarchical design methodology is not supported with the Mentor front-end and back-end.

- **Open Links to Other Systems** — HP is committed to an open structure, allowing our access to other CAD systems data. Mentor does not like to merge with other systems, instead preferring to replace everything.

- **Links to Test and Manufacturing** -- HP is perceived to be a superior provider of links to test, and Mentor concedes this application. This should be a very strategic sales tactic for HP.

- **HP Service/Support** — HP has a strong company reputation for quality hardware and support. Number 1 ranking in DataPro, five consecutive years.

- **Superior Platforms** — Performance and Reliability of HP platforms is better than Apollo.

- **Cost of Ownership** — Support costs of Board Station are almost 2:1 higher than HP.

Mentor Buzz-Word List

October 12, 1988

AccuLib
Analog parts library for Accu Sim.

AccuSim
Mentor's new proprietary analog simulator.

Analysis/RT
Mentor's CASE system specification tool.

Auditor
Documentation and requirements traceability tool of Mentors that conforms to DOD-STD-2167A.

AutoTherm
Mentor's PCB thermal analysis tool, FEA-based, part of Package Station.

AVIDesigner
(ASIC Vendor Independent Designer) Mentor's capability to capture generic schematics and retarget the same schematic to different ASIC vendors or technologies

Board Station
Mentor bundled Apollo-based PCB layout software. (Registered Trade Mark)

Capture Station
Mentor Apollo platform with design capture software. (Trade Marked). Bundled system.

Cell Station
Mentor workstation based on Apollo and logical and physical design software for standard cell integrated circuits, bundled system. (Not Trade Marked)

CELLFLOOR
Mentor standard cell floor plan tool.

CELLGRAPH
Mentor standard cell manual editor.

CellPlace
Mentor standard cell placer routine. (Trade-Mark)

CELLPOWER
Mentor standard cell power routing tool.

CellRouter
Mentor standard cell signal router. (Trade Mark)

Change Control
Mentor's (context) revision control system for their documentation tools.

Chip Station
Mentor bundled system of Apollo hardware and custom IC software. (Trade Mark)

ChipGraph
Mentor full-custom IC layout tool that outputs GDSII and CIF.

ChipLister
Mentor procedurial I/F information ChipGraph IC database.

Compute Engine
Mentor term for a computational server. (Trade Mark) Proprietary Hardware.

Mentor Buzz-Word List, cont'd

DCA
Mentor utility that transports documentation files from PC-based word- processing packages into Contex documentation tool. (Trade Mark)

Design Station
Mentor system using Apollo hardware and design capture and documentation software, bundled. (Registered Trade Mark)

Designer
Mentor CASE software design tool.

DOC
Mentor documentation preparation package. Bundled with everything except Entry and Capture Stations. (TradeMark)

Dracula II
Mentor IC design rule checker. OEMed from ECAD (Cadence).

Entry Station
Mentor PC AT based schematic capture, DOS based, Software only. (Trade Mark)

FabLink
Mentor PCB fabrication link tools to manufacturing, NC, ATE and etc.

Falcon
Internal name for Mentor's next generation toolset. Widely known outside of Mentor.

Gate Station
Mentor bundled system of Apollo hardware and logic and physical design of gate array integrated circuits.

GateGraph
Mentor manual router for gate arrays.

GatePlace
Mentor gate array placement tool.

GateRoute
Mentor gate array routing package, autorouter.

Hardware Modeling Library (HML)
Mentor Hardware Modeling Library, allows actual components to be used in modeling. (Trade Mark)

HML
See Mentor's "Hardware Modeling Library"

Idea Station
Mentor bundled system based on Apollo and design capture, simulation and documentation software. (Trademark)

LAYOUT
Mentor PCB placement and routing tool. (Trade Mark)

LIBRARIAN
Mentor PCB library editor. (Trade Mark)

MSIMON
One of Mentor analog simulators. Digital MOS only Simulator.

MSPICE
Graphical front-end to any SPICE simulator. Berkley 26.6 included in product. (Trade Mark)

MSPICE PLUS
MSPICE front-end to ADT's SPICE PLUS simulator.

Mach 1000
Mentor's recommended solution for a simulation accelerator. Available from Zycad.

Mentor Buzz-Word List, cont'd

NETED
Mentor schematic capture tool. (Trade Mark)

Package Station
Mentor package design and analysis tool, includes 3D and thermal analysis.

PACKAGE
Mentor PCB signal to physical packaging tool. (Trade Mark)

PCB Portal
Mentor feedback method from Package Station back to Board Station, allows board blank changes.

PicEd
Mentor IDEA system picture editor. Allows drawing capability to be included in DOC. (Trade Mark)

QuickFault
Mentor fault simulation product, with links to Tektronics DAS9200.

QuickFault LAN
Server portion of QuickFault (i.e. no front-end) to be used for LAN-based acceleration of fault grading.

QuickGrade
Mentor's patented probabilistic fault grader.

QuickPart Build
QuickPart builder . (Trade Mark)

QuickParts
Mentor part library of compiled sheet parts. More accurate and less disc space used.

QuickPath
Mentor digital critical path analysis tool.

Quicksim
Mentor digital simulator.

QUICKSIM
Same as Quicksim. (Trade Mark)

REMEDI
Mentor IC graphical LVS checker correlator between schematic and layout.

RSIM
Remote simulation interface.

SCD
Structured Chip Design, Mentor's buzz about their design methods used in ChipGraph.

SmartParts
Mentor PCB parts library. (TradeMark)

SYMED
Schematic symbols graphics editor used by Mentor, does not need to enter NETED to use. (Trade Mark)

Table Generator
Mentor optional software product in Contex documentation management; builds tables out of information. (Trade Mark)

3D Design Station
Mentor's mechnical design station without the thermal analysis capability.

Appendix A: Mentor Graphics Corporation Pricing

Mentor List Prices: (source Mentor Graphics Price list of October 1988) $US

ENTRY STATION - PC/AT Based - Schematic Capture only

Entry Station	$1,995 *	$25 **	(software only)

CAPTURE STATION - Apollo Based - Schematic Capture Only (NetEd)

DN3010M-4.0/19	$12,500 *	$166 **
DN3010C-4,0/19	$22,500	$206
DN3500M-8.0/19	$31,900	$293
DN3500C-8.0/19	$41,900	$353
DN3500EC-8.0/19	$48,900	$403

DESIGN STATION - Apollo Based - Schematic Capture (NetEd), Remote Simulation (RSIM) and Documentation (DOC)

DN3010-4.0/19	$23,700	$248
DN3010C-4.0/19	$33,700	$268
DN3500M-8.0/19	$42,900	$403
DN3500C-8.0/19	$52,900	$463
DN3500EC-8.0/19	$59,900	$513
DN4500M-16.0/19	$64,900	$544
DN4500C-16.0/19	$74,900	$606
DN4500EC-16.0/19	$81,900	$656
DN10010C-16.0/19	$149,900	$1,198
DN10020C-16.0/19	$194,900	$1,538
DN10030C-16.0/19	$239,900	$1,878
DN10040C-16.0/19	$284,900	$2,218

IDEA STATION - Apollo Based - Schematic Capture (NetEd), Local Simulation (QUICKSIM) and Documentation (DOC)

DN3010M-4.0/19	$33,700	$348
DN3010C-4.0/19	$43,700	$368
DN3500M-8.0/19	$52,900	$503
DN3500C-8.0/19	$62,900	$563
DN3500EC-8.0/19	$69,900	$613
DN4500M-16.0/19	$79,900	$692
DN4500C-16.0/19	$89,900	$756
DN4500C-16.0/19	$96,900	$806
DN10010C-16.0/19	$169,900	$1,398
DN10020C-16.0/19	$214,900	$1,733
DN10030C-16.0/19	$259,900	$2,078
DN10040C-16.0/19	$304,900	$2,418

Appendix A: Mentor Graphics Corporation Pricing cont'd

BOARD STATION - Apollo Based - Schematic Capture (NetEd), Remote Simulation (RSIM), Documentation (DOC), Parts Assignment (PCB PACKAGE), Parts Creation (LIBRARIAN), PCB Placement and Routing (LAYOUT), Links to Manufacturing (FABLINK)

DN3010C-4.0/19	$73,700	$806
DN3500C-8.0/19	$90,900	$843
DN3500EC-8.0/19	$97,900	$893
DN4500C-16.0/19	$118,900	$1,046
DN4500EC-16.0/19	$125,900	$1,096
DN10010C-16.0/19	$199,900	$1,698
DN10020C-16.0/19	$244,900	$2,038
DN10030C-16.0/19	$289,900	$2,378
DN10040C-16.0/19	$334,900	$2,718

PACKAGE STATION - Apollo Based - 3D Design & Drafting (3D DESIGN), Thermal Analysis (AUTOTHERM), Link to Board Station (PCB PORTAL), and Documentation (DOC)

DN3010C-4.0/19	$59,700	$715
DN3500C-8.0/19	$76,900	$703
DN3500EC-8.0/19	$83,900	$753
DN4500C-16.0/19	$104,900	$906
DN4500EC-16.0/19	$111,900	$956
DN10010C-16.0/19	$184,900	$1,548
DN10020C-16.0/19	$229,900	$1,888
DN10030C-16.0/19	$274,900	$2,228
DN10040C-16.0/19	$319,900	$2,568

WORKSTATION OPTIONS - Apollo Based

170Mb Disk	$4,500		$57
380Mb Disk	$7,500		$91
2Mb RAM (DN3000)	$1,600	(8Mb Total)	$8
8Mb RAM (DN3500)	$6,500	(32Mb Total)	$32
16Mb RAM (DN4500)	$13,000	(32Mb Total)	$64
16Mb RAM (DN10000)	$12,800	(128Mb Total)	$24
DN10000CPU Upgrade	$47,500	(4 CPUs Max)	$130
60Mb Cartridge Tape	$2,000		$27
IBM PC Co-processor	$2,700		$27

TRAINING CLASSES

IDEA Station Basic training	4 days	$1,200/student
IDEA Station Basic training	4 days on site	$9,600/class
Board Station Basic Training	5 days	$1,500/student
Board Station Basic Training	5 days on site	$12,000/class
SystemManagement training	4 days	$1,200 /student
System Management training	4 days on site	$1,200/day
IDEA Station training videos		$1,100/set
Package Station training videos		$1,100/set

Appendix A: Mentor Graphics Corporation Pricing cont'd

* Standard list price, subject to standard discount table of Dollar Volume Discount

(in thousands)	
$0-$100	LIST
101-250	5%
251-500	10%
501-1,000	14%
1,001-2,000	17%

** Basic monthly hardware and software maintence. Hardware maintence consists of on site maintenence with 24 hour response 5 days a week. A response center support line with 2 hour response for application and operating system questions as well as modem access for electronic communication is included in the quoted prices. A monthly bulletin is part of the service. Software revisions and manual revisions are included.

Appendix B: Product Coverage Comparison

	Conventional PCB		PLD ASIC	
Design Step	Mentor	HP	Mentor	HP
Architecture Design				
Structured Des.				
HW/SW Partition				
Implm. Indep.			PLDesigner	PLDDS
Library Parts				
Sch. Parts Creat	SYMED	DCS/PCDS		
PCB Parts Creat	Librarian	DCS/PCDS		
Hardware Models	HML	yes		
Mil Std Parts		no		
Design Capture	NETED	DCS		
Behavioral	BML	HILO HDL	PLDesigner	
Wave/STD/Boa			PLDesigner	PLDDS
Schematic Capt	NETED	DCS		PLDDS/DCS
Digital Simulation	QUICKSIM	HILO-3/ System HILO		HILO-3/ System HILO
Logic Sim.	QUICKSIM	System-HILO		System-HILO
HW Sim.	HML	HiChip		HiChip
Fault Analysis	QUICKFAULT	HILO FAULT		HILO FAULT
Timing Analysis	QUICKSIM/PATH	System-HILO HiTime		System-HILO HiTime
Analog Simulation	MSPICE	AWB/Saber		
SW Analog				
Mixed Mode		no		
Stress/reliabil		AWB/Saber		
RF/microwave		MDS		
Physical Layout	LAYOUT	PCDS		
Edit	LAYOUT	PCDS		
Forced Router	yes	yes		
Rip-Up Router	yes	yes		
Random Route	yes	no		
Other Router		no		
DRC		on-line		
Manuf. Outputs	FABLINK	Mfg links		
Prototype Testing				
Waveform Cap/Com		HP16500A		HP16500A
Digital HW Test		HP16500A		HP16500A
Analog Waveform				
Analog HW Test				
System Integr Test				

Appendix B: Product Coverage Comparison, cont'd

	Conventional PCB		PLD ASIC	
Design Step	Mentor	HP	Mentor	HP
Mfg. Test Prep. Fault Analysis Test Generation Tester Links	TSSI	3065/TSSI		
Mechanical Design 2D 3D Thermal Analysis	PACKAGE PACKAGE AutoTherm	ME-30 ME-30		
Documentation Text & Graph Integrated Tech. Pub.	DOC DOC DOC	FRAME FRAME FRAME		
SW Firmware	Designer	HP64000		
Engineering Parts				
Project Mgmt.				
Design Mgmt.		DSM		
File Management	Domain OS	DDC		
Misc	Expand_PCB Expand_SIM			
Silicon Compilers				
System Level Sim				
MSPICE PLUS				

Appendix B: Product Coverage Comparison, con'td

	Standard Cell ASIC		Gate Array ASIC	
Design Step	Mentor	HP	Mentor	HP
Architecture Design Structured Des. HW/SW Partition Implm. Indep.			AVID	
Library Parts Sch. Parts Creat PCB Parts Creat Harware Models Mil Std Parts	Vendor Kits	DCS	Vendor Kits	DCS
Design Capture Behavioral Wave/STD/Boa Schematic Capt	NETED	DCS	NETED	DCS
Digital Simulation Logic Sim. HW Sim. Fault Analysis Timing Analysis	PCDesigner	HILO-3/ System HILO System-HILO HiChip HILO FAULT System HILO/ HiTime	QUICKSIM	HILO-3/ System HILO System-HILO HiChip HILO FAULT System HILO/ HiTime
Analog Simulation SW Analog Mixed Mode Stress/reliabil RF/microwave				
Physical Layout Edit Forced Router Rip-Up Router Random Router Other Router DRC Manuf. Outputs	CELLFLOOR CELLGRAPH CELLPOWER/ CELLROUTER/ GATEROUTE DRACULA II CHIPGRAPH		CELLPOWER/ CELLROUTER/ GATEROUTE	
Prototype Testing Waveform Cap/Com Digital HW Test Analog HW Test		HP16500A HP16500A		HP16500A HP16500A
System Integr Test				

AppendixB: Product Coverage Comparison, con'td

	Standard Cell ASIC		Gate Array ASIC	
Design Step	Mentor	HP	Mentor	HP
Mfg. Test Prep. Fault Analysis Test Generation Tester Links		DICE		DICE
Mechanical Design 2D 3D Thermal Analysis				
Documentation Text & Graph Integrated Tech. Pub.				
SW/Firmware				
Engineering Parts				
Project Mgmt.				
Design Mgmt.				
File Management				
Misc				
Silicon Compilers	GENESIL CONCORDE			
System Level Sim				

Appendix B: Product Coverage Comparison, con'td

	Custom ASIC		Hybrid	
Design Step	Mentor	HP	Mentor	HP
Architecture Design Structured Des. HW/SW Partition Implm. Indep.				
Library Parts Sch. Parts Creat PCB Parts Creat Harware Models Mil Std Parts				
Design Capture Behavioral Wave/STD/Boa Schematic Capt				
Digital Simulation Logic Sim. HW Sim. Fault Analysis Timing Analysis	 QUICKSIM	HILO-3/ System HILO System-HILO HiChip HILO FAULT System HILO/ HiTime	 QUICKSIM	
Analog Simulation SW Analog Mixed Mode Stress/reliabil RF/microwave	MSIMON	AWB/Saber MDS		
Physical Layout Edit Forced Router Rip-Up Router Random Router Other Router DRC Manuf. Outputs	CHIPGRAPH CELLGRAPH CELLPOWER/ CELLROUTER/ GATEROUTE DRACULA II CHIPGRAPH			EGS/MDS
Prototype Testing Waveform Cap/Com Digital HW Test Analog HW Test		 HP16500A HP16500A		
System Integr Test				

Appendix B: Product Coverage Comparison, con'td

	Custom ASIC		Hybrid	
Design Step	Mentor	HP	Mentor	HP
Mfg. Test Prep. Fault Analysis Test Generation Tester Links		DICE		
Mechanical Design 2D 3D Thermal Analysis				
Documentation Text & Graph Integrated Tech. Pub.				
SW/Firmware				
Engineering Parts				
Project Mgmt.				
Design Mgmt.				
File Management				
Misc				
Silicon Compilers	GENESIL CONCORDE			
System Level Sim				


HEWLETT
PACKARD