HEWLETT PACKARD

Daisy/Cadnetix

vs

HP EE DesignCenter

Competitive Report
April, 1989

Electronic Design Division
Fort Collins, Colorado
(303) 229-4335

For Internal Use Only

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Introduction

This report provides business and technical competitive information on Daisy Systems CAE/CAD business including the recent acquisition of Cadnetix Corporation, in comparison to HP's EE DesignCenter products. At the time of this writing, integration of the operations of Daisy and Cadnetix were only beginning. Other than the top management positions and organization, few decisions have been announced concerning product integration and marketing strategies. As a result, each section of the report presents Daisy information and Cadnetix information, with a summation of what might be the outcome the merger. Within this document, 'Daisy' refers to Daisy before the acquistion of Cadnetix and 'Cadnetix' refers to Cadnetix prior to the acquisition. Daisy/Cadnetix refers to the combined companies after the acquistion. The report is a reference tool for EDD's sales organization and is intended for HP internal use only.

The business analysis section contains both statistical information and background material on Daisy and Cadnetix. Business information was obtained through company press releases, brochures, SEC filings, outside research consultants, and customer contacts. The report is HP's interpretation of information in the public domain and information obtained through outside consultants. HP does not guarantee the information's completeness, timeliness, or accuracy.

The document also contains technical information on products offered by Daisy and Cadnetix and possible merged products as compared to EDD's product offerings. Product comparisons are based on technology comparisons, as opposed to product feature comparisons. Product strengths and weaknesses are also included. The technical information was obtained through field-based systems engineers and factory support engineers research and through the use of paid consultants.

Executive Summary

Daisy/Cadnetix believe they will emerge having the EDA industry's largest R&D investment, its most experienced and comprehensive sales force, and unparallelled depth in core system-design technologies — in other words, as the company best positioned to assume leadership of EDA solutions for system designers.

Daisy believes the merger will combine Cadnetix's strong position in the printed circuit board layout segment with Daisy's superiority in the design and simulation arenas. To Daisy's strengths in CAE, Cadnetix adds leadership in user interfaces, innovative work in front-to-back integration spanning CAE, CAD, and CAM, and a reputation as a technology leader. Some of the individual strengths that each company had, will dissipate once they are merged. For example, one of Cadnetix's strengths was good front-to-back integration. This will weaken if Cadnetix's back end is married to Daisy's front end, as the merger plan calls for.

Daisy/Cadnetix Strengths

- Exclusive focus on system and ASIC design problems
- Commitment to front-to-back integration
- Easy-to-master user interface across an entire product line
- Superior networking capabilities
- Strong financial management and sound business practices
- Substantial installed base
- Comprehensive worldwide service and support network

HP Strengths

- Open links to other vendors' CAD systems
- Comparably priced for full systems
- Hierarchical design support
- On-line rule checking
- Graphical simulation interface
- Superior provider of links to test
- Service and support
- Routing capabilities

Company Background

History

Daisy Systems was formed in 1980 by Aryeh Finegold and David Stamm, both former Intel engineers frustrated with the fact that the computer-aided technological revolution had not yet reached the electronic design process. Daisy was the first of three major computer-aided-engineering (CAE) companies in the early 1980's to deliver the Logician, a CAE workstationtargeted mainly for the IC design market. Revenues grew rapidly, but by 1985 the industry was changing and Daisy was struggling with the problems associated with an inexperienced management team. The electronic computer-aided-design (ECAD) market was maturing, with more sophisticated customers demanding easy to use products and standard platforms and operating systems. It was only in 1988 that Daisy finally made the transition to standard operating systems on standard platforms. Daisy chose the Sun 386i platform for this purpose. The current applications environment is primarily the SunOS version of UNIX with graphics users accessing applications via the X Windows system and networking via TCP/IP, NFS, and Ethernet.

In 1986 and 1987, officers with more experience in corporate business were hired. Norman Friedman joined the board of directors and in 1987 took over as CEO. By May 1988, Wall Street was confident that Friedman had indeed turned the company back toward profit and growth. In the meantime, however, Mentor had established clear leadership in the ECAD market with nearly double Daisy's revenues. It was agreed by industry analysts that Daisy would have to expand its product line, boost sales, and raise spending on research and development to remain competitive. Daisy was cash-rich and therefore an acquisition, as opposed to internal growth, was a more viable option to expanding the product line.

Cadnetix was founded in February 1982 by Bruce Holland, Steve Koch, and Gary Bliss. The focus of the firm was on providing an integrated front-to-back CAE/CAD/CAM design solution. The first system, the CDX-5000 printed circuit board design workstation, was shipped in late 1983. By June 1985, product sales were at $4.3 million and 50 seats had been shipped. The following year was filled with one product announcement after another. In 1986, Cadnetix announced its first IBM PC/AT- based products, adding a low-cost schematic capture option to their proprietary workstation-based design simulation and layout software. In 1987, Cadnetix announced an OEM agreement with SUN to offer a complete line of CAE/CAD/CAM systems based on the SUN workstation.

On June 6, 1988, Cadnetix acquired HHB Softron, a company specializing in logic and fault simulation. HHB Softron had just previously acquired Simucad, a software simulation company. Cadnetix's reasoning was to safeguard the source code for HHB's CADAT which Cadnetix had integrated into their overall product line to make the transition from one application to another more effortless.

On September 30, 1988, Daisy announced a hostile tender bid for Cadnetix after first trying to accomplish a friendly merger. It took approximately ten weeks before an agreement was reached. On December 13, 1988, Daisy acquired 50.1% of the stock of the combined companies of Cadnetix, HHB Softron, and Simucad for approximately $200 million (U.S.). **Figure 1** is a diagram depicting the merger of the companies.

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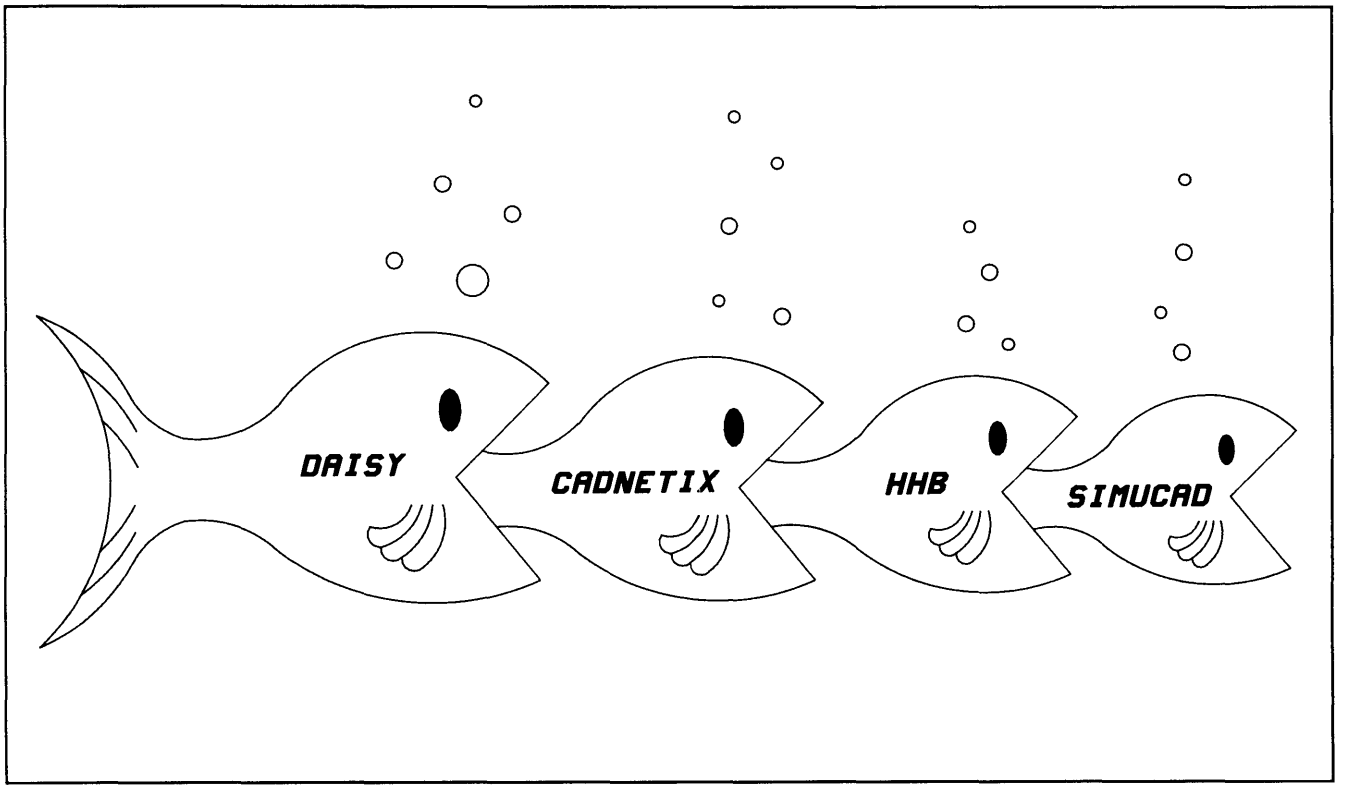

Figure 1: Diagram of merged companies

The merger plan called for Daisy and Cadnetix to function as one company by midyear 1989, although full integration of the two product lines was at least twelve months away from the time the merger was successfully accomplished. Daisy/Cadnetix began immediately to integrate management and employees.

Daisy/Cadnetix chairman and CEO, Norman Friedman, is a seasoned executive with a reputation for developing and successfully executing innovative business growth strategies. He oversees corporate development, finance and administration, domestic and international sales, customer support, operations and human resources.

Bruce Holland, founder of both NBI and Cadnetix, serves as president and COO of Daisy/Cadnetix. He is responsible for marketing, engineering and manufacturing, with integration of the two product lines as his primary focus for the near term. Many industry analysts identify Bruce Holland as the integral figure to making this merger a success. It is the Cadnetix engineers who must fit the Daisy software under their common user interface and into their product line. These engineers are intensely loyal to Bruce Holland and his vision. If Holland leaves Daisy/Cadnetix before the product line integration is complete, there is a strong possibility that key engineers will also leave. **Figure 2** is an organization chart of the new management structure in Daisy/Cadnetix.

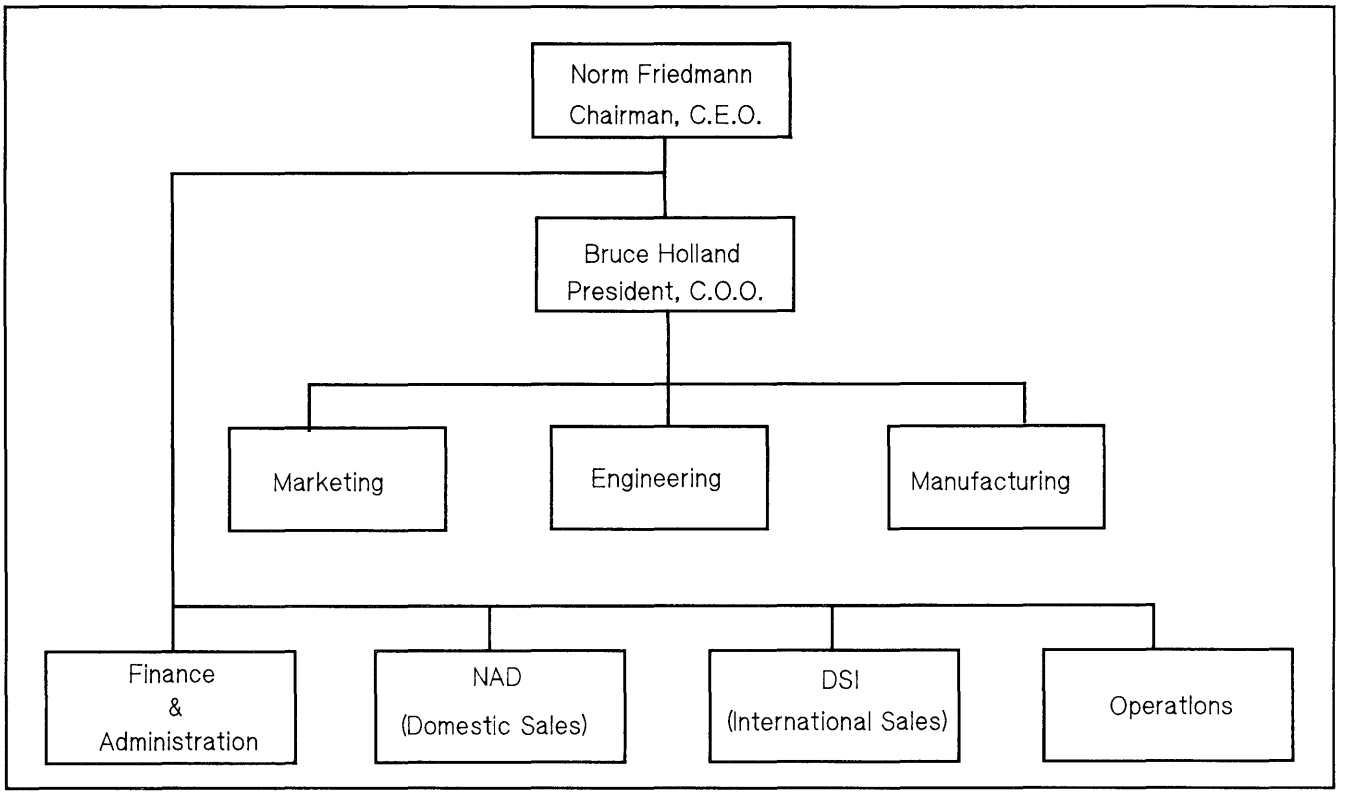

Figure 2: Daisy/Cadnetix Employee Organization Chart

Daisy/Cadnetix has broken the company up into five separate "sites" reporting to Norman Friedman, chairman and CEO, and Bruce Holland, president and COO. The sites are composed of Daisy headquarters in Mountain View, CA; Daisy's Israel Design Center; Cadnetix in Boulder, CO; and the Cadnetix subsidiaries: HHB Systems, Mahwah, N.J., and Simucad, Palo Alto, CA. HHB Systems will operate as an independent subsidiary with its own organizational elements and separate business mission in the areas of digital simulation, test, and hardware modeling, with specific focus on OEM relationships. There are rumors that Daisy/ Cadnetix is selling HHB, though they intend to keep CADAT, to Racal-Redac. The sale would alleviate some of Daisy/Cadnetix's current cash-flow problems.

According to Daisy's competitors, Daisy faces a severe challenge as it works to integrate Cadnetix, HHB Softron, and Simucad into its corporate and product structure. One issue Daisy and Cadnetix face is their tremendous product overlap. Both companies provide schematic capture, simulation, and PCB tools, so whose tools will be sold and supported? Cadnetix is well known for its implicit back annotation to their schematic capture from PCB layout. This large selling factor will disappear if Daisy's front end is integrated with Cadnetix's back end. There is also the fact that the product lines run on incompatible hardware. Daisy runs only on

History, cont'd

Intel-based architecture, namely the Sun 386i, IBM PC, and Logician, which may indicate that Daisy's product is not portable to the MC68000 architecture of Apollo and Sun 3/4 platforms. Currently, Daisy has almost all their products on the Sun 386i. Cadnetix currently runs most their products on Sun 3's with a few on the newer Sun 4's. Cadnetix's proprietary graphics accelerator is tied to the lesser selling Sun 3 and is not available on the more popular Sun 4.

Many of Daisy/Cadnetix's competitors believe the acquisition will propel Daisy/Cadnetix into a spiral of disorganization during which the competition will be able to pick off many Daisy and Cadnetix installations. Daisy/Cadnetix competitors are predicting the merger will put Daisy/Cadnetix out of commission for at least two years or more. Daisy software integration alone will require time-consuming rewrites to fit under Cadnetix's user interface. Daisy/Cadnetix is also faced with a support nightmare. Platforms, software, integration will cost them a tremendous amount of resources.

General Information

Headquarters

Daisy/Cadnetix Corporation
700 Middlefield Road
Mountain View, CA 94039-7006

CEO of Sales, Corporate Development, Financial, and Customer Support : Norman Friedman, formerly Daisy CEO

COO of Product Marketing, Software and Hardware Development, and Manufacturing : Bruce Holland, formerly Cadnetix CEO and president

Number of Employees

Total Employees for Daisy/Cadnetix: approximately 1500, worldwide

***Daisy:**	Sales and Support:	220	***Cadnetix:**	Sales and Admin.:	340
	Marketing:	100		Marketing:	30
	R & D:	240		R & D:	170
	Manufacturing:	100		Manufacturing:	23

*Approximate figures before merger.

Daisy is the world's number-one supplier of specialized simulation accelerators with more units sold than all other companies combined. Daisy has a world-wide customer base covering a wide range of industries including military/aerospace, computers, semiconductors, telecommunications, and consumer electronics. Cadnetix, on the other hand, has been spending money and resources trying to penetrate the European and Far Eastern markets. With the merger, each will help the other influence their collective markets positively.

Tables 1 and 2 show the regional segmentations of Daisy and Cadnetix installed base in units shipped. The total shipped to date figures are cumulative, while the other figures represent the number shipped in that year. The table also lists figures for systems shipped each year. The last column of each table presents compounded annual growth rate (CAGR) in regional segmentations of their markets. N/A represents not applicable.

Table 1: Regional Segmentations of Daisy's Installed Base

	1983	1984	1985	1986	1987	CAGR 83-87
World-wide Workstations	407	1429	2001	1400	831	20%
North America	297	1020	1423	630	316	2%
Europe	66	260	402	630	292	45%
Far East	44	149	176	140	210	48%
Rest of World	0	0	0	0	14	n/a
Total Shipped to date	476	1905	3580	4980	5258	82%
CAE Systems	407	1244	1691	1167	694	14%
PCB Systems	n/a	n/a	n/a	143	77	n/a
IC Systems	n/a	185	309	90	61	n/a

Source: Dataquest, July 1988

Table 2: Regional Segmentations of Cadnetix's Installed Base

	1983	1984	1985	1986	1987	CAGR 83-87
World-wide Workstations	n/a	n/a	300	616	990	n/a
North America	n/a	n/a	278	576	673	n/a
Europe	n/a	n/a	0	0	257	n/a
Far East	n/a	n/a	22	40	59	n/a
Rest of World	n/a	n/a	0	0	0	n/a
Total Shipped to date	n/a	n/a	300	916	1844	n/a
CAE Systems	n/a	n/a	104	224	345	n/a
PCB Systems	n/a	n/a	196	392	644	n/a
IC Systems	n/a	n/a	0	0	0	n/a

Source: Dataquest, July 1988

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Daisy/Cadnetix Target Markets

Industry analysts say that the technologies of the two merged companies will complement each other. Both companies supply products for computer-aided engineering and design of electronic circuits.

- **CAE** - computer-aided engineering
- **CAD** - computer-aided design
- **CAM** - computer-aided manufacturing
- **PCB** - printed circuit board layout
- **CAT** - computer-aided test

Daisy and Cadnetix Technology Partners

Daisy previously had a "make-rather-than-buy" corporate culture so there were relatively few third-party relationships of any kind. With Daisy's move to standard platforms, this policy changed. Daisy now believes in working with carefully selected strategic partners to tightly integrate third-party products into the product line. Cadnetix on the other hand, has always used third-party relationships to supplement their products. Daisy/Cadnetix sites this as a focus and believes that working with third-parties will allow the new company to focus its internal R&D resources on core technologies while bringing customers the broadest solutions possible. Among the areas currently served by products from third parties are logic synthesis, thermal analysis, and technical publishing.

Daisy

Current Daisy third-party agreements are:

- **Silicon Compilers, Inc.**— joint development agreement to develop a new design methodology incorporating Daisy's EDA tools and Silicon Compiler's compilation technology for VLSI design.
- ECAD **Inc.**-- licenses the DRACULA IC verification product. (ECAD Inc. is now a part of Cadence.)
- **Logic Automation**— agreed to make their SmartModel behavioral models available for use with the Daisy simulators.
- **Frame** -- technical publishing system
- **Pacific Numerix** — thermal analysis package

Cadnetix

Third-party agreements prior to being acquired by Daisy were:

- **Cimlinc (Cadlinc)** — mechanical data can be exchanged between Cadnetix and Cadlinc systems. Also, an informal relationship to assist in joint sales. No joint marketing activities.
- **Interleaf** — joint marketing agreement to allow joint sales activities for documentation package.
- **Helios** — thermal analysis package
- **Pacific Numerix** — thermal analysis package
- **NEC** — ASIC supplier of CMOS 4/4A 1.5 Micron Series, CMOS 5/5A 1.2 Micron Series
- **NCR** — Standard-cell ASIC supplier
- **Matra Harris** — ASIC supplier
- **VLSI** — ASIC supplier
- **Zycad** — CATS accelerator units for HHB
- **Cadence** — Simucad has an OEM relationship where it supplies Cadence and XYL with simulation software.
- **Silvar-Lisco** — HHB purchased schematic capture software. Assume agreement to have lapsed now that Cadnetix purchased HHB.
- **Analogy** — Saber analog simulator

Cadnetix Technology Partners, cont'd

- **LSI Logic Corporation** — agreement to develop and distribute LSI Logic's semicustom IC design creation and verification tools on Cadnetix workstations. The tools will be fully integrated with Cadnetix's product line taking advantage of their user interface.
- **Minc, Inc.** *— OEM license for PLD design tools, sold on an OEM basis on the PC-AT and SUN platforms.
- **Sun Microsystems, Inc.** — a licensing agreement for Sun's Network File System (NFS) protocols for IBM PCs and compatibles. This contract is a follow-on to an earlier agreement between the two companies that allowed implementation of NFS on Cadnetix's workstations and special-purpose computers.

* Since Daisy has their own PLD product (PLD Master) this 3rd-party relationship could go away.

Financial and Market Share Information

Financials

Daisy

Daisy's software tools for the design of custom integrated circuits met with early success, with revenues booming from $4.6 million in 1982, to more than $122 million in 1985. But by the mid 1980's, Daisy had fallen behind in technology and sales leveled off at $100 million. Last year Daisy suffered a loss of more than $16 million. Daisy knew it was time to expand the product line in order to catch up with the competition. Despite the problems in fiscal 1986 and 1987, Daisy has kept R&D spending high. However, a very high proportion of that has been spent on porting software rather than adding functionality.

Cadnetix

Cadnetix has enjoyed average annual growth of more than 40% and has been consistently profitable. Their income has only been exceeded by Mentor. Cadnetix started to experience the typical problems of a maturing company during 1987 and 1988 and attempted to restructure themselves to achieve continued profitable growth. In the last quarter before merging with Daisy System Corp., Cadnetix recorded a net loss of over $19 million. This was due to the acquisition costs and decreased sales of its recently-acquired subsidiary HHB Systems.

Daisy/Cadnetix

The Daisy/Cadnetix merger has created the second-largest CAD firm offering system-level design tools with sales expected to reach $200 million this year. The Cadnetix takeover is expected to add $80 million in sales this year to Daisy's current $120 million in sales. The merger will also generate many immediate cross-selling opportunities within the customer base of the two firms. Daisy/Cadnetix reported a net loss of $66 million for the first quarter ended Dec. 31, 1988 as a result of numerous special charges and adjustments related to the acquisition of 50.1 percent of Cadnetix Corp. stock. The second phase of the merger of Daisy and Cadnetix will entail the acquisition of the remaining 49.9% of the outstanding shares of Cadnetix. Daisy/Cadnetix expects to continue to report increasing profits from operations. Daisy/Cadnetix cash flow from the combined enterprise will be adequate to service acquisition financing and fund future growth. Analysts predict however, that interest and goodwill write-offs could wipe out profits for the merged company for years to come.

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Tables 3 and 4 show the regional segmentations of revenue for Daisy and Cadnetix between 1983 and 1987. The figures in the tables represent millions of dollars per year.

Table 3: Regional Segmentations of Daisy's Revenue

Daisy	1983	1984	1985	1986	1987	CAGR 83-87
Total Revenues	28.4	81.5	134.0	96.6	103.5	38%
North America	21.3	56.0	92.8	43.5	39.0	16%
Europe	4.1	12.8	27.8	43.5	37.9	75%
Far East	3.0	12.8	13.4	9.7	24.9	69%
Rest of World	0	0	0	0	1.8	n/a

Source: Dataquest, July 1988

Table 4: Regional Segmentations of Cadnetix's Revenue

Cadnetix	1983	1984	1985	1986	1987	CAGR 83-87
Total Revenues	n/a	n/a	23.1	34.7	53.9	n/a
North America	n/a	n/a	21.3	32.4	36.6	n/a
Europe	n/a	n/a	0	0	14.0	n/a
Far East	n/a	n/a	1.9	2.3	3.2	n/a
Rest of World	n/a	n/a	0	0	0	n/a

Source: Dataquest, July 1988

Market Share

Daisy perceives itself as the market leader in hardware accelerators and physical modelers and is now the second largest supplier of board-level CAE tools, including front end design/simulation and PCB layout products, with a 12% share of the front end and a 3% share of the back end market.

In 1987, Cadnetix was the fourth largest supplier of PCB CAD tools. Cadnetix believed the keys to its successful marketing strategy in a market shifting to integrated systems were networking,shared databases, manufacturing interfaces, a consistent user interface across applications, and low-cost access to high-performance computing resources.

With the merger, Daisy/Cadnetix remains the second largest supplier behind Mentor. In comparison, among vendors of EDA software, HP places fifth.

Figure 3 compares the total revenues of the combined markets of technical workstation platforms of CAE, PCB, and IC. Daisy/Cadnetix is the second largest provider of board-level tools for the CAE, PCB and IC markets as compared to HP's fifth place 5.3% share. When broken down into separate markets, Daisy/Cadnetix maintains second place in the separate markets, as shown in **Figures 4, 5,** and **6.** But in the IC market, while maintaining second place, Daisy/Cadnetix demonstrates a markedly lower percentage than Mentor's first place position, as does HP. Daisy recently announced that after the merger, IC development will be through third parties only. They will continue to support ChipMaster but will look to third parties for future products for IC design.

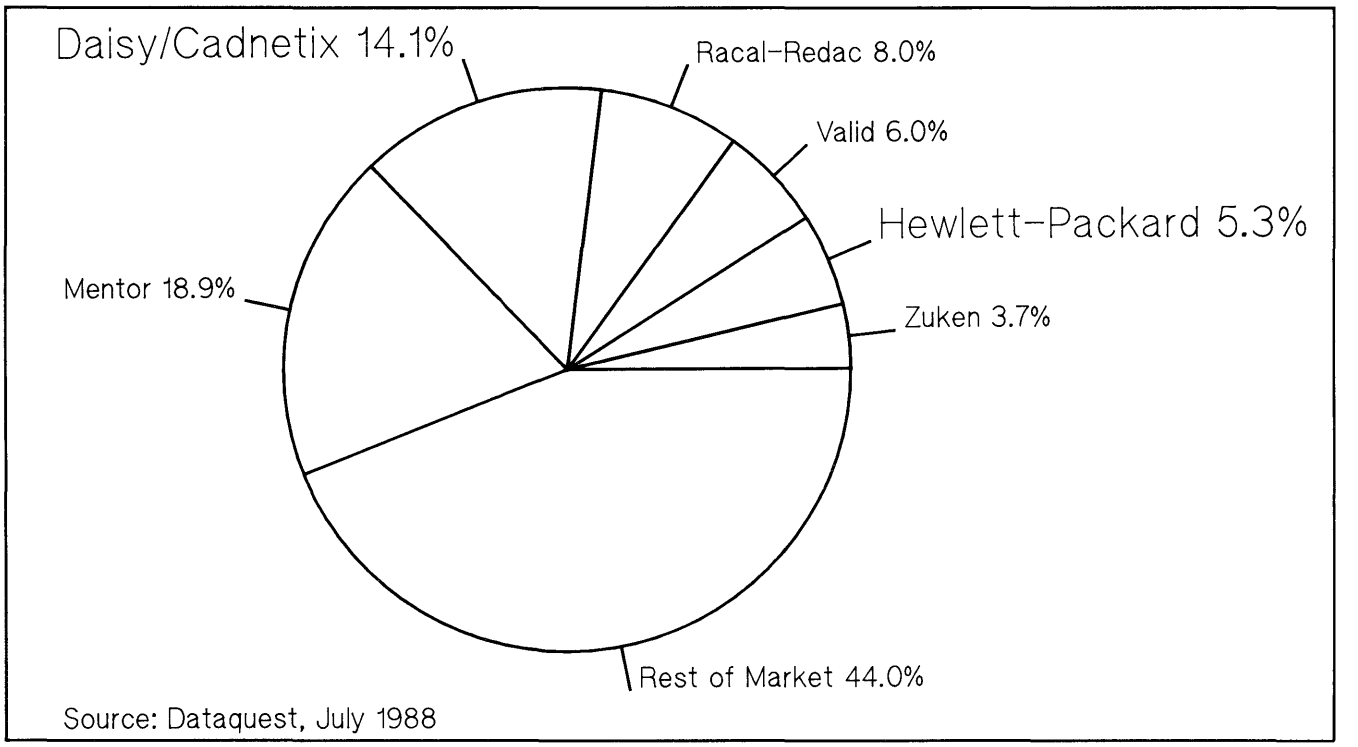

Figure 3: Market Share 1987, Total CAE, PCB, IC Markets

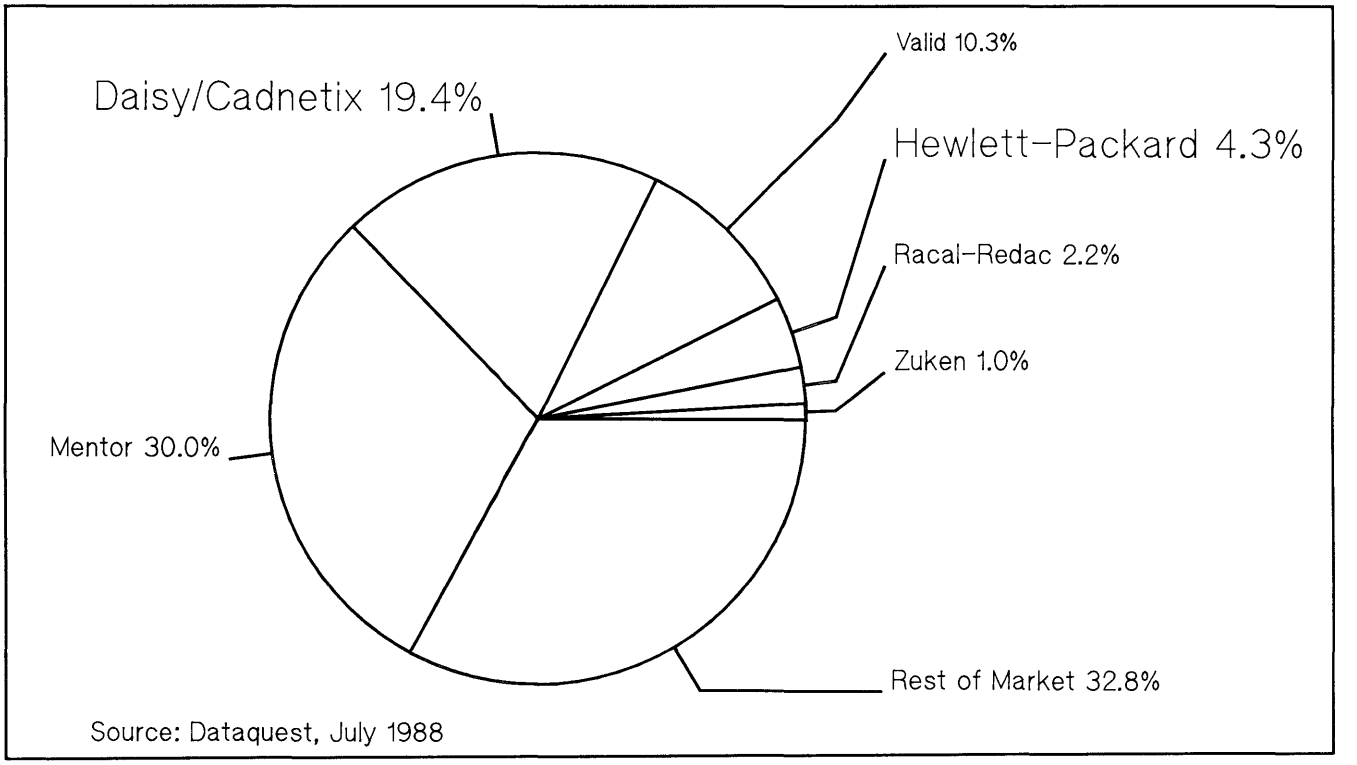

Figure 4: Market Share 1987, CAE Market

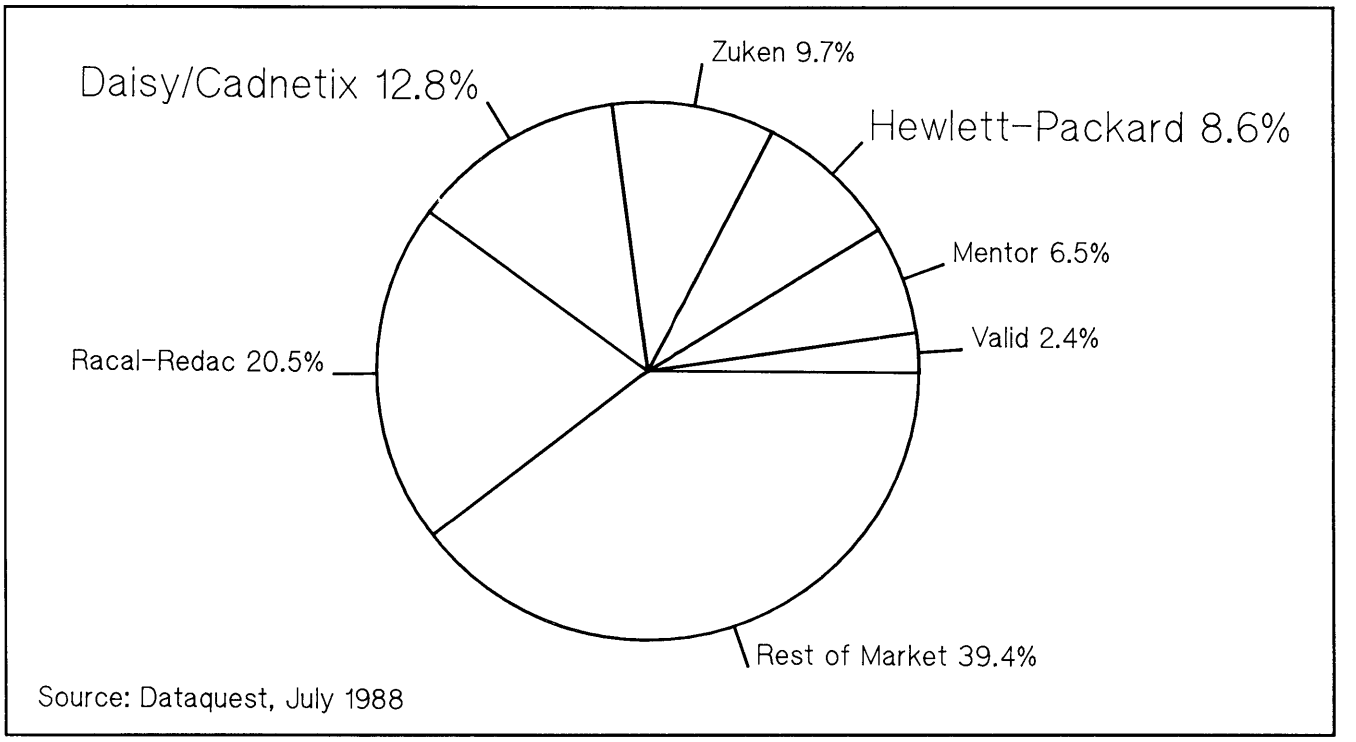

Figure 5: Market Share 1987, PCB Market

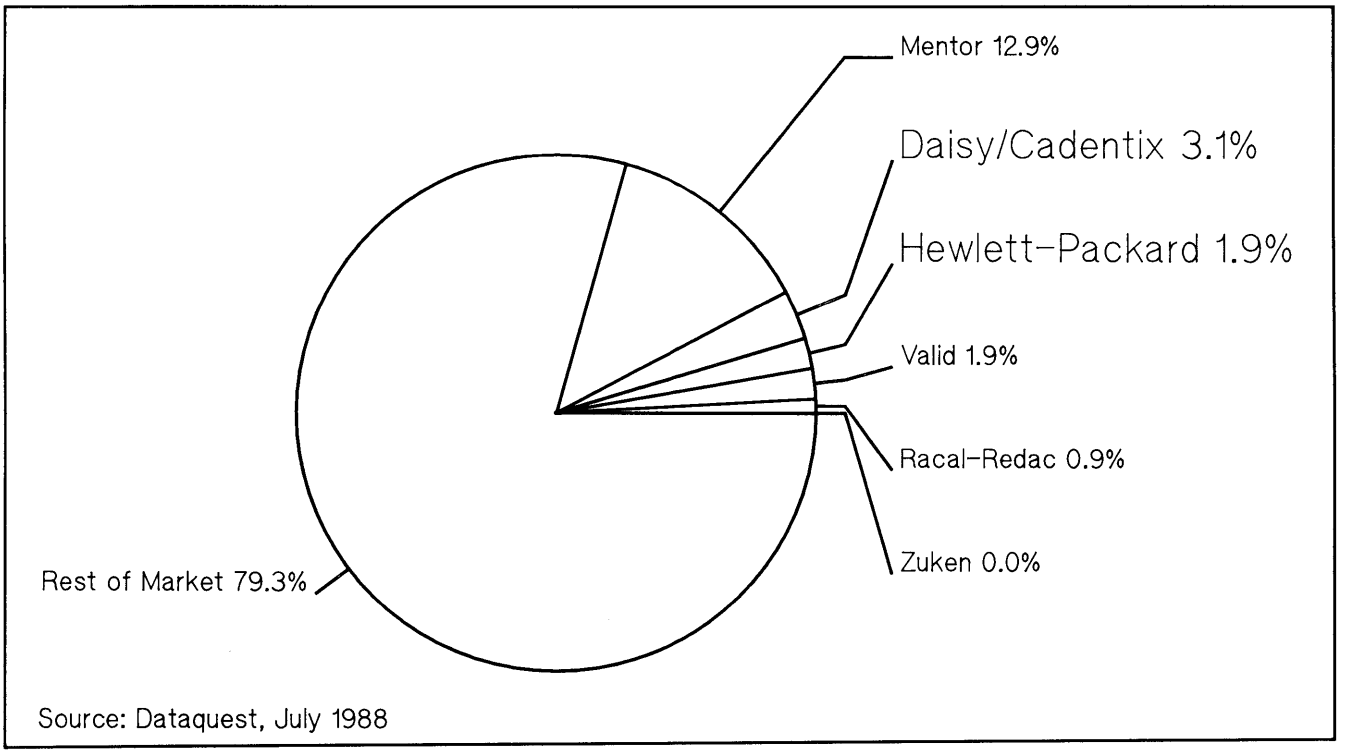

Figure 6: Market Share 1987, IC Market

Product Family

Platforms

Daisy's product offering includes several hardware platforms for its CAE/CAD/CAM applications.

Daisy Platforms:

- Sun 386i with Intel 80386 processor and Sun-4 servers
- Logician 386 with Intel 80386 microprocessor with SUNOS operating system
- MegaLogician simulation accelerator
- GigaLogician
- IBM PC/AT or compatible

Daisy Software

Daisy application software covers both ASIC and PCB CAE/CAD/CAM.

Daisy offers the following software:

- **Advansys** -- schematics and simulation for Sun 386i
- **Logician 386** — schematics and netlisting
- **Personal Logician 386** — schematics and netlisting for IBM/PC or compatible
- **ACE** — advanced drawing editor
- **Entry !**— allows schematic capture, modeling, netlisting and text editing
- **Daisy Logic Simulator (DLS)** — digital simulation
- **Mega Daisy Logic Simulator** — digital simulation
- **Daisy Timing Verifier** — logic simulation
- **A/D Lab** — mixed analog and digital simulation
- **DSPICE/Virtual Lab** — analog simulation
- **PLD Master** — PLD simulation
- **Pattern** — allows graphics based editing of IC layout
- **Editor** — text editor
- **Daisy Libraries** — set of component libraries containing both graphic representations of common components as well as functional and timing models used for computer simulation of electronic designs
- **Deepboard** — logic simulator
- **BoardMaster** — PCB design and layout package
- **STAR Router** — PCB CAD for auto routing of PCBs
- **Mechanical Documentation Program (MDP)** — two dimensional mechanical drafting package that is closely integrated with BoardMaster for creating final PCB documentation
- **GateMaster** — gate array layout
- **ChipMaster** — custom layout
- **MegaFAULT** — fault simulator

Cadnetix Platforms

Cadnetix sells bundled systems using the Sun 3/60 or 3/50 hardware. For CAD/CAM applications they have a graphics accelerator mounted on a Sun 3/110 chassis using a Sun 3/60 card set. The Sun 4 is available for CAE database applications, but not yet for CAD applications. Cadnetix still sells their own workstations but sales of proprietary workstations have dropped to less than 20% of their workstation sales.

- **CDX 7600** — Sun 3/60, screenless server
- **CDX 75000XP** — route engine
- **CDX 70000S*** — basic configurable analysis engine

* This was Cadnetix's attempt at building a proprietary simulation accelerator. This will be discontinued with the merger because Daisy and HHB both have their own simulation accelerators.

Cadnetix Software

- CDX 3000 — PC system software and network card
- CDX 3150 — PC digital waveform editor
- CDX 3200 — PC analog design grapher
- CDX 9500 — (Sun 3/50) schematic editor
- CDX 9510 — (Sun 3/50) schematic editor and digital simulation
- CDX 9600 — (Sun 3/60) schematic editor
- CDX 9610 — (Sun 3/60) schematic editor and digital simulation
- CDX 9630 — (Sun 3/50) schematic editor and analog simulation

Cadnetix Software bundled with Hardware

- **CDX 5000 S**— (CDX workstation) PCB design
- **CDX 50000 S** — (CDX workstation) PCB design plus graphics accelerator
- **CDX 5600** — (Sun 3/60) PCB design
- **CDX 56000 SP** — (Sun 3/60) PCB design plus graphics accelerator
- **CDX 56010 SP** — (Sun 3/60) PCB design with graphics accelerator plus digital simulation
- **CDX 66000 SP** — (Sun 3/60) graphics accelerator, CAM
- **CDX 66500 SP** — (Sun 3/60) graphics accelerator, CAM and CAD

For a complete listing of Daisy, Cadnetix, and HP product coverages, see Appendix B.

Daisy/Cadnetix Platforms and Software

Daisy/Cadnetix's integration strategy is straightforward. It begins with the selection of a primary hardware platform. As the two product lines come together, Daisy/Cadnetix will focus on UNIX-based Sun and Sun-compatible workstations. Longer term, the company will maintain a primary focus on UNIX® systems rather than on a specific hardware platform.

The following lists the products that Daisy/Cadnetix have acknowledged will probably be kept and supported in the future.

Daisy:

- **ASIC's** — tools for every step of the ASIC design process
- **MegaLogician**— first hardware accelerator
- **GigaLogician**- accelerator for large electronic system designs
- **Libraries** — extensive set of component libraries for simulation, consisting of more than 4,500 components
- **Physical Modeling Extension (PMX)** — popular physical modeler
- **Analog system design and simulation systems and Daisy's system** — enabling designers to analyze mixed digital and analog circuit designs.

Cadnetix:

- **User Interface**-- easy-to-use and same across all product lines
- **CADAT** — industry-standard, board-level fault simulation system from HHB. Will be combined with Daisy's DLS (digital logic simulator) and will incorporate the best features of CADAT
- **Analog simulation**— PACSIM, high-performance circuit simulation tool
- **PCB Layout**
  - — autorouting
  - — Route Engine, speeds up the board layout process as well as ensuring a high-performance rip-up and reroute capability
  - — Surface Mount technology on either side of the PCB
  - — INTELLIGEN, automatic test pattern generation (ATPG) system for nearly 100% fault coverage of complex sequential ASIC designs.
- **CAM Workstation**— first intelligent, integrated computer-aided workstation

UNIX® is a registered trademark of AT&T in the U.S. and other countries.

Pricing Comparison

Figure 7 compares pricing on Daisy's and HP's physical design systems for single seats. Daisy only runs on a the Sun 386i PC platform, whereas HP does not offer a PC platform.

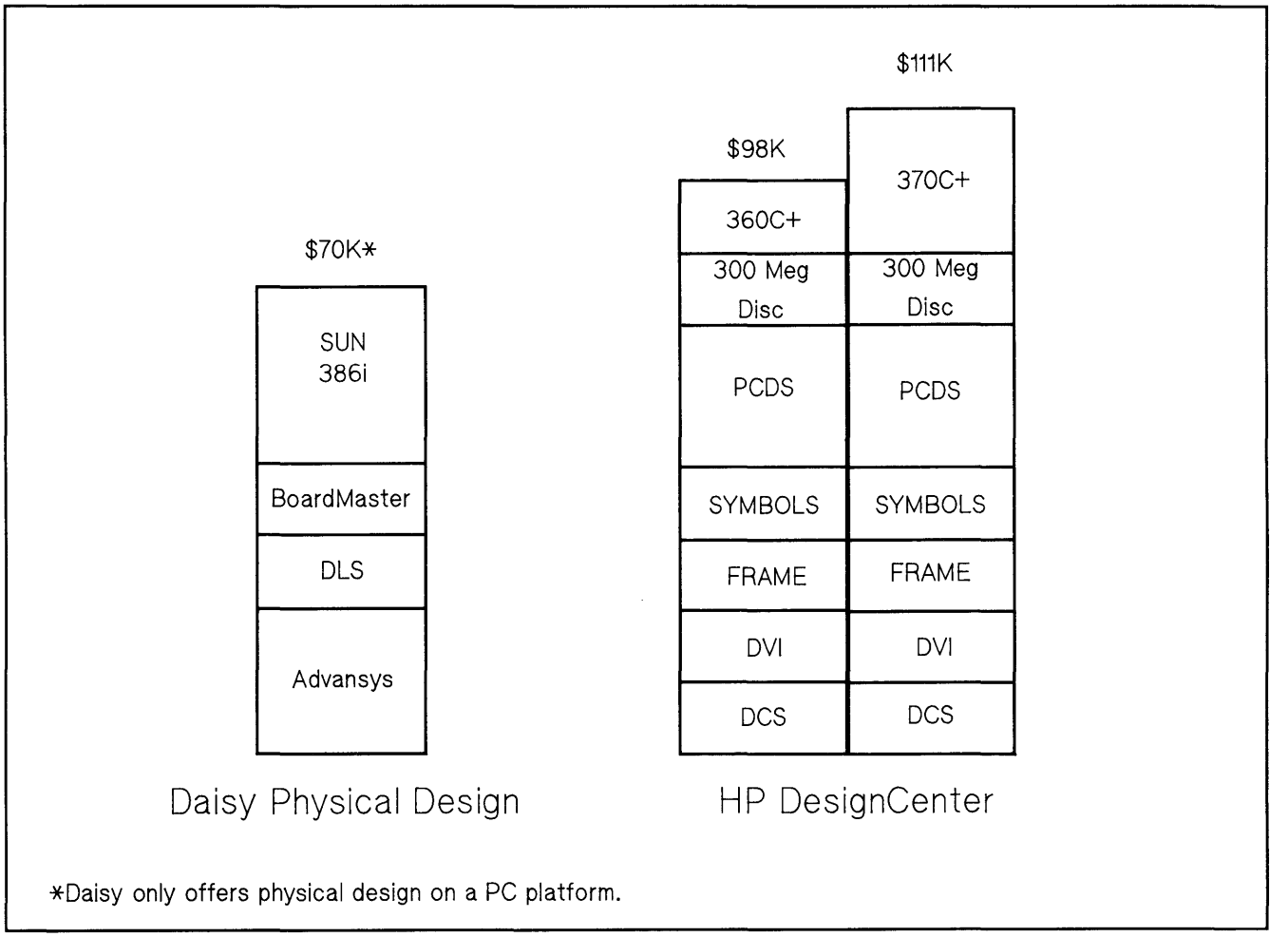

Figure 7: Pricing Comparison, Physical Design Systems, Single Seat

Figure 7A compares pricing on Cadnetix's and HP's physical design systems for single seats. HP is competitive in pricing with Cadnetix systems.

For a listing of Daisy and Cadnetix individual product prices, see Appendix A.

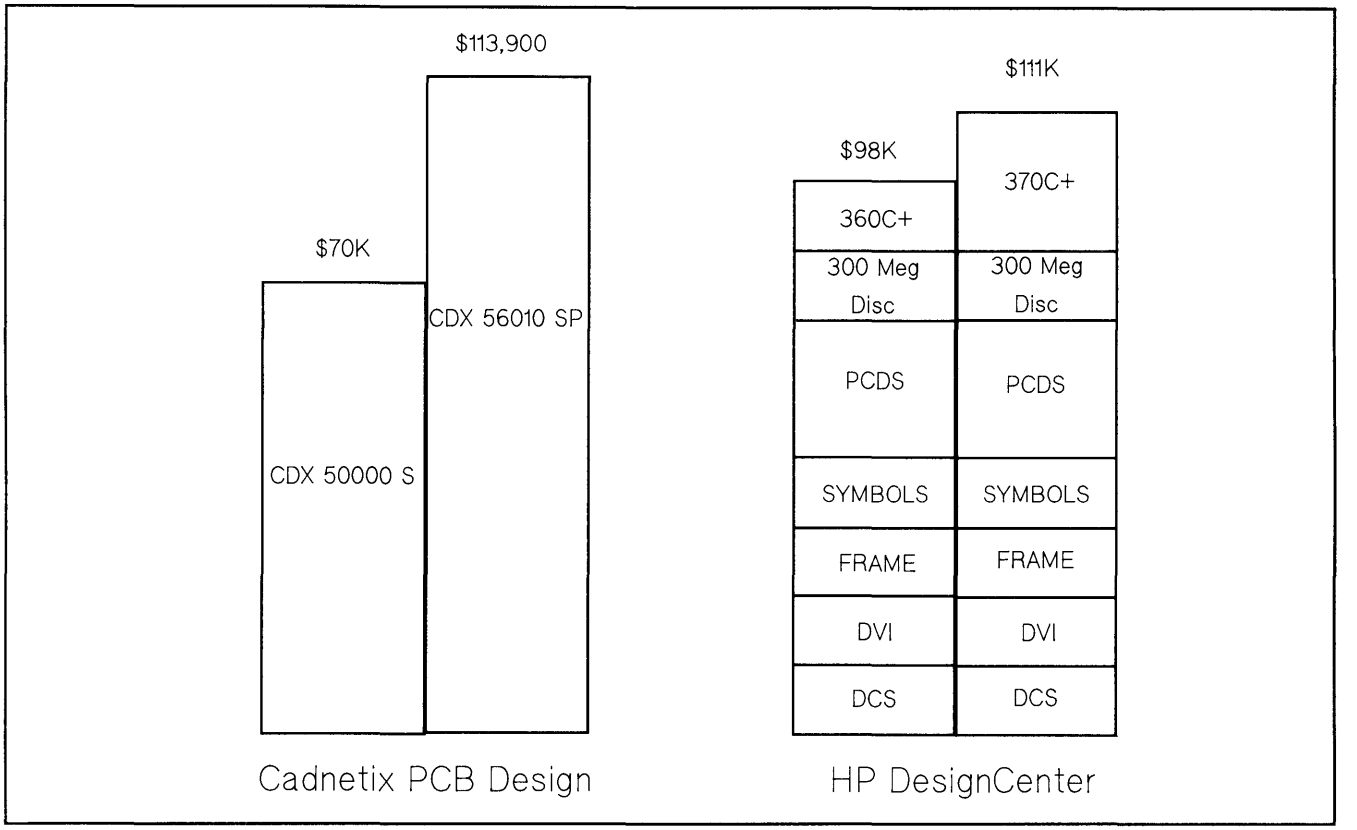

Figure 7A: Pricing Comparison, Physical Design Systems, Single Seat

Service and Support

Daisy obtains 80-85% of their revenue from their existing customer base in upgrades and additional workstation sales. The company's sales and marketing structure reflects that trend. About 33% of Daisy's employees are employed in sales and support roles. There is a direct sales force world-wide with one applications engineer per salesperson. The applications engineers are responsible both for pre- and post-sales activities. They are supported by product specialists in each region and in the head office. International sales are mainly managed via subsidiaries.

In 1988, there was a strengthening of Daisy's sales efforts due to the introduction of standard platforms and a solidifying of the company's sales organizations. For example, Dennis Sabo was newly appointed as vice president of Daisy's North American sales. Under his direction, both the quality and size of the organization has been enhanced.

Service and Support, cont'd

Cadnetix has a direct sales force with twenty-one sales offices in the U.S. and twelve other sales outlets world-wide covering Canada, Europe, and the Far East. The company has wholly-owned subsidiaries in the U.K., the Federal Republic of Germany, Belgium and France. The Southwest Cadnetix Users Group offers a 24-hour bulletin board service for U.S. users nationwide. This service is sponsored by Integrated Technology Corporation, Tempe, AZ, a modem supplier.

Daisy/Cadnetix claims they have a combined worldwide sales staff representing one of the largest and most experienced sales forces in the EDA industry. With the merger recently accomplished, the field organization began cross training conferences. Because of this, Daisy/Cadnetix sales and support personnel have been unreachable to their customers. Another reason adding to the installed-base uneasiness.

Daisy/Cadnetix installed base has good reason to be uneasy. The corporate culture clash that many analysts identified is most evident in the area of sales and support. Cadnetix sales and support personnel had a close, open relationship with Cadnetix upper management. Whereas, Daisy maintained a more reserved policy for sales and support staff, preferring to keep company goals and information to upper management only. The clash is evident because Daisy personnel are now the directors of the sales and support division. Already to date, many Cadnetix sales and support engineers have left the company and more are predicted to leave. The Cadnetix installed-base must be feeling uninformed and very leery of what the future might bring.

Daisy/Cadnetix Future Products and Markets

Daisy/Cadnetix believes it has created one of the strongest offerings of system-level design tools in the industry, and generated many immediate cross-selling opportunities within its shared customer bases. With the merger, Daisy/Cadnetix's marketing goals revolve around its penetration into the CAD/CAE PCB market segment. Daisy believes the acquisition of Cadnetix will accelerate Daisy/Cadnetix's rise to a leadership position in PCB CAD. Furthermore, Daisy believes Cadnetix's strength in turnkey CAD systems for PCB layout fits nicely with their strength in ASIC design and system simulation.

Part of the reason there is not a clear-cut marketing strategy for the newly merged company is because of the hostile nature of the merger. Daisy was hoping to sit down with Cadnetix before the merger was complete and gain their participation in putting together a meaningful product integration plan and a market positioning strategy. Cadnetix refused and Daisy was not able to release any information on what the merger would mean to its organization or product line until the merger had actually taken place.

The future of Daisy and Cadnetix products has an aura of surrounding confusion. Even now it is not clear where they are headed or what products will be kept and dropped. Daisy/Cadnetix insists that the integration strategy is straightforward. It begins with the selection of a primary hardware platform. As the two product lines come together, Daisy/Cadnetix will focus on UNIX-based Sun and Sun-compatible workstations. Longer term, the company will maintain a primary focus on UNIX systems rather than on a specific hardware platform. Daisy/Cadnetix also states that existing products will be supported and enhanced for the next two years. After that, new products will be offered. Customers on software support will get the revisions/conversions free of charge.

HP Internal Use Only

Daisy/Cadnetix Future Products and Markets, cont'd

Daisy/Cadnetix has announced some immediate integration and product plans. Integration for front ends, with CED (Cadnetix front end) being able to pass information through a one-way EDIF link to ACE (Daisy's schematic capture system), is planned. Also promised is the upward transfer of the libraries for simulation systems; and a new digital simulation environment based on Daisy's DLS (Digital Logic Simulator), and incorporating the best features of CADAT, an industry-standard, board-level fault simulation system from HHB. It is fairly assured that Cadnetix's front end will disappear. The danger if the front end goes away is loss of Cadnetix's smooth integration from one application to another. Daisy/Cadnetix will continue with the present PCB systems for the next two years when a new product, tentatively named "CadMaster," will be made available. Before two years passes, the Daisy BoardMaster system will have a revision that includes high frequency and hybrid support. Daisy also promised that enhancements to existing Daisy and Cadnetix products will be released in the near future. Enhancements promised this year include electrical rule checking (ERC) on Daisy, the GigaLogician hardware modeler, and Intellegen from HHB. The migration of ACE to UNIX and DOS systems was also promised.

To counter recent analog design products from Mentor Graphics and Valid Logic systems, Daisy has formed an analog division and shifted its analog product lines to the Palo Alto site under Mr. Burrow, the former president of Simucad. Currently, Daisy has Spice, Cadnetix has SABER, and Simucad has PACSIM. It is not known which of these products will be kept.

All future products offered by Daisy/Cadnetix will feature the Cadnetix user interface for ease of use and consistency and providing a strong foundation for the ultimate integration of a complete CAE/CAD/CAM tool suite. To complete the tool suite, the company is first building a core set of tools by merging the many product offerings of both companies—a process that is well underway, according to Daisy management. In cases where both Daisy and Cadnetix offer tools for the same function, the next version of that tool will combine the best features of both and provide a safe migration path for data residing in earlier versions of each tool. Throughout this process, Daisy/Cadnetix will continue to support all existing products and will work closely with customers to upgrade from existing products quickly and cost-effectively.

One merger benefit; together the companies have the largest R&D staff and the largest R&D investment focused exclusively on EDA for system designers in the industry. This means that even during a period in which considerable engineering resources will be focused on integrating the two product lines, the company will have the R&D capacity to move ahead with key advanced technology development projects more rapidly than either company could have done on its own.

Daisy/Cadnetix Sales Pitches

Through all the press releases and announcements concerning the goals of the newly merged company, one statement repeatedly stands out: "the combination of Daisy and Cadnetix will provide one of the largest offerings of system-level design tools in the industry." Rest assured that Daisy/Cadnetix will use this statement as one of the focal points in their new sales strategy. Daisy believes combining Daisy and Cadnetix products into one CAE/CAD/CAM product line with a consistent user interface, they will be well positioned to offer system designers a comprehensive solution to their entire system design process.

Before the merger, one of Daisy's strongest selling points was ASIC support. Daisy was the first CAEE company to make a point of supporting ASIC users with special products. Daisy claims they were the dominant system chosen by ASIC users who wish to communicate with the ASIC foundry.

Cadnetix's strong sales pitches were the ease of use of their systems (one common user interface) and integrated database, (schematic, to board layout, to CAM.) Cadnetix also successfully focused its sales and marketing efforts on the smaller accounts that larger companies, such as Mentor and Daisy, were ignoring. With the merger, Cadnetix's sales focus on smaller accounts will complement Daisy'ssales concentration on the larger accounts.

With the merger, these separate points will still be strong selling tools for Daisy/Cadnetix. But the time delay until the integrated product line takes over is in their competitors favor. Daisy's software is sophisticated in nature, preferring many steps whereas Cadnetix's software stresses ease of use, simplicity almost for simplicity's sake. Daisy's software will have to be fit under Cadnetix's common user interface. This will not be accomplished easily or quickly.

Right now Daisy and Cadnetix customers are very leery of what the future will bring. This is the time when HP should be stressing their integrated product line and HP's support costs, among the lowest in the industry. But this advantage period for the competition will only last until Daisy/Cadnetix prove that the integration is successfully working, two years at the most. And when Daisy/Cadnetix returns and their goals are met, they will have one of the strongest offerings in system-level design tools in the industry. Now is the time for their competitors to strike, while the customer base is leery, and the product line in disarray.

Technology Analysis

Introduction

This section contains technical comparisons of Daisy Systems CAD/CAM business including the recent acquisition of Cadnetix, and HP/EDD applications for standard logic design, design verification, PLD design and verification, documentation, and PCB layout. It is also a presentation of the strengths and weaknesses of Daisy, Cadnetix, and HP/EDD products. Only the products with the highest probability of being kept by the newly merged company are presented.

Spider diagrams are used for comparing the technical applications. Each application is divided by product component or parameters. The parameters establish the axis of the spider diagrams. In some cases, such as standard logic design entry design verification, and board layout, there are several subcategories or attributes for each axis.

For each axis a whole number between 1 and 10 is used by HP field and factory support engineers. The larger the number, the "better" the performance of the application for that measurement axis. A value of 10 indicates the best, or state of the art, for current products on the market. A value of 1 indicates no capability, while a 5 is considered average. Unknown information is left blank and not included in the calculations. The subcategories are averaged and rounded to the nearest integer for plotting on the axis.

Schematic capture and simulation for Daisy were studied at a service bureau in the U.S. on a Daisy proprietary PL-286 Workstation. Revision 1.5 of ACE, Daisy's schematic editor and version 5.02 of Daisy's Logic Simulator were evaluated. The hardware contained 4 Megabytes of RAM with an 80 Megabyte disk, and 4 Megabytes of Swap. Libraries were contained on a networked 400 Megabyte Eagle disk.

Schematic capture and board layout for Cadnetix were evaluated on a basic Cadnetix model CDX 5000 S. The software used for the Cadnetix comparisons was rev D4.0F.

Cadnetix

Figure 8 is a flow chart depicting the Cadnetix CAE/CAD system. Cadnetix built its original reputation on its ability to offer high-performance PCB CAD facilities. This was greatly influenced by the route engines that the company developed.

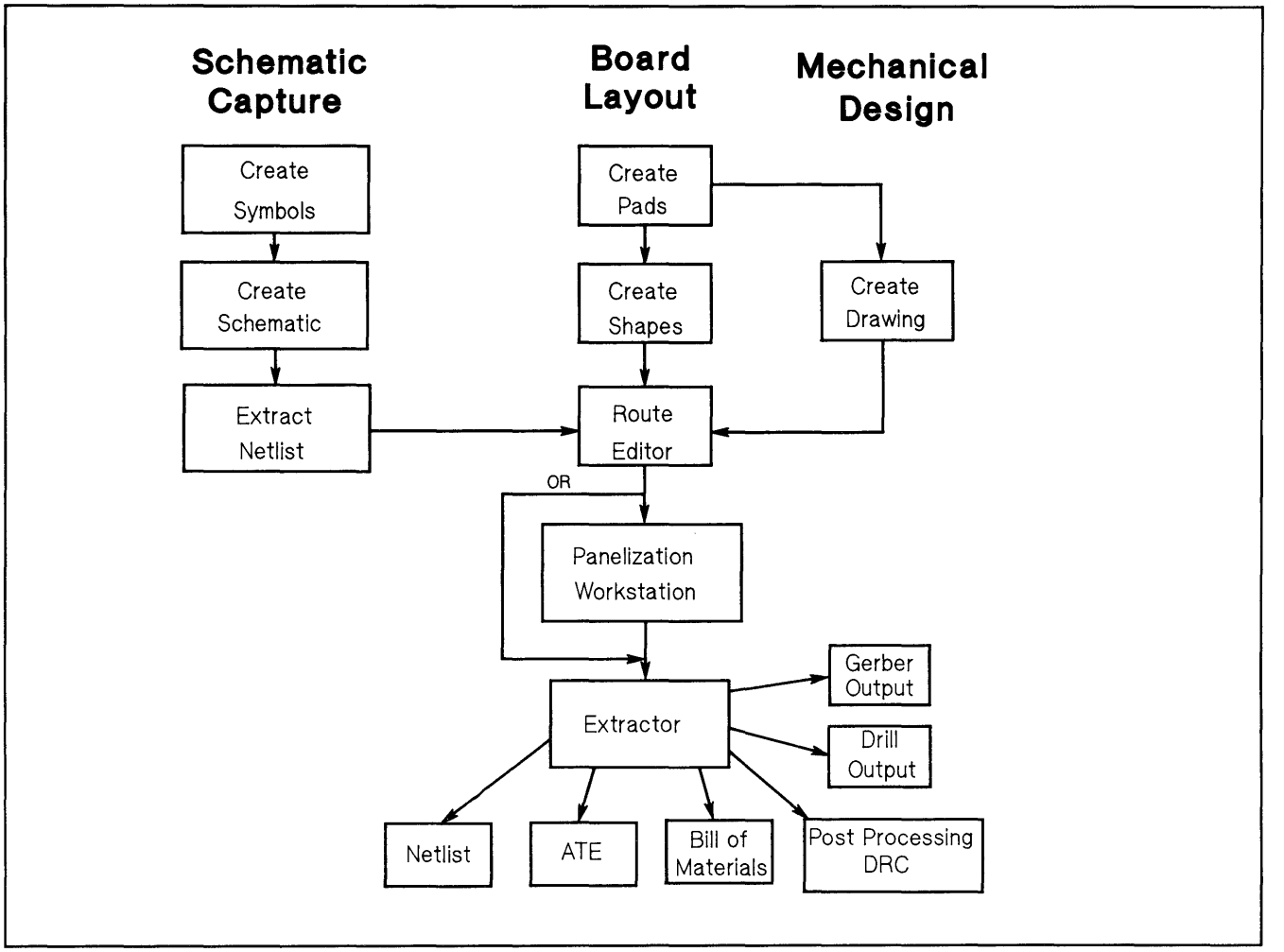

Figure 8: Flow Chart of Cadnetix CAE/CAD System

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Standard Logic Design Entry

Figure 9 is a comparison of Daisy's and HP's design process as it applies to design capture. Daisy differs from HP in that it requires its users to run various design file compilers at each step of the process. The difference with Daisy's system becomes immediately apparent when the user exits the circuit editing environment and moves into simulation. Each time a change is made to the schematic, four separate compilers must massage the design file data before it is ready for simulation. The strengths of Daisy Logician and HP EDS design processes are listed in the Design Verification section.

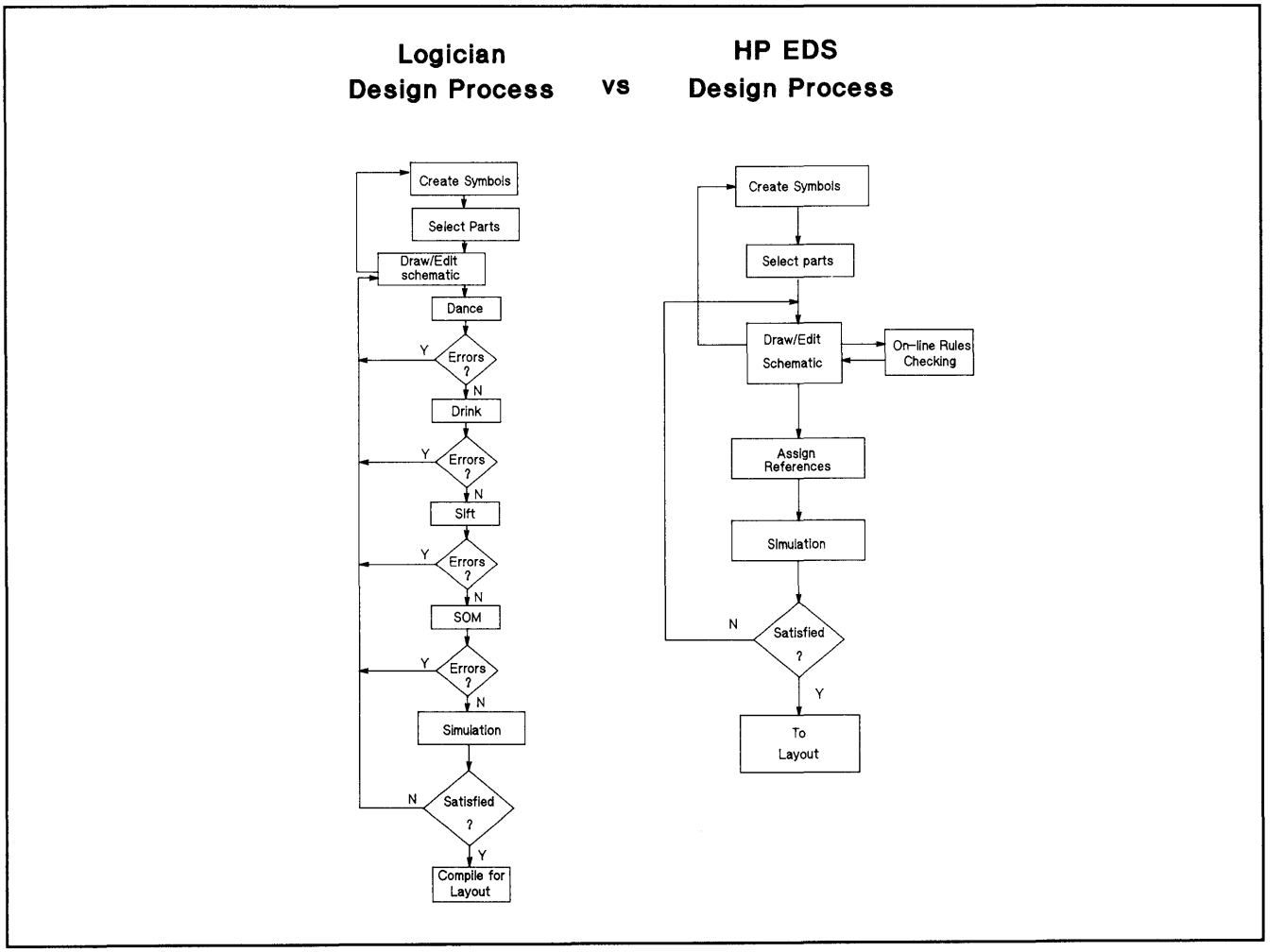

Figure 9: Daisy Logician Design Process vs HP EDS Design Process

Figure 10 is a comparison of Cadnetix's and HP's design process. Cadnetix has to perform an association step in order to extend the Netlist while HP EDS does not have to perform this step. HP EDS also uses an object-oriented data structure and has built-in simulation.

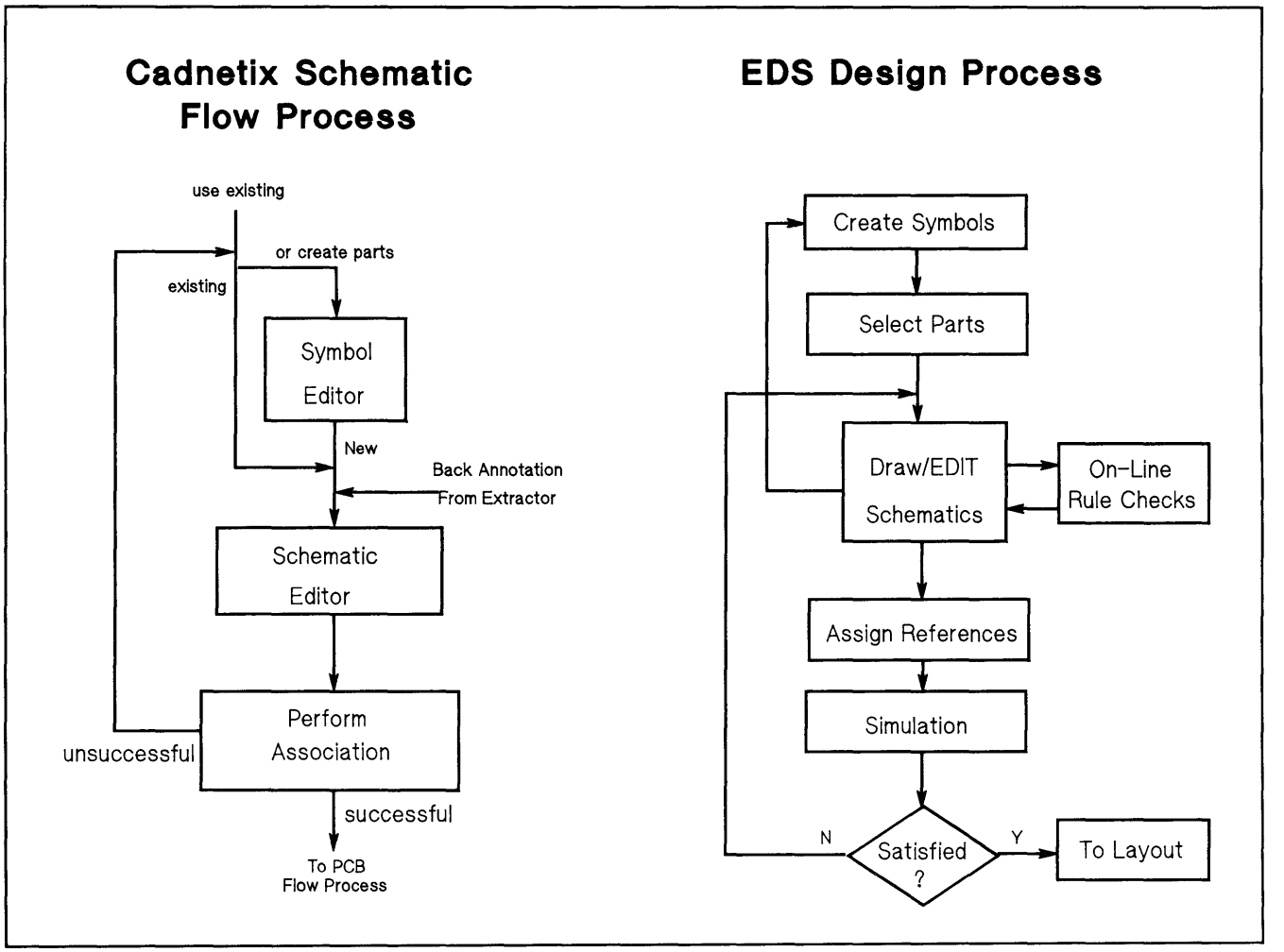

Figure 10: Cadnetix and HP EDS Design Processes

Figures 11 and 12 are spider diagrams comparing the standard logic design entry systems of Daisy and Cadnetix with HP. The parameters and their attributes chosen are:

- **User Interface**
  - —flexible command entry
  - —operating system access
  - —windowing
  - —customizability
  - —commonality
- **Libraries**
  - —coverage
  - —completeness
  - —creation
  - —standards
- **Editor**
  - —graphics performance
  - —speed of design entry
  - —part selection
  - —design rule checking
  - —flat design
  - —hierarchical design
- **Capacity**
  - —IC design
  - —PCB design
- **Data Access**
  - —industry standard database
  - —access language
  - —design file access
- **Technology**
  - —PCB
  - —IC
- **Links**
  - —EDIF
  - —IGES
  - —test
  - —simulation
  - —layout
  - —documentation
- **General**
  - —learning tools
  - —revision control
  - —quality
  - —engineering changes

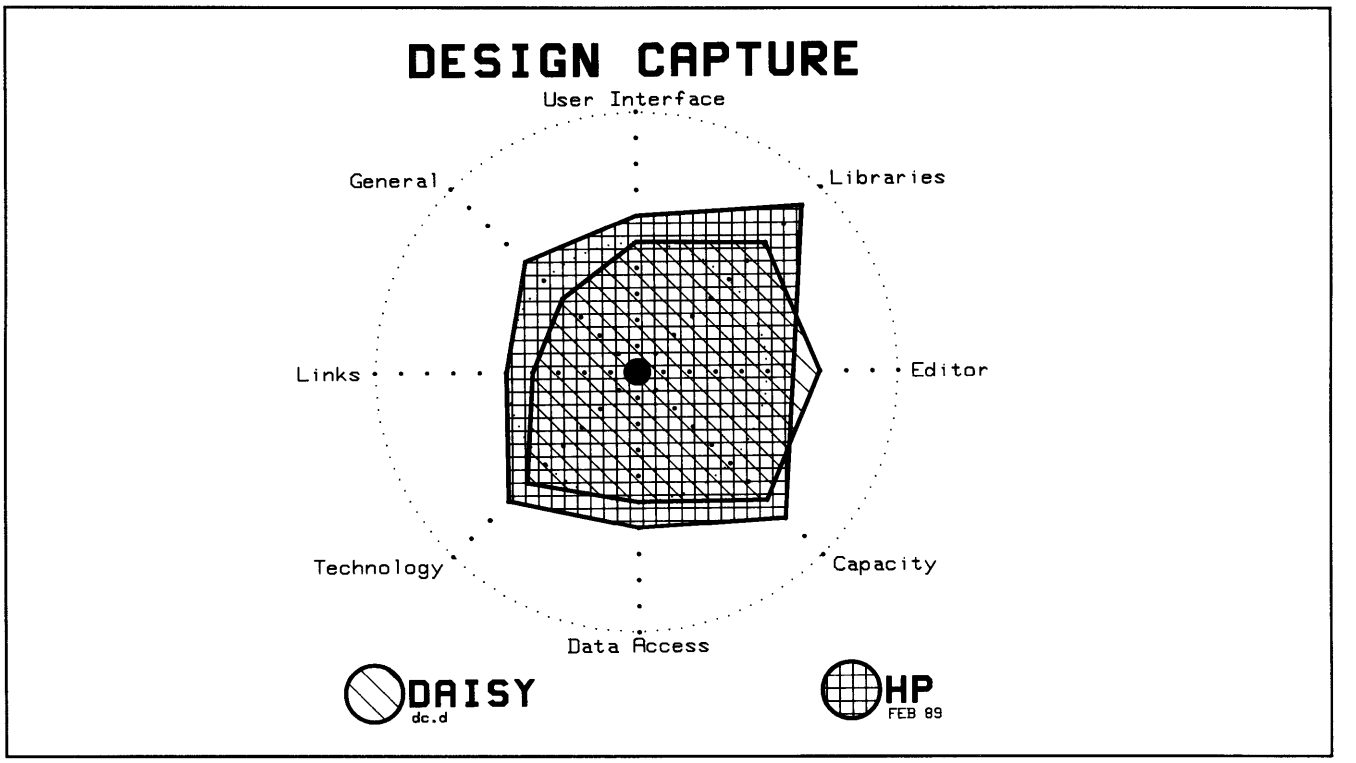

Figure 11: Standard Logic Design Entry, Daisy Logician vs HP EDS

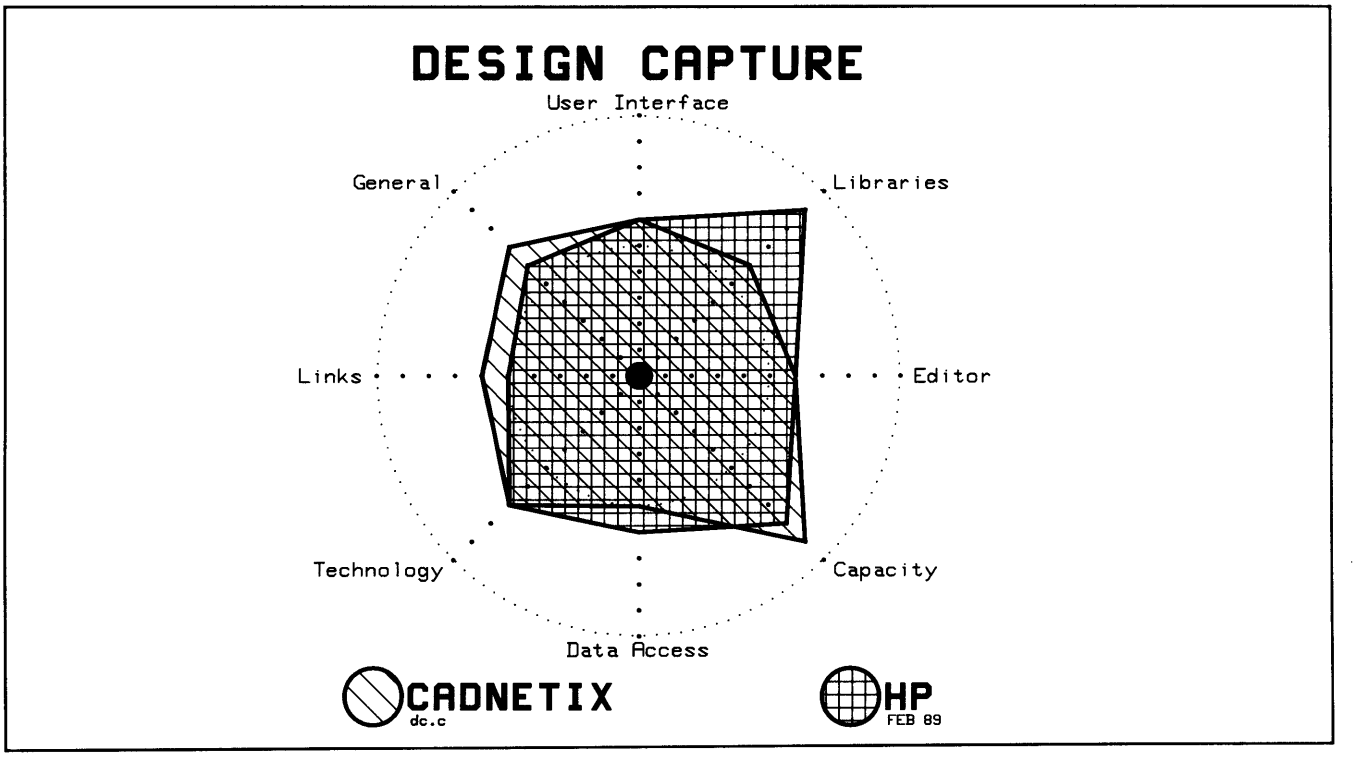

Figure 12: Standard Logic Design Entry, Cadnetix vs HP EDS

Design Verification: Daisy vs HP

Figure 13 is a diagram of Daisy's and HP's process as it applies to simulation. Daisy differs from HP in that it requires its users to run various design file compilers at each step of the process. The difference with Daisy's system becomes immediately apparent when the user exits the circuit editing environment and moves into simulation. Each time a change is made to the schematic, four separate compilers must massage the design file data before it is ready for simulation.

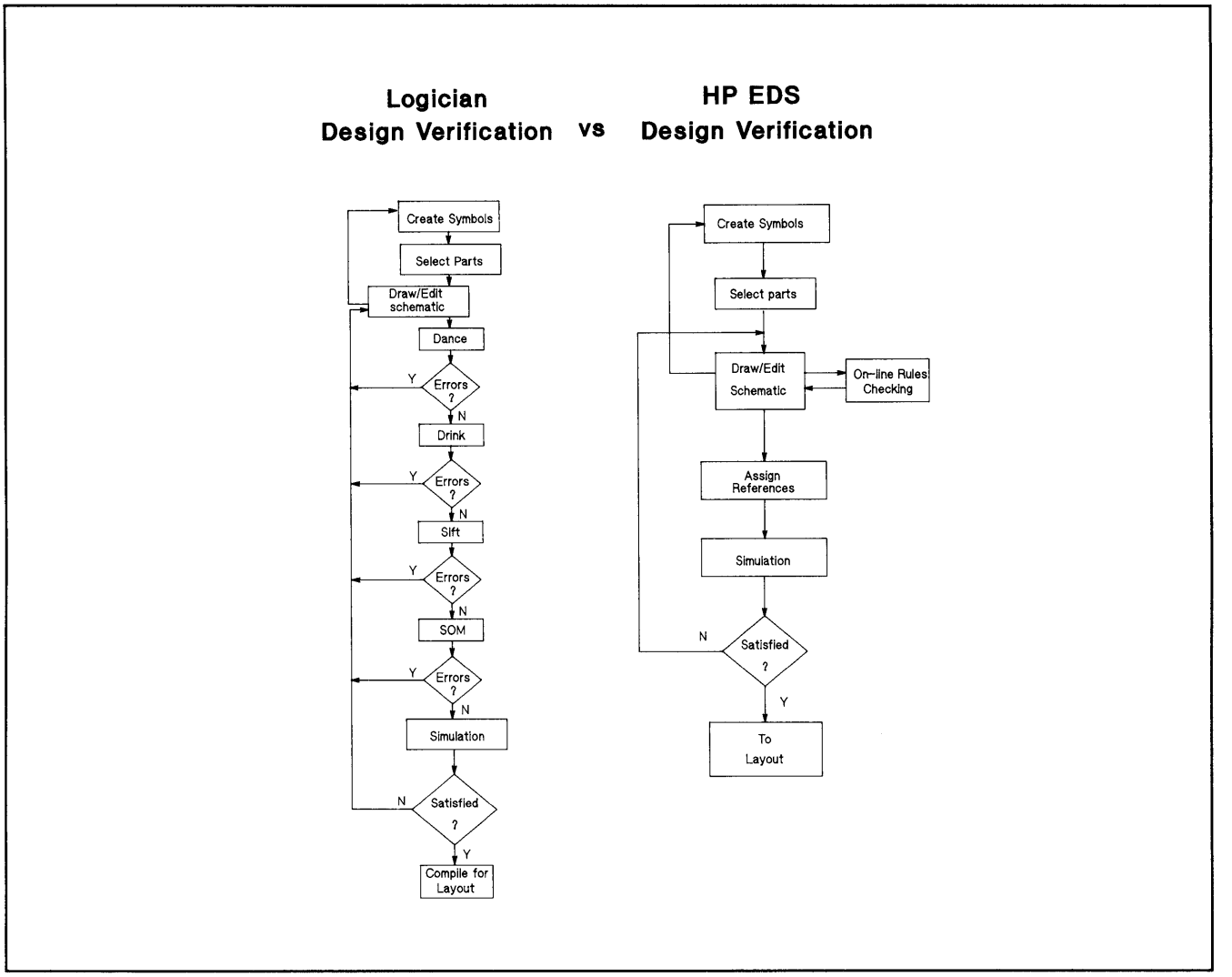

Figure 13: Daisy Logician Design Verification vs HP EDS Design Verification

Figure 14 is a spider diagram comparing Daisy and HP design verification systems. The parameters and attributes chosen for this comparison are:

- **Simulator Performance**
  - —state initialization
  - —acceleration support
  - —simulator speed
  - —simulator capacity
  - —mixed mode capability
- **Timing Analysis**
  - —back annotation of timing info
  - —physical modeling support
  - —diagnostics
  - —static and dynamic analysis
- **Links**
  - --software interfaces
  - --netlist generation
  - --to analog/mixed mode
  - --to ASIC/PLD tools
  - --to test
- **Model Language**
  - --ease of creating models
  - --debug capabilities
  - --physical shell creation
  - --HDL's supported
- **Stimulus Creation**
  - --graphical
  - --algorithmic
  - --tester compatibility
- **Results Analysis**
  - —interactive waveform
  - —what-if analysis
  - —simulator interactivity
  - —results analysis tools
  - —circuit debug capabilities
- **Usability**
  - —design cycle complexity
  - —simulator interactivity
  - —remote/distributed simulate
  - --ease of use
  - --run-time status reports
- **Libraries**
  - --coverage
  - --physical modeling supported
  - --ASIC/PLD coverage
  - --standards supported
- **Fault Analysis**
  - --testability assessment
  - --physical modeling support
  - --simulator speed
  - --fault lists and types
  - --selective fault analysis

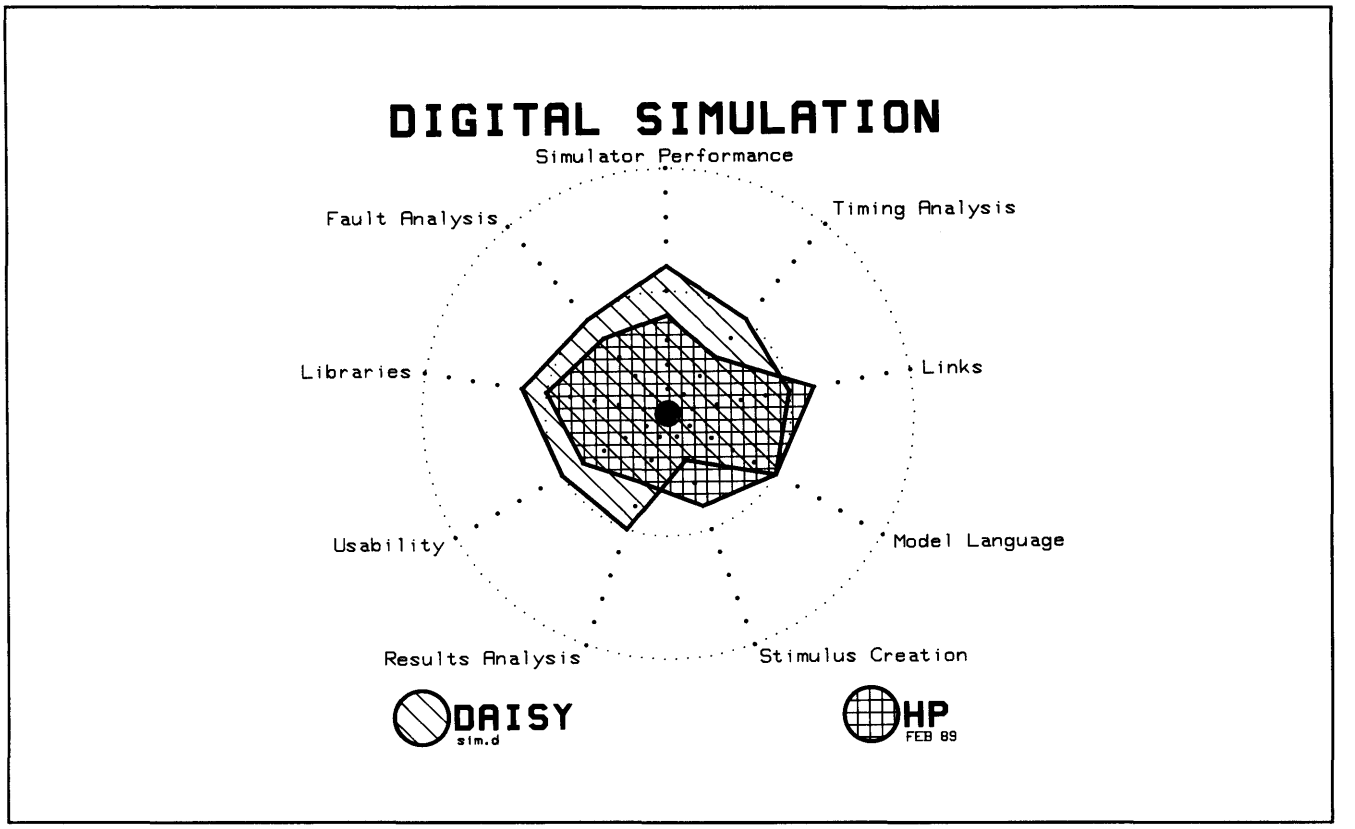

Figure 14: Design Verification Systems, Daisy Logician vs HP EDS

Daisy Logician(Design Verification) Strengths

- **Auto-Increment Naming** — ACE incorporates an auto-increment naming mechanism where the user supplies a wild card character (Data#, for example) in a name and as each element is entered in the design, that character is replaced by a number and automatically incremented.
- **Array Creation** — ACE provides a means of automatically creating repetitive structures. Users provide the tool with the number of desired replications down and across and then interactively adjust the spacing of the elements and the total size of the array.
- **Context Window** — A super view of the entire design is available to the user and shows, in addition to the entire design, an outline surrounding the part of the design currently being worked on.
- **Initialization of Stimulus** — Daisy allows for the user to specify the initial state of logic components within a design.
- **Consistent Interface** — Though the logic simulator and schematic editor are different programs, their user interfaces are similar assisting the new user in learning how to use the tools. Daisy uses both pop-up menus and icons to enter commands into the system.
- **Capture/Simulation Integration** — While running the simulator, it is possible to simultaneously view the schematic, identify nodes of interest, and have the corresponding traces displayed in the simulator trace window. It is also possible to push down into the hierarchy of a schematic to explore a design in search of errors.
- **Interactive Capabilities of Simulator** — Daisy's logic simulator provides easy to use commands for setting breakpoints, displaying traces in different radices and performing delta time calculations.

HP EDS (Design Verification) Strengths compared with Daisy

- **Single Step Access to Simulation** — HP EDS offers single step access to simulation via the Design Verification Interface with no need to do design compilation. This saves time, as compared to Daisy's method which requires that its user perform no less than four separate design compilation steps to move a circuit from the capture phase to simulation. This results in wasted engineering time as the user waits until each phase is finished.
- **Good Control of Verification Iteration** — HP EDS controls the generation of modified files for simulation. In HP EDS, complete netlist and stimulus does not have to be extracted when only one level of hierarchy is changed. Daisy requires users to repeat all compilation steps when design changes have been made.
- **Link to Prototyping** — Daisy has no equivalent to the HP 74240A link to the 16500 family of logic analyzers for prototype development and test.
- **On-Line Rule Checking** — ORC minimizes the time spent debugging the design before it can be expanded for layout (assigning references) or simulation (opening the simulation page). With Daisy, each compilation step can produce errors that force the user to return to step one and perform the compilation sequence all over again.
- **Industry-Standard Platform** — While Daisy is migrating to the Sun 386i, their simulation accelerators remain on proprietary hardware. HP offers an industry-standard platform running the Unix system for all of its design automation software.
- **Link to HP 64000 Development System** — HP EDS links code from compilers and partitions the code across multiple memory devices. Daisy requires the manual partitioning of memory contents and offers no links to microprocessor development systems.

Design Verification: Cadnetix vs HP

Cadnetix does not provide a proprietary solution for design verification, instead using HHB Softron's source code for CADAT. Cadnetix has integrated the source code for CADAT into their overall product line to make movements from one application to another effortless. Cadnetix recently acquired HHB Softron to ensure that the source code would not be acquired by another company.

Cadnetix Digital Design Verification Strengths

- **Industry Standard Simulators Supported** — Cadnetix links SPICE and Saber. However, these interfaces are at a primitive netlist level.
- **Strong Set of Primitives for Gate-Level Modeling** — A good set of parametrized primitives come with the simulator. These range from MOS gates to ALU units.
- **Correct Dual Delay and Common Mode Ambiguity Analysis** — This feature works very well for Cadnetix.

HP EDS Design Verification Strengths compared to Cadnetix

HP EDS competes extremely well against Cadnetix, as these following points indicate.

- **Application Aimed at EEs** — HP EDS is designed for electrical engineers who desire a highly productive design verification tool. Cadnetix suite of software is oriented to PCB design with links to simulation and hierarchical design added on.
- **Quick Verification Loop** — HP EDS has good control of data during the verification process. Cadnetix requires you to control the data.

HP EDS Design Verification Strengths compared to Cadnetix

- **Fast Schematic Capture and Netlist Extraction** -- HP EDS has good circuit capture and circuit modification functionality. Cadnetix has some nice features but overall, Cadnetix is slower than HP EDS due to poor circuit modification functionality and poor software performance. Additionally, Cadnetix requires a hierarchical linking before netlist extraction, while HP EDS does not.
- **Graphical/Textual Stimulus Generation** — HP EDS has a simulation page as part of the model. The simulation page has powerful graphical and textual editing tools where Cadnetix requires the use of *vi* (UNIX editor) and an understanding of the CADAT textual stimulus language.
- **Easy Access to Simulation Control** — HP EDS grants access to the simulator controls through schematic capture. Cadnetix requires running the simulator and interacting with the menu.
- **Good Control of Verification Iteration** —HP EDS controls the generation of modified files for simulation. In HP EDS, complete netlist and stimulus does not have to be extracted when only one level of hierarchy is changed.
- **Simulation Server Access** — HP EDS gives transparent access to simulation servers which reduces the verification iteration time. Cadnetix uses a manual copy of files to remote servers.
- **Link to HP 64000 Development Systems** — HP EDS links code from compilers and partitions the code across multiple memory devices. Cadnetix/CADAT requires the manual partitioning of memory contents and an addition to the library before simulation.
- **Link to PLDDS** — HP EDS can automatically create a pal symbol and simulation model. However, this is not handled (well) in Cadnetix/CADAT.
- **HILO Behavioral Modelling Language** — HILO has a flexible behavioral modeling language. The modeling language preferred by Cadnetix/CADAT is C.
- **Timing Check Parameters Included in Models** — Timing checks are implemented by the HILO simulator and are included in quality models. CADAT implements timing checks, but doesn't have data in its released library.
- **Design Database is Open** — When user defined data extraction is needed, HP DDL provides access. Cadnetix/CADAT allows access only with RINF for pre-defined reports.
- **ASIC Support** — HP EDS has a growing list of ASIC design kits which are jointly supported by HP and the vendor.
- **Simulator Control** — HILO has good stand-alone verification tools. CADAT does not have these features.
- **Links to Prototyping** — HP 16500A CAE link has no equivalent on Cadnetix/CADAT.

PLD Design and Verification

There was little information available about the capabilities or performance of Daisy's PLD Master product, therefore no comparisons were possible.

Cadnetix offers a third party product from MINC called PL Design. HP offers the proprietary PLDDS (HP PLD Design System), one of the most advanced PLD design tools available. HP PLDDS is oriented towards the system designer wanting to take full advantage of the latest PLD technology. Comparisons of Cadnetix's PL Designer and HP PLDDS strengths is below.

Cadnetix's PL Designer Strengths

- **Quicker device support (through more frequent customer updates)**
- **More flexibility in automatic device selection/ partitioning**
- **Lower price**
- **PC support**

HP PLDDS Strengths

- **Graphical STD editor**
- **Waveform Entry for synchronous and asynchronous circuits**
- **Schematic Entry**
- **Graphical Debuggers for Schematic, Waveform, and STD entry**
- **Support of Hierarchy for STD entry**
- **Support of mixed abstractions with Hierarchy**
- **Automatic and Functional Test Vector Generation**
- **Tighter Links to System CAE**

Documentation

Daisy and Cadnetix do not provide tools for documentation nor for revision control or revision management. This is a major hole in Daisy's and Cadnetix's strategy. They have adopted Sun standard platforms though, thus giving them the ability tosupport FrameMaker, Interleaf, and Simucad.

HP offers FrameMaker, a professional document publishing software designed for the engineer, scientist or technical professional.

HP FrameMaker Strengths

- **Complete word processor**
- **Graphics program** — allows importing, formatting, and creating graphics
- **Interactive page and document layout**
- **HP FrameViewer** — provides view-only access to FrameMaker documents
- **International FrameMaker** — provides localization in 5 languages

PCB CAD (Board Layout)

Daisy acknowledges Cadnetix's superiority in PCB layout, but plans on continuing Daisy's BoardMaster product. Within two years BoardMaster will have a revision that includes high frequency and hybrid support. Daisy's current BoardMaster is very similar to HP PCDS, except that in BoardMaster, both the schematic and the board are viewable simultaneously. BoardMaster has flashy menus, an autorouter, and schematic and PCB active simultaneously, but overall, not very impressive in performance compared to HP PCDS.

Figure 15 is a diagram of the design processes of Cadnetix board layout system and HP PCDS.

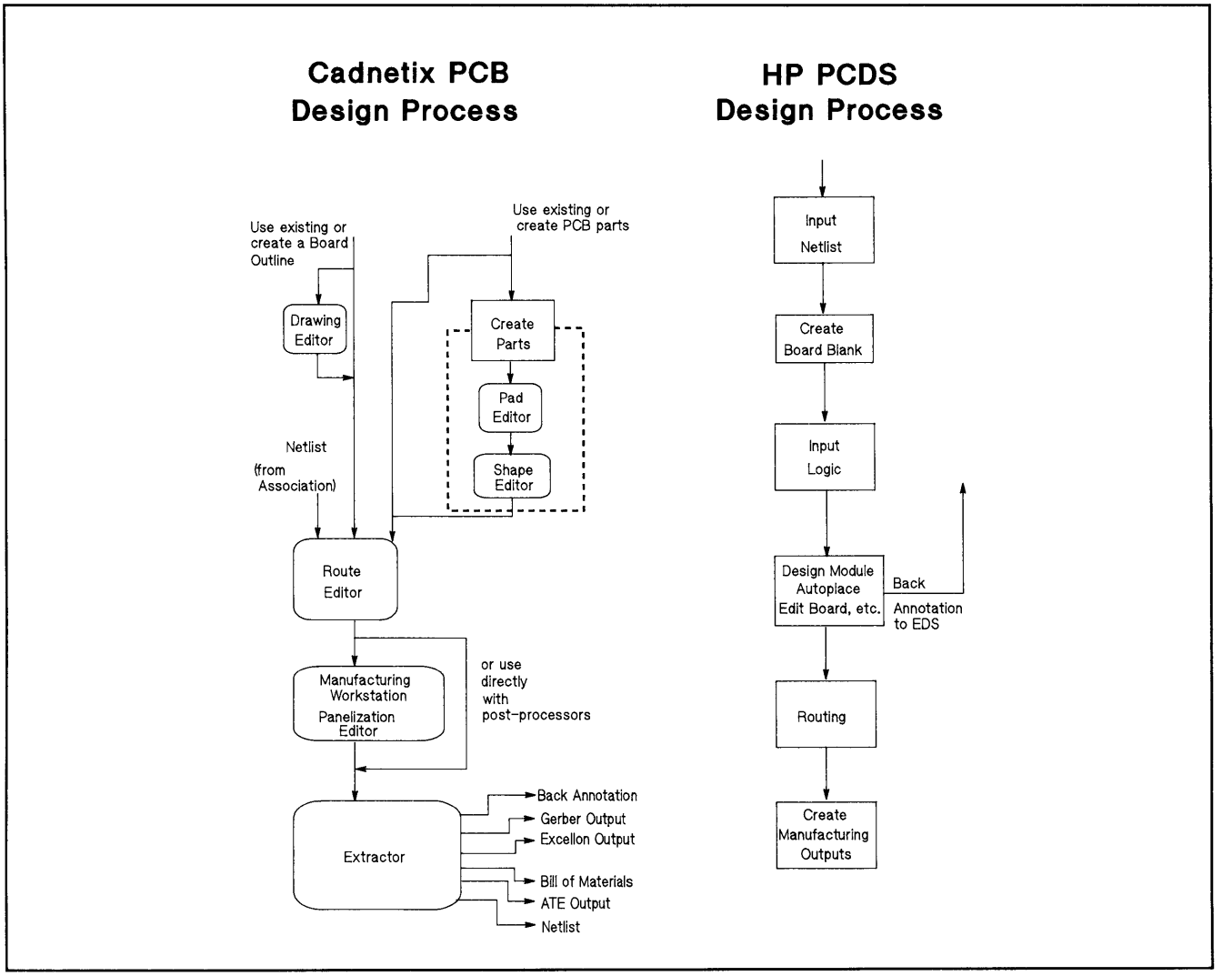

Figure 15: PCB Board Layout, Cadnetix vs HP PCDS

Figure 16 is a spider diagram comparing Cadnetix and HP board layout systems. The parameters and attributes chosen for this comparison are:

- **Manufacturing Outputs**
  - —panelization
  - —photoplotters
  - —drill
  - —pick and place
  - —assembly drawings
  - —reports
- **Library**
  - —creation
  - —maintenance
  - —vendor supplied quantity
- **Editing**
  - —interactive placement
  - —interactive routing
  - —design rule checking
  - —logic information access
- **Place & Route**
  - —automatic placer
  - —automatic router
- **Technology**
  - —surface mount
  - —through hole
  - —hybrid thick film
  - —hybrid thin film
  - —multi layer
  - —metal core
  - —ECL
- **Links**
  - —front end
  - —mechanical engineering
  - —documentation
  - —thermal
  - —test
  - —EDIF
  - —IGES
  - —open system
- **General**
  - —user interface
  - —customizability
  - —quality
  - —reliability
  - --engineering changes

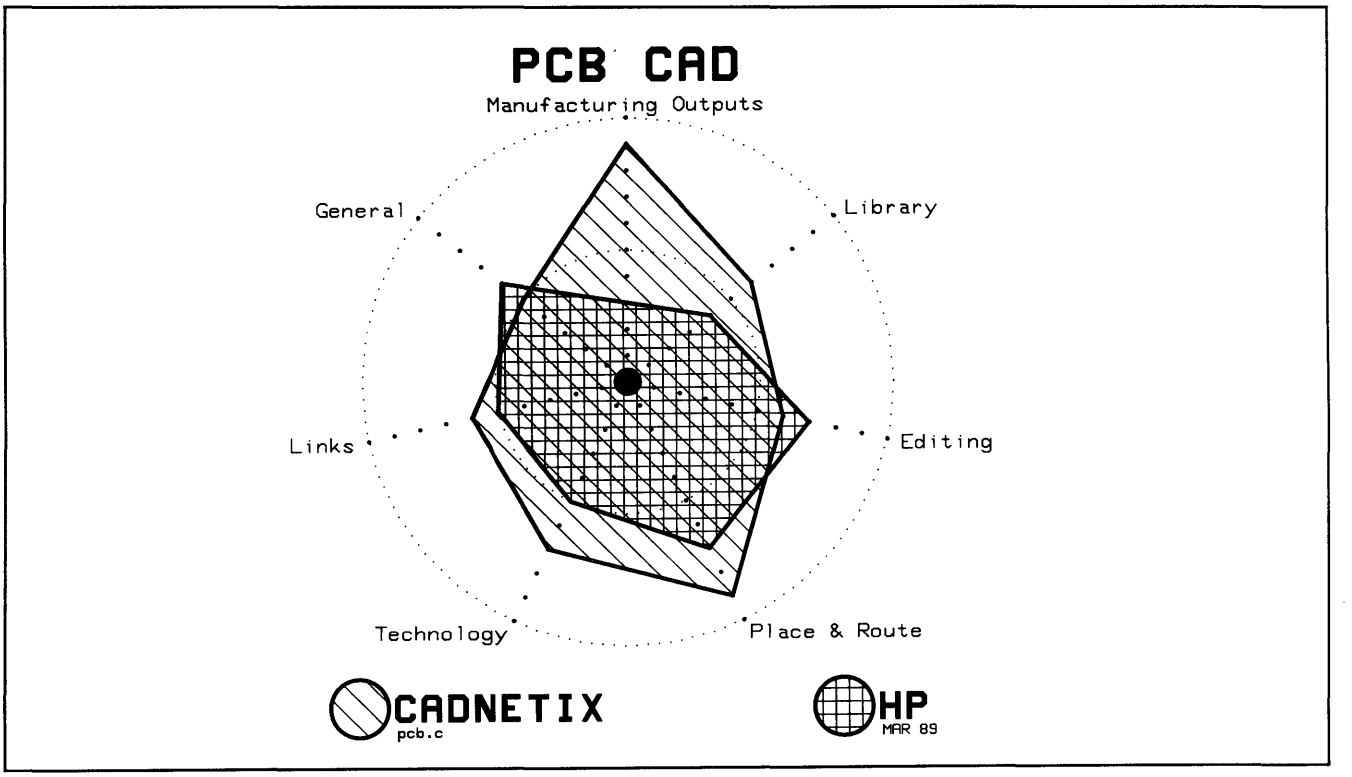

Figure 16: PCB Board Layout, Cadnetix vs HP PCDS

Cadnetix Board Layout Strengths

- **Graphical Creation of Library Part** — The creation of a library part is similar to the schematic process, plus the insertion of pins for a part is very fast.
- **Integration between Schematic and Printed Circuit Board Product** — Very tight integration of front-to-back application.
- **Stretch Command** — Very powerful implementation of STRETCH for routes.
- **Human Interface** — The Cadnetix interface is easy to adapt to and is the same interface for every application.
- **ECL Support** — The Cadnetix system does ECL designs easily, and adapts the termination of traces to minimize reflections. The Cadnetix system also daisy-chains part.
- **Priorities Assigned to Signals** — The priority of traces runs 1..100 (low to high). Standard traces are priority 25, ECL traces are priority 50. Autorouters route highest priority traces first. User can allocate and change priority.
- **Routers** — Cadnetix has two routers, its standard router which is an average router, and the Route Engine III, a proprietary hardware accelerated router which is considered as "state of the art".
- **Manufacturing Outputs** — The CDX-60000S Manufacturing Workstation performs single instance editing of boards and panelization. It also provides ASCII drill, pad, profiling, insertion, and test data outputs. It also places test coupons on the board for evaluation of manufacturing quality.

HP PCDS Strengths compared to Cadnetix

- **Link to Documentation System** — HP PCDS passes pictures into our documentation tool (FrameMaker) while Cadnetix does not provide integrated documentation.
- **HP Router** — The HP router is better than Cadnetix standard router.
- **Placement** — HP PCDS placement tools are superior both in scope and execution when compared to Cadnetix.
- **Open Links to Other Systems** — HP is committed to an open structure, allowing our access to other CAD systems data.
- **HP Service and Support** — HP has a strong company reputation for quality hardware and support. Number 1 ranking in DataPro, five consecutive years.

Daisy and Cadnetix Buzz-Word List

Analog Environment
A logical group consisting of the Analog Data Grapher and SABER.

Analog Data Grapher
Analog waveform data entry product.

Asynchronous Communications
Daisy package allowing for reliable data transfer between the Logician and a host computer, or between two Logicians. With this package, the Logician can function as a remote terminal to a design automation mainframe, and design automation input files can be transferred directly for simulation or backup.

Batch Router
A spooled router.

BISYNC/RJE Communications
Logician package facilitating the transmission and reception of files using the common synchronous serial line protocol known as BISYNC. BISYNC can be used to link two Logicians or to link a Logician to a host mainframe computer. BISYNC can be used for both short links, and with modems for medium to long distance telephone links.

CADAT
Third-party simulation product.

ChipMaster
A system for the physical layout of integrated circuits. The hardware and software, fully integrated with the Logician workstation, allow for layout on large designs.

Communications
Daisy package that provides for file transfer between the Logician and a host computer, or between two Logicians.

DCS
Daisy Circuit Simulator (DCS) is based on the SPICE programed developed at the Univ. of California at Berkeley. However, DCS allows interactive simulation, has improved convergence, speed, and circuit models. DCS can be used to perform non-linear DC, non-linear transient, adn linear AC analyses.

DFS
Daisy Fault Simulator (DFS) verifies the accuracy of a test pattern written for a circuit. The Fault simulator inserts errors in the circuit, then runs the test pattern to check if the faults have been detected. Since DFS is integrated into the Daisy Logic Simulator environment, it uses the same interface as DLS and shares the same database information created earlier by SIFT and SOM.

DQL
Cadnetix Database Query Language for extracting subsets of data from the CAM database.

DTA
Daisy Testability Analyzer (DTA) determines how testable a digital circuit will be. If the circuit turns out to be difficult to test, DTA will show you how to increase the circuit's testability by inserting test points at optimum points in the design.

Daisy Local Area Network
Provides the capability of linking Daisy workstations with an "Ethernet" network for sharing data and devices.

Digital Environment
A logical group consisting of the Graphical Editor and CADAT.

Drawing Editor
Tool to create board outlines, and do general drawing.

GateMaster
A layout editor that lets you create an actua;l physical layout of the design.

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Daisy and Cadnetix Buzz-Word List, cont'd

LAN/VAX
Provides an interface between the Daisy Local Area Network and larger host computers running under DEC's VMS operating system.

Manufacturing Workstation
Cadnetix proprietary panelization system.

MINC
Third-party PLD design product.

Pad Editor
Tool to draw pads and pad stacks.

Panel Editor
Tool used by the Manufacturing Workstation to do panelization.

Route Editor
Tool to design PCBs.

ROUTE ENGINE III
Cadnetix proprietary hardware router.

SABER
Third-party analog simulation product.

Schematic Editor
Tool to use schematic parts to create schematics.

Shape Editor
Tool to add pads with package/part outlines.

SING
SING takes the output from DANCE and DRINK, and creates files that can be used as input to any simulation tool.

Symbol Editor
Tool to draw lower level symbols (schematic parts).

TEC
A Text editing system called Techwrite, where you can format text interactively using the screen editor. You can also run a TEC input file containing formatting commands through the test processor (TEXT) to produce a completely formatted document.

TestMaster
Contains three test analysis tools to generate test data for your design: Daisy Testability Analyzer (DTA); Daisy Fault Simulator (DFS, MDFS); Tester Interface (TIN)

TIN
The Tester Interface (TIN) is a software package that lets you derive test vectors from the output created by the logic simulator (DLS/MDLS).

VT100 Terminal Emulator
Software package that allows the Logician to perform the essential functions of the DEC VT100 terminal. The emulator gives Logician users access to the simulators and other software tools on the VAX systems without using a separate terminal.

Appendix A: Daisy and Cadnetix List Software Prices

Daisy:

Advansys	Schematics & simulation	$ 23,000
Logician 386	Schematics & netllisting	50,000*
Personal Logician 386	Schematics & netlisting	25,000*
Entry!	Schematics	6,000
Daisy Logic Simulator	Digital simulation	15,000
Mega Daisy Logic Simulator	Digital simulation	40,000
DSPICE/Virtual Lab	Analog simulation	17,000
A/D Lab	Mixed analog & digital	13,000
PLD Master	PLD Design	10,500
DeepBoard Daisy Libraries*	Logic simulation & libraries	40,000*
BoardMaster	PCB layout	10,500
STAR Router	Autorouter	12,000
GateMaster	Gate array layout	22,000
ChipMaster	Custom IC layout	26,000
Pattern Editor	Graphics pattern editor	3,000
Mega FAULT	Fault simulator	40,000
ACE	Schematic capture	6,000
PMX	Physical modeler	16,500
XL Server	Accelerator/server	97,500
GigaLogician	Accelerator	180,000

* includes hardware

Cadnetix:

CDX 3000	PC System Software & Network Card	$3,000
CDX 3150	PC digital waveform editor	3,000
CDX 3200	PC analog data grapher	3,000
CDX 9500	Schematic editor for Sun 3/50	14,900
CDX 9600	Schematic editor for Sun 3/60	22,400
CDX 9610	CDX 9600 plus digital simulation	32,900
CDX 5000 S*	CAD workstation	54,000*
CDX 5600*	CAD workstation on Sun 3/60	69,900*
CDX 56000 SP*	CDX 5600 plus graphics accelerator	89,000*
CDX 66000 SP	CAM station on Sun 3/60 with graphics accelerator	113,900
CDX 75000 XP	Route Engine	89,900
CDX 9630	CDX 9600 plus analog simulation	40,900
CDX 50000 S	CDX 5000 S plus graphics accelerator	69,900
CDX 70000 S	Configurable analysis engine	30,900-150,000
CDX 6000 S	PCB manufacturing station	119,000

* includes hardware

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Appendix B: Product Coverage Comparison

	Conventional PCB		PLD	
Design Step	Daisy	HP	Daisy	HP
Architecture Design				
Structured Des.				
HW/SW Partition				
Implm. Indep.			PLD Master	PLDDS
Library Parts				
Sch. Parts Creat	ACE, ENTRY!	DCS/PCDS		
PCB Parts Creat	BoardMaster	DCS/PCDS		
Hardware Models		yes		
Mil Std Parts	yes	no		
Design Capture	ACE	DCS		
Behavioral		HILO HDL	PLD Master	
Wave/STD/Boa			PLD Master	PLDDS
Schematic Capt		DCS		PLDDS/DCS
Digital Simulation	DLS	HILO-3/ System HILO		HILO-3/ System HILO
Logic Sim.	DLS/DeepBoard	System-HILO		System-HILO
HW Sim.		HiChip		HiChip
Fault Analysis		HILO FAULT		HILO FAULT
Timing Analysis	DTS	System-HILO HiTime		System-HILO HiTime
Analog Simulation	DSPICE/AID LAB	AWB/Saber		
SW Analog				
Mixed Mode	A/D LAB	no		
Stress/reliabil		AWB/Saber		
RF/microwave		MDS		
Physical Layout	BoardMaster	PCDS		
Edit		PCDS		
Forced Router	Star	yes		
Rip-Up Router	Star	yes		
Random Route	Star	no		
Other Router		no		
DRC		on-line		
Manuf. Outputs		Mfg links		
Prototype Testing				
Waveform Cap/Com		HP16500A		HP16500A
Digital HW Test		HP16500A		HP16500A
Analog Waveform				
Analog HW Test				
System Integr Test				

Appendix B: Product Coverage Comparison, cont'd

	Conventional PCB		PLD	
Design Step	Daisy	HP	Daisy	HP
Mfg. Test Prep. Fault Analysis Test Generation Tester Links		 3065/TSSI		
Mechanical Design 2D 3D Thermal Analysis	 MDP MDP	 ME-30 ME-30		
Documentation Text & Graph Integrated Tech. Pub.		 FRAME FRAME FRAME		
SW Firmware		HP64000		
Engineering Parts				
Project Mgmt.				
Design Mgmt.		DSM		
File Management		DDC		
Misc	XLServer accelerator			
Silicon Compilers				
System Level Sim				
MSPICE PLUS				

Appendix B: Product Coverage Comparison, con'td

	Standard Cell ASIC		Gate Array ASIC	
Design Step	Daisy	HP	Daisy	HP
Architecture Design Structured Des. HW/SW Partition Implm. Indep.				
Library Parts Sch. Parts Creat PCB Parts Creat Hardware Models Mil Std Parts	ACE ACE PMX	DCS	ACE ACE PMX	DCS
Design Capture Behavioral Wave/STD/Boa Schematic Capt	ACE	DCS	ACE	DCS
Digital Simulation Logic Sim. HW Sim. Fault Analysis Timing Analysis	MEGA/GIGA Logician	HILO-3/ System HILO System-HILO HiChip HILO FAULT System HILO/ HiTime	MEGA/GIGA Logician	HILO-3/ System HILO System-HILO HiChip HILO FAULT System HILO/ HiTime
Analog Simulation SW Analog Mixed Mode Stress/reliabil RF/microwave				
Physical Layout Edit Forced Router Rip-Up Router Random Router Other Router DRC Manuf. Outputs	ChipMaster Design Kit		GateMaster Design Kit	
Prototype Testing Waveform Cap/Com Digital HW Test Analog HW Test		HP16500A HP16500A		HP16500A HP16500A
System Integr Test				

AppendixB: Product Coverage Comparison, con'td

	Standard Cell ASIC		Gate Array ASIC	
Design Step	Daisy	HP	Daisy	HP
Mfg. Test Prep. Fault Analysis Test Generation Tester Links		DICE		DICE
Mechanical Design 2D 3D Thermal Analysis				
Documentation Text & Graph Integrated Tech. Pub.				
SW/Firmware				
Engineering Parts				
Project Mgmt.				
Design Mgmt.				
File Management				
Misc				
Silicon Compilers				
System Level Sim				

Appendix B: Product Coverage Comparison, con'td

	Custom ASIC		Hybrid	
Design Step	Daisy	HP	Daisy	HP
Architecture Design Structured Des. HW/SW Partition Implm. Indep.				
Library Parts Sch. Parts Creat PCB Parts Creat Hardware Models Mil Std Parts	ACE ACE PMX		ACE	
Design Capture Behavioral Wave/STD/Boa Schematic Capt	ACE		ACE	
Digital Simulation Logic Sim. HW Sim. Fault Analysis Timing Analysis	MEGA/GIGA Logician	HILO-3/ System HILO System-HILO HiChip HILO FAULT System HILO/ HiTime	MEGA/GIGA Logician	
Analog Simulation SW Analog Mixed Mode Stress/reliabil RF/microwave		AWB/Saber MDS		
Physical Layout Edit Forced Router Rip-Up Router Random Router Other Router DRC Manuf. Outputs				EGS/MDS
Prototype Testing Waveform Cap/Com Digital HW Test Analog HW Test		 HP16500A HP16500A		
System Integr Test				

Appendix B: Product Coverage Comparison, con'td

	Custom ASIC		Hybrid	
Design Step	Daisy	HP	Daisy	HP
Mfg. Test Prep. Fault Analysis Test Generation Tester Links		DICE		
Mechanical Design 2D 3D Thermal Analysis				
Documentation Text & Graph Integrated Tech. Pub.				
SW/Firmware				
Engineering Parts				
Project Mgmt.				
Design Mgmt.				
File Management				
Misc				
Silicon Compilers				
System Level Sim				

Appendix B: Product Coverage Comparison

	Conventional PCB		PLD	
Design Step	Cadnetix	HP	Cadnetix	HP
Architecture Design Structured Des. HW/SW Partition Implm. Indep.				 PLDDS
Library Parts Sch. Parts Creat PCB Parts Creat Hardware Models Mil Std Parts	 CDX 5000/6000 CDX 56000 yes	 DCS/PCDS DCS/PCDS yes no		
Design Capture Behavioral Wave/STD/Boa Schematic Capt	CDX 5000/6000 yes yes	DCS HILO HDL DCS		 PLDDS PLDDS/DCS
Digital Simulation Logic Sim. HW Sim. Fault Analysis Timing Analysis	CDX 9510/9610 (CADAT) CDX 9510/9610 CATS CDX 9510/9610 CDX 9510/9610	HILO-3/ System HILO System-HILO HiChip HILO FAULT System-HILO HiTime		HILO-3/ System HILO System-HILO HiChip HILO FAULT System-HILO HiTime
Analog Simulation SW Analog Mixed Mode Stress/reliabil RF/microwave	CDX 9630 (SABER)	AWB/Saber no AWB/Saber MDS		
Physical Layout Edit Forced Router Rip-Up Router Random Route Other Router DRC Manuf. Outputs	CDX 56000 yes yes yes yes Route Engine yes CDX 66000	PCDS PCDS yes yes no no on-line Mfg links		
Prototype Testing Waveform Cap/Com Digital HW Test Analog Waveform Analog HW Test		 HP16500A HP16500A		 HP16500A HP16500A
System Integr Test				

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Appendix B: Product Coverage Comparison, cont'd

	Conventional PCB		PLD	
Design Step	Cadnetix	HP	Cadnetix	HP
Mfg. Test Prep. Fault Analysis Test Generation Tester Links		 3065/TSSI		
Mechanical Design 2D 3D Thermal Analysis	 included	 ME-30 ME-30		
Documentation Text & Graph Integrated Tech. Pub.		 FRAME FRAME FRAME		
SW Firmware		HP64000		
Engineering Parts				
Project Mgmt.				
Design Mgmt.		DSM		
File Management	Unified Database	DDC		
Misc				
Silicon Compilers				
System Level Sim				
MSPICE PLUS				

Appendix B: Product Coverage Comparison, con'td

	Standard Cell ASIC		Gate Array ASIC	
Design Step	Cadnetix	HP	Cadnetix	HP
Architecture Design Structured Des. HW/SW Partition Implm. Indep.				
Library Parts Sch. Parts Creat PCB Parts Creat Hardware Models Mil Std Parts		DCS		DCS
Design Capture Behavioral Wave/STD/Boa Schematic Capt		DCS		DCS
Digital Simulation Logic Sim. HW Sim. Fault Analysis Timing Analysis		HILO-3/ System HILO System-HILO HiChip HILO FAULT System HILO/ HiTime		HILO-3/ System HILO System-HILO HiChip HILO FAULT System HILO/ HiTime
Analog Simulation SW Analog Mixed Mode Stress/reliabil RF/microwave				
Physical Layout Edit Forced Router Rip-Up Router Random Router Other Router DRC Manuf. Outputs				
Prototype Testing Waveform Cap/Com Digital HW Test Analog HW Test		HP16500A HP16500A		HP16500A HP16500A
System Integr Test				

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AppendixB: Product Coverage Comparison, con'td

	Standard Cell ASIC		Gate Array ASIC	
Design Step	Cadnetix	HP	Cadnetix	HP
Mfg. Test Prep. Fault Analysis Test Generation Tester Links		DICE		DICE
Mechanical Design 2D 3D Thermal Analysis				
Documentation Text & Graph Integrated Tech. Pub.				
SW/Firmware				
Engineering Parts				
Project Mgmt.				
Design Mgmt.				
File Management				
Misc Silicon Compilers				
System Level Sim				

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Appendix B: Product Coverage Comparison, con'td

	Custom ASIC		Hybrid	
Design Step	Cadnetix	HP	Cadnetix	HP
Architecture Design Structured Des. HW/SW Partition Implm. Indep.				
Library Parts Sch. Parts Creat PCB Parts Creat Harware Models Mil Std Parts				
Design Capture Behavioral Wave/STD/Boa Schematic Capt				
Digital Simulation Logic Sim. HW Sim. Fault Analysis Timing Analysis		HILO-3/ System HILO System-HILO HiChip HILO FAULT System HILO/ HiTime		
Analog Simulation SW Analog Mixed Mode Stress/reliabil RF/microwave		AWB/Saber MDS		
Physical Layout Edit Forced Router Rip-Up Router Random Router Other Router DRC Manuf. Outputs				EGS/MDS
Prototype Testing Waveform Cap/Com Digital HW Test Analog HW Test		 HP16500A HP16500A		
System Integr Test				

Appendix B: Product Coverage Comparison, con'td

	Custom ASIC		Hybrid	
Design Step	Cadnetix	HP	Cadnetix	HP
Mfg. Test Prep. Fault Analysis Test Generation Tester Links		DICE		
Mechanical Design 2D 3D Thermal Analysis				
Documentation Text & Graph Integrated Tech. Pub.				
SW/Firmware				
Engineering Parts				
Project Mgmt.				
Design Mgmt.				
File Management				
Misc				
Silicon Compilers				
System Level Sim				


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