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NOTE: This page provides a running history of changes for a multi-page drawing which cannot conveniently be re-issued completely after each change. When making a change, list for each page all before-and-after numbers (within reason; use judgement, and use "extensive" revision note if loss of past history is tolerable, or retype complete page) and associate with each a symbol made up of the change letter and a serial subscript to appear here and on the page involved (there enclosed in a circle, triangle, or other attention-getting outline).

Ltr	REVISIONS	DATE	INITIALS
B	REVISED PER PCO 52-0844	3-29-85	BR/MR
	98626A Test Prokdure		

Model No.	Stock No. 98626-66501
Title TEST PROCEDURE	
Description	Date 3-29-85
By BILL ROBINSON	Sheet No. 1 of 12
Supersedes	Drawing No. A-98626-66501-3

98626-66501 TEST PROCEDURE

This document describes the testing of the 98626-66501 D-Series Input and Output (DIO) RS-232 interface board (RS232).

CONTENTS

1. TESTS PERFORMED

The 98626-66501 board is tested in Product Verification. The only test performed is the bench test (No 3060 testing is done on this board in Product Verification). If a board does not pass the bench test, it is sent to Defect Analysis for repair.

2. HOW TESTS ARE DONE

2.1. Equipment Required

HP Series 9000 Model 226 (9826) or Model 236 (9836) Computer with:
HPL ROM Board (98604A) or HPL RAM Disc (98614A)
98256A - 256K RAM Memory Board
98620A - DMA Controller Board

9888A Bus Expander (must have hardened backplane)
OPTIONAL - second 9888A Bus Expander (with hardened backplane)

ET30106 - HPL Test Disc
ET30117 - Hardened Backplane (in 9888A Bus Expander)

98626-67950 - RS232 Test Connector

2.2. Test Setup

Normally, you will test six boards in one hardened backplane during one test run If less than six boards are tested, follow steps 2.2.1 through 2.2.4 for one, two, three, four, or five boards.

2.2.1. Set U1, U2, U3, and U20 on each of 6 boards to the setting shown in figure 1.

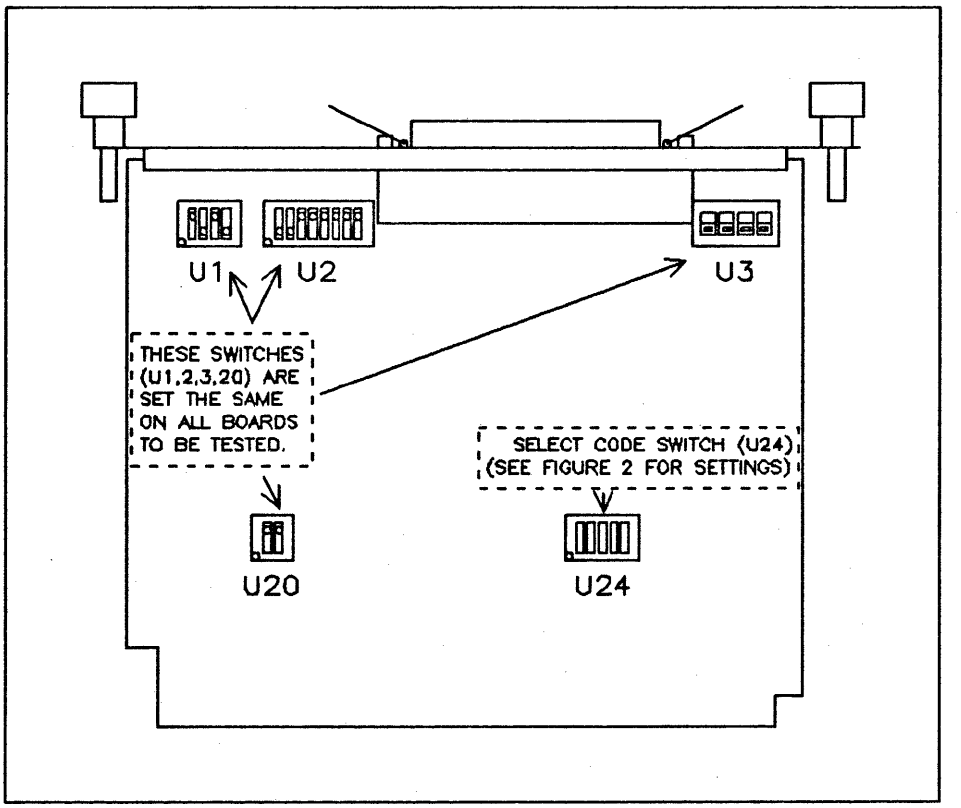

FIGURE #1 - 98626-66501

2.2.2. Figure 2 shows select code switches (U24) of all six boards being tested. Each board must have its own unique select code. Set the select code switch of board one to 1, board two to 2, board three to 3, board four to 4, board five to 5, and board six to 6. (**NOTE**: The way the select code switches are shown in figure 2 - '1' in the lower right corner and '6' at upper left - also represents how boards to be tested are installed in the 9888A Bus Expander. See figure 3 and note how the boards are shown in the Bus Expander.)

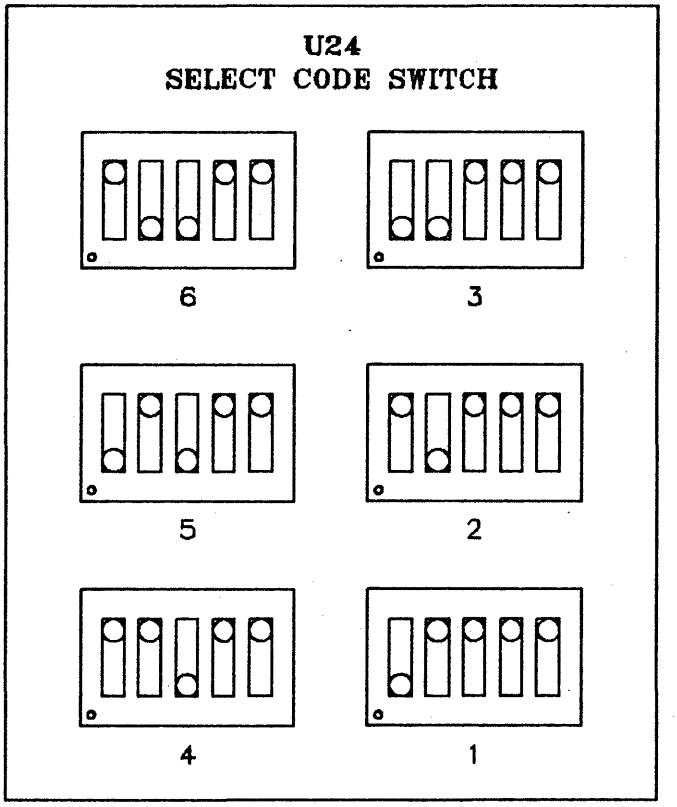

FIGURE #2 - SELECT CODE SWITCHES

2.2.3. Make sure power to the 9826 Computer and 9888A Bus Expander is OFF. Install boards to be tested in order of their select code (1 through 6), starting on the right side of the Bus Expander. (**NOTE**: when installing boards into the Bus Expander, make sure to align the boards with the connectors on the backplane and push the boards in using the thumbscrews on the sides of the panel.) A loaded Bus Expander is shown in figure 3.

CAUTION

BE SURE THE POWER SWITCHES ON THE BUS EXPANDER AND THE COMPUTER ARE OFF WHEN INSTALLING OR REMOVING BOARDS. OTHERWISE, DAMAGE TO BOTH THE COMPUTER AND THE BOARD BEING INSTALLED/REMOVED MAY RESULT.

2.2.4. Install an RS232 Test Connector (98626-67950) on each board to be tested.

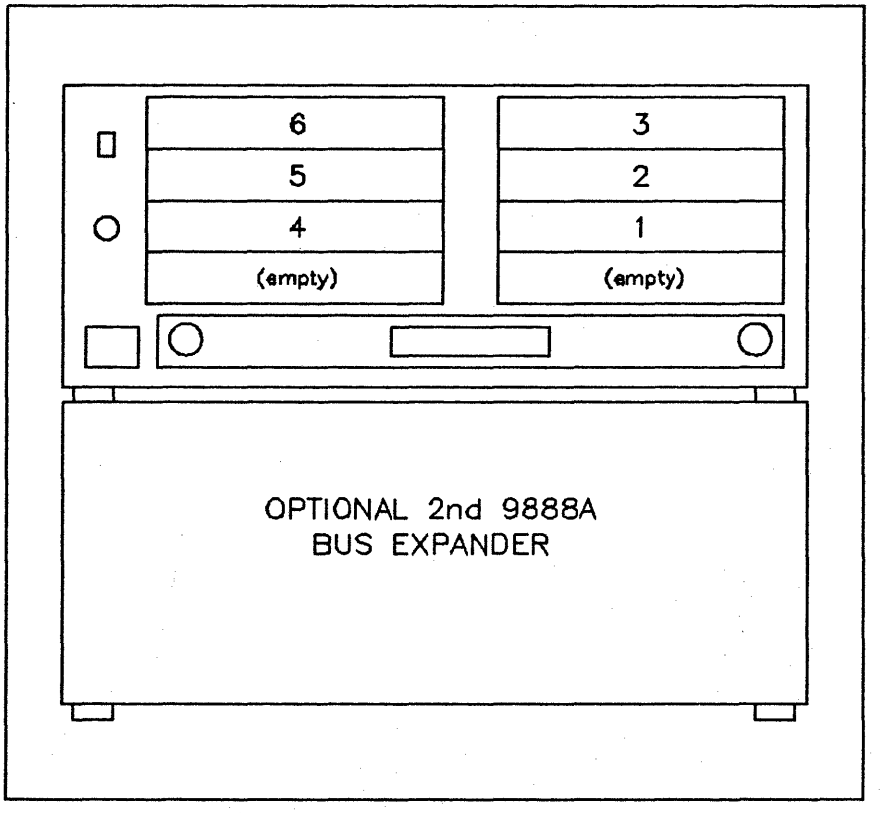

FIGURE #3 - 9888A BUS EXPANDERS WITH BOARDS TO BE TESTED

2.3. Running the Test

2.3.1. Insert the disc (ET30106) into the disc drive of the 9826 Computer. (**NOTE:** A 9836 Computer can be used in place of the 9826 Computer.)

2.3.2. Turn the power switch of the Bus Expander to ON.

2.3.3. Turn the power switch of the 9826 Computer to ON. The test will run automatically and test all boards, one at a time. If all 6 boards pass the bench test, the 9826 Computer's display will show the following:

::SEVEN I/O CARDS ARE PRESENT::
98620A: DMA
98626A AT S/C 1
98626A AT S/C 2
98626A AT S/C 3
98626A AT S/C 4
98626A AT S/C 5
98626A AT S/C 6

98626A ON S/C 1
PASSED

98626A ON S/C 2
PASSED

98626A ON S/C 3
PASSED

98626A ON S/C 4
PASSED

98626A ON S/C 5
PASSED

98626A ON S/C 6
PASSED

END OF TESTING

The names of tests that are run on the boards will be seen at the lower left of the 9826 Computer's display as the test is being performed. If one of the boards being tested does not pass one of the tests, the following is an example of what could be displayed on the 9826 Computer's screen:

98626A ON S/C 2
98626A ON S/C 2 - problem with OCD3/OCD4 outputs
******* BOARD FAILED *******

Then, either the next board will be tested or, if there are no more boards to test, testing will end. (If you are using the optional second Bus Expander, you can set up six boards in that Bus Expander (see 'Test Setup' section) to run when testing in the current Bus Expander finishes.)

2.3.4. When testing in the current Bus Expander finishes, turn off the 9826 Computer AND 9888A Bus Expander. If an error has occurred on a tested board at a specific select code, tag the board to be repaired with its' error message and date and send it to Defect Analysis.

2.3.5. If you have the optional second 9888A Bus Expander and it is loaded with boards that are ready to test, turn that Bus Expander on, THEN turn the 9826 Computer on to test these boards. If you are not using the optional second Bus Expander, remove the boards you have just finished testing and set up six more boards to be tested (see 'Test Setup' section) and repeat the process. (**NOTE**: It does not matter whether you turn off the 9826 Computer or 9888A Bus Expander first, but it does matter how you turn them ON. Make sure you turn on the 9888A Bus Expander first, THEN turn on the 9826 Computer.)

2.3.6. Set switches of boards that pass the Product Verification Test to the shipping switch positions shown in figure 4 (**NOTE**: The only change is to set the select code switch to the position shown - which is select code 9).

2.3.7. Stamp the boards that pass the Product Verification Test with the bench test stamp to indicate that they have been tested.

2.3.8. Continue testing until all boards in the workorder are completed.

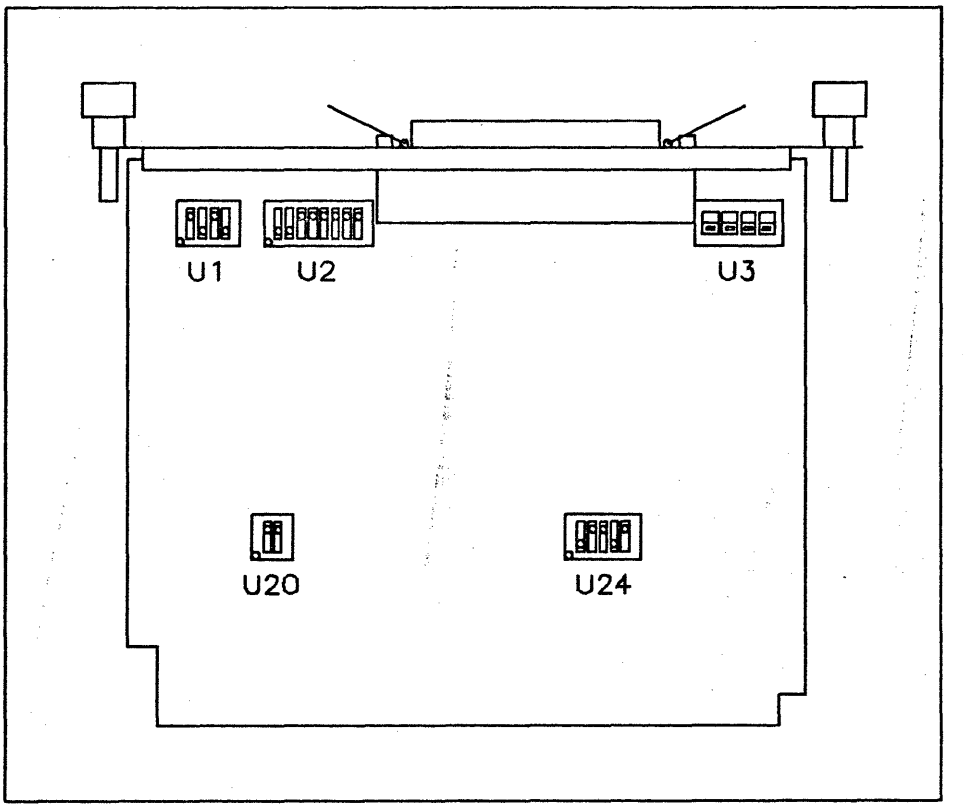

FIGURE #4 - 98626-66501 SHIPPING SWITCH POSITIONS

3. PREPARING BOARDS FOR SHIPPING

The following steps should be done for each board that passes the Product Verification Test before it is sent to shipping.

3.1. Do an overall visual check of the board including the following: check that components are not lifted from the board; check for components not installed properly - particularly capacitors, resistors, and resistor packs; check for the switches set to their shipping position (see figure 4); check both sides of the board for excess solder, and close or touching component legs; and, check the painted panel for dirt and scratches.

3.2. Check the date-code of the printed circuit board to make sure it is the right date-code.

3.3. Check each printed circuit board for the bench test stamp.

3.4. Record the serial number of the printed circuit board in the shipping log. (The serial number is located on the white tag on the pad side of the board.)

3.5. Attach the warranty sticker to the pad side of the board, near the serial number tag.

3.6. Clean the gold, male contact-fingers of the printed circuit board with a clean cloth and alcohol.

3.7. Send the board to the shipping area.

4. FURTHER DOCUMENTATION

The following list of documentation is included as a reference for those who want more information about testing of this board.

DOCUMENT DESCRIPTION	DOCUMENT NUMBER
98626 Theory of operation	A-98626-66501-9
98626 Schematic	C-98626-66501-4
98626 Engineering Ref. Spec. (ERS)	A-98626-90300-1
98626 Component Locator	D-98626-66501-5
3060 Test Description	A-ET13330-9001-1
3060 Noded Assy. Dwg.	C-ET13330-6001-1
3060 Noded Schematic	C-ET13330-6001-5
Designer's GT 9826 Cardcage	A-5955-6551-1
DIO Bus Specification	5955-7669
RS-232 Interface Installation	98626-90000
BASIC Interfacing Techniques	98613-90020
ET30106 Description (HPL Test Disc)	A-ET30106-97001
ET30117 Description (Hard Backplane)	A-ET30117-97001
98626-67950 Description	B-98626-67950-1

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Ltr	REVISIONS	DATE	INITIALS
A	As Issued Per PCO 11594	11-9-81	

Model No. 98626A	Stock No.
Title 98626A EXTERNAL REFERENCE SPECIFICATION	
Description	Date 5 October 1981
By Lloyd NELSON	Sheet No. 1 of 17
Supersedes	Drawing No. A-98626-90300-1

98626A EXTERNAL REFERENCE SPECIFICATION

1.1 SWITCH DESCRIPTIONS

There are five switches on the 98626A interface assembly. These are a select code switch, interrupt level switch, modem status line disconnect switch, line characteristics switch and a baud rate select switch. The line characteristics and baud rate switches are read at power up/reset and used to determine default values to initialize the UART to.

Refer to Figure 1 for switch locations and orientations.

Select Code Switch

The setting of this switch determines the base address which the interface will respond to as follows:

Setting	Address
00000	600000
00001	610000
.	.
.	.
11111	7F0000

Interrupt Level Switch

The setting of this switch determines the level which the interface will interrupt on as follows:

Setting	Interrupt Level
00	3
01	4
10	5
11	6

Line Characteristics Switch

This switch is used to select power up/reset values for the character length, parity, stop bits and handshake type. See description of register 7 for details.

Modem Status Line Disconnect Switch

03	02	01	00
RI	DSR	CTS	CD

This switch is used to disconnect and tie high interface receiver inputs connected to unused modem status lines so that they always appear ON. This may be done for one of two reasons. First, crosstalk in a cable can cause spurious interrupts to be generated if the UART is enabled to interrupt on changes of the modem status lines. Second, system drivers may require that certain modem status lines be ON before transmitting or receiving data and the device on the other end may not drive these lines.

Baud Rate Select Switch

This switch is used to select a power up/reset value for the baud rate. Refer to a description of register five for details.

1.2 CONNECTOR PINOUT

The connector pinout is intended to be compatible with the ALVIN interface and the 2621 terminal so that common cables may be used. The signal and circuit definitions are for the DTE cable. The DCE cable will map the circuit line so that operation is transparent to the drivers.

Signal	Circuit	Pin	Pin	Circuit	Signal
OCD4		1	26		OCD3
		2	27		
		3	28		
		4	29		
		5	30		
		6	31		OCR3
		7	32	TT	
		8	33		
RI	CE	9	34		
+12		10	35		+5
-12		11	36		+5
Txd	BA	12	37	SD	
RTS	CA	13	38	TS	
DTR	CD	14	39	TR	
SRTS (OCD2)	SCA	15	40	CH	DRS (OCD1)
		16	41		
		17	42	BB	Rxd

Signal	Circuit	Pin		Pin	Circuit	Signal
	SC	18		43		
		19		44	CB	CTS
		20		45	CC	DSR
		21		46	CF	CD
		22		47	SCF	SCD (OCR2)
		23		48	AB	GND
Shield		24		49		
		25		50		

11.1 INTERFACE REGISTER MAP AND RESET STATE

MS : 0 : 0 : 0 0 0 1 0		1 READ
RESET INTERFACE		1 WRITE
IE : IR : INT LVL		3
OCD3 : OCD4 : OCR2 : OCR3 : BAUD RATE SELECT		5
0 : 0 : SCD :		
LINE CHARACTERISTICS SWITCH		7
RECEIVER/TRANSMITTER BUFFER		17 DLAB=0
DIVISOR LATCH LEAST SIGNIFICANT BYTE		17 BLAB=1
0 0 0 0 : MSCI : RLSI : TREI : RBFI		19
	0 : 0 : 0 : 0	DLAB=0
DIVISOR LATCH MOST SIGNIFICANT BYTE		19 DLAB=1
0 0 0 0 0 : INT ID : INTR		21
	0 0 : 1	

LTR	P.C. NO.	APPROVED	DATE
	See Pg.1	for Revision	11-9-81
REVISIONS			

MODEL 98626A STK. NO.

98626A EXTERNAL REFERENCE SPECIFICATION

BY Loyd Nelson DATE 05 October 1981

APPD. SHEET NO. 4 5 OF 17 16

SUPERSEDES DWG. NO. A-98626-90200-1

11.1 INTERFACE REGISTER MAP AND RESET STATE (cont'd.)

DLAB	BRK	PARITY	STB	CHAR LENGTH	
0	0	0 0 0	0	0 0	23

	Loop	SRT	DRS	RTS	DTR	
0 0 0	0	0	0	0	0	25

	TSRE	THRE	BI	FE	PE	OE	DR	
0	1	1	0	0	0	0	0	27

CD	RI	DSR	CTS	DCD	TERI	DDSR	DCTS	
				0	0	0	0	29

When the interface is reset, register bits with an underscored lable are set to the state shown. All other labeled bits are either unchanged or reflect the current state of the input or switch to which they are connected. A zero or one in an unlabeled box indicates that that bit is always in that state.

11.2 REGISTER DESCRIPTIONS

Address 1 READ - ID Register

07	06	05	04	03	02	01	00
MS	0	0	0	0	0	1	0

MS - Master/Slave
When this bit is a one, it indicates that this is a remote port for data or commands.

Address 1 WRITE - Control Register 0

07	06	05	04	03	02	01	00
Reset Interface							

Address 3 READ/WRITE - Interface Interrupt Register

07	06	05	04	03	02	01	00
IE	IR	INT LEVEL SWITCH		X	X	X	X

IE - Interrupt Enable
Writing a one to this bit enables the interface to interrupt whenever the IR bit is a one.

IR - Interrupt Condition (READ ONLY)
The UART interrupt request line is asserted.

INT LEVEL - Interrupt level switch setting (READ ONLY).

00 - Interrupt level 3
01 - Interrupt level 4
10 - Interrupt level 5
11 - Interrupt level 6

Address 5 READ/WRITE

07	06	05	04	03	02	01	00
OCD3	OCD4	OCR2 (SCD)	OCR3	BAUD RATE SELECT			

BAUD RATE SELECT SWITCH - (READ ONLY)
These four bits correspond to the setting of the baud rate select switch on the interface. This switch is read by the interface drivers at power up/reset to determine an initial value to initialize the UART buad rate to as follows:

Setting	Baud Rate
0000	50
0001	75
0010	110
0011	134.5
0100	150
0101	200
0110	300
0111	600
1000	1200
1001	1800
1010	2000
1011	2400
1100	3600
1101	4800
1110	7200
1111	9600

OCR3 - Optional Circuit Receiver 3 (READ ONLY).
This bit returns the current state of the line connected to optional circuit receiver 3. It is a one when the line is ON and a zero when it is OFF.

SCD - Secondary Carrier Detect (READ ONLY).
This bit returns the current state of the Secondary Carrier Detect line. It is a one when the line is ON and zero when it is OFF.

OCD4 - Optional Circuit Driver 4.
OCD3 - Optional Circuit Driver 3.
Writing a one or zero to these bits turns the corresponding circuit driver ON or OFF respectively. These bits can be read to determine the current state of the driver.

Address 7 READ

07	06	05	04	03	02	01	00
LINE CHARACTERISTICS SWITCH							
HANDSHAKE TYPE		LINE CONTROL REGISTER INITIALIZATION					

LINE CHARACTERISTICS SWITCH
This register returns the setting of the line characteristics switch on the interface. This switch is read by the operating system at power up/reset and used to determine an initial value to initialize the UART line control register to and also to determine what type of software handshake if any should be implemented.

HANDSHAKE
The setting of these two switches will be used at power up to determine the type of software handshake as follows:

Setting	Handshake
00	Ack/Eng
01	Xon/Xoff
10	none
10	none

LINE CONTROL REGISTER INIT
The setting of these switches will be used to initialize the UART line control register at power up/reset and will be written into the corresponding bit of that register. See the description of that register for further details.

Addresses 17 - 29 access UART registers.

Address 17 READ (DLAB=0) - UART Receiver Buffer
WRITE (DLAB=0) - UART Transmitter Holding Register

07	06	05	04	03	02	01	00
:							:
:							:
:							:

The UART receiver and transmitter are both doubly buffered. A character to be transmitted is written into the transmitter holding register. When the transmitter shift register becomes empty, the character is automatically transferred to it and shifted out. Another character may then be written into the holding register while the first is being shifted out. Received characters are shifted into the receiver shift register. When this register becomes full, the data is automatically transferred to the receiver buffer where it may be read while another character is shifted in.

Address 17 READ/WRITE (DLAB=1) - Baud Rate Divisor Latch LSByte
Address 19 READ/WRITE (DLAB=1) - Baud Rate Divisor Latch MSByte

07	06	05	04	03	02	01	00
:							:
:							:
:							:

The UART has an internal Baud Rate Generator. The Baud Rate is set by writing a divisor into the 16 bit divisor latch and is determined by

Baud Rate = 153600/Baud Rate Divisor

To access the Baud Rate Divisor Latch, is is necessary to get the DLAB (Divisor Latch Access) bit of the Line Control register. This will prevent access to the Transmitter Holding register, Receiver Buffer, and the Interrupt Enable register but will allow all other UART registers to be accessed in their normal manner. The DLAB bit should be cleared once the Divisor Latch is initialized.

Address 19 READ/WRITE (DLAB=0) - Interrupt Enable Register

07	06	05	04	03	02	01	00
0	0	0	0	MSCI	RLSI	TREI	RBFI

The four LSB of this register enable the UART to interrupt on specific conditions as described below. These bits are set/cleared by writing out a one/zero and are also cleared when the interface is Reset.

RBFI - Enable Receiver Buffer Full Interrupts.
When set, the UART will interrupt whenever the DR bit of the Line Status register is a one. The interrupt is cleared by reading the receiver buffer or writing a zero to the DR bit of the Line Status register.

TREI - Enable Transmitter Holding Register Empty Interrupts.
When set, the UART will interrupt whenever the THRE bit of the Line Status register is a one. The interrupt is cleared by writing a character into the Transmitter Holding register or by reading the Interrupt Identification register (if the interrupt was caused by an empty Holding register).

RLSI - Enable Receiver Line Status Interrupts.
When set, the UART will interrupt whenever any of the OE, PE, FE, or BI bits of the Line Status register is a one. These bits and the interrupt can be cleared by reading the Line Status register.

MSCI - Enable Modem Status Change Interrupts.
When set, the UART will interrupt when any of the DCD, DCTS, TERI, or DDSR bits of the Modem Status register is a one. These bits and the interrupt can be cleared by reading the Modem Status register.

Address 21 READ - Interrupt Identification Register

07	06	05	04	03	02	01	00
0	0	0	0	0	INT ID		INTR

INT ID - Interrupt Cause ID
Indicates the highest priority interrupt currently pending. When the interrupt ID register is read, the highest priority interrupt currently pending is frozen and no other interrupts will be acknowledged until the condition causing the interrupt is cleared.

INT ID	INTERRUPT CAUSE
11	Receiver Line Status (highest priority)
10	Receiver Buffer Register Full
01	Transmitter Holding Register Empty
00	Modem Line Status change (lowest priority)

Receiver Line Status Interrupt.
A Receiver Line Status interrupt is generated whenever the RLSI bit of the Interrupt Enable register is set and any of the OE, PE, FE, or BI bits of the Line Status register is a one. The interrupt can be cleared by reading the Line Status register which also clears the OE, PE, FE, and BI bits.

Receiver Buffer Full Interrupt.
A Reciever Buffer Full interrupt is generated whenever the RBFI bit of the interrupt enable register is set and DR bit of the Line Status register is a one. The interrupt is cleared by reading the receiver buffer or by writing a zero to the DR bit.

Transmitter Holding Register Interrupt.
A transmitter holding register empty interrupt is generated whenever the TREI bit of the Interrupt Enable register is set and the THRE bit of the Line Status register is a one. The interrupt is cleared by writing into the Transmitter Holding register or by reading the Interrupt Identification register.

Modem Line Status Change.
A Modem Line Status Change interrupt is generated whenever the MSCI bit of the Interrupt Enable register is set and any of the DRLS, DCTS, DDSR, or TERI bits of the Modem Line Status register is a one. The interrupt can be cleared by reading the Modem Line Status register which clears the DRLS, DCTS, DDSR, and TERI bits.

INTR - Interrupt Pending.
This bit is a zero whenever the UART is requesting an interrupt.

Address 23 - READ/WRITE - Line Control Register

07	06	05	04	03	02	01	00
			PARITY				
DLAB	BRK	STK	EVEN	PEN	STOP	CHAR LENGTH	

DLAB - Divisor Latch Access Bit.
When this bit is set to a one, it is possible to access the divisor latches of the Baud Rate generator during a read or write to registers 17 and 19.

BRK - Set Break.
When this bit is set to a one, the TxD line will be forced to the Spacing (logic zero) state and remain there regardless of other transmitter activity. This bit must be cleared to disable the break and reenable normal transmitter activity.

STK - Stick.
EVEN - Even Parity.
The type of parity that is transmitted or recieved is determined by the setting of these two bits.

Setting	Parity
00	odd parity
01	even parity
10	parity bit '1'
11	parity bit '0'

PEN - Parity Enable.
When set to a one, this bit enables the transmitter to transmit and the receiver to check for a parity bit between the last bit of the data word and any stop bits. When this bit is set to zero, no parity bit is transmitted or checked.

CHAR LENGTH - Character Length.
The setting of these two bits determines the length of the transmitted and received characters as follows:

Setting	Bits/Char
00	5
01	6
10	7
11	8

STOP - Stop Bits.
This bit, along with the number of bits/character determines the number of stop bits transmitted after every character.

Setting	Bits/Char	Stop Bits
0	5, 6, 7, 8	1
1	5	1.5
1	6, 7, 8	2

Address 25 READ/WRITE - Modem Control Register

07	06	05	04	03	02	01	00
0	0	0	Loop	SRTS (OCD2)	DRS (OCD1)	RTS	DTR

Loop - Loopback.
When set to one, this bit enables a loopback feature for diagnostic testing. The serial output of the UART and therefore TxD are set to the Marking state. The UART receiver input is disconnected and the output of the transmitter shift register is looped back into the receiver shift register. The modem control inputs CTS, DSR, CD, and RI are disconnected externally and connected internally to the four modem control outputs DTR, RTS, DRS, and SRTS.

When in loopback mode, receiver and transmitter interrupts are fully operational. The modem control interrupt source is now the modem control output register bits instead of the modem control inputs.

DRS - Data Rate Select.
SRTS - Secondary Request to Send.
RTS - Request to Send.
DTR - Data Terminal Ready.
Writing out a one or zero to these bits sets the corresponding modem control line ON or OFF respectively. The current state of the lines can be read back.

Address 27 READ/WRITE - Line Status Register

07	06	05	04	03	02	01	00
0	TSRE	THRE	BI	FE	PE	OE	DR

TSRE - Transmitter Shift Register Empty.
This bit is set to a one whenever the Transmitter Shift register is empty.

Bits 06 - 00 of this register can all be set by writing out a one in addition to the being set by the conditions described below.

THRE - Transmitter Holding Register Empty.
This bit is set to a one whenever the Transmitter Holding register is empty. It is cleared whenever a character is written into the Transmitter Holding register.

BI - Break Indicator.
This bit is set to a one whenever the received data input is held in the spacing condition for longer than a full work transmission time. This bit is cleared whenever the Line Status register is read.

FE - Framing Error.
This bit is set to a one whenever the stop bit after the last data bit or parity bit is at the spacing level. This bit is cleared whenever the Line Status register is read.

PE - Parity Error.
This bit is set to a one when the received character does not have the correct even or odd parity as selected by the parity select bit. This bit is cleared whenever the Line Status register is read.

OE - Overrun Error.
This bit is set to a one whenever the Receiver Buffer register was not read before the next character was transferred in from the Receiver Shift register. This bit is cleared whenever the Line Status register is read.

DR - Data Ready.
This bit is set to a one whenever a character has been transferred into the receiver buffer register. This bit is cleared by reading the receiver buffer register or writing zero to this bit of the Line Status register.

Address 29 READ/WRITE - Modem Status Register

07	06	05	04	03	02	01	00
CD	RI	DSR	CTS	DCD	TERI	DDSR	DCTS

CD - Carrier Detect (READ ONLY).
This bit returns the current state of the CD line. It is a one when the CD line is ON and zero when it is OFF.

RI - Ring Indicator (READ ONLY).
This bit returns the current state of the RI line. It is a one when the RI line is ON and zero when it is OFF.

DSR - Data Set Ready (READ ONLY).
This bit returns the current state of the DSR line. It is one when the DSR line is ON and zero when it is OFF.

CTS - Clear to Send (READ ONLY).
This bit returns the current state of the CTS line. It is one when the CTS line is ON and zero when it is OFF.

DCD - Delta Carrier Detect.
This bit is set when the CD line has changed since the last time the Modem Status register was read.

TERI - Trailing Edge of Ring Indicator.
This bit is set whenever the RI line has changed from an ON to an OFF condition.

DDSR - Delta Data Set Ready.
This bit is set whenever the DSR line to has changed since the last reading of the Modem Status register.

DCTS - Delta Clear to Send.
This bit indicates that the CTS line has changed since the last reading of the Modem Status register.

Appendix I. Rev. A Register Map.

Address 1 READ - ID Register
1 WRITE - Reset Interface

07	06	05	04	03	02	01	00
X	X	X	0	0	0	0	0
RS	NOP						

RS - Reset Interface.
This bit is latched by the interface. It is set by writing out a one, at power up, and whenever the Reset line is asserted. A zero must be written to this bit to clear the reset and enable the interface.

Address 3 READ - Interrupt Status Register.

07	06	05	04	03	02	01	00
X	IR	INT LEVEL		X	X	X	X

IR - Interface is requesting interrupt service.

INT LEVEL - Interrupt Level switch setting.

00 - Interrupt level 3
01 - Interrupt level 4
10 - Interrupt level 5
11 - Interrupt level 6

Address 5 READ - Switch 2 Setting.

07	06	05	04	03	02	01	00
Switch 2							

Address 7 READ - Switch 3 (4 LSB) setting.

07	06	05	04	03	02	01	00
X	X	X	X	Switch 3 (4 LSB)			

Reading register 7 returns the setting of the four LSB of switch 3.