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CIO Parallel Interface Device Adapter

External Reference Specification

Roseville Networks Division

Location Code: 52-7560

Project Number: 27114B

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Project Manager: John McHugh
Product Manager: Bill Wang
Development Engineer: Pery Pearson
Development Engineer: Thang Le
Diagnostic Engineer: Bill Hooper
Production Engineer: Ken Konesky
Support Engineer: Dary Wong

PREFACE

Preliminary
Revision 1.0 11/14/88
Revision 2.0 01/27/89
EDITING HISTORY:

10/24/88: Outline of ERS (TL)
11/04/88: Preliminary description of registers (TL)
11/14/88: Preliminary ERS (TL)
11/17/88: Correct A28/B28 pin swap mistake
Correct set/reset definition for DEND and ATTN
Add info about single-ended termination
12/08/88: General correction based on ERS review of 11/29
12/09/88: Change DEND/CEND on 27114B to PEND/HEND
Define FP data to be non-inverted
01/20/89: Drop DIAG bit, invert sense of PZERO bit in reg7
to become NZERO bit, swap header blocks +/-
01/25/89: Define FP data to be inverted (comp. with 27114A)
Clarification of EDGE and LOAD bits
03/28/89: Proof-read and corrections made for grammar and
technical accuracy.

NOTE:

This document is strictly an external reference specification for the 27114B card. It only specifies what is seen and observable at its interface points: the CIO backplane and the parallel frontplane interface.

For more information as how it operates in a system, the readers must confer with other documents: HP-CIO Standard Document, the respective driver's ERS etc...

Contrary to the expectation of some readers, this document is not intended to be used as an ERS for the GPIO product which consists of both a hardware (card) and a software (driver) product. As a product, some of the card's behaviors will be greatly influenced by how the driver is written. That kind of information is to be covered in another document which describes the hardware/software interaction.

It is assumed that the reader is familiar with the CIO standard (HP-CIO STANDARD DOCUMENT, Version 2.2 - Roseville Networks Division).

This document is written in a format compatible with TDP's Manu formatter, requiring no special environments. It is currently available as a set of 12 files:

afi1ers afi2ers afi3ers afi42ers afi43ers afi44ers afi46ers
afi47ers afi5ers afi6ers afi7ers afi8ers

INTRODUCTION

SECTION 1

The 27114B is a 16 bit parallel device adapter for the CIO channel. It has a 64 level FIFO used to buffer data between the CIO backplane and the adapter's frontplane interface. A counter is provided to allow an exact number of handshakes to take place. The 27114B can interrupt the host in various situations: end of count, end of handshake (from a peripheral) or a peripheral attention.

The 27114B is intended to replace the 27114A to remedy some of its deficiencies:

* Insufficient grounding for single-ended applications
* Vague control of frontplane handshakes due to the presence of a FIFO
* Limited number of frontplane control and status signals
* Limited number of frontplane handshake modes
* Lack of features which allow asynchronous termination of input/output

Some of the features which are removed from the 27114A are:

* Backplane parity option
* Pass-through frontplane parity option
* Testhood detection capability (not available to user's program)

Besides the above changes and deletions, the following changes should also be noted for the new design of the AFI card:

* The use of synchronous state machines throughout (no delay lines, and no RC time delay circuits)
* A degradation of frontplane handshake performance

As for compatibility, the 27114B should be fully compatible with the 27114A when it is used with previously released drivers (1.0 through 3.0 versions of the HP-UX/Series 800 operating system). The 27114B can be used with the old single-ended cables (but not recommended for new applications).

Since the 27114A's on-line diagnostic is very specific to the 27114A hardware, it will not be compatible with the new 27114B hardware. To diagnose 27114B cards used in systems which have older drivers and diagnostics, the diagnostic must be updated.

As far as raw performance is concerned, the 27114B should be a slower than the 27114A. How much impact this will have on the overall system performance remains to be seen. The slight performance sacrifice is necessary to implement other required features in the 27114B.

TERMINOLOGY DEFINITIONS

SECTION 2

2.1 INPUT/OUTPUT DEFINITION

The input direction is defined as the flow of data from the user's peripheral to the system's memory. A read is a transaction which moves data from the IO card to the CPU.

The output direction is defined as the flow of data from the system's memory to the user's peripheral. A write is a transaction which moves data from the CPU to the IO card.

2.2 WORD, BYTE AND TRANSFER

Word and byte have their usual meanings of 16 and 8 bit data units (the 32 bit word definition used by the Spectrum program is not used here since it is always easier to say 'word' than 'half word').

Since the 27114B's data path is 16 bits wide, it is sometimes confusing to describe the amount of data being transferred as N*2 bytes or N words. The rest of this document will always assume that the 27114B transfers data in the 16 bit mode. Each transfer is therefore equivalent to one 16 bit word.

2.3 LITTLE/BIG ENDIANS

This document uses the normal convention of 0 being the least significant bit in any data or address field.

2.4 LEADING/TRAILING EDGES

As a signal changes from one level to another level, it is defined as the leading edge if the change allows the signal to be in the asserted state. When a signal changes from the asserted state to the deasserted state,

the edge is called a trailing edge.

2.5 CIO INVERSION OF LOGIC

DATA INVERSION:

The CIO backplane is a low-true logic bus. A 1 in the program domain results in a low voltage level on the corresponding signal and vice versa. Since the AFI card does not invert signals between itself and the CIO bus, the same logic interpretation applies between the program domain and the hardware of the 27114B card. This must be considered when one is to work on the 27114B hardware.

This version of the ERS defines all frontplane signals such that a 0 in the user's program domain will correspond with a low at the frontplane (no logic inversion for frontplane outputs and inputs). This is applicable to both the data and the control/status lines.

ASSERTION/DEASSERTION:

A signal is in its assertion condition when it is at the level which causes a result to happen. It is in its deassertion condition when it is at the level which cannot cause a result. These levels can be low or high (electrically), 0 or 1 (logically). Clarifications will be attempted in the rest of this document to qualify an assertion condition as either low true or high true.

LOW/HIGH:

Low means the voltage is at a TTL low level, nominally below 0.8 Volts. High means the voltage is at a TTL high level, nominally above 2.0 Volts. These will be used to indicate the conditions of various circuits on the 27114B hardware.

0/1:

0 means a false logic in the program domain. 1 means a true logic in the program domain. When descriptions are given in 0 and 1 or true and false, these are described in the program domain.

SET/RESET(CLEARED):

Set/reset conditions are usually used to describe the state of flipflops or register bits on the 27114B. A set condition means the flipflop is in the asserted state and is a 1. A reset condition means the flipflop is in the deasserted state and is a 0.

CONVENTION:

* Assertion/deassertion are always qualified with low/high or 0/1 or false/true
* Hardware description uses low/high
* Logic description in the program domain uses 0/1 or false/true

2.6 GLOSSARY

Definition of terms which are unique to the 27114B card and its environment.

CONFIGURATION

SECTION 3

3.1 CONFIGURATION FEATURES

To customize the 27114B card for any application, the user has the following choices:

* single-ended (unbalanced) or balanced differential cable
* desirable cable length (3m and 12m standard)
* the number of control lines vs other output features like HEND and PDIR
* the number of status lines vs other input features like PEND and ATTN
* the length of PCTL high and low time
* the hysteresis time of the PFLG signal

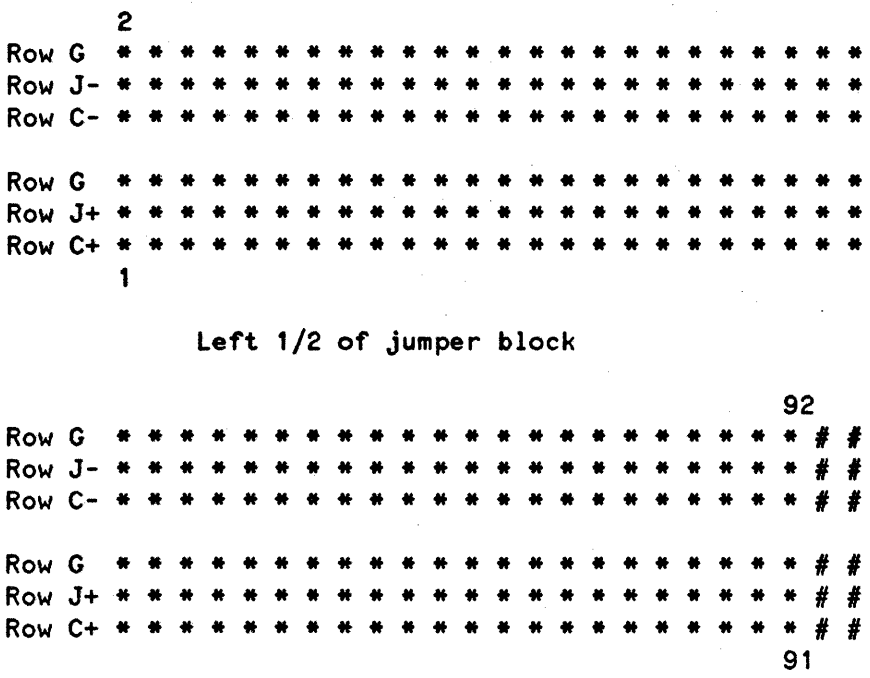
3.1.1 Single-ended/Differential Ouputs

To provide a good solution to single-ended cable applications, there is a jumper block arrangement on the 27114B card which allows the user to dynamically reconfigure the connection of signals in a 27114B cable.

Each signal received or driven by the 27114B is available as a pair of differential signals, an inverting (-) and a non-inverting (+) output. If the input to a line driver is at a TTL high level, the (+) output is at a high level and the (-) output is at a low level. If the input is at a TTL low level then the (+) output is at a low level while the (-) output is at a high level.

The 27114B will be supplied with only one cable type, differential, which has 47 twisted pairs. The previously available single-ended cables are not recommended for use with the 27114B. They are still compatible with the 27114B but for a new application, the 47 twisted pair cable is recommended since it should outperform the single ended cable in all aspects of electrical characteristics.

The jumper block consists of 6 rows of 48 pins arranged in the following manner:



Right 1/2 of jumper block

Only 46 of the 48 columns are actually used. The rightmost two columns are not used. Markings are done for jumpers 1, 2, 91 and 92. Also marked is G, J, and C- for the upper rows and G, J, and C+ for the lower rows.

All pins on the G rows are grounded. All pins on the J+/J- rows are connected to the (+)/(-) signals on the connector, respectively. All pins on the C+/C- rows are connected to the driver/receiver packs' output/inputs (+)/(-), respectively. There is a space between the C+ and lower G rows to prevent unintentional shorting of C+ signals to ground. 12 jumper blocks are supplied. Each block can be used to connect 8 sets of pins on adjacent rows. 6 of these, stacked end to end will allow one entire row to be shorted to an adjacent row (J+ to either C+ or G). The other 6 are used for the other set of signals (J- to either C- or G).

To configure in the differential mode, each signal from the connector on the J+ row must be connected to a package pin at the same column on the C+ row. Likewise, signals on the J- row must be connected to package pins on the C- row. Therefore signals go straight between the driver/receivers and the connector pins (J+ to C+, J- to C-).

To configure in a single ended mode, one rail of the connector pins (either J+ or J-) is grounded (connected to G), leaving the other set of pins connected straight to the driver/receiver packs. For example, in the case of a low true connection, row J+ is connected to row G and row J- is connected to row C-. In this case, (-) signals go straight to the cable but the companion wires on the cables (connected to J+ pins) are grounded. This arrangement maintains a good degree of noise tolerance for all single ended signals.

The characteristic impedance for each signal should be very close to that of the twisted pairs. The following illustrates the view of the jumper blocks with respect to the frontplane connector in different cases:

DIFFERENTIAL: Connector - Empty row - Jumper block - Empty row - Jumper block

LOW TRUE: Connector - Empty row - Jumper block - Jumper block - Empty row

HIGH TRUE: Connector - Jumper block - Empty row - Empty row - Jumper block

3.1.2 Line Termination

To properly terminate the cable in the different frontplane connection modes, the termination load and reference packs must be installed according to the following scheme.

IDENTIFICATION OF PIN 1 OF TERMINATION SOCKETS: There are three 20 pin termination sockets on the 27114B card. Pin 1 of these sockets has a square pad on the printed circuit assembly board. All other pins have a round pad. Pin 11 is the pin which diagonally opposes pin 1. Pin 10 is on the same side of pin 1 but at the other end of the package. Pin 20 is the other corner pin.

IDENTIFICATION OF PIN 1 OF SIPs: The SIPs (single in-line packages) have 10 pins in one straight line. Pin 1 is the first pin on the end which is usually marked with a solid band or a dot.

IDENTIFICATION OF PIN 1 OF DIPs: The DIPs (dual in-line packages) have 16 pins arranged as two rows of 8 pins. Looking from the top, there is usually a dot at one corner or a notch at one end of the pack. The dot marks where pin 1 is. If the DIP is positioned such that the notch is up, pin 1 is the first pin on the left row from the top.

DIFFERENTIAL (BALANCED MODE):

3 16-pin DIPs (1810-0964) are required. These must be plugged into the three termination sockets such that their pin 1 goes to pin 2 of the socket (the four corner pins of the sockets are not used).

LOW-TRUE SINGLE-ENDED (UNBALANCE MODE):

3 10-pin load SIPs (1810-0677) and 3 10-pin reference SIPs (1810-0906) are required. Pin 1 of the load SIPs must be connected to pin 20 of the termination sockets. Pin 1 of the reference SIPs must be connected to pin 1 of the termination sockets.

HIGH-TRUE SINGLE-ENDED (UNBALANCE MODE):

3 10-pin load SIPs (1810-0677) and 3 10-pin reference SIPs (1810-0906) are required. Pin 1 of the load SIPs must be connected to pin 1 of the termination sockets. Pin 1 of the reference SIPs must be connected to pin 20 of the termination sockets.

3.1.3 Cable length

There are currently two cable lengths available: 3 m and 12 m. These should be adequate for most applications. Note that the 12 m cable should not be used in single-ended applications due to the inherent low noise margin of the single-ended signals.

It should be noted that the DuPont company, Cumberland, PA. (USA) has been willing to manufacture the differential cable in any cable length. Inquiries should be referenced to HP's drawing numbers, 27114-63001 and 27114-63003.

*** SAFETY NOTE ****

The overall length of the 27114B cable cannot exceed a length at which the total shield path resistance exceeds 100 milli-ohms. This shield path includes the shield of the cable from one end to another, plus the shield trace on the 27114B and the shield connection on the host (typically between the backplane's shield connector pin and the safety ground plug of a three prong plug of the system).

*** TO BE VERIFIED ***

The shield path resistance for a 12 m cable meets the above specification for all existing supported systems.

The 27114B product is tested with two different cable lengths: 3 m and 12 m. Note that if there is excessive signal reflection, certain cable lengths may be much more sensitive to self-induced noise. From an electrical performance point of view, it is projected that the cable could be extended to a length longer than 25 m. If this is the case, the user must be assured that all electrical specifications are still within the required ranges (voltages, timing etc...).

Due to a restriction of resources, the project team will not be able to guarantee cables longer than the supported 12m length.

3.1.4 PCTL Pulse Extension

One of four jumper positions (J1 through J4) must be selected to insert a delay in the PCTL path. The following table illustrates how:

Jumper position selected	Delay added to PCTL's transition: high to low	low to high
J4 (P 3)	150 ns	50 ns
J3 (C 2)	100 ns	50 ns
J2 (T 1)	50 ns	50 ns
J1 (L 0)	0 ns	0 ns

Note that the assertion state of PCTL is low.

Only one jumper can be installed in the above four positions.
There will be an indeterminate result if more than one position has a jumper in it.

3.1.5 PFLG Filtering

Jumpers J5 through J8 can be used to select a filtering effect for the PFLG signal. The following table illustrates the selection:

Jumper position selected	PFLG sync time
J8 (P 3)	4 clocks (150 - 200 ns)
J7 (F 2)	3 clocks (100 - 150 ns)
J6 (L 1)	2 clocks (50 - 100 ns)
J5 (G 0)	1 clock (0 - 50 ns)

As PFLG is an asynchronous signal to the card, it is always sync'ed first before being used by the state machine on board the 27114B.

The minimum selectable value is one clock. The 50 ns associated with this (as shown in the table) means that if PFLG is stable for at least 50 ns, it is guaranteed to be seen by the 27114B. It does not mean that the card will ignore a PFLG which is stable for less than 50 ns. The exact timing of the PFLG signal will determine whether the change could be seen or not.

The other 3 positions (J6 through J8) require the change in PFLG to be solid for the appropriate amount of time as shown in the previous table. For example, if jumper position J7 is selected, a change in PFLG is guaranteed to be recognized if it has happened more than 150 ns. It could also be recognized if it has been more than 100 ns but this is not really guaranteed (depending upon the actual timing of PFLG versus the 27114B's sampling clock). If the PFLG signal temporarily reverses to its original level for 15 ns or more,

*** CHECK THIS 15 ns NUMBER ****

the filtering circuit resets its timer and the change is considered to start after the temporary reversal.

This filtering selection should be very effective in filtering out false triggers to the PFLG circuit should the application exhibit excessive noise on that signal (mostly due to cross-coupled noise or line reflection).

3.1.6 Control/Status Options

The user has the option to configure the frontplane control and status lines. Control lines are outputs which the user's program can control directly, independent of the state of the driver or the hardware. They are programmable directly as control bits in registers in the hardware. Their states do not affect the operation of the rest of the 27114B hardware. Status lines are input lines which can be sampled and read directly as bits in status registers on the 27114B hardware. The states of the status inputs do not affect the function or condition of the rest of the hardware.

The 27114B has six control outputs. Four of these are permanently assigned as controls, and two of them can be reassigned to carry two different functions: HEND and PDIR. The card powers up with the HEND and PDIR functions selected. Both of these function outputs are selected via the same option bit; they cannot be selected individually. The HEND output is asserted with the last output word or after the last input word. The PDIR output reflects the state of the direction control bit on the AFI card.

The 27114B has six status inputs. Two of these are also connected to two alternative circuits, PEND and ATTN. When these circuits are enabled (independently), they can activate different functions on the hardware. The card powers up with the ATTN option selected and the PEND option unselected. The ATTN circuit is compatible with the 27114A. Any falling edge (high to low) of the ATTN signal can trigger and log a pending interrupt condition in the ARQ flipflop (if properly enabled). The PEND

circuit can be used by a peripheral to terminate a transfer prior to the exhaustion of its count. The PEND needs to be asserted high with the last input word or after the last output word.

3.2 CONFIGURATION AT SHIPPING

As shipped from the factory, the 27114B will be configured for a differential application. It will have a 3 m cable and will power up like a 27114A card. The PCTL pulse extension is set at 0 ns. The PFLG hysteresis selection is set at 0 ns.

3.3 SYSTEM CONFIGURATION

Due to the restriction placed on CIO level 1 cards (the AFI is a level 1 card), the AFI card can only respond to group 0 pollings. This requires that the card be placed in slot 0 through 7 of any CIO backplane.

To configure/reconfigure the card in a HP-UX system, please refer to the appropriate system administrator manual for the correct procedure. Essentially, this step requires that the 27114B card be declared in a configuration file with proper information like the driver's major number, the slot position, the CIO channel slot position, etc... A kernel build then generates a complete new kernel which supports the 27114B card.

HARDWARE SPECIFICATION

SECTION 4

4.1 GENERAL HARDWARE OVERVIEW

The following measurements are for the main PCA (less cable and testhood):

* Size: 0.171 m (Width) X 0.174 m (Depth) X 0.0134 m (Height)
  Height is measured from top surface of PCA
  to top of tallest component (SIP, 1810-0677).
* Weight: approximately 0.300 Kg
* Current consumption: approximately 2 A (5 V only)
* Operating environment: HP Class B

4.2 BACKPLANE SPECIFICATION

LEVEL 1 CARD:

The 27114B AFI card is a CIO level 1 card. This renders the card different than most (if not all) other CIO cards. The CIO's level 2 protocol is not applicable to this card.

CIO BACKPLANE ADDRESSING:

4 CIO signals are used to address 1 of 16 registers on the 27114B card: BP1/CBYT/CEND/BP0 (arranged in this order of significance). Note that while some other CIO programming documentation (including the CIO standard) may have a different address naming convention, the method used on this module was adapted after that which was originally used on the series 500 machines.

SLOT LIMITATION:

As noted earlier, the AFI is a level 1 card and therefore restricted to group 0 polls. Consequently, it must be in a slot in the range of 0 through 7. This restriction is imposed due to the design of the TTL channel adapter for the series 840/850 machine.

COMPATIBILITY:

The AFI 27114B is designed to be compatible with the CIO standard (version 2.2 11/1986). It should be compatible with all existing CIO backplanes on Series 800 systems.

CIO BACKPLANE PERFORMANCE:

Depending on the number of data words presently stored in the FIFO on board the 27114B, the backplane transfer rate varies. Bursting is allowed as long as there are at least 8 or more possible transfers. For example,

in the output direction, bursting is allowed whenever there is 0 through 55 words in the FIFO. In the input direction, if there are more than 8 words in the FIFO, bursting is allowed. Other than those, data will be handled on a word by word basis with a poll between them. This approach serves to simplify the backplane interface (eliminating the 4 external latches and the associated state machine to control them in the old 27114A) and maintain approximately the same burst transfer speed.

CIO PARITY:

Since there are no real demands for the CIO parity function and it takes at least 3 chips to support, this feature is not supported on the 27114B.

4.3 MID-PLANE SPECIFICATION

4.3.1 Reset

CIO RESET:

Upon power up or the assertion of the /RST signal on the CIO backplane, the 27114B goes into the hard-reset state. Until it is removed from this state, all normal accesses are ignored. Only a write to the data register (register 0) with a 1 in the data bit corresponding to the slot which the 27114B is in would bring it out of its hard-reset state.

A hard-reset resets the ARE flipflop (interrupt is disabled) and sets the RESET flipflop. Both of these are also accessible with writes to register 1 (CIO CONTROL register).

CARD RESET:

When the RESET flipflop is set, the 27114B is in the (soft) reset state. This resets all frontplane state machines and presets all write data register (register 1) bits to 1. The RESET flipflop does not affect the ARE flipflop.

FRONTPLANE RESET:

The FIFO is reset with the CRFF bit in the write register 7 (AFI CONTROL register). This means it is also reset with a reset condition or a hard-reset condition. As long as the CRFF bit is a 1, the FIFO remains in the reset state.

STATE MACHINE RESET:

The state machine is also reset with the CRFF bit like the FIFO. As explained in more detail later on, the state machine controls all the handshakes between the FIFO and both the frontplane and the backplane circuits. The power-up/reset default state is such that the 27114B:

* guarantees to bring its PCTL to a low deassertion state immediately. PCTL is kept in this state until the 27114B is programmed by the host for a transfer.
* asserts the HEND output to a low level
* does not take any handshake from a peripheral until it is programmed to do so by the host

INTERRUPT RESET:

The interrupt circuit consists of two flipflops: ARE (enable) and ARQ (register). ARE is reset by a hard reset condition only. ARQ is reset with any read from register 9 (CIO STATUS register).

4.3.2 FIFO

The 27114B uses a FIFO to improve data flow between the frontplane and the backplane. The FIFO is a 64 level deep, 18 bit wide FIFO. It is built with 2 CY7C409 64 X 9 FIFO chips from Cypress Semiconductor.

The FIFO is used in a half-duplex mode. Depending on the direction of data transfer, it can take data from the frontplane or the backplane and output data to the other party. 16 bits are used to carry data between the frontplane and the backplane. The 17th bit is used exclusively for the PEND signal. The PEND's direction of flow is from the frontplane to the backplane in the case of input transfers. For output transfers, the PEND circuit bypasses and does not use the 17th bit of the FIFO. The 18th bit is used to carry the HEND signal from the CIO backplane to the frontplane. It is useful only in output transfers. For input transfers, the HEND circuit does not use the 18th bit of the FIFO.

The CY7C409 FIFO chip has a feature which facilitates the design of the 27114B. It has two status outputs which indicate whether there is more than 1/8, 1/2 or 7/8 of data being stored in the FIFO. By taking advantage of these flags, the bursting feature on the CIO backplane is enabled whenever there is room for at least 8 transfers. As the number of available transfers drops below 8, the bursting feature is turned off, and all transfers are done on a word-by-word basis. In the non-bursting case, a service poll is done between two consecutive transfers (other CIO cards can also be serviced before the next transfer happens). Bursting on CIO allows up to 32 transfers to be done between service polls.

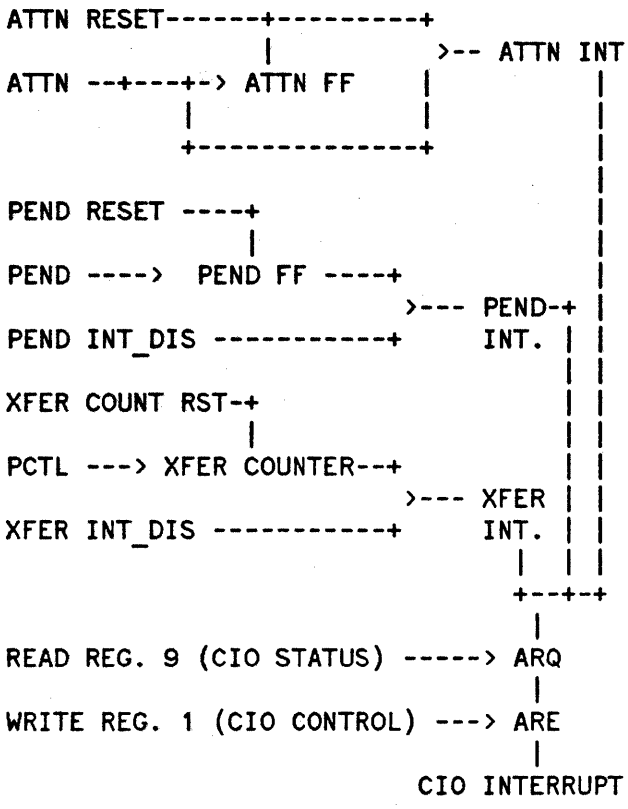
The effective FIFO length in the output direction is 55 levels. Service polls are answered positively only when there are room for 8 words or more in the FIFO. Burst Request is asserted low during all CIO transfers to the 27114B. Due to the delayed response from the CIO handshake state machine, there might be occasionally up to 58 words stored in the FIFO.

The effective FIFO length in the input direction is still 64 levels. Any time the FIFO has less than 8 words, transfers will be done in the non-bursting mode.

Upon a reset condition (CRFF being asserted with a 1, soft reset or hard reset), the FIFO is cleared and all stored words (if there are any) are lost; all outputs become low.

4.3.3 Interrupts

There are three interrupt sources on the 27114B: PEND, ATTN and the transfer counter (the 27114A has only one: ATTN). The power up default mode inhibits both PEND and transfer counter interrupts and enables the ATTN interrupt.



PICTURE: INTERRUPT CIRCUIT ON 27114B

All three sources are OR'ed together such that the first high assertion of the three will set the ARQ flipflop (provided that there is no current reading of register 9, the CIO STATUS register). This action is of the edge-trigger type which means a read of register 9 will clear the ARQ flipflop regardless of the condition of the three interrupt sources. If ARQ is cleared while an interrupt source is still asserted high, a second interrupt assertion (high) does not set ARQ again.

If ARE is set (interrupt is enabled), the setting of ARQ brings the 27114B into the interrupt state. In this state, the 27114B drives the ARQ signal on the CIO bus with an open-collector gate. When polled with an attention poll, the 27114B responds via the UAD line on the backplane. Any reading of the CIO STATUS register (register 9) will clear the ARQ flipflop. The ARE flipflop is controllable via bit 0 and 1 of the CIO CONTROL register (register 1/write).

PEND INTERRUPT:

The PEND interrupt is enabled when the PEND option is selected and when the PEND INT_DIS bit is 0. Any falling edge of PEND will cause the PEND flipflop to be set. This PEND flipflop remains set until it is cleared with a 1 in the PEND RESET bit (PEND RESET is also used to disable the PEND circuit). This action of setting the PEND flipflop is independent of the ARQ flipflop. If it is the first interrupt of the three, it also sets the ARQ flipflop (if so enabled). The PEND flipflop is not affected by the CRFF bit.

ATTN INTERRUPT:

The ATTN interrupt is enabled whenever the ATTN option is selected (power up default). Any falling edge of ATTN will set the ATTN flipflop in this case. If the other two interrupt sources are not currently asserted high at that time, the ARQ flipflop is also set (if enabled). The ATTN flipflop remains set until the ATTN circuit is disabled with a 0 programmed in the ATTN OPTION bit in register B (AFI CONTROL2 register). The ATTN flipflop is provided to record the interrupt caused by the ATTN input at the frontplane of the 27114B card. This is most useful when there are multiple interrupts (for example, a short pulse is applied to the ATTN input immediately before or after another on-board interrupt occurrence. The driver should be able to detect that there is an ATTN interrupt and another on-board interrupt).

Note that the ATTN flipflop and the ARQ circuit are independent. A falling edge on the ATTN can set the ARQ flipflop regardless of the state of the ATTN flipflop. Unless the ATTN flipflop is cleared by each interrupt service routine, it is hard to tell if the current interrupt was also caused by the ATTN input if either or both PEND and the transfer counter are found to be the cause of the interrupt. This is done to allow the 27114B to be backward compatible with the 27114A. In the 27114A-compatible mode, the ATTN interrupt flipflop remains set indefinitely after the first ATTN interrupt (until a power-up or reset condition is applied to the 27114B card).

TRANSFER COUNTER INTERRUPT:

The transfer counter interrupt is enabled with the enabling of the transfer counter and the setting of the ZERO INT_DIS bit to 0. As the transfer counter counts down to 0, the Transfer counter interrupt signal is asserted high. Section 4. 3. 5 addresses the enable/disable of the transfer counter circuit. To determine if the transfer counter is a possible cause for an interrupt, bit Zero in the read register 7 (AFI STATUS register) can be inspected.

4.3.4 PEND Function

The PEND function is optional. When selected, it allows a peripheral to terminate a transfer even when the transfer's count is not a 0 yet. The PEND option on the 27114B can be selected with a 0 programmed in the PEND RESET bit of write register B (AFI CONTROL2 register). A write of 1 will reset the PEND flipflop and disable its function. The power up default state disables the PEND option.

For input transfers, the frontplane PEND signal is clocked into the FIFO as the 17th data bit (low bit). Its timing (set-up time and hold time) must satisfy the same requirements as those of the input data words. A low PEND indicates that the peripheral wants to terminate the data transfer with the current data handshake. As the input handshake is completed, the PEND flipflop is set and the frontplane handshake state machine is disabled, preventing further handshakes from happening. As the data word propagates through the FIFO, it shows up eventually at the CIO backplane. As this word is handshaked on the CIO backplane, the CIO's DEND signal is asserted low for the duration of the transfer (with respect to IO_SB of CIO) while the Burst Request circuit is deasserted high, regardless of the condition of the FIFO (it should have been deasserted anyway). The CIO channel adapter should have the same transfer count as that maintained on-board the 27114B. The 17th output from the FIFO is designed to be low true to assure that the CIO's DEND signal is asserted low only when there is an input data transfer.

For output transfers, any time a falling edge is detected on the PEND input (a transition from high to low), the PEND flipflop is set. This edge can happen any time: during or after a handshake. However, after the PEND flipflop is set, the frontplane handshake circuit is disabled. Therefore, if the edge is detected after a handshake has initiated, the handshake will go through. It is best that the peripheral changes the state of the PEND signal only immediately after a handshake has completed.

To abort the current data transfer on the CIO bus, the 27114B fakes a ready for data condition and yanks on the DEND line as the channel transfers the next word. After the next CIO data output transfer (in case there is still some room in the FIFO) or service poll, the CIO frontplane handshake state machine automatically answers positively to service polls (regardless of the condition of the FIFO) and at the same time, disables the burst request signal. As the CIO does the next output data transfer, the CIO's DEND signal is asserted low to inform the CIO channel that it should terminate the transfer. Note that the actual count maintained by the CIO channel adapter is always bigger than the count maintained by the transfer counter on-board the 27114B since there are some words left dangling in the FIFO (or being lost due to the overflow).

In both cases, the setting of the PEND flipflop can also cause the ARQ flipflop to be set if the PEND DIS_INT bit is a 0. An interrupt could be generated in this case if the ARE flipflop is also set.

Immediately after a CRFF reset, the 27114B asserts the CIO's DEND signal low with any CIO read of the data register since there is no valid data word in the FIFO. Note that the CIO channel is not supposed to do any data transfer in this case (27114B is in the input mode and the FIFO is empty). If there is valid data in the FIFO, the assertion of PEND depends on whether the PEND feature is enabled and the frontplane PEND input was asserted low for that word.

If the 27114B's output mode is selected after a reset, the PEND circuit is not asserted until a peripheral deasserts (low) the PEND input.

The driver must reset the PEND flipflop before each transaction if the PEND flipflop was set by a peripheral in the previous operation. This is particularly important to generate a PEND type interrupt and to assure a normal output transfer (output transfers will stop with the first word if the PEND flipflop is still set).

4.3.5 HEND

The HEND option of the 27114B allows the card to signal to a peripheral that the last transfer has happened (input) or is about to happen (output). The HEND circuit is enabled with the PDIR option bit found in the write register B/lower (AFI CONTROL2 register). The power up default state is that this feature is enabled.

When enabled, the output which normally corresponds to the CTL4 control bit is driven according to the state of the HEND circuit. The HEND output is driven by either the 18th data output of the FIFO or the zero count output of the transfer counter.

There is no HEND flipflop to register the fact that HEND is asserted on the frontplane (driving the peripheral). The HEND bit in the AFI STATUS register reflects the state of the HEND output.

The power-up (default) state of HEND is asserted low. This is due to the fact that the FIFO is cleared to a low level for all of its outputs. HEND is asserted high immediately with the first input transfer (when the data is shifted into the FIFO) or just prior to the availability of the first output data word (with the same set-up timing availability).

For output data transfers, as the HEND signal is asserted low on the CIO bus, a low value is also clocked into the 18th data bit of the FIFO. As this last word propagates through the FIFO and finally shows up at the frontplane, the HEND output is driven to the asserted low state. This output has the same timing as the other data outputs as far as set-up/hold time availability is concerned. Subsequently, when the transfer counter reaches zero, this circuit also drives the HEND output to its assertion state (kind of a reenforcement). The HEND output remains asserted low until the FIFO is reset and the counter is loaded

with a non-zero value. Consequently, this requires the FIFO to be reset before each output transfer starts so that the HEND output can be initialized to the non-assertion state.

For input data transfers, the HEND signal is asserted low on the frontplane immediately after the last handshake has started. As soon as the transfer counter reaches zero, HEND is asserted (immediately after the deassertion to assertion edge of the PCTL control output). HEND is normally driven by the transfer counter for input data transfers.

The HEND output remains in the low assertion state as long as the transfer counter's output is a zero. This is true in both input and output data transfer cases. Loading the transfer counter's counter with a non zero value or presetting the transfer counter will deassert the HEND output.

As a product concern, HEND may be left asserted until the next call (this is true in the case that the driver doesn't bother reloading or presetting the counter at the end of a transaction). If the peripheral expects a deasserted HEND (high), the card must be reset via a driver call first.

The assertion of HEND does not inhibit the frontplane from handshaking. In output transfer cases, this should not be a problem because the CIO has given all the data to the FIFO and all data in the FIFO has been handshaked out so there won't be any more possible handshakes, even if the peripheral wants to do so. In input transfer cases, a HEND assertion condition is normally a result of the transfer counter reaching zero. This later condition inhibits the frontplane handshake circuit. In the rare case described above where the CIO's counter is programmed with a value at least 64 less than that in the transfer counter, the card would continue to handshake as normal.

NOTE: The HEND frontplane signal is not driven in the case where the counter is not used for an input transfer; for an output transfer without the counter, the CIO channel drives HEND, and for transfers using the counter (in and out), the counter asserts HEND when the counter reaches zero and PCTL is low. HEND is asserted low prior to the first handshake of a transfer due to its remaining asserted from the end of the previous transfer; the default state of HEND after a reset or power-up is also a low assertion.

4.3.6 CEND/HEND Interaction

This section illustrates a hypothethical case of two 27114B cards being connected to each other and the effect of HEND/PEND between the two cards. 4 cases will be looked at:

SLAVE READS MORE THAN MASTER WRITES
SLAVE WRITES LESS THAN MASTER READS

Both cases are similar with the HEND/PEND timing coinciding with that of the data lines. The timing of an output device's HEND has the same set-up and hold time as the last data word and this meets the same requirement for the input device's PEND input. Both master and slave should terminate with their PCTL in the deasserted state and the correct count remainder.

SLAVE READS LESS THAN MASTER WRITES

The slave asserts its HEND low immediately after the deasserted to asserted edge of its PCTL for the last handshake. The master doesn't look at this signal (seen as PEND to it) until after the slave's PCTL goes back to the deasserted state. Both master and slave should terminate with their PCTL in the deasserted state and the correct count remainder (0 for the slave).

SLAVE WRITES MORE THAN MASTER READS

This scenario doesn't work. Since the master's HEND is asserted low at the same time as its PCTL's assertion, the slave may or may not be able to start the acknowleging cycle (due to the finite delay between PCTL and HEND). The result is that it is unknown if the master completes the handshake.

4.3.7 Transfer Counter

The transfer counter is a 24 bit counter which can count down (logically) from 0xFFFFFF to 0. The logical zero output from the counter is actually activated whenever the count is between 0 and 0x00FFFF (65535 decimal). The effective range of the counter is therefore between a maximum of 0xFFFFFF (16,777,215 decimal) and a minimum of 0x00FFFF (65535), the first value where the zero count output is activated.

Therefore, it is advisable that all counts should be made with an offset of 0x00FFFF. For example, to allow 5 transfers to go through the frontplane, a count of 5+0x00FFFF or 0x010004 must be programmed in the counter. Once this offset is used, it must be subtracted from a value read from the counter to calculate the exact remaining count.

The counter value is accessible as read/write register A (for the lower and middle bytes) and read/write register B/upper (for the upper byte). The default power up state of the counter is: the counter contains the maximum count, it is disabled, its interrupt is disabled, and its load control bit is set (to 1). This default state allows the counter to be transparent to the rest of the 27114B.

The counter has two parts: a write register which holds a value written to the counter and a counter which does the counting. The value held in the write register remains the same unless a new value is written to the transfer counter circuit. The counter part can count down or it can be loaded or reset.

The counter is controlled by three bits: Count Reset (in write register B/lower, AFI CONTROL2 register), ZERO INT_DIS and Load Count (both in write register 7, the AFI CONTROL register). A 1 programed into the Count Reset bit keeps the counter in the reset mode, inhibiting it from counting (this is also the power up default mode). A 0 programmed in the ZERO INT_DIS enables the transfer counter circuit to set the ARQ flipflop when it counts down to a value in the logical zero range (0 through 0xFFFF). The default value for this bit is a 1 (disable). The Load Count bit is used to transfer a value currently stored in the counter's write register to its actual counter (a read register). This bit has a default value of 1. Whenever this bit is a 1, the content of the actual counter is the same as the value last written to its write register. This bit should be kept at 0 for the counter to count.

The counter counts down (logically) with each deasserting-to-asserting edge of the frontplane handshake control output PCTL (a transition from a high to a low level). Upon reaching the logical zero count (set when the actual count is within the range of 0 and 0xFFFF), the transfer counter disables the frontplane handshake. By reading the contents of this counter, one can determine how many handshakes have actually happened, regardless of the current state of the FIFO. Note that in input data transfers, a logical zero count does not necessarily mean that all data words have arrived in the host's memory, just that all words have been accepted by the AFI card (some of them may still be in the FIFO). Also, in output transfers, a logical zero count doesn't mean that the FIFO is empty.

It should be noted here that due to the critical timing required by the frontplane handshake circuit, the counter is checked with the deasserting to asserting edge of the PCTL circuit, which may or may not be acknowledged already by a peripheral. Therefore, the user (driver) must take into account the current state of the PCTL circuit when determining if the actual count is one less (in the case of PCTL still being asserted) or the same as the read counter value (in the case of PCTL being deasserted).

It should also be noted that the zero count interrupt happens only when both the count is zero and PCTL is deasserted. That means an interrupt can occur only after the last handshake (with the counter equal to zero) has completed.

In both input and output cases, the HEND output (when the option is selected) is asserted low whenever the transfer counter's output is a logical zero.

The default power up value of the counter is the maximum count. It is recommended that the transfer counter be loaded or preset before each transaction.

4.3.8 State Machine

A synchronous state machine is used in the 27114B hardware to control the movement of data between the frontplane and the backplane. The state machine actually consists of two independent state machines, one for shift-in and one for shift-out.

The shift-in state machine is responsible for controlling the input of data into the FIFO. In output data transfers, it writes a data word into the FIFO every time the CIO channel writes to the data register (it is the responsibility of the CIO channel to observe the service poll result before doing so). In input data transfers, it assumes the duty of frontplane handshaking while also controlling the writing of input data into the FIFO.

The shift-out state machine controls the reading of data out of the FIFO. In output transfers, it controls the handshake circuit as data is read from the FIFO. In input transfers, it clocks a word out after each read from the data register is made by the CIO channel.

The frontplane handshake part of each of these two state machines are disabled whenever one or more of three conditions exists: the word counter's content is a zero, the PEND flipflop is set, or the frontplane is disabled.

4.3.9 Miscellaneous

There is no GPIO mode. If there was a GPIO mode, the 27114B would behave as though it had only one level of storage in the FIFO. This perhaps would simplify the interface to a non-intelligent driver. From a system level, the 27114B would behave very much like a true GPIO card if the driver were written to take advantage of the on-board transfer counter.

For output transfers, the driver should complete the call only when the frontplane handshake circuit has stopped (either because of an exhaustive count or a PEND condition) or a time-out has happened. If the count is less than 64, the driver can elect to do the data moving itself to avoid the unnecessary step of having to set up a DMA transaction for the CIO channel.

For input transfers, it can terminate the call whenever the CIO channel adapter has completed the CIO DMA transaction. If the transfer count is less than 64, the driver can also elect to do the data moving itself after the frontplane transaction has stopped.

For read/write of fixed values (like 1 word), the counter really doesn't have to be reloaded every time. This could save two writes to the card.

Behaving like this, there should not be any differentiation between the 27114B and other GPIO cards (e.g. the 27112).

There is no support for a frontplane parity option. The available but not officially supported frontplane parity feature of the 27114A was never activated or used. Physical restrictions in the layout of the 27114B prevent this feature from being implemented.

POWER UP INDICATOR:

Some customer feedbacks indicate that there is a need for an output which could be used to indicate that the card is powered up and is in a stand-by state. Such a need can easily be satisfied with the inverted output of any output control line. All control lines are powered up in the low state. Their inverted output are driven to a high state when power is applied and the reset pulse is received by the 27114B card. As long as the control output is not changed by the user's program, this is a good indicator.

4.3.10 Register Address Table

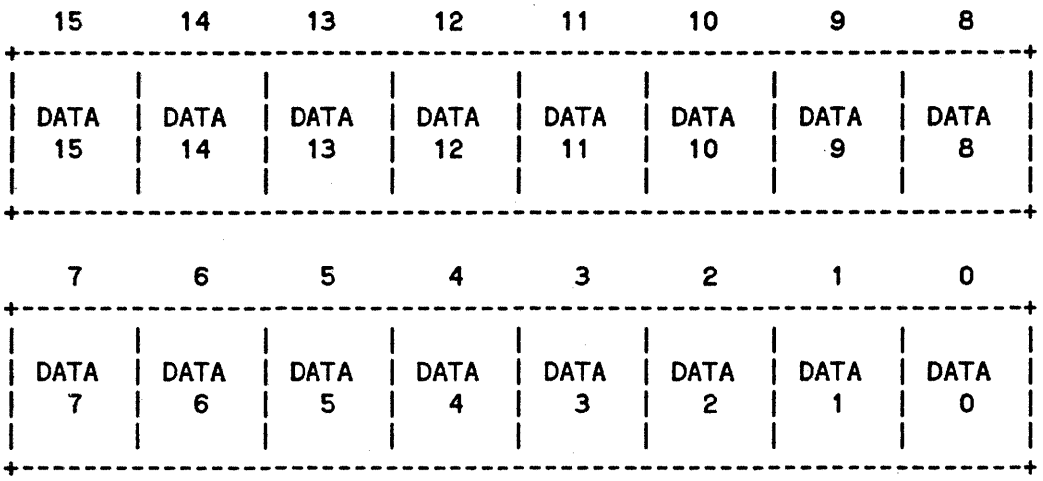
Register address table:

NOTE:
* Bit N is always less significant than bit N + 1
* When written down, a bit is always more significant than bits on its right

BP1	CBYT	CEND	BPO	REG	Function	
					Read	Write
0	X	X	0	0,2,4,6	Input data	Output data
0	0	0	1	1	Sense Reg.	CONTROL Reg.
0	0	1	1	3	I.D. Reg.	N/A
0	1	1	1	7	AFI Sta Reg	AFI Cnt Reg.
1	0	0	1	9	CIO STATUS	N/A
1	0	1	0	A	AFI Counter	AFI Counter
1	0	1	1	B	H AFI Count Low N/A	H AFI Count Low AFI Ct12

4.3.11 Register Bit Definition

Reg 0 - Read: Input Data Reg 0 - Write: Output Data



DATA REGISTER - Read or Write:

The Register 0 - Data Register is not a read/write register. Writing and reading to this register has different meanings as explained later in this chapter. This register is the only one that CIO accesses which can be bursted (more than one IO_SB [IO strobe] per sync cycle can be done).

Due to the inversion of data on the CIO bus, all data will appear in the FIFO in the inverted form. A 1 in the program domain will translate to a low level in the FIFO, causing the corresponding (+) output to be at a low level and the (-) output to be at a high level.

INPUT - Reading of register 0:

* Function/Operation:

Reading from register 0 returns 16 data bits currently available at the output of the FIFO.

If the AFI card is currently in the input mode (AFI CONTROL BIT 7 [PDIR] = 1), a shift-out pulse is sent to the FIFO; a stable data word is returned to the CIO channel. If the FIFO has at least one data word in it (its output ready is asserted), the returned data word is valid (a word which had been written to the FIFO earlier). After the read completes, the current data word will be thrown away and a new data word will be made available at the FIFO's output (if there is any others). If the FIFO is currently empty, the shift-out pulse is probably ignored (see the validity section); the returned data word is a garbage word. Note that if the FIFO is empty, the card does not respond to service polls in the input mode and therefore the channel should not access the input data register at all. Note 2: Even though the channel should not access the input data register, it is capable of doing so; of particular interest is the case of forced access by a diagnostic.

If the AFI card is currently in the output mode, there are no shift-out or shift-in pulses being sent to the FIFO. The returned word could be unstable in this case (the set up time may not be valid) since the FIFO's output is under the control of the frontplane part of the FIFO state machine. If the frontplane circuit is in a known stable state, this reading could be used to do local loopback on the AFI card.

* Validity:

The returned word is valid only if the AFI is in the input mode and the FIFO currently has a valid data word at its output. The second condition can be observed via one of two methods: CIO service poll response or AFI STATUS' OR (FIFO Output Ready) bit. The CIO service poll response from the card will be asserted if the FIFO's output is ready when the card is in the input mode and the backplane poll response enable bit is asserted (high).

The status of the FIFO is unknown if a read is made from it while its Output Ready indicates that the output is not valid: the shift-out pulse could either be ignored (normally) or counted (in case another word has just propagated to the output).

* Default value:

The AFI card is in the input mode. The FIFO is empty, and its OR is not asserted. The AFI does not respond to service polls. The FIFO's output is stable but undefined.

OUTPUT - Writing to register 0:

* Function/Operation:

Writing to register 0 will latch the output word in the latch in front of the FIFO.

If the AFI card is currently in the output mode, a shift-in pulse is sent to the FIFO. If the FIFO has room for one or more words, the latched word is clocked into the FIFO. This happens immediately after the write completes (before the next CIO channel's operation, be it another write [IO_SB], sync or poll operation). If the FIFO is full, the shift-in pulse will probably be ignored (see the validity section); the latched word would be destroyed by the next latching action.

If the AFI card is in the input mode, there will be no shift-in or shift-out pulses being sent to the FIFO.

* Validity

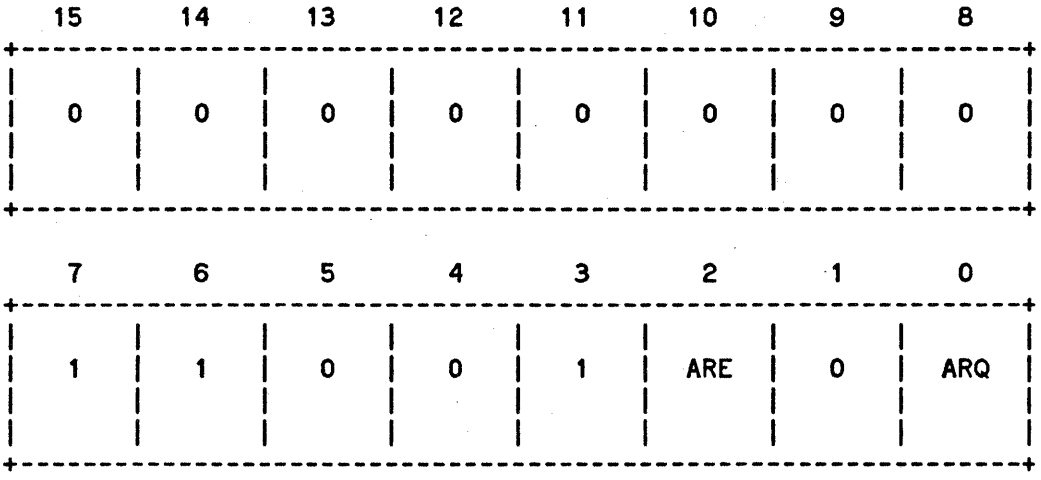
The output word is stored in the FIFO only if the AFI is in the output mode and the FIFO currently has room for a valid data word. The second condition can be observed via one of two methods: CIO service poll response or AFI STATUS' IR (FIFO Input Ready) bit. The CIO service poll response from the card will be asserted if the FIFO's input is ready when the card is in the output mode and the backplane poll response enable bit is asserted (high).

The status of the FIFO is unknown if a write is made to it while its Input Ready indicates that the FIFO is full: the shift-in pulse could either be ignored (normally) or counted (in case another location has just propagated to the input).

* Default value:

The AFI card is in the input mode. The FIFO is empty, its Input Ready is asserted (high). The AFI card does not respond to service polls.

Reg 1 - Read: CIO Sense Register



Function/Operation:

The reading of this register returns the CIO SENSE register for the AFI card. All but two bits are returned with a fixed value at all times. Bit 2, ARE, reflects the state of the Attention Request Enable flipflop. Bit 0, ARQ, indicates the state of the Attention Request flipflop. These two bits are defined as followes (as seen by the programmer):

ARE: 1 means interrupts from the AFI card are enabled
0 means interrupts are disabled

ARQ: 1 means there is a pending interrupt on the AFI card
0 means there is no pending interrupt

The AFI card drives the ARQ line on the CIO bus whenever both of these bits are 1.

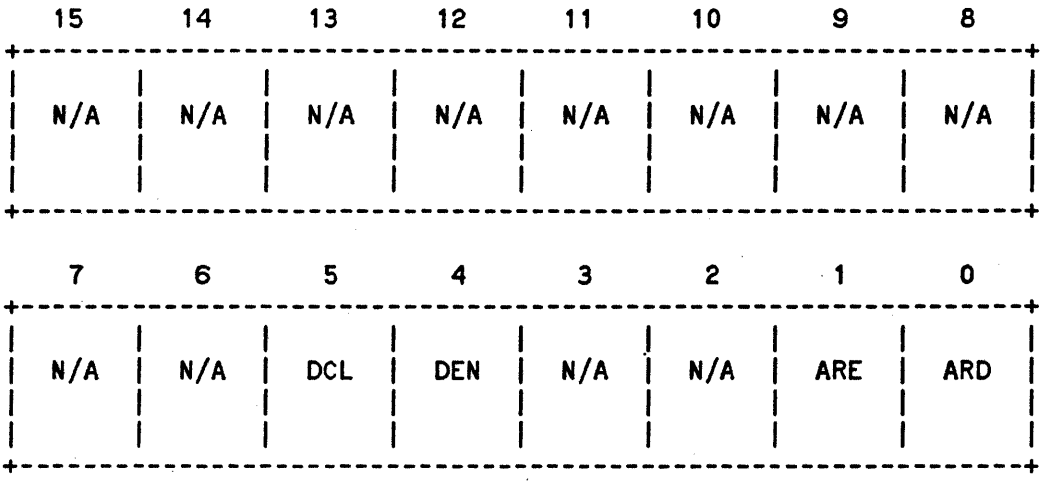
Validity:

These bits are valid at all times when the AFI card is not in the hard reset mode.

Default value:

ARE: 0
ARQ: 0

Reg 1 - Write: CIO CONTROL Register



Function:

This CIO CONTROL register defines two independent control flipflops on the AFI card: the ARE flipflop and the (soft) reset flipflop.

There are four bits: DCL, DEN and ARE, ARD.

```
DCL: A 1 written to this bit sets the (soft) Reset flipflop
     A 0 written to this bit causes no side effects.

DEN: A 1 written to this bit resets the Reset flipflop
     A 0 written to this bit causes no side effects.

ARE: A 1 written to this bit enables interrupts by setting
      the ARE flipflop
     A 0 written to this bit causes no side effects.

ARD: A 1 written to this bit disables interrupts by
      resetting the ARE flipflop.
     A 0 written to this bit causes no side effects.
```

When both DCL and DEN bits are written with 1's, the Reset flipflop will be toggled to the opposite state.

When both ARE and ARD bits are written with 1's, the ARE flipflop will be toggled to the opposite state.

Operation:

When set, the Reset flipflop resets all other circuits on the AFI card except for the ARE flipflop and the hard reset condition. The Reset flipflop can be used to preset all affected circuits to a known state (referred to in the rest of this document as the default state). The Reset flipflop must be reset before the AFI card can operate normally.

When set, the ARE flipflop enables interrupts from the AFI card. Please refer to the chapter on interrupts for the different interrupt sources available on the AFI card. When reset, the ARE flipflop disables all interrupts from the AFI card.

Validity:

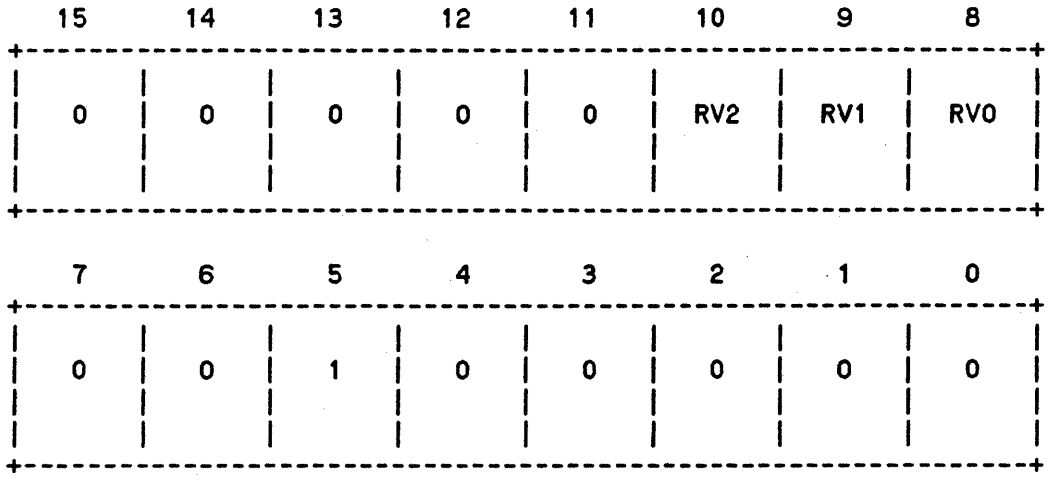
Any write to the CIO CONTROL register is valid whenever the AFI card is not in the hard reset condition.

Default (hard reset):

The Reset flipflop is set when a hard reset condition occurs (the equivalent of a DCL).

The ARE flipflop is reset when a hard reset condition occurs (the equivalent of an ARD).

Reg 3 - Read: CIO ID Register



Function:

This CIO ID register returns the card's ID and revision number.
The returned value indicates:

* The card's ID is 32 (same as the old 27114A's)
* The card's revision is programmed by 3 jumpers (S8 through S10, where S10 is the most significant)
  The 27114B must be programmed with a revision of 2 or more to differentiate it from earlier hardware versions.
  (0 and 1 are reserved for the 27114A card)
* The card does not support CIO parity generation/checking

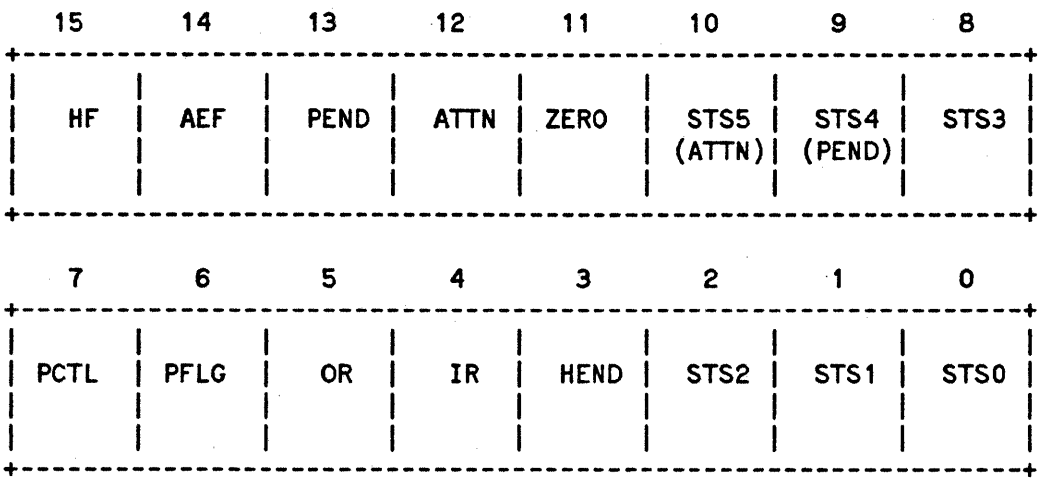
Validity:

This register is valid any time the AFI card is not in the hard reset condition.

Default:

This register does not change in normal operation. Whenever a hardware design change is significant enough, the revision number will be adjusted. The new revision number will always be larger than previous revision numbers.

Reg 7 - Read: AFI STATUS Register



Validity:

This register is valid any time the AFI card is not in the hard reset condition.

Bit 15 - HF:

HF - Half Full - indicates whether the FIFO is more or less than half full. The combination of HF and AEF reflects approximately how many words are currently in the FIFO:

HF	AEF	Words stored
0	1	0 - 8
0	0	9 - 31
1	0	32 - 55
1	1	56 - 64

Default: 0

Bit 14 - AEF:

AEF - Almost Empty/Full - indicates the near empty or near full condition of the FIFO. See bit HF.

Default: 1

Bit 13 - PEND:

PEND - Peripheral END - indicates the current state of the PEND flipflop. The PEND flipflop is set whenever the peripheral asserts the PEND input and the PEND option is enabled. The PEND flipflop is reset when the PEND option is disabled. A 1 means the PEND flipflop is set.

Default: 0

Bit 12 - ATTN:

ATTN- ATTeNtion - indicates the current state of the ATTN flipflop. The ATTN flipflop is set whenever the peripheral deasserts the ATTN input and the ATTN option is enabled. The ATTN flipflop is reset when the ATTN option is disabled. A 1 means the ATTN flipflop is set.

Default: unknown

Bit 11 - ZERO:

ZERO indiçates that the transfer counter has reached the 0 count. When the counter reaches a value in the range of zero through 0xFFFF, this bit is asserted to 0. This bit is a 1 for all other values of the counter.

Default: 1

Bit 10, 9 and 8 - STS5, STS4 and STS3:

The three status bits STS5, STS4 and STS3 are used to return the state of three inputs on the frontplane. The STS5 input is used for the ATTN interrupt circuit. Regardless of whether the ATTN option is enabled or not, this input is always reflected in bit STS5. The STS4 input is used for the PEND circuit. Regardless of whether the PEND option is enabled or not, this input is always reflected in bit STS4.

The reported value is that which was sampled by the falling (leading) edge of the sync pulse of the read action. A 0 is reported when the + input is at a voltage more positive than that of the - input (differential mode) or when the low true input is driven to a low level. The application must maintain these inputs in a steady state until after the read action is carried out. The timing between the read call and the actual read action is driver dependent.

Default: unknown value (what ever is being driven into these inputs). In case the inputs are not used and not connected to anything on the peripheral side, these bits are all 0's in case of a single ended application (for a differential application, the default unused values are unknown).

THE FOLOWING 5 BITS HAVE THE SAME MEANING AS DEFINED IN THE 27114A's ERS:

Bit 7 - PCTL:

The state of the Peripheral ConTroL output is reported in this bit position. When the PCTL output is asserted

high, a 0 is returned in this bit. A 1 in this bit indicates that the PCTL is currently deasserted low.

Bit 6 - PFLG:

The state of the Peripheral FLaG input is reported in this bit position. When the PFLG input is asserted high, a 0 is returned in this bit. A 1 in this bit indicates that the PFLG is currently deasserted low.

The value returned in this bit is independent of the value programmed in the EDGE bit of the AFI CONTROL register.

Bit 5 - OR:

The Output Ready bit indicates the state of the output of the FIFO. A 0 indicates that the FIFO's output is not valid. A 1 indicates that the FIFO's output is currently valid. Note that unless both the frontplane and backplane activities have been shut down for a while, the value returned in this bit and the IR bit can change from reading to reading.

Bit 4 - IR:

The Input Ready bit indicates the state of the input of the FIFO. A 0 indicates that the FIFO is full and cannot accept more data words. A 1 indicates that the FIFO is not full and can accept at least one more data word.

Bit 3 - HEND:

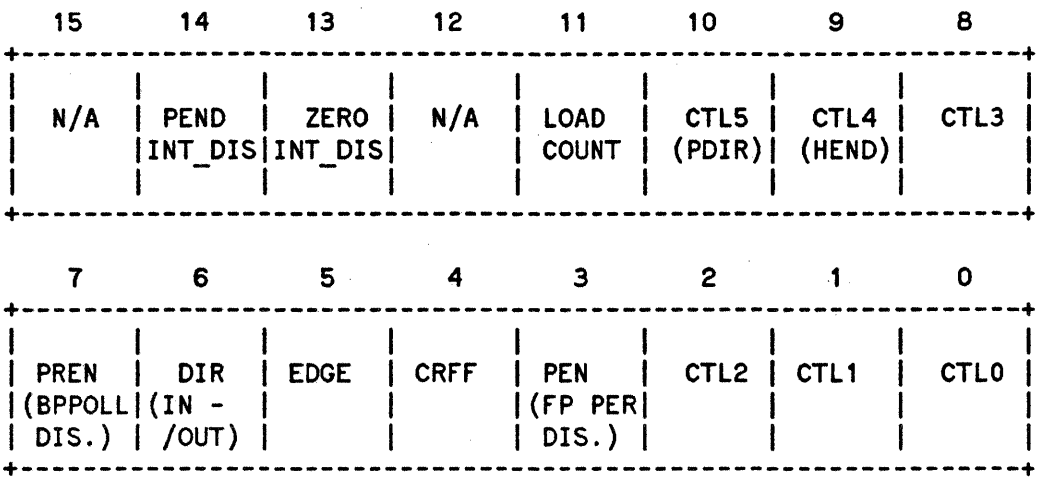
This bit reflects the current state of the HEND circuit. The HEND circuit is connected to the CTL4 output if the PDIR option is selected (default).
This bit is valid even if the PDIR option is not selected. A 1 is returned if the HEND output is currently asserted low, indicating that the transaction has ended or is about to end. A 0 is returned if the HEND output is currently not asserted.

Bit 2, 1 and 0 - STS2, STS1 and STS0:

STS2, STS1 and STS0 are status bits. These bits reflect the state of the related inputs at the frontplane. The reported value is that which was sampled by the falling (leading) edge of the sync pulse of the read action. A 0 is reported when the + input is at a voltage more positive than that of the - input (differential mode) or when the low true input is driven to a low level.

Default: unknown value (what ever is being driven into these inputs).

Reg 7 - Write: AFI CONTROL Register



Validity:

This register is valid any time the AFI card is not in the hard reset mode. Care must be taken not to disturb some of these bits as noted below in their descriptions.

Default value:

All bits in this register have a default value of 1.

Function:

Bit 15 - N/A:

Not used

Bit 14 - PEND INT_DIS:

This bit is used to enable/disable the PEND interrupt option. A 1 programmed in this bit disables the PEND interrupt. A 0 programmed in this bit enables the PEND interrupt. Any value programmed in this bit does not change the state of the PEND flipflop.

If the PEND flipflop is set and a 0 is programmed in this bit, the ARQ flipflop is set. If the ARE flipflop is also set, the card asserts the ARQ line on the CIO backplane and also responds to CIO Attention Request polls.

Bit 13 - ZERO INT_DIS:

This bit is used to enable/disable the Zero word count interrupt option. A 1 programmed in this bit disables the Zero

word count interrupt. A 0 programmed in this bit enables the Zero word count interrupt. Any value programmed in this bit does not change the state of the transfer counter.

If the transfer counter indicates a word count of zero and a 0 is programmed in this bit, the ARQ flipflop is set. If the ARE flipflop is also set, the card asserts the ARQ line on the CIO backplane and also responds to CIO Attention Request polls.

Bit 12 - NA:

Not used.

Bit 11 - LOAD COUNTER:

This bit is used to load the transfer counter. The transfer counter consists of two parts: a register and a counter. The register part is writeable as write register A and B (part of B). The counter part is readable as register A and B. The counter part is controlled by three inputs: a load input (this LOAD COUNTER bit), a reset input (see register B) and a clocking source (internal to on card hardware). As this bit is a 1 and the counter is not reset, the current content of the register part is transferred to the counter's output. This makes the counter a read/writeable register. The counter cannot count in this case. This bit should be programmed with a 0 for normal operation.

This bit should not be changed while there is the possibility of a handshake being conducted at the frontplane. If this rule is violated, the contents of the counter is unknown (it could be the newly programmed value or that plus one or something else).

Bit 10, 9 and 8 - CTL5, CTL4 and CTL3:

These three bits are used to control three respective frontplane outputs. When a 1 is written to a bit, its corresponding + output will be at a lower voltage than its corresponding - output.

The output for bit CTL5 is shared with the PDIR output function as defined by the PDIR Output Option bit (in register B).

The output for bit CTL4 is shared with the HEND output as defined by the PDIR option.

The output for bit CTL3 is not shared.

THE FOLLOWING 5 BITS HAVE THE SAME MEANINGS AS DEFINED IN THE 27114A's ERS:

Bit 7 - PREN:

The Poll Response ENable (more appropriately, Poll response disable) bit is used to disable responses to CIO's service polls. When this bit is set to a 1 (default), all service polls will be answered negatively (there is no low assertion of the UAD line). When this bit is programmed with a 0, CIO backplane poll response is enabled. The 27114B would drives the UAD line to a low state if it is capable of sourcing or sinking a data transfer (the direction of transfer is implied in prior arrangements between the three parties: host/CIO/card)

Note that CIO data transfers to/from the FIFO are not affected by the absence of service poll responses. The channel can be forced to do data transfers as direct register accesses.

Bit 6 - DIR:

The DIRection bit is used to define the direction of data transfer in the 27114B hardware. This bit controls the operation of the FIFO and its controller, the state machine. A 1 programmed in this bit (default) defines the direction of transfer as the input mode. A 0 defines the output transfer mode.

Bit 5 - EDGE:

The EDGE bit is used to select which edge or level of the PFLG input is to be used by the handshake state machine. A 1 programmed in this bit (default value) selects the assertion-to-deassertion (falling or busy-to-ready) edge of PFLG as the triggering edge in the case of the FIFO handshake mode. In the full handshake modes, a 1 selects the low level of PFLG as the assertion (busy) level. A 0 selects the rising edge of PFLG for the FIFO mode and the high level of PFLG as the assertion (busy) level in the other handshake modes. Please refer to 5.5.2 for a complete explanation of PFLG (as far as the activating edge is concerned).

With a direct connection of PCTL to PFLG (as in the case of the 27114 loopback testhood), the EDGE bit must be a 0 (non-default value) for automatic handshaking to take place.

Bit 4 - CRFF:

The CleaR FiFo bit is used to reset the FIFO and the state machine circuit.

It does not affect the ARE interrupt enable flipflop, the interrupt circuits (ARQ, PEND, ATTN) or the counter. These have their own reset control bits.

A 1 programmed in this bit resets the FIFO and the state machine (default state). A 0 must be programmed in this bit before the FIFO and the state machine can operate normally.

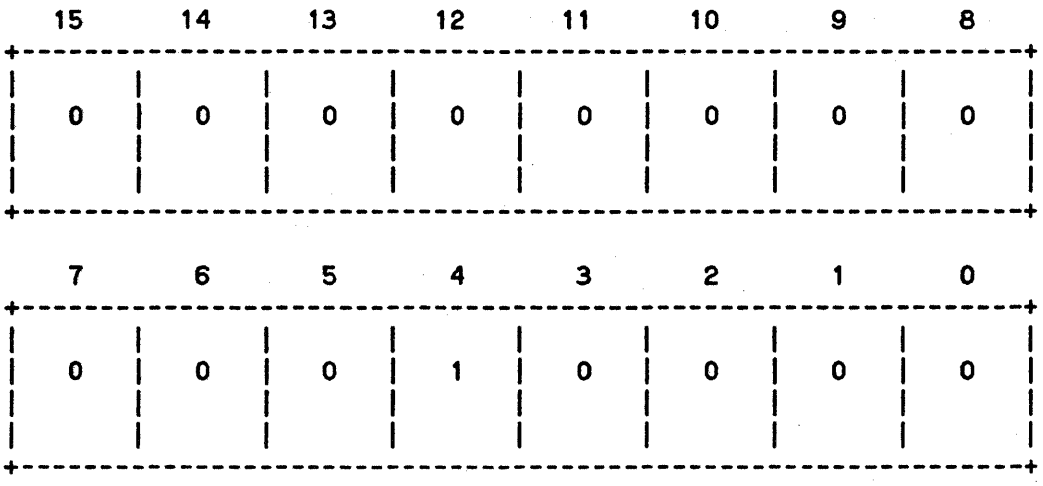
Bit 3 - PEN:

The Peripheral ENable bit (or more appropriately, peripheral disable bit) is used to disable the frontplane interface. A 1 programmed in this bit (default value) disables the frontplane interface. A 0 programmed in this bit will enable the frontplane. If a handshake has already started, the disabling of the frontplane does not take effect until the end of the current handshake. Note that the frontplane line drivers are normally disabled (tri-stated) by this bit as soon as the bit becomes a 1.

Bit 2, 1 and 0 - CTL2, CTL1 and CTL0:

These three bits are used to control three respective frontplane outputs. When a 1 is written to a bit, its corresponding + output will be at a lower voltage than its corresponding - output.

Reg 9 - Read: CIO STATUS Register



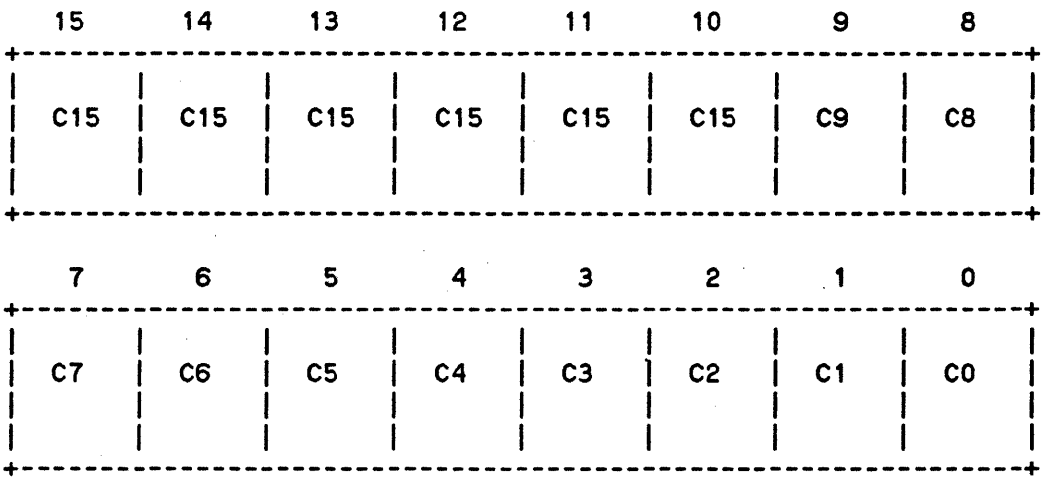
Function:

This is a register architected by the CIO standard. It contains a fixed value at all times (0x0010). Reading this register clears any pending ARQ (Attention Request) condition on the 27114B card.

Validity:

This register is valid any time the AFI card is not in the hard reset condition.

Reg A - Read: AFI COUNTER-LM Register



Function:

A read of this register returns the middle and lower bytes of the transfer counter. The upper byte of the transfer counter is contained in the upper half of register B.

The transfer counter consists of two parts: a register and a counter. A write to the counter (register A and B's upper) updates the value stored in the write register, but the content of the counter is not changed (unless the LOAD bit is currently a 1). A Load Counter action must be done to load the contents of the register into the counter (see the description of the Load Counter bit in register 7 write, CIO CONTROL register). When the counter counts down, the content of the register is preserved. A read from the counter (register A and B's upper) would return the current value of the counter.

A single output from the transfer counter is used to enable/disable the frontplane handshake circuit and to send an ARQ interrupt to the host. This output is asserted to indicate a logical zero whenever the count in the transfer counter is equal or less than 65535 (0xFFFF). This is equivalent to all counts which have the upper byte being a 0 or whenever the read register B-upper is a 0. It is suggested that an offset of 65535 be added to all counts such that the logical zero count is equivalent to an actual count of 65535.

When enabled, the counter counts down from a preset value with each rising edge of the PCTL frontplane output (before a potential acknowledgement from a peripheral). The transfer counter is disabled with any of the following conditions:

* When the PEND flipflop is set (indirectly via the blocking of the PCTL clock)
* When the COUNTER RESET bit (Register B - write) is a 1
* When the frontplane handshake disable bit (PEN - Register 7 - write) is a 1 (indirectly via the blocking of the PCTL clock)

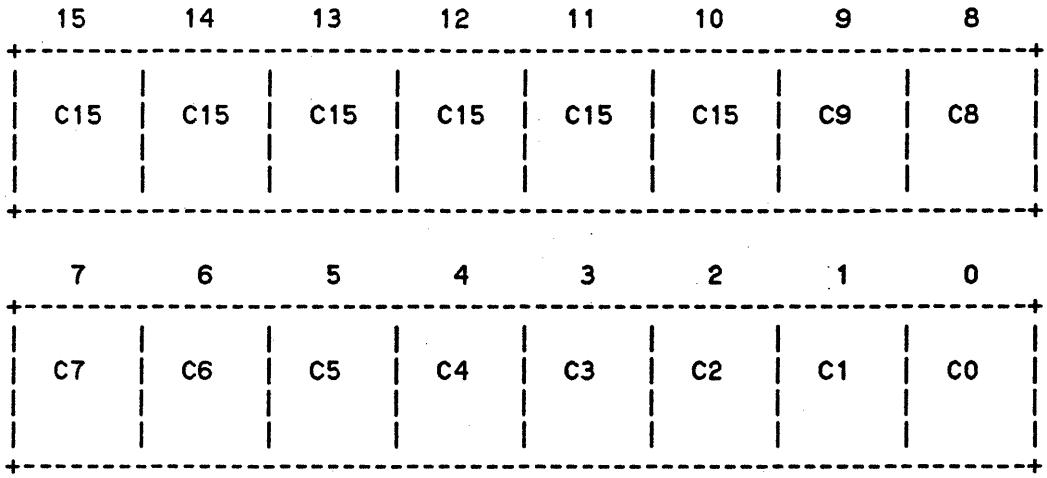
Validity:

This register is valid any time the AFI card is not in a hard reset condition and the card is not actually engaged in any frontplane transaction. If the card is counting down while this register is being read, the output is undetermined.

Default value:

0xFFFF.

Reg A - Write: AFI COUNTER-LM Register



Function:

A write to this register loads a value into the middle and lower bytes of the register part of the transfer counter. Please refer to the section on read register A for a description of the transfer counter.

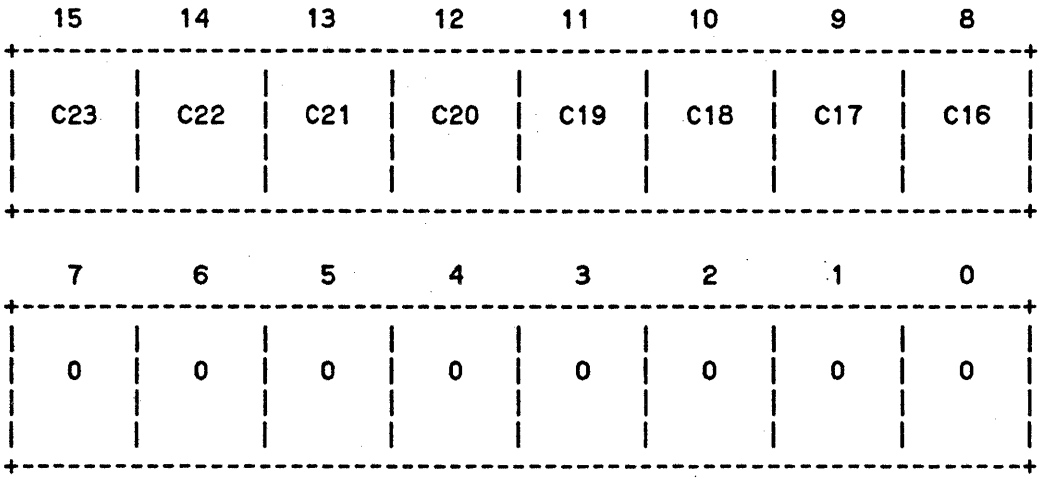
Validity:

A write can be made to this register any time the AFI card is not in a hard reset condition.

Default:

The counter is loaded with 0xFFFF.

Reg B - Read: AFI COUNTER-H Register



This register returns the upper byte of the transfer counter. Please refer to register A - read for more information on the transfer counter and its operation. The logical zero count output is asserted whenever the count in this upper byte is 0, regardless of the current count in the middle and lower bytes.

Default:

0xFF00.

Reg B - Write: AFI COUNTER-H Register/AFI CONTROL2 Register

15	14	13	12	11	10	9	8
C23	C22	C21	C20	C19	C18	C17	C16

7	6	5	4	3	2	1	0
ATTN OPT. ENA	PDIR OPT. ENA	COUNT RESET	PEND RESET	N.A.	MODE2	MODE1	MODE0

This register has two parts: AFI COUNTER-H and AFI CONTROL2.

For the AFI COUNTER-H part, please refer to the register
A - write. Its default value is all 1's.

For bit 7 through 0, the description follows:

Default for bit 7 through 0: all 1's.

Bit 7 - ATTN OPTION ENABLE:

The ATTeNtion OPTION ENABLE bit enables/disables the ATTN interrupt flipflop. A 1 written to this enables the ATTN flipflop such that it could be triggered by the ATTN input on the frontplane (default). A 0 disables the interrupt flipflop by resetting it. As long as a 0 is programmed in this bit, the ATTN flipflop stays in the reset state.

The ATTN interrupt cannot be masked otherwise: if an event happens on the frontplane input and the ATTN flipflop is held in the reset state, the event is lost. Only events which happen while the ATTN flipflop is not reset can result in an interrupt pending. An interrupt pending can be translated to a CIO interrupt if the ARE flipflop is set.

Bit 6 - PDIR OPTION ENABLE:

The PDIR option is used to enable/disable the PDIR and HEND option.

PDIR OPTION:

The Peripheral DIRection OPTION ENABLE bit defines whether the CTL5 output at the frontplane is driven with the

information in the DIR bit (of register 7-write) or with the information programmed in bit CTL5 (of register 7-write).

A 1 programmed in this bit selects the DIR bit option. Whenever the DIR bit is programmed with a 1 for input data transfers, the corresponding + output is at a lesser voltage than the - output of that signal.

A 0 programmed in this bit selects the CTL5 bit option. Please refer to register 7-write for the use of this bit and the polarity of the output.

HEND OPTION:

When a 1 is written to this bit, the HEND option is selected. When a 0 is written to this bit, the HEND option is disabled.

When the HEND option is enabled, the frontplane output related to control bit CTL4 is redefined as the HEND output. Otherwise, this output reflects the value as programmed in bit CTL4 of register 7-write.

When enabled, the HEND output is asserted low (the + output is at a less positive voltage than the - output) whenever the last output word is being handshaked out or after the last input word has been handshaked in (counter is zero).

The state of the HEND output is reported via bit HEND in the AFI STATUS register (bit 3).

Bit 5 - COUNTER RESET:

The COUNTER RESET bit is used to reset the transfer counter (the counter part only).
A 1 programmed in this bit resets and keeps the counter in the reset state (disabled state). A 0 enables the counter to count down. The counter is preset to 0xFFFFFF after a reset. The contents of the counter's write register is 0xFFFFFF at power-up and after any reset.

Bit 4 - PEND RESET:

The PEND RESET bit is used to reset the PEND flipflop. A 1 programmed in this bit resets and keeps the PEND flipflop in the reset state, therefore disabling its function. A 0 programmed in this bit enables the PEND function.

When enabled, the PEND function allows the assertion of the PEND input at the frontplane to terminate the data transfer on the CIO side. The PEND flipflop is set whenever this event happens. Depending on the setting of the PEND INT_DIS bit and the ARE flipflop, an interrupt could be sent to the CIO channel.

As the PEND flipflop is set, frontplane handshakes are disabled.

In input transfers, a 17th bit of the FIFO is set whenever an input word is handshaked in with the PEND input asserted. As the word is presented at the CIO side, the CIO's DEND line is asserted with the word's transfer. This signals the CIO's DMA controller to terminate the transfer, regardless of what the DMA counter is at.

In output transfers, the setting of the PEND flipflop forces the CIO poll response circuit to answer positively to any CIO service polls, faking the condition that the card is ready for more data to transfer. This is done regardless of the state of the FIFO. As the next transfer is done by the CIO, PEND is asserted on the CIO to indicate that the AFI card wants to terminate the CIO DMA operation. The actual number of frontplane handshakes should be deducted from the current count in the transfer counter and the original count.

Bit 3: N.A.

Bit 2, 1 and 0 - MODE2, MODE1 and MODE 0:

These three mode bits are used to define the frontplane handshake modes as follow:

M2	M1	M0	Handshake mode
1	1	1	FIFO, master
1	1	0	Full, master
1	0	0	Full, slave

All other values are reserved and must not be used. The card may not function if a reserved value is used.

These mode bits must not be changed unless the frontplane handshake circuit is disabled

4.4 FRONT-PLANE SPECIFICATION

4.4.1 Point of Reference

It should not be understated as to the importance of how the frontplane specifications are done. The user must clearly understand the obligation on their part and the availability on HP's part as far as how the 27114B hardware product (the combination of PCA and cable) can perform in their application environment.

The 27114B will be specified with the following cable options:

* For single-ended applications, the 3 m 47-twisted pair cable
* For differential applications, both the 3 m and 12 m 47-twisted pair cables.

4.4.2 General Observations

RFI grounding requirement and unintentional interference:

*** TO BE SUPPLIED ***

Limitation and HP's responsibility

*** TO BE SUPPLIED ***

Importance of short ground paths: shielding and logical grounds

*** TO BE SUPPLIED ***

Relationship between signal quality and impedance mismatch

*** TO BE SUPPLIED ***

Ground loop effects

*** TO BE SUPPLIED ***

Ground current due to shift in reference voltages: its noise effects.

*** TO BE SUPPLIED ***

Cross-coupled noise.

*** TO BE SUPPLIED ***

Helpful hints for a practical peripheral connection

*** TO BE SUPPLIED ***

Trade-offs between single-ended and differential connections

*** TO BE SUPPLIED ***

4.4.3 Electrical Specification

4.4.3.1 REQUIREMNETS.

SHIELDING TERMINATION REQUIREMENT:

The outer shield of the 27114B cable can be accessed via two methods: the drain wire and the "rook".

It is recommended that the drain wire be grounded to the nearest chassis ground on the user's peripheral via a high pass connection. It is also recommended that the "rook" be grounded to the most massive ground block on the user's peripheral for good RFI performance, also via a high pass filter.

```
**********************************************************
*          IMPORTANT SAFETY NOTE:                        *
*                                                        *
*The user must insulate the exposed rook in his/her      *
*final application environment.  If this step is not     *
*taken, there will be a safety hazard condition in       *
*the installation.  A typical example is if line         *
*voltage comes into contact with the unprotected         *
*rook at the peripheral end.  If this is the case,       *
*the entire shield is energized and could be fatal       *
*to anyone/thing who/which is currently in contact       *
*with the shield, directly or indirectly by touching     *
*the rook at the other end or the 27114B card or the     *
*host system which houses the card.                      *
**********************************************************
```

The use of high-pass filters will help in draining some of the high frequency current off the outer jacket of the cable. A direct connection sometimes works, but care must be taken to assure that there is no excessive potential between the peripheral's ground and the 27114B's host's ground.

LINE TERMINATION REQUIREMENT, SINGLE-ENDED:

Each output from the 27114B used in the single-ended mode must be terminated with a voltage divider having a parallel equivalent resistance of approximately 132 ohms. This voltage divider must provide a

Thevenin equivalent output of not less than 3 Volts but not more than 5 volts. It is required that the voltage

divider must be able to dissipate the full power applied when its output is shorted to ground.

LINE TERMINATION REQUIREMENT, DIFFERENTIAL:

Each +/- pair of signals output from the 27114B must be terminated at the user's end as close to their receiver as possible with a termination resistor between the two lines. The value of the termination resistor must be approximately 120 ohms (+/- 10 %).

GROUND RETURN REQUIREMENT, SINGLE-ENDED:

To minimize cross-coupled noise between data lines and control lines and between themselves, the 47-twisted pair cable must be used. Each of the 46 signals will be carried by one conductor of a pair. The 47th pair is used exclusively for grounding. The corresponding conductor of that pair is used for ground return for that signal. It is extremely important for the user to maintain this approach between the end of the 27114B cable and their line driver/receivers. It is recommended that the individual ground return lines be connected to the ground pin of the respective driver/receiver packs. A possible alternative is to connect these wire to a suitable, isolated ground plane which carries only these ground return currents and no other currents. The use of the 27114-63002 single-ended cables is not recommended for this 27114B card due to the lack of ground return conductors.

TRUE BALANCED DIFFERENTIAL:

The 27114B implements a line termination design such that the complementing signal currents for any one signal is always equal in amplitude. This design allows no current to flow through the ground connection. The end result is that there is absolutely no shifting of reference voltage when any or all signals change states. The same cannot be said for many so called "differential" interfaces (such as SCSI) where the differential mode is not necessarily a balanced interface mode (a large amount of ground current is allowed when signals change states).

GROUND RETURN REQUIREMENT, DIFFERENTIAL:

Even though there is no ground current resulting from the use of true balanced differential signals, there is always a small amount of potential difference between the ground planes of the two interconnecting device. To provide an escape valve for this ground differential, two conductors are provided in the differential cable.

The two conductors available in the 47-twisted pair 27114B cable must be grounded to the ground plane of the user's peripheral, as close as possible to the line driver/receiver group. This should be sufficient in most applications since the shield of the cable can also act as an alternate route to carry any differential ground current (this is not recommended however since the RFI radiation from the system will increase significantly).

In the event that these two ground lines are insufficient, the user has the option of converting some of the differential signals to single-ended signals or to eliminate them altogether. The conversion or elimination can be done by repositioning the appropriate jumper block(s). Each jumper block will affect 6 or 8 signals, depending on the block. By conversion from differential to single-ended, each block will add an extra 8 ground lines. By elimination, each block will add 16 ground lines. Signals to be considered are: output data in input only application (and vice versa), control/status input/outputs (these signals are more static by their nature), upper/lower bytes of data in 8 bit applications, etc...

GROUND SHIFT VOLTAGE DIFFERNTIAL REQUIREMENT:

Upper limit: 100 mV max (TO BE VERIFIED)

The specified common mode voltage should be measured between the two frontplane ground planes of the 27114B and the user's peripheral. This measurement should be done when there are no data transfers between the two units.

NOTE:

The actual limit is much lower than this and is dependent on other factors:

* The derated value should be sufficiently less than 7 V.

* The capability of the receiver used in the user's peripheral as far as common mode voltage rejection is concerned.

* The ability to carry the ground current due to the ground voltage differential. Normally this is carried by both the 27114B's cable and the system's ground distribution circuit. The shield and the 2 conductors available in the 27114B cable will not carry more than 0.5 A ********** CHECK THIS NUMBER ********** of ground differential current without being physically burned out (each ground wire in the 27114B cable is of 30 AWG size and can carry 0.5 A current).

IMPEDANCE CONTINUITY REQUIREMENTS:

To assure a reliable connection, the user must maintain the continuity of impedance matching in both the output and input data buses. All connections must be made as short as possible. All intermediate cabling between the 27114B's cable and the user's line driver/receivers must be as short as possible.

DRIVE CAPABILITY REQUIREMENT:

Signal Description	Value Min	Typ	Max
Absolute, 3 m cable (single-ended output, + or -)	*** TO BE SUPPLIED ***		
Differential, 3 m cable	*** TO BE SUPPLIED ***		
Absolute, 12 m cable (single-ended output, + or -)	*** TO BE SUPPLIED ***		
Differential, 12 m cable	*** TO BE SUPPLIED ***		

Table 4.4.3.1. Minimal input voltage (required)

4.4.3.2 OUTPUT/INPUT SPECIFICATION.

This section describes the electrical specification which the 27114B presents to a peripheral.

Signal Description	Value Min	Typ	Max
Absolute, 3 m cable (single-ended output, + or -)	*** TO BE SUPPLIED ***		
Differential, 3 m cable	*** TO BE SUPPLIED ***		
Absolute, 12 m cable (single-ended output, + or -)	*** TO BE SUPPLIED ***		
Differential, 12 m cable	*** TO BE SUPPLIED ***		

Table 4.4.3.2.1 Minimal output voltage (available)

Signal Description	Value Min	Typ	Max
Absolute, 3 m cable (single-ended output, + or -)	*** TO BE SUPPLIED ***		
Differential, 3 m cable	*** TO BE SUPPLIED ***		
Absolute, 12 m cable (single-ended output, + or -)	*** TO BE SUPPLIED ***		
Differential, 12 m cable	*** TO BE SUPPLIED ***		

Table 4.4.3.2.3 Equivalent input impedance (available)

Input default state when peripherals are not connected or powered off.

*** TO BE VERIFIED ***

The 27114B will exhibit a high impedance load for its input receiver when power is not applied to the card.

*** TO BE VERIFIED (high input impedance) ***

The 27114B's line drivers will appear as a high impedance load when power is not applied to the card. The line drivers are not guaranteed not to spike when power is first applied to the card or when power is removed.

The peripheral must not be confused when the 27114B's power is turned off in the case when it drives its outputs to either a high or a low state (especially in the case of single-ended applications).

4.4.3.3 LINE TERMINATION.

The 27114B provides line termination for each of its input lines. This is done to minimize the reflection at the receivers' inputs. The 27114B supports both balanced and unbalanced interfaces.

In the balanced mode (differential line), the line termination includes 120 ohm resistors connecting each (+) input to a corresponding (-) input. These termination resistors are housed in 3 DIP chips. Each chip has 8 resistors. Each resistor can dissipate 218 mW. The maximum stable input differential voltage (pin to pin) must not exceed 4.6 Volts RMS to meet this heat dissipation requirement. The part number for the DIPs is 1810-0964.

In the unbalanced (single-ended) mode, each input line is terminated with a voltage divider consisting of two resistors, 220 ohms and 330 ohms. The voltage divider forms a Thevenin equivalent circuit of 3 Volts and 132 ohms. Each voltage divider can dissipate 250 mW. Since the maximum power that can be dissipated in the divider is around 114 mW, the substitution of 125 mW voltage dividers for the 250 mW units is acceptable (but not recommended for reliability reasons). The voltage dividers are housed in 10 pin SIPs; each SIP contains 8 voltage dividers. The part number for the SIPs is 1810-0677.

To provide a stable bias for the unused input in the case of unbalanced operation mode, a different type of voltage divider is used to supply a reference voltage of 1.56 volts. These voltage dividers are also housed in SIPs with 8 of them per pack. The value of the individual resistors are 1.5 Kohms and 3.3 Kohms. The part number for these SIPs is 1810-0906.

The above DIPs and SIPs are socketed in three 20 pin DIP sockets. Pins 1 and 20 of the sockets are connected to VCC. Pins 10 and 11 of the sockets are connected to GRD. The other 16 pins are connected to the (+) and (-) inputs of 8 receivers. They are arranged such that pins 2 through 9 go to the non-inverted inputs and pins 12 through 19 go to the inverted inputs. Opposing pins (2 and 19, 3 and 18 etc...) go to the same receiver. Note that the third socket supports only 7 receivers.

For a balanced mode input configuration, the DIPs are installed such that pin 1 is lined up to pin 2 of the socket. As such, each of the DIPs 8 resistors will bridge both inputs of a receiver. When configured in an unbalanced mode (either high true or low true), the DIPs must be removed and replaced with the SIPs. The DIPs are replaced with 3 termination load SIPs (1810-0677) and 3 reference SIPs (1810-0906). The load SIPs must be positioned on the side of the socket which corresponds to the low true or high true configuration.

For low-true single-ended applications, the load SIPs must be positioned on the inverted input side (pins 12 through 19) with pin 1 connected to VCC (pin 20 of the socket). Likewise, for high-true single-ended applications, the load SIPs must be positioned such that pin 1 is in pin 1 of the socket. Done in this way, each output of the load SIP should be at approximately 3.0 volts.

The reference SIPs must be installed in the other rail of each socket such that pin 1 of the SIPs go to either pin 1 or 20 of the sockets, whichever one that does not already have a load SIP installed. Done in this way, each output of the reference SIP should be at approximately 1.56 volts.

4.4.3.4 SOFT ERROR RATE.

Environment for the specification of the soft error rate and mean and distribution variances for the soft error rate using the following cables:

*** TO BE SUPPLIED ***

Single-ended cable, 3m length
Differential cable, 3m length
Differential cable, 12m length

NOTE: experiments will be performed to define these parameters. It should be made clear to the users that these are the observed results and HP is not going to guarantee that duplicated results can be seen in the user environment. Ideally, these soft error rates should be at least an order of magnitude better than those of a high density DRAM chip (1 Mbit chip?).

4.4.3.5 OUTPUT ENABLE.

All line drivers are enabled only when the 27114B is in the output mode and the frontplane handshake is enabled (as controlled by the PDIR and PEN bits in the AFI Control register). The line drivers can remain enabled even after the handshake circuit is disabled either because of a PEND or the counter having a zero count.

The line drivers are disabled in the data input mode at all times.

The above description is reversed whenever the testhood is used. With the testhood installed, the line drivers are enabled at all time unless the 27114B is in the output mode with the PEN bit clear to 0. This allows loopback testing via the testhood to be performed.

4.4.3.6 BI-DIRECTIONAL DATA BUS.

Since the frontplane data drivers are enabled only when the 27114B talks, it is theoretically possible to join the input and output data buses at the peripheral side. This is not recommended since there is no line termination done at the output of the line drivers.

If such a bidirectional bus is used, there will be unavoidable reflection at the output of the drivers (an open circuit). This works only if substantial set up time is given to input data (driven by the peripheral). The total set up time should be in the order of 2 to 3 time that of the time it takes the signal to travel the length of the cable. Note that the 27114B circuit has about 100 ns input data set up time already built into its frontplane handshake circuit. Output data should not be affected if the peripheral appears as a high input impedance load on the bus since it is terminated at the other end.

Other factors which should be considered in this case are:

* Additional exposure to cross-coupled noise

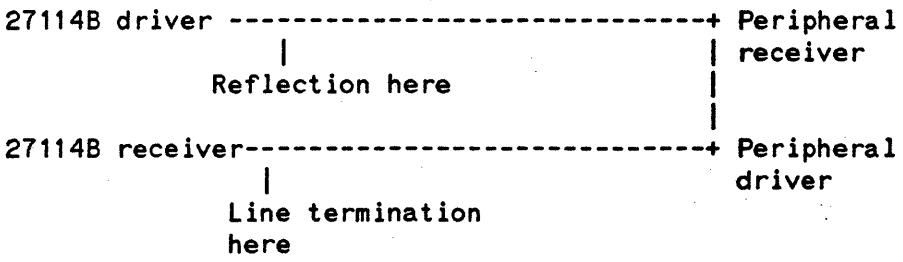


FIGURE: Bi-directional bus configuration

A**** LEVEL1 ****

4.5 FRONT-PLANE CONNECTOR PIN-OUT

4.5.1 Option's Pin-out

Depending on the option selected, the following table illustrates the dual function of 4 frontplane signals

Default	Option	selected with
ATTN	STS5	No ATTN Option
STS4	PEND	PEND Option
PDIR	CTL5	No PDIR Option
HEND	CTL4	No PDIR Option

4.5.2 Differential: By Signal Names

Signal Name	FP Pin #	Per Pin #	In/Out
SD0+	C02	C01	O
SD0-	B01	A01	O
SD1+	C04	C03	O
SD1-	B03	A03	O
SD2+	B05	C05	O
SD2-	C06	A05	O
SD3+	C08	C07	O
SD3-	B07	A07	O
SD4+	B09	C09	O
SD4-	C10	A09	O
SD5+	C12	C11	O
SD5-	B11	A11	O
SD6+	B13	C13	O
SD6-	C14	A13	O
SD7+	C16	C15	O
SD7-	B15	A15	O
SD8+	B17	A17	O
SD8-	C18	C17	O
SD9+	C21	A19	O
SD9-	A21	C19	O
SDA+	B21	C20	O
SDA-	C22	B19	O
SDB+	B23	A23	O
SDB-	C24	C23	O
SDC+	B25	A25	O
SDC-	C26	C25	O
SDD+	C28	A27	O
SDD-	B27	C27	O
SDE+	B29	A29	O
SDE-	C30	C29	O
SDF+	C32	A31	O
SDF-	B31	C31	O

Table 4.5.2. (1 of 3) Signal names to FP/Peripheral pins Differential

Signal Name	FP Pin #	Per Pin #	In/Out
RD0+	C01	C02	I
RD0-	A01	B01	I
RD1+	C03	C04	I
RD1-	A03	B03	I
RD2+	C05	B05	I
RD2-	A05	C06	I
RD3+	C07	C08	I
RD3-	A07	B07	I
RD4+	C09	B09	I
RD4-	A09	C10	I
RD5+	C11	C12	I
RD5-	A11	B11	I
RD6+	C13	B13	I
RD6-	A13	C14	I
RD7+	C15	C16	I
RD7-	A15	B15	I
RD8+	A17	B17	I
RD8-	C17	C18	I
RD9+	A19	C21	I
RD9-	C19	A21	I
RDA+	C20	B21	I
RDA-	B19	C22	I
RDB+	A23	B23	I
RDB-	C23	C24	I
RDC+	A25	B25	I
RDC-	C25	C26	I
RDD+	A27	C28	I
RDD-	C27	B27	I
RDE+	A29	B29	I
RDE-	C29	C30	I
RDF+	A31	C32	I
RDF-	C31	B31	I

Table 4.5.2. (2 of 3) Signal names to FP/Peripheral pins
Differential

Signal Name	FP Pin #	Per Pin #	In/Out
GND	A20	B20	
GND	B20	A20	
SHIELD	A10	A10	
N.C.	B10	B10	
CTL0+	A24	A16	O
CTL0-	B24	B16	O
CTL1+	A26	B18	O
CTL1-	B26	A18	O
CTL2+	B28	A30	O
CTL2-	A28	B30	O
CTL3+	A04	B02	O
CTL3-	B04	A02	O
HEND/CTL4+	B08	A06	O
HEND/CTL4-	A08	B06	O
PDIR/CTL5+	B32	A12	O
PDIR/CTL5-	A32	B12	O
PCTL+	B22	B14	O
PCTL-	A22	A14	O
STS0+	A16	A24	I
STS0-	B16	B24	I
STS1+	B18	A26	I
STS1-	A18	B26	I
STS2+	A12	B32	I
STS2-	B12	A32	I
STS3+	B02	A04	I
STS3-	A02	B04	I
STS4/PEND+	A06	B08	I
STS4/PEND-	B06	A08	I
ATTN/STS5+	A30	B28	I
ATTN/STS5-	B30	A28	I
PFLG+	B14	B22	I
PFLG-	A14	A22	I

Table 4.5.2. (3 of 3) Signal names to FP/Peripheral pins
Differential

4.5.3 Differential: By Front-Plane pins

FP Pin #	Per Pin #	Signal Name	In/Out
A01	B01	RD0-	I
A02	B04	STS3-	I
A03	B03	RD1-	I
A04	B02	CTL3+	O
A05	C06	RD2-	I
A06	B08	STS4/PEND+	I
A07	B07	RD3-	I
A08	B06	HEND/CTL4-	O
A09	C10	RD4-	I
A10	A10	SHIELD	
A11	B11	RD5-	I
A12	B32	STS2+	I
A13	C14	RD6-	I
A14	A22	PFLG-	I
A15	B15	RD7-	I
A16	A24	STS0+	I
A17	B17	RD8+	I
A18	B26	STS1-	I
A19	C21	RD9+	I
A20	B20	GND	
A21	C19	SD9-	O
A22	A14	PCTL-	O
A23	B23	RDB+	I
A24	A16	CTL0+	O
A25	B25	RDC+	I
A26	B18	CTL1+	O
A27	C28	RDD+	I
A28	B30	CTL2-	O
A29	B29	RDE+	I
A30	B28	ATTN/STS5+	I
A31	C32	RDF+	I
A32	B12	PDIR/CTL5-	O

Table 4.5.3. (1 of 3) FP pin to Peripheral/Signal name Differential

FP Pin #	Per Pin #	Signal Name	In/Out
B01	A01	SD0-	O
B02	A04	STS3+	I
B03	A03	SD1-	O
B04	A02	CTL3-	O
B05	C05	SD2+	O
B06	A08	STS4/PEND-	I
B07	A07	SD3-	O
B08	A06	HEND/CTL4+	O
B09	C09	SD4+	O
B10	B10	N.C.	
B11	A11	SD5-	O
B12	A32	STS2-	I
B13	C13	SD6+	O
B14	B22	PFLG+	I
B15	A15	SD7-	O
B16	B24	STS0-	I
B17	A17	SD8+	O
B18	A26	STS1+	I
B19	C22	RDA-	I
B20	A20	GND	
B21	C20	SDA+	O
B22	B14	PCTL+	O
B23	A23	SDB+	O
B24	B16	CTL0-	O
B25	A25	SDC+	O
B26	A18	CTL1-	O
B27	C27	SDD-	O
B28	A30	CTL2+	O
B29	A29	SDE+	O
B30	A28	ATTN/STS5-	I
B31	C31	SDF-	O
B32	A12	PDIR/CTL5+	O

Table 4.5.3. (2 of 3) FP pin to Peripheral/Signal name Differential

FP Pin #	Per Pin #	Signal Name	In/Out
C01	C02	RD0+	I
C02	C01	SD0+	O
C03	C04	RD1+	I
C04	C03	SD1+	O
C05	B05	RD2+	I
C06	A05	SD2-	O
C07	C08	RD3+	I
C08	C07	SD3+	O
C09	B09	RD4+	I
C10	A09	SD4-	O
C11	C12	RD5+	I
C12	C11	SD5+	O
C13	B13	RD6+	I
C14	A13	SD6-	O
C15	C16	RD7+	I
C16	C15	SD7+	O
C17	C18	RD8-	I
C18	C17	SD8-	O
C19	A21	RD9-	I
C20	B21	RDA+	I
C21	A19	SD9+	O
C22	B19	SDA-	O
C23	C24	RDB-	I
C24	C23	SDB-	O
C25	C26	RDC-	I
C26	C25	SDC-	O
C27	B27	RDD-	I
C28	A27	SDD+	O
C29	C30	RDE-	I
C30	C29	SDE-	O
C31	B31	RDF-	I
C32	A31	SDF+	O

Table 4. 5. 3. (3 of 3) FP pin to Peripheral/Signal name
Differential

4.5.4 Differential: By Peripheral Pins

Per Pin #	FP Pin #	Signal Name	In/Out
A01	B01	SD0-	O
A02	B04	CTL3-	O
A03	B03	SD1-	O
A04	B02	STS3+	I
A05	C06	SD2-	O
A06	B08	HEND/CTL4+	O
A07	B07	SD3-	O
A08	B06	STS4/PEND-	I
A09	C10	SD4-	O
A10	A10	SHIELD	
A11	B11	SD5-	O
A12	B32	PDIR/CTL5+	O
A13	C14	SD6-	O
A14	A22	PCTL-	O
A15	B15	SD7-	O
A16	A24	CTL0+	O
A17	B17	SD8+	O
A18	B26	CTL1-	O
A19	C21	SD9+	O
A20	B20	GND	
A21	C19	RD9-	I
A22	A14	PFLG-	I
A23	B23	SDB+	O
A24	A16	STS0+	I
A25	B25	SDC+	O
A26	B18	STS1+	I
A27	C28	SDD+	O
A28	B30	ATTN/STS5-	I
A29	B29	SDE+	O
A30	B28	CTL2+	O
A31	C32	SDF+	O
A32	B12	STS2-	I

Table 4.5.4. (1 of 3) Peripheral pin to FP/Signal name Differential

Per Pin #	FP Pin #	Signal Name	In/Out
B01	A01	RD0-	I
B02	A04	CTL3+	O
B03	A03	RD1-	I
B04	A02	STS3-	I
B05	C05	RD2+	I
B06	A08	HEND/CTL4-	O
B07	A07	RD3-	I
B08	A06	STS4/PEND+	I
B09	C09	RD4+	I
B10	B10	N.C.	
B11	A11	RD5-	I
B12	A32	PDIR/CTL5-	O
B13	C13	RD6+	I
B14	B22	PCTL+	O
B15	A15	RD7-	I
B16	B24	CTL0-	O
B17	A17	RD8+	I
B18	A26	CTL1+	O
B19	C22	SDA-	O
B20	A20	GND	
B21	C20	RDA+	I
B22	B14	PFLG+	I
B23	A23	RDB+	I
B24	B16	STS0-	I
B25	A25	RDC+	I
B26	A18	STS1-	I
B27	C27	RDD-	I
B28	A30	ATTN/STS5+	I
B29	A29	RDE+	I
B30	A28	CTL2-	O
B31	C31	RDF-	I
B32	A12	STS2+	I

Table 4.5.4. (2 of 3) Peripheral pin to FP/Signal name Differential

Per Pin #	FP Pin #	Signal Name	In/Out
C01	C02	SD0+	O
C02	C01	RD0+	I
C03	C04	SD1+	O
C04	C03	RD1+	I
C05	B05	SD2+	O
C06	A05	RD2-	I
C07	C08	SD3+	O
C08	C07	RD3+	I
C09	B09	SD4+	O
C10	A09	RD4-	I
C11	C12	SD5+	O
C12	C11	RD5+	I
C13	B13	SD6+	O
C14	A13	RD6-	I
C15	C16	SD7+	O
C16	C15	RD7+	I
C17	C18	SD8-	O
C18	C17	RD8-	I
C19	A21	SD9-	O
C20	B21	SDA+	O
C21	A19	RD9+	I
C22	B19	RDA-	I
C23	C24	SDB-	O
C24	C23	RDB-	I
C25	C26	SDC-	O
C26	C25	RDC-	I
C27	B27	SDD-	O
C28	A27	RDD+	I
C29	C30	SDE-	O
C30	C29	RDE-	I
C31	B31	SDF-	O
C32	A31	RDF+	I

Table 4.5.4. (3 of 3) Peripheral pin to FP/Signal name Differential

4.5.5 Single-ended/Low-true: By Signal Names

For low-true cable/connector applications, all + input/outputs should be used as ground. The - signals should be used to carry the signals. Grounds and n.c. and shield remain the same.

Signal name	FP pin#	Peripheral pin#
SHIELD	A10	A10
N.C.	B10	B10
GND	A17	B17
GND	A19	C21
GND	A20	B20
GND	A23	B23
GND	A25	B25
GND	A27	C28
GND	A29	B29
GND	A31	C32
GND	B05	C05
GND	B09	C09
GND	B13	C13
GND	B17	A17
GND	B20	A20
GND	B21	C20
GND	B23	A23
GND	B25	A25
GND	B29	A29
GND	C01	C02
GND	C02	C01
GND	C03	C04
GND	C04	C03
GND	C05	B05
GND	C07	C08
GND	C08	C07
GND	C09	B09
GND	C11	C12
GND	C12	C11
GND	C13	B13
GND	C15	C16
GND	C16	C15
GND	C20	B21
GND	C21	A19
GND	C28	A27
GND	C32	A31
GND	A04	B02
GND	A12	B32
GND	A16	A24
GND	A24	A16
GND	A26	B18
GND	B28	A30

GND	B02	A04
GND	B14	B22
GND	B18	A26
GND	B22	B14
GND	A06	B08
GND	A30	B28
GND	B08	A06
GND	B32	A12

Table 4.5.5. (1 of 3) Signal name to FP/Peripheral pins
Low-true Single-ended

Signal name	FP pin#	Per pin#	In/Out
RD0-	A01	B01	I
RD1-	A03	B03	I
RD2-	A05	C06	I
RD3-	A07	B07	I
RD4-	A09	C10	I
RD5-	A11	B11	I
RD6-	A13	C14	I
RD7-	A15	B15	I
RD8-	C17	C18	I
RD9-	C19	A21	I
RDA-	B19	C22	I
RDB-	C23	C24	I
RDC-	C25	C26	I
RDD-	C27	B27	I
RDE-	C29	C30	I
RDF-	C31	B31	I
STS0-	B16	B24	I
STS1-	A18	B26	I
STS2-	B12	A32	I
STS3-	A02	B04	I
STS4/PEND-	B06	A08	I
ATTN/STS5-	B30	A28	I
PFLG-	A14	A22	I

Table 4.5.5. (2 of 3) Signal name to FP/Peripheral pins
Low-true Single-ended

Signal name	FP pin#	Per pin#	In/Out
SD0-	B01	A01	O
SD1-	B03	A03	O
SD2-	C06	A05	O
SD3-	B07	A07	O
SD4-	C10	A09	O
SD5-	B11	A11	O
SD6-	C14	A13	O
SD7-	B15	A15	O
SD8-	C18	C17	O
SD9-	A21	C19	O
SDA-	C22	B19	O
SDB-	C24	C23	O
SDC-	C26	C25	O
SDD-	B27	C27	O
SDE-	C30	C29	O
SDF-	B31	C31	O
CTL0-	B24	B16	O
CTL1-	B26	A18	O
CTL2-	A28	B30	O
CTL3-	B04	A02	O
HEND/CTL4-	A08	B06	O
PDIR/CTL5-	A32	B12	O
PCTL-	A22	A14	O

Table 4.5.5. (3 of 3) Signal name to FP/Peripheral pins
Low-true Single-ended

4.5.6 Single-ended/High-true: By Signal Names

For high-true cable/connector applications, all - input/outputs should be used as ground. The + signals should be used to carry the signals. Grounds and n.c. and shield remain the same.

Signal name	FP pin#	Per pin#	In/Out
SHIELD	A10	A10	
N.C.	B10	B10	
GND	A20	B20	
GND	B20	A20	
GND	A01	B01	
GND	A03	B03	
GND	A05	C06	
GND	A07	B07	
GND	A09	C10	
GND	A11	B11	
GND	A13	C14	
GND	A15	B15	
GND	A21	C19	
GND	B01	A01	
GND	B03	A03	
GND	B07	A07	
GND	B11	A11	
GND	B15	A15	
GND	B19	C22	
GND	B27	C27	
GND	B31	C31	
GND	C06	A05	
GND	C10	A09	
GND	C14	A13	
GND	C17	C18	
GND	C18	C17	
GND	C19	A21	
GND	C22	B19	
GND	C23	C24	
GND	C24	C23	
GND	C25	C26	
GND	C26	C25	
GND	C27	B27	
GND	C29	C30	
GND	C30	C29	
GND	C31	B31	
GND	A02	B04	
GND	A14	A22	
GND	A18	B26	
GND	A22	A14	
GND	B04	A02	
GND	B12	A32	
GND	B16	B24	

GND	B24	B16
GND	B26	A18
GND	A28	B30
GND	A08	B06
GND	A32	B12
GND	B06	A08
GND	B30	A28

Table 4.5.6. (1 of 3) Signal name to FP/Peripheral pins
High-true Single-ended

Signal name	FP pin#	Per pin#	In/Out
RD0+	C01	C02	I
RD1+	C03	C04	I
RD2+	C05	B05	I
RD3+	C07	C08	I
RD4+	C09	B09	I
RD5+	C11	C12	I
RD6+	C13	B13	I
RD7+	C15	C16	I
RD8+	A17	B17	I
RD9+	A19	C21	I
RDA+	C20	B21	I
RDB+	A23	B23	I
RDC+	A25	B25	I
RDD+	A27	C28	I
RDE+	A29	B29	I
RDF+	A31	C32	I
STS0+	A16	A24	I
STS1+	B18	A26	I
STS2+	A12	B32	I
STS3+	B02	A04	I
STS4/PEND+	A06	B08	I
ATTN/STS5+	A30	B28	I
PFLG+	B14	B22	I

Table 4.5.6. (2 of 3) Signal name to FP/Peripheral pins
High-true Single-ended

Signal name	FP pin#	Per pin#	In/Out
SD0+	C02	C01	O
SD1+	C04	C03	O
SD2+	B05	C05	O
SD3+	C08	C07	O
SD4+	B09	C09	O
SD5+	C12	C11	O
SD6+	B13	C13	O
SD7+	C16	C15	O
SD8+	B17	A17	O
SD9+	C21	A19	O
SDA+	B21	C20	O
SDB+	B23	A23	O
SDC+	B25	A25	O
SDD+	C28	A27	O
SDE+	B29	A29	O
SDF+	C32	A31	O
CTL0+	A24	A16	O
CTL1+	A26	B18	O
CTL2+	B28	A30	O
CTL3+	A04	B02	O
HEND/CTL4+	B08	A06	O
PDIR/CTL5+	B32	A12	O
PCTL+	B22	B14	O

Table 4.5.6. (3 of 3) Signal name to FP/Peripheral pins
High-true Single-ended

4.5.7 Logic Sense

A low level in the system's memory appears as a 0 bit in the user's program domain. However, since the CIO channel adapter inverts all data on the CIO backplane and the 27114B does not compensate for this, a 0 in the program domain becomes a high level on the 27114B card. This high level drives the + output of any driver to a high level and the - output to a low level. Similarly, when the + input of a receiver is at a higher voltage than its - input, the output of the receiver is a high level. This high level appears on the CIO bus as a high and in the program domain as a 0 bit.

For single-ended applications, either the + or - inputs are connected to a reference level. For low-true single-ended, a 0 in the program domain is translated to a high level on the 27114B card and a low level at its low-true single-ended output (- output).

4.5.8 Front-plane Signal Definition

The following section defines all signals on the frontplane of the 27114B card. Whenever a signal is available as a pair, both inverted and non-inverted input/outputs are available. Note the double function of CTL5/4 and STS5/4.

SD[0..15] - SEND DATA 0 THROUGH 15 (16 PAIRS):

These are the data bits output from the 27114B. The data is inverted between the host's memory and the frontplane. A 0 bit in the host becomes a high level at the frontplane (the + output is more positive than the - output). These outputs are enabled only when the 27114B is in the output transfer mode and when its frontplane interface is enabled (subject to the control of a host's interface software or driver) or if pin B10 of the frontplane connector is grounded (and the PEN bit is a 1).

RD[0..15] - RECEIVE DATA 0 THROUGH 15 (16 PAIRS):

These are the data bits input to the 27114B. The data is inverted between the frontplane and the host memory. A high level input (the + input is more positive than the - input) becomes a 0 bit in the host's memory.

GND - GROUND (2 CONDUCTORS):

These are logic ground lines. There are 2 dedicated ground lines when the 27114B is used in the differential mode. When used in a single-ended mode, there are 46 extra ground lines available (one from each differential pair). Each of the extra ground wires is paired with a signal to form a transmission line with a controlled characteristic impedance.

SHIELD (1 CONDUCTOR):

The shield connection is used to provide a reliable drain path between the shield of the cable and the host's earth ground. It is designed to withstand a 1A AC current for at least 20 minutes with a residue resistance of less than 0.1 ohm as measured between the cable jacket and the connector pin.

PCTL - PERIPHERAL CONTROL (ONE PAIR):

The 27114B uses this output to handshake data to/from a peripheral. Refer to section 4.6 for timing information and logic levels.

PFLG - PERIPHERAL FLAG (ONE PAIR):

The 27114B observes this input to handshake data to/from a peripheral. Refer to 4.6 for more information.

PDIR/CTL5 - PERIPHERAL DIRECTION/CONTROL5 (ONE PAIR):

The frontplane pins used by this output are shared by the CTL5 output function and the PDIR function. The selection as to which one is to drive the frontplane pins is defined by the PDIR_OPTION bit in the AFI CONTROL2 register. The power-up/reset default state is that PDIR drives the pins.

PDIR FUNCTION (ONE PAIR):

The 27114B asserts this output to a high level when it is in the output transfer mode. It drives this output to a low level when it is in the input transfer mode.

HEND/CTL4 - CHANNEL END/CONTROL4 (ONE PAIR):

The frontplane pins used by this output are shared by the CTL4 output function and the HEND function. The selection as to which one is to drive the frontplane pins is defined by the PDIR_OPTION bit in the AFI CONTROL2 register (same as PDIR/CTL5's). The power-up/reset default state is that HEND drives the pins.

HEND FUNCTION:

The 27114B asserts HEND to a low level to indicate the last output transfer is about to begin or the last input transfer has just started.

NOTE: The HEND frontplane signal is not driven in the case where the counter is not used for an input transfer; for an output transfer without the

counter, the CIO channel drives HEND, and for transfers using the counter (in and out), the counter asserts HEND when the counter reaches zero and PCTL is low. HEND is asserted low prior to the first handshake of a transfer due to its remaining asserted from the end of the previous transfer; the default state of HEND after a reset or power-up is also a low assertion.

CTL[0..5] - CONTROL 0 THROUGH 5 (6 PAIRS):

The 27114B asserts these outputs to a high level when a 0 is written the corresponding bit CTLx of the AFI CONTROL register. These outputs are independent of other conditions on the 27114B (except for the shared functions of CTL5/CTL4 as note above).

ATTN/STS5 - ATTENTION/STATUS5 (ONE PAIR):

This input from the 27114B's frontplane is used by both the STS5 input function and the ATTN function.

ATTN - ATTENTION:

When enabled, a high to low assertion of the ATTN input causes an interrupt event to be logged in the 27114B's interrupt circuit. If the interrupt enable is also asserted high, the 27114B interrupts the host. This interrupt function is independent of other internal interrupt sources inside the 27114B hardware.

PEND/STS4 - DEVICE END/STATUS4 (ONE PAIR):

This input from the 27114B's frontplane is used by both the STS4 input function and the PEND function

PEND - PERIPHERAL END:

The peripheral can assert PEND to a low level prior to the last input transfer or any time after the last output transfer. For input operation, the timing of PEND must meet the same data set-up requirement as that of input data. If the PEND function is selected (default: not selected) as defined by bit PEND_RESET in the AFI CONTROL2 register, the 27114B will relay this transfer termination request to the CIO backplane. It does so by requesting that the CIO channel terminate the data transfer with the last input word or (by prompting the channel for more output words) the last output word. The assertion of PEND will shutdown the frontplane handshake of the 27114B: immediately in an output transfer or right after the next input transfer.

STS[0..5] - STATUS 0 THROUGH 5 (6 PAIRS):

These inputs are reported as status bits STS 0 through 5 in the AFI STATUS register. Their states are sampled immediately prior to the actual reading. A 0 is reported if the corresponding input is asserted high. They are reported as they appear at the frontplane, independent of all other conditions on the 27114B (even when ATTN and PEND options are selected).

4.6 FRONT-PLANE HANDSHAKE MODES

ASSUMPTION:

There is no pulse extension for PCTL (0 ns delay, both edge, J1 is selected). There is no filtering effect for PFLG (one clock sync, J5 is selected). J1 and J5 refer to the jumper positions of the 2x8 header on the board which are the zero positions of "PFLG" and "PCTL", respectively.

The following timing diagrams and performance estimates assume that each PCTL transition is acknowledged by an appropriate PFLG edge within 100 ns. This should be enough to cover the state machine clock to output delay time (20 ns), driver delay times (30 ns), receiver delay times (40 ns), travel time (0 ns for 0 ft cable) and sync time (10 ns). This assumes PFLG is looped back to PCTL inside the peripheral.

Actual applications probably will have to add a decision making time inside the peripheral.

The EDGE bit is defined as 0 (non-default) in all cases.

Except for the PCTL-to-PFLG delay assumption above, all timing values in this section are specified at the frontplane connector of the 27114B hardware. Timing at the end of a cable must be adjusted to reflect the travel time, the extra skew factor and the shifted point of reference due to lesser noise margin. Pleaser refer to the end of this section (4.6) for more information on these subjects.

The timing of the HEND signal is given with the assumption that output data transfers are done by the CIO channel adapter using its normal poll/service method and that the transfer counter is loaded with the same transfer count as the CIO's. If a direct access output to the output data register is used to output the last transfer word, the CIO's CEND signal is not asserted for the last word. Consequently, the frontplane's HEND output will be asserted only when the counter reaches the logical zero count.

NOTE: The HEND frontplane signal is not driven in the case where the counter is not used for an input transfer; for an output transfer without the counter, the CIO channel drives HEND, and for transfers using the counter (in and out), the counter asserts HEND when the counter reaches zero and PCTL is low. HEND is asserted low prior to the first handshake of a transfer due to its remaining asserted from the end of the previous transfer; the default state of HEND after a reset or power-up is also a low assertion.

State information is given for reference purposes. It is not visible to the user. The same is true for OR (output ready), IR (input ready), SO (shift out) and SI (shift in).

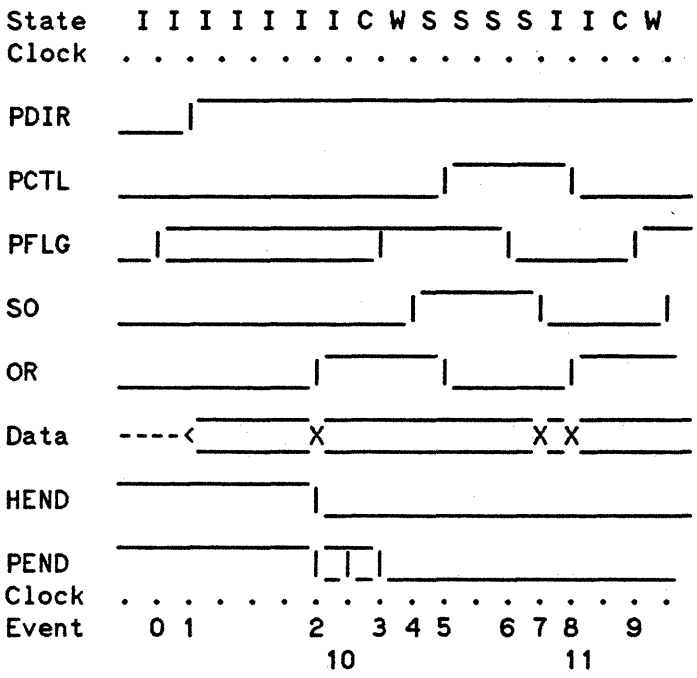
For data output transfers, the states are those defined for the shift-out state machine:

I - Idle
C - Control out
S - Shift-out
W - Wait

For data input transfers, the states are those defined for the shift-in state machine:

I - Idle
C - Control in
U - set-Up
S - Shift-in
W - Wait

4.6.1 Full Mode/Output/Slave



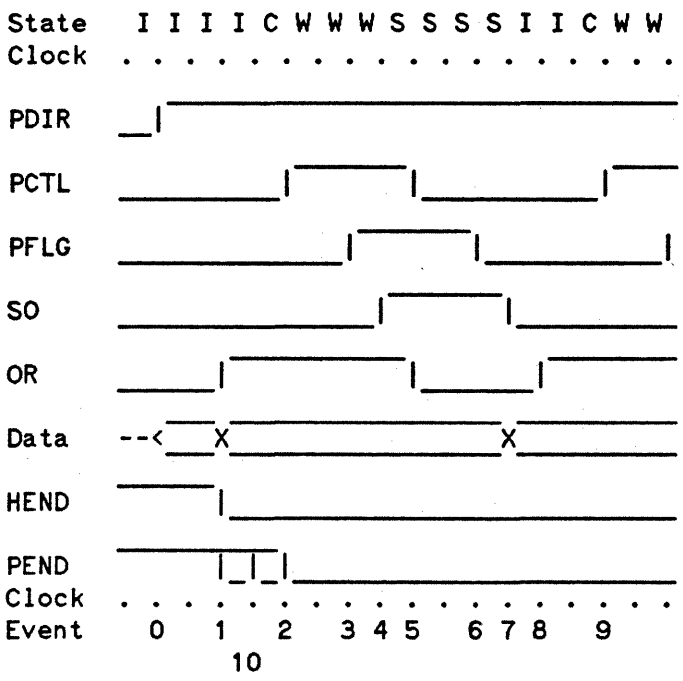
0. The peripheral asserts PFLG to start a transfer.
   (Note this could happen as late as 3.)
1. PDIR is asserted high to indicate an output.
   The driver outputs are enabled.
2. Output data from the FIFO is valid and OR is asserted.
   HEND is asserted here if this is the last output from
   27114B.
3. The peripheral asserts PFLG to start a transfer.
   (Note this could happen as early as 0.)
4. Detecting an asserted PFLG, SO is asserted high.
5. One clock later, OR responds by going low.
   PCTL is asserted to acknowledge the master.
6. PFLG is deasserted some time later.
7. SO is completed. Output data becomes invalid.
8. New output data is valid, OR is asserted
   (Note that this could happen later.)
   Another cycle starts (like step #2).
   HEND is asserted here by the transfer counter.
9. Like step #3
10. If PEND is asserted before this clock edge,
    the 27114B will not start this transfer.
    Only a falling edge is needed to abort the
    transfer.

Data/HEND set up time
(before the rising edge of PCTL): 200 ns min.

Data hold time
(after the falling edge of PFLG): 50 ns min.

The transfer cycle takes 8 clocks to complete.
The corresponding data transfer rate is 2.5 Mtransfers/s

4.6.2 Full Mode/Output/Master

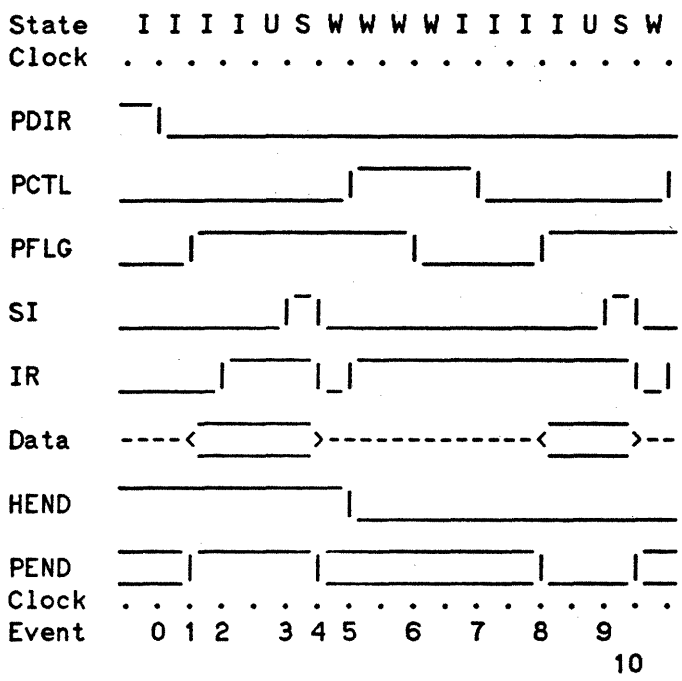


0. PDIR is asserted high to indicate the data output mode.
   The driver outputs are enabled.
1. Output data is available and OR is asserted.
   HEND is asserted here if the output word is the last one from 27114B.
2. 2 clocks later, PCTL is asserted high.
3. The peripheral acks the rising PCTL by asserting PFLG high.
   (Note this could happen later.)
4. PFLG assertion is detected, and SO is asserted.
5. One clock after SO's assertion, PCTL is deasserted to ack the rising PFLG.
6. The peripheral deasserts PFLG low sometime later (50 ns here).
7. SO is deasserted to complete the cycle.
   Data became invalid.
8. Same as #1 above.
9. Same as #2 above.
10. If PEND is asserted before this clock edge, the transfer will not start.
    Only a falling edge is needed to abort the transfer.

Data/HEND set up time
 (before the rising edge of PCTL): 100 ns min.
Data hold time
 (after the falling edge of PFLG): 50 ns min.

The transfer cycle takes 10 clocks to complete.
The corresponding data transfer rate is 2 Mtransfers/s

4.6.3 Full Mode/Input/Slave

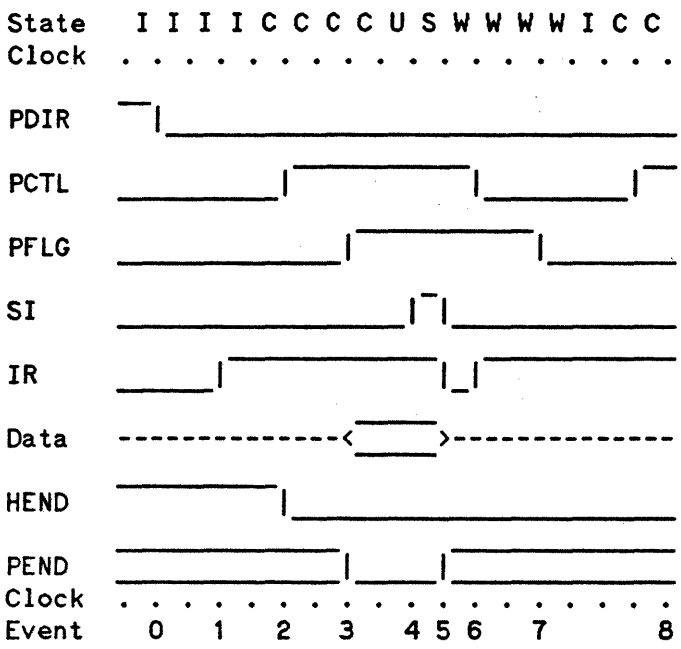


0. PDIR is deasserted to indicate the data input mode.
   The peripheral can drive the input data bus at any time.
1. The peripheral asserts PFLG to start the transfer.
   Data must be valid at the same time.
   PEND must be deasserted high unless this is the last data input from the peripheral.
2. 27114B's FIFO has room for data. (IR)
3. Data is latched into the FIFO.
4. The latching is done.
5. PCTL is asserted to acknowledge the rising PFLG.
   Data and PEND can change (as early as 4).
   The FIFO is ready again (this could happen later).
   If this is the last word accepted by 27114B,
   HEND is asserted low with the rising PCTL.
6. The peripheral deasserts PFLG to ack the rising PCTL.
7. PCTL is deasserted to ack the falling PFLG.
8. A new cycle starts. PEND is asserted for the last input from the peripheral.
9. Like #3 above.
10. Like #4 above.

Input data set up time: 100 ns min.
(If data is asserted with rising PFLG)
Input data hold time: -50 ns min.
(From falling PCTL)

The transfer takes 10 cycles to complete
The corresponding data transfer rate is 2 Mtransfers/s

4.6.4 Full Mode/Input/Master



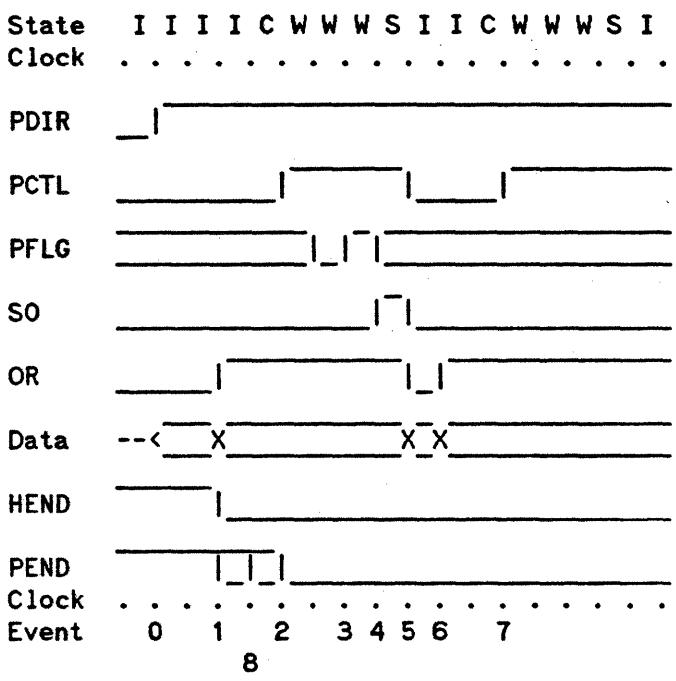
0. PDIR is deasserted to indicate the data input mode.
   The peripheral can drive the input data bus at any time.
1. 27114B's FIFO has room for data.
2. PCTL is asserted to indicate 27114B's readiness.
   If this is the last word accepted by 27114B,
   HEND is asserted low with the rising PCTL.
3. The peripheral asserts PFLG to ack the rising PCTL.
   Data must be valid at the same time.
   PEND must be deasserted unless this is the last data input from the peripheral.
   The above diagram shows the timing required for the last transfer from the peripheral.
4. Data is latched into the FIFO.
5. The latching is done.
6. PCTL is deasserted to acknowledge the rising PFLG.
   Data and PEND can change (as early as 5).
   The FIFO is ready again (this could happen later).
7. The peripheral deasserts PFLG to ack the falling PCTL.
8. A new cycle starts.

Input data set up time: 100 ns min.
(If data is asserted with rising PFLG)
Input data hold time: -50 ns min.
(From falling PCTL)

The transfer takes 11 cycles to complete
The corresponding data transfer rate is 1.8 Mtransfers/s

4.6.5 FIFO Mode/Output

(27114A's mode)



0. PDIR is asserted to indicate the data output mode.
   The driver outputs are enabled from here on.
1. The output data is available and OR is asserted.
   HEND is asserted here if the output word
   is the last one from 27114B.
2. 2 clocks later, PCTL is asserted high.
   PFLG could be either low or high.
3. The peripheral acks the rising PCTL by asserting
   PFLG high from a deasserted state.
   (Note 2 to 3 could take longer.)
4. The PFLG assertion is detected. SO is asserted.
5. One clock after SO's assertion, PCTL is
   deasserted to ack the rising PFLG.
   PFLG could be either high or low.
   Data became invalid.
6. Data from 27114B becomes available again.
7. Two clocks cycle later, PCTL is asserted
   again; PFLG could be either high or low.
8. If PEND is asserted low prior to this
   time, the transfer will not take place.
   Only a falling edge is required to abort
   the transfer.

Output data/HEND set up time: 100 ns min.
(before the rising edge of PCTL)

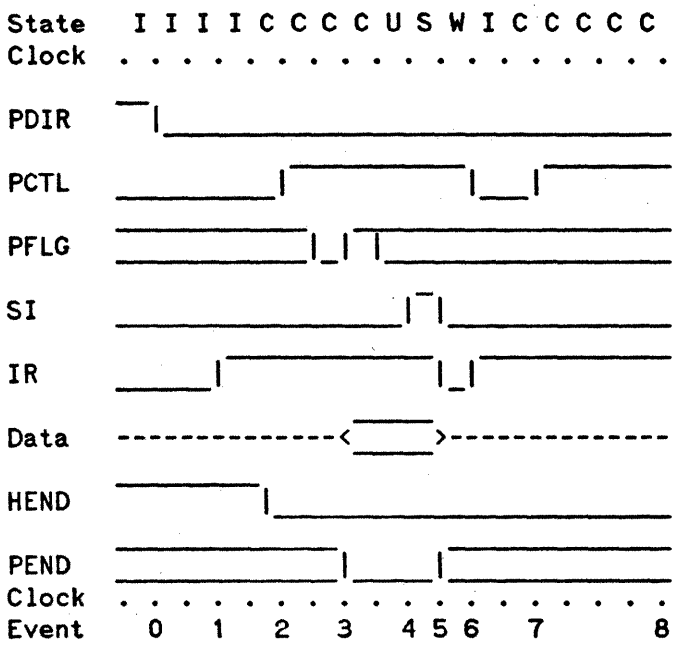
```
Output data hold time:              100 ns min.
 (after the falling edge of PFLG)
PCTL low time:                      150 ns approx.

The transfer takes 7 cycles to complete
The corresponding data transfer rate is 2.8 Mtransfers/s
```

This handshake mode is called "pulse" mode in the 27114A's documents. Since the timing of the mode looks more like that of a FIFO's than other actual pulse mode handshakes, the "FIFO" term is used here instead.

In output transfers, PCTL appears as an output ready (OR) of the FIFO while the PFLG input can be considered as the shift-out (SO) input. While the FIFO has available data, its OR is asserted high. When SO is asserted high, OR goes low temporarily and then high again (if there is another valid output word).

4.6.6 FIFO Mode/Input

(27114A's mode)



0. PDIR is deasserted to indicate the data input mode.
   The peripheral can drive the input data bus at any time.
1. 27114B's FIFO has room for data.
2. PCTL is asserted to indicate 27114B's readiness.
   If this is the last word accepted by 27114B,
   HEND is asserted low with the rising PCTL.
   PFLG could be either high or low.
3. The peripheral asserts PFLG from a deasserted state.
   to ack rising PCTL.
   Data must be valid at the same time.
   PEND must be deasserted unless this is the
   last data input from the peripheral.
   The above timing diagram shows the last transfer
   from the peripheral.
4. Data is latched into the FIFO.
5. The latching is done.
6. PCTL is deasserted to acknowledge the rising PFLG.
   Data and PEND can change (as early as 5).
   The FIFO is ready again (this could happen later).
7. PCTL is asserted again to start another cycle.
   PFLG could be either high or low.
   A new cycle starts.

Input data set up time: 100 ns min.
(If data is asserted with rising PFLG)

```
Input data hold time:          -50 ns min.
  (From falling PCTL)
PCTL low time:                 100 ns approx.

The transfer takes 8 cycles to complete
The corresponding data transfer rate is 2.5 Mtransfers/s
```

In input transfers, PCTL appears as an input ready (IR) of the FIFO while the PFLG input can be considered as the shift-in (SI) input. While the FIFO has room for data, its PCTL (IR) is asserted high. When PFLG (SI) is asserted high, PCTL (IR) goes low temporarily and then high again (if there is room for another word).

4.6.7 Other Modes

There are no other frontplane handshake modes available at this time.

4.6.8 Performance Consideration

The following sections are intended to supply a potential user with the information needed in order to predict the performance of the 27114B in terms of transfer rate and the effects of a 27114B on a CIO backplane. It does not provide information on specific implementations of the CIO backplane. Backplane-specific information must be found elsewhere.

The fundamental limiters of performance are as follows:

1. The maximum burst data transfer rate of the CIO backplane.
   This is a function of the channel adapter design.
   CIO specs a maximum data rate of 5 Mega words per second.

2. The ability of the CIO channel adapter to meet that rate given contention on the bus which the channel adapter resides on.
   Bursting on the CIO backplane is limited to 32 transfers. A poll is always done between bursts.

3. Priority on the backplane and the scheme used to determine the allocation of such bandwidth as exists between device adapters. This depends on the channel adapter design, choice of card slot, and the operating system.

4. Overhead on the backplane associated with polling. This depends on the design of the poll timing in the channel adapter as well as the service algorithm used by the channel adapter. The service algorithm is typically in the channel adapter microcode.

5. Fixed overhead in the frontplane handshake hardware. This time is determined by the design of the 27114B.

6. Cable length. The longer the cable, the slower the handshake cycle.

7. Time taken by a peripheral to move data after seeing PCTL asserted. This depends on the peripheral design.

The limits listed in numbers 1, 2, 3 and 4 are beyond the scope of this document with the exception of a description of the general effects. For details, please consult the CIO standard manuals.

4.6.8.1 FRONT-PLANE LIMITS.

The frontplane limits to performance are made up of the cycle time required to access the FIFO and logic delays on the board. The following discussion assumes that the backplane is keeping up with the average transfer rate on the frontplane in a timely fashion; e.g. the frontplane handshake logic is never held off by a shortage of data at the FIFO output or a shortage of space in the FIFO. This is not normally true.

The cycle time for data to move from the 27114B to a peripheral is made up of the events in the sequence below:

1. PCTL is asserted onto cable to indicate to the peripheral that data is available.

2. The propagation delay down the cable to the peripheral and rise time effects when the transition is seen at the peripheral end.

3. Receiver delay at the peripheral end. (This depends on the peripheral design.)

4. Time for the peripheral to act to accept data. (If any hold-off is needed.)

5. Assertion of PFLG at the driver input (On the peripheral).

6. Driver delay to PFLG on the cable (On the peripheral end).

7. Propagation delay to the 27114B + rise time effects when the transition is seen at the 27114B end.

8. Receiver delay in the PFLG path at the 27114B.

9. Time needed in the 27114B to move the next word onto the data lines and cycle PCTL low then back high with a set up of data prior to PCTL being asserted again.

10. Driver delay in the PCTL path (on the 27114B).

As noted above, 1, 3, 5, 6, 8, 9 and 10 are covered by the performance computation following each handshake timing diagram. 2 and 7 are assumed to be 16 ns for a cable length of 10 ft. 4 is assumed to be 0 in each case.

The performance figures provided in this section assumes a 10 ft cable with a signal travel time of 32 ns (round trip).

The total cycle time for the 27114B is:

```
Output/Full/Slave:  450 ns   Input/Full/Slave:   550 ns
Output/Full/Master: 550 ns   Input/Full/Master:  600 ns
Output/FIFO:        400 ns   Input/FIFO:         450 ns
(27114A/Output:     314 ns)  (27114A/Input:      324 ns)
```

These translate to the following rates (in MBytes/s):

```
Output/Full/Slave:  4.4 MB/s  Input/Full/Slave:   3.6 MB/s
Output/Full/Master: 3.6 MB/s  Input/Full/Master:  3.3 MB/s
Output/FIFO:        5.0 MB/s  Input/FIFO:         4.4 MB/s
(27114A/Output:     6.3 MB/s) (27114A/Input:      6.1 MB/s)
```

Note that there has been some performance degradation in going from the 27114A to the 27114B. This should not be a concern since the CIO's upper limit is known to be around 4.8 Mbytes/s.

4.6.8.2 CABLE LENGTH.

As a cable becomes longer, the loss is higher and the capacitive loading is larger. The first factor tends to cut into the noise margin of the signal. The second factor rounds out the rise and fall time of signals. Its effects are greater for signals with very low or very high duty cycles than those with mid-range duty cycles. This is due to the excessive charge (or lack of) which needs to be neutralized in order to change the voltage level in the cable. The result of this second factor is that the skew between data (sometimes very static) and controls (mostly repetitive) become more apparent as the cable gets longer.

The cycle time for data transfer on the frontplane is increased with increased cable length. The propagation delay of the cable and the effects of resistive losses in the lines come into play.

The propagation delay in the cable is about 1.6 nsec per foot of cable. This delay in the signal path shows up in the cycle time as length(in feet) * 1.6 * 2. The factor of 2 is because the delay is incurred in PCTL to the peripheral and PFLG returning.

The effects of resistive loss in the line show up in two ways. The first is that in long cables (becomes noticeable at > 150 feet), pulses on lines may not even show up at the far end. The second is in skew between signals due to the rise time of the signals.

If the cable is more than about 150 feet long, the rise time and fall times of the signals become significant. In the FIFO handshake mode, the PCTL line pulses low for some guaranteed minimum time at the 27114B end of the cable (100 ns min) and it is up to the system designer or peripheral designer to ensure that this is sufficient to be seen by the peripheral. However, as the cable is lengthened, the rise and fall times increase due to resistive losses in the lines resulting in narrower and narrower pulses seen at the receiving end of the cable. The only option open to a designer is to set a new time constant on the 27114B. This option is not supported currently.

The other problem with long cables is the skew seen due to the rise times. The thresholds on receivers will vary and the rise time of signals in long cables is slow; signals driven at the same time may cross through receiver thresholds at different times. The danger exists that the set up time for data prior to the reception of PCTL could be affected enough to cause problems. The time constant for the set up of data driven by the 27114B is 100 ns. The time constant for the de-skewing of received data is also 100 ns.

4.6.8.3 CIO DATA BURSTING.

The 27114B card is capable of moving bursts of data between the FIFO on it and the backplane. The 27114B will move a burst of data which is as long as it can be, somewhere between 1 word and the maximum of 32 (imposed by the CIO backplane), any time it responds to an SRQ poll and is granted service by the channel adapter. The size of these bursts is dependent on the rate at which the frontplane is capable of moving data into or out of the 27114B and the rate at which the 27114B is capable of winning data transfer cycles from the channel adapter.

The size of the transfer depends on the number of words (or spaces, depending on transfer direction) which are available in the FIFO during a burst. For output transfers, when there are more than 55 words in the FIFO, the burst is terminated early by the 27114B. It deasserts the BR- control line to the channel adapter. It also helps to prevent a particular 27114B from tying up all lower priority cards on the backplane with short and inefficient transfers. If the frontplane cannot keep up with back-to-back full length bursts, it will let a lower priority card have the opportunity to win an SRQ POLL.

In input transfers, bursting is not done when there are less than 8 words available in the FIFO to be read by the CIO channel.

INTERACTION BETWEEN BACKPLANE AND FRONTPLANE

There are two cases here that are of interest. The first is the case of a frontplane connection which is capable of outrunning the average transfer rate seen on the backplane side. The second is the case of a backplane connection which is capable of outrunning the average transfer rate of the frontplane.

The fast frontplane and slow backplane situation shows up on the backplane as an 27114B card which always responds to SRQ polls and always moves the maximum allowed burst of data when it is provided service. If it is a high priority card, it will tend to lock out lower priority cards and hog the entire backplane unless some relatively intelligent SRQ service algorithm happens to be implemented in the channel adapter. (No such "intelligent" channel adapters are presently being built or developed.) Keep in mind that unless data is continuously flowing into the machine from somewhere else, this hogging of the backplane bandwidth cannot go on indefinitely.

This is definitely the case when competing with a BIC chip based card. The HPIB card can be starved down to about 268 K bytes per second by a lower priority 27114B running at its maximum possible rate. This is only for the time during which DMA's for both cards are enabled and both cards are attempting to move data at the same time. The issue of whether or not a card is ever really starved to the degree that it has noticeable undesirable affects depends on the statistical nature of traffic on that channel adapter. This question becomes important in real-time control.

In the fast frontplane and slow backplane situation, the frontplane will find itself moving bursts of data as it gets them. Looking at the frontplane transfers, one would see bursts of data mirroring the bursts being moved between the channel adapter and the FIFO.

The slow frontplane and fast backplane situation shows up on the backplane as a 27114B taking something less than the maximum burst size in a transfer.

In this case, the frontplane transfers will appear smooth and not reflect the burst nature of transfers on the backplane side of the card (unless the peripheral is designed such that it tends to bunch up transfers).

4.6.9 Machine/machine transfers

If both parties behave by the rules and as long as they don't both talk or listen at the same time, there should be a reliable connection regardless of who starts first, the talker or the listener, the master or the slave.

It should be noted that a reliable connection requires both parties to be in stand-by states before they should attempt to make a connection. They must be able to detect the condition that the other party is in. Most critically, they must know whether the other machine is actually powered on or not.

The PEND and HEND features can be used to successfully terminate a transfer if there is a mismatch of count between the sender and the receiver. Due to the timing of the HEND output, the slave should not enable its PEND feature in any master-read/slave-write transfers in which the master's count is equal to or less than the slave's count. If this is the case, the last read of the master will not be acknowledged.

4.7 EDGE BIT AND PFLG

The PFLG input from the frontplane is exclusive-nor'ed with the EDGE bit before it is fed to the frontplane handshake circuit ("the state machine"). The timing diagrams in section 4.6. assume that the EDGE bit is programmed with a 0 (the non power-up/default state). If the EDGE bit is programmed with a 1 (default), the value of PFLG in those timing diagrams must be reversed.

Since the EDGE bit can be used to change the level which the state machine perceives the PFLG input, it is a useful technique to simulate different levels of the PFLG input.

It should be noted that the loopback testhood requires a 0 EDGE bit to function properly as an infinite sourcer or sinker of data.

4.8 CABLE SPECIFICATION

4.8.1 General Constructrion

The cable has 48 twisted pairs of 32 gauge wire wrapped in a combination of foil/braid shield and jacketed in standard HP jade gray PVC. The connectors on both 27114 ends of the cable are DIN 41650 type C headers (Eurocard connectors).

Both ends behave in the same manner and can be installed either way. The wiring is made such that if the cable is used to connect two AFI cards, the positive output of a signal on one card is connected to the positive input of a matching signal on the other card (e.g. PCTL+ to PFLG+). This arrangement allows the same cable to be used for AFI to AFI connection.

RF shielding is done via the rook-to-slot contact at the point the cable exits the CIO card cage and also via the clipping mechanism. Safety grounding is also provided via the rook-to-slot contact.

The cable assembly is mated to a male (pin) 96-position Eurocard connector on the 27114A card. A 1/2" wire-wrap connector (DIN header type R) is supplied as the matching connector at the user end. Only two lengths are provided: 3 m and 12 m. Custom-made cables for other lengths can be ordered directly from the OEM supplier, DuPont Connector Systems. Its impedance is about 120 ohms. The resistance per foot is about 60 milliohms. Propagation delay in the cable is about 5 nanoseconds per meter.

4.8.2 Differential/Single-ended

The cable described in the preceding section is recommended for both differential and single-ended applications. It should provide better controlled characteristic impedance for single-ended applications than the previously available single-ended cables.

4.9 PERIPHERAL CONNECTOR

The 27114B cable is designed to mate with a 96 pin DIN connector. It is recommeded that the user's application provide this connector directly as their interface to the 27114B card.

4.9.1 Wire-wrap Connector

The 27114B is delivered with a 96-pin DIN wire wrap connector which should offer some degree of flexibility to certain users.

4.9.2 Other Connectors

Other types of DIN connectors can also be used with the 27114B's cable. The 27114B's cable is not compatible with those DIN-look alike connectors which have an offset built into their connector.

4.10 LOOPBACK MODE

Loopback testing can be done at one of two levels: internal FIFO loopback or external loopback with the testhood.

If the frontplane is disabled, anything written to the FIFO is actually retained until it is consumed. It is possible to change the direction control from output to input and read back what was written to the FIFO. Since the effective FIFO length in the output direction is only 55 words, any write of 56 words or more using the bursting mode on CIO will not be completed. The full depth (64 words) of the FIFO can still be accessed if the last 9 words are written out using the non-bursting transfer mode. Reading back from the FIFO will guarantee word for word for the first 64 words or more. This testing does not test the line drivers or the line receivers.

Loopback testing with the testhood provides a more thorough testing. Data can actually be passed through the frontplane line drivers and receivers. A possible test algorithm is as follow:

* Enable backplane poll response, select the data output mode, define EDGE as 0 and enable the FIFO.
* Write one word to register 0.
* Change the direction to the data input mode.
* Fake a handshake by redefining the EDGE bit as 1.
* Read in 2 words.

The second word should be the same as the first word if the path through the loopback testhood is not defective.

This test does not stress the line drivers or receivers as far as noise margin and loading are concerned.

Similar testing techniques could be applied to fully test all other control, status and handshake input/outputs.

4.11 LOOPBACK TESTHOOD

The loopback hood consists of a matching connector and a small PC board. It is designed to fit in a standard CIO cardcage with a closed door when installed in a 27114B card.

The loopback testhood makes the following connections:

Outputs		Inputs
SD[0..15]	are wired to	RD[0..15]
PCTL	is wired to	PFLG
CTL0	is wired to	STS0
CTL1	is wired to	STS1
CTL2	is wired to	ATTN/STS5
CTL3	is wired to	STS3
HEND/CTL4	is wired to	STS4/PEND
PDIR/CTL5	is wired to	STS2
GND(J1/B10)	is wired to	DIAG (invert the driver enable line)

This is subjected to change

The presence of the loopback testhood is detected automatically by the 27114B hardware. This inverts the enable control of the output line drivers. The line drivers are normally enabled only when the 27114B is in the output mode and the PEN bit is a 0; they are now disabled. In other combinations of the PEN bit and PDIR bit, the line drivers are enabled. This allows the line drivers to be enabled when the 27114B is in the receive mode.

Loopback via the testhood can be accomplished by outputting something to the FIFO with the frontplane handshake disabled. This should keep the data in the FIFO. As the direction is changed to the input mode, the line drivers are enabled and they drive the line receivers via the loopback hood. By simulating clock edges on the PFLG line with the EDGE bit, one or more data words can be input from the frontplane (which is being driven with what is currently at the output of the FIFO).

THEORY OF OPERATION

SECTION 5

The 27114B is a parallel interface card designed as a replacement for the infamous "AFI" 27114A card. As such, it corrects several main weaknesses of the AFI-A card. This chapter will briefly explain how the card functions.

The 27114B can be viewed as a FIFO operating in a controlled environment. It is most useful when used to transfer large blocks of data between the host and a peripheral. It can act as a DMA controller in this sense. The FIFO can store up to 64 words of 18 bits each. 16 of the data bits are used to carry the actual data. The 17th and 18th bits are used to carry the PEND and HEND information (more on these features later).

The 27114B operates in the half-duplex mode. It can only transfer output data or input data and never both at the same time. The hardware is controllable by the host at any point in time.

A state machine on-board the 27114B is used to control the FIFO and the handshaking of data between the FIFO and both the CIO backplane and the parallel frontplane. Three different handshake modes are offered on the frontplane: FIFO mode (old 27114A AFI mode), full mode/slave and full mode/master.

A jumper selection on-board the 27114B can be used to extend the effective pulse width of the PCTL pulse and to filter out unwanted noise on the PFLG input.

Frontplane data can be wired in either a differential mode (balanced signal) or single-ended mode (unbalanced signal, low or high true). The selection is done via the positioning of jumper blocks on the card.

The 27114B card can be roughly broken up into the following functional blocks:

* Backplane address decoding
* Backplane data transfer
* Backplane poll response
* FIFO and data path
* 24 bit transfer counter
* Misc. CIO and AFI control/status registers
* State machines
* Frontplane line driver/receivers
* Interrupt circuit
* HEND circuit
* PEND circuit

5.1 New Features

The new features are added to the design with an objective of being backward compatible with the 27114A. This includes the addition of registers A, B and the expansion of register 7.

All new features are defined such that the 27114B can function as a 27114A without any access to register A or B and with any kind of information being written to the expanded part of register 7.

The definition of these new features thus becomes more or less bound by the desired default state: ATTN must be enabled, the PDIR option must be selected, the counter must be reset, PEND must be disabled, interrupts can only come from ATTN and the handshake mode is the pulse mode.

5.2 Backplane address decoding

The backplane address decoding is done by the DECODER PAL20L10. This decoder asserts low one of its 10 output lines to select different circuits on the 27114B to respond to the current CIO transaction.

To repond to any transaction on the CIO bus, the 27114B must not be in the hard reset condition. This condition is entered whenever the power is first applied or when the PPON line on the CIO bus is deasserted. The 27114B is taken out of this hard reset condition when an appropriate address teaching operation is done to it. This operation is essentially a write to its data register with the data bit corresponding to its slot number being asserted to a low level.

As the 27114B gets out of the hard reset condition, the Reset flipflop remains set and the ARE flipflop remains cleared. The 27114B can also respond to other register accesses once the hard reset condition is removed.

Register addressing is done using four control lines on the CIO: BP1, CBYT, CEND and BP0 (in that order of significance, high to low). Out of the possible 16 addresses, the 27114B implements only 10 of them: 0/2/4/6, 1, 3, 7, 9, A and B. The 0/2/4/6 group responds singly as one register (data register).

Except for reading the data register and the CIO STATUS register, all other reads are non-destructive. A reading of the data register may clock a data word out of the FIFO circuit if it is done appropriately. Any read of the CIO STATUS register can potentially clear a pending interrupt condition being stored in the ARQ flipflop.

All writes to the 27114B's registers are potentially destructive.

5.3 Backplane data transfer

Backplane data transfer is under the control of a state machine. The correct data transfer protocol requires the CIO channel adapter to detect a positive answer from the 27114B card to one of its service polls before a data transfer is made to this card. However, the CIO channel can address register 0 any time it likes to initiate a data transfer. This is especially important in the case of a diagnostic application program.

The CIO channel operates essentially in two disctintive, non-overlapping phases: polls and syncs. The poll phases are used to determine who is ready to transfer data on the CIO bus (or in case of an interrupt, who has interrupted). The sync phase is used to do the actual data transfer. By looking at the responses it gets from each poll, the CIO channel can determine which slot it must service next. For each slot, a sync phase is used. Normally, only one data transfer is made per sync cycle. However, if the selected IO card asserts low its Burst Request line, the channel can continue up to a maximum limit of 32 words per sync phase. This allows a low overhead method to tranfer large amounts of data. The 27114B takes advantage of this whenever it can.

For output data transfers, the 27114B reponds to service polls any time it has room for 8 or more words in its FIFO (the word count is 55 or less). Output data transfers will always be requested with the Burst Request feature from the 27114B card. When the number of words in the FIFO exceeds 55 (approximately), the card stops answering to poll responses and also deasserts high the Burst Request output. Within one to three transfers later (depending upon the exact timing), the CIO channel will stop bursting data to the 27114B. Poll answering and burst requests are resumed when the number of words stored in the FIFO drops to a level below 55.

For input data transfers, the 27114B responds positively to service polls any time it has one or more data words in its FIFO. As the number of words stored in the FIFO exceeds 8, the 27114B starts asserting low the Burst Request line to the CIO channel. This is a convenient arrangement since with light loading on the frontplane, the channel can occasionally come out and get a data word from the 27114B with every sync cycle (between two polls). As the load increases and the data gets piled up in the FIFO, the bursting mode is entered and the CIO channel can move a larger number of words every time it services the 27114B card.

5.4 Backplane poll response

The backplane poll response circuit is part of the POL16L8 PAL. Poll responses are done whenever the CIO channel does a service poll or an attention poll. Service polls are used to figure out who on the bus needs to transfer data next. Attention polls are used to determine the party or parties who interrupted immediately prior to the poll.

The 27114B responds to the service poll by asserting low the UAD line on the CIO bus. It does so only if it is ready and capable of doing a data transfer (see above). In the case of attention polls, the 27114B answers to the poll if its ARQ flipflop is set (indicating a pending interrupt) and the ARE flipflop is set (interrupt is enabled).

In the event of a PEND assertion in the output transfer mode, service polls are also acknowledged to force the transfer of one more output word such that the CIO's DEND signal can be asserted.

External latches are used to synchronize midplane signals to assure a minimal probability of having unstable data set up and hold times during polls on the CIO bus.

5.5 FIFO and data path

The FIFO is used primarily to carry data between the frontplane and the backplane circuits. Its 17th and 18th bits are used for the PEND and HEND functions.

The effective FIFO length is 55 words in the output direction due to the way poll responses are done in this mode. In input transfers, its full length (64 words) can be used.

There is no parity generation or checking between the 27114B and the CIO channel.

For any read, all involved buffers and transceivers are enabled immediately as a sync pulse is asserted low on the CIO backplane. For reads from the FIFO, the trailing edge of the IO_SB (IO strobe) signal is used to remove the current word from the output of the FIFO.

For all writes, the data is latched with the trailing edge of IO_SB. In case of writes to the FIFO, the data is latched externally to the FIFO before the actual write to the FIFO is done.

All interactions between the CIO and the FIFO is controlled by the state machine.

5.6 24 bit transfer counter

The 24 bit transfer counter can be used to keep track of how many transfers are supposed to happen. It can be programmed with a positive count and enabled to count down at the completion of a handshake. As the count becomes 0x00FFFF or less, the counter will disable the frontplane handshake circuit, preventing further handshakes from happening.

The counter can be disabled by presetting its output to the maximum count and keeping it in the reset state. This is the default state after a reset or power up condition.

5.7 Misc. CIO and AFI control/status registers

Beside the read/write register 0 (data register), there are four other CIO registers that are available on the 27114B to meet the requirement of the CIO standard.

Read register 1 (Sense register) returns the definition of the 27114B (level 0 card) and the state of the ARE and ARQ interrupt flipflops.

Write register 1 (CIO CONTROL register) is used to control the state of the ARE and RESET flipflop.

Read register 3 (ID register) returns the ID of the 27114B card (32) and its current revision number (2 or greater).

Read register 9 (STATUS register) returns a fixed value, but the reading action also clears the ARQ flipflop.

There are 5 other registers that are unique to the 27114B:

Write register 7 (AFI CONTROL register) and Write register B/lower (AFI CONTROL2 register) are used to control the hardware on the 27114B card.

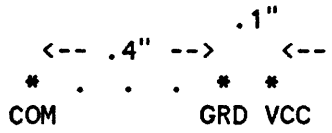
Read register 7 (AFI STATUS register) is used to return the state of the different circuits on the 27114B card.

Register A and B/upper are used to implement the transfer counter.

5.8 Programming of revision number

The revision number on the 27114B can be programmed to any value between 0 and 7. This is accomplished via the appropriate installation of three jumpers, one for each bit of the revision number.

Each jumper consists of three holes: one common hole (going to the input of the revision latch) and two other holes (VCC and ground). The VCC and ground holes are positioned such that their distances to the common hole is . 5" and . 4", respectively. The following illustration shows how:



A zero ohm resistor should be loaded (per jumper) such that it connects the COM hole with either the VCC or GRD hole. When the VCC hole is selected, the bit is read as a 1. When the GRD hole is selected, the bit is read as a 0.

The three jumpers are labelled as S10, S9 and S8. S10 is the most significant bit.

5.9 State machine

The FIFO state machine is implemented entirely in one PAL, the FIF22V10 PAL. Critical signals are sync'ed externally to the PAL with a latch which is clocked with the same clock edge which goes into this PAL.

The state machine actually has two state machines in it. Each one takes care of one side of the FIFO: one controls the input of the FIFO, the other controls the output of the FIFO. Both of these state machines act as the frontplane handshake controller in the appropriate input/output mode.

The state machine runs off a 20 MHz clock (50 ns period). It takes its input from the frontplane control input (PFLG), from the FIFO (IR and OR), and from the AFI CONTROL registers (Mode2/1/0, reset etc...).

The state machine runs all the time. To disable its frontplane part, the frontplane enable bit can be turned off. To disable the backplane interface part, the state machine must be reset and kept in this state. The BPREN (backplane poll response enable bit) cannot completely disable the backplane interface. This bit can only be used to disable the answering of polls on the CIO backplane. Note that a forced access to/from a data register is still possible even if there is no poll answer from a card. If the state machine is disabled, the FIFO is unaccessible from the backplane (except for FIFO reset). Other than that, CIO accesses to the data registers can activate the state machine to do a data-shift in or shift-out.

5.10 Frontplane line driver/receivers

The frontplane line drivers are used to drive output data whenever the 27114B is enabled and is programmed to be in the output mode. With the installation of a testhood, the enable/disable function is reversed. This allows an external loopback test to be done with a testhood when the 27114B is in the receive mode.

Besides the data line drivers and receivers, there are 7 other sets of line drivers and receivers used to implement the handshake control circuit as well as 6 possible control outputs and 6 status inputs. 2 of the control outputs do double duty as the HEND and PDIR outputs. 2 of the status inputs can be used by the PEND and ATTN circuits, which are also selected as options.

5.11 BALANCED/UNBALANCED MODE

Differential line drivers and receivers are used at the frontplane to drive and receive signals. In the unbalanced mode, either inverted or non-inverted outputs of the line drivers are used to source/sink a single-ended signal. A reference voltage is applied to one of the inputs (the inverted or non-inverted one) of the line receivers while the other ones are used as single-ended inputs.

Termination is provided in both balanced and unbalanced signal modes. Termination matching is 132 ohms (equivalent) for the single ended mode and 120 ohms for the differential mode.

There is a 6 by 48 matrix of pins which provides the selection between the single-ended and differential signal configurations via the use of jumper blocks.

5.12 SIGNAL CONDITIONING

The output handshake signal PCTL can be extended from 0 to 150 ns in increments of 50 ns with the configuration of a jumper. The extension of the deassertion-to-assertion transition allows more data set-up time to be seen by a peripheral if needed.

The input handshake signal PFLG can be filtered through a qualifier circuit. The qualifying periods range from 0-50 ns through 150-200 ns, depending on the placement of another jumper. Changes in the PFLG must be maintained in a stable state for a minimum amount of time (the smaller number which is selectable from 0, 50, 100, and 150ns) before it can be seen by the 27114B handshake circuit. The larger number in each pair is the maximum amount of time that a stable signal must have to be seen. The circuit has two functions: delay the incoming PFLG to increase the input data set-up time and to filter out unwanted transitionals on the PFLG line.

5.13 Interrupt circuit

The interrupt circuit in the 27114B consists of three parts: the ARE interrupt enable flipflop, the ARQ interrupt pending flipflop and the three interrupt sources, ATTN, PEND, and ZERO.

The ARE flipflop is controlled by writes to the write register 1. It can disable or enable the assertion of the ARQ line on the CIO bus by the 27114B card. Its state is also used to determine whether the 27114B responds to attention polls or not.

The ARQ flipflop is used to register an interrupt event. This can happen independent of the state of the ARE flipflop. Whenever the first of the three interrupt sources becomes valid, the ARQ logs the interrupt event. Any read of the CIO STATUS register will clear this flipflop.

There are three separate interrupt sources on the 27114B: the ATTN input from the frontplane (27114A's compatible function) and the PEND and the zero transfer counter sources. The PEND interrupt is used to terminate a call in case a peripheral decides to abort a transfer before the completion of the number of transfers programmed into the transfer counter. The transfer counter's interrupt is used to indicate that the transfer of the pre-programmed number of words has completed.

5.14 HEND circuit

The HEND circuit is used to signal a peripheral when the 27114B has completed all transfers. It is provided as an option. If not selected, its output can be used to carry an extra, independent control output. The default state after a reset or a power-up condition is that this option is enabled.

HEND is asserted high at the end of the transfer. For output transfers, it is asserted before the last transfer takes place with the same timing as output data. For input transfers, it is asserted after the last transfer takes place, immediately after the trailing edge of PCTL.

5.15 PEND circuit

The PEND circuit provides a mechanism which allows a peripheral to abort a transfer before the host-requested number of transfer is reached. This option is selectable and PEND is capable of generating an interrupt when properly enabled.

The state of the input is available as a status bit for other use in case this feature is not selected. The default state after a reset or a power up condition is that this option is disabled.

For input transfers, a peripheral must assert PEND before the last transfer is to take place (with the same timing requirement as for other input data). For output transfers, PEND can be asserted any time after the last transfer has started (please refer to the timing diagrams in this ERS for the exact timing).

PROGRAMMING GUIDE

SECTION 6

6.1 OUTPUT TRANSFERS

Output transfers: walk through a typical programming sequence to output a single word and to output a block of words.

6.2 INPUT TRANSFERS

6.3 LOOPBACK TRANSFERS

Loopback transfers: how to verify the function of the line drivers and receivers.

6.4 PROGRAMMING EXAMPLES

Programming examples: actual program (real working program)

Low level program using peek/poke mode of the AFIDAD diagnostic:

Provide a typical example to show how input/output transfers can actually be performed. This should be beneficial to the OEM who likes to write their own driver. This is also a good tutorial for those in HP having to write or maintain the driver.

High level program using the supplied driver to do generic transfers (input/output). Including all different optional ioctl calls and their effects.

6.5 ERROR LIST

AFI driver's error list

6.6 ALTERNATE SOURCE

Please refer to the AFI Hardware/Software Interaction document for a high level program example plus other useful information.

27114A COMPATIBILITY

SECTION 7

Objectives

Features which are no longer available

New features and their backward compatible default modes

INTERNAL REFERENCE SPECIFICATION

SECTION 8

This is intended for the reader who must understand the card enough to support and maintain the hardware. This will substitute for the separate IRS.

8.1 GENERAL DESIGN ISSUES

FUSE: A discrete 4A fuse is used instead of a trace fuse due to the latter's large variance in rating. The overall current consumption of the card is estimated to be between 1.5A and 2.0A at 5V.

PULL-UP: All data lines on the card are pulled up to +5 volts via 2.2 Kohm resistors. This is done to provide a default value of 0 for each bit if the register being read does not drive the data line corresponding to that bit.

CLOCKING: A 20 MHz crystal oscillator is used to generate a clock for the FIFO control circuit. The CIO bus does provide a 14.7 MHz clock but this one is not useful in the design since it is too slow for the application. The clock driver is a 74LS125 with its enable input being grounded via a discrete resistor. This allows the 3065 tester to substitute a different clock more suitable to its operation.

8.1.1 Backplane Interface

BACKPLANE TIMING: The CIO backplane operates in one of two non-overlapping cycles: SYNC and POLL. The SYNC cycle is used to transfer data. Each SYNC cycle can have one or more IOSB strobes. Each data transfer is to take place with respect to the trailing edge of the IOSB signal. The address of each transfer is defined with the BP1/BP0/CBYT/CEND (register address), along with the card address. In the case of the data register, CBYT and CEND can be of any combination. These two are also used to indicate whether the transferred data unit is a byte (with CBYT) or the last one (CEND). The POLL cycle is used to determine if any CIO card is ready for a data transfer (service polls) or has interrupted recently (attention polls).

BACKPLANE TRANSCEIVERS: All backplane drivers and transceivers are selected such that they can drive a minimum of 48 mA. These include the 74ALS245-1 transceivers, the 74ALS240-1 buffers and the 74F38 open-collector NAND gates.

DECODER: A 10 output PAL (20L10) is used to decode register address for the 27114B card. This is barely enough as evidenced by the fact that registers A and B must shares two outputs (WRITEA and READA). Further decoding must be done for these two outputs. The READ0 and IOSB signals are also combined in the FIFO control circuit to detect the data reading pulse. Note that all write outputs are qualified with the IOSB signal whereas all read outputs are only qualified with the entire SYNC pulse.

POLL RESPONSE: The poll response function is implemented in the POL16L8 PAL. The UAD line is driven low by an open collector gate whenever the card is ready for a data transfer (service poll) or has interrupted (attention poll). This can be done in any POLL cycle.

In the output mode, poll responses are answered whenever there is room for 9 or more transfers in the FIFO. As the availability becomes less than 9 words, service polls are ignored (not answered). This term is defined with a sync'ed version of the HF and AEF. Since these two signals are latched with either trailing edge of POLL or IOSB, the poll response may still be answered even with 55 words already in the FIFO (but definitely not if there are 56 words or more in the FIFO).

The input poll response is similar to that of the output mode. The 27114B answers to polls whenever it has one or more words in its FIFO. In the case of 9 or more words in the FIFO, the HF and AEF outputs from a FIFO are used to force a poll response. When the number of available words drops below 9, the OR (output ready) of a FIFO is sampled with the leading edge of POLL for the poll answering purpose. Since the OR output of a FIFO is always deasserted low immediately after the SO leading edge which follows closely to the leading edge of IOSB, there is no possibility of falsely latching an OR condition as a ready (more word) when in fact there is are more valid words from the FIFO.

In the input mode, a set PEND flipflop will cause a poll response regardless of the state of the FIFO. This is done to make sure that even if the FIFO is full, the channel is going to do more data input. When the next data input is done, DEND is asserted on the CIO bus to tell the channel to terminate the transfer. The data remaining in the FIFO is considered to be garbage.

Attention polls are answered when both ARQ and ARE are high. This term is updated with each leading edge of SYNC (SARQ is the output from the SYNC latch). If the 27114B has been asserting the CIO's ARQ line (with an open collector gate) for 20 ns or more before the leading edge of an attention POLL, it will answer to that poll.

BURST REQUEST: The burst request output is normally tristated. It is driven to either an asserted or deasserted state only when the card is engaged in a data transfer to or from its input/output data register (SYNC cycles). The tristate signal is driven during the entire time the SYNC signal is asserted low and the card is addressed (any register) and is not in a hard reset state. The burst request signal is guaranteed to change only with the leading edge of SYNC or the trailing edge of IOSB.

Burst request is asserted only when the PEND signal is not asserted. The following description assumes that PEND is not asserted.

Burst request is handled differently in the input and output modes. In the output mode, burst request is asserted whenever there is room for 9 words or more. When the number of words in the FIFO reaches 55, the burst request output is turned off. If this coincides with the last transfer of a CIO burst, there will be no more output transfers (if the frontplane is inactive, the number of words in the FIFO will remain at 55). Otherwise, there could be as many as 3 more transfers before the channel finally stops. This is possible since the SHF (sync'ed half full) and SAEF (sync'ed almost empty/full) output of the sync latch is updated with the trailing edge of IOSB of the 56th word. As the channel sees the absence of BR (burst request) in the transfer corresponding to the 57th word, it can still add one extra transfer, the 58th word.

In the input mode, the burst request output is asserted whenever there are 9 or more words in the FIFO. When there are less than 9 words in the FIFO, the burst request output is driven to the deasserted state (high on CIO bus). This requires that the CIO channel do only one transfer per SYNC cycle. Similar to the output mode, the burst request output may not actually be turned off until there are only 8 words left in the FIFO. Consequently, there might be as few as 6 words left in the FIFO when a burst DMA has stopped. Note that the AEF output from a FIFO changes from high (asserted) to low immediately after the input of word #10. But since this signal is latched with the trailing edge of either IOSB or POLL, the burst request output is not updated until after word #9 has been read. Therefore, the channel sees this during the transfer of word #8, and it can still do one extra transfer to take word #7 out before stopping.

PEND FUNCTION: The CIO's DEND signal is driven by the 27114B whenever it is addressed in a SYNC cycle. The DEND signal is driven to a low level (assertion level) whenever the current transfer is considered by the card to be the last transfer.

In the input mode, this output is a function of the 17th data bit (bit #16) output from the FIFO. The corresponding input to the FIFO is taken from the frontplane's PEND receiver via a disable gate which is controlled by the PEND RESET bit in the AFI CONTROL2 register. The assertion level for this 17th data bit is low true. With the pull-up resistor, the signal is guaranteed to be false (high TTL level) unless it is driven by the FIFO's read register to a low level. All other register accesses (including the data output register) will float this to the deasserted level (high); therefore it cannot drive DEND to a low state on the CIO bus, even if the card is in the input mode.

In the output mode, PEND is asserted whenever the PEND flipflop is set. The setting of the PEND flipflop is done directly by the corresponding frontplane signal.

If the DEND signal is to be driven to the asserted level (low on CIO) during a data transfer (duration of an IOSB pulse), the burst request is driven to the deasserted level (high on CIO), regardless of the current state of the FIFO.

SYNC LATCH: The 74ALS874 synchronize latch is split into two sections: one is clocked with leading edges of POLL and the other is clocked with the trailing edges of either POLL or IOSB. CARQ, SARQ, IR (not used) and OR are latched with the leading edge of POLL. SDEND, SHF and SAEF are latched with the trailing edges of POLL or IOSB (it is very impractical to combine unlike edges from POLL and IOSB).

CARQ must be stable during any read from the register 1 (Sense register). Since an attention poll is always done between the assertion of the CIO's ARQ line and the time the interrupt service routine reads the register 1, it is guaranteed that the returned state of the ARQ flipflop is updated for the service. Without this sync action, the data bit corresponding to ARQ in register 1 could change at any time, including when the register is read.

SARQ must be updated for each attention poll so the leading edge of POLL is a very appropriate clock source.

OR must be updated at least with a POLL edge so that the card can respond to service polls when there are 9 or less data words in the FIFO. OR cannot be sampled with the trailing edge of IOSB since it may not have changed state in response to the leading edge of IOSB. OR must be updated with either edge of POLL. The leading edge of POLL is selected.

SDEND must be updated with each transfer. This signal is used to assert the CIO's DEND signal in the output mode. Since the PEND could be asserted at any time, the signal must be latched with a trailing edge of IOSB (the leading edge will not provide sufficient set-up time to the trailing edge for the burst request signal which must be turned off if DEND is asserted). The POLL edge in this case is of no use for this signal.

SHF and SAEF must be updated with both POLL and IOSB. They need to be updated with POLL to react to the case where there is no current data transfer (like from 56 words to 55 words in the output mode). They also need to be updated while a data transfer is happening (to turn off burst request).

HARD RESET: The hard reset flipflop is implemented with a feedback term in the POL16L8 PAL. The engineering note on page 7-59 of the HP-CIO STANDARD guarantees that a single data line can only be asserted during any address teaching operation. Therefore, this card will not be accidentally brought out of its hard reset state unless such an operation is done to it.

8.1.2 Interrupts

All interrupt sources must be cleared before an ARQ interrupt can be set again by any one of them. The ATTN interrupt can happen independent of the ATTN flipflop. This is done such that the 27114B will still be compatible with the 27114A card. The ATTN flipflop is used to register the frontplane interrupt just in case there is more than one interrupt source responsible for an interrupt. Both PEND and ZERO have their own interrupt mask bit. Both PEND and ATTN are sync'ed before being used.

There is no sync latch used for this PAL20R4. The four registered outputs are implemented as independent latches so they do not require the pre-sync'ing of the inputs. The ARQ flipflop is implemented as a feedback gate so there is no requirement for sync'ing either; though ARQ is routed through a gate external to the PAL to avoid race conditions.

An extra output of the PAL20R4 interrupt PAL is used to enable the frontplane data line drivers.

8.1.3 FIFO And Its Control Circuit

COUNTER: The counter circuit consists of three 8-bit counter chips to provide a count range from 0 to 16 Mbytes. The first two stages could have been wired to implement a synchronous count but the third one must use a ripple carry-out from the second stage any way. The ripple carry-out method is used to connect the three stages together. The decoding of register A and B is done using the different enable inputs of the counter chips. Since the carry-out output of the last stage is used as an output, it really doesn't matter what the count is as long as it is within 65535 of the maximum count. The maximum count is therefore restricted to 2**24-2**16. Note that the description in the ERS is the logical description of the actual hardware. The actual hardware counts up and a reset would clear the counter to zero.

FIFO CONTROLLER: The FIFO control function is done with the FIF22V10 FIFO PAL. All inputs to the PAL (except for the mode bit inputs) are synchronized with the same clock as the PAL itself. Before the mode bits can be changed, the frontplane handshake must be disabled.

Outputs OPCTL and IPCTL are OR'ed together to generate the PCTL signal. These two outputs are never asserted (low) at the same time. They are driven by two different state machines: shift-in and shift-out. The shift-in state machine drives PCTL when the card is in the output mode. The shift-out state machine drives PCTL when the card is in the input mode. The two outputs are inverted (with !) since it is easier to read the equation.

As NCRFF is asserted low, all flipflops in the PAL22V10 go to the preset state. Since both OPCTL and IPCTL outputs are of type 'pos', they become high instantly (the ! declaration does not affect the flipflop<-->output relationship). All other outputs are of type 'neg' by default. They become all low. Both state machine thus go to their idle state when NCRFF is asserted low. Without the declaration of type 'pos' for the OPCTL and IPCTL outputs, they would remain at the low level (asserted) as long as NCRFF is asserted. This could result in PCTL being asserted at the frontplane, an unacceptable condition.

FIFO SELECTION: The Cypress CY7C409 64X9 FIFO is selected here since it has two status outputs, HF (Half Full) and AEF (Almost Empty Full). The decoding of these two outputs can tell approximately how much data is in the FIFO; e.g. whether there is room for 9 more words or if at least 9 words are available. This allows the burst mode to be turned on constantly if there is room for more than 8 transfers. As the availability drops below this level, the data transfer is either turned off completely (output mode) or

changed to the non-bursting mode (input mode). The 8 word cushion provides plenty of time for the CIO channel to brake and stop without any data overrun or underrun problem.

Of the other FIFOs available on the market, only TI's 74ALS229A comes close to the Cypress chip. The 74ALS229A is configured as 16X4 which means 5 20 pin chips are required to implement what can be done with 2 28 pin (slim) chips, yet having only 16 levels of storage compared to the 64 levels of storage of the Cypress approach. The TI FIFO will also require a little more support circuitry to decode some condition like when the FIFO's capacity is within 2 of its limit.

FIFO TIMING: It is clearly shown that the timing from the FIFO circuitry is taken from only one of the two FIFO chips. This is quite acceptable since these outputs are not time critical. The HF and AEF outputs are very much the same from the two FIFOs (at most an offset of one word). The IR is guaranteed to be valid for all writes from the CIO side since the maximum number of words used in the FIFO will not exceed 58 in the output mode. The 200 ns cycle time of CIO is plenty to cover the shift-in pulse and the response for IR from both FIFO chips. The same reasoning can be applied for shift-in's from the frontplane side. OR has much the same story.

8.1.4 Frontplane Interface

EXTENSION OF PCTL: The PCTL signal can be stretched with one of 4 possible levels: 0 ns, 50 ns, 100 ns and 150 ns. The selection is made with a movable jumper to select one of four possible connections. The 0 ns position connects the PCTL output of the FIFO circuit directly to the PCTL line driver. The 50 ns, 100 ns and 150 ns positions connect the line driver's input to one of three registered outputs of the EXT16R6 PAL. These registered outputs form a shift register which propages the PCTL signal from the FIFO circuit. As soon as PCTL becomes deasserted high, all outputs become high with the next cycle. Effectively, a 50 ns delay is added for the trailing edge (assertion to deassertion) of PCTL in addition to the selectable (50, 100, 150 ns) delay for the leading edge of PCTL (deassertion to assertion).

FILTERING OF PFLG: As a precaution against excessive noise in some applications, a filtering circuit is added to remove unwanted pulses in the PFLG signal. The circuit consists of a jumper block which allows the selection of a PFLG signal filtering factor of 0 ns, 50 ns, 100 ns or 150 ns. The 0 ns filtering selection is basically a latch of the incoming PFLG signal (from the line receiver). The other selection requires that PFLG must change and be stable for an appropriate amount of time (50, 100 or 150 ns) before the change takes effect. The effect is such that if a temporary pulse is seen, the output remains unchanged. Only if the change lasts longer than the specified time will the output reflect the change. The implementation of this "filter" is done with a set-reset flipflop which is cleared any time the input is the same as the output (unless the zero filter option is selected). If the input is different than the output when the next clock edge arrives, this set-reset flipflop (Q1) is set. For the next two clock edges, two other flipflops are also set in a shift register manner. As all three flipflops become set, the output flipflop will switch to the current value of the input to the circuit. The instance that the input becomes the same as the output, the first (Q1) flipflop is cleared and the entire circuit must restart.

PFLG LABELING: The schematic shows J1/A14 and J1/B14 as being RPPFLG and RNPFLG, respectively. These net names refer to the polarity of the receiver chip inputs, U84/14 and U84/15, no the frontplane signals, PFLG- and PFLG+. The PFLG+ and PFLG- signal polarities are correct as shown in the ERS. The purpose of this apparent inversion is to eliminate an inverter gate from the circuit. Below is a list of corresponding signals, frontplane pins, and net names, in that order. PFLG+ = J1/B14 = RNPFLG (positive input) PFLG- = J1/A14 = RPPFLG (negative input)

LINE TERMINATION: To improve impedance matching, a 132 ohms equivalent load is used to terminate the line in the single-ended mode. The reference voltage load is still a 1.5K/3.3K which defines a

reference voltage between 1.4 V and 1.6 V. The layout of the board is done such that all positive signals go to the pin 2 through pin 9 side of the termination sockets. The pin out of the connector is the same as that of the 27114A card.

HEADER: A block of 6X48 double-pole headers is used to convert between differential (balanced) and single-ended (unbalanced) modes. 4 sets of these headers are not used but are provided since the selected Bergstick block (3X48, from Samtech) is a convenient one to use. For each signal, the corresponding frontplane connector pin goes to the middle pin of the jumper. The entire row on top of the middle row (depends on how the board is positioned) is grounded. The pins in the bottom row are connected to the corresponding line driver outputs or line receiver inputs. There is a space between the upper 3 rows and the lower 3 rows. The space is there to avoid the case that a user might mistakenly short out the entire row of signals to ground. The 3X48 header block closer to the frontplane connector corresponds to the inverted signals (-), and the other header block corresponds to the non-inverted signals (+).

To configure the frontplane in the balanced (differential) mode, the 12 jumper blocks (8 positions each) must be used to short out the middle pins and the pins which go to the receivers and drivers. To configure the frontplane in the low-true single-ended (unbalanced) mode, the lower row (further from the frontplane connector) must be switched to by-pass the frontplane connector signals to ground. This is done by repositioning all 6 (x8) jumper blocks such that they connect the middle pins to the ground pins. The inverted signals of the upper row should be allowed to go through between the frontplane and the line driver/receivers. This method should provide a fairly consistent characteristic impedance for all single ended lines, plus ample room for the ground return currents.

Besides the repositioning of the jumper blocks, care must be taken to replace the DIPs with the appropriate SIPs to maintain the impedance matching.

8.1.5 Control Registers

All write registers in the 27114B card are cleared with the hard reset condition. This is a must to assure that the new features will not be enabled when used with an older driver which only knows the 27114A card.

A 74ALS574 is used to implement the AFI Status register/lower byte. There is really no good reason why an inverted output latch couldn't have been used.

There is only one control bit used to define the selection of the PDIR and HEND option.

8.2 DECODER PAL20L10

```
module decoderpal
"original 10/28/88: 48F8
"11/14/88: XXXX Schematic version (some signals' polarity get inverted)
"12/09/88: 5F93 use bp1/cend/!cbyt/bp0 as reg address
"12/12/88: 5FA2 inverse cend/cbyt, use bp1/cbyt/cend/bp0
"12/12/88: 6056, nhardreset as qualifier, use bp1/!cbyt/cend/bp0
"02/10/89: 604c, pin 10 is used for 3065 test disabling of outputs.

flag '-r3'
title   'AFI REG ADDRESS DECODER PAL
        Revision 2.0 , Dec 12, 1988
        CS 604c'

DEC20L10        device 'P20L10';


     c,l,h,x,z = .C.,0,1,.X.,.Z.;

" inputs
bp1             pin     1 ; " high true
ncbyt           pin     2 ; " low true
cend            pin     3 ; " high true
bp0             pin     4 ; " high true
mypa            pin     5 ;
sync            pin     6 ;
doutnin         pin     7 ;
iosb            pin     8 ;
nhardreset      pin     9 ;
test3065        pin     10 ;

" outputs
nwrite0         pin     14 ;
nread0          pin     15 ;
nread1          pin     16 ;
nwrite1         pin     23 ;
nread3          pin     17 ;
nread7          pin     18 ;
nwrite7         pin     19 ;
nread9          pin     20 ;
nreadab         pin     21 ;
nwriteab        pin     22 ;

" unused I
nc11            pin     11 ;
nc13            pin     13 ;
```

```
equations
" all reads are not strobed with iosb
" all writes are strobed with iosb
" all outputs except nwrite0 are qualified with nhardreset

" Disable PAL when this input is grounded for 3065 testing.
enable nwrite0  = test3065 ;
enable nread0   = test3065 ;
enable nread1   = test3065 ;
enable nwrite1  = test3065 ;
enable nread3   = test3065 ;
enable nread7   = test3065 ;
enable nwrite7  = test3065 ;
enable nread9   = test3065 ;
enable nreadab  = test3065 ;
enable nwriteab = test3065 ;

!nread0   = nhardreset & mypa & sync & !bp1 & !bp0 & !doutnin ;

!nwrite0  = mypa & sync & !bp1 & !bp0 & doutnin & iosb;
" no !nhardreset since it is used to clear nhardreset

!nread1   = nhardreset & mypa & sync & !bp1 & ncbyt & !cend & bp0 & !doutnin;

!nwrite1  = nhardreset & mypa & sync & !bp1 & ncbyt & !cend & bp0 & doutnin
            & iosb;

!nread3   = nhardreset & mypa & sync & !bp1 & ncbyt & cend & bp0 & !doutnin ;

!nread7   = nhardreset & mypa & sync & !bp1 & !ncbyt & cend & bp0 & !doutnin;

!nwrite7  = nhardreset & mypa & sync & !bp1 & !ncbyt & cend & bp0 & doutnin
            & iosb ;

!nread9   = nhardreset & mypa & sync & bp1 & ncbyt & !cend & bp0 & !doutnin ;

!nreadab  = nhardreset & mypa & sync & bp1 & ncbyt & cend & !doutnin ;

!nwriteab = nhardreset & mypa & sync & bp1 & ncbyt & cend & doutnin
            & iosb;

end decoderpal
```

8.3 POLL RESPONSE PAL16L8

```
module polpal
" Original 10/31/88: 40A7
" ARQ/Service polls are limited to group 0
" Change 11/7/88: Adjust timing fsor poll response - Change effective FIFO
" length fsor the output mode to 55.
" 11/14/88: XXXX Schematic version
" 11/30/88: 18/19 pin swap; br active high
" 12/01/88: sarq is low true, from S38 44D2
" 12/01/88: preset low true 44E2
" 04/12/89: removed 'bpena' term from attn poll response eqn. 4462

flag '-r3'
title     'AFI HARDRESET/POLL RESPONSE/BURST REQUEST/DEND PAL
           Revision 1.0 , Nov 14, 1988
           CS 4462    '

POL16L8    device 'P16L8';


     c,l,h,x,z = .C.,0,1,.X.,.Z.;

" inputs
" Burst request group
shf          pin    1 ; " From a FIFO via poll/iosb latch
safe         pin    2 ; " From a FIFO via poll/iosb latch
" Hard reset group
nwrite0      pin    3 ; " From DEC20L10
iuad         pin    4 ; " From CIO
preset       pin    5 ; " From CIO, combination of ppon and nrst
" DEND group
sdend        pin    6 ; " DEND via poll/iosb latch
bd17         pin    7 ; " From FIFO, low true
" Poll response group
sir          pin    8 ; " From FIFO ckt via poll latch
sor          pin    9 ; " From FIFO ckt via poll latch
bp0          pin    11 ;
outnin       pin    13 ;
bpena        pin    14 ; " nreset is built into this input
sarq         pin    15 ; " Combination of are/arq, from poll latch, low true
bp1          pin    16 ;

" outputs
ouad         pin    12 ; " to Poll OC driver dsirectly
nhardrst     pin    17 ; " Hard reset output
dend         pin    18 ; " to TS driver
burstreq     pin    19 ; " to sync latch

equations
```

```
" Hard reset csircuit
!nhardrst     = (!nhardrst & !(!nwrite0 & !iuad)
              # preset) ;
" CIO spec guarantees that iuad is valid whenever nwrite0 is asserted,
" not just at the trailing edge (Eng. note 7-59)

" Poll response csircuit
" for output, response with 0-55 spaces:
ouad          = bpena & !bp1 & !bp0 & !safe
              # bpena & !bp1 & !bp0 & outnin & !shf
" and a forced response with DEND in output case:
              # bpena & !bp1 & !bp0 & outnin & sdend
" for input, cover the case of 56-64:
              # bpena & !bp1 & !bp0 & !outnin & shf
" and the case of 0-8:
              # bpena & !bp1 & !bp0 & !outnin & sor
" attention poll repsonse:
              # bp1 & !bp0 & !sarq ;
" sir is stable during poll/output transfer
" sor is stable during poll/input transfer
" ouad goes to open-collectsor gate which is qualified with poll

burstreq      = !safe & !(outnin & sdend # !outnin & !bd17)
               # !shf & outnin & !(outnin & sdend # !outnin & !bd17)
               # shf & !outnin & !(outnin & sdend # !outnin & !bd17) ;
" this output drives a TS buffer
" burst only when there are rooms for at least 8 transfers and DEND is
" not asserted.  Line driver must be external to PAL.
" both safe and shf are synced version of the outputs from a FIFO

dend          = outnin & sdend
" sdend is synced with IOSB/POLL
              # !outnin & !bd17 ;

end polpal
```

8.4 INTERRUPT PAL20R4

```
module intpal
" Original 11/7/88: XXXX
" ATTN ff is for 27114B.  Feed to ARQ must be done directly with !nattn.
" Change ARQ trigger condition such that in the B mode, DEND/WC interrupt
" can happen with FATTN being a high
" 11/14/88: Schematic version
" 12/01/88: separate clock edge/output and si/output for dend 7211
" 12/01/88: change nzero to pzero according to a new schematic 7212
" 12/14/88: change to 20R4 to get rid of potential problems of anomaly
" due to lack of sync latch for critical signal. ARQ and ARQ1 are now
" of non-registered type 6EEF.
" 12/30/88: 6eef, changed fpena to !fpena since '576 inverts it.
" 1/13/89: fpena is not inverted (not sync by 576), 6EEF
" 1/24/89: invert the sense of driverena such that a normal high at pin
" B10 would disable drivers (with a low).  With loopback, a low B10
" inverts everything (6A35)
" 02/06/89 take out ncrff, use input for extra delay (arq1 feedback is
" done externally) (6AED)
" 02/10/89: 6fa7, fpena sync'd and inverted to !fpena.
" and change driverena output to !driverena.
" 02/22/89: 6FC9, invert sense of fpend input (use of 822)
" take pzero out of fphsena term (pzero is actually a combo of pzero
" and pctl).
" 02/24/89 driverena output must be low when card is in output mode and fp
" is enabled 6A8F


flag '-r3'
title     'AFI ATTN/ARQ/DEND
           Revision 2.0 , Feb 24, 1988
           CS 6A8F    '

INT20R4    device 'P20R4';


     c,l,h,x,z = .C.,0,1,.X.,.Z.;

" inputs
" DEND circuit
outnin          pin    2 ; " direction control
ndendrst        pin    3 ; " low true
si              pin    4 ; " from FIF22V10
!fdend           pin    5 ; " from fp receiver
" ARQ circuit
dendena         pin    6 ; " dend interrupt enable
zeroena         pin    7 ; " from control register
pzero           pin    8 ; " from counter
nread9          pin     9 ; " from DEC20L10
```

```
nattnena        pin     10 ; " from control register
nattn           pin     11 ; " from fp receiver
!fpena          pin     14 ; " from control register after sync
darq1           pin     23 ; " delayed arq1, same phase

"enable
grd11           pin     13 ;

" outputs
fphsena         pin     15 ; " low true
arq1            pin     16 ; " ARQ state machine
attn            pin     17 ;
qnattn          pin     18 ;
dend            pin     19 ; " DEND output
qdend           pin     20 ; " DEND state machine
arq             pin     21 ; " ARQ output
driverena       pin     22 ;

equations
" FP handshake enable
!fphsena        = !dend & "!pzero & "fpena ;
!driverena       = "!dend & !pzero &" fpena & outnin;

" ATTN flipflop (for 27114B application only)
qnattn          := nattn ;
attn            := attn & !nattnena
                #  !nattn & !nattnena & qnattn ;

" DEND
qdend           := fdend ;
dend            := fdend & !qdend & ndendrst & outnin
" for output, use edge of dend
                #  fdend & !outnin & ndendrst & si
" for input, use si
                #  dend & ndendrst ;
" maintain until being reset
"dend            := fdend & !qdend & ndendrst & (outnin # si)
"                #  dend & ndendrst ;

!arq = !arq & nread9
" maintain if set until !nread9
    # darq1 & (!nattn & !nattnena & attn # dend & dendena # pzero & zeroena);
"   # arq1 & (!nattn & !nattnena & attn # dend & dendena # pzero & zeroena);
" set if an edge is observed of the possible interrupt conditions
!arq1 = !nattn & !nattnena & attn # dend & dendena # pzero & zeroena ;
" a delayed version of the possible interrupt conditions

end intpal
```

8.5 STATE MACHINE PAL22V10

```
module  fifopal
" 10/18/88: Original
" 10/21/88: Full/master, Full/slave, Fifo X Input, Output X FP, BP
" 10/27/88: 95A4, add d!noutnin to CIO handshake to eliminate false
" handshake in case of CIO read data in output mode and vice versa.
" 10/28/88: 855D, change to nread0/iosb/nwrite0 from strdata/d!noutnin
" 11/7/88: XXXX, combine iosb and nread0, output oclock to clock
" ir/or for backplane sync purpose
" 11/11/88: XXXX, invert sense of ipctl and opctl
" 11/27/88: 6740, correct sense of qpflg and iosbrd0
" 12/06/88: 8207, change to pos: opctl,ipctl. This forces pctl to low
" when card is reset (opctl/ipctl to high).
" 12/07/88: state ishiftin: branch to iwait if slave/full 9577
" 12/21/88: fpena input inverted to !fpena so it won't be delayed an
" extra clock cycle by the '576.
" 12/21/88: 958A, !pcrff changed to pcrff since '576 inverts signal.

" the following must be implemented for the actual PC board version
" 12/07/88: xxxx, NCRFF now goes through 576 (inverted output)
" 02/05/89: add nzero pin, used to disable (in place of the hidden
" zero component in fphsena which is now qualified with pctl)
" 02/10/89: a418, pins 16 and 19 swapped to accomodate extra terms.
" 02/13/89: add strobe/master/input; strobe/master/output
" (must declare oq2 [and oq1,iq2,iq1] to be of type pos) 7478
" 02/23/89: change state definition such that PAL wakes up in
" iidle and oidle.  B6D5

flag    '-r3'

title   '
        AFI FIFO CONTROL PAL22V10
        REV= 1.0 Nov 14, 88
        CS = B6D5
        '
FIF22V10   device 'P22V10';

" inputs
aclock          pin     1       ; " 20 MHz clock
nir             pin     2       ; " ir from '576
nor             pin     3       ; " or from '576
write0          pin     4       ; " nwrit1 via '576
mode0           pin     5       ; " mode definition, direct from AFI CTL2
mode1           pin     6       ;
mode2           pin     7       ;
pcrff           pin     8       ; " master reset: crff, high true
!fpena          pin     9       ; " handshake ena, from INT20R4
npflg           pin     10      ; " PFLG via '576
noutnin         pin     11      ; " xfer direction
```

```
qpflg          pin     13      ; " delayed version of PFLG
iosbrd0        pin     14      ; " strobed version of nread0, high true
nzero          pin     23      ;

" outputs
oq2            pin     15      ;
!opctl         pin     16      ; " ipctl and opctl are combined to gen pctl
!ipctl         pin     17      ; " ipctl and opctl are combined to gen pctl
iq1            pin     18      ;
iq2            pin     19      ;
so             pin     20      ; " SO to FIFO's
si             pin     21      ; " SI to FIFO's
oq1            pin     22      ;

aclear,sset    Node 25, 26     ; " as applied to 'pos' output
" node 25: asynchronous clear 'pos' outputs to low
" node 26: synchronous set 'pos' outputs to high

ipctl, opctl    istype 'pos'    ; " a set guarantees these to be high
oq2,oq1,iq1,iq2 istype 'pos'    ; " a set guarantees these to be high
"other 'neg' outputs are 'set' to 0 (idle)

" Operating mode definition
mode        = [mode2, mode1, mode0];
fifo        = 000 ;     " 0 FIFO mode (current AFI mode)
fullmaster  = 001 ;     " 4 full mode, master
fullslave   = 011 ;     " full mode, slave
strmaster   = 101 ;     " strobe mode, master
strslave    = 111 ;     " strobe mode, slave

"
" Overview:
" There are two state machines in this PAL: shift-in and shift-out
" In input transfers, Shift-in monitors PFLG and drives both PCTL
" and SI while Shift-out controls SO according to the activity of STRDATA
" In output transfers, Shift-out uses SI to clock data in the FIFO
" with each strobe of STRDATA and Shift-in controls PCTL and SO to
" handshake with PFLG

" Shift-in state machine.
" State definition: si is a 1 only in the shiftin state
" This bit is used to drive the SI inputs of the FIFO's
istate      = [iq2, iq1, si] ;
"iidle       = 000 ;
iidle       = 110 ;
ictlout     = 100 ;
isetup      = 010 ;
ishiftin    = 011 ;
iwait       = 000 ;

" Shift-out state machine.
" State definition: so is a 1 only in the shiftout state
" This bit is used to drive the SO inputs of the FIFO's
ostate      = [oq2, oq1, so] ;
```

```
"oidle      = 000 ;
oidle       = 110 ;
octlout     = 100 ;
osetup      = 000 ;
oshiftout   = 011 ;
owait       = 010 ;

equations
sset      = pcrff;
aclear    = 0 ;

"**********************************
"*      Shift-in state machine    *
"**********************************
state_diagram [iq2, iq1, si]

"*****************************************************************
state iidle:
" Reset state
" Slave-full input

ipctl := 0 ;

if (nzero & fpena & !npflg & noutnin & (mode == fullslave)) then isetup
" full/slave: goto isetup when pflg is asserted
else if (nzero & fpena & npflg & noutnin & !nir & (mode == fullmaster)) then
  ictlout
" full/master: goto ictlout, assert ctl and wait for !npflg
else if (nzero & fpena & noutnin & !nir & (mode == fifo)) then ictlout
" fifo/master: goto ictlout w/o looking at !npflg
else if (nzero & fpena & noutnin & !nir & (mode==strmaster)) then ictlout
" strobe/master: goto wait, assert pctl
else if (!noutnin & write0) then isetup
" strobed output data from CIO: allowed only in output mode
else iidle;

"*****************************************************************
state ictlout:

ipctl := noutnin ;
" qualified with noutnin so as not to interfere with the other s.m.

if (!npflg & (mode == fullmaster)) then isetup
else if (!npflg & (mode == strmaster)) then isetup
" wait for high pflg then shiftin and complete
else if (!npflg & !qpflg & (mode == fifo)) then isetup
    " look for edge of !npflg in fifo mode
else ictlout ;

"*****************************************************************
state isetup:
" allow set up time for input data
" is one clock sufficient?
```

```
ipctl := ipctl & noutnin ;

if (!nir & noutnin) then ishiftin    " test for !nir in full/slave mode
          " it should be true for full/master and fifo modes
else if (!write0 & !noutnin) then ishiftin
    " wait for trailing edge of nwrite0 before shift in
else isetup;

"*************************************************************
state ishiftin:
" the only state which has si == 1

ipctl := ipctl & noutnin ;

if (noutnin & (mode == fullslave)) then iwait
" goto iwait to wait for !pflg in full/slave
else iidle ;
" back to iidle for full/master, fifo and CIO

"*************************************************************
state iwait:

ipctl := (mode == fullslave) & noutnin ;    " for slave full

" wait here until !npflg == 0 (full mode)
" if (npflg # (mode == fifo)) then iidle
if npflg then iidle
" in fifo mode, never mind !npflg
else iwait;

"***********************************
"*      Shift-out state machine    *
"***********************************
state_diagram [oq2, oq1, so]
" to cut complexity, opctl doesn't have to be qualified with !noutnin
" unless it is a special circumstance

state oidle:
" Idle state for the shift-out state machine

opctl := 0 ;

if (nzero & fpena & !noutnin & !nor & npflg & (mode == fullmaster)) then
  octlout
" full/master mode
else if (nzero & fpena & !noutnin & !nor & (mode == fullslave)) then octlout
else if (nzero & fpena & !noutnin & !nor & (mode == fifo)) then octlout
else if (nzero & fpena & !noutnin & !nor & (mode == strmaster)) then octlout
else if (noutnin & !nor & iosbrd0) then oshiftout
" strobed input data from CIO: allowed only during input mode
else oidle ;

"*************************************************************
state octlout:
```

```
opctl := !noutnin & (mode == fullmaster) # !noutnin & (mode == fifo)
        # !noutnin & (mode == strmaster) ;

goto owait ;

"*****************************************************************
state owait:

opctl = opctl & !noutnin ;

if (!npflg & (mode == fullmaster)) then oshiftout
else if (!npflg & !qpflg & (mode == fifo)) then oshiftout
" edge detection for !npflg
else if (!npflg & (mode == fullslave)) then oshiftout
else if (!npflg & (mode == strmaster)) then oshiftout
else owait ;

"*****************************************************************
state oshiftout:
" the state assignment must be done such that only this state can set so

opctl = (mode == fullslave) & !noutnin ;

if (npflg & !noutnin) then oidle
else if (!noutnin & (mode == fifo)) then oidle
else if (!noutnin & (mode == strmaster)) then oidle
else if (!iosbrd0 & noutnin) then oidle
else oshiftout ;

end fifopal
```

8.6 HANDSHAKE EXTENSION PAL16R6

```
module extpal
" Original 11/30/88: 41C8
" 12/01/88: use pctlin to turn off pctl1/2/3 49BC
" 12/02/88: 3,4,5 pin rotation
" 12/02/88: invert sense of pflg output 4981
" 02/10/89: 4961, use pin 9 for 3065 testing to disable output 12 and 19.
" 04/20/89: 4A1E, added external clock delay path, pins 8 & 12.

flag '-r3'
title     'AFI PCTL DELAY/PFLG FILTERING
           Revision 1.0 , Nov 30, 1988
           CS 4A1E    '

EXT16R6     device 'P16R6';


     c,l,h,x,z = .C.,0,1,.X.,.Z.;

" inputs
clock20   pin    1 ; " 20 MHz clock
clock     pin    2 ; " 20 MHz clock
pflgin    pin    5 ; " PFLG after EDGE XOR gate
zero      pin    3 ; " jumper 0
one       pin    4 ; " jumper 1
pctlin    pin    6 ; " from NAND gate
two       pin    7 ; " jumper 2
delayin   pin    8 ; " externally delayed delayout

"enable
ground    pin   11 ; " ground this to enable Q outputs
test3065  pin    9 ; " ground this to disable outputs

" outputs
delayout  pin   12 ; " delayed version of clock
pctl3     pin   13 ; " to switch 3 of PCTL
pctl2     pin   14 ; " to switch 2 of PCTL
pctl1     pin   15 ; " to switch 1 of PCTL
!pflgout  pin   16 ; " to FIF22V10 and 74ALS576 (do not sync again)
q2        pin   17 ; " internal state of PFLG filter
q3        pin   18 ; " internal state of PFLG filter
q1        pin   19 ; " internal state of PFLG filter


equations
" disable outputs when test3065 is grounded for 3065 testing
enable delayout  = test3065 ;
enable q1        = test3065 ;
```

```
" pflg filtering
delayout = clock ;
" used to generate a clock edge pulse
q1       = q1 & (pflgout & !pflgin # !pflgout & pflgin)
         # clock & !delayin
         # !zero ;
" assert q1 with clock edge if input <> ouput; clear instantly
q2       := q1 # (!one) ;
q3       := q2 # (!two) ;
" ring counter
pflgout := pflgout & (!q1 # !q2 # !q3) # pflgin & q3 & q2 & q1 ;
" Maintain if any q is false.  Update if they are all true.

pctl1  := pctlin ;
pctl2  := pctl1 & pctlin ;
pctl3  := pctl2 & pctlin ;
" ring counter

end extpal
```

Table of Contents

Section 5
THEORY OF OPERATION