64000

HP64000 Logic Development System

Model 64110A Mainframe

HEWLETT PACKARD

CERTIFICATION

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

WARRANTY

This Hewlett-Packard system product is warranted against defects in materials and workmanship for a period of 90 days from date of installation. During the warranty period, HP will, at its options, either repair or replace products which prove to be defective.

Warranty service of this product will be performed at Buyer's facility at no charge within HP service travel areas. Outside HP service travel areas, warranty service will be performed at Buyer's facility only upon HP's prior agreement and Buyer shall pay HP's round trip travel expenses. In all other cases, products must be returned to a service facility designated by HP.

For products returned to HP for warranty service. Buyer shall prepay shipping charges to HP and HP shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to HP from another country.

HP warrants that its software and firmware designated by HP for use with an instrument will execute its programming instructions when properly installed on that instrument. HP does not warrant that the operation of the instrument, or software, or firmware will be uninterrupted or error free.

LIMITATION OF WARRANTY

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside of the environmental specifications for the product, or improper site preparation or maintenance.

NO OTHER WARRANTY IS EXPRESSED OR IMPLIED. HP SPECIFICALLY DISCLAIMS THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

EXCLUSIVE REMEDIES

THE REMEDIES PROVIDED HEREIN ARE BUYER'S SOLE AND EXCLUSIVE REMEDIES. HP SHALL NOT BE LIABLE FOR ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, WHETHER BASED ON CONTRACT, TORT, OR ANY OTHER LEGAL THEORY.

ASSISTANCE

Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.

For any assistance, contact your nearest Hewlett-Packard Sales and Service Office. Addresses are provided at the back of this manual.

CW&A 2/81

HEWLETT-PACKARD

SERVICE MANUAL

MODEL 64110A
MAINFRAME

SERIAL NUMBERS

This manual applies directly to models with serial numbers prefixed 2103A - 2138A.

©copyright Hewlett-Packard Company/Colorado Springs Division 1982
1900 Garden of the Gods Road, Colorado Springs, Colorado, U.S.A.

All Rights Reserved

Manual Part Number 64110-90901
Microfiche Part Number 64110-90801 PRINTED: MARCH 1982

SAFETY SUMMARY

The following general safety precautions must be observed during all phases of operation, service, and repair of this instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the instrument. Hewlett-Packard Company assumes no liability for the customer's failure to comply with these requirements.

GROUND THE INSTRUMENT.

To minimize shock hazard, the instrument chassis and cabinet must be connected to an electrical ground. The instrument is equipped with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE.

Do not operate the instrument in the presence of flammable gases or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS.

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE.

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

USE CAUTION WHEN EXPOSING OR HANDLING THE CRT.

Breakage of the Cathode-ray Tube (CRT) causes a high-velocity scattering of glass fragments (implosion). To prevent CRT implosion, avoid rough handling or jarring of the instrument. Handling of the CRT shall be done only by qualified maintenance personnel using approved safety mask and gloves.

DO NOT SUBSTITUTE PARTS OR MODIFY INSTRUMENT.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the instrument. Return the instrument to a Hewlett-Packard Sales and Service Office for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

Dangerous voltages, capable of causing death, are present in this instrument. Use extreme caution when handling, testing, and adjusting.

SS-2-1/76

TABLE OF CONTENTS

TABLE OF CONTENTS

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS

List of Tables

LIST OF TABLES

List of Tables

SECTION I

GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. This manual contains technical information and theory necessary to install, maintain, and troubleshoot the Model 64110A mainframe. This information describes the overall system and how the various components relate to one another with the emphasis on troubleshooting and repair.

1-3. The manual is organized into eight sections: Section I introduces the reader to the manual and gives a brief physical description of the 64110A mainframe. Section II describes the installation, removal and handling procedures. Section III discusses operation and Section IV describes performance tests. Section V contains adjustment procedures. Section VI lists the replaceable parts and Section VII contains backdating information needed to make this manual applicable to older instruments. Section VIII presents theory of operation and troubleshooting of the mainframe.

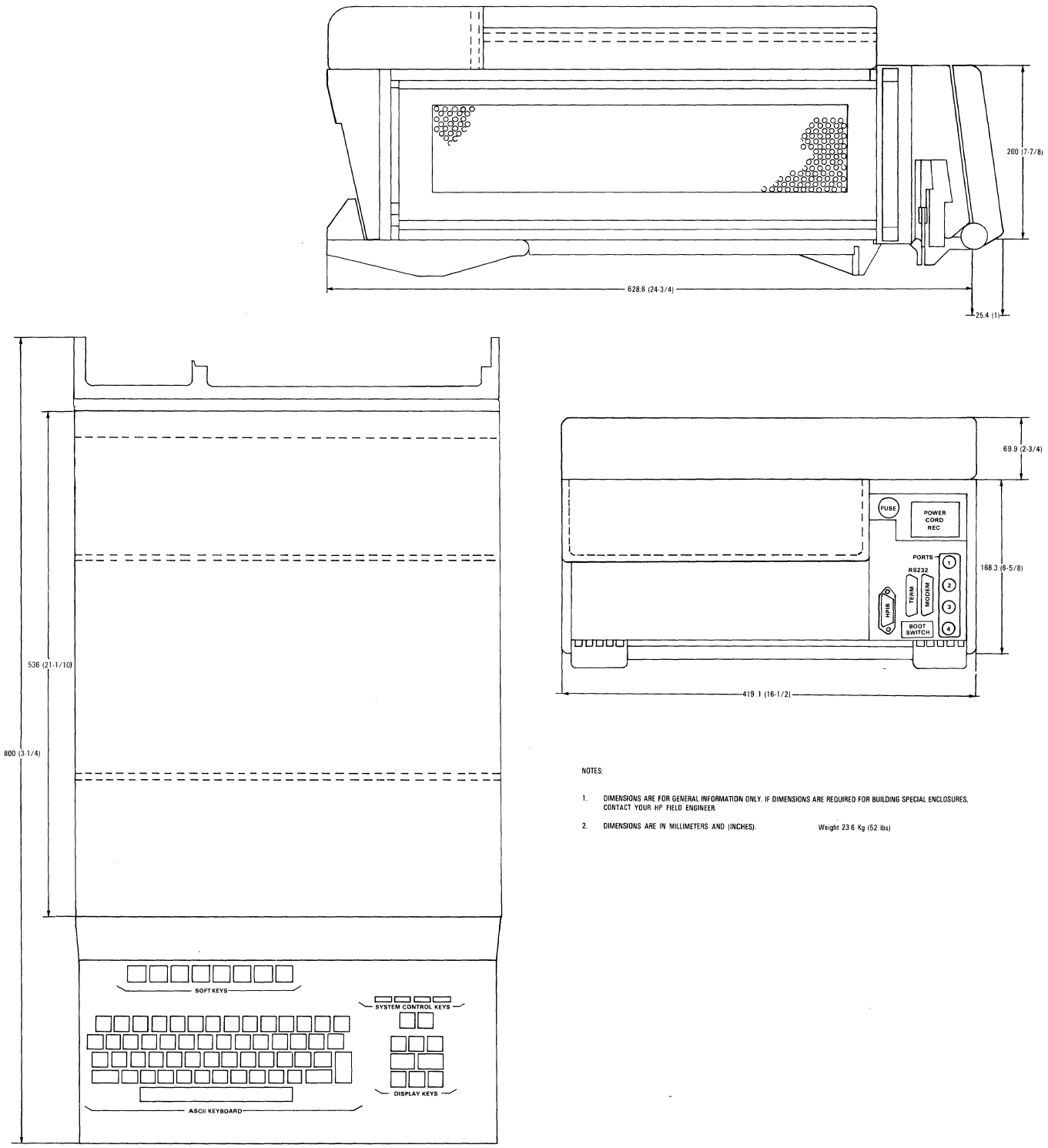
1-4. SAFETY CONSIDERATIONS.

1-5. This product is a Safety Class 1 instrument provided with a protective earth terminal. The instrument and manual should be reviewed for safety markings and instructions before operation.

1-6. PHYSICAL DESCRIPTION.

1-7. The 64110A is a transportable mainframe with integral accessory storage. It has a high resolution 9 inch CRT display which is protected during transportation by the foldup keyboard. The standard cabinet feet are extendable for both bench and vertical operation.

1-8. The flexible disc drive and option slots allow a variety of analysis configurations and if fitted with the rack mount option, using HP-IB or RS-232C interfaces, the Model 64110A can be used in automated test applications. The mainframe dimensions are given in figure 1-1.



NOTES:

1. DIMENSIONS ARE FOR GENERAL INFORMATION ONLY. IF DIMENSIONS ARE REQUIRED FOR BUILDING SPECIAL ENCLOSURES, CONTACT YOUR HP FIELD ENGINEER.
2. DIMENSIONS ARE IN MILLIMETERS AND (INCHES). Weight 23.6 Kg (52 lbs)

Figure 1-1. Mainframe Dimensions

1-9. MAINFRAME CONFIGURATION.

1-10. Figure 1-2 shows the configuration of the mainframe. The major areas of the mainframe are:

CRT Display	CPU/IO Board
Keyboard	Display Controller Board
Rear Panel	Display Driver Boards (2)
Cardcage	Local Mass Storage/RS-232C Board
Power Supply	Local Mass Storage Unit

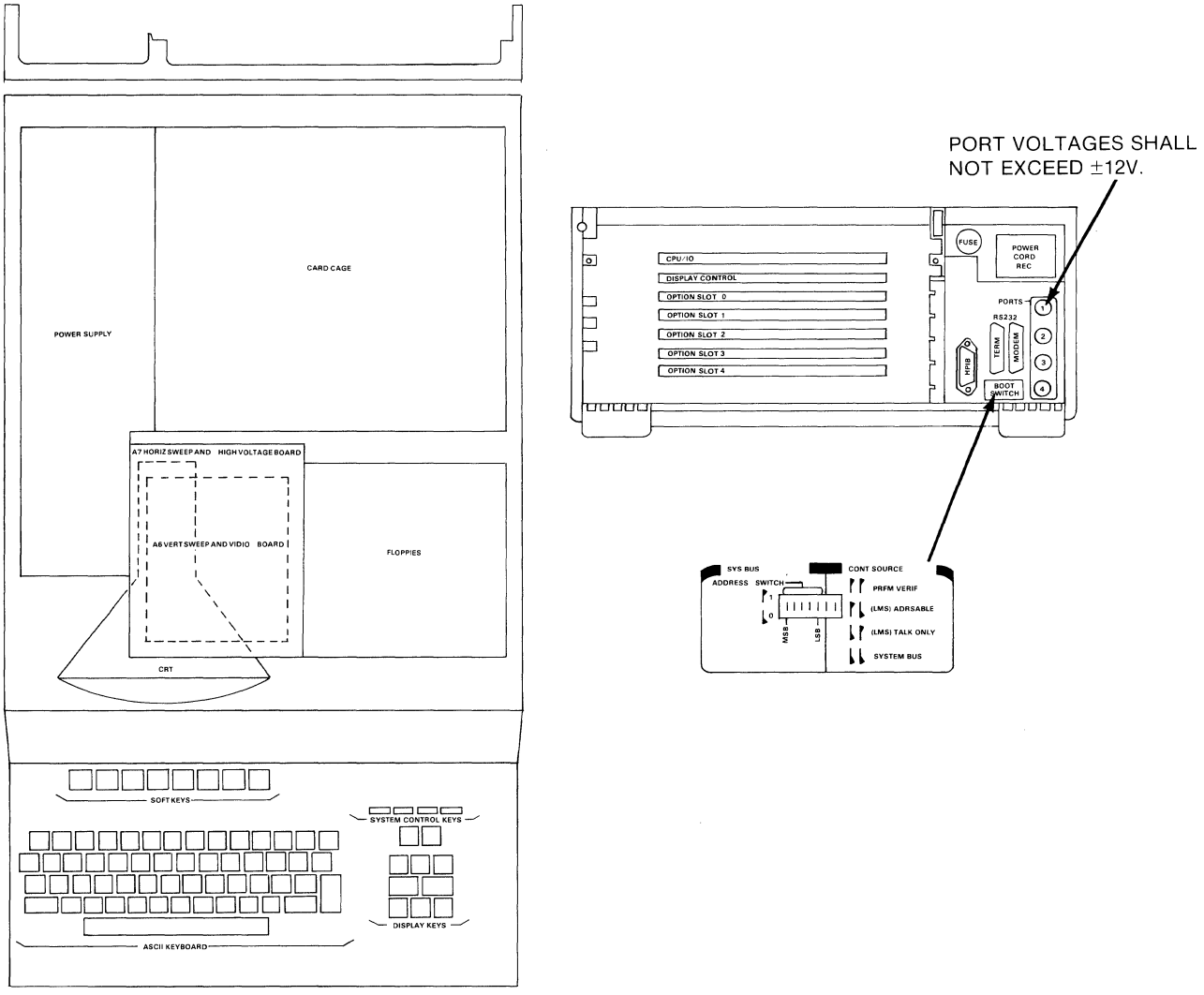


Figure 1-2. Mainframe Configuration

1-11. The four areas of the rear panel are power input, HP-IB system interface bus, RS-232C serial interface, and system control source. The power functions are at the top of the rear panel.

1-12. There are seven printed circuit board slots. See figure 1-2. The top two slots have printed circuit boards installed at the factory. These boards must be installed in the order given for the Model 64110A to operate. The two required boards are:

CPU/IO in slot A
Display Controller in slot B

1-13. The printed circuit boards interface through the motherboard at the back of the card cage, and through cables connecting the CPU/IO board to the keyboard,flexible disc drive/RS-232C board and rear panel board. A cable also connects the flexible disc drive/RS-232C board to the rear panel board.

1-14. For convenience, board identifier labels for the top two boards are located on the right hand side, between the rear panel and the cardcage. The five option slots are numbered 0-4.

1-15. There is a limit to the number and types of option boards that may be installed in the cardcage without exceeding the capability of the power supply. This limit is determined by the amount of available current from the power supplies. Refer to the installation section, Section II, for the determination of the power limitations.

1-16. INSTRUMENTS COVERED BY THIS MANUAL.

1-17. Attached to the instrument is a serial number plate. The serial number is in the form: 0000A00000. It is in two parts; the first four digits and the letter are the repair prefix and the last four digits are the suffix. The prefix is the same for all identical instruments; it changes only when a change is made to the instrument. However, the suffix is assigned sequentially and is different for each instrument. The contents of this manual apply to instruments with serial number prefix(es) listed under SERIAL NUMBERS on the title page.

1-18. An instrument manufactured after the printing of this manual may have a serial number prefix that is not listed on the title page. This unlisted serial number prefix indicates the instrument is different from those described in this manual. The manual for this newer instrument is accompanied by a yellow Manual Changes supplement. This supplement contains "change information" that explains how to adapt the manual to the newer instrument.

1-19. In addition to change information, the supplement may contain information for correcting errors in the manual. To keep this manual as current and accurate as possible, Hewlett-Packard recommends that you periodically request the latest Manual Changes supplement. The

supplement for this manual is identified with the manual print date and part number, both of which appear on the manual title page. Complimentary copies of the supplement are available from the Hewlett-Packard sales/service office.

1-20. For information concerning a serial number prefix that is not listed on the title page or in the Manual Changes supplement, contact your nearest Hewlett-Packard sales/service office.

1-21. MAINFRAME OPTIONS.

1-22. The mainframe options are the options available from the factory when ordering a mainframe. These do not include analysis options such as state and timing.

Table 1-1. Mainframe Options

Model 64110A	Logic Development System with Flexible Disc Drive
Option 032	Includes Host RAM Expansion
Option 034	Includes Accessories Pouch

1-23. ANALYSIS OPTIONS.

1-24. There are many possible options and configurations including State and Timing Analysis. Refer to the 64000 Configuration Guide, available at any Hewlett-Packard sales/service office, for possible configurations.

1-25. RACK MOUNTING.

1-26. The 64110A can be rack mounted. It requires a standard HP SYSTEM-II, 7H rack mount kit. Refer to the Hewlett-Packard Catalog for ordering information.

1-27. ACCESSORIES SUPPLIED.

1-28. A list of accessories supplied with this mainframe is contained in table 1-2.

Table 1-2. Accessories Supplied

Accessory	Part Number
Power Cord	See table 2-2
Operating Manual	64110-90902
Service Manual	64110-90901
Operating System On Flexible Disc	64110AF

1-29. ACCESSORIES AVAILABLE.

1-30. The Service Tool Kit, part number 64110-68701, contains all the accessories shown in table 1-3, except the power supply test board.

Table 1-3. Accessories Available

Accessory	Part Number
Extender Board	64110-66503
Flexible Disc Drive Extender Cable	64110-61620
Flexible Disc Drive Extender Cable	64110-61621
Flexible Disc Drive Extender Cable	64110-61622
I/O Extender Cable	64110-61618
Power Supply Flexible Extender	64110-66520
Power Supply Test Board	64110-66519
Rear Panel Cable Extender	64110-66522
RS-232C Extender Cable	64110-61619

1-31. RECOMMENDED TEST EQUIPMENT.

Table 1-4. Recommended Test Equipment

HP 5004A or 5005A Signature Analyzer
Digital voltmeter capable of .01 V resolution
Oscilloscope
Standard hand tools for electronic printed circuit board repair

1-32. LEVEL OF SERVICE.

1-33. This is a Preliminary Component Level Manual. It contains information that provides component level servicing of the Model 64110A. Detailed schematics, theory of operation and Signature Analysis loops are provided in Section VIII.

SECTION II

INSTALLATION

2-1. INTRODUCTION.

2-2. This section contains information for unpacking, initial inspection, and installation of the Model 64110A Logic Development System mainframe.

2-3. INITIAL INSPECTION.

a. Unpack the mainframe.

b. Keep the shipping carton and cushioning material until the contents have been checked. The carrier will want to inspect the shipping materials if a claim is made.

c. Check the mainframe mechanically and electrically. The electrical performance verification is given in Section IV.

d. If the contents are not complete, there is mechanical damage or defect, or it does not pass the performance verification test then notify the carrier as well as the Hewlett-Packard sales-service office. HP will arrange for repair or replacement at its option without waiting for the claim against the carrier to be settled.

2-4. POWER REQUIREMENTS.

2-5. The Model 64110A requires 110 or 220 VAC (+-15%) at 48-66 Hz. The line voltage selector switch is located along the left side, under the side cover. The fuse required is a non-delay type of 8 A for the 110 V and 4 A for the 220 V. The power on/off switch is a push type labeled LINE and is located at the top left corner of the front panel.

```
********************** CAUTION **********************
*                                                   *
*  The instrument can be damaged if the line voltage  *
*  switch  is not set to  the correct input voltage.  *
*                                                   *
*****************************************************
```

2-6. POWER REQUIREMENTS WORKSHEET.

2-7. There is a limit to the number and types of option boards that may be installed in the cardcage without exceeding the capability of the power supply. This limit is determined by the amount of available current from the power supply. Table 2-1 lists the power supply loads for the basic mainframe with the mandatory mainframe boards installed. Refer to the flexible disc drive appendix of this manual for its power usage and fill in the current values in table 2-1. Subtract the total of the mainframe plus the flexible disc drive to determine the available current for remaining options. Space has been left to do calculations in the manual.

Table 2-1. Power Requirements Worksheet

	-3.25 V	-5.20 V	+5.00 V	+12.00 V	-12.00 V	+12.00 VDD
AVAILABLE CURRENT	see note	see note	30.00 A	4.50 A	1.00 A	1.50 A
REQUIRED CURRENT						
Mainframe w/floppy	0.00 A	0.01 A	5.70 A	2.80 A	0.01 A	1.11 A
Option 1						
Option 2						
Option 3						
Option 4						
Option 5						
TOTAL REQUIRED						

NOTE. Sum of -3.25V and -5.20 V available current is 20.0 amperes.

2-8. POWER CORD.

2-9. The proper power cord is listed by mainframe option number in table 2-2. If the appropriate power cord is not included with the instrument, notify the nearest HP sales/service office and a replacement cord will be provided.

Table 2-2. Power Cord Options

Location	Part Number
USA	8120-1378
Great Britian	8120-1351
Australia	8120-1369
Europe	8120-2857
Switzerland	8120-2104
Denmark	8120-2957

2-10. SITE SELECTION AND SYSTEM BUS OPERATION.

2-11. The Model 64110A is a transportable mainframe and may be used as a stand alone unit or as part of an HP-IB or RS-232C bused system. Refer to the Operation Reference Manual for specific information.

2-12. OPERATING ENVIRONMENT.

2-13. The Model 64110A may be operated in environments within the limits shown below. It should be protected from temperature extremes which cause condensation within the instrument.

Temperature.....+10 to +44 degrees Celsius
Humidity.....20 to 80% relative humidity
Altitude.....4 600 m (15 000 ft)

2-14. STORAGE ENVIRONMENT.

2-15. The Model 64110A may be stored or shipped in environments within the following limits:

Temperature.....-40 to +70 degrees Celsius
Humidity.....20 to 80% relative humidity
Altitude.....15 300 m (50 000 ft)

2-16. ORIGINAL PACKAGING.

2-17. Containers and packing materials identical to those used in factory packaging are available through Hewlett-Packard sales and service offices.

2-18. OTHER PACKAGING.

2-19. The following general instructions should be used for repacking with commercially available materials:

a. Wrap the Model 64110A in heavy paper or plastic.

b. Use a strong shipping container. A double-wall carton made of 350 pound test material is adequate.

c. Use a layer of shock absorbing material 70 to 100 mm (3 to 4 inch) thick around all sides of the 64110A to provide firm cushioning and prevent movement inside the container.

d. Seal shipping container securely.

e. Mark shipping container FRAGILE to ensure careful handling.

f. In any correspondence, refer to the instrument by model number and full serial number.

2-20. ASSEMBLY AND DISASSEMBLY.

2-21. Specific procedures for assembly and disassembly of the 64110A mainframe can be found in Section VI, Replaceable Parts.

SECTION III

OPERATION

Complete operation of this system from the keyboard is described in the Model 64110A Operating Reference Manual and is not duplicated in this service manual.

SECTION IV

PERFORMANCE TESTS

4-1. INTRODUCTION.

4-2. This section describes the mainframe performance verification (PV) power-up sequence and tests.

4-3. The mainframe PV is a series of tests resident in the mainframe that confirm correct operation of the mainframe hardware and firmware. The PV can be started at any time using the rear panel switches. It can also be started from the front panel when the operating system has been loaded and a disc drive is connected.

4-4. The mainframe power-up mode is determined by the positions of the control source switches on the rear panel.

a. When the switches are set to performance verification, the system will power-up with the performance verification display test on the screen.

b. When the source switches are set to either of the local mass storage modes the display will read "SELF TEST COMPLETE".

c. When the switches are in the system bus mode, the power-up is from disc, and the system bus configuration will be displayed.

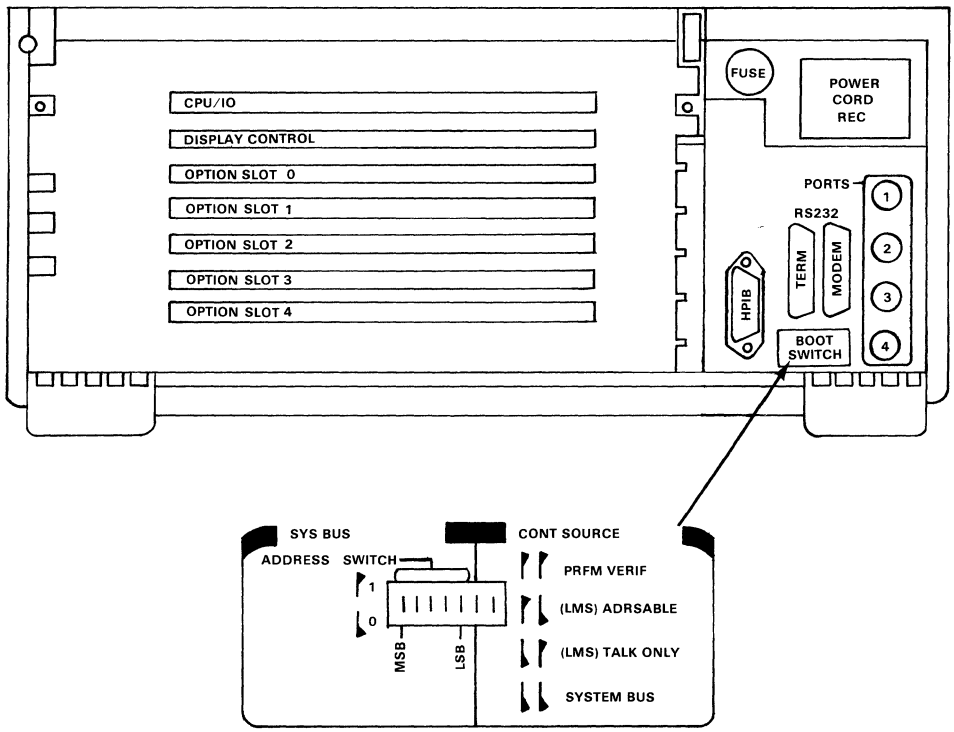


Figure 4-1. Rear Panel Switches

4-5. STARTING PERFORMANCE VERIFCATION.

4-6. To start the mainframe PV, perform the following steps.

a. Set rear panel switches to PV positions. See figure 4-1.

b. Turn power off, then on.

4-7. The mainframe will beep several times and then show the PV display test screen. See paragraphs on how to use the PV test displays. Refer to the next paragraphs for a description of the automatic power-up ROM and RAM tests.

4-8. PV POWER-UP EVENT SEQUENCE.

4-9. The mainframe automatically executes the power-up ROM and RAM tests every time the power has been turned off, then on. Table 4-1 shows the events that occur during PV power-up.

Table 4-1. PV Power-Up Sequence (1 of 2)

a. Check power-up status by reading reserved location in RAM.
b. Initialize CRT controller chip (U33).
c. Blank the screen.
d. Initiate ROM test. A failing ROM address range and byte will be displayed.
e. Initiate RAM test. If a failure occurs, an SA loop is entered and the failing RAM IC numbers are displayed.
f. Read rear panel switches and powers-up (in PV mode).
g. Suspend operation of the PHI chip (U36 on the CPU/IO board) and take it off-line.
h. Initialize the CRT chip U33 on display control board and enable the display and sounds the beeper once.
i. Disable interrupts and CPU direct memory access.
j. Clear base page RAM (F000 - FFFF hex).
k. Set up interrupt vector.

Table 4-1. PV Power-Up Sequence (2 of 2)

l. Clear keyboard power-up interrupts and clear display.

m. Set up and enable keyboard interrupts for display test and move cursor off screen.

n. Determine which flexible disc drive is present so the correct softkey will appear, then display the softkeys.

o. Start SA interval.

1. Write display test pattern to screen and enable keyboard interrupts.

2. Toggle I/O data lines and service the delta time interrupt.

3. Cycle through interrupt masks and service the delta time interrupt.

4. Read rear panel switches and write to local mass storage control board.

5. Toggle all even I/O address lines and read keyboard.

6. Send "move cursor" commands and clear SA interval.

p. Read and write from RAM.

q. Read keyboard.

r. Issue an I/O write.

s. Begin SA interval again.

4-10. The beeper is used to indicate the sucessful completion of certain phases of power-up. See table 4-2.

Table 4-2. PV Power-Up Beeper Sequence

a. BEEP.....hardware initialization.

b. BEEP.....ROM software initialization.

c. BEEP BEEP BEEP....ROM test completed.

d. BEEP BEEP.....RAM test completed.

4-11. POWER-UP ROM TEST.

4-12. Purpose.

4-13. The ROM test verifies that all of the firmware in ROM used for power-up and performance verification is good. The test also checks that the CPU is able to access ROM memory via the bi-directional address and data buses.

4-14. Area Tested.

4-15. Multiplexer, memory address/data bus, address latches, demultiplexed data bus from ROM, demultiplexed address bus to/from ROM, CPU and associated timing circuitry.

4-16. Operation.

a. This test executes a checksum on each of the ROMs as long as the kernel of ROM needed to run the test is good.

b. If an error is detected, then a bit is set in an error mask.

c. The error mask is then used to output an error message to the screen stating a ROM failure, the address range of the failure, and the byte (0 or 1).

d. If a failure is detected the test will loop continuously. See CPU section IV for more information.

e. On failures, the power-up ROM test will display the error message shown in table 4-3, assuming that the kernel of ROM required to run the power-up test is good. Use the table to determine which ROM unit number is failing.

Table 4-3. Power-Up ROM Test Errors

SELF-TEST FAILURE
ROM TEST:

FAILING ADDRESS RANGE	BYTE(S)
xxxx-xxxx	xx

Failed Addresses	Byte	Failed ROM Unit
0020-1FFF	0	U51 Lower 8K ROM
0020-1FFF	1	U48
2000-3BFF	0	U50 Upper 8K ROM
2000-3BFF	1	U49

g. When the ROM test passes, the mainframe will beep three times and begin the RAM test.

4-17. POWER-UP RAM TEST.

4-18. Purpose.

4-19. The RAM test verifies the ability to read from and write to all RAM located on the display control board and checks for refresh. Note that this test occurs only on power-up. Another RAM test occurs during PV and has a different error message.

4-20. Area Tested.

4-21. All RAMs including refresh ability, the multiplexed memory address/data bus from the CPU, motherboard connections between CPU and display controller board, demultiplexed address/data bus to and from RAM, and timing counter circuitry.

4-22. Operation.

a. This is a different test than the one performed during PV.

b. The RAM test takes approximately 7 seconds.

c. All RAM locations are toggled to insure READ/WRITE operation.

d. Refresh ability is verified.

e. The actual operation of the routine is as follows:

1. Load RAM with a count, starting with zero.

2. Read RAM and compare with count.

3. Check for an error. If error occurs, go to error sequence.

4. If there is no previous error, wait one second.

5. Read RAM and compare with count.

6. Check for an error. If error occurs, go to error sequence.

7. If there is no previous error, load RAM with complement of count, starting at zero.

8. Read RAM and compare with the complement of the count.

9. Check for an error. If error occurs go to error sequence.

10. If there is no previous error, wait one second.

11. Read RAM and compare with count.

12. Check for an error, if error occurs, go to error sequence.

f. If there are not any errors in either RAM error mask then the system will beep twice. But, if an error exists then the following error sequence occurs:

   1. Reset the delta timer to prevent auto-restart.

   2. Set the SA latch.

   3. Write to and read from all of RAM.

   4. Provide stimulus to CRT controller.

   5. Output RAM error display header information (including refresh error message if refresh error flag set).

   6. Reset SA latch.

   7. Output individual failing unit number for lower 16K RAM.

   8. Output individual failing unit number for upper 16K RAM.

g. When a failure occurs, the routine attempts to output the error message shown in table 4-4. Depending on which RAM is failing, a random pattern on the CRT, or incorrect spelling of messages can occur. Therefore, a RAM test failure is always suspect.

   If Chips U23-U30 and U38-U45 on the display controller board are failing, the display will be in error. If this occurs, see Section VIII troubleshooting.

Table 4-4. Power-Up RAM Test Errors

```
 SELF-TEST FAILURE
*RAM TEST:
 FAILING UNIT NUMBERS (S)
 -------------------------
 XY

 Where XY is the RAM U-number.
 * Displays RAM TEST:  or  RAM TEST: REFRESH FAILURE
```

4-23. USING THE PV DISPLAY-TEST.

4-24. The PV display-test should be on screen after the power-up tests. See figure 4-2. To continue to the PV-Tests Display, press the <PV TESTS> softkey.

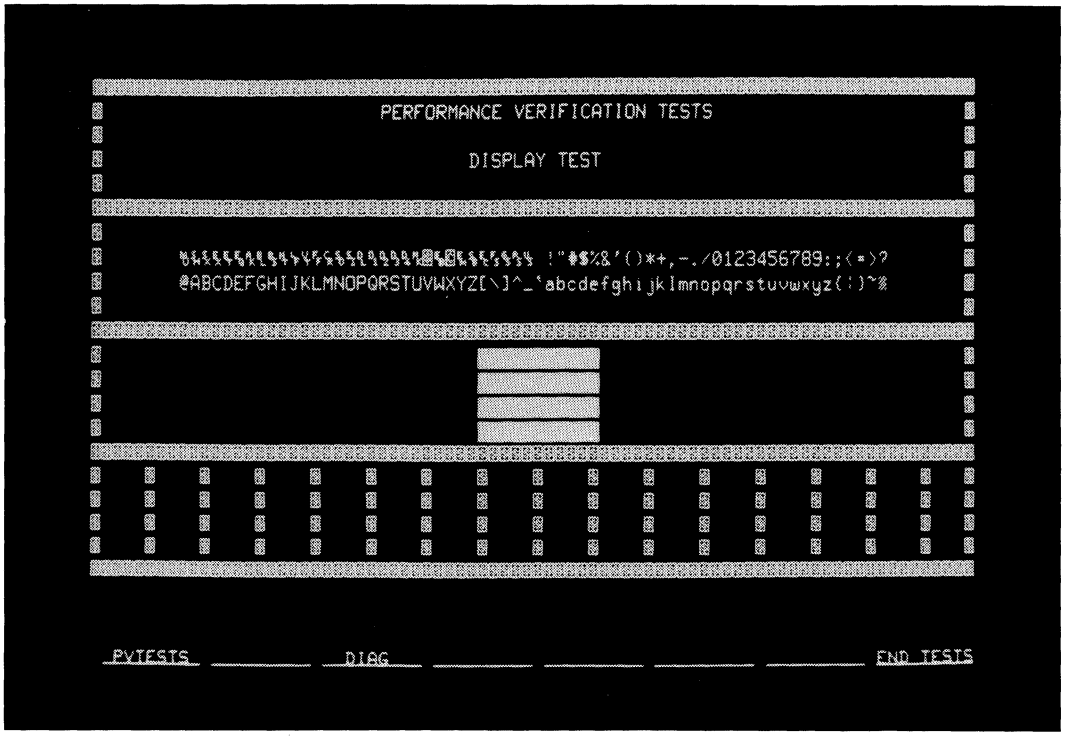


Figure 4-2. PV Display-Test

Table 4-5. PV Display-Test Softkeys

<PV TESTS>	displays the performance verification tests screen.
<DIAG>	starts the floppy disc diagnostic.
<END TEST>	terminates PV tests, clears error counts and repeats power-up sequence to PV display test.
[B]	causes the mainframe beeper to beep. This indicates that the CPU is able to recognize and process interrupts. A failure to beep indicates the CPU is "lost" or the I/O or beeper circuitry is faulty.

4-25. USING THE PV-TESTS DISPLAY.

4-26. The PV-tests display first appears showing only the first line of the screen, which is the ROM test. Press the <NEXT TEST> softkey until all tests are shown on the display. The highlighted test is the test that is ready to be run. See figure 4-3.

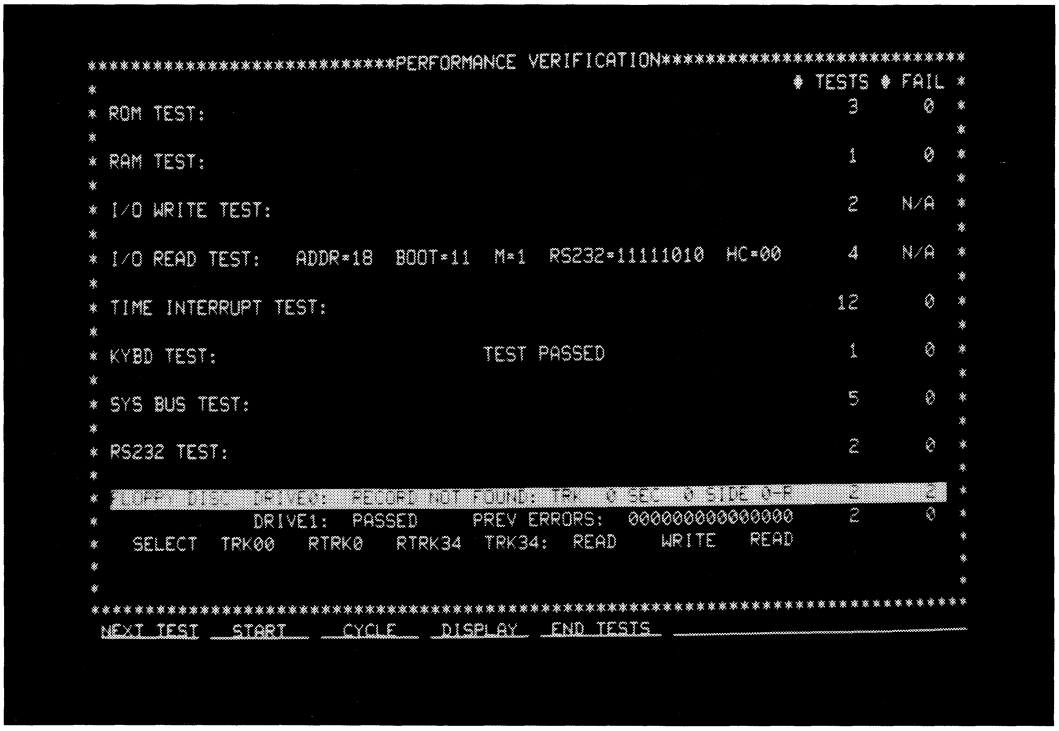


Figure 4-3. PV-Tests Display

Table 4-6. PV-Tests Display Softkeys

<NEXT TEST>.....moves highlight line to following test. When pressed during a test, the test is completed before the next one is selected.

<START>.....begins the test highlighted test. Pressing <START> during a test causes the test to complete at the end of the current repetition.

<CYCLE>.....cycles through all tests, except the keyboard test. This is a good initial inspection test.

<DISPLAY>.....presents the PV display test. When pressed during a test, returns to the PV display test after completion of the test.

<END TESTS>.....repeats power-up sequence to PV display test. If pressed during a test, the test finishes, then the power-up is performed.

NOTES: If the rear panel switches are unaltered, the repower-up will be back to the display test. The key being pressed is displayed in the lower left corner as: Key Down="X"

4-27. PV ROM TEST.

4-28. Purpose.

4-29. The ROM test verifies that all of the firmware in ROM used for boot-up and performance verification is good. The test also checks that the CPU is able to access ROM memory via the bidirectional address and data buses.

4-30. Area Tested.

4-31. Multiplexer, memory address/data bus, address latches, demultiplexed data bus from ROM, demultiplexed address bus to and from ROM, CPU and associated timing circuitry.

4-32. Operation.

a. This test is similar to the ROM test which is performed during power-up; although, there is a different error message.

b. Each test takes approximately 1/2 second.

c. A routine reads the ROM contents, computes a checksum and compares it with a checksum also located in ROM.

d. Assuming that the kernel of ROM required to run the ROM TEST is alright, the test will attempt to output an error mask if the test fails. The mask is a 16 bit word shown in table 4-7. A one in any of the bits signifies a ROM. Use the table to determine which ROM is failing.

Table 4-7. PV ROM Test Errors

IC MASK = 000000000000ABCD
15--------------0

Bit	Failed Addresses	Byte	Failed ROM Unit	
D	0020-1FFF	0	U51	Lower 8K ROM
C	0020-1FFF	1	U48	
B	2000-3BFF	0	U50	Upper 8K ROM
A	2000-3BFF	1	U49	

4-33. PV RAM TEST.

4-34. Purpose.

4-35. This PV RAM TEST is executed only from the PV menu. Note that this is a different test from the power-up RAM test and gives a different error message. The test verifies the ability to read and write from all RAM located on the display control board and checks for refresh.

4-36. Area Tested.

4-37. All RAMs including refresh ability, the multiplexed memory address/data bus from the CPU, motherboard connections between CPU and display controller board, demultiplexed address/data bus to and from RAM, and timing counter circuitry.

4-38. Operation.

a. This test takes approximately eight seconds.

b. Data from ROM is written into RAM, and then read back and compared to the ROM contents.

c. The second step writes walking 1's and 0's to each RAM address and reads it back. The walking 1's and 0's are visible on the CRT as a blinking pattern with characters moving to the bottom of the screen.

d. Table 4-8 shows the PV RAM test error mask. The XXXX is the hexadecimal form of the 16 bit error mask. There is a one-to-one correlation between the data bit set in the error mask and the failing RAM.

   Depending on which RAM is failing, a random pattern on the CRT, or incorrect spelling of messages can occur. Therefore, a RAM test failure is always suspect. If Chips U23-U30 and U38-U45 on the display controller board are failing, the display will be in error. If this occurs, see Section VIII troubleshooting.

Table 4-8. PV RAM Test Errors

RAM TEST: BIT ERROR MASK	UPPER BANK=XXXX	LOWER BANK=XXXX
Example,	UPPER BANK=0201	LOWER BANK=3000
RAMs in Error	U39, U23	U70, U69

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UPPER	U-45	44	43	42	41	40	39	38	30	29	28	27	26	25	24	23
LOWER	U-72	71	70	69	68	67	66	65	58	57	56	55	54	53	52	51

4-39. PV I/O WRITE TEST.

4-40. Purpose.

4-41. This test provides audible feedback that the test is executing by beeping, and provides the following SA stimulus. The I/O WRITE TEST cycles the PHI chip register addresses, cycles the interrupt masks, cycles the slot select lines, and stimulates the four rear panel BNC connectors.

4-42. Area Tested.

4-43. The test is not a pass/fail test. It provides stimulus for signature analysis in the following circuitry: Option slot select lines on the motherboard, all connections from option slots to the rear panel BNC connectors, the beeper circuitry, PHI register address latch, and the interrupt mask circuitry.

4-44. Operation.

a. This test will not display a failure. The main purpose of the test is for signature analysis (SA).

b. The only noticeable failure will be the loss of the audible beeper.

4-45. PV I/O READ TEST.

4-46. Purpose.

4-47. This test reads the rear panel switches, the hardware configuration jumpers, the RS-232C switch settings, and the master controller, noncontroller configuration. It is also used with signature analysis.

4-48. Area Tested.

4-49. Rear panel dip-switches, the cable to the rear panel, I/O circuitry, and the RS-232C dip-switches.

4-50. Operation.

a. Upon initiation of the I/O READ TEST, the PV menu displays the message shown in table 4-9.

Table 4-9. I/O Read Test Errors

I/O READ TEST: ADDR=xx BOOT=xx M=x RS-232=xxxxxxxx HC=xx

Where:

ADDR=xx..... is the HP-IB address (0-1F) as set by the rear panel switches.

BOOT=xx.....shows the source set by the rear panel switches.

M=x.....is the mainframe mode.

x=1 for master controller
x=0 for non-controller (slave)

RS-232=xxxxxxxx.....read from U60 on the CPU/IO board.
76543210

Bit 0 0 = Mainframe as terminal
1 = Mainframe as modem

Bit 1 Not used

Bit 2 Word Length
Bit 3

Bit 3	Bit 2	Word Length
0	0	5
0	1	6
1	0	7
1	1	8

Bit 4 Parity Enable 0= Parity Disabled
1= Parity Enabled

Bit 5 Parity Odd/Even 0= Odd Parity
1= Even Parity

Bit 6 Number of stop bits
Bit 7

Bit 7	Bit 6	# of Stop Bits
0	0	INVALID
0	1	1
1	0	1.5
1	1	2

HC=xx.....The hexadecimal representation of the six hardware jumpers. They are not used at this time.

4-51. PV TIME INTERRUPT TEST.

4-52. Purpose.

4-53. The TIME INTERRUPT TEST indicates proper operation of the 50 to 60 Hz LINSYN to the CPU via the delta time interrupt circuitry.

4-54. Area Tested.

4-55. LINSYN, a 50 to 60 Hz signal from the power supply, the delta time interrupt circuitry on the CPU/IO board, and interrupts to the CPU.

4-56. Operation.

4-57. Upon initiation, the PV test counts and displays LINSYN interrupts to the CPU.

4-58. PV KEYBOARD TEST.

4-59. Purpose.

4-60. The KEYBOARD TEST indicates proper keyboard switch closure and keyboard decoding.

4-61. Area Tested.

4-62. All 77 keyswitches, keyboard decoding electronics, keyboard cable, and the keyboard RAM/state machine.

4-63. Operation.

a. When initiated, the KEYBOARD TEST instructs the user to press all of the keyboard keys in a left-to-right top-to-bottom sequence.

b. The sequence begins with the leftmost softkey and includes all display and cursor control keys.

c. The keyboard test requires this specific sequence. Furthermore, even if all keyswitches and the decoding circuitry are working, a key that is pressed out of sequence will cause a "FAILED TEST" message and end the test.

d. The order in which the keys are pressed is given in figure 4-4.

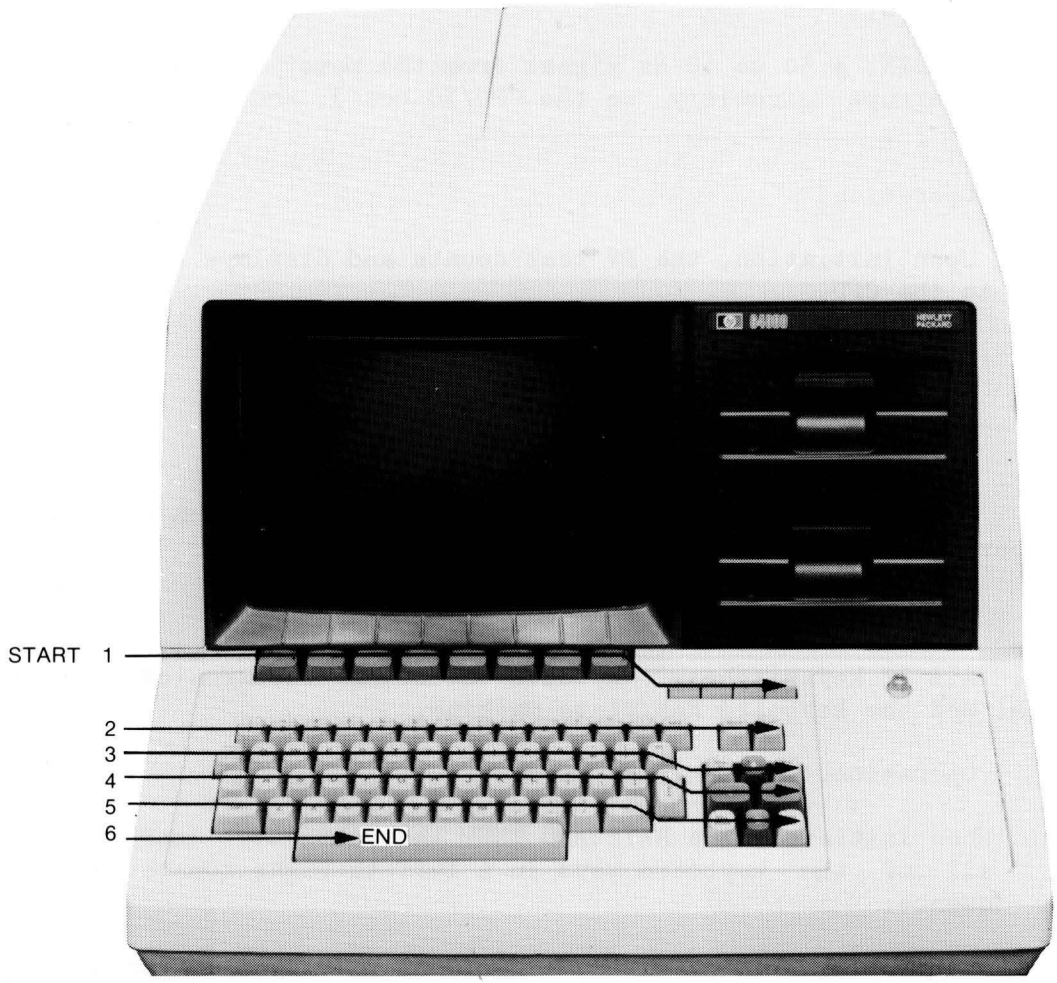


Figure 4-4. Keyboard Test, Key Sequence

e. Note the KEYBOARD TEST is skipped while PV is in the cycle mode.

4-64. PV SYSTEM BUS TEST.

```
********************  CAUTION  ***********************
*                                                     *
*  This test should  NOT  be run if the mainframe     *
*  is connected to a system bus and is the master     *
*  controller.                                        *
*                                                     *
*******************************************************
```

4-65. Purpose.

4-66. This test checks for proper operation of the PHI chip (U36 on the CPU/IO board). It also checks the data, address and counter circuitry from the CPU to the PHI chip.

4-67. Area Tested.

4-68. Data, address, control and interrupt lines from the CPU to the PHI chip.

4-69. Operation.

a. The SYSTEM BUS TEST takes the PHI chip off-line, then reads and writes to various registers on the chip.

b. The transceivers and the cable to the rear panel HP-IB connector are not presently being checked.

c. If a failure occurs, this test may take up to two minutes to fail.

4-70. RS-232 TEST PROCEDURE.

4-71. Purpose.

4-72. The test checks proper operation of the USART, U57 on the local mass storage/RS-232C board. It also checks the data and control circuitry associated with RS-232C.

4-73. Area Tested.

4-74. The 8251 USART, the baud rate generator, loop back relays, line drivers, the interface to the CPU, and the rear panel cable.

4-75. Operation.

NOTE

Before starting the test, locate slide switch U60 on the flexible disc drive/RS-232C board. Set the front switch to the left or full duplex position. Set the remaining switches on U60 to the right side to establish the maximum baud rate. The test may be run at any baud rate, but will run faster at maximum.

a. Energizes the loop back relays to loop transmit data, and handshake lines back on receive data.

b. Sends a character stream.

c. Compares receive character stream to the transmit character stream.

d. Notes:

1. The voltage translators cannot be signaturized on the higher voltage side.

2. This test may take up to two minutes if a failure is detected.

4-76. PV FLEXIBLE DISC DRIVE TEST.

4-77. See flexible disc drive appendix to this manual.

SECTION V

ADJUSTMENTS

5-1. INTRODUCTION.

5-2. This section describes adjustments and checks required to return the instrument to peak operating capability after repairs have been made.

5-3. The seven adjustments described are the +7 V, focus, intensity, horizontal position, width (horizontal gain), yoke, and height (vertical gain) adjustment.

5-4. SAFETY CONSIDERATIONS.

5-5. Although this instrument has been designed in accordance with international safety standards, general safety precautions must be observed during all phases of operation, service, and repair of the instrument. Failure to comply with precautions listed in the Safety Summary at the front of this manual or with specific warnings given throughout the manual could result in serious injury or death. Service adjustments should be performed only by qualified service personnel.

5-6. DIRECTION STANDARD.

5-7. All directions assume the operator is facing the front panel of the instrument.

5-8. +7 VOLT ADJUSTMENT.

5-9. The +7 V adjustment is found on the CPU/IO A3 board and sets the +7 V supply to the CPU, chip U29.

a. Equipment required - a voltmeter capable of .01 VDC resolution is required.

b. Remove the top cover. Refer to figure 6-1.

c. Locate the test point, labeled "+7V adj". It is located near the right edge of the board, near the lower right corner of the U29 heat sink.

d. Connect the positive lead of the voltmeter to the "+7V adj." test point and the negative lead to the ground test point in the lower right corner of the board.

e. Adjust R6 (+7V adjust) for +7.0V +/- 0.3V.

5-10. DISPLAY ADJUSTMENTS.

5-11. The display adjustments are found on the secondary board A6, the flyback board A7 and the yoke. Table 5-1 lists the adjustments and gives their locations.

```
********************** WARNING **********************
*                                                   *
*  The display adjustments are performed with the   *
*  instrument energized . Read the Safety Summary at*
*  the front of this manual before making any       *
*  adjustments.                                     *
*                                                   *
*****************************************************
```

a. Equipment required - nonconducting screwdriver or an adjustment tool.

b. Remove the top cover. Refer to figure 6-1.

c. Remove the bottom cover. Refer to figure 6-2.

d. Lay the mainframe on its right side.

Table 5-1. Display Adjustments

ADJUSTMENT	SPEC.	COMPONENT	COMMENTS
FOCUS	best focus	A7R13	Back of flyback A7 board. Access is through the high voltage cover with the top cover removed.
INTENSITY	readable	A7R12	
WIDTH	16.5 cm +- 0.2 cm	A7L2	Component side of flyback A7 board. Access is direct with bottom cover removed.
HORIZONTAL POSITION	centered	A6R3	Back of A6 secondary board Access is direct with the bottom cover removed.
HEIGHT (VERT. GAIN)	11.0 cm +- 0.2 cm	A6R20	
YOKE	level	Yoke	Located around the neck of the CRT. The high voltage cover must be removed. See warning on the cover.

e. Set the system control switches to the performance verification position.

f. Set main power switch off then on. Note, the display test pattern should be on the screen. Refer to Figure 5-1.

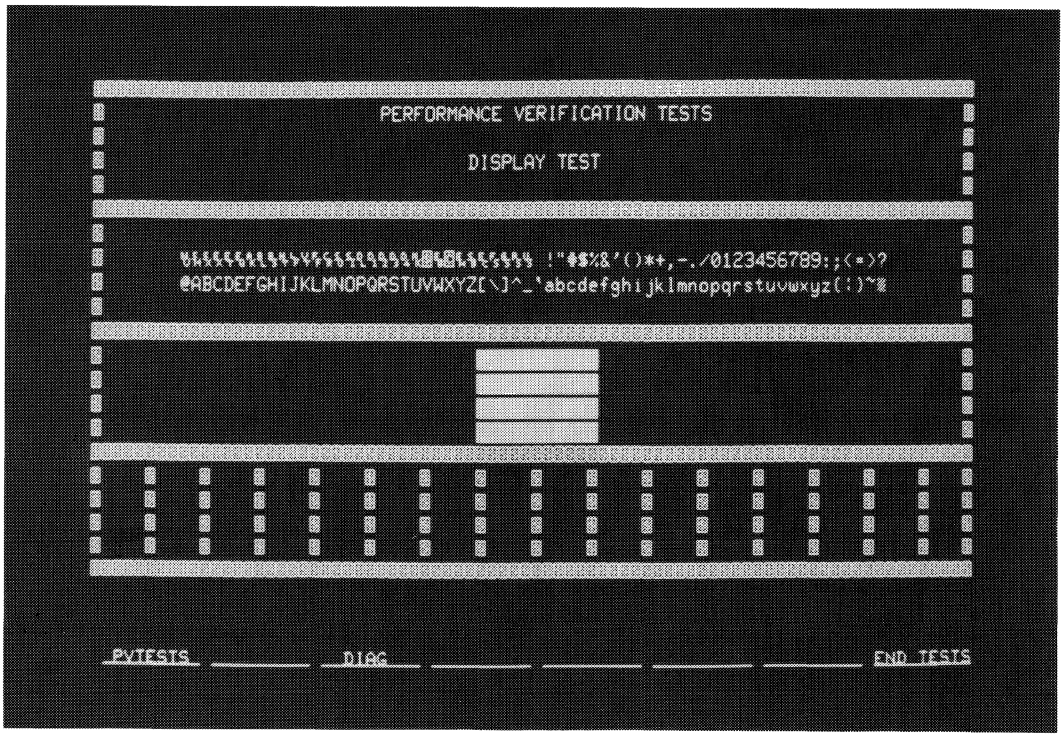


Figure 5-1. Display Test Pattern

g. Width (Horizontal Gain) Adjustment.

1. Insert adjustment tool throuh the HORIZ GAIN hole in the high voltage cover.

2. Adjust the variable inductor, L1, for a display width of 16.5cm +/- 0.2cm.

h. Horizontal Position Adjustment.

1. Adjust potentiometer R3 so that the display test pattern is centered in the bezel.

i. Height (Vertical Gain) Adjustment.

1. Adjust potentiometer R20 (V GAIN) so that the display test pattern is 11.0 cm +/- 0.2 cm high.

NOTE

There is no vertical position adjustment and pattern may be offset up to 1 cm. Magnetic fields from soldering irons, transformers, and other electromagnetic field producing electronics may cause a portion of the display to be off screen in the vertical direction. Reducing the vertical gain or removing the electromagnetic field producing device should fix this problem. Also, distortion may occur when the A6 and A7 boards are out of position.

j. Focus Adjustment.

1. Insert the adjustment tool through the FOCUS access hole in the high voltage cover.

2. Adjust potentiometer R13 (FOCUS) for the best overall focus.

k. Intensity Adjustment.

1. Insert adjustment tool through the intensity access hole in the high voltage cover.

2. Adjust potentiometer R12 (INTENSITY) to increase the intensity from its lowest level until the display is clearly readable.

```
********************  CAUTION  ********************
*                                                  *
*  If the intensity is set too bright damage may   *
*  result to the CRT.                              *
*                                                  *
****************************************************
```

1. Yoke Adjustment.

```
********************  WARNING  **************************
*                                                        *
*  This adjustment requires removal of the high          *
*  voltage cover. There are dangerous voltages (12KV)    *
*  beneath this cover, capable of causing death. Use     *
*  extreme caution when servicing. All adjustments       *
*  should be performed only by qualified service         *
*  personnel.                                            *
*                                                        *
**********************************************************
```

1. Equipment required - a non-conducting (shielded) flat head screw driver.

2. Remove the high voltage cover. Note the warning at the beginning of this procedure.

3. Loosen the yoke neck screw.

4. Rotate the yoke until the display is level.

5. Retighten the yoke neck screw.

```
*********************  CAUTION  ************************
*                                                      *
*  The yoke must be positioned forward, against the    *
*  CRT bell. Tighten the yoke securely.                *
*                                                      *
********************************************************
```

SECTION VI

REPLACEABLE PARTS

6-1. INTRODUCTION.

6-2. This section contains information for ordering parts. Table 6-1 lists abbreviations used in the parts list and throughtout the manual. Table 6-2 lists all replaceable parts in reference designator order. Table 6-3 contains the names and addresses that correspond to the manufacturer's five-digit code numbers.

6-3. ABBREVIATIONS.

6-4. Table 6-1 lists abbreviations used in the parts list, schematics and throughout the manual. In some cases, two forms of the abbreviation are used: one all in capital letters, and two partial or no capitals. This occurs because the abbreviations in the parts list are always capitals. However, in the schematics and other parts of the manual, other abbreviation forms are used with both lowercase and uppercase letters.

6-5. REPLACEABLE PARTS LIST.

6-6. Tables 6-2 through 6-14 are the lists of replaceable parts. Each list is organized as follows:

a. Chassis-mounted parts in alphanumerical order by reference designator.

b. Electrical assemblies and their components in alphanumerical order by reference designator.

c. Miscellaneous.

6-7. ORDERING INFORMATION.

6-8. To order a part listed in the replaceable parts table, quote the Hewlett-Packard part number and check digit, indicate the quantity required, and address the order to the nearest Hewlett-Packard sales and service office.

6-9. DIRECT MAIL ORDER SYSTEM.

6-10. Within the USA, Hewlett-Packard can supply parts through a direct mail order system. Advantages of using the system are as follows:

a. Direct ordering and shipment from the HP Parts Center in Mountain View, California.

b. No maximum or minimum on any mail order (there is a minimum order amount for parts ordered through a local HP sales and service office when the orders require billing and invoicing).

c. Prepaid transportation (there is a small handling charge for each order).

d. No invoices - to provide these advantages, a check or money order must accompany each order.

6-11. Mail-order forms and specific ordering information are available through your local HP Sales/Service Office. Addresses and phone numbers are located at the back of this manual.

Table 6-1. Reference Designators and Abbreviations

REFERENCE DESIGNATORS

A	= assembly	**F**	= fuse	**MP**	= mechanical part	**U**	= integrated circuit
B	= motor	**FL**	= filter	**P**	= plug	**V**	= vacuum, tube, neon bulb, photocell, etc
BT	= battery	**IC**	= integrated circuit	**Q**	= transistor		
C	= capacitor	**J**	= jack	**R**	= resistor	**VR**	= voltage regulator
CP	= coupler	**K**	= relay	**RT**	= thermistor	**W**	= cable
CR	= diode	**L**	= inductor	**S**	= switch	**X**	= socket
DL	= delay line	**LS**	= loud speaker	**T**	= transformer	**Y**	= crystal
DS	= device signaling (lamp)	**M**	= meter	**TB**	= terminal board	**Z**	= tuned cavity network
E	= misc electronic part	**MK**	= microphone	**TP**	= test point		

ABBREVIATIONS

A	= amperes	**H**	= henries	**N/O**	= normally open	**RMO**	= rack mount only
AFC	= automatic frequency control	**HDW**	= hardware	**NOM**	= nominal	**RMS**	= root-mean square
AMPL	= amplifier	**HEX**	= hexagonal	**NPO**	= negative positive zero (zero temperature coefficient)	**RWV**	= reverse working voltage
		HG	= mercury				
BFO	= beat frequency oscillator	**HR**	= hour(s)				
BE CU	= beryllium copper	**HZ**	= hertz	**NPN**	= negative-positive-negative	**S-B**	= slow-blow
BH	= binder head					**SCR**	= screw
BP	= bandpass			**NRFR**	= not recommended for field replacement	**SE**	= selenium
BRS	= brass	**IF**	= intermediate freq			**SECT**	= section(s)
BWO	= backward wave oscillator	**IMPG**	= impregnated	**NSR**	= not separately replaceable	**SEMICON**	= semiconductor
		INCD	= incandescent			**SI**	= silicon
CCW	= counter-clockwise	**INCL**	= include(s)			**SIL**	= silver
CER	= ceramic	**INS**	= insulation(ed)	**OBD**	= order by description	**SL**	= slide
CMO	= cabinet mount only	**INT**	= internal	**OH**	= oval head	**SPG**	= spring
COEF	= coeficient			**OX**	= oxide	**SPL**	= special
COM	= common	**K**	= kilo=1000			**SST**	= stainless steel
COMP	= composition					**SR**	= split ring
COMPL	= complete	**LH**	= left hand	**P**	= peak	**STL**	= steel
CONN	= connector	**LIN**	= linear taper	**PC**	= printed circuit		
CP	= cadmium plate	**LK WASH**	= lock washer	**PF**	= picofarads= 10^{-12} farads	**TA**	= tantalum
CRT	= cathode-ray tube	**LOG**	= logarithmic taper			**TD**	= time delay
CW	= clockwise	**LPF**	= low pass filter	**PH BRZ**	= phosphor bronze	**TGL**	= toggle
				PHL	= phillips	**THD**	= thread
DEPC	= deposited carbon	**M**	= milli=10^{-3}	**PIV**	= peak inverse voltage	**TI**	= titanium
DR	= drive	**MEG**	= meg=10^{6}	**PNP**	= positive-negative-positive	**TOL**	= tolerance
		MET FLM	= metal film			**TRIM**	= trimmer
ELECT	= electrolytic	**MET OX**	= metallic oxide	**P/O**	= part of	**TWT**	= traveling wave tube
ENCAP	= encapsulated	**MFR**	= manufacturer	**POLY**	= polystyrene		
EXT	= external	**MHZ**	= mega hertz	**PORC**	= porcelain	**U**	= micro=10^{-6}
		MINAT	= miniature	**POS**	= position(s)		
F	= farads	**MOM**	= momentary	**POT**	= potentiometer	**VAR**	= variable
FH	= flat head	**MOS**	= metal oxide substrate	**PP**	= peak-to-peak	**VDCW**	= dc working volts
FIL H	= fillister head	**MTG**	= mounting	**PT**	= point		
FXD	= fixed	**MY**	= "mylar"	**PWV**	= peak working voltage	**W/**	= with
						W	= watts
G	= giga (10^{9})	**N**	= nano (10^{-9})	**RECT**	= rectifier	**WIV**	= working inverse voltage
GE	= germanium	**N/C**	= normally closed	**RF**	= radio frequency		
GL	= glass	**NE**	= neon	**RH**	= round head or right hand	**WW**	= wirewound
GRD	= ground(ed)	**NI PL**	= nickel plate			**W/O**	= without

6-12. POWER SUPPLY REMOVAL.
ASSEMBLY A1.

```
************************  WARNING  ************************
*                                                         *
*  Ensure the instrument is deenergized prior to power    *
*  supply removal.                                        *
*                                                         *
***********************************************************
```

a. Remove the power cord W2.

b. Remove the top cover MP1, rear door MP5, bottom cover MP4, and left side cover MP3. Refer to Figures 6-1 and 6-2.

c. Remove eight H37 screws. Refer to figure 6-6.

d. Disconnect the line switch extender MP11 from line switch.

e. Tilt power supply up at the front then slide it forward and up until it clears the mainframe.

f. Install in reverse order.

6-13. PRIMARY BOARD REMOVAL.
ASSEMBLY A1A1.

a. Remove the power supply assembly A1 from the mainframe.

b. Remove the six H22 corner strut screws. The two corner struts MP20, MP21, and the power board brace MP19, can be removed as one piece. See figure 6-9.

c. Unscrew shaft MP18 from coupler MP22.

d. Slide the shaft out.

e. Disconnect the cables from connectors A1A1J1-J5.

f. Remove the AC line filter A1A5 by removing the four H13 screws.

g. Slide the primary board A1A1, out of the power supply assembly, A1.

```
********************  CAUTION  ********************
*                                                  *
*  The control return (Cont Ret) and control in    *
*  (Cont In) test points can be bent during re-    *
*  moval.                                          *
*                                                  *
****************************************************
```

h. Assemble in reverse order.

6-14. +5/+12 VOLT SUPPLY BOARD REMOVAL. ASSEMBLY A1A2.

a. Remove the power supply assembly A1.

b. Remove the six H22 corner strut screws. The two corner struts MP20, MP21 and the power board brace MP19, can be removed in one piece. Refer to figure 6-9.

c. Lay the power supply on its side with the fans facing down.

d. Remove the two H19 +5, -12 volt board screws. There are two access holes in the -3.25, -5.2 volt board that allow access to the +5, -12 volt board.

e. Disconnect the cables at A1A1J4 and A1A3J1.

f. Lift the +5, +12 volt board up and out of the power supply assembly.

g. Assemble in reverse order. Ensure the board slides into the board guide and sets properly in A1A4J3.

```
********************  CAUTION  ********************
*                                                  *
*  The cable that connects from the top of trans-  *
*  former A1A2T1 to the A1A1 board above has heat  *
*  shrink tubing protecting it. The cable from the *
*  bottom of the transformer connects to the A1A3  *
*  board below.                                    *
*                                                  *
****************************************************
```

6-15. -3.25, -5.2 VOLT SUPPLY BOARD REMOVAL. ASSEMBLY A1A3.

a. Remove the power supply assembly A1.

b. Remove the six H22 corner strut screws. The two corner struts MP20, MP21, and the power board brace can be removed in one piece. Refer to figure 6-9.

c. Lay the power supply on its side with the fans facing down.

d. Remove the two H19 screws holding the -3.25, -5.2 volt board.

e. Disconnect the cable to A1A3J1.

f. Lift the -3.25, -5.2 volt board up and out of the power supply assembly.

g. Assemble in reverse order.

6-16. POWER SUPPLY INTERCONNECT BOARD REMOVAL. ASSEMBLY A1A4.

a. Remove the power supply assembly A1.

b. Remove the two H22 from the bottom and top corner struts. See figure 6-9.

c. Remove the shaft extention MP18 from switch A1A1S1.

d. Remove the two H22 from the front power supply bracket MP17.

e. Lay the power supply on its side with the fans facing up.

f. Lift the front power supply bracket MP17 up, until A1A4J2 and J3 separate from both the +5,+ 12 volt board and the -3.25, -5.2 volt board.

```
******************  CAUTION  ******************
*                                              *
*  Do not pull too hard since A1A1W1 is still  *
*  connected to A1A4J1 and damage may result.  *
*                                              *
************************************************
```

g. Disconnect A1W1 from A1A4J2.

h. Remove one H13 and three H65 screws holding the board.

i. Separate the power supply interconnect board A1A4 from the power supply front bracket MP17.

j. Assemble in reverse order.

6-17. CRT DISPLAY REMOVAL.

********** WARNING **********
*
* Hazardous voltages exist on the display driver boards and on the CRT. To avoid electrical shock, use the following procedure. Wear safety glasses when handling the CRT.
*
* The CRT may charge by itself while disconnected.
*
****

a. Turn off the power and remove the power cord W1.

b. Lay the instrument on its left side.

c. Remove the two H26 screws from the bottom of the CRT. See figure 6-4.

d. Swing the key board out so it forms a straight line with the bottom of the mainframe.

e. Gently pry out the CRT bezel MP32.

NOTE

The CRT filter MP33 does not need to be removed from the CRT bezel. If the filter is removed, replace it with the non-reflecting side facing out.

f. Remove the top cover MP1. Refer to figure 6-1.

g. Remove the high voltage cover MP66, by removing seven H19 and two H24 screws.

h. Swing the display driver A6 secondary board and the A7 flyback board out of the way.

i. Disconnect the CRT socket W2.

j. Remove three H8 screws that retain the CRT, leaving the one screw which holds the ground strap in place.

k. Discharge the CRT.

1. Connect a jumper wire between the ground strap of the CRT and the metal shaft of an insulated screwdriver.

2. Slip the screwdriver tip under the protective rubber cap of the post accelerator lead and momentarily press the tip against the lead to discharge the CRT.

```
********************  CAUTION  ************************
*                                                      *
*  Discharge the CRT to the ground test point shown    *
*  on the A7 flyback board in figure 4-1. Component    *
*  damage may occur if the CRT is discharged to other  *
*  areas.                                              *
*                                                      *
********************************************************
```

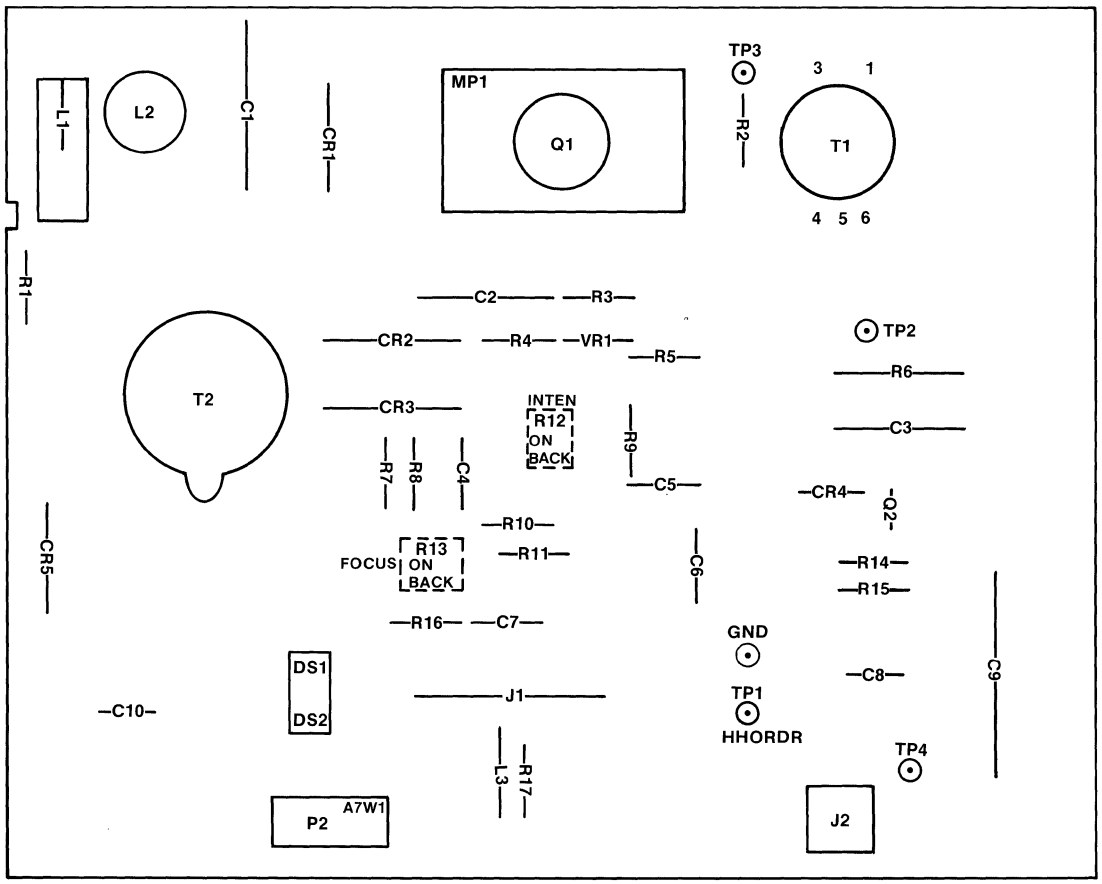


Figure 6-1. CRT Display Discharge Point

l. Remove the high voltage lead from the CRT.

m. Remove the remaining H8 screw.

n. Disconnect the yoke cable from A7J2.

o. Remove the CRT through the front of the instrument.

p. Assemble in reverse order; except, start the H8 screw in step m before inserting the CRT. The CRT may charge by itself while disconnected; be sure to discharge it before handling.

NOTE

Be sure that the ground strap makes good connection to the CRT mounting ear and that all H8 mounting screws are tightened securely.

Table 6-2. Mainframe Replaceable Parts List

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	64110A	5		MAINFRAME-64110A	28480	64110A
A1	64110-62601	0	1	ASSEMBLY-POWER SUPPLY	28480	64110-62601
A2	64110-66501	7	1	ASSEMBLY-MOTHERBOARD #1	28480	64110-66501
A3	64110-66507	3	1	BOARD ASSEMBLY-CPU/I.O.	28480	64110-66507
A4	64110-66502	8	1	ASSEMBLY-KEYBOARD	28480	64110-66502
A5	64110-66519	7		BOARD-DISPLAY CONTROL	28480	64110-66519
A6	64110-66506	2	1	BOARD ASSEMBLY-SECTION DRIVE	28480	64110-66506
A7	64110-66505	1	1	TRANSFORMER-FLYBACK	28480	64110-66505
A8	64110-66508	4	1	BOARD ASSEMBLY-REAR	28480	64110-66508
A11	64110-66509	5	1	BOARD ASSEMBLY-MINI/RS232	28480	64110-66509
A12	64110-61001	2	1	ASSEMBLY-FOOT	28480	64110-61001
A13	64110-65102	2	1	ASSEMBLY-HINGE (LEFT)	28480	64110-65102
AL1	9100-4218	3	1	DEFLECTION YOKE	28480	9100-4218
H1	0380-0016	4	1	SPACER-RND .188-IN-LG .194-IN-ID	00000	ORDER BY DESCRIPTION
H2	0380-1334	1	4	SPACER-RND .75-IN-LG .156-IN-ID	00000	ORDER BY DESCRIPTION
H3	0380-1337	4	4	SPACER-RND .185-IN-LG .25-IN-ID .5-IN-OD	00000	ORDER BY DESCRIPTION
H4	0380-1461	5	1	SPACER	28480	0380-1461
H5	0400-0009	9	1	GROMMET-RND .125-IN-ID .25-IN-GRV-OD	28480	0400-0009
H6	0510-0952	4	2	RETAINER-RING E-R EXT .094-IN-DIA STL	28480	0510-0952
H7	0510-1180	2	1	HOOK-LOOP FASTENER	28480	0510-1180
H8	0624-0441	7	4	SCREW-TPG 8-16 .625-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H9	0905-0923	6	6	O-RING .176-IN-ID .07-IN-XSECT-DIA EPR	83259	2-008 E540-80
H10	1400-0611	0	3	CLAMP-FL-CA 1-WD	06915	CFCC-8
H11	1480-0582	2	1	PIN-GRV .125-IN-DIA 1-IN-LG CARB-STL	28480	1480-0582
H13	2200-0103	2	14	SCREW-MACH 4-40 .25-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H14	2200-0107	6	4	SCREW-MACH 4-40 .375-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H15	2200-0111	2	8	SCREW-MACH 4-40 .5-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H16	2200-0139	4	2	SCREW-MACH 4-40 .25-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H17	2200-0142	9	1	SCREW-MACH 4-40 .312-IN-LG 100 DEG	00000	ORDER BY DESCRIPTION
H18	2200-0164	5	10	SCREW-MACH 4-40 .188-IN-LG UNCT 82 DEG	00000	ORDER BY DESCRIPTION
H19	2200-0165	6	7	SCREW-MACH 4-40 .25-IN-LG 82 DEG	00000	ORDER BY DESCRIPTION
H20	2200-0173	6	1	SCREW-MACH 4-40 1-IN-LG 82 DEG	00000	ORDER BY DESCRIPTION
H21	2360-0113	2	5	SCREW-MACH 6-32 .25-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H22	2360-0115	4	3	SCREW-MACH 6-32 .312-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H23	2360-0117	6	4	SCREW-MACH 6-32 .375-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H24	2360-0121	2	7	SCREW-MACH 6-32 .5-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H25	2360-0129	0	1	SCREW-MACH 6-32 1-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H26	2360-0182	5	5	SCREW-MACH 6-32 .312-IN-LG 82 DEG	00000	ORDER BY DESCRIPTION
H27	2360-0183	6	1	SCREW-MACH 6-32 .375-IN-LG 82 DEG	00000	ORDER BY DESCRIPTION
H28	2360-0194	9	6	SCREW-MACH 6-32 .312-IN-LG 100 DEG	00000	ORDER BY DESCRIPTION
H29	2360-0200	8	5	SCREW-MACH 6-32 .5-IN-LG 100 DEG	00000	ORDER BY DESCRIPTION
H30	2360-0207	5	1	SCREW-MACH 6-32 .875-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H31	2360-0423	7	1	SCREW-MACH 6-32 .562-IN-LG PAN-HD-POZI	28480	2360-0423
H32	2360-0436	2	5	SCREW-MACH 6-32 .688-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H33	2420-0003	7	10	NUT-HEX-DBL-CHAM 6-32-THD .094-IN-THK	00000	ORDER BY DESCRIPTION
H34	2510-0045	8	2	SCREW-MACH 8-32 .375-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H35	2510-0099	2	4	SCREW-MACH 8-32 .25-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H36	2510-0106	2	2	SCREW-MACH 8-32 .5-IN-LG 100 DEG	00000	ORDER BY DESCRIPTION
H37	2510-0192	6	8	SCREW-MACH 8-32 .25-IN-LG 100 DEG	00000	ORDER BY DESCRIPTION
H38	2680-0172	1	2	SCREW-MACH 10-32 .375-IN-LG 100 DEG	28480	2680-0172
H39	3050-0006	6	4	WASHER-SHLDR NO. 10 .2-IN-ID .5-IN-OD	28480	3050-0006
H40	64110-08801	8	1	WASHER-KEYBOARD	28480	64110-08801
H41	64110-08802	9	1	WASHER-KEYBOARD	28480	64110-08802
H42	64110-08803	0	1	WASHER-KEYBOARD	28480	64110-08803
H43	2190-0007	2	1	WASHER-LK INTL T NO. 6 .141-IN-ID	28480	2190-0007
H44	2360-0203	1	4	SCREW-MACH 6-32 .625-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H45	0624-0476	8	10	SCREW-TPG 6-19 .682-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H90	64110-04108	0	1	COVER-HATCH	28480	64110-04108
MP1	64110-04102	4	1	COVER-TOP	28480	64110-04102
MP2	5061-1992	6	1	SIDE COVER/HANDLE	28480	5061-1992
MP3	64110-04106	8	1	PANEL-SIDE COVER	28480	64110-04106
MP4	64110-04109	1	1	COVER-BOTTOM	28480	64110-04109
MP5	4040-1810	2	1	REAR-DOOR	28480	4040-1810
MP6	1400-0540	4	1	RETAINER RING-LED CLIP 0.270-IN SERRATED	28480	1400-0540
MP7	5040-7235	8	1	STRAP-HANDLE	28480	5040-7235
MP8	5040-7219	8	1	CAP-STRAP HANDLE	28480	5040-7219
MP9	5040-7220	1	1	CAP-STRAP HANDLE	28480	5040-7220
MP10	7121-1340	8	1	LABEL-INFO	28480	7121-1340
MP11	4040-1813	5	1	EXTENDER-SWITCH	28480	4040-1813
MP23	64110-00602	1	1	SHIELD-REAR	28480	64110-00602
MP24	64110-04107	9	2	COVER-GROUND	28480	64110-04107
MP25	64110-04107	9		COVER-GROUND	28480	64110-04107
MP26	1450-0599	8	1	LENS CAP AMB-TP .28-DIA PNL SNAP-IN	07416	CLF 280 ATP

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Mainframe Replaceable Parts List (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
MP27	64110-01204	1	2	BRACKET-CABLE CLAMP	28480	64110-01204
MP28	64110-01204	1		BRACKET-CABLE CLAMP	28480	64110-01204
MP29	5041-2018	7	1	KEYCAP-LINE	28480	5041-2018
MP30	64110-01205	2	1	BRACKET-STRAIN RELIEF	28480	64110-01205
MP31	64110-01218	7	1	BRACKET-LED	28480	64110-01218
MP32	4040-1816	8	1	BEZEL-CRT	28480	4040-1816
MP33	4330-1057	4	1	CRT FILTER	28480	4330-1057
MP34	4040-1814	6	2	SIDE FOOT-FRONT	28480	4040-1814
MP35	4040-1814	6		SIDE FOOT-FRONT	28480	4040-1814
MP36	5020-8837	6	2	STRUT-CORNER	28480	5020-8837
MP37	5020-8837	6		STRUT-CORNER	28480	5020-8837
MP38	64110-05501	9	1	BOX-SHIELD	28480	64110-05501
MP39	64110-00101	5	1	DECK	28480	64110-00101
MP40	4040-1817	9	2	CARD GUIDE	28480	4040-1817
MP41	4040-1817	9		CARD GUIDE	28480	4040-1817
MP42	4040-1808	8	1	BEZEL-FRONT	28480	4040-1808
MP43	5020-8805	8	1	FRAME-FRONT	28480	5020-8805
MP44	4040-1809	9	1	BEZEL-REAR	28480	4040-1809
MP45	64110-00501	9	1	STRUT-TOP	28480	64110-00501
MP46	64110-00503	1	1	STRUT-BOTTOM	28480	64110-00503
MP47	64110-02001	8	1	CASTING-REAR	28480	64110-02001
MP48	64110-01206	3	2	SPACER-BOARD GUIDE	28480	64110-01206
MP49	64110-01206	3		SPACER-BOARD GUIDE	28480	64110-01206
MP50	7121-1237	2	1	LABEL-UPPER REAR	28480	7121-1237
MP51	7121-1236	1	1	LABEL-CARD CAGE	28480	7121-1236
MP52	7121-1235	0	1	LABEL-LOW REAR	28480	7121-1235
MP53	7121-1611	6	1	LABEL-INFO	28480	7121-1611
MP54	64110-02301	1	1	TROUGH-CABLEKEEP	28480	64110-02301
MP55	64110-01212	1	1	CLAMP-CABLE REAR BOARD	28480	64110-01212
MP56	64110-25103	9	1	HINGE (RIGHT) MACH	28480	64110-25103
MP57	64110-01215	4	1	KEYBOARD-CABINET STRAP	28480	64110-01215
MP58	64110-23701	9	1	ROD-PIVOT (LEFT)	28480	64110-23701
MP59	64110-23702	0	1	ROD-PIVOT (RIGHT)	28480	64110-23702
MP60	4040-1807	7	1	KEYBOARD BASE	28480	4040-1807
MP61	4040-1806	6	1	KEYBOARD INSERT	28480	4040-1806
MP62	7121-1339	5	1	LABEL-INFO	28480	7121-1339
MP63	64110-04105	7	1	PLATE-CABLE KEYBOARD	28480	64110-04105
MP64	5040-7202	9	1	TRIM STRIP-TOP	28480	5040-7202
MP66	64110-04110	4	1	COVER-HIGH VOLTAGE	28480	64110-04110
MP67	64110-01202	9	1	BRACKET-DISPLAY DRIVE	28480	64110-01202
V1	2090-0049	0	1	TUBE-ELECTRON CRT	28480	2090-0049
W1	8120-1378	1	1	CABLE ASSY 18AWG 3-CNDCT JCK-JKT	28480	8120-1378
W2	64110-61601	8	1	CABLE-CRT BASE	28480	64110-61601
W3	64110-61602	9	1	CABLE (REAR)	28480	64110-61602
W4	64110-61604	1	1	CABLE-KEYBOARD	28480	64110-61604
W11	64110-61614	3	1	CABLE-POWER LIGHT	28480	64110-61614

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. A1 Power Supply Replaceable Parts List

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1	64110-62601	0	1	POWER SUPPLY ASSEMBLY	28480	64110-62601
A1A1	64110-66511	9	1	PRIMARY BOARD ASSEMBLY	28480	64110-66511
A1A2	64110-66513	1	1	BOARD ASSEMBLY, +5/-12	28480	64110-66513
A1A3	64110-66514	2	1	BOARD ASSEMBLY, P.S. -3/-5	28480	64110-66514
A1A4	64110-66512	0	1	BOARD ASSEMBLY-P.S. INTERCONNECT	28480	64110-66512
A1A5	64110-62701	1	1	LINE FILTER ASSEMBLY	28480	64110-62701
A1B1	3160-0339	1	2	FAN-TBAX 95-CFM 95/128V 50/60-HZ	28480	3160-0339
A1B2	3160-0339	1		FAN-TBAX 95-CFM 95/128V 50/60-HZ	28480	3160-0339
A1F1	2110-0342	0	1	FUSE 8A 250V NTD 1.25X.25 UL	75915	314008
A1H13	2200-0103	2	13	SCREW-MACH 4-40 .25-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A1H19	2200-0165	6	4	SCREW-MACH 4-40 .25-IN-LG 82 DEG	00000	ORDER BY DESCRIPTION
A1H22	2360-0115	4	8	SCREW-MACH 6-32 .312-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A1H23	2360-0117	6	6	SCREW-MACH 6-32 .375-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A1H32	2360-0436	2	8	SCREW-MACH 6-32 .688-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A1H37	2510-0192	6	4	SCREW-MACH 8-32 .25-IN-LG 100 DEG	00000	ORDER BY DESCRIPTION
A1H64	2110-0569	3	1	FUSEHOLDER COMPONENT NUT; THREAD M12.7	28480	2110-0569
A1H65	2200-0109	8	3	SCREW-MACH 4-40 .438-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A1H66	2200-0167	8	2	SCREW-MACH 4-40 .375-IN-LG 82 DEG	00000	ORDER BY DESCRIPTION
A1H67	2360-0210	0	8	SCREW-MACH 6-32 .625-IN-LG 82 DEG	00000	ORDER BY DESCRIPTION
A1H68	2360-0182	5	4	SCREW-MACH 6-32 .312-IN-LG 82 DEG	00000	ORDER BY DESCRIPTION
A1H69	3160-0329	9	8	FASTENING CLIP .390 IN WD BY .375 IN H	28480	3160-0329
A1MP12	2110-0565	9	1	FUSEHOLDER CAP 12A MAX FOR UL	28480	2110-0565
A1MP13	2110-0566	0	1	FUSEHOLDER-EXTR POST 12A 250 V	28480	2110-0566
A1MP14	64110-01207	4	1	BRACKET-FUSE	28480	64110-01207
A1MP15	64110-04101	3	1	CUR-LOW VOLTAGE	28480	64110-04101
A1MP16	64110-01201	8	8	BRACKET-FAN	28480	64110-01201
A1MP17	64110-01217	6	1	BRACKET-FRONT	28480	64110-01217
A1MP18	64110-23703	1	1	SHAFT-EXTENSION	28480	64110-23703
A1MP19	64110-01216	5	1	BRACE-POWER BOARD	28480	64110-01216
A1MP20	5020-8837	6	2	STRUT-CORNER	28480	5020-8837
A1MP21	5020-8837	6		STRUT-CORNER	28480	5020-8837
A1MP22	01830-23201	3	3	SHAFT-COUPLER	28480	01830-23201
A1P1	1251-3168	1	1	CONNECTOR 5-PIN F POST TYPE	28480	1251-3168
A1W1	64110-61603	0	2	CABLE-FAN	28480	64110-61603
A1W2	64110-61603	0		CABLE-FAN	28480	64110-61603
A1W3	64110-61611	0	1	CABLE-POWER SUPPLY	28480	64110-61611

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-4. A1A1 Primary Board Replaceable Parts List

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1A1	64110-66511	9	1	BOARD ASSEMBLY-PRIMARY	28480	64110-66511
A1A1AS1	64110-01213	2	1	BRACKET-SWITCH ASSEMBLY	28480	64110-01213
A1A1C1	0160-4834	6	1	CAPACITOR-FXD .047UF +-10% 100VDC CER	28480	0160-4834
A1A1C2	0160-4554	7	5	CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A1A1C3	0160-5246	6	5	CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-5246
A1A1C4	0180-0197	8	3	CAPACITOR-FXD 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
A1A1C5	0180-0197	8		CAPACITOR-FXD 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
A1A1C6	0160-5246	6		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-5246
A1A1C7	0160-5246	6		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-5246
A1A1C8	0160-4822	2	1	CAPACITOR-FXD 1000PF +-5% 100VDC CER	28480	0160-4822
A1A1C9	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A1A1C10	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A1A1C11	0180-0376	5	1	CAPACITOR-FXD .47UF+-10% 35VDC TA	56289	150D474X9035A2
A1A1C12	0160-5267	1	2	CAPACITOR-FXD 4700PF +-5% 50VDC CER	28480	0160-5267
A1A1C13	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A1A1C14	0160-5246	6		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-5246
A1A1C15	0180-0197	8		CAPACITOR-FXD 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
A1A1C16	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A1A1C17	0160-4811	9	2	CAPACITOR-FXD 270PF +-5% 100VDC CER	28480	0160-4811
A1A1C18	0160-4625	3	2	CAPACITOR-FXD 1500PF +-5% 100VDC CER	28480	0160-4625
A1A1C19	0160-4625	3		CAPACITOR-FXD 1500PF +-5% 100VDC CER	28480	0160-4625
A1A1C20	0160-5246	6		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-5246
A1A1C21	0180-0373	2	2	CAPACITOR-FXD .68UF+-10% 35VDC TA	56289	150D684X9035A2
A1A1C22	0180-0373	2		CAPACITOR-FXD .68UF+-10% 35VDC TA	56289	150D684X9035A2
A1A1C23	0180-3040	6	2	CAPACITOR-FXD 850UF+50-10% 200VDC AL	28480	0180-3040
A1A1C24	0180-3040	6		CAPACITOR-FXD 850UF+50-10% 200VDC AL	28480	0180-3040
A1A1C25	0160-4048	4	1	CAPACITOR-FXD .022UF +-20% 250VAC(RMS)	C0633	PME 271 M 522
A1A1C26	0160-5347	8	4	CAPACITOR-FXD 1.0UF 400VDC	28480	0160-5347
A1A1C27	0160-4962	1	1	CAPACITOR-FXD 1.0UF 250VDC	28480	0160-4962
A1A1C28	0160-5347	8		CAPACITOR-FXD 1.0UF 400VDC	28480	0160-5347
A1A1C29	0160-5347	8		CAPACITOR-FXD 1.0UF 400VDC	28480	0160-5347
A1A1C30	0160-5347	8		CAPACITOR-FXD 1.0UF 400VDC	28480	0160-5347
A1A1C31	0160-2220	0	1	CAPACITOR-FXD 1200PF +-5% 300VDC MICA	28480	0160-2220
A1A1C32	0160-5267	1		CAPACITOR-FXD 4700PF +-5% 50VDC CER	28480	0160-5267
A1A1C33	0160-4811	9		CAPACITOR-FXD 270PF +-5% 100VDC CER	28480	0160-4811
A1A1C34	0160-4557	0	2	CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A1A1C35	0180-0374	3	1	CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
A1A1C36	0180-2946	9	1	CAPACITOR-FXD 330UF+50-10% 35VDC AL	28480	0180-2946
A1A1C37	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A1A1CR1	1901-0050	3	3	DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A1A1CR2	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A1A1CR3	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A1A1CR4	1906-0224	3	1	DIODE-FW BRDG 600V 25A	04713	MDA2506
A1A1CR5	1901-0029	6	2	DIODE-PWR RECT 600V 750MA DO-29	28480	1901-0029
A1A1CR6	1901-0029	6		DIODE-PWR RECT 600V 750MA DO-29	28480	1901-0029
A1A1CR7	1906-0051	4	1	DIODE-FW BRDG 100V 1A	28480	1906-0051
A1A1CR8	1906-0006	9	1	DIODE-FW BRDG 400V 1A	1B546	VE48
A1A1DS1	1990-0685	7	1	LED-LAMP LUM-INT=200UCD	28480	HLMP-6620
A1A1H11	1400-0249	0	2	CABLE TIE .062-.625-DIA .091-WD NYL	06383	PLT1M-8
A1A1H14	2200-0107	6	2	SCREW-MACH 4-40 .375-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A1A1H16	2200-0139	4	3	SCREW-MACH 4-40 .25-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A1A1H50	2190-0005	0	3	WASHER-LK EXT T NO. 4 .116-IN-ID	28480	2190-0005
A1A1H51	2190-0011	8	4	WASHER-LK INTL T NO. 10 .195-IN-ID	28480	2190-0011
A1A1H52	2260-0001	5	3	NUT-HEX-DBL-CHAM 4-40-THD .094-IN-THK	28480	2260-0001
A1A1H54	2360-0197	2	2	SCREW-MACH 6-32 .375-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A1A1H55	2360-0135	8	1	SCREW-MACH 6-32 1.5-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A1A1H56	2420-0001	5	1	NUT-HEX-W/LKWR 6-32-THD .109-IN-THK	00000	ORDER BY DESCRIPTION
A1A1H57	2680-0128	7	4	SCREW-MACH 10-32 .25-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A1A1H58	3050-0239	7	5	WASHER-FL NM NO. 8 .17-IN-ID .375-IN-OD	28480	3050-0239
A1A1H59	8151-0013	4	1	WIRE 22AWG 1X22	28480	8151-0013
A1A1H93	0890-0100	8	1	POL SHK WHT .33 FT.	28480	0890-0100
A1A1J1	1251-4291	3	1	CONNECTOR 5-PIN M POST TYPE	28480	1251-4291
A1A1J2	1251-0599	6	2	CONNECTOR 3-PIN M POST TYPE	28480	1251-0599
A1A1J3	1251-0599	6		CONNECTOR 3-PIN M POST TYPE	28480	1251-0599
A1A1J4	1251-4685	9	1	CONNECTOR 4-PIN M POST TYPE	28480	1251-4685
A1A1L1	9140-0254	3	1	INDUCTOR 430UH 10% .6DX1.6LG	28480	9140-0254
A1A1MP3	1400-0082	9	1	CLAMP-CABLE .125-DIA .375-WD NYL	28480	1400-0082
A1A1MP4	1970-0083	7	1	TUBE-ELECTRON	28480	1970-0083
A1A1MP5	1205-0445		1	HEATSINK	28480	1205-0445
A1A1MP6	1205-0373		1	HEATSINK TO-220	13103	6030B-TT

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-4. A1A1 Primary Board Replaceable Parts List (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1A1Q1	1854-0215	1	1	TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A1A1Q2	1853-0036	2	1	TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
A1A1Q3	1854-0827	1	2	TRANSISTOR NPN SI TO-220AB PD=100W	04713	MJE-13009
A1A1Q4	1854-0827	1		TRANSISTOR NPN SI TO-220AB PD=100W	04713	MJE-13009
A1A1R1	0757-0438	3	7	RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A1A1R2	0757-0280	3	4	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1A1R3	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1A1R4	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1A1R5	0757-0279	0	1	RESISTOR 3.16K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3161-F
A1A1R6	0757-0462	3	1	RESISTOR 75K 1% .125W F TC=0+-100	24546	C4-1/8-T0-7502-F
A1A1R7	0757-0442	9	1	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A1A1R8	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A1A1R9	0757-0346	2	1	RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
A1A1R10	0698-3430	5	1	RESISTOR 21.5 1% .125W F TC=0+-100	03888	PME55-1/8-T0-21R5-F
A1A1R11	0698-3161	9	1	RESISTOR 38.3K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3832-F
A1A1R12	0757-0439	4	2	RESISTOR 6.81K 1% .125W F TC=0+-100	24546	C4-1/8-T0-6811-F
A1A1R13	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A1A1R14	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A1A1R15	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A1A1R16	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1A1R17	0698-6450	5	1	RESISTOR 2.5K .1% .125W F TC=0+-50	28480	0698-6450
A1A1R18	0698-8961	7	1	RESISTOR 909K 1% .125W F TC=0+-100	28480	0698-8961
A1A1R19	0757-0439	4		RESISTOR 6.81K 1% .125W F TC=0+-100	24546	C4-1/8-T0-6811-F
A1A1R20	0757-0463	4	1	RESISTOR 82.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-8252-F
A1A1R21	0698-3159	5	2	RESISTOR 26.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2612-F
A1A1R22	0698-3159	5		RESISTOR 26.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2612-F
A1A1R23	0757-0273	4	2	RESISTOR 3.01K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3011-F
A1A1R24	0757-0273	4		RESISTOR 3.01K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3011-F
A1A1R25	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A1A1R26	0757-0289	2	1	RESISTOR 13.3K 1% .125W F TC=0+-100	19701	MF4C1/8-T0-1332-F
A1A1R27	0757-0417	8	2	RESISTOR 562 1% .125W F TC=0+-100	24546	C4-1/8-T0-562R-F
A1A1R28	0757-0417	8		RESISTOR 562 1% .125W F TC=0+-100	24546	C4-1/8-T0-562R-F
A1A1R29	0761-0014	0	2	RESISTOR 180 5% 1W MO TC=0+-200	28480	0761-0014
A1A1R30	0761-0014	0		RESISTOR 180 5% 1W MO TC=0+-200	28480	0761-0014
A1A1R31	0757-0367	7	2	RESISTOR 100K 1% .5W F TC=0+-100	28480	0757-0367
A1A1R32	0757-0367	7		RESISTOR 100K 1% .5W F TC=0+-100	28480	0757-0367
A1A1R33	0698-3618	1	1	RESISTOR 82 5% 2W MO TC=0+-200	27167	FP42-2-T00-82R0-J
A1A1R34	0757-0394	0	2	RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-51R1-F
A1A1R35	0757-0394	0		RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-51R1-F
A1A1R36	0698-3432	7	1	RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
A1A1R37	0757-0428	1	1	RESISTOR 1.62K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1621-F
A1A1R38	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A1A1RT1	0837-0215	4	2	THERMISTOR-SURGE PTCTR USED AS SURGE	15454	SG220
A1A1RT2	0837-0215	4		THERMISTOR-SURGE PTCTR USED AS SURGE	15454	SG220
A1A1RT3	0837-0172	2	1	THERMISTOR DISC 2.5-OHM	15454	SG-3
A1A1RV1	0837-0120	0	2	VARISTOR-130VAC	28480	0837-0120
A1A1RV2	0837-0120	0		VARISTOR-130VAC	28480	0837-0120
A1A1SG1	1970-0050	8	2	TUBE-ELECTRON SURGE V PTCTR	28480	1970-0050
A1A1SG2	1970-0050	8		TUBE-ELECTRON SURGE V PTCTR	28480	1970-0050
A1A1T1	9100-4192	2	1	TRANSFORMER-BALUN	28480	9100-4192
A1A1T2	9100-2652	5	1	TRANSFORMER	28480	9100-2652
A1A1T3	9100-0417	6	1	TRANSFORMER-POWER 115/230V 48-66HZ	28480	9100-0417
A1A1T4	9100-2659	2	2	TRANSFORMER	28480	9100-2659
A1A1T5	9100-2659	2		TRANSFORMER	28480	9100-2659
A1A1TP1	0360-0535	0	3	TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A1A1TP2	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A1A1TP3	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A1A1U1	1826-0680	5	2	IC 8-DIP-P PKG	28480	1826-0680
A1A1U2	1826-0565	5	1	IC-TL494	28480	1826-0565
A1A1U3	1826-0065	0	1	IC COMPARATOR PRCN 8-DIP-P PKG	S0545	UPC311C
A1A1U4	1820-2111	9	1	IC DRVR TTL INV	01295	SN75468N
A1A1U5	1820-1423	4	1	IC MV TTL LS MONOSTBL RETRIG DUAL	01295	SN74LS123N
A1A1U6	1826-0680	5		IC 8-DIP-P PKG	28480	1826-0680
A1A1VR1	1826-0345	9	1	IC V RGLTR TO-220	07263	UA78M12UC
A1A1VR2	1826-0276	5	1	IC 78L05A V RGLTR TO-92	04713	MC78L05ACP
A1A1VR3	1826-0847	6	1	IC-REF-02	28480	1826-0847
A1A1XU1	1200-0796	8		SOCKET-IC 8-CONT DIP DIP-SLDR	28480	1200-0796
A1A1XU2	**1200-0607**	**4**		SOCKET-IC 16-CONT DIP-SLDR		**1200-0607**
A1A1XU3	1200-0796	8		SOCKET-IC 8-CONT DIP DIP-SLDR	28480	1200-0796
A1A1XU4	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1A1XU5	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1A1XU6	1200-0796	8		SOCKET-IC 8-CONT DIP DIP-SLDR	28480	1200-0796
A1A1S1	**3101-2150**	1		SWITCH-PB		**3101-2150**

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-5. A1A2 +5/–12V Board Replaceable Parts List

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1A2	64110-66524	4	1	BOARD ASSEMBLY, +5/-12	28480	64110-66524
A1A2C1	0160-4832	4	6	CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
A1A2C2	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
A1A2C3	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
A1A2C4	0180-2945	8	2	CAPACITOR-FXD 100UF+50-10% 35VDC AL	28480	0180-2945
A1A2C5	0180-2945	8		CAPACITOR-FXD 100UF+50-10% 35VDC AL	28480	0180-2945
A1A2C6	0180-0374	3	3	CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
A1A2C7	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
A1A2C8	0180-2946	9	1	CAPACITOR-FXD 330UF+50-10% 35VDC AL	28480	0180-2946
A1A2C9	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
A1A2C10	0180-2948	1	4	CAPACITOR-FXD 1000UF+50-10% 10VDC AL	28480	0180-2948
A1A2C12	0180-0116	1	1	CAPACITOR-FXD 6.8UF+-10% 35VDC TA	56289	150D685X9035B2
A1A2C13	0160-4835	7	1	CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
A1A2C14	0160-4822	2	2	CAPACITOR-FXD 1000PF +-5% 100VDC CER	28480	0160-4822
A1A2C15	0180-0197	8	2	CAPACITOR-FXD 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
A1A2C16	0180-0197	8		CAPACITOR-FXD 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
A1A2C17	0160-4822	2		CAPACITOR-FXD 1000PF +-5% 100VDC CER	28480	0160-4822
A1A2C18	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
A1A2C19	0160-0164	7	1	CAPACITOR-FXD .039UF +-10% 200VDC POLYE	28480	0160-0164
A1A2C20	0160-0161	4	1	CAPACITOR-FXD .01UF +-10% 200VDC POLYE	28480	0160-0161
A1A2C21	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
A1A2C22	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
A1A2C23	0180-2948	1		CAPACITOR-FXD 1000UF+50-10% 10VDC AL	28480	0180-2948
A1A2C24	0180-2948	1		CAPACITOR-FXD 1000UF+50-10% 10VDC AL	28480	0180-2948
A1A2C25	0180-2948	1		CAPACITOR-FXD 1000UF+50-10% 10VDC AL	28480	0180-2948
A1A2C26	0180-0291	3	4	CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
A1A2C27	0180-0291	3		CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
A1A2C28	0180-0291	3		CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
A1A2C29	0180-0291	3		CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
A1A2CR1	1906-0079	6	1	DIODE-FW BRDG 100V 10A	1B546	VJ148X
A1A2CR2	1906-0006	9	1	DIODE-FW BRDG 400V 1A	1B546	VE48
A1A2CR3	1901-0050	3	8	DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A1A2CR4	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A1A2CR5	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A1A2CR6	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A1A2CR7	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A1A2CR8	1906-0239	0	1	DIODE-CT-RECT 45V 30A	01281	SD-241
A1A2CR12	1901-0028	5	7	DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
A1A2CR13	1901-0028	5		DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
A1A2CR14	1901-0028	5		DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
A1A2CR15	1901-0028	5		DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
A1A2CR16	1901-0028	5		DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
A1A2CR17	1901-0028	5		DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
A1A2CR18	1901-0028	5		DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
A1A2CR19	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A1A2CR20	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A1A2CR21	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A1A2DS1	1990-0685	7	1	LED-LAMP LUM-INT=200UCD	28480	HLMP-6620
A1A2H16	2200-0139	4	2	SCREW-MACH 4-40 .25-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A1A2H23	2360-0117	6	4	SCREW-MACH 6-32 .375-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A1A2H24	2360-0121	2	1	SCREW-MACH 6-32 .5-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A1A2H50	2190-0005	0	2	WASHER-LK EXT T NO. 4 .116-IN-ID	28480	2190-0005
A1A2H52	2260-0001	5	2	NUT-HEX-DBL-CHAM 4-40-THD .094-IN-THK	28480	2260-0001
A1A2H56	2420-0001	5	1	NUT-HEX-W/LKWR 6-32-THD .109-IN-THK	00000	ORDER BY DESCRIPTION
A1A2H71	0380-0111	0	4	STANDOFF-RVT-ON .25-IN-LG 6-32THD	00000	ORDER BY DESCRIPTION
A1A2H72	0380-0843	5	2	STANDOFF-RVT-ON .125-IN-LG 4-40THD	00000	ORDER BY DESCRIPTION
A1A2H73	0590-0076	1	4	NUT-HEX-PLSTC LKG 4-40-THD .143-IN-THK	28480	0590-0076
A1A2H74	2200-0123	6	4	SCREW-MACH 4-40 1.25-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A1A2H75	2580-0003	5	1	NUT-HEX-W/LKWR 8-32-THD .125-IN-THK	00000	ORDER BY DESCRIPTION
A1A2H76	3050-0005	5	1	WASHER-SHLDR NO. 6 .14-IN-ID .375-IN-OD	28480	3050-0005
A1A2H77	3050-0239	7	3	WASHER-FL NM NO. 8 .17-IN-ID .375-IN-OD	28480	3050-0239
A1A2H78	3050-0791	6	6	INSULATOR-XSTR NYLON	28480	3050-0791
A1A2H79	0380-0327	0	4	SPACER-RND .125-IN-LG .09-IN-ID	28480	0380-0327
A1A2H80	1400-0249	0	2	CABLE TIE .062-.625-DIA .091-WD NYL	06383	PLT1M-8
A1A2J1	1251-3195	4	2	CONNECTOR 4-PIN M POST TYPE	28480	1251-3195
A1A2J2	1251-3195	4		CONNECTOR 4-PIN M POST TYPE	28480	1251-3195
A1A2L1	9140-0459	0	2	INDUCTOR 1MH 10%	28480	9140-0459
A1A2L2	9140-0459	0		INDUCTOR 1MH 10%	28480	9140-0459
A1A2L3	9140-0457	8	1	INDUCTOR 100UH 10%	28480	9140-0457
A1A2L4	9140-0500	2	1	INDUCTOR 22UH 10%	28480	9140-0500

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-5. A1A2 +5/–12V Board Replaceable Parts List (Cont'd)

Reference Designation	HP Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
A1A2MP1	1205-0219	0	1	HEAT SINK SGL TO-66-CS	28480	1205-0219
A1A2MP2	1205-0242	9	2	HEAT SINK SGL TO-3-CS	28480	1205-0242
A1A2MP3	1205-0242	9		HEAT SINK SGL TO-3-CS	28480	1205-0242
A1A2MP4	1205-0373	7	2	HEAT SINK SGL PLSTC-PWR-CS	13103	6030B-TT
A1A2MP5	1205-0373	7		HEAT SINK SGL PLSTC-PWR-CS	13103	6030B-TT
A1A2MP6	3103-0038	7	2	SWITCH-THERMAL	28480	3103-0038
A1A2MP7	3103-0038	7		SWITCH-THERMAL	28480	3103-0038
A1A2MP8	64110-61613	2	1	CABLE-TEMP REGULATOR	28480	64110-61613
A1A2MP9	64110-09101	3	2	SPRING-THERMAL BRACKET	28480	64110-09101
A1A2MP10	64110-09101	3		SPRING-THERMAL BRACKET	28480	64110-09101
A1A2Q1	1854-0215	1	2	TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A1A2Q2	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A1A2R1	0698-3156	2	1	RESISTOR 14.7K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1472-F
A1A2R2	0757-0437	2	6	RESISTOR 4.75K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4751-F
A1A2R3	0757-0283	6	2	RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2001-F
A1A2R4	0757-0437	2		RESISTOR 4.75K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4751-F
A1A2R5	0757-0280	3	6	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1A2R6	0757-0444	1	1	RESISTOR 12.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1212-F
A1A2R7	0757-0437	2		RESISTOR 4.75K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4751-F
A1A2R8	0757-0283	6		RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2001-F
A1A2R9	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1A2R10	0757-0437	2		RESISTOR 4.75K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4751-F
A1A2R11	0698-0084	9	1	RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
A1A2R12	0757-0437	2		RESISTOR 4.75K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4751-F
A1A2R13	0757-0437	2		RESISTOR 4.75K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4751-F
A1A2R14	0757-0428	1	1	RESISTOR 1.62K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1621-F
A1A2R15	0699-0752	0	2	RESISTOR 1.78K .1% .125W F TC=0+-25	28480	0699-0752
A1A2R16	0698-7518	8	2	RESISTOR 200 .25% .125W F TC=0+-50	19701	MF4C1/8-T2-200R-C
A1A2R17	0757-0458	7	2	RESISTOR 51.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5112-F
A1A2R18	0757-0290	5	1	RESISTOR 6.19K 1% .125W F TC=0+-100	19701	MF4C1/8-T0-6191-F
A1A2R19	0757-1094	9	1	RESISTOR 1.47K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1471-F
A1A2R20	0757-0458	7		RESISTOR 51.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5112-F
A1A2R21	0698-3215	4	1	RESISTOR 499K 1% .125W F TC=0+-100	28480	0698-3215
A1A2R22	0757-0465	6	2	RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
A1A2R23	0757-0442	9	2	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A1A2R24	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1A2R25	0757-0465	6		RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
A1A2R26	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A1A2R27	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1A2R28	0698-7518	8		RESISTOR 200 .25% .125W F TC=0+-50	19701	MF4C1/8-T2-200R-C
A1A2R29	0699-0752	0		RESISTOR 1.78K .1% .125W F TC=0+-25	28480	0699-0752
A1A2R30	0698-3696	5	1	RESISTOR 39 5% 1W MO TC=0+-200	27167	FP32-1-T00-39R0-J
A1A2R31	0698-0093	0	1	RESISTOR 10 5% 1W MO TC=0+-200	28480	0698-0093
A1A2R32	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1A2R33	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1A2R34	0757-0439	4	1	RESISTOR 6.81K 1% .125W F TC=0+-100	24546	C4-1/8-T0-6811-F
A1A2R35	0757-0346	2	1	RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
A1A2R36	2100-2633	5	1	RESISTOR-TRMR 1K 10% C SIDE-ADJ 1-TRN	30983	ET50X102
A1A2R37	0757-0431	6	1	RESISTOR 2.43K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2431-F
A1A2ST1	3103-0038	7		SWITCH-THERMAL	28480	3103-0038
A1A2ST2	3103-0038	7		SWITCH-THERMAL	28480	3103-0038
A1A2T1	9100-2657	0	1	TRANSFORMER	28480	9100-2657
A1A2U1	1826-0680	5	4	IC 8-DIP-P PKG	28480	1826-0680
A1A2U2	1820-1577	9	1	IC SCHMITT-TRIG CMOS NAND QUAD 2-INP	3L585	CD4093BF
A1A2U3	1820-2019	6	1	IC SCHMITT-TRIG CMOS HEX	04713	MC14584BCP
A1A2U4	1826-0680	5		IC 8-DIP-P PKG	28480	1826-0680
A1A2U5	1826-0680	5		IC 8-DIP-P PKG	28480	1826-0680
A1A2U6	1826-0680	5		IC 8-DIP-P PKG	28480	1826-0680
A1A2VR1	1826-0393	7	1	IC V RGLTR TO-220	27014	LM317T
A1A2VR2	1826-0221	0	1	IC V RGLTR TO-220	04713	MC7912CT
A1A2VR3	1826-0677	0	1	IC-LM338	28480	1826-0677
A1A2XU1	1200-0796	8	4	SOCKET-IC 8-CONT DIP DIP-SLDR	28480	1200-0796
A1A2XU2	1200-0638	7	2	SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A1A2XU3	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A1A2XU4	1200-0796	8		SOCKET-IC 8-CONT DIP DIP-SLDR	28480	1200-0796
A1A2XU5	1200-0796	8		SOCKET-IC 8-CONT DIP DIP-SLDR	28480	1200-0796
A1A2XU6	1200-0796	8		SOCKET-IC 8-CONT DIP DIP-SLDR	28480	1200-0796

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-6. A1A3 -3.25/-5.20V Board Replaceable Parts List

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1A3	64110-66514	2	1	BOARD ASSEMBLY-P.S. -3/-5	28480	64110-66514
A1A3C1	0160-4832	4	6	CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
A1A3C2	0160-4557	0	4	CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A1A3C3	0160-4833	5	2	CAPACITOR-FXD .022UF +-10% 100VDC CER	28480	0160-4833
A1A3C4	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A1A3C5	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A1A3C6	0160-5267	1	2	CAPACITOR-FXD 4700PF +-5% 50VDC CER	28480	0160-5267
A1A3C7	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
A1A3C8	0180-0197	8	4	CAPACITOR-FXD 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
A1A3C9	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
A1A3C10	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A1A3C11	0160-5267	1		CAPACITOR-FXD 4700PF +-5% 50VDC CER	28480	0160-5267
A1A3C12	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
A1A3C13	0180-0197	8		CAPACITOR-FXD 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
A1A3C14	0180-0197	8		CAPACITOR-FXD 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
A1A3C15	0160-0164	7	2	CAPACITOR-FXD .039UF +-10% 200VDC POLYE	28480	0160-0164
A1A3C16	0160-0164	7		CAPACITOR-FXD .039UF +-10% 200VDC POLYE	28480	0160-0164
A1A3C17	0180-2948	1	8	CAPACITOR-FXD 1000UF+50-10% 10VDC AL	28480	0180-2948
A1A3C18	0180-2948	1		CAPACITOR-FXD 1000UF+50-10% 10VDC AL	28480	0180-2948
A1A3C19	0180-2948	1		CAPACITOR-FXD 1000UF+50-10% 10VDC AL	28480	0180-2948
A1A3C20	0180-2948	1		CAPACITOR-FXD 1000UF+50-10% 10VDC AL	28480	0180-2948
A1A3C21	0180-2948	1		CAPACITOR-FXD 1000UF+50-10% 10VDC AL	28480	0180-2948
A1A3C22	0180-2948	1		CAPACITOR-FXD 1000UF+50-10% 10VDC AL	28480	0180-2948
A1A3C23	0180-2948	1		CAPACITOR-FXD 1000UF+50-10% 10VDC AL	28480	0180-2948
A1A3C24	0160-0155	6	2	CAPACITOR-FXD 3300PF +-10% 200VDC POLYE	28480	0160-0155
A1A3C25	0160-0155	6		CAPACITOR-FXD 3300PF +-10% 200VDC POLYE	28480	0160-0155
A1A3C26	0160-5149	8	2	CAPACITOR-FXD 3.3UF 250VDC	28480	0160-5149
A1A3C27	0160-5149	8		CAPACITOR-FXD 3.3UF 250VDC	28480	0160-5149
A1A3C28	0180-2948	1		CAPACITOR-FXD 1000UF+50-10% 10VDC AL	28480	0180-2948
A1A3C29	0180-0197	8		CAPACITOR-FXD 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
A1A3C30	0160-4808	4	1	CAPACITOR-FXD 470PF +-5% 100VDC CER	28480	0160-4808
A1A3C31	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
A1A3C32	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
A1A3C33	0160-4822	2	1	CAPACITOR-FXD 1000PF +-5% 100VDC CER	28480	0160-4822
A1A3C34	0160-4833	5		CAPACITOR-FXD .022UF +-10% 100VDC CER	28480	0160-4833
A1A3CR1	1906-0239	0	2	DIODE-CT-RECT 45V 30A	01281	SD-241
A1A3CR2	1906-0239	0		DIODE-CT-RECT 45V 30A	01281	SD-241
A1A3CR3	1901-0919	3	2	VOLTAGE SUPPRESSOR VRM=287V	28480	1901-0919
A1A3CR4	1906-0077	4	2	DIODE-FW BRDG 400V 5A	28480	1906-0077
A1A3CR5	1906-0077	4		DIODE-FW BRDG 400V 5A	28480	1906-0077
A1A3CR6	1901-0919	3		VOLTAGE SUPPRESSOR VRM=287V	28480	1901-0919
A1A3H23	2360-0117	6	8	SCREW-MACH 6-32 .375-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A1A3H71	0380-0111	0	8	STANDOFF-RVT-ON .25-IN-LG 6-32THD	00000	ORDER BY DESCRIPTION
A1A3H72	0380-0843	5	2	STANDOFF-RVT-ON .125-IN-LG 4-40THD	00000	ORDER BY DESCRIPTION
A1A3H73	0590-0076	1	2	NUT-HEX-PLSTC LKG 4-40-THD .143-IN-THK	28480	0590-0076
A1A3H74	2200-0123	6	2	SCREW-MACH 4-40 1.25-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A1A3H75	2580-0003	5	2	NUT-HEX-W/LKWR 8-32-THD .125-IN-THK	00000	ORDER BY DESCRIPTION
A1A3H76	3050-0005	5	2	WASHER-SHLDR NO. 6 .14-IN-ID .375-IN-OD	28480	3050-0005
A1A3H77	3050-0239	7	4	WASHER-FL NM NO. 8 .17-IN-ID .375-IN-OD	28480	3050-0239
A1A3H78	3050-0791	6	2	INSULATOR-XSTR NYLON	28480	3050-0791
A1A3J1	1251-3195	4	1	CONNECTOR 4-PIN M POST TYPE	28480	1251-3195
A1A3L1	9140-0500	2	2	INDUCTOR 22UH 10%	28480	9140-0500
A1A3L2	9140-0500	2		INDUCTOR 22UH 10%	28480	9140-0500
A1A3MP1	1205-0266	7	4	HEAT SINK SGL TO-3-CS	28480	1205-0266
A1A3MP2	0890-0029	0		POL SHK BLK .187	28480	0890-0029
A1A3Q1	1854-0215	1	2	TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A1A3Q2	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A1A3Q3	1855-0443	9	2	TRANSISTOR MOSFET N-CHAN E-MODE	28480	1855-0443
A1A3Q4	1855-0443	9		TRANSISTOR MOSFET N-CHAN E-MODE	28480	1855-0443
A1A3R1	0757-0280	3	5	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1A3R2	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1A3R3	0757-0449	6	4	RESISTOR 20K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2002-F
A1A3R4	0757-0401	0	4	RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101 -F
A1A3R5	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1A3R6	0757-0400	9	4	RESISTOR 90.9 1% .125W F TC=0+-100	24546	C4-1/8-T0-90R9-F
A1A3R7	0757-0464	5	2	RESISTOR 90.9K 1% .125W F TC=0+-100	24546	C4-1/8-T0-9092-F
A1A3R8	0757-0346	2	4	RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
A1A3R9	0757-0438	3	1	RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A1A3R10	0757-0449	6		RESISTOR 20K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2002-F

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-6. A1A3 -3.25/-5.20V Board Replaceable Parts List (Cont'd)

Reference Designation	HP Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
A1A3R11	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A1A3R12	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1A3R13	0757-0464	5		RESISTOR 90.9K 1% .125W F TC=0+-100	24546	C4-1/8-T0-9092-F
A1A3R14	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
A1A3R15	0757-0400	9		RESISTOR 90.9 1% .125W F TC=0+-100	24546	C4-1/8-T0-90R9-F
A1A3R16	0757-0449	6		RESISTOR 20K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2002-F
A1A3R17	0757-0439	4	2	RESISTOR 6.81K 1% .125W F TC=0+-100	24546	C4-1/8-T0-6811-F
A1A3R18	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1A3R19	0757-0446	3	3	RESISTOR 15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1502-F
A1A3R20	0757-0400	9		RESISTOR 90.9 1% .125W F TC=0+-100	24546	C4-1/8-T0-90R9-F
A1A3R22	0757-0317	7	1	RESISTOR 1.33K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1331-F
A1A3R23	0757-0449	6		RESISTOR 20K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2002-F
A1A3R24	0757-0439	4		RESISTOR 6.81K 1% .125W F TC=0+-100	24546	C4-1/8-T0-6811-F
A1A3R25	0757-0283	6	1	RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2001-F
A1A3R26	0698-4020	1	1	RESISTOR 9.53K 1% .125W F TC=0+-100	24546	C4-1/8-T0-9531-F
A1A3R27	0757-0400	9		RESISTOR 90.9 1% .125W F TC=0+-100	24546	C4-1/8-T0-90R9-F
A1A3R30	0757-0446	3		RESISTOR 15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1502-F
A1A3R31	0698-6612	1	1	RESISTOR 2K .1% .125W F TC=0+-50	28480	0698-6612
A1A3R32	0698-4081	4	1	RESISTOR 1.82K .1% .125W F TC=0+-50	03888	PME55-1/8-T2-1821-B
A1A3R33	0698-5449	0	1	RESISTOR 5K .1% .125W F TC=0+-50	19701	MF4C1/8-T2-5001-B
A1A3R34	0698-4200	9	1	RESISTOR 3.419K .25% .125W F TC=0+-100	03888	PME55-1/8-T0-3491R-C
A1A3R35	0698-3601	2	2	RESISTOR 10 5% 2W MO TC=0+-200	27167	FP42-2-T00-10R0-J
A1A3R36	0698-3601	2		RESISTOR 10 5% 2W MO TC=0+-200	27167	FP42-2-T00-10R0-J
A1A3R37	5020-2519	9	2	RESISTOR-FXD RES SEN 2 MEGOHM	28480	5020-2519
A1A3R38	0761-0044	6	2	RESISTOR 82 5% 1W MO TC=0+-200	28480	0761-0044
A1A3R39	0761-0044	6		RESISTOR 82 5% 1W MO TC=0+-200	28480	0761-0044
A1A3R40	5020-2519	9		RESISTOR-FXD RES SEN 2 MEGOHM	28480	5020-2519
A1A3R41	0757-0446	3		RESISTOR 15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1502-F
A1A3R42	0757-0398	4	1	RESISTOR 75 1% .125W F TC=0+-100	24546	C4-1/8-T0-75R0-F
A1A3R43	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
A1A3R44	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
A1A3R45	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A1A3R46	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A1A3T1	9100-2658	1	1	TRANSFORMER	28480	9100-2658
A1A3T2	9100-2656	9	1	TRANSFORMER	28480	9100-2656
A1A3U1	1820-1288	9	1	IC DRVR TTL CLOCK DRVR TTL-TO-MOS 1-INP	04713	MMH0026CL
A1A3U2	1826-0565	5	2	IC-TL494	28480	1826-0565
A1A3U3	1826-0065	0	2	IC COMPARATOR PRCN 8-DIP-P PKG	S0545	UPC311C
A1A3U4	1826-0065	0		IC COMPARATOR PRCN 8-DIP-P PKG	S0545	UPC311C
A1A3U5	1826-0565	5		IC-TL494	28480	1826-0565
A1A3UX1	1200-0607	0	3	SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1A3UX2	1200-0638	7	1	SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-7. A1A4 Interconnect Board Replaceable Parts List

Reference Designation	HP Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
A1A4	64110-66512	0	1	BOARD ASSEMBLY,P.S. INTERCONNECT	28480	64110-66512
A1A4J1	1251-6481	7	1	CONNECTOR-100 PIN	28480	1251-6481
A1A4J2	1200-0607	0	1	SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1A4J3	1251-6480	6	2	CONNECTOR-60 PIN	28480	1251-6480
A1A4J4	1251-6480	6		CONNECTOR-60 PIN	28480	1251-6480
A1A4R1	0757-0346	2	1	RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
A1A4R2	0698-8812	7	1	RESISTOR 1 1% .125W F TC=0+-100	28480	0698-8812

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-8. A2 Motherboard Replaceable Parts List

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A2	64110-66501	7	1	BOARD ASSEMBLY-MOTHERBOARD #1	28480	64110-66501
A2C1	0180-0094	4	1	CAPACITOR-FXD 100UF+75-10% 25VDC AL	56289	30D107G025DD2
A2H80	1400-0249	0	1	CABLE TIE .062-.625-DIA .091-WD NYL	06383	PLT1M-8
A2J1	1251-3024	8	1	CONNECTOR 26-PIN M RECTANGULAR	28480	1251-3024
A2J2	1251-5702	3	7	CONNECTOR-PC EDGE 43-CONT/ROW 2-ROWS	28480	1251-5702
A2J3	1251-5702	3		CONNECTOR-PC EDGE 43-CONT/ROW 2-ROWS	28480	1251-5702
A2J4	1251-5702	3		CONNECTOR-PC EDGE 43-CONT/ROW 2-ROWS	28480	1251-5702
A2J5	1251-5702	3		CONNECTOR-PC EDGE 43-CONT/ROW 2-ROWS	28480	1251-5702
A2J6	1251-5702	3		CONNECTOR-PC EDGE 43-CONT/ROW 2-ROWS	28480	1251-5702
A2J7	1251-5702	3		CONNECTOR-PC EDGE 43-CONT/ROW 2-ROWS	28480	1251-5702
A2J8	1251-5702	3		CONNECTOR-PC EDGE 43-CONT/ROW 2-ROWS	28480	1251-5702
A2J12	1251-4322	1	1	CONNECTOR 3-PIN M POST TYPE	28480	1251-4322
A2L1	9140-0254	3	1	INDUCTOR 430UH 10% .6DX1.6LG	28480	9140-0254
A2MP1	0590-0519	7	8	THREADED INSERT-NUT 4-40 .062-IN-LG STL	28480	0590-0519
A2MP2	1251-7112	3	2	CONNECTOR-4 PIN	28480	1251-7112
A2MP3	1251-5595	2	2	POLARIZING KEY-POST CONN	28480	1251-5595
A2R1	0698-3440	7	1	RESISTOR 196 1% .125W F TC=0+-100	24546	C4-1/8-T0-196R-F
A2R2	0757-0404	3	1	RESISTOR 130 1% .125W F TC=0+-100	24546	C4-1/8-T0-131-F
A2R3	0683-2225	3	1	RESISTOR 2.2K 5% .25W FC TC=-400/+700	01121	CB2225
A2TP1	0360-0535	0	7	TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A2TP2	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A2TP3	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A2TP4	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A2TP5	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A2TP6	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A2TP7	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A2U1	1810-0288	6	3	NETWORK-RES 10-SIP MULTI-VALUE	28480	1810-0288
A2U2	1810-0288	6		NETWORK-RES 10-SIP MULTI-VALUE	28480	1810-0288
A2U3	1810-0288	6		NETWORK-RES 10-SIP MULTI-VALUE	28480	1810-0288

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-9. A3 CPU/IO Board Replaceable Parts List

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A3	64110-66507	3	1	BOARD ASSEMBLY- CPU/I.O.	28480	64110-66507
A3C1	0160-2055	9	40	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C2	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C3	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C4	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C5	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C6	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C7	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C8	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C9	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C10	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C11	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C12	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C13	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C14	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C15	0180-0228	6	3	CAPACITOR-FXD 22UF+-10% 15VDC TA	56289	150D226X9015B2
A3C16	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C17	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C18	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C19	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C20	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C21	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C22	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C23	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C24	0180-0197	8	1	CAPACITOR-FXD 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
A3C25	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C26	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C27	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C28	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C29	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C30	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C31	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C32	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C33	0180-0228	6		CAPACITOR-FXD 22UF+-10% 15VDC TA	56289	150D226X9015B2
A3C34	0180-0116	1	1	CAPACITOR-FXD 6.8UF+-10% 35VDC TA	56289	150D685X9035B2
A3C35	0180-0228	6		CAPACITOR-FXD 22UF+-10% 15VDC TA	56289	150D226X9015B2
A3C36	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C37	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C38	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C39	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C40	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C41	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C42	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C43	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C44	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3C45	0160-2308	5	1	CAPACITOR-FXD 36PF +-5% 300VDC MICA	28480	0160-2308
A3C46	0180-0309	4	1	CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A3C47	0140-0200	0	3	CAPACITOR-FXD 390PF +-5% 300VDC MICA	72136	DM15F391J0300WV1CR
A3C48	0140-0200	0		CAPACITOR-FXD 390PF +-5% 300VDC MICA	72136	DM15F391J0300WV1CR
A3C49	0140-0200	0		CAPACITOR-FXD 390PF +-5% 300VDC MICA	72136	DM15F391J0300WV1CR
A3C50	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A3E1	1258-0182	7	5	CONNECTOR-R & P 1 MALE PLUG	28480	1258-0182
A3E2	1258-0182	7		CONNECTOR-R & P 1 MALE PLUG	28480	1258-0182
A3E3	1258-0182	7		CONNECTOR-R & P 1 MALE PLUG	28480	1258-0182
A3E4	1258-0153	2	1	PROGRAM HEADER	28480	1258-0153
A3E10	1258-0182	7		CONNECTOR-R & P 1 MALE PLUG	28480	1258-0182
A3E11	1258-0182	7		CONNECTOR-R & P 1 MALE PLUG	28480	1258-0182
A3H78	3050-0791	6	1	INSULATOR-XSTR NYLON	28480	3050-0791
A3H86	2260-0009	3	7	NUT-HEX-W/LKWR 4-40-THD .094-TN-THK	00000	ORDER BY DESCRIPTION
A3H87	2200-0143	0	1	SCREW-MACH 4-40 .375-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A3H92	**8151-0013**		**1**	FINE WIRE		
A3J5	1251-4388	9	1	CONNECTOR 3-PIN M POST TYPE	28480	1251-4388
A3L1	9140-0112	2	1	INDUCTOR RF-CH-MLD 4.7UH 10%	28480	9140-0112
A3MP1	1205-0338	4	1	HEAT SINK SGL PLSTC-PWR-CS	28480	1205-0338
A3MP2	09825-67908	8	1	GASKET-BPC	28480	09825-67908
A3MP3	1480-0116	8	2	PIN-GRV .062-IN-DIA .25-IN-LG STL	28480	1480-0116
A3MP4	1480-0116	8		PIN-GRV .062-IN-DIA .25-IN-LG STL	28480	1480-0116
A3MP5	5040-6069	4	2	EXTRACTOR-BLUE	28480	5040-6069
A3MP6	5040-6069	4		EXTRACTOR-BLUE	28480	5040-6069
A3MP7	1200-0844	7	2	RETAINER-SUBSTRATE STEEL; NICKEL PLATE	28480	1200-0844
A3MP8	1200-0847	0	1	SOCKET-SBSTR 48-CONT CERAMIC DIP-SLDR	28480	1200-0847

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-9. A3 CPU/IO Board Replaceable Parts List (Cont'd)

Reference Designation	HP Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
A3R1	0757-0290	5	3	RESISTOR 6.19K 1% .125W F TC=0+-100	19701	MF4C1/8-T0-6191-F
A3R2	0757-0290	5		RESISTOR 6.19K 1% .125W F TC=0+-100	19701	MF4C1/8-T0-6191-F
A3R3	0757-0280	3	5	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A3R4	0698-3159	5	1	RESISTOR 26.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2612-F
A3R5	0757-0290	5		RESISTOR 6.19K 1% .125W F TC=0+-100	19701	MF4C1/8-T0-6191-F
A3R6	2100-3212	8	1	RESISTOR-TRMR 200 10% C TOP-ADJ 1-TRN	28480	2100-3212
A3R7	0757-0422	5	1	RESISTOR 909 1% .125W F TC=0+-100	24546	C4-1/8-T0-909R-F
A3R8	0757-0282	5	1	RESISTOR 221 1% .125W F TC=0+-100	24546	C4-1/8-T0-221R-F
A3R9	0698-3432	7	2	RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
A3R10	0757-0200	7	2	RESISTOR 5.62K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5621-F
A3R11	0698-3432	7		RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
A3R12	0757-0200	7		RESISTOR 5.62K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5621-F
A3R13	0698-3446	3	2	RESISTOR 383 1% .125W F TC=0+-100	24546	C4-1/8-T0-383R-F
A3R14	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A3R15	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A3R16	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A3R17	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A3R18	0757-0449	6	1	RESISTOR 20K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2002-F
A3R19	0698-3446	3		RESISTOR 383 1% .125W F TC=0+-100	24546	C4-1/8-T0-383R-F
A3R20	0757-0442	9	1	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A3S1	3101-2138	8	1	SWITCH-PB SPDT MOM .02A 20VAC	28480	3101-2138
A3TP1	0360-0535	0	17	TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP2	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP4	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP5	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP6	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP7	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP8	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP9	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP10	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP11	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP12	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP13	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP15	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP16	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP17	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP18	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3TP19	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A3U1	1820-2058	3	4	IC MISC TTL S QUAD	07263	MC3448AL
A3U2	1810-0519	6	2	NETWORK-RES 11-SIP MULTI-VALUE	28480	1810-0519
A3U3	1810-0519	6		NETWORK-RES 11-SIP MULTI-VALUE	28480	1810-0519
A3U4	1820-2058	3		IC MISC TTL S QUAD	07263	MC3448AL
A3U5	**1820-2058**			**IC-MISC TTL S QUAD**	**07263**	**MC3448AL**
A3U6	1820-1243	6	2	IC GATE TTL LS AND TPL 3-INP	01295	SN74LS15N
A3U7	1820-1197	9	2	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A3U8	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A3U9	1816-1092	4	1	IC-27LS00N RAM	28480	1816-1092
A3U10	1820-1989	7	2	IC CNTR TTL LS BIN DUAL 4-BIT	07263	74LS393PC
A3U11	1820-2024	3	9	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A3U12	1820-1216	3	2	IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A3U13	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A3U14	1810-0276	2	7	NETWORK-RES 10-SIP1.5K OHM X 9	01121	210A152
A3U15	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A3U16	1810-0276	2		NETWORK-RES 10-SIP1.5K OHM X 9	01121	210A152
A3U17	1820-0693	8	3	IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
A3U18	1820-1199	1	1	IC INV TTL LS HEX 1-INP	01295	SN74LS04N
A3U19	1820-2058	3		IC MISC TTL S QUAD	07263	MC3448AL
A3U20	1820-1211	8	1	IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS86N
A3U21	1810-0276	2		NETWORK-RES 10-SIP1.5K OHM X 9	91121	210A152
A3U22	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A3U23	1820-1917	1	5	IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
A3U24	1820-1730	6	2	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A3U25	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A3U26	1820-1281	2	3	IC DCDR TTL LS 2-TO-4-LINE DUAL 2-INP	01295	SN74LS139N
A3U27	1820-1917	1		IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
A3U28	1820-1216	3		IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A3U29	5061-3011	4	1	HYBRID-BPC	28480	5061-3011
A3U30	1820-1208	3	2	IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
A3U31	1810-0276	2		NETWORK-RES 10-SIP1.5K OHM X 9	01121	210A152
A3U32	1820-1212	9	2	IC FF TTL LS J-K NEG-EDGE-TRIG	01295	SN74LS112AN
A3U33	1820-1112	8	5	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A3U34	1820-1144	6	1	IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
A3U35	1820-1205	0	1	IC GATE TTL LS AND DUAL 4-INP	01295	SN74LS21N
A3U36	1AA6-6004	0	1	IC-PHI CHIP	28480	1AA6-6004

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-9. A3 CPU/IO Board Replaceable Parts List (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A3U37	1820-1208	3		IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
A3U38	1820-1195	7	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS175N
A3U39	1810-0276	2		NETWORK-RES 10-SIP1.5K OHM X 9	01121	210A152
A3U40	1820-2206	3	2	IC MISC TTL LS	01295	SN74LS640N
A3U41	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A3U42	1810-0276	2		NETWORK-RES 10-SIP1.5K OHM X 9	01121	210A152
A3U43	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A3U44	1810-0280	8	2	NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
A3U45	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A3U46	1810-0276	2		NETWORK-RES 10-SIP1.5K OHM X 9	01121	210A152
A3U47	1820-2206	3		IC MISC TTL LS	01295	SN74LS640N
A3U48	64110-10006	0	4	**ROM 1**		**64110-10018**
A3U49	64110-10007	1		**ROM 3**		**64110-10018**
A3U50	64110-10005	9		**ROM 2**		**64110-10018**
A3U51	64110-10004	8		**ROM 0**		**64110-10018**
A3U52	1810-0280	8		NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
A3U53	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A3U54	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A3U55	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A3U56	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A3U57	1820-0693	8		IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
A3U58	1820-1281	2		IC DCDR TTL LS 2-TO-4-LINE DUAL 2-INP	01295	SN74LS139N
A3U59	1820-1243	6		IC GATE TTL LS AND TPL 3-INP	01295	SN74LS15N
A3U60	1820-1322	2	1	IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
A3U61	1820-1423	4	1	IC MV TTL LS MONOSTBL RETRIG DUAL	01295	SN74LS123N
A3U62	1820-1212	9		IC FF TTL LS J-K NEG-EDGE-TRIG	01295	SN74LS112AN
A3U63	1820-1989	7		IC CNTR TTL LS BIN DUAL 4-BIT	07263	74LS393PC
A3U64	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A3U65	1820-0693	8		IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
A3U66	1810-0278	4	1	NETWORK-RES 10-SIP3.3K OHM X 9	01121	210A332
A3U67	1820-1281	2		IC DCDR TTL LS 2-TO-4-LINE DUAL 2-INP	01295	SN74LS139N
A3U68	1820-1204	9	1	IC GATE TTL LS NAND DUAL 4-INP	01295	SN74LS20N
A3U69	1820-1917	1		IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
A3U70	1820-1917	1		IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
A3U71	1820-2102	8	2	IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
A3U72	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
A3U73	1820-1240	3	1	IC DCDR TTL S 3-TO-8-LINE 3-INP	01295	SN74S138N
A3U74	1820-1917	1		IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
A3U75	1820-1072	9	1	IC DCDR TTL S 2-TO-4-LINE DUAL 2-INP	01295	SN74S139N
A3U76	1820-0539	1	1	IC BFR TTL NAND QUAD 2-INP	01295	SN7437N
A3U77	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A3U78	1820-1425	6	1	IC SCHMITT-TRIG TTL LS NAND QUAD 2-INP	01295	SN74LS132N
A3U79	1820-1288	9	1	IC DRVR TTL CLOCK DRVR TTL-TO-MOS 1-INP	04713	MMH0026CL
A3VR1	1826-0393	7	1	IC V RGLTR TO-220	27014	LM317T
A3XE1	1251-1556	7	4	CONNECTOR-SGL CONT SKT .018-IN-BSC-SZ	28480	1251-1556
A3XE2	1251-1556	7		CONNECTOR-SGL CONT SKT .018-IN-BSC-SZ	28480	1251-1556
A3XE3	1251-1556	7		CONNECTOR-SGL CONT SKT .018-IN-BSC-SZ	28480	1251-1556
A3XE10	1251-1556	7		CONNECTOR-SGL CONT SKT .018-IN-BSC-SZ	28480	1251-1556
A3XE11	1251-1556	7		CONNECTOR-SGL CONT SKT .018-IN-BSC-SZ	28480	1251-1556
A3XU1	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A3XU2	1200-0612	7	2	SOCKET-IC 22-CONT DIP DIP-SLDR	28480	1200-0612
A3XU3	1200-0612	7		SOCKET-IC 22-CONT DIP DIP-SLDR	28480	1200-0612
A3XU4	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A3XU5	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A3XU10	1200-0638	7	1	SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A3XU19	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A3XU22	1200-0639	8	11	SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A3XU23	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A3XU24	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A3XU25	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A3XU40	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A3XU43	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A3XU45	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A3XU47	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A3XU48	1200-0541	1	4	SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
A3XU49	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
A3XU50	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
A3XU51	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
A3XU53	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A3XU54	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A3XU61	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A3XU74	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-10. A4 Keyboard Replaceable Parts List

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A4	64110-66502	8	1	BOARD ASSEMBLY-KEYBOARD	28480	64110-66502
A4C1	0160-2055	9	4	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C2	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C3	0180-0309	4	1	CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A4C4	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C5	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C6	0140-0199	6	1	CAPACITOR-FXD 240PF +-5% 300VDC MICA	72136	DM15F241J0300WV1CR
A4H70	0624-0270	0	2	SCREW-TPG 2-32 .25-IN-LG PAN-HD-SLT	00000	ORDER BY DESCRIPTION
A4J1	1251-5649	7	1	CONNECTOR 20-PIN M POST TYPE	28480	1251-5649
A4L1	9100-2247	4	1	INDUCTOR RF-CH-MLD 100NH 10% .105DX.26LG	28480	9100-2247
A4MP1	0371-2382	2	8	KEY CAP-SOFT	28480	0371-2382
A4MP2	0371-2382	2		KEY CAP-SOFT	28480	0371-2382
A4MP3	0371-2382	2		KEY CAP-SOFT	28480	0371-2382
A4MP4	0371-2382	2		KEY CAP-SOFT	28480	0371-2382
A4MP5	0371-2382	2		KEY CAP-SOFT	28480	0371-2382
A4MP6	0371-2382	2		KEY CAP-SOFT	28480	0371-2382
A4MP7	0371-2382	2		KEY CAP-SOFT	28480	0371-2382
A4MP8	0371-2382	2		KEY CAP-SOFT	28480	0371-2382
A4MP9	0371-2262	7	1	KEY CAP "CLR LINE"	28480	0371-2262
A4MP10	0371-2261	6	1	KEY CAP "RECALL"	28480	0371-2261
A4MP11	0371-2260	5	1	KEY CAP "LOCK"	28480	0371-2260
A4MP12	0371-2259	2	1	KEY CAP "RESET"	28480	0371-2259
A4MP13	0371-2241	2	1	KEY CAP "1"	28480	0371-2241
A4MP14	0371-2240	1	1	KEY CAP "2"	28480	0371-2240
A4MP15	0371-2239	8	1	KEY CAP "3"	28480	0371-2239
A4MP16	0371-2238	7	1	KEY CAP "4"	28480	0371-2238
A4MP17	0371-2237	6	1	KEY CAP "5"	28480	0371-2237
A4MP18	0371-2236	5	1	KEY CAP "6"	28480	0371-2236
A4MP19	0371-2235	4	1	KEY CAP "7"	28480	0371-2235
A4MP20	0371-2234	3	1	KEY CAP "8"	28480	0371-2234
A4MP21	0371-2258	1	1	KEY CAP "9"	28480	0371-2258
A4MP22	0371-2257	0	1	KEY CAP "0"	28480	0371-2257
A4MP23	0371-2245	6	1	KEY CAP "EQUAL"	28480	0371-2245
A4MP24	0371-2244	5	1	KEY CAP "UP & SQIGGL"	28480	0371-2244
A4MP25	0371-2256	9	1	KEY CAP "REV.SLASH"	28480	0371-2256
A4MP26	0371-2227	4	1	KEY CAP "BACKSPACE"	28480	0371-2227
A4MP27	0371-2243	4	1	KEY CAP "INSERT CHAR"	28480	0371-2243
A4MP28	0371-2242	3	1	KEY CAP "DELETE CHAR"	28480	0371-2242
A4MP29	0371-2228	5	1	KEY CAP "TAB"	28480	0371-2228
A4MP30	0371-2217	2	1	KEY CAP "Q"	28480	0371-2217
A4MP31	0371-2223	0	1	KEY CAP "W"	28480	0371-2223
A4MP32	0371-2205	8	1	KEY CAP "E"	28480	0371-2205
A4MP33	0371-2218	3	1	KEY CAP "R"	28480	0371-2218
A4MP34	0371-2220	7	1	KEY CAP "T"	28480	0371-2220
A4MP35	0371-2225	2	1	KEY CAP "Y"	28480	0371-2225
A4MP36	0371-2221	8	1	KEY CAP "U"	28480	0371-2221
A4MP37	0371-2209	2	1	KEY CAP "I"	28480	0371-2209
A4MP38	0371-2215	0	1	KEY CAP "O"	28480	0371-2215
A4MP39	0371-2216	1	1	KEY CAP "P"	28480	0371-2216
A4MP40	0371-2246	7	1	KEY CAP "AT SIGN"	28480	0371-2246
A4MP41	0371-2230	9	1	KEY CAP "LFT BRACKET"	28480	0371-2230
A4MP42	0371-2247	8	1	KEY CAP "DEL"	28480	0371-2247
A4MP43	0371-2250	3	1	KEY CAP "ROLL UP"	28480	0371-2250
A4MP44	0371-2254	7	2	KEY CAP "ARROW UP"	28480	0371-2254
A4MP45	0371-2251	4	1	KEY CAP "NEXT PAGE"	28480	0371-2251
A4MP46	0371-2255	8	1	KEY CAP "CNTL"	28480	0371-2255
A4MP47	0371-2201	4	1	KEY CAP "A"	28480	0371-2201
A4MP48	0371-2219	4	1	KEY CAP "S"	28480	0371-2219
A4MP49	0371-2204	7	1	KEY CAP "D"	28480	0371-2204
A4MP50	0371-2206	9	1	KEY CAP "F"	28480	0371-2206
A4MP51	0371-2207	0	1	KEY CAP "G"	28480	0371-2207
A4MP52	0371-2208	1	1	KEY CAP "H"	28480	0371-2208
A4MP53	0371-2210	5	1	KEY CAP "J"	28480	0371-2210
A4MP54	0371-2211	6	1	KEY CAP "K"	28480	0371-2211
A4MP55	0371-2212	7	1	KEY CAP "L"	28480	0371-2212
A4MP56	0371-2248	9	1	KEY CAP "SEMICOL"	28480	0371-2248
A4MP57	0371-2249	0	1	KEY CAP "COL & STAR"	28480	0371-2249
A4MP58	0371-2229	6	1	KEY CAP "RT BRACKET"	28480	0371-2229
A4MP59	0371-2263	8	1	KEY CAP "RETURN"	28480	0371-2263
A4MP60	0371-2264	9	2	KEY CAP "ARO/L"	28480	0371-2264

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-10. A4 Keyboard Replaceable Parts List (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A4MP61	0371-2264	9		KEY CAP "ARO/R"	28480	0371-2264
A4MP62	0371-2265	0	2	KEY CAP "SHIFT"	28480	0371-2265
A4MP63	0371-2226	3	1	KEY CAP "Z"	28480	0371-2226
A4MP64	0371-2224	1	1	KEY CAP "X"	28480	0371-2224
A4MP65	0371-2203	6	1	KEY CAP "C"	28480	0371-2203
A4MP66	0371-2222	9	1	KEY CAP "V"	28480	0371-2222
A4MP67	0371-2202	5	1	KEY CAP "B"	28480	0371-2202
A4MP68	0371-2214	9	1	KEY CAP "N"	28480	0371-2214
A4MP69	0371-2213	8	1	KEY CAP "M"	28480	0371-2213
A4MP70	0371-2232	1	1	KEY CAP "COMMA"	28480	0371-2232
A4MP71	0371-2233	2	1	KEY CAP "PERIOD"	28480	0371-2233
A4MP72	0371-2231	0	1	KEY CAP "SLASH"	28480	0371-2231
A4MP73	0371-2265	0		KEY CAP "SHIFT"	28480	0371-2265
A4MP74	0371-2253	6	1	KEY CAP "PREV PAGE"	28480	0371-2253
A4MP75	0371-2254	7		KEY CAP "ARROW DOWN"	28480	0371-2254
A4MP76	0371-2252	5	1	KEY CAP "ROLL DOWN"	28480	0371-2252
A4MP77	0371-1490	1	1	SPACE BAR	28480	0371-1490
A4MP78	1530-0344	1	2	LINK	28480	1530-0344
A4MP79	1530-0345	2	2	CRANK GUIDE	28480	1530-0345
A4MP80	1460-1841	6	1	CRANK	28480	1460-1841
A4R1	0757-0401	0	1	RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A4R2	0757-0346	2	1	RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
A4S76	3101-2409	6	76	SWITCH-PB SPST-NO MOM .1A	28480	3101-2409
A4S77	3101-2466	5	1	SWITCH-PB SPST-NO MOM .1A	28480	3101-2466
A4U1	1820-1240	3	2	IC DCDR TTL S 3-TO-8-LINE 3-INP	01295	SN74S138N
A4U2	1820-1240	3		IC DCDR TTL S 3-TO-8-LINE 3-INP	01295	SN74S138N
A4U3	1906-0229	8	12	DIODE-ARRAY 50V 400MA	01295	TID133
A4U4	1906-0229	8		DIODE-ARRAY 50V 400MA	01295	TID133
A4U5	1906-0229	8		DIODE-ARRAY 50V 400MA	01295	TID133
A4U6	1906-0229	8		DIODE-ARRAY 50V 400MA	01295	TID133
A4U7	1906-0229	8		DIODE-ARRAY 50V 400MA	01295	TID133
A4U8	1906-0229	8		DIODE-ARRAY 50V 400MA	01295	TID133
A4U9	1820-1217	4	1	IC MUXR/DATA-SEL TTL LS 8-TO-1-LINE	01295	SN74LS151N
A4U10	1826-0138	8	2	IC COMPARATOR GP QUAD 14-DIP-P PKG	01295	LM339N
A4U11	1826-0138	8		IC COMPARATOR GP QUAD 14-DIP-P PKG	01295	LM339N
A4U12	1906-0229	8		DIODE-ARRAY 50V 400MA	01295	TID133
A4U13	1906-0229	8		DIODE-ARRAY 50V 400MA	01295	TID133
A4U14	1906-0229	8		DIODE-ARRAY 50V 400MA	01295	TID133
A4U15	1906-0229	8		DIODE-ARRAY 50V 400MA	01295	TID133
A4U16	1906-0229	8		DIODE-ARRAY 50V 400MA	01295	TID133
A4U17	1906-0229	8		DIODE-ARRAY 50V 400MA	01295	TID133
A4U18	1810-0275	1	2	NETWORK-RES 10-SIP1.0K OHM X 9	01121	210A102
A4U19	1810-0275	1		NETWORK-RES 10-SIP1.0K OHM X 9	01121	210A102
A4VR1	1902-3002	3	1	DIODE-ZNR 2.37V 5% DO-7 PD=.4W TC=-.074%	28480	1902-3002
A4W1			**1**	**GROUND WIRE**		

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-11. A5 Display Controller Replaceable Parts List

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A5	64100-66519	5	1	DISPLAY CONTROLLER BOARD ASSEMBLY	28480	64100-66519
C1,2	0160-2055	9	30	CAPACITOR-FXD .01μF +80-20% 100VDC CER	28480	0160-2055
C3	0160-4822	2	1	CAPACITOR-FXD 1000Pf +-5% 100VDC CER	28480	0160-4822
C4,5	0160-2055	9		CAPACITOR-FXD .01μF +80-20% 100VDC CER	28480	0160-2055
C6	0160-3622	8	42	CAPACITOR-FXD .1μF +80-20% 100VDC CER	28480	0160-3622
C7	0160-2055	9		CAPACITOR-FXD .01μF +80-20% 100VDC CER	28480	0160-2055
C8,9	0160-3622	8		CAPACITOR-FXD .1μF +80-20% 100VDC CER	28480	0160-3622
C10	0160-2055	9		CAPACITOR-FXD .01μF +80-20% 100VDC CER	28480	0160-2055
C11	0160-3622	8		CAPACITOR-FXD .1μF +80-20% 100VDC CER	28480	0160-3622
C12	0160-2055	9		CAPACITOR-FXD .01μF +80-20% 100VDC CER	28480	0160-2055
C13,-15	0160-3622	8		CAPACITOR-FXD .1μF +80-20% 100VDC CER	28480	0160-3622
C16	0160-2055	9		CAPACITOR-FXD .01μF +80-20% 100VDC CER	28480	0160-2055
C17-22	0160-3622	8		CAPACITOR-FXD .1μF +80-20% 100VDC CER	28480	0160-3622
C23	0160-2055	9		CAPACITOR-FXD .01μF +80-20% 100VDC CER	28480	0160-2055
C24,25	0160-3622	8		CAPACITOR-FXD .1μF +80-20% 100VDC CER	28480	0160-3622
C26,27	0160-2055	9		CAPACITOR-FXD .01μF +80-20% 100VDC CER	28480	0160-2055
C28,30	0160-3622	8		CAPACITOR-FXD .1μF +80-20% 100VDC CER	28480	0160-3622
C31	0160-2055	9		CAPACITOR-FXD .01μF +80-20% 100VDC CER	28480	0160-2055
C32-37	0160-3622	8		CAPACITOR-FXD .1μF +80-20% 100VDC CER	28480	0160-3622
C38	0160-2055	9		CAPACITOR-FXD .01μF +80-20% 100VDC CER	28480	0160-2055
C39,40	0160-3622	8		CAPACITOR-FXD .1μF +80-20% 100VDC CER	28480	0160-3622
C41,42	0160-2055	9		CAPACITOR-FXD .01μF +80-20% 100VDC CER	28480	0160-2055
C43-45	0160-3622	8		CAPACITOR-FXD .1μF +80-20% 100VDC CER	28480	0160-3622
C46	0160-2055	9		CAPACITOR-FXD .01μF +80-20% 100VDC CER	28480	0160-2055
C47-52	0160-3622	8		CAPACITOR-FXD .1μF +80-20% 100VDC CER	28480	0160-3622
C53	0160-2055	9		CAPACITOR-FXD .01μF +80-20% 100VDC CER	28480	0160-2055
C54,55	0160-3622	8		CAPACITOR-FXD .1μF +80-20% 100VDC CER	28480	0160-3622
C56,57	0160-2055	9		CAPACITOR-FXD .01μF +80-20% 100VDC CER	28480	0160-2055
C58	0160-3622	8		CAPACITOR-FXD .1μF +80-20% 100VDC CER	28480	0160-3622
C59	0160-2055	9		CAPACITOR-FXD .01μF +80-20% 100VDC CER	28480	0160-2055
C60-62	0160-3622	8		CAPACITOR-FXD .1μF +80-20% 100VDC CER	28480	0160-3622
C63	0160-2055	9		CAPACITOR-FXD .01μF +80-20% 100VDC CER	28480	0160-2055
C64	0160-3622	8		CAPACITOR-FXD .1μF +80-20% 100VDC CER	28480	0160-3622
C65,66	0160-2055	9		CAPACITOR-FXD .01μF +80-20% 100VDC CER	28480	0160-2055
C67,68	0180-0374	3	2	CAPACITOR-FXD 10μF +-10% 20VDC TA	56289	150D106X902082
C69	0160-2055	9		CAPACITOR-FXD .01μF +80-20% 100VDC CER	28480	0160-2055
C70	0180-0116	1	1	CAPACITOR-FXD 6.8μF +-10% 35VDC TA	56289	150D685X9035B2
C71-76	0160-2055	9		CAPACITOR-FXD .01μF +80-20% 100VDC CER	28480	0160-2055
CR1-4	1901-0535	9	4	DIODE-SM SIG SCHOTTKY	28480	1901-0535
L1	9170-0029	3	2	CORE-SHIELDING BEAD	28480	9170-0029
MP1,2	5040-6067	2	2	PC EXTRACTOR	28480	5040-6067
P2,3	1258-0182	7	2	TEST JUMPER	28480	1258-0182
P4	1810-0307	0	1	NETWORK-CNDCT MODULE DIP; 16 PINS; 0.100	28480	1810-0307
R1-4	0757-0280	3	11	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R5	0698-3438	3	1	RESISTOR 147 1% .125W F TC=0+-100	28480	0698-3438
R6-9	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R10-15	0698-7028	5	6	RESISTOR 27 10% .125W CC TC=-270/+540	01121	BB2701
R16-18	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R19	0684-1211	7	1	RESISTOR 120 10% .25W FC TC=-400/+600	01121	CB1211
TP1-13	0360-0535	0	20	TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
TPGND	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
U1	1820-0681	4	3	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U2	1820-1453	0	2	IC CNTR TTL S BIN SYNCHRO POS-EDGE-TRIG	01295	SN74S163N
U3,4	1820-1917	1	2	IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U5	1820-1201	6	1	IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
U6	1820-1453	0		IC CNTR TTL S BIN SYNCHRO POS-EDGE-TRIG	01295	SN74S163N
U7	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U8	1820-1112	8	3	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74N
U9	1820-1322	2	2	IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U10	1820-0629	0	2	IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U11	1820-1449	4	1	GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U12	1820-0693	8	3	IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
U13	1820-1144	6	2	IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02
U14	1820-0683	6	2	IC INV TTL S HEX 1-INP	01295	SN74S04N
U15	1820-1208	3	4	IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
U16	1820-0688	1	2	IC GATE TTL S NAND DUAL 4-INP	01295	SN74S20N
U17	1820-1211	8	1	IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS86N
U18	1820-0629	0		IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U19	1820-1197	9	1	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U20	1820-0688	1		IC GATE TTL S NAND DUAL 4-INP	01295	SN74S20N
U21	1820-0683	6		IC INV TTL S HEX 1 INP	01295	SN74S04N
U22	1820-1322	2		IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U23-30	1818-1396	5	32	IC NMOS 16348-BIT RAM DYN 200NS 3S	50088	MK4116N-3
U31,32	1820-2024	3	3	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U33	1820-2191	5	1	IC MICROPROC-ACCESS NMOS 8-BIT	34649	C8275
U34	1810-0536	7	1	NETWORK-RES 27OHM 16 PIN DIP	28480	1810-0536
U35	1820-1144	6		IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
U36	1820-1208	3		IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
U37	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U38-45	1818-1396	5	32	IC NMOS 16384-BIT RAM DYN 200-NS 3-S	50088	MK4116N-3
U46	1820-1997	7	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U47	1820-1208	3		IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
U48	1820-0693	8		IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
U49,50	1820-1015	0	2	IC MUXR/DATA-SEL S 2-TO-1-LINE QUAD	01295	SN74S158N
U51-58	1818-1396	5	32	IC NMOS 16384-BIT RAM DYN 200-NS 3-S	50088	MK4116N-3
U59	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74
U60	1820-1191	3	2	IC FF TTL S D-TYPE POS-EDGE-TRIG COM	01295	SN74S175N
U61	1820-0697	2	1	IC DRVR TTL S NAND LINE DUAL 4-INP	01295	SN74S140N
U62-64	1820-1435	8	3	IC CNTR TTL LS BIN UP/DOWN SYNCHRO	01295	SN74LS669N
U65-72	1818-1396	5	32	IC NMOS 16384-BIT RAM DYN 200-NS 3-S	50088	MK4116N-3
U73	0960-0530	7	1	OSCILLATOR 25MHz	28480	0960-0530
U74	1816-1496	3	1	IC ROM 2KX8	28480	1816-1496
U75,76	1820-1432	5	2	IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS163AN
U77	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74
U78	1820-1130	0	1	IC GATE TTL S NAND 13-INP	01295	SN74S133N
U79-82	1820-1428	9	4	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS158N
U83	1820-1208	3		IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
U84	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U85	1820-2075	4	1	IC MISC TTL LS	01295	SN74LS245N
U86	1820-1451	8	1	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S38N
U87	1820-1191	3		IC FF TTL S D-TYPE POS-EDGE-TRIG COM	01295	SN74S175N

See introduction to this section for ordering information

Table 6-11. A5 Display Controller Replaceable Parts List (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U88	1820-0685	8	1	IC GATE TTL S NAND TPL 3-INP	01295	SN74S10N
U89,90	1820-1303	9	2	IC SHF-RGTR TTL S R-S PRL-IN PRL-OUT	01295	SN74S195N
U91	1820-0693	8		IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
XU1,2	1200-0607	0	32	SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0607
XU23-30	1200-0607	0		SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0607
XU33	1200-0654	7	1	SOCKET-IC 40-CONT DIP-SLDR	24840	1200-0654
XU34	1200-0607	0		SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0607
XU38-45	1200-0607	0		SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0607
XU51-58	1200-0607	0		SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0607
XU65-72	1200-0607	0		SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0607
XU74	1200-0541	1	1	SOCKET-IC 24 CONT DIP SLDR	28480	1200-0541

Table 6-12. A6 Secondary Drive Board Replaceable Parts List

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A6	64110-66506	2	1	BOARD ASSEMBLY-SECTION DRIVE	28480	64110-66506
A6C1	0180-2879	7	5	CAPACITOR-FXD 22UF+50-10% 25VDC AL	28480	0180-2879
A6C2	0180-2879	7		CAPACITOR-FXD 22UF+50-10% 25VDC AL	28480	0180-2879
A6C3	0160-2930	9	6	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2930
A6C4	0160-2930	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2930
A6C7	0180-2879	7		CAPACITOR-FXD 22UF+50-10% 25VDC AL	28480	0180-2879
A6C8	0160-2930	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2930
A6C9	0180-2879	7		CAPACITOR-FXD 22UF+50-10% 25VDC AL	28480	0180-2879
A6C10	0160-2930	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2930
A6C11	0180-0197	8	2	CAPACITOR-FXD 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
A6C12	**0140-0149**	6	1	CAPACITOR-FXD **470PF** +-5% 300VDC MICA	28480	**0140-0149**
A6C13	0160-2940	1	1	CAPACITOR-FXD 470PF +-5% 300VDC MICA	28480	0160-2940
A6C14	0160-2930	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2930
A6C15	0160-0157	8	1	CAPACITOR-FXD 4700PF +-10% 200VDC POLYE	28480	0160-0157
A6C16	0180-2879	7		CAPACITOR-FXD 22UF+50-10% 25VDC AL	28480	0180-2879
A6C17	0160-0168	1	1	CAPACITOR-FXD .1UF +-10% 200VDC POLYE	28480	0160-0168
A6C18	0180-0094	4	2	CAPACITOR-FXD 100UF+75-10% 25VDC AL	56289	30D107G025DD2
A6C19	0180-0291	3	1	CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
A6C20	0160-3508	9	1	CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A6C22	0180-2880	0	1	CAPACITOR-FXD 2200UF+50-10% 16VDC AL	28480	0180-2880
A6C23	0180-0094	4		CAPACITOR-FXD 100UF+75-10% 25VDC AL	56289	30D107G025DD2
A6C24	0160-0154	5	1	CAPACITOR-FXD 2200PF +-10% 200VDC POLYE	28480	0160-0154
A6C25	0160-4832	4	4	CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
A6C27	0160-2930	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2930
A6C28	0180-0197	8		CAPACITOR-FXD 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
A6C29	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
A6C30	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
A6C31	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
A6CR1	1901-0535	9	1	DIODE-SM SIG SCHOTTKY	28480	1901-0535
A6CR2	1901-0050	3	7	DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A6CR3	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A6CR4	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A6CR5	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A6CR6	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A6CR7	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A6CR8	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A6CR9	1901-0620	3	1	DIODE-SWITCHING 60V 400MA DO-35	9N171	NDP250
A6CR10	1901-0022	9	4	DIODE-STABISTOR 10V 250MA	28480	1901-0022
A6CR11	1901-0022	9		DIODE-STABISTOR 10V 250MA	28480	1901-0022
A6CR12	1901-0022	9		DIODE-STABISTOR 10V 250MA	28480	1901-0022
A6CR13	1901-0022	9		DIODE-STABISTOR 10V 250MA	28480	1901-0022
A6CR14	1901-0040	1	1	DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A6H13	2200-0103	2	3	SCREW-MACH 4-40 .25-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A6H50	2190-0005	0	3	WASHER-LK EXT T NO. 4 .116-IN-ID	28480	2190-0005
A6H52	2260-0001	5	3	NUT-HEX-DBL-CHAM 4-40-THD .094-IN-THK	28480	2260-0001
A6J2	1200-0607	0	1	SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A6L1	9100-2276	9	1	INDUCTOR RF-CH-MLD 100UH 10% .105DX.26LG	28480	9100-2276
A6L2	9140-0115	5	1	INDUCTOR RF-CH-MLD 22UH 10% .23DX.57LG	28480	9140-0115
A6L3	9140-0114	4	1	INDUCTOR RF-CH-MLD 10UH 10% .166DX.385LG	28480	9140-0114
A6LS1	9160-0244	3	1	SPEAKER- .1W	28480	9160-0244
A6MP1	01425-01207	2	3	CLIP-CABLE	28480	01425-01207
A6MP2	0360-0535	0	11	TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A6Q1	1854-0215	1	2	TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A6Q2	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A6Q3	1854-0467	5	1	TRANSISTOR NPN 2N4401 SI TO-92 PD=310MW	03508	2N4401
A6Q4	1853-0271	7	1	TRANSISTOR PNP 2N4403 SI TO-92 PD=310MW	04713	2N4403
A6Q5	1854-0798	5	1	TRANSISTOR NPN SI DARL PD=1W	04713	MPS-U45
A6Q6	1853-0449	1	1	TRANSISTOR PNP SI DARL PD=1W	04713	MPS-U95
A6Q7	1854-0246	8	2	TRANSISTOR NPN SI PD=350MW FT=250MHZ	04713	SPS 233
A6Q8	1854-0472	2	1	TRANSISTOR NPN SI DARL PD=500MW	04713	MPS-A14
A6Q9	1854-0246	8		TRANSISTOR NPN SI PD=350MW FT=250MHZ	04713	SPS 233
A6R1	0757-0460	1	1	RESISTOR 61.9K 1% .125W F TC=0+-100	24546	C4-1/8-T0-6192-F
A6R2	0757-0430	5	4	RESISTOR 2.21K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2211-F
A6R3	**2100-0558**	7	1	RESISTOR-TRMR 50K 10% C TOP-ADJ 1-TRN	28480	**2100-0558**
A6R4	0698-3450	9	3	RESISTOR 42.2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4222-F
A6R5	0683-8215	3	3	RESISTOR 820 5% .25W FC TC=-400/+600	01121	CB8215
A6R6	0683-8215	3		RESISTOR 820 5% .25W FC TC=-400/+600	01121	CB8215
A6R7	0683-8215	3		RESISTOR 820 5% .25W FC TC=-400/+600	01121	CB8215
A6R8	0683-1215	9	2	RESISTOR 120 5% .25W FC TC=-400/+600	01121	CB1215
A6R9	0757-0419	0	2	RESISTOR 681 1% .125W F TC=0+-100	24546	C4-1/8-T0-681R-F
A6R10	0764-0016	8	1	RESISTOR 1K 5% 2W MO TC=0+-200	28480	0764-0016

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-12. A6 Secondary Drive Board Replaceable Parts List (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A6R11	0757-0124	4	2	RESISTOR 39.2K 1% .125W F TC=0+-100	28480	0757-0124
A6R12	0757-0419	0		RESISTOR 681 1% .125W F TC=0+-100	24546	C4-1/8-T0-681R-F
A6R13	0683-1215	9		RESISTOR 120 5% .25W FC TC=-400/+600	01121	CB1215
A6R14	0757-0430	5		RESISTOR 2.21K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2211-F
A6R15	0757-0430	5		RESISTOR 2.21K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2211-F
A6R16	0757-0430	5		RESISTOR 2.21K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2211-F
A6R17	0683-1025	9	2	RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A6R18	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A6R19	0757-0465	6	2	RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
A6R20	2100-3213	9	1	RESISTOR-TRMR 200K 10% C TOP-ADJ 1-TRN	28480	2100-3213
A6R21	0757-0442	9	1	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A6R22	0757-0465	6		RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
A6R23	0757-0124	4		RESISTOR 39.2K 1% .125W F TC=0+-100	28480	0757-0124
A6R24	0757-0463	4	2	RESISTOR 82.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-8252-F
A6R25	0686-2215	7	1	RESISTOR 220 5% .5W CC TC=0+529	01121	EB2215
A6R26	0683-1015	7	1	RESISTOR 100 5% .25W FC TC=-400/+500	01121	CB1015
A6R27	0683-2235	5	1	RESISTOR 22K 5% .25W FC TC=-400/+800	01121	CB2235
A6R28	0757-0470	3	1	RESISTOR 162K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1623-F
A6R29	0757-0463	4		RESISTOR 82.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-8252-F
A6R30	0698-3450	9		RESISTOR 42.2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4222-F
A6R31	0698-3450	9		RESISTOR 42.2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4222-F
A6R32	0683-2215	1	1	RESISTOR 220 5% .25W FC TC=-400/+600	01121	CB2215
A6R33	0686-0335	8	1	RESISTOR 3.3 5% .5W CC TC=0+412	01121	EB33G5
A6R34	0757-0473	6	1	RESISTOR 221K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2213-F
A6R35	0698-3443	0	1	RESISTOR 287 1% .125W F TC=0+-100	24546	C4-1/8-T0-287R-F
A6R36	0698-3428	1	1	RESISTOR 14.7 1% .125W F TC=0+-100	03888	PME55-1/8-T0-14R7-F
A6R37	0757-0458	7	1	RESISTOR 51.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5112-F
A6R38	0686-1005	1	1	RESISTOR 10 5% .5W CC TC=0+412	01121	EB1005
A6R39	0698-3157	3	2	RESISTOR 19.6K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1962-F
A6R40	0698-3157	3		RESISTOR 19.6K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1962-F
A6R41	0698-3447	4	1	RESISTOR 422 1% .125W F TC=0+-100	24546	C4-1/8-T0-422R-F
A6R42	0757-0443	0	1	RESISTOR 11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1102-F
A6U1	1820-1451	8	1	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S38N
A6U2	1820-0471	0	1	IC INV TTL HEX 1-INP	01295	SN7406N
A6U3	1826-0939	7	1	IC OP AMP GP QUAD 14-DIP-P PKG	27014	LM2900N
A6U4	1820-1437	0	1	IC MV TTL LS MONOSTBL DUAL	01295	SN74LS221N
A6U5	1820-1204	9	1	IC GATE TTL LS NAND DUAL 4-INP	01295	SN74LS20N
A6U6	1820-1422	3	1	IC MV TTL LS MONOSTBL RETRIG	01295	SN74LS122N
A6U7	1826-0180	0	1	IC TIMER TTL MONO/ASTBL	01295	NE555P
A6VR1	1902-0644	3	1	DIODE-ZNR 1N5363B 30V 5% PD=5W TC=+29MV	28480	1902-0644
A6VR2	1902-0041	4	1	DIODE-ZNR 5.11V 5% DO-35 PD=.4W	28480	1902-0041
A6W1	64110-61609	6	1	CABLE ASSEMBLY-MOTHER	28480	64110-61609

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-13. A7 Transformer Flyback Board Replaceable Parts List

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A7	64110-66505	1	1	TRANSFORMER-FLYBACK	28480	64110-66505
A7C1	0160-4740	3	1	CAPACITOR-FXD .015F +-5% 400VDC POLYP	28480	0160-4740
A7C2	0180-2881	1	2	CAPACITOR-FXD 10UF+50-10% 50VDC AL	28480	0180-2881
A7C3	0180-2881	1		CAPACITOR-FXD 10UF+50-10% 50VDC AL	28480	0180-2881
A7C4	0160-2902	5	1	CAPACITOR-FXD .01UF +-20% 1KVDC CER	28480	0160-2902
A7C5	0160-4230	6	3	CAPACITOR-FXD .01UF +80-20% 1KVDC CER	71590	GAP-103
A7C6	0160-4230	6		CAPACITOR-FXD .01UF +80-20% 1KVDC CER	71590	GAP-103
A7C7	0160-4230	6		CAPACITOR-FXD .01UF +80-20% 1KVDC CER	71590	GAP-103
A7C8	0180-2913	0	1	CAPACITOR-FXD 470UF+50-10% 50VDC AL	28480	0180-2913
A7C9	0160-3355	4	1	CAPACITOR-FXD 1UF +-5% 200VDC MET-POLYC	28480	0160-3355
A7C10	0180-2880	0	1	CAPACITOR-FXD 2200UF+50-10% 16VDC AL	28480	0180-2880
A7CR1	1901-0050	3	1	DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A7CR2	1901-0719	1	2	DIODE-PWR RECT 400V 3A 300NS	04713	MR854
A7CR3	1901-0719	1		DIODE-PWR RECT 400V 3A 300NS	04713	MR854
A7CR4	1901-0845	4	2	DIODE-HV RECT 2KV 50MA 250NS	1B546	VG-2X
A7CR5	1901-0845	4		DIODE-HV RECT 2KV 50MA 250NS	1B546	VG-2X
A7DS1	2140-0013	5	2	LAMP-GLOW 5AB-A 70/57VDC 300UA T-2-BULB	08806	5AB-A(NE-23A)
A7DS2	2140-0013	5		LAMP-GLOW 5AB-A 70/57VDC 300UA T-2-BULB	08806	5AB-A(NE-23A)
A7H23	2360-0117	6	2	SCREW-MACH 6-32 .375-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A7H80	1400-0249	0	1	CABLE TIE .062-.625-DIA .091-WD NYL	06383	PLT1M-8
A7H88	0380-0334	9	2	STANDOFF-RVT-ON .375-IN-LG 4-40THD	00000	ORDER BY DESCRIPTION
A7H89	0380-0342	9	2	STANDOFF-RVT-ON .125-IN-LG 6-32THD	00000	ORDER BY DESCRIPTION
A7J1	1251-3475	3	1	CONNECTOR 10-PIN M POST TYPE	28480	1251-3475
A7J2	1251-5502	1	1	CONNECTOR 4-PIN M UTILITY	28480	1251-5502
A7L1	9140-0179	1	1	INDUCTOR RF-CH-MLD 22UH 10% .166DX.385LG	28480	9140-0179
A7L2	9140-0319	1	1	INDUCTOR-FIXED LINEARITY; DEFL CURRENT	28480	9140-0319
A7L3	9140-0481	8	1	COIL-VAR 20UH-80UH PC-MTG	28480	9140-0481
A7MP1	1205-0267	8	1	HEAT SINK SGL TO-3-CS	28480	1205-0267
A7MP2	1400-1138	8	1	CLIP-CMPNT .37-DIA NYL	28480	1400-1138
A7Q1	1854-0467	5	1	TRANSISTOR NPN 2N4401 SI TO-92 PD=310MW	03508	2N4401
A7Q2	1854-0623	5	1	TRANSISTOR NPN 2N6306 SI TO-3 PD=125W	04713	2N6306
A7R1	0683-2215	1	1	RESISTOR 220 5% .25W FC TC=-400/+600	01121	CB2215
A7R2	0683-1015	7	3	RESISTOR 100 5% .25W FC TC=-400/+500	01121	CB1015
A7R3	0683-1045	3	2	RESISTOR 100K 5% .25W FC TC=-400/+800	01121	CB1045
A7R4	0683-2225	3	1	RESISTOR 2.2K 5% .25W FC TC=-400/+700	01121	CB2225
A7R5	0683-1045	3		RESISTOR 100K 5% .25W FC TC=-400/+800	01121	CB1045
A7R6	0683-1025	9	1	RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A7R7	0683-4745	6	4	RESISTOR 470K 5% .25W FC TC=-800/+900	01121	CB4745
A7R8	0683-4745	6		RESISTOR 470K 5% .25W FC TC=-800/+900	01121	CB4745
A7R9	0683-1055	5	2	RESISTOR 1M 5% .25W FC TC=-800/+900	01121	CB1055
A7R10	0683-4745	6		RESISTOR 470K 5% .25W FC TC=-800/+900	01121	CB4745
A7R11	0683-4745	6		RESISTOR 470K 5% .25W FC TC=-800/+900	01121	CB4745
A7R12	2100-3892	0	2	RESISTOR-TRMR 2.5M 10% C TOP-ADJ 1-TRN	28480	2100-3892
A7R13	2100-3892	0		RESISTOR-TRMR 2.5M 10% C TOP-ADJ 1-TRN	28480	2100-3892
A7R14	0683-1015	7		RESISTOR 100 5% .25W FC TC=-400/+500	01121	CB1015
A7R15	0764-0016	8	1	RESISTOR 1K 5% 2W MO TC=0+-200	28480	0764-0016
A7R16	0683-1055	5		RESISTOR 1M 5% .25W FC TC=-800/+900	01121	CB1055
A7R17	0683-1015	7		RESISTOR 100 5% .25W FC TC=-400/+500	01121	CB1015
A7T1	9100-4195	5	1	TRANSFORMER-HORIZONTAL	28480	9100-4195
A7T2	9100-4182	0	1	TRANSFORMER-FLYBACK NORMAL DRIVE 24500HZ	28480	9100-4182
A7TP1	0360-0535	0	5	TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A7TP2	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A7TP3	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A7TP4	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A7TP5	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A7VR1	1902-3245	6	1	DIODE-ZNR 21.5V 5% DO-35 PD=.4W	28480	1902-3245
A7W1	64110-61610	9	1	CABLE ASSEMBLY-DISPLAY DRIVE	28480	64110-61610

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-14. A8 Rear Board Replaceable Parts List

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A8	64110-66508	4	1	BOARD ASSEMBLY-REAR	28480	64110-66508
A8BN1	1250-1032	2	4	CONN RF BNC-BHD MTG	28480	1250-1032
A8BN2	1250-1032	2		CONN RF BNC-BHD MTG	28480	1250-1032
A8BN3	1250-1032	2		CONN RF BNC-BHD MTG	28480	1250-1032
A8BN4	1250-1032	2		CONN RF BNC-BHD MTG	28480	1250-1032
A8H81	0380-0332	7	1	STANDOFF-RVT-ON .187-IN-LG 4-40THD	00000	ORDER BY DESCRIPTION
A8H83	2190-0068	5	4	WASHER-LK INTL T 1/2 IN .505-IN-ID	28480	2190-0068
A8H84	2950-0054	1	4	NUT-HEX-DBL-CHAM 1/2-28-THD .125-IN-THK	00000	ORDER BY DESCRIPTION
A8H85	1251-0218	6	4	LOCK-SUBMIN D CONN	28480	1251-0218
A8J1	1251-7100	9	1	CONNECTOR 26-PIN M POST TYPE	28480	1251-7100
A8J2	1251-4946	5	2	CONNECTOR 25-PIN F D SUBMIN	28480	1251-4946
A8J3	1251-4946	5		CONNECTOR 25-PIN F D SUBMIN	28480	1251-4946
A8S1	3101-1974	8	1	SWITCH-RKR DIP-RKR-ASSY 7-1A .05A 30VDC	28480	3101-1974

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-15. List of Manufacturers' Codes

Mfr No.	Manufacturer Name	Address		Zip Code
C0633	RIFA	BROMMA	SE	
S0545	NIPPON ELECTRIC CO	TOKYO	JP	
00000	ANY SATISFACTORY SUPPLIER			
01121	ALLEN-BRADLEY CO	MILWAUKEE	WI	53204
01281	TRW INC SEMICONDUCTOR DIV	LAWNDALE	CA	90260
01295	TEXAS INSTR INC SEMICOND CMPNT DIV	DALLAS	TX	75222
02111	SPECTROL ELECTRONICS CORP	CITY OF IND	CA	91745
03508	GE CO SEMICONDUCTOR PROD DEPT	AUBURN	NY	13201
03888	K D I PYROFILM CORP	WHIPPANY	NJ	07981
04713	MOTOROLA SEMICONDUCTOR PRODUCTS	PHOENIX	AZ	85008
06383	PANDUIT CORP	TINLEY PARK	IL	60477
06915	RICHCO PLASTIC CO	CHICAGO	IL	60646
07263	FAIRCHILD SEMICONDUCTOR DIV	MOUNTAIN VIEW	CA	94042
07416	NELSON NAME PLATE CO	LOS ANGELES	CA	90039
08806	GE CO MINIATURE LAMP PROD DEPT	CLEVELAND	OH	44112
1B546	VARO SEMICONDUCTOR INC	GARLAND	TX	75040
13103	THERMALLOY CO	DALLAS	TX	75234
15454	AMETEK/RODAN DIV	ANAHEIM	CA	92806
16299	CORNING GLASS WKS COMPONENT DIV	RALEIGH	NC	27604
18324	SIGNETICS CORP	SUNNYVALE	CA	94086
19701	MEPCO/ELECTRA CORP	MINERAL WELLS	TX	76067
24546	CORNING GLASS WORKS (BRADFORD)	BRADFORD	PA	16701
27014	NATIONAL SEMICONDUCTOR CORP	SANTA CLARA	CA	95051
27167	CORNING GLASS WORKS (WILMINGTON)	WILMINGTON	NC	28401
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO	CA	94304
3L585	RCA CORP SOLID STATE DIV	SOMERVILLE	NJ	
30983	MEPCO/ELECTRA CORP	SAN DIEGO	CA	92121
32293	INTERSIL INC	CUPERTINO	CA	95014
34344	MOTOROLA INC	FRANKLIN PARK	IL	60131
34649	INTEL CORP	MOUNTAIN VIEW	CA	95051
51506	ACCURATE SCREW MACHINE CO	MONTVALE	NJ	07645
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS	MA	01247
71590	CENTRALAB ELEK DIV GLOBE-UNION INC	MILWAUKEE	WI	50501
71744	CHICAGO MINIATURE LAMP WORKS	CHICAGO	IL	60640
72136	ELECTRO MOTIVE CORP	FLORENCE	SC	06226
75042	TRW INC PHILADELPHIA DIV	PHILADELPHIA	PA	19108
75915	LITTELFUSE INC	DES PLAINES	IL	60016
83259	PARKER SEAL CO DIV PARKER-HANNIFIN	LEXINGTON	KY	90231
9N171	UNITRODE COMPUTER PRODUCTS CORP	METHUEN	MA	

See introduction to this section for ordering information

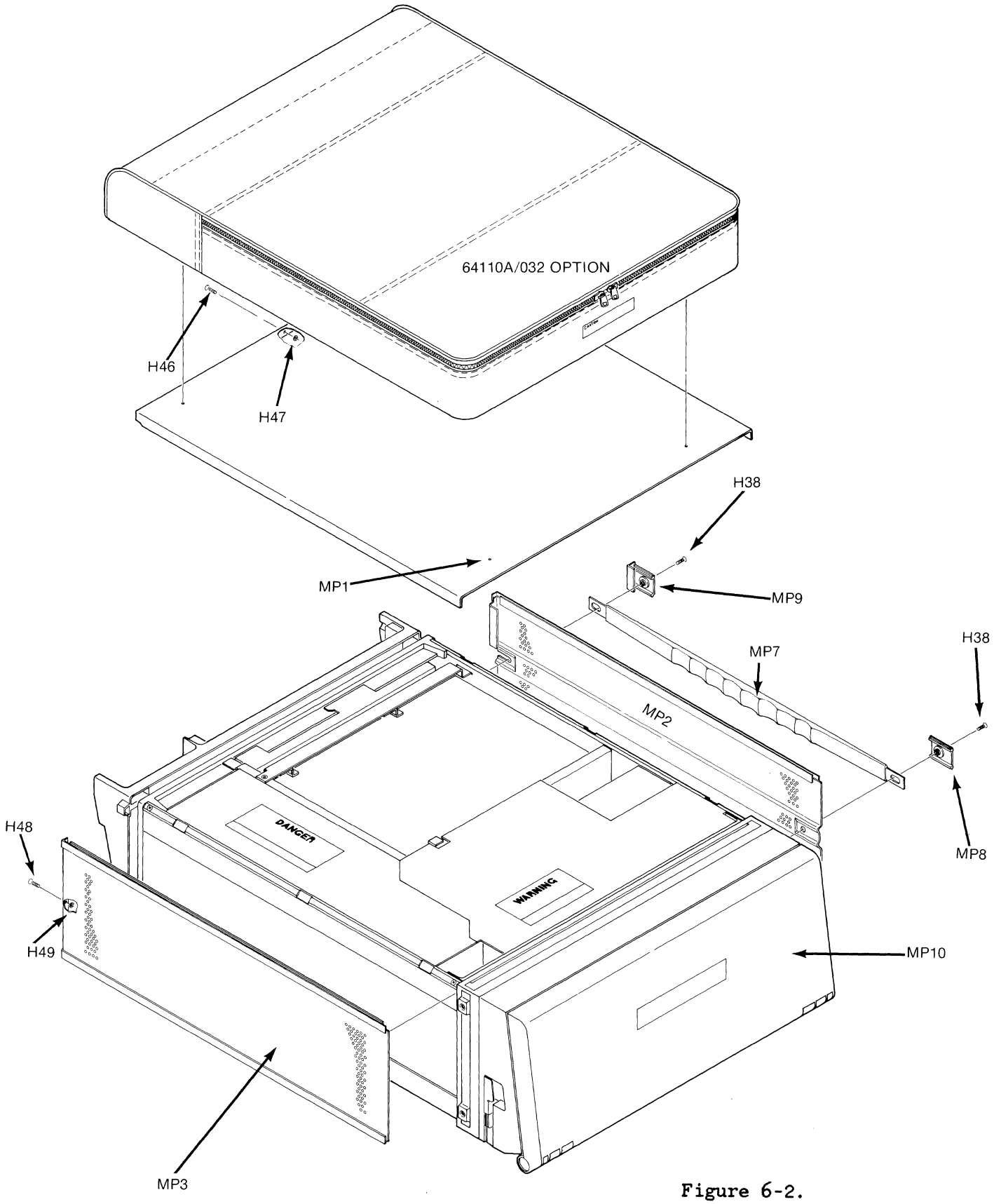


Figure 6-2.
Top Cover Parts Locator

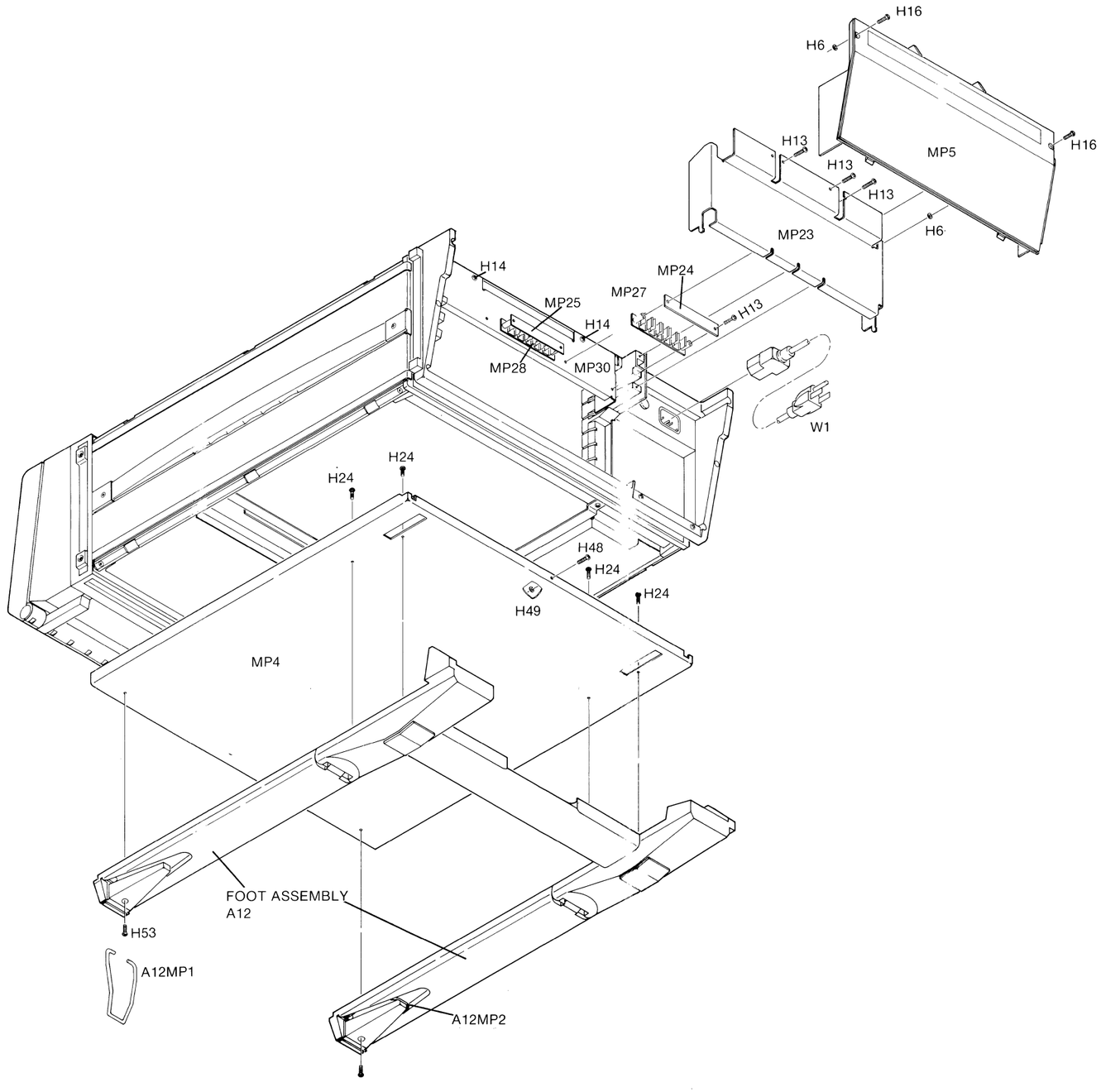
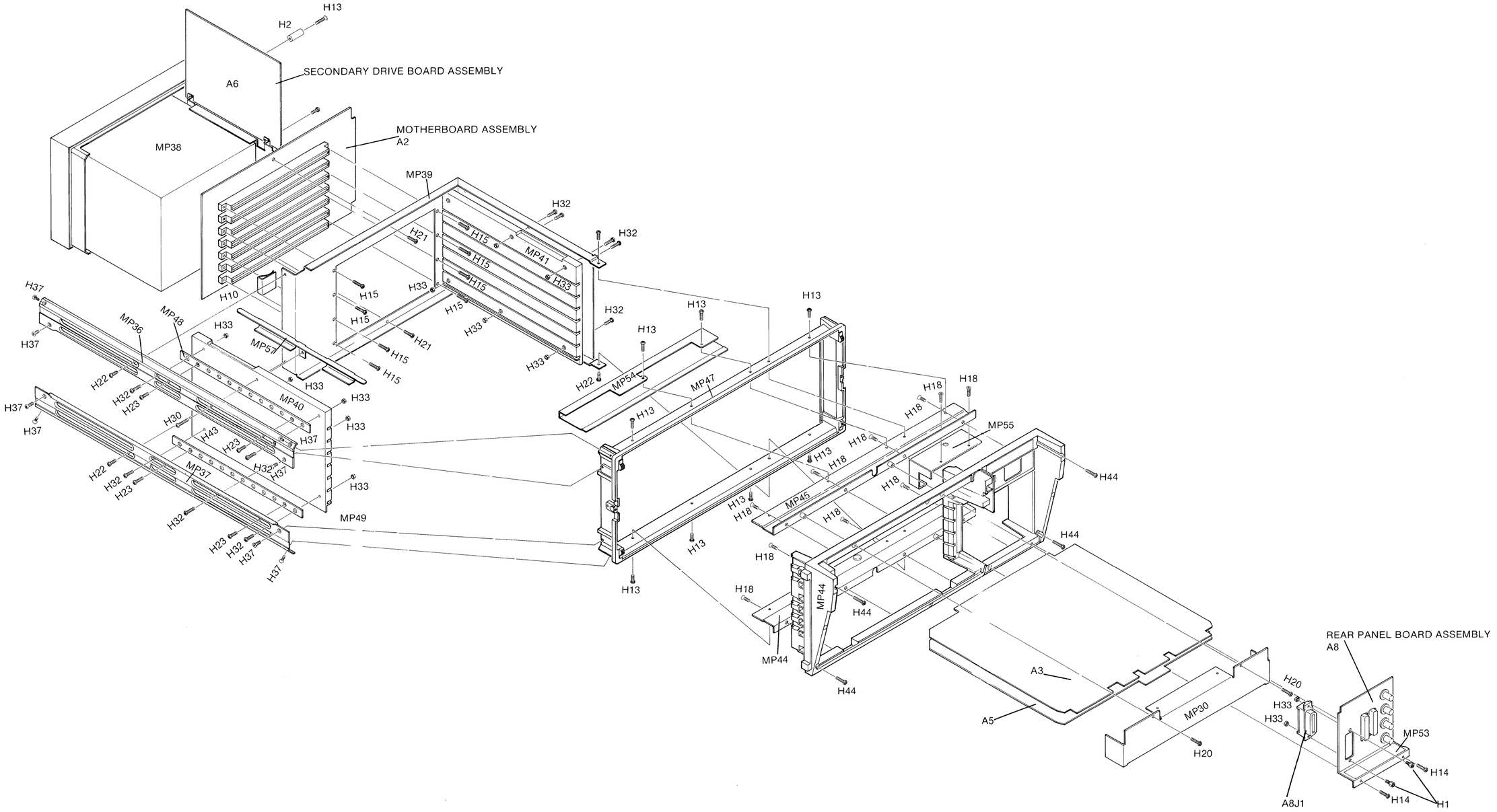


Figure 6-3.
Bottom Cover Parts Locator



0380-1482

Figure 6-4.
Cardcage Parts Locator
6-37/(6-38 blank)

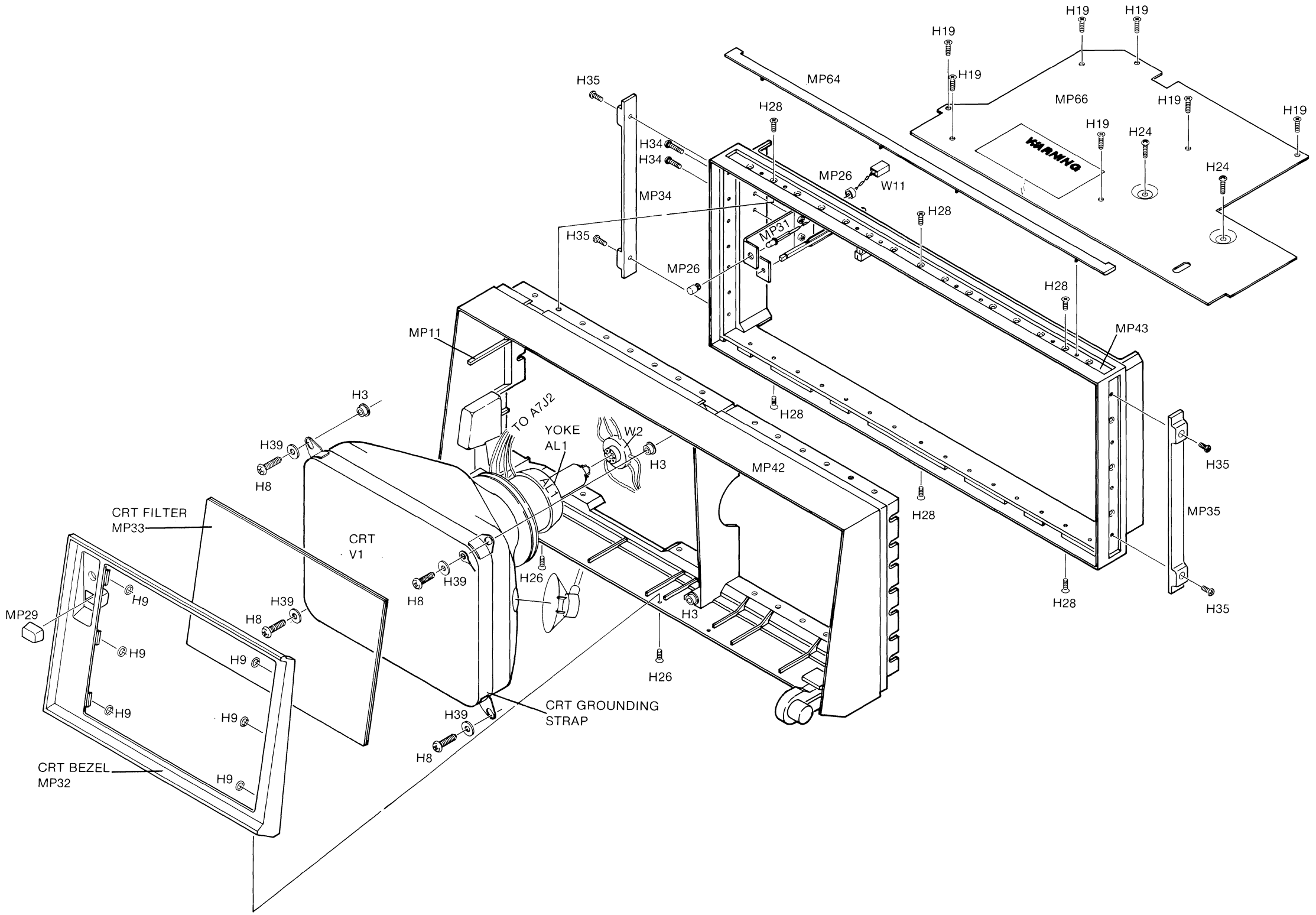


Figure 6-5.
CRT Parts Locator

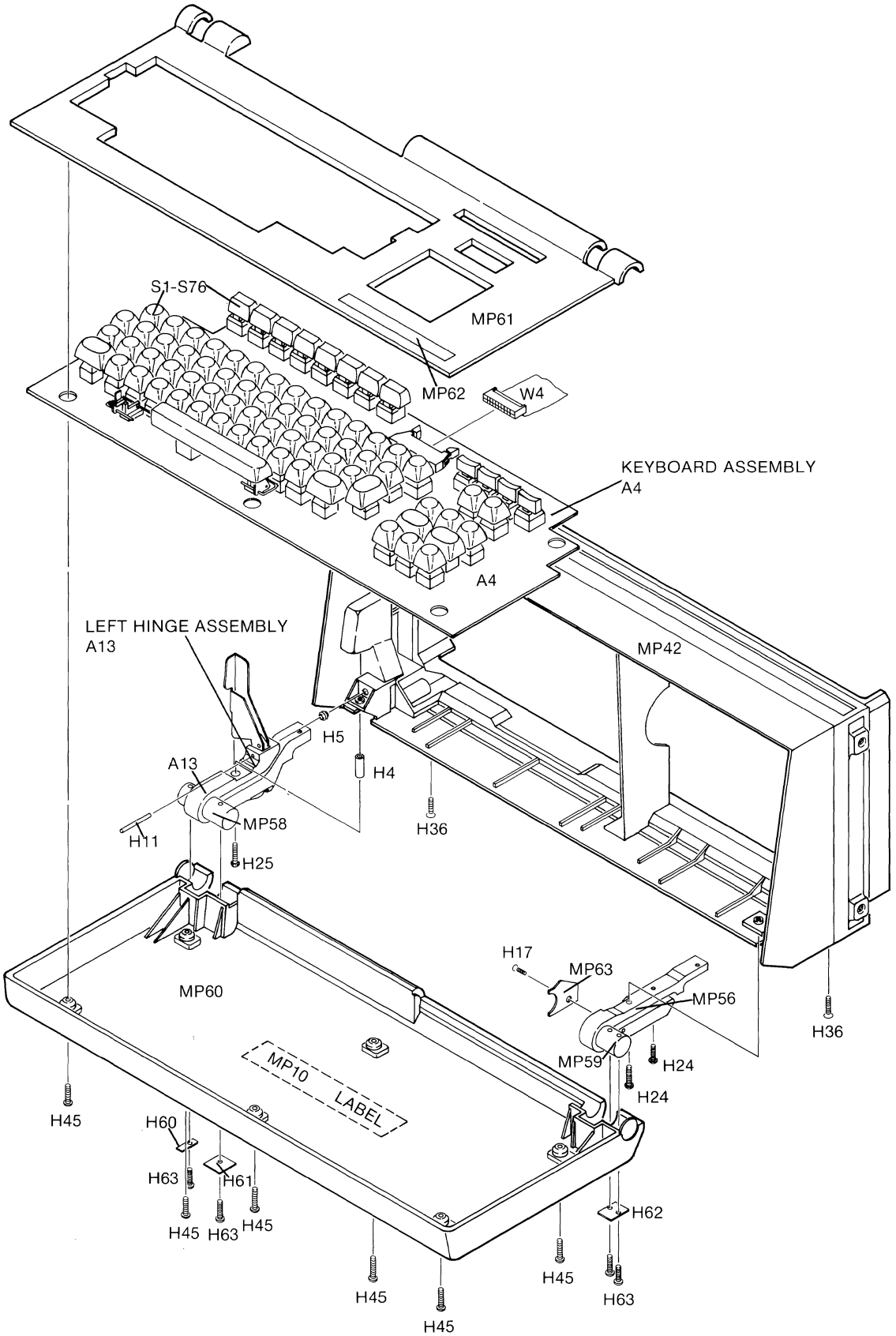


Figure 6-6.
Keyboard Parts Locator
6-41/(6-42 blank)

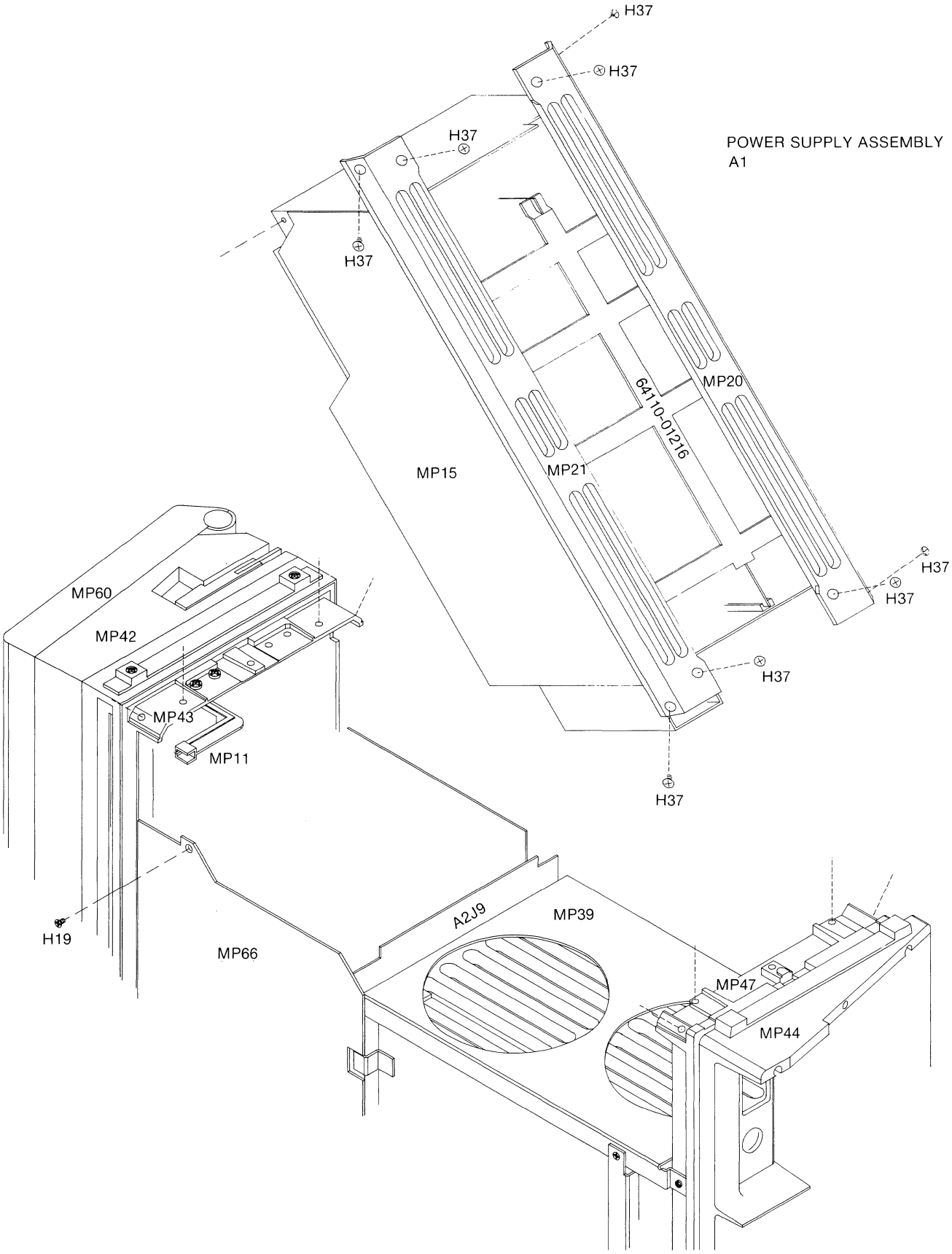


Figure 6-7.
Power Supply Parts Locator
6-43/(6-44 blank)

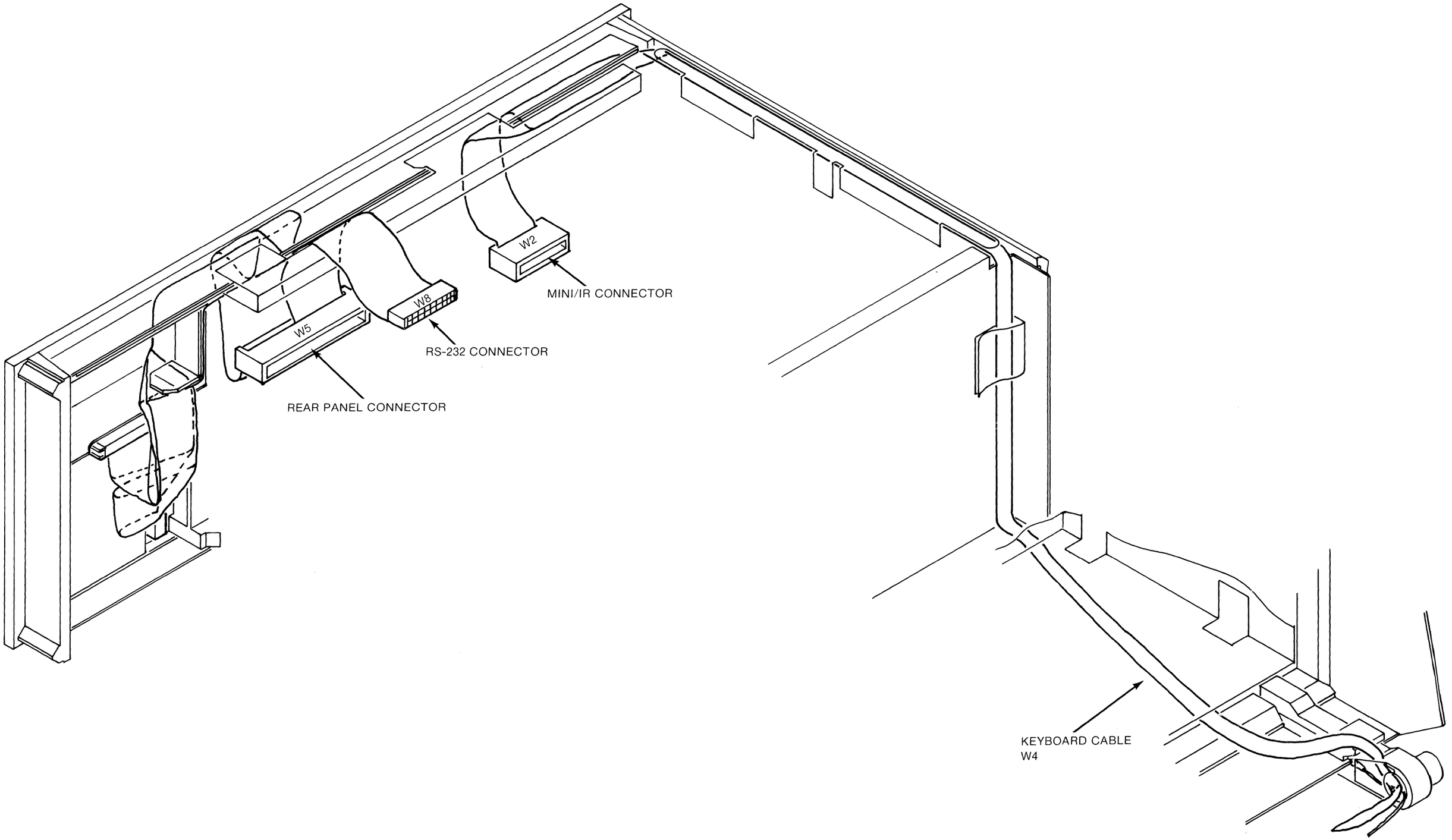
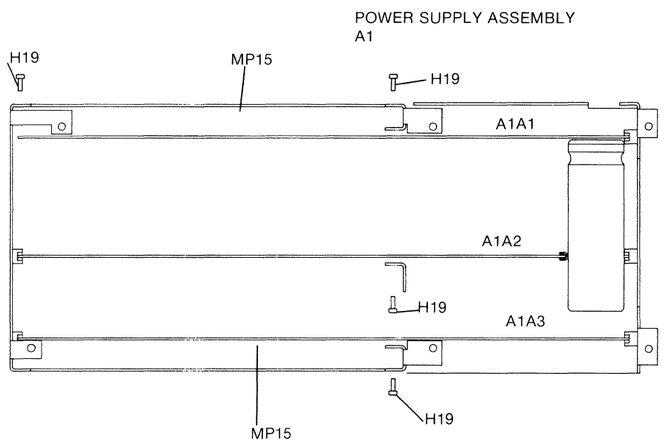


Figure 6-8.
Mainframe Cables Parts Locator



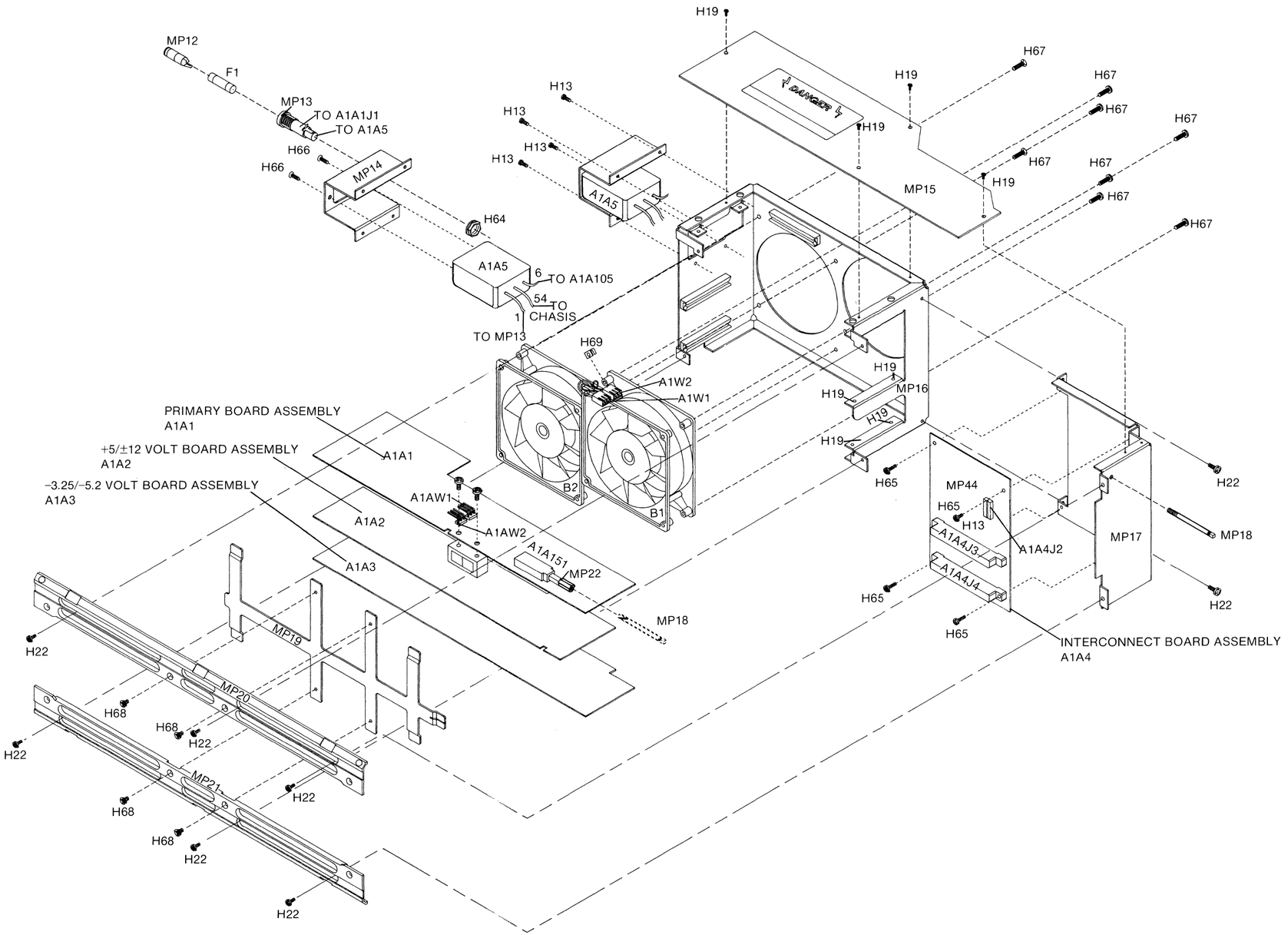


Figure 6-9.
Power Supply Subassemblies Parts Locator

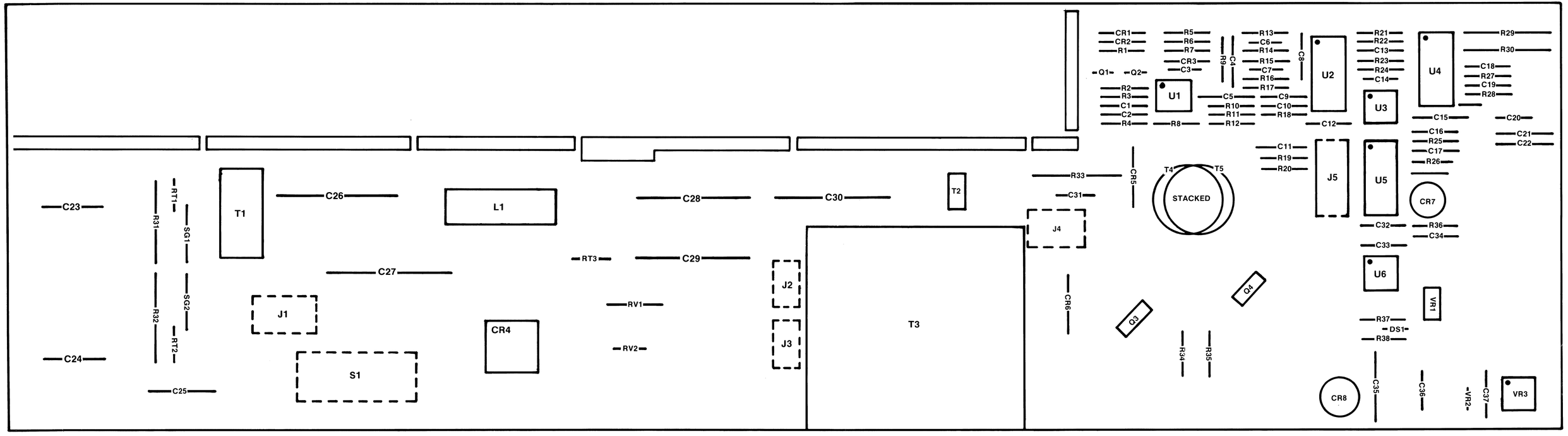


Figure 6-10.
Primary Board A1A1 Component Locator
6-49/(6-50 blank)

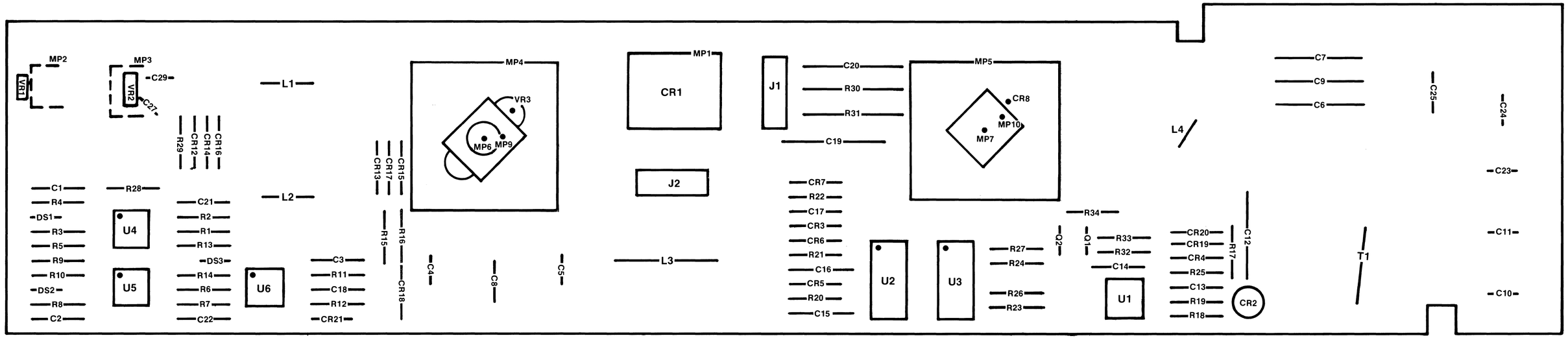


Figure 6-11.
+5, -12 Volt Board A1A2 Component Locator
6-51/(6-52 blank)

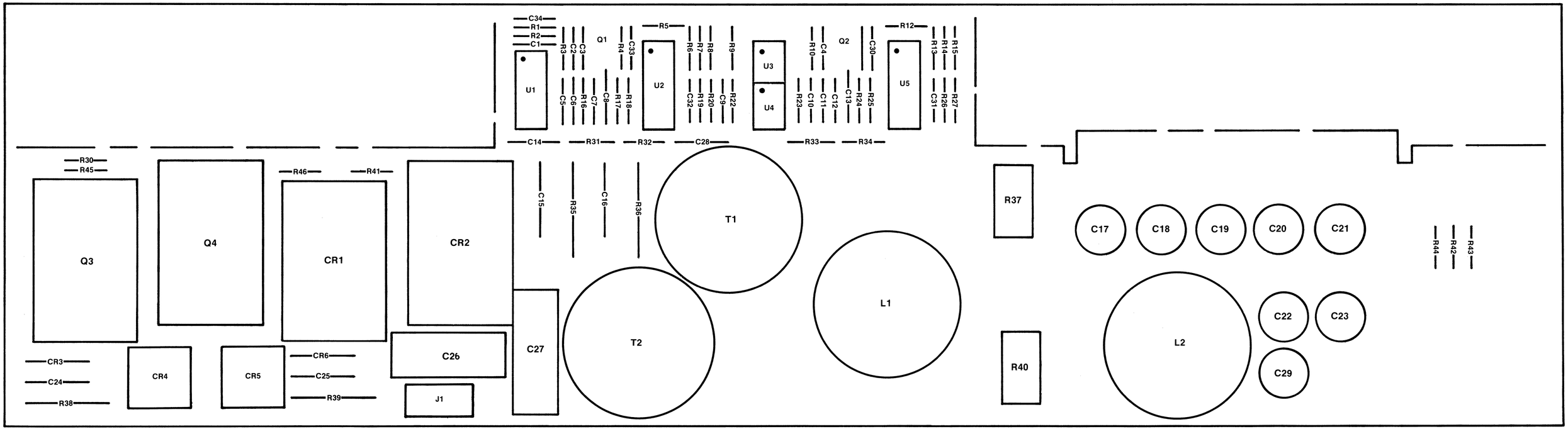


Figure 6-12.
-3.25, -5.2 Volt Board A1A3 Component Locator
6-53/(6-54 blank)

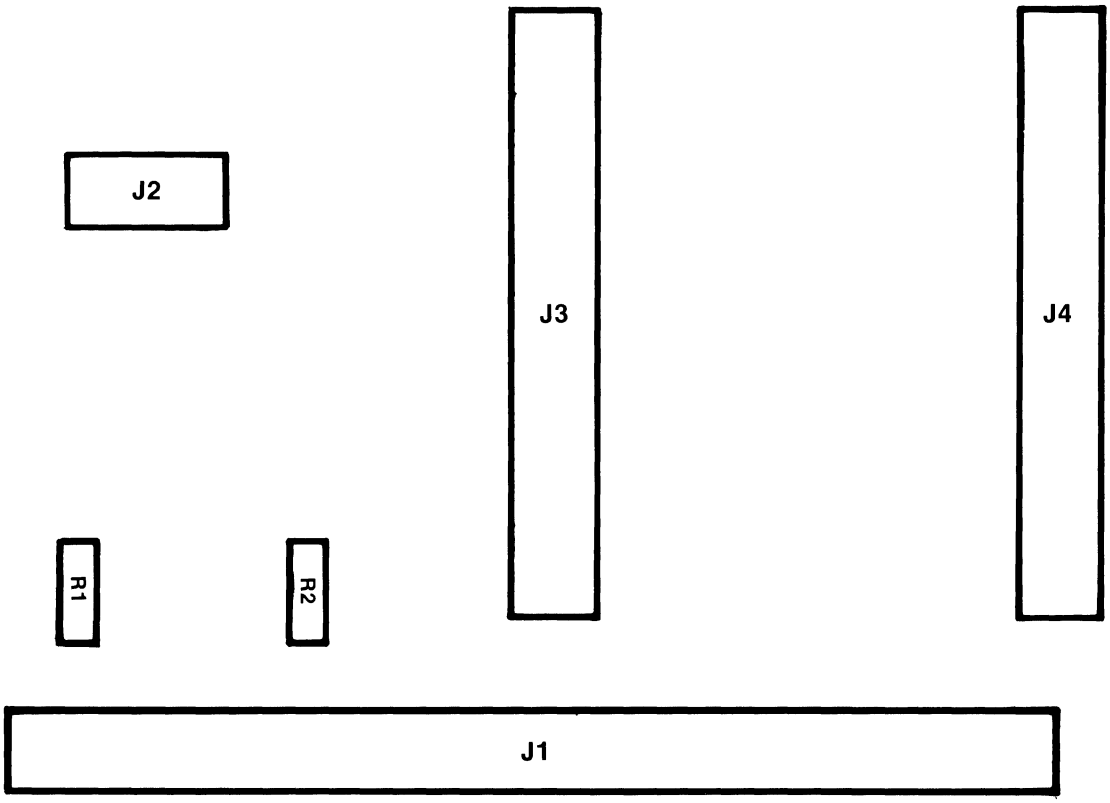


Figure 6-13.
Interconnect Board A1A4 Component Locator

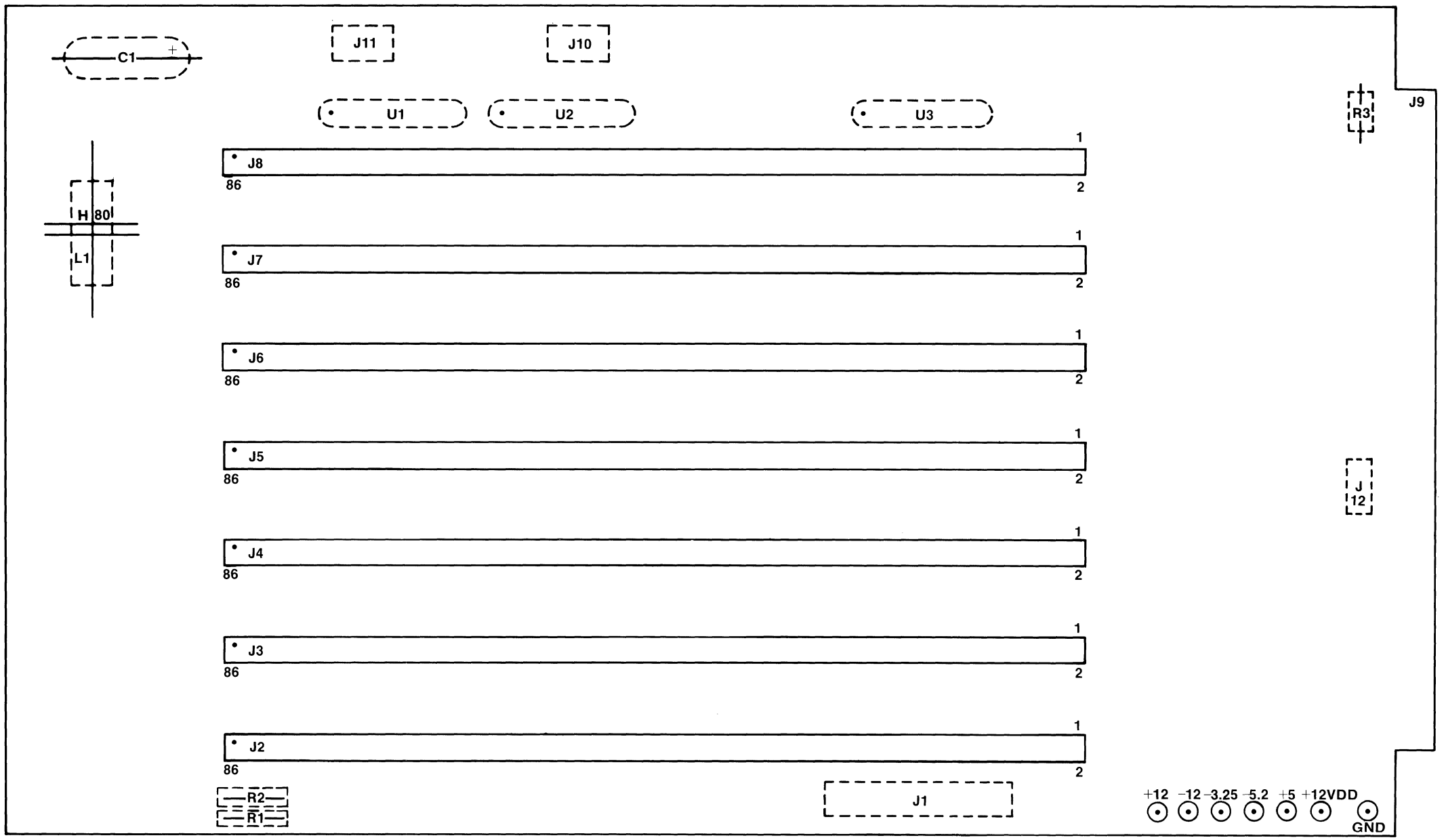


Figure 6-14.
Motherboard A2 Component Locator
6-57/(6-58 blank)

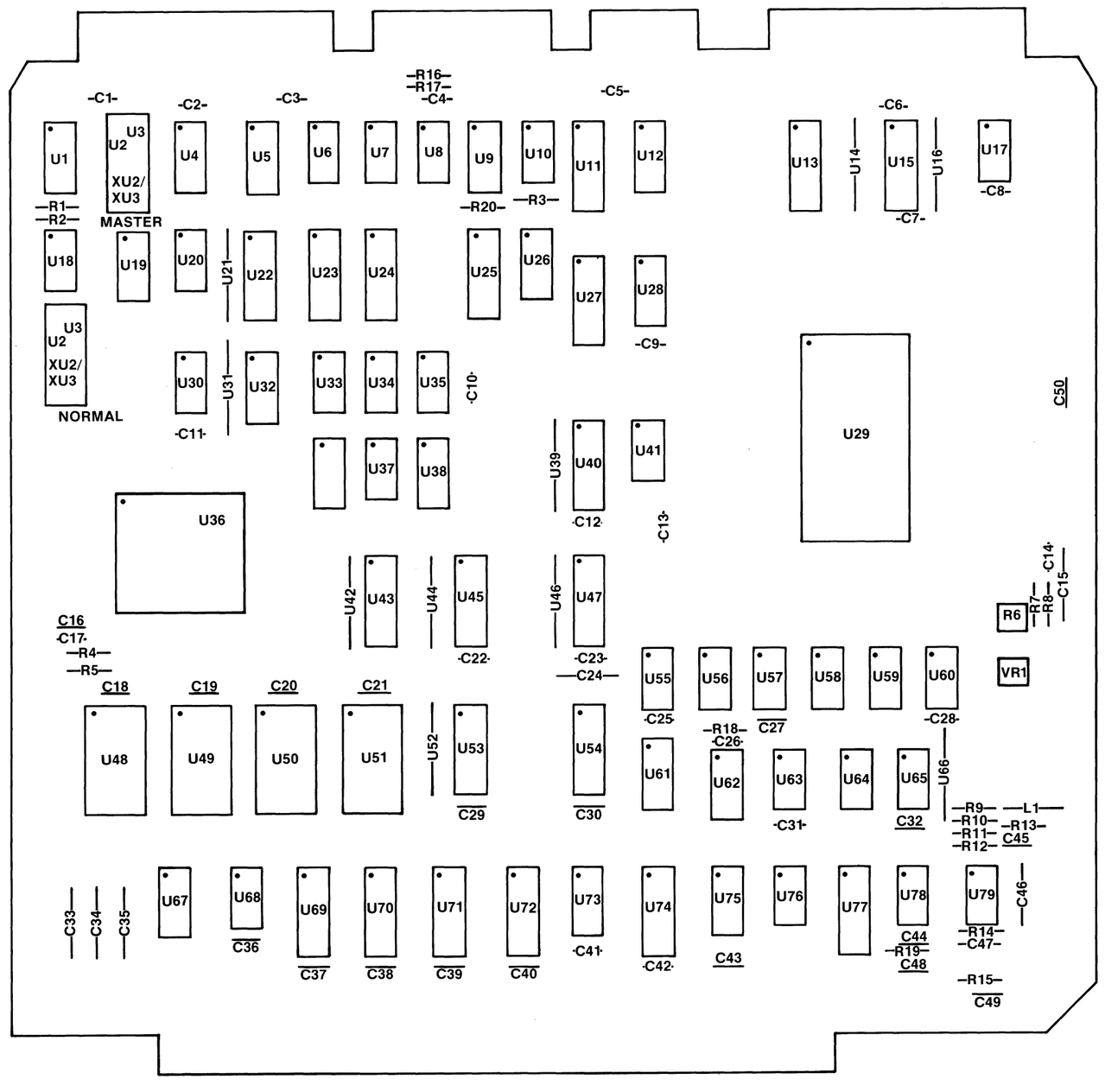


Figure 6-15.
CPU/IO Board A3 Component Locator

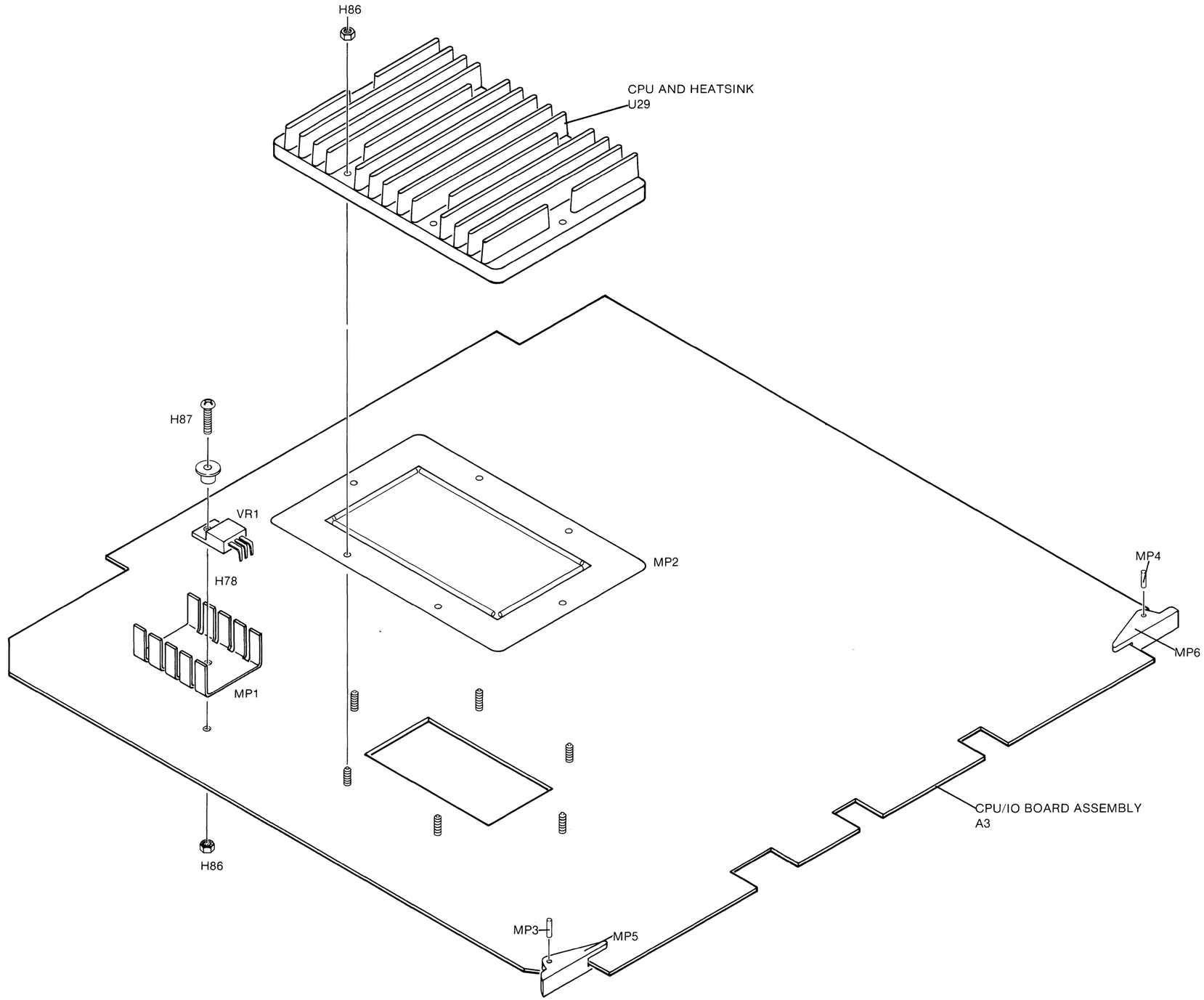


Figure 6-16.
CPU/IO Mechanical Parts Locator

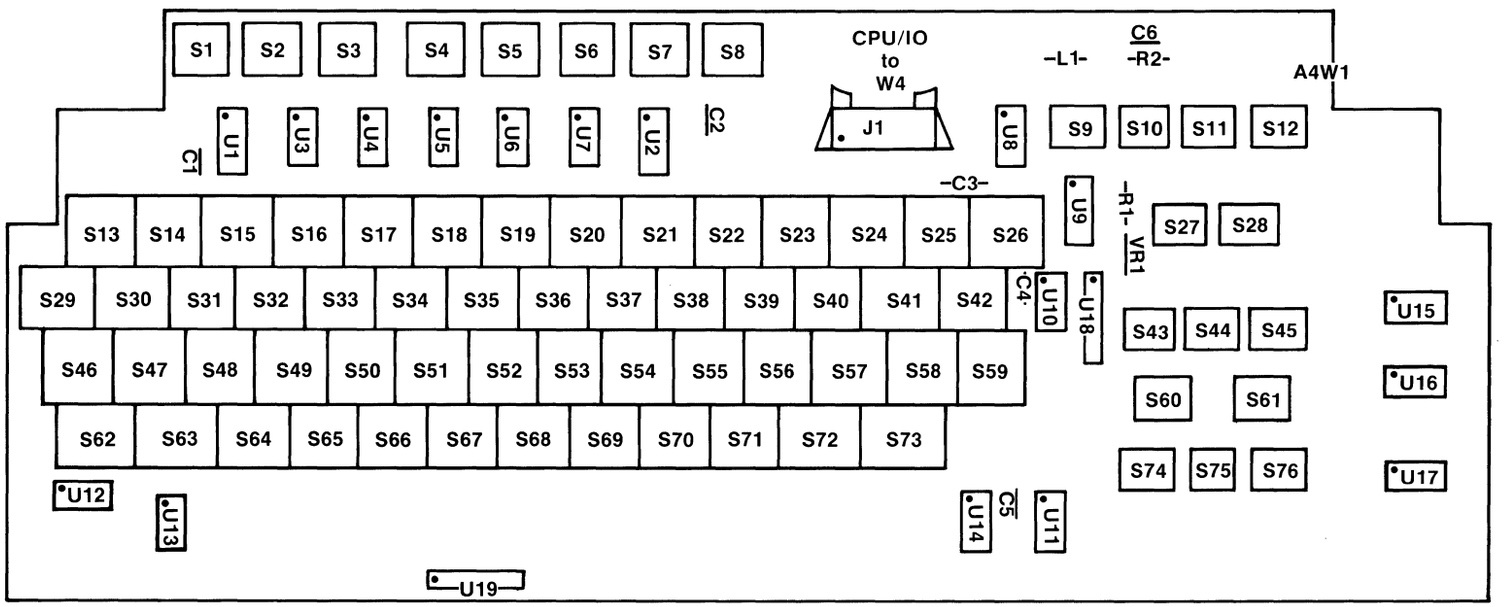


Figure 6-17.
Keyboard Board A4 Component Locator

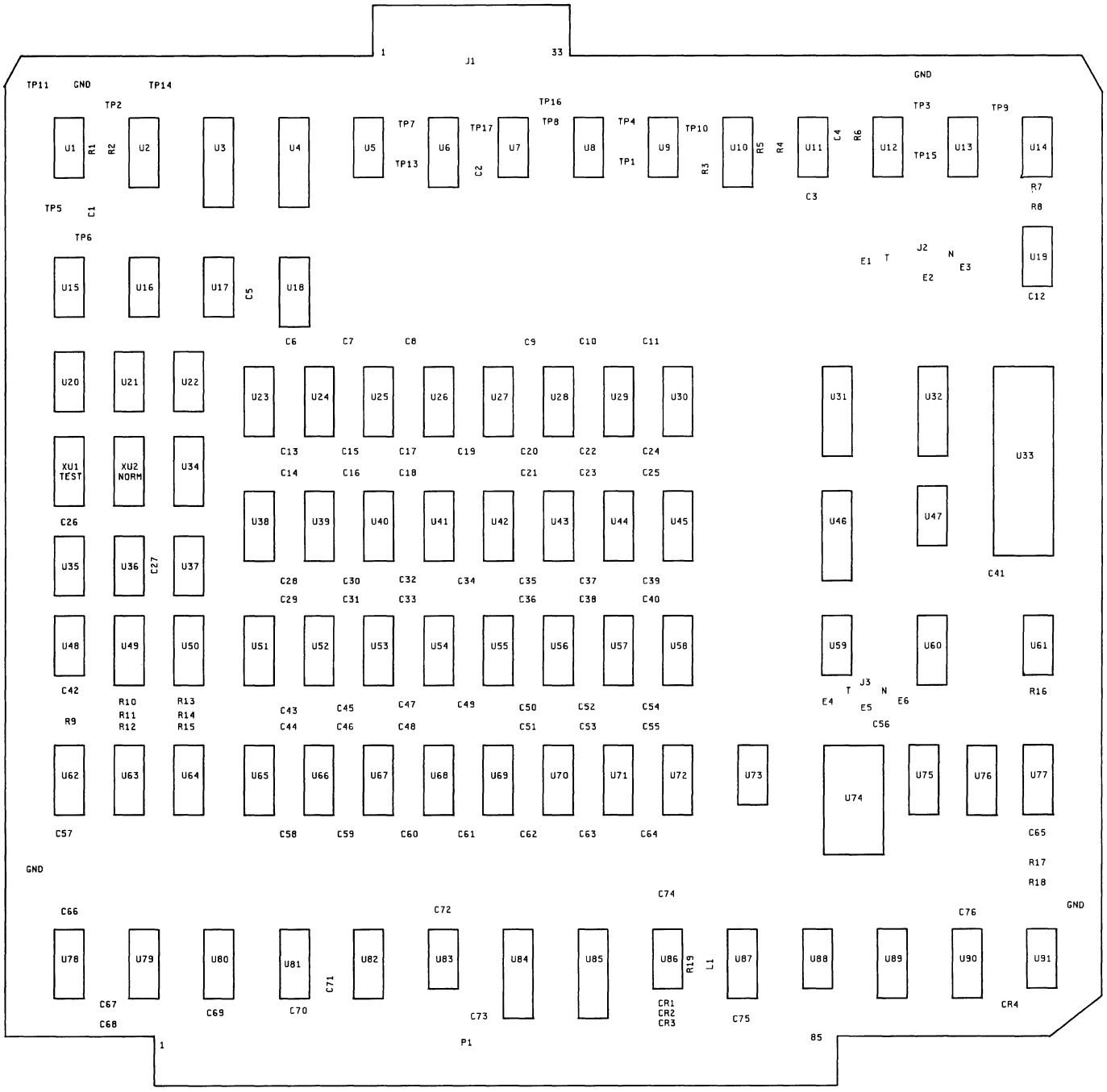


Figure 6-18. Display Controller Component Locator

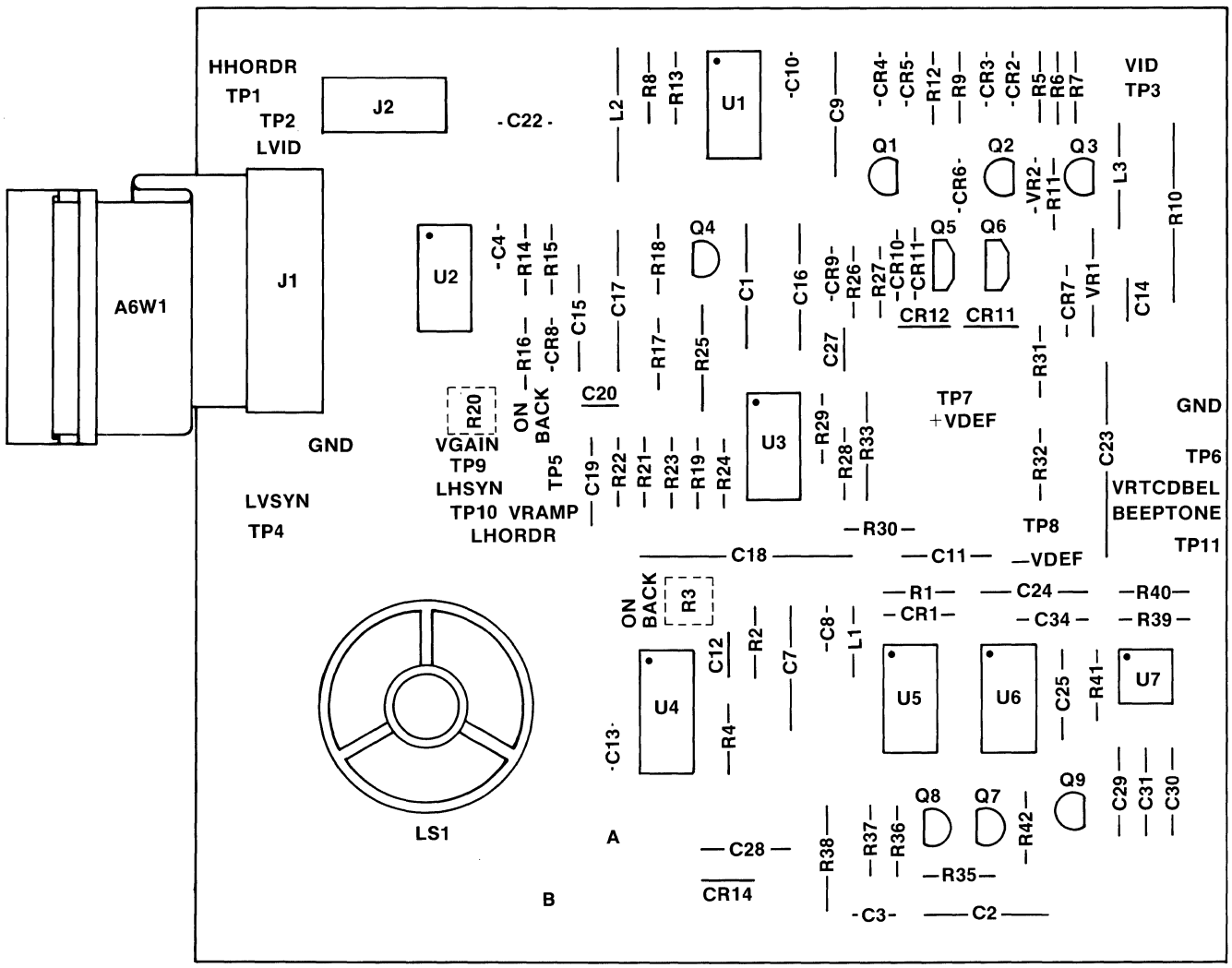


Figure 6-19. Secondary Drive Board A6 Component Locator

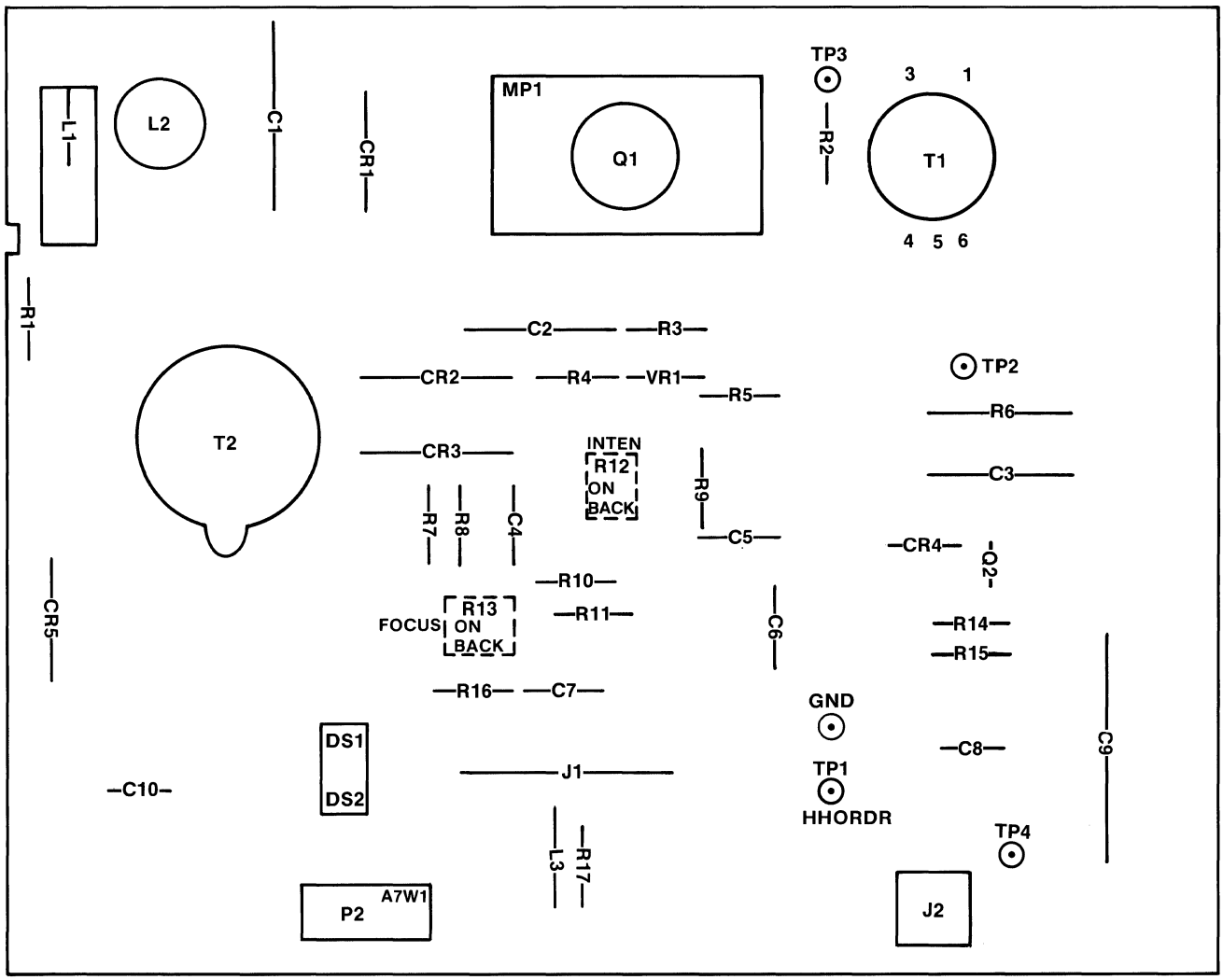


Figure 6-20. Flyback Board A7 Component Locator

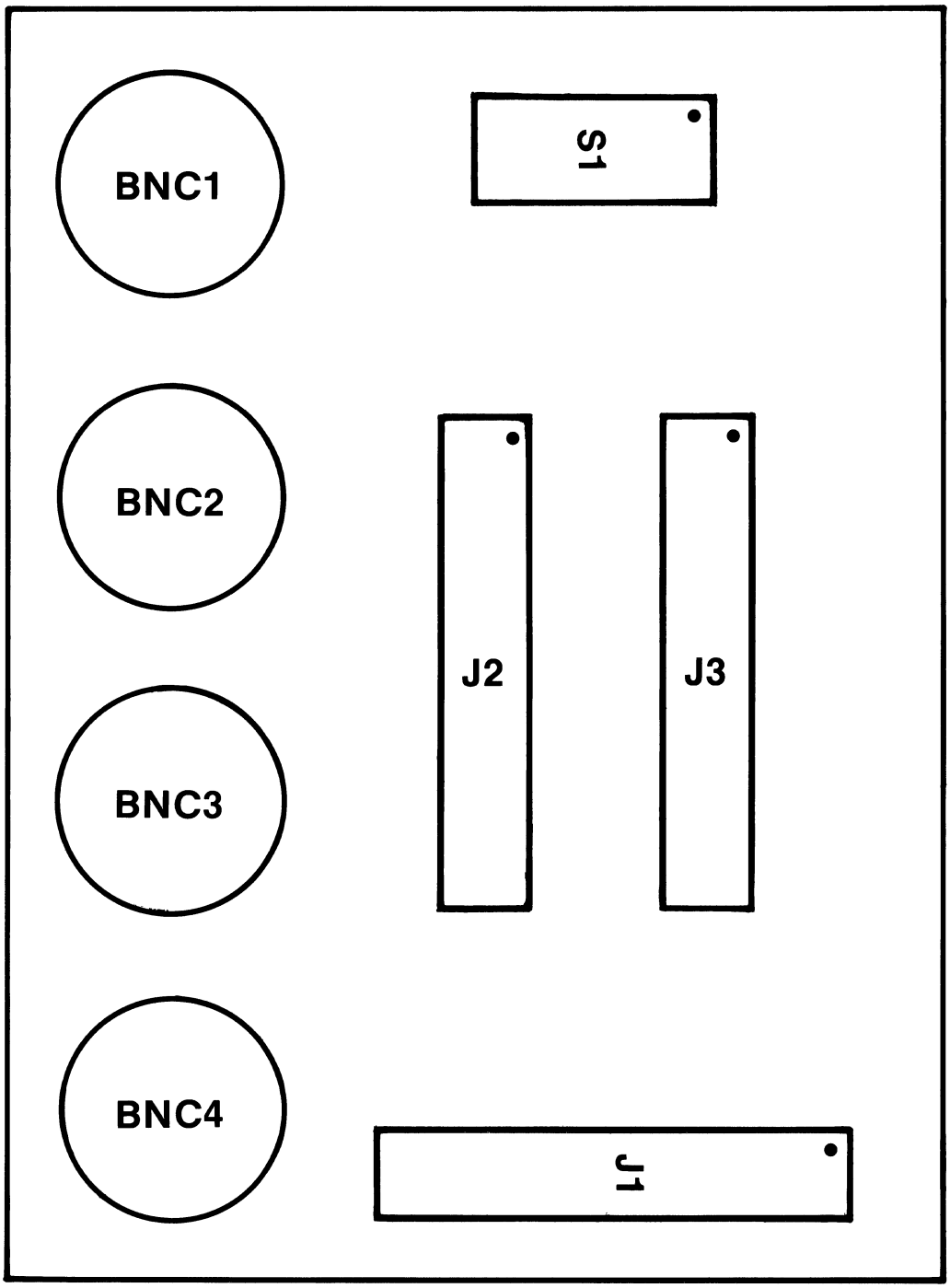


Figure 6-21. Rear Board A8 Component Locator

SECTION VII

MANUAL CHANGES

This section normally contains information for backdating this manual for models with serial number prefixes prior to the one shown on the title page. Because this edition includes the information for the first serial number prefixes, there is no backdating material.

SECTION VIII

SERVICE

8-1. INTRODUCTION.

8-2. The service section contains information necessary to service the Model 64110A Logic Development System mainframe. The information is presented in the following order:

8-3. Within each mainframe subject area the information is presented in sequence of block level description, schematic level description, troubleshooting, and finally, performance verification setups.

8-4. SAFETY CONSIDERATIONS.

8-5. This section contains warnings and cautions that must be followed for your protection and to avoid damage to the equipment. Read the safety summary on the back of the title page and all warnings given at the beginning of procedures, prior to servicing.

8-6. MAINFRAME OVERVIEW.

8-7. The overall mainframe consists of the following:

Power supply	Cardcage and motherboard
Rear panel	CPU/IO board
Keyboard	Display controller board
Display driver boards (2)	CRT display
Local mass storage/RS-232C board	Flexible disc drive

8-8. The flexible disc drive and local mass storage/RS-232C board information is included in the appendix.

8-9. MAINFRAME OVERALL BLOCK DESCRIPTION.

8-10. The relationships between the overall functional areas are shown on figure 8-1.

8-11. POWER SUPPLY BLOCK DESCRIPTION.
ASSEMBLY A1.

8-12. The power supply assembly consists of four printed circuit boards and many discrete components. The printed circuit boards are:

Primary supply board

+5, +-12 volt supply board

-3.25, -5.2 volt supply board

Interconnect board

8-13. The power supply accepts AC line voltage and provides other circuits with the following regulated dc voltages: +12V display driver, +12V, +5V, -5.2V, -3.25V and -12V. It also provides the LPOP, LIR15 and LINSYN signals.

8-14. The +12V display driver supplies power exclusively to the display driver circuitry. The LPOP signal is generated when power is first turned on and whenever there is a power failure on the AC line or +5V supply. This signal goes to the CPU/IO section where it initializes the CPU and I/O circuits.

8-15. LIR15 is generated when the power supply senses a line voltage drop below a set value. It is the only high priority interupt and goes to the CPU/IO and display driver sections. It blanks the display driver, and retracts the head from the flexible disc.

8-16. The LINSYN is a TTL signal generated from line power at line frequency and goes to the CPU/IO section where it is used in the auto-reset circuit.

8-17. CPU/IO BLOCK DESCRIPTION.
ASSEMBLY A3.

8-18. The CPU/IO functions are contained on a single printed circuit board located in card slot A. It is identified by the blue extractor tabs.

8-19. The CPU communicates through the input/output section to collect, process and redistribute data as supplied or requested by the peripherals. The input/output section contains the keyboard and HP-IB interface circuitry. Also, it contains the circuits necessary to process various interrupts, LINSYN, power fail information, and to select and interchange data with any particular slot in the cardcage.

8-20. The CPU/IO, printed circuit board A3, hosts the following functions; CPU, program ROMs, interrupt mask, mapped I/O and cardselect, keyboard scan, HP-IB, bank switching, and auto-reset.

8-21. The CPU collects, processes and redistributes data as defined in service routines stored in the program ROMs. The data is supplied or requested by the peripherals through interrupt request to the interrupt mask. Data interchange between card slots in the cardcage is controlled by the mapped I/O and card-select sections.

8-22. The CPU/IO board contains the necessary control and handshake circuits for communicating over the HP-IB link to the disc and printer and the RS-232C link to the various peripheral devices connected to this bus. The CPU/IO board also contains circuits necessary for:

a. Processing the various interrupts from the keyboard, RS-232C and HP-IB circuits.

b. Enabling the beeper via the CPU/IO board.

c. Allowing the CPU to select and interchange data with any of the several boards in the cardcage.

d. Monitoring LINSYN and power fail status and providing such information to the CPU.

8-23. DISPLAY CONTROLLER BLOCK DESCRIPTION.
ASSEMBLY A5.

8-24. Located in card slot B is the display controller board. It is identified by white extractor tabs. The display controller board provides three functions:

System clock generator

System RAM and RAM controller

CRT controller

8-25. The system clock generator provides the following clocks for use by the entire system:

L25MHz.....used by the CPU and sent to all option slots.

LSCLK1.....used by the CPU

DOTCLK.....25 MHz

RAMCLK.....12.5 MHz

LCHAR.....2.78 MHz

8-26. The RAM and RAM control provides 32k x 16 bits of dynamic RAM to be used by the system processor and the CRT controller chip. It also regulates access by the system processor and CRT controller chip to and from the RAM.

8-27. The CRT control is provided by the CRT controller chip which functions like a microprocessor to determine the information to be displayed, and to control the display drive section.

8-28. DISPLAY DRIVER BLOCK DESCRIPTION.
ASSEMBLIES A6 AND A7.

8-29. The display driver block includes two printed circuit boards. The secondary drive board contains the secondary drive and beeper circuitry. It is called assembly A6 and is mounted by hinges on the bottom of the chassis. The flyback board, assembly A7, is mounted by hinges to the top of the mainframe.

8-30. The two display driver boards provide the video, vertical, horizontal, and bias voltages to drive the CRT. The video drive circuit, on the secondary board, features two signal levels, one for regular video, and one for inverse video. The inverse video level is less to compensate for the brightness of a lit background.

8-31. The beeper provides an audio tone which is activated to alert the operater at designated points in performance verification or normal operation.

8-32. The high voltage circuit, on the flyback board, generates CRT grid voltage of -40 V, +200 to 700 V, and 0 to 470 V necessary to provide intensity and focus adjustments.

Table 8-1. Memory Map

ADDRESS	MEMORY FUNCTION
FFFF FE00	BASE PAGE RAM (512)
FDFF FA18	DISPLAY (1040)
F9F0	BLANKED DISPLAY ROW
F9EF C000	HOST RAM (15,216)
BFFF 8002	HOST RAM (16K)
8001 8000	DISPLAY CONTROL
7FFF 4000	MEMORY MAPPED I/O SLOT SELECTED (16K)
3FFF 0020	HOST ROM (16K)
001F 0000	BPC REGISTERS (INTERNAL)

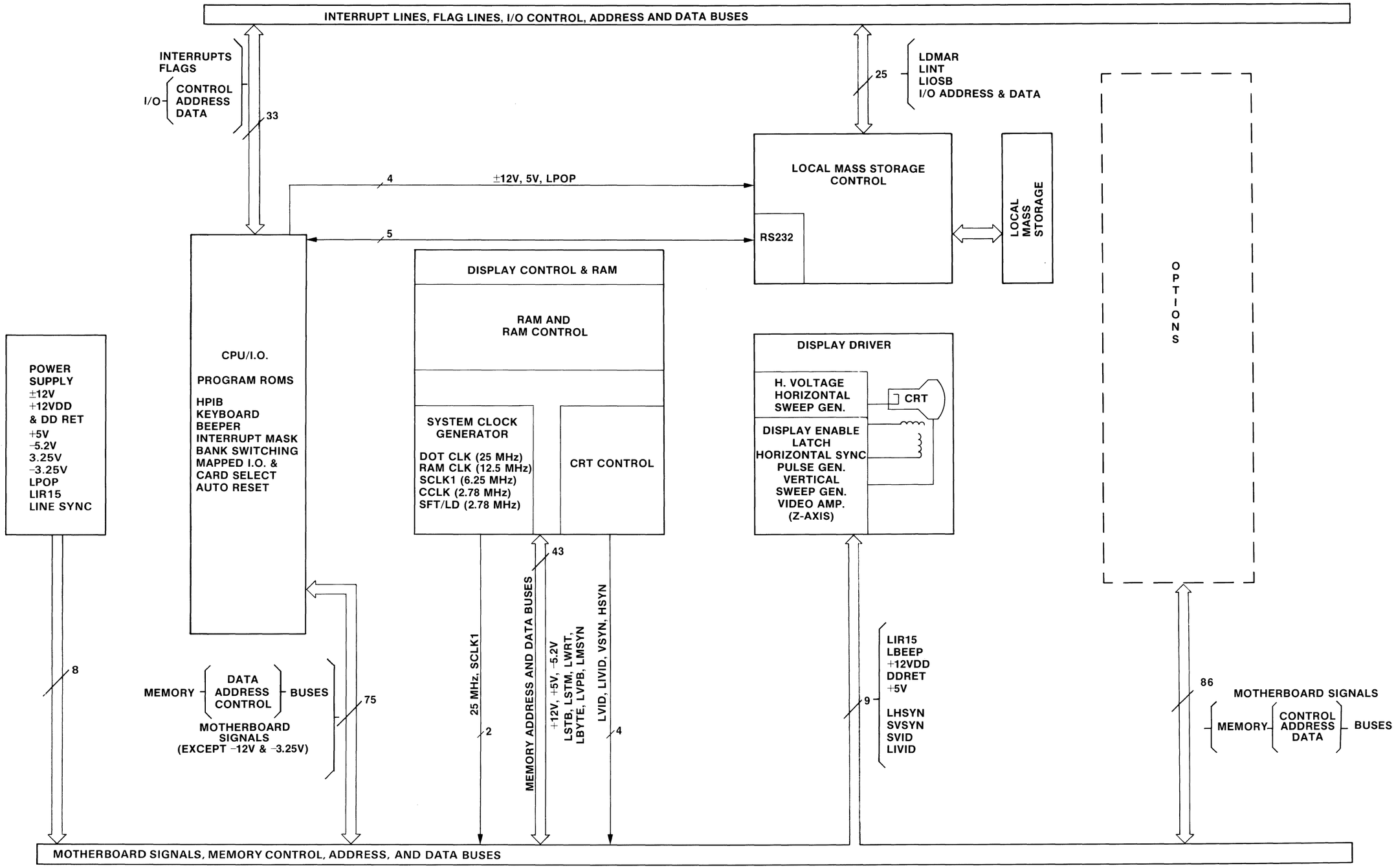


Figure 8-1.
Mainframe Overall Block Diagram (Sheet 1 of 2)

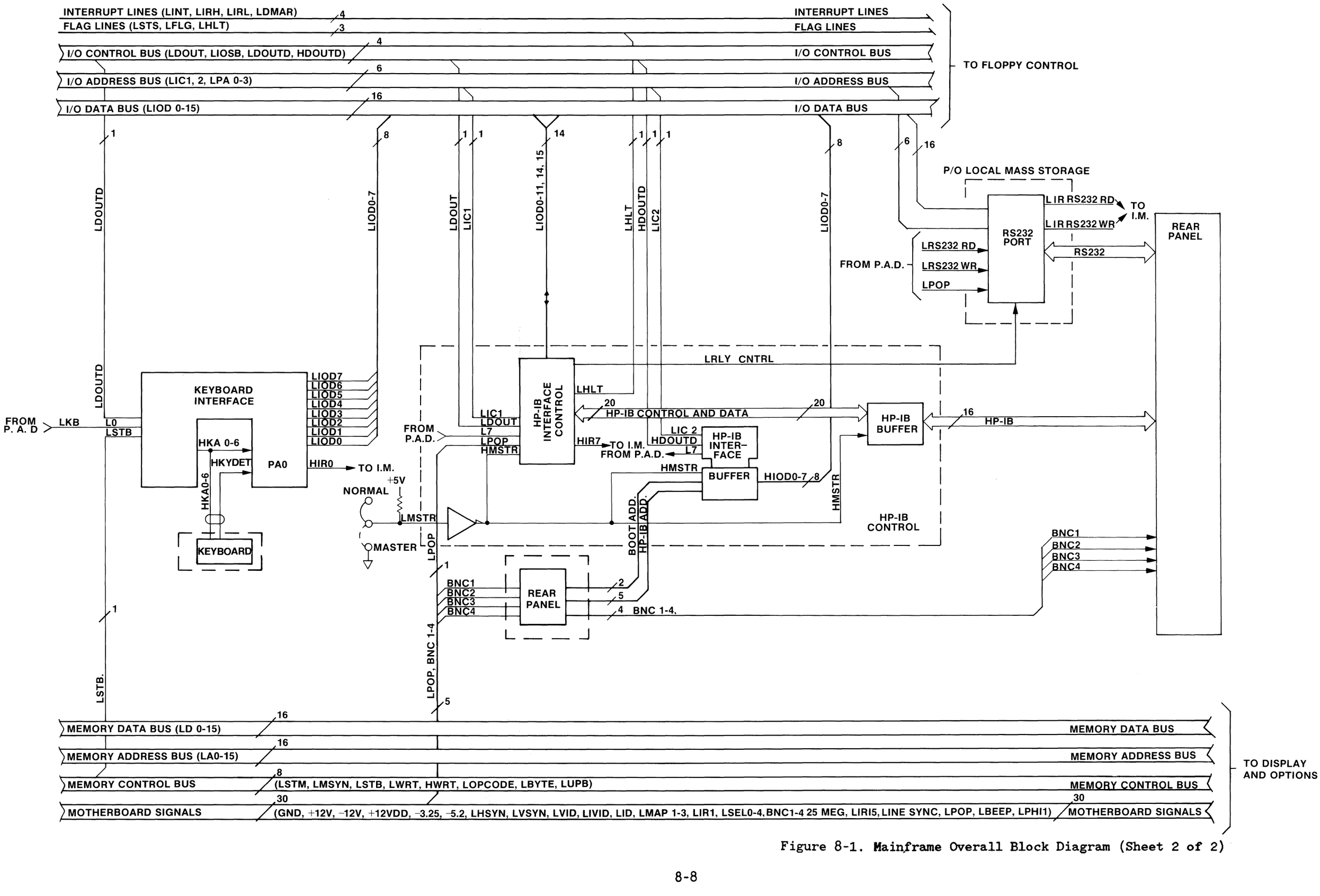


Figure 8-1. Mainframe Overall Block Diagram (Sheet 2 of 2)

8-33. MAINFRAME OVERALL TROUBLESHOOTING.

```
**********  WARNING  **********
*                              *
*  Read the Safety Summary at the front of  *
*  this  manual before troubleshooting the  *
*  instrument.                 *
*                              *
********************************
```

8-34. Before troubleshooting, refer to the Model 64110A Operating Reference Manual for general operating information as suspected malfunctions may be caused by improper operation.

8-35. Visually inspect the instrument. Look for loose or burned components that might suggest a source of trouble. Verify that all circuit board connections are making good contact and are not shorting to an adjacent circuit. Attempt to complete the Performance Verification in Section IV. If no obvious trouble is found, check the instrument power-supply voltages and external line voltage before any extensive troubleshooting.

8-36. Troubleshooting for the 64110A mainfame consists of a step by step procedure based on failures in performance verification tests, failures of signatures in signature analysis, and traditional oscilloscope troubleshooting. The procedure reflects the following hierarchy.

8-37. The hierarchy for troubleshooting the mainframe is:

a. First, the power supply must be fully operational before any other part of the mainframe will work.

b. Second, the CPU must be able to access ROM properly since the code for basic operations and performance verification is resident in ROM.

c. Third, the CPU must be able to acces RAM for scratch pad memory and display functioning.

d. Fourth, the display should be operational for feedback on the operation of the mainframe.

e. Fifth, the I/O functions are repaired.

8-38. Before troubleshooting the mainframe, remove all option cards and make sure that all jumpers are in the normal position. The procedure assumes that all jumpers are in the normal position. Any option card has the potential of causing the mainframe to operate incorrectly by interfering with the memory bus transactions of the CPU or causing the power supply to shut down.

8-39. When using signature analysis the approach is to troubleshoot:

a. First, the control signals. If the control signals are bad, the output of the IC's will be bad.

b. Second, addressing if appropriate.

c. Third, if the above are correct, the actual data bit failure checking the input versus the output of the IC.

8-40. Any device connected to the signature analysis node (input or output to an IC or passive components) may cause the bad signature.

8-41. Always use the schematics when taking signatures.

8-42. POWER-UP SELF TEST FAILURE.

8-43. First, draw as much information as possible from the power-up self test beep sequence. These tests will verify the ability of the CPU to access ROM and RAM correctly. The display test pattern verifies the display operation, and then the PV menu tests allow the checking of the I/O functions.

8-44. A failure in the power on self tests may be determined by noting the beep sequence. Table 8-2 details the beep sequence during power-up self tests and the step to go to on failure.

Table 8-2. Power-Up Failure - Beep Sequence Failing

BEEP....the beeper beeps when power is first turned on. This does not mean that the power supply is fully operational.

BEEP NOT PRESENT....check power supply

POWER SUPPLY FAILURE....go to power supply troubleshooting paragraphs.

POWER SUPPLY OK....go to signature analysis test loop determination table.

BEEP....software is initiated and the display is enabled.

BEEP NOT PRESENT....check power supply

POWER SUPPLY FAILURE....go to power supply troubleshooting paragraphs.

POWER SUPPLY OK....go to signature analysis test loop determination table.

3 BEEPS....Indicates ROM test passed

SEQUENCE OF 3 BEEPS NOT PRESENT....check power supply

POWER SUPPLY FAILURE....go to power supply troubleshooting paragraphs.

POWER SUPPLY OK....go to power-up ROM test table.

APPROXIMATE 7 SECOND DELAY

2 BEEPS....Indicates RAM test passed

SEQUENCE OF 2 BEEPS NOT PRESENT....check power supply

POWER SUPPLY FAILURE....go to power supply troubleshooting paragraphs.

POWER SUPPLY OK....go to RAM troubleshooting paragraphs.

Table 8-3. Power-Up Failure - Beep Sequence Passing

NO DISPLAY....Press [B] key.

MAINFRAME BEEPS....go to display troubleshooting paragraphs.

NO BEEP....go to signature analysis test loop determination table.

WRONG BOOT SOURCE....use signature analysis setup A table. (Power-up boot rear panel switch read setup).

NO KEYS BEING READ....go to keyboard test failure in PV-tests failures table.

INCORRECT IDENTIFICATION OF OPTION CARDS....use signature analysis setup C (PV menu I/O write test setup) to troubleshoot the slot select circuitry, and check for stuck bits on the CPU memory bus.

MAINFRAME REBOOTS APPROXIMATELY EVERY 2 SECONDS....move jumper J6 to test to disable auto-reset. Check low priority interrupt circuitry to find possible constant low priority interrupt and use appropriate SA setup to troubleshoot. Use signature analysis setup C table (PV menu I/O write test setup) to troubleshoot delta time interrupt circuit.

LOSS OF KEYBOARD REPEATER FUNCTION....go to time interrupt test failure in PV-tests failures table.

8-45. PV MENU SELF-TEST FAILURE.

Table 8-4. PV-Tests Failures (1 of 2)

ROM TEST FAILURE....Decode error mask and replace failing ROM(s).

DOESN'T FIX PROBLEM....go to ROM troubleshooting table.

SELF-TEST FAILURE
ROM TEST:

FAILING ADDRESS RANGE	BYTE(S)
xxxx-xxxx	xx

Failed Addresses	Byte	Failed ROM Unit
0020-1FFF	0	U51 Lower 8K ROM
0020-1FFF	1	U48
2000-3BFF	0	U50 Upper 8K ROM
2000-3BFF	1	U49

RAM TEST FAILURE....Decode error mask and replace failing RAM(s).

DOESN'T FIX PROBLEM....go to RAM troubleshooting paragraph.

SELF-TEST FAILURE
*RAM TEST:
FAILING UNIT NUMBERS (S)

XY

Where XY is the RAM U-number.
* Displays RAM TEST: or RAM TEST: REFRESH FAILURE

Table 8-4. PV-Tests Failures (2 of 2)

I/O READ ERROR....use signature analysis setup F table (PV menu I/O read test setup) to troubleshoot.

TIME INTERRUPT TEST FAILURE.

CHECK LINSYN SIGNAL FROM POWER SUPPLY.

BAD....go to power supply troubleshooting paragraphs.

GOOD....use signature analysis setup C table (PV menu I/O write test setup) to check that the interrupts are being issued from delta time interrupt circuitry, and that the CPU is clearing delta time interrupt latch and autoreset counters.

KEYBOARD TEST FAILURE....use signature analysis setup E table (keyboard freerun setup).

BAD Vh.

NO CLOCK....use signature analysis setup 0 table (CRT controller outputs-hardware loop setup) to troubleshoot HSYN.

NO START/STOP....use signature analysis setup E table (keyboard freerun setup) to troubleshoot state machine and keyboard counters.

VALID Vh.

BAD SIGS....troubleshoot.

NO BAD SIGS....use signature analysis setup D table (keyboard buffer test setup) to troubleshoot.

SYSTEM BUS TEST FAILURE....go to system bus troubleshooting paragraph.

RS232 TEST FAILURE....use signature analysis setup H table (PV menu rs232 test setup) and signature analysis setup C (PV menu I/O write test setup) to troubleshoot. The RS232 connectors and cable are not tested in the PV menu RS232 test.

8-46. TEST LOOP DETERMINATION SIGNATURE ANALYSIS SETUP TROUBLESHOOTING.

Table 8-5. Signature Analysis Test Loop Determination

LOOPNAME: TEST LOOP DETERMINATION

The memory signature analysis latch is set and reset during the execution of the software tests. The interval is unique to the test being performed.

SETUP NAME: TEST LOOP DETERMINATION

In the event that the display is not functioning correctly, this setup can be used to determine which of the tests the mainframe is executing.

All option boards removed

All jumpers in normal position

ST/SP/START: A3TP5, rising edge (MEM SA LATCH)

QUAL/STOP: A3TP5, falling edge (MEM SA LATCH)

CLOCK: A3TP1, rising edge (LSTB)

Signatures

Vh = CA27 POWER ON RAM TEST LOOP-SIMPLE RAM FAILURE
Go to simple RAM failure troubleshooting.

Vh = AH68 POWER ON RAM TEST LOOP-REFRESH FAILURE
Go to RAM refresh failure troubleshooting.

Vh = AU94 DISPLAY TEST
If wrong or no display, go to display troubleshooting.

NO RECOGNIZABLE Vh Go to ROM troubleshooting.

8-47. SYSTEM BUS TROUBLESHOOTING.

Table 8-6. System Bus Failures

FAILING PV MENU SYSTEM BUS TEST.

YES....use signature analysis setup G table (PV menu system bus test setup) and signature analysis setup C (PV menu I/O write test setup) to troubleshoot.

NO....setup G, the PV menu system bus test does not completely check the mainframe. The following suggestions will help you to isolate the failure to the mainframe, system bus cables, or other devices connected to the system bus if a failure exists on the system bus.

1. Verify that the system bus configuration is correct. If the configuration is wrong, this can cause problems in bus communications. Refer to the site selection and installation manual for proper bus configuration.

   Disc set to address 0 and printer set to address 1; required by operating system software.

   Mainframes set to addresses 2-7 with no two at the same address.

   No more than two connectors connected to any device. Twenty meters maximum total cable length.

   Only one master controller, and the master located at the end of the chain of devices.

2. Suspect the HP-IB cables.

3. If there are more than the disc and one mainframe, remove all but the master controller and disc from the bus. If the failure goes away, add one device at a time until the failing device is found. Troubleshoot that device. If the failure remains, swap the components listed below for troubleshooting a failing mainframe. If that doesn't work then the problem is with the disc or system bus cable.

4. If the problem is isolated to a mainframe, swap the HP-IB transceivers, PHI chip, and rear panel cables and connectors. These are not tested in the system bus test. The HP-IB transceivers and PHI chip are in sockets, so the socket could be causing the problem.

5. Problems may be caused by the line power source. Refer to section I for proper power sources.

Table 8-7. Signature Analysis Setup A (1 of 3)

LOOPNAME: POWER-UP BOOT REAR PANEL SWITCH READ

The Memory SA latch is set and reset around the reading of the rear panel switches on boot up.

SETUP NAME: POWER-UP BOOT REAR PANEL SWITCH READ

This setup is used to troubleshoot the circuitry associated with the reading of the rear panel seitches in the event that the mainframe fails to read the rear panel seitches correctly.

ST/SP/START: A3TP5, rising edge (MEM SA LATCH)

QUAL/STOP: A3TP5, falling edge (MEM SA LATCH)

CLOCK: A3TP1, rising edge (LBIOSB)

Vh = U952

Node	Signature	Node	Signature
U 11- 5	low	U 27-14	high
U 13- 4	U952	U 28- 5	high
U 13- 5	high	U 28-15	high
U 13- 6	high		
U 13- 7	high		
U 13- 8	0000		
U 13- 9	U952		
U 13-11	U952		
U 13-12	0000		
U 13-13	high		
U 13-14	high		
U 13-15	high		
U 13-16	U952		
U 15- 3	low		
U 17- 8	high		
U 17- 9	low		

Table 8-7. Signature Analysis Setup A (2 of 3)

Node	Signature
Set switches to	
HPIB address-1F	
Boot source to PV	
TERM/MOD jumper A3J10 to MOD	
Master controller	
U 22- 1	high
U 22- 3	low
U 22- 5	low
U 22- 7	low
U 22- 9	low
U 22-12	low
U 22-14	low
U 22-15	low
U 22-16	low
U 22-18	low
U 22-19	low
U 40- 1	low
U 40-11	U952
U 40-12	U952
U 40-13	U952
U 40-14	U952
U 40-15	U952
U 40-16	U952
U 40-17	U952
U 40-18	U952
U 40-19	low
U 43- 1	high
U 43- 3	low
U 43- 5	low
U 43- 7	low
U 43- 9	low
U 43-12	low
U 43-14	low
U 43-16	low
U 43-17	low
U 43-18	low
U 43-19	high
U 47- 1	low
U 47-11	U952
U 47-12	U952
U 47-13	U952
U 47-14	U952
U 47-15	U952
U 47-16	U952
U 47-17	U952
U 47-18	U952
U 47-19	low
Set switches to	
HPIB address 00	
Boot source to System Bus	
TERM/MOD jumper A3J10 to TERM	
U 22- 1	high
U 22- 2	high
U 22- 3	low
U 22- 5	low
U 22- 7	low
U 22- 9	low
U 22-12	low
U 22-14	low
U 22-16	low
U 22-18	low
U 22-19	high
U 40- 1	low
U 40-11	U952
U 40-12	U952
U 40-13	U952
U 40-14	U952
U 40-15	U952
U 40-16	U952
U 40-17	U952
U 40-18	U952
U 40-19	low

Table 8-7. Signature Analysis Setup A (3 of 3)

Node	Signature
U 43- 1	high
U 43- 3	low
U 43- 5	low
U 43- 7	low
U 43- 9	low
U 43-12	low
U 43-14	low
U 43-16	low
U 43-18	low
U 43-19	high
U 47- 1	low
U 47-11	U952
U 47-12	U952
U 47-13	U952
U 47-14	U952
U 47-15	U952
U 47-16	U952
U 47-17	U952
U 47-18	U952
U 47-19	low

Table 8-8. Signature Analysis Setup B (1 of 3)

LOOPNAME: DISPLAY TEST

During the display test the following I/O functions are performed.

I/O data lines are toggled

Delta time interrupt latch and counters are cleared

Interrupt masks are cycled

Rear panel switches are read

The floppy is written to

Even I/O addresses are toggled

Keyboard is read

SETUP NAME: I/O BUS TEST

This setup may be used to troubleshoot the above circuitry. Executing display test and with keyboard buffer A3U25 removed, set switches as follows:

HPIB addr 0

Boot source PV

Term/Mod jumper J10 to Term

Hardware configuration jumpers-none installed

Mainframe set to normal (non-master controller)

ST/SP/START: A3TP5, rising edge (MEM SA LATCH)

QUAL/STOP: A3TP5, falling edge (MEM SA LATCH)

CLOCK: A3TP7, rising edge (LBIOSB)

Vh = 80C0

Table 8-8. Signature Analysis Setup B (2 of 3)

Node	Signature	Node	Signature
U 11- 5	000C	U 24- 2	U6CC
U 11- 7	38A9	U 24- 5	7C65
U 11- 9	HFC7	U 24- 6	8971
U 11-12	UAH8	U 24- 9	U1H9
U 11-14	UAH5	U 24-12	AUA9
U 11-16	7A6P	U 24-15	7ACP
U 11-18	80C9	U 24-16	U835
		U 24-19	96U3
U 12- 9	80C1		
U 12-10	high	U 26- 9	80C1
U 12-12	UAH9		
U 12-15	high	U 27-14	80CC
U 13- 4	UAH8	U 28- 7	80C2
U 13- 5	38A9	U 28-10	7A66
U 13- 6	UAH5	U 28-13	high
U 13- 7	HFC7	U 28-14	high
U 13- 8	7A6P	U 28-15	80C8
U 13- 9	80C9		
U 13-11	80C9	U 30- 3	80C8
U 13-12	7A6P	U 30- 6	80C8
U 13-13	HFC7		
U 13-14	UAH5	U 34- 1	0002
U 13-15	38A9		
U 13-16	UAH8	U 35- 6	80CC
		U 35- 8	0000
U 15- 3	000C		
U 15-17	000C		
U 17- 5	80C0		
U 17- 8	80CC		
U 17- 9	000C		
U 20- 3	80C2		

Table 8-8. Signature Analysis Setup B (3 of 3)

Node	Signature
U 40- 2	3839
U 40- 3	952H
U 40- 4	F644
U 40- 5	6H5A
U 40- 6	C4C9
U 40- 7	6AF0
U 40- 8	F1UU
U 40- 9	1792
U 40-11	9722
U 40-12	414U
U 40-13	PA70
U 40-14	3409
U 40-15	PHPA
U 40-16	46U4
U 40-17	159H
U 40-18	C889
U 41- 5	80C0
U 47- 2	PA4F
U 47- 3	P57C
U 47- 4	5HU1
U 47- 5	545C
U 47- 6	6A37
U 47- 7	2H32
U 47- 8	0187
U 47- 9	C69U
U 47-11	362U
U 47-12	8137
U 47-13	AH82
U 47-14	PA87
U 47-15	H4PC
U 47-16	HH41
U 47-17	65FC
U 47-18	6AUF
U 58- 4	000C
U 58- 5	80CC

Table 8-9. Signature Analysis Setup C (1 of 3)

LOOPNAME: PV MENU I/O WRITE

During the test, the following I/O writes are performed:

Cycle interrupt masks

Bank switching, slot select

PHI register addresses

Beeper

SETUP NAME: PV MENU I/O WRITE TEST

The setup allows the troubleshooting of the above I/O circuitry and I/O busses.

Executing PV menu I/O write test

ST/SP/START: A3TP5, rising edge (MEM SA LATCH)

QUAL/STOP: A3TP5, falling edge (MEM SA LATCH)

CLOCK: A3TP7, rising edge (LBIOSB)

VH = UF8H

Table 8-9. Signature Analysis Setup C (2 of 3)

Node	Signature	Node	Signature
U 11- 5	0001	U 24- 2	2487
U 11- 7	550A	U 24- 5	09A3
U 11- 9	7720	U 24- 6	23CA
U 11-12	PFH1	U 24- 9	A968
U 11-14	7842	U 24-12	C4U2
U 11-16	PAH4	U 24-15	135F
U 11-18	9296	U 24-16	990A
		U 24-19	2U2U
U 12- 9	7P47		
U 12-10	0605	U 26- 5	high
U 12-12	9493		
U 12-15	high	U 27-14	UF8F
U 13- 4	PFH1	U 28- 7	high
U 13- 5	550A	U 28-10	UF8H
U 13- 6	7842	U 28-13	high
U 13- 7	7720	U 28-14	high
U 13- 8	PAH4	U 28-15	105F
U 13- 9	9296		
U 13-11	9296	U 30- 6	105F
U 13-12	PAH4		
U 13-13	7720	U 34- 4	0000
U 13-14	7842	U 34-13	UF8F
U 13-15	550A		
U 13-16	PFH1	U 35- 6	7P47
		U 35- 8	0000
U 15- 3	0001		
		U 37- 3	105F
U 17- 8	UF8F		
U 17- 9	0001	U 38- 2	P4C7
		U 38- 7	FCHC
U 18- 8	UF8F	U 38-11	4C4F
		U 38-15	2HH8
		U 40- 2	69P5
		U 40- 3	52H1
		U 40- 4	26C9
		U 40- 5	4774
		U 40- 6	C0HU
		U 40- 7	1347

Table 8-9. Signature Analysis Setup C (3 of 3)

Node	Signature
U 41- 9	high
U 41-10	0000
U 47- 2	9HHH
U 47- 3	U83A
U 47- 4	U9P8
U 47- 5	07C1
U 47- 6	774A
U 47- 7	64HH
U 47- 8	762A
U 47- 9	62HA
U 54- 2	OPPU
U 54- 5	FHU8
U 54- 6	PCPU
U 54- 9	9P3P
U 54-12	6HF9
U 54-15	657C
U 54-16	A987
U 54-19	FPUA
U 73- 6	6150
U 73-11	UF8H
U 73-12	UF8H
U 73-13	UF8H
U 73-14	UF8H
U 73-15	UF8H
U 75- 1	04C7
U 75- 4	UF8H
U 75- 9	77HP
U 75-10	C924
U 75-11	HP59
U 75-12	PF2P
On A10 Mini and RS232	
U 63- 2	4C4F
U 63- 3	low

Table 8-10. Signature Analysis Setup D (1 of 2)

LOOPNAME: DISPLAY TEST

Included in the display test is the software necessary to take signatures on the keyboard buffer.

SETUP NAME: KEYBOARD BUFFER TEST

If the keyboard buffer or I/O bus transceivers fail, this test can be used to isolate the failure. When in this setup, the low priority interrupts are disabled so the keyboard interrupt routine is not called. Keys with alternate 1's and 0's are pressed to provide the stimulous.

Executing display test

LIRL jumper J9 to test

Auto-reset jumper J6 to test

Keyboard RAM A3U9 removed

Press dash key and take signatures

Press return key and take signatures

ST/SP/START: A3TP5, rising edge (MEM SA LATCH)

QUAL/STOP: A3TP5, falling edge (MEM SA LATCH)

CLOCK: A3TP18, rising edge (LRDKYBD)

Vh = 0001

Table 8-10. Signature Analysis Setup D (2 of 2)

With [RETURN] Depressed		With Dash Key Depressed	
Node	Signature	Node	Signature
U 10- 3	0001	U 10- 3	0000
U 10- 4	0000	U 10- 4	0001
U 10- 5	0001	U 10- 5	0000
U 10- 6	0001	U 10- 6	0001
U 10- 9	0001	U 10- 9	0000
U 10-10	0000	U 10-10	0000
U 10-11	0000	U 10-11	0001
U 25- 3	0000	U 25- 3	0001
U 25- 5	0001	U 25- 5	0001
U 25- 7	0001	U 25- 7	0000
U 25- 9	0001	U 25- 9	0001
U 25-12	0001	U 25-12	0000
U 25-14	0000	U 25-14	0001
U 25-16	0001	U 25-16	0000
U 25-18	0001	U 25-18	0000
U 33- 9	0001	U 33- 9	0001
U 40-11	0000	U 40-11	0001
U 40-12	0001	U 40-12	0000
U 40-13	0000	U 40-13	0001
U 40-14	0000	U 40-14	0000
U 40-15	0001	U 40-15	0000
U 40-16	0000	U 40-16	0001
U 40-17	0000	U 40-17	0001
U 40-18	0000	U 40-18	0000

Table 8-11. Signature Analysis Setup E (1 of 3)

LOOPNAME: KEYBOARD FREERUN

This is a hardware loop in which the keyboard circuitry is allowed to freerun. The asynchronous operations of the CPU servicing the keyboard interrupts and the pressing of a key are disabled by moving the jumper in A3XU1 to the test position. All locations in the keyboard status RAM are written high and then low to allow checking of the RAM.

SETUP NAME: KEYBOARD FREERUN

Keyboard freerun causes a unique signature to be generated on the HKYDET line for each key pressed. A failure in the keyboard scanning circuitry may be isolated using this setup.

Move keyboard freerun jumper A3XU1 to test

Move the auto reset enable jumper A3J6 to test

ST/SP/START: A3TP17, rising edge (HKA7)

QUAL/STOP: A3TP17, rising edge (HKA7)

CLOCK: A3TP19, rising edge (LHSYN)

Vh = 8P54

Table 8-11. Signature Analysis Setup E (2 of 3)

Node	Signature	
U 9- 6	65P1	Keyboard scan circuitry on the A3 CPU/IO board.
U 10- 3	0863	
U 10- 4	HH53	
U 10- 5	H10F	
U 10- 6	3A9A	
U 10- 9	2946	
U 10-10	F61C	
U 10-11	0108	
U 15- 9	FCF2	
U 20-11	71CC	
U 33- 5	CU1U	
U 33- 6	314C	
U 33- 9	65P1	
U 1- 7	0FP0	Keyboard A4 multiplexers and demultiplexers.
U 1- 9	A51H	
U 1-10	3AFP	
U 1-11	F7UF	
U 1-12	14H1	
U 1-13	2603	
U 1-14	0C2P	
U 1-15	H9UH	
U 2- 7	9UH4	
U 2- 9	9658	
U 2-10	0P9F	
U 2-11	82H3	
U 2-12	462F	
U 2-13	09HF	
U 2-14	U6H6	
U 2-15	067U	
		Keyboard A4 comparator ICs.
U 9- 1	F878	SK8 depressed
U 9- 2	1180	[RESET] depressed
U 9- 3	80F8	[BACK SPACE] depressed
U 9- 4	882C	[I] depressed
U 9-12	1180	[PREV. PAGE] depressed
U 9-13	80F8	[RETURN] depressed
U 9-14	1180	[NEXT PAGE] depressed
U 9-15	1180	[DELETE CHAR] depressed

Table 8-11. Signature Analysis Setup E (3 of 3)

The following signatures are taken on the HKYDET line A3XU1 pin 15 or A4U3 pin 5. A unique signature applies to each key depressed.

Key Pressed	Signature	Key Pressed	Signature
SK1	84UU	@	P3F8
SK2	F84U	[	0P3F
SK3	47F8	UNDERSCORE	70P3
SK4	047F	ROLL UP	H70P
SK5	2160	UP ARROW	6H70
SK6	0216	NEXT PAGE	A6H7
SK7	3021	CNTL	077P
SK8	UA30	A	3077
CLR LINE	4A3A	S	ACUA
RECALL	U4A3	D	2ACU
CAPS LOC	UU4A	F	H2AC
RESET	4UU4	G	AH2A
1	7CF5	H	FAH2
2	87CF	J	8AA4
3	887C	K	CH2F
4	7887	L	3CH2
5	H788	;	C3CH
6	1H78	:	8C3C
7	CU17	]	08C3
8	HCU1	RETURN	608C
9	6HCU	LEFT ARROW	F608
0	46HC	RIGHT ARROW	CF60
DASH	146H	LEFT SHIFT	UA1H
CARROT	P146	Z	A8UF
\	AP14	X	3A8U
BACK SPACE	5AP1	C	43A8
INSERT CHAR	A026	V	FA0U
DELETE CHAR	FA02	B	2FA0
TAB	48UC	N	F719
Q	A48U	M	8F71
W	F307	,	78F7
E	FF30	.	H78F
R	2FF3	/	5H78
T	P2FF	RIGHT SHIFT	95H7
Y	6P2F	ROLL DOWN	U95H
U	16P2	DOWN ARROW	FU95
I	516P	PREV PAGE	1FU9
O	FFPF	SPACE BAR	7190
P	UFFP		

Table 8-12. Signature Analysis Setup F (1 of 3)

LOOPNAME: PV MENU I/O READ TEST

A read of the RS232 switch settings, rear panel switch settings. and master or non-master controller is done during the I/O read test. The switch settings are output to the display in the following format.

I/O READ TEST ADDR=XX BOOT=XX M=X RS232=XXXXXXXXX HC=XX

ADDR is the HPIB address 00 to 1F as set by rear panel switches.

BOOT is the boot source as set by the rear panel switches.

00 = System bus
01 = Local mass storage talk only
10 = Local mass storage addressable
11 = Performance Verification

M is 1=master controller, 0=normal (non-master controller)

RS232 switch settings are:

Bit 0....A3J10	0 = TERM, 1 = MOD
Bit 1....not used	always = 1
Bit 2....A10U55 S6	0 = closed, 1 = open
Bit 3....A10U55 S5	0 = closed, 1 = open
Bit 4....A10U55 S4	0 = closed, 1 = open
Bit 5....A10U55 S3	0 = closed, 1 = open
Bit 6....A10U55 S2	0 = closed, 1 = open
Bit 7....A10U55 S1	0 = closed, 1 = open

HC are the hardware configuration jumpers, not used at this time.

SETUP NAME: PV MENU I/O READ TEST

By setting the switches such that all zeros should be read and then so all ones should be read, the bit or bits that are in error may by traced through the circuitry to find the failed component.

Executing I/O read test

No hardware configuration jumpers installed

ST/SP/START: A3TP5, rising edge (MEM SA LATCH)

QUAL/STOP: A3TP5, falling edge (MEM SA LATCH)

CLOCK: A3TP7, rising edge (LBIOSB)

Vh = 0007

Table 8-12. Signature Analysis Setup F (2 of 3)

Node	Signature
U 11- 5	0007
U 11- 7	0003
U 11- 9	0004
U 11-12	0006
U 11-14	0001
U 11-15	0007
U 11-16	0001
U 11-18	0004
U 12- 9	0006
U 12-10	high
U 12-12	0007
U 12-15	high
U 13- 4	0006
U 13- 5	0003
U 13- 6	0001
U 13- 7	0004
U 13- 8	0001
U 13- 9	0004
U 13-11	0004
U 13-12	0001
U 13-13	0004
U 13-14	0001
U 13-15	0003
U 13-16	0006
U 15- 3	0007
U 15-17	0007
U 17- 5	0007
U 17- 8	0000
U 17- 9	0007
U 27-14	0000
U 28- 7	high
U 28-10	0007
U 28-13	high
U 28-14	0003
U 28-15	0005
U 30- 3	0005
U 30- 6	0005

Node	Signature
U 34- 4	0000
U 34-13	0000
U 35- 6	0004
U 35- 8	0004
	Switch settings
	HPIB address 1F
	Boot source-PV
	RS232 switches A10U5-open
	TERM/MOD jumper A3J1-MOD
	Master controller
U 22- 1	0005
U 22- 3	0007
U 22- 5	0007
U 22- 7	0007
U 22- 9	0007
U 22-12	0007
U 22-14	0007
U 22-16	0007
U 22-18	0007
U 22-19	0005
U 40- 1	0007
U 40-11	0000
U 40-12	0000
U 40-13	0000
U 40-14	0000
U 40-15	0000
U 40-16	0000
U 40-17	0000
U 40-18	0000
U 40-19	0004
U 43- 1	0005
U 43- 3	0007
U 43- 5	0007
U 43- 7	0007
U 43- 9	0007
U 43-12	0007
U 43-14	0007
U 43-16	0007
U 43-18	0007
U 43-19	0005

Table 8-12. Signature Analysis Setup F (3 of 3)

Node	Signature
U 47- 1	0007
U 47-11	0000
U 47-12	0000
U 47-13	0000
U 47-14	0000
U 47-15	0000
U 47-16	0000
U 47-17	0000
U 47-18	0000
U 47-19	0004

Switch settings
HP-IB address-00
Boot source-System Bus
See note below.
RS232 switches A10U5-closed
TERM/MOD jumper A3J1-TERM
Normal (non-master controller)

Node	Signature
U 22- 1	high
U 22- 3	0005
U 22- 5	0005
U 22- 7	0007
U 22- 9	0005
U 22-12	0005
U 22-14	0005
U 22-16	0005
U 22-18	0005
U 22-19	high

Node	Signature
U 40- 1	0007
U 40-11	0002
U 40-12	0002
U 40-13	0002
U 40-14	0002
U 40-15	0002
U 40-16	0000
U 40-17	0002
U 40-18	0002
U 40-19	0004

Node	Signature
U 43- 1	0005
U 43- 3	0007
U 43- 5	0007
U 43- 7	0007
U 43- 9	0005
U 43-12	0005
U 43-14	0007
U 43-16	0007
U 43-18	0007
U 43-19	0005

Node	Signature
U 47- 1	0007
U 47-11	0006
U 47-12	0002
U 47-13	0004
U 47-14	0004
U 47-15	0004
U 47-16	0004
U 47-17	0004
U 47-18	0004
U 47-19	0004

NOTE: Change switches from PV to system bus after test is executing.

Table 8-13. Signature Analysis Setup G (1 of 2)

LOOPNAME: PV MENU SYSTEM BUS TEST

During the test, the PHI chip is taken off line and the internal registers of the PHI chip are written to and read from. Note: The failure code given should the test fail does not present usable information. If the test fails, it may take up to two minutes to complete.

SETUP NAME: PV MENU SYSTEM BUS TEST

Stimulus is provided for troubleshooting the I/O bus transceivers, PHI control circuitry, and the functioning of most of the PHI chip itself.

Executing PV menu system bus test

ST/SP/START: A3TP5, rising edge (MEM SA LATCH)

QUAL/STOP: A3TP5, falling edge (MEM SA LATCH)

CLOCK: A3TP7, rising edge (LBIOSB)

Vh = 9A4A

Node	Signature	Node	Signature
U 11- 5	9029	U 13- 4	9A4C
U 11- 7	452U	U 13- 5	452U
U 11- 9	HU65	U 13- 6	0001
U 11-12	9A4C	U 13- 7	HU65
U 11-14	0001	U 13- 8	0001
U 11-15	9029	U 13- 9	0000
U 11-16	0001	U 13-11	0000
U 11-18	0000	U 13-12	0001
		U 13-13	HU65
U 12- 9	9A4C	U 13-14	0001
U 12-10	high	U 13-15	452U
U 12-12	9A4A	U 13-16	9A4C
U 12-13	high		
U 12-15	high		

Table 8-13. Signature Analysis Setup G (2 of 2)

Node	Signature	Node	Signature
U 15- 3	9029	U 40- 2	61U6
U 15-17	9029	U 40- 3	574F
		U 40- 4	8CP6
U 17- 5	9A4A	U 40- 5	A18F
U 17- 8	0A63	U 40- 6	H32F
U 17- 9	9029	U 40- 7	5549
		U 40- 8	4PUH
U 18- 8	0A63	U 40- 9	4F66
		U 40-11	H62F
U 27-14	0A63	U 40-12	H4C7
		U 40-13	FU03
U 28- 7	high	U 40-14	4966
U 28-10	9A4A	U 40-15	3CF6
U 28-13	high	U 40-16	11AF
U 28-14	high	U 40-17	FH06
U 28-15	0001	U 40-18	UCCF
U 30- 4	0001	U 47- 2	ACC6
U 30- 5	HU65	U 47- 3	ACC6
U 30- 6	HU64	U 47- 4	3C9P
		U 47- 5	3C9P
U 34- 4	0000	U 47- 6	3C9P
U 34-13	0A63	U 47- 7	3A12
		U 47- 8	98A3
U 35- 6	9A4C	U 47- 9	C415
U 35- 8	0000	U 47-11	2P5U
		U 47-12	02P9
U 37- 3	HU64	U 47-13	A058
U 37- 6	452U	U 47-14	A1H4
		U 47-15	A1H4
U 38- 2	07A8	U 47-16	A1H4
U 38- 7	17FA	U 47-17	31UF
U 38-11	high	U 47-18	31UF
U 38-15	2427		
		U 63- 2	high
		U 63- 3	low

Table 8-14. Signature Analysis Setup H (1 of 2)

LOOPNAME: PV MENU RS232 TEST

The mainframe has loopback relays to loop back control and data signals from the output of the USART chip through the voltage translators and back to the receive ports. SA stimulus is provided in this testing loop.

NOTE

The failure code given, should the test fail, does not present usable information. If the test fails, it may take up to 2 minutes to complete.

SETUP NAME: PV MENU RS232 TEST

A failure in the RS232 circuitry may be isolated using this setup.

Executing PV menu RS232 test

Top switch of S2 (A10U60) in closed position

RS232 switches S1 (A10U55) in closed position

ST/SP/START: A3TP5, rising edge (MEM SA LATCH)

QUAL/STOP: A3TP5, falling edge (MEM SA LATCH)

CLOCK: A3TP7, rising edge (LBIOSB)

VH = 00UP

Node	Signature	Node	Signature
U 11- 5	0019	U 13- 4	00UU
U 11- 7	00P6	U 13- 5	00P6
U 11- 9	007P	U 13- 6	0003
U 11-12	00UU	U 13- 7	007P
U 11-14	0003	U 13- 8	0065
U 11-15	0019	U 13- 9	001A
U 11-16	0065	U 13-11	001A
U 11-18	001A	U 13-12	0065
		U 13-13	007P
U 12- 9	00UU	U 13-14	0003
U 12-10	high	U 13-15	00P6
U 12-12	00UP	U 13-16	00UU
U 12-15	high		

Table 8-14. Signature Analysis Setup H (2 of 2)

Node	Signature
U 15- 3	0019
U 15-17	0019
U 17- 5	00UP
U 17- 8	00P7
U 17- 9	0019
U 27-14	00P7
U 28- 7	high
U 28-10	00UF
U 28-13	009A
U 28-14	00P6
U 28-15	007U
U 30- 3	high
U 34- 4	0000
U 34-13	00P7
U 35- 6	00UU
U 35- 8	0018
U 40- 2	0059
U 40- 3	0039
U 40- 4	0019
U 40- 5	0019
U 40- 6	0019
U 40- 7	0019
U 40- 8	005U
U 40- 9	0019
U 40-11	00UU
U 40-12	00C9
U 40-13	00UU
U 40-14	00UU
U 40-15	00UU
U 40-16	00UU
U 40-17	00HU
U 40-18	00CU

Node	Signature
ON A10 MINI AND RS232	
U 43-11	0041
U 43-12	0021
U 43-13	0001
U 43-14	0001
U 43-15	0001
U 43-16	0001
U 43-17	0047
U 43-18	0001
U 57- 3	003U
U 57-14	00F1
U 57-15	0000
U 57-17	003U
U 57-19	00UP
U 57-22	001U
U 57-23	003U
U 57-24	001U
U 62- 3	0081
U 62- 5	009A
U 62- 7	00F1
U 62- 9	low
U 62-12	00P6
U 62-14	00P6
U 63- 2	0081
U 63- 3	0000

8-48. POWER SUPPLY BLOCK DESCRIPTION.
ASSEMBLY A1.

8-49. The relationships between the power supply functional areas are shown on figure 8-2.

8-50. The Model 64110A uses a switching power supply which provides all other circuits with the following regulated voltages and signals:

+12 volt main supply

+12 volt display driver supply (12VDD)

-12 volt supply

-5 volt supply

-5.2 volt supply

-3.25 volt supply

LPOP, Low power-on pulse

LIR15, Power failure interrupt

LINSYN, Line synchronization

8-51. The power supply contains an overcurrent shutdown, individual overcurrent protection on the -3.25 and -5.2 V supplies, RAM protect, a 40 KHz clock, and control power circuits.

8-52. PRIMARY POWER BLOCK DESCRIPTION. ASSEMBLY A1A1.

8-53. Line voltage, either 110 or 220 V, is supplied through the AC line filter, fuse F1, and the power on/off switch S1, to the line voltage selector AS2.

8-54. The line voltage selector does two things. First, it determines if there will be straight through rectification at 220 V, or rectification with voltage doubling at 110 V. This maintains approximately 160 VDC, switched at 40 kHz, on the primary of the power transformer A2T1. Second, it ensures the primary of T4 sees only 110 V for either line supply voltage.

8-55. CONTROL-POWER BLOCK DESCRIPTION.
ON ASSEMBLY A1A1.

8-56. The power supply control circuitry provides supply and reference power for use in the power supply. Control-power is the first to come up and consists of +12VCONT, +5VREF, and +5VCONT. The power is

continuously available whenever line voltage is supplied to the line voltage selector.

8-57. TEST POINTS AND 40 kHz CLOCK BLOCK DESCRIPTION.
ON ASSEMBLY A1A1.

8-58. Test points VCONTIN and CONTRET provide an access point to apply external power to the control power circuits. This will allow generation of control power without requiring main system power. The 40 kHz clock is generated by two one-shot multivibrators in U5 and is used to set the base frequency of the regulator circuits for the +5, -5.2 and -3.25 V supplies.

8-59. OVERPOWER PROTECTION BLOCK DESCRIPTION.
ON ASSEMBLY A1A1.

8-60. The overpower protection circuit must sense current in order to make a determination of the supply power consumption. The current sensor is transformer T3, which has its primary wired in series with the primary of the power transformer. This current is input to the overpower protection circuit U6, which produces a SHUTDOWN signal and turns on the overpower indicator DS1, when an overpower condition is reached. The SHUTDOWN signal is wire ORed with the other shutdown signals to the +5 V regulator U2.

8-61. +5 VOLT SUPPLY BLOCK DESCRIPTION.
ON ASSEMBLY A1A2.

8-62. This is the dominant supply. Its regulator controls the power to the primary of the power transformer. Therefore, the other lines will go down if the +5 V line goes down.

8-63. The first of four transformer primaries supplies power directly to the fullwave rectifier CR8 which rectifies it to +5 VDC. The +5 V line is filtered by L4 and C10, 11, 23-25 and then regulated at +5 V (+-5%) by regulator A1U2.

8-64. The regulator senses the line level and compares it to the +5V-REF level from the control power circuits. If the level is not correct, the regulator will increase or decrease the duty cycle of the switching transistors A1Q1 and A1Q2 in the primary of the power transformer.

8-65. The regulator circuit A1U2, combines with the overvoltage protection circuits of the supply lines to shutdown the supply in an overvoltage situation. This is accomplished by wire ORing the SHUTDOWN signals of the overvoltage protection circuits to the dead time control comparator input of the +5 V regulator A1U2. When a SHUTDOWN signal is applied to this input, the regulator will turn both switching transistors A1Q1 and A1Q2 off, thus, no power will be supplied to the primary of the power transformer.

8-66. +-12 VOLT SUPPLY BLOCK DESCRIPTION.
ON ASSEMBLY A1A2.

8-67. The fourth secondary supplies fullwave rectifier A1CR1, which supplies approximately 20 VDC to the linear regulators A2VR1, 2 and 3, producing +12 V, -12 V, and +12 VDD, regulated at +-5%. The +12 VDD line supplies the display driver circuits, and the +12 V and -12 V supplies are general purpose supplies for all other circuits.

8-68. RAM PROTECT BLOCK DESCRIPTION.
ON ASSEMBLY A1A2.

8-69. The RAM protect circuit U6 is used to detect the presence of the -5.2 V supply. The -5.2 V supply must be present at any time the +5 and +12 V supplies are supplied to RAM or damage may result to the RAM. If the -5.2 V supply is not present, the RAM protect indication DS3, is lighted and a SHUTDOWN signal is sent to the +5 V regulation circuit A1A2.

8-70. -3.25 VOLT SUPPLY BLOCK DESCRIPTION.
ON ASSEMBLY A1A3.

8-71. The second secondary supplies power through switching transistor Q3, to the -3.25V transformer T1. Rectifier CR2, rectifies the voltage from the -3.25 V transformer which is filtered by L1 and C17-20. The regulator circuit U5 senses the voltage level on the -3.25 V line, monitors the voltage drop across R37 for current levels through the -3.25 V line, compares the levels with the +5VREF and varies the duty cycle of the switching transistor Q3 to maintain -3.25 V (+-3%).

8-72. The overcurrent protection circuit A2U5 senses the -3.25 V and compares it with +5VREF. When an overcurrent condition exists, it lights the -3.25 V overvoltage indicator A2DS2, and sends a SHUTDOWN signal to the +5 V regulator circuit A1U3.

8-73. -5.2 VOLT SUPPLY BLOCK DESCRIPTION.
ON ASSEMBLY A1A3.

8-74. The -5.2 V supply operates the same as the -3.25 V supply and is maintained at -5.2 V (+-5%). It receives its power from the third power transformer secondary through switching transistor Q4, the -5.2 V transformer T2, the fullwave rectifier CR5, and filter circuit L2 and C21-23, 28. The -5.2 V power is sensed by R40 and regulator U2.

8-75. Overcurrent protection is provided by A2U4 which lights the -5.2 V overcurrent indicator A2DS1, and sends a SHUTDOWN signal to the +5 V regulator A1U2.

8-76. LPOP, L1R15, AND LINE SYNC BLOCK DESCRIPTION. ON ASSEMBLY A1A2.

8-77. The power supply produces three signals to be used by the other circuits; LPOP, LIR15 and LINSYN. LPOP is generated when power is first turned on and whenever there is a power failure on the AC line or +5 V supply. This signal goes to the CPU and I/O section where it initializes the CPU and I/O circuits.

8-78. LIR15 is generated when line voltage drops below a set value and goes to the CPU/IO and display driver sections. It blanks the display and aborts any writes to the floppies. LINSYN is a TTL signal generated from the line frequency and goes to the CPU and I/O section where it is used in the auto-reset circuitry.

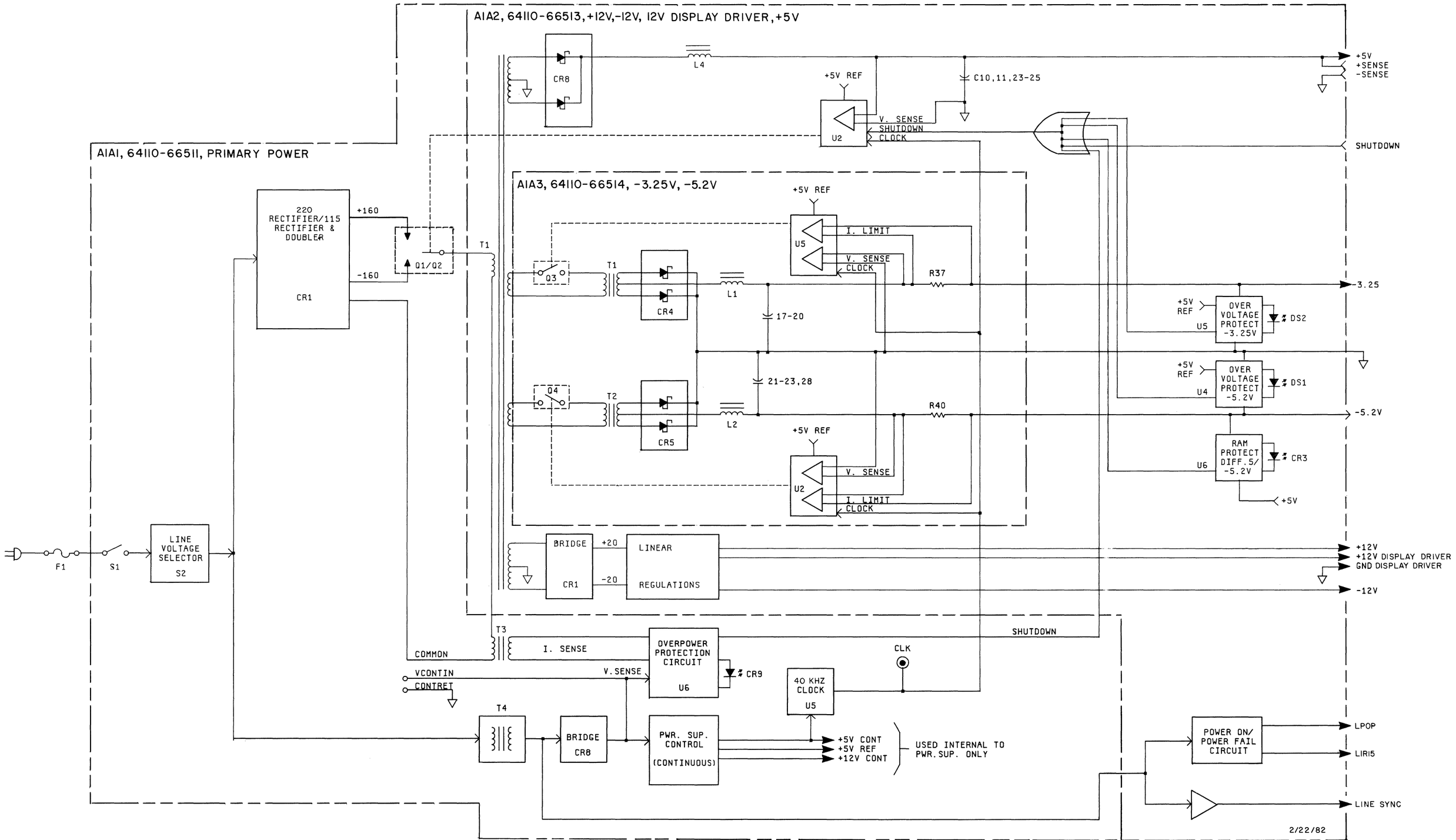


Figure 8-2.
Power Supply Block Diagram

8-79. POWER SUPPLY SCHEMATIC DESCRIPTION.
ASSEMBLY A1.

8-80. General.

8-81. The power supply assembly schematic functionally corresponds to the power supply block diagram (figure 8-2). The four boards which make up the power supply are shown on the schematic, service sheet number 1 (figure 8-3).

Description	Ref Des	64110-Number	Location
Primary	A1A1	66511	Top of chassis
+5, +-12 Volt	A1A2	66513	Middle of chassis
-3.25, -5.2 Volt	A1A3	66514	Bottom of chassis
Interconnect	A1A4	66512	Side of chassis

8-82. The line voltage is fed through the AC line filter, fuse, and power switch. Capacitor C27 provides additional RFI filtering. Thermistor RT3 nominally keeps any peak in-rush currents below 100 amperes to protect the power switch. The voltage select switch has two positions selecting 110 or 220 volt input.

8-83. The line selector switch effectively reconnects the input bridge from full wave configuration in the 220 mode to a half wave doubler configuration in the 110 mode. The line filter is a modular unit which starts to provide effective filtering at frequencies above 150KHz.

8-84. PRIMARY SUPPLY SCHEMATIC DESCRIPTION.
ASSEMBLY A1A1.

8-85. Assembly A1A1 is the primary power supply board. It sets up correct primary voltages and supplies the current drive to the primaries of A2T1 and T2 through a 40 kHz pulse width modulated switching network.

8-86. Diode CR4 is a full wave rectifier bridge that supplies power to the main energy storage capacitors C23 and C24 to develop the primary supplies. Resistors R31 and R32 are 100 k ohm bleeder resistors for the main capacitors.

8-87. Spark gaps SG1 and SG2 in series with thermistors RT1 and RT2 provide a non-destructive means of catching incorrect strapping on the power supply input. In the event that the supply is connected for 110 volt operation and plugged into 220 volt main, one or both of the spark gaps will fire and discharge the energy.

8-88. Transformer T1 and C25 are a common mode filter, and C26, C29 and L1 are a CLC filter. Both provide filtering at a lower freqency than the input modular line filter.

8-89. The main power switching transistors Q3 and Q4 are connected across the half bridge capacitors C28, C30. The two transistors turn on alternately, causing current to flow in alternate directions through the primaries of T2 and A2T1, thus supplying power for the supplies. The main power transistors have diodes CR5, CR6 across the collector/emitter junctions to insure the storage energy in any leakage inductance in the primaries of T2 and A2T1 will be returned to the energy storage network.

8-90. The +5 V supply is regulated by controlling the duty cycle on-time of the 40 kHz switching transistors. Chip U2 monitors the +5 V supply and compares it to the +5 V reference via the voltage sense amplifier. The pulse width on output pins 8 and 11 increases as the voltage differential on the voltage comparitor increases. The +5 V reference comes from VR3 on the A1A1 primary board. Resistor R16 and C7 filter noise, and R15 compensates for the input bias current for the voltage sense amplifier. The +5 V sense is detected at the motherboard to help compensate for printed circuit board trace voltage drops. Ten ohm resistor R1 on the A1A4 interconnect board provides +5 V sense when the supply is removed from the mainframe. Resistor R17 and C8 filter noise and R13 compensates for the input bias current.

8-91. The open collector outputs of U2 turn on and off the darlington pair devices U4 which cause current to flow in the primaries of T4 and T5. Transformers T4 and T5 comprise the base drive circuitry for the power switches Q3 and Q4. The primary windings of T4 and T5 are connected in such a polarity that when primary current is forced to flow by the darlington switches U4A/BC, the respective power switch base is driven off. These transformers are actually energy storage elements. During the time that the drive transistors are turned on, each transformer stores energy which is later released into the secondary when the darlington switches are turned off. On the primary, components R27, C19, R28 and C18 form what is called a snubber network to reduce RF interference problems.

8-92. The other two darlington pair devices U4 are driven by signals CC1 and CC2, Cross Conductor 1 and 2. During heavy load situations when the switching transistors are on for full duty cycle, stored charge could keep one switching transistor turned on when the other is turning on. This would have the effect of shorting the two primary supplies together thus destroying components. Signals CC1 and CC2 keep one switching transistor turned off until the other is completely turned off.

8-93. The +5 V current being supplied to the instrument is sensed by monitoring the voltage across the +5 V inductor A2L4. This voltage is supplied to the current limit amplifier sense input of U2. When this voltage becomes large enough, the current limit amplifier of U2 begins to limit the duty cycle on the +5 V supply. The current limit foldback point is 33-35 amperes.

8-94. Integrated circuits U5A/B are two halves of a monostable multivibrator connected in a loop. It is the 40 kHz clock for the power supply. The clock is low true with a very short duty cycle. Its frequency of operation is determined by R25 and C17 connected to pin 15 of U5A and R26, C32 connected to pin 7 of U5B.

8-95. Resistor R11 and C5 provide the soft start at power-up. Pin 4 of U2 is the dead time control input. This input controls the maximum on-time of the output pulse. Until C12 has discharged to approximately 100 mV, the dead time control comparator is limiting the maximum pulse width, thus causing the pulse width to increase gradually, causing the supply to come-up in a slower manner.

8-96. Transistors Q2 and Q1 and their passive components form a discrete SCR which latches or triggers when current is sunk through R1 to ground. This circuit latches whenever sufficient current is sunk through R1 to ground. The input side of R1 is clamped to 5 volt control supply. The input current is limited by R4 and noise on the input line is filtered by C2.

8-97. Chip U1 and its associated components provide low voltage lockout to U2. Until the 12 volt control power supply is above 11 volts, it keeps the VCC line to U2 off. If the 12 V control power drops below 10 V, U1 shuts down power to U2. It also resets the dead time control circuitry via R8 and CR3 to ensure that if power is being cycled rapidly, the supply will still come up slowly. Resistors R5, R6 and R7 set the trip point for U1.

8-98. Network R13, R15 and C8 provide some input filtering against 40 kHz noise on the error sensing line. The reference line includes filtering in the form of R15, R16, and C7 to reduce susceptibility to noise. Resistors R13 and R15 balance the input bias current and set up the AC gain.

8-99. Chip U3 is the clock receiver circuit. It is a 311 OP AMP arranged with its passive components R23, R24, R9, and C14 to set up the clock threshold voltage at 2.5 V. The input of U3 is clocked by the 40 kHz generator U5A/B. The output of U3 is directly across U2 timing capacitor C12 to provide a discharge path, thus setting the switching rate of 40 kHz.

8-100. +5, +-12 VOLT SUPPLY SCHEMATIC DESCRIPTION. ASSEMBLY A1A2.

8-101. Assembly A1A2 generates +5, +-12, +12 VDD supply voltages along with LINSYN to the processor. It also generates the LPOP signal which resets the processor and low line signal LIR15.

8-102. Signal LINSYN input comes from A1T3. In this case, one of the secondary lines is connected to a resistive voltage divider R17 and R25 whose output is clamped to ground and to the 12 V control voltage. That line then becomes one of two inputs to the Schmitt input gate U2C with the other input held high. The output is then nearly square with

a 60 Hz period. The output drives the base of Q2. Transistor Q2 collector is pulled up to 5 volts through R27. That collector signal then becomes the LINSYN output.

8-103. Part of the main power transformer T1 is used for generating the +5 V supply. Diodes CR8, CR19, CR20 make up a full wave center-tapped bridge rectifier. Components L4 and five 1000 uF capacitors, C10-11 and C23-25, make up the +5 V supply filter. In addition to conventional components, a pair of diodes CC1 and CC2 are provided in order to sense potential for cross-conduction and to hold the main power switching devices off until conduction due to storage time in the main switches Q1 and Q2 has ceased. These two diodes also have pull up resistors R32, R33 in order to reduce any storage time problems associated with the darlingtons A1U4A/BCD, which they control.

8-104. Part of the main power transformer T1 is used to generate +12 V for the display driver, +-12 V supplies for other loads. The supplies are fed from T1 through a fast recovery bridge rectifier CR1. The +12 VDD supply is separate from the main +12 V output because of the sensitivity of the display driver circuitry to noise. Voltage regulator VR1 (+12VDD) regulates the +12 V for the display driver. Its filtering is done through L1, C4 and C6. Diode CR12 and CR13 are placed in the circuit for reverse polarity protection in case of a short.

8-105. Voltage regulator VR2 regulates the -12 V main supply and its filtering is done through L2, C5 and C7. Diodes CR14 and CR16 are the reverse polarity protection diodes. Voltage regulator VR3 regulates the main +12 V supply. The filter network consist of L3, C8 and C9. Diodes CR15 and CR17 are the reverse polarity protection diodes for this circuit. All three outputs are routed to the A1A4 interconnect board and out to the instrument.

8-106. Chips U5 and U4 are used to sense -3.25 and -5.2 V overvoltage. IC U6 is used to sense the condition when +5 V is available and -5.2 V is not. The availability of +5 V without -5.2 V could cause damage to the RAM circuitry of the peripheral processor memory. Once a shutdown is activated, a divider network drives the remote activate input to the shutdown ICs and a LED. The shutdown is then latched and requires a power-on reset.

8-107. The LED provides a visual indication of the failure mode. The shutdown signals go to the A1A1 board where they shut down the main switching transistors via the switching regulator A1U2. The overtemperature thermostats provided in the power supply utilize U4. They latch U4 in the shutdown mode, thus keeping the supply from turning on again when it cools. Therefore, LED DS1 indicates either a -5.2 V shutdown or temperature shutdown.

8-108. Integrated circuit A1U6 is part of the overcurrent detector. Transformer A1T2 is the overcurrent transformer and is connected in series with the main power transformer primary of T1. The secondary of A1T2 contains a full wave bridge A1CR7, and a filter network A1R36 and C34. In the event that the voltage at pin 2 of A1U6 exceeds the trip point of 2.6 volts, it will issue a shutdown signal to the A1A1 board and latch itself. In addition, LED A1A1DS1 will come on and stay on

indicating that the shut down mode was due to an over power condition.

8-109. LINSYN is a TTL level square wave signal generated by U2C and Q2 running at line frequency. Chip U2 is driven by line voltage transformed down to CMOS levels by A1T3. Diodes CR3 and CR4 clamp the inputs to the CMOS gate U2 to +12 V and ground to keep line transients from damaging the IC.

8-110. Signals LPOP and LIR15 are generated through U1 from the A1T3 secondary. Full wave bridge CR2 output is divided and filtered to drive U1 which provides low-line indication. Whenever the line voltage drops into the low-line region, it sets the RS flip-flop U2A/D. At power-up, the state of the flip-flop is reset. As long as that is true, U2B output can not go low until time-out of the input pin 6 of U2B, which is set by R21 and C16. Therefore, about one second after +12 V main power supply output is up, pin 4 of U2 will go low. That low signal will be coupled through C17 and will drive the output of U3A high for about 70 microseconds which will in turn drive the LPOP line low for about 70 microseconds.

8-111. The circuit also interlocks the timing between an LIR15 low true output and any subsequent LPOP signal following restoration of power. If the input line voltage drops below acceptable limits for a very brief period of time, the flip-flop will be delayed by about 100 microseconds. Therefore, no LPOP will be delivered any closer to the LIR15 negative edge than 100 microseconds. That timing is required by the central processing unit.

8-112. Voltage regulators A1VR1 (+12 V control), VR2 (+5 V control), and VR3 (+5 V reference), supply the control voltages that enable the power supply to start-up and shut-down in an orderly way. Regulator VR3 supplies the precision +5 V reference so that no adjustment for the +5 V supply is needed. The input for the regulators comes from A1T3 and a full wave bridge A1CR8. The filter capacitors A1C13, C15, C16, C35, and C37 provide high frequency stability.

8-113. -3.25, -5.2 VOLT SUPPLY SCHEMATIC DESCRIPTION.
ASSEMBLY A1A3.

8-114. The A1A3 board generates the -3.25 and -5.2 V supplies. The two supplies are pulse width modulated switching supplies similar to the +5 V supply. Power for these switching supplies comes from the secondary coils of the +5 V primary transformer A2T1. For this reason, the +5 V supply must be regulating for a minimum load before the -3.25 and -5.2 V supplies can regulate.

8-115. The -3.25 volt supply is generated through CR4, A2T1, and the power switching transistor Q3. Transistor Q3 is a FET power switch. The FET switch is driven by a 40z kH signal from the pulse width modulator U5 control regulator via Q2 and U1A. The FET switch provides the power drive to the primary of T1. The secondary of T1 feeds the -3.25 V supply filter network L1 and C17-20.

8-116. The power switch contains a snubber network consisting of C24 and R38. Resistor R45 provides turn off stability. Resistor R30 insures the FET is protected in the event that the drive crcuitry is removed from the board. The -3.25 and -5.2 V outputs are fed through transformer T1 to the filter network L1, C17-20.

8-117. The -5.2 V supply is set up like the -3.25 V supply. The passive components are of different values for the different voltage outputs of two supplies. The -5.2 V circuit consists of CR5, Q4, T2, L2, C21-23, C28. Chip U2 is its control regulator and functions the same as U5 but have different clocking signals. The timing control is C11, R24 (for U5) and C6, R17 (for U2). The timing is set up so that the external clock signal always overrides and provides the reset. The controller incorporates fold back current limit which is set at just above 20 amperes. Both controllers use remote sensing to the output voltage. A separate sense line is brought out to the mother board distribution bus.

8-118. Both supplies' modulating regulators have a clock network similar to the +5 V supply. The 40 kHz clock signal from the clock circuitry on the A1A1 primary board overrides and resets the timing capacitors on pin 5 of the regulator ICs to set the pulse width modulated signal at 40 kHz.

8-119. The voltage sense for the voltage sense amplifier for the regulator ICs are remotely sensed at the motherboard. The 10 ohm resistors A3R43 and A3R44 insure that the supply is still functional in the event that the supply is removed from the mainframe.

8-120. As in the +5 volt regulator there are some additional capacitors C31 and C32. These capacitors in combination with C30 and C33 provide rejection of 40 kHz noise. Tight tolerance resistors are used to insure the input reference quality is maintained. Both U2 and U5 have conventional RC compensation networks.

8-121. Components C1, C7-8, C12-14, C29, R8, R14, R42 are simply filtering for the +12 V control power supply and the +5 V reference supply.

8-122. POWER SUPPLY TROUBLESHOOTING.

8-123. Power Supply troubleshooting consists of failure modes and suggested steps to take in troubleshooting. When a failure is isolated to a block of components, refer to the theory and troubleshoot those components.

```
****************************** WARNING ******************************
*                                                                    *
*  Hazardous voltages and charges exist on the power supply.         *
*  The main filter capacitors take approximately 2 minutes to        *
*  discharge after line power is removed from the supply. Use        *
*  tool to discharge the main filter capacitors before servic-       *
*  ing.                                                              *
*                                                                    *
**********************************************************************
```

8-124. Remove the power supply from the mainframe and install the power supply test board. It contains minimum loads required to bring the 12V supplies into full regulation and LED indicators to indicate operation of the different supplies. Removing the supply from the mainframe will verify that the failure is with the supply and not with the mainframe motherboard or boards installed in the frame.

8-125. The A1A2 and A1A3 boards may be extended using the power supply flexible extender cable. The A1A1 board should be left in the supply frame during troubleshooting because of the hazardous voltages and charges present on the primary rails.

8-126. FUSE IS BLOWN.

8-127. Line voltage is rectified by A1A1CR4 and filtered to develop the primary rails. Shorts in the rectifier or filter components will cause the fuse to blow.

8-128. A1A1Q3 and 4 are the main switching transistors. The control network for these transistors should never turn on both at the same time. If it does, the primary rails will be shorted together, the fuse will blow and Q3 and 4 will be destroyed.

8-129. If A1A1Q3 and 4 are found bad, use the troubleshooting outlined in the 5V supply control circuitry troubleshooting to isolate any problems there before turning on the supply in a fully functional mode.

8-130. If the supply fails intermittently under heavy loads where A1A1Q3 and 4 fail, check the cross conduction diodes A1A2CR19 and 20. The signals CC1 and CC2 are supposed to keep the transistors from turning on at the same time when stored charge is holding on one of the transistors.

8-131. There are three LED indicators on the A1A2 board and one on the A1A2 board to indicate shutdown modes of the power supply.

8-132. LED A1A1DS1 ON.

8-133. This LED indicates that the power supply was shut down due to an overpower condition. The possible reasons for this and suggested troubleshooting steps are listed below.

8-134. A1A1Q3 and 4 turned on at the same time. Use the troubleshooting outlined in the 5V regulator control circuitry troubleshooting to isolate possible problems there.

8-135. A short on circuitry on the secondaries of A1A2T1, A1A3T1 or T2 may be translated back through the transformers and cause the shutdown due to overpower. The secondary windings of A1A2T1 connect via cables and connectors. These may be disconnected to isolate which of the secondaries is causing the heavy load. Disconnecing A1A3J1 will cause the RAM protect shutdown to shut down the supply. Disconnecting A1A2J1 will remove power from the plus and minus 12V and 12V display supplies. Check for shorted components.

8-136. LED A1A2DS1 ON.

8-137. The LED indicates either a -5.2V overvoltage or a thermal shutdown or an overvoltage of the 5V reference volatage. If either of the thermal switches close due to an overtemperature condition, A1A2U4 is used to latch the shutdown so that the supply remains shutdown until power is cycled even if the supply has cooled. If the -5.2V supply becomes more negative than -6.47 volts, or the 5V ref becomes more positive than 6.27 volts, U4 issues a shutdown signal, lights LED DS1 and latches itself.

8-138. Disconnect A1A2J2 and check the thermal switches.

8-139. Remove A1A2U4 to disable the shutdown. Check the -5.2V and 5V ref supplies to isolate which is failing. The 5V ref supply is a voltage regulator IC located on the A1A1 board. Use the regulator control troubleshooting to troubleshoot the -5.2 volt supply.

8-140. LED A1A2DS2 ON.

8-141. The LED indicates a -3.25 overvoltage or 5V ref. overvoltage shutdown. If the -3.25V supply becomes more negative than -4.2 volts or if the 5V ref. supply becomes more positive than 6.0 volts, A1A2U5 issues a shutdown signal, lights LED A1A2DS2, and latches itself to keep the supply shut down.

8-142. Remove A1A2U5 to disable the shutdown. Check the -3.25V and 5V ref supplies to isolate which is failing. The 5V ref supply is a voltage regulator IC located on the A1A1 board. Use the regulator control troubleshooting to troubleshoot the -3.25 volt supply.

8-143. LED A1A2DS3 ON.

8-144. The LED indicates a RAM protect shutdown. If the 5V supply is present without the -5.2 supply, or if the difference between the two supplies becomes too great, the RAM may be damaged. If the -5.2V supply becomes more positive than -2.7 volts, or if the 5V supply becomes more positive than 6.1 volts, A1A2U6 issues a shutdown signal, lights LED A1A2DS1 and latches itself to keep the supply shut down.

8-145. Remove A1A2 U6 to diable the shutdown. Check the 5V and -5.2V supplies to isolate which is failing, and troubleshoot the appropriate supply using the regulator control troubleshooting.

8-146. CONTROL REGULATOR TROUBLESHOOTING.

8-147. Disconnect A1A1J4. This will open the connection between A1A1Q3 and Q4, and remove the power drive for the primary of A1A2T1, thus removing the chance of shorting the primary rails together if Q3 and Q4 should turn on together. Removing the drive from the primary of T1 will cause the supply voltages to never come up so that the regulator ICs will run at full duty cycle.

8-148. Check the output waveforms of the regulator ICs. If they are correct troubleshoot the darlington pairs and the associated drive circuitry for the switching transistors. If these are okay, suspect the switching transistors.

8-149. If the output waveforms of regulator ICs are not correct check the inputs as outlined below.

8-150. Check the 12V supply voltage for the regulator IC. A1A1U2 is responsible for the supply voltage for A1A1U2. It does not apply the supply voltage to U2 until the control voltage has reached 11 volts and on power down disables the supply voltage to U2 when the 12 volt control voltage has dropped below 10 volts. The supply voltage for the other regulator ICs comes from the 12V control regulator A1A1VR1 with some additional filtering capacitors on the A1A3 board. (12 Volt control 11.5 to 12.5 volts.)

8-151. Check the 5 volt reference voltage. It is supplied by voltage regulator A1A1VR3. (4.975V to 5.025V)

8-152. Check the current limit Amp inputs. Pin 15 should be at 5 volts, pin 15 should be less than 5 volts. An error here could indicate an failure in U2 reference voltage output, or a possible short on the output filtering capacitors for the 5V supply.

8-153. Check the clock input waveform on pin 5. Trace the waveform to the clock generator circuitry A1A1U5 to troubleshoot.

8-154. Check the dead time control input pin 4. This should be low. If it is high, check for a shutdown signal. If there is no shutdown signal, troubleshoot the discreet SCR A1A1Q1 and Q2.

8-155. PROCEDURE FOR USING THE POWER SUPPLY TEST BOARD 64110-66519.

8-156. First, verify that all green LEDs are lit signifying that all supplies are operational.

8-157. Second, verify that all power supplies are in spec at the test points on the test board.

Table 8-15. Power Supply Test Point Specifications

Supply	spec
5 volt	4.75-5.25
12 volt	11.4-12.6
-12 volt	-11.4-(-12.6)
12 volt display	11.4-12.6
-3.25 volt	-3.153-(-3.347)
-5.2 volt	-4.94-(-5.46)

8-158. Third, verify that all supplies are in spec at full load by pressing one load switch at a time. (5V load switch must be pressed simultaneously with each of the other loads to insure adequate duty cycle for the main switcher.)

Table 8-16. Power Supply Load Specifications

Supply	spec
5 volt	4.75-5.25
12 volt	11.4-12.6
-12 volt	-11.4-(-12.6)
12 volt display	11.4-12.6
-3.25 volt	-3.153-(-3.347)
-5.2 volt	-4.94-(-5.46)

8-159. Remove the RAM protect shutdown IC A1A2U6 and Check the -3.25 and -5.2 volt supply current limit by pressing the +5, -3.25 and -5.2 volt load switches simultaneously and checking the voltage at the -3.25V and -5.2V test points. The voltage at the -3.25V test point should be less than or equal to 1.8 volts in magnitude. The voltage at the -5.2V test point should be less than or equal to 1.4 volts in magnitude.

8-160. Fourth, verify the RAM protect shutdown by pressing the RAM protect test switch on the test board.

8-161. POWER SUPPLY SIGNATURE ANALYSIS.

There are no signature analysis loops for the power supply.

NOTES

NOTES

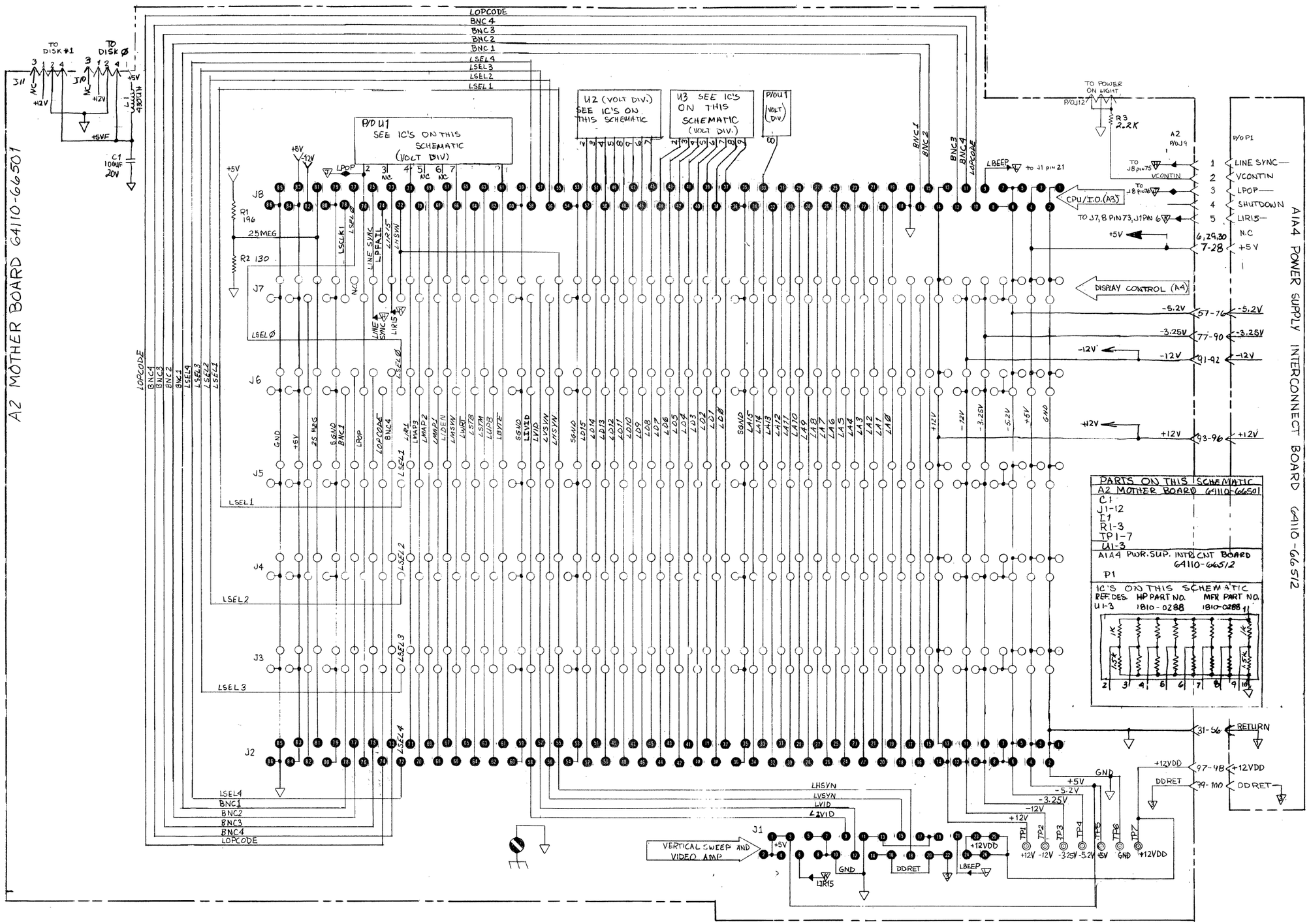


Figure 8-4.
Motherboard Schematic
8-59/(8-60 blank) PS

8-162. CPU/IO BLOCK DESCRIPTION.
ASSEMBLY A3.

8-163. The relationships between the CPU/IO functional areas are shown on figure 8-5.

8-164. CENTRAL PROCESSING UNIT BLOCK DESCRIPTION.

8-165. The microprocessor CPU controls data and addresses on both the CPU bus and the input/output bus. The CPU clock generator develops LPHI1 and LPHI2.

8-166. LOW POWER-ON PULSE GENERATOR BLOCK DESCRIPTION.

8-167. The Low Power-on pulse generator (LPOP) syncronizes LPOP with LPHI1. The generator also insures that any pulse from LPOP has a minimum pulse width of approxitmately 35 ns.

8-168. MEMORY BUS TIMING BLOCK DESCRIPTION.

8-169. The Low upper byte, P/O memory bus timing indicates to the device being addressed if the information on the data bus is the upper or lower byte of a word. Low byte, P/O memory bus timing indicates to the device being addressed if the word on the data bus is eight or sixteen bits.

8-170. The memory bus timing develops the control signals necessary for the CPU to communicate with the device connected to it via the CPU memory bus, ie. ROMs, option cards, display controller and RAM, etc.

8-171. ADDRESS LATCH BLOCK DESCRIPTION.

8-172. The address latch latches the address from the multiplexed instruction/data/address bus. The information on the output of these latches produce the CPU memory address bus.

8-173. ROM DECODING BLOCK DESCRIPTION.

8-174. ROM decoding decodes the CPU address bus allowing the CPU program counter to select the various ROMs for execution of software.

8-175. I/O BUS BLOCK DESCRIPTION.

8-176. The CPU communicates with the I/O circuits primarily via the I/O bus. This bus is a traditional bus in that it carries data, address and control information. The data bus is a 16-bit bidirectional bus that carries data to and from the HP-IB interface chip, the RS-232C interface chip, and the low priority interrupt circuit. This bus also receives data from the keyboard circuits and switch mode status

from the RS-232 circuits.

8-177. The address portion of the I/O bus consists of 4-bits of peripheral address (LPA0-LPA3). These bits allow up to 16 peripheral addresses to be decoded (by the peripheral address decoder) which allows the CPU to select the various I/O circuits it wants to talk to. However, only 9 of the possible 16 peripheral addresses are used in the 64110 system. See table 8-17.

Table 8-17. I/O Internal Addresses

MNEMONIC		FUNCTION
PA0	LDYBD	Keyboard
PA2	L(DELTA)T	Auto-reset timer clear
PA5	LRS232WR	Serial interface write
PA6	LRS232RD	Serial interface read
PA7	LHP-IB	Rear panel board, HP-IB
PA9	LBEEP	DSA latch, beeper, display enable
PA10	LSLOT SEL	Bank switching, slot select latch
PA12	LINT MASK	Interrupt mask
PA15	LIRHCLR	Clear high order interrupt

8-178. PERIPHERAL ADDRESS DECODER SCHEMATIC DESCRIPTION.
FIGURE 8-13; U12, U28.

8-179. Decoders U12 and U28 decode one-of-eight lines each (for a maximum capability of 16 lines) depending on the states of the three binary select inputs (pins 1, 2, and 3) and the three enable inputs (pins 4, 5 and 6). The same address inputs can be used for both decoder chips because only one chip is enabled at a time. This is implemented by feeding peripheral address signal LPAB3 to the low true enable input of U12 and to the high true enable input of U28. This means that U12 and U28 are never enabled at the same time. Also, note that pin 4 of U28 is tied to ground thus requiring that only pins 5 and 6 be low for U28 to be enabled.

8-180. Although U12 and U28 have the capability of decoding up to 16 lines, only 9 are used in the current 64110 system application. Five of the peripheral addresses LKYBD, L(DELTA)T, LRS232RD, LRS232WR, and LHPIB are produced by U28 and the remaining four addresses LBEEPEN, LSLOT SEL, LINT MASK, and LIRH are produced by U12.

8-181. PERIPHERAL DECODER ENABLE LOGIC SCHEMATIC DESCRIPTION.
FIGURE 8-13, U34B/CD.

8-182. The I/O strobe (LBIOSB), Interrupt (HINT), Data Out Delayed (HDOUTD), and Data Out (LDOUTB) commands from the CPU are ANDed by U34C,D and then NORed by U34B to produce an enable signal for enabling Peripheral Address Decoders U12 and U28. This enable signal appears at output pin 4 of U34B and is fed to gate input pin 5 of both U12 and U28 (note, however, that the two other gate inputs to U12 and U28 must

also be of the proper state). Table 8-18 is the truth table for the Decoder Enable Logic.

Table 8-18. Decoder Enable Logic Truth Table

LIOSB	LDOUT	LINT	LDOUTD	U34B
0	0	X	X	0
X	X	1	1	0
U34B = 1 for all other combinations				

8-183. SA INTERVAL, CARD ID ENABLE BLOCK DESCRIPTION.

8-184. In addition to the nine peripheral addresses, there are two interface control addresses (LIC1 and LIC2) that the CPU uses to control the signature analyzer start/stop signals (SA interval) and the card ID address decoder. This latter circuit produces the ID enable signal (LID) that is distributed to each of the option card slots where it enables the various option PC boards to communicate their unique identification codes to the CPU.

8-185. LOW PRIORITY INTERRUPT MASK BLOCK DESCRIPTION.

8-186. The low priority interrupt circuitry is a series of gates and latches. By generating a particular peripheral address (LINT MASK and other I/O read/write control signals), the CPU can turn on I/O data buffers, write an interrupt mask into this logic, and then the low priority interrupt (LIRL) will only be generated when one of the enabled (unmasked) circuits requests an interrupt. When this happens, the CPU again enables I/O data buffers and reads the Interrupt ID to determine which circuits have requested the interrupts. Once it determines this, the CPU then writes out another peripheral address to the device to service the circuit that requested the interrupt.

8-187. HIGH LEVEL INTERRUPT LATCH BLOCK DESCRIPTION.

8-188. Whenever power is about to fail, the Power Supply sends interrupt request signal LIR15 to the high priority interrupt latch. This produces high priority interrupt request HIRH which is sent to the CPU to inform it that power is failing. The CPU then responds with the appropriate address code for generating the power fail set peripheral address (LIRHCLR) to clear the high priority interrupt.

8-189. AUTO-RESET BLOCK DESCRIPTION.

8-190. This circuit produces the power-on signal (LPOP) whenever either of two events occur: (1) when the delta-time counters are allowed to time-out due to the CPU taking too long to respond to the sync-pulse interrupts, and (2) when the processor reset switch is

pressed. The delta-time feature maybe disabled by the auto-reset enable jumper.

8-191. MEMORY MAPPED I/O CARD SELECT AND BANK SWITCHING CONTROL BLOCK DESCRIPTION.

8-192. This circuitry provides the ability to select each of the option cards occupying any of the 5 option card slots. This is accomplished by decoding four I/O data bits from the CPU (the other two bits are for enabling the decoder chip). When the CPU writes or reads from an address in the range reserved for the option slots, LA14 and LA15 from the memory address bus enable the card select decoder. Each of these 5 cardslot select signals (LSEL0 thru LSEL4) is routed to a specific card slot in the cardcage where it causes that particular card slot to be enabled.

8-193. HP-IB CONTROL, BLOCK DESCRIPTION.

8-194. The PHI chip and associated circuitry allows the CPU to communicate over the HP-Interface Bus (HP-IB) with peripheral devices that are designed to be compatible with the IEEE 488 general purpose interface bus. However, since the 64110 operating system software incorporates instruction code only for the HP disc drives and the HP 2631A and 2608 line printers, these are the only peripheral devices that can be driven from the HP-IB bus.

8-195. HP-IB INTERFACE BLOCK DESCRIPTION.

8-196. The acronym PHI stands for Processor to HP-IB Interface. This chip is a self-contained microcontroller that adapts a wide variety of microprocessor chips to the HP-IB bus. Some of the general characteristics of the PHI chip are:

a. Data is sent at the rate of the slowest listener, up to one megabyte per second.

b. Data transfer is a asynchronous.

c. More than one peripheral device can accept data simultaneously.

8-197. To ensure that the transfer of data is accomplished in an orderly manner, a set of three handshake signals are used: Data Valid (HDAV), Ready for Data (HRFD), and Data Accepted (HDAC). These three handshake signals ensure that each listener is ready to accept data, that the data on the data bus in valid, and that the data has been accepted by all listeners.

8-198. HP-IB BUFFER BLOCK DESCRIPTION.

8-199. HP-IB Data XCVRS, the transmit control signals from the PHI chip, are buffered and inverted before being sent to the HP-IB data transceivers. These signals control channel selection and the direction of data flow thru the data transceivers. The HP-IB data transceivers are bidirectional and handle three types of signals: HP-IB data, handshake, and bus management.

8-200. The HP-IB data consists of instructions and data that are passed back and forth between the CPU and the peripheral devices on the HP-IB bus (i.e., printer or disc). The handshake signals were discussed above and are used to control and coordinate the transfer of data. The bus management signals consist of five control/status signals that are used for such things as activating all peripheral devices at the same time, clearing the interface, service request, etc.

8-201. RS-232C PORT BLOCK DESCRIPTION.

8-202. This circuitry allows the CPU to communicate over the RS-232C serial interface bus to peripheral devices. It is located on the local mass storage device. Refer to the local mass storage appendix of the manual.

8-203. KEYBOARD BLOCK DESCRIPTION.

8-204. The keyboard is composed of two basic blocks, the keyboard-scan circuitry and the keyboard. The keyboard-scan circuitry is found on the CPU/IO board; it scans the keyboard to detect key changes and status. The keyboard is a switch matrix. The columns and rows are continually scanned, and if a key is depressed, a HKYDET signal is generated for use by the scan circuitry.

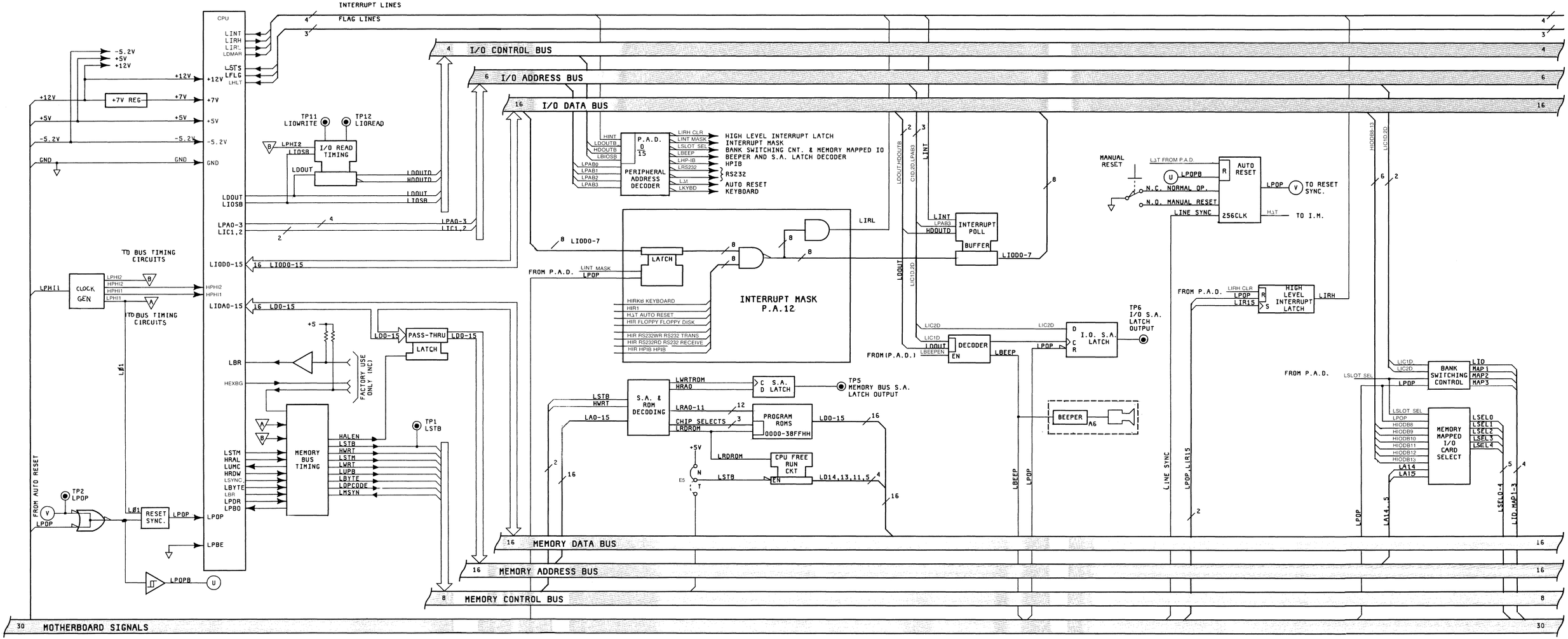


Figure 8-5.
CPU/IO Block Diagram
8-67/(8-68 blank) CI

8-205. CPU/IO SCHEMATIC DESCRIPTION.

8-206. The following paragraphs describe functions shown on the CPU/IO schematics, figures 8-12 through 8-19.

8-207. CPU SCHEMATIC DESCRIPTION.
FIGURE 8-12.

8-208. The microprocessor used in the Model 64110A mainframe is made by Hewlett-Packard. The microprocessor can be thought of as two microprocessors combined on one substrate. First, the basic microprocessor, called the CPU processor, has a 16 bit bidirectional bus with the data and address time multiplexed. The 16 bit bus is demultiplexed into a 16 bit data bus and a 16 bit address bus. The data bus, address bus, and some control lines, (e.g., LWRT, LSTB, etc.), are called the CPU memory bus. The CPU memory bus is distributed throughout the mainframe over the mother board.

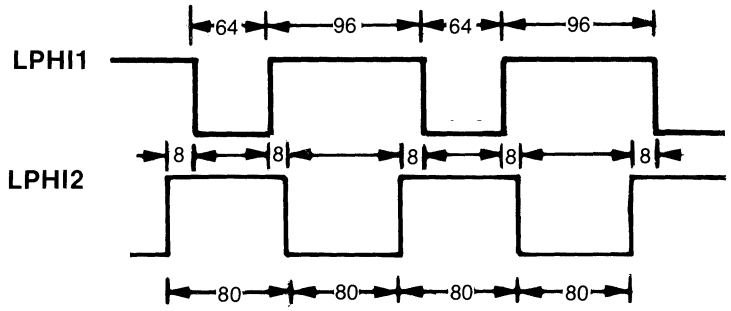
8-209. The second half of the microprocessor is called the input-output processor. The I/O processor has a 16 bit bidirectional data bus, with a 4 bit address bus. Along with the 4 bit address bus, there are two other control lines that can be used to expand the I/O address bus. In addition there are control lines that are independent of the CPU control lines. The I/O data bus, address bus, and I/O control lines form the I/O bus.

8-210. CPU POWER SUPPLY SCHEMATIC DESCRIPTION.
FIGURE 8-12.

8-211. The CPU requires +5 V, -5.2 V, +12 V, and +7 V. The +7 V supply is derived from on board regulator VR1, that is supplied by +12 V.

8-212. CLOCK GENERATOR SCHEMATIC DESCRIPTION.
FIGURE 8-12.

8-213. Clock generators U79 and U78B/CD develop LPHI1 and LPHI2. See figure 8-6. The Clock is derived from the 6.25 MHz signal LSCLK1 on the display control board. LPHI1 and LPHI2 are nonoverlapping signals.



NOTE: TIMES ARE IN NS.

Figure 8-6. CPU Clock Generator Timing

8-214. LOW POWER-ON PULSE GENERATOR SCHEMATIC DESCRIPTION. FIGURE 8-12.

8-215. Chips U57B, U60B/C, U61A, U76C, and P/O U77 form the low power-on pulse syncronizer. The circuitry synchronizes LPOP with LPHI1, and ensures LPOP has a minimum pulse width of approximately 35 ns. LPOP is generated by the power supply (and the CPU/IO board in the event the system becomes lost in its software). In either case, LPOP will cause the CPU to be initialized.

8-216. MEMORY CYCLE TIMING SCHEMATIC DESCRIPTION. FIGURE 8-12.

8-217. Chips U55A/B, U56A, U57A, U58B, U59, U60D, U65A/B, U74, and U76A/B develop the signals necessary for the CPU to communicate with the devices connected to it, i.e., ROM, PROM programmer, display controller, etc. These signals are developed from LPHI1, LPHI2, and five signals from the CPU; HRAL, LSTM, LPDR, HSYNC, and HRD. The timing relationship of the signals needed for the CPU communications are shown in figures 8-7 and 8-8. An explanation of each of these signals may be found in table 8-48.

8-218. CPU ADDRESS BUS SCHEMATIC DESCRIPTION. FIGURE 8-12.

8-219. Latches U71 and U72 capture the address from the low instruction/data/address bus (LIDA) at the correct time, indicated to the latches by High Address Latch (HADL).

8-220. ADDRESS BUFFERS SCHEMATIC DESCRIPTION.
FIGURE 8-12.

8-221. Buffers U69, U70 provide the necessary inversion of the address bus for the ROMs.

8-222. CHIP SELECT SCHEMATIC DESCRIPTION.
FIGURE 8-14.

8-223. Data selector U67A,B decodes the addresses for ROM chip selection.

8-224. ROM SCHEMATIC DESCRIPTION.
FIGURE 8-14.

8-225. ROMs U48-51 contain utility routines for power up of the mainframe, and performance verifications for the mainframe and the local mass storage options. The jumpers in the ROM address lines have several combinations to allow different sizes of ROMs to be used. Jumper information is given on the schematic for the indicated board revision.

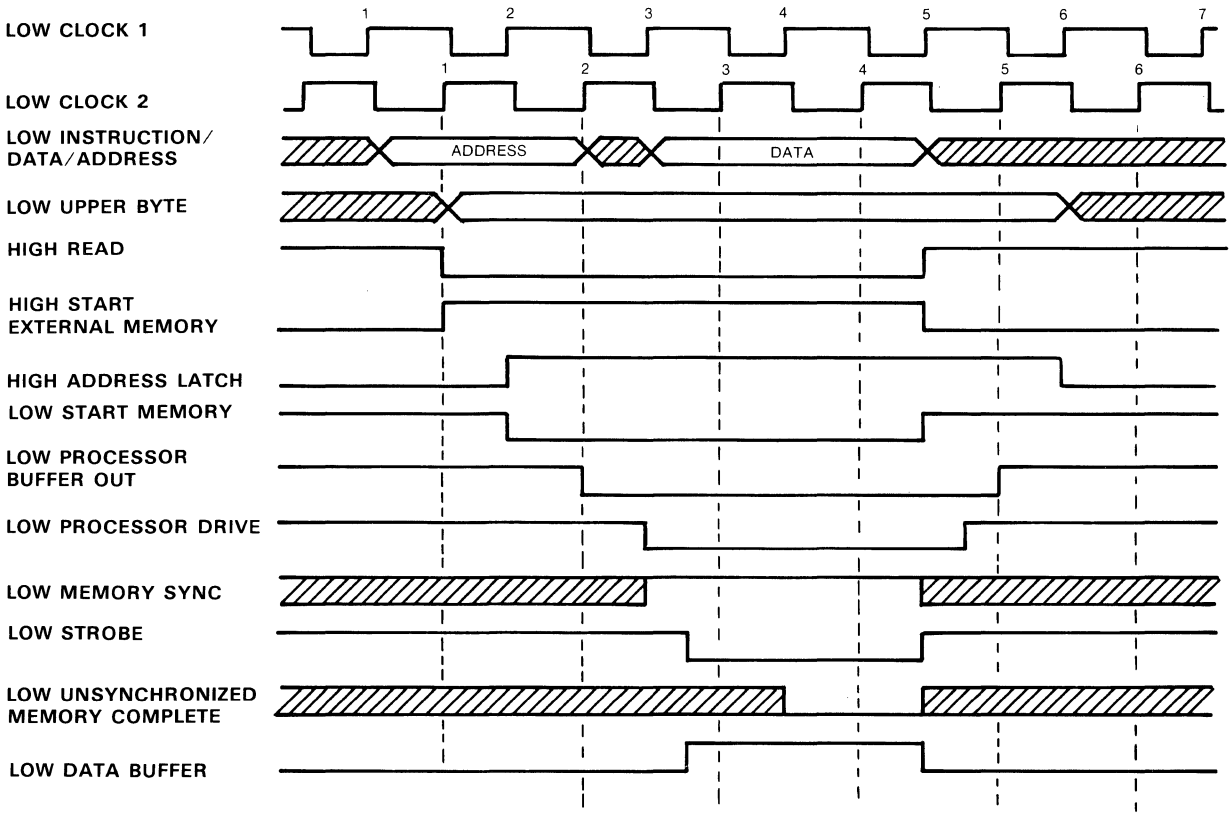


Figure 8-7. Typical Write Memory Cycle

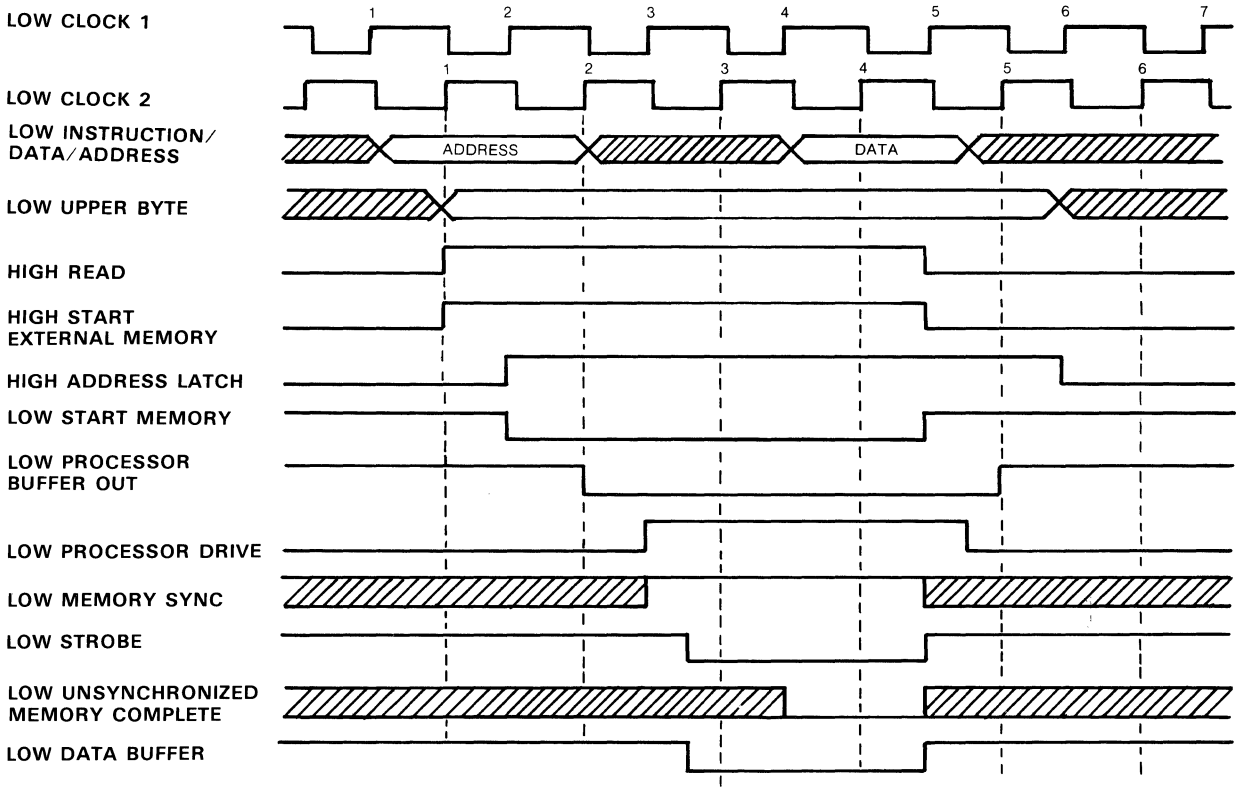


Figure 8-8. Typical Read Memory Cycle

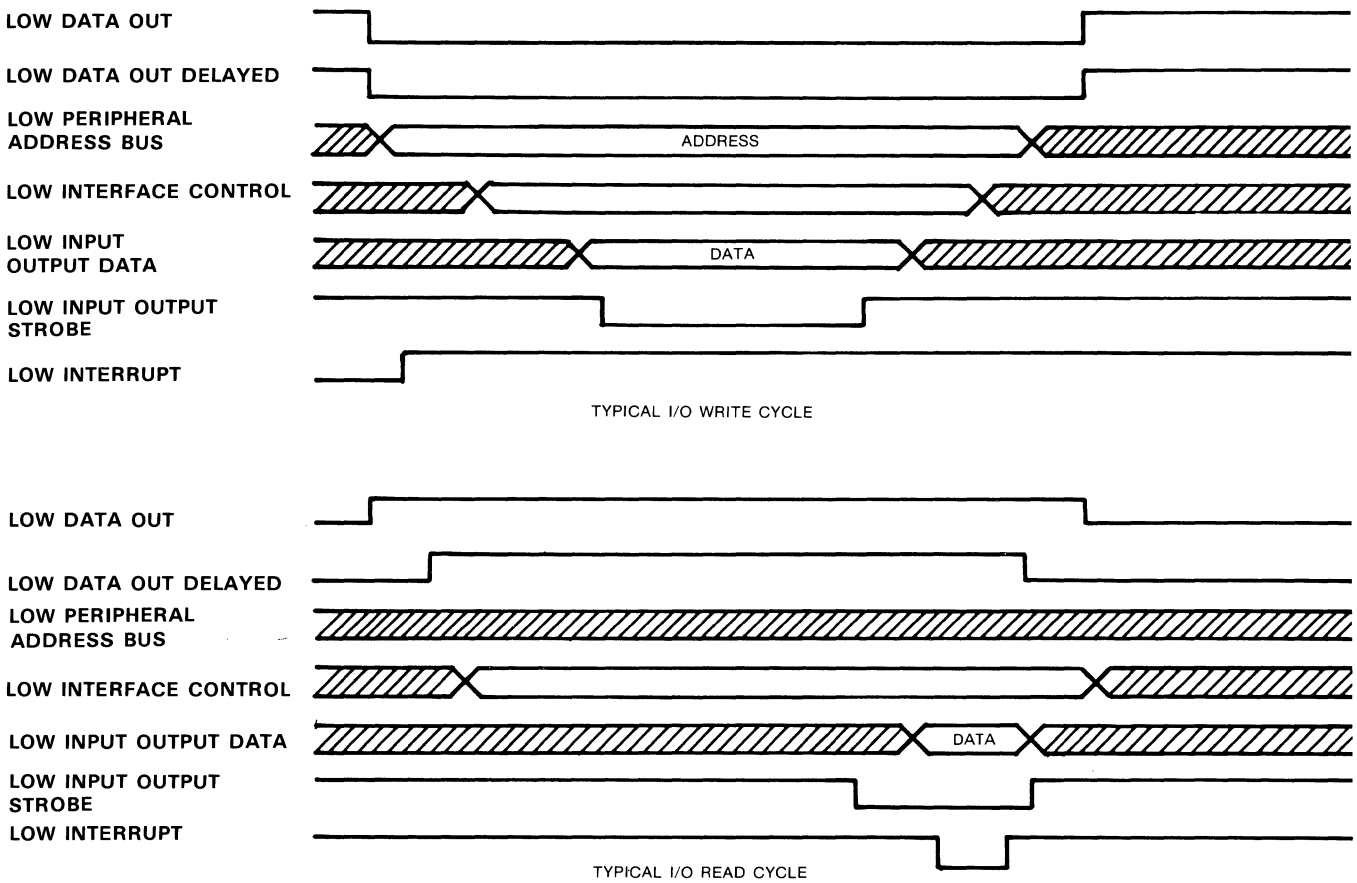


Figure 8-9. Typical I/O Read and Write Cycle

8-226. DATA BUS SCHEMATIC DESCRIPTION.
FIGURE 8-14.

8-227. Buffers U53 and U45 provide buffering between the ROM outputs and the CPU data bus. Because the data bus has addresses multiplexed on it, the data can only be on the data bus at certain times. Therefore, the outputs of U53 and U45 are active only when Low Data Buffered (LDBUF) is true.

8-228. TEST/RESET SCHEMATIC DESCRIPTION.
FIGURE 8-14.

8-229. ICs U67A and U74 will cause the CPU to count from 0020 hex to 3C00 hex, then reset to 0020 hex and count to 3C00 hex again. This cycle will continue as long as jumper E10 is in the test mode and the buffers U53 and U45 are removed or disabled. The test mode is used by a service person when troubleshooting with signature analysis.

8-230. SA INTERVAL LATCH SCHEMATIC DESCRIPTION.
FIGURES 8-12, 8-13 and 8-14.

8-231. The SA latches U58A/B and U64A are used while taking signature analysis for setting up the intervals required to get valid signatures. There is the memory bus SA latch U64A, CPU memory latch U58B, and the I/O memory latch U58A.

8-232. INPUT/OUTPUT BUS SCHEMATIC DESCRIPTION.

8-233. Activity on the input/output bus is software dependent. However, when there is activity, the timing sequence is predictable.

8-234. Timing diagrams for both read and write cycles are shown in figures 8-7 and 8-8.

8-235. I/O DATA TRANSCEIVER SCHEMATIC DESCRIPTION.
FIGURE 8-13; U40, U47.

8-236. I/O data and instructions are routed thru transceivers U41 and U47 to the various I/O circuits that require communications with the CPU. This includes the low priority interrupt logic, card slot select logic, HP-IB controller and the keyboard. These two transceivers are bidirectional and are each 8 bits wide. The transceivers are enabled by either LDOUTB, LINT and LRORP, or by any of the following peripheral addresses: LKYBD, LHP-IB or LBEEPEN. The direction of data flow is controlled by LDOUTB where the flow is to the CPU when LDOUTB = 1 and from the CPU to the I/O circuits when LDOUTB = 0.

8-237. BEEPER DECODER SCHEMATIC DESCRIPTION.
FIGURE 8-17, U26B.

8-238. Beeper decoder U26B is a 2-to-4 line decoder that decodes the LDOUTB and LIC1D commands from the CPU for the purpose of generating the SA start-stop interval and activating the beeper circuits on the A6 secondary board. Peripheral command LBEEPEN enables this decoder when the CPU operating system has determined the proper conditions exist. Table 8-19 is the truth table for U26B.

Table 8-19. Beeper Decoder Truth Table

EN LBEEPEN Pin 15	0 LIC1D Pin 13	1 LDOUT Pin 14	Outputs 12	11	10	9	Function Activated
1	X	X	1	1	1	1	None
0	0	0	0	1	1	1	None
0	0	1	1	0	1	1	None
0	1	0	1	1	0	1	Beeper & Display
0	1	1	1	1	1	0	S/A Interval

8-239. BEEPER START PULSE GENERATOR SCHEMATIC DESCRIPTION.
FIGURE 8-27, U6A.

8-240. Monostable multivibrator U6A is triggered when LBEEP and LIC1D are true and LDOUT is false. When triggered, U16A generates a pulse approximately 220 milliseconds in duration which turns Q7 on and causes C28 to rapidly charge up to +5 VDC thru R36. When the U16A output pulse terminates, C28 exponentially discharges thru R37 thus creating a pulse that has a steep leading edge and a sloping trailing edge which causes the beeper to produce a bell sound. This pulse turns on Q8 thus providing +5 VDC (HBON) to one side of the beeper speaker.

8-241. SA LATCH SCHEMATIC DESCRIPTION.
FIGURE 8-17, U41A.

8-242. This is one-half of a D-type flip-flop that has interface command LIC2D as its D input and is clocked by the pin 9 output of decoder U26B. The output of U41A is fed to test point TP6 and serves as the SA start-stop signal for troubleshooting the I/O circuits.

8-243. CARD ID LATCH AND DECODER SCHEMATIC DESCRIPTION.
FIGURE 8-17; U54, U75B.

8-244. Latch U54 is a D-type flipflop a portion of which is used for storing interface commands LIC1D and LIC2D when the CPU causes peripheral address LSLOT SEL to occur. The remaining segment of U54 is used for latching the I/O data bits for generating the card slot select

commands (see slot select circuit description).

8-245. The two outputs on pins 16 and 19 of U54 are fed to decoder U75B where they are decoded into four discrete signals: ID Enable (LID) and MAP commands LMAP1 thru LMAP3. Signal LID is output on pin 67 of J1 and enables the option card ID circuits for the option cards that may be located in any of the five option card slots. The three MAP signals serve as address lines for expansion of the option card memory capabilities. Table 8-20 is the truth table for U75B.

Table 8-20. Card ID Decoder Truth Table

LIC2D	LIC1D	LID	LMAP1	LMAP2	LMAP3
0	0	0	1	1	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	1	1	1	0

8-246. SLOT SELECT LATCH SCHEMATIC DESCRIPTION.
FIGURE 8-17, U54.

8-247. Latch U54 consists of six segments of an 8-element D-type flipflop (the other two sections serve as the card ID latch). Its purpose is to latch (store) I/O address bits 8-13 and is under CPU control (i.e., enabled) via peripheral address LSLOT SEL. When the CPU wants to store I/O bits 8-13, it causes the LSLOT SEL perpheral address line to be pulsed. This causes I/O bits 8-13 to be latched at the positive going edge of LSLOT SEL.

8-248. SLOT SELECT DECODER SCHEMATIC DESCRIPTION.
FIGURE 8-17, U73.

8-249. Address bits 8-13 from latch U54 serve as the address input to Slot Select Decoder U73. Addresses LA14 and LA15 from the memory address bus are are used to provide the chip select function of U73 as shown in truth table 8-21. Whenever the CPU reads or write to the address range reserved for the option slots, LA14 and LA15 are in a state to enable the slot selector. The jumpers in the memory address lines LA13-15 must be in the A position for operation of the mainframe.

Table 8-21. Slot Select Decoder Enable Truth Table

CPU Memory Address Bits LA15	LA14	U73 Selected
1	0	Yes
All other conditions		No

8-250. Decoder U73 is a 4-line to 16-line decoder that decodes the four input address lines. Each of the five outputs from U73 (LSEL0-LSEL4) is routed to pin 72 of each of the option card slots as follows:

LSEL0 J6-72
LSEL1 J5-72
LSEL2 J4-72
LSEL3 J3-72
LSEL4 J2-72

8-251. INTERRUPT BUFFER ENABLE LOGIC SCHEMATIC DESCRIPTION. FIGURE 8-17, U26A.

8-252. Latch U26A is a D-type together with gate U20 decode LPA3, LINT and HDOUTB to produce the Interrupt Buffer Enable signal (LIBE). Table 8-22 is the truth table for LIBE.

Table 8-22. Interrupt Buffer Enable Truth Table

LPA3	LINT	HDOUTB	LIBE
1	0	0	0
LIBE = 1 for all other combinations			

8-253. HIGH PRIORITY INTERRUPT LATCH SCHEMATIC DESCRIPTION. FIGURE 8-17, U62.

8-254. This latch is a D-type flip-flop that is clocked by the negative going edge of Power Fail Interrupt (LIR15) and set by either LPOP or peripheral address LIRHCLR

8-255. Latch U62 is set by LPOP at system power-up (or by pressing the Reset Test switch). This is done by LPOP passing thru AND gate U59B and on to the set input of U62 , pin 10. Latch U62 remains in the set state until a power fail interrupt (LIR15) occurs. When the power supply senses that a power failure is imminent, LIR15 goes low which is inverted by U77 before clocking U62 . The clocking of U62 causes output pin 7 (HIRH) to go high which is inverted by U27 thus producing the high priority (unmaskable) interrupt signal LIRH. This

signal is sent via the I/O bus to the CPU and informs the controller that power is failing.

8-256. After receiving the message that power is failing, the CPU responds by writing to peripheral address decoders U12/U28 to produce the power fail set (LIRHCLR) address. The LIRHCLR bit performs two functions. First, it sets power fail latch to disable the LPOP pulse generator U61, and second, it sets high priority interrupt latch U62 thus canceling the high priority interrupt caused earlier by LIR15.

8-257. DELTA-T INTERRUPT LATCH SCHEMATIC DESCRIPTION. FIGURE 8-17, U64B.

8-258. The 60/50 Hz LINSYN signal from the power supply enters on pin 75 of J1 and is buffered by U77 before being applied to D-type flip-flop U64B and modulo-16 counter U63A. Latch U64B is clocked by each positive-going edge of LINSYN thus causing the Q output at U64B to latch high due to the D input of U64B being tied to +5 vdc.

8-259. The Q output of U64B is interrupt signal HIR (Delta) T and is routed to the low priority interrupt logic and causes a low priority interrupt (LIRL) to be sent to the CPU via the I/O bus. After a nominal delay, the CPU responds with peripheral address L(DELTA)T which resets latch U64B which in turn causes HIR (Delta) T to go low and reset counters of U63A,B.

8-260. If the CPU takes longer than 2.24 seconds (2.6 seconds for 50Hz line frequency) to respond with the L(DELTA)T address, the Delta-T Interrupt Timers (U63A,B) will time-out thus producing a high output on U63A which is fed to gate U30D. The output to U30D then goes low and is routed (assuming the auto-reset enable mode is selected) to the A2 trigger input of LPOP pulse generator U61A. The triggering of U61A causes the LPOP signal to be produced which in turn resets all of the circuits that it is tied to.

8-261. DELTA-T INTERRUPT COUNTER SCHEMATIC DESCRIPTION. FIGURE 8-17, U63A, B.

8-262. Binary counters U63A/B are each modulo-16 counters that are decaded thus creating a modulo-128 counter. Counter 63B is incremented one count by each occurance of LINSYN. When this counter reaches a count of 8, pin 8 goes high. At a count of 16, pin 8 goes low at which time U63A is incremented. When U63A has been incremented 8 times, its pin 8 output goes high which corresponds to 16 x 8 = 128 pulses of LINSYN or about 2.2 seconds for a line frequency of 60Hz. If the output of U63A is allowed to go high (i.e., time out) before being reset by the occurance of L(DELTA)T, the LPOP reset signal is generated (see paragraph 8-145).

8-263. MANUAL RESET DE-BOUNCE LATCH SCHEMATIC DESCRIPTION. FIGURE 8-17, U62A.

8-264. This circuit is latched with the first contact closure of the Processor Reset Switch and thus prevents multiple triggering (due to contact bounce) of LPOP Generator U61 A when the system is manually reset.

8-265. LOW PRIORITY INTERRUPT LOGIC SCHEMATIC DESCRIPTION. FIGURE 8-17; U8A/BCD, U6A/BC.

8-266. The eight, low priority interrupts are gated thru AND gates U6A/BCD. These gates can be disabled (masked) by the CPU as a result of latching the masking code into the interrupt mask latch U24. Latch U24 is cleared by LPOPB.

8-267. The unmasked interrupts are routed to interrupt data buffer U23 and also are ANDed by U6A/BC to produce low priority interrupt signal LIRL. This signal is routed to the CPU and causes the CPU to initiate an interrupt poll to determine which peripheral device requested the interrupt. The interrupt poll consists of the CPU sending interrupt signals LINT and LDOUT to the 16-bit wide I/O data tranceivers U40 and U47 via AND gate U35B.

8-268. LINT enables the two data transceivers, while LDOUTB controls the direction of data flow which in this case is back towards the CPU. LIBE enables buffer U23 to put the interrupt code on the I/O data lines. The format of the interrupt code sent to the CPU identifies the device that requested the interrupt (i.e., the location of the logic 0 in bits LIOD0 thru LIOD7 identifies the interrupting device). Table 8-23 shows the ID code for the eight interrupts.

Table 8-23. Interrupt ID Codes

Interrupting Device	I/O Data Bits 7	6	5	4	3	2	1	0
HP-IB	0	1	1	1	1	1	1	1
RS-232 Receive	1	0	1	1	1	1	1	1
RS-232 Transmit	1	1	0	1	1	1	1	1
(NOT USED)	1	1	1	0	1	1	1	1
Local Mass Storage	1	1	1	1	0	1	1	1
Delta Time	1	1	1	1	1	0	1	1
Option	1	1	1	1	1	1	0	1
Keyboard	1	1	1	1	1	1	1	0

8-269. REAR PANEL SWITCH BUFFER SCHEMATIC DESCRIPTION. FIGURE 8-15, U22.

8-270. This is an uni-directional, 8 channel buffer that relays the status of the rear panel mode control switch S1 to the CPU. Control is

provided by the PHI control logic.

8-271. ADDRESS LATCH SCHEMATIC DESCRIPTION.
FIGURE 8-15, U38.

8-272. This is a D-type flip-flop that is used to store four bits (HIOD8-HIOD11) of the I/O address data. Bits 9-11 control the selection of the PHI chip internal address registers while bit 8 serves to control the RS-232 loop-back test feature.

8-273. PHI CONTROL LOGIC SCHEMATIC DESCRIPTION.
FIGURE 8-15; U30A/B, U37A/B.

8-274. This circuit is an array of four NAND gates that decode five input control signals from the CPU. Its purpose is to control the selection of rear panel switch buffer U22, address latch U38, and PHI chip U36. The five input control signals are: HDOUTD, LIC1D, LIC2D, LDOUT and LHP-IB. Truth table 8-24 shows the control relationships.

Table 8-24. PHI Control Logic Truth Table

Input Control Signals					Chip Select Status		
LIC1	LIC2	LHP-IB	LDOUT	HDOUTD	BUF U22	LTCH U38	PHI U36
X	0	0	X	0	Yes	No	No
X	0	0	0	X	No	Yes	No
0	X	0	X	X	No	No	Yes

X=Don't Care

8-275. PHI SCHEMATIC DESCRIPTION.
FIGURE 8-15, U36.

8-276. The PHI chip provides a high speed (up to 1 Mbyte) interface to the HP Interface Bus (HP-IB) for processors and other state oriented devices. It is compatible with nearly any 8 or 16-bit CPU and requires a minimum of external logic. Together with the four bipolar tri-state transceivers (U1,U4,U5,U19 on the rear panel), the PHI chip provides the complete logical and electrical interface between the CPU and the HP-IB. In addition, it provides buffering for inbound and outbound data transfer through two First-In-First-Out (FIFO) registers which can be addressed by the host CPU.

8-277. The following I/O signals are provided by the PHI chip for CPU interfacing:

1. A 8-bit wide bi-directional data bus (LD8-D15)
2. LD0 and LD1 are status bits that indicate which byte of the record is being transferred.
3. A 3-bit address (LA13-LA15) for selecting one of eight internal registers
4. A read/write control (R/W) that controls the direction of data flow.
5. An interrupt line (LINT) to alert the CPU of selected events.
6. Three handshake lines HRFD, HDAC and HDAV to cooridinate data transfer with the HP-IB.
7. A Direct Memory Request line (LDMARQ) for directly accessing the CPU memory (not used).

8-278. HP-IB LINES, SCHEMATIC DESCRIPTION.
FIGURE 8-15.

8-279. The HP-IB transfers data and commands between the components of the 64110 Logic Development System on 16 signal lines. The interface functions for each system component are performed within the component so only passive cabling is needed to connect the system. The cables connect all instruments, controllers, and other components of the system in parallel.

8-280. The eight data I/O lines (HDIO1-8) are reserved for the transfer of data and other messages in a byte-serial, bit-parallel manner. Data and message transfer is asynchronous and is coordinated by the three handshake lines: Data Valid (HDAV), Ready for Data (HRFD), and Data Accepted (HDAC). The other five lines are for management of bus activity. See figure 8-10.

8-281. Devices connected to the bus may be talkers, listeners, or controllers. The controlling mainframe dictates the role of each of the other devices (disc or printer) by setting the LATN (Attention) line true and sending talk or listen addresses on the data lines.

8-282. Addresses are set into each device by switches built into the device. While the LATN line is true, all devices must listen to the data lines. When the LATN line is false, only devices that have been addressed will actively send or receive data; all others ignore the data lines.

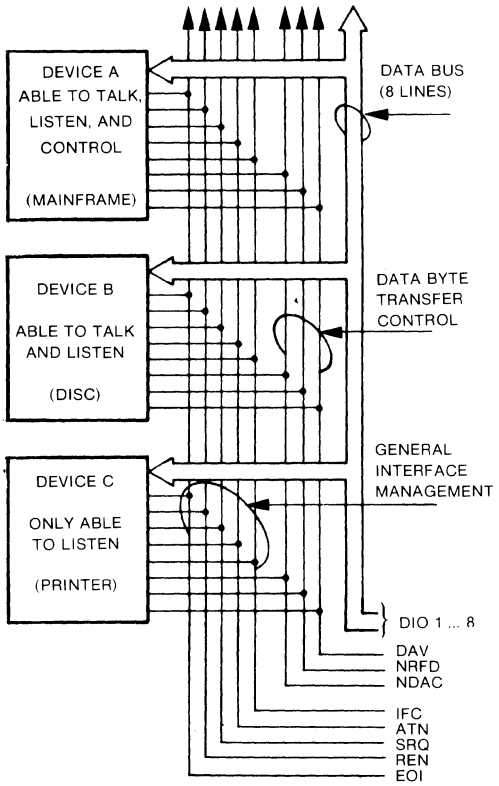


Figure 8-10. HP-IB Signal Lines

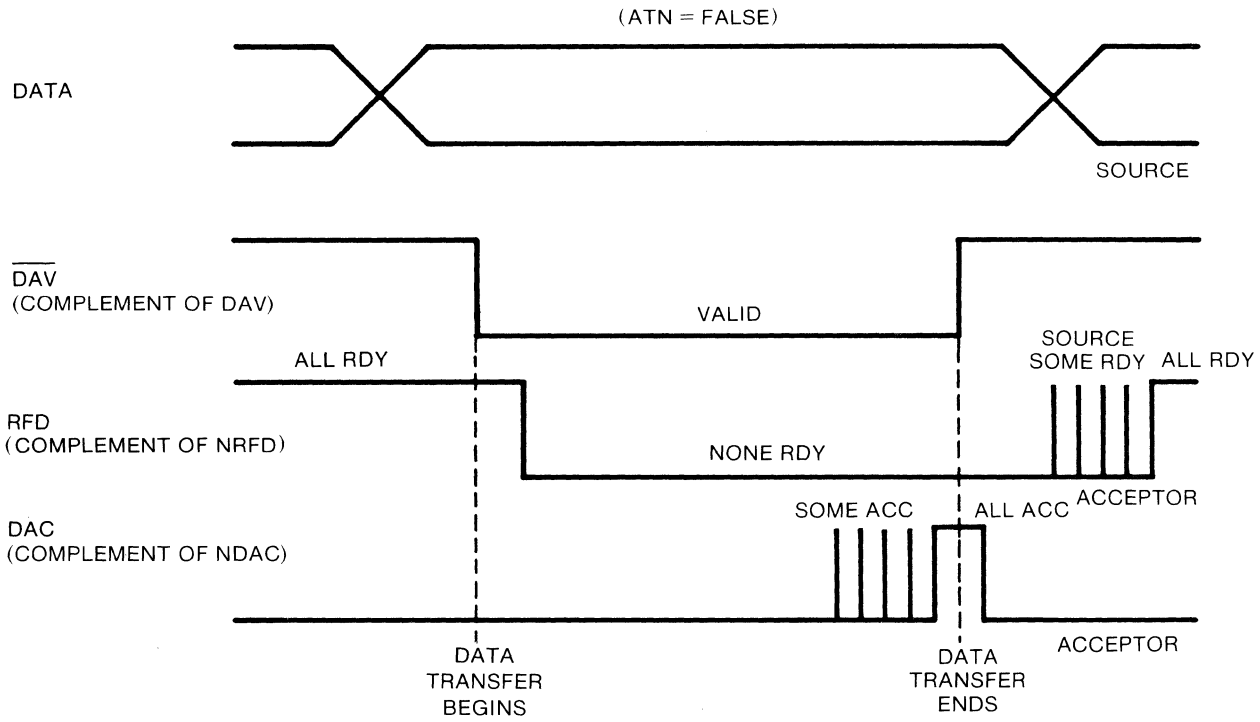


Figure 8-11. HP-IB Handshake Timing

8-283. Several listeners can be active simultaneously but only one talker can be active at a time. Whenever a talk address is put on the data lines (while LATN is true), all other talkers are automatically unaddressed.

8-284. Information is transmitted on the data lines under sequential control of the three handshake lines (HDAV, HRFD and HDAC). No step in the sequence can be initiated until the previous step is completed. Information transfer can proceed as fast as devices can respond, but no faster than allowed by the slowest device presently addressed as active. This permits several devices to receive the same message byte concurrently. See figure 8-11.

8-285. The LATN line is one of the five bus management lines. When LATN is true, addresses and universal commands are transmitted on only seven of the data lines using the ASCII code. When LATN is false, any code of 8 bits or less understood by both the talker and listener(s) may be used.

8-286. The LIFC (Interface Clear) line places the interface system in a known quiescent state via the abort message. The LREN (Remote Enable) line is used with the Remote, Local and Clear Lockout/Set Local messages to select either local or remote control of each device.

8-287. Any active device can set the LSRQ (Service Request) line true. This indicates to the CPU that the device on the bus wants attention. The LEOI (End or Identify) line is used by a device to indicate the end of a multiple-byte transfer sequence. When the controlling main frame sets both the LATN and LEOI lines true, each device capable of a parallel poll indicates its current status on the HDIO line assigned to it.

8-288. KEYBOARD-SCAN SCHEMATIC DESCRIPTION.

8-289. The keyboard-scan circuitry consists of seven functional areas:

Control state machine

Key-depressed latch

Key status RAM

Address counter

Interrupt request latch

Address decoder

Output buffer

8-290. When a key change occurs, an interrupt is sent to the processor. The processor then reads the key address and status and sends the appropriate information to the display circuitry.

8-291. CONTROL STATE MACHINE SCHEMATIC DESCRIPTION.

8-292. The keyboard control state machine is clocked through its four states by Low Horizontal Sync, LHSYN. The output states are determined by the Q outputs of the two J-K flip-flops U32A/B.

8-293. Keyboard Control States.

8-294. Control State 1. The keyboard status RAM is disabled.

8-295. Control State 2. The keyboard address counter is incremented, and the keyboard status RAM remains disabled to allow the outputs of the address counter to stabilize. Also, the signals to write the old status at the RAM output are present.

8-296. Control State 3. Signal HKYDET is sampled, the RAM is activated and its output is compared to High Key Detect, HKYDET. The comparison is sampled in state 1 for key change detection.

8-297. Control State 4. The scan circuitry checks for a key change. If a change is detected, High Interrupt Request Keyboard is generated and the scan circuitry is placed in a halt state until the processor acknowledges the interrupt and reads the key address and status. Also, the current key status is stored in the keyboard status RAM.

8-298. KEY-DEPRESSED LATCH SCHEMATIC DESCRIPTION.

8-299. The key-depressed latch, latches the status of HKYDET at the beginning of state 4. Pin U32-7 goes high and latches the HKYDET signal at pin U33-9. This status is maintained through all other states.

8-300. KEY STATUS RAM SCHEMATIC DESCRIPTION.

8-301. The key status RAM stores the status of every key for use in detection of key changes.

8-302. Key Status States.

8-303. Status State 1. The RAM is disabled to eliminate erroneous key change detection.

8-304. Status State 2. The address counter is incremented and the RAM is disabled to allow the outputs of the counter to stabilize.

8-305. Status State 3. The RAM is activated and the addressed key's previous state is available to be compared with the current state.

8-306. Status State 4. The current status of the addressed key is written into memory.

8-307. ADDRESS COUNTER SCHEMATIC DESCRIPTION.

8-308. The address counter is an eight bit count up counter which is incremented at the beginning of status state 3. Its output defines the key being checked and is used by the CPU, the keyboard status RAM, and the keyboard.

8-309. INTERRUPT REQUEST LATCH SCHEMATIC DESCRIPTION.

8-310. The interrupt request latch compares the current with the status of the addressed key using an exclusive OR gate and an interrupt request latch. If the status has changed at the beginning of Status State 1 (refer to 8-289), a High Interrupt Request Keyboard is sent to the CPU. The keyboard control state machine is halted, keeping the keyboard address counter frozen at the address of the key which has changed status until the CPU has acknowledged the interrupt request.

8-311. ADDRESS DECODER SCHEMATIC DESCRIPTION.

8-312. The address decoder monitors High Data Out Delayed, HDOUTD, and L0. When both are low, it enables the keyboard output buffer which places the key address and status on the I/O buffered data bus. Signal HDOUTD will be low when the CPU is not writing to the data bus, and L0 will be low when the CPU wishes to access the keyboard.

8-313. OUTPUT BUFFER SCHEMATIC DESCRIPTION.

8-314. The output buffer places the key address and status on the I/O buffered data bus when Low Read Keyboard, the output of the keyboard address decoder, goes low.

Table 8-25. Keyboard States

State	U32A	U32B	Action
1	0	1	Keyboard status RAM disabled
2	1	1	Increment keyboard address counter, RAM remains disabled.
3	1	0	Sample HKYDET, activate RAM and compare output to HKYDET.
4	0	0	Check for change, store new status, halt and wait for processor read if change is detected.

8-315. KEYBOARD SCHEMATIC DESCRIPTION.

8-316. The keyboard is a switch matrix composed of sixteen columns and eight rows. The columns are defined by High Key Address 0-3, HKA0-3, and two binary-to-octal decoders. The rows are defined by A4-6 and an eight input demultiplexer. The selected row and column determine the particular key being scanned. If a key is depressed when it is being scanned, a High Key Detect, HKYDET, signal is sent to the keyboard scan circuitry.

8-317. The row selected is determined by HKA0-3. Signal HKA0-2 determines which of eight outputs from the selected binary-tooctal decoder is sent low, and HKA3 determines which binary-tooctal decoder is enabled.

8-318. The column selector decodes HKA4-6 and determines which of eight inputs will be seen at its output. Its output is High Key Detect, HKYDET.

8-319. The keyboard is continually scanned by the keyboard scan circuitry. The current status of HKYDET for each value of HKA0-6 is compared in the scan circuitry with each previous status to determine if a change was made and its status. Signal HKYDET high indicates the key is depressed and low indicates it is released.

8-320. CPU/IO TROUBLESHOOTING.

Table 8-26. ROM Troubleshooting (1 of 2)

STEP 1. ROM FAILURE LEGIBLE ON DISPLAY?

YES....replace failing ROM IC(s).

Failed Addresses	Byte	Failed ROM Unit	
0020-1FFF	0	U51	Lower 8K ROM
0020-1FFF	1	U48	
2000-3BFF	0	U50	Upper 8K ROM
2000-3BFF	1	U49	

DOESN'T FIX PROBLEM....go to step 3. The test may be interpreting the failure of an IC other than the ROM IC(s) as a ROM IC failure. CPU Freerun will allow you to isolate failures in other IC's.

NO....Go to step 2. A failure in the display may be masking the output of the ROM failure to the display. ROM failure decode will give you this same information.

STEP 2. ROM FAILURE SUMMARY....use power-up ROM test table (ROM failure summary setup).

GOOD Vh....use the setup to isolate the failing ROM IC(s) and replace.

DOESN'T FIX PROBLEM....go to step 3. The test may be interpreting the failure of an IC other than the ROM IC(s) as a ROM IC failure. CPU Freerun will allow you to isolate failures in other IC's.

BAD Vh....go to step 3. The bad Vh indicates that the ROM failure setup is not running because the CPU is not able to access ROM or the kernel of ROM needed for running the setup is not good. CPU freerun allows you to troubleshoot the ROM circuitry with a minimum of timing and control circuitry working.

Table 8-26. ROM Troubleshooting (2 of 2)

STEP 3. CPU FREERUN....use signature analysis setup I table (CPU freerun setup).

GOOD Vh....Take signatures and troubleshoot.

NO BAD SIGNATURES....Check LMSYN signal from display controller. Part of the setup for CPU freerun is to disable LMSYN coming from the display controller board. If LMSYN is low, in normal operation it will cause the CPU to wait indefinately.

LMSYN IS LOW....use signature analysis setup U table (RAM cycle selector/generator setup) to troubleshoot the display controller board.

BAD Vh....go to signature analysis setup J table (freerun decode setup). Freerun decode will allow you to isolate failures in the CPU freerun hardware.

STEP 4. FREERUN DECODE....use signature analysis setup J table (freerun decode setup).

GOOD Vh....Take signatures and troubleshoot.

BAD Vh....go to worst case troubleshooting table. Not even the minimum hardware of the CPU, timing and control and the address latches is operating. Worst case troubleshooting will give you suggestions for troubleshooting this hardware.

Table 8-27. Worst Case Troubleshooting

CHECK BPC INPUTS:

Power Supplies

Clocks

Check for pulse low on LPOP on pressing of reset button.

Check for LMSYN signal low.

If LMSYN is low, in normal operation it will cause the CPU to wait indefinately.

LMSYN IS LOW....use RAM cycle selector/generator SA setup to troubleshoot the display controller board.

Check low and high priority interrupt inputs to BPC.

LAST RESORT TROUBLESHOOTING....Use a data probe and the reset button to check for activity on memory buses.

Table 8-28. Power-Up ROM Test

LOOPNAME: POWER-UP ROM TEST

On power-up, checksums of the program ROMs are computed to verify the program content of ROM. If a failure is detected a bit in an error word is set. This error word is used to output an error message to the display and the test repeats indefinately.

SETUP NAME: ROM FAILURE SUMMARY

During self test ROM test the error word is output to the data bus. If the display is inoperative, the user may determine the address range of and byte of the failing ROM by taking signatures on the data bus and using the table below.

CPU executing Self Test ROM Test

ST/SP/START: A3TP5, rising edge (MEM SA LATCH)

QUAL/STOP: A3TP5, falling edge (MEM SA LATCH)

CLOCK: A3TP10, rising edge (MEM SA LATCH CLOCK LWRTROM)

byte 0	byte 1	byte 0	byte 1	
0000 - 3FFF	0000- 3FFF	0000 - C300	0000 - C300	A signature of 0000 means the address range is good. A signature of 0001 means the address range is bad.
LD0	LD1	LD2	LD3	

Table 8-29. Signature Analysis Setup I (1 of 2)

LOOPNAME: CPU FREERUN

This is a hardware forced loop which forces the CPU to execute LDA with A instruction beginning with address 0020H and counting through the ROM address range to C300H at which time a JMP direct, base page to 0020H is jammed onto the data bus and the loop repeats.

SETUP NAME: CPU FREERUN

This loop is used to troubleshoot the program ROMs and CPU memory buses in the event that the software is unable to execute any software.

CPU Freerun jumper A3J7 to Test

LMSYN Jumper A3J8 to Test

Auto Reset Jumper A3J6 to Test

ROM Buffers A3U45 and A3U53 Removed

Display Driver Disabled.

ST/SP/START: A3TP4, falling edge (LRDROM)

QUAL/STOP: A3TP4, rising edge (LRDROM)

CLOCK: A3TP1, rising edge (LSTB)

Vh = 8AHF

Table 8-29. Signature Analysis Setup I (2 of 2)

Node	Signature all ROMs installed	Signature A3U49 and 50 removed
U 45- 2	99C1	769C
U 45- 4	1255	8674
U 45- 6	7H08	9PH6
U 45- 8	1227	H58U
U 45-11	A876	7AH6
U 45-13	2880	1F90
U 45-15	487A	9HF1
U 45-17	93H2	9HU0
U 53- 2	UU7P	3AAU
U 53- 4	9625	4804
U 53- 6	P277	037C
U 53- 8	AF21	0A75
U 53-11	7C29	C34H
U 53-13	3A6P	8406
U 53-15	8A9A	PPP3
U 53-17	1F91	A8C5

Node	Signature
U 67-11	0H40
U 67-12	879F
U 69- 3	0U03
U 69- 5	F31F
U 69- 7	1F93
U 69- 9	23C5
U 69-12	79C4
U 69-14	2893
U 69-15	49F0
U 69-16	U7H0
U 69-18	961F
U 70-12	20C4
U 70-14	63A9
U 71- 2	1FF0
U 71- 5	7H0F
U 71- 6	A24U
U 71- 9	U368
U 71-12	A969
U 71-15	964U
U 71-16	49F0
U 71-19	85HU

Node	Signature
U 72- 6	P975
U 72- 9	AA68

Table 8-30. Signature Analysis Setup J

LOOPNAME: FREERUN DECODE

This is a hardware interval which must be initiated by pressing the RESET button on the CPU I/O board.

SETUP NAME: FREERUN DECODE

Freerun decode allows the troubleshooting of the circuitry used to generate the CPU freerun loop and the memory SA latch.

Auto reset jumper A3J6 to test

LMSYN jumper A3J8 to test

ROM buffers A3U45 and A3U53 removed

Press the RESET button on the A3 CPU I/O board for each signature

ST/SP/START: A3TP8, falling edge (LA0)

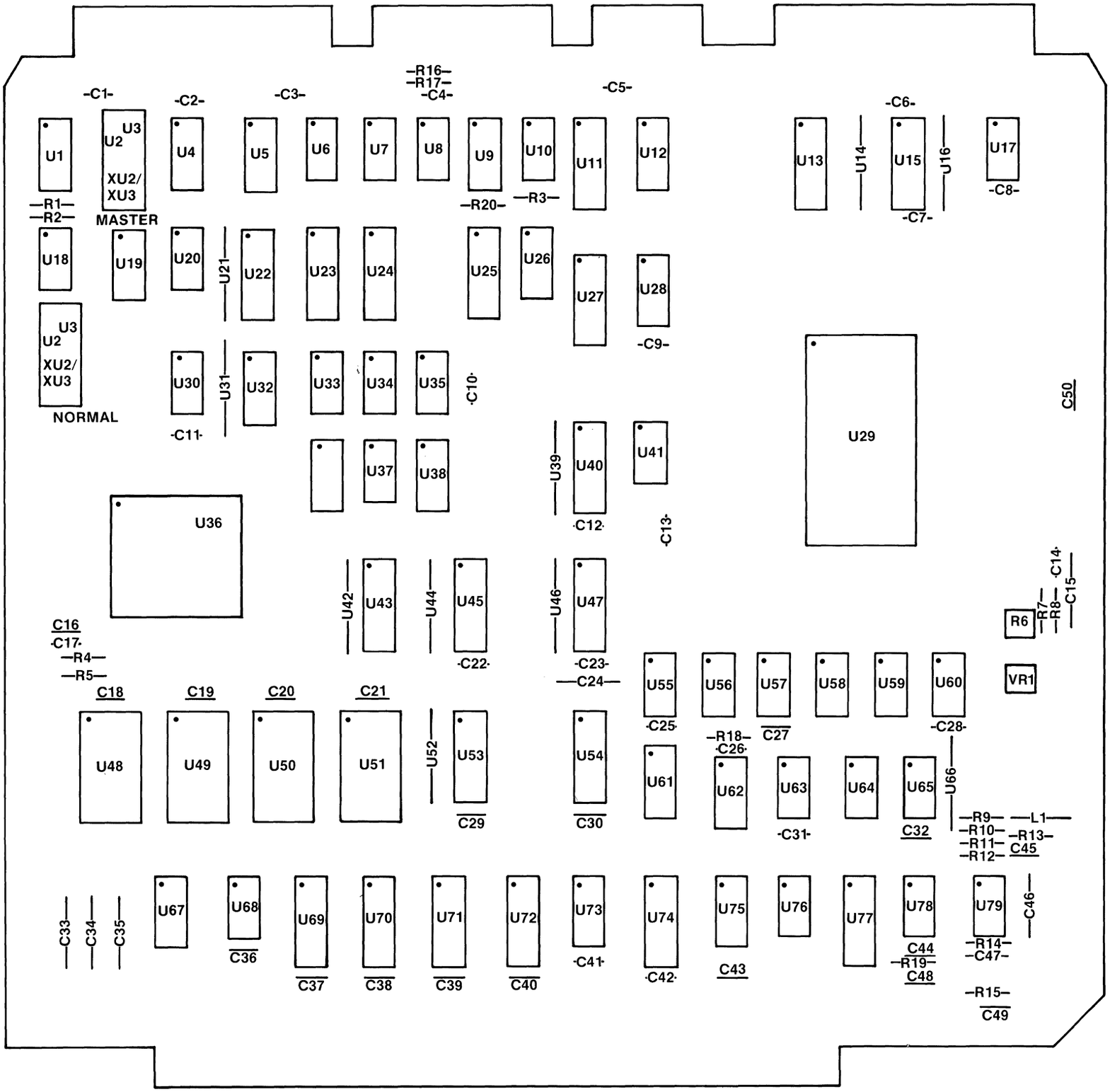
QUAL/STOP: A3TP9, rising edge (LA15)

CLOCK: A3TP1, rising edge (LSTB)

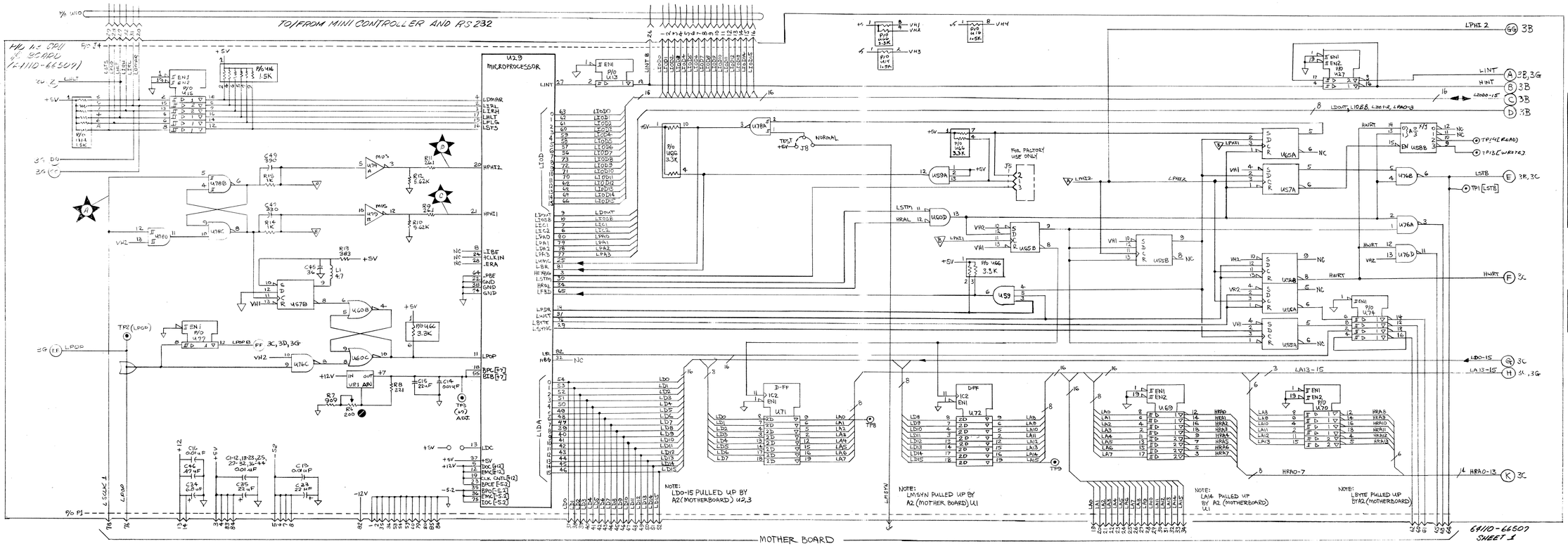
Vh = 782P

Node	Signature
U 64- 5	low
U 67- 5	high
U 67- 8	0093
U 67- 9	high
U 67-11	36C7
U 67-12	4P0A
U 68- 6	FHP3
U 70- 5	3C96
U 70- 9	3C96
U 70-16	HPP0
U 70-18	1293
U 72- 2	6ACH
U 72- 5	A6FP
U 72-12	A2F9
U 72-15	43C8
U 72-16	4009
U 72-19	0H71

NOTES



CPU/IO Component Locator



ICs ON THIS SCHEMATIC

REF DES.	HP PART NO.	MFR PART NO.
U13,15,77	1820-2024	74LS244
U14,16	1810-0276	210A152
U79	5061-3011	5061-3011
U55,56	1820-1112	74LS74
U57,65	1820-0693	74S74
U59	1820-1243	74LS15
U60	1820-1322	74S02
U66	1810-0278	210A232
U69,70,27	1820-1917	74LS240
U71,72	1820-2102	74LS373
U76	1820-0539	7437
U78	1820-1425	74LS132
U79	1820-1288	MMH0026CL

PARTS ON THIS SCHEMATIC

C1-16,18-25,27-49
R6-15
VR1 1C-LM317 1826-0393
L1 4.7UH 9140-0112

IC POWER SUPPLY CONFIGURATIONS

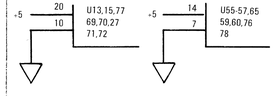
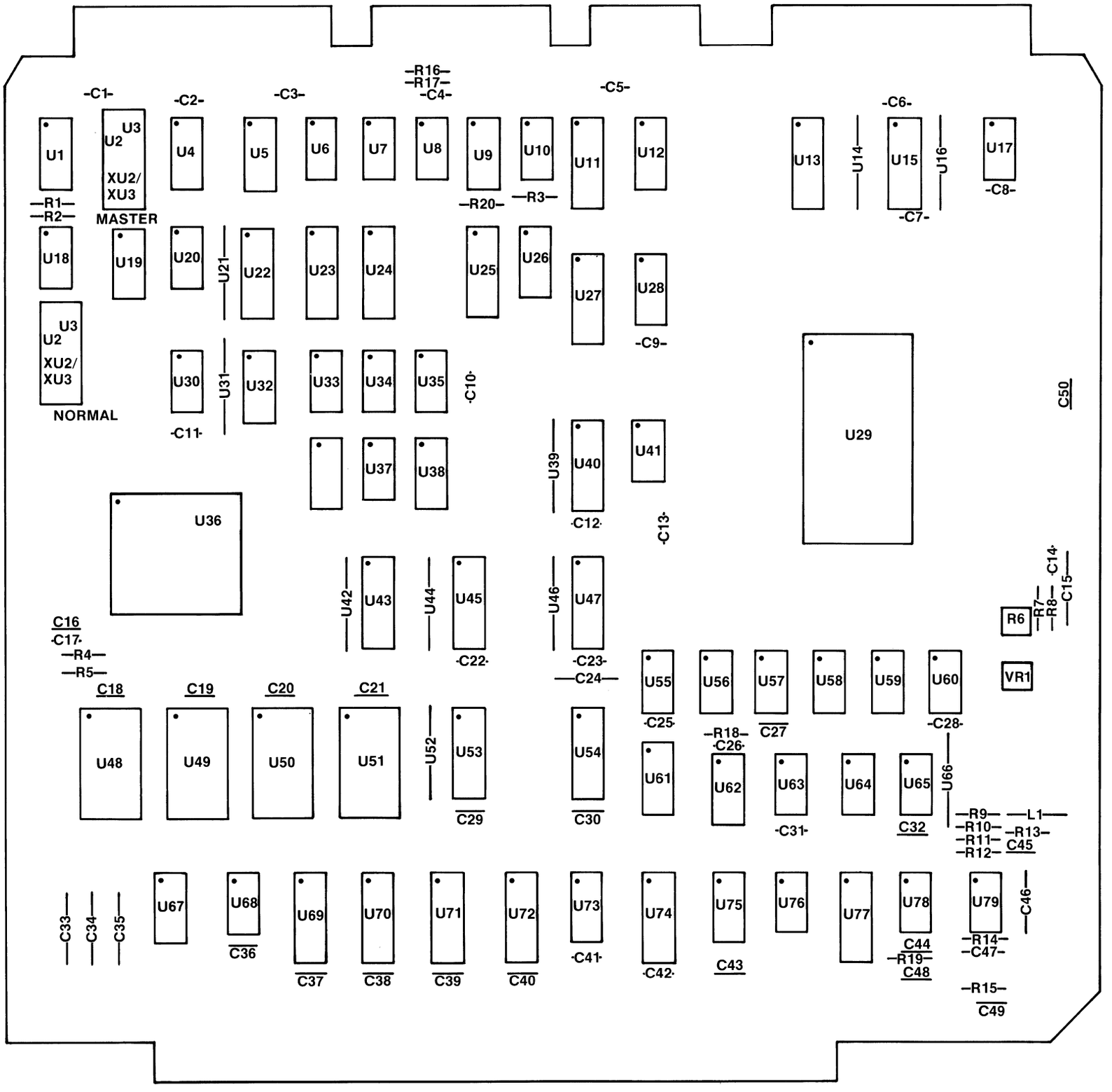
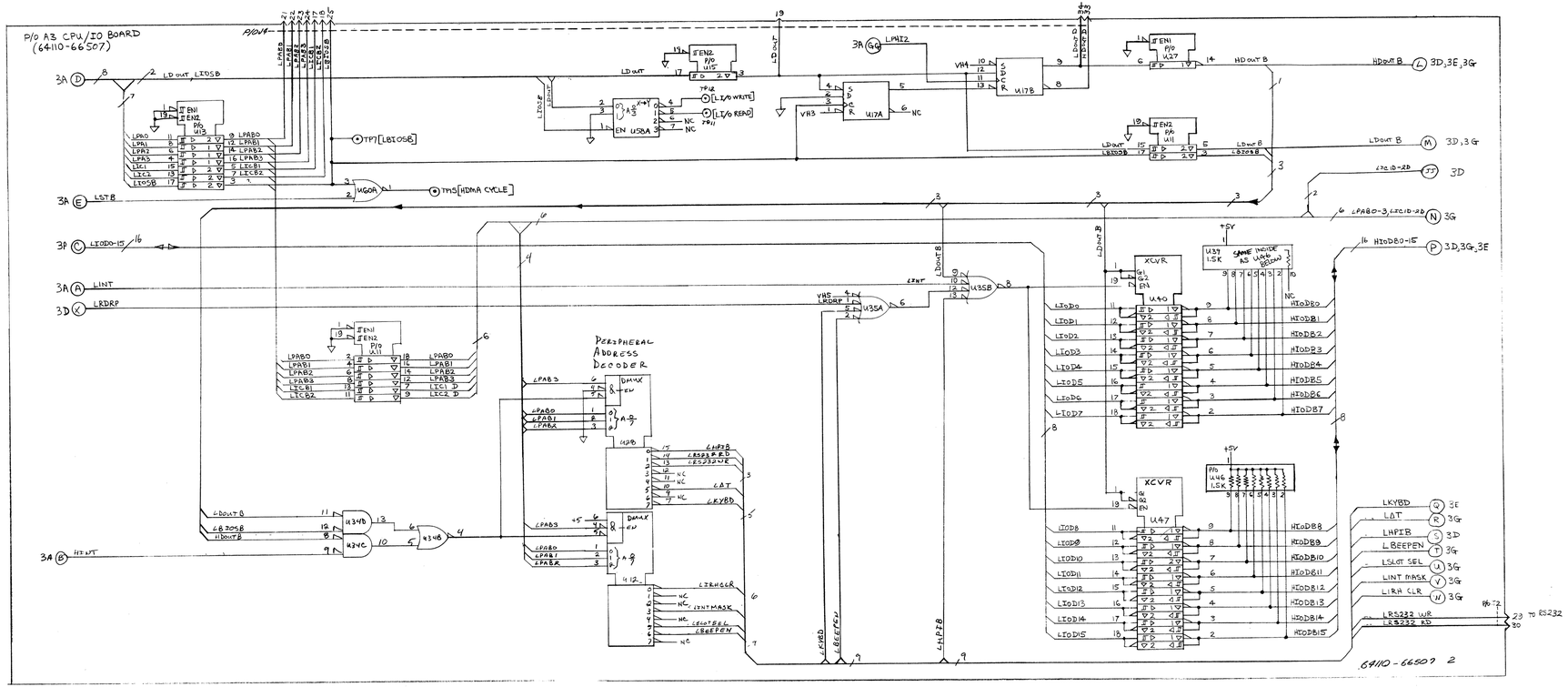


Figure 8-12.
CPU, CPU/IO Schematic 1 of 7
8-95 CI



CPU/IO Component Locator



ICs ON THIS SCHEMATIC

REF DES.	HP PART NO.	MFR PART NO.
U11,13,15	1820-2024	74LS244
U12,28	1820-1216	74LS138
U17	1820-0693	74S74
U27	1820-1917	74LS240
U34	1820-1144	74LS02
U35	1820-1205	74LS21
U39,46	1810-0276	210A152
U40,47	1820-2206	74LS640
U58	1820-1281	74LS139
U60	1820-1322	74S02

IC POWER SUPPLY CONFIGURATIONS

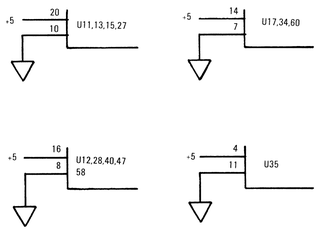
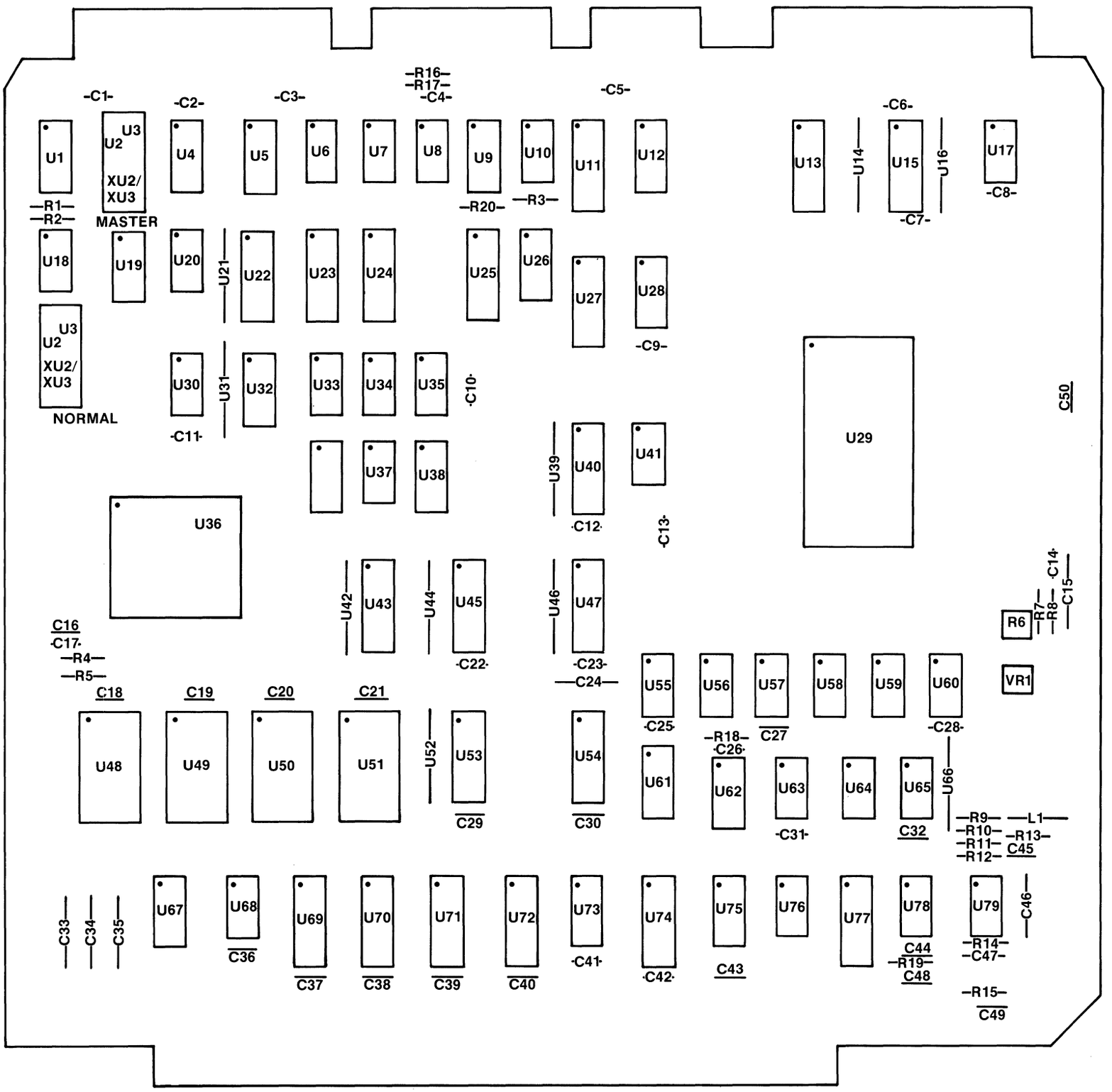
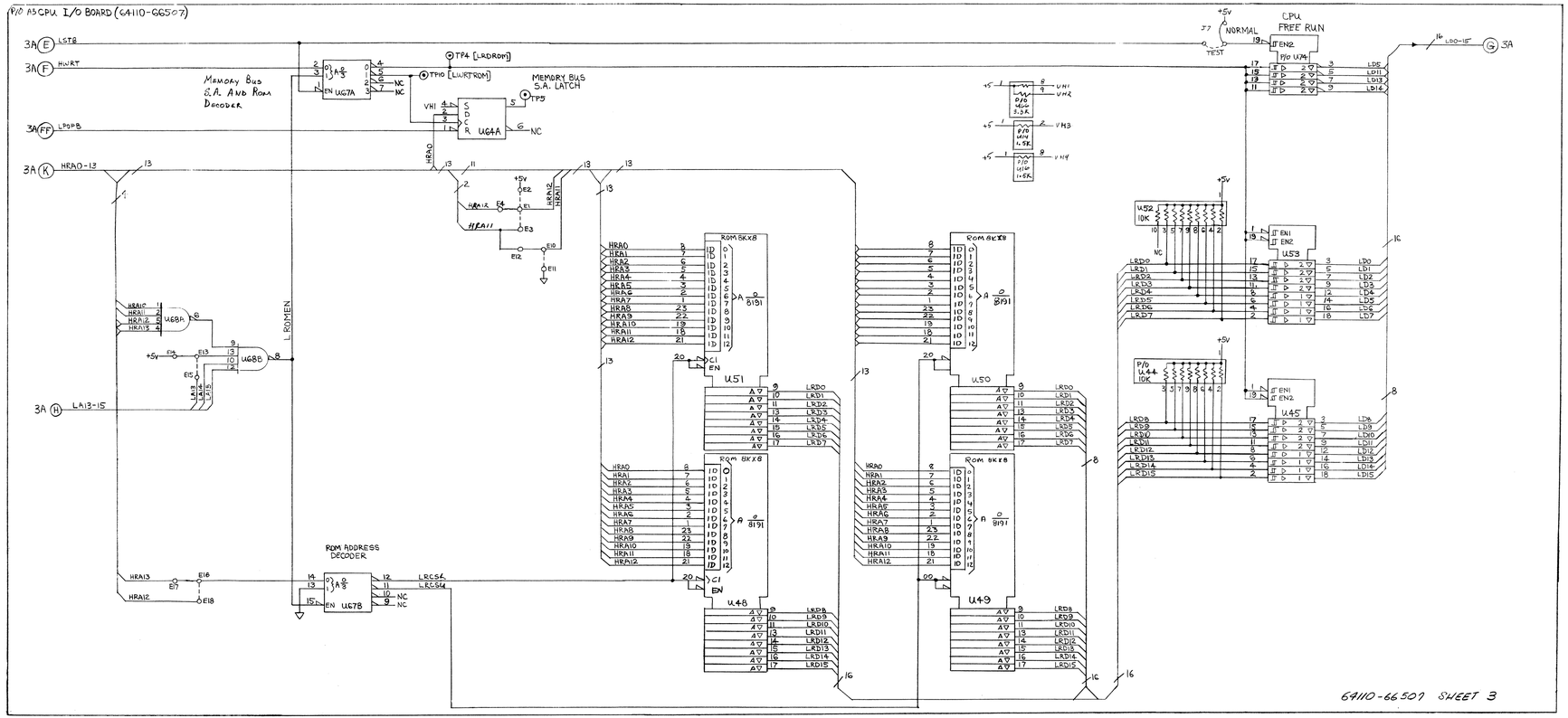


Figure 8-13.
Peripheral Address Decoder, CPU/IO Schematic 2 of 7
8-97 CI



CPU/IO Component Locator



ICs ON THIS SCHEMATIC

REF DES.	HP PART NO.	MFR PART NO.
U44,52	1810-0276	210A152
U45,53	1820-2024	74LS244
U48-51		ROMS 0-3
U64	1820-1112	74LS74
U67	1820-1281	74LS139
U68	1820-1204	74LS20
U74	1820-1917	74LS240

IC POWER SUPPLY CONFIGURATIONS

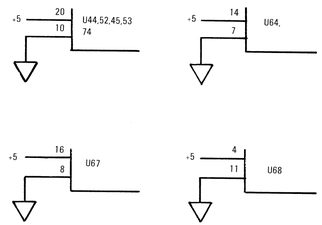
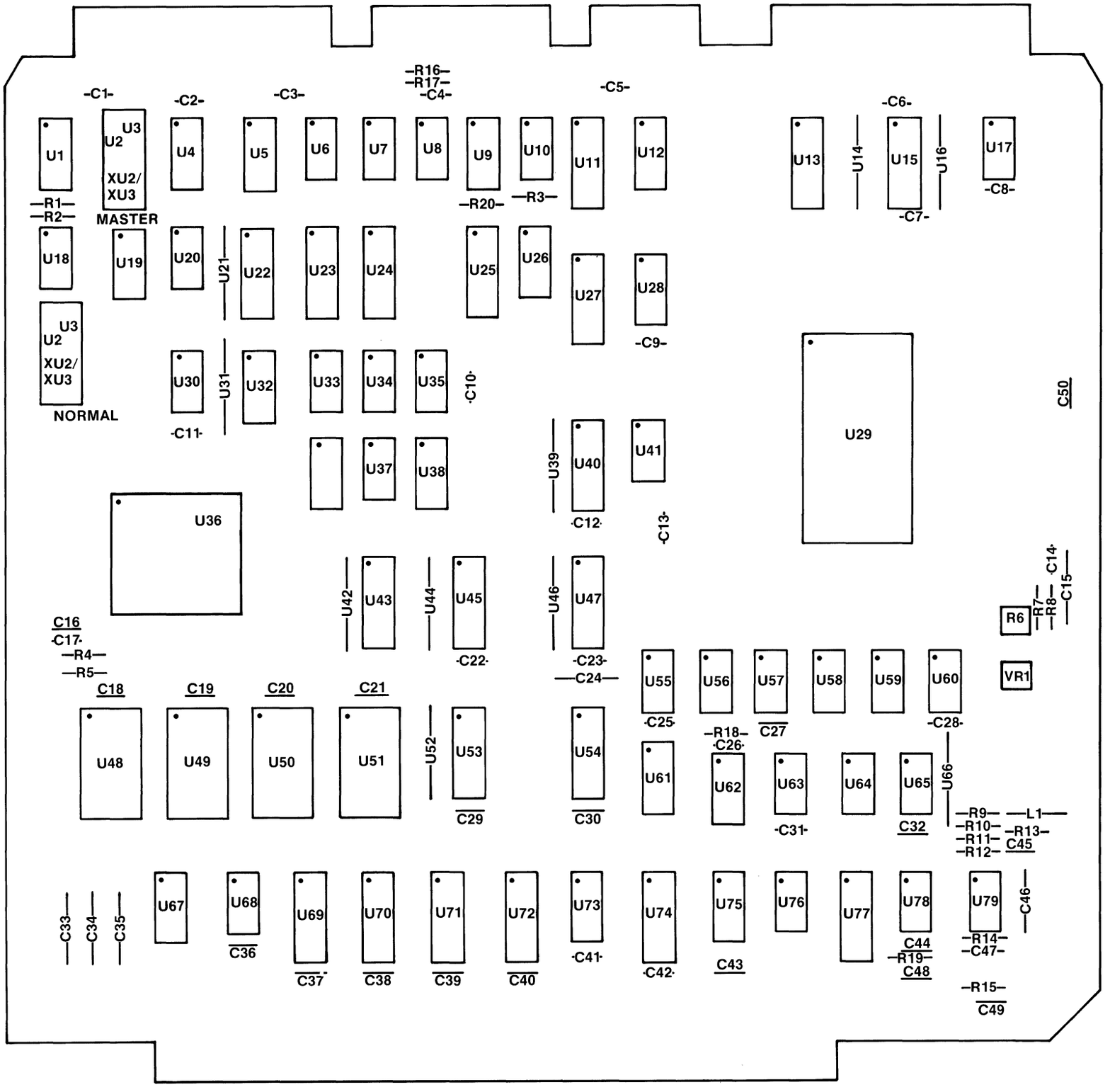
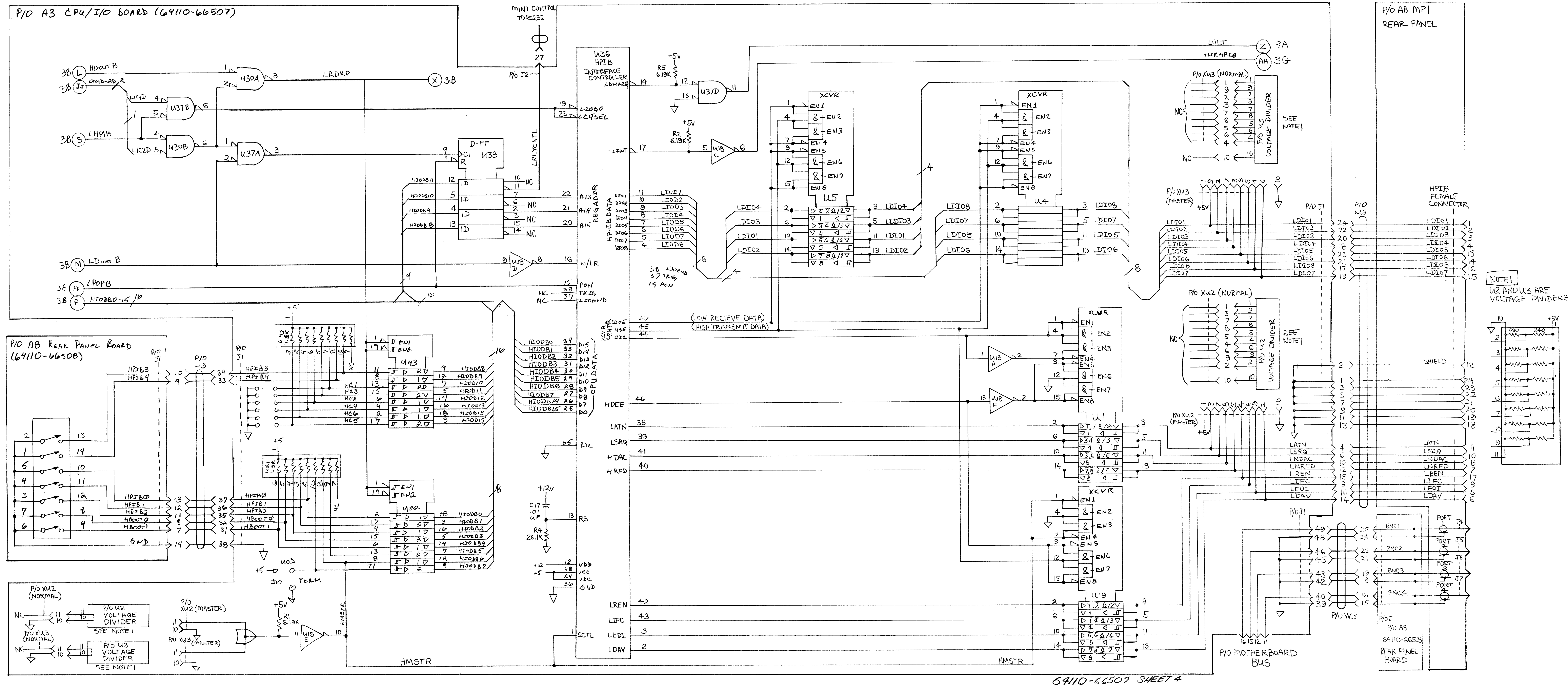


Figure 8-14.
ROM, CPU/IO Schematic 3 of 7
8-99 CI



CPU/IO Component Locator



ICs ON THIS SCHEMATIC

REF DES.	HP PART NO.	MFR PART NO.
U1,4,5,19	1820-2058	MC3448
U2,3	1810-0519	1810-0519
U18	1820-1199	74LS04
U21	1810-0276	RES PACK 1.5K
U22	1820-2024	74LS244
U30,37	1820-1208	74LS32
U36	1AA6-6004	1AA6-6004
U38	1820-1195	74LS175

PARTS ON THIS SCHEMATIC

C17
R1,2,4,5

IC POWER SUPPLY CONFIGURATIONS

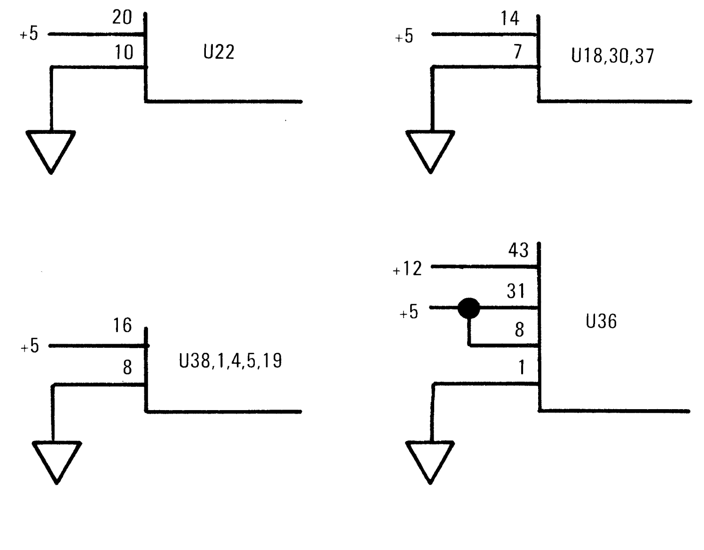
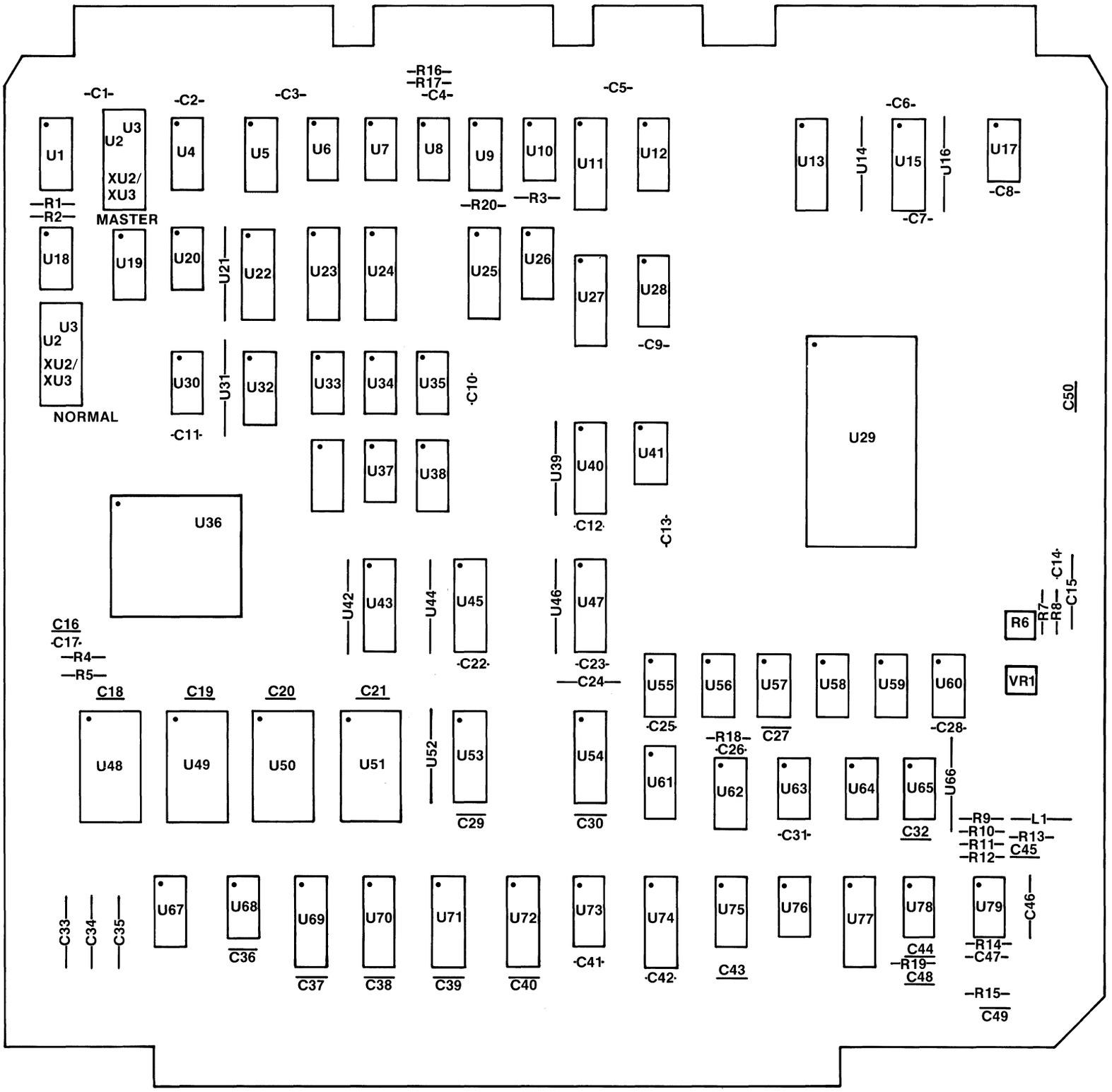
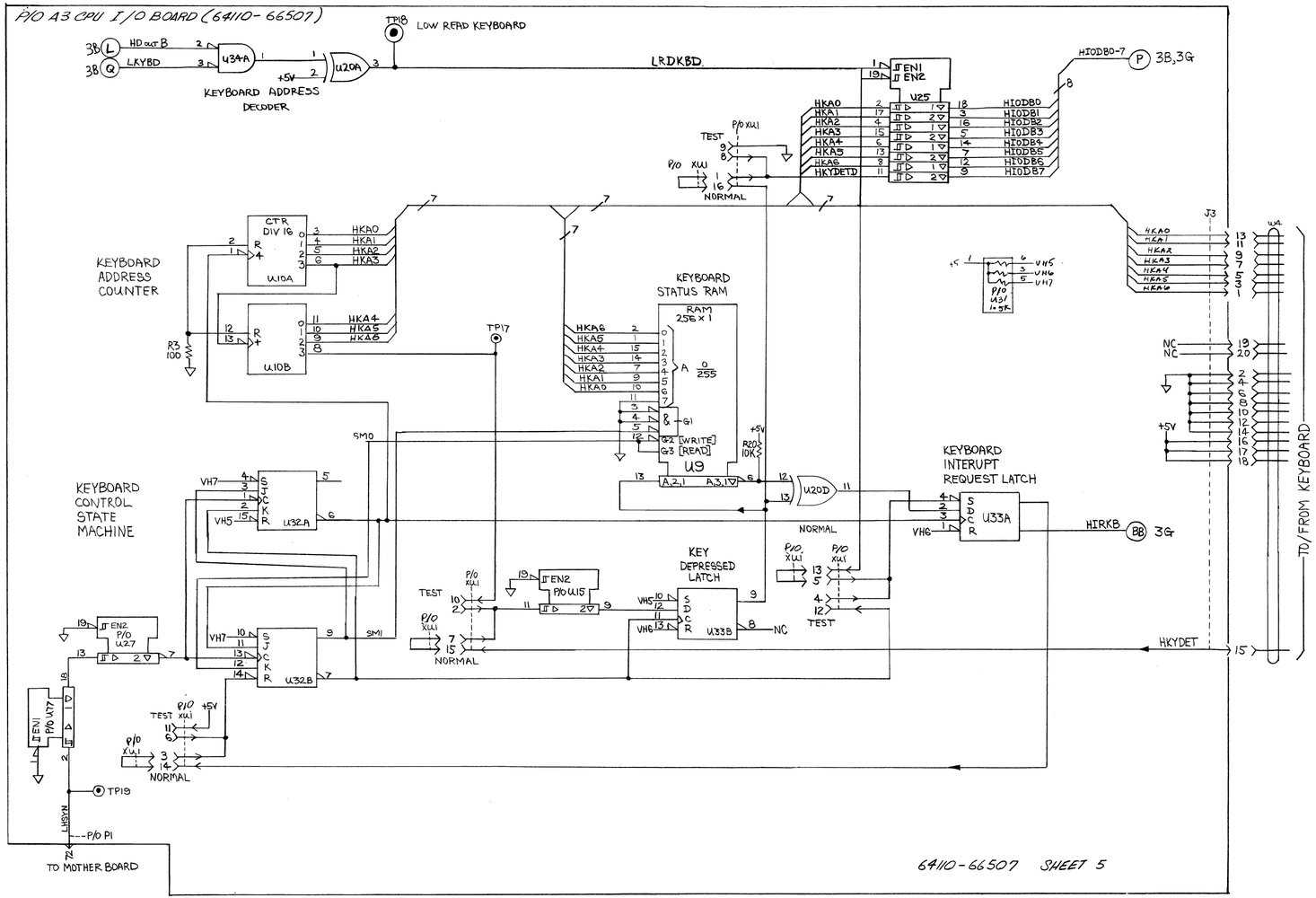


Figure 8-15.
HP-IB Controller, CPU/IO Schematic 4 of 7



CPU/IO Component Locator



ICs ON THIS SCHEMATIC

REF DES.	HP PART NO.	MFR PART NO.
U9	1819-1092	1816-1092
U10	1820-1989	74LS393
U15,25,77	1820-2024	74LS244
U20	1820-1211	74LS86
U27	1820-1917	74LS240
U32	1820-1212	74LS112
U33	1820-1112	74LS74
U34	1820-1144	74LS02

PARTS ON THIS SCHEMATIC

R3,20

IC POWER SUPPLY CONFIGURATIONS

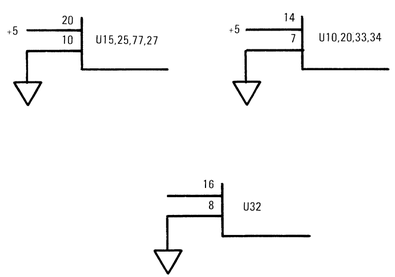
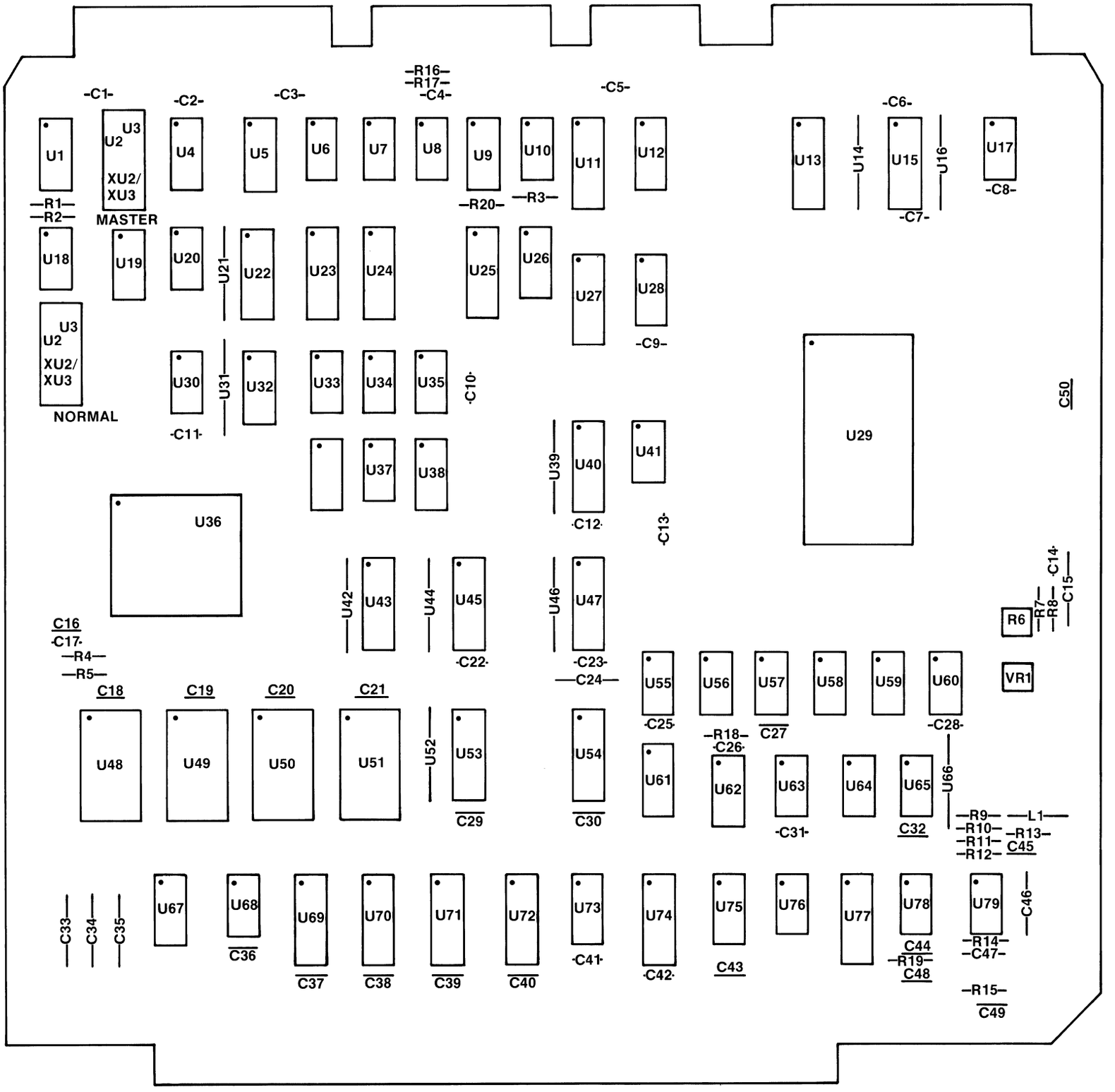
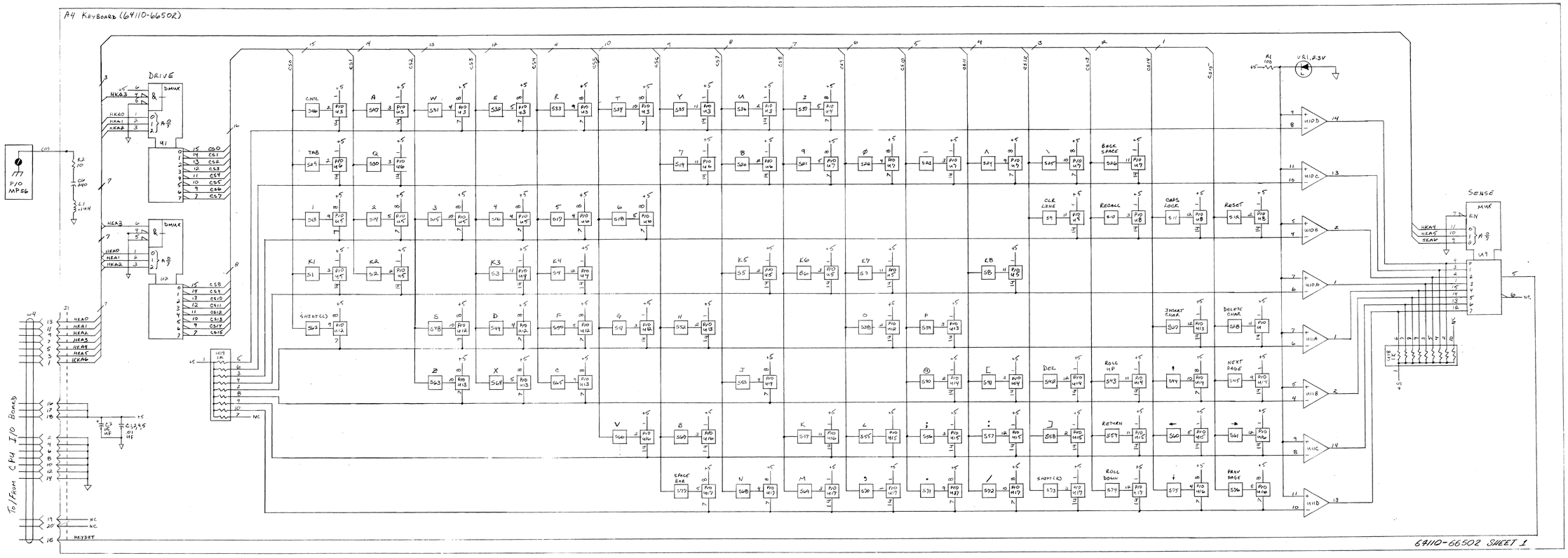


Figure 8-16.
Keyboard Scanner CPU/IO Schematic 5 of 7
8-103 CI



CPU/IO Component Locator

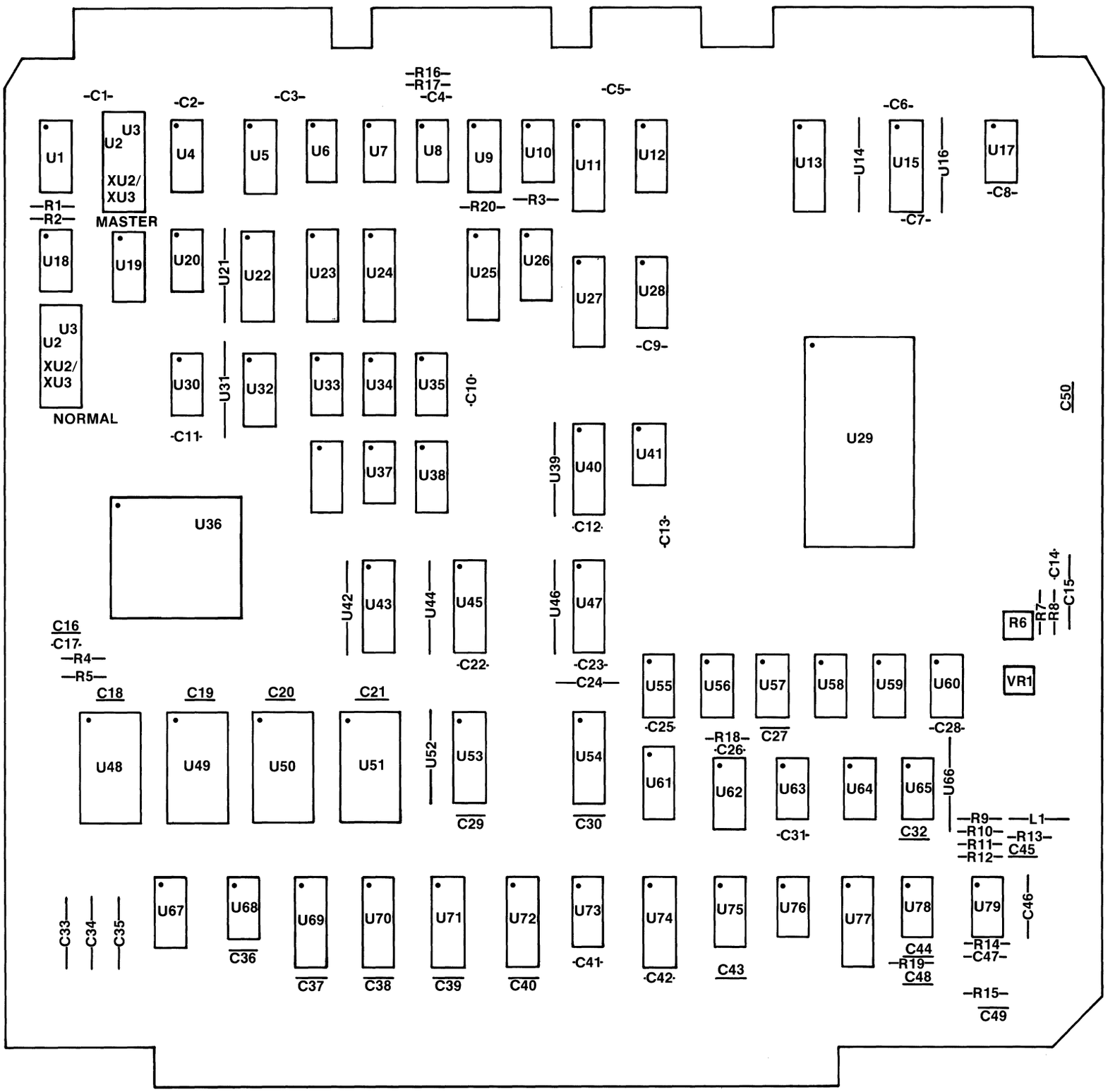


ICs ON THIS SCHEMATIC

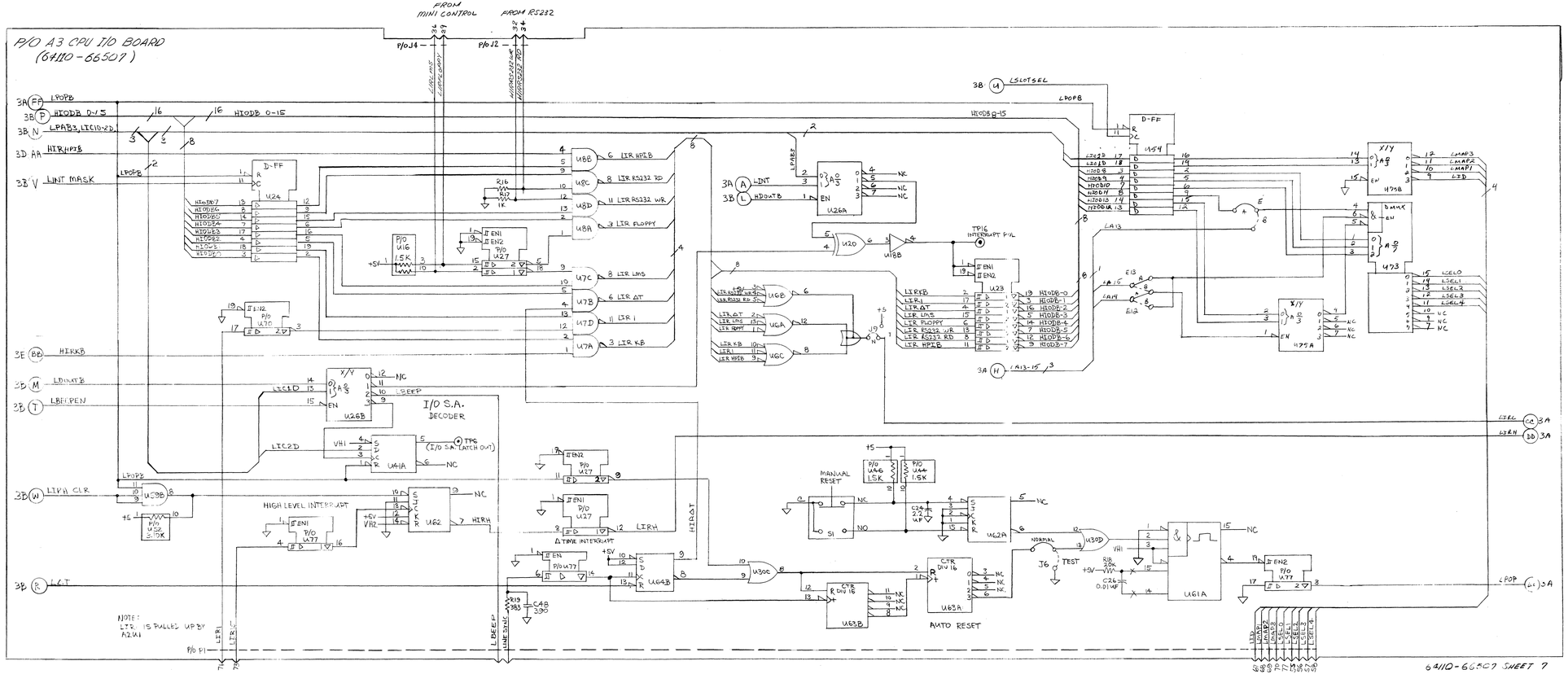
REF DES.	HP PART NO.	MFR PART NO.
U1,2	1820-1240	74LS138
U9	1820-1217	74LS151
U10,11	1826-0138	LM339
U3-8,12-17	1906-0229	MC1107D

R1,2,-L1
C1,6,-VR1

Figure 8-17.
Keyboard, CPU/IO Schematic 6 of 7



CPU/IO Component Locator



ICs ON THIS SCHEMATIC

REF DES.	HP PART NO.	MFR PART NO.
U6,59	1820-1243	74LS15
U7,8	1820-1197	74LS00
U16,42,46	1810-0276	210A152
U18	1820-1199	74LS04
U20	1820-1211	74LS86
U23,27,70	1820-1917	74LS240
U24,54	1820-1730	74LS273
U25,77	1820-2024	74LS244
U26	1820-1281	74LS139
U30	1820-1208	74LS32
U41,64	1820-1112	74LS74
U44,52	1810-0288	210A103
U61	1820-1322	74S02
U62	1820-1212	74LS112
U63	1820-1240	74S138

PARTS ON THIS SCHEMATIC

C24,26,48 R16,17,19,20

IC POWER SUPPLY CONFIGURATIONS

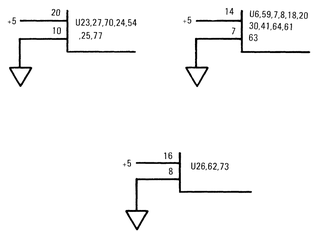


Figure 8-18.
LPOP Generator/Interrupt Logic, CPU/IO Schematic 7 of 7

8-321. DISPLAY CONTROLLER BLOCK DESCRIPTION.

8-322. The display controller board serves two main functions,

1. Provides the processor with a read/write (RAM) memory.

2. Generates the video control signals.

8-323. The address range alloted to the RAM is from 8002 (hexadecimal) to FFFF. A part of this memory (from F9F0 to FF00) is dedicated to storing display information. See table 8-1.

8-324. RAM WRITE BLOCK DESCRIPTION.

8-325. The processor writes data into the RAM by placing the address of the location to be written to on the address bus, selecting the memory and write functions by means of the RAM cycle selector/-generator circuitry, and then presenting the data to be stored on the data bus. The RAM cycle selector/generator circuitry is responsible for gating the address through to the RAM address lines. Since the RAM address lines are multiplexed into two 7-bit segments, the RAM cycle selector/generatormust also control the byte select function (U49-50).

8-326. RAM READ BLOCK DESCRIPTION.

8-327. The processor reads data from the RAM by placing the address of the location to be read on the address bus, selecting the memory and read function and then gating the RAM data out to the data bus through buffers U31,U85, and U84. The RAM cycle selector/generator and the RAM control and decode are responsible for the correct selection of the RAM output buffers.

8-328. DISPLAY SETUP BLOCK DESCRIPTION.

8-329. The CRT controller U33 must be programmed with display parameters, i.e. number of characters per row, number of rows, and number of lines per character row, before a display can be generated. The bi-directional buffer U85, allows the processor to directly load the display parameters into the CRT controller. This programming takes place very early in the systems operating program and is latched into the CRT controller, thus occuring only once during power up.

8-330. DISPLAY OPERATION DESCRIPTION.

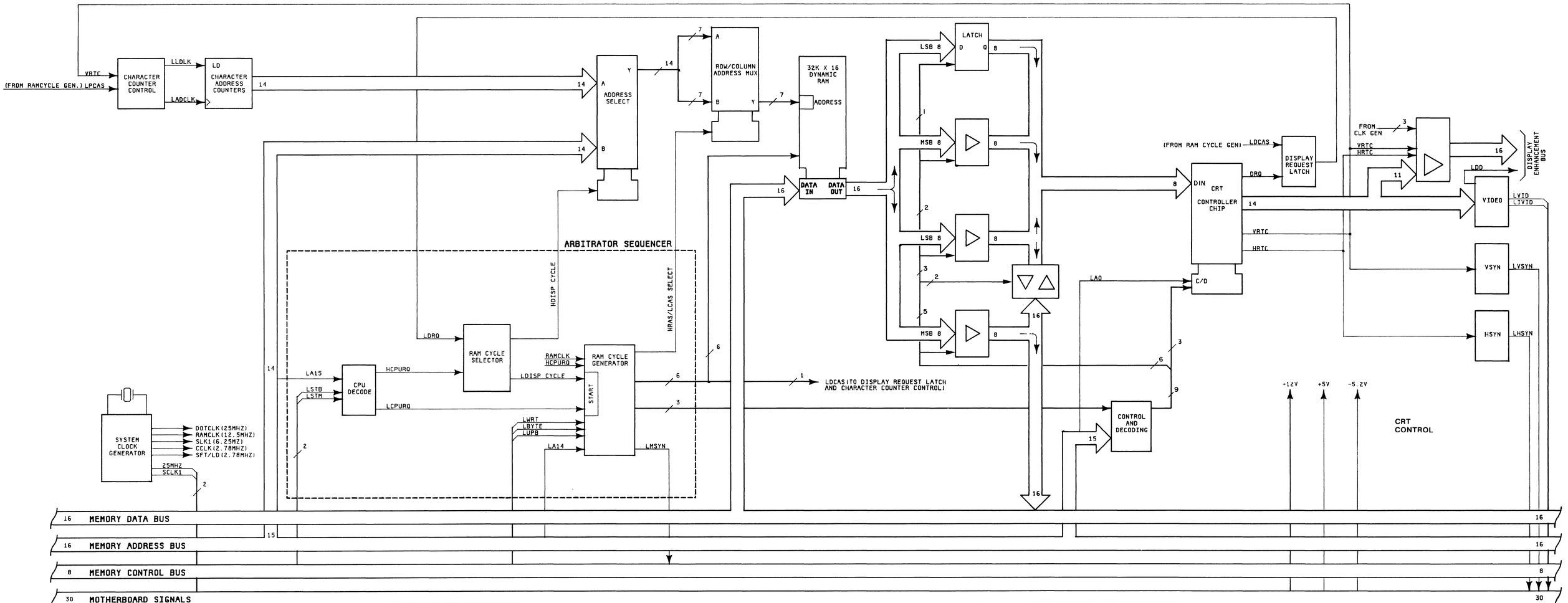
8-331. A display operation is similar to a RAM read operation. However, the address for the display data is not taken from the address bus, but from the binary counters U62-64. When the binary counters are reset by the LLDCNT (Load Counter) signal, the address of the

first display location is loaded into the counters. The RAM cycle selector/generator circuitry now gates the display address, instead of the address bus, through to the address input lines of the RAM.

8-332. The data out is now gated through the display buffers U32 and U46. Since the CRT controller can only accept an 8 bit slice of data at a time, U42 latches half the 16 bit output of the RAM and passes its data after the data from U32 has been accepted by the CRT controller. This sequence also saves the processor the task of calling that display address again to retrieve the other 8 bits. The saved time frees the RAM for a refresh operation.

8-333. The CRT controller (U33) primary function is to refresh the display by buffering the display data and to keep track of the character position. The CRT controller also generates the vertical and horizontal sync pulses used to trigger the sweep circuits of the display driver board. The CRT controller outputs a code to the character generating ROM at U74 that describes the character to be displayed and what horizontal line is to be sent to the video drive circuits.

8-334. The character generating ROM parallel loads the display information into the shift registers U89 and U90, which serially output the display information to the display driver board.



BLOCK DIAGRAM FOR THE 64110-66519
DISPLAY CONTROLLER

1/82

Figure 8-19.
Display Controller Block Diagram
8-111/(8-112 blank) DC

8-335. DISPLAY CONTROLLER SCHEMATIC DESCRIPTION.

8-336. The following paragraphs describe functions shown on figures 21 through 24.

8-337. The display controller board produces signals for the CRT, contains a system clock and RAM which is shared by the CPU. The RAM cycle selector/generator circuitry controls timesharing of this RAM between the display controller board and the CPU.

8-338. Information to be displayed on the screen is written into the RAM space by the CPU at the addresses that are addressed by the counters for the display circuitry. Fourteen address bits are required to decode one location in RAM. Signal LA14 is used to select the upper or lower banks of RAM.

8-339. RAM WRITE SCHEMATIC DESCRIPTION.

8-340. The CPU initiates a RAM write function by pulling address bit 15 (LA15) low. Address bit 15 is sent to the RAM selector/generator circuitry producing a gating signal, output from U18, pin 7. This gating signal selects the CPU address lines LA0-13 from the address select circuit. The address lines (LA0-13) are input to the byte select circuit and the upper or lower byte is selected by a gating signal from U48A, pin 5 to produce output address line LA0-6.

8-341. Address lines A0-6, sent to the RAM circuit determine where data (LD0-15) from the CPU will be stored in RAM. The row address bits are strobed into the upper or lower bank of RAM by means of clocking signals LURAS and LLRAS respectively. The column address bits are strobed into the upper or lower bank of RAM by clocking signals LUCAS and LLCAS respectively. Control signals LWLB and LWUB determine whether data is written into the upper or lower byte.

8-342. RAM READ SCHEMATIC DESCRIPTION.

8-343. The CPU reads data from the RAM by placing the address of the location to be read on the address bus (LA0-14). Data (LD0-15) is read from the RAM when signals LWLB and LWUB are inactive (high). Data LD0-15 is gated to the data bus through buffers U31, U85, and U84. The arbitrator sequencer and RAM data out routing circuits select the RAM output buffers U31, U84, and U85. Data is routed to the CPU on the LD0-15 bus.

8-344. DISPLAY SCHEMATIC DESCRIPTION.

8-345. The CRT controller (U33) is loaded with display parameters (LD0-7) directly from the CPU by means of U85. The display parameters are loaded once during power up. The CRT controllers primary function is to refresh the display and keep track of character position.

8-346. The address for display information is taken from the character address counters circuit (U62 thru 64). Signal Load Counter (LLDCNT) resets the address counters and the address of the first display location is loaded. This address is set to the address select circuitry. The RAM cycle selector/generator circuitry now gates the display address, instead of the address bus through the Row/Column Address MUX circuitry to the address input lines of the RAM.

8-347. The output data (LD0-7) is gated through the display controller (U33). Since the CRT controller can accept only 8 bits of data at a time, U46 latches half of the 16 bit output of the RAM. Data from U46 is accepted by the CRT controller after the data from U32 is accepted. The CRT controller then produces an address which is sent to the character generator ROM circuit U74, describing the character to be displayed and what horizontal line is to be sent to the video drive circuits. The character generator ROM circuit then parallel loads the display information into the shift register circuit (U89 and U90). The character patterns are shifted to the output circuitry in serial form.

8-348. DISPLAY CONTROLLER TROUBLESHOOTING.

8-349. RAM TROUBLESHOOTING.

8-350. RAM troubleshooting is divided into simple RAM failure and RAM refresh failure. Different circuitry may be causing the different failure types.

Table 8-31. RAM Troubleshooting

REFRESH ERROR ON DISPLAY....go to RAM refresh failure troubleshooting table.

SIMPLE RAM ERROR ON DISPLAY....go to simple RAM failure troubleshooting table.

ILLEGIBLE DISPLAY....use signature analysis test loop determination table to discern failure type.

REFRESH ERROR....go to RAM refresh failure troubleshooting table.

SIMPLE RAM ERROR....go to simple RAM failure troubleshooting table.

Table 8-32. Simple RAM Failure Troubleshooting (1 of 3)

STEP 1. LEGIBLE DISPLAY?

YES....replace RAM(s)

DOESN'T FIX PROBLEM....go to step 2. Since the RAM is used to store display information, the failure may be corrupting the displayed failure information. The SA RAM failure summary table will give you this information.

NO....go to step 2. Since the RAM is used to store display information, the failure may be corrupting the displayed failure information. The SA RAM failure summary table will give you this information.

STEP 2. RAM FAILURE SUMMARY....use the RAM failure summary table to find failing RAM IC(s) and replace.

DOESN'T FIX PROBLEM....go to step 3. The failure may be due to a failure in the data path to the RAM, addressing or control. CPU RAM writes will allow you to check for this type of failure.

Table 8-32. Simple RAM Failure Troubleshooting (2 of 3)

STEP 3. CPU RAM WRITES....use signature analysis setup K table (CPU RAM writes setup). First, check the ability of the CPU to write information to the RAM.

GOOD Vh....take signatures

BAD SIGS ON RAM TIMING AND CONTROL SIGNALS....use signature analysis setup U table (RAM cycle selector/generator setup) to troubleshoot. If these signals are not correct information may not be written to or read from RAM correctly. Since these signals are mostly Vh and 0000, an error in these signals may not be detected.

BAD SIGS ON MEMORY DATA OR ADDRESS BUS.
These bad signatures indicate a failure of the CPU to write correct data to RAM. This could be due to the CPU, the connections from the CPU to the RAM, the pullups on the MB, the address latches on the CPU I/O board, any IC that connects to the buses, or the address multiplexers.

NO BAD SIGNATURES....go to step 4. The addresses checked in CPU RAM writes was only during the CAS strobe portion of the address. A failure in the row/column multiplexers might not be detected. CPU RAS address check will let you find a failure of this type.

BAD Vh....troubleshoot the signature analysis latch and the CPU timing and control circuitry on the CPU,I/O board using a scope.

STEP 4. CPU RAS ADDRESS CHECK....use signature analysis setup L table (CPU AS address check setup).

BAD Vh....go to signature analysis setup U table (RAM cycle selector/generator setup) to troubleshoot.

GOOD Vh.

NO BAD SIGS....go to step 5.

TIMING AND CONTROL SIGNATURE ERRORS....use signature analysis setup U table (RAM cycle select/generator setup) to troubleshoot.

Table 8-32. Simple RAM Failure Troubleshooting (3 of 3)

STEP 5. ADDRESS SIGNATURE ERRORS....use signature analysis setup M table (CPU RAM reads setup). Before signatures on the output of the RAM can be correct, addressing and data from the CPU must be correct. You should have already checked these functions using CPU RAM writes and CPU RAS address check.

BAD Vh.

NO CLOCK SIGNAL....go to signature analysis setup U table (RAM cycle selector/generator setup) to troubleshoot.

NO START/STOP SIGNAL....go to ROM troubleshooting table.

GOOD Vh.

RAM or RAM ADDRESS TIMING AND CONTROL SIG ERRORS....go to signature analysis setup U table (RAM cycle selector/generator setup) to troubleshoot.

DATA CONTROL AND DECODE SIG. ERRORS....use signature analysis setup N table (RAM access control and decode setup) to troubleshoot.

DATA OR ADDRESS SIG ERRORS....troubleshoot.

8-351. RAM REFRESH FAILURE TROUBLESHOOTING.

8-352. RAM refresh is accomplished by the display accesses to RAM. Circuitry in the display counters causes a RAS address for each of the 128 row addresses of both banks of RAM to be generated as the display accesses the RAM for display information. Troubleshooting in this section will allow you to isolate problems with individual RAM ICs or with the display address counters, CRT controller, and control circuitry.

8-353. Retention of the RAM ICs may be greater than 1 sec. Even with refresh not operating, only a few RAM ICs may fail the RAM refresh test. Taking the key signatures in display RAS Address check will verify that the refresh circuitry is working.

Table 8-33. RAM Refresh Failure Troubleshooting (1 of 2)

STEP 1. LEGIBLE DISPLAY?

YES....replace failing RAM IC(s)

DOESN'T FIX PROBLEM....go to step 2. Since the RAM is used to store display information, the failure may be corrupting the displayed failure information. The signature analysis RAM failure summary table will give you this information.

NO....go to step 2. Since the RAM is used to store display information, the failure may be corrupting the displayed failure information. The signature analysis RAM failure summary table will give you this information.

STEP 2. RAM FAILURE SUMMARY....use signature analysis RAM failure summary table to find failing RAM IC(s) and replace.

DOESN'T FIX PROBLEM....go to step 3. Refresh is accomplished by the display accesses to RAM, CRT controller outputs-hardware setup will check to see that the CRT controller is operating correctly.

STEP 3. CRT CONTROLLER OUTPUTS-HARDWARE....use signature analysis setup 0 table (CRT controller outputs-hardware loop setup).

BAD Vh.

NO CLOCK....troubleshoot.

NO START/STOP....go to step 5.

VALID Vh.

CRT CONTROLLER IC PINS 1-5, 7-8 SIGNATURE ERRORS....go to step 5. The CRT controller is not operating correctly, CPU program of the CRT controller will allow you to verify that the CRT controller is being programmed correctly by the CPU.

OTHER SIGNATURE ERRORS....troubleshoot

NO BAD SIGNATURES....go to step 4. If the display address counters are not working correctly, refresh may not be done. Addresses are checked only during the RAS portion of the address since the RAS addressing is what does the refresh for the RAM.

Table 8-33. RAM Refresh Failure Troubleshooting (2 of 2)

STEP 4. DISPLAY RAS ADDRESS CHECK....use signature analysis setup R table (display RAS address check setup).

BAD Vh.

NO CLOCK....use signature analysis setup U table (RAM cycle selector/generator setup) to troubleshoot.

NO START/STOP....go to step 5.

VALID Vh.

ADDRESS TIMING AND CONTROL SIG ERRORS....use signature analysis setup U table (RAM cycle selector/generator setup) to troubleshoot.

OTHER SIG ERRORS....troubleshoot.

STEP 5. CPU PROGRAM OF CRT CONTROLLER....use signature analysis setup P table (CPU program of CRT controller setup).

BAD Vh.

NO CLOCK....use signature analysis setup N table (RAM access control and decode setup) to troubleshoot.

NO START/STOP....go to ROM troubleshooting table, step 4.

VALID Vh.

BUFFER TIMING AND CONTROL SIG ERRORS....use signature analysis setup N table (RAM access control and decode setup) to troubleshoot.

OTHER SIG ERRORS....troubleshoot.

NO BAD SIGNATURES....check power supplies and clock to CRT controller. If outputs are bad and all inputs are good, replace the CRT controller.

Table 8-34. Display Troubleshooting

ARE THE DISPLAY AND CHARACTERS THE CORRECT SIZE AND INTENSITY?.... First, isolate the problem to the display controller or driver boards.

YES....go to display controller troubleshooting table. The correct size indicates that the driver boards are operating correctly. If the display is wrong, it is because the display controller is sending the wrong video information.

NO....are HSYN, VSYN, and VIDEO signals correct coming from the display controller board?

YES....troubleshoot display driver

NO....go to display controller troubleshooting table.

Table 8-35. Display Controller Troubleshooting (1 of 2)

STEP 1. CRT CONTROLLER OUTPUTS-DISPLAY TEST....use signature analysis setup S table (CRT controller outputs-display test setup).

BAD Vh.

NO CLOCK....troubleshoot with scope

NO START/STOP....go to step 3.

VALID Vh.

CRT CONTROLLER IC PINS 1-5, 7-8 SIGNATURE ERRORS....go to step 3. The CRT controller is not operating correctly, CPU program of the CRT controller will allow you to verify that the CRT controller is being programmed correctly by the CPU.

CRT CONTROLLER IC HCC0-6 OUTPUT SIGNATURE ERRORS....go to step 2. If the character code outputs are wrong, it may be because the CRT controller is getting wrong information from RAM

OTHER SIGNATURE ERRORS....troubleshoot.

NO BAD SIGNATURES....use scope to troubleshoot video circuitry. The video circuitry runs at 25 MHz; this is too fast for signature analysis so a scope is required to troubleshoot.

Table 8-35. Display Controller Troubleshooting (2 of 2)

STEP 2. CRT CONTROLLER READ FROM RAM....use signature analysis setup T table (CRT controller read from RAM setup).

BAD Vh.

NO CLOCK....use signature analysis setup U table (RAM cycle selector/generator setup) to troubleshoot.

NO START/STOP....use signature analysis setup O table (CRT controller outputs-hardware loop setup) to troubleshoot.

VALID Vh.

RAM TIMING AND CONTROL OR ADDRESS MUX CONTROL SIG ERRORS.. use signature analysis setup U table (RAM cycle selector-generator setup) to troubleshoot.

RAM DATA OUTPUT SIGNATURE ERRORS ONLY....use signature analysis setup R table (display RAS address check setup) to check RAS address to RAM. If no errors are found, suspect the RAM or any IC connected to the RAM memory data bus.

OTHER BAD SIGNATURES....troubleshoot.

NO BAD SIGNATURES....check power supplies and clock to CRT controller. If outputs are bad and all inputs are good, replace the CRT controller.

STEP 3. CPU PROGRAM OF CRT CONTROLLER....use signature analysis setup P table (CPU program of CRT controller).

BAD Vh.

NO CLOCK....signature analysis setup N table (RAM access control and decode setup) to troubleshoot.

NO START/STOP....go to ROM troubleshooting table, step 4.

BUFFER TIMING AND CONTROL SIG ERRORS....use signature analysis setup N table (RAM access control and decode setup) and signature analysis setup U table (RAM cycle selector/generator setup) to troubleshoot.

OTHER SIG ERRORS....troubleshoot.

NO BAD SIGNATURES....check power supplies and clock to CRT controller. If outputs are bad and all inputs are good, replace the CRT controller.

Table 8-36. Signature Analysis RAM Failure Summary (1 of 2)

LOOPNAME: POWER ON RAM TEST FAILURE OR REFRESH FAILURE

If a failure is detected during the power on RAM self-test, the test enters a signature analysis loop that writes and reads RAM and stimulates the CRT controller. The loop also outputs the error masks onto the memory data bus and the CPU attempts to display the failing IC numbers.

SETUP NAME: RAM FAILURE SUMMARY

Since display information is stored in RAM, the output to the display of the failing RAM IC numbers may be illegible. This setup allows the taking of signatures on the memory data bus during the time that the error masks are present on the memory data bus. The value of the signature and the data bit may be decoded to isolate the failing RAM IC numbers.

Executing power on RAM test or refresh failure loop

ST/SP/START: A3TP5, rising edge (MEM SA LATCH)

QUAL/STOP: A3TP5, rising edge (MEM SA LATCH)

CLOCK: A3TP10, rising edge (MEM SA CLOCK)

Vh = 0007

Table 8-36. Power On RAM or Refresh Test Failure (2 of 2)

RAM Failure Summary

	Signature			
	0000	0002	0004	0006
Bit		Failing RAM		
LD0	no fail	U23	U51	U23, U51
LD1	no fail	U24	U52	U24, U52
LD2	no fail	U25	U53	U25, U53
LD3	no fail	U26	U54	U26, U54
LD4	no fail	U27	U55	U27, U55
LD5	no fail	U28	U56	U28, U56
LD6	no fail	U29	U57	U29, U57
LD7	no fail	U30	U58	U30, U58
LD8	no fail	U38	U65	U38, U65
LD9	no fail	U39	U66	U39, U66
LD10	no fail	U40	U67	U40, U67
LD11	no fail	U41	U68	U41, U68
LD12	no fail	U42	U69	U42, U69
LD13	no fail	U43	U70	U43, U70
LD14	no fail	U44	U71	U44, U71
LD15	no fail	U45	U72	U45, U72

Table 8-37. Signature Analysis Setup K (1 of 2)

LOOPNAME: POWER ON RAM TEST FAILURE

If a failure is detected during the power on RAM self-test, the test enters a signature analysis loop that writes and reads RAM and stimulates the CRT controller. The loop also outputs the error masks onto the memory data bus and the CPU attempts to display the failing IC numbers.

SETUP NAME: CPU RAM WRITES

This setup allows the checking of the CPU data path to the RAM during the write of data to RAM by the CPU. It also allows the checking of the CPU address path from the CPU to the address multiplexers. The mainframe is forced to execute the power on RAM failure test loop by removing RAM IC A5U23.

Remove RAM IC A5U23

Executing power on RAM test failure loop

ST/SP/START: A3TP5, rising edge (MEM SA LATCH)

QUAL/STOP: A3TP5, falling edge (MEM SA LATCH)

CLOCK: A3TP13, rising edge (LMEM WRITE)

Vh = H37A

Table 8-37. Signature Analysis Setup K (2 of 2)

Node	Signature	Node	Signature
U 16- 6	0001	U 85-11	7045
U 16- 8	0001	U 85-12	P6FF
		U 85-13	C9HH
U 23- 3	0001	U 85-14	3H08
U 23- 4	0001	U 85-15	P1H6
U 23-15	1A8H	U 85-16	4F3A
		U 85-17	2AU8
U 37- 3	0001	U 85-18	3121
U 37- 6	F9U6		
U 37- 8	0001		
U 37-11	1A8H		
U 38- 3	0001		
U 51- 4	0001		
U 51-15	F9U6		
U 79- 2	63F3		
U 79- 5	P8FC		
U 79-11	61C1		
U 80- 2	HA56		
U 80- 5	44P6		
U 80-11	8A4P		
U 80-14	1P30		
U 81- 2	F7PA		
U 81- 5	683U		
U 81-11	U7H3		
U 82- 2	6U3A		
U 82- 5	87F2		
U 82-11	6019		
U 82-14	U08C		
U 84- 3	728H		
U 84- 5	UH82		
U 84- 7	UF05		
U 84- 9	1UPA		
U 84-12	9093		
U 84-14	P58U		
U 84-16	84H6		
U 84-18	F35F		

Table 8-38. Signature Analysis Setup L (1 of 2)

LOOPNAME: POWER ON RAM TEST FAILURE

If a failure is detected during the power on RAM self-test, the test enters a signature analysis loop that writes and reads RAM and stimulates the CRT controller. The loop also outputs the error masks onto the memory data bus and the CPU attempts to display the failing IC numbers.

SETUP NAME: CPU RAS ADDRESS CHECK

This setup allows the checking of CPU addressing during the RAS address to RAM.

Executing power on RAM test failure loop

ST/SP/START: A3TP5, rising edge (MEM SA LATCH)

QUAL/STOP: A3TP5, falling edge (MEM SA LATCH)

CLOCK: A5TP11, rising edge (HPRAS)

Vh = 7H37

Table 8-38. Signature Analysis Setup L (2 of 2)

Node	Signature	Node	Signature
U 16- 6	7H37	U 50- 4	0UH9
U 16- 8	7H37	U 50- 7	0337
		U 50- 9	7143
U 18- 7	0000	U 50-12	0U51
U 18-11	0000		
U 18-12	0000	U 79- 2	2HP3
		U 79- 4	50H4
U 23- 3	PUC5	U 79- 5	626H
U 23- 4	0000	U 79- 7	1U5A
U 23- 5	0U51	U 79- 9	6A39
U 23- 6	0337	U 79-11	170P
U 23- 7	7143		
U 23-10	38HU	U 80- 2	0UH9
U 23-11	40P0	U 80- 4	72PP
U 23-12	0UH9	U 80- 5	0337
U 23-13	8C0C	U 80- 7	7P00
U 23-15	UCA3	U 80- 9	0F74
		U 80-11	7143
U 37- 3	0000	U 80-12	7266
U 37- 6	UCA3	U 80-14	0U51
U 37- 8	0000		
U 37-11	8694	U 81- 2	8C0C
		U 81- 4	U63F
U 38- 3	PUC5	U 81- 5	38HU
		U 81- 7	45P8
U 51- 4	0000	U 81- 9	3HH7
U 51-15	UCA3	U 81-11	40P0
U 48- 4	0000	U 82- 2	96CP
U 48- 5	7H37	U 82- 4	PC89
		U 82- 5	HACA
U 49- 4	8C0C	U 82- 7	A78H
U 49- 7	38HU	U 82- 9	C017
U 49- 9	40P0	U 82-11	FH20
		U 82-12	3C0A
		U 82-14	463H

Table 8-39. Signature Analysis Setup M (1 of 3)

LOOPNAME: POWER ON RAM TEST FAILURE

If a failure is detected during the power on RAM self-test, the test enters a signature analysis loop that writes and reads RAM and stimulates the CRT controller. The loop also outputs the error masks onto the memory data bus and the CPU attempts to display the failing IC numbers.

SETUP NAME: CPU RAM READS

This setup allows the checking of data as it is being read from RAM by the CPU, addressing by the CPU, and CAS addressing to RAM.

Executing power on RAM test failure loop

ST/SP/START: A3TP5, rising edge (MEM SA LATCH)

QUAL/STOP: A3TP5, falling edge (MEM SA LATCH)

CLOCK: A5TP15, rising edge (LCPU READ)

Vh = P000

Table 8-39. Signature Analysis Setup M (2 of 3)

Node	Signature	Node	Signature
U 1- 8	P000	U 31- 1	0000
		U 31- 2	A247
U 7- 3	P000	U 31- 3	8AAA
		U 31- 4	5AH3
U 15- 4	H555	U 31- 5	P444
U 15- 5	high	U 31- 6	4013
U 15- 6	high	U 31- 7	9838
U 15- 8	high	U 31- 8	PU53
U 15-10	3555	U 31- 9	4A2H
		U 31-11	4A2H
U 16- 1	high	U 31-12	PU53
U 16- 2	0000	U 31-13	9838
U 16- 4	P000	U 31-14	4013
U 16- 5	0000	U 31-15	P444
U 16- 6	P000	U 31-16	5AH3
U 16- 8	P000	U 31-17	8AAA
		U 31-18	A247
U 18- 7	0000		
		U 32- 1	P000
U 21- 8	3555		
U 21-10	0000	U 35- 5	0000
		U 35-10	0000
U 23- 3	P000		
U 23- 4	P000	U 36-11	755U
U 23- 5	H555		
U 23- 6	9F7F	U 37- 3	P000
U 23- 7	0344	U 37- 4	955U
U 23-10	91P6	U 37- 6	P000
U 23-11	F760	U 37- 8	P000
U 23-12	3987	U 37-10	0000
U 23-13	7302	U 37-11	P000
		U 37-12	0000
		U 38- 3	P000
		U 46- 1	P000
		U 46-11	P000

Table 8-39. Signature Analysis Setup M (3 of 3)

Node	Signature	Node	Signature
U 48- 2	P000	U 82- 2	CH21
U 48- 4	0000	U 82- 4	5H21
U 48- 5	P000	U 82- 5	9F7F
		U 82- 7	7F7F
U 49- 4	C2F8	U 82- 9	CCCC
U 49- 7	1PFH	U 82-11	5CCC
U 49- 9	PAFA	U 82-12	3555
		U 82-14	H555
U 50- 4	CH21		
U 50- 7	9F7F	U 83- 8	P000
U 50- 9	5CCC		
U 50-12	H555	U 84- 1	0000
		U 84- 2	CUUU
U 51- 4	P000	U 84- 3	AH28
U 51-15	P000	U 84- 4	F8AA
		U 84- 5	C211
U 79- 2	C2F8	U 84- 6	FF7H
U 79- 4	52F8	U 84- 7	APH6
U 79- 5	1PFH	U 84- 8	CF46
U 79- 7	UPFH	U 84- 9	6251
U 79- 9	0AFA	U 84-11	6251
U 79-11	PAFA	U 84-12	CF46
		U 84-13	APH6
U 80- 2	U293	U 84-14	FF7H
U 80- 4	1293	U 84-15	C211
U 80- 5	3PP0	U 84-16	F8AA
U 80- 7	HPP0	U 84-17	AH28
U 80- 9	2H70	U 84-18	CUUU
U 80-11	FH70		
U 80-12	HC89	U 85- 1	P000
U 80-14	3C89	U 85-11	8AAA
		U 85-12	P444
U 81- 2	H827	U 85-13	9838
U 81- 4	3827	U 85-14	4A2H
U 81- 5	HC96	U 85-15	PU53
U 81- 7	3C96	U 85-16	4013
U 81- 9	HAF7	U 85-17	5AH3
U 81-11	3AP7	U 85-18	A247
		U 85-19	0000

Table 8-40. Signature Analysis Setup N (1 of 2)

LOOPNAME: POWER ON RAM TEST FAILURE

If a failure is detected during the power on RAM self-test, the test enters a signature analysis loop that writes and reads RAM and stimulates the CRT controller. The loop also outputs the error masks onto the memory data bus and the CPU attempts to display the failing IC numbers.

SETUP NAME: RAM ACCESS CONTROL AND DECODE

This setup is used to troubleshoot the control circuitry used to enable the RAM data buffers during CPU accesses to RAM and to the CRT controller The mainframe is forced to execute the power on RAM test failure loop by removeing RAM IC A5U23.

Remove RAM IC A5U23

Executing power on RAM failure loop

ST/SP/START: A3TP5, rising edge (MEM SA LATCH)

QUAL/STOP: A3TP5, falling edge (MEM SA LATCH)

CLOCK: A3TP1, rising edge (LSTB)

Vh = CA27

Table 8-40. Signature Analysis Setup N (2 of 2)

Node	Signature	Node	Signature
U 1- 8	HC2U		
U 5- 3	75FC		
U 7- 3	3785		
U 15-11	2347		
U 21- 3	6645		
U 21-10	U869		
U 21-11	424P		
U 35-10	8HA2		
U 47- 3	2347		
U 78- 1	A91A		
U 78- 2	50C0		
U 78- 3	5FAC		
U 78- 4	U664		
U 78- 5	F8FF		
U 78- 6	2838		
U 78- 7	4P85		
U 78- 9	5HCA		
U 78-10	APH5		
U 78-11	6445		
U 78-12	9CPU		
U 78-13	U94H		
U 78-14	4534		
U 78-15	P29H		
U 83- 1	HC2U		
U 83- 2	HF62		
U 83- 5	HC2U		
U 83- 6	APP5		
U 83- 8	U869		
U 83-10	0000		
U 83-11	3785		

Table 8-41. Signature Analysis Setup 0 (1 of 2)

LOOPNAME: CRT CONTROLLER OUTPUTS-HARDWARE LOOP

By moving jumpers J2 and J3 to the test position, the CRT accesses to RAM are disabled. The CRT controller is still accessed by the CPU and configured. The CRT controller runs providing horizontal and vertical retrace signals to horizontal and vertical sync circuitry.

SETUP NAME: CRT CONTROLLER OUTPUTS-HARDWARE LOOP

This setup allows checking the horizontal and vertical sync circuitry and checking for proper configuration of the CRT controller IC.

Move jumpers A5J2 and A5J3 to TEST.

ST/SP/START: A5TP16, rising edge (HVRTC)

QUAL/STOP: A5YP16, rising edge (HVRTC)

CLOCK: A5TP4, rising edge (HCAHR)

Vh = HU61

Table 8-41. Signature Analysis Setup 0 (2 of 2)

Node	Signature	Node	Signature
U 3- 3	745H		
U 3- 7	8C75		
U 3- 9	212H		
U 11- 6	589H		
U 11- 8	4179		
U 12- 9	9A00		
U 33- 1	AC3F		
U 33- 2	5414		
U 33- 3	63UP		
U 33- 4	UP4F		
U 33- 5	3763		
U 33- 7	HA1H		
U 33- 8	2008		
U 33-30	HU61		
U 59- 6	FU65		
U 59- 9	34A6		
U 75-11	P54H		
U 76-15	268H		
U 77- 5	08PU		
U 77- 9	2A82		
U 86- 8	P54H		
U 87-11	3A2F		
U 91- 5	2HCC		
U 91- 9	P54H		

Table 8-42. Signature Analysis Setup P (1 of 2)

LOOPNAME: POWER ON RAM TEST FAILURE

If a failure is detected during the power on RAM self-test, the test enters a signature analysis loop that writes and reads RAM and stimulates the CRT controller. The loop also outputs the error masks onto the memory data bus and the CPU attempts to display the failing IC numbers.

SETUP NAME: CPU PROGRAM OF CRT CONTROLLER

This setup alllows the checking of the data path from the CPU to the CRT controller IC, addressing, and control. The mainframe is forced to loop on RAM failure test by removing RAM IC U23.

Remove RAM IC U23

Executing power on RAM failure test

ST/SP/START: A3TP5, rising edge (MEM SA LATCH)

QUAL/STOP: A3TP5, falling edge (MEM SA LATCH)

CLOCK: A5TP17, rising edge (LCS)

Vh = H7P4

Table 8-42. Signature Analysis Setup P (2 of 2)

Node	Signature	Node	Signature
U 5- 3	0000	U 83- 8	H7P4
U 5- 6	AP7C	U 83-11	0000
		U 83-12	H7P4
U 7- 3	0000		
U 7- 6	H7P4	U 85- 1	0000
		U 85- 2	A391
U 15-11	H7P4	U 85- 3	2235
		U 85- 4	8242
U 17- 6	0000	U 85- 5	HPU1
		U 85- 6	A9A4
U 21- 3	H7P4	U 85- 7	AA06
		U 85- 8	H2A3
U 31- 1	H7P4	U 85- 9	U898
		U 85-11	U898
U 32- 1	H7P4	U 85-12	H2A3
		U 85-13	AA06
U 33-12	7172	U 85-14	A9A4
U 33-13	0547	U 85-15	HPU1
U 33-14	F9F3	U 85-16	8242
U 33-15	0A5F	U 85-17	2235
U 33-17	55A6	U 85-18	A391
U 33-18	U5H1	U 85-19	0000
U 33-19	7475		
		U 88- 8	H7P4
U 35-13	12U8	U 88-10	0000
		U 88-11	0000
U 46- 1	H7P4		
U 46-11	H7P4		
U 47- 8	H7P4		

Table 8-43. Signature Analysis Setup R (1 of 2)

LOOPNAME: POWER ON RAM TEST FAILURE

If a failure is detected during the power on RAM self-test, the test enters a signature analysis loop that writes and reads RAM and stimulates the CRT controller. The loop also outputs the error masks onto the memory data bus and the CPU attempts to display the failing IC numbers.

SETUP NAME: DISPLAY RAS ADDRESS CHECK

The refresh of the dynamic RAM is performed by a RAS of each of the row addresses of the RAM as the CRT controller IC accesses RAM for display data. This setup is used to check the display addressing during RAS and therefore refresh circuitry during the CRT controller accesses to RAM. Since the display is operative during the RAM failure loop, the mainframe is forced into this known loop by removing RAM IC A5U23.

Remove RAM IC A5U23

Executing power on RAM test failure loop

ST/SP/START: A5TP16, rising edge (HVRTC)

QUAL/STOP: A5TP16, rising edge (HVRTC)

CLOCK: A5TP7, rising edge (HDRAS)

Vh = 279A

Table 8-43. Signature Analysis Setup R (2 of 2)

Node	Signature	Node	Signature
U 5- 8	279A	U 48- 5	279A
U 5- 9	279A		
		U 49- 4	9U8C
U 7-11	279A	U 49- 7	355A
U 7-12	279A	U 49- 9	3P32
U 8- 6	0000	U 50- 4	46H1
U 8- 8	72P9	U 50- 7	0H97
U 8- 9	72P9	U 50- 9	AH4P
		U 50-12	861H
U 15- 5	high		
U 15- 6	high	U 51- 4	279A
U 15- 8	high	U 51-15	high
U 16- 2	0000	U 62-11	7H02
U 16- 6	279A	U 62-12	355A
U 16- 8	279A	U 62-13	3P32
U 16-10	0000	U 62-14	46H1
		U 62-15	1355
U 17- 3	9U8C		
		U 63-11	A9FP
U 18- 7	279A	U 63-12	H3CP
		U 63-13	6H44
U 21- 2	P289	U 63-14	PF45
U 23- 3	279A	U 64-11	0H97
U 23- 4	279A	U 64-12	AH4P
U 23- 5	861H	U 64-13	861H
U 23- 6	0H97	U 64-14	F513
U 23- 7	AH4P	U 64-15	8447
U 23-10	355A		
U 23-11	3P32	U 79- 4	C811
U 23-12	46H1	U 79- 7	12F0
U 23-13	9U8C	U 79- 9	19A8
U 23-15	279A		
		U 80- 4	8P54
U 35- 4	0000	U 80- 7	U424
		U 80- 9	4AHP
U 36-11	279A	U 80-12	FCHU
U 36-13	279A		
		U 81- 4	279A
U 37- 3	279A	U 81- 7	279A
U 37- 6	279A	U 81- 9	279A
U 37- 8	279A		
U 37-10	279A	U 82- 4	614C
U 37-11	279A	U 82- 7	2A0H
U 37-12	0000	U 82- 9	8AH4
		U 82-12	A187
U 38- 3	279A		

Table 8-44. Signature Analysis Setup S (1 of 2)

CRT CONTROLLER OUTPUTS - DISPLAY TEST

LOOPNAME: DISPLAY TEST

During the display test signature analysis loops are set and reset around the repetitive display pattern. Control stimulus is provided to the CRT controller IC during the display loop.

SETUP NAME: CRT CONTROLLER OUTPUTS-DISPLAY TEST

DESCRIPTION: This setup allows the checking of the CRT controller IC outputs including the character code outputs and control signals. It also allows the checking of the character generator ROM and HSYN and VSYN circuitry.

Executing display test

ST/SP/START: A5TP16, rising edge (HVRTC)

QUAL/STOP: A5TP16, rising edge (HVRTC)

CLOCK: A5TP4, rising edge (HCHAR)

Vh = UA11

Table 8-44. Signature Analysis Setup S (2 of 2)

Node	Signature	Node	Signature
U 3- 3	676P	U 59- 3	0000
U 3- 5	5HP8	U 59- 6	8719
U 3- 7	5312	U 59- 8	UP63
U 3- 9	C18H	U 59- 9	0472
U 3-12	676P	U 59-11	0000
U 3-14	5312		
U 3-16	4489	U 60- 2	0000
U 3-18	C18H	U 60- 6	0000
		U 60-10	0000
U 4- 3	U239	U 60-11	UA11
U 4- 5	P328		
U 4- 7	890C	U 74- 9	738F
U 4- 9	7U45	U 74-10	C67P
U 4-12	A2F2	U 74-11	3930
U 4-14	89H9	U 74-13	417H
U 4-16	0828	U 74-14	C8PU
U 4-18	0000	U 74-15	56A6
		U 74-16	2PP7
U 9- 1	0472	U 74-17	0000
U 11- 6	1U91	U 75- 2	0000
U 11- 8	P1F7	U 75-11	127U
U 12- 9	UA11	U 76- 2	0000
		U 76-15	3F33
U 17- 8	9H7U		
		U 77- 5	06H6
U 33- 1	9H7U	U 77- 9	0520
U 33- 2	A903		
U 33- 3	CP98	U 86- 8	127U
U 33- 4	4C9F		
U 33- 7	8554	U 87-11	P86P
U 33- 8	UA11		
U 33-23	A7U9	U 91- 3	UA11
U 33-24	731A	U 91- 5	8719
U 33-25	1939	U 91- 9	127U
U 33-26	58H3		
U 33-27	73F8		
U 33-28	U239		
U 33-29	0828		
U 33-35	UA11		
U 33-36	0000		
U 33-37	0000		

Table 8-45. Signature Analysis Setup T (1 of 3)

LOOPNAME: DISPLAY TEST

During the display test signature analysis loops are set and reset around the repetitive display pattern. Control stimulus is provided to the CRT controller IC during the display loop.

SETUP NAME: CRT CONTROLLER READ FROM RAM

This setup is used to troubleshoot the circuitry associated with the CRT contoller access to RAM. This consists of the address counters, data path, and control of the data buffers and data latch. The address is during the CAS portion of the address.

Executing display test

ST/SP/START: A5TP3, rising edge (LSYNC VRTC)

QUAL/STOP: A5TP3, falling edge (LSYNC VRTC)

CLOCK: A5TP13, rising edge (LDCAS)

Vh = P5H2

Table 8-45. Signature Analysis Setup T (2 of 3)

Node	Signature	Node	Signature
U 1- 8	high	U 21- 2	5FC1
U 1-11	5FC1		
		U 23- 3	high
U 2-11	0000	U 23- 4	P5H2
		U 23- 5	73P7
U 5- 6	0000	U 23- 6	8P54
U 5- 8	0000	U 23- 7	U2P6
		U 23-10	0000
U 7- 6	P5H2	U 23-11	0000
U 7-11	P5H2	U 23-12	6C86
		U 23-13	0000
U 8- 6	72P9	U 23-15	0000
U 8- 8	0000		
U 8- 9	P5H2	U 32- 2	75CF
		U 32- 3	901U
U 9-10	H5AU	U 32- 4	CF87
		U 32- 5	A454
U 12- 5	P5H2	U 32- 6	78AH
U 12- 6	0000	U 32- 7	84AC
		U 32- 8	2AF2
U 13- 1	74P7	U 32- 9	9135
U 13- 4	6179	U 32-11	5616
U 13-10	4186	U 32-12	0A6C
U 13-13	75FH	U 32-13	7U21
		U 32-14	307H
U 15-11	high	U 32-15	72CP
		U 32-16	4319
U 16- 6	high	U 32-17	A164
U 16- 8	high	U 32-18	7328
		U 32-19	5FC1
U 17- 3	CP11		
U 17- 6	P5H2	U 33- 5	0000
U 18- 5	P5H2	U 35-10	low
U 18- 7	P5H2	U 35-13	0000
U 18- 9	0000		
		U 37- 3	P5H2
U 19- 3	A6FC	U 37- 6	high
U 19- 6	PUC9	U 37- 8	P5H2
U 19- 8	96UA	U 37-11	0000

Table 8-45. Signature Analysis Setup T (3 of 3)

Node	Signature	Node	Signature
U 38- 3	high	U 62-11	P2A0
		U 62-12	AAU8
U 46- 2	7328	U 62-13	4P5P
U 46- 3	4657	U 62-14	6H2U
U 46- 4	FPP0	U 62-15	5U8F
U 46- 5	4319		
U 46- 6	307H	U 63-11	6C86
U 46- 7	CH8H	U 63-12	8P54
U 46- 8	2522	U 63-13	U2P6
U 46- 9	0A6C	U 63-14	73P7
U 46-12	9135	U 63-15	high
U 46-13	FPHC		
U 46-14	6U9U	U 64-11	A775
U 46-15	84AC	U 64-12	8H02
U 46-16	A454	U 64-13	2P42
U 46-17	1315	U 64-14	C963
U 46-18	PFUA	U 64-15	52A2
U 46-19	901U		
		U 79- 4	5CF3
U 47- 3	high	U 79- 7	4U2A
U 47- 6	C963	U 79- 9	AC8F
U 47- 8	P5H2		
		U 80- 4	8P54
U 48- 2	P5H2	U 80- 7	6C86
U 48- 4	0000	U 80- 9	1734
U 48- 5	P5H2	U 80-12	9635
U 49- 4	0000	U 81- 4	P5H2
U 49- 7	0000	U 81- 7	P5H2
U 49- 9	0000	U 81- 9	P5H2
U 50- 4	A2U8	U 82- 4	88UH
U 50- 7	8P54	U 82- 7	42A7
U 50- 9	U2P6	U 82- 9	68H0
U 50-12	73P7	U 82-12	FC90
U 51- 4	P5H2	U 83- 5	high
U 51-15	high	U 83- 6	high
		U 83-11	high
		U 88- 8	low

Table 8-46. Signature Analysis Setup U (1 of 2)

LOOPNAME: RAM CYCLE SELECTOR/GENERATOR

This is a hardware loop. By moving the test jumper P4 from the normal (XU2) to the test (XU1) position, the RAM cycle selector/generator circuitry is forced to run at the RAM clock rate.

SETUP NAME: RAM CYCLE SELECTOR/GENERATOR

This setup is used to troubleshoot the RAM cycle selector/generator circuitry.

Remove the CPU I/O board

Disable the display driver by disconnecting the cable that connects from the A6 vertical and secondary drive board to the A7 flyback board.

Move P4 from normal (XU2) to test (XU1).

ST/SP/START: A5TP14, rising edge (RCARRY)

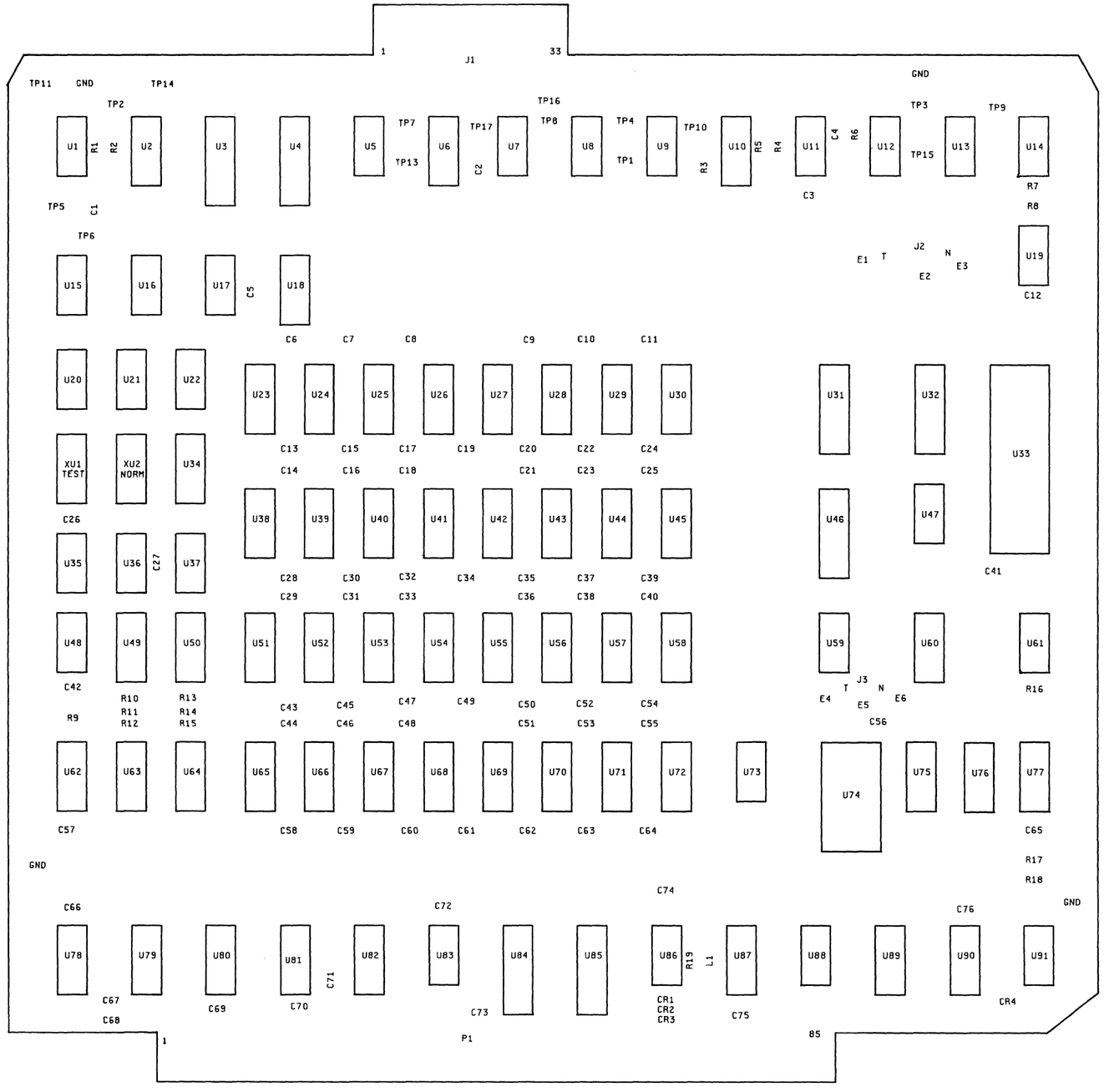
QUAL/STOP: A5TP14, rising edge (RCARRY)

CLOCK: A5TP2, rising edge (RAMCLOCK)

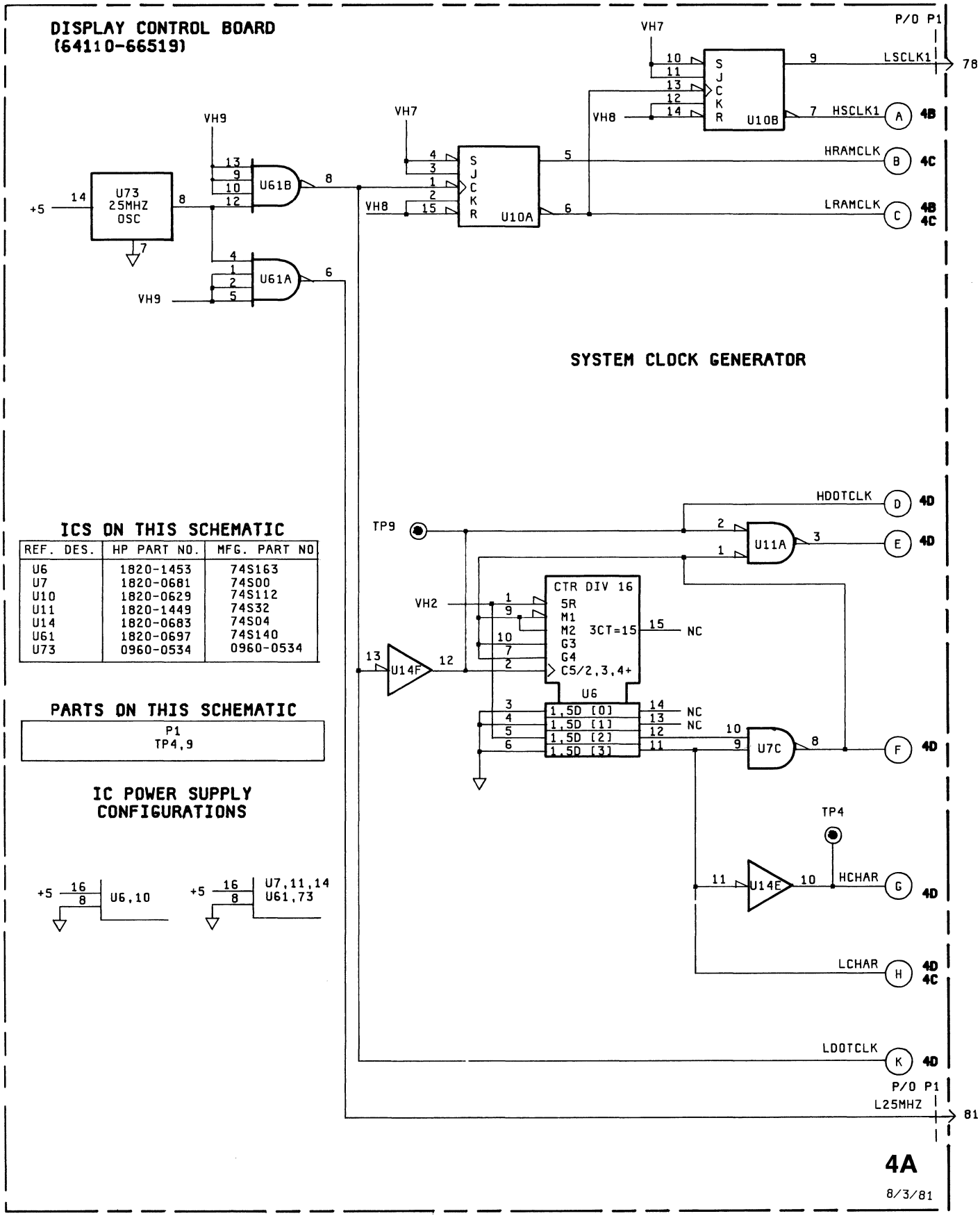
Vh = UP73

Table 8-46. Signature Analysis Setup U (2 of 2)

Node	Signature	Node	Signature
U 1- 3	55H1	U 22- 1	low
U 1- 8	UP51	U 22- 4	low
		U 22- 5	UP73
U 2-11	8135	U 22- 8	low
U 2-12	86F1	U 22- 9	high
U 2-13	98PH	U 22-10	low
U 2-14	ACA2	U 22-13	669P
U 5-11	8117	U 23- 3	UF74
		U 23- 4	7U46
U 9-11	55H1	U 23-15	7U24
U 9-12	low		
U 9-13	ACA2	U 32-11	high
U 15- 3	7U24	U 35- 1	0022
U 15- 4	high	U 35- 4	2275
U 15- 5	high		
U 15- 6	high	U 36- 3	high
U 15- 8	high	U 36- 6	ACU7
		U 36-11	HF06
U 16- 6	UF74		
U 16- 8	UF74	U 37- 3	7U46
		U 37- 6	UP51
U 18- 7	HF06	U 37- 8	7U46
U 18- 9	2275	U 37-11	7U24
U 18-12	high		
		U 38- 3	UF74
U 20- 6	high		
U 20- 8	H4C1	U 48- 5	7U46
		U 48- 8	8175
U 21- 3	high	U 48- 9	7U06
U 21- 4	low		
U 21- 6	7U46	U 51- 4	7U46
U 21- 8	low	U 51-15	UP51
U 21-10	high		
U 21-11	low	U 86-11	0022



Display Controller Component Locator



ICS ON THIS SCHEMATIC

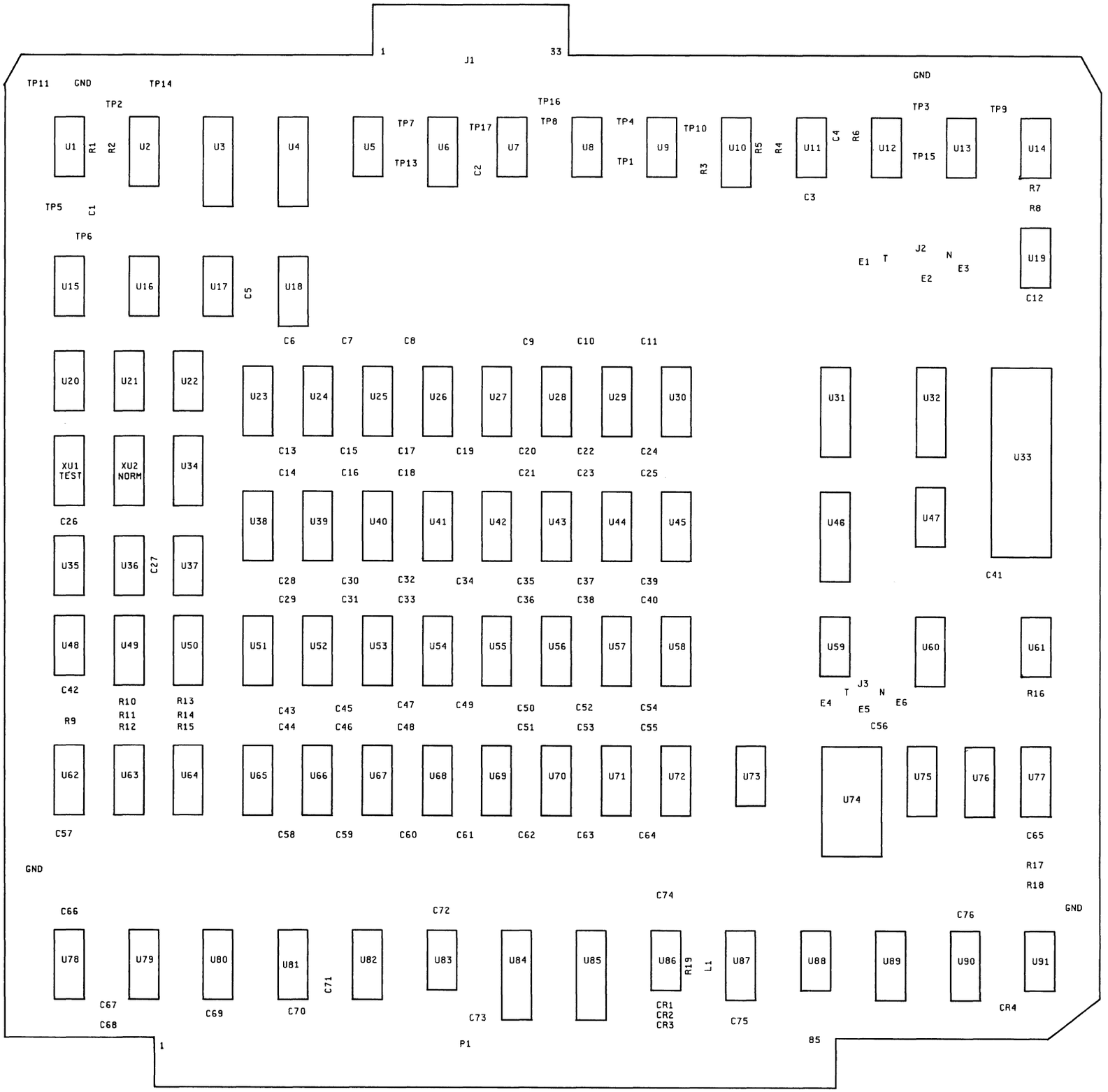
REF. DES.	HP PART NO.	MFG. PART NO
U6	1820-1453	74S163
U7	1820-0681	74S00
U10	1820-0629	74S112
U11	1820-1449	74S32
U14	1820-0683	74S04
U61	1820-0697	74S140
U73	0960-0534	0960-0534

PARTS ON THIS SCHEMATIC

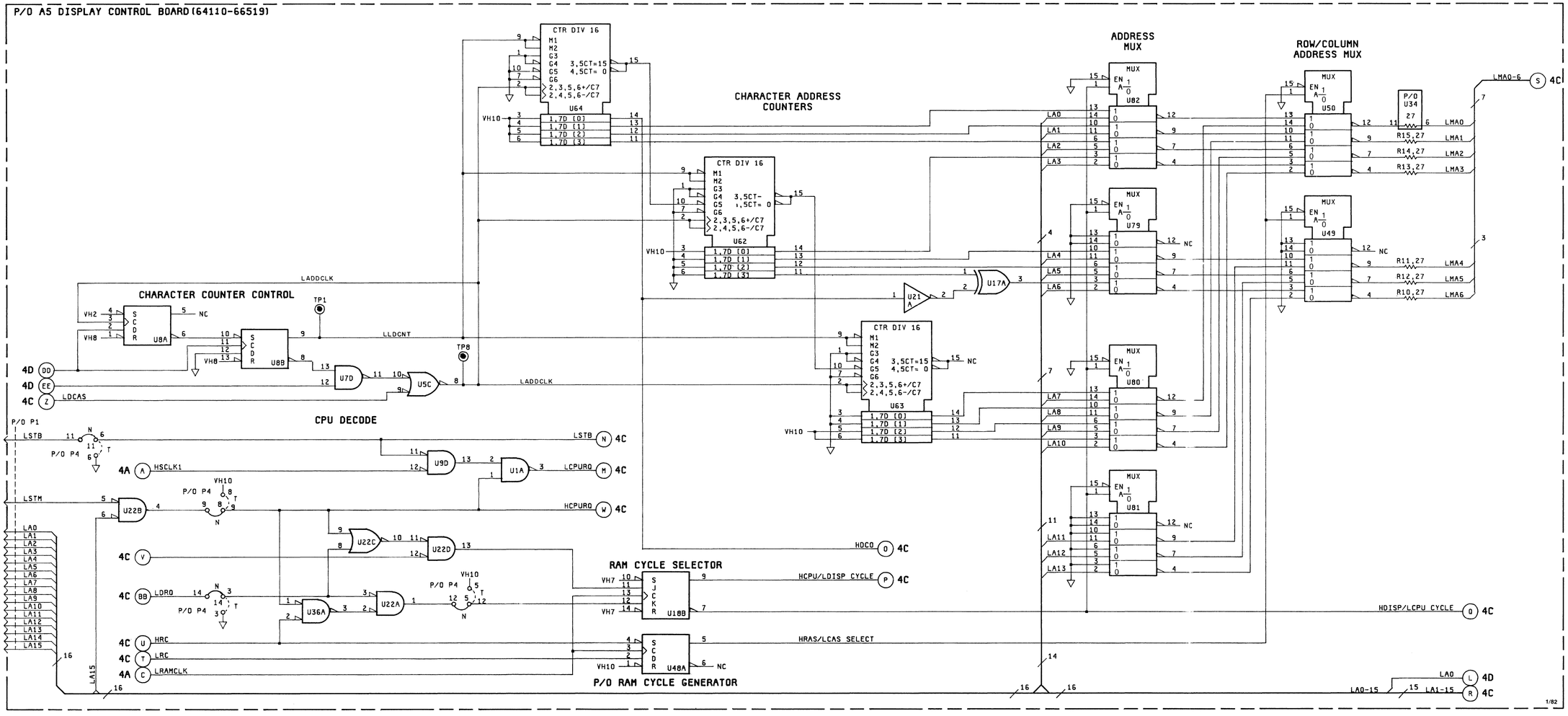
P1
TP4,9

IC POWER SUPPLY CONFIGURATIONS

Figure 8-20.
System Clock/Generator, Display Controller Schematic 1 of 4



Display Controller Component Locator



ICS ON THIS SCHEMATIC

REF. DES.	HP PART NO.	MFG. PART NO.
U1,7	1820-0681	74S00
U5	1820-1201	74LS08
U8	1820-1112	74LS74AN SLT
U9,22	1820-1322	74S02
U17	1820-1211	74LS86
U18	1820-0629	74S112
U21	1820-0683	74S04
U34	1820-0536	316B270
U36	1820-1208	74LS32
U48	1820-0693	74S74
U49,50	1820-1015	74S158
U62-64	1820-1435	74LS669N
U79-82	1820-1428	74LS158

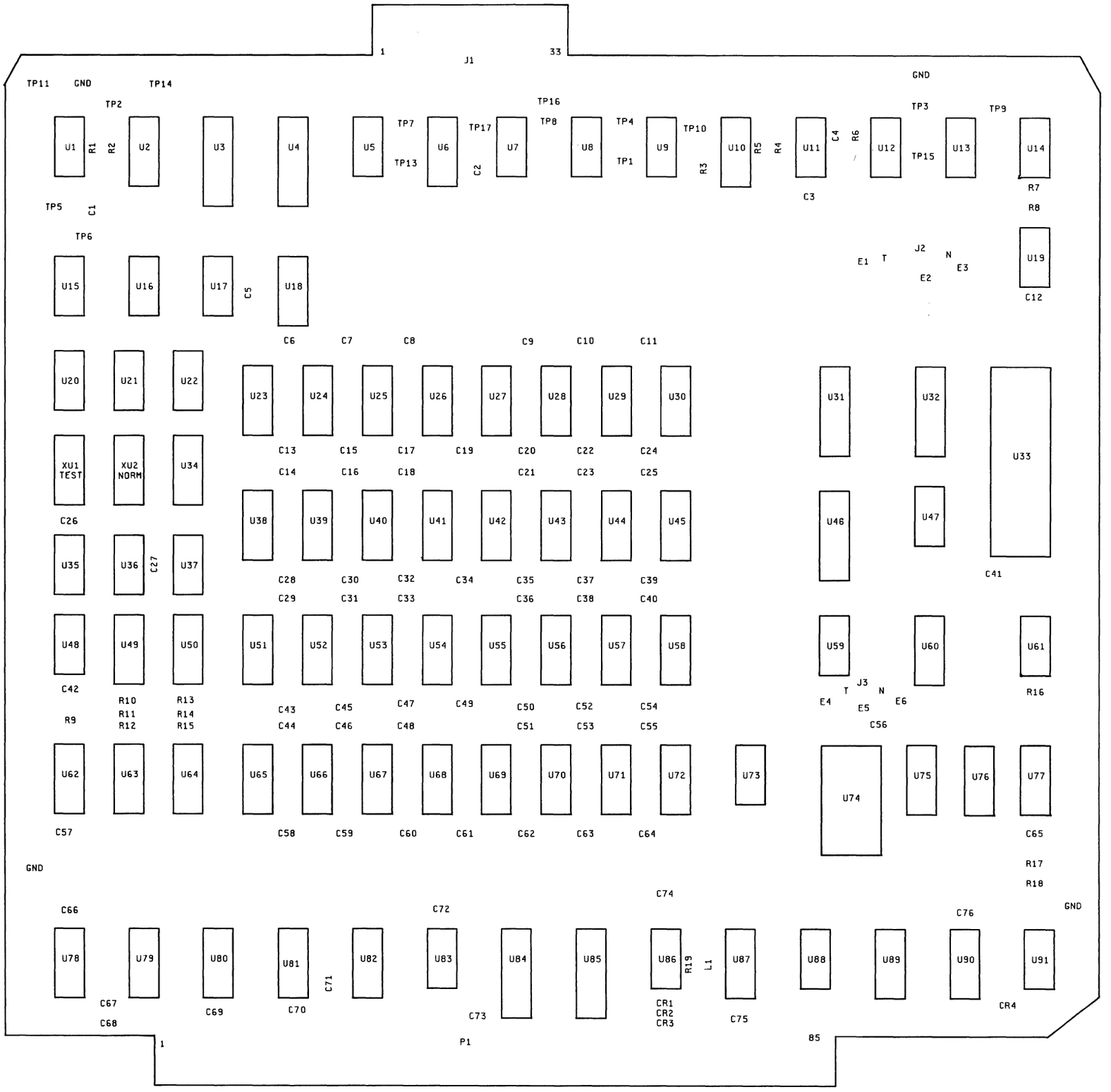
PARTS ON THIS SCHEMATIC

P4
R10-15
TP1,8
U1,5,7-9,17,18,21,22,34,36,47,48,49,50,62-64,79-82

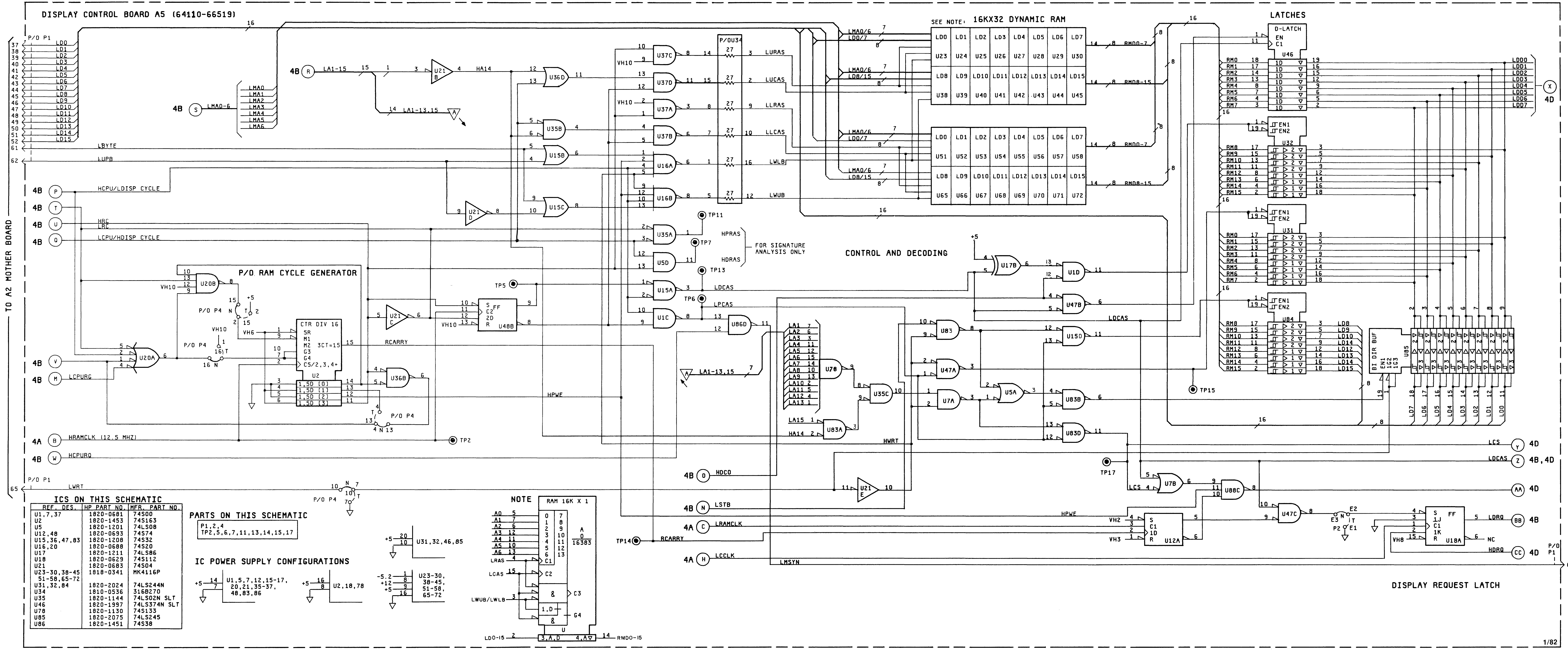
IC POWER SUPPLY CONFIGURATIONS

+5 — 14 — 7 — U1,5,7-9,17,21,22,48
+5 — 16 — 8 — U18,49,50,62-64,79-82

Figure 8-21.
Character Address Counter/Mux, Display Controller Schematic 2 of 4
8-149 DC



Display Controller Component Locator

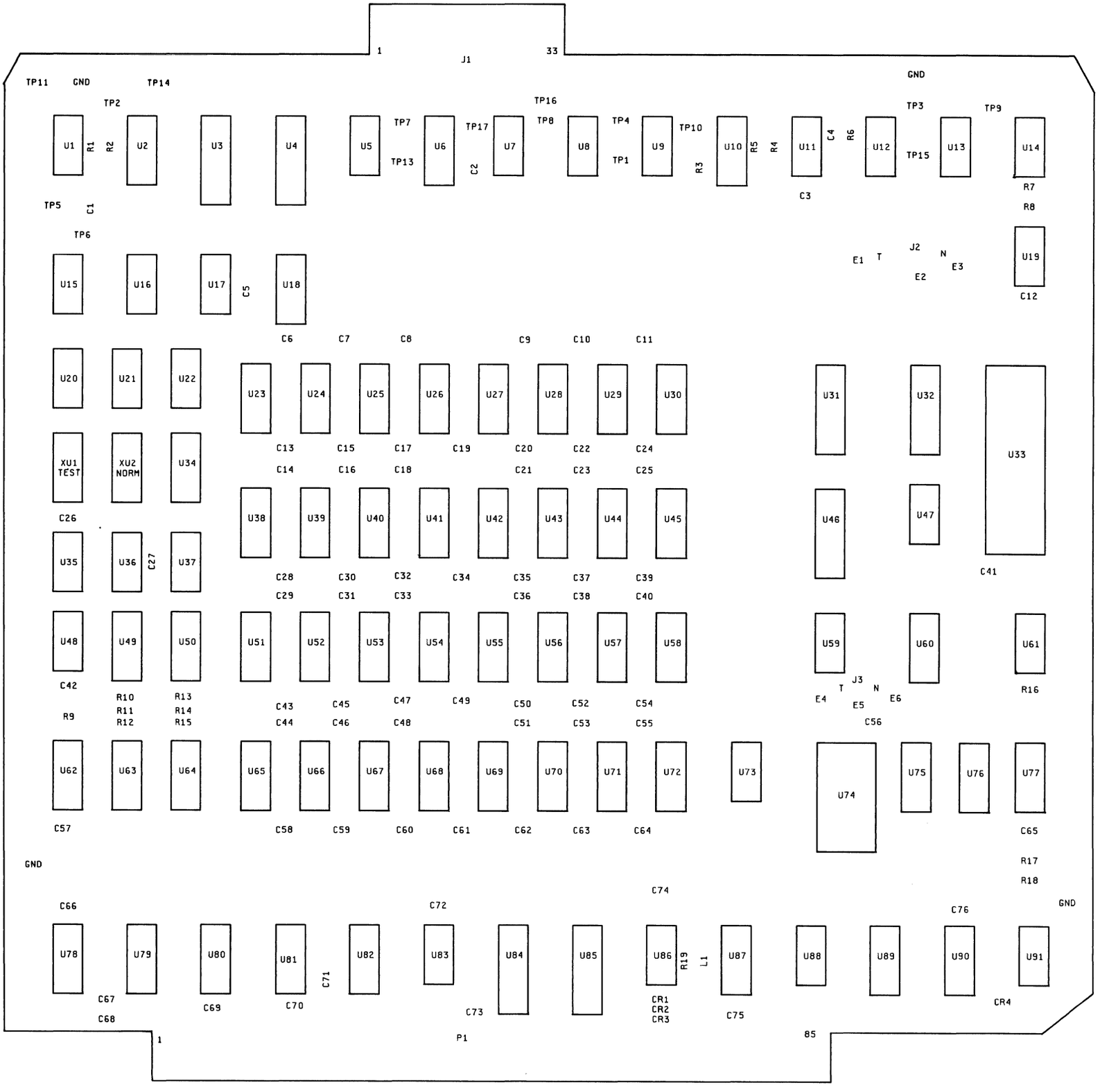


ICS ON THIS SCHEMATIC

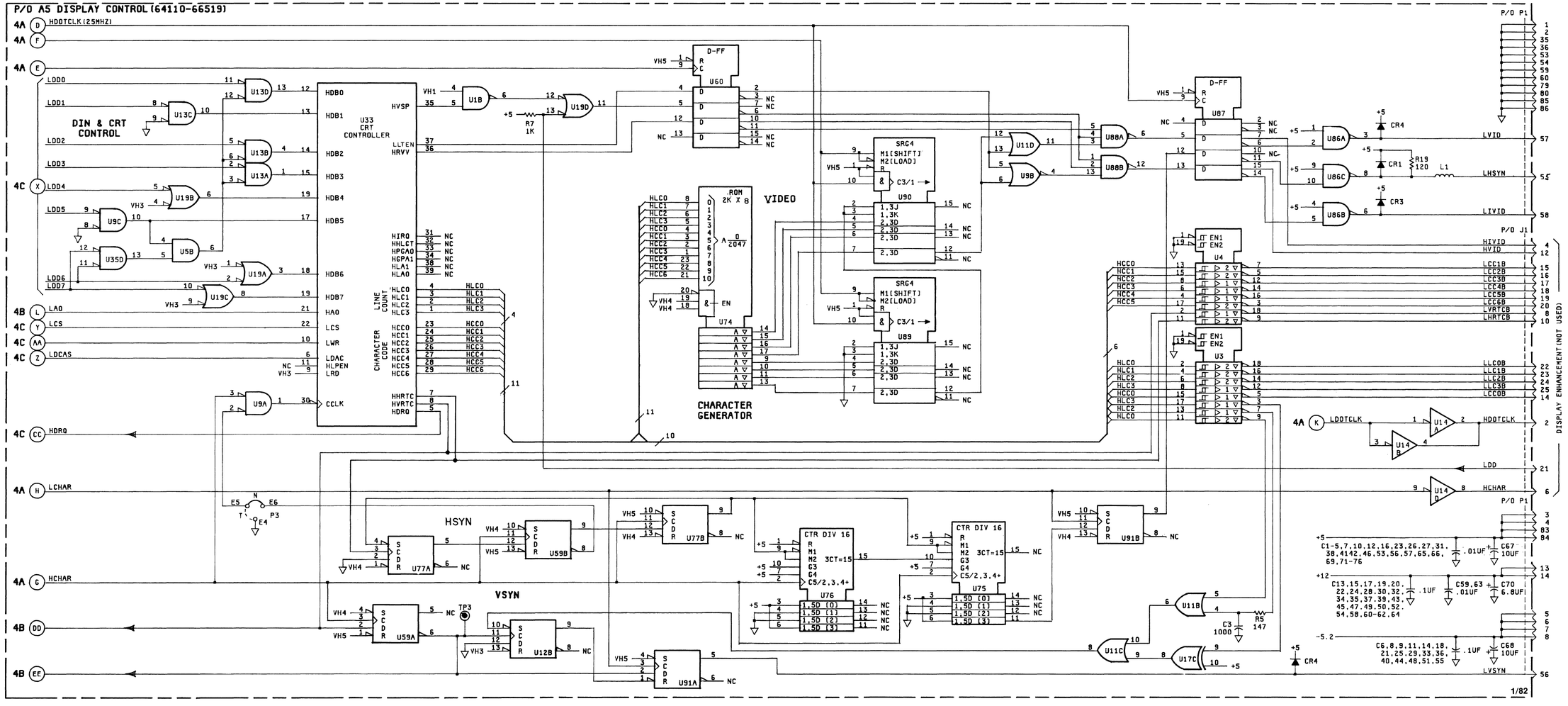
REF. DES.	HP PART NO.	MFR. PART NO.
U1,7,37	1820-0681	74S00
U2	1820-1453	74S163
U5	1820-1201	74LS08
U12,48	1820-0693	74S74
U15,36,47,83	1820-1208	74S32
U16,20	1820-0688	74S20
U17	1820-1211	74LS86
U18	1820-0629	74S112
U21	1820-0683	74S04
U23-30,38-45 51-58,65-72	1818-0341	MK4116P
U31,32,84	1820-2024	74LS244N
U34	1810-0536	316B270
U35	1820-1144	74LS02N SLT
U46	1820-1997	74LS374N SLT
U78	1820-1130	74S133
U85	1820-2075	74LS245
U86	1820-1451	74S38

4C

Figure 8-22.
Character Generator/Latches, Display Controller Schematic 3 of 4



Display Controller Component Locator



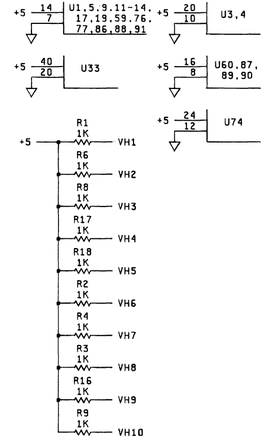
ICS ON THIS SCHEMATIC

REF. DES.	HP PART NO.	MFG. PART NO.
U1	1820-0681	74S00
U3,4	1820-1927	74LS240N
U5	1820-1201	74LS08
U9	1820-1322	74S02
U11	1820-1449	75532
U12,91	1820-0693	74S74
U13	1820-1144	74LS02N SLT
U14	1820-0683	74S04
U17	1820-1211	74LS86
U19	1820-1197	74LS00
U33	1820-2191	8275A
U59,77	1820-1112	74LS74AN SLT
U60,87	1820-1191	74S175
U74	1820-1496	1816-1496
U75,76	1820-1432	74LS163
U86	1820-1451	74S38N
U88	1820-0685	74S10
U89,90	1820-1303	74S195

PARTS ON THIS SCHEMATIC

C1-76
CR1-4
L1
P3
R1-9,16-19
TP3
U1,3-5,9,11-14,17,19,33,59,60,74-77,86-91

IC POWER SUPPLY CONFIGURATIONS



4D

Figure 8-23.
RAM, Display Controller Schematic 4 of 4
8-153/(8-154 blank) DC

8-354. DISPLAY DRIVER BLOCK DESCRIPTION.

8-355. The display driver board provides the video drive, sweeps, and bias voltages to drive the CRT. The video drive circuit features two drive levels, one for regular video, one for inverse video. The inverse video drive is about half the intensity of the regular video drive to avoid glare.

8-356. The high voltage circuit generates grid voltage of -40 V, +200 to 700 V, and 0 to 470 V necessary to provide intensity and focus adjustments. The beeper circuit provides an audible feedback to signify the occurrence of specific events during performance verification and normal operation.

8-357. DISPLAY DRIVER SCHEMATIC DESCRIPTION.

8-358. The display driver boards provide the video drive, sweeps, and bias voltages to drive the CRT.

8-359. The display controller IC U33 on the display controller board is responsible for providing horizontal and vertical retrace signals and the low video and low inverse video signals. The other signal necessary for the display driver to operate is LBEEP from the CPU/IO board.

8-360. With no video signal applied, low inverse video (LIVID) and low video (LVID) are high, forcing the outputs of U1A and U1B low. Transistor Q3 is an emitter follower and supplies necessary current to keep the Q3 emitter voltage near 30 V and the video off.

8-361. If LVID goes low with LIVID high, the output of U1A releases the base of Q2 and allows it to turn on. CR2 and CR3 prevent it from saturating. When Q2 turns on, it holds the base voltage of Q3 low forcing the emitter voltage of Q3 low and the video full on.

8-362. If LIVID were to go low while LVID was low, Q1 would be allowed to turn on. But since the base voltage of Q3 is being held low by Q2, it makes no difference what state Q1 is in.

8-363. If LIVID is low while LVID is high, the input of U1B releases Q1 to turn on while U1A holds Q2 off. The voltage drop across VR2, CR6 and Q1 establishes an intermediate base voltage on the emitter follower Q3, and the video is at an intermediate intensity level.

Table 8-47. Video Truth Table

LVID	LIVID	FUNCTION
L	H	NORMAL BRIGHTNESS
L	L	NORMAL BRIGHTNESS
H	L	HALF BRIGHTNESS
H	H	OFF

8-364. 2500 Hz TONE GENERATOR SCHEMATIC DESCRIPTION. FIGURE 8-27, U7.

8-365. Timer U7 is a monolithic timing circuit that is operated in the astable (freerunning) mode to generate a 2500 Hz tone. The tone frequency is determined by R39, R40 and C30. The output of U7 controls Q9 which in turn modulates the five volts, appearing across R42, with the 2500 Hz tone signal.

8-366. DISPLAY ENABLE LATCH SCHEMATIC DESCRIPTION. FIGURE 8-26; U5A, B.

8-367. The latch U5A/B is found on the flyback A7 board. Latch U5A/B is set simultaneously with the activation of the beeper start pulse generator. When U5A/B is set, the display-on signal (HDE) is produced which is sent to the display driver to activate the CRT display. U5A/B is reset whenever system power is cycled off and on and whenever a power interrupt (LIR15) is generated by the mainframe power supply.

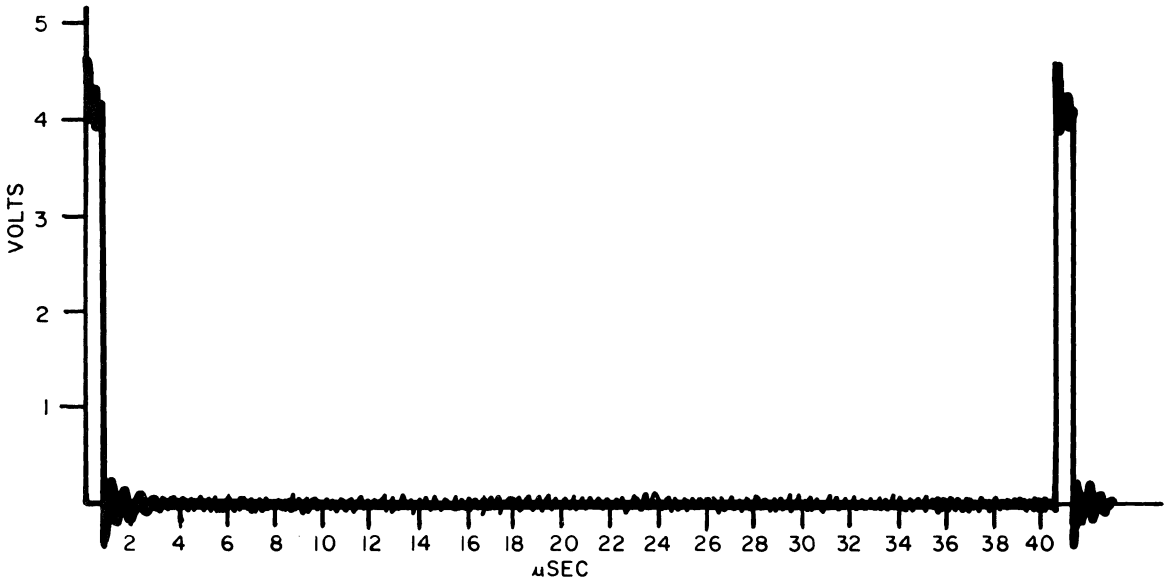
8-368. HORIZONTAL SWEEP AND HIGH VOLTAGE SCHEMATIC DESCRIPTION.

8-369. When low Horizontal Sync (LHSYN) occurs, the falling edge triggers the single shot U1A. By adjusting the pulse width of U1A, the falling edge of the output of U1A is being delayed in triggering U1B, thus providing horizontal position control (TP3). The pulse width of U1B is fixed (TP5).

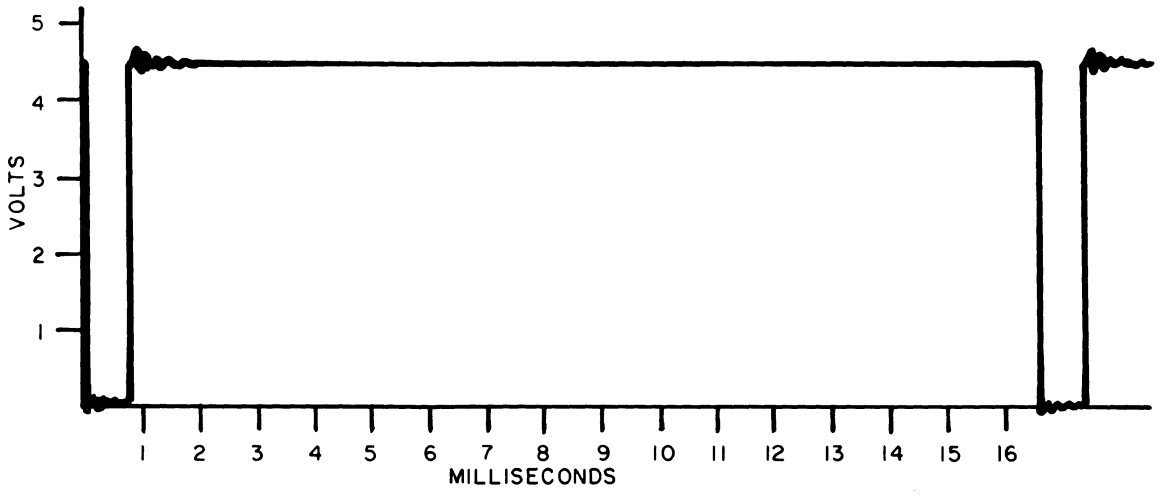
8-370. The negative output of U1B gets reinverted by U4C (a high voltage output, open-collector inverter). U4C switches Q1 off and on to drive current through T1. When T1 turns Q2 on, current is drawn from the 12V supply through the primary of T2 and the other secondary of T1. Q2 drives the current through the yoke for horizontal deflection. CR4 and C4 form the rectifier/filter for the +40V supply. The +12KV supply is internally rectified by the flyback, T2, with the aquadag of the CRT acting as the filter. The -40V supply is rectified and filtered by CR6 and C11, aided by clamp VR1. The intensity and focus voltages are formed by voltage divider networks supplied by CR5.

8-371. When low Vertical Sync (LVSYN) occurs, it's inverted through the high voltage, open-collector output, U4A to drive the inverting input of the current mode op-amp U2B which is configured as an integrator. Variable feedback from U2A provides a means of adjusting vertical gain. The threshold detector, U2C, drives the complementary pair, Q4 and Q5, for Vertical Sweep (TP1).

8-372. LVSYN is also used to switch Q3 on and off. Q3, C22 and blocking diode CR8 form a voltage doubler circuit to double the voltage available to U2 and the pair, Q4 and Q5, during retrace (see signal on U2P14).



Horizontal Sync P1, Pin 55



Vertical Sync P1, Pin 56

Figure 8-24. Horizontal and Vertical Sync Waveforms

NOTES

NOTES

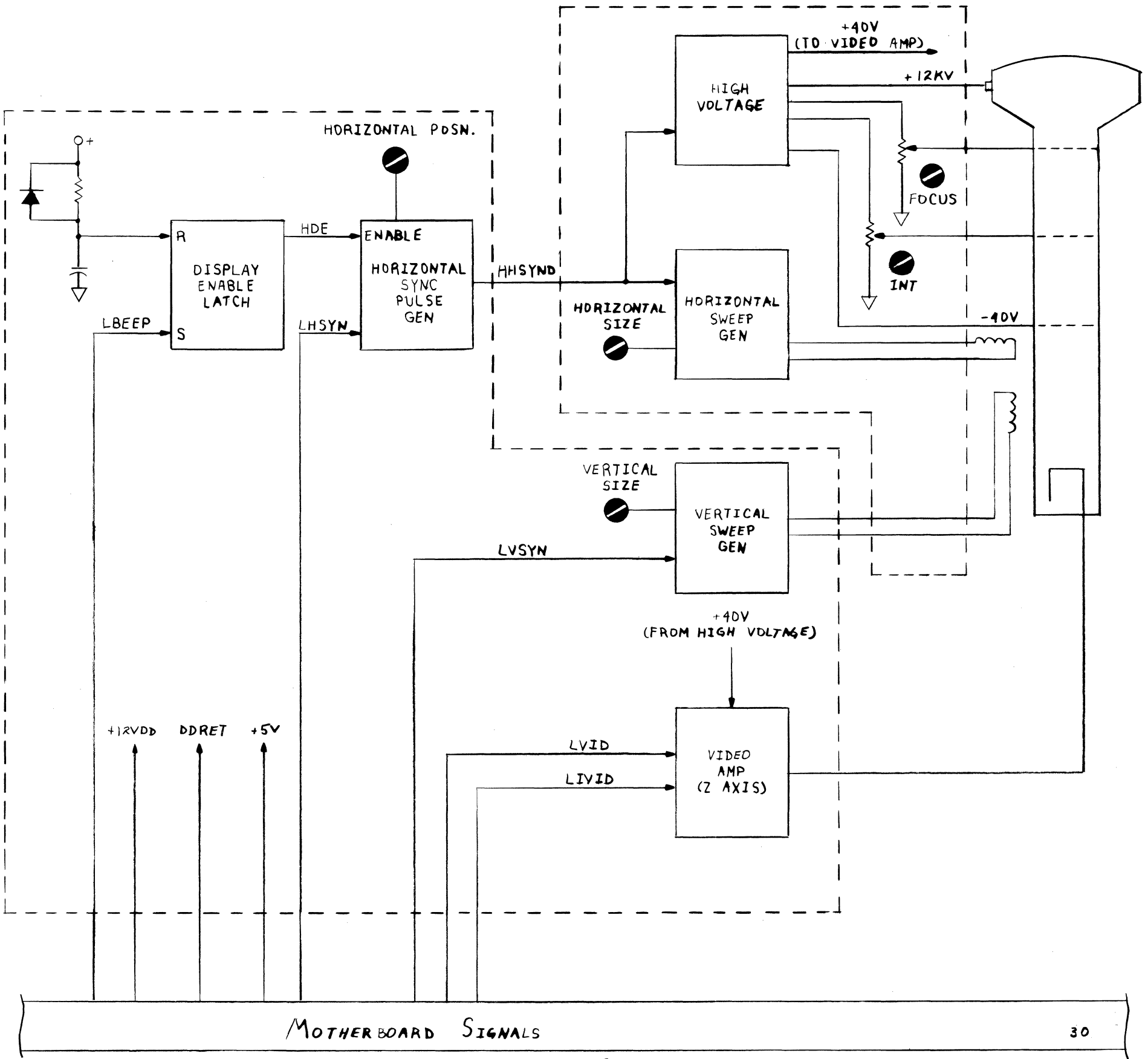
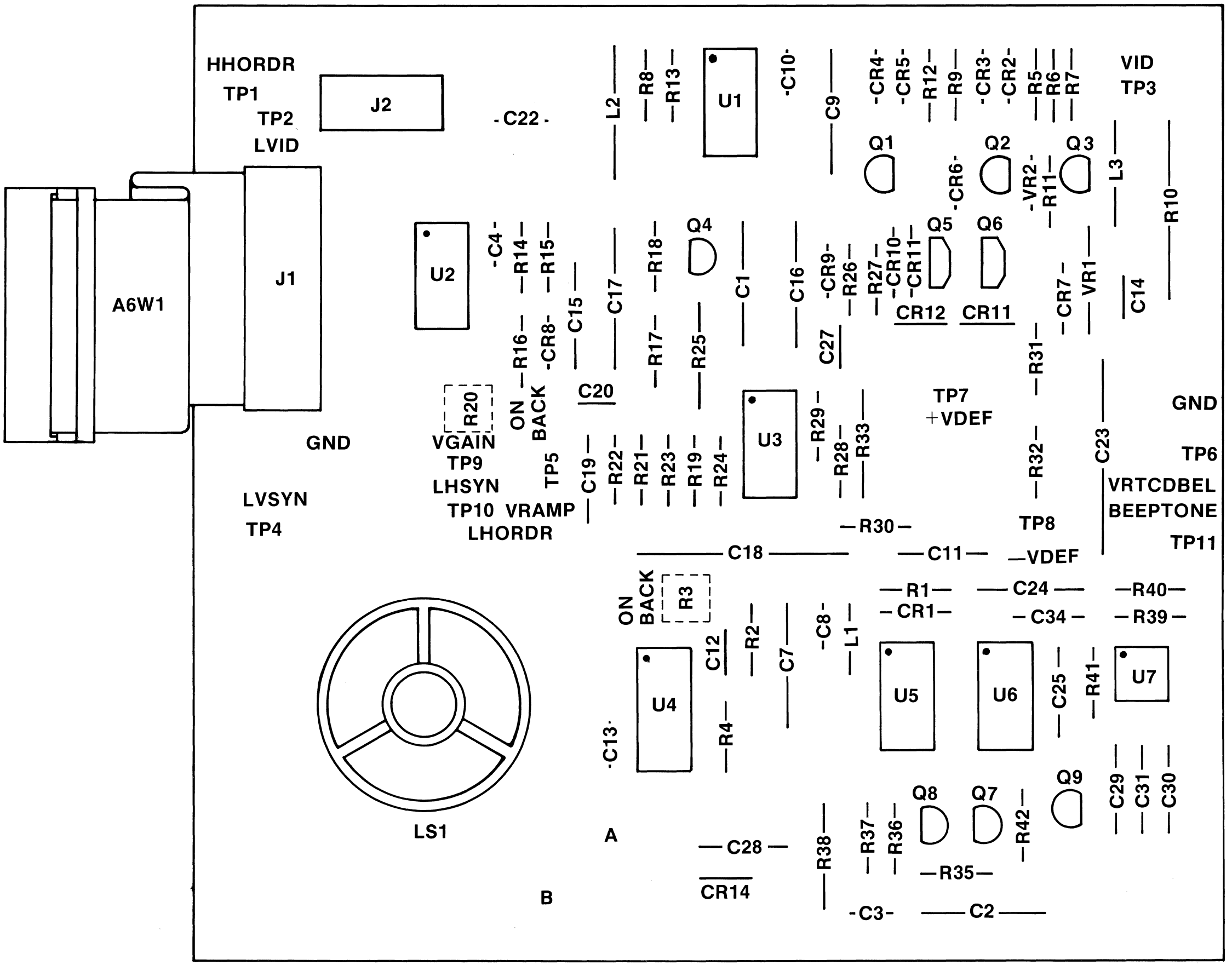
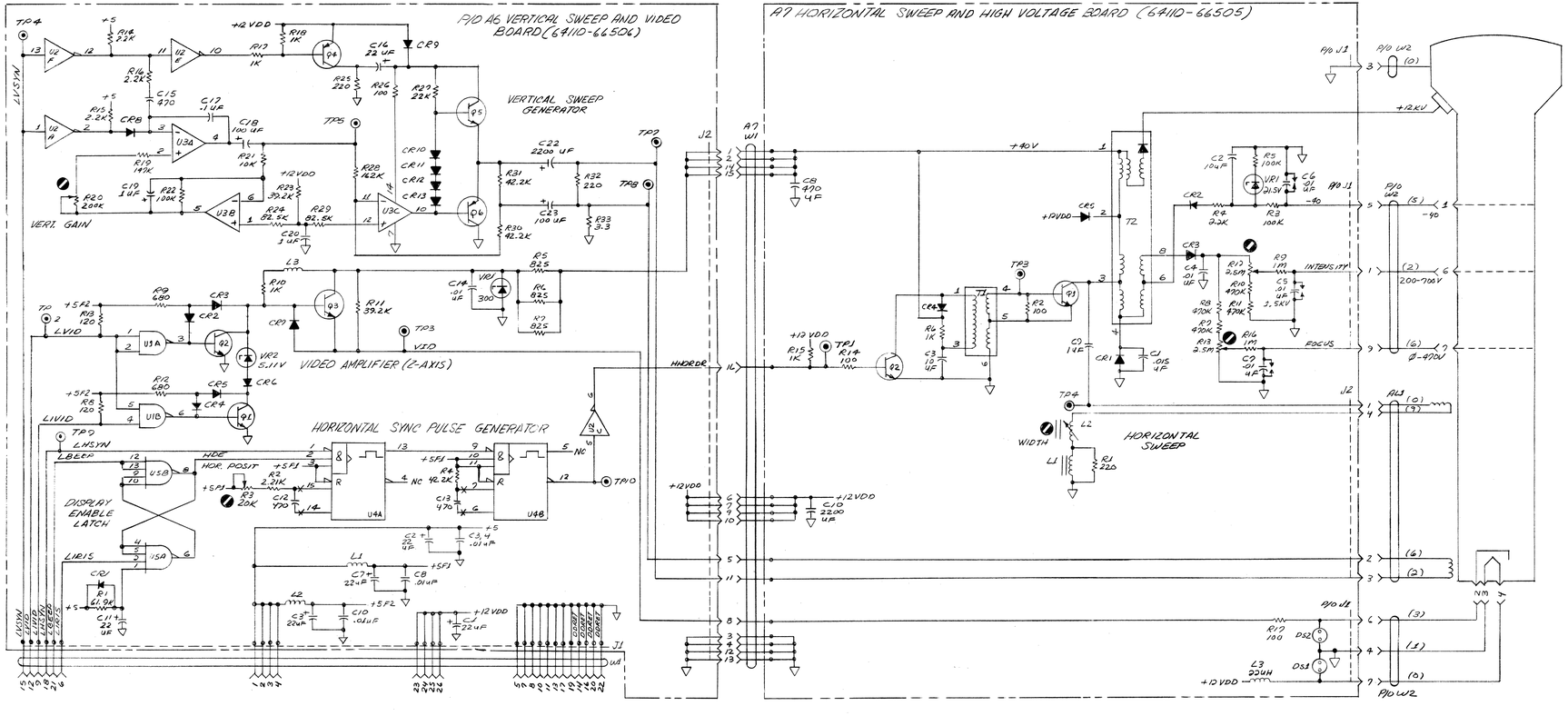


Figure 8-25. Display Driver Block Diagram



Display Driver Component Locator



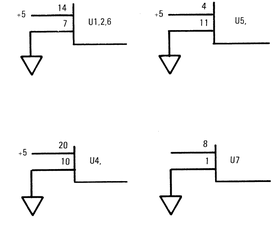
A6 ICs ON THIS SCHEMATIC

REF DES.	HP PART NO.	MFR PART NO.
U1	1820-1451	74538
U2	1820-0471	7406
U3	1826-0939	01921
U4	1820-1437	74LS221
U5	1820-1204	74LS20
U6	1820-1422	74LS122
U7	1826-0180	LIN 555

PARTS ON THIS SCHEMATIC

C1-30 R1-42 Q1-9	CR1-9,L1-3 VR1,2,LS1 Speaker

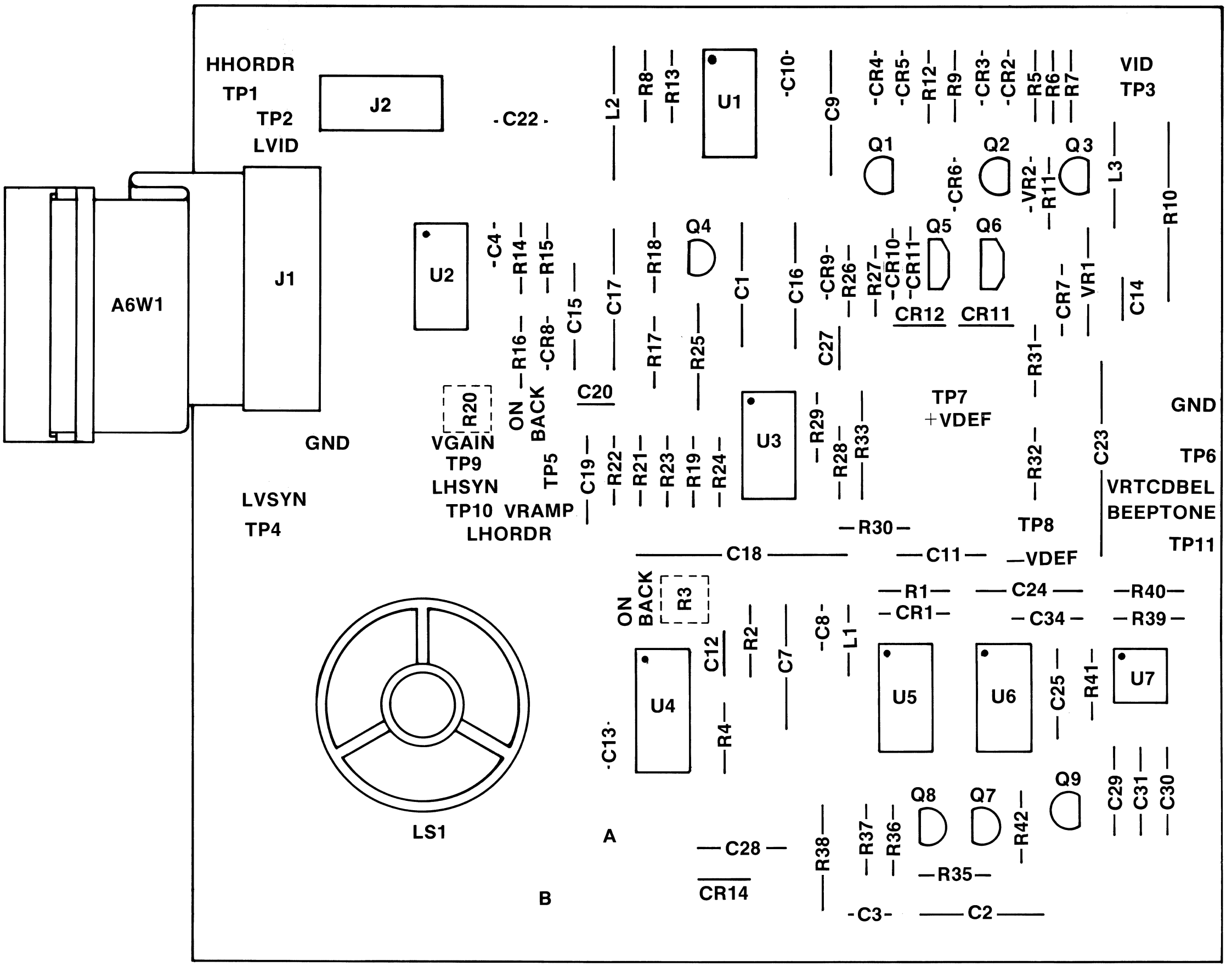
IC POWER SUPPLY CONFIGURATIONS



A7 PARTS ON THIS SCHEMATIC

C1-10 R1-16 Q1 Q2 CR1-5	VR1 DS1,2 L1-3 T1,2

Figure 8-26.
A6 and A7 Boards, Display Driver Schematic 1 of 2
8-163 DD



Display Driver Component Locator

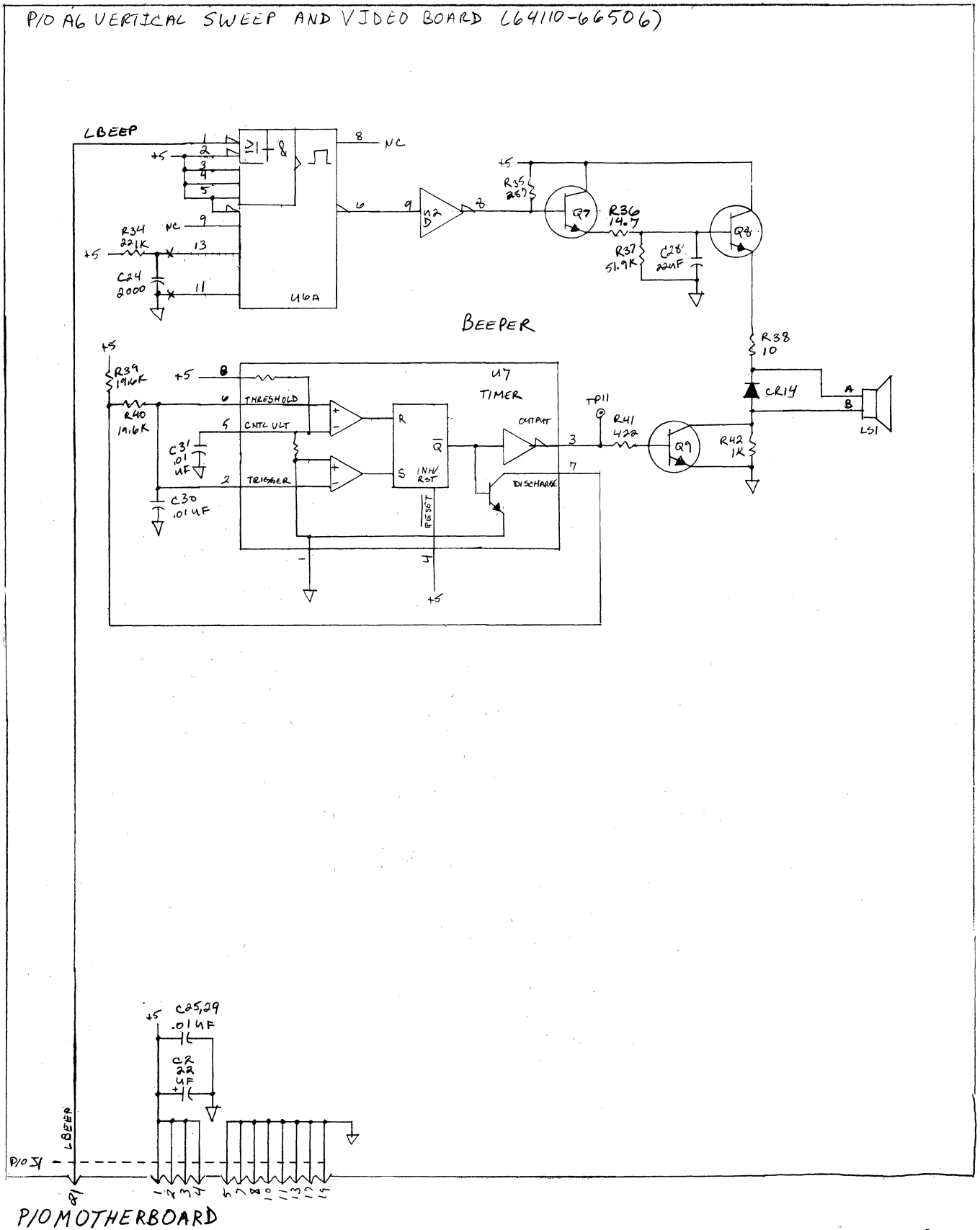


Figure 8-27.
Beeper, Display Driver Schematic 2 of 2
8-165/(8-166 blank) DD

8-373. MNEMONICS.

8-374. Signals in the 64110A have been assigned mnemonics that describe the active state and function of the signal line. A prefix letter (H, L, P, or N) indicates the active state of the signal, and the remaining letters indicate its function. An H prefix indicates that the function is active in the high state; an L prefix indicates that the function is active in the low state. Mnemonics with no L or H prefix should be assumed H. The prefix P indicates that the function is active on the positive-going transition and an N means the function is active on the negative-going transition. Mnemonic definitions are listed alphabetically in table 8-48.

Table 8-48. Mnemonics (1 of 11)

BNC1-4	BNC outputs from rear panel.
CLKIN	Clock Input. Not used.
DOTCLK	Dot Clock. 25 MHz clock for video circuitry.
HADL	High Address Latch. When high, latches the 16 bit address from the LIDA bus into two 8 bit latches, to be sent out on the address Bus.
HBG	High Bus Grant. When high, acknowledges Low Bus Request (LBR) has been received. However, the requesting device must wait until High External Bus Grant is true before using the LIDA bus.
HBON	High Beeper On. When high, activates the beeper.
HCLKCNTL	High Clock Control. When high, allows HPHI1 and 2 to be input directly, as opposed to inputing the clock into CLKIN and having the CPU derive its own HPHI1 and 2.
HDAC	High Data Accepted. Indicates acceptance of data by all devices.
HDBUF	High Data Buffered. When high, enables two 8 bit buffers to transfer data from ROM to the data bus.
HDC0	High Display Counter Zero. Active high, indicates least significant bit of the display address counter is logic low.
HDE	High Display Enable. When high, enables the CRT display.
HDIO1-8	High Data I/O Bits. Connected to HP-IB I/O lines via transceiver chips.
HDOUTB	High Data Out Buffered. Inverted LDOUTB.

Table 8-48. Mnemonics (2 of 11)

HDOUTD	High Data Out Delayed. When high, indicates to the addressed peripheral device the CPU will write data to it. Similar to LDOUT, but delayed until LPHI2.
HEXBG	High External Bus Grant. When high, indicates to the requesting device that it may use the LIDA bus.
HINT	High Interrupt. Inverted LINT.
HIOD0-15	High Input/Output Data 0 through 15. Inverted LIOD0-15; appears on device side of transceiver.
HIR	High Interrupt Request RS232 Write. When high, the CPU is being requested to write to the RS232 port.
HIR (DELTA)T	High Interrupt Request Delta Time. Interrupt signal coming from the delta-time circuitry.
HIRH	High Interrupt Request High. The only high priority interrupt which is sent to the CPU to inform it that power is failing.
HIRH CLR	High Interrupt High Clear. When high, it resets the high level interrupt latch.
HIRHP-IB	High Interrupt Request HP-IB. When high, it requests a low priority interrupt of the processor allowing access through the HP-IB port.
HIRKB	High Interrupt Request Keyboard. When high, a low priority interrupt is sent to the processor requesting it to service the keyboard.
HIRMINI	High Interrupt Request Mini. When high a low priority interrupt is sent to the processor requesting it to service the mini drives.
HIR RS232 RD	High Interrupt Request RS232 Read. When high, the CPU is being requested to read from the RS232 port.
HIRL	High Interrupt Request Low. An external device requests an interrupt by pulling this line high. HIRL is the lowest priority interrupt, and has no preempt abilities, therefore, must wait its turn. HIRH and LPOP can preempt HIRL.

Table 8-48. Mnemonics (3 of 11)

HIR15	High Interrupt 15. Generated in power supply to indicate that a power failure is imminent and causes high level interrupt HIRH.
HKA0-6	High Keyboard Address. Used to decode keyboard.
HKYDET	High Key Detect. Indicates a key is depressed and will step the keyboard scan and send an interrupt to the processor if this is a key change.
HMSTR	High Master. System is acting as master on the bus.
HPBOOT0-1	Boot signals from rear panel. Determines how instrument is booted; PV, flexible disc drive, system bus, etc.
HPCLK1-2	High Processor Clock 1 and 2. Two complementary, nonoverlapping clocks; required by the CPU.
HPHI1-2	High PHI 1-2. Two complementary, nonoverlapping clocks required by several devices on the CPU/IO board for timing.
HPRAS	High BPC Row Address Strobe. Active high, indicates processor accessing RAM. Used only for Signature Analysis troubleshooting.
HPWE	CPU Write Enable. Active high, enables write operation either into RAM or CRT controller.
HRAL	High Register Access Line. When an address on the LIDA bus is within the range reserved for register designation, HRAL goes high to prevent external memory from responding to any memory cycle having the same address.
HRD	High Read. When high, indicates the CPU will read from devices external to it. When low, the CPU will write to devices such as memory.
HRDW	High Read/Write. When high, indicates the CPU will read from devices external to it. When low, the CPU will write to devices such as memory.
HROM	High Read Only Memory. When high, indicates the CPU is addressing ROM (0000-4000 HEX).
HSCLK1	High System Clock 1. A 6.25 MHz clock for CPU/IO board.
HSTB	High Strobe. Complement of LSTB. When high, and in the write mode, indicates the data bus has valid information on it. When high and in the read mode, indicates the CPU is not driving the bus, and the device addressed can now drive it.

Table 8-48. Mnemonics (4 of 11)

HSYNC	High Sync. When high, indicates the CPU is fetching an opcode.
L25MHz	Low 25 MHz Clock. For general purpose bus use.
LA0-15	Low Address 0 through 15. A 16 bit bus demultiplexed from the LIDA0-15 bus. Used by the CPU to address various devices in the system, including ROM. The bus is sent only from the CPU.
LADDCLK	Low Address Clock. Active low, clock signal that increments the display counters.
LATN	Low Attention. Ties to HP-IB ATN line via transceiver. Defines type of data on data bus; address/commands or data.
LBE	Low Bus Enable. Tied to ground.
LBEEP	Low Beep. Output from LBEEPEN.
LBEEPEN	Low Beep Enable. When low, the beeper circuits are enabled.
LBIOSB	Low Buffered Input/Output Strobe. Buffered version of LIOSB.
LBL	Low Byte Left. When low, indicates the left or upper eight data bits of a memory cycle will be used, as opposed to the right or lower eight data bits and is used only when LBYTE is low.
LBR	Low Bus Requested. Provides the way for an external device to request uninterrupted use of the LIDA bus.
LBYTE	Low Byte. When low, indicates that a memory cycle is to involve an eight bit byte, rather than the full sixteen bits of the word.
LCHAR	Low Character Clock. Character clock used by CRT controller chip.
LCS	Low Chip Select. Active low, enables both the read and write functions for the CRT controller.
LD0-15	Low Data 0 through 15. A 16 bit bidirectional bus connected to the LIDA0-15 bus. Used to transfer data to and from the CPU. When LSTB is low, data is present on bus.

Table 8-48. Mnemonics (5 of 11)

LDAV	Low Data Valid. Ties to HP-IB DAV line via transceiver chip. Indicates availability and validity of data on the data bus.
LDBUF	Low Data Buffered. When low, enables two 8 bit buffers to transfer data from the ROMs to the data bus.
LDCAS	Low Display Column Address Strobe. Active low, indicates data request from CRT controller is being serviced.
LDMAR	Low Direct Memory Access Request. A peripheral device pulls this line low when it wants direct access to memory.
LDMARQ	Low Direct Memory Request. Used to request direct memory access cycles to transfer data to the outbound FIFO or from the inbound FIFO. See LHLT.
L(DELTA)T	Low Delta Time. When low it clears the LIR(DELTA)T interrupt and resets the auto-reset counter.
LDOUT	Low Data Out. When low, indicates to the addressed peripheral device, the CPU will write to it.
LDOUTB	Low Data Out Buffered. Buffered version of LDOUT.
LDOUTD	Low Data Out Delayed. Complement of HDOUTD. When low, indicates to the addressed peripheral device the CPU will write data to it. Similar to LDOUT, but delayed until LCLK2.
LDRQ	Low Data Request. Active low signal from CRT controller requesting data.
LEOI	Low End Or Identify. Bidirectional line that ties to HP-IB EOI line via transceiver chip. Indicates end of data transfer or identifies initiation of polling operation.
LERA	Low Extended Register Addressing. When pulled low by an external device, the internal registers have increased addressing range on the LIDA Bus.
LFLG	Low Flag. Can be tested by software. Used as a flag by any peripheral device connected to the CPU. The peripheral devices are wire OR'ed to this line.
LHLT	Low Halt. Can be tested by software. Used as a flag to the CPU by HP-IB.
LHP-IB	Low HP-IB. When low the HP-IB port is being accessed.

Table 8-48. Mnemonics (6 of 11)

LHSYN	Low Horizontal Sync. Active low, signal from display controller to display driver circuitry that enables the horizontal electron beam retrace function.
LIBE	Low Interrupt Buffer. Enables interrupt buffer.
LIC1-2	Low Interface Control 1 and 2. These two lines can provide up to four states used to control peripheral devices. How these lines are controlled is determined by software.
LIC1B	Low Interface Control 1 Buffered. LIC1 signal after being buffered once.
LIC2B	Low Interface Control 2 Buffered. LIC2 signal after being buffered once.
LIC1D	Low Interface Control 1 Delayed. LIC1 signal after being buffered twice.
LIC2D	Low Interface Control 2 Delayed. LIC2 signal after being buffered twice.
LID	Low ID. Enables Card Select to output ID of option.
LIDA0-15	Low Instruction/Data/Address 0 through 15. A 16 bit bidirectional bus the CPU uses to communicate over. Information is true low. In this system, the bus is demultiplexed into separate address and data buses.
LIFC	Low Interface Clear. Ties to HP-IB IFC line via transceiver chip. Places I/O system into known idle state.
LIMASK	Low Interrupt Mask Address. When low, enables interrupt mask latch.
LINSYN	Line Synchronization. Generated by the power supply. The sync pulses are counted by delta time counter which reaches its terminal count in about 2 seconds at which time reset signal LPOP is generated if the CPU doesn't reset the counter before the terminal count is reached.
LINT	Low Interrupt. The CPU pulls this line low to poll the input/output bus to determine which peripheral device needs service.
LINT MASK	Low Interrupt Mask. When low the interrupt mask is enabled to allow decoding of the low level interrupts.

Table 8-48. Mnemonics (7 of 11)

LIOD0-15	Low Input/Output Data 0 through 15. A 16 bit bidirectional bus. The CPU uses this bus to communicate with I/O ports. Information is true low, and is used in conjunction with LPAB0-3.
LIOSB	Low Input/Output Strobe. When low, indicates the data on the input/output bus is valid.
LIR (DELTA)T	Low Interrupt Request Delta Time. Generated from HIR (DELTA)T. When low, it requests a low priority interrupt of the CPU and if not serviced in 2.3 seconds a LPOP will be generated, in the auto-reset circuit, resetting the processor.
LIRHP-IB	Low Interrupt Request HP-IB. Generated from HIRHP-IB. When low, it requests a low priority interrupt of the processor allowing access through the HP-IB port.
LIRKB	Low Interrupt Request Keyboard. Inverted HIRKB.
LIRMINI	Low Interrupt Request Mini. Generated from HIRMINI. When low a low priority interrupt is sent to the processor requesting it to service the mini drives.
LIR RS232 RD	Low Interrupt Request RS232 Read. Generated from HIR RS232 RD. When low, the CPU is being requested to read from the RS232 port.
LIR RS232 WR	Low Interrupt Request RS232 Write. Generated from HIR RS232 WR. When low the CPU is being requested to write to the RS232 port.
LIRH	Low Interrupt Request High. Generated from HIRH. An external device requests an interrupt by pulling this line low. LIRH has a higher priority than Low Interrupt Request Low (LIRL), and can preempt the lower priority even while it is in process. LPOP can preempt LIRH.
LIRHCLR	Low Interrupt High Clear. Generated from HIRHCLR. When low it resets the high level interrupt latch.
LIRL	Low Interrupt Request Low. Generated from HIRL. An external device requests an interrupt by pulling this line low. LIRL is the lowest priority interrupt, and has no preempt abilities, therefore, must wait its turn. LIRH and LPOP can preempt LIRL.
LIR15	Low Interrupt 15. Generated from HIR15 in power supply to indicate that a power failure is imminent and causes high level interrupt LIRH.

Table 8-48. Mnemonics (8 of 11)

LIVID	Low Inverse Video. Active low, signal from display controller to display driver circuitry that enables half-bright dot on CRT screen.
LKYBD	Low Keyboard. When low and the interrupt mask is enabled, LIRKB is generated.
LLCAS	Low Lower Byte Column Address Strobe. When low, strobes column address to lower byte in RAM.
LLDCNT	Low Load Display Counter. Active low, loads the first address of display memory into the display address counters U58, U59, and U60.
LLRAS	Low Lower Byte Row Address Strobe. When low, strobes row address to lower byte in RAM.
LMAP1-3	Low Peripheral Addresses. Selects one of nine peripheral address commands used to enable or activate various I/O circuits.
LMSYN	Low Memory Sync. A signal from addressed devices. When low, forces the CPU to wait until the addressed device can complete the read or write operation.
LOPCODE	Low Opcode. When low, indicates to a HP Model 1611A Logic State Analyzer the information on the data bus is an opcode. Used for factory troubleshooting.
LPAB0-3	Low Peripheral Address Bus 0-3. Identifies which one of 16 peripheral devices will be involved in an I/O operation.
LPA0-3	Low Peripheral Address Bus 0 through 3. Identifies which one of 16 peripheral devices will be involved in I/O operation.
LPBE	Low Processor Buffer Enable. Always low. Enables the internal CPU buffers for the LIDA bus.
LPBO	Low Processor Buffer Out. Controls the direction of the CPU's internal, bidirectional, LIDA buffers. When low, information is transmitted from the CPU.
LPCAS	Low Processor Column Address Strobe. Active low, indicates CPU is accessing RAM in either read or write operation.
LPFAIL	Low Power Fail. Active low, indicates main AC power is too low to operate system.

Table 8-48. Mnemonics (9 of 11)

LPFS	Low Power Fail Set Address. When low, sets power fail latch which in turn provides LPFAIL to the CPU/IO board via the mainframe bus.
LPHI1-2	Low Clock 1-2. Two complementary, nonoverlapping clocks; required by several devices on the CPU/IO board for timing.
LPDR	Low Processor Drive. When low, the CPU is driving the LIDA bus.
LPOP	Low Power On Pulse. When low, initializes and prevents the CPU from running. When LPOP is released, the processor begins operation at address 20 Hex. LPOP is synchronized with LPHI1 before being input to the CPU. LPOP can preempt LIRL and LIRH.
LPOPB	Low Power On Pulse Buffered. Buffered LPOP.
LRKBD	Low Read Keyboard. When low data on data bus is from keyboard.
LRAMCLK	Low RAM Clock. A 12.5 MHz clock for RAM and display functions.
LRSRD	Low RS-232C Read Address. When low, serves as read command to RS-232C transceiver (USART).
LRSWR	Low RS-232C Write Address. When low, serves as write command to RS-232C transceiver (USART).
LRS232RD	Low RS232 Read. When low and the interrupt mask is enabled, LIR RS232 RD is generated.
LRS232WR	Low RS232 Write. When low and the interrupt mask is enabled, LIR RS232 WR is generated.
LSCLK1	Low System Clock 1. A 6.7 MHz clock used throughout the system.
LSLOT SEL	Low Slot Select. When low the slot select buffer (UXX) is enabled.
LSMC	Low Synchronized Memory Complete. A CPU output, not used in this system.
LSEL0-4	Low Slot Select. Goes to each of the 5 card slots and causes each card to generate its unique ID code. LIDEN must also be present.

Table 8-48. Mnemonics (10 of 11)

LSTB	Low Strobe. Active low, during write operation, indicates data bus information is valid; during read operation indicates CPU is not driving the data bus and addressed device can drive data bus.
LSTM	Low Start Memory. Used to initiate a memory cycle. When low, indicates that the information on the address bus is valid.
LSTS	Low Status. Can be tested by software. Used as a flag by any peripheral device connected to the CPU. The peripheral devices are wire OR'ed to this line.
LUMC	Low Unsynchronized Memory Complete. When low, allows the CPU to complete its memory cycle. If the memory needs to make the processor wait, due to long access times, it pulls LMSYN low, causing LUMC to go high. When LUMC is high the CPU must wait.
LUCAS	Low Upper Byte Column Address Strobe. When low, strobes column address to upper byte in RAM.
LUPB	Low Upper Byte. Active low, indicates only upper eight bits of data bus involved in memory operation. When this signal is high, indicates lower eight bits being used. LUPB is gated by LBYTE.
LURAS	Low Upper Byte Row Address Strobe. When low, strobes row address to upper byte in RAM.
LVID	Low Video. Active low, signal from display controller to display driver that enables full-bright dot on CRT screen.
LVSYN	Low Vertical Sync. Active low, signal from display controller to display driver circuitry that enables the vertical electron beam retrace function.
LWLB	Low Write Lower Byte. When low, writes data to lower byte in RAM.
LWRT	Low Write. Active low, CPU writes to addressed device.
LWUB	Low Write Upper Byte. When low, writes data to upper byte in RAM.
PA0-15	Peripheral Address 0 through 15. Outputs from peripheral address decoder used to select I/O functions.

Table 8-48. Mnemonics (11 of 11)

RAMCLK	RAM Clock. Timing signal used in all RAM operations.
REN	(Low) Remote Enable. Ties to HP-IB REN line via transceiver. Enables alternate devices to provide programming data.
RCARRY	Ripple Carry. Indicates sequencer Ú2 has returned to initial state.
RFD	(High) Ready For Data. Indicates that devices are ready to accept data. Ties to HP-IB NRFD line via transceiver chip.
R/W	Read/Write Command. When high, specifies that the PHI chip perform a write function; when low, specifies a read function.
SHUTDOWN	Is generated in several places and is responsible for turning off the PWMs.
SRQ	(Low) Service Request. Ties to HP-IB SRQ line via transceiver. Indicates a need for service; causes interrupt of current sequence in CPU.

HEWLETT PACKARD

MODEL 64110A
MAINFRAME FLEXIBLE DISC DRIVE
(FLOPPY)

REPAIR NUMBERS

This mainframe manual applies directly to Models with serial numbers prefixed 2103A - 21038A.

© copyright Hewlett-Packard Company/Colorado Springs Division 1982
1900 Garden of the Gods Road, Colorado Springs, Colorado, U.S.A.

All Rights Reserved

Manual Part Number 64110-90901
Microfiche Part Number 64110-90801

PRINTED: MARCH 1982

SAFETY SUMMARY

The following general safety precautions must be observed during all phases of operation, service, and repair of this instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the instrument. Hewlett-Packard Company assumes no liability for the customer's failure to comply with these requirements.

GROUND THE INSTRUMENT.

To minimize shock hazard, the instrument chassis and cabinet must be connected to an electrical ground. The instrument is equipped with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE.

Do not operate the instrument in the presence of flammable gases or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS.

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE.

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT SUBSTITUTE PARTS OR MODIFY INSTRUMENT.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the instrument. Return the instrument to a Hewlett-Packard Sales and Service Office for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

Dangerous voltages, capable of causing death, are present in this instrument. Use extreme caution when handling, testing, and adjusting.

SS-1-1/76

Section TABLE OF CONTENTS Page

Section TABLE OF CONTENTS Page

Section TABLE OF CONTENTS Page

Section TABLE OF CONTENTS Page

LIST OF ILLUSTRATIONS

Figure LIST OF ILLUSTRATIONS (Cont'd) Page

Title

LIST OF TABLES

Table Title Page

SECTION I

GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. This manual contains information and theory necessary to operate, install, maintain, and troubleshoot the (FLOPPY) flexibe disc drives in the 64110A mainframe.

1-3. SAFETY CONSIDERATIONS.

1-4. The flexible disc drive units are installed in a 64110A Mainframe and contains voltages in +-12 V range. Review the mainframe service manual for general safety considerations.

1-5. PHYSICAL DESCRIPTION.

1-6. Each flexible disc drive is a semi-random access mass storage system employing a flexible magnetic medium. It consists of a servo electronics circuit board, a drive electronics circuit board, and a RS-232/mini control board.

1-7. Each drive module contains all the mechanical parts necessary for physically handling the disc. These include the drive spindle and motor, 2 heads each having read/write and erase capability, write protect sensor, track 0 sensor, index sensor, and activity LED on the front panel. Each drive module also contains a servo control board which controls the DC drive motor speed and a drive electronics board which interprets and generates control signals, controls movement of the read/write head to the correct position, and also reads and writes data.

1-8. The flexible magnetic medium used for Local Mass Storage is called a flexible disc. A disc measures 133.4 mm (5.25 inches) in diameter and has a 3.8 cm (1.5 inch) hole for alignment on the disc drive spindle. The disc is enclosed in a protective polyvinylcholride (PVC) jacket with a slot for access to the recording surfaces. Both sides of the flexible disc are used for data storage.

1-9. The recording head in the drive module is positioned by a mechanism driven by a stepper motor and taut metal band. The head positioning mechanism operates in an open loop configuration; that is, there is no feedback to the drive electronics board to determine the actual position of the head.

1-10. The heads are mechanically coupled to the door mechanism so that closing of the door (pushing the latch to the left) causes the heads to make contact with the media.

1-11. ENVIRONMENTAL AND PHYSICAL SPECIFICATIONS.

1-12. OPERATING ENVIROMENT.

1-13. The flexible disc drives may be operated in environments within the following limits:

a. Relative Humidity: 20% to 80% while at 29.4°C (85°F)
b. Altitude: 0 to 4572 m (0 to 15000 ft)

It should be protected from temperature extremes which cause condensation within the instrument.

1-14. STORAGE ENVIRONMENT.

1-15. The fexible disc drive may be stored or shipped in environments within the following limits:

a. Temperature: -41°C to 71°C (-40.8°F to 159.8°F)
b. Relative Humidity: 20% to 80% at 29.4°C (85°F)
c. Altitude: 0 to 4572 m (0 to 15000 feet)

1-16. RECORDING CHARACTERISTICS.

1-17. HP PHYSICAL TRACK FORMAT.

a. Recording Mode: Modified Frequency Modulated (MFM)
b. Rotational Speed: 300 RPM +-1.5% (+-4.5 RPM)
c. Bit Density: 5456 BPI on Track 34
d. Tracks Per Inch: 48
e. Sides Per Disc: 2
f. Tracks Per Sides: 35
g. Sectors Per Track: 16
h. Bytes Per Sector: 256 (362 including overhead bytes)
i. Bytes Per Disc: 286,720 (formatted) 420,000 (unformatted)

1-18. MEDIA LIFE.

a. Revolutions 2,500,000 revolutions on any track.

b. Head Life: More than 15,000 hours of operation with HP media.

1-19. PERFORMANCE SPECIFICATIONS.

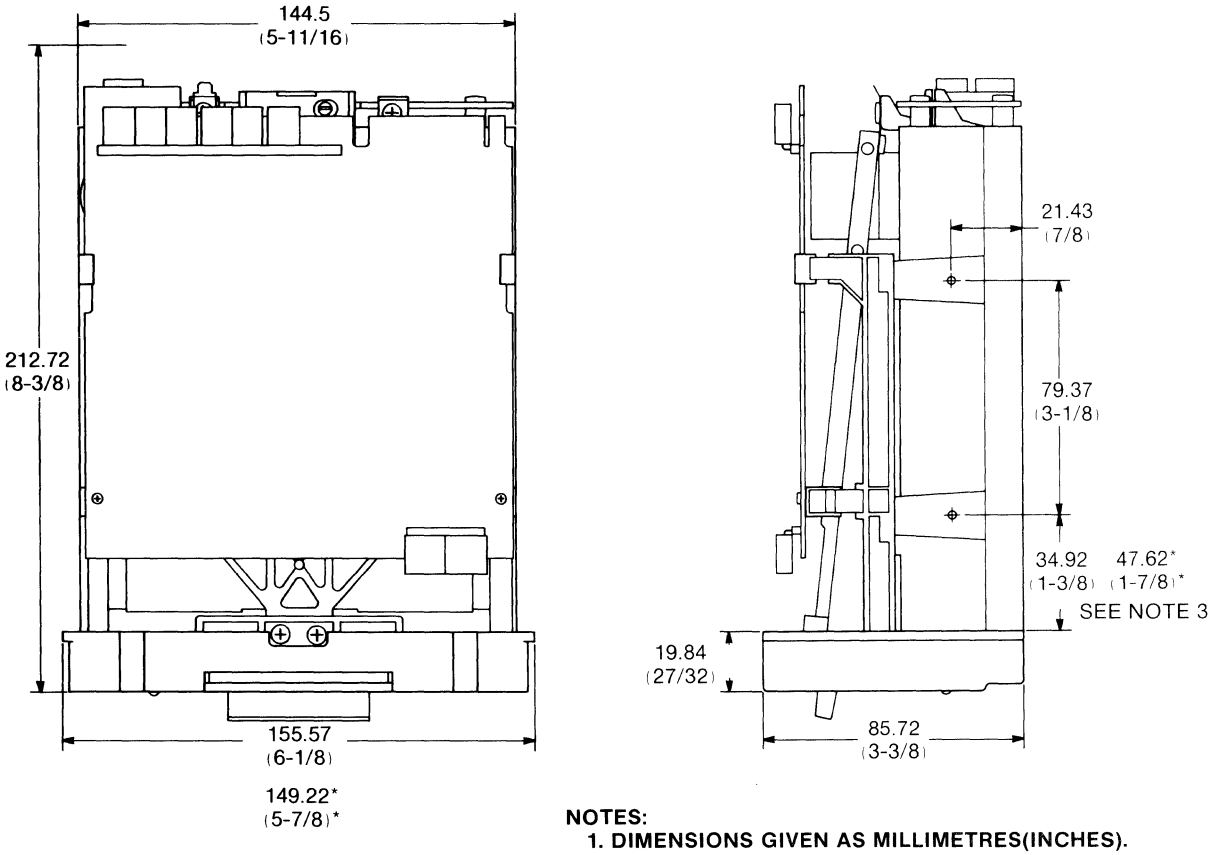
a. Soft Read Errors: 1 in 10 billion bits read on innermost track.
b. Seek Errors: 1 in 10 million seeks.
c. "Soft Error" is defined as an error that cannot be recovered from using an HP approved retry scheme.

1-20. ALIGNMENT LIMITS.

a. Radial Alignment: 1.1 mils maximum of track center at track 16 measured at 20°C (68°F) and 50% humidity.
b. Azimuth: 18 degrees maximum clockwise or counterclockwise on tracks 16 and 34.

1-21. PHYSICAL DIMENSIONS.

1-22. Figure 1-1 illustrates the physical dimensions of a single flexible disc drive unit.



NOTES:
1. DIMENSIONS GIVEN AS MILLIMETRES(INCHES).
2. *DENOTES DIFFERING TANDON DRIVE DIMENSIONS.
3. THIS DIMENSION FROM BACK OF FACEPLATE.

Figure 1-1. Physical Dimensions

1-23. POWER REQUIREMENTS.

1-24. Table 1-1 gives the power requirements for a single or double flexibl disc drive plus a RS-232/mini control board. The values include the power-up transient which is considered to be the most limiting case.

Table 1-1. Power Requirements

With (1) drive	+5V current use =	1.7A - 1.8A	During PV
With (2) drives	+5V current use =	3.4A - 3.6A	During PV

1-25. FLEXIBLE DISC DRIVE ASSEMBLIES.

1-26. The flexibe disc drives used in the 64110A mainframe are Model HP9130K drives with the following:

1-27. Drive board P/N 09130-66501.

1-28. Mechanical drive assembly with servo board and front panel P/N 4040-1915 and door latch P/N 4040-1913 and associated hardware. This part also has an exchange assembly number HP P/N 09130-69600.

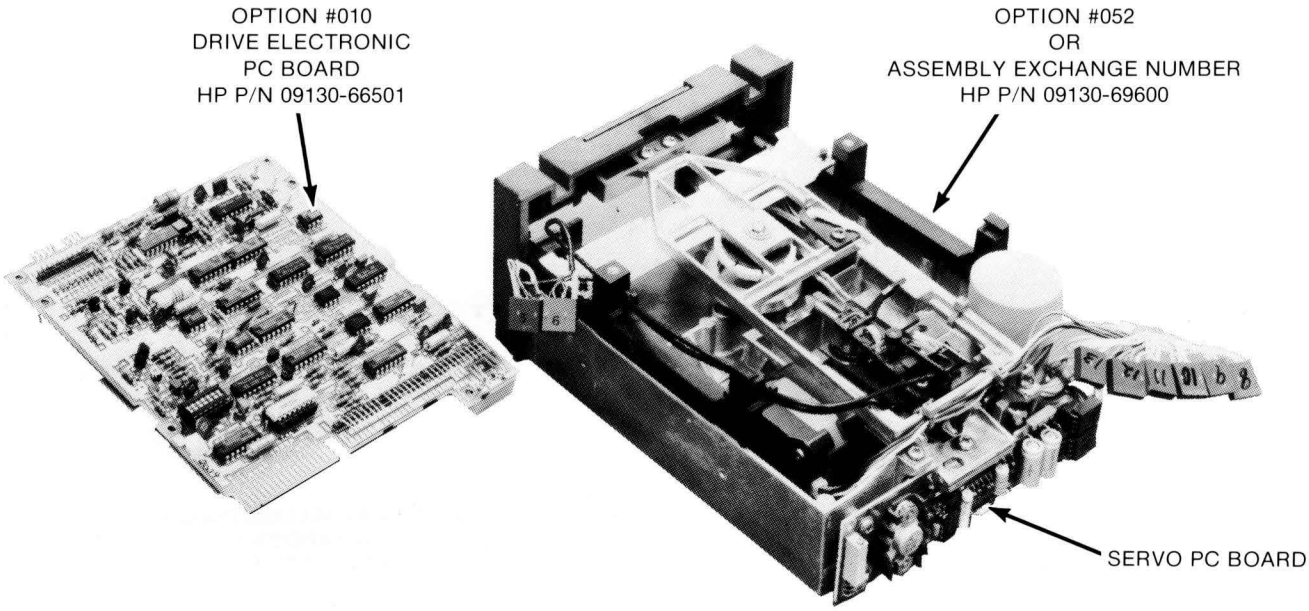


Figure 1-2. Exchange Assembly

1-29. RECOMMENDED TEST EQUIPMENT.

1-30. Refer to table 1-2 for a list of recommended test equipment.

Table 1-2. Recommended Test Equipment

Product Support Package	
Service Kit	
Alignment tool or small shank screwdriver	
HP 5314A or equivalent frequency counter	
Spindle motor adjustment tool	P/N 8710-1385
Oscilloscope	HP 1740A or equivalent
Alignment Disc	P/N 9164-0151
Torque Driver	P/N 8710-0670
#1 Posidriv Screwdriver	P/N 8710-0899
#2 Posidriv Screwdriver	P/N 8710-0900
3/16 Thin Wall Nutdriver	P/N 8720-0001
5004 or 5005 Signature Analyzer.	

SECTION II

INSTALLATION AND REMOVAL

2-1. INTRODUCTION.

2-2. This section contains information for unpacking, initial inspection, installation and removal of the flexible disc drives.

2-3. The flexible disc drive units are installed in a 64110A Mainframe at the factory. Therefore, the initial inspection procedure assumes the units are installed. An installation and removal procedure will be included for installing a new unit or removing a defective unit.

2-4. FLEXIBLE DISC DRIVE REMOVAL PROCEDURE.

2-5. The following procedure should be used when removing a flexible disc drive unit from a 64110A Mainframe.

a. Switch power OFF on the mainframe and disconnect the AC power cord.

b. Remove the top and bottom covers. There is one screw for each cover on the rear that holds it in place. Gently slide the covers back for removal (see fig. 2-1).

c. Remove two screws (H26) on the underneath of the mini drive bezel (A10MP1).

d. Pull the bezel forward from its top. There are two tabs on the top of the bezel which need to be gently pried away from the front panel with a flat screwdriver while pulling the bezel out from the top. Remove bezel.

e. Remove the two screws attaching the right side cover (side with handle) and the one screw holding the left side cover and remove.

f. Remove the high voltage cover (MP66) by removing the six screws (H29) and two flexible disc drive hold down screws (H24).

```
**********************************************************************
*                                                                    *
*                            WARNING                                 *
*                                                                    *
*  Exercise EXTREME CAUTION with the high voltage cover off!         *
*  Lethal voltages exist in the area under the HV cover.             *
*                                                                    *
**********************************************************************
```

g. Remove four screws (H24) on top and bottom of EM shield (MP2) which hold both left and right flexible disc drives in place.

h. Unplug the drive keyed-power-cable P2 from J2 and disconnect ribbon control cable P1 from J1. Exercise caution when removing and installing cable connectors.

i. Slide flexible disc drive(s) out of mainframe gently.

2-6. Reverse the removal procedure for installation of the flexible disc drive(s). Make sure cables and connectors are firmly attached.

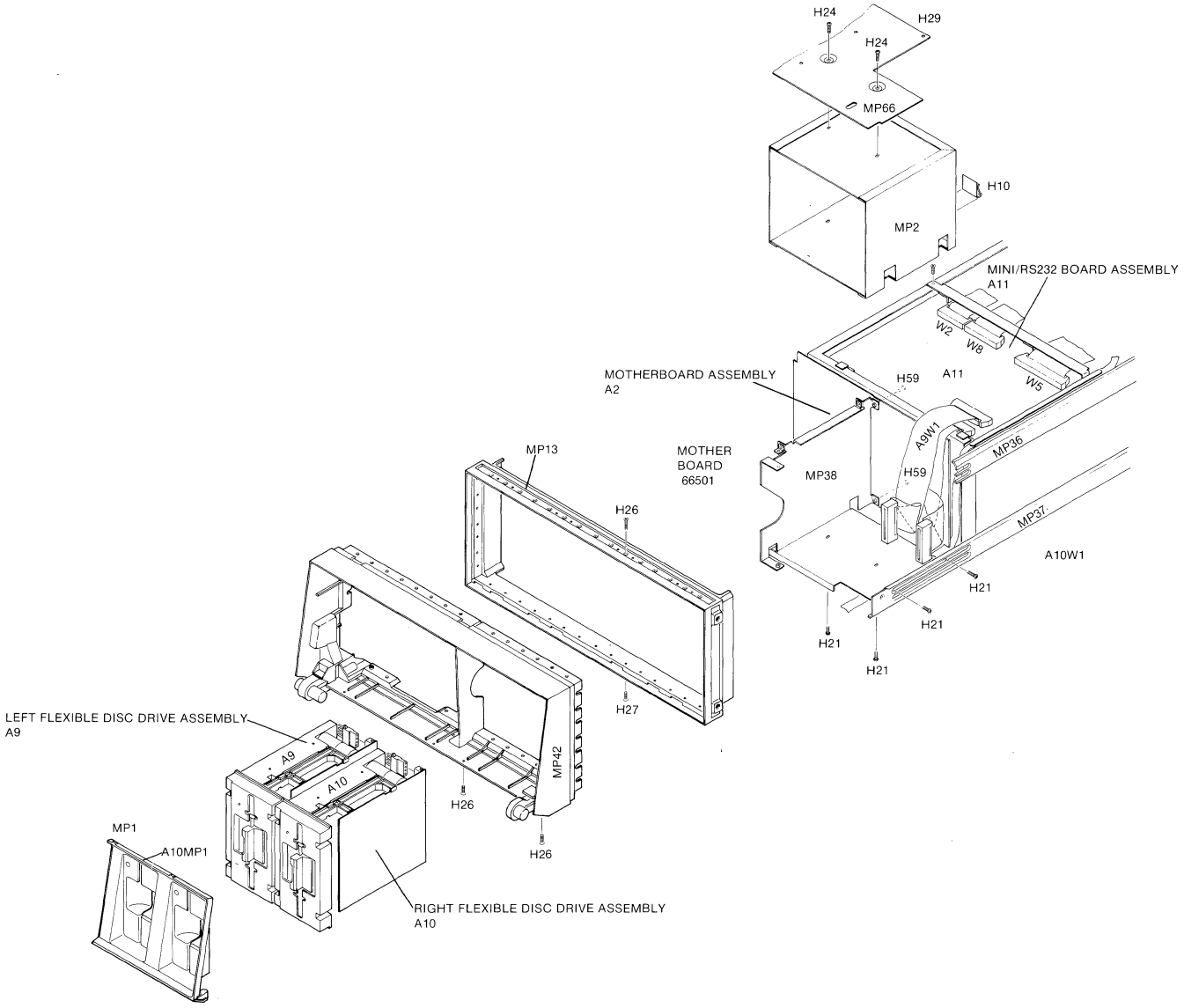


Figure 2-1. Flexible Disc Drive Removal

2-7. FLEXIBLE DISC DRIVE JUMPER CONFIGURATIONS.

2-8. Each flexible disc drive is shipped with a jumper block installed on the drive electronics board. The specific configuration of the jumper block installed depends on the board part number and the particular installation.

2-9. The jumper configurations described here are found on the 09130-66501 drive electronics board.

2-10. The jumpers on the 09130-66501 drive electronics board are located in a 16 pin DIP socket designated U1E. The jumpers and their functions are listed in table 2-1.

Table 2-1. Flexible Disc Drive Jumpers and Functions

Jumper Name	U1E Pin Numbers	Function
1 HS	1 and 16	The head load solenoid is activated when the drive is selected if this jumper is left installed. Since the flexible disc drive does not have a head load solenoid, this jumper is a don't care.
2 DS0	2 and 15	When this jumper is intact, the drive responds to drive address 0.
3 DS1	3 and 14	When this jumper is intact, the drive responds to drive address 1.
4 DS2	4 and 13	When this jumper is intact, the drive responds to drive address 2.
5 DS3	5 and 12	When this jumper is intact, the drive responds to drive address 3.
6 MUX	6 and 11	When this jumper is intact, the drive is always selected. This jumper should only be used in installations having one drive on the mainframe. The 64110A has two drives so this is not installed.
7 NOT USED	7 and 10	This jumper is not used.
8 HM	8 and 9	If both the HS and HM jumpers are left intact, the motor will come on when the drive is selected. The drives are shipped with 7 jumpers in the jumper block (the HM jumper is left open).

2-11. TERMINATION RESISTOR PACKAGES.

2-12. On drive electronics board P/N 09130-66501, the 16 pin DIP socket U2F is for insertion of the termination resistor package. The resistor package must be installed. The unit is shipped this way.

2-13. SOLDERED JUMPERS.

2-14. Jumper wires are soldered in R50 and R56. Locations R51 and R57 are left open. The unit is shipped this way.

2-15. PACKAGING.

2-16. ORIGINAL PACKAGING.

2-17. Containers and packing materials identical to those used in factory packaging are available through Hewlett-Packard offices.

2-18. OTHER PACKAGING.

2-19. The following general instructions should be used for re-packing the flexible disc drive with commercially available materials:

a. Wrap the flexible disc drive P/N 09130-69600 flexible disc drive in heavy paper or plastic.

b. Use a strong shipping container. A double-wall carton made of 350-pound test material is adequate.

c. Use a layer of shock-absorbing material 70 to 100 mm (3 to 4 in) thick around all sides of the flexible disc drive to provide firm cushioning and prevent movement inside the container.

d. Seal shipping container securely.

e. Mark shipping container FRAGILE to ensure careful handling.

f. In any correspondence, refer to instrument by model number and full serial number.

2-20. FLEXIBLE DISC MEDIA.

2-21. The storage medium used in the flexible disc drive, is a flexible disc. Both sides of the flexible disc are used for data storage. Each disc must be initialized before it can be used for data storage. The initialization procedure marks each disc track, checks for defective tracks, and establishes file directories. Refer to the formatting procedure in section III of this manual and the Flexible Disc Drive Reference Manual for specifi details.

CAUTION

Only HP media is approved for use in the 9130K flexible disc drive. Use of other media may result in premature disc failure or damage to the drive. HP media will always have an HP label on it.

HP rigorously tests each batch of media for error rate and wear performance in addition to initial vendor qualification. Only in this way can HP assure reliable media performance.

The use of non-HP media for single use applications such as data interchange will probably not damage the drive or media but, if extended use is anticipated, the data must be transferred to HP media.

Extended use of non-HP approved media will void warranty and service contracts on the instruments.

SECTION III

OPERATION

3-1. INTRODUCTION.

3-2. Complete operation of the flexible disc drive is beyond the scope of this manual. Please refer to the Flexible Disc Drive Reference Manual for complete operating instructions.

3-3. OPERATING CLEANLINESS.

3-4. To prevent potential damage or data loss, it is extremely important to maintain the cleanliness of the disc and air within the disc drive. The disc drive should not be operated in an environment in in which dust, smoke, moisture, oil or chemical vapor or other foreign matter are present. Also, be sure to strictly follow the disc handling guidelines, found in the Flexible Disc Drive Reference Manual.

3-5. DISC LOADING.

3-6. Insert the flexible disc into the drive (be sure that the label faces right and the notch is facing up). Push the disc in until it hits against the rear of the disc drive, then close the door latch. Never force the latch, as the media can be latched off center within the protective jacket.

3-7. WRITE PROTECTION.

3-8. The disc has the capability of being write protected. This feature prevents the accidental erasure of data previously recorded on the disc. The write protect is enabled when the write protect notch on the jacket of the disc is covered (see fig. 3-1). When the notch is uncovered, data can be written on the disc.

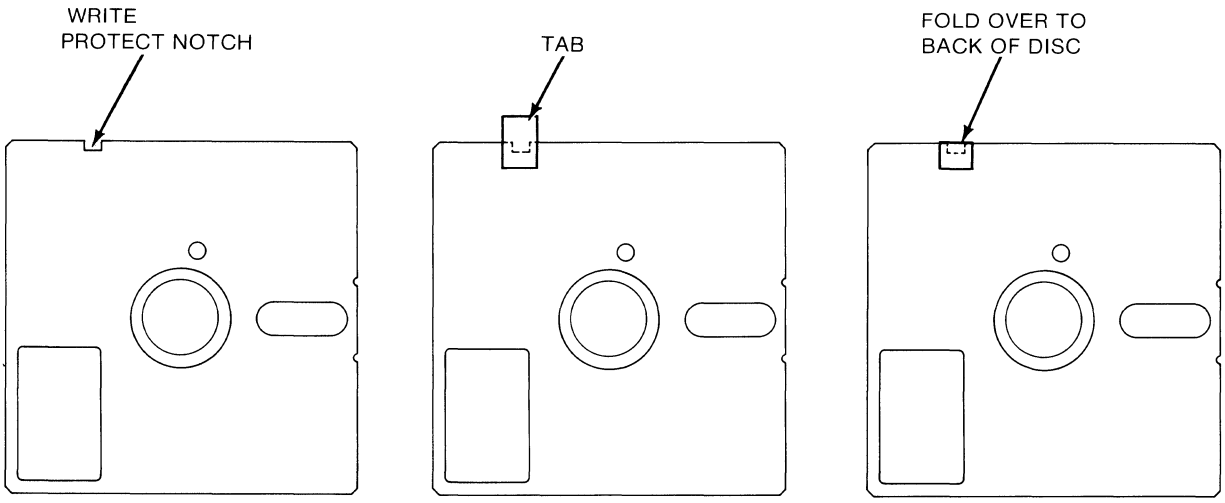


Figure 3-1. Write Protect Tab Installation

3-9. FORMATTING THE DISC.

3-10. Use the following procedure to format a disc:

```
*****************************************
*                CAUTION                *
*                                       *
* Formatting a disc causes all data on  *
* that disc to be destroyed.            *
*****************************************
```

a. Turn on mainframe.

b. Press --Floppy-- soft key.

c. Press disc_utility soft key.

d. Press format.

e. Type in the number of the drive (0 or 1) that the formatting is to occur on (0=left drive, 1=right drive).

f. Press return.

SECTION IV

PERFORMANCE TESTS

4-1. INTRODUCTION.

4-2. This section describes the Performance tests for the flexible disc drive . There are two modes of testing, performance verification and operation verification. Refer to the portion of the mainframe service manual for more information on initiating performance verification.

4-3. The performance verification test will verify to an 85% confidence level that the mini drives are functioning correctly.

4-4. The operation verification procedures allow the operator to verify all specifications; and, with the aid of error codes in the troubleshooting portion of Section VIII (see par. 8-125), troubleshoot the flexible disc drives from the mainframe keyboard.

4-5. PERFORMANCE VERIFICATION TEST PROCEDURE.

4-6. In order to initiate mainframe performance verification (PV) the following methods may be used:

a. Place the control source switches in the performance verification position shown on the control source label on the rear panel.

b. Turn power OFF then back ON. The display test pattern (see fig. 4-1) should be on screen.

c. Press the PVTESTS softkey.

d. Press the NEXT TEST softkey until the FLOPPY DISC DRIVE test is displayed (see fig. 4-2).

e. Press START to initiate the test. Press START again to stop test.

f. If no more tests are required, change control source switches to the desired boot source and press END TESTS and the system will re-boot.

OR

g. There is another method that can be initiated from the front panel when a boot is from a hard disc or floppy disc if the operating software has been loaded. To do this, press CNTL and RESET together.

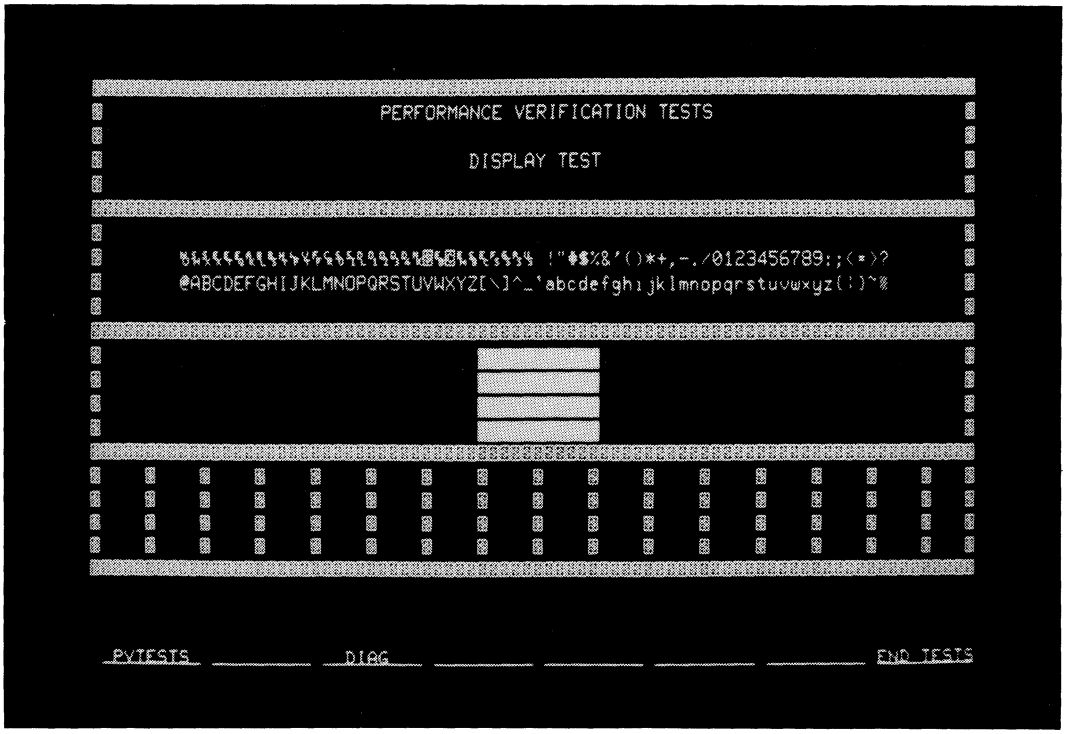


Figure 4-1. Display Test Pattern

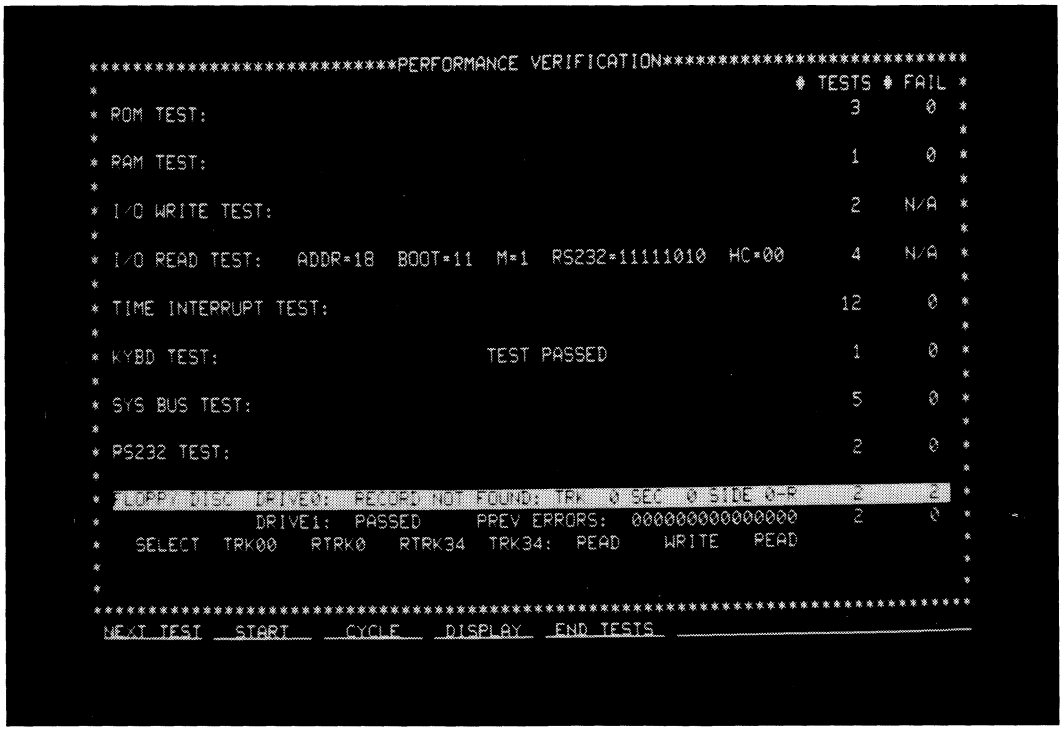


Figure 4-2. PV Test Display

4-7. During the Floppy test the mainframe software will perform eight tests on the flexible disc drives. A description of each test is given in section VIII (see par. 8-105). The following is the sequence of events that occurs during a test cycle.

```
*******************************************************
*                      NOTE                           *
*                                                     *
*  It is required that a formatted disc be used       *
*  when performing the floppy PV. Also, the           *
*  WRITE electronics are not tested if a disc         *
*  containing data on track 34 is present in the      *
*  drive being tested. Furthermore, the floppy        *
*  PV will only verify to an 85% confidence           *
*  level that the disc drives are operational.        *
*  In order to completely test the drives,            *
*  the floppy drive diagnostics (operation            *
*  verification) must also be performed.              *
*******************************************************
```

Purpose:

The FLOPPY DISC TEST tests several functions of the two flexible disc drives and the RS-232/mini controller board electronics.

Area Tested:

CPU and I/O data lines, floppy controller board electronics, the cable from the RS-232/mini board to the drives, drive READ/WRITE electronics and mechanics, and the CPU/IO and floppy I/O data and control line cable.

Operation:

a. Response from floppy controller chip is tested by writing a pattern to the track register in the mini drive controller chip (MDC) and reading it back.

b. When initiated, each floppy drive is cycled through the following series of tests:

1. The drive is selected.

2. The drive is restored (head moved to track 00).

3. Step inward to track 1 (check TRK00 indicator OFF)

4. Step out to track 00, check track 0 indicator ON.

5. Read all sectors on track 0, side 0; check for all errors.

6. Step to track 34, read all sectors on both sides.

c. The PV routines now check to see if there is any data on track 34. Track 34 will be a spare track on a disc with no bad tracks. However, if there is a bad track on a disc, then track 34 is allocated as useable even though it may contain information.

d. If data exists on track 34, a READ/WRITE test is not performed and a message indicating this is displayed on the CRT. If track 34 is available, the following is performed:

7. Known data on side 0, sector 0 is read.

8. A random data pattern is written to side 0, sector 1.

9. The pattern is read from side 0 sector 1 and compared with what was written.

10. Steps 7,8 and 9 are repeated on track 34,side 1.

4-8. When a test fails an error message is displayed. Refer to table 8-1 (Mini Floppy PV Error Messages) for a quick reference explanation of the error messages, and refer to table 8-2 for a detailed description of each error message and some possible trouble and corrective measures to service a failure.

4-9. When the test passes, a binary error word is displayed which indicates the area of previous failures. This word will contain a one wherever a failure has previously occured and can be decoded to correspond with the error messages normally displayed. Refer to table 8-1 for an explanation of the error messages.

4-10. OPERATION VERIFICATION TESTS.

4-11 In order to perform the operation verification tests the following sequence should be used to access the DIAG mode tests:

a. Place the control source switches in the performance verification position shown on the control source label on the rear panel.

b. Turn power OFF then back ON. The display test pattern (see fig. 4-1) should be on screen.

c. Press the DIAG softkey. The Floppy Disc Diagnostic Display (see fig. 4-3) should be displayed.

d. Press the DIAG softkey again. The Floppy Test Menu First Level (see fig. 4-4) should be displayed.

e. Set up desired tests and press the TEST softkey to initiate. The Floppy Test Menu Second Level (see fig. 4-5) should be displayed.

f. When the desired test is finished press the STOP TEST softkey.

g. Press END DIAG to exit the DIAG mode. The display test pattern should be on screen.

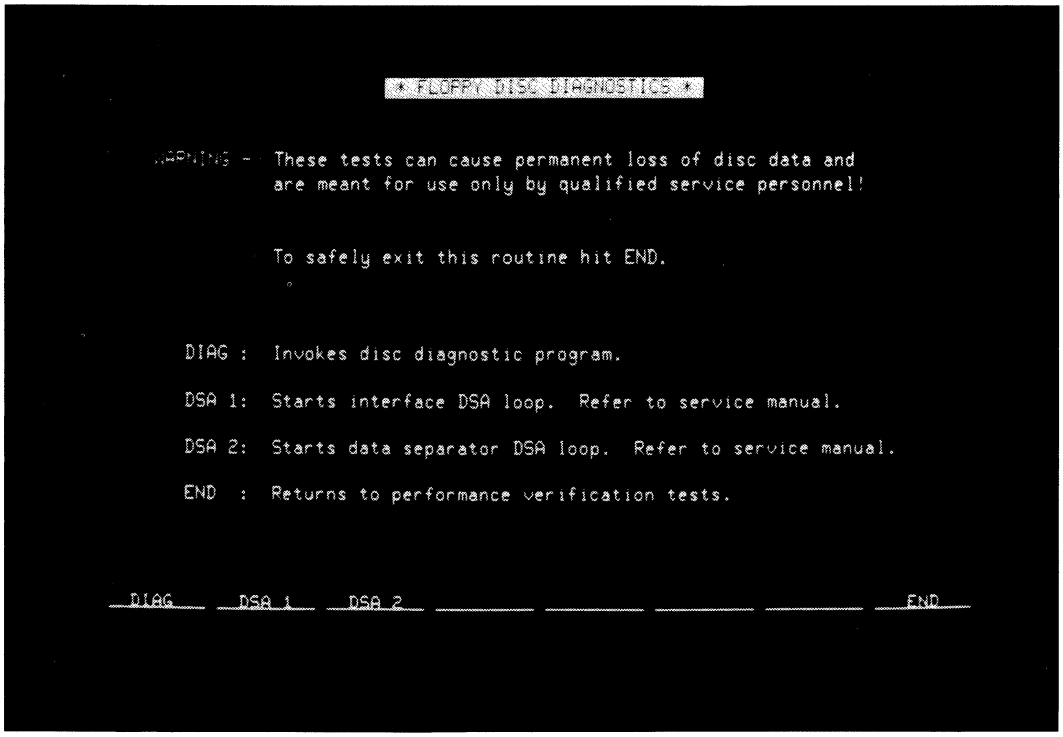


Figure 4-3. Floppy Disc Diagnostic Display

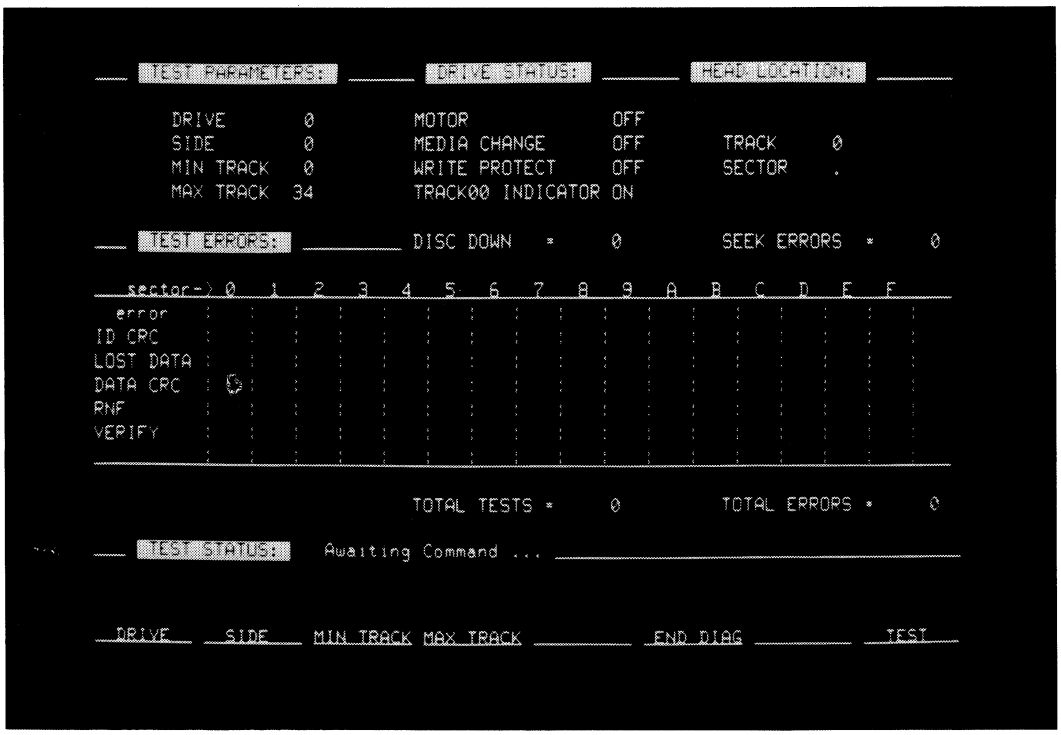


Figure 4-4. Floppy Test Menu First Level

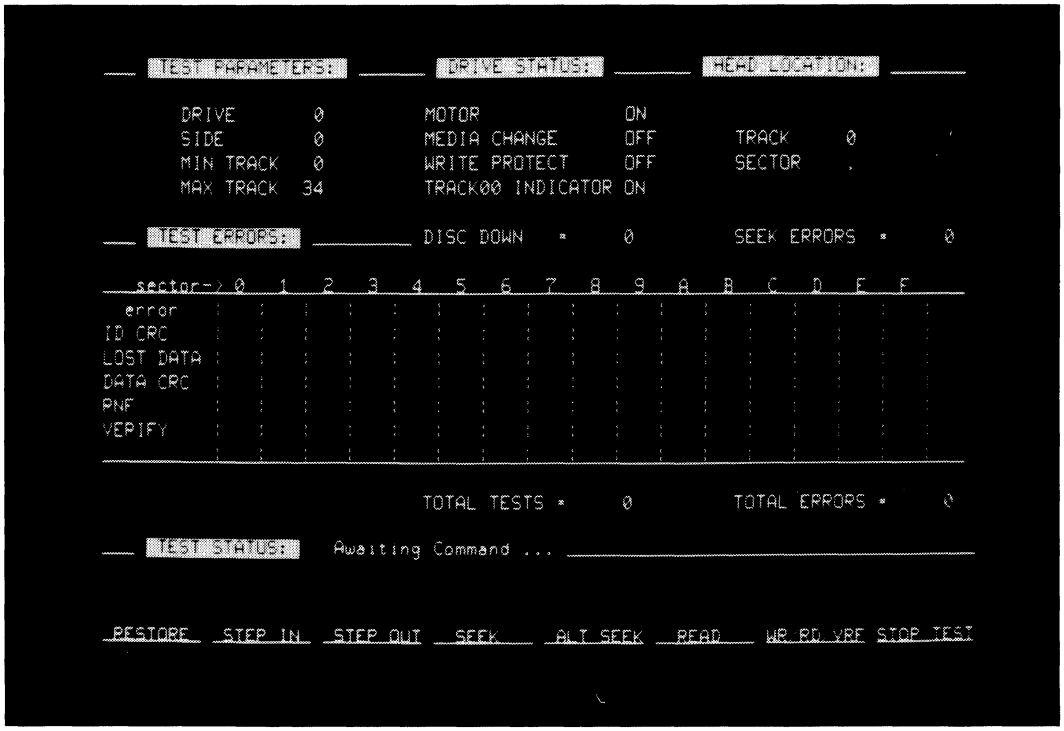


Figure 4-5. Floppy Test Menu Second Level

4-12. Perform all or part of the following tests to verify that the flexible disc drives are operating properly:

```
**********************************************************************
*                              NOTE                                  *
*  The Performance Verification should be                            *
*  performed prior to the Operation Verification                     *
*  procedures.When the DIAG mode is required use the sequence*
*  described in section IV (see par. 4-10) to access the             *
*  DIAG tests.                                                       *
**********************************************************************
```

4-13. MEDIA CHANGE TEST.

a. Go to DIAG mode and make sure media change indication occurs when media is removed and reset when other drive is selected.

4-14. MOTOR CONTROL TEST.

a. Remove both discs from drives and leave doors open.

b. Go to DIAG mode and observe that drive spindle only turns when motor indication for that drive is in the TEST mode.

4-15. DRIVE READY TEST.

a. When running the Operation Verification READ test, open the door of each drive and observe "...Disc Down..." failure for the drive being tested.

4-16. DRIVE SELECT TEST.

a. Go to DIAG mode and observe drive select LEDs to make sure that the corresponding LED is only on when drive is selected.

4-17. FORMAT A DISC. (check for index pulses at FDCC.)

a. Refer to disc format procedure given in Section III of this manual.

4-18. HEAD ALIGNMENT TEST.

```
**************************************************
*                                                *
*                    CAUTION                     *
*                                                *
*   All previous tests should have passed before *
*   executing this test to prevent possible      *
*   damage to the alignment disc.                *
*                                                *
**************************************************
```

4-19. This test requires performing Steps a through i of the Radial Head Alignment procedure and then the Head Azimuth Alignment Check. The Radial Head Alignmemt procedure is found in Section V (see par. 5-19).

```
**************************************************
*                                                *
*                    CAUTION                     *
*                                                *
*  The Radial Head Alignment is a difficult      *
*  procedure!  (Steps a through i of section     *
*  V (see par. 5-19) are a check only.           *
*                                                *
**************************************************
```

4-20. HEAD AZIMUTH ALIGNMENT CHECK.

4-21. The head azimuth is not field adjustable due to its very delicate nature. For this reason, the nearest HP Sales/Service office should be contacted to have this adjustment done. To determine whether the head azimuth is out of limits, perform the following procedures:

a. Use the procedure in section V (see par. 5-5) to set-up flexible disc drives as shown in section V (see fig. 5-1).

b. Call up the DIAG test on the mainframe.

c. Insert the alignment disc P/N 9164-0151 into drive and close the latch.

d. Select drive to be adjusted.

e. Connect and set-up scope as follows:

Trigger on Channel A (pos)
Display Channel B

	Channel A	Channel B
Sensitivity	N/Div	1V/Div
TIME/Div	1msec/Div	1msec/Div
Coupling	DC	AC
Connections	(Drive Electronics Board)	
Singals	TP7(INDEX)	TP4(READ DATA)
Gnd	TP6(GND)	TP10(GND)

f. Observe the waveform at TP4 should look similar to that of Figure 4-6. Examine the waveform for heads 1 and 2. If lobe A is greater in amplitude than lobe B or if lobe D is greater in amplitude than lobe C, then the head azimuth is out of alignment.

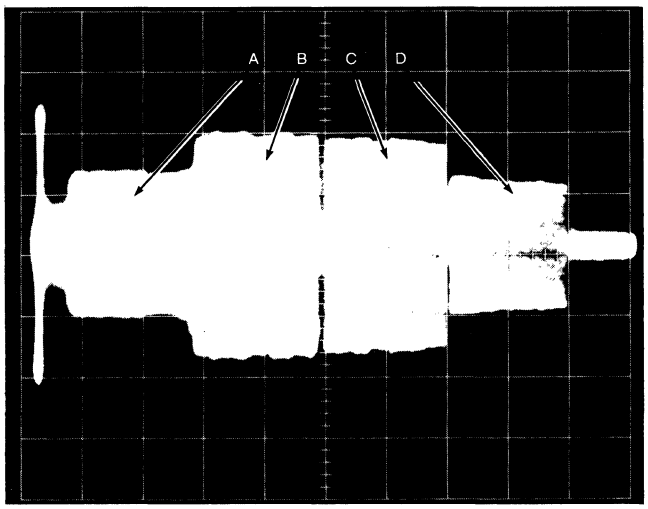


Figure 4-6. Head Azimuth Waveform

g. Check both heads by selecting one side, perform the check then select the other side. The side selection is made during test set-up from the mainframe.

4-22. SOFT ERROR RATE TEST.

a. Select drive and seek to track 34.

b. Go to DIAG and do a RD/WRT/VR test once.

c. Do READ test 30,518 times (approx. 3 hrs. 25 min.)

```
**********************************************
*                                            *
*                   NOTE                     *
*                                            *
*  After this test is executed the disc      *
*  used must be reformated before the        *
*  performance verification will pass.       *
*                                            *
**********************************************
```

d. Verify that there is not more than one error displayed.

SECTION V

ADJUSTMENTS

5-1. INTRODUCTION.

5-2. This section provides the adjustment procedures for the flexible disc drives. These procedures are recommended to return the drive to its original optimum performance after maintenance or repair. Included at the beginning of each procedure is a list of required tools. Table 1-2 in section I is a list of all the required tools. All these procedures assume the access to the service equipment listed in table 1-2 of this manual.

5-3. There are two catagories of adjustments given in this section. the first two are the spindle motor speed and spindle motor drive adjustments. These may be performed in the field. The second set of adjustments are; radial head alignment, track 0 switch adjustment, index emitter/detector adjustment, and the write protect switch adjustment. These adjustments should not be performed except in emergency situations due to their delicate nature. These adjustments are never to be performed at the customers location. If a non-field adjustment needs to be done, contact the nearest HP sales/service office. Locations and addresses are given at the back of this manual.

5-4. TEST AND ADJUSTMENT DRIVE ACCESS PROCEDURE.

5-5. The following procedure is a general set up procedure which allows access to the flexible disc drive for testing and adjustments:

a. Remove flexible disc drive from mainframe by following the procedures in section II (see par. 2-4) and place it along side the mainframe.

b. Supply power and control to the flexible disc drive by connecting the power and control extender cables between the RS-232/mini control board and the drive unit. Make sure that pin one on the control board is connected to pin one on the drive under test. The part number for the mini power extender cable is HP P/N 64110-61620, and the part number for the RS-232/mini control extender cable is HP P/N 64110-61621.

5-6. FIELD ADJUSTMENTS.

5-7. SPINDLE MOTOR SPEED ADJUSTMENT.

5-8. The spindle motor speed should be re-adjusted whenever a new spindle motor or servo electronics board is installed. Refer to section V (see fig. 5-1) while making this adjustment.

a. Required Tools:

1. Alignment tool or small insulated shank screwdriver.

2. HP 5314A or equivalent frequency counter (if primary power frequency is unknown or unstable or when adjusting motor speed under incandescent lighting).

5-9. KNOWN PRIMARY POWER AND FLUORESCENT LIGHTING.

5-10. Follow these instructions when primary power is a known 50 or 60 Hz and this adjustment is done under fluorescent lighting.

a. Check the spindle pulley to see that it has a strobe label P/N 7121-1451.

b. Enter the DIAG Test on the mainframe. Refer to section IV, operation verification tests.

c. Select the drive to be adjusted.

d. Press TEST and note the motor status light is ON indicating the drive motor is running.

e. Observe the strobe pattern on the spindle pulley. For 50Hz primary power observe inner pattern. For 60Hz, observe the outer pattern.

f. Locate and adjust the potentiometer on the servo board until the proper pattern on the strobe label stabilizes.

5-11. PRIMARY POWER FREQUENCY IS UNSTABLE OR UNKNOWN.

5-12. If the primary power frequency is unstable or unknown, follow these instructions:

a. Connect the frequency counter input to TP7 (index) and TP6 (ground) on the drive electronics board.

b. Enter the DIAG Test on the mainframe. Refer to section IV operation verification tests.

c. Select the drive to be adjusted.

d. Press TEST and note the motor status light is ON indicating the drive motor is running.

e. Locate and adjust the potentiometer on the servo board until a 200ms +/-1% period is observed on the counter display. This will assure a 300 RPM spindle speed. (see fig. 5-1)

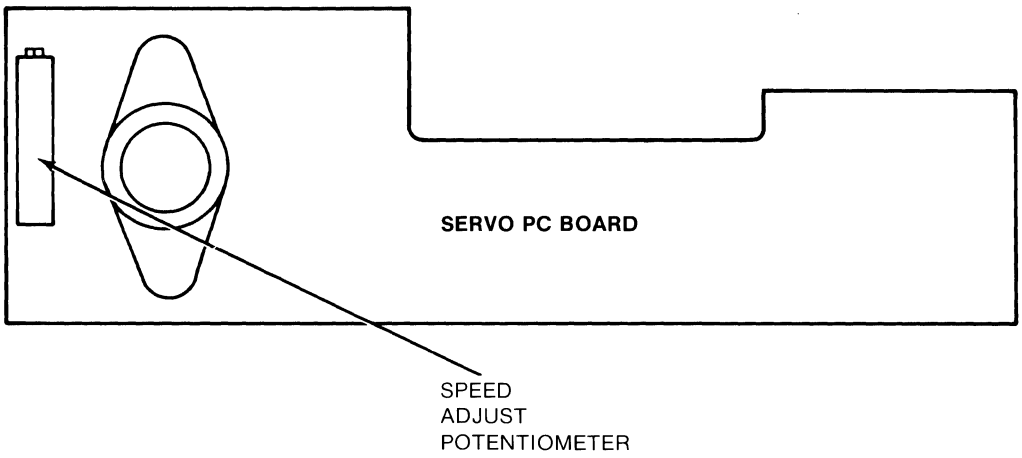


Figure 5-1. Spindle Motor Speed Adjustment

5-13. SPINDLE DRIVE BELT ADJUSTMENT.

5-14. This adjustment is to ensure proper drive belt tension. This adjustment should be made whenever the drive belt or drive spindle motor is replaced.

a. Required Tools:

1. #1 posidrive screwdriver
2. Spindle motor adjustment tool P/N 8710-1385

b. Refer to section V (see fig. 5-1) while performing these steps:

c. Place the drive assembly on its side so that the bottom of the drive faces you.

d. Remove the drive belt.

e. Place the spindle motor adjustment tool on the bottom of the drive as shown (see fig. 5-2) so that the small end of the adjustment tool rests against the motor pulley and the large end rests against the spindle pulley.

f. Slightly loosen the spindle motor retaining screws and move the motor until it rests firmly against the adjustment tool.

g. Re-tighten the spindle motor retaining screws and reinstall the drive belt.

```
**********************************************************
*                          NOTE                          *
*                                                        *
*  There is a good chance that the drive motor is        *
*  not exactly perpendicular to the drive casting        *
*  on which it is mounted.  This will cause the          *
*  drive belt to slip from the drive pulley when         *
*  it is rotated.  After a belt is installed,            *
*  rotate the drive spindle approximately 10             *
*  revolutions to insure the belt will not               *
*  slip from the drive pulley.                           *
**********************************************************
```

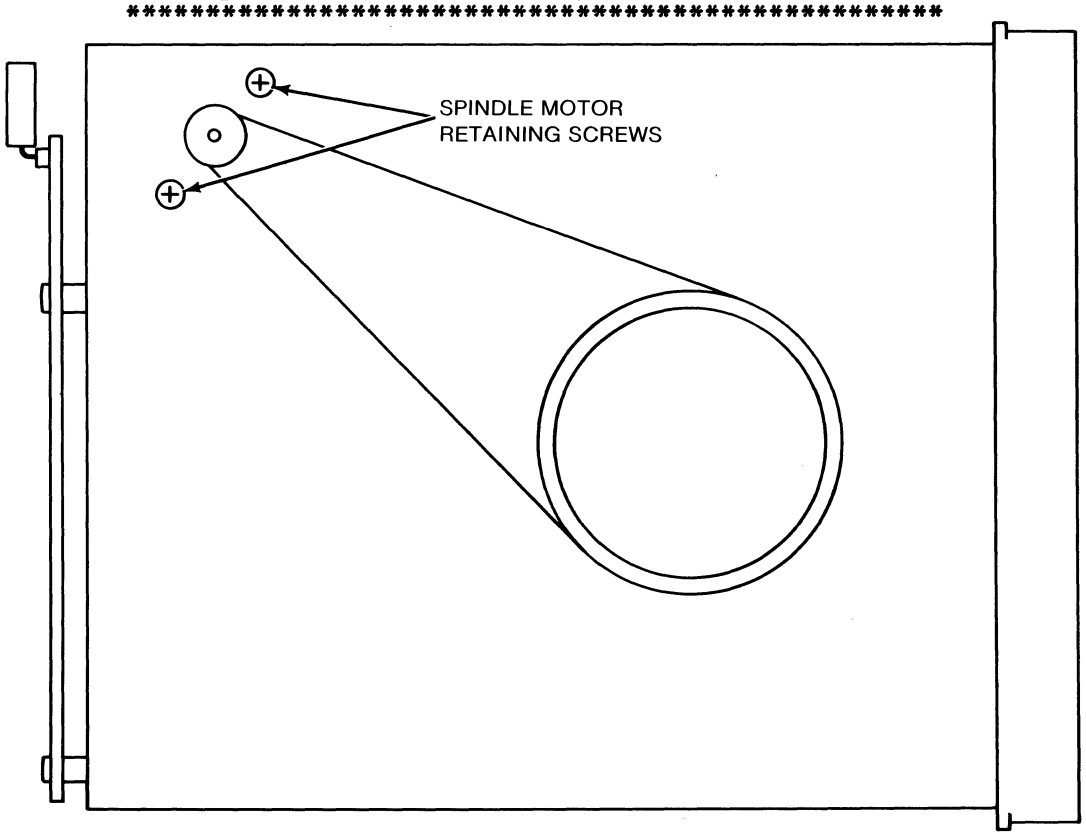


Figure 5-2. Spindle Drive Belt Adjustment

5-15. FACTORY ADJUSTMENTS.

5-16. The following adjustments should not be performed except in emergency situations due to their delicate nature. These adjustments are never to be performed at the customers location.

5-17. The adjustments described in this section are:

a. Radial Head Alignment
b. Track 0 Switch Adjustment
c. Index Emitter/Detector Adjustment
d. Write Protect Switch Adjustment

5-18. REQUIRED TOOLS AND TEST EQUIPMENT.

a.	Oscilloscope	HP 1740A or equilvalent
b.	Alignment Disc	P/N 9164-0151
c.	Torque Driver	P/N 8710-0670
d.	#1 Posidriv Screwdriver	P/N 8710-0899
e.	#2 Posidriv Screwdriver	P/N 8710-0900
f.	3/16 Thin Wall Nutdriver	P/N 8720-0001

5-19. RADIAL HEAD ALIGNMENT.

****
*
* NOTE
*
* Steps a through i serve as a
* radial head alignment check.
*
****

****
*
* NOTE
*
* If radial alignment steps j through l
* are performed track 0 adjustment will
* be required. The track 0 adjustment
* should only be done in an extreme
* emergency due to its delicate nature.
* Never should this procedure be done
* at customer location.
*
****

5-20. To properly align the read/write heads, perform to the following steps in the order shown. Refer to table 8-2, section VIII for head misalignment symptoms.

a. Set-up flexible disc drive . Use procedure in section V (see par. 5-5).

b. Enter the DIAG test on the mainframe. Refer to section IV operation verification tests.

c. Insert the alignment disc P/N 9164-0151 into the drive and close the latch.

d. Select drive to be tested and press TEST softkey.

e. Press RESTORE softkey.

f. Step to track 16

g. Connect and set-up the scope as follows:

TRIGGER Channel A (Pos)
Display Channel B

	Channel A	Channel B
Sensitivity	1V/Div	.1V/Div
TIME/Div	20msec	20msec
Coupling	DC	AC
Connection	(Drive Electronics Board)	
Signal	TP7(INDEX)	TP4(READ DATA)
Gnd	TP6(GND)	TP10(GND)

h. With the scope connected, the pattern shown in section V (see fig. 5-3) should be observed.

i. Both lobes of the pattern should be within 80% in amplitude of each other.

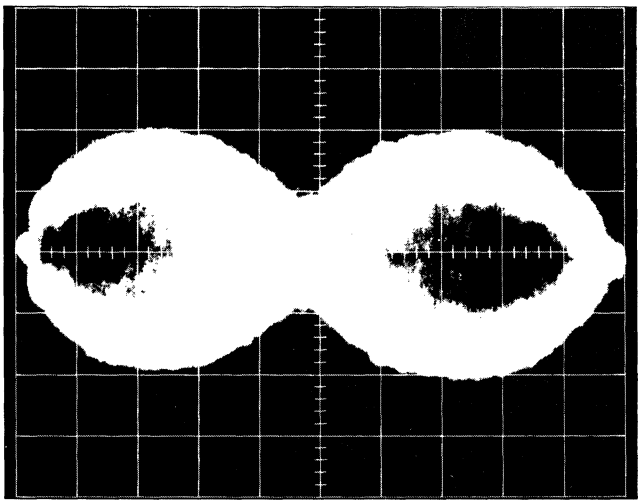


Figure 5-3. Radial Head Alignment Waveform

j. If the amplitude of one of the lobes of the waveform is less than 80% (.8 mils) of the other, slightly loosen the three screws shown in section V (see fig. 5-4) and adjust the radial head alignment by gently turning the head alignment cam screw.

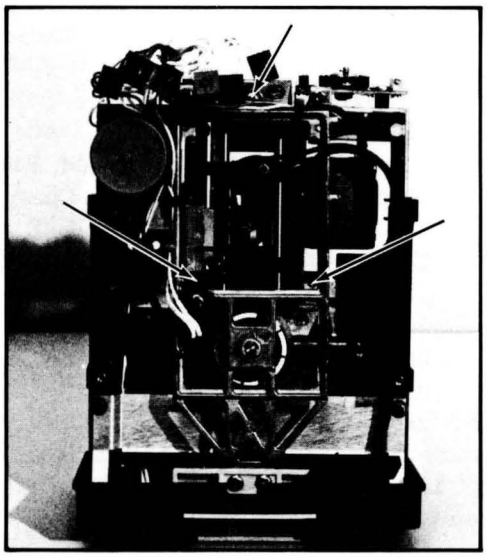


Figure 5-4. Head Assembly Retaining Screws

k. After the radial alignment has been completed, re-tighten the three screws loosened in step j while observing the scope pattern (see fig. 5-3). Tighten the retaining screws with the torque-driver set at 8 inch pounds.

l. Check the other side by selecting the other side in the test set-up.

5-21. TRACK 0 SWITCH ADJUSTMENT (extremely difficult adjustment).

5-22. Track 0 switch adjustment should be performed only in an extreme emergency due to its delicate nature. Never should this be performed at the customer's location. It should be performed whenever the radial head alignment is changed. To properly adjust the track 0 switch, follow these steps in the order shown:

a. Connect the equipment as in the procedure in section V (see par. 5-5).

b. Insert a formatted disc into the drive.

c. Go to DIAG mode (refer to section IV operation verification test) and set MIN TRACT to 0 and MAX TRACK to 4.

d. Press TEST then RESTORE and then ALT SEEK.

e. Connect and setup scope as follows:

TRIGGER	Channel A (pos)	
DISPLAY	Channel B	
	Channel A	Channel B
Sensitivity	1V/DIV	2V/DIV
Time/DIV	5mS/DIV	5mS/DIV
Coupling	DC	AC
Connections	(Drive Electronics Board)	
	Channel A	Channel B
Signal	TP12 (STEP)	U4F pin 1
GND	TP10 (GND)	TP6 (GND)

f. With the scope connnected and set-up, the waveform should be similar to that in section V (see fig. 5-5). The duration from T0 to T1 must be less than 18ms and the duration from T0 to T2 must be less than 24ms. If these times are within the limits, no adjustment is neccesary. If either of the time limits is exceeded, proceed with steps g thru l.

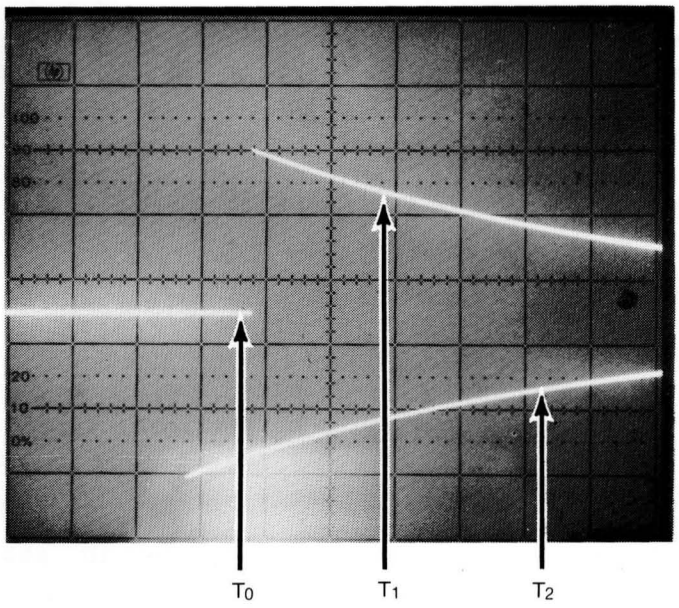


Figure 5-5. Track 0 Waveform

g. Remove connectors P5 and P6 from the front of the drive board.

h. Rest the drive board on a piece of insulating material such as cardboard.

i. Slightly loosen the track 0 switch retaining screw shown in section V (see fig. 5-6).

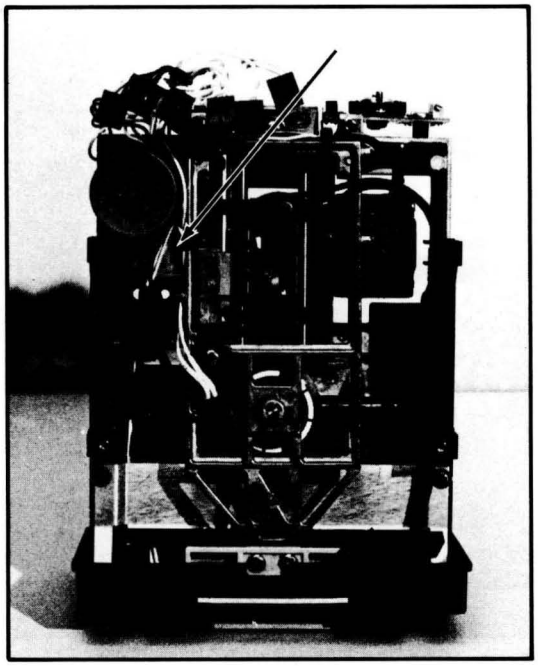


Figure 5-6. Track 0 Retaining Screw

j. Adjust the switch position until the time requirements in step f are met.

k. With the torque driver adjusted to 8 inch pounds, re-tighten the track 0 switch retaining screw while observing the oscilloscope pattern (see fig. 5-5).

l. Reinstall the drive board and connectors P5 and P6. Tighten the board retaining screws with the torque driver set to 8 inch pounds.

5-23. INDEX EMITTER/DETECTOR ADJUSTMENT.

5-24. This adjustment is required when the index emitter/detector assembly has been replaced. To do this adjustment use the following steps:

a. Connect the equipment as in the procedure in section V (see par. 5-5).

b. Place drive on its side as in section V (see fig. 5-7).

c. Go to DIAG mode. See section IV operation verification tests.

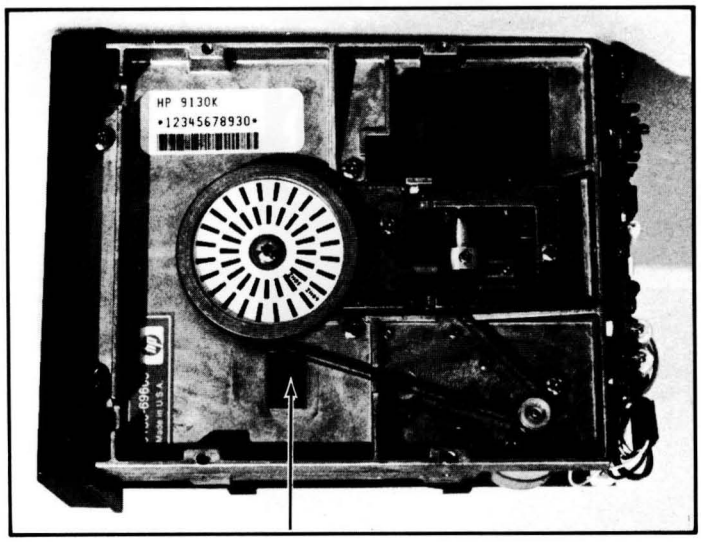


Figure 5-7. Index Detector Retaining Screw

d. Insert alignment disc into the disc and close the latch.

e. Select drive to be tested and press TEST soft key.

f. Press Restore, step to track 16, side 0 soft key.

g. Connect and setup the oscilloscope as follows:

Connect channel A to TP7/E7 (INDEX) and ground lead to TP6/E11.
Connect channel B to TP1/E1 (READ DATA) and ground TP10/E11.

Trigger:	Internal on channel A (POS)
Display:	Channel B
Volts/DIV:	.02V/DIV (using 10:1 probe)
Time/DIV:	.1ms/DIV

h. The oscilloscope presentation should look like the Index to Burst Waveform (see fig. 5-8).

i. Loosen the index detector retaining screw (see fig. 5-7) and move the detector until the INDEX to DATA burst time is approximately 400 us +/= 300 us for side 0.

j. Re-tighten the index detector retaining screw using the torque driver set to 8 inch pounds while observing the pattern on the scope (see fig. 5-8).

k. Check the INDEX and DATA time for head 1 by depressing and releasing the SELECT HEAD 1 push button switch on the DSU.

l. If the INDEX to DATA time is too far out, adjust the index emitter located on the top side of the drive assembly and then re-do steps i through k.

m. Tighten the index emitter and detector retaining screws using the torque driver set to 8 inch pounds.

n. Reassemble the drive assembly.

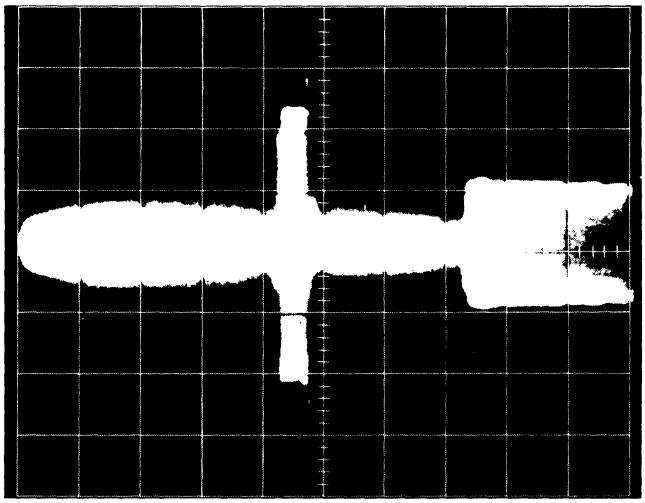


Figure 5-8. Index to Burst Waveform

5-25. WRITE PROTECT SWITCH ADJUSTMENT.

5-26. The disc drive head assembly may be severely damaged while performing this adjustment. For this reason, replacement or adjustment of this switch is not to be done in the field.

SECTION VI

REPLACEABLE PARTS

6-1. INTRODUCTION.

This section contains information for ordering parts. Table 6-1 lists abbreviations used in the parts list and throughtout the manual. Table 6-2 lists all replaceable parts in reference designator order. Table 6-3 contains the names and addresses that correspond to the manufacturer's five-digit code numbers.

6-2. ABBREVIATIONS.

Table 6-1 lists abbreviations used in the parts list, schematics, and throughout the manual. In some cases, two forms of the abbreviation are used: one; all in capital letters, and two; partial or no capitals. This occurs because the abbreviations in the parts list are always capitals. However, in the schematics and other parts of the manual, other abbreviation forms are used with both lowercase and uppercase letters.

6-3. REPLACEABLE PARTS LIST.

Table 6-2 is the list of replaceable parts and is organized as follows:

a. Chassis-mounted parts in alphanumerical order by reference designator.

b. Electrical assemblies and their components in alphanumerical order by reference designator.

c. Miscellaneous.

6-4. ORDERING INFORMATION.

To order a part listed in the replaceable parts table, quote the Hewlett-Packard part number and check digit, indicate the quantity required, and address the order to the nearest Hewlett-Packard sales/service office.

6-5. DIRECT MAIL ORDER SYSTEM.

Within the USA, Hewlett-Packard can supply parts through a direct mail order system. Advantages of using the system are as follows:

a. Direct ordering and shipment from the HP Parts Center in Mountain View, California.

b. No maximum or minimum on any mail order (there is a minimum order amount form ordered through a local HP sales/service office when the orders require billing and invoicing).

c. Prepaid transportation (there is a small handling charge for each order).

d. No invoices - to provide these advantages, a check or money order must accompany each order.

Mail-order forms and specific ordering information are available through your local HP sales/service office. Addresses and phone numbers are located at the back of this manual.

Table 6-1. Reference Designators and Abbreviations

REFERENCE DESIGNATORS

A	= assembly	**F**	= fuse	**MP**	= mechanical part	**U**	= integrated circuit
B	= motor	**FL**	= filter	**P**	= plug	**V**	= vacuum, tube, neon bulb, photocell, etc
BT	= battery	**IC**	= integrated circuit	**Q**	= transistor		
C	= capacitor	**J**	= jack	**R**	= resistor	**VR**	= voltage regulator
CP	= coupler	**K**	= relay	**RT**	= thermistor	**W**	= cable
CR	= diode	**L**	= inductor	**S**	= switch	**X**	= socket
DL	= delay line	**LS**	= loud speaker	**T**	= transformer	**Y**	= crystal
DS	= device signaling (lamp)	**M**	= meter	**TB**	= terminal board	**Z**	= tuned cavity network
E	= misc electronic part	**MK**	= microphone	**TP**	= test point		

ABBREVIATIONS

A	= amperes	**H**	= henries	**N/O**	= normally open	**RMO**	= rack mount only
AFC	= automatic frequency control	**HDW**	= hardware	**NOM**	= nominal	**RMS**	= root-mean square
AMPL	= amplifier	**HEX**	= hexagonal	**NPO**	= negative positive zero (zero temperature coefficient)	**RWV**	= reverse working voltage
		HG	= mercury				
BFO	= beat frequency oscillator	**HR**	= hour(s)				
BE CU	= beryllium copper	**HZ**	= hertz	**NPN**	= negative-positive-negative	**S-B**	= slow-blow
BH	= binder head					**SCR**	= screw
BP	= bandpass			**NRFR**	= not recommended for field replacement	**SE**	= selenium
BRS	= brass	**IF**	= intermediate freq			**SECT**	= section(s)
BWO	= backward wave oscillator	**IMPG**	= impregnated	**NSR**	= not separately replaceable	**SEMICON**	= semiconductor
		INCD	= incandescent			**SI**	= silicon
CCW	= counter-clockwise	**INCL**	= include(s)			**SIL**	= silver
CER	= ceramic	**INS**	= insulation(ed)	**OBD**	= order by description	**SL**	= slide
CMO	= cabinet mount only	**INT**	= internal	**OH**	= oval head	**SPG**	= spring
COEF	= coeficient			**OX**	= oxide	**SPL**	= special
COM	= common	**K**	= kilo=1000			**SST**	= stainless steel
COMP	= composition					**SR**	= split ring
COMPL	= complete	**LH**	= left hand	**P**	= peak	**STL**	= steel
CONN	= connector	**LIN**	= linear taper	**PC**	= printed circuit		
CP	= cadmium plate	**LK WASH**	= lock washer	**PF**	= picofarads= 10^{-12} farads	**TA**	= tantalum
CRT	= cathode-ray tube	**LOG**	= logarithmic taper			**TD**	= time delay
CW	= clockwise	**LPF**	= low pass filter	**PH BRZ**	= phosphor bronze	**TGL**	= toggle
				PHL	= phillips	**THD**	= thread
DEPC	= deposited carbon	**M**	= milli=10^{-3}	**PIV**	= peak inverse voltage	**TI**	= titanium
DR	= drive	**MEG**	= meg=10^{6}	**PNP**	= positive-negative-positive	**TOL**	= tolerance
		MET FLM	= metal film			**TRIM**	= trimmer
ELECT	= electrolytic	**MET OX**	= metallic oxide	**P/O**	= part of	**TWT**	= traveling wave tube
ENCAP	= encapsulated	**MFR**	= manufacturer	**POLY**	= polystyrene		
EXT	= external	**MHZ**	= mega hertz	**PORC**	= porcelain	**U**	= micro=10^{-6}
		MINAT	= miniature	**POS**	= position(s)		
F	= farads	**MOM**	= momentary	**POT**	= potentiometer	**VAR**	= variable
FH	= flat head	**MOS**	= metal oxide substrate	**PP**	= peak-to-peak	**VDCW**	= dc working volts
FIL H	= fillister head	**MTG**	= mounting	**PT**	= point		
FXD	= fixed	**MY**	= "mylar"	**PWV**	= peak working voltage	**W/**	= with
						W	= watts
G	= giga (10^{9})	**N**	= nano (10^{-9})	**RECT**	= rectifier	**WIV**	= working inverse voltage
GE	= germanium	**N/C**	= normally closed	**RF**	= radio frequency		
GL	= glass	**NE**	= neon	**RH**	= round head or right hand	**WW**	= wirewound
GRD	= ground(ed)	**NI PL**	= nickel plate			**W/O**	= without

Table 6-2. Replaceable Parts List

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A9	09130-69600	1	1	DISK DRIVE EXCHANGE(DOES NOT INCL. A9A2)	28480	09130-69600
A9MP1	4040-1915	8	1	DRIVE-FRONT PANEL	28480	4040-1915
A9MP2	0950-0448	5	1	BELT-DRIVE	28480	0950-0448
A9MP3	4040-1913	6	1	HP LATCH (BROWN)	28480	4040-1913
A9W1	64110-61607	4	1	CABLE-MINI (LEFT)	28480	64110-61607
A9W2	64110-61612	1	1	CABLE-MINI (POWER)	28480	64110-61612
A9A1	09130-66500	4	1	SERVO ELECTRONICS BOARD	28480	09130-66500
A9A2	09130-66501	5	1	DRIVE ELECTRONICS BOARD	28480	09130-66501
A9A3	09130-67920	4	1	MOTOR ASSEMBLY-SERVO	28480	09130-67920
A9A4	09130-67923	7	1	INDEX ASSEMBLY	28480	09130-67923
A9A5	09130-67917	9	1	SWITCH ASSEMBLY-TRACK (LEFT)	28480	09130-67917
A9A6	09130-61604	9	1	LED ASSEMBLY-FRONT PANEL	28480	09130-61604

NOTE

Subassemblies A9A1 through A9A6 are the same as A10A1 through A10A6. Refer to the A10 Listing for these parts and numbers.

* The part number given for the mini drive is an exchange assembly part number. It includes all parts listed for A9 or A10 except A9/A10A2, Drive Electronics Board.

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts List (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A10	09130-69600	1	1	DISK DRIVE EXCHANGE(DOES NOT INCL.A10A2)	28480	09130-69600
A10MP1	4040-1915	8	1	DRIVE (FRONT PANEL)	28480	4040-1915
A10MP2	0950-0448	5	1	BELT-DRIVE	28480	0950-0448
A10MP3	4040-1913	6	1	HP LATCH (BROWN)	28480	4040-1913
A10W1	64110-61606	3	1	CABLE-MINI (RIGHT)	28480	64110-61606
A10W2	64110-61612	1	1	CABLE-MINI (POWER)	28480	64110-61612
A10A1	09130-66500	4	1	SERVO ELECTRONICS BOARD	28480	09130-66500
A10A2	09130-66501	5	1	DRIVE ELECTRONICS BOARD	28480	09130-66501
A10A3	09130-67920	4	1	MOTOR ASSEMBLY-SERVO	28480	09130-67920
A10A4	09130-67923	7	1	INDEX ASSEMBLY	28480	09130-67923
A10A5	09130-67417	4	1	SWITCH ASSEMBLY-TRACK (RIGHT)	28480	09130-67417
A10A6	09130-61604	9	1	LED ASSEMBLY(FRONT PANEL)	28480	09130-61604

* The part number given for the mini drive is an exchange assembly part number. It includes all parts listed for A9 or A10 except A9/A10A2, Drive Electronics Board.

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts List (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A10A1	09130-66500	4		SERVO ELECTRONICS BOARD	28480	09130-66500
A10A1C1	0180-0058	0	2	CAPACITOR-FXD 50UF+75-10% 25VDC AL	56289	30D506G025CC2
A10A1C2	0180-0058	0		CAPACITOR-FXD 50UF+75-10% 25VDC AL	56289	30D506G025CC2
A10A1C3	0160-4557	0	1	CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A10A1C4	0180-0291	3	1	CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
A10A1C5	0160-5334	3	1	CAPACITOR-FXD .01UF 100VDC	28480	0160-5334
A10A1C6	0160-4833	5	1	CAPACITOR-FXD .022UF +-10% 100VDC CER	28480	0160-4833
A10A1H1	1205-0438	5	1	HEAT SINK SGL TO-66-CS	28480	1205-0438
A10A1H2	2420-0001	5	1	NUT-HEX-W/LKWR 6-32-THD .109-IN-THK	00000	ORDER BY DESCRIPTION
A10A1H3	2360-0454	4	2	SCREW-MACH 6-32 .5-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A10A1H4	2360-0454	4		SCREW-MACH 6-32 .5-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A10A1H5	2360-0121	2	1	SCREW-MACH 6-32 .5-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A10A1H6	2190-0060	7	1	WASHER-LK INTL T 1/4 IN .256-IN-ID	28480	2190-0060
A10A1H12	0380-0340	7	2	SPACER-RND .25-IN-LG .143-IN-ID	00000	ORDER BY DESCRIPTION
A10A1H13	0380-0340	7		SPACER-RND .25-IN-LG .143-IN-ID	00000	ORDER BY DESCRIPTION
A10A1J1	1251-4051	3	1	CONNECTOR 10-PIN M POST TYPE	28480	1251-4051
A10A1L1	9140-0607	0	1	INDUCTOR RF-CH-MLD 3.3UH 10% .2DX.45LG	28480	9140-0607
A10A1Q1	1854-0648	4	1	TRANSISTOR NPN 2N6300 SI DARL TO-66	04713	2N6300
A10A1Q2	1854-0215	1	1	TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A10A1R1	0683-2035	3	1	RESISTOR 20K 5% .25W FC TC=-400/+800	01121	CB2035
A10A1R2	0683-1055	5	1	RESISTOR 1M 5% .25W FC TC=-800/+900	01121	CB1055
A10A1R3	0757-0280	3	2	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A10A1R4	2100-3154	7	1	RESISTOR-TRMR 1K 10% C SIDE-ADJ 17-TRN	02111	43P102
A10A1R5	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A10A1R6	0757-0469	0	1	RESISTOR 150K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1503-F
A10A1R7	0683-4715	0	2	RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
A10A1R8	0683-1025	9	3	RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A10A1R9	0683-4715	0		RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
A10A1R10	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A10A1R11	0811-1668	9	1	RESISTOR 1.5 5% 2W PW TC=0+-400	75042	BWH2-1R5-J
A10A1R12	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A10A1R13	0683-1225	1	1	RESISTOR 1.2K 5% .25W FC TC=-400/+700	01121	CB1225
A10A1R14	0683-2225	3	1	RESISTOR 2.2K 5% .25W FC TC=-400/+700	01121	CB2225
A10A1U1	1826-0842	1	1	IC CONV FREQ/V 14-DIP-P PKG	27014	LM2917N

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts List (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A10A2	09130-66501	5		DRIVE ELECTRONICS BOARD	28480	09130-66501
A10A2C1	0180-0197	8	1	CAPACITOR-FXD 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
A10A2C2	0160-5205	7	3	CAPACITOR-FXD 470PF +-10% 200VDC CER	28480	0160-5205
A10A2C3	0160-5206	8	1	CAPACITOR-FXD 68PF +-10% 200VDC CER	28480	0160-5206
A10A2C4	0160-4441	1	4	CAPACITOR-FXD .47UF +-10% 50VDC CER	28480	0160-4441
A10A2C5	0160-4441	1		CAPACITOR-FXD .47UF +-10% 50VDC CER	28480	0160-4441
A10A2C6	0160-2055	9	16	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A10A2C7	0160-4441	1		CAPACITOR-FXD .47UF +-10% 50VDC CER	28480	0160-4441
A10A2C8	0160-4441	1		CAPACITOR-FXD .47UF +-10% 50VDC CER	28480	0160-4441
A10A2C9	0160-5219	3	1	CAPACITOR-FXD 4700PF 100VDC	28480	0160-5219
A10A2C10	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A10A2C11	0160-5208	0	1	CAPACITOR-FXD 270PF +-10% 200VDC CER	28480	0160-5208
A10A2C12	0160-5205	7		CAPACITOR-FXD 470PF +-10% 200VDC CER	28480	0160-5205
A10A2C13	0160-5205	7		CAPACITOR-FXD 470PF +-10% 200VDC CER	28480	0160-5205
A10A2C14	0160-5207	9	1	CAPACITOR-FXD 1200PF +-10% 100VDC CER	28480	0160-5207
A10A2C15	0160-4835	7	2	CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
A10A2C16	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
A10A2C17	0180-0100	3	8	CAPACITOR-FXD 4.7UF+-10% 35VDC TA	56289	150D475X9035B2
A10A2C18	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A10A2C19	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A10A2C20	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A10A2C21	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A10A2C22	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A10A2C23	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A10A2C25	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A10A2C26	0180-0100	3		CAPACITOR-FXD 4.7UF+-10% 35VDC TA	56289	150D475X9035B2
A10A2C27	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A10A2C28	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A10A2C29	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A10A2C30	0180-0100	3		CAPACITOR-FXD 4.7UF+-10% 35VDC TA	56289	150D475X9035B2
A10A2C32	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A10A2C33	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A10A2C34	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A10A2C35	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A10A2C36	0180-0100	3		CAPACITOR-FXD 4.7UF+-10% 35VDC TA	56289	150D475X9035B2
A10A2C37	0180-0100	3		CAPACITOR-FXD 4.7UF+-10% 35VDC TA	56289	150D475X9035B2
A10A2C38	0180-0100	3		CAPACITOR-FXD 4.7UF+-10% 35VDC TA	56289	150D475X9035B2
A10A2C39	0180-0100	3		CAPACITOR-FXD 4.7UF+-10% 35VDC TA	56289	150D475X9035B2
A10A2C40	0160-5209	1	2	CAPACITOR-FXD 330PF +-10% 200VDC CER	28480	0160-5209
A10A2C41	0160-5209	1		CAPACITOR-FXD 330PF +-10% 200VDC CER	28480	0160-5209
A10A2C42	0180-1746	5	1	CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
A10A2C43	0180-0100	3		CAPACITOR-FXD 4.7UF+-10% 35VDC TA	56289	150D475X9035B2
A10A2C44	0180-0374	3	1	CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
A10A2CR1	1901-0050	3	18	DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A10A2CR2	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A10A2CR3	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A10A2CR4	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A10A2CR5	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A10A2CR6	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A10A2CR7	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A10A2CR8	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A10A2CR9	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A10A2CR10	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A10A2CR11	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A10A2CR12	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A10A2CR13	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A10A2CR17	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A10A2CR18	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A10A2CR19	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A10A2CR20	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A10A2CR21	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A10A2CR23	1901-0704	4	1	DIODE-PWR RECT 1N4002 100V 1A DO-41	01295	1N4002
A10A2H1	0380-1331	8	2	SPACER	00000	ORDER BY DESCRIPTION
A10A2H2	4040-1854	4	1	SHIELD	28480	4040-1854
A10A2J2	1251-4617	7	1	CONNECTOR 4-PIN M UTILITY	28480	1251-4617
A10A2J3	1251-4051	3	1	CONNECTOR 10-PIN M POST TYPE	28480	1251-4051
A10A2J4	1251-5855	7	1	CONNECTOR 16-PIN M POST TYPE	28480	1251-5855
A10A2L1	9100-2283	8	2	INDUCTOR RF-CH-MLD 390UH 10% .105DX.26LG	28480	9100-2283
A10A2L2	9100-2283	8		INDUCTOR RF-CH-MLD 390UH 10% .105DX.26LG	28480	9100-2283
A10A2L3	9100-2281	6	1	INDUCTOR RF-CH-MLD 270UH 10% .105DX.26LG	28480	9100-2281
A10A2L4	9140-0118	8	1	INDUCTOR RF-CH-MLD 500UH 5% .2DX.45LG	28480	9140-0118

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts List (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A10A2Q1	1854-0215	1	6	TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A10A2Q2	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A10A2Q3	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A10A2Q5	1853-0036	2	4	TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
A10A2Q6	1853-0036	2		TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
A10A2Q7	1853-0036	2		TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
A10A2Q8	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A10A2Q9	1853-0036	2		TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
A10A2Q10	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A10A2Q11	1854-0215	1		TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A10A2R1	0757-0441	8	4	RESISTOR 8.25K 1% .125W F TC=0+-100	24546	C4-1/8-T0-8251-F
A10A2R2	0757-0441	8		RESISTOR 8.25K 1% .125W F TC=0+-100	24546	C4-1/8-T0-8251-F
A10A2R3	0757-0441	8		RESISTOR 8.25K 1% .125W F TC=0+-100	24546	C4-1/8-T0-8251-F
A10A2R4	0698-3159	5	2	RESISTOR 26.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2612-F
A10A2R5	0698-3159	5		RESISTOR 26.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2612-F
A10A2R6	0683-3625	9	1	RESISTOR 3.6K 5% .25W FC TC=-400/+700	01121	CB3625
A10A2R7	0683-1025	9	23	RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A10A2R8	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A10A2R9	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A10A2R10	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A10A2R11	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A10A2R12	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A10A2R13	0683-1825	7	1	RESISTOR 1.8K 5% .25W FC TC=-400/+700	01121	CB1825
A10A2R14	0683-1515	2	3	RESISTOR 150 5% .25W FC TC=-400/+600	01121	CB1515
A10A2R16	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A10A2R17	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A10A2R18	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A10A2R19	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A10A2R20	0683-7515	4	4	RESISTOR 750 5% .25W FC TC=-400/+600	01121	CB7515
A10A2R21	0683-3915	0	5	RESISTOR 390 5% .25W FC TC=-400/+600	01121	CB3915
A10A2R22	0683-1035	1	4	RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A10A2R23	0683-3915	0		RESISTOR 390 5% .25W FC TC=-400/+600	01121	CB3915
A10A2R24	0698-4438	5	1	RESISTOR 3.09K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3091-F
A10A2R25	0698-4462	5	2	RESISTOR 768 1% .125W F TC=0+-100	24546	C4-1/8-T0-768R-F
A10A2R26	0683-3925	2	1	RESISTOR 3.9K 5% .25W FC TC=-400/+700	01121	CB3925
A10A2R27	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A10A2R28	0683-4735	4	1	RESISTOR 47K 5% .25W FC TC=-400/+800	01121	CB4735
A10A2R29	0683-2225	3	2	RESISTOR 2.2K 5% .25W FC TC=-400/+700	01121	CB2225
A10A2R30	0683-2225	3		RESISTOR 2.2K 5% .25W FC TC=-400/+700	01121	CB2225
A10A2R31	0698-3495	2	1	RESISTOR 866 1% .125W F TC=0+-100	24546	C4-1/8-T0-866R-F
A10A2R34	0698-4425	0	1	RESISTOR 1.54K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1541-F
A10A2R35	0698-4462	5		RESISTOR 768 1% .125W F TC=0+-100	24546	C4-1/8-T0-768R-F
A10A2R36	0683-7515	4		RESISTOR 750 5% .25W FC TC=-400/+600	01121	CB7515
A10A2R37	0683-3915	0		RESISTOR 390 5% .25W FC TC=-400/+600	01121	CB3915
A10A2R38	0683-8225	5	2	RESISTOR 8.2K 5% .25W FC TC=-400/+700	01121	CB8225
A10A2R39	0683-3915	0		RESISTOR 390 5% .25W FC TC=-400/+600	01121	CB3915
A10A2R40	0683-7515	4		RESISTOR 750 5% .25W FC TC=-400/+600	01121	CB7515
A10A2R41	0683-8225	5		RESISTOR 8.2K 5% .25W FC TC=-400/+700	01121	CB8225
A10A2R42	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A10A2R43	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A10A2R44	0683-3025	3	1	RESISTOR 3K 5% .25W FC TC=-400/+700	01121	CB3025
A10A2R45	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A10A2R47	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A10A2R48	0683-3015	1	1	RESISTOR 300 5% .25W FC TC=-400/+600	01121	CB3015
A10A2R49	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A10A2R52	0683-1515	2		RESISTOR 150 5% .25W FC TC=-400/+600	01121	CB1515
A10A2R53	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A10A2R54	0757-0289	2	1	RESISTOR 13.3K 1% .125W F TC=0+-100	19701	MF4C1/8-T0-1332-F
A10A2R55	0698-3449	6	1	RESISTOR 28.7K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2872-F
A10A2R58	0698-3624	9	1	RESISTOR 150 5% 2W MO TC=0+-200	28480	0698-3624
A10A2R59	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A10A2R60	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A10A2R61	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A10A2R62	0683-1515	2		RESISTOR 150 5% .25W FC TC=-400/+600	01121	CB1515
A10A2R63	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A10A2R64	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A10A2R65	0683-7515	4		RESISTOR 750 5% .25W FC TC=-400/+600	01121	CB7515
A10A2R66	0683-3915	0		RESISTOR 390 5% .25W FC TC=-400/+600	01121	CB3915
A10A2R68	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A10A2R69	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A10A2R70	0757-0416	7	1	RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
A10A2R71	0698-3158	4	1	RESISTOR 23.7K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2372-F
A10A2R72	0757-0441	8		RESISTOR 8.25K 1% .125W F TC=0+-100	24546	C4-1/8-T0-8251-F
A10A2R73	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A10A2R74	0683-5125	8	1	RESISTOR 5.1K 5% .25W FC TC=-400/+700	01121	CB5125

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts List (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A10A2R75	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A10A2R76	0683-5105	4	1	RESISTOR 51 5% .25W FC TC=-400/+500	01121	CB5105
A10A2U1E	1251-4292	4	1	SHUNT BLOCK	28480	1251-4292
A10A2U1F	1820-0621	2	3	IC BFR TTL NAND QUAD 2-INP	01295	SN7438N
A10A2U2B	1820-0471	0	1	IC INV TTL HEX 1-INP	01295	SN7406N
A10A2U2C	1820-2520	4	1	IC DRVR TTL DUAL	01295	SN75463N
A10A2U2D	1826-0408	5	1	IC 8-DIP-P PKG	32293	ICL8212CPA
A10A2U2E	1820-1416	5	1	IC SCHMITT-TRIG TTL LS INV HEX 1-INP	01295	SN74LS14N
A10A2U2F	1810-0325	2	1	NETWORK-RES 16-DIP150.0 OHM X 8	01121	316B151
A10A2U3A	1826-0064	9	1	IC WIDEBAND AMPL VID 14-DIP-C PKG	04713	MC1733CL
A10A2U3B	1820-1204	9	2	IC GATE TTL LS NAND DUAL 4-INP	01295	SN74LS20N
A10A2U3C	1820-0621	2		IC BFR TTL NAND QUAD 2-INP	01295	SN7438N
A10A2U3D	1820-0174	0	1	IC INV TTL HEX	01295	SN7404N
A10A2U3E	1820-0668	7	1	IC BFR TTL NON-INV HEX 1-INP	01295	SN7407N
A10A2U4A	1826-0194	6	1	IC WIDEBAND AMPL VID 14-DIP-P PKG	18324	NE592A
A10A2U4B	1820-1204	9		IC GATE TTL LS NAND DUAL 4-INP	01295	SN74LS20N
A10A2U4C	1820-1112	8	2	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A10A2U4D	1820-2208	5	2	IC DRVR TTL DUAL	01295	SN75462P
A10A2U4E	1820-2208	5		IC DRVR TTL DUAL	01295	SN75462P
A10A2U4F	1820-0621	2		IC BFR TTL NAND QUAD 2-INP	01295	SN7438N
A10A2U5B	1826-0065	0	1	IC COMPARATOR PRCN 8-DIP-P PKG	50545	UPC311C
A10A2U5C	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A10A2U5D	1820-1211	8	1	IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS86N
A10A2U5E	1820-1260	7	1	IC MV TTL MONOSTBL DUAL	01295	SN74221N
A10A2XU1E	1200-0853	8	2	SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0853
A10A2XU2F	1200-0853	8		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0853

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts List (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A10A3	09130-67920	4		SERVO MOTOR ASSEMBLY	28480	09130-67920
A10A3B1	3140-0654	1	1	MOTOR-SPINDLE DRIVE	28480	3140-0654
A10A3H1	3050-1056	8	2	WASHER-SHOULDERED	51506	15250-050-065-N-1
A10A3H2	2360-0332	7	2	SCREW-MACH 6-32	28480	2360-0332
A10A3MP1	1401-0180	0	1	CAP-MOTOR END	28480	1401-0180
A10A3MP2	1600-1024	5	1	SHIELD-MOTOR	28480	1600-1024
A10A3P2	1251-4273	1	1	CONNECTOR-5-PIN FEMALE	28480	1251-4273

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts List (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A10A4	09130-67923	7		INDEX ASSEMBLY	28480	09130-67923
A10A4CR1	1990-0443	5	1	LED-INFRARED BVR=2V	28480	199C-0443
A10A4H1	2360-0331	6	1	SCREW-MACH 6-32	28480	2360-0331
A10A4H2	2360-0119	8	1	SCREW-MACH 6-32	00000	ORDER BY DESCRIPTION
A10A4H3	3050-0635	7	1	WASHER-FLAT	28480	3050-0635
A10A4MP1	4040-1852	2	1	HOLDER-EMITTER	28480	4040-1852
A10A4MP2	4040-1851	1	1	HOLDER-DETECTOR	28480	4040-1851
A10A4P10	1251-3965	6	1	CONNECTOR-4-PIN FEMALE	28480	1251-3965
A10A4Q1	1990-0792	7	1	TRANSISTOR-PHOTO	01295	TIL99

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts List (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A10A5	09130-67917	9		SWITCH ASSEMBLY-TRACK LEFT	28480	09130-67917
A10A5H1	2360-0331	6	1	SCREW-MACH 6-32 .25-IN-LG PAN-HD-POZI	28480	2360-0331
A10A5H2	2200-0149	6	2	SCREW-MACH 4-40 .625-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A10A5H3	3050-0222	8	2	WASHER-FL MTLC NO. 4 .125-IN-ID	28480	3050-0222
A10A5H4	1600-1059	6	2	SPRING-MODULE	28480	1600-1059
A10A5H5	2360-0370	3	2	SCREW-MACH 6-32 .375-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A10A5MP1	1600-1025	6	1	BRACKET-SWITCH	28480	1600-1025
A10A5MP2	0590-1312	0	1	NUT PLATE 4-40	00000	ORDER BY DESCRIPTION
A10A5MP3	4040-1847	5	1	HOLDER-SPRING	28480	4040-1847
A10A5P11	1251-3965	6	1	CONNECTOR-4-PIN FEMALE	28480	1251-3965
A10A5S2	3101-2438	1	2	SWITCH-TRACK (LEFT OR RIGHT)	28480	3101-2438

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts List (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A10A6	09130-61604	9		LED ASSEMBLY-FRONT PANEL	28480	09130-61604
A10A6CR3	1990-0794	9	1	DIODE-LED (RED)	71744	CM4-23
A10A6H14	1250-0610	0	1	BUSHING-COLLAR LED	28480	1250-0610
A10A6P9	1251-3965	6	1	CONNECTOR-4 PIN FEMALE	28480	1251-3965

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts List (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A11	64110-66509	5	2	MINI CONTROL AND RS232	28480	64110-66509
A11	64110-66509	5		BOARD ASSEMBLY-MINI/RS232	28480	64110-66509
A11C1	0160-2055	9	27	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A11C2	0180-0116	1	2	CAPACITOR-FXD 6.8UF+-10% 35VDC TA	56289	150D685X9035B2
A11C3	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A11C4	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A11C5	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A11C6	0180-0309	4	1	CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	150D475X0010A2
A11C7	0160-0298	8	2	CAPACITOR-FXD 1500PF +-10% 200VDC POLYE	28480	0160-0298
A11C8	0160-0300	3	1	CAPACITOR-FXD 2700PF +-10% 200VDC POLYE	28480	0160-0300
A11C9	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A11C10	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A11C11	0180-0116	1		CAPACITOR-FXD 6.8UF+-10% 35VDC TA	56289	150D685X9035B2
A11C12	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A11C13	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A11C14	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A11C15	0140-0226	0	2	CAPACITOR-FXD 320PF +-1% 300VDC MICA	72136	DM15F321F0300WV1C
A11C16	0160-0298	8		CAPACITOR-FXD 1500PF +-10% 200VDC POLYE	28480	0160-0298
A11C17	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A11C18	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A11C19	0160-2204	0	4	CAPACITOR-FXD 100PF +-5% 300VDC MICA	28480	0160-2204
A11C20	0160-2204	0		CAPACITOR-FXD 100PF +-5% 300VDC MICA	28480	0160-2204
A11C21	0180-0374	3	3	CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
A11C22	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
A11C23	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
A11C24	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A11C25	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A11C26	0140-0226	0		CAPACITOR-FXD 320PF +-1% 300VDC MICA	72136	DM15F321F0300WV1C
A11C27	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A11C28	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A11C29	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A11C30	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A11C31	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A11C32	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A11C33	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A11C34	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A11C35	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A11C36	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A11C37	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A11C38	0140-0207	7	3	CAPACITOR-FXD 330PF +-5% 500VDC MICA	72136	DM15F331J0500WV1CR
A11C39	0140-0207	7		CAPACITOR-FXD 330PF +-5% 500VDC MICA	72136	DM15F331J0500WV1CR
A11C40	0140-0207	7		CAPACITOR-FXD 330PF +-5% 500VDC MICA	72136	DM15F331J0500WV1CR
A11C41	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A11C42	0160-2204	0		CAPACITOR-FXD 100PF +-5% 300VDC MICA	28480	0160-2204
A11C43	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A11C44	0160-2204	0		CAPACITOR-FXD 100PF +-5% 300VDC MICA	28480	0160-2204
A11C45	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A11CR1	1901-0040	1	6	DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A11CR2	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A11CR3	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A11CR4	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A11CR5	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A11CR6	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A11E1	1258-0151	0	1	PROGRAM HEADER	28480	1258-0151
A11E2	1258-0183	8	1	PROGRAM HEADER	28480	1258-0183
A11E3	1258-0182	7	1	CONNECTOR-R & P 1 MALE PLUG	28480	1258-0182
A11H13	2200-0103	2	1	SCREW-MACH 4-40 .25-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A11J1	1251-5615	7	3	CONNECTOR 34-PIN M POST TYPE	28480	1251-5615
A11J2	1251-5615	7		CONNECTOR 34-PIN M POST TYPE	28480	1251-5615
A11J3	1251-5653	3	1	CONNECTOR 50-PIN M POST TYPE	28480	1251-5653
A11J4	1251-5615	7		CONNECTOR 34-PIN M POST TYPE	28480	1251-5615
A11J5	1251-7335	2	1	CONNECTOR	28480	1251-7335
A11MP1	64110-04701	9	1	SUPPORT-TOP BOARD	28480	64110-04701
A11MP2	64110-05001	4	2	CATCH	28480	64110-05001
A11Q1	1854-0215	1	1	TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	2N3904
A11R1	0757-0442	9	8	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A11R2	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A11R3	0757-0280	3	7	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A11R4	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A11R5	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts List (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A11R6	0757-1094	9	2	RESISTOR 1.47K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1471-F
A11R7	0757-0438	3	2	RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A11R8	0757-0273	4	2	RESISTOR 3.01K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3011-F
A11R9	0757-0273	4		RESISTOR 3.01K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3011-F
A11R10	0757-0455	4	2	RESISTOR 36.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3652-F
A11R11	0757-0455	4		RESISTOR 36.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3652-F
A11R12	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A11R13	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A11R14	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A11R15	0698-3154	0	4	RESISTOR 4.22K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4221-F
A11R16	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A11R17	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A11R18	0698-3154	0		RESISTOR 4.22K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4221-F
A11R19	0698-3154	0		RESISTOR 4.22K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4221-F
A11R20	0698-3156	2	1	RESISTOR 14.7K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1472-F
A11R21	0698-3150	6	1	RESISTOR 2.37K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2371-F
A11R22	0757-0429	2	2	RESISTOR 1.82K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1821-F
A11R23	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A11R24	0757-0429	2		RESISTOR 1.82K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1821-F
A11R25	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A11R26	0757-0461	2	2	RESISTOR 68.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-6812-F
A11R27	0757-0461	2		RESISTOR 68.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-6812-F
A11R28	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A11R29	0698-3154	0		RESISTOR 4.22K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4221-F
A11R30	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A11R31	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A11R32	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A11R33	0757-0443	0	3	RESISTOR 11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1102-F
A11R34	0757-0443	0		RESISTOR 11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1102-F
A11R35	0757-0443	0		RESISTOR 11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1102-F
A11R36	0757-0416	7	1	RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
A11R37	2100-3354	9	1	RESISTOR-TRMR 50K 10% C SIDE-ADJ 1-TRN	28480	2100-3354
A11R38	0757-1094	9		RESISTOR 1.47K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1471-F
A11TP1-18	0360-0535	0	18	TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A11U1	1820-1633	8	2	IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
A11U2	1820-2456	5	1	IC-FD1791A-01	28480	1820-2456
A11U3	1810-0280	8	3	NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
A11U4	1820-1425	6	1	IC SCHMITT-TRIG TTL LS NAND QUAD 2-INP	01295	SN74LS132N
A11U7	1820-1112	8	3	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A11U8	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A11U9	1820-0535	7	1	IC DRVR TTL AND DUAL 2-INP	01295	SN75451BP
A11U10	1826-0207	2	1	IC OP AMP WB 8-DIP-P PKG	01295	LM318P
A11U11	1820-1858	9	1	IC FF TTL LS D-TYPE OCTL	01295	SN74LS377N
A11U14	1820-1212	9	5	IC FF TTL LS J-K NEG-EDGE-TRIG	01295	SN74LS112AN
A11U15	1820-1244	7	1	IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS153N
A11U16	1820-1212	9		IC FF TTL LS J-K NEG-EDGE-TRIG	01295	SN74LS112AN
A11U17	1820-1212	9		IC FF TTL LS J-K NEG-EDGE-TRIG	01295	SN74LS112AN
A11U18	1820-1212	9		IC FF TTL LS J-K NEG-EDGE-TRIG	01295	SN74LS112AN
A11U19	1820-1633	8		IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
A11U20	1820-1197	9	3	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A11U21	1820-1989	7	2	IC CNTR TTL LS BIN DUAL 4-BIT	07263	74LS393PC
A11U22	1820-1144	6	1	IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
A11U23	1810-0271	7	1	NETWORK-RES 10-SIP200.0 OHM X 9	01121	210A201
A11U24	1820-1470	1	2	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS157N
A11U25	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A11U26	1820-1997	7	6	IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
A11U27	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
A11U28	1820-1730	6	2	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A11U29	1820-2024	3	3	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A11U30	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
A11U31	1820-1260	7	3	IC MV TTL MONOSTBL DUAL	01295	SN74221N
A11U32	1820-1428	9	2	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS158N
A11U33	1820-1989	7		IC CNTR TTL LS BIN DUAL 4-BIT	07263	74LS393PC
A11U34	1820-1433	6	1	IC SHF-RGTR TTL LS R-S SERIAL-IN PRL-OUT	01295	SN74LS164N
A11U35	1820-1260	7		IC MV TTL MONOSTBL DUAL	01295	SN74221N
A11U36	1820-1423	4	1	IC MV TTL LS MONOSTBL RETRIG DUAL	01295	SN74LS123N
A11U37	64110-10001	5	1	ROM-ASM CONTROL	28480	64110-10001
A11U38	1820-1917	1	3	IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
A11U39	1820-1212	9		IC FF TTL LS J-K NEG-EDGE-TRIG	01295	SN74LS112AN
A11U40	1820-1470	1		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS157N
A11U41	1820-1216	3	1	IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A11U42	1820-1917	1		IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
A11U43	1820-2723	9	1	IC RCVR TTL LS BUS DRVR OCTL	01295	SN7465620N
A11U44	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts List (Cont'd)

Reference Designation	HP Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
A11U45	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
A11U46	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A11U47	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A11U48	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
A11U49	64110-10002	6	1	ROM-ASM OUT DC	28480	64110-10002
A11U50	1820-1246	9	1	IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS09N
A11U51	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A11U52	1820-1428	9		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS158N
A11U53	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A11U54	1810-0280	8		NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
A11U55	3101-2371	1	1	SWITCH-SL 8-1A DIP-SLIDE-ASSY .1A 50VDC	28480	3101-2371
A11U56	1810-0280	8		NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
A11U57	1820-2289	2	1	IC UART NMOS	34649	C8251A
A11U58	1813-0131	4	1	IC GEN DUAL	34344	K1135A
A11U59	1810-0275	1	1	NETWORK-RES 10-SIP1.0K OHM X 9	01121	210A102
A11U60	3101-2372	2	1	SWITCH-SL 5-1A DIP-SLIDE-ASSY .1A 50VDC	28480	3101-2372
A11U61	1820-1917	1		IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
A11U62	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A11U63	1820-0509	5	1	IC DRVR DTL LINE DRVR QUAD	04713	MC1488L
A11U64	1820-0990	8	1	IC RCVR DTL NAND LINE QUAD	01295	SN75189AJ
A11U65	0490-0617	4	3	RELAY-REED 1C 250MA 28VDC 5VDC-COIL	28480	0490-0617
A11U66	0490-0617	4		RELAY-REED 1C 250MA 28VDC 5VDC-COIL	28480	0490-0617
A11U67	0490-0617	4		RELAY-REED 1C 250MA 28VDC 5VDC-COIL	28480	0490-0617
A11U68	1820-1260	7		IC MV TTL MONOSTBL DUAL	01295	SN74221N
A11W8	64110-61608	5	1	CABLE-RS232	28480	64110-61608
A11W10	64110-61612	1	1	CABLE-FLOP POWER	28480	64110-61612
A11W13	64110-61605	2	1	MINI + I/AR	28480	64110-61605
A11XE3	1251-1556	7	3	CONNECTOR-SGL CONT SKT .018-IN-BSC-SZ	28480	1251-1556
A11XU2	1200-0654	7	1	SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
A11XU5	1200-0638	7	3	SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A11XU6	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A11XU10	1200-0796	8	1	SOCKET-IC 8-CONT DIP DIP-SLDR	28480	1200-0796
A11XU12	1200-0639	8	12	SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A11XU13	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A11XU26	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A11XU27	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A11XU28	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A11XU30	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A11XU31	1200-0607	0	6	SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A11XU33	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A11XU35	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A11XU36	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A11XU37	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A11XU38	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A11XU44	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A11XU45	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A11XU46	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A11XU47	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A11XU48	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A11XU49	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A11XU57	1200-0567	1	1	SOCKET-IC 28-CONT DIP DIP-SLDR	28480	1200-0567
A11XU58	1200-0539	7	1	SOCKET-IC 18-CONT DIP DIP-SLDR	28480	1200-0539
A11XU68	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A11Y1	0410-1298	1	1	CRYSTAL-QUARTZ 4 MHZ HC-18/U-HLDR	28480	0410-1298
A11Z1	9164-0128	0	4	FLOPPY DISK	28480	9164-0128

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. List of Manufacturers' Code

Mfr No.	Manufacture Name	Address	Zip Code
S0545	NIPPON ELECTRIC CO	TOKYO JP	
00000	ANY SATISFACTORY SUPPLIER		
01121	ALLEN-BRADLEY CO	MILWAUKEE WI	53204
01295	TEXAS INSTR INC SEMICOND CMPNT DIV	DALLAS TX	75222
02111	SPECTROL ELECTRONICS CORP	CITY OF IND CA	91745
04713	MOTOROLA SEMICONDUCTOR PRODUCTS	PHOENIX AZ	85008
16299	CORNING GLASS WKS COMPONENT DIV	RALEIGH NC	27604
18324	SIGNETICS CORP	SUNNYVALE CA	94086
19701	MEPCO/ELECTRA CORP	MINERAL WELLS TX	76067
24546	CORNING GLASS WORKS (BRADFORD)	BRADFORD PA	16701
27014	NATIONAL SEMICONDUCTOR CORP	SANTA CLARA CA	95051
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO CA	94304
32293	INTERSIL INC	CUPERTINO CA	95014
51506	ACCURATE SCREW MACHINE CO	MONTVALE NJ	07645
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS MA	01247
71744	CHICAGO MINIATURE LAMP WORKS	CHICAGO IL	60640
72136	ELECTRO MOTIVE CORP	FLORENCE SC	06226
75042	TRW INC PHILADELPHIA DIV	PHILADELPHIA PA	19108

SECTION VII

MANUAL CHANGES

7-1. GENERAL.

7-2. This section normally contains information for backdating this manual for models with serial number prefixes prior to the one shown on the title page. Because this edition includes the information for the first serial number prefixes, there is no backdating material.

SECTION VIII

SERVICE

8-1. INTRODUCTION.

8-2. The service section provides the user with information necessary to service the flexible disc control and drives.

8-3. This section is divided into two groups. The first contains the fundamentals of flexible disc recording, and block and component level theory of operation. This information will enable the user to understand the operation of the floppy system in order to more effectively troubleshoot a problem. The second portion contains troubleshooting information. This includes descriptions of the error messages given during PV and DIAG tests, troubleshooting using signature analysis, troubleshooting hints, and detailed service sheets.

8-4. SAFETY CONSIDERATIONS.

8-5. Read the Safety Summary at the front of this manual before servicing this instrument. Review each procedure (before performing it) for cautions and warnings . For example, when working around the power supply and the display circuitry in the mainframe; caution should be taken to avoid the potentially lethal voltages. In general however, the flexible disc drives use only +-12 Volts and +5 Volts.

8-6. FLEXIBLE DISC RECORDING FUNDAMENTALS.

8-7. To better understand the operation of the flexible disc drive, read this description of disc recording principles. Refer to figures 8-1 through 8-3 while reading this section.

8-8. The flexible magnetic media used with the 64110A disc drive measures 5.25 inches in diameter. Both surfaces are coated with a ferromagnetic iron oxide. Both sides are used for data storage. Each side contains 35 circular tracks. Each track is divided into 16 pie slice shaped regions called sectors. A sector can contain up to 256 bytes of data. Surface, track and sector information is used to reference data location on the disc. Data is encoded on the disc (ones and zeros) by changing the orientation of small magnetic dipoles in the magnetic coating on the disc. There is no correlation between magnetic polarity of the dipoles and the ones and zeros. The ones and zeros are indicated by the location of the dipole polarity transitions.

8-9. The disc is soft sectored; that is, there is no physical features on the disc indicating of where each sector begins. In order to allow soft sectoring, each sector is divided into two fields. For each sector there is an ID field which contains information to identify the sector. Next there is a data field which contains the actual data. Thus, the ID field serves as a fixed marker for the beginning of each sector.

8-10. The makeup of the ID and DATA fields are similar. Both fields begin with a series of synchronization bytes (zeros). These bytes allow the decoder circuitry of the controller time to synchronize itself with the data on the disc. Following the synchronizing bytes, is the address mark byte which indicates that the beginning of an ID or DATA field has been located. The address mark is a specially recorded data pattern that does not occur in any data stream and is used to sychronize the data decoding circuits in the RS-232/Mini Disc Controller (MDC).

8-11. A series of information bytes follows the address mark. In an ID field, these bytes indicate the logical cylinder, head and sector address. In a DATA field, these bytes are the data being stored in the sector.

8-12. At the end of each field are two cyclic redundancy check (CRC) bytes. This check word (16 bits long) allows detection of most errors that occur in the data storage and recovery of information from a disc.

8-13. There are two gaps following each field on a track. The gaps allow for variations in disc rotational speed, index detector alignment variations and time for the hardware to prepare for the next field.

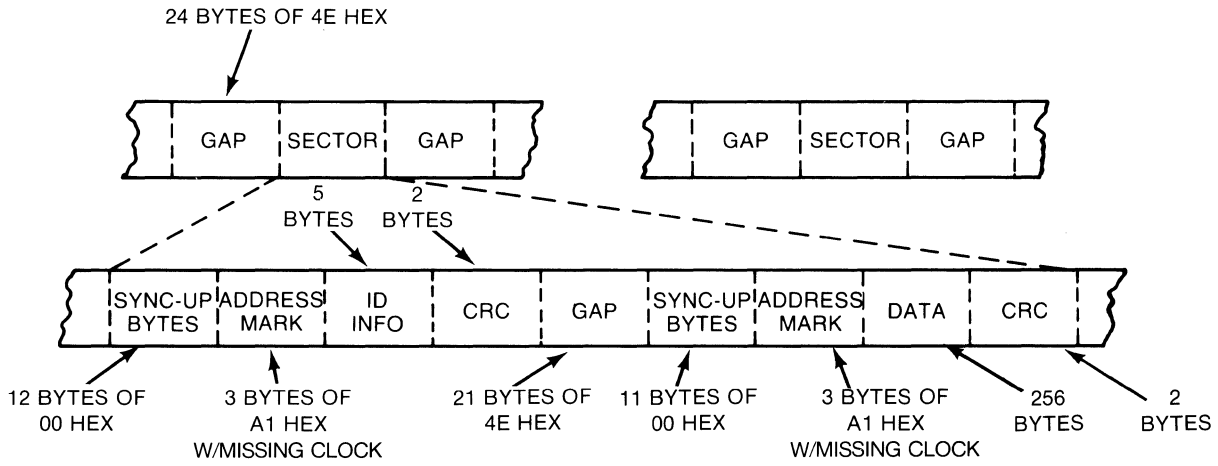


Figure 8-1. ID and Data Field Content

8-14. The logical sectors are numbered consecutively. However, the sectors (see figure 8-2) may occur in any physical order around the track. This allows the sectors to be staggered to optimize system performance (interleaving).

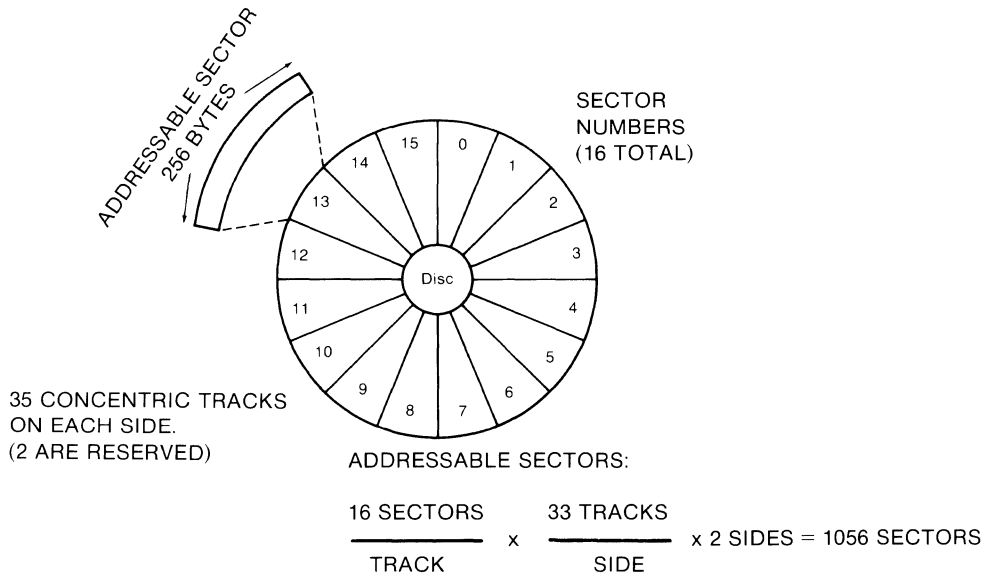


Figure 8-2. Media Sector and Track Structure

8-15. The outermost track on the disc is track 0 and the innermost track is 34. Each track has a physical address as described previously. There is also a logical track address associated with each good track. The logical track address is written in the ID field of each sector on the track. If a flexible disc has no bad tracks, the logical track has the same address as the physical track.

8-16. The recording head (see Figure 8-3) is moved in and out by a stepper motor assembly. Write current passes through the head coil to selectively magnetize portions of the disc. To read back data, the magnetized material is passed under the head, thereby inducing read-current into the head coil.

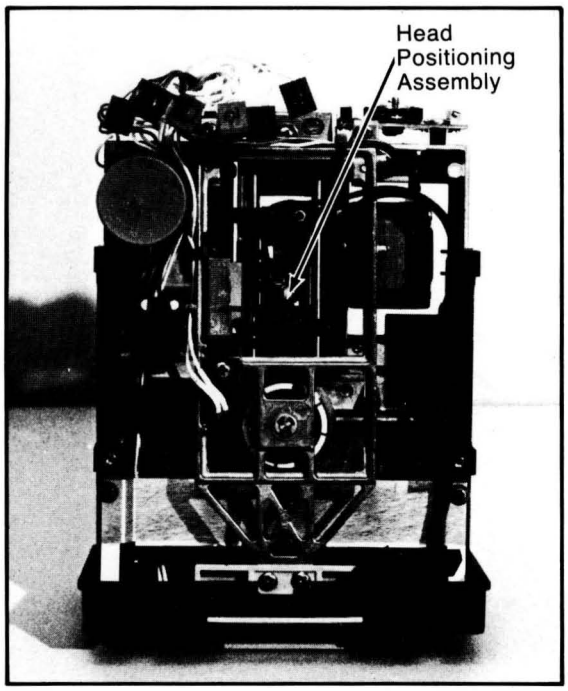


Figure 8-3. Head Positioning Assembly

8-17. FLOPPY BLOCK DIAGRAM THEORY.

8-18. The flexible disc drive is divided into two major functions; the first function is the RS-232/mini controller, and the second is the
flexible disc drives.

8-19. The block diagram for the RS-232/mini controller and flexible disc drive functions are shown on figure 8-4 and 8-5. The left half of the block diagram is the RS-232/mini control board A11 and the right half is showing the flexible disc drives (Drive 0 and 1) with drive 0 showing the internal functions. Mini Drive Block Diagram is a more detailed diagram (see fig. 8-5).

8-20. RS-232/MINI CONTROL BLOCK THEORY.

8-21. The RS-232/mini controller is part of the 64110A mainframe. It interfaces the flexible disc drives with the mainframe by supplying the drive with power, data, timing, and control signals.

8-22. The RS-232/mini controller is divided into eleven subfunctions.

a. Interface Control Latch

b. DMA/CPU Address Selector

c. SA Stimulus Latch

d. CPU Interface/DMA State Machine

e. Data Latches

f. 4MHz Oscillator

g. Mini Drive Controller

h. Drive Control Latches/Buffers

i. Drive Status Buffers

j. Data Separator

k. Disc Drive Multiplexer and Control Buffering

8-23. INTERFACE CONTROL LATCH.

8-24. Refer to figure 8-5. The control latch is responsible for capturing the upper byte of I/O data and providing this information to the DMA/CPU address selector.

8-25. DMA/CPU ADDRESS SELECTOR.

8-26. Refer to figure 8-5. The address selector, which is gated by the state machine, generates control signals to the mini drive control chip (MDC). The state of the control signals is determined by the output of the interface control latch.

8-27. SIGNATURE ANALYSIS STIMULUS LATCH.

8-28. Refer to figure 8-5. The output of the SA stimulus latch can be connected to either the input of the DMA state machine, jumper E2, or to the inputs of the data separator circuitry, jumper E1. This is provided for the user as an effective way of troubleshooting the DMA state machine and data separator by forcing them into known state sequences.

8-29. CPU INTERFACE/DMA STATE MACHINE.

8-30. Refer to figure 8-5. The CPU Interface/DMA State Machine performs two functions. First, a major portion of the circuitry does byte packing and unpacking so that the 16 bit I/O bus can interface to the 8 bit bus of the MDC in an effective way. Second, the state machine provides signals for enabling the data latches and providing next state information for itself.

8-31. DATA LATCHES.

8-32. Refer to figure 8-5. The data latches are used for loading and transfering 8 bit read/write, status and control signals to and from the drive circuitry from the 16 bit 64110A I/O bus. The enabling and clocking of the data latches is performed by the DMA state machine.

8-33. 4MHz OSCILLATOR.

8-34. Refer to figure 8-4. The oscillator block is comprised of a 4MHz crystal oscillator that is used to clock a 4 bit binary counter. The 2MHz and 500KHz outputs are used to clock the data separator and the 1MHz output is used to clock the mini drive controller chip.

8-35. MINI DRIVE CONTROLLER (MDC) CHIP.

8-36. Refer to figure 8-4. The mini drive controller (MDC) chip is divided into two functions. The first is the microprocessor interface that uses control signals to determine whether it is in a read or a write mode. Then, once it has determined its R/W status it will then read or write data via the data access lines to the data latches. The second section, the disc interface, implements the commands from the microprocessor interface section. The disc interface section processes commands and status signals from the disc drive MUX. Also, the MDC will provide encoded information to be written onto the disc and a means of decoding read data to be output to the system.

8-37. DRIVE CONTROL LATCH/BUFFER.

8-38. Refer to figure 8-4. This block is responsible for providing control signals to each disc drive.

8-39. DRIVE STATUS BUFFERS.

8-40. Refer to figure 8-4. The drive status buffers provide the system with information necessary to determine the status of the disc drives.

8-41. DATA SEPARATOR.

8-42. Refer to figure 8-4. This block is responsible for dividing the 1's and 0's on the data stream into half bit cells, and phase locking this data for use by the MDC. The data stream consists of raw encoded information from the disc. Furthermore, the raw read-information is delayed and phase locked with a read clock as soon as seven sync bytes have been read from the disc.

8-43. DISC DRIVE MULTIPLEXER AND CONTROL BUFFERING.

8-44. Refer to figure 8-4. This block is the final interface to the disc drives. The multiplexer selects between the two sets of signals going to/from the two flexible disc drives depending on which drive is currently active.

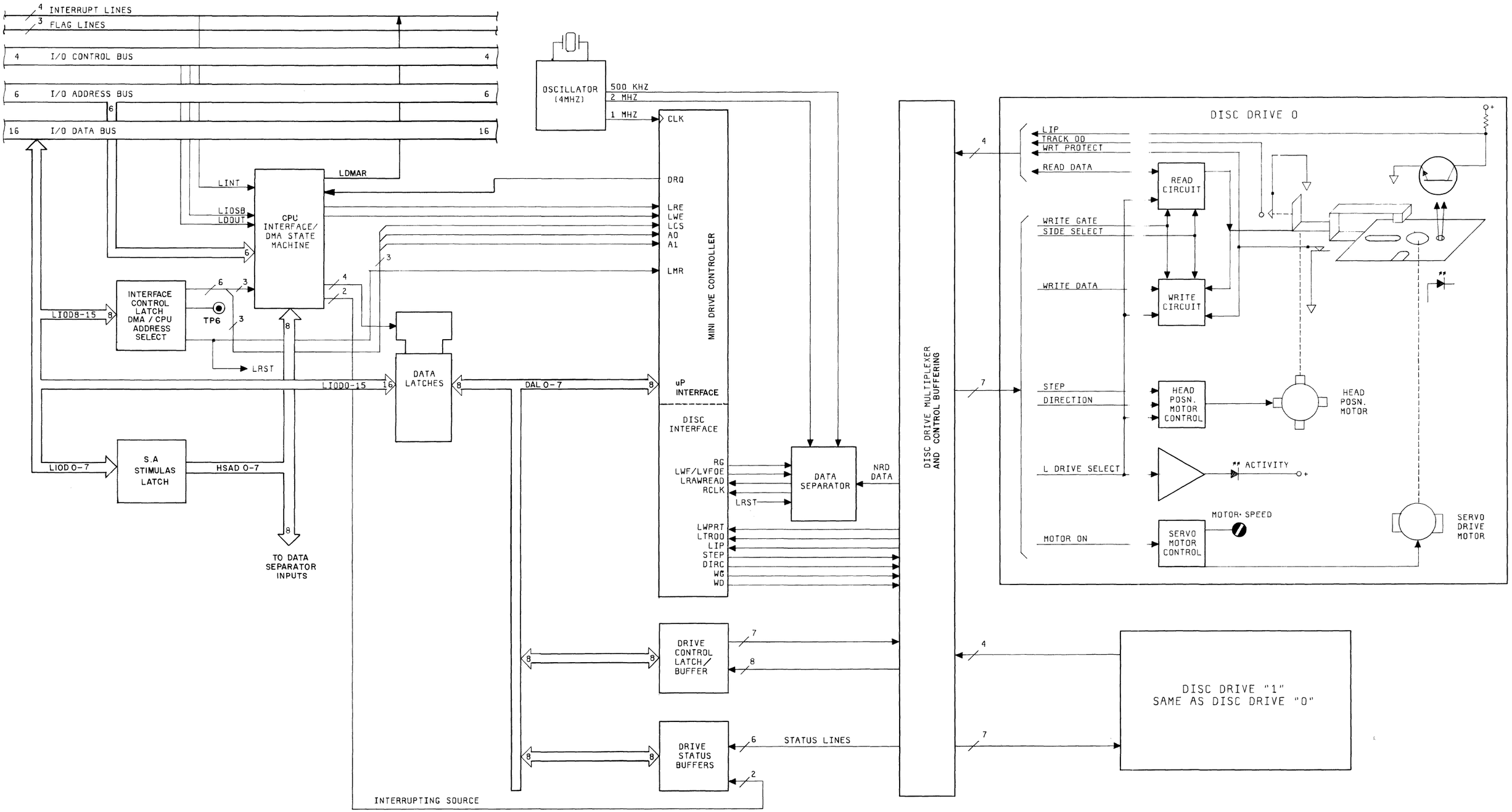


Figure 8-4.
Mini Control Block Diagram
8-7 AP

8-45. FLEXIBLE DISC DRIVE BLOCK THEORY.

8-46. This section describes the block digram theory for the disc drives. Figure 8-5 is a detailed block diagram of the disc drives and should be used with this section.

8-47. INDEX PULSE SHAPING NETWORK.

8-48. The index pulse circuitry consists of an index LED, photo transistor and pulse shaping network. The index hole in the flexible disc passes between the index LED and photo transistor, causing the photo transistor to conduct. The detected signal is then shaped and buffered and output on the Index Pulse interface line (J1-8). This signal, although inverted, may be observed at TP7 on the drive electronics board.

8-49. WRITE PROTECT SENSOR.

8-50. The write protect sensor consists of a switch which is opened when a write protected disc is inserted into the drive. This signal is delayed by an RF filter to eliminate transient noise from the switch. This will cause the write protect line (J1-28) to go low and TP9 to go high.

8-51. TRACK 0 SWITCH.

8-52. The level on the track 0 interface is a function of the head assembly position. When the head assembly is positioned at track 0 and the stepper motor indicates phase 0, J4-19 is pulled low, causing TP8 and the track 0 interface line to be pulled low.

8-53. SPINDLE MOTOR DRIVE CONTROL.

8-54. The spindle drive system consists of a spindle assembly driven by a DC motor-tachometer combination and the servo electronics board.

8-55. The servo electronics includes a current limiter and interface control line.

8-56. When the Drive Motor Enable line is low, the drive motor is allowed to come up to speed. This speed is adjustable by potentiometer R4 located on the servo electronics board.

8-57. A current sensing resistor, also located on the servo electronics board limits the motor current to 900mA. If this limit is exceeded, the motor is disabled.

8-58. HEAD POSITION CONTROL.

8-59. The head position control conists of a four phase stepper motor drive which changes one phase for each track advancement of the head assembly. In addition to the logic for motion control, a gate is provided to inhibit repositioning during a write operation.

8-60. POWER-ON CIRCUIT.

8-61. This circuit detects when the +5VDC and +12VDC are valid and prevents writing/reading/erasing/stepping until such time.

8-62. DATA CIRCUITRY.

8-63. All signals required to control the data circuitry are provided by the host system and are shown in the functional block diagram of Figure 8-5. These signals are as follows:

a. Drive Select
b. Write Enable
c. Write Data
d. Side Select

8-64. There are 4 drive select lines connected to the data electronics. A shunt block determines the drive number. The drive number is established by clipping three of the jumpers on the shunt block or adding a shunt to an empty block. When the selected drive select line is pulled low, the data circuitry is enabled and the drive is conditioned to respond to step or read/write commands. On the 64110A all of the jumpers are intact and the drive is enabled with DS0.

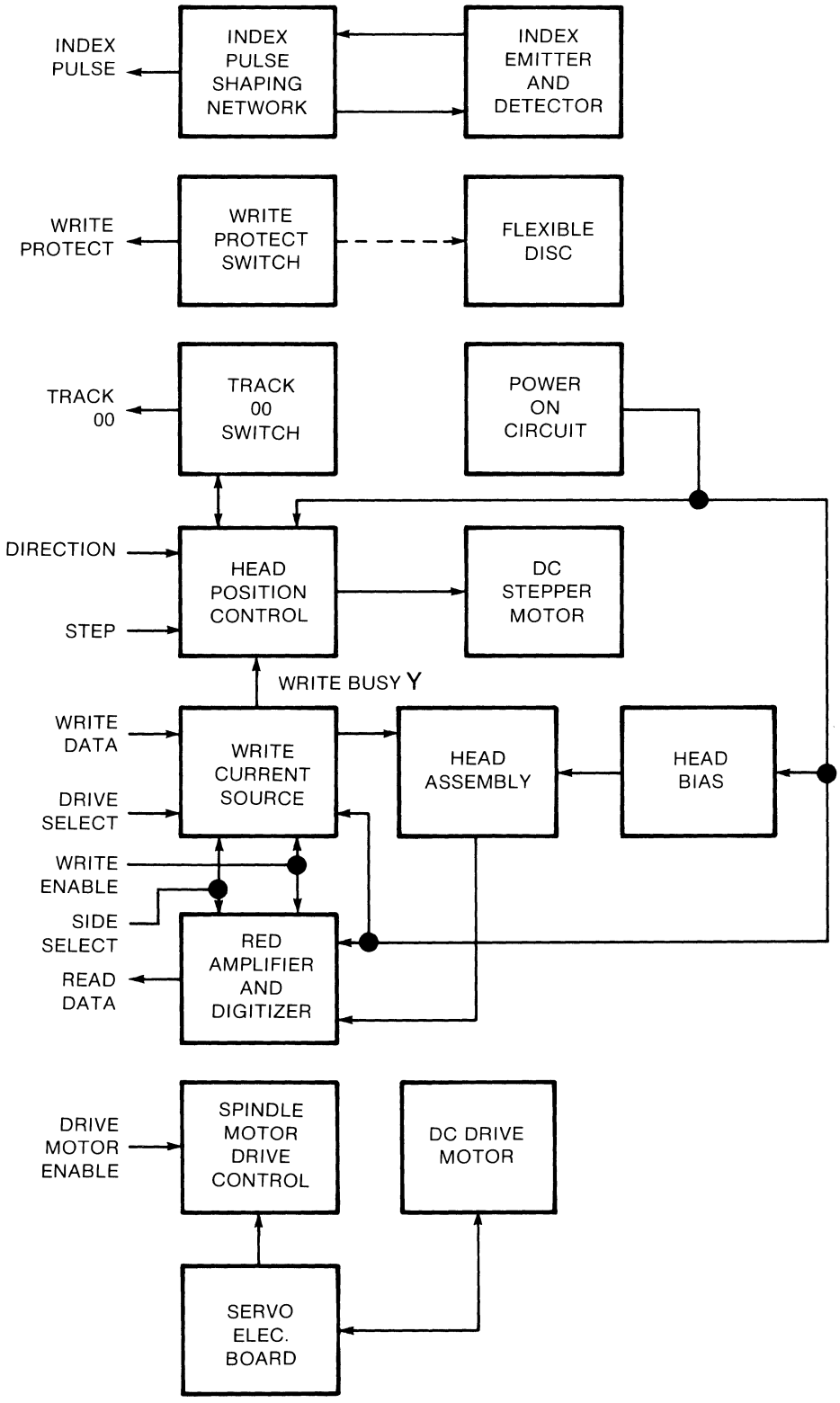


Figure 8-5. Mini Drive Block Diagram

8-65. WRITING DATA.

8-66. The write electronics consists of the following circuits:

a. Write/erase current source
b. Waveform generator
c. Trim erase current source
d. Head select logic
e. Bias Source

8-67. The read/write winding on the head is center tapped. During a write operation, the current from the write-current source flows in the alternate halves of the winding under the control of the write waveform generator.

8-68. Before recording can begin, certain conditions must be satisfied . The conditions required before writing (i.e., unit ready) must be established by the host system as follows:

a. Drive speed stabilization. This will exist 250ms after starting the drive motor.

b. Subsequent to any step operation, the positioner must be allowed to settle. This requires 20ms total after the last step pulse is initiated, i.e., 5ms for the step motion and 15ms for settling.

8-69. The following operations are performed when writing data. These operations may be overlapped if required.

8-70. Figure 8-6 shows the relevent timing diagram for a write operation. At T=0 when the unit is ready, the write enable line goes low. This enables the write-current source and bias circuitry.

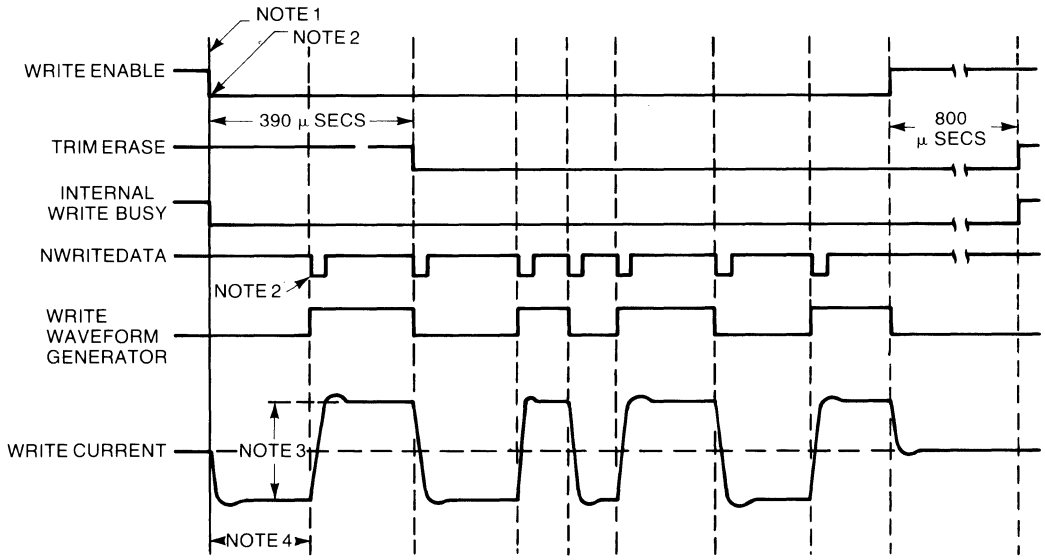
8-71. Since the trim erase gaps are behind the read/write gap, the TRIM ERASE control goes true 390us after the WRITE ENABLE interface line. It should be noted that this value is optimized between the requirements at track 0 and track 34 so that the effect of the trim erase gaps on previous information is minimized.

8-72. Figure 8-6 shows the information on the WRITE DATA interface line, and the output of the write waveform generator which toggles on the leading edge of every WRITE DATA pulse.

8-73. At the end of recording, at least one additional pulse on the WRITE DATA line must be inserted after the last significant WRITE DATA pulse to avoid excessive peak shift effects.

8-74. The TRIM ERASE signal must remain true for 800us after the termination of WRITE ENABLE to ensure that all recorded data are trim erased. This value is again optimized between the requirements at track 0 and 34.

8-75. The duration of a write operation is from the true going edge of WRITE ENABLE to the false going edge of TRIM ERASE. This is indicated by the internal WRITE BUSY waveform shown.



NOTES:
1. 1 = 0 = 250 Milliseconds after drive motor starts or 20 milliseconds after last step pulse, (whichever is the latest time)
2. Unsynchronized
3. 8.5 ma peak to peak
4. 4 μ seconds minimun, 8 μ seconds maximum

Figure 8-6. Write Timing Diagram

8-76. READING DATA.

8-77. The read-electronics consists of the following circuitry:

a. Read switch/side select
b. Read amplifier
c. Filter
d. Differentiator
e. 0 Crossing detector

8-78. The read-switch is used to isolate the read-amplifier from the voltage excursion across the magnetic head during a write operation. The side select is used to enable one of the read/write/erase heads.

8-79. Before reading can begin, the drive must be in a ready condition. As with the data recording operation, this ready condition must be established for data recording. A 100us delay must exist from the trailing edge of the TRIM ERASE signal to allow the read-amplifier to settle after the transient caused by the read-switch returning to the read mode.

8-80. Referring to figure 8-7, the output signal from the read/write head is amplified by a read-amplifier and filtered to remove noise by a linear phase filter. The linear output from the filter is passed to the differentiator which generates a waveform whose zero crossovers

correspond to the peaks of the read signal. This signal is then fed to the comparator and digitizer circuit.

8-81. The comparator and digitizer circuitry generates a 1us READ DATA pulse corresponding to each peak of the read signal. This composite read-data-signal is then sent to the host system via the READ DATA interface line.

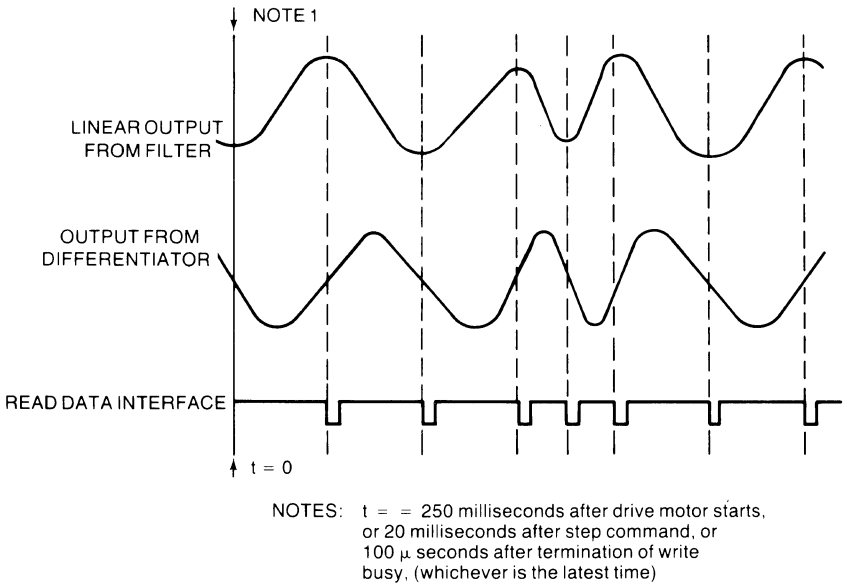


Figure 8-7. Read Timing Diagram

8-82. RS-232/MINI CONTROL THEORY OF OPERATION.

8-83. MINI CONTROL. (See service sheets 11A,B figures 8-10 and 8-13)

8-84. The CPU may execute I/O to any 1 of 16 peripheral addresses (defined by LPA 0-3) and to any one of four registers at each address. The state of the CPU registers are defined by the state of LIC1 and LIC2:

LIC2	LIC1	Register	Function
H	H	R4	All DMA except last byte
H	L	R5	Command
L	H	R6	Last byte of DMA
L	L	R7	SA test

8-85. Address and register information is guaranteed valid while LIOSB is low or, in other words, LIOSB is the I/O bus clock. U41 causes LMYPA to go low whenever peripheral address 4 is addressed. If the access is a write to R5 (a command) the data is clocked into U8 and U28 (PCMD) via U52. A write to R7 (used only for SA testing) enables U11. Through U52, a write to any register other than R7 (DMA or command) enables U27 and U45. Whereas, a read from R4 or R6 (DMA) reads data from U26 and U44 (LRD).

8-86. U8B enables DMA upon command through R5 (PCMD). HDMAEN allows U7B to be set on the rising edge of HDMARQ from the state machine output U48. This generates a DMA request through U7B and U50C. An access through R6 (LR6), the last byte of DMA, clears the enable. This in turn, generates an interrupt (LIR3) through U14C, U29B, U51A,B and U50A indicating the end of a DMA cycle.

8-87. U30, U37, U49 and U48 comprise the controller state machine. U30 and U48, used to synchronize the state machine, are clocked by the normal and inverted outputs of a 2 MHz clock which runs asynchronously to the CPU clock. U37 and U49 are ROMs. The purpose of the state machine is to interface between the CPU's 16 bit I/O bus and control bus, to U2's 8 bit bus. The state machine provides packing and and unpacking of words into bytes when required (during DMA), and passing single bytes through without waiting for a second byte during commands.

8-88. U46 and U47 form a data control register. One example of this registers operation is as follows: During a read operation the RS-232/mini disc controller U2 is reading data from disc 0 and needs to write to disc 1 after its read routine is executed. First, the disc 0 drive operating conditions will be captured by the control latch U46. Then, the MDC will execute a read on disc 0. After the read is done the control latch is loaded with the operating conditions for disc 1 via the data latches. Then, the MDC will execute a write on disc 1. The drive control buffer U47 is used for determining drive status and to provide a return path for SA stimulus.

8-89. U28, U29 and U8 form a drive status register that informs the system if the drives are operating, media has changed, write protected, requesting DMA, or the MDC U2 has generated an interrupt.

8-90. U40 the DMA/CPU address selector is used to generate control signals for the internal data register of the mini disc controller U2.

8-91. U36 is used to detect that there is media in the drives and that the motor is turning. Index pulses will occur every 200 ms, which will keep the monostables retriggered. U25 detects a media change by monitoring the write protect switch.

8-92. U19, U24 and U1 are the final interface to the disc drives. Control and data signals are sent to U19 and U1 from U2 and control latch, U46. Status information from the drives is multiplexed by U24. The reason for multiplexing this information is that the mini drive controller is designed for single drive operation.

8-93. The control board clock generation is done by the circuitry surrounding Y1, a 4 MHz crystal oscillator. R22, R23 and R24 bias U20C,D so the chip will operate in the linear region if the crystal is not oscillating. The crystal oscillates in the series-resonant mode.

8-94. MINI CONTROL DATA SEPARATOR. (See service sheet 11C figure 8-13)

8-95. Due to the encoding scheme used, data from the disc drive consists of a train of pulses whose pulse-to-pulse spacing may be 4us, 6us or 8us. In practice, up to 200ns of jitter may exist around these nominal values. The function of the data separation circuitry is to recover a clock from this data stream. Each block of data to be recovered is preceded by a sync field consisting of 96 pulses spaced at 4uS (12 bytes of 0's).

8-96. U33 and U50 detect the presence of the sync field in the following manner: U33B counts a 2 MHz clock so if 5uS or more elapses between sent pulses on pin 12, U33A will be reset by U50B. Since the sync field pulses occur at a nominal 4us, U33A will count sync field pulses and QD will present a positive edge to U34 after 8, 24, 40, 56 pulses. U34 QB and QD will transition from low to high after 24 (3 bytes) and 56 (7 bytes) pulses respectively. After U2 has recognized four bytes of the sync field, it will set HRG high which will prevent U34 from being reset by the interpulse spaces of 6uS and 8uS which will occur in the data. However, HRG will be reset if an address mark is not found in 16 bytes or if the head is in the incorrect position.

8-97. U14, U15, U16, U9 , U10 and U35 comprise a phase locked loop. U35, the VCO, runs at a nominal 500KHz. When no data is being inspected off the disc, the PLL is locked to a 500KHz reference in order to keep the loop in its active region. The DC voltage at TP2 should be within +- 2V of ground under these conditions.

8-98. U15 is responsible for three operations. First, when no data is being inspected it will lock the VCO, U35, to the 500KHz reference signal. Second, after U34 QB goes high U15 will lock the VCO to the 250KHz signal while inspection is done of the sync field. Last, when U34 QD goes high the VCO is locked to the 4uS, 6uS, or 8uS data pulses.

8-99. U17, U18, and U14 cause an in-phase switch between the 500KHz reference and the sync field (these signals have a random phase relationship). Assume that U34 QB has just gone high: The next time U14 pin 9 transitions low, U17A will be clocked true. This will lock U14 pins 9 and 5 low (the PLL will be locked to the reference) and stop the VCO, U35. The second sync pulse which occurs after this will clock U18 true which will switch U15. Then, the sync field is presented to the PLL and the VCO is restarted in phase. The second sync pulse is the one necessary to insure that both halves of U35 have timed out before they are restarted.

8-100. U31A moves the data transition, either 1-0 or 0-1, to the center of each half bit cell. U31B then sets the data transition pulse width for U2.

8-101. RS-232/MINI DRIVE THEORY OF OPERATION. (See service sheets 1 and 2 figures 8-10 and 8-13)

8-102. The theory of operation for the flexible disc drives will be provided at a later date. The block diagram theory for the mini drives should be used at this time for an understanding of the operation of the flexible disc drives.

8-103. TROUBLESHOOTING.

8-104. This section contains troubleshooting information necessary to service the Flexible Disc System in conjunction with the host 64110A Logic Developement Station. Contained are descriptions of each of the eight PV tests, decriptions of the PV error codes, the use of signature analysis, service sheet layout, the logic convention used on service sheets, definitions of mnemonics on service sheets, and some troubleshooting hints.

8-105. PERFORMANCE VERIFICATION (PV) TEST DESCRIPTIONS.

8-106. The following is a description of each of the eight tests performed during a single performance verification (PV) test cycle.

8-107. FLOPPY CONTROLLER RESPONSE TEST.

8-108. During this test the CPU writes AA hex to the track register in the mini disc controller chip and then reads it back and compares it. If this test fails error message 14 (NO RESPONSE FROM DISC CONTROLLER) is displayed.

8-109. SELECT TEST.

8-110. This test selects the drive to be tested, turns on the motor and checks for drive ready indication from the drive. If this test fails error message 1 (... DISC DOWN...) will be displayed.

8-111. TRACK 00 TEST.

8-112. This test issues a restore command to the drive and checks for the TRACK 00 indicator line to be active over track 0 and inactive over track 1. If this test fails error messages 2, 3, or 4 may be displayed. These are:

TRACK 00 INDICATOR ON OVER TRACK XX
TRACK 00 INDICATOR NOT ON OVER TRACK 0
TRACK 0 NOT FOUND

8-113. READ TRACK 0 TEST.

8-114. This test reads all 16 sectors of track 0 on both sides of the disc. The possible error messages generated are message 1, 5, 6, ,7, 8 and 9. These are:

...DISC	DOWN...
LOST DATA:	TRK XX SEC XX SIDE X-R/W
DATA CRC ERROR:	TRK XX SEC XX SIDE X-R/W
ID CRC ERROR:	TRK XX SEC XX SIDE X-R/W
RECORD NOT FOUND:	TRK XX SEC XX SIDE X-R/W
SEEK ERROR:	TRK XX NOT VERIFIED

8-115. READ TRACK 34 TEST.

8-116. This test reads all 16 sectors of track 34 on both sides of the disc. The possible error messages generated are message 1, 5, 6, 7, 8 and 9. These are:

...DISC DOWN...	
LOST DATA:	TRK XX SEC XX SIDE X-R/W
DATA CRC ERROR:	TRK XX SEC XX SIDE X-R/W
ID CRC ERROR:	TRK XX SEC XX SIDE X-R/W
RECORD NOT FOUND:	TRK XX SEC XX SIDE X-R/W
SEEK ERROR:	TRK XX NOT VERIFIED

8-117. TRACK 34 CHECK TEST.

8-118. This test checks track 34 to determine if it has been used. This is done by reading the data on track 34, sector 0 on both sides. If the track is not used the data read will be all zeros. The possible error messages are 1, 5, 6, 7, 8, 9, 11, and 12. These are:

...DISC DOWN...	
LOST DATA:	TRK XX SEC XX SIDE X-R/W
DATA CRC ERROR:	TRK XX SEC XX SIDE X-R/W
ID CRC ERROR:	TRK XX SEC XX SIDE X-R/W
RECORD NOT FOUND:	TRK XX SEC XX SIDE X-R/W
SEEK ERROR:	TRK XX NOT VERIFIED
READ KNOWN DATA ERROR:	SIDE X
NO DISC SPACE AVAILABLE FOR WRITE TEST	

8-119. TRACK 34 WRITE TEST.

8-120. This test writes to track 34 sector 1 on both sides of the disc. The error messages that can be generated are 1, 5, 6, 7, 8, 9, and 10. These are:

```
...DISC DOWN...
LOST DATA:                TRK XX SEC XX SIDE X-R/W
DATA CRC ERROR:           TRK XX SEC XX SIDE X-R/W
ID CRC ERROR:             TRK XX SEC XX SIDE X-R/W
RECORD NOT FOUND:         TRK XX SEC XX SIDE X-R/W
SEEK ERROR:               TRK XX NOT VERIFIED
NO WRITE--DISC PROTECTED
```

8-121. TRACK 34 READ/VERIFY WRITE.

8-122. This test reads the data written in the previous test and verifies that it is the same as the data written. The error messages that can be generated are 1, 5, 6, 7, 8, 9, and 13. These are:

```
...DISC DOWN...
LOST DATA:                TRK XX SEC XX SIDE X-R/W
DATA CRC ERROR:           TRK XX SEC XX SIDE X-R/W
ID CRC ERROR:             TRK XX SEC XX SIDE X-R/W
RECORD NOT FOUND:         TRK XX SEC XX SIDE X-R/W
SEEK ERROR:               TRK XX NOT VERIFIED
WRITE ERROR:  SIDE X
```

8-123. PV ERROR MESSAGES.

8-124. While running the floppy PV test an error may be encountered and an error number given. Table 8-1 gives the error number to message conversion.

Table 8-1. Mini Floppy PV Error Messages

ERROR #	ERROR MESSAGE
1	...DISC DOWN...
2	TRACK 00 INDICATOR ON OVER TRACK XX
3	TRACK 00 INDICATOR NOT ON OVER TRACK 0
4	TRACK 0 NOT FOUND
5	LOST DATA: TRK XX SEC XX SIDE X-R/W
6	DATA CRC ERROR: TRK XX SEC XX SIDE X-R/W
7	ID CRC ERROR: TRK XX SEC XX SIDE X-R/W
8	RECORD NOT FOUND: TRK XX SEC XX SIDE X-R/W
9	SEEK ERROR: TRACK XX NOT VERIFIED
10	NO WRITE--DISC WRITE PROTECTED
11	READ KNOWN DATA ERROR: SIDE X
12	NO DISC SPACE AVAILABLE FOR WRITE TEST
13	WRITE ERROR: SIDE X
14	NO RESPONSE FROM DISC CONTROLLER
15	not currently used

When the current test passes a record of previous errors is displayed in the form of an error mask. A "1" is set in each of the bit positions corresponding to the ERROR # of previous errors.

```
                    ERROR # ->  15 --------------1
PREVIOUS ERROR MASK:    XXXXXXXXXXXXXXX
```

For example, an error message reads:

```
PASSED    PREV ERRORS: 000000001000001
```

This indicates that the present test passes but during one or more of the previous tests, errors occurred due to the disc being down (ERROR #1) and ID CRC errors (ERROR #7).

8-125. DESCRIPTION OF ERROR CODES AND TROUBLESHOOTING.

8-126. Table 8-2. is a description of each error code in table 8-1. Also, some possible troubleshooting and corrective measures to follow if one of these error codes is given during PV.

Table 8-2. Description Of PV Error Codes

CODE #	DESCRIPTION
1	"...DISC DOWN..." This message indicates that the drive ready line of the disc being tested was not read in the true state. Possible trouble/corrective measure: a. No media in drive/Insert media and close door. b. No index pulses from drive or motor not running/Check index pulse circuitry and servo motor. c. Index pulses but no drive ready indication/Check drive ready circuitry. d. Drive ready signal true on floppy control board/Check CPU interface with interface DSA loops.
2	"TRACK 00 INDICATOR ON OVER TRACK XX" This message indicates that the MDC was able to verify, by reading the ID portion of the track data, that the head was positioned over track XX. However, the CPU read the TRACK 00 status bit from the Mini Drive Controller (MDC) and it was in the true state.

Possible trouble/corrective measures:

a. Go to DIAG mode (see section IV operation verification tests) and select correct drive and step to TRACK XX.

b. TRACK 00 signal is true at input to Mini Controller Chip (MDC)/Troubleshoot TRACK 00 detector circuitry, may have to do TRACK 00 switch adjustment.

c. TRACK 00 signal is false at input to MDC/Troubleshoot CPU interface circuitry with DSA interface loops.

3 "TRACK 00 INDICATOR NOT ON OVER TRACK 0" This message indicates that it was verified by reading the ID portion of the track data, that the head was positioned over track 0 but the CPU read the TRACK00 status bit from the MDC and it was in the false state.

Possible trouble/corrective measures:

a. Go to DIAG mode (see section IV operation verification tests) and select correct drive and restore it.

b. TRACK00 signal is false at input to MDC/Troubleshoot track 00 detector circuitry; may have to do a Track 00 switch adjustment.

c. TRACK00 is true at input to MDC/Troubleshoot CPU interface circuitry with DSA interface loops.

4 "TRACK 0 NOT FOUND" This message indicates that after the restore command the CPU read the TRACK00 indicator to be false and that the head was not positioned over track 0.

Possible trouble/corrective measures:

a. Go to DIAG mode (see section IV operation verification tests) and try the RESTORE command for the drive that failed.

b. Bad head positioning circuit/Check step and direction lines from the mini drive controller and stepper motor circuitry.

c. CPU interface to MDC bad/Check interface circuitry using DSA interface loops.

5 "LOST DATA TRK XX SEC XX SIDE X R/W" This message indicates that the CPU did not respond to either an interrupt or a DMA request from the mini drive controller. Also, the data in the MDC was lost.

Possible trouble/corrective measures:

a. CPU interface to MDC is bad/Check interface circuitry using DSA interface loops.

b. DMA path to CPU bad/Check using logic probe or ohmmeter.

c. Mainframe interrupt circuitry bad/Troubleshoot with DSA in mainframe I/O write test.

6 "DATA CRC TRK XX SEC XX SIDE X R" This message is generated when the mini drive controller chip detects a CRC error in the data portion of a sector read operation.

Possible trouble/corrective measures:

a. Bad media/Reformat a new disc and repeat test.

b. Data separator circuit bad/Check using DSA data separator loops.

c. Bad drive read electronics/Check read data waveforms with the ones shown in the drive and drive head alignment procedures. See radial head alignment procedure in Section V (see par. 5-19).

7 "ID CRC TRK XX SEC XX SIDE X R/W" When this message is generated the MDC chip has detected a CRC error in the ID portion of a sector read operation.

Possible trouble/corrective measure:

a. Same as trouble/corrective measures used in code 6 above.

8 "RECORD NOT FOUND TRK XX SEC XX SIDE X R/W" This message is generated when the code for the desired track, sector, and side were not found on the current track in any of the ID fields.

Possible trouble/corrective measure:

a. Bad media/Reformat a new disc and repeat test.

b. Data separator circuit bad/Check using DSA data separator loops.

c. Bad drive electronics/Check the read data waveforms with the waveforms given in the drive and drive head alignment procedures given in Section V.

d. Bad head positioning circuit/Check the step and direction lines from the mini drive controller and stepper motor circuitry.

9 "SEEK ERROR: TRK XX NOT VERIFIED" When this message is generated the code for the desired track is not found in the ID field.

Possible trouble/corrective measure:

a. The trouble and corrective measures are the same as code 8 above.

10 "NO WRITE DISC WRITE PROTECTED" This message is generated when the CPU reads the write protect line (through the activity register) for the selected drive in the true state during a write operation.

Possible trouble/corrective measure:

a. Disc write protected/Use disc that is not write protected.

b. The write protect signal is true when the disc is not write protected/Troubleshoot the write protect circuitry.

c. Write protect line operates correctly, but, the CPU interface is bad/Check CPU interface using DSA with activity buffer moved to mode buffer location.

11 "READ KNOWN DATA ERROR: SIDE X" When the data read on track 34, during the track 34 check, is not all zeros then an error is displayed.

Possible trouble/corrective measure:

a. Bad media/Reformat a new disc and perform test again.

b. Data separator circuit bad/Check using DSA data separator loops.

c. Bad drive read electronics/Check the read data waveforms with the waveforms given in the drive and head alignment procedures given in Section V.

d. Bad head positioning circuit/Check step and direction lines from the mini drive controller and stepper motor circuitry.

12 "NO DISC SPACE AVAILABLE FOR WRITE TEST" This message is generated when the first byte of data read on track 34, during the track 34 check, is not all zeros.

Possible trouble/corrective measure:

a. The trouble and corrective measures are the same as code 11 above.

13 "WRITE ERROR: SIDE X" When the data written to track 34 during the track 34 write test does not match the data read back during the track 34 read/verify test this message will be generated.

Possible trouble/corrective measure:

a. Bad media/reformat a new disc and perform the test again.

b. Bad write circuitry/check write gate, write data, and write protect signals to the MDC and the write waveforms to the drive units.

14 "NO RESPONSE FROM DISC CONTROLLER" This message is generated when the CPU cannot write 55 Hex to the track register in the Mini Drive Controller and read it back correctly.

Possible trouble/corrective measure:

a. CPU interface to MDC bad/check interface circuitry using DSA interface loops.

8-127. TROUBLESHOOTING HINTS.

8-128. The following are some things to check before troubleshooting the RS-232/mini control board.

a. Make sure the clocks on U30 pin 11 and U48 pin 11 are clocking at 2MHz.

b. Check that U41 pin 12 (LMYPA) is toggling. This indicates that the CPU is working and communicating with the mini disc controller.

c. The CPU will not work at all if LIR3 or LDMAR are pulled low at the wrong time. U50 may be removed to disable these signals.

d. Test STEP and RESTORE commands before a READ or WRITE to disc. These require that a lot less circuitry be functional.

e. The phase detector U16 locks the NEGATIVE transitions of "VCO Data" and "VCO OSC" together.

f. For a simple analysis, consider U10 to be an integrator.

g. Check that the VCO will lock to the 500KHz reference record.

h. If in real trouble, wire a header which will hold HVFOE high and HRG low. This breaks the loop between the sync detector, PLL, and U2 (MDC).

8-129. The following is some specification that should be tested before troubleshooting.

a.	U2 pin 24	1MHz +-1% square wave
b.	U36 pins 5 and 13	225mS <= PW <= 300mS
c.	U31 pin 13 U31 pin 12	1uS +- 50nS 150nS <= PW <= 190nS
d.	U35 pin 4 U35 pin 13 with TP1 grounded	period = 2uS +- 100nS asymmetry of square wave <= 5%
e.	TP2 PLL locked to 500KHz reference	+-2V of ground

8-130. TROUBLESHOOTING USING SIGNATURE ANALYSIS (SA).

8-131. The RS-232/mini control board has been designed to use signature analysis for troubleshooting to component level. Signature analysis is a technique that enables the signature analyzer to display a compressed four digit "fingerprint" or signature of the data stream at a given node. Any fault associated with a device on that node will force a change in the data stream and, therefore, result in an erroneous signature.

8-132. The troubleshooting consists of connecting the signature analyzer and tracing good and bad signatures back through gates and memory elements until a part with correct inputs and faulty outputs is isolated. Signatures are determined to be good or bad by comparison to the good signatures given in this section. SA tables 8-6 thru 8-18 are represented by a red shaded letter at a given node that correlates to the letter given with the SA table. For example, Table 8-6. Loop A, the red shaded letter "A" is given on the schematic where loop A signatures can be taken.

8-133. KEY SIGNATURES.

8-134. While using SA on the RS-232/mini Control Board some of the loops may contain key signatures. The use of the key signatures will reduce troubleshooting time considerably. A key signature is indicated with a "+" next to the node on the SA table and is a red unshaded letter on the service sheet. The key signatures should be checked before doing all of that loop. If the key signatures are good then the rest of the signatures in that loop are good.

8-135. INTERFACE LOOP.

8-136. The SA tables for the interface loop contain key signatures However, it is recommended that the key signatures in loops A, B and M be taken first. If all of the key signatures are good then no more signatures need to be taken in the interface loop. Although, if some of the key signatures in loops A, B and M are wrong other SA loops may

be necessary to find a problem.

8-137. In the interface loop, SA tables A-J are used to exercise all of the CPU/MDC interface circuitry. In this loop it the test jumper E2 is in the interface TEST position, XU12. This connects the output of the SA stimulus latch to the inputs of DMA state machine. This allows the CPU to directly control the state machine. Also, the clock for the state machine is connected to LMYPA so that the state machine is clocked only when the CPU communicates with register 4. This makes all interface circuitry synchronous with the CPU and thus allows SA. SA tables A-J are outlined below:

Table A -- Check overall interface

Table B -- Check Floppy ASM

Table M -- Check all Data (I/O Bus) to/from RS-232/mini controller

Table C -- To check I/O bus decoding

Table D -- Check Data written to Floppy drives

Table E -- Checks Floppy Read Latches

Table F -- Check Data out of U27

Table G -- Check Data from U45

Table H -- Check Data from mode buffer U47

Table I -- Check Data from the MDC (MSB)

Table J -- Check Data from the MDC (LSB) and from U47

8-138. DATA SEPARATOR LOOP.

8-139. In this loop the test jumper E1 is in the Data Separator TEST position, XU5. This connects the output of the SA latch to the data separator inputs. Also, LMYPA is connected to the L2MHZ input to the data separator. This makes all of the data separator circuitry synchronous to the CPU and thus allows for SA. SA tables K and L are outlined below:

Table K -- Check Data Separator circuitry

Table L -- To check U15 multiplexer to make sure it is multiplexing the HDATA1US signal properly. There are no signature nodes for this loop. just check for correct VH.

Table 8-3. SA Loop A

```
INTERFACE LOOP_A

PC BOARD: 64110-66509  Floppy control

CIRCUITRY TESTED: Overall interface

PROCEDURE: Remove U29 mode buffer (U29 can be tested by exchanging
           with U47). Remove all option boards. Move E2 TEST jumper
           to interface TEST position in XU12. Press DSA 1 soft key
           to initiate test.

SETUP: CLOCK - neg. edge TP10 (LMYPA)
       START - neg. edge TP7 (SA GATE)
       STOP  - pos. edge TP7 (SA GATE)
       VH    - PCP5
       +     - KEY SIGNATURE
       !     - This signature is with drive 1 connected.
       %     - This signature is with drive 0 connected.


U  1- 1  FHP9
U  1- 3  FHP9 +
U  1- 7  2603 +
U  1-13  FHP6
U  1-14  0000 +/FHP9 +!
U  1-17  260F

U  2- 2  C6F7
U  2- 3  CH09
U  2- 4  H180
U  2- 5  CU94
U  2- 6  5944
U  2- 7  H700 +
U  2- 8  9P1H +
U  2- 9  H700 +
U  2-10  C8H3 +
U  2-11  059F +
U  2-12  9P1H +
U  2-13  059F +
U  2-14  4F81 +
U  2-19  PCP5
U  2-38  0000
U  2-39  2814

U  4- 1  0000
U  4- 2  AHA7
U  4- 3  PCP5
U  4- 4  559F
U  4- 5  CUH5
U  4- 6  AHA7
U  4- 8  10H0
U  4- 9  CUH5
```

U	4-10	UC35
U	4-11	080F
U	4-12	3A65
U	4-13	CH09
U	7- 1	UC35
U	7- 2	PCP5
U	7- 3	PCP5
U	7- 4	PCP5
U	7- 6	10H0
U	7- 8	PCP5
U	7-11	UC35 +
U	7-12	5430 +
U	7-13	PCP5
U	8- 1	588P
U	8- 3	PCP5
U	8- 6	FU75
U	8- 8	5430
U	8- 9	CUH5
U	8-10	PCP5
U	8-11	PCP5
U	8-13	PCP5
U	11- 1	248A
U	11- 2	5U1F
U	11- 5	12HU
U	11- 6	P6CC
U	11- 9	7U1F
U	11-11	PCP5
U	11-12	P943
U	11-15	C4PA
U	11-16	P57A
U	11-19	1199
U	12- 1	5U1F
U	12- 2	1199
U	12- 3	12HU
U	12- 4	P57A
U	12- 5	P6CC
U	12- 6	C4PA
U	12- 7	7U1F
U	12- 8	P943
U	12- 9	PCP5
U	12-10	0000
U	12-11	0000
U	12-12	PCP5
U	12-13	P943
U	12-14	7U1F
U	12-15	C4PA
U	12-16	P6CC
U	12-17	P57A
U	12-18	12HU
U	12-19	1199

```
U 12-20  5U1F

U 13- 1  5U1F
U 13- 2  1199
U 13- 3  12HU
U 13- 4  P57A
U 13- 5  P6CC
U 13- 6  C4PA
U 13- 7  7U1F
U 13- 8  P943
U 13- 9  PCP5 +
U 13-10  0000
U 13-11  PCP5
U 13-13  FU75 +
U 13-14  5F17 +
U 13-15  PCP5 +
U 13-16  10H0 +
U 13-17  559F +
U 13-18  H50F +
U 13-19  H42F +
U 13-20  2C8P +

U 19- 1  2603
U 19- 3  FHP9 +
U 19- 7  FHP9 +
U 19-12  0000/2603 %
U 19-13  260F
U 19-17  260F

U 22- 4  FHP6
U 22- 5  2603
U 22- 6  2603
U 22- 8  FHP9
U 22- 9  FHP9
U 22-10  260F
U 22-11  260F
U 22-12  FHP6
U 22-13  000U

U 24- 1  FHP9

U 25- 1  260F
U 25- 2  PCP5
U 25- 3  PCP5
U 25- 4  0000
U 25- 5  PCP5
U 25- 6  FHP9
U 25- 8  2603
U 25- 9  PCP5
U 25-10  0000
U 25-11  PCP5
U 25-12  PCP5
U 25-13  FHP6
```

```
U 26- 1  PCP5
U 26- 3  059F +
U 26- 4  059F +
U 26- 7  H700 +
U 26- 8  H700 +
U 26-11  PU2A
U 26-13  4F81 +
U 26-14  9P1H +
U 26-17  C8H3 +
U 26-18  9P1H +

U 27- 1  1UFH
U 27- 2  059F
U 27- 5  059F
U 27- 6  H700
U 27- 9  H700
U 27-11  PCP5
U 27-12  4F81
U 27-15  9P1H
U 27-16  C8H3
U 27-19  9P1H

U 28- 2  C215
U 28- 5  PCP5
U 28- 6  7316
U 28- 9  FUU2
U 28-11  PCP5
U 28-12  19A1
U 28-15  0000
U 28-16  6PH0
U 28-19  2922

U 29- 1  588P +
U 29- 3  H700
U 29- 5  H700
U 29- 6  FHP9 +
U 29- 7  059F
U 29- 8  6UF8 +
U 29- 9  059F
U 29-11  CFCA +
U 29-12  4F81
U 29-13  PCP5
U 29-14  9P1H
U 29-15  2603
U 29-16  C8H3
U 29-18  9P1H
U 29-19  588P

U 30- 1  0000
U 30- 2  A199
U 30- 3  7U1F
U 30- 4  5U1F
U 30- 5  3199
U 30- 6  88FF
U 30- 7  1199
```

U 30- 8	12HU
U 30- 9	096U
U 30-11	PCP5 +
U 30-12	PAC6
U 30-13	P943
U 30-14	P57A
U 30-15	6FAA
U 30-16	PH4A
U 30-17	P6CC
U 30-18	C4PA
U 30-19	4462
U 32- 1	P810
U 32- 2	FF9A
U 32- 3	FF9A
U 32- 4	277U
U 32- 5	277U
U 32- 6	PCP5
U 32- 7	03U5
U 32- 9	277U
U 32-10	FF9A
U 32-11	PCP5
U 32-12	248A
U 32-13	FF9A
U 32-14	0000
U 32-15	0000
U 37- 1	A199
U 37- 2	4462
U 37- 3	PH4A
U 37- 4	6FAA
U 37- 5	3199
U 37- 6	88FF
U 37- 7	096U
U 37- 9	559F
U 37-10	H50F
U 37-11	H42F
U 37-12	2C8P
U 37-13	0000
U 37-14	0000
U 37-15	PAC6
U 38- 1	0000
U 38- 3	PCP5
U 38- 4	FHP5
U 38- 8	260F
U 38-12	FHP9
U 38-16	2603
U 38-17	0000
U 39- 1	F3U1
U 39- 2	0000
U 39- 3	PCP5
U 39- 4	PCP5
U 39- 5	842H

```
U 39- 6  6UF8
U 39- 7  CFCA
U 39- 9  575U
U 39-10  PCP5
U 39-11  PCP5
U 39-12  0000
U 39-13  10H0
U 39-14  19A1
U 39-15  19A1

U 40- 1  559F
U 40- 2  PCP5
U 40- 3  FUU2
U 40- 4  CU94
U 40- 5  PCP5
U 40- 6  2922
U 40- 7  5944
U 40- 9  CH09
U 40-10  7316
U 40-11  0000
U 40-12  5F17
U 40-13  6PH0
U 40-14  C215
U 40-15  0000

U 44- 1  PCP5 +
U 44- 3  059F +
U 44- 4  059F +
U 44- 7  H700 +
U 44- 8  H700 +
U 44-11  6624 +
U 44-13  4F81 +
U 44-14  9P1H +
U 44-17  C8H3 +
U 44-18  9P1H +

U 45- 1  AHU4
U 45- 2  059F
U 45- 5  059F
U 45- 6  H700
U 45- 9  H700
U 45-11  PCP5
U 45-12  4F81
U 45-15  9P1H
U 45-16  C8H3
U 45-17  79H8

U 46- 1  PCP5
U 46- 2  FHP6
U 46- 3  H700 +
U 46- 4  H700 +
U 46- 5  FHP6
U 46- 6  260F
U 46- 7  9P1H +
U 46- 8  4F81 +
```

```
U 46- 9  260F
U 46-10  0000
U 46-11  CHHU
U 46-12  FHP6
U 46-13  059F +
U 46-14  059F +
U 46-15  FHP6
U 46-16  260F
U 46-17  C8H3 +
U 46-18  9P1H +
U 46-19  260F

U 47- 1  080F
U 47- 2  260F
U 47- 3  H700
U 47- 4  260F
U 47- 5  H700
U 47- 6  260F
U 47- 7  059F
U 47- 8  260F
U 47- 9  059F
U 47-11  FHP6
U 47-12  4F81
U 47-13  FHP6
U 47-14  9P1H
U 47-15  FHP6
U 47-16  C8H3
U 47-17  FHP6
U 47-18  9P1H
U 47-19  080F

U 48- 1  0000
U 48- 2  588P
U 48- 3  8H32
U 48- 4  U66C
U 48- 5  UC35
U 48- 6  C6F7
U 48- 7  51A1
U 48- 8  9U2U
U 48- 9  H180
U 48-11  0000
U 48-12  PU2A
U 48-13  P27A
U 48-14  03C4
U 48-15  1UFH
U 48-16  6624
U 48-17  U067
U 48-18  67F7
U 48-19  AHU4

U 49- 1  67F7
U 49- 2  U067
U 49- 3  03C4
U 49- 4  P27A
U 49- 5  8H32
```

```
U 49- 6  U66C
U 49- 7  51A1
U 49- 9  9U2U
U 49-10  2C8P
U 49-11  H42F
U 49-12  H50F
U 49-13  559F
U 49-14  0000
U 49-15  0000

U 50- 1  3897 +
U 50- 2  000U +
U 50- 3  000U
U 50- 8  PCP5 +
U 50- 9  PCP5
U 50-10  PCP5

U 51- 1  CFCA +
U 51- 2  6UF8 +
U 51- 3  H372
U 51- 4  H372
U 51- 5  H372
U 51- 6  3897

U 52- 1  A754
U 52- 2  277U
U 52- 3  277U
U 52- 4  PCP5
U 52- 5  0000
U 52- 6  03U5
U 52- 7  PCP5
U 52- 9  PCP5
U 52-10  248A
U 52-11  0000
U 52-12  PCP5
U 52-13  0000
U 52-14  248A
U 52-15  PCP5

U 61- 2  0000
U 61- 3  FF9A
U 61- 4  4FC1
U 61- 5  P810
U 61- 6  0000
U 61- 8  PCP5
U 61- 9  0000
U 61-11  PCP5
U 61-12  0000
U 61-14  PCP5
U 61-15  03U5
U 61-16  A754
U 61-17  277U
U 61-18  0000
```

Table 8-4. SA Loop B

```
INTERFACE LOOP_B

PC BOARD: 64110-66509  Floppy control

CIRCUITRY TESTED: Floppy State Machine

PROCEDURE: Remove U29 mode buffer (U29 can be tested by exchanging
           with U47). Remove all option boards. Move E2 TEST jumper
           to interface TEST position in XU12. Press DSA 1 soft key
           to initiate test.

SETUP: CLOCK - neg. edge TP10 (LMYPA)
       START - neg. edge TP8  (LRST)
       STOP  - pos. edge TP8  (LRST)
       VH    - H9A0
       +     - KEY SIGNATURE

U  2- 2  PCF9 +
U  2- 4  12P3 +

U  4- 4  1875 +
U  4-10  7226
U  4-12  FC43 +

U  7- 1  7226 +
U  7-11  7226 +

U  8- 1  1046 +

U 11- 1  0001
U 11- 2  8211
U 11- 3  6PF2
U 11- 5  7C65
U 11- 6  2137
U 11- 9  33FH
U 11-11  H9A0
U 11-12  635A
U 11-15  FP0C
U 11-16  C623
U 11-19  25CF

U 26-11  A240 +

U 27- 1  F020 +

U 29- 1  1046 +
U 29- 19 1046 +

U 30- 1  0000
U 30- 2  99P6
U 30- 3  33FH
U 30- 4  8211
```

U 30- 5	U478
U 30- 6	92HP
U 30- 7	25CF
U 30- 8	7C65
U 30- 9	CHC2
U 30-11	H9A0
U 30-12	04HH
U 30-13	635A
U 30-14	C623
U 30-15	6P61
U 30-16	25PC
U 30-17	2137
U 30-18	FP0C
U 30-19	H275
U 37- 1	99P6
U 37- 2	H275
U 37- 3	25PC
U 37- 4	6P61
U 37- 5	U478
U 37- 6	92HP
U 37- 7	CHC2
U 37- 9	1875
U 37-10	6P9H
U 37-11	9354
U 37-12	UH4A
U 37-13	0000
U 37-14	0000
U 37-15	04HH
U 38- 5	FC43
U 38- 9	0000
U 38-11	H9A0
U 38-15	12P3
U 44-11	A0P5 +
U 45- 1	C425 +
U 48- 1	0000
U 48- 2	1046
U 48- 3	4A6F
U 48- 4	P44F
U 48- 5	7226
U 48- 6	PCF9
U 48- 7	CH73
U 48- 8	4U26
U 48- 9	12P3
U 48-11	0000
U 48-12	A240
U 48-13	2P61
U 48-14	PAA0
U 48-15	F020
U 48-16	A0P5
U 48-17	2C2C

U 48-18	02AA
U 48-19	C425
U 49- 1	02AA
U 49- 2	2C2C
U 49- 3	PAA0
U 49- 4	2P61
U 49- 5	4A6F
U 49- 6	P44F
U 49- 7	CH73
U 49- 9	4U26
U 49-10	UH4A
U 49-11	9354
U 49-12	6P9H
U 49-13	1875
U 49-14	0000
U 49-15	0000

Table 8-5. SA Loop M

```
INTERFACE LOOP_M

PC BOARD: 64110-66509  Floppy control

CIRCUITRY TESTED: All data (I/O bus) to and from floppy controller

PROCEDURE: Remove U29 mode buffer (U29 can be tested by exchanging
           with U47). Remove all option boards. Move E2 TEST jumper
           to interface TEST position in XU12. Press DSA 1 soft key
           to initiate test.

SETUP:  CLOCK - pos. edge TP10 (LMYPA)
        START - neg. edge TP7  (SA GATE)
        STOP  - pos. edge TP7  (SA GATE)
        VH    - PCP5
        +     - KEY SIGNATURE



U  8-12  407C +

U 11- 3  HP0C +
U 11- 4  AC42 +
U 11- 7  FF31 +
U 11- 8  H582 +
U 11-13  403H +
U 11-14  8198 +
U 11-17  HF8A +
U 11-18  F858 +

U 26- 2  UCA9 +
U 26- 5  438U +
U 26- 6  P366 +
U 26- 9  F596 +
U 26-12  6HA3 +
U 26-15  407C +
U 26-16  3841 +
U 26-19  CF2H +

U 27- 3  UCA9 +
U 27- 4  438U +
U 27- 7  P366 +
U 27- 8  F596 +
U 27-13  6HA3 +
U 27-14  407C +
U 27-17  3841 +
U 27-18  CF2H +

U 28- 3  UCA9 +
U 28- 4  438U +
U 28- 7  P366 +
U 28- 8  F596 +
```

```
U 28-13  6HA3 +
U 28-14  407C +
U 28-17  3841 +
U 28-18  CF2H +

U 44- 2  H582 +
U 44- 5  FF31 +
U 44- 6  AC42 +
U 44- 9  HP0C +
U 44-12  403H +
U 44-15  8198 +
U 44-16  HF8A +
U 44-19  F858 +

U 45- 3  H582 +
U 45- 4  FF31 +
U 45- 7  AC42 +
U 45- 8  HP0C +
U 45-13  403H +
U 45-14  8198 +
U 45-17  HF8A +
U 45-18  F858 +
```

Table 8-6. SA Loop C

```
INTERFACE LOOP_C

PC BOARD: 64110-66509 Floppy control

CIRCUITRY TESTED: I/O bus decoding

PROCEDURE: Remove U29 mode buffer (U29 can be tested by exchanging
           with U47). Remove all option boards. Move E2 TEST jumper
           to interface TEST position in XU12. Press DSA 1 soft key
           to initiate test.

SETUP: CLOCK - pos. edge TP7 CPU/IO board (LBIOSB)
       START - pos. edge TP6 CPU/IO board (I/O SA LATCH)
       STOP  - neg. edge TP6 CPU/IO board (I/O SA LATCH)
       VH    - 9CCH
       +     - KEY SIGNATURE



U  5- 6  H164 +

U  7- 3  H164 +
U  7-13  H164 +

U  8- 3  1FAA +
U  8-10  H543 +
U  8-11  1FAA +

U 11- 1  188H +
U 11-11  H164 +

U 12- 9  H164

U 13- 9  H164 +

U 26- 1  02HP +

U 27-11  FC37 +

U 28-11  1FAA +

U 30-11  H164 +

U 32- 1  3H75
U 32- 2  P552
U 32- 3  P552
U 32- 4  7PPU
U 32- 5  7PPU
U 32- 6  9CCH
U 32- 7  6662
U 32- 9  CP45
U 32-10  P552
```

U 32-11	9CCH
U 32-12	188H
U 32-13	P552
U 32-14	0000
U 32-15	0000
U 41- 1	FF56
U 41- 2	3CHU
U 41- 3	190F
U 41- 4	0000
U 41- 5	0000
U 41- 6	8CU1
U 41-12	H164
U 44- 1	02HP +
U 45-11	FC37 +
U 48-11	4AH9 +
U 52- 1	02HU
U 52- 2	CP45
U 52- 3	CP45
U 52- 4	H543
U 52- 5	0000
U 52- 6	6662
U 52- 7	1FAA
U 52- 9	FC37
U 52-10	188H
U 52-11	0000
U 52-12	02HP
U 52-13	0000
U 52-14	188H
U 52-15	H164
U 61- 3	7PPU
U 61- 4	9962
U 61- 5	3H75
U 61- 6	0000
U 61- 8	9CCH
U 61- 9	104F
U 61-11	8CU1
U 61-12	0000
U 61-14	9CCH
U 61-16	02HU
U 61-17	7PPU

Table 8-7. SA Loop D

```
INTERFACE LOOP_D

PC BOARD: 64110-66509  Floppy control

CIRCUITRY TESTED: Data written to floppy drives

PURPOSE: Remove U29 mode buffer (U29 can be tested by exchanging
         with U47). Remove all option boards. Move E2 TEST jumper
         to interface TEST position in XU12. Press DSA 1 soft key
         to initiate test.

SETUP: CLOCK - neg. edge TP16 (near U 53)
       START - pos. edge TP6 CPU/IO board (I/O SA LATCH)
       STOP  - neg. edge TP6 CPU/IO board (I/O SA LATCH)
       VH    - 399F
       +     - KEY SIGNATURE



U  2-19  6C35 +

U  4- 5  0A66 +
U  4- 9  0A66 +

U  7-12  33UA +

U  8- 3  5613
U  8- 8  33UA
U  8- 9  0A66
U  8-10  6U8U
U  8-11  5613
U  8-12  U74A

U 11- 3  1443 +
U 11- 4  1443 +
U 11- 7  46CA +
U 11- 8  46CA +
U 11-13  7C48 +
U 11-14  29C1 +
U 11-17  29U0 +
U 11-18  29C1 +

U 26- 2  C4F8 +
U 26- 5  98F4 +
U 26- 6  71P3 +
U 26- 9  606H +
U 26-12  HA15 +
U 26-15  U74A +
U 26-16  U834 +
U 26-19  52PF +
```

```
U 27- 3  C4F8 +
U 27- 4  98F4 +
U 27- 7  71P3 +
U 27- 8  606H +
U 27-13  HA15 +
U 27-14  U74A +
U 27-17  U834 +
U 27-18  52PF +

U 28- 2  5U64
U 28- 3  C4F8
U 28- 4  98F4
U 28- 5  6C35
U 28- 6  19P9
U 28- 7  71P3
U 28- 8  606H
U 28- 9  9064
U 28-11  5613
U 28-12  6651
U 28-13  HA15
U 28-14  U74A
U 28-15  U7UC
U 28-16  H45F
U 28-17  U834
U 28-18  52PF

U 39-14  6651 +
U 39-15  6651 +

U 40- 3  9064 +
U 40- 6  086P +
U 40-10  19P9 +
U 40-13  H45F +
U 40-14  5U64 +

U 44- 2  46CA +
U 44- 5  46CA +
U 44- 6  1443 +
U 44- 9  1443 +
U 44-12  7C48 +
U 44-15  29C1 +
U 44-16  29U0 +
U 44-19  29C1 +

U 45- 3  46CA +
U 45- 4  46CA +
U 45- 7  1443 +
U 45- 8  1443 +
U 45-13  7C48 +
U 45-14  29C1 +
U 45-17  29U0 +
U 45-18  29C1 +
```

Table 8-8. SA Loop E

```
INTERFACE LOOP_E

PC BOARD: 64110-66509 Floppy control

CIRCUITRY TESTED: Floppy read latches

PROCEDURE: Remove U29 mode buffer (U29 can be tested by exchanging
           with U47). Remove all option boards. Move E2 TEST jumper
           to interface TEST position in XU12. Press DSA 1 soft key
           to initiate test.

SETUP: CLOCK - pos. edge TP11 (LRD)
       START - neg. edge TP7  (SA GATE)
       STOP  - pos. edge TP7  (SA GATE)
       VH    - 0007
       +     - KEY SIGNATURE



U 26- 2  0003
U 26- 5  0003
U 26- 6  0003
U 26- 9  0003
U 26-12  0003
U 26-15  0003
U 26-16  0003
U 26-19  0003

U 27- 3  0003 +
U 27- 4  0003 +
U 27- 7  0003 +
U 27- 8  0003 +
U 27-13  0003 +
U 27-14  0003 +
U 27-17  0003 +
U 27-18  0003 +

U 44- 2  0002
U 44- 5  0002
U 44- 6  0002
U 44- 9  0002
U 44-12  0001
U 44-15  0001
U 44-16  0001
U 44-19  0001

U 45- 3  0002
U 45- 4  0002
U 45- 7  0002
U 45- 8  0002
U 45-13  0001
U 45-14  0001
```

U 45-17	0001
U 45-18	0001

Table 8-9. SA Loop F

```
INTERFACE LOOP_F

PC BOARD: 64110-66509 Floppy control

CIRCUITRY TESTED: Data out of U29

PROCEDURE: Remove U29 mode buffer (U29 can be tested by exchanging
           with U47). Remove all option boards. Move E2 TEST jumper
           to interface TEST position in XU12. Press DSA 1 soft key
           to initiate test.

SETUP: CLOCK - pos. edge  TP14 (LOEM)
       START - neg. edge  TP7  (SA GATE)
       STOP  - pos. edge  TP7  (SA GATE)
       VH    - 0003
       +     - KEY SIGNATURE


U  2- 7  0002 +
U  2- 8  0002 +
U  2- 9  0002 +
U  2-10  0002 +
U  2-11  0002 +
U  2-12  0002 +
U  2-13  0002 +
U  2-14  0002 +

U 27- 2  0002
U 27- 5  0002
U 27- 6  0002
U 27- 9  0002
U 27-12  0002
U 27-15  0002
U 27-16  0002
U 27-19  0002

U 46- 7  0002 +
U 46- 8  0002 +
U 46-13  0002 +
U 46-14  0002 +
U 46-17  0002 +
U 46-18  0002 +
```

Table 8-10. SA Loop G

```
INTERFACE LOOP_G

PC BOARD: 64110-66509  Floppy control

CIRCUITRY TESTED: Data from U45

PROCEDURE: Remove U29 mode buffer (U29 can be tested by exchanging
           with U47). Remove all option boards. Move E2 TEST jumper
           to interface TEST position in XU12. Press DSA 1 soft key
           to initiate test.

SETUP: CLOCK - pos. edge TP12 (LOEL)
       START - neg. edge TP7  (SA GATE)
       STOP  - pos. edge TP7  (SA GATE)
       VH    - OUP7
       +     - KEY SIGNATURE



U  2- 7  0A2H +
U  2- 8  0F24 +
U  2- 9  0A2H +
U  2-10  0F14 +
U  2-11  0201 +
U  2-12  0F24 +
U  2-13  0201 +
U  2-14  0408 +

U 45- 6  0A2H
U 45- 9  0A2H
U 45-12  0408
U 45-15  0F24
U 45-16  0F14
U 45-19  0F24

U 46- 3  0A2H +
U 46- 4  0A2H +
U 46- 7  0F24 +
U 46- 8  0408 +
U 46-13  0201 +
U 46-14  0201 +
U 46-17  0F14 +
U 46-18  0F24 +
```

Table 8-11. SA Loop H

```
INTERFACE LOOP_H

PC BOARD: 64110-66509  Floppy control

CIRCUITRY TESTED: Data from U47

PROCEDURE: Remove U29 mode buffer (U29 can be tested by exchanging
           with U47). Remove all option boards. Move E2 TEST jumper
           to interface TEST position in XU12. Press DSA 1 soft key
           to initiate test.

SETUP: CLOCK - pos. edge TP9
       START - neg. edge TP7  (SA GATE)
       STOP  - pos. edge TP7  (SA GATE)
       VH    - 0003
       +     - KEY SIGNATURE



U 44- 3  0002 +
U 44- 4  0002 +
U 44- 7  0002 +
U 44- 8  0002 +
U 44-13  0001 +
U 44-14  0001 +
U 44-17  0001 +
U 44-18  0001 +

U 47- 1  0000
U 47- 3  0002
U 47- 5  0002
U 47- 7  0002
U 47- 9  0002
U 47-12  0001
U 47-14  0001
U 47-16  0001
U 47-18  0001
U 47-19  0000
```

Table 8-12. SA Loop I

```
INTERFACE LOOP_I

PC BOARD: 64110-66509  Floppy control

CIRCUITRY TESTED: Data from floppy controller (MSB)

PROCEDURE: Remove U29 mode buffer (U29 can be tested by exchanging
           with U47). Remove all option boards. Move E2 TEST jumper
           to interface TEST position in XU12. Press DSA 1 soft key
           to initiate test.

SETUP: CLOCK - pos. edge U26-PIN 11 (LLM)
       START - neg. edge TP7  (SA GATE)
       STOP  - pos. edge TP7  (SA GATE)
       VH    - 07U3
       +     - KEY SIGNATURE



U  2- 7  07H3
U  2- 8  07H3
U  2- 9  07H3
U  2-10  07H3
U  2-11  07H3
U  2-12  07H3
U  2-13  07H3
U  2-14  07H3

U 26- 3  07H3 +
U 26- 4  07H3 +
U 26- 7  07H3 +
U 26- 8  07H3 +
U 26-13  07H3 +
U 26-14  07H3 +
U 26-17  07H3 +
U 26-18  07H3 +

U 29- 1  0020
U 29- 3  07H3
U 29- 5  07H3
U 29- 7  07H3
U 29- 9  07H3
U 29-12  07H3
U 29-14  07H3
U 29-16  07H3
U 29-18  07H3
U 29-19  0020
```

Table 8-13. SA Loop J

```
INTERFACE LOOP_J

PC BOARD: 64110-66509  Floppy control

CIRCUITRY TESTED: Data from floppy controller (LSB) and data
                  from mode buffer U47.

PROCEDURE: Remove U29 mode buffer (U29 can be tested by exchanging
           with U47). Remove all option boards. Move E2 TEST jumper
           to interface TEST position in XU12. Press DSA 1 soft key
           to initiate test.

SETUP: CLOCK - pos. edge U44-PIN 11 (LLL)
       START - neg. edge TP7  (SA GATE)
       STOP  - pos. edge TP7  (SA GATE)
       VH    - 001U
       +     - KEY SIGNATURE



U  2- 7  000A
U  2- 8  0011
U  2- 9  000A
U  2-10  0011
U  2-11  000A
U  2-12  0011
U  2-13  000A
U  2-14  0011

U 44- 7  000A +
U 44- 8  000A +
U 44-13  0011 +
U 44-14  0011 +
U 44-15  001U +
U 44-16  001U +
U 44-17  0011 +
U 44-18  0011 +

U 47- 1  001F
U 47- 3  000A
U 47- 5  000A
U 47- 7  000A
U 47- 9  000A
U 47-12  0011
U 47-14  0011
U 47-16  0011
U 47-18  0011
U 47-19  001F
```

8-140. SERVICE SHEET LAYOUT.

8-141. Each service sheet represents in detail the circuitry that controls each of the functional areas shown in table 8-14. Reduced block diagrams and component locators are given with each service sheet. These are gray shaded to show the general relationships of the particular circuitry to the overall system.

8-142. RS-232/MINI CONTROL AND DRIVE AND SERVICE SHEET LAYOUT.

8-143. The circuitry for the RS-232/mini control board is shown on service sheets 11A-11C and the circuitry for the mini drives is shown on sheets 1 and 2. Refer to table 8-14 for a list of service sheets and the functional circuitry shown on each.

Table 8-14. Service Sheet to Function

Service Sheet Number	Functions Shown
11A Figure 8-10	uP Interface/DMA State Machine
	CPU Decode
	DMA/CPU Address Selector
	Interrupt Circuitry
	DMA Request
	SA Stimulus Latch
	DMA Acknowledge Latch
	Processor Request Latch
	DMA Enable Latch
	Interface Control Latch
	Data Latches
11B Figure 8-13	4MHz Oscillator
	Drive Ready Monostables
	Media Change Latches
	CPU/Drive Interface
	Drive Control Latch and Buffer
	Drive Status Buffer
	Disc Drive Multiplexer and Control Buffering
11C Figure 8-16	Data Separator Circuitry
	Voltage Controlled Oscillator
	Zero Detection
	Phase Detection
	Drive Power Supply
1 Figure 8-18	Servo Electronics
2 Figure 8-21	Drive Electronics

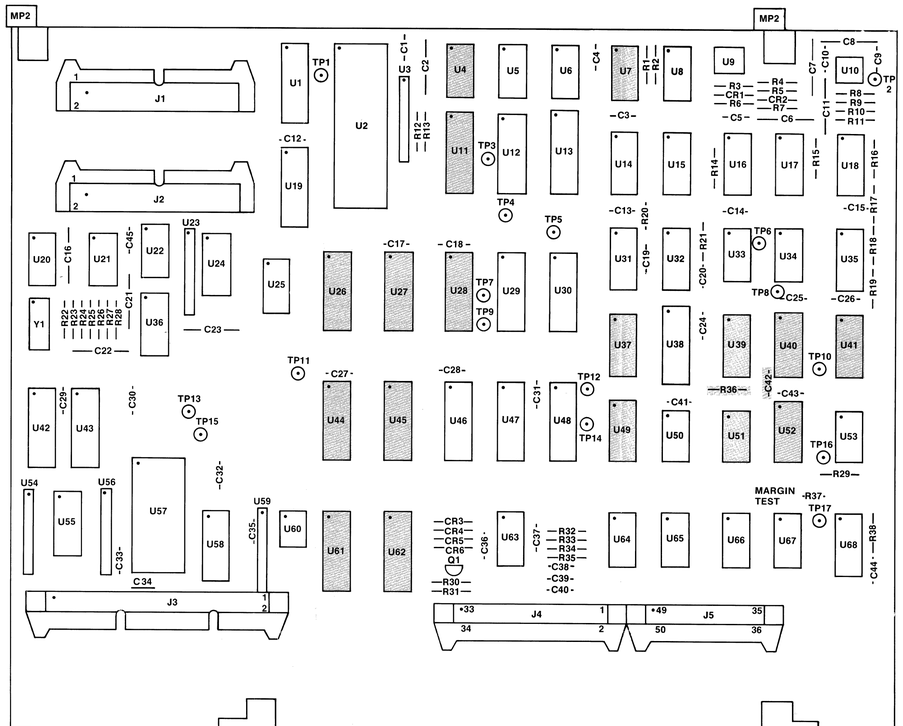


Figure 8-8. Component Locator for Service Sheet 11A

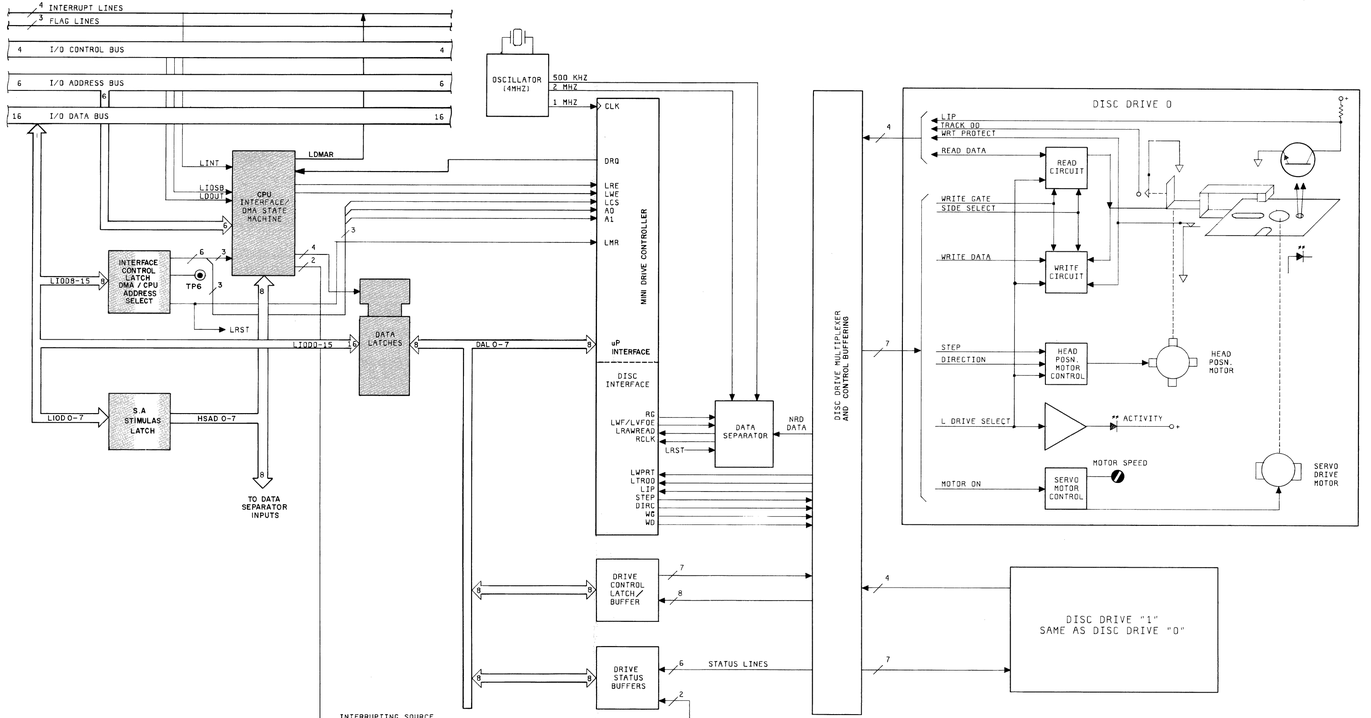
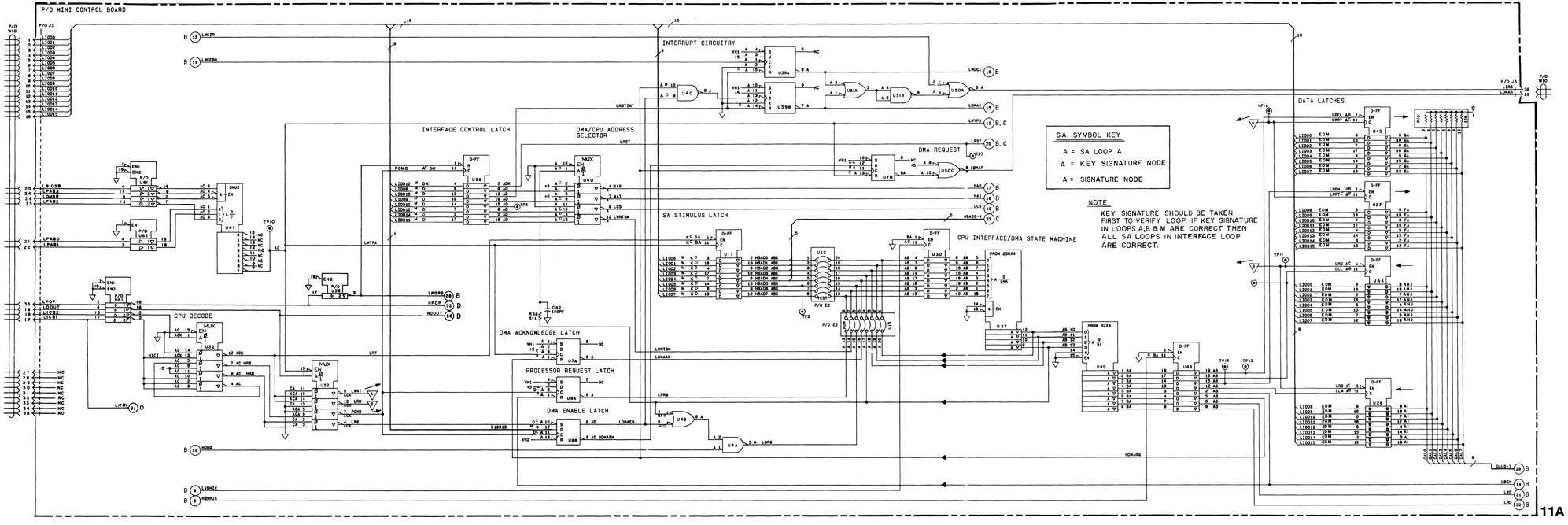


Figure 8-9. RS-232/Mini Control Block Diagram for Service Sheet 11A



ICs ON THIS SCHEMATIC

REF DES.	HP PART NO.	MFR PART NO.
U4	74LS132	74LS123
U7,8	1820-1112	74LS74AN
U11	1820-1858	74LS377
U26,27,44,45,48	1820-1997	74LS374N
U32,52	1820-1428	74LS158
U37	64110-10001	ROM-ASM CONTROL
U38,61	1820-1917	74LS240N
U39	1820-1212	74LS112
U41	1820-1216	74LS138
U49	64110-10002	ROM-ASM OUT DC
U50	1820-1246	74LS09
U51	1820-1197	74LS00
U62	1820-2024	74LS244N
U28	1820-1730	74LS273N
U40	1820-1470	74LS157

PARTS ON THIS SCHEMATIC

R36
C42

IC POWER SUPPLY CONFIGURATIONS

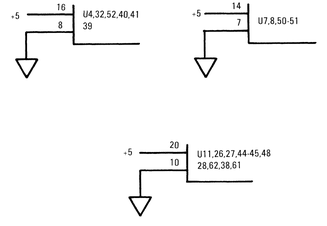


Figure 8-10.
RS-232/Mini Control Service Sheet 11A.
8-51 AP

Figure 8-11. Component Locator for Service Sheet 11B

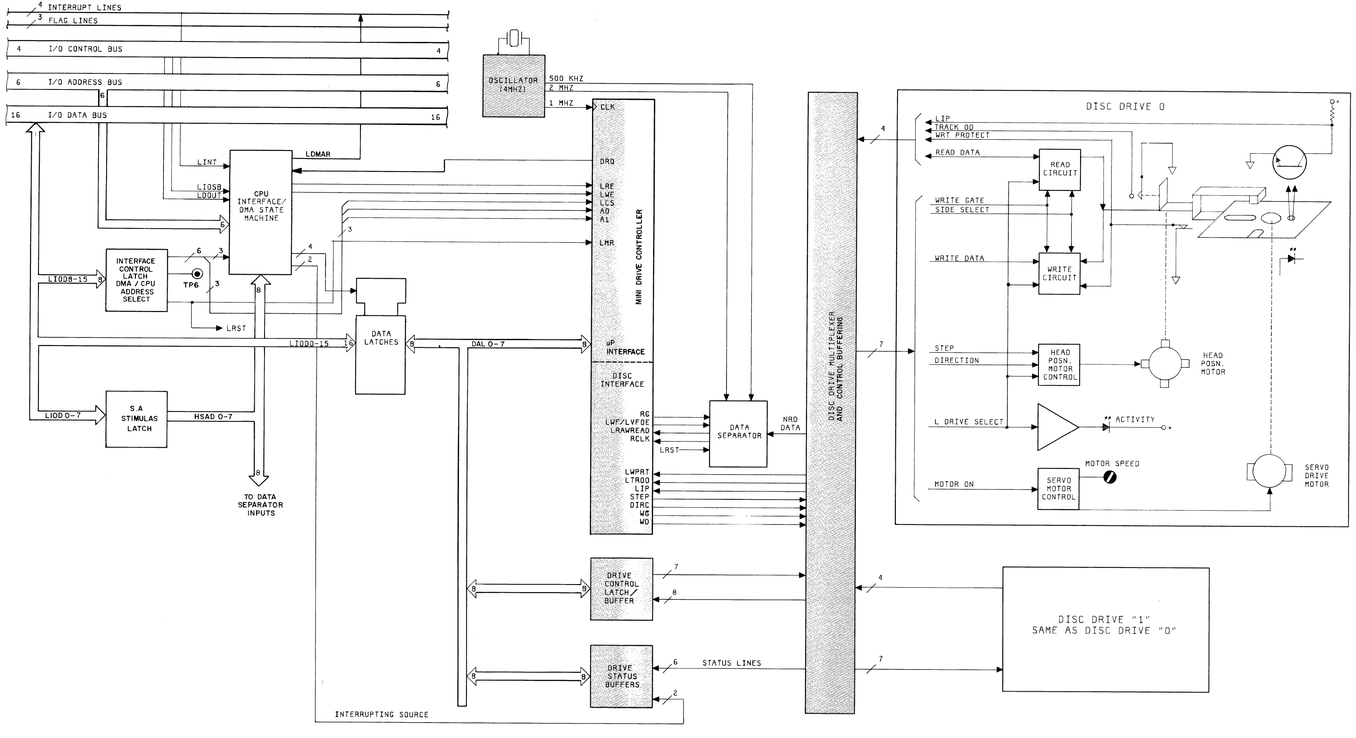
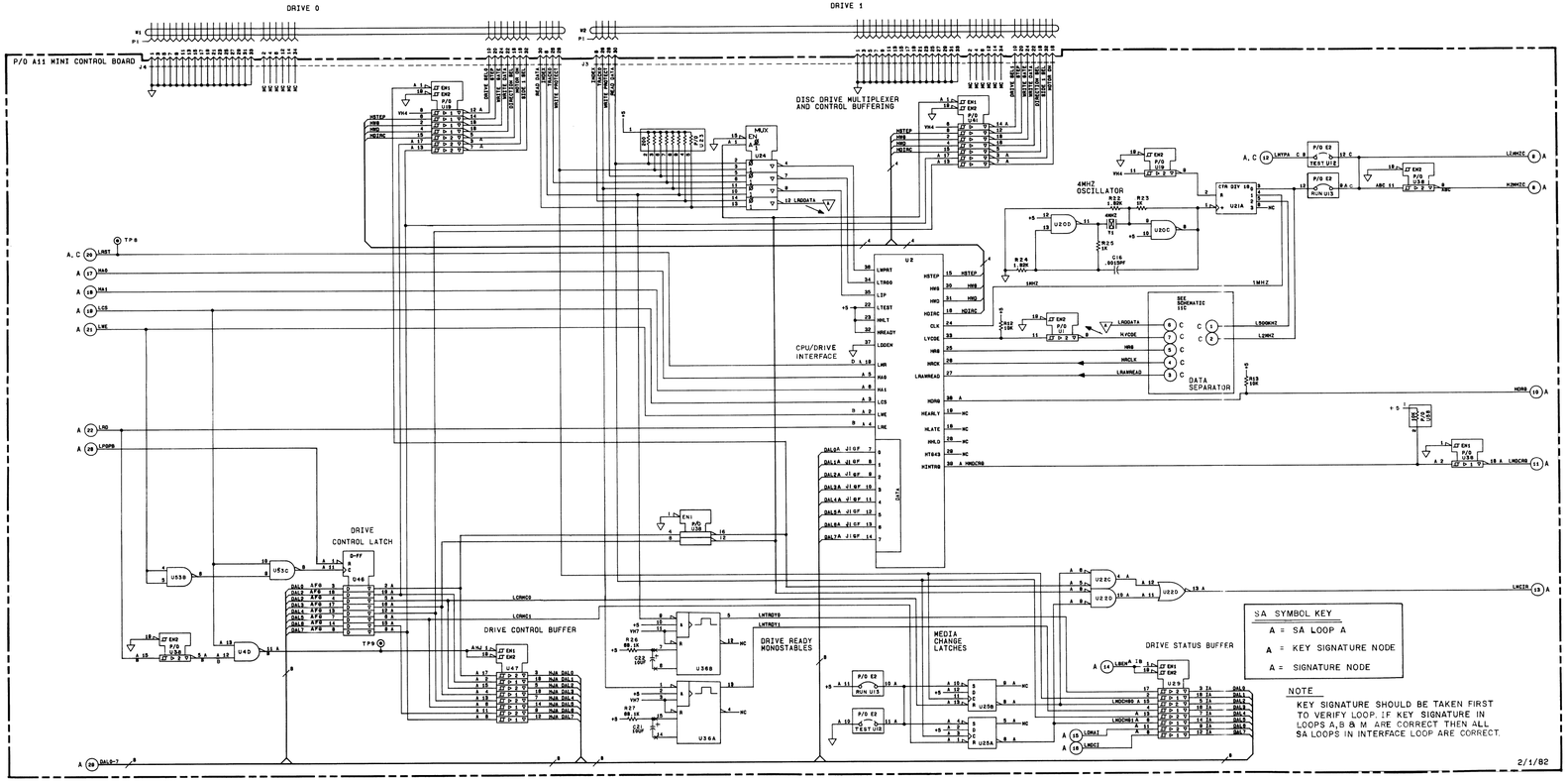


Figure 8-12. RS-232/Mini Control Block Diagram for Service Sheet 11B



ICs ON THIS SCHEMATIC

REF DES.	HP PART NO.	MFR PART NO.
U1,19	1820-1633	74S240
U2	1820-2456	FD1791A-01
U20,53	1820-1197	74LS00
U21	1820-1989	74LS393
U22	1820-1144	74LS02
U23	1810-0271	RESNET 200X9
U24	1820-1470	74LS157
U25	1820-1112	74LS74AN
U29,47	1820-2024	74LS244
U36	1820-1423	74LS123
U38	1820-1917	74LS240
U46	1820-1730	74LS273
U58	1813-0131	K1135

PARTS ON THIS SCHEMATIC

R12,13,22,25-27
C16,21,27

IC POWER SUPPLY CONFIGURATIONS

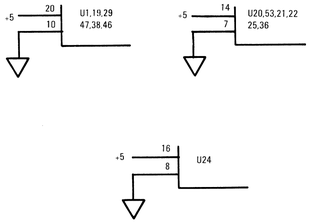


Figure 8-13.
RS-232/Mini Control Service Sheet 11B
8-53 AP

Figure 8-14. Component Locator for Service Sheet 11C

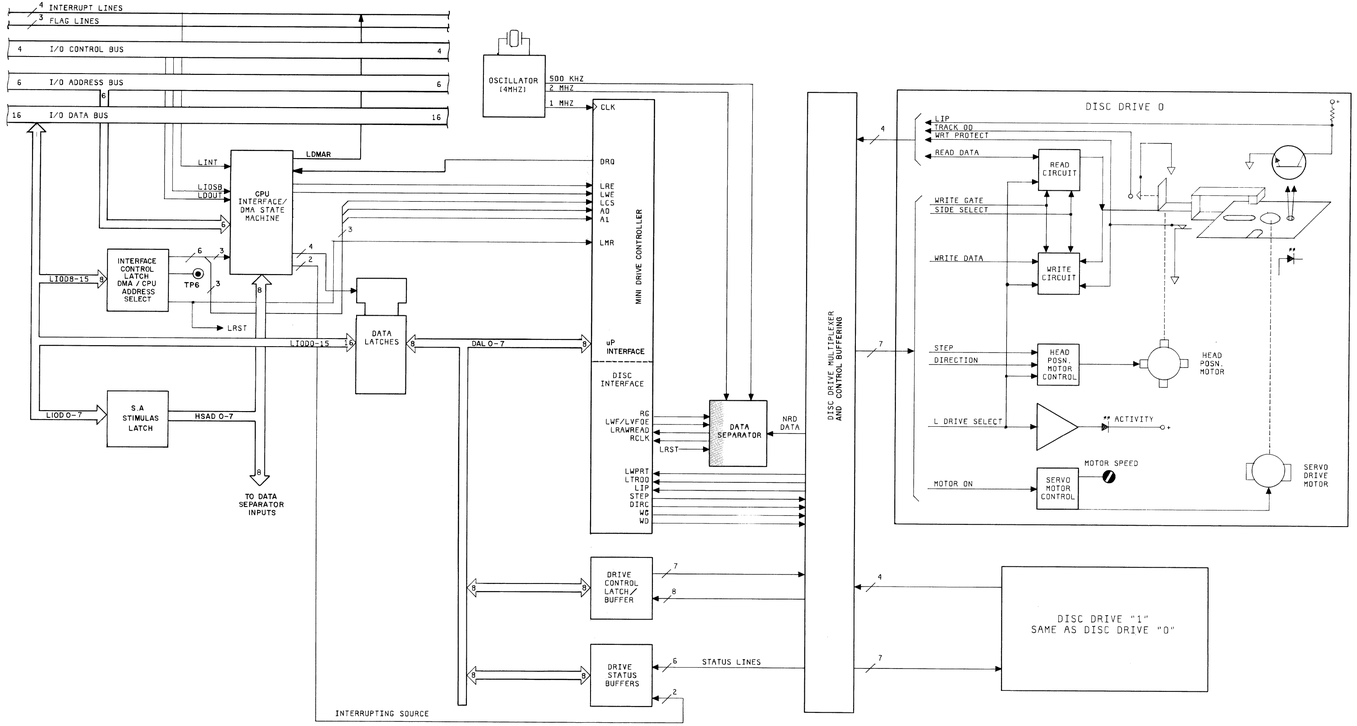


Figure 8-15. Rs-232/Mini Control Block Diagram for Service Sheet 11C

Table 8-15. SA Loop K

DATA SEPARATOR LOOP_K

PC BOARD: 64110-66509 Floppy control

CIRCUITRY TESTED: Data separator circuitry

PROCEDURE: Remove all option boards. Move E1 TEST jumper to separator TEST position in XU5. Press DSA 2 soft key to initiate test.

SETUP: CLOCK - pos. edge TP10 (LMYPA)
START - neg. edge U11-PIN 15 (SA GATE)
STOP - pos. edge U11-PIN 15 (SA GATE)
VH - HCH5
\+ - KEY SIGNATURE

U 5- 1 5944	U 14- 1 5A44	U 16-10 HCH5
U 5- 2 5U2F	U 14- 2 HCH5	U 16-11 HCHF
U 5- 3 8P80	U 14- 3 383P	U 16-12 0000
U 5- 4 CAHF	U 14- 5 HH3A	U 16-13 4U2F
U 5- 5 5A44	U 14- 9 H015	U 16-14 4FA6
U 5- 6 0000	U 14-11 383P	U 16-15 4U2F
	U 14-12 HCH5	
U 9- 1 7CA3 +	U 14-13 CAHF	U 17- 1 H015
U 9- 2 7CA3 +		U 17- 2 0000
U 9- 6 55AP +	U 15- 1 0000	U 17- 3 0HA5
U 9- 7 55AP +	U 15- 2 P733	U 17- 4 165A
	U 15- 3 5A44	U 17- 5 2P64
U 11- 1 5690	U 15- 4 0000	U 17- 6 383P
U 11- 2 5944	U 15- 5 0000	U 17- 9 6P1C
U 11- 3 HPU6	U 15- 6 4H3A	U 17-10 HCH5
U 11- 4 27PU	U 15- 7 0000	U 17-11 2P64
U 11- 5 8P80	U 15- 9 4U2F	U 17-12 0000
U 11- 6 5A44	U 15-10 H015	U 17-13 0000
U 11- 7 H8U7	U 15-11 0000	U 17-14 0HA5
U 11- 8 64A3	U 15-12 0000	U 17-15 5623
U 11- 9 846P	U 15-13 0000	
U 11-11 0000	U 15-14 5C86	U 18- 1 0000
U 11-12 C107	U 15-15 0000	U 18- 2 0000
U 11-13 0P71		U 18- 3 6P1C
U 11-14 5691	U 16- 1 4FA6	U 18- 4 HCH5
U 11-15 0000	U 16- 2 0000	
U 11-16 CAHF	U 16- 3 HCH5	
U 11-17 19F6	U 16- 4 HCH5	
U 11-18 P8F9	U 16- 5 7CA3	
U 11-19 5U2F	U 16- 7 55AP	

U 18- 5	5C86
U 18- 6	8053
U 18-11	5944
U 18-15	0HA5
U 28- 4	UUCF
U 28- 5	165A
U 28-11	8H45
U 31- 4	HCH5
U 31-10	HCH5
U 31-11	5944
U 31-12	HCH5
U 31-13	0000
U 32- 1	8H45
U 32-12	5690
U 32-13	HCH5
U 33- 1	HCH5
U 33- 2	82A4
U 33- 6	488C
U 33- 8	82F8
U 33-10	CH11
U 33-12	0000
U 33-13	0000
U 34- 1	HCH5
U 34- 2	HCH5
U 34- 4	0HA5
U 34- 6	P733
U 34- 8	488C
U 34- 9	F82F
U 35- 9	2P64
U 38- 4	0000
U 38- 6	0000
U 38- 8	5690
U 38-12	8H45
U 38-14	HCH5
U 38-16	HCH5
U 50- 4	CH11
U 50- 5	82F8
U 50- 6	82A4
U 50-11	5623
U 50-12	8053
U 50-13	0HA5
U 51- 8	0000
U 51- 9	HCH5
U 51-10	HCH5
U 51-11	HCH5
U 51-12	0000
U 51-13	0000
U 52- 1	HCH5
U 52- 5	0000
U 52- 6	5690
U 52- 7	8H45
U 52- 9	8H45
U 52-10	5690
U 52-12	HCH5
U 52-14	5690
U 52-15	0000
U 53- 1	82A4
U 53- 2	84U9
U 53- 3	F82F
U 53-11	84U9
U 53-12	5U2F
U 53-13	HCH5

Table 8-16. SA Loop L

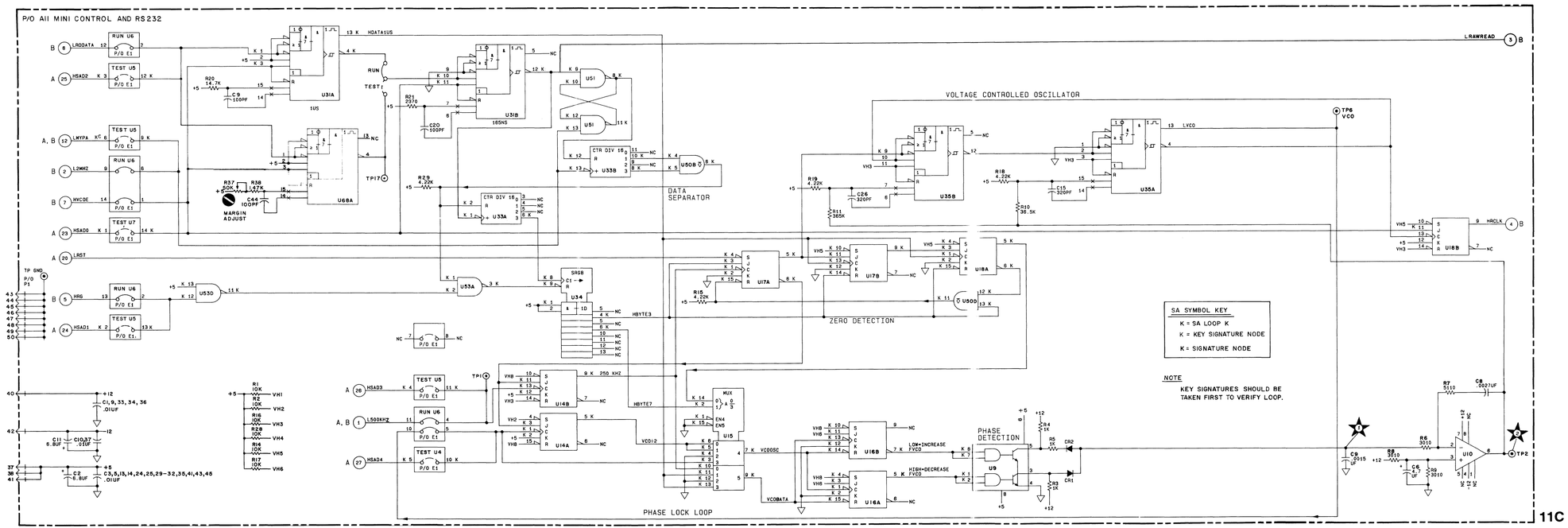
DATA SEPARATOR LOOP_L

PC BOARD: 64110-66509 Floppy control

CIRCUITRY TESTED: U15 multiplexer

PROCEDURE: Remove all option boards. Move E1 TEST jumper to separator TEST position in XU5. Check U15 multiplexer to make sure it is multiplexing the HDATA1US signal properly. There are no signature nodes for this loop, just verify that VH is correct. Press DSA 2 soft key to initiate test.

SETUP: CLOCK - pos. edge U15-PIN 9
START - pos. edge U18-PIN 11
STOP - pos. edge U18-PIN 11
VH - 72A2



ICs ON THIS SCHEMATIC

REF DES.	HP PART NO.	MFR PART NO.
U9	1820-0535	75U5IN LIN
U10	1826-0207	OP AMP LM318
U14,16-18	1820-1212	74LS112
U15	1820-1244	k74LS153
U31,38,35	1820-1260	74221N
U33	1820-1989	74LS393
U34	1820-1433	74LS164
U50	1820-1246	74LS09
U51,53	1820-1197	74LS00

PARTS ON THIS SCHEMATIC

R3,6-11,15,18-21
29,37,38
C2,3-5,10,13,14,24,25,29-32,35,41
C6,8,9,15,20,26,44,43,45
C1,33,34,36,11
CR1,2

IC POWER SUPPLY CONFIGURATIONS

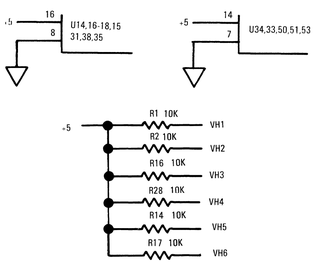
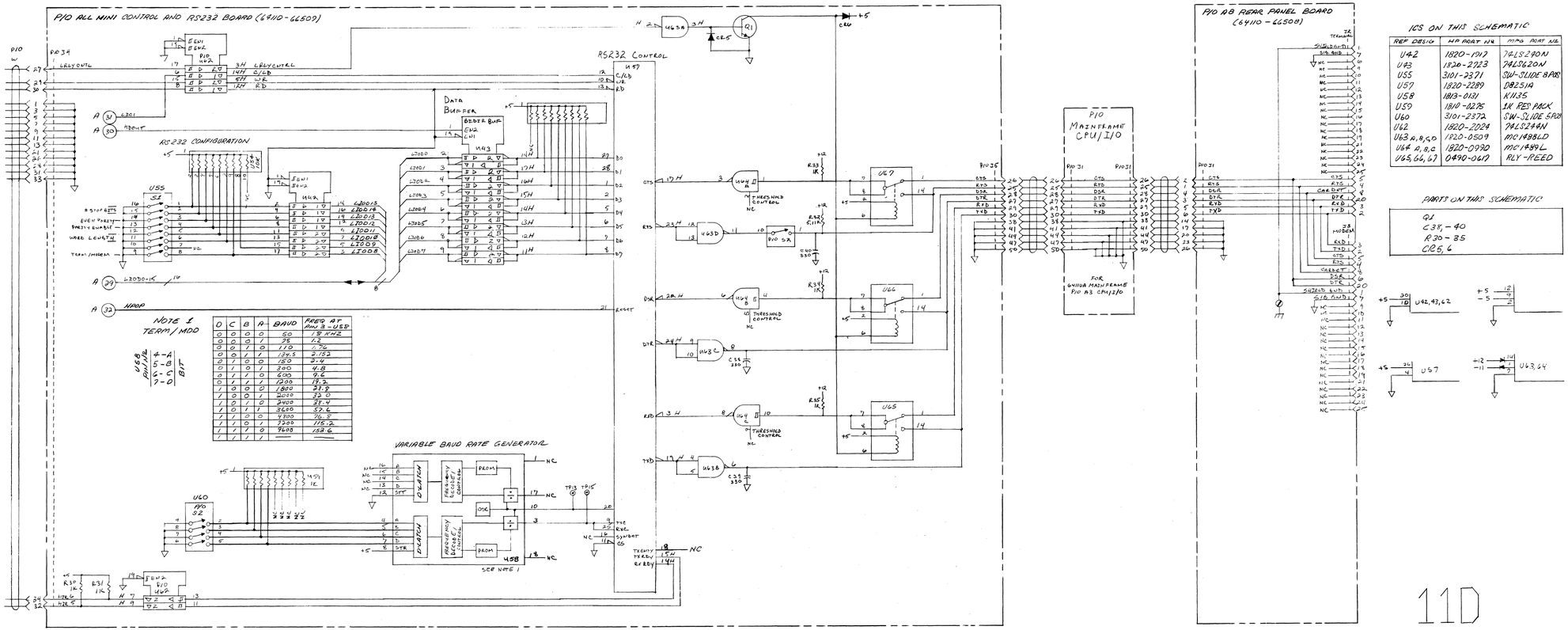


Figure 8-16.
RS-232/Mini Control Service Sheet 11C
8-59 AP

Figure 8-17. RS-232/Mini Control Component Locator 11D



REF DESIG	HP PART NO	MFR PART NO
U42	1820-1917	74LS290N
U43	1820-2723	74LS620N
U55	3101-2371	SW-SLIDE 8POS
U57	1820-2289	DB25IA
U58	1813-0131	K1135
U59	1810-0275	1K RES PACK
U60	3101-2372	SW-SLIDE 5POS
U62	1820-2024	74LS244N
U63,A,B,C,D	1820-0509	MC1488LD
U64 A,B,C	1820-0990	MC1489L
U65,66,67	0490-0617	RLY-REED

D	C	B	A	BAUD	FREQ AT PINS 3-USS
0	0	0	0	50	1.8 KHZ
0	0	0	1	75	1.2
0	0	1	0	110	.76
0	0	1	1	134.5	2.152
0	1	0	0	150	9.4
0	1	0	1	300	4.8
0	1	1	0	600	9.6
0	1	1	1	1200	19.2
1	0	0	0	1800	21.9
1	0	0	1	2000	32.0
1	0	1	0	2400	38.4
1	0	1	1	3600	57.6
1	1	0	0	4800	76.8
1	1	0	1	7200	115.2
1	1	1	0	9600	153.6
1	1	1	1	——	——

Figure 8-18.
RS-232/Mini Control Service Sheet 11D
8-61 AP

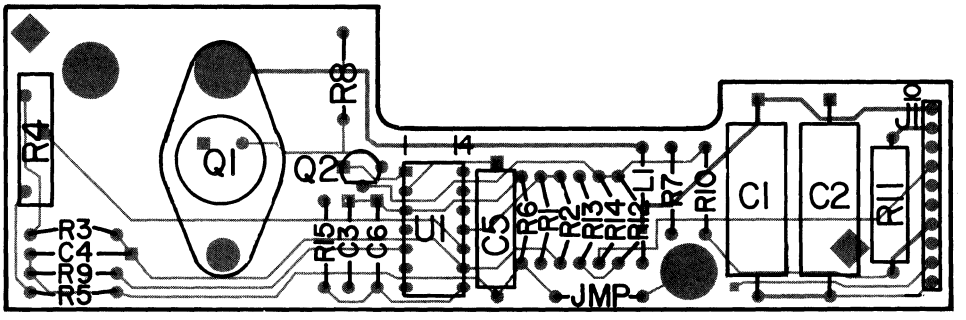


Figure 8-19. Component Locator for Service Sheet 1

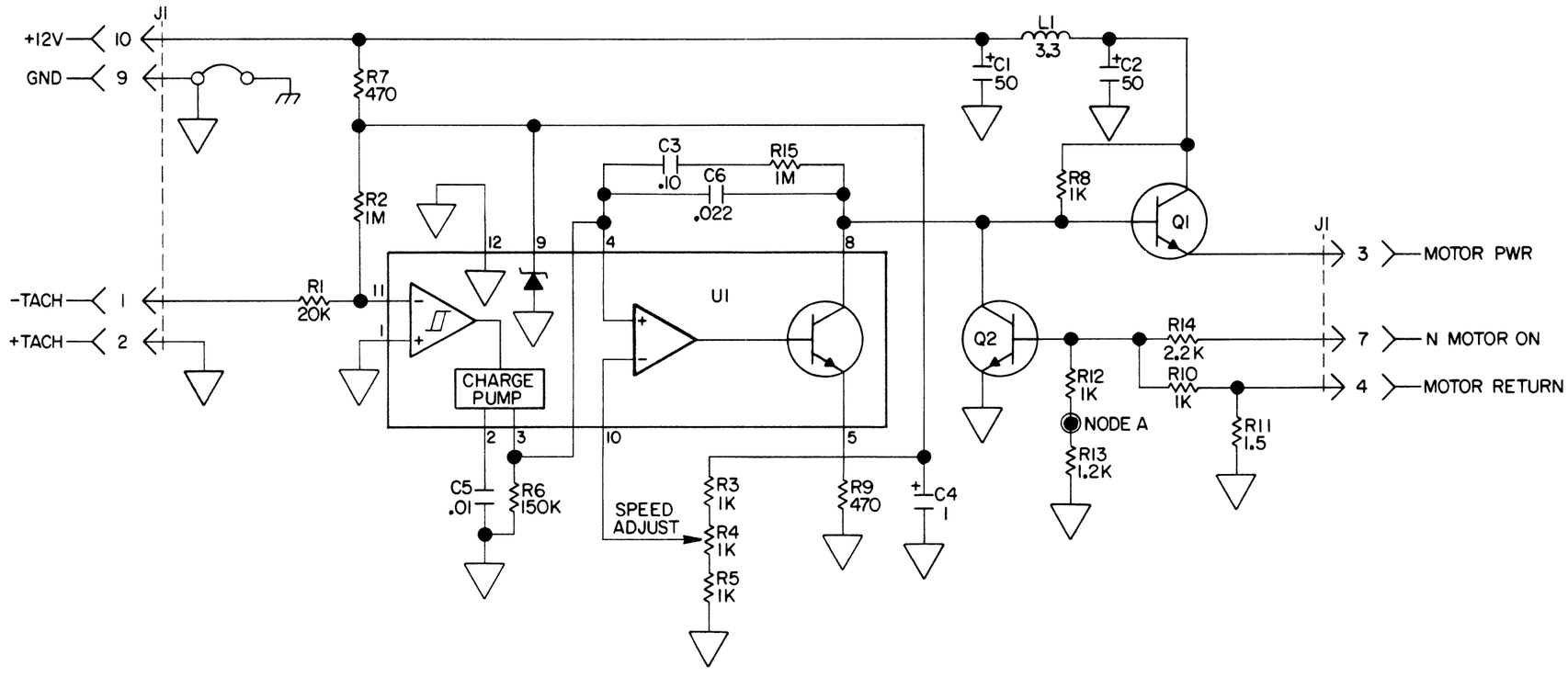


Figure 8-20.
Servo Electronics Service Sheet 1
8-63 AP

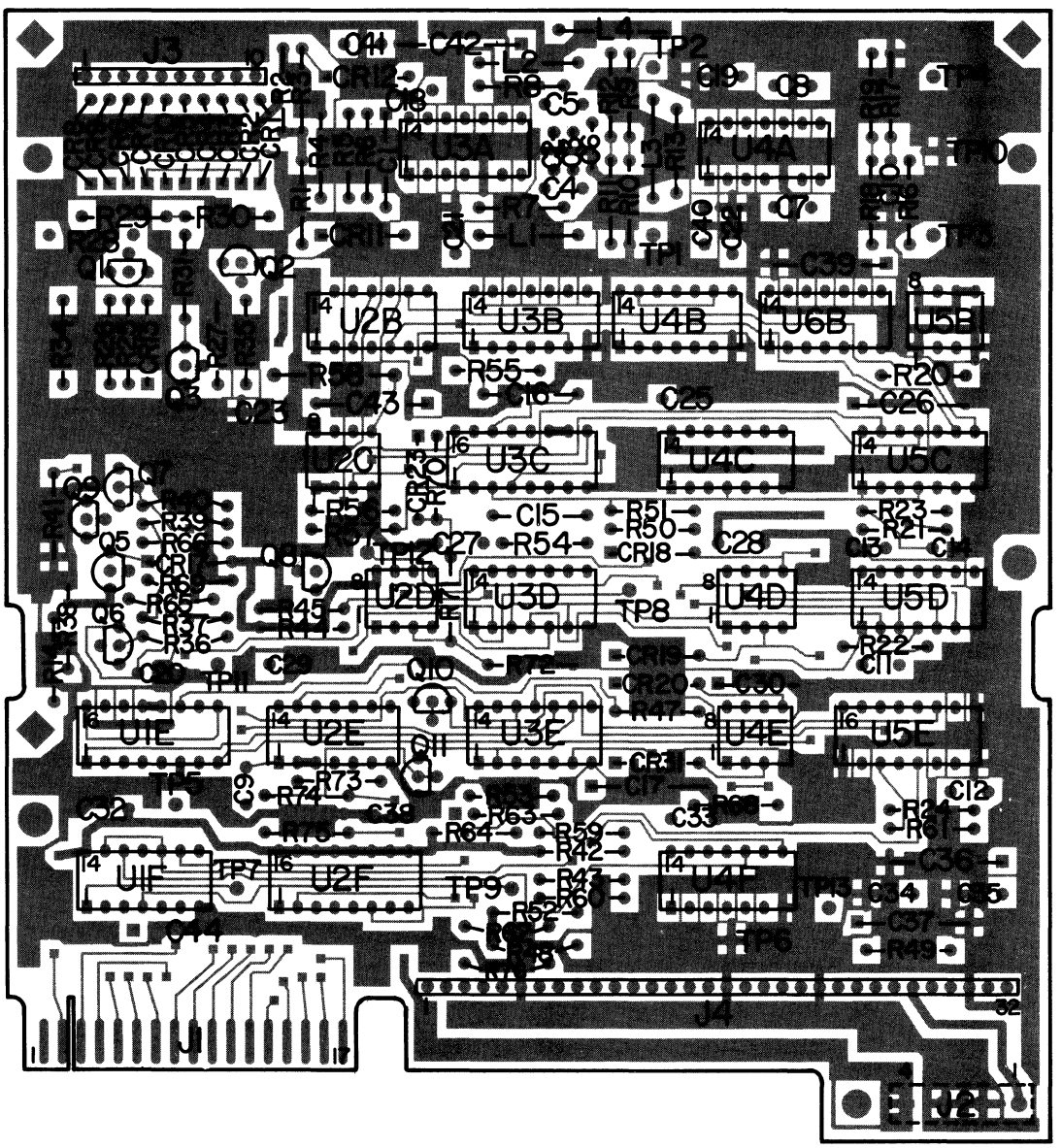


Figure 8-21. Component Locator for Service Sheet 2

NOTES:
1. COMPONENT NOT ON TANDON BOARD.
2. COMPONENTS ON TANDON BOARD ONLY.
3. R31 IS 768Ω ON TANDON BOARD.

Figure 8-22.
Drive Electronics Service Sheet 2
8-65 AP

8-144. LOGIC CONVENTION.

8-145. The positive logic convention is used for logic variables and the circuits comprising the 64110A flexible disc drive. positive logic difines a logic 1 as a more positive voltage (high) and a logic 0 as the more negative voltage (low). Ideally, the low and high voltage levels are 0V and +5V, respectively. Due to voltage drops over interconnecting PC board traces, etc., the actual levels may vary from these ideal values. Therefore, the voltage levels for a logic 1 and 0 are defined as follows:

TTL Voltage Levels

Binary Quantity	Voltage Limit
Input 0	< 0.8 V
Input 1	> 2.0 V
Output 0	< 0.4 V
Output 1	> 2.4 V

8-146. LOGIC SYMBOLOGY.

8-147. Table 8-4 gives a summary of the logic symbology used in this manual.

Table 8-17. Logic Symbology

GENERAL

All signals flow from left to right, relative to the symbol's orientation with inputs on the left side of the symbol, and outputs on the right side of the symbol (the symbol may be reversed if the dependency notation is a single term.)

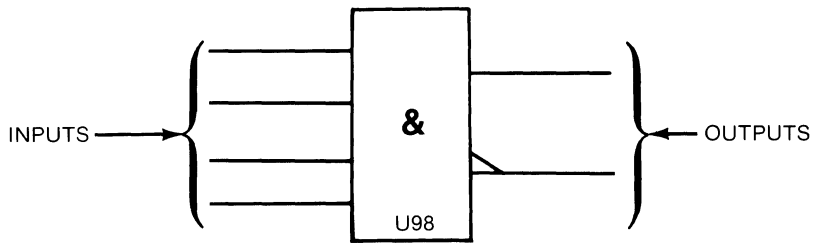
All dependency notation is read from left to right (relative to the symbol's orientation).

An external state is the state of an input or output outside the logic symbol.

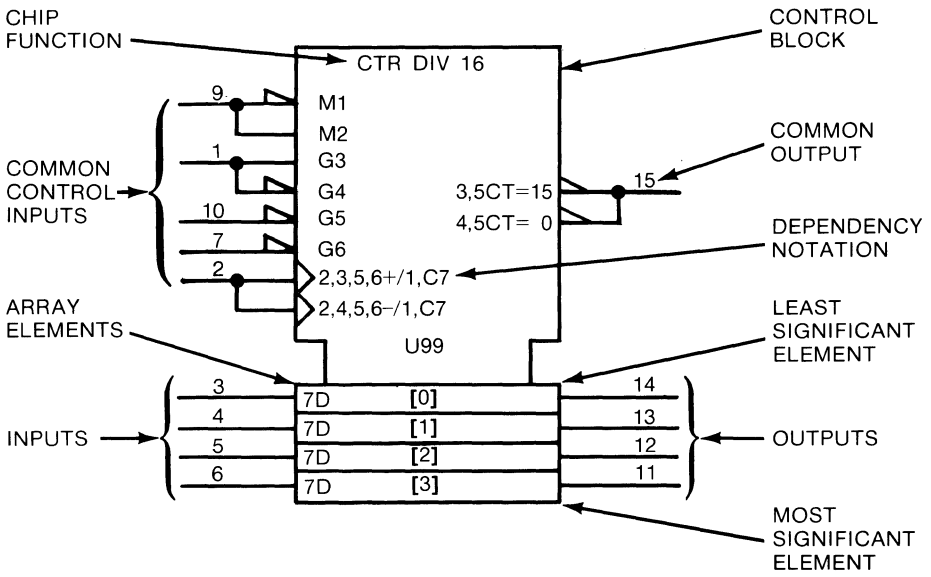
An internal state is the state of an input or output inside the logic symbol. All internal states are True = High.

SYMBOL CONSTRUCTION

Some symbols consist of an outline or combination of outlines together with one or more qualifying symbols, and the representation of input and output lines.



Some have a common Control Block with an array of elements:



CONTROL BLOCK - All inputs and dependency notation affect the array elements directly. Common outputs are located in the control block. (Control blocks may be above or below the array elements.)

ARRAY ELEMENTS -All array elements are controlled by the control block as a function of the dependency notation. Any array element is independent of all other array elements. Unless indicated, the least significant element is always closest to the control block. The array elements are arranged by binary weight. The weights are indicated by powers of 2 (shown in **[ ]**).

LS-09-81 - 1

Table 8-17. Logic Symbology

INPUTS - Inputs are located on the left side of the symbol and are affected by their dependency notation.

Common control inputs are located in the control block and control the inputs/outputs to the array elements according to the dependency notation.

Inputs to the array elements are located with the corresponding array element with the least significant element closest to the control block.

OUTPUTS - Outputs are located on the right side of the symbol and are effected by their dependency notation.

Common control outputs are located in the control block.

Outputs of array elements are located in the corresponding array element with the least significant bit closest to the control block.

CHIP FUNCTION - The labels for chip functions are defined, i.e., CTR - counter, MUX - multiplexer.

DEPENDENCY NOTATION

Dependency notation is always read from left to right relative to the symbol's orientation.

Dependency notation indicates the relationship between inputs, outputs, or inputs and outputs. Signals having a common relationship will have a common number, i.e., C7 and 7D....C7 controls D. Dependency notation 2,3,5,6+/1,C7 is read as when 2 and 3 and 5 and 6 are true, the input will cause the counter to increment by one count....or (/) the input (C7) will control the loading of the input value (7D) into the D flip-flops.

The following types of dependencies are defined:

a. AND (G), OR (V), and Negate (N) denote Boolean relationship between inputs and outputs in any combination.

b. Interconnection (Z) indicates connections inside the symbol.

c. Control (C) identifies a timing input or a clock input of a sequential element and indicates which inputs are controlled by it.

d. Set (S) and Reset (R) specify the internal logic states (outputs) of an RS bistable element when the R or S input stands at its internal 1 state.

e. Enable (EN) identifies an enable input and indicates which inputs and outputs are controlled by it (which outputs can be in their high impedance state).

f. Mode (M) identifies an input that selects the mode of operation of an element and indicates the inputs and outputs depending on that mode.

g. Address (A) identifies the address inputs.

h. Transmission (X) identifies bi-directional inputs and outputs that are connected together when the transmission input is true.

DEPENDENCY NOTATION SYMBOLS

A	Address (selects inputs/outputs) (indicates binary range)	N	Negate (compliments state)
C	Control (permits action)	R	Reset Input
EN	Enable (permits action)	S	Set Input
G	AND (permits action)	V	OR (permits action)
M	Mode (selects action)	Z	Interconnection
		X	Transmission

LS-09-81 - 2

Table 8-17. Logic Symbology

OTHER SYMBOLS

∩ Analog Signal	◺◿ Inversion	→ Shift Right (or up)
& AND	O Negation	/ Solidus (allows an input or output to have more than one function)
} { Bit Grouping	—✕— Nonlogic Input/Output	▽ Tri-State
▷ Buffer	◇ Open Circuit (NPN) (external resistor)	, Causes notation and symbols to effect inputs/outputs in an AND relationship, and to occur in the order read from left to right.
! Compare	◇ Open Circuit (PNP) (external resistor)	( ) Used for factoring terms using algebraic techniques.
▷ Dynamic	≥1 OR	[ ] Information not defined.
=1 Exclusive OR	◇ Passive Pull Down (internal resistor)	Φ Logic symbol not defined due to complexity.
⊓ Hysteresis	◇ Passive Pull Up (internal resistor)	
? Interrogation	⌐ Postponed	
— Internal Connection	← Shift Left (or down)	

LABELS

BG	Borrow Generate	CO	Carry Output	J	J Input
BI	Borrow Input	CP	Carry Propagate	K	K Input
BO	Borrow Output	CT	Content	P	Operand
BP	Borrow Propagate	D	Data Input	T	Transition
CG	Carry Generate	E	Extension (input or output)	+	Count Up
CI	Carry Input	F	Function	–	Count Down

MATH FUNCTIONS

Σ	Adder	>	Greater Than
ALU	Arithmetic Logic Unit	<	Less Than
COMP	Comparator	CPG	Look Ahead Carry Generator
DIV	Divide By	π	Multiplier
=	Equal To	P-Q	Subtractor

CHIP FUNCTIONS

BCD	Binary Coded Decimal	DIR	Directional	RAM	Random Access Memory
BIN	Binary	DMUX	Demultiplexer	RCVR	Line Receiver
BUF	Buffer	FF	Flip-Flop	ROM	Read Only Memory
CTR	Counter	MUX	Multiplexer	SEG	Segment
DEC	Decimal	OCT	Octal	SRG	Shift Register

DELAY and MULTIVIBRATORS

⊓⊓⊓	Astable
100 ns	Delay
1⊓	Nonretriggerable Monostable
NV	Nonvolatile
⊓⊓⊔	Retriggerable Monostable

LS-09-81 - 3

8-148. MNEMONICS.

8-149. Signals in the 64110A flexible disc drive have been assigned mnemonics that describe the active state and function of the signal (see table 8-17). A prefix letter (H, L, P, or N) is used to indicate the active state of the signal and the remaining letters indicate its function A "H" prefix indicates that the function is active in the "high" state; a "L" prefix indicates that the function is active in the "low" state; a "P" prefix indicates the clock signal is active on the positive edge of the clock; a "N" indicates the clock is active on the negative edge of the clock. Table 8-18 is a listing of the mnemonics used on the service sheets.

Table 8-18. Mnemonics

MNEMONIC	DESCRIPTION
DS0-3	Drive Select 0 through 3. When low, the drive is selected and will respond to step or read/write commands. This system uses DS0 only.
HA 0-1	High Address inputs 0-1. These inputs in conjunction with the chip select and write inputs select between the status register, track register, sector register, data register and command registers internal to the mini disc controller chip.
HBYTE 3	High Byte 3. When true,this signal indicates that three consecutive bytes of zeros or ones have been received from the disc.
HBYTE 7	High Byte 7. When true, this signal indicates that seven consecutive bytes of zeros or ones have been received from the floppy disc read electronics.
HDATA1US	High Data 1 microsecond. This signal pulses true for 1 microsecond whenever a flux transition is detected from the disc drive.
HDIRC	High Direction. When high the heads are stepped out (away from center) and when low the heads are stepped in with each step pulse.
HDMAEN	High DMA Enable. This signal is set true by the CPU when it is ready for a DMA operation. This signal is set to the false state when the DMA operation is completed.
HDMARQ	High DMA Request. Signal from CPU Interface/DMA state machine that indicates that the mini disc controller chip is requesting a DMA cycle.

HDRQ	High Data Request. When high indicates that the mini disc controller's data register is full if a read operation is occurring, or empty during a write operation. This line cleared when the CPU does a read or write to the data register.
HINHIBIT	High Inhibit. Signal in data separator circuitry which halts the VCO during a sinkup cycle. When this signal goes to the false state, the VCO is again started in phase with incoming data.
HMDCRQ	High Mini Disc Controller Request. HINTRQ a signal from mini disc controller chip which, when true, indicates that the mini disc controller chip wishes to interrupt the CPU operation.
HR5,6	High Register 5,6. When in the true state indicates that the CPU is communicating with the mini disc controller via either register 5 or register 6 internal to the CPU. The state of the registers is determined by LIC1 and LIC2.
HRCLK	High Read Clock. Clock signal from data separator circuitry which is in phase with the LRAWRD signal.
HRG	High Read Gate. Signal from the mini disc controller chip which indicates to the data separator circuitry that a field of zeros or ones has been encountered. When true, it does not allow data separator to re-syncronize.
HSA D0-7	High Signiture Analysis Data 0-7. These signals are the outputs of the SA stimulus latch. The lower byte of the LIOD (0-7) bus is used by the CPU to make the interface and data separator circuitry synchronous with the CPU.
HVCOE	High Voltage Control Oscillator Enable. Compliment of LVCOE.
H2MHZC	High 2 MHz Clock. The inverted 2 MHz clock used to clock data from the output of the state machine.
LA0-2	Low Address 0-2. Signals from CPU which are used to select the address of mini disc controller chip or other registers in which read and write operations are to occur.
LBEN	Low Buffer Enable. When low, this signal enables the drive status buffers and also resets the processor request flip-flop.

LCS	Low Chip Select. Input to the mini disc controller chip which enables the CPU interface portion of the mini disc controller chip.
LCRMC0,1	Low Clear Media Change 0,1. Low true signals which clear there respective media change flip-flops. These signals are controlled by the CPU.
LDAL 0-7	Low Data Access Lines 0-7 Bidirectional lines that carry data and commands to and from the mini disc controller chip, drive status register, etc.
LDMAAK	Low DMA Acknowledge. Signal to the CPU interface state machine which indicates that the DMA request from the mini disc controller has been acknowledged.
LDMAEN	Low DMA Enable. Compliment of HDMAEN.
LDMAI	Low Direct Memory Access Interrupt. An interrupt to the CPU when the MDC is requesting DMA and LDMAEN is not true.
LDMAR	Low Direct Memory Access Request. When low, indicates to the CPU that the MDC wants direct access to memory.
LDOUT	Low Data Out. Signal from CPU which indicates read or write operation on the I/O bus (Low=Write). This is valid when LIOSB is low.
LDRQ	Low Data Request. Compliment of HDRQ.
LIC1-2	Low Interface Control 1 and 2. These lines can provide up to four states used to control peripheral devices. How these lines are controlled is determined by software.
LINT	Low Interrupt. The microprocessor pulls this line low to poll the Input/Output Bus to determine which peripheral device requested the interrupt.
LIOD0-15	Low Input/Output Data 0 through 15. The LIOD bus is a bi-directional bus. The CPU uses this bus to communicate with I/O ports. Information is true low, and is used in conjunction with LPAB0-3.

LIOSB	Low Input/Output Strobe. When this signal goes from low to high, the data on the I/O bus is valid.
LIR3	Low Interrupt Request 3. Interrupt request from mini controller board to the interrupt circuitry on the I/O board that the mini controller is in need of service by the CPU.
LLL	Low Latch Least. Signal from CPU interface state machine which latches the least significant byte of data during a CPU read cycle.
LLM	Low Latch Most. Signal from CPU interface state machine which latches the most significant byte of data during a CPU read cycle.
LMDCI	Low Mini Disc Controller Chip Interrupt. Flags signal to CPU that indicates that the mini disc controller chip is currently requesting an interrupt.
LMCIR	Low Media Change Interrupt Request. Interrupt signal from media change flip-flops indicating that media has been changed on the disc.
LMDCHG0,1	Low Media Change 0,1. When low, the corresponding signal indicates that the media has been changed on the appropriate disc.
LMR	Low Master Reset. Input to the mini disc controller chip, when true, resets internal status registers.
LMDCRQ	Low Mini Disc Controller Request. Compliment of HMDCRQ.
LMYPA	Low My Peripheral Address. Goes low when the CPU is communicating with the mini drive circuitry. This signal is formed when Peripheral Address 4 is accessed by the CPU. Also, LMYPA is used as the clock during SA.
LNTRDY0,1	Low Not Ready 0,1 When true, these signals indicate that the corresponding disc drive is not ready. i.e. index pulses have dropped below a specified rate.
LOEL	Low Output Enable Lower. When true, this signal enables the least significant 8 bits of data to appear on the disc interface bus during a microprocessor write cycle.

LOEM	Low Output Enable Most. When true, this signal enables the 8 most significant bits to the disc interface bus during a microprocessor write cycle.
LPOP	Low Power On Pulse. This signal pulses low when power is cycled. When pulsed low, it will initialize and reset the CPU and mini drive control circuitry.
LPOPB	Low Power On Pulse Buffered. When low, resets drive and interface control latches.
LPA0-3	Low Peripheral Address 0 through 3. Identifies which one of the 16 peripheral devices will be involved in a I/O operation.
LPRQ	Low Processor Request. When true, this signal indicates that the CPU is requesting a cycle from the the CPU interface/DMA state machine.
LRAWRD	Low Raw Read. Read data from data separator circuitry which has a specific phase relationship to HRCLK.
LR7	Low Register 7. When true, this signal indicates that the CPU is communicating on the I/O bus through register 7.
LRDDATA	Low Read Data. When true, indicates to the data separation circuitry that a flux transition has occurred on the disc.
LRD	Low Read. When true, this signal indicates that the microprocessor is executing a read cycle from the mini disc control circuitry through the data latches.
LRST	Low Reset. Signal from microprocessor when true, resets the mini disc controller circuits.
LRSTINT	Low Reset Interrupt. Signal from the microprocessor. When true, it resets the mini disc controller chip interrupts and DMA interrupt request flip-flops.
LVCO	Low Voltage Control Oscillator. Low true output of VCO oscillator.
LVCOE	Low Voltage Control Oscillator Enable. Signal from mini disc controller chip which is made true when the mini disc controller is inspecting data coming from the disc. When true, enables data separator

circuitry.

LWE — Low Write Enable.
Signal to mini disc controller chip which enables write circuitry with in conjunction with LCS.

LWRT — Low Write.
When true, corresponding signal indicates that the CPU is executing a write to the mini disc circuitry through the data latches.

LWRTSM — Low Write State Machine.
Signal from microprocessor which indicates whether a read or write operation should be executed during the next CPU/DMA state machine interface cycle.

LWPRT0,1 — Low Write Protect 0,1.
When true, corresponding signal indicates that the disc installed in the disc drive is write protected. See Write Protect. Also, used to set corresponding media change flip-flop.

LRE — Low Read Enable.
Input to mini disc controller chip which enables read circuitry in conjunction with LCS.

L2MHz — Low 2 MHz.
2 MHz signal derived from the 4 MHz oscillator circuit.

L2MHZC — Low 2 MHz Clock.
Used to clock data to the input of the state machine.

L500KHz — Low 500 KHz.
A 500 KHz signal derived from the 4MHz oscillator circuit. This signal is used by the PLL to sync the VCO when not inspecting data from the disc.

PCMD — Positive Command.
Control signal from the CPU which pulses low during a write to the mini disc through register 5. The positive edge of this signal latches data into the interface control latch and the DMA enable latch and sets the processor request latch.

VCODATA — Voltage Controlled Oscillator Data.
This signal is compared with VCOOSC in the phase comparator circuitry.

VCOOSC — Voltage Control Oscillator.
This signal is compared with VCODATA in phase comparator circuit.

HIGH DECREASE FVCO	Signal from phase detector when true decreases the frequency of the voltage control oscillator.
LOW INCREASE FVCO	When in the true state, this signal changes the voltage to the voltage control oscillator in such a way as to increase its frequency.
INDEX	An index pulse occurs once every revolution of the disc (200 msec. nominal) to indicate the beginning of a track.
MOTOR ON	A low logic level on this line causes the drive motor to accelerate and stabilize in less than 250 msec. When this line goes high, the drive motor decelerates to a stop.
SIDE ONE SELECT	A high logic level selects the side "0" read/write head and a low logic level selects the side "1" read/write head.
STEP	Pulses low to step the head in or out. Direction is Direction is controlled by HDIRC.
TRACK0	This line indicates to the controller that the read/write head is positioned on track 0. The track 0 signal remains low until the head is moved from track 0. This is accomplished by anding the track 0 switch and phase 0 of the stepper motor control.
WRITE DATA	When the disc drive is selected, this line provides the bit serial composite write data pulses that control the switching of the write current in the selected head. The write electronics must be enabled by the write gate line.
WRITE GATE	When this line is low, the write electronics are enabled for writing data (read electronics are disabled). This line enables write current to flow in the selected read/write head.
WRITE PROTECT	This line goes low when the disc is write protected to disable the write electronics.

64110-90901 Printed in USA